A 60 pW g_mC Continuous Wavelet Transform circuit for portable EEG systems

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Abstract

This paper presents a low power, low voltage and low frequency bandpass filter implementation of a Continuous Wavelet Transform (CWT) for use with physiological signals in the Electroencephalogram (EEG) range (1–150 μV, 1–70 Hz bandwidth). Experimental results are presented for a 1 V, 7th order g_mC filter based CWT with filter centre frequencies ranging from 1–64 Hz.

Low power and low frequency operation is achieved by biasing the transconductor transistors at low current levels in the deep weak inversion region. The resulting increased mismatch and reduced bandwidth are compensated for at the topology level. The filter has a 43 dB dynamic range and a 60 pW power consumption. This power consumption is three orders of magnitude lower than existing CWT implementations and assessed via a suitable figure of merit the performance is better than all considered bandpass filters. The improvement in the state-of-the-art originates from the close integration of the application requirements, CWT theory, bandpass filter design theory, and low transconductance transconductor design. These topics are described in detail.

I. Introduction

Low power consumption is a crucial parameter in all modern electronic design. In particular, for portable and wearable electronics extreme miniaturisation is required and this limits the available battery size and power draw. Wearable Electroencephalography (EEG) is an example of such a power limited system [1]. The EEG records the voltage between electrodes placed on the scalp, typically in the range 1–150 μV peak-to-peak over a 1–70 Hz bandwidth, and provides a non-invasive interface to the brain. Discrete, lightweight and comfortable devices are essential for user acceptance in applications ranging from epilepsy diagnosis to brain-computer

interfaces [1]. To this end, a series of low power integrated EEG front-end amplifiers have been reported [2]–[4], as have low power integrated transceivers for bio-telemetry applications [5], [6]. However, it is agreed that further decreases in the average system power consumption can be achieved via the inclusion of online signal processing, or *intelligence*, in the portable EEG device itself [1], [4]: by providing real-time data reduction the utilisation of the relatively high power transceiver can be decreased. Provided that the signal processing uses very little power, the power saved from the transceiver leads to a reduction in the overall system power consumption.

The Continuous Wavelet Transform (CWT) is a well known signal processing technique and is potentially very suitable for use within this low power aim. The CWT of a signal $f(t)$ is

$$W(a,b) = \frac{1}{\sqrt{a}} \int_{-\infty}^{\infty} f(t)\psi^*\left(\frac{t-b}{a}\right) dt \tag{1}$$

where $\psi(t)$ is the *mother wavelet*, a is the dimensionless analysis *scale* and b is the time at which the transform is taken. At each analysis scale (1) corresponds to the convolution of $f(t)$ with an impulse response

$$h(t) = \frac{1}{\sqrt{a}}\psi\left(\frac{-t}{a}\right). \tag{2}$$

Given the properties of the CWT it is found that $h(t)$ corresponds to a bandpass filter structure [7], [8]: the mother wavelet determines the shape of the bandpass filter, and the centre frequency is set by the analysis scale. A low power CWT can thus be provided by a low power bandpass filter with impulse response $h(t)$.

This paper reports experimental results for an on-chip implementation of a Mexican hat-like mother wavelet CWT, named the Low Power CWT (LPCWT) as it is suitable for very low power use. The LPCWT is implemented as a g_mC bandpass filter optimised for low voltage and low power operation with physiological signals. Inherently low power and low frequency operation is achieved by the use of very low currents and transistors operating in the deep weak inversion region. Ordinarily the use of this operating region is avoided due to noise and bandwidth issues and decreased current matching. We present techniques for addressing these issues, making high order system design feasible. The net result is a seven pole, two zero, 2 Hz centre frequency g_mC filter implemented in a 0.35 μm CMOS process. The power consumption is 60 pW with a 43 dB dynamic range. This power consumption is nearly three orders of magnitude below the nearest previous CWT implementation using any mother wavelet. The improvement in the

state-of-the-art performance originates from the close integration of the application requirements, CWT theory, bandpass filter design theory, and low transconductance transconductor design. All of these topics are considered in detail. The end filter then compliments the work of [2]–[7], [9], moving towards having a full EEG system, with node intelligence, integrated on-chip.

The remainder of this paper is organised as follows. Section II presents the LPCWT mother wavelet, the g_mC filter topology, and its associated properties. The utilised transconductor and deep weak inversion region design issues are then considered in Section III. Section IV presents the measured filter performance which is discussed and compared to previous work in Section V.

II. LPCWT WAVELET FILTER TOPOLOGY

A. Transfer function

The LPCWT mother wavelet function was proposed in [7] and has the transfer function

$$H(s) = \frac{-\pi^{1/4}\sqrt{\frac{8}{3}a^5}s^2}{1 + sT + \left(\frac{T^2}{2} - \frac{a^2}{2}\right)s^2 + \left(\frac{T^3}{6} - \frac{Ta^2}{2}\right)s^3 + \cdots} \tag{3}$$

where the denominator is a truncated Maclaurin expansion of the term $e^{sT-a^2s^2/2}$ and T is a delay (in seconds) introduced to ensure that $H(s)$ is open loop stable. The LPCWT wavelet has the impulse response shown in Fig. 1, and was designed so that this impulse response resembles the Mexican hat mother wavelet (the second derivative of a Gaussian function), defined as

$$\psi(t) = \frac{2}{\pi^{1/4}\sqrt{3a}}\left(1 - \frac{t^2}{a^2}\right)e^{-t^2/2a^2} \tag{4}$$

with the transfer function:

$$\Phi(s) = \frac{-\pi^{1/4}\sqrt{\frac{8}{3}a^5}s^2}{e^{-a^2s^2/2}}. \tag{5}$$

$\Phi(s)$ has a low Q factor of 1.2 making the Mexican hat CWT very suitable for on-chip implementation. However, the presence of the exponential term in the denominator of (5) means that the Mexican hat wavelet cannot be implemented as a finite order, stable, analogue filter. [7] presented an approximation procedure, developing the LPCWT wavelet. The LPCWT is a wavelet in its own right, but one which resembles the Mexican hat.

Given (3), application realistic testing is then essential to asses the performance of the LPCWT, to determine the order of the filter required, and the performance compared to the ideal Mexican

hat. Our intended application is the real-time analysis of EEG signals in a portable monitor [9]. The aim is to use CWT coefficients to automatically detect epileptic spike features, which are of use for epilepsy diagnosis. By only storing or transmitting these spike features and ignoring background sections of data, data reduction can be achieved [1], [9]. [7] demonstrated that 3rd and 5th order LPCWT wavelets are not suitable for use within this aim as they lead to a noticeable degradation in performance compared to the Mexican hat wavelet. However, the 7th order LPCWT achieves comparable performance in this realistic usage situation and so is suitable for use [7]. Hence for use in the EEG data reduction algorithm of [9], the values $a = 0.1$ and $T = 0.4$ s are used here. These give a low, 2.1 Hz, centre frequency filter to be implemented and the numerical value of this LPCWT transfer function is

$$H(s) = \frac{-6.88 \times 10^{-3} s^2}{\begin{array}{l} 2.34 \times 10^{-8} s^7 + 1.34 \times 10^{-6} s^6 + 3.70 \times 10^{-5} s^5 + 6.79 \times 10^{-4} s^4 \\ +8.67 \times 10^{-3} s^3 + 0.075 s^2 + 0.40 s + 1 \end{array}}. \quad (6)$$

B. $g_m C$ filter topology

A key advantage of the LPCWT over previous analogue CWT methods is that it results in a transfer function which has a strictly Hurwitz denominator and a purely even numerator. As a result a doubly terminated LC ladder topology is possible, and a prototype network is illustrated in Fig. 2(a). Doubly terminated LC ladders have a minimal sensitivity to inexact component values [10], [11] and so an intrinsically robust CWT implementation can be achieved. This is additionally important for very low power, low voltage applications where the use of transistors biased in the weak inversion operating region is unavoidable. This operating region is associated with decreased matching of currents in current mirrors (see Section III-A), but the LC ladder topology helps overcome this limitation, facilitating low power operation.

For on-chip implementation a $g_m C$ filter simulation of the LC ladder prototype is shown in Fig. 2(b). From Fig. 2(b) C_2 is the smallest capacitor present and if capacitor values are expressed as ratios y to this (i.e. $y_x = C_x/C_2$) the implemented transfer function is

$$H(s) = \frac{ax^2}{bx^7 + cx^6 + dx^5 + ex^4 + fx^3 + gx^2 + hx + 1} \quad (7)$$

where

$$a = 2y_{L1} \tag{8}$$

$$b = y_1 y_3 y_4 y_{L1} y_{L2} y_{L3} \tag{9}$$

$$c = y_3 y_4 y_{L1} y_{L2} y_{L3} + y_1 y_3 y_{L1} y_{L2} y_{L3} \tag{10}$$

$$d = y_3 y_{L1} y_{L2} y_{L3} + y_3 y_4 y_{L2} y_{L3} + y_1 y_4 y_{L1} y_{L3} + y_1 y_4 y_{L1} y_{L2} + y_1 y_3 y_4 y_{L1} y_{L3} + y_1 y_3 y_{L1} y_{L2} + y_3 y_4 y_{L1} y_{L3} \tag{11}$$

$$e = y_1 y_{L1} y_{L3} + y_{L1} y_4 y_{L3} + y_1 y_3 y_{L1} y_{L3} + y_3 y_{L1} y_{L3} + y_{L1} y_3 y_4 y_{L3} + y_3 y_{L2} y_{L3} + y_3 y_{L1} y_{L2} + y_1 y_{L1} y_{L2} + y_4 y_{L1} y_{L2} \tag{12}$$

$$f = y_4 y_{L2} + y_3 y_{L2} + y_{L1} y_{L2} + y_3 y_{L1} + y_1 y_{L1} + y_3 y_{L1} y_{L3} + y_{L1} y_{L3} + y_1 y_3 y_{L1} + y_4 y_{L1} + y_3 y_4 y_{L3} + y_1 y_4 y_{L1} + y_4 y_{L3} \tag{13}$$

$$g = 2y_{L1} + y_{L2} + y_4 y_{L1} + y_1 y_{L1} + y_3 y_{L3} + y_3 y_{L1} + y_{L3} \tag{14}$$

$$h = y_3 + y_{L1} + y_4 + 1 \tag{15}$$

$$x = \frac{sC_2}{g_m}. \tag{16}$$

x is thus a modified complex frequency variable indicating that only g_m and C_2 affect the centre frequency of the filter. For layout C_2 can thus be used as the unit capacitance and all others matched to this. Capacitor ratios y can be well matched, giving the wanted filter shape while the filter centre frequency can be tuned by changing the transconductance. This arrangement is also beneficial as C_2 is the only floating capacitor in the design. All other capacitors are connected between a transconductor input and ground and so can be pre-distorted to correct for the transconductor parasitic capacitances, helping to give the correct filter shape.

Note that, as with all LC ladder based implementations of arbitrary transfer functions, it is not possible to ensure that the correct centre frequency gain is realised. This can be compensated for by the presence of an ideal transformer, amplifier, or simply compensating for the expected values in the next part of the circuit. For the case here, the $g_m C$ filter of Fig. 2(b) has -1.3511 V/V extra gain compared to the LPCWT transfer function (6), and this is corrected for in the results graphs below. Furthermore, as will be seen in Section III-B, pre-distortion of C_2 results in the gain factor being modified to -1.76 V/V.

C. g_mC filter performance

For the low power, low voltage and low frequency applications intended for the LPCWT, noise is a significant design parameter limiting the dynamic range. If the noise of the k^{th} transconductor in Fig. 2(b) is modelled as a voltage source, $V_k(j\omega)$, in series with the transconductor negative input terminal, nine transfer functions can be defined from each noise source to the output node:

$$H_k(j\omega) = \frac{V_{out}(j\omega)}{V_k(j\omega)}. \tag{17}$$

If all of the transconductors are the same, and $V_k(j\omega)$ has power spectral density $S(\omega)$, the filter input referred noise is then given by

$$S_i(\omega) = S(\omega) \sum_k \left| \frac{H_k(j\omega)}{H(j\omega)} \right|^2 \tag{18}$$

and the *noise transfer function* can be defined as

$$N(\omega) = \frac{S_i(\omega)}{S(\omega)} = \sum_k \left| \frac{H_k(j\omega)}{H(j\omega)} \right|^2 \tag{19}$$

$$\begin{aligned} = {} & \frac{1}{2} + 4.4 \times 10^3 \left| \frac{1}{x} \right|^2 + 4.4 \times 10^{-3} \left| 17.2 + \frac{7.6}{x} + \frac{1}{x^2} \right|^2 \\ & + 4.4 \times 10^{-3} \left| 9.6x^2 + 7.6 + \frac{1}{x} \right|^2 \\ & + 8.7 \times 10^{-3} \left| 101.3x^2 + 79.5x + 27.7 + \frac{7.6}{x} + \frac{1}{x^2} \right|^2 \\ & + 4.4 \times 10^{-3} \left| 606.7x^3 + 475.8x^2 + 175.6x + 52.9 + \frac{7.0}{x} \right|^2 \\ & + 4.4 \times 10^{-3} \left| 2566.0x^4 + 2012.3x^3 + 844x^2 + 303.0x + 57.3 + \frac{7.6}{x} \right|^2 . \end{aligned} \tag{20}$$

Importantly (20) is only a function of x, the modified frequency variable. As a result only the centre frequency of the filter affects the input referred noise. No further optimisations at the filter topology level are possible.

III. Deep weak inversion implementation of the LPCWT

For low frequency operation, keeping the required filter capacitances at values realistic for on-chip implementation, a transconductance of 100 pS is required. With a low, 1 V, V_{DD} on-chip

signals are of the order of milli-Volts, and transconductances of 100 pS inevitably imply that currents of the order of pico-Amps are present. Given that these currents are present anyway, the circuit proposed here makes use of similarly low currents for the fundamental transconductor operation. This intrinsically provides the low frequency and low power operation required, without the need for complex transconductor topologies.

The simplest differential input transconductor is the NMOS differential pair as shown in Fig. 3. The transconductance when all transistors are operating in weak inversion is given by

$$g_m = \frac{I_{bias}}{2nU_t} \tag{21}$$

where all symbols have their standard meanings. For the used process, n is approximately 1.3. Thus if I_{bias} is 6.5 pA the required 100 pS transconductance is realised utilising no special circuit techniques, keeping the potential complexity, noise and mismatch low. Nine identical transconductors from Fig. 3 are used in the LPCWT filter, all sharing the same M6 bias transistor.

The specific current, I_S from the EKV model of weak inversion transistor operation [12], is approximately 230 nA for a square NMOS transistor in the used 0.35 μm process. At $I_{DS} = 6.5$ pA the transistor inversion factor ($i_f = I_{DS}/I_S$) is thus 3×10^{-5} and all transistors are operating in the deep weak inversion region. Some important design issues specific to this operating region are thus now addressed and overcome.

A. Deep weak inversion circuit design techniques

1) Biasing: Fig. 4(a) shows a replication of the transistor characterisation work from [13]: the $I_{DS} - V_{GS}$ curve of an on-chip 1 μm by 1 μm NMOS transistor is plotted. The ability to measure and process pico-Amp on-chip currents is clearly demonstrated; on-chip current processing is not limited by leakage currents until femto-Amp levels. [13] used negative V_{GS} values to provide very low currents in a current mode, first order, log domain, low pass filter. Numerous published implementations have since used pico-Amp scale currents in parts of the design, but not to implement the full circuit functionality.

However, apparent from Fig. 4(a) is that at pico-Amp currents the leakage current in the bondpads becomes significant. This is seen as the *levelling off* of the measured results compared to the simulated ones, and can prevent external current biasing of deep weak inversion circuits. If significant, the Fig. 3 transconductor can be voltage biased: the fixed $I_{DS} - V_{GS}$ relationship

of bias transistor M6 can be used to ensure that the transconductor has the correct bias current even if extra current is drawn from the external current source as bondpad leakage current.

2) Linearity: The linearity of a differential pair based transconductor was derived in [14] in terms of i_f. If Γ represents the maximum allowable difference between the ideal linear and actual non-linear transconductor output current, the linear range can be found as [14]

$$V_{lin} = 1.5nU_t\sqrt{\Gamma(1+i_f)}. \tag{22}$$

The presence of the inversion factor demonstrates the significant loss in input range between strong and weak inversion operation. In the weak inversion region, however, little decrease is present as deeper weak inversion is used. If $\Gamma = 0.05$ (5%), for standard weak inversion $i_f = 0.1$ and $V_{lin} = 11.4$ mV. For deep weak inversion as $i_f \to 0$, $V_{lin} \to 10.9$ mV. Utilising deep weak inversion thus reduces the linear range by only 0.5 mV. Compared to the standard weak inversion design case, deep weak inversion is no more challenging.

3) Noise: The wanted bandpass filter has a 2.1 Hz centre frequency and such low frequency operation is ordinarily associated with large amounts of flicker noise. However, the flicker noise corner frequency is given by [15]

$$f < \frac{KI_{DS}}{2qWL}. \tag{23}$$

where f is frequency, K is a process and transistor dependent parameter and all other symbols have their standard meanings. For transistors biased at pico-Amps I_{DS} is so low that thermal noise still dominates at 2 Hz. Simulations of the end filter indicate that the largest in-band flicker noise component is only 0.01% of the total noise. As a result NMOS transistors can be used for the input stage of the transconductor without significantly affecting the low frequency noise produced. Ordinarily PMOS inputs may have been preferred due to their lower flicker noise coefficient, but in this case it makes no practical difference. The lower NMOS threshold voltage then simplifies operation from a low, 1 V supply.

4) Matching: The current matching of supposedly identical transistors is much worse when they are operating in the weak inversion region compared to the strong inversion region [16]. Fig. 4(b) illustrates this for the 0.35 μm process used here using simulated results showing the relative current mismatch from 100 Monte-Carlo runs with different average drain currents and transistor widths. Decreased matching at low currents, and the size dependence of the matching,

is clearly seen. Also seen, however, is a *levelling off* of the mismatch at very low currents. Between weak inversion operation and deep weak inversion operation there is no significant decrease in matching. The challenge of designing robust deep weak inversion circuits is again no more than that of standard weak inversion design.

B. Transistor sizing and capacitor pre-distortion

As noted previously, leakage currents are generally of the order of femto-Amps and are not found to present a major limitation for a 6.5 pA bias current. Instead, transistor sizing is a direct trade-off between mismatch and bandwidth. Larger devices have improved matching at the cost of increased parasitic capacitances and reduced bandwidth. The bandwidth is also decreased at lower bias currents. Small signal analysis shows that the low frequency frequency response of the transconductor is dominated by a single pole and zero [17]:

$$g_m \rightarrow \frac{g_m}{2} \cdot \frac{s + 2\omega_o}{s + \omega_o} \tag{24}$$

where ω_o is set by the bias current and the parasitic capacitances present. Using the transistor sizes in Fig. 3, ω_o is 37 Hz although the close proximity of the dominating pole and zero results in an increase of the 3 dB bandwidth to 52 Hz. Even this bandwidth, 1.4 decades above the filter centre frequency, introduces significant distortion into the in-band filter response, as shown in Fig. 5. This could be resolved by using smaller transistors, reducing the parasitic capacitors, and accepting the additional mismatch introduced. Alternatively here, larger transistors are used, and the distortion of the filter frequency response is overcome by pre-distorting the value of the floating capacitor C_2.

By substituting (24) into (7) it is possible to model the limited transconductor bandwidth and its effect on the filter transfer function. C_2 is then pre-distorted from the initial value of 2.48 pF to improve the match between the wanted and implemented responses. A value of $C_2 = 3$ pF is used here, significantly improving the filter shape compared to the non-pre-distortion case, as shown in Fig. 5. With this pre-distortion and a 6 pA bias current the LPCWT centre frequency is now 2 Hz, and experimental results in Section IV are presented for this 2 Hz case. The 2.1 Hz case can be achieved by re-tuning via the M6 bias condition if desired; all centre frequency tunings use the same pre-distorted C_2 value.

Finally, note that the C_2 pre-distortion also has an effect on the filter's centre frequency gain and the arbitrary gain factor between the wanted and implemented responses is corrected to -1.76 V/V to achieve the best possible agreement. For implementation, the grounded capacitors in the design are also pre-distorted from the values in Fig. 2(b), by approximately 750 fF per connected transconductor, compensating for the input capacitance of the transconductors.

IV. Experimental results

The LPCWT filter was fabricated in a 0.35 μm, single well, 2 poly, 3 metal CMOS process and a micrograph is given in Fig. 6. Detailed measurements are presented here for one chip selected at random from the supplied samples and assumed to be representative. No pre-selection to get the best or worst performance has been done. Nine other chips are tested for matching of the gain and group delay responses only. All measurements are PCB based and to drive the test equipment the output node of the filter is buffered.

A. Wavelet operation

Fig. 7(a) shows the measured Bode magnitude response and filter group delay for a 2 Hz centre frequency LPCWT filter using a 20 mV_{pp} input signal. The ideal LPCWT $H(s)$ function, (3), is also shown. To quantify inter-chip variations results from ten different chips from the same batch are present and in each case 100 repeat readings are averaged to remove the effects of noise in any one reading. All filters use a 6 pA bias current and the mean centre frequency found is 2 Hz, as desired, with a standard deviation of 0.04 Hz, 2% of the centre frequency value. The centre frequency gain tends to be below that of the schematic and extracted simulations, by approximately 0.93 dB, but this is within the range predicted by Monte-Carlo simulations.

Fig. 7(b) then shows the operation of a single chip at a range of centre frequency tunings. These centre frequencies are chosen as dyadic values over 1–64 Hz, covering the 70 Hz EEG bandwidth. Note that from (1) the gain of the CWT depends on the the analysis scale used. However, the g_mC LPCWT filter does not have this property, with all centre frequency tunings having the same gain. A factor of $\sqrt{f_c/2}$ where f_c is the filter centre frequency has been applied in Fig. 7(b) to allow the two cases to be directly compared. To tune the LPCWT filter only the bias value is changed, as detailed in Table I, where both current and voltage biasing schemes can be used. Differences between the simulated and measured values are explained by changes

in temperature between measurements and a measured 60 mV process variation in the threshold voltage. For each tuning of the mother wavelet $H(s)$, (3), both a and T are varied.

The measured impulse response, which shows the implemented LPCWT wavelet function, is shown in Fig. 8(a) for the 2 Hz centre frequency filter. For direct comparison with the wanted response the DC level at the filter output is removed and the area of the applied impulse corrected for. For presentation mains noise is also removed and the 0.93 dB gain difference observed in the Bode response is corrected for incorporating the negative sign from the -1.76 V/V gain factor. The correct LPCWT operation is clearly seen. Fig. 8(b) then shows 10 s of real EEG data processed by the LPCWT filter to demonstrate the filter operation on real input signals.

Finally, returning to Fig. 7(b), it can be seen that the measured group delay is approximately equal to T. This factor thus delays the filter output, and depending on the intended use of the transform this constant may want to be compensated for elsewhere. The overall group delay is not constant, but this is not a requirement for a valid CWT. Moreover, the variation in the group delay is much smaller than the impulse response duration from Fig. 8(a). The CWT is governed by a finite trade-off between the frequency resolution and the time resolution, with the frequency resolution being given approximately by the passband width of the bandpass filter and the time resolution by the duration of the impulse response. Thus any potential timing differences from the non-constant group delay are much smaller than the fundamental time resolution of the transform, and are consequently negligible.

B. Noise and input range

The measured input referred noise closely matches the simulated value and is 51 μVrms over a 1.5–2.5 Hz passband. As the LPCWT filter has a passband only 1 Hz wide the Total Harmonic Distortion (THD) is not a suitable measure of distortion as the harmonic components of a fundamental at the filter centre frequency necessarily fall outside the passband where they are attenuated and cannot be accurately measured. Nevertheless, measured using a 2 Hz, 20 $\mathrm{mV_{pp}}$ input signal the THD is 0.3%. Instead, the filter distortion is measured via the third order Intermodulation Distortion (IMD3). Sine waves at 2 and 2.1 Hz are applied so that the modulation products fall within the passband, although it is noted that this passband is not flat. Both input components have amplitude 5 mV and the end result taken from averaging over ten readings. Both the extracted simulation and measured result give the IMD3 as -20 dBc. Tolerating -20 dBc

of IMD3 the input linear range of the filter is thus 20 mV_{pp} giving a dynamic range of 42.8 dB. The Input Common Mode Range (ICMR) for correct filtering operation is found to be 0.4–0.6 V, with the nominal common mode being 0.5 V.

C. Power consumption and area

For a 2 Hz centre frequency filter the nominal bias current required is 6 pA. This corresponds to a filter power consumption of 60 pW which readily satisfies the low power requirement of the LPCWT. In reality, of course, this figure excludes the power consumption of the necessary current or voltage bias circuitry. The required bias is currently generated off-chip, and on-chip it must be robust to process variations and proportional to absolute temperature so it would not be unreasonable to expect the power consumption of this stage to be significant, likely dominating over the LPCWT power consumption. The implementation of such a bias block is beyond the scope of the LPCWT filter itself and so is not considered here in detail. [18] presented a 400 pA bias current block and combined with the current splitters proposed in [13] could be used to generate the required current.

For practical use however, it is noted that similar bias blocks will be required for the EEG front-end amplifier, ADC and other circuit blocks making up any complete system. It is thus not a lone requirement of the LPCWT stage, and the same block could be used to bias all of the stages in the system. More importantly, in comparison to the 25 μW per channel power consumption of a typical EEG front-end system [3], the 60 pW required by the LPCWT is insignificant. In terms of the power budget, the signal processing provided by the LPCWT is *free*: information about the signal can be obtained without any meaningful increase in the total system power consumption. An additional area of 0.216 mm^2 per analysis scale is required, but this too is essentially negligible compared to the volume required for the packaging, PCB, battery and other factors required to form a complete end system.

V. Discussion

Table II summarises the simulated and measured LPCWT performance and Table III compares this to the performance of other reported bandpass filters. Absolute performance is assessed through the power consumption while a relative comparison is provided by using the Figure of

Merit (FOM) from [19]:

$$\text{FOM} = \frac{P \cdot V_{DD}}{p \cdot f_c \cdot DR} \tag{25}$$

where P is the filter power consumption, p is the number of poles, and DR is the filter dynamic range. Lower FOM figures indicate better filter performance. Only filters with experimental results and sufficient details to derive the FOM are considered.

In Table III only [20], [21] report previous experimental CWT or Short-Time Fourier Transform implementations. The lowest reported power consumption for these is 390 nW. [22] reports measured results for a CWT filter with a power consumption $<$110 nW, but sufficient details to derive the FOM are not given. If simulated results are considered, [23] reports a 3$^{\text{rd}}$ order, 30 nW CWT filter; and [24] a 62 nW, 6$^{\text{th}}$ order CWT filter (similar to the order used here). In all cases the 60 pW power consumption of the LPCWT is nearly three orders of magnitude, or more, lower than these previous CWT implementations.

In addition to the lowest absolute power consumption, the FOM is improved by a factor of 3.45 compared to all the bandpass filters considered in Table III. Moreover, only one of the considered filters is capable of operating in the 2 Hz centre frequency region as required by the data reduction algorithm of [9]: [25] reports a bandpass filter with a minimum centre frequency of 0.1 Hz. However this comes at the cost of a large FOM and the maximum centre frequency is also limited to 5 Hz so a tuning range equivalent to the LPCWT filter is not possible. Note also that [26] reports a 2 pole bandpass filter with 60 dB dynamic range, a 122 μW power consumption and 11.1 Hz centre frequency. The lower frequency cut-off is at 0.88 Hz however, and so although the centre frequency reported is 11 Hz it may be possible to use the same technique to operate in the 2 Hz region. Similarly [27] reports a good performance 4$^{\text{th}}$ order bandpass filter with 250 pW power consumption at 10 Hz. Neither of these papers, however, provide sufficient details to derive the FOM and so they are not included in Table III.

Overall it is clear that the LPCWT reported here has excellent performance and can be of meaningful use for the online, low power, processing of physiological signals.

VI. Conclusions

This paper has presented a low frequency and low power 7$^{\text{th}}$ order bandpass filter for implementing the Continuous Wavelet Transform in the analogue domain. Nominal operation is

achieved with a 2 Hz centre frequency for a 43 dB dynamic range and 60 pW power consumption. Operation over a 1–64 Hz range, covering the bandwidth of the EEG, has also been demonstrated.

Wearable electronics require extreme miniaturisation and low power consumption to operate from physically small batteries. The Low Power CWT (LPCWT) presented here provides an ideal signal processing basis for use in online data reduction algorithms for reducing the total system power consumption. In comparison to the power required for the EEG front-end circuits the generation of CWT coefficients is *free*.

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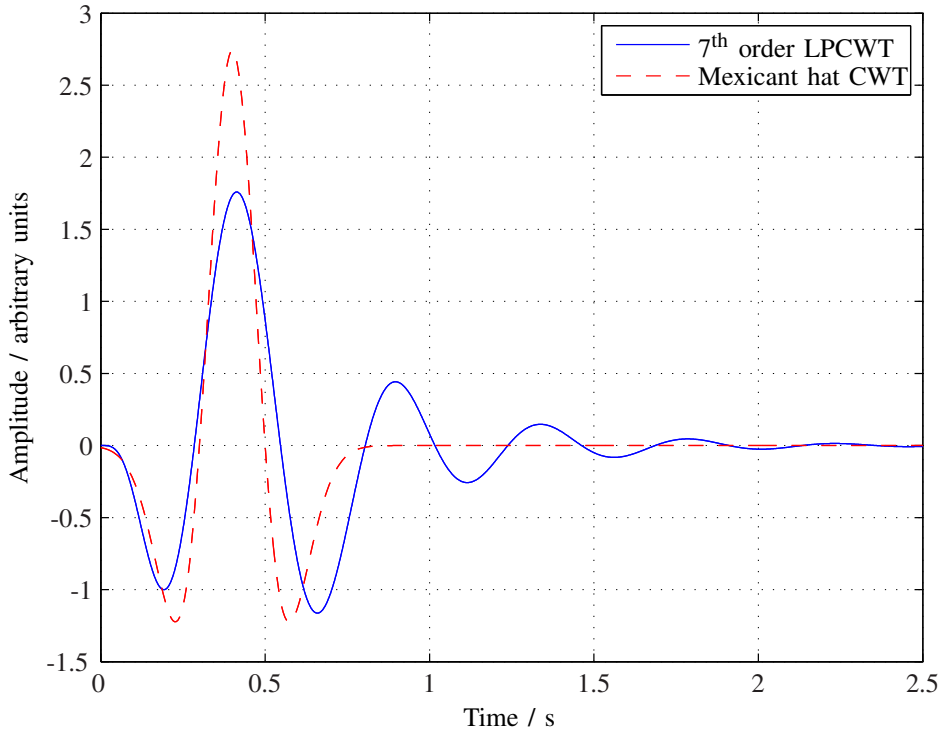


Fig. 1. The LPCWT mother wavelet, shown at scale $a = 0.1$ and $T = 0.4$ s, is designed to resemble the Mexican hat mother wavelet impulse response shape [7]. The Mexican hat wavelet is also shown and has been delayed by an amount T to allow a direct comparison to be made.

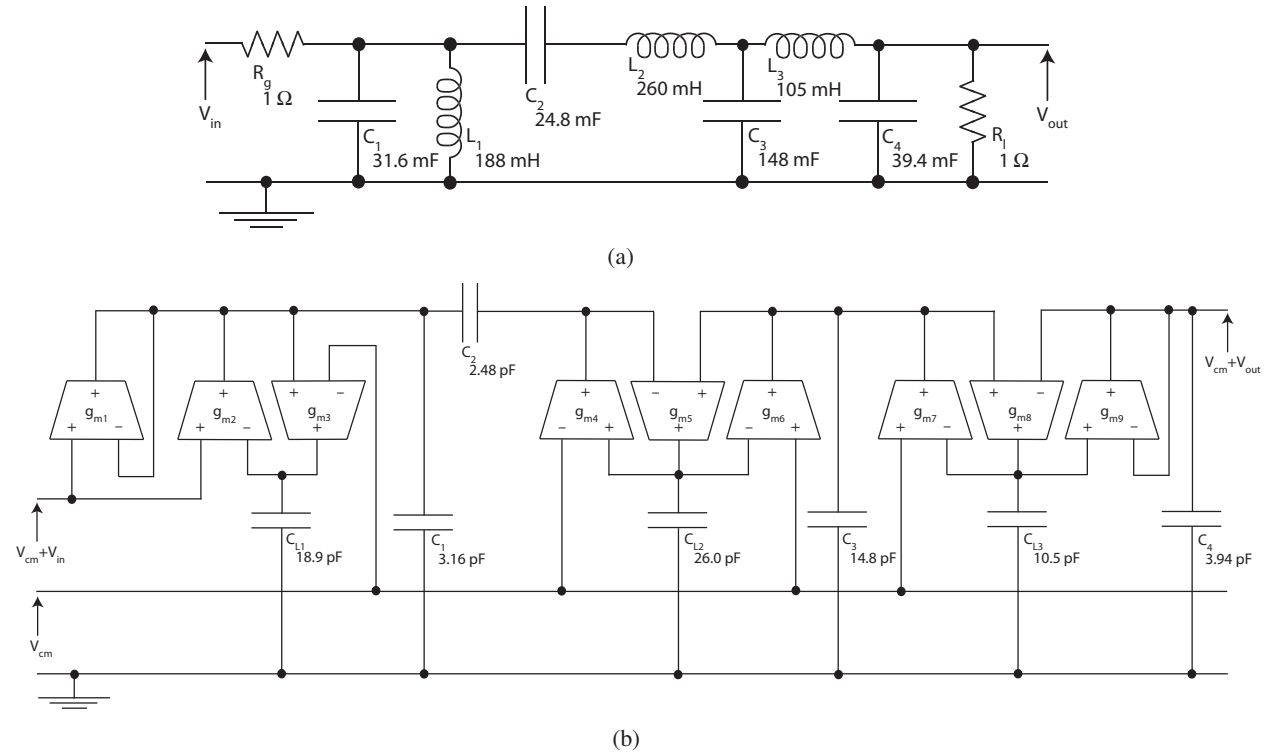


Fig. 2. Filter structures for implementing the 7^{th} order LPCWT (3). (a) Doubly terminated LC ladder prototype. (b) $g_m C$ simulation of the LC ladder prototype giving the LPCWT circuit implemented on-chip. All transconductances are 100 pS.

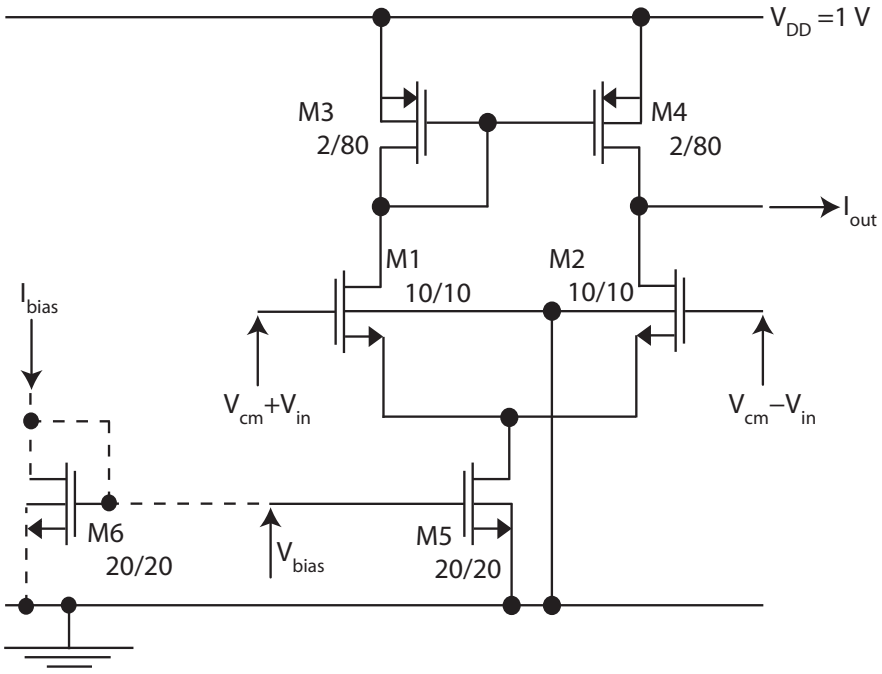
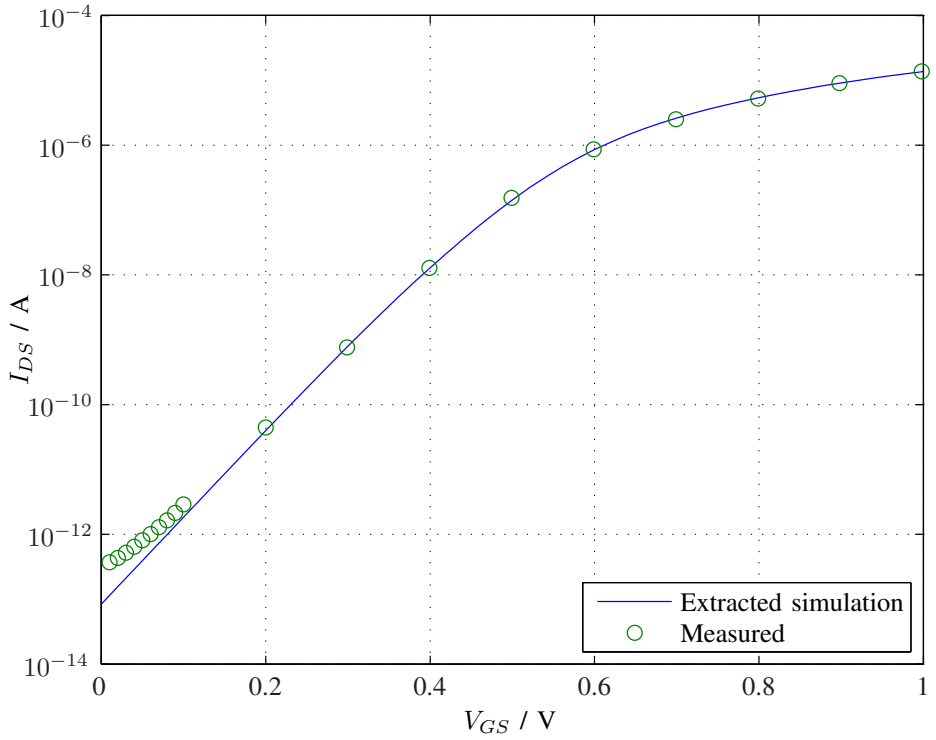
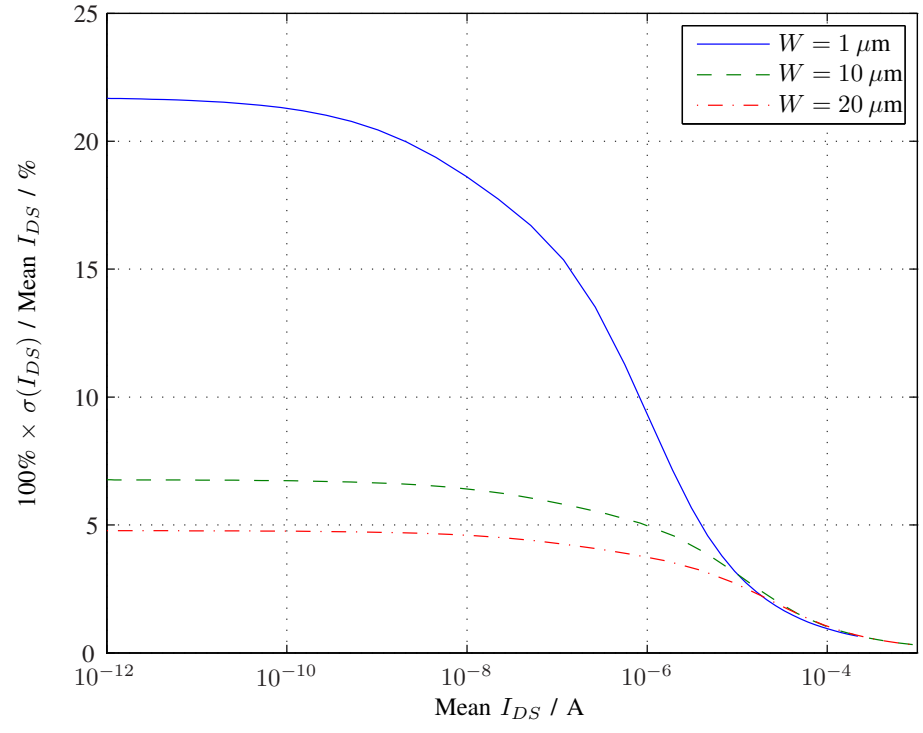


Fig. 3. NMOS differential pair transconductor used in the LPCWT $g_m C$ filter.



(a)



(b)

Fig. 4. Summary of trade-offs in deep weak inversion circuit design. (a) Measured $I_{DS} - V_{GS}$ results demonstrating the use of pico-Amp on-chip currents. At very low currents leakage currents in the bondpad limit the measurable current. (b) Relative current mismatch at different levels of transistor inversion and transistor widths (W). All transistor lengths are 1 μm. A high mismatch is present in weak inversion, but there is also a levelling off of mismatch between week and deep weak inversion operating regions.

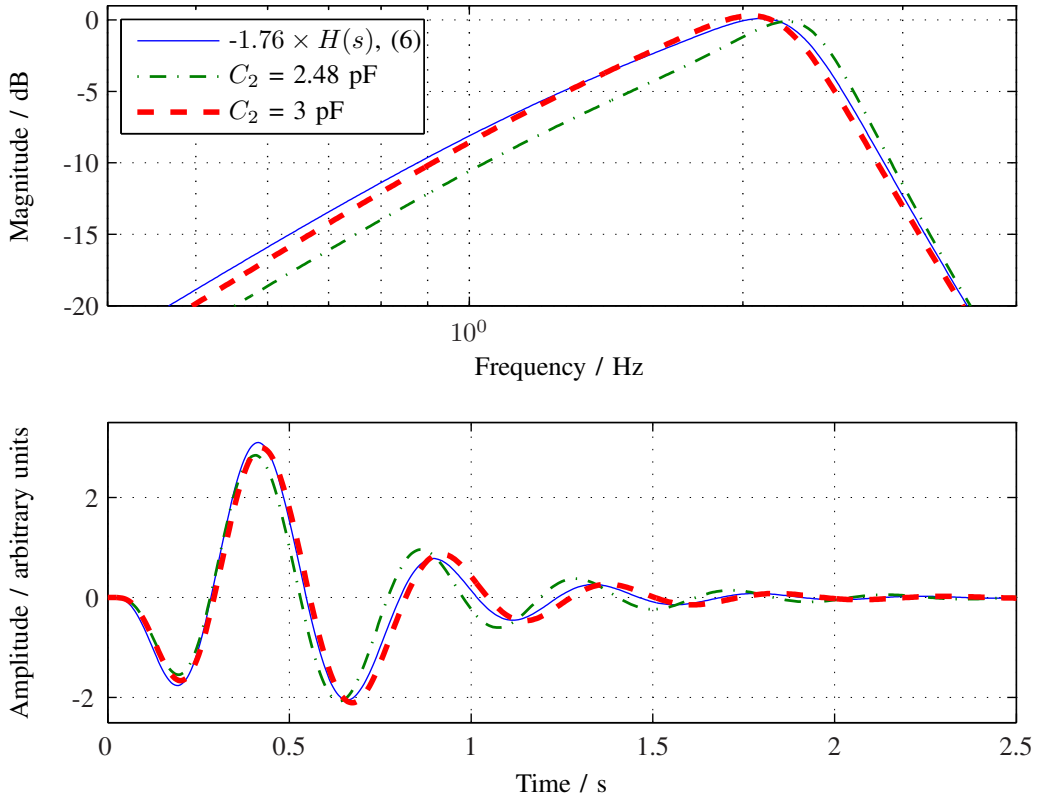


Fig. 5. LPCWT Bode magnitude and impulse responses. The limited transconductor bandwidth introduces distortion to the filter shape when using the ideal 2.48 pF value for C_2. Pre-distorting C_2 to 3 pF can overcome this from the topology level allowing larger transistors, with better matching, to be used.

Fig. 6. Micrograph of the fabricated g_mC filter.

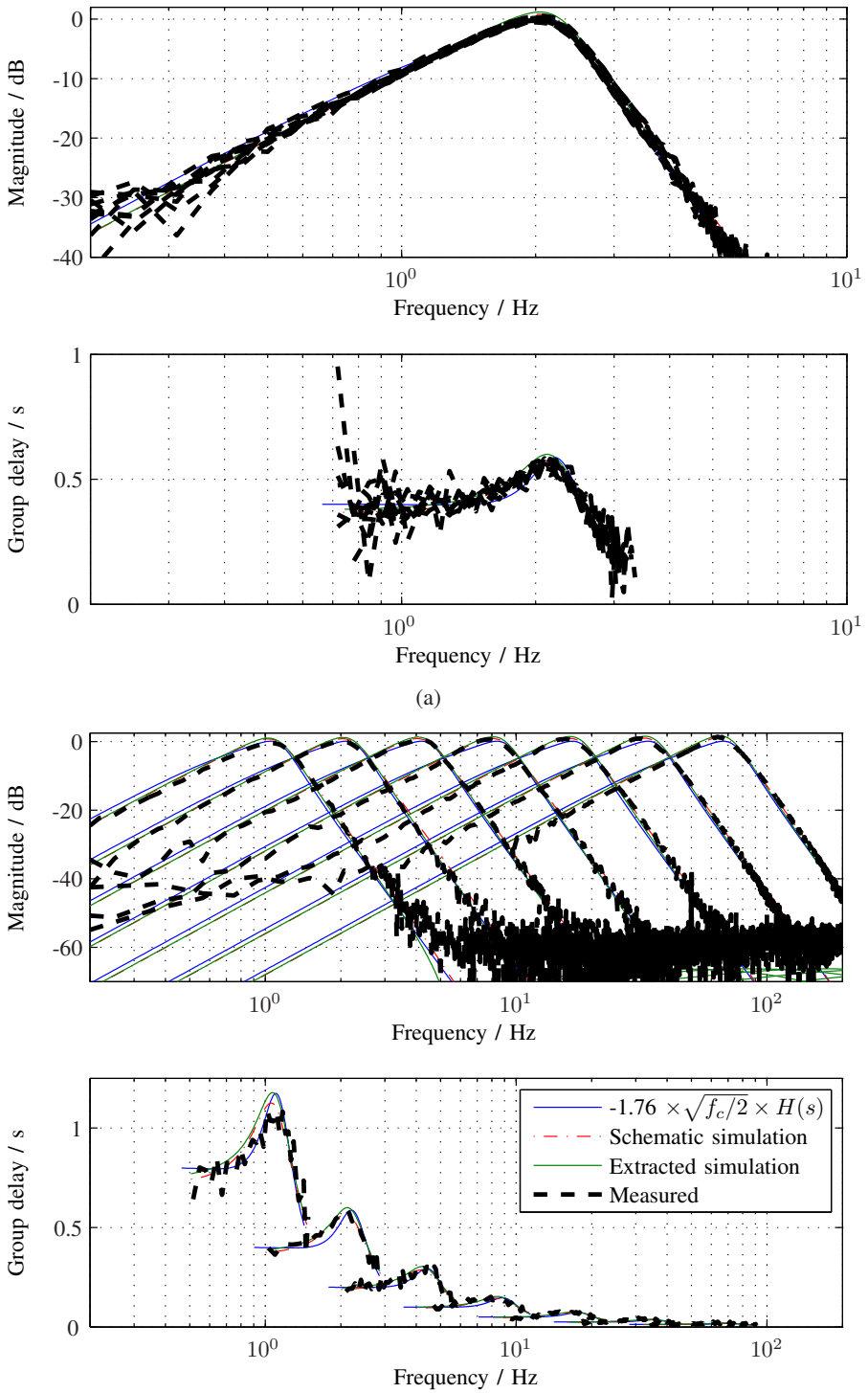
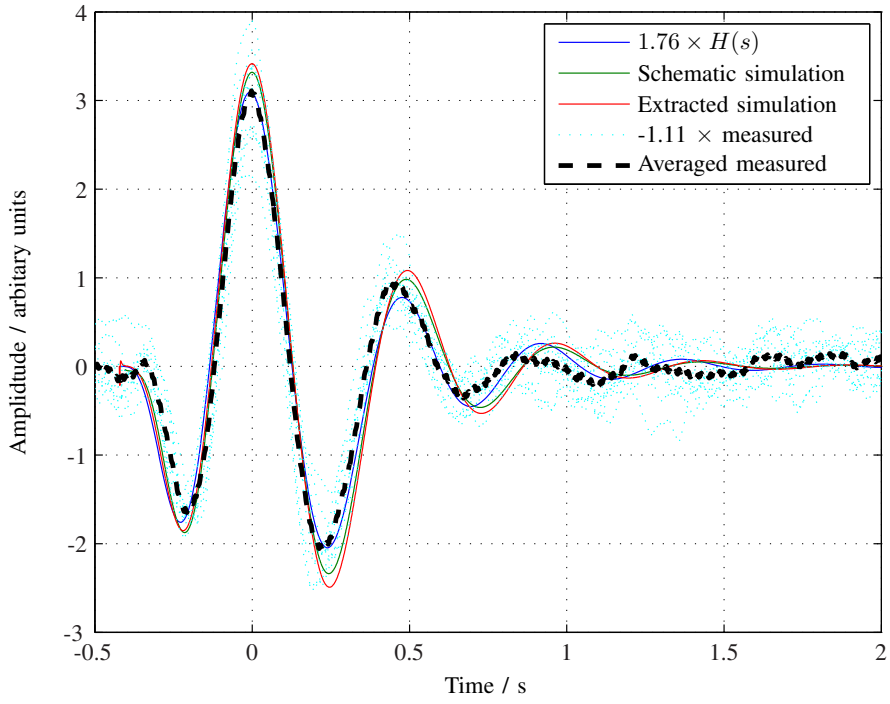
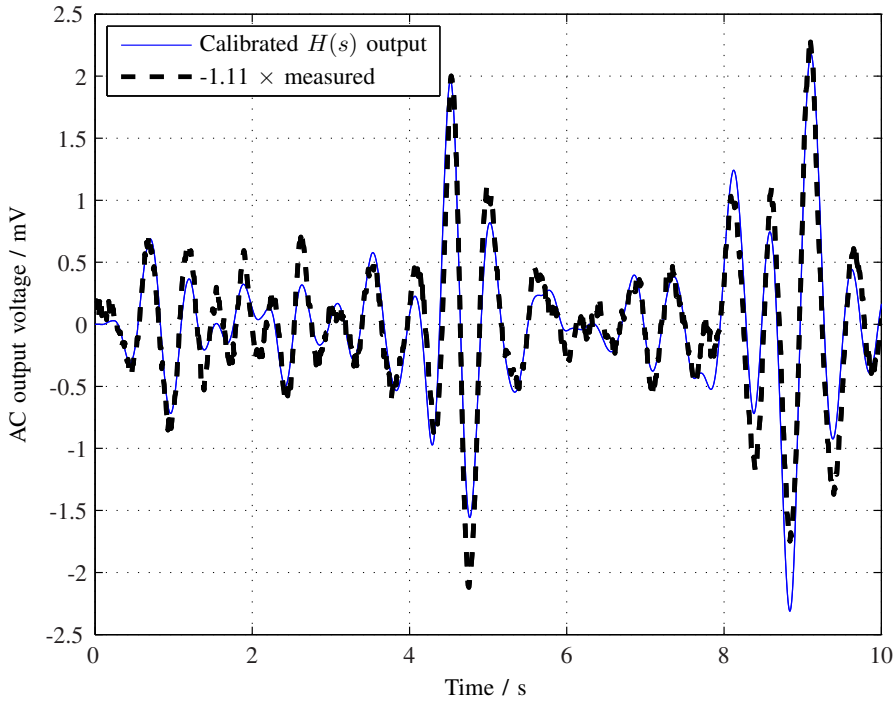


Fig. 7. Measured frequency responses demonstrating the LPCWT operation. The solid blue line shows the ideal LPCWT $H(s)$ function, (3), and the thick dashed line the measured implementation of this. (a) Responses for ten different chips biased with a 6 pA current. (b) Measured responses for one chip at seven centre frequency tunings. Tuning parameters are given in Table I.



(a)



(b)

Fig. 8. LPCWT transient responses. (a) Measured impulse response of the 2 Hz LPCWT filter shows the LPCWT wavelet. Before averaging the peak value of each response is shifted to occur at time 0 s. (b) 10 s of EEG data processed by the 2 Hz LPCWT shows the filter operation on real input signals.

TABLE I

SIMULATED AND MEASURED BIASING CONDITIONS REQUIRED TO FORM A WAVELET FILTER BANK AS ILLUSTRATED IN FIG. 7(B). ALL SIMULATIONS ARE PERFORMED AT 27°C.

f_c / Hz	I_{bias} / pA		V_{bias} / mV		Temp. / °C	a	T / s
	Extracted	Measured	Extracted	Measured			
1	3.25	2.5	119.6	62.4	26.5	0.2	0.8
2	6.5	6	141.9	85.4	26.5	0.1	0.4
4	13	13.5	164.2	111.6	26.5	0.05	0.2
8	26	28	186.5	162.9	26.0	0.025	0.1
16	53	58	209.6	162.9	25.5	0.0125	0.05
32	106	115	232.2	187.9	25.0	6.25×10^{-3}	0.025
64	213	230	254.9	210.9	25.0	3.125×10^{-3}	0.0125

TABLE II

SUMMARY OF SIMULATED AND MEASURED FILTER PERFORMANCE.

Parameter	Extracted simulation	Measured
Power supply	1 V	
CMOS process technology	0.35 μm	
Area	0.216 mm^2 (420×513 μm)	
Centre frequency (f_c) tuning range	Dyadic values in 1–64 Hz range covering EEG bandwidth	
Temperature dependence	Centre frequency directly proportional to temperature	
Bias current	6.5 pA (at 27°C, f_c 2.1 Hz)	6 pA (at 26.5°C, f_c 2 Hz)
Bias voltage	141.7 mV (at 27°C, f_c 2.1 Hz)	85.4 mV (at 26.5°C, f_c 2 Hz)
ICMR	400–600 mV	400–600 mV
Signal input range	Up to 20 mV$_{pp}$	Up to 20 mV$_{pp}$
SNR (×100 pre-amplification)	Up to 43 dB	Up to 43 dB
Output noise (at 2 Hz)	-85.5 dBVrms/$\sqrt{\text{Hz}}$	-86.9 dBVrms/$\sqrt{\text{Hz}}$
Input referred noise (integrated over 1.5–2.5 Hz passband)	51 μVrms	51 μVrms
THD (2 Hz, 20 mV$_{pp}$ input)	0.26%	0.30%
IMD3 (2, 2.1 Hz inputs, 20 mV$_{pp}$ total)	-19.99 dBc	-20.02 dBc
Dynamic range (for -20 dBc IMD3 at output)	42.8 dB	42.8 dB

TABLE III

COMPARISON OF BANDPASS FILTER PERFORMANCES FROM THE LITERATURE. LOWER FOM VALUES ARE BETTER. ONLY FILTERS WITH EXPERIMENTAL RESULTS AND SUFFICIENT DETAILS TO DERIVE THE FOM ARE CONSIDERED.

Ref.	Year	Process / μm	Minimum reported f_c / Hz	Power consumption (P) / W	Supply voltage (V_{DD}) / V	Number of poles (p)	Centre frequency (f_c) / Hz	Dynamic range[a] (DR) / dB	FOM
[28]	1997	1.60	12.5	8.8 n	1.8	3	50	62	17.1×10^{-13}
[25]	2002	1.20	0.1	28 μ	3.0	4	0.1	64.6	3.90×10^{-7}
[29]	2003	1.50	100	6.4 μ	2.8	4	10 k	65	68.5×10^{-13}
[30]	2004	0.80	100	2.5 μ	1.25	2	2 k	78	100×10^{-13}
[31]	2004	0.35	40	2.0 μ	1.0	2	40 k	45	5.56×10^{-13}
[32]	2005	0.35	30	290 n	1.8	4	75	51	341×10^{-13}
[20][b]	2005	0.18	14	6.5 μ	1.5	10	25 k	30	12.9×10^{-13}
[19]	2007	0.35	100	68 n	1.0	6	670	49	3.45×10^{-13}
[33]	2008	0.50	70	1.1 μ	3.3	2	1 k	55	336×10^{-13}
[21][b]	2009	0.18	500	875 n	1.2	8	3.5 k	37	10.1×10^{-13}
This work	2010	0.35	1	60 p	1.0	7	2	43	1.00×10^{-13}

[a]Calculated here as the RMS value of a sine wave with amplitude at the linear range limit divided by the RMS value of the in-band noise.

[b] [20], [21] are previously reported wavelet, or Short-Time Fourier Transform, bandpass filters using the Gabor wavelet.