A 0.006 mm² 1.2 µW Analog-to-Time Converter for Asynchronous Bio-Sensors

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Abstract—This paper presents a low-power analog-to-time converter (ATC) for integrated bio-sensors. The proposed circuit facilitates the direct conversion of electrode bio-potential recordings into time-encoded digital pulses with high efficiency without prior signal amplification. This approach reduces the circuit complexity for multi-channel instrumentation systems and allows asynchronous digital control to maximize the potential power savings during sensor inactivity. A prototype fabricated using a 65-nm CMOS technology is demonstrated with measured characteristics. Experimental results show an input-referred noise figure of 3.8 µVrms for a 11-kHz signal bandwidth while dissipating 1.2 µW from a 0.5-V supply and occupying 60 × 80 µm² silicon area. This compact configuration is enabled by the proposed asynchronous readout that shapes the mismatch components arising from the multi-bit quantizer and the use of capacitive feedback.

Index Terms—Analog-to-time conversion, asynchronous, bio-sensor, delta-sigma, instrumentation, low noise, low voltage.

I. INTRODUCTION

The current trend in sensor systems is to integrate many analog sensors together with larger digital systems to provide smart data collection for miniaturized wearables or low-cost system-in-package (SiP) electronics [1], [2]. The digital-oriented design flow of these systems compels designers to look for sensor interfaces that accommodate the trends in CMOS technology scaling and smaller supply voltages for digital power reduction. For this reason, many data converters and sensing circuits have utilized voltage controlled oscillators (VCOs) to convert analog signals into a periodic digital waveform where information is encoded by its frequency. This type of conversion is highly applicable at every technology node and the time encoded output is considerably more robust than the voltage output of conventional amplifiers when considering supply noise and the process, voltage, and temperature (PVT) variations. The time-domain concept has seen extensive use in recent publications because the voltage-to-frequency conversion provides high gain and exceptional dynamic range [3]–[5] that can also accommodate conventional chopper techniques [6], [7].

The conversion from analog to frequency is not the only means by which analog circuits can encode signals in the time domain. It is well known that both synchronous [8] and asynchronous [9] oversampling modulators will generate a pulsewidth-modulated (PWM) output bit stream. However, these realizations conventionally do not perform integration in the time domain and instead use charge pumps that suffer from typical drawbacks in advanced CMOS technologies such as gain degradation and limited voltage swing [10]. In contrast, the modulating characteristic of oscillators can negate component mismatch in any proceeding digital-to-analog conversion since the digital output inherently provides data-weighted averaging [5].

In order to retain high performance and minimize the requirement of ideal analog components, time-based systems should be designed in a fashion where only small error signals are processed in the analog domain with constrained linearity. Signals with large dynamics should be time-encoded and manipulated with robust digital logic. The proposed analog-to-time converter (ATC) realization that follows this concept is shown in Fig. 1. This topology presents an asynchronous delta–sigma modulator (ADSM) that accumulates a phase difference between two oscillators to realize time-based integration and utilizes capacitive feedback to linearize the conversion.

Here, the sensor’s voltage fluctuations on VIN modulate the pulsewidth of the PWM signal generated by the phase detector by combining multiple phases from each stage in the oscillator. In this fashion, the output bitstream DOUT can effectively resolve finer quantization levels. In contrast to prior oscillator-based systems that are clocked, the asynchronous operation proposed here enables the high-speed signal processing with oscillator-based filters [11] or a continuous-time digital core [12]. Both avoid the need for a high-speed clock when processing a large number of recording channels and can therefore enable substantial power saving.

Fig. 1. Proposed ATC that provides closed loop conversion of an analog input voltage into an asynchronous multi-bit digital data stream.
This paper is a first step toward realizing a sensor system that fundamentally only processes using the time-encoded signals and can potentially operate using a supply voltage of only several hundred millivolts since the circuit can accurately convert millivolt level signals without prior analog signal amplification [13], [14]. This is because oscillator-based integrators can operate with a voltage headroom close to transistor threshold voltage without diminishing loop gain or dynamic range. This advantage is not diminished by practical issues and large common-mode interference or electrode offset can be rejected because the sensor input is capacitively coupled to the main feedback loop. There are a number of established techniques such as using a dc servo loop or performing ripple rejection, which prevent these issues from degrading circuit performance [15]. This means that the voltage appearing at $V_X$ well controlled through feedback and that the amplifier can maximize power efficiency factor (PEF) [16] without requiring additional voltage overhead to accommodate voltage fluctuation at its input.

This paper presents the implementation and modeling aspects of the oscillator-based ATC using the following organization. Section II details the instrumentation topology and Section III describes the corresponding transistor level implementation, Section IV discusses the impact of technology and mismatch parameters of this circuit, Section V presents the measured results of a fabricated prototype, and Section VI concludes this paper.

II. CONCEPT AND ATC ARCHITECTURE

This section introduces the operating principle and circuit dynamics of the proposed instrumentation system that is used to sense intra-cortical neural activity using a conventional electrode instrumentation setup. Such a scenario would record activity in vivo or ex vivo from 1 Hz to 10-kHz frequency band where the signals are no larger than a few millivolts in amplitude [17]. The circuit sensitivity must match the noise characteristics of the electrode or biological tissue and target a noise floor of around 50 nV/√Hz [18]. These sensitivity conditions require the circuit to dissipate several microamps and easily leads to a circuit bandwidth much larger than 10 kHz. For this reason, this ATC will provide gain for a bandwidth exceeding 10 kHz since it is more resource effective to rely on proceeding processing stages to perform filtering when necessary.

A block diagram of the proposed architecture is shown in Fig. 2(a). For clarity, this shows the single-ended equivalent of the fully differential circuit that was implemented. The difference in potential between the two electrode inputs $V_R$ and $V_{IN}$ is chopped at the chopper frequency $f_{chp}$ to generate an up-modulated voltage waveform that couples the input onto $V_X$ through $C_f$. The essential mechanism here is that signals appearing on $V_X$ induce a current that feeds into two oscillators with different polarities after being demodulated. This current forces the oscillators to accumulate a relative phase difference because the phase is dependent on the integral of injected current [19]. This phase difference is then evaluated for each oscillator tap using XOR logic to yield multiple time-encoded PWM signals that can also be chopped using digital logic. The resulting digital signal is capacitively coupled onto $V_X$ in parallel to close the loop. This is the main signal amplifying path that realizes a first-order asynchronous ΔΣ modulator and this sense using $N$ phase detectors in parallel represents asynchronous quantization of the phase difference with a resolution of $\log_2(1+N)$ bits. Using this interpretation, we can construct the corresponding analytical model that is shown in Fig. 2(b) and will assist in deducing the design’s parameter dependencies

$$H(s) = \frac{1}{s/k_1 + Nf} \approx \frac{1}{s \cdot \frac{C_{GF} \cdot V_{RG}}{G_m} + \frac{C_F}{C_f} + \frac{C_C}{C_C + C_G/N}}$$

$$f = \frac{C_F}{C_f + C_F} \cdot \frac{N C_U}{C_F + N C_U + C_G}$$

First, the expression in (1) can be derived to characterize the signal amplifying loop. The feedback factor $f$ evaluated in (2) corresponds to the capacitive coupling of a particular PWM phase Q on to $V_X$ with respect to the capacitors $C_I$, $C_F$, $C_G$, and $C_U$. In this case, $C_G$ can be digitally tuned to provide varying gain settings (41–53 dB). The oscillator’s integration factor $k_1$ is derived by evaluating the impulse sensitivity function (ISF). The ISF captures how the oscillator phase is affected as a function of charge being injected into the virtual supply of the oscillator $V_R$ [19]. Following the derivation for (2) in [11], this factor can be assumed constant.
and is simply dependent on the transconductance \( G_m \), loading capacitance of each delay stage \( C_{\text{gate}} \), and the voltage across the oscillator \( V_{\text{RG}} \) such that \( k_1 = G_m/(\text{NC}_{\text{gate}} V_{\text{RG}}) \).

The second control loop is used to reject near-dc aggressors that will appear at the input of the main transconductor. Chopping will prevent the input-referred noise profile from being corrupted by flicker noise but in turn several large tones will appear at harmonics of \( f_{\text{chp}} \) because off-set is being up-modulated. Moreover, because this structure is not providing narrowband amplification, the feedback must actively suppress these tones to avoid the output from being saturated and distorted. These components are \( V_{\text{RG}} A_{\text{ripple}} = k_1 f_{\text{chp}} \), which induces a 90° phase shift. The phase shift can be corrected for by using the chopper clock that is delayed by 1/4th of the period when demodulating \( Q \) to recover the off-set. The flicker rejection further depends on the transfer function \( F(s) \) which represents how the recovered signal is smoothed and fed back onto \( V_X \). Using a charge pump in addition to the pseudo-resistor \( R_P \) will yield an expression for \( F(s) \) according to (3), where \( C_L \) and \( I_{\Delta} \) represent the main integration capacitor and charge pump bias current, respectively. This is also shown in Fig. 2

\[
F(s) = \frac{N I_{\Delta}}{s(C_L C_I R P_S + C_L + C_I)}.
\]

Combining \( F(s) \) and \( A_{\text{ripple}} \) will then predict how the noise aggressors at \( V_t \) are removed. The frequency-dependent response in Fig. 3 evaluates this control mechanism at different points in the loop using the following implemented circuit parameters: \( N = 5 \), \( f_{\text{chp}} = 75 \text{ kHz} \), \( C_I = 288 \text{ fF} \), \( C_G = 69 \text{ fF} \), \( C_F = C_U = 14 \text{ fF} \), \( R_P = 100 \text{ M\ensuremath{\Omega}} \), \( C_L = 1.6 \text{ pF} \), and \( I_{\Delta} = 5 \text{ nA} \). This shows the influence of noise at the input \( (e_{\text{IN}}^2) \) with respect to the ripple at the ATC output and the fluctuations on \( V_X \) as a function of frequency. First, note that the increased chopper frequency enables this circuit to increase its bandwidth and reject more of the low-frequency band including common-mode signals that asymmetrically couple onto \( V_X \). In addition, the second-order low-pass characteristic provides increased rejection of the chopper and oscillator tones such that the two control loops operate in isolation. A known drawback of increasing \( f_{\text{chp}} \) is the reduction in input impedance but as shown in Section IV-A, this reduction can be mitigated with technology scaling and using a smaller value for \( C_I \).

Given these dynamics, there is still an important distinction to be made with regards to the rate of information seen at the output and the 3-dB bandwidth for signal amplification that in this case is the product of \( f k_1 \approx 250 \text{ kHz} \). The digital output will encode an effective number of bits \( \text{(ENOB)} \) that relates to the ATC’s precision \( \text{[i.e., signal-to-noise and distortion ratio (SNDR)]} \) and presents pulsewidth information of every cycle that in this case is oversampled by \( N \) parallel phases. However, for one phase, the entropy rate can be estimated in terms of \( f_{\text{osc}} \) \( \text{(SNDR-1.76)/6.02} \). This highlights an important motivation for time-domain processing since this information rate may easily be 10\times larger than a clocked digital bitstream that maximally yields 1 bit per clock cycle. Optimistically, this implies that time-domain techniques achieve a proportional boost in power efficiency since the digital power dissipation is a function of \( f_{\text{osc}} \) even though a higher rate of information is being processed. For the latter to hold, we must require the analog and oscillator sub-blocks to operate with the negligible power budget.

### III. Circuit Implementation

The transistor schematic for the proposed ATC is shown in Fig. 4, and the size of each device is listed in Table I. This circuit can be segmented into four parts corresponding to the transconductor, oscillator, delay stage, and flicker rejection circuit. Each sub-block, including the capacitor array, will be described in the following. This configuration uses two bias voltages \( V_{\text{BN}} \) and \( V_{\text{BP}} \) to source the annotated drain currents. Both of these voltages are derived on-chip using a simple current mirror structure and a 1-\( \mu \text{A} \) off-chip reference. Furthermore, an external reference voltage \( V_C \) is used to control the common mode voltage of \( V_R \) that is placed at \( V_{\text{DD}}/2 \). Note that the 65-nm technology used here provides transistors that can be configured with 150-mV (lvt), 250-mV (vt), and 350-mV (hvt) threshold voltages \( V_{\text{TH}} \). The lvt option is used exclusively to reduce the supply voltage to 0.5 V with the exception of \( M_{23-24} \) which use a 250-mV threshold.

#### A. Low-Noise Transconductor

The complementary style transconductor [Fig. 4(a)] is adopted from [20] to exploit two aspects of oscillator-based integration. The first is that the operating conditions and transistor characteristics do not influence the loop gain of the time-based integrator but rather affect the noise characteristics which are already improved due to current recycling. Second, the voltage fluctuation across \( V_X \) and \( V_S \) is negligible particularly if all transistors in the \( G_m \) cell and oscillator are in sub-threshold operation. This implies that the circuit can operate reliably with a narrow \( V_{\text{DS}} \) margin for each transistor since the gate voltage \( V_X \) is carefully controlled in closed loop and there is little concern for instability. The self-biasing cascodes \( M_{3,6} \) biases each input pair with \( V_{\text{DS}} \) that is highly correlated with the threshold voltage and provides abundant dummy devices to improve matching. The cascodes also reduce the parasitic gate capacitance of the transconductor by reducing the Miller effect that may otherwise lead to increased noise.

![Fig. 3. Closed loop response of the flicker rejection loop due to input-referred noise \( e_{\text{IN}}^2 \) evaluated with respect to the ripple magnitude seen at \( Q \) (solid), the feedback seen at \( V_X \) (dotted), and the open loop response \( F(s) \cdot A_{\text{ripple}} \) (dashed).](image)
Achieving good noise performance for this configuration relies on minimizing the drain-current noise from each transistor in the oscillator when referred to the input [7]. As the ratio $I_{M10}/I_{M0}$ is reduced, the noise efficiency factor (NEF) of this circuit will asymptotically decrease to the optimal value for this topology (i.e., $\eta \sqrt{2}$) [21]. On the other hand, $I_{M10}$ controls the oscillation frequency which must be sufficiently large such that the oscillator harmonics lie out of band similar to the chopper harmonics.

The lack of filtering requirements allows the asynchronous implementation to choose a large $f_{osc}$ by reducing $C_{gate}$ such that any intermodulation products with $f_{chp}$ do not fall in-band [22], and the circuit size is minimized. When using this configuration as a clocked ΔΣ modulator [23], this freedom is lost because $k_1$ must be directly related to the oversampling ratio. If the system can afford, a fast oversampling clock $f_{osc}$ can still be large but it would be more effective to choose $f_{osc}$ close to the Nyquist frequency such that the harmonics of $f_{osc}$ can be removed reliably during decimation as they have already been shaped by the loop filter. This circuit also constrains the minimum value for $N$ due to the limited linearity of the transconductor for a given input range. This is because the ratio $2V_{DD}/f/(N + 1)$ determines the maximum peak-to-peak amplitude of the error signal seen at $V_X$. Fortunately, for high-gain applications, $f$ is small resulting in sub-millivolt signal at $V_X$, and therefore high linearity can be achieved while using just a few phases in parallel.

Table I

<table>
<thead>
<tr>
<th>Device</th>
<th>Size (W/L)</th>
<th>Device</th>
<th>Size (W/L)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M_0$</td>
<td>26/5</td>
<td>$M_{15-16}$</td>
<td>0/2.5</td>
</tr>
<tr>
<td>$M_{1-2}$</td>
<td>16/0.25</td>
<td>$M_{17-18}$</td>
<td>2/5</td>
</tr>
<tr>
<td>$M_{3-4}$</td>
<td>2/1</td>
<td>$M_{19-20}$</td>
<td>10/0.2</td>
</tr>
<tr>
<td>$M_{5-6}$</td>
<td>4/0.5</td>
<td>$M_{21-22}$</td>
<td>1/6/0.4</td>
</tr>
<tr>
<td>$M_{7-8}$</td>
<td>0.8/1.4</td>
<td>$M_{23-24}$</td>
<td>0.96/4</td>
</tr>
<tr>
<td>$M_{9}$</td>
<td>32/0.1</td>
<td>Logic</td>
<td>0/3/1</td>
</tr>
<tr>
<td>$M_{10}$</td>
<td>6/5</td>
<td>Switch$^{chp}$</td>
<td>1/0.1 ($P_{type}$)</td>
</tr>
<tr>
<td>$M_{11-12}$</td>
<td>1.5/2.4</td>
<td>Switch$^{ch}$</td>
<td>1/0.2 ($N_{type}$)</td>
</tr>
<tr>
<td>$M_{13-14}$</td>
<td>2.3/2.5</td>
<td>$C_L$</td>
<td>21/21</td>
</tr>
</tbody>
</table>

B. Pseudo-Differential Oscillator

The main feature of the oscillators [Fig. 4(b)] used by this ATC is that it uses differential logic and the delay stage [Fig. 4(c)] is biased around the middle of the supply making the digital buffers for phase detection more power efficient. The corresponding advantages are best contrasted with a simple inverter delay cell that uses a capacitive load to ground. First, the inverter-based implementation would experience voltage spikes on $V_R$ due to discontinuous conduction of current but would also contaminate the ground with the ac current pulses. The configuration adopted from [24] exhibits continuous charging and discharging currents that can be confined within the virtual supply nodes $V_G/V_R$. Moreover, using switching transistors that are several square micrometers in size to load for the preceding gate reduces the sensitivity to process variation with smaller area requirements since the transistor gate capacitance achieves a higher density than poly-poly or metal-oxide-metal (MOM) capacitors.

C. Flicker Rejection Stage

The flicker removal circuit [Fig. 4(d)] biases the input of the transconductor by feeding back common-mode and differential-mode signals using a cross-coupled load to enable low voltage operation without an additional common-mode feedback circuit [20]. The differential feedback provides flicker cancellation by demodulating the digital output using a switched current digital to analog converter (DAC) that integrates on $C_L$ which is a large vertical metal-insulator-metal (MIM) capacitor placed over the analog circuitry. The diode connected devices $M_{21-22}$ represent pseudo-resistors of 100 MΩ that provide a resistive path to $V_X$ and further smooth high-frequency tones from $f_{chp}$ and $f_{osc}$. A significant variation in resistive value is inherently expected but it is important to note that it does not influence the signal amplifying path and the non-dominant poles are far away from the 8-kHz bandwidth of $F(s)$ in (3) by virtue of not using a second analog integrator that may compromise stability. The common mode feedback regulates $V_R$ with respect to $V_C$ by biasing the common mode of $V_X$. For this loop, the gain arises from transconductance ratio $g_{mM19-M20}/g_{mM23-M24}$ together

Fig. 4. Transistor level implementation of the ATC circuit in Fig. 2(a). Here, the complementary structure represents (a) main transconductor. (b) Pseudo-differential oscillator where each delay cell is shown in (c). (d) Flicker rejection stage where only the gray section is replicated for each phase. Note that all devices have their body connected to the corresponding supplies with the exception of $M_{5-8}$ which have the body connected to the drain of $M_9$. Furthermore, $M_{13-16}$ and $M_{21-22}$ their body connected to $V_R$ and either terminal of $C_L$, respectively.
with the drain resistance ratio \( \text{rds}_{M10}/(\text{rds}_{M0} + \text{rds}_{M9}) \). This readily provides over 30 dB of gain with the dominant pole provided by the pseudo-resistors that will also attenuate the input common-mode signals.

D. Capacitive Feedback Network

Both electrode inputs feed into separate capacitor arrays that offset the scaled PWM signal generated at the output to calculate the differential error signal on \( V_X \). Each array is \( 20 \times 23 \) \( \mu \text{m}^2 \) in size and uses 28 elements in a \( 4 \times 7 \) configuration with \( 2.7 \times 2.7-\mu \text{m}^2 \) horizontal MOM capacitors with six fingers on metal layers 2–7. The following allocation is used: \( C_I = 17\times, C_F = 1\times, C_U = 5\times, C_G = [0–5]\times \). The particular configuration in Fig. 2 can readily accommodate changes in dynamic range or adjustments in \( N \). This is because \( f \) is dominated by the ratio \( C_F/C_I \) such that the design can freely change the number of phases being fed back without significantly changing the amplification dynamics. In addition, increasing \( C_F \) will extend the dynamic range of the circuit since the noise floor will remain unchanged while providing less signal gain and having excessive circuit bandwidth.

IV. IMPACT OF TECHNOLOGY PARAMETERS

This section further highlights two features of the proposed topology that can be taken advantage of in advanced CMOS technologies where mismatch and process variation are the leading concern for designers. First, we will summarize the scaling properties that arise while chopping in the input signal, and then, we will show that also for the asynchronous case, the time-domain integration fundamentally helps with mitigating mismatch in digital-to-analog conversion using a behavioral model as an example.

A. CMOS Scaling of Chopper Impedance

First, consider the input impedance \( R_{\text{IN}} \) of the simple chopper structure used here [25]. For sensor applications, it is essential to maintain a large input impedance that avoids signal attenuation because many integrated sensors exhibit a source resistance of several megaohms

\[
C_I = 10C_{\text{GM}} = \frac{20}{3}WLC_{\text{ox}} \tag{4}
\]

\[
f_{\text{chp}} = 2f_{\text{cor}} = \frac{2K_F}{WLC_{\text{ox}}e_{\text{gd}}^2}. \tag{5}
\]

The expression in (4) is first used to select \( C_I \) as \( 10\times \) the parasitic capacitance \( C_{\text{GM}} \) seen on \( V_X \) due to the transconductance. This configuration avoids degrading the noise performance during amplification [17]. \( C_I \) is further equated in terms of the width \( W \) and length \( L \) of the input transistors. The chopper frequency is placed at exactly twice the corner frequency \( f_{\text{cor}} \) which is the frequency at which the flicker noise is equal to the thermal noise floor \( e_{\text{gd}}^2 \) of the target input-referred noise profile. Rearrangement of the terms will yield (5), which uses the trap density \( K_F \) to estimate for flicker noise for a specific fabrication process [26]

\[
R_{\text{IN}} = \frac{1}{2C_I f_{\text{chp}}} = \frac{3C_{\text{ox}}e_{\text{gd}}^2}{80 K_F} \tag{6}
\]

Equation (6) calculates the expected input resistance and provides a first-order estimation of amplifier impedance with respect to process parameters. The fact that \( R_{\text{IN}} \) depends linearly on \( C_{\text{ox}} \) implies that input resistance can be improved by using more advanced technologies. The expected values for \( R_{\text{IN}} \) are plotted in Fig. 5 as a function of CMOS technology with varying noise requirements. Eventually, the gate leakage will inhibit this trend as the associated shot noise limits the sensitivity for technologies beyond 65 nm. This result primarily constrains the selection of transistor size [25] that in turn determines \( f_{\text{chp}} \) and \( f_{\text{osc}} \).

B. Modulated Mismatch in Oscillators

Mismatch due to process variation is the primary cause of distortion during multi-bit signal conversion. Minimizing this source of nonlinearity is essential for both synchronous and asynchronous \( \Delta \Sigma \) modulators because mismatch in the feedback DAC is not shaped by the loop filter [27]. Fortunately, the modulating property of the oscillator can remove this distortion if the phase readout is performed in a parallel fashion [5]. Here, we will concisely demonstrate that property arises because the mismatch induced components are simply being averaged and induce a dc-offset together with tones at the harmonic components of \( f_{\text{osc}} \). This uses a mapping that relates the phase difference \( x \) to the generated PWM waveform as a function of time \( \tau \) defined in (7). The following expression in (8) then evaluates the analog feedback voltage that appears on \( V_X \) in the ideal case for a given a phase difference of \( \Delta \phi \) between the two oscillators

\[
A(\tau, x) \triangleq \begin{cases} 
1 & \tau \text{(mod} 1) < x \\
0 & \text{otherwise}
\end{cases} \tag{7}
\]

\[
V_X(t) = f \cdot \sum_{k=0}^{N-1} A(t \cdot f_{\text{osc}} + \frac{k}{N}, \Delta \phi) \tag{8}
\]

\[
Q_k(t) = \left(1 + \frac{\sigma_{\text{C},k}}{C_U}\right) A(t \cdot f_{\text{osc}} + \frac{k}{N}, \sigma_{\tau-\mu,k} + \Delta \phi). \tag{9}
\]

There are two-independent sources of mismatch for each phase: the deviation in capacitor weights of \( C_U \), \( \sigma_{\text{C},k} \) and the differential delay variation in oscillator stages as a fraction of the oscillation period \( \sigma_{\tau,k} \) that includes the digital gates
generating $Q$ (i.e., inverters and XOR-gate). These are used to formulate (9) that considers a particular phase of $Q(t)$ and the random mismatch variables that have process dependent normal distributions. The variation in delay will locally increase/decrease the pulselength of $Q$ for a specific phase $k$. This is a time-invariant component of the gate delay while $\Delta \phi$ and $T_{osc}$ are signal dependent. Precisely formulating the cumulative variation of $\sigma_T$ will relate the transistor sizing, gate capacitance, and threshold voltage of each delay during operation.

Notice that $A$ is a linear function of $\Delta \phi$ with a gain of 1 for the dc component of the PWM output which can be further expanded to extract the high-frequency behavior. However, by design, these components are intentionally avoided which should reveal that the capacitor weights are always uniformly distributed. Expanded to extract the high-frequency behavior. However, the dc component of the PWM output which can be further expanded to extract the high-frequency behavior. However, the dc component of the PWM output which can be further expanded to extract the high-frequency behavior. However, the dc component of the PWM output which can be further expanded to extract the high-frequency behavior. However, the dc component of the PWM output which can be further expanded to extract the high-frequency behavior. However, the dc component of the PWM output which can be further expanded to extract the high-frequency behavior.

Verifying this behavior is best done by modifying the behavioral model commonly used for oscillators [28] to accommodate multi-phase readout using the above-mentioned expressions. Such a model is shown in Fig. 6. This configuration uses an internal time variable at $v_T$ that accumulates according to $f_{osc}$. Given a set of quantization levels $L_k$ or equivalently the number of phases, a logical function $B$ will compute the corresponding PWM waveform of $Q$, which are weighted by the associated capacitor $C_k$. In this case, the digital gate delay arising from computing the phase difference and applying feedback to the capacitive DAC can also be modeled by adjusting $\tau_{dly}$

$$B(\phi_S, \phi_R, L) \triangleq (\phi_S > L > \phi_R) \lor (\phi_S < \phi_R < L)$$

$$\lor (L < \phi_S < \phi_R). \quad (10)$$

The logical expression in (10) simply compares the two phases with respect to $L$ and evaluates the digital condition for which the output should be high. This representation implies that the delays correspond to the interval between each level which can be distributed uniformly as $L_k = (0.5 + k)/L$ for integers $k$ from 0 to $N - 1$. By distributing the quantization levels from 0 to 1, the corresponding delays are inherently normalized to the periodicity of $\phi_S/\phi_R$ without explicitly having to compute values with respect to $f_{osc}$ even when it is dynamically changing. In addition, a difference in oscillator frequency between $X_{1-2}$ can also be accommodated by adding a second integrated frequency component to the summation node.

Now the impact of mismatch can be simulated by adding parameter variation in the quantizer levels and the feedback weights ($f$). The analogous case where the mismatch is not modulated (i.e., $f_{osc}$ is 0) loosely corresponds to a flash-based ADC since the phase is simply being compared with $N$ thresholds. The corresponding spectra of the flash quantizer is shown in Fig. 7 and the oscillating quantizer is shown in Fig. 8 where we observe the distortion components in different bands of the spectrum.

V. MEASURED RESULTS

The commercially available Taiwan Semiconductor Manufacturing Company (TSMC) 65-nm CMOS low power mixed signal (MS) RF technology (1P9M 6X1Z1U RDL) was used to prototype the proposed circuit and demonstrate measured noise and linearity characteristics. The chip micro-photograph of this prototype is shown in Fig. 9. The setup used to take
these measurements is shown in Fig. 10 and uses a custom printed circuit board to regulate $V_{DD}$ on-board with additional decoupling.

The external biasing allows this setup to first tune the circuit sensitivity by adjusting the 1-μA reference current which scales all bias currents proportionally and then using $V_C$, the oscillation frequency can be fine-tuned as $V_R$ is controlled which modulates $I_{M\text{10}}$. The supply voltage can be tuned but reducing the supply below 0.5-V limits the biasing current and reduces the circuit sensitivity. Similarly, increasing the supply is mainly constrained by the buffers that digitize the oscillator waveform and can induce a large leakage current beyond a voltage of 0.65 V.

The tone generated by the Agilent signal generator is attenuated resistively by a factor of 10 to achieve a low-noise differential test signal at the input of the instrumentation circuit. Two phases from the asynchronous output Q are captured at 500 MS/s using high-speed digital scope which can then be post-processed off-line to investigate the features of separate PWM signals during different operating conditions. Both the chopper tones and PWM carrier can be observed outside the signal bandwidth at harmonics of 78 and 350 kHz, respectively.

The characterization procedure evaluates the SNDR for varying input amplitudes and frequencies. For a particular device, this characteristic is shown in Fig. 11. In extension, Figs. 12 and 13 show the distortion components as a function of amplitude along single amplitude (SA) and the frequency along single frequency (SF), respectively. Fig. 14 shows what the input-referred power spectral density of $Q$ looks like for a particular operating point at P. Here, the lowest gain setting of 41 dB was used to demonstrate operation with the maximum dynamic range. Although the circuit bandwidth theoretically exceeds the range of frequencies resolved here, the interfering tones shown in Fig. 14 prevent inaccurate measurements to confirm this result. Using a similar procedure, the common-mode rejection ratio (CMRR) is characterized and shown in Fig. 15. Again, Figs. 16 and 17 show the distortion components due to a common-mode input as a function of amplitude along SA and frequency along SF, respectively. Due to the limited voltage overhead from the current sources in the transcondutor, the high-frequency common-mode interference can result in degenerated operation as they are not attenuated by the pseudo-resistor. This mode of failure where the oscillators are saturated is outlined by the dashed region.

Note that flicker noise from each oscillator is not removed by the chopper configuration in Fig. 4. However, there is no apparent 1/f noise profile in the 10–100-Hz band even though
the oscillators are small in size. This is because the rms gate-voltage fluctuation due to flicker noise at each device is scaled by the open-loop gain of the ATC when referred to the input.

The maximum achieved total harmonic distortion was 60 dB for a 1-kHz sinusoidal input. The main source of performance degeneration in this circuit for larger input signals is due to the use of poorly regulated bias currents in the differential pair and relying on pseudo-differential phase read-out that allows some common-mode fluctuation at \( V_S \) to couple to the output \( Q \). Either introducing cascodes or using a folded cascode topology may improve linearity at the cost of increasing the required voltage headroom or reducing the noise efficiency. However, the dynamic range exceeding 50 dB should be sufficient for the physiological range of amplitudes for neural activity given that there are no external aggressors present during recording. We can further confirm the effectiveness of the mismatch rejection technique as the Monte Carlo simulation results indicate that each phase should exhibit 1.1% standard deviation in coupling factor for a \( 3 - \sigma \) confidence interval. This should lead to a similar distortion characteristic shown in Fig. 7 with a large number of dominant harmonics being generated due to mismatch errors. Instead, distortion is dominated by the second and third harmonic typical of more conventional analog nonlinearity.

The input impedance of this circuit was estimated by removing the resistive attenuation network and instead capacitively coupling the signal generator to the input. This assumes that the input will exhibit a \( RC \) time constant that is dominated by the coupling capacitor and the resistive/leakage component from the chopper in combination with the electrostatic discharge protection that can be measured directly. The frequency-dependent response is shown in Fig. 18. The 3-dB cutoff frequency was estimated at 21.8 Hz. In this case, two 0.47-nF capacitors were used to couple both inputs which implies the input resistance is around 31 M\( \Omega \). Parasitics at the input or capacitor variation can inflate this value and it is likely the impedance is closer to the analytical estimate of 22 M\( \Omega \) according to (6).

The detailed system characteristics are summarized in Table II. The system power dissipation was specified at 1.3 \( \mu \)W from these measurements. The relative power and area utilization of each sub-circuit is compared in Fig. 19. As expected, a large fraction of both power and area is used by the main analog circuits that consist of the low-noise transconductor and the flicker rejection stage. This distribution maximizes the NEF and shows that the asynchronous digital logic can provide additional functionality without a significant resource overhead. In relation to the work in [7], this ATC topology exhibits a significant reduction in power budget although input-referred noise figure is slightly increased. This improvement is not as pronounced in comparison with [8] but instead the figure of merit is superior. Other works show that both time-based and voltage-based instrumentation can achieve near ideal noise efficiency but only select topologies enable more advanced CMOS process to yield a smaller silicon
TABLE II
SYSTEM CHARACTERISTICS AND COMPARISON WITH STATE OF THE ART

<table>
<thead>
<tr>
<th>Parameter</th>
<th>This Work</th>
<th>[8]</th>
<th>[29]</th>
<th>[7]</th>
<th>[6]</th>
<th>[30]</th>
<th>[31]</th>
<th>[32]</th>
<th>[33]</th>
<th>[34]</th>
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<tbody>
<tr>
<td>Application</td>
<td>EAP</td>
<td>BCG</td>
<td>LFP</td>
<td>LFP</td>
<td>ECG</td>
<td>EAP</td>
<td>EAP</td>
<td>EAP</td>
<td>EAP</td>
<td>EAP</td>
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<tr>
<td>Technology [nm]</td>
<td>65</td>
<td>40</td>
<td>130</td>
<td>40</td>
<td>40</td>
<td>65</td>
<td>65</td>
<td>90</td>
<td>180</td>
<td>65</td>
</tr>
<tr>
<td>Modality</td>
<td>Time</td>
<td>Time</td>
<td>Volt</td>
<td>Time</td>
<td>Volt</td>
<td>Volt</td>
<td>Volt</td>
<td>Volt</td>
<td>Volt</td>
<td>Mix</td>
</tr>
<tr>
<td>Supply-V [V]</td>
<td>0.5</td>
<td>0.6</td>
<td>1.2</td>
<td>1.2</td>
<td>1.2</td>
<td>0.6</td>
<td>1</td>
<td>1</td>
<td>0.45</td>
<td>0.5</td>
</tr>
<tr>
<td>Supply-I [A]</td>
<td>2.55 μ</td>
<td>5.5 μ</td>
<td>5.3 μ</td>
<td>14 μ</td>
<td>2.5 μ</td>
<td>3 n</td>
<td>3.3 μ</td>
<td>2.8 μ</td>
<td>2.1 μ</td>
<td>10 μ</td>
</tr>
<tr>
<td>Bandwidth [Hz]</td>
<td>11 k</td>
<td>150</td>
<td>500</td>
<td>5 k</td>
<td>200</td>
<td>370</td>
<td>8.2 k</td>
<td>10.5 k</td>
<td>10 k</td>
<td>10 k</td>
</tr>
<tr>
<td>Input Range [mVpp]</td>
<td>4</td>
<td>40</td>
<td>-</td>
<td>8</td>
<td>400</td>
<td>25</td>
<td>220</td>
<td>1</td>
<td>1</td>
<td>1</td>
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<tr>
<td>CMRR [dB]</td>
<td>&gt;60*</td>
<td>60</td>
<td>90</td>
<td>97</td>
<td>60</td>
<td>&gt;80</td>
<td>&gt;45</td>
<td>73</td>
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<tr>
<td>SFDR [dB]</td>
<td>60</td>
<td>56</td>
<td>72</td>
<td>70</td>
<td>79</td>
<td>75</td>
<td>&gt;40</td>
<td>&gt;37</td>
<td>&gt;46</td>
<td>&gt;34</td>
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<tr>
<td>Noise Floor [V/√Hz]</td>
<td>36 n</td>
<td>0.6 μ</td>
<td>46n</td>
<td>32 n</td>
<td>5 n</td>
<td>27.5n</td>
<td>1.4 μ</td>
<td>3n</td>
<td>29n</td>
<td>29n</td>
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<tr>
<td>RMS Noise [μV_m]</td>
<td>3.8</td>
<td>7.8</td>
<td>1.1</td>
<td>2.3</td>
<td>5.2</td>
<td>26</td>
<td>4.1</td>
<td>3.04</td>
<td>3.2 μ</td>
<td>4.9 μ</td>
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<td>Area [mm²]</td>
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<td>0.013</td>
<td>0.015</td>
<td>0.135</td>
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<td>0.042</td>
<td>0.137</td>
<td>0.25</td>
<td>0.013</td>
</tr>
<tr>
<td>NEF/PEF</td>
<td>2.2/2.4</td>
<td>8.1/39</td>
<td>2.9/10</td>
<td>4.7/27</td>
<td>22/581</td>
<td>2.1/2.6</td>
<td>3.2/10</td>
<td>1.9/3.6</td>
<td>1.57/11</td>
<td>5.99/18</td>
</tr>
</tbody>
</table>

* For common-mode frequencies <200 Hz

footprint. The pioneering work in [34] already demonstrated that resource efficient signal acquisition is best realized by combing signal quantization and amplification into a single loop. The main drawback was that this mixed signal topology was still relatively complex for hundreds of channels and linearizing the feedback for closed loop quantization came with a considerable reduction in noise efficiency. However, the operation of the clocked VCO and the modulated DAC in the feedback enable a powerful technique that trades off excessive bandwidth for reduced circuit size or DAC complexity. The same technique is applied here to enable a compact multichannel configuration. Our future work will extend on the current prototype by additionally providing electrode off-set cancellation for in vivo experiments with multi-channel recording capabilities.

VI. CONCLUSION

This paper proposes a chopper stabilized ATC to enable high-impedance electrode instrumentation for integrated sensing systems that require ultralow-voltage operation for power saving. The time-domain techniques enabled by this ATC topology alleviate the difficulty of performing precise instrumentation in advanced CMOS technologies while also providing improved power efficiency together with a substantial reduction in size. The presented configuration achieves a power budget of 1.2 μW for a 36-nV/√Hz noise floor requirement and a compact silicon footprint of 0.006 mm². In extension to presenting the implementation details, this paper also provides essential modeling and analytical tools for further optimization. This will enable other mixed-signal systems that require high-noise efficiency, high speed, or asynchronous signal conversion to effectively adopt time-based techniques and utilize the presented circuit implementation.

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REFERENCES


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