High Capacitance Silicon Nanowire Array Electrodes

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Dissertation submitted to fulfil in part the requirements for the degree of Doctor of Philosophy
DECLARATION

The content of this dissertation relates to original work carried out in Imperial College London, primarily in the Department of Electrical and Electronic Engineering and the Department of Chemistry, with all other material being acknowledged and/or referred to as otherwise. The work carried out is the original work of the author, with intra-university collaborations with MRes projects of Lu Qiao and Foivia Konstantinou, and as such, contains work done in collaboration with them.
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PUBLICATIONS

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ABSTRACT

The interest in the development of improved, alternative and application-specific electrical energy storage solutions presents the opportunity for Si-based device with the functionality of electrochemical capacitors (ECs). Metal-assisted chemical etching (MACE) provides a low temperature and low-cost method of obtaining a high-density array of high aspect ratio silicon nanowires. The high surface area of the silicon nanowire arrays (SiNWA) is utilised to develop a high capacitance electrode, in conjunction with an ionic liquid (IL) electrolyte giving low volatility, high thermal stability, and high chemical stability enabling a higher operating voltage. High silicon reactivity necessitates passivation of the Si surface. A low temperature (120 °C) wet oxidation process provides a highly dense, ultra-thin (~1.4 nm) protective layer that extends the operating voltage and yields a high energy and power density, bringing the SiNWA electrode within the range of ECs. An alternative coating of metal oxide (TiO$_2$) provides further performance improvement, and with energy and power densities of 0.9 and 2228 W·kg$^{-1}$ respectively, places the developed SiNWA electrode towards the frontier of EC devices, as per the Ragone plot. Intermittent presence of apparent faradaic peaks observable on the cyclic voltammetry (CV) plots of SiNWA electrodes was analysed and attributed to the presence of deep level traps (DLTs) as a result of residual Ag from the MACE process. Multiple post-etch doping steps to degenerately dope the surface – pinning the Fermi level below the Si valence band – were found to mitigate the effect of the DLTs, improving the capacitive character and cycling stability of the electrodes.
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Perhaps the most important acknowledgements for this project go to Lu Qiao and Foivia Konstantinou, the MRes students under the same joint supervision who were my partners in carrying out this project. The dedication, enthusiasm, contributions and friendship they brought to this endeavour were invaluable; I could not have asked for better collaborators to work with on this project.

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# TABLE OF CONTENTS

Glossary of Acronyms ........................................................................................................................................... 10

List of Figures and Tables ........................................................................................................................................ 11

1. Introduction ......................................................................................................................................................... 16

2. Background .......................................................................................................................................................... 20
   2.1. Electrochemical capacitors .......................................................................................................................... 20
       2.1.1. Electrical Energy Storage ....................................................................................................................... 20
       2.1.2. Capacitance ........................................................................................................................................... 21
       2.1.3. The Electric Double Layer ..................................................................................................................... 22
       2.1.4. Pseudocapacitance ............................................................................................................................... 24
       2.1.5. Comparisons ........................................................................................................................................ 25
   2.2. Silicon Nanowire Array (SiNWA) ................................................................................................................ 26
       2.2.1. Methods .............................................................................................................................................. 27
       2.2.2. Applications ......................................................................................................................................... 28
       2.2.3. Metal-Assisted Chemical Etching (MACE) [48] .................................................................................. 29
   2.3. Liquid Electrolytes for ECs .......................................................................................................................... 31
       2.3.1. Aqueous and Organic Electrolytes ........................................................................................................ 31
       2.3.2. Ionic Liquids ......................................................................................................................................... 32

3. Literature Review: Electrochemical Capacitor Electrodes .................................................................................. 34
   3.1. Double Layer Capacitance .......................................................................................................................... 34
   3.2. Pseudocapacitance ....................................................................................................................................... 37
   3.3. Si-based Electrodes ...................................................................................................................................... 38

4. Experimental Methodology ................................................................................................................................ 41
   4.1. Fabrication .................................................................................................................................................... 41
       4.1.1. Metal-Assisted Chemical Etching (MACE) ........................................................................................... 41
       4.1.2. Spin-On Doping (SOD) ......................................................................................................................... 43
       4.1.3. Nitric Acid Oxidation of Silicon (NAOS) ............................................................................................ 43
4.1.4. Contact Formation ................................................................. 44
4.1.5. Materials .............................................................................. 45
4.2. Characterisation ........................................................................ 45
  4.2.1. Three Electrode Half-Cell .................................................... 46
  4.2.2. Cyclic Voltammetry (CV) ..................................................... 48
  4.2.3. Electrical Impedance Spectroscopy (EIS) ............................. 49
  4.2.4. Chronopotentiometry (CP) .................................................. 52
5. Electrode Development .................................................................. 54
  5.1. Nanostructuration with SiNWA .............................................. 54
  5.2. Introducing Spin-On Doping (SOD) ......................................... 57
  5.3. Initial Surface Passivations ..................................................... 61
    5.3.1. Fluorocarbon Polymer Deposition .................................... 62
    5.3.2. Electrochemical Oxidation ............................................... 65
  5.4. Nitric Acid Oxidation of Silicon (NAOS) ................................... 69
  5.5. TiO$_2$ coatings on SiNWA ..................................................... 75
    5.5.1. Fabrication of TiO$_2$ coatings on SiNWA ......................... 75
    5.5.2. Results and Analysis ....................................................... 79
6. Further Analyses .......................................................................... 81
  6.1. Investigating Additional Parameters ...................................... 81
    6.1.1. Effects of Varied SODs ..................................................... 81
    6.1.2. Effect of Varied Oxidation Temperatures .......................... 88
    6.1.3. Effect of Nanostructuration ............................................. 89
    6.1.4. Effect of Alternative Oxidation ....................................... 91
    6.1.5. Effect of Electrolyte ....................................................... 94
  6.2. Analysing and Identifying Redox Peaks .................................. 96
    6.2.1. Analysis of Potential Causes ........................................... 96
    6.2.2. Low Frequency Noise Analysis ...................................... 98
    6.2.3. Implications of Redox Peaks on Capacitive Performance ...... 101
<table>
<thead>
<tr>
<th>Acronym</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>ACN</td>
<td>Acetonitrile</td>
</tr>
<tr>
<td>CNT</td>
<td>Carbon Nanotube</td>
</tr>
<tr>
<td>CP</td>
<td>Chronopotentiometry</td>
</tr>
<tr>
<td>CV</td>
<td>Cyclic Voltammetry</td>
</tr>
<tr>
<td>CVD</td>
<td>Chemical Vapour Deposition</td>
</tr>
<tr>
<td>EDLC</td>
<td>Electric Double Layer Capacitor</td>
</tr>
<tr>
<td>EIS</td>
<td>Electrical Impedance Spectroscopy</td>
</tr>
<tr>
<td>EW</td>
<td>Electrochemical Window</td>
</tr>
<tr>
<td>GCD</td>
<td>Galvanostatic Charge/Discharge</td>
</tr>
<tr>
<td>IL</td>
<td>Ionic Liquid</td>
</tr>
<tr>
<td>MACE</td>
<td>Metal-assisted Chemical Etching</td>
</tr>
<tr>
<td>NAOS</td>
<td>Nitric Acid Oxidation of Silicon</td>
</tr>
<tr>
<td>NW</td>
<td>Nanowire</td>
</tr>
<tr>
<td>NWA</td>
<td>Nanowire Array</td>
</tr>
<tr>
<td>PC</td>
<td>Propylene Carbonate</td>
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<tr>
<td>PMMA</td>
<td>Poly(methyl methacrylate)</td>
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<tr>
<td>PTFE</td>
<td>Polytetrafluoroethylene</td>
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<tr>
<td>rGO</td>
<td>Reduced Graphene Oxide</td>
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<tr>
<td>RTA</td>
<td>Rapid Thermal Annealer</td>
</tr>
<tr>
<td>RTIL</td>
<td>Room Temperature Ionic Liquid</td>
</tr>
<tr>
<td>RTO</td>
<td>Rapid Thermal Oxidation</td>
</tr>
<tr>
<td>SEM</td>
<td>Scanning Electron Microscopy</td>
</tr>
<tr>
<td>SiNW</td>
<td>Silicon Nanowire</td>
</tr>
<tr>
<td>SiNWA</td>
<td>Silicon Nanowire Array</td>
</tr>
<tr>
<td>SOD</td>
<td>Spin-On Doping</td>
</tr>
<tr>
<td>VLS</td>
<td>Vapour-Liquid-Solid</td>
</tr>
</tbody>
</table>
# LIST OF FIGURES AND TABLES

## Figures

<table>
<thead>
<tr>
<th>Figure</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Figure 1.1</td>
<td>Ragone plot showing a range of portable electrical energy storage mechanisms, contrasting energy density against power density [10].</td>
<td>17</td>
</tr>
<tr>
<td>Figure 2.1</td>
<td>Schematic illustrations and corresponding potential curves versus distance from the surface of (a) Helmholtz model, (b) Gouy–Chapman model, and (c) Stern model (Image and caption from [33]).</td>
<td>23</td>
</tr>
<tr>
<td>Figure 2.2</td>
<td>Double layer capacitor (distance based on [27]).</td>
<td>24</td>
</tr>
<tr>
<td>Figure 2.3</td>
<td>Comparison of the mechanisms of double layer capacitance (left) and pseudocapacitance (right) [36].</td>
<td>25</td>
</tr>
<tr>
<td>Figure 2.4</td>
<td>RIE etched Si pillars of 280 nm diameter [49].</td>
<td>27</td>
</tr>
<tr>
<td>Figure 2.5</td>
<td>VLS-CVD growth of Si nanowires [56].</td>
<td>28</td>
</tr>
<tr>
<td>Figure 2.6</td>
<td>MACE etch process [65]. Process shows 1) Preferential reduction of oxidant at the metal surface, 2) Holes generated from reduction diffuse through the metal into toward the metal interface with the Si substrate, 3) Injected holes into Si cause oxidation of the Si at the Si-metal interface, with the oxide dissolved by HF, 4) Increased hole concentration at the Si-metal interface results in faster oxidation and dissolution by HF, i.e. etching, and 5) If hole injection rate exceeds its consumption rate, holes may diffuse to other areas of the substrate, which may result in things such as sidewall etching and pore formation.</td>
<td>30</td>
</tr>
<tr>
<td>Figure 2.7</td>
<td>Electrochemical potentials of Si substrate and oxidative agents [48].</td>
<td>31</td>
</tr>
<tr>
<td>Figure 3.1</td>
<td>Visualisation demonstrating that electrosorption of ions is only possible with the pore size being at least equal to the bare ion size, and that larger pores can adsorb multiple ions [82].</td>
<td>35</td>
</tr>
<tr>
<td>Figure 3.2</td>
<td>Visualisation of 2D graphene as a building block for 0D buckyballs (left), 1D nanotubes (middle) or 3D graphite (right) [89]</td>
<td>36</td>
</tr>
<tr>
<td>Figure 3.3</td>
<td>Non-rectangular cyclic voltammograms of Co and Ni based electrodes (left) contrasted with the quasi-rectangular capacitor-like CV of a pseudocapacitive MnO2 electrode [35].</td>
<td>38</td>
</tr>
<tr>
<td>Figure 3.4</td>
<td>CVD grown SiNWs at different NW lengths of a) 5, b) 10 and c) 20 µm. Gold catalyst tip observed in inset of a) [120].</td>
<td>39</td>
</tr>
<tr>
<td>Figure 4.1</td>
<td>SEM image of a MACE etched SiNW [4].</td>
<td>41</td>
</tr>
<tr>
<td>Figure 4.2</td>
<td>Structural formula of the ions comprising the IL, with the [Bmim]+ cation (left) and [NTf2]− anion (right) [135].</td>
<td>46</td>
</tr>
<tr>
<td>Figure 4.3</td>
<td>Diagram (a) and photograph (b) of the electrochemical measurement cell [142].</td>
<td>47</td>
</tr>
<tr>
<td>Figure 4.4</td>
<td>Three electrode electrochemical measurement cell, showing potential being monitored between reference (RE) and working (WE) electrode, with the power supply driven and current measured between the working and counter (CE) electrode.</td>
<td></td>
</tr>
<tr>
<td>Figure 4.5</td>
<td>Determination of electrochemical window (EW) and current (i) for CV measurement of capacitive quasi-rectangular shapes (a) and with redox peaks (b) [142].</td>
<td></td>
</tr>
<tr>
<td>Figure 4.6</td>
<td>Current vs scan rate for CV measurements. The linear gradient of the graph is fitted to extract a value of capacitance [3].</td>
<td></td>
</tr>
<tr>
<td>Figure 4.7</td>
<td>Equivalent RC series (left) representing double layer capacitance ($C_{dl}$) and solution resistance ($R_s$), along with its Nyquist plot (right) from EIS measurements. Real impedance intercept is equal to $R_s$ with complex impedance (from $C_{dl}$) increasing with lower frequencies.</td>
<td></td>
</tr>
<tr>
<td>Figure 4.8</td>
<td>Simplified Randles circuit (left) and its associated Nyquist plot (right) from EIS. Polarisation resistance ($R_p$) is introduced in addition to the solution resistance ($R_s$) and double layer capacitance ($C_{dl}$).</td>
<td></td>
</tr>
<tr>
<td>Figure 4.9</td>
<td>Modified Randles circuit to model our electrode-electrolyte system, with contact resistance ($R_c$) and capacitance ($C_c$) introduced to model its effect and enable better circuit fitting.</td>
<td></td>
</tr>
<tr>
<td>Figure 4.10</td>
<td>Chronopotentiometry trace, and determination of values of capacitance, energy and power from it.</td>
<td></td>
</tr>
<tr>
<td>Figure 5.1</td>
<td>Si electrode samples with ~100 nm Al back contacts. SiNWA (left) and the control, bulk Si (right).</td>
<td></td>
</tr>
<tr>
<td>Figure 5.2</td>
<td>CV measurements with $\nu = 50$ mV/s of n-type (top) and p-type (bottom) SiNWA (red) and bulk Si (black) samples.</td>
<td></td>
</tr>
<tr>
<td>Figure 5.3</td>
<td>Profile of doping concentrations of phosphorus dopant with boron doped Si substrates (bulk, pyramid, NWA, and pyramid-NWA hybrid) after an SOD step with similar processing, as simulated with Sentaurus [55].</td>
<td></td>
</tr>
<tr>
<td>Figure 5.4</td>
<td>CV measurements with $\nu = 50$ mV/s of n-type (top) and p-type (bottom) SiNWA (black) and SOD treated SiNWA (red) samples.</td>
<td></td>
</tr>
<tr>
<td>Figure 5.5</td>
<td>CV measurements with $\nu = 50$ mV/s of n-type (top) and p-type (bottom) SOD treated SiNWA samples with thin (red), thick (blue) and no (black) fluorocarbon polymer films deposited.</td>
<td></td>
</tr>
<tr>
<td>Figure 5.6</td>
<td>CV scanning of 20 cycles of marginally increased anodic potentials at ~1.2 V for electrochemical oxidation of SOD treated SiNWA samples.</td>
<td></td>
</tr>
<tr>
<td>Figure 5.7</td>
<td>CV measurements with $\nu = 50$ mV/s of n-type (top) and p-type (bottom) SOD treated SiNWA samples with (red) and without (black) electrochemical oxodisation.</td>
<td></td>
</tr>
<tr>
<td>Figure 5.8</td>
<td>CV measurements with $\nu = 50$ mV/s of n-type (top) and p-type (bottom) SOD treated SiNWA samples without (black) and with nitric acid oxidation (NAOS) at 90 °C (red) and 120 °C (blue).</td>
<td></td>
</tr>
<tr>
<td>Figure 5.9</td>
<td>Zoomed-in Nyquist plots of actual (red) and fitted (blue) of best performing n-type (top left) and p-type (top right) SOD treated SiNWA samples with nitric acid oxidation (NAOS) with frequency ranging from 0.1 to 100k Hz. Fitting is carried out with equivalent circuit (bottom) showing series resistance ($R_s$), charge transfer resistance ($R_{CT}$), double layer capacitance ($C_{DL}$), and resistance and capacitance arising from the sample contact ($R_C$ and $C_C$).</td>
<td></td>
</tr>
<tr>
<td>Figure 5.10</td>
<td>GCD curves at 1 mA for the best performing n-type (black) and p-type (red) SOD treated SiNWA samples with nitric acid oxidation (NAOS).</td>
<td></td>
</tr>
<tr>
<td>Figure 5.11</td>
<td>SEM imaging of SiNWA samples coated with three TiO$_2$ processes of (a) TiCl$_4$ treatment, (b) 3x Ti-dip procedure and (c) autoclave. Inset of (a) shows a zoomed in portion highlighting TiO$_2$ particles amongst the broken NWs, whilst insets of (b) and (c) show top views of the TiO$_2$ nanoparticle and TiO$_2$ layer coverage respectively.</td>
<td></td>
</tr>
<tr>
<td>Figure 5.12</td>
<td>CV measurements at $v = 50$ mV/s of SiNWA electrodes coated with three TiO$_2$ coating processes of TiCl$_4$ treatment (black), 3x Ti-dip (red) and autoclave (blue).</td>
<td></td>
</tr>
<tr>
<td>Figure 6.1</td>
<td>CV measurements at $v = 50$ mV/s of SOD and 120 °C NAOS treated SiNWA electrodes, with the SOD dopant atom of boron (red), aluminium (blue) and gallium (green) in comparison with an equivalent control sample without SOD (black).</td>
<td></td>
</tr>
<tr>
<td>Figure 6.2</td>
<td>CV measurements at $v = 100$ mV/s of SOD and 90 °C NAOS treated SiNWA electrodes, with the SOD dopant atom of boron (red), aluminium (blue) and gallium (green) in comparison with an equivalent control sample without SOD (black).</td>
<td></td>
</tr>
<tr>
<td>Figure 6.3</td>
<td>CV measurements at $v = 100$ mV/s of 3x SOD applied and NAOS treated SiNWA electrodes, with the SOD dopant atom of boron (red), aluminium (blue) and gallium (green).</td>
<td></td>
</tr>
<tr>
<td>Figure 6.4</td>
<td>CV measurements at $v = 50$ mV/s of SiNWA electrodes with NAOS treatment at varied temperatures of room temperature (red), 90 °C (blue) and 120 °C (black).</td>
<td></td>
</tr>
<tr>
<td>Figure 6.5</td>
<td>CV measurements at $v = 100$ mV/s of SOD and 120 °C NAOS treated bulk Si electrodes, with the SOD dopant atom of boron (red), aluminium (blue) and gallium (green) in comparison with an equivalent control sample without SOD (black).</td>
<td></td>
</tr>
<tr>
<td>Figure 6.6</td>
<td>CV measurement at $v = 100$ mV/s of a 120 °C NAOS treated bulk Si electrode treated in the MACE etch bath without nucleated Ag.</td>
<td></td>
</tr>
<tr>
<td>Figure 6.7</td>
<td>CV measurements at $v = 100$ mV/s of SiNWA electrodes with varied oxidations of RTO (red) and NAOS treatment at 120 °C (black).</td>
<td></td>
</tr>
<tr>
<td>Figure 6.8</td>
<td>CV measurements at $v = 100$ mV/s of SiNWA electrodes with 2x RTO and oxide strip followed by 90 °C NAOS (red), 3x B SOD followed by 90 °C NAOS (blue) in comparison with NAOS treatment at 90 °C (black).</td>
<td></td>
</tr>
</tbody>
</table>
Figure 6.9  CV measurements at ν = 50 mV/s of a SiNWA electrode with NAOS treatment at 120 °C with 4 different electrolytes: an aqueous 0.5 M NaClO₄ solution (red), organic 0.5 M NaClO₄ in PC solution (blue), [Emim][HSO₄] ionic liquid (green) and [Bmim][NTf₂] ionic liquid (black).

Figure 6.10  Normalised current noise spectral density vs frequency (log-log) for the NWAs showing peaks (a) and degenerately doped NWAs with no peaks (b). Dashed lines give spectrum slopes of 2 and 0.9 for (a) and 1 for (b). Inset of (a) gives normalised current spectral noise multiplied by frequency, with the peak position determining the characteristic trap level’s lifetime of ~5 s [1].

Figure 6.11  Energy band diagram sketch for SiNWA with a) non-degenerate and b) degenerate doping. 1, 2 and 3 gives equilibrium, positive and negative bias respectively. a (acceptor) and d (donor) are the associated Ag related trap levels. Nₜ refers to trap density, with superscripts of T referring to a charge neutral donor trap either being filled with electrons (0) or empty (+) [1].

Figure 6.12  Capacitance retention over 3000 cycles for NAOS treated SiNWA electrodes with (red) and without (black) peaks. Retention percentage at the 3000th cycle is shown.

Figure 7.1  Ragone plot showing a range of portable electrical energy storage mechanisms, contrasting energy density against power density [10]. Placement of a B SOD and NAOS treated sample [3] (blue circle) as well as 3x Ti-dip coated sample [2] (red star) on the plot is shown.

Tables

<table>
<thead>
<tr>
<th>Table</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Table 2.1</td>
<td>Contrast of relative strengths and weaknesses of double layer and pseudocapacitance [41, 28, 29].</td>
<td>26</td>
</tr>
<tr>
<td>Table 2.2</td>
<td>Contrast of the relative strengths and weaknesses of electrochemical capacitors, as compared to conventional capacitors and rechargeable batteries [42].</td>
<td>26</td>
</tr>
<tr>
<td>Table 5.1</td>
<td>Current, Capacitance, and Electrochemical Window characteristics for n- and p- type SiNWA and bulk Si samples. Projected surface area of measurement cell is 2.8 cm².</td>
<td>57</td>
</tr>
<tr>
<td>Table 5.2</td>
<td>Current, Capacitance, and Electrochemical Window characteristics for n- and p- type SiNWA samples with and without SOD application. Projected surface area of measurement cell is 2.8 cm².</td>
<td>60</td>
</tr>
<tr>
<td>Table 5.3</td>
<td>Current, Capacitance, and Electrochemical Window characteristics for n- and p- type SiNWA samples with SOD application and fluorocarbon film deposition. Projected surface area of measurement cell is 2.8 cm².</td>
<td>64</td>
</tr>
<tr>
<td>Table 5.4</td>
<td>Current, Capacitance, and Electrochemical Window characteristics for n- and p- type SiNWA samples with SOD application and electrochemical oxidation. Projected surface area of measurement cell is 2.8 cm².</td>
<td>68</td>
</tr>
<tr>
<td>Table 5.5</td>
<td>Current, Capacitance, and Electrochemical Window characteristics for n- and p- type SiNWA samples with SOD application and nitric acid oxidation at two temperatures. Projected surface area of measurement cell is 2.8 cm$^2$.</td>
<td>72</td>
</tr>
<tr>
<td>Table 5.6</td>
<td>EWs and extracted capacitances of the SiNWA samples with TiO$_2$ coatings.</td>
<td>80</td>
</tr>
<tr>
<td>Table 6.1</td>
<td>EW and extracted areal capacitance measurements for SiNWA electrodes with single or no SOD treatments with various dopant atoms and NAOS coating at 120 °C.</td>
<td>83</td>
</tr>
<tr>
<td>Table 6.2</td>
<td>EW and extracted areal capacitance measurements for SiNWA electrodes with single or no SOD treatments with various dopant atoms and NAOS coating at 90 °C.</td>
<td>85</td>
</tr>
<tr>
<td>Table 6.3</td>
<td>Extracted areal capacitance measurements for repeat fabrications of SiNWA electrodes with single or no SOD treatments with various dopant atoms and NAOS coating at 90 °C.</td>
<td>86</td>
</tr>
<tr>
<td>Table 6.4</td>
<td>EW and extracted areal capacitance measurements for repeat fabrications of SiNWA electrodes with multiple SOD treatments with various dopant atoms and NAOS coating.</td>
<td>88</td>
</tr>
<tr>
<td>Table 6.5</td>
<td>EW and extracted areal capacitance measurements for SiNWA electrodes with NAOS treatment at varied temperatures.</td>
<td>89</td>
</tr>
<tr>
<td>Table 6.6</td>
<td>EW and extracted areal capacitance measurements for a SiNWA electrode with RTO.</td>
<td>93</td>
</tr>
<tr>
<td>Table 6.7</td>
<td>Extracted EW measurements for a 120 °C NAOS treated SiNWA electrode with various electrolytes (see Fig. 6.9).</td>
<td>96</td>
</tr>
<tr>
<td>Table 6.8</td>
<td>EW and extracted areal capacitance measurement for NAOS treated SiNWA electrodes with degenerate (multiple SOD) and non-degenerate (no post-etch SOD) doping.</td>
<td>101</td>
</tr>
</tbody>
</table>
1. INTRODUCTION

Global progress and our daily lives are being ever increasingly dominated by the use of energy in its electrical form. Our home and work life necessities, as well as entertainment, travel, healthcare, communications; nearly all aspects of our lives have become intertwined with the consumption of energy. More and more of it is being migrated from being powered by other traditional sources of energy towards some form of electrical power, as issues of environmental protection, efficiency, and portability become more relevant.

One of the key challenges of electrical energy use is in bridging the gap between production and utilisation, and within this, a particularly challenging one to address is the storage of energy in an appropriate form. On a larger scale, appropriate storage of electrical energy could lead to things like significant improvements in the use of renewable and sustainable forms of energy such as wind energy; this is currently limited due to the juxtaposition of the intermittency of wind and the need of balancing power generation and load [8]. On the application level with portable power, issues faced include that of achieving the right balance between the energy and power levels required for optimum usage. This is easily demonstrated with one of the most relevant examples of high-use portable electric power, electric vehicles. On the one hand, vehicles would require a high energy density, with more energy packed into less mass to provide range and efficiency. However, solutions for these often have limited power delivery, and with high instantaneous power also desirable (e.g. for acceleration, or even on the waste energy recovery side), a higher power density storage solution may be utilised alongside this.

The range of portable electrical power storage devices is well shown with the Ragone plot (Fig. 1.1), which plots the gravimetric densities of power against energy storage, as these two generally have an inverse relationship [9]. On it, we can see the well-known and established technologies of rechargeable batteries and capacitors. Capacitors are storage mechanisms that store energy electrostatically in the form of an electric field between two conductors sandwiching a non-conducting layer. Rechargeable batteries can store an increased amount of energy electrochemically, with reversible chemical reactions accumulating and releasing the energy. A comparison between the utility of the two could be imagined with “hare and tortoise” analogy: the capacitor is able to provide high amounts of power in short bursts, whilst the “slow and steady” battery is able to deliver a lower amount of power for significantly longer with its greater energy.
Figure 1.1 – Ragone plot showing a range of portable electrical energy storage mechanisms, contrasting energy density against power density [10].

Bridging the gap between these are electrochemical capacitors (ECs). They can be defined as a device that “stores electrical energy in the interface between an electrolyte and a solid electrode” [10]. It can be seen that they offer the advantage of providing a much greater energy density that conventional capacitor storage, whilst still retaining much of the higher power density seen with capacitors as compared to batteries. This works out in a way that they can be imagined as devices with capacity approaching that of batteries, but with the abilities to be charged in a much quicker time and provide higher power outputs, amongst other advantages such as increased cycle life and durability. These can make them an attractive alternative to the use of rechargeable batteries for portable power.

One of the key reasons that ECs are able to provide greater charge storage than conventional capacitors is the increased surface area of charge storage. With the relevant surface being the electrode-electrolyte interface, an electrode with a high specific active surface area accessible to the electrolyte can provide a significant power boost. As such, electrode materials have traditionally included high surface area carbon materials such as activated carbon [11], whilst recent advances have been looking more towards nanostructures such as nanowires [11, 12], nanotubes [11, 13] and nanoparticles [14] to provide this. The other main source of the boost in capacitance in contrast to
conventional capacitors, e.g. electrolytic capacitors, is the lack of a solid dielectric between electrode and electrolyte, thus minimising the distance between the opposing charge storing layers.

In terms of chemically inactive (non-faradaic) EC electrode materials, various forms of carbon have remained at the forefront of the technology. We propose the idea of silicon as an alternative material for ECs. Historically, silicon has suffered from a number of comparative disadvantages that have made it unsuitable for considerable consideration as a viable electrode material for high capacitance systems. These include: (1) A low specific surface area, despite a good true areal capacitance value of \( \sim 5 \mu \text{F} \cdot \text{cm}^{-2} \) [15], comparable to that of carbon [16], (2) poor chemical stability, with low breakdown voltages in aqueous environments [17], and (3) comparative high cost and difficulty of production. However, in the modern day, all three of these issues are ones that no longer apply or can be addressed effectively. Additionally, the use of silicon as an electrode may offer further advantages of its own.

Silicon is the second most abundant element in the earth’s crust after oxygen, accounting for more than the next 6 elements combined [18]. In our increasingly digitalised world, the demand and consumption of silicon has continued to increase, with a lot more scope for additional production and further reduction in the costs of doing so [19, 20, 21]. Furthermore, the silicon processing industry has progressed in leaps and bounds, with the drive for smaller and smaller device sizes expanding the scope and capacity of silicon processing. In terms of stability, whilst silicon does not fare well in aqueous media, non-aqueous electrolytes, good packaging and improvements in passivation pave the way for silicon’s use. In addition to being fairly stable in non-aqueous condition, silicon offers the advantages of high thermal stability – enabling it to be used in a wider range of temperatures and undergo high temperature processing techniques – and the potential of good integration with other silicon based devices, such as with CMOS technologies.

The aims and objectives of this project are, to:

- Investigate boosting capacitance by nanotexturing silicon to give a high specific surface area by fabrication and experimental measurements
- Devise a suitable Si-based electrode-electrolyte system with promising real-world application potential (e.g. high operating voltage, green credentials)
- Characterise the developed system to evaluate its capacitive device performance
- Tune fabrication of Si-based electrode to optimise this performance
- Achieve a system with performance characteristics in line with commercial supercapacitors
We propose an electrode material based on nanostructured silicon, in the form of a Silicon Nanowire Array (SiNWA) fabricated via metal-assisted chemical etching (MACE). The MACE technique applied to silicon allows to obtain a high density of high aspect ratio wires with nanoscopic diameter, thus providing a very substantial increase to the specific active surface area of silicon. In contrast to other methods of silicon nanowire fabrication, MACE has the advantage of being simple and low cost, without the necessity for any specialised equipment. Also, as a wet, solution based fabrication process, its production can be easily scaled.

Whilst silicon can be used in other non-aqueous media such as organic electrolytes, our investigations primarily focus on the use of room temperature ionic liquids (RTILs or just ILs) as our chosen electrolyte, with the IL [Bmim][NTf2] being the primary electrolyte used. As electrolytes, ILs offer certain advantages, such as having high thermal and chemical stability (i.e. lower reactivities with chosen electrode materials), low volatility and vapour pressure; they have also been classed as being “green solvents” as a result of aspects such as these [22]. Additionally, being completely composed of ions mean that ILs can offer a good ion concentration (a molarity of 3.4 M with [Bmim][NTf2]) to contribute to the capacitive charge layer.

The scope of this thesis shall cover the author’s investigation into the use of MACE fabricated SiNWA as a high capacitance electrode material. After some brief background about the mechanisms, research and experimentation, the journey starting from initial explorations into the feasibility of SiNWA as an electrode, continuing to successfully developing a comparable electrochemical capacitor, and finally looking at potential improvements and analyses of phenomenon involved shall be explored.
2. BACKGROUND

2.1. Electrochemical capacitors

The subject of investigation is high capacitance electrodes, for operation as electrochemical capacitors. In order to understand the mechanisms involved and its place in the spectrum of electrical energy storage solutions, a bit of background information is presented.

2.1.1. Electrical Energy Storage

Perhaps the greatest challenge to solving global energy problems and increasing the use of renewable and environmentally friendly ‘green’ energy is the issue of electrical energy storage [23]. The limitations involved in the storage of energy produced and used electrically has necessitated alternative forms of storage such as in water reservoirs as potential energy [24, 25, 23] or in molten salt as heat energy [26, 23]. However, these solutions are costly and large-scale, at the national or regional level of electricity distributions. A greater prevalence of energy storage at the smaller scale and application level would allow us to utilise our electrical energy better, with production not having to be carried out simultaneously with usage.

The realm of device mechanisms that store energy to be directly stored by and dispensed as electricity is shown well with a Ragone plot [27, 28] as in Fig 1.1. In terms of energy and power densities, electrochemical capacitors – also known by supercapacitors – occupy the region in between that of conventional capacitors and rechargeable batteries. They can attain significantly higher charge storage densities than conventional capacitors, whilst still retaining a lot of the higher power densities seen in capacitors and unachievable with battery technology.

This enables a different range of applications, where higher power discharge or faster charging than batteries with a greater amount of specific energy than conventional capacitors may be desired. A prime example of supercapacitor applications is in electric cars, with the supercapacitors being able to provide a greater instantaneous power boost than the batteries, useful for acceleration. With the focus on developing, and increasing prevalence, of small and low power devices, as well as the desire for convenience and rapidity in device charging, there is a good prospect of a greater appetite for electrochemical capacitor usage.

In terms of storage mechanism, electrochemical capacitors (ECs) can be further categorised into two, double layer capacitance, and pseudocapacitance [28, 29]. ECs can be operating with either mechanism, or in a hybrid form with both mechanisms involved; for example, with different mechanisms for the two electrodes. Double layer capacitance operates on a similar principle to that
of conventional capacitance, with charge being stored electrostatically. Pseudocapacitance is faradaic, and involves the occurrence of redox reactions between the electrode and electrolyte as a means of charge storage, thus being more similar to battery storage. Accordingly, double layer capacitors and pseudocapacitors would tend to occupy respective positions along the Ragone plot of being nearer conventional capacitors and rechargeable batteries respectively. Pseudocapacitors, due to their faradaic nature, tend to have a shorter cycle lifetime, be slower to charge and discharge and be capable of achieving higher capacitances than double layer capacitors.

2.1.2. Capacitance

Capacitance is the mechanism by which capacitors store charge, with an accumulation of electric charge of opposing polarities between two conductors forming an electric field between them. This capacitance (C) can be quantified in terms of the magnitude of charge stored on each conductor (Q) and the electric field between them (V) with Eq. 2.1.

Equation 2.1 – Capacitance as a function of charge stored in an electric field

\[ C = \frac{Q}{V} \]

With conventional capacitors, the two conductors are separated by a non-conducting layer, known as the dielectric (if not a vacuum). The device capacitance of an ideal conventional capacitor can be determined with its material parameters and knowledge of the dielectric material. This is easiest explained with the example of a simple parallel plate capacitor (Fig 2.1) separated by a dielectric material. With knowledge of the surface area in parallel (A), the thickness of the dielectric layer separating the plates by a distance (d), and the relative permittivity of the dielectric (\( \varepsilon_r \)), we can quantify the capacitance with Eq. 2.2, which includes the vacuum permittivity (\( \varepsilon_0 \)). The distance is assumed to be significantly smaller than the area, so that fringe field effects at the edges can be considered negligible.

Equation 2.2 – Capacitance of a capacitor in terms of device parameters of dimensions and permittivity

\[ C = \frac{\varepsilon_0 \varepsilon_r A}{d} \]

Eq. 2.2 can be imagined in terms of Eq. 2.1. A large surface area allows for a greater accumulation of charge, and with a constant electric field strength between the charges, the potential between them is proportional to the distance. An additional factor is introduced by the dielectric, as polarisation of charge within the dielectric can reduce the electric field within it, thus decreasing the field strength per unit charge and increasing the capacitance [30]. We therefore know that to achieve a high device
capacitance, we would want to achieve a high surface area and minimise the distance between the conductors. With the same separation distance, a dielectric material placed between them can also boost the capacitance compared to having vacuum or air.

Capacitor design attempts to take these into account. In order to improve specific capacitances (i.e. capacitance per unit mass or volume), different techniques are applied. With lower capacitances, all-solid capacitor types such as ceramic or film capacitors are used, with metal and ceramic/film layers alternate to act as conductor and dielectric. For higher capacitor values, electrolytic capacitors are often chosen. Electrolytic capacitors operate with only one metallic electrode. This electrode is thinly oxidised to form a dielectric layer, with an electrolyte in contact with this layer forming the other electrode. The thin oxide layer as dielectric reduces the effective capacitive distance, thus improving the capacitance per volume and cost, though at the expense of reduced stability and operating voltage. At the higher end of specific capacitance, we move onto electrochemical capacitors. These capacitors operate with an electrode in contact with an electrolyte; no solid dielectric separates the two.

2.1.3. The Electric Double Layer

The electrical double layer forms the basis for the more “classic” supercapacitor, with the terms Electrical Double Layer Capacitor (EDLC) sometimes being used synonymously with supercapacitors [27, 31]. It however applies, to the electrostatic, non-faradaic mechanism by which electrochemical capacitors store charge.

The electric double layer is formed when, in the absence of an intermediary dielectric or other insulative layer, charge is accumulated directly at the surface of an electrode material in contact with an electrolyte. The most well-known model to explain this phenomenon is perhaps the Helmholtz double layer [27], though the Gouy-Chapman model and the Stern modification to this [28] exist as theoretical explanations as well [32].
Figure 2.1 – Schematic illustrations and corresponding potential curves versus distance from the surface of (a) Helmholtz model, (b) Gouy–Chapman model, and (c) Stern model (Image and caption from [33]).

Regardless of the model used to describe the layer, the means by which double layer capacitance is able to achieve significantly greater magnitudes of capacitance than conventional capacitance is straightforwardly extracted from the equation for a conventional capacitive device (Eq 2.2). Without the intervening insulator layer, the effective capacitive distance reduces to that between the electrode surface charge and the effective distance of the ionic counter charge on the electrolyte side. In the simplest explanation, we can imagine this as the midpoint of the ion layer adsorbed to the electrode surface. As this is at the molecular or even atomic level, with the ions, the distance in most cases can be sub-nanoscopic with distances of <1 nm [31, 27]. With this being up to two orders of magnitude lower than capacitors with dielectrics of no more than a few nanometres, we can see how this enables a substantial capacitance boost.
In addition to having the distance reduced, the direct electrode-electrolyte environment allows for an additional level of mechanical freedom, with the electrolyte – especially one with high liquidity – able to mould to the electrode morphology. This allows for a greater surface area of a non-standard morphology to act as the electrode surface site for capacitance. It is for this reason that EDLCs utilise electrode materials with a high specific surface area. Perhaps the most classical and established of this is the use of activated carbon [34] with its specific surface area of $>1000 \text{ m}^2\cdot\text{g}^{-1}$ providing for specific capacitances of around $\sim100 \text{ F}\cdot\text{g}^{-1}$ [28].

Therefore, we can see that with the minimisation of distance between the capacitive conductors, a role played here by the electrode and electrolyte, along with the ability to utilise electrode materials of high specific surface area, we are able to obtain electrostatic capacitances of substantially increased specific values over conventional capacitance.

2.1.4. Pseudocapacitance

Pseudocapacitance is another mechanism of electrochemical capacitance, and in a sense, is more “electrochemical”. It is faradaic, involving the transfer of charge between electrode and electrolyte [35, 36, 37]. Therefore, in addition to and in contrast to double layer capacitance, pseudocapacitance involves chemical reactivity at the electrode-electrolyte interface as a means of charge storage.
An electrochemically active electrode material, in conjunction with a suitable electrolyte, can enhance electrical charge storage with electron transfer at the interface. The addition of the chemical storage component to the electrostatic one can offer a greater energy density than can normally be achieved with EDLCs [36, 37, 38]. Electrode materials utilised for pseudocapacitance include transition metal oxides such as Mn, and Ru oxides [28, 36, 37], as certain conductive polymers such as polyaniline (PANI) and polypyrrole (PPy) [39, 40, 37].

![Figure 2.3 – Comparison of the mechanisms of double layer capacitance (left) and pseudocapacitance (right) [36].](image)

2.1.5. Comparisons

2.1.5.1. Between Mechanisms

Within the realm of electrochemical capacitance, each mechanism has its own pros and cons in terms of utility. The lack of any redox activity in EDLCs mean that although they are able to store a relatively lower amount of energy, they are more stable and can operate quicker (thus providing greater current power density) than pseudocapacitors. The relative strengths and weaknesses between the two mechanisms is outlined in Table 2.1. It should be noted that capacitor devices can be designed with either mechanism, or even in a hybrid combination of double layer and pseudocapacitance.
Table 2.1 – Contrast of relative strengths and weaknesses of double layer and pseudocapacitance [41, 28, 29].

<table>
<thead>
<tr>
<th>Double Layer Capacitance</th>
<th>Aspect</th>
<th>Pseudocapacitance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lower. No faradaic charge storage 20-50 µF·cm⁻²</td>
<td>Capacitances</td>
<td>Higher due to faradaic charge storage 200-2000 µF·cm⁻²</td>
</tr>
<tr>
<td>Highly reversible</td>
<td>Charging/Discharging Stability</td>
<td>Quite reversible, but limited by intrinsic electrode-kinetic rate</td>
</tr>
<tr>
<td>Does not suffer from poorer cyclability due to faradaic reactions</td>
<td></td>
<td>Redox reactions can often cause poorer cycling stability</td>
</tr>
</tbody>
</table>

2.1.5.2. With Other Storage Technologies

The contrast of ECs with the portable electrical storage technologies on either side of on the Ragone plot (Fig 1.1) is similar to that between double layer and pseudo-capacitance. Compared to conventional capacitors, ECs are able to store a significantly larger energy density, whilst retaining a lot of the power density they are capable of supplying. This power density is notably larger than that of rechargeable batteries, enabling quick charge/discharge. These, and other relative differences are outlined in Table 2.2.

Table 2.2 – Contrast of the relative strengths and weaknesses of electrochemical capacitors, as compared to conventional capacitors and rechargeable batteries [42].

<table>
<thead>
<tr>
<th></th>
<th>Conventional Capacitor (Electrolytic)</th>
<th>Electrochemical Capacitor (Carbon-based)</th>
<th>Battery</th>
</tr>
</thead>
<tbody>
<tr>
<td>Energy Density (Wh·kg⁻¹)</td>
<td>&lt;0.1</td>
<td>1 – 10</td>
<td>10 – 100</td>
</tr>
<tr>
<td>Power Density (W·kg⁻¹)</td>
<td>&gt;&gt;10k</td>
<td>500 – 10k</td>
<td>&lt;1000</td>
</tr>
<tr>
<td>Cycle Life (no. cycles)</td>
<td>Infinite</td>
<td>&gt;500k</td>
<td>~1000</td>
</tr>
<tr>
<td>Charge/Discharge Time</td>
<td>10⁻⁶ – 10⁻³ seconds</td>
<td>minutes</td>
<td>hours</td>
</tr>
</tbody>
</table>

2.2. Silicon Nanowire Array (SiNWA)

Silicon nanowires (SiNWs) are formed of silicon that has been nanostructured to form high aspect ratio structures, with diameters in the nanoscale range. Nanowires have special characteristics compared to scaled up similar structures, with the nanoscopic nature of the wire diameter meaning that they can be modelled as one-dimensional structures [43, 44, 45, 46]. This enables them to have
different characteristics such as a reduced thermal conductivity [44], and allow one dimensional carrier transport [44, 46], which can be utilised in device designs such as the single electron transistor [47].

2.2.1. Methods

SiNWs can be fabricated by a number of different methods, with them being broadly categorised as being either “top down” or “bottom up” [48]. Top down methods involve the etching of silicon to form the nanostructures, whilst bottom up methods involve the growth of nanowires on a substrate.

Top down methods include both dry etching techniques such as reactive-ion etching (RIE, also known as plasma etching) [49, 50, 51, 52], and wet etch techniques such as metal-assisted chemical etching (MACE) [48, 53]. RIE etching of silicon involves forming a suitable mask on silicon, which can be done by means of techniques such as lithography [49, 52], or even by depositing nanoparticles which may or may not be pre-treated with the plasma [54] to form a suitable mask [50, 51]. Features of the RIE technique for SiNW formation include the etch process being anisotropic, in the direction of the electric field across which the plasma bombards the substrate. It also requires the use of a vacuum environment and special equipment to carry out. This could potentially lower production throughput, and could also affect issues such as the cost of production scaling, if the device were to be mass produced.

Figure 2.4 – RIE etched Si pillars of 280 nm diameter [49].

Wet etching of silicon can also be done with mask formation, such as with lithography and KOH etching [55]. MACE is a process that may or may not include mask formation [48], and as the chosen etch technique for this project, shall be expanded on in Section 2.2.3.

Bottom up techniques can more costly and harder to scale than top down methods, as they require the use of specialised equipment and conditions to fabricate. A well-known SiNW growth method is the vapour-liquid-solid (VLS) chemical vapour deposition (CVD) technique [56, 57]. The process works
by introducing a catalyst for Si growth onto a substrate; e.g. a Au-Si alloy. Introduction of a Si containing vapour causes the liquid to adsorb the vapour particles into it, and its catalytic nature enables it to act as a site for growth of crystallised Si at the interface between the liquid droplet and solid substrate. This enables a high quality of Si to be grown upwards beneath the droplet in the form of a wire.

Figure 2.5 – VLS-CVD growth of Si nanowires [56].

This technique also offers its own advantages over top down techniques. Greater control needed in diameter control and spacing can be offered, especially when wire diameters approach the limits of traditional lithography, as patterning and etching at the scale of ~10 nm no longer becomes as cost effective [58]. Also, the technique isn’t reliant on the condition of the substrate, whereas quality of the fabricated wires is entirely dependent on the initial substrate quality for top down techniques.

2.2.2. Applications

The nature of SiNWs make them useful for investigation in a number of applications. In addition to our application of high capacitance electrodes (see Section 3.3), these include utilisation of solar energy [59, 55, 60], generating electrical energy from heat [61, 62, 7], and sensing applications [63, 64]. Utility in solar applications include having an improved carrier collection efficiency due to shorter carrier length [60] as well as low reflectivity (better light trapping) [55]. The lower thermal conductivity of SiNWs compared to bulk Si allow them to maintain higher temperature gradients, thus making them a good candidate material for thermoelectric generation [61, 62, 7]. The high surface area to volume ratio of the SiNWs allows for a high intrinsic gain, giving high sensitivity for sensor applications such as biosensing [63], and infrared detection [64].
2.2.3. Metal-Assisted Chemical Etching (MACE) [48]

Metal-assisted chemical etching is a top-down method of fabrication that can yield a high density of crystalline Si nanowires. It is a method that is simple, low-cost and can be done simply in a chemical lab without any expensive or specialised equipment. MACE can also offer the advantage of better parameter control in terms of shape, doping and dimensions. The process being intrinsically anisotropic means that the wires can be in a uniform crystalline direction and orientation, even on non-level surfaces [55]. VLS growth of SiNWs can offer only circular wires, whilst with patterning, MACE can offer other shapes, and dimensions such as diameter and length are mainly only limited lithography and time, allowing a large range of diameters and tuneable length. Also, additional doping does not necessarily need to be done as the doping level can be chosen and controlled with the substrate. And, although MACE can result in the roughness of nanowires, the process causes fewer surface defects than other top-down processes such as RIE.

The key composition of the MACE process consists of the Si substrate, noble metal (e.g. Au, Ag, Pt) catalyst, HF etchant and an oxidant such as H$_2$O$_2$. The basis of the process is that the catalyst metal acts as a mask and a site for the reduction of the oxidative agent and subsequent oxidation and dissolution of the Si substrate. The sinking of the metal particles into the substrate leave the surrounding Si freestanding, which can be shaped in the form of SiNWs.

The process begins with the deposition of the noble metal particulate onto the Si surface. These can be via methods such as thermal evaporation, sputtering, spin coating or electroless deposition as used in this project. Evaporation and sputter coating processes carried out in vacuum are useful when careful patterning of the resulting wires is required. When no strict patterning is required, electroless deposition in solution can offer a simple method to obtain the wires, without any regularity in spacing and morphology. As this project looks primarily to increase the surface area, and patterning isn’t required, we employ the electroless method of deposition for the etch.

Electroless deposition as done in this project is carried out in a solution of HF and AgNO$_3$, with Ag being the noble metal to be deposited. A Si substrate in contact with this solution forms a galvanic cell, with the electrochemical energy level of the Ag$^+$/Ag redox system being more positive than the Fermi energy level of the Si substrate (Fig. 2.7). The Ag$^+$ ion is reduced at the surface forming elemental Ag. This reduction injects a hole into the Si surface, thus oxidising the Si atoms beneath the Ag particles and allowing the particles to sink into the substrate, forming the etch pit. Over time, the Ag particles grow into larger nuclei to be deposited, and as it sinks, charge transfer continues to preferentially occur at the etch site instead of nucleating on the sidewalls. Thus, these nuclei eventually grow into dendrites. The nanowire density and diameter can be tuned to a certain extent by varying the
concentrations of HF and AgNO₃, although the resulting nanowires shall still consist of a range of nanowires with centred around and average.

Figure 2.6 – MACE etch process [65]. Process shows 1) Preferential reduction of oxidant at the metal surface, 2) Holes generated from reduction diffuse through the metal into toward the metal interface with the Si substrate, 3) Injected holes into Si cause oxidation of the Si at the Si-metal interface, with the oxide dissolved by HF, 4) Increased hole concentration at the Si-metal interface results in faster oxidation and dissolution by HF, i.e. etching, and 5) If hole injection rate exceeds its consumption rate, holes may diffuse to other areas of the substrate, which may result in things such as sidewall etching and pore formation.

As there is dispute in the exact reactions involved and the pathways in which the Si atoms travel, I shall leave the reader to refer to that in [48]; a simple 3 reaction explanation fitting the process exists in [66]. The process (Fig 2.6) begins with the reduction of the oxidative agent at the site of the metal catalyst. This causes the holes generated from this reduction to be injected into the Si substrate at the metal-Si contact, resulting in the oxidation of Si. This enables the HF to dissolve the Si atoms beneath the metal; the metal sinks into the substrate as more dissolution of Si occurs. This process works well, even with highly doped Si substrates, as the electrochemical potential of H₂O₂ is significantly more positive than that of the Si valence band, and thus holes can be injected deep into the valence band of Si. One of the results of hole injection could be that, if the hole injection rate is greater than the consumption rate, this could result in the injected holes moving from beneath the metal to the sidewalls of the etch pit, which could cause porosity of the pit walls, which would be the walls of the SiNWs.
2.3. Liquid Electrolytes for ECs

The most commonly used and researched liquid electrolytes for ECs can be classified into three categories: aqueous electrolytes, organic electrolytes, and ionic liquids [28, 39, 67], with organic electrolytes being the most used [27, 28, 67]. Solid electrolytes such as gel polymer electrolytes are also investigated for ECs [39, 67], though shall not be expanded upon here. The role of the electrolyte is a significant one in the EC system, and plays a significant role in affecting the performance of the EC. This is most apparent in terms of its effect on the EW, due to the relative stabilities of the three types of electrolytes. As the energy equation for capacitance dictates, the factor of energy increase with an increase in the EW is exponential, with an exponent of 2.

2.3.1. Aqueous and Organic Electrolytes

Aqueous electrolytes – the most common being acid (H$_2$SO$_4$) and alkaline (KOH) solutions – have the advantages of being low cost and having high conductivities and low viscosities [39, 42]. The higher dielectric constant of aqueous electrolytes in comparison to non-aqueous ones [41], mean that higher values of specific capacitance can be achieved with the same electrode. This disparity can be significant, with values of 100-110 F·g$^{-1}$ and 180-200 F·g$^{-1}$ being seen for the same high surface area carbon electrodes in organic and aqueous media respectively [68, 69]. However, despite these advantages, the usage of aqueous electrolytes for ECs usually yields to organic electrolytes due to its low EW resulting in lower energy densities and operating voltages. The operating potential window of ECs employing aqueous electrolytes is limited by the decomposition of water by electrolysis to a value of 1.23 V [70, 39], though EWs achieved are typically lower at ~1 V [27, 28, 71].

Figure 2.7 – Standard potentials (with reference to standard hydrogen electrode) of Si valence and conduction band edges and various redox systems [48].
Organic electrolytes, with the absence of water and oxygen, allow us to reach higher operating voltages for ECs. The most common organic-based electrolytes are those with the organic solvents acetonitrile (ACN) and propylene carbonate (PC), with salts added for conduction [39, 67, 42, 72]. Operating voltages can reach 2.3-2.7 V for organic electrolytes, which provides the additional advantage of being able to boost the energy storage ability of the EC. However, in addition to being more expensive, the use of organic electrolytes with their significantly lower conductivities than aqueous electrolytes cause a comparative increase in resistance [27, 42]. This in turn means that whilst we may improve the operating voltage and energy, this may come at the cost of reduced power capability due to increased effective resistance, though again, this would be balanced by an increase in maximum power attainable with the square of the operating voltage as well.

2.3.2. Ionic Liquids

Room temperature ionic liquids (RTILs or ILs), are solvent-free liquids composed entirely of ions. ILs used as EC electrolytes can have comparative limitations compared to aqueous and organic electrolytes such as higher viscosity and a lower conductivity despite being composed completely of ions, and their higher cost, though this may reduce with wider prevalence and an increased scale of production [39]. Like the jump from aqueous to organic electrolytes, ILs also suffer from a comparatively lower specific capacitance, such as in [73], with values for a carbon-based electrode of \( \sim 75 \text{ F} \cdot \text{g}^{-1} \) for ILs as compared to \( \sim 200 \text{ and } \sim 120 \text{ F} \cdot \text{g}^{-1} \) for aqueous and organic electrolytes respectively.

Despite having a few comparative shortcomings, ILs also offer certain advantages over aqueous and organic electrolytes, particularly when certain application parameters are desired over others. The most notable one of this is in terms of the extended EW of ILs; ILs can extend the EW and thus operating voltage domain beyond 3 V [72, 67, 28, 74]. With voltage windows of \( \geq 4 \text{ V} \) with ECs being reported [75, 76, 77], this would enable a significant boost in energy storage over aqueous electrolytes with their EW limited to 1 V, even taking potentially lower specific capacitances into account. With a high temperature stability in addition to the high chemical stability [78, 76], this enables EDLC operation at higher temperatures \( \geq 60 \, ^\circ\text{C} \) [76, 28]. These reasons, along with a low vapour pressure, low toxicity and being non-flammable have ILs being touted as a “green” electrolyte as well [78]. This is in comparison to the high volatility, flammability and toxicity of organic electrolytes such as those with an ACN solvent [75, 39, 67].

With these factors in mind, the choice of an IL electrolyte for our Si-based electrode seems appropriate. The high chemical stability counteracts the high reactivity of Si, particularly compared to aqueous environments, and the wide EW allows for applications requiring higher energy density or a larger operating voltage. Additionally, the high thermal stability enables the use of high temperature...
applications which Si is suited for. Green credentials such as low toxicity and volatility also promote
the good applicability of ILs, and an expansion in the production and utility of ILs in the future may
mitigate the issue of relatively higher cost as well.
3. LITERATURE REVIEW: ELECTROCHEMICAL CAPACITOR ELECTRODES

With looking into the use of SiNWAs as EC electrodes, it would be useful for us to look into some of the current research conducted on EC electrode development, particularly towards the use of novel and nanoscale materials to further enhance performance. In this chapter, we shall have a brief look at some of these. This shall begin with looking into double layer capacitor electrodes, primarily of more recent carbon-based materials, followed by looking into electrochemically active pseudocapacitive materials explored and their impact on the capacitive ability of the electrodes. Finally, as this research primarily focuses on developing a Si-based electrode, we shall look into the current status of Si-based electrodes for ECs.

3.1. Double Layer Capacitance

Double layer capacitors rely heavily on electrode materials that can provide a very high specific surface area (SSA) to boost their capacitance far beyond that achievable with conventional capacitors. With the capacitance being electrostatic, and thus the energy storage not being boosted by chemically active means, finding a high surface area is essential to achieving a high energy storage density. Additional important features for an electrode include having a high electrical conductivity and good electrochemical stability with a given electrolyte [28]. As such, various forms of carbon with high specific surface areas, including activated carbon [28, 79], carbon nanotubes [28, 79] and graphene [79], are the primary materials used as and explored for EDLCs.

Of these, activated carbon is the most widely used current EDLC material [28, 79, 34]. This is due to its relatively low cost, coupled with the very high SSA that it provides. Activated carbon can be derived from a number of low cost raw materials, such as coconut shells, animal waste, wood and coal [28, 80]. The process of activation of carbon results in the development of a porous network within the carbon bulk, with a wide range of pore diameters, including larger “macro” pores of >50 nm, down to “micro” pores of <2 nm [28], of which smaller “ultramicro” pores may be too small for good access of the electrolyte ions, which may depend on the ion size [81, 82, 28].
Figure 3.1 – Visualisation demonstrating that electrosorption of ions is only possible with the pore size being at least equal to the bare ion size, and that larger pores can adsorb multiple ions [82].

The processes of the activation of carbon can be classed into two main methods, i.e. physical and chemical activation [83]. Physical activation involves the pyrolysis of the carbon containing precursor, followed by gasification (with steam, noble gases or carbon dioxide etc) for pore development [84, 85], whilst chemical activation [81] involves impregnation of the material with reagents (which may be an acid, base or salt) that aid the activation process. Advantages of chemical activation include a lower pyrolysis temperature and quicker activation [86].

Activating carbon develops material with a SSA of around 1000-2000 m$^2$·g$^{-1}$. This can lead to specific capacitance values in excess of 100 F·g$^{-1}$ [28, 80, 34]. A SSA of 2000 m$^2$·g$^{-1}$ and capacitance of 100 F·g$^{-1}$ gives an areal capacitance of 5 µF·cm$^{-2}$, which is consistent with the value we expect for Si bulk surfaces (see Section 3.3) as well. Higher capacitances can be achieved with aqueous as opposed to organic electrolytes, though at the cost of a reduced EW due to water decomposition [28]. There are a few disadvantages of the use of activated carbon as an electrode. These include having a non-ideal pore size distribution and dispersion, with pores having the potential of being too small for ions or too large to be able to provide a significant SSA advantage, with both limiting the attainment of high capacitances. With the limitations of electrolyte ion accessibility and poor electrical conductivity of the highly porous structure with its small particle and pore sizes, a high internal resistance can cause limitations on the achievable power density as well [79, 87, 28].
More recently, alternative carbon structures/materials have been investigated as potentially improved alternatives to activated carbon, including carbon nanotubes (CNTs) and graphene [79]. In addition to the high SSA, they can provide additional advantages such as better electrolyte accessibility and electrical properties. The single-atom thick, dense carbon lattice of graphene can be visualised as the basic building block of many carbon structures such CNTs and graphite; a single-walled nanotube can be imagined as a rolled-up graphene sheet (Fig 3.2).

Figure 3.2 – Visualisation of 2D graphene as a building block for 0D buckyballs (left), 1D nanotubes (middle) or 3D graphite (right) [88].

CNTs have been extensively researched into as high capacitance electrodes [79, 89, 90, 91], with capacitances of similar values to activated carbon. A key improvement as compared to activated carbon of CNTs is that the high electrical conductivity results in achieving higher power densities (kWs per kg) whilst still maintaining a high energy density with its high SSA. Issues faced with the application of CNTs however, include high contact resistances with a current carrying contact, and the need for optimising geometry for better electrolyte access to the surface. Improved performance can be realised with geometries such as with vertically aligned CNTs [92, 93, 94], fabricated by a controlled
CVD process, as opposed to random entanglement of the CNTs restricting the electrolyte accessible SSA. However, industrial scaling of well-arranged CNTs remains an obstacle [79].

An even more recent material of interest for energy storage with both batteries and supercapacitors has been graphene. The nature of graphene makes it a very attractive material of investigation for ECs, with the single atom thickness of the graphene lattice layer making it very light for a very high surface area; it has a very high SSA of 2630 m²·g⁻¹ [95, 73], giving it a very high theoretical specific capacitance of 550 F·g⁻¹ [96]. Along with the high surface area, other advantages it offers in comparison to other carbon materials is an exceptionally high electrical conductivity and high mechanical and thermal stability [96, 97, 98].

Whilst not yielding pristine graphene, a means of obtaining cost effective graphene material is the reduction of graphene oxide, which can be derived inexpensively and with high yield from a low-cost graphite raw material [99]. The resulting product is often known as reduced graphene oxide (rGO) as it only partly recovers graphene, and exhibits more defects than pristine graphene [99, 100]. Capacitances derived from rGO have demonstrated capacitances of between 99 to 205 F·g⁻¹ [101, 102, 73]. The capacitance obtained can be affected by the choice of electrolyte, with capacitance values ranging from ~200, ~120, and ~75 F·g⁻¹ for aqueous, organic, and ionic liquid electrolytes respectively [73]. With the high SSA and electrical conductivity, they can also attain excellent power and energy densities, exemplified by a reported rGO-based electrode in aqueous electrolyte achieving power and energy densities of 10 kW·kg⁻¹ and 28.5 Wh·kg⁻¹ respectively [101].

3.2. Pseudocapacitance

In addition to the primarily carbon-based nanoscale materials used for double layer capacitance, EC materials include pseudocapacitive materials that add redox storage onto the electrostatic double layer storage. These are primarily in the form of transition metal oxides/hydroxides [103], as well as conducting polymers [40]. These materials can be employed in a number of ways, such as being deposited as nanoparticles on a carbon material framework to add onto the capacitance [104, 105, 106], in hybrid conjunction with a carbon electrode [107] or other pseudocapacitive electrode [108], and being developed as nanostructures such as nanowires/nanotubes [109, 110, 108], nanosheets [111], and nanoparticles [104, 105, 106] to improve the capacitive performance.

The additional element of chemical charge storage through fast redox reactions occurring at the electrode-electrolyte interface mean that by mass, pseudocapacitive electrodes can achieve higher capacitances than their double layer counterparts. This can be up to an order higher, with values for
nanostructured Co hydroxides being reported to reach up to 1920 F·g⁻¹ [112] and 2800 F·g⁻¹ [113], and conducting polymers reported to be reaching 950 F·g⁻¹ [114].

![Graph showing cyclic voltammograms of Co and Ni based electrodes contrasted with the quasi-rectangular capacitor-like CV of a pseudocapacitive MnO₂ electrode.](image)

*Figure 3.3 – Non-rectangular cyclic voltammograms of Co and Ni based electrodes (left) contrasted with the quasi-rectangular capacitor-like CV of a pseudocapacitive MnO₂ electrode [35].*

Whilst a wide range of metal oxides/hydroxides and conducting polymers are termed under the umbrella of EC and supercapacitor electrodes as being pseudocapacitive, they often exhibit non-standard CV and charge/discharge shapes compared to that expected of capacitors [114, 112, 113, 104, 115], as a result of the redox charge storage in addition to any electrostatic charge storage. This is in contrast to the more classical pseudocapacitor materials such as MnO₂ [107], Mn₃O₄ [116], and RuO₂ [105], which exhibit the quasi-rectangular shape as expected of EDLCs and other capacitors. Whilst the high energy and, more significantly, power densities of the electrode materials exhibiting non-standard CV and charge/discharge behaviour place them more within the EC spectrum as opposed to the battery spectrum, it has been proposed [35] that they be termed otherwise as faradaic but not “pseudo-” capacitive electrodes. This is as they exhibit a signature which is more battery like, and as such, pseudocapacitance should be reserved for those electrodes with a more capacitor-like character.

### 3.3. Si-based Electrodes

Perhaps the most relevant review for this project is the state of other investigations into the use of Si as a basis for capacitor electrodes. Whilst some of this is in the form of non-NW structures of Si being used as a substrate or frame for other capacitor materials such as pseudocapacitive ones [117, 118], we are particularly interested in high aspect ratio Si structures such as the SiNWAs used for this project. This includes, as we started with in the project, bare SiNWs investigated as electrodes, as well as coatings and modifications employed.
The investigations into the use of bare SiNWs as EC electrodes are very recent ones, with published initial investigations being seen in 2012 [15], a year before the beginning of this project. These investigations [15, 119, 120] however, include the use of a bottom-up CVD technique with specialised vacuum equipment as opposed to our top-down MACE etch (see Section 2.2.3).

Bare SiNWs of length ~10 µm, diameter of ~100 nm, a high dopant concentration of $4 \cdot 10^{19}$ and density of $\sim 10^8$ NWs·cm$^{-2}$ are investigated as electrodes in [15] with an organic electrolyte, using both CV and GCD measurement techniques. Values of 34 and 46 µF·cm$^{-2}$ are extracted from CV curves for n- and p-type respectively, with the corresponding values extracted from GCD being 5.5 and 6.5 µF·cm$^{-2}$ respectively. Both of these, however, demonstrate an increase with SiNWs of ~7-fold compared to bulk Si. Despite the use of an organic electrolyte, the EWs of the electrodes are limited to ≤1 V, with increased potentials resulting in surface modification of Si.

![Figure 3.4](image)

**Figure 3.4** – CVD grown SiNWs at different NW lengths of a) 5, b) 10 and c) 20 µm. Gold catalyst tip observed in inset of a) [119].

Improvements observed with changes in parameters are explored in [119] and [120], in terms of NW length and density, respectively. Samples in [119] are evaluated using the GCD method, comparable to that in [15], with NW lengths of 5, 10 and 20 µm. Improvements in areal capacitance are observed with increasing NW lengths; the capacitance doubles with length doubling from 5 to 10 µm. Whilst an improvement is observed by further NW growth to a 20 µm length, it is with a diminishing return of 1.35 times the 10 µm. This could be due to longer wires produced being without regularity (Fig 3.4), and constricting full access to the increased surface area obtained. The value achieved reached ~10-fold of bulk capacitance. In [120], the parameter looked at is the density of NWs. Alternative templating for SiNW growth leads to a higher NW density of $8 \cdot 10^9$ NWs·cm$^{-2}$, which results in a further ~7-fold areal capacitance increase, from 5.2 to 36.7 µF·cm$^{-2}$.

With the EW of the electrodes being limited to ~1 V with bare Si, the full potential of a high energy density attained with the high surface area of the SiNWs cannot be realised. For that reason, investigations have been carried out with coatings on the NWs that would enable them to achieve
better electrochemical stability. Coatings to improve electrode stability with nanostructures Si include Si oxide [121], SiC [17], diamond [122] and graphene [123]. SiC coatings were investigated as a response to corrosion of SiNWs in aqueous electrolytes with some success, yielding capacitances of up to 1.7 mF·cm⁻² with SiC coated SiNWs of ~32 µm length [17]. A graphene coating on porous Si was shown to double the EW from 1.3 to 2.7 V, and increase energy density by a factor of >10 [123]. The use of an ionic liquid electrolyte in addition to coatings [122, 121] has demonstrated EWs of up to 4V. Boron-doped diamond coated on SiNWs showed capacitances of up to 105 µF·cm⁻² [122]. Electrochemically performed oxidation of SiNWs in ionic liquid (EMI-TFSI) extended the usually seen ~1 V of Si electrodes in both aqueous and organic electrolytes up to 4 V [121].

In addition to coatings to improve stability, coatings of pseudocapacitive materials have been deposited on Si structure electrodes, including SiNWs, in order to boost capacitance [118, 124, 125]. The high surface area and good conductivity of the Si electrode frame combines with the faradaic charge storage to boost specific capacitance values. This includes SiNWs coated with NiO [124] and MnO₂ [125]. Though tested in a limited EW, NiO coatings on SiNWs demonstrated high specific capacitances of up to 787.5 F·g⁻¹, with the SiNW frame yielding low internal electrode resistance to supplement the high capacitance of NiO. MnO₂ nanoflakes deposited on SiNWs in conjunction with an IL electrolyte yielded areal capacitances of 13 mF·cm⁻² (~51 F·g⁻¹), with the high EW of 2.2 V leading to a high energy density achieved.
4. EXPERIMENTAL METHODOLOGY

As a primarily lab-based research project, the methodology involved primarily consists of experimental techniques. In this project, this can be broadly split into two main phases: 1) the fabrication of the electrode, and 2) the characterisation techniques employed to evaluate the performance of the fabricated electrode.

4.1. Fabrication

4.1.1. Metal-Assisted Chemical Etching (MACE)

As highlighted in Section 2.2, SiNWs can be fabricated with a variety of techniques. The method we use for the fabrication of our SiNWA electrodes is a top-down, wet chemical etch known as metal-assisted chemical etching (MACE). The metal of choice for our process is Ag, introduced in the form of AgNO$_3$ to be deposited by electroless deposition onto the sample surface. Whilst single-step etches can also produce nanowires [55], we use a two-step etch, with the first step being the nucleation of the Ag from a solution of AgNO$_3$ and HF onto the sample surface (see Section 2.2.3.). This is followed up by an etch solution containing an oxidative agent (H$_2$O$_2$) and HF to carry out an etch process at a faster etch rate in conjunction with the Ag particles deposited from the nucleation step.

![Figure 4.1 – SEM image of a MACE etched SiNWA [4].](image)

The two-step etch process used in this process was especially developed in-house for highly doped (0.01- 0.02 Ω·cm) Si wafers by Bin Xu [62]. SiNWA etch recipes have to be tweaked in accordance with the doping density of the substrate, as the morphology of wires are dependent on solution concentrations. Higher concentrations of H$_2$O$_2$ used with highly doped silicon results in porosity of the nanowires [126]; the defects increasing present in the presence of more doping atoms offer a site for re-nucleation of the Ag particles, which results in pore forming lateral etching, giving us porous nanowire sidewalls. Other factors such as the amount of Ag nucleated on the surface during
electroless deposition and the etch rate also vary with the doping density of the initial substrate. In order to achieve highly crystalline nanowires with good mechanical strength a lower concentration of the oxidant H₂O₂ has to be used – giving a slow etch rate – with high doping concentrations.

Samples are cleaved – primarily into 2 cm by 2 cm squares – from the Si wafers using a diamond-tipped pen to create a groove before applying pressure to cleave the sample along the crystalline direction. After cleaving, and immediately before the etch process, a thorough cleaning of the nanowires is carried out to ensure the absence of contaminants that would cause a detrimental effect to both etch and resulting sample quality. This is done by sonication of the samples for 3-5 minutes in IPA, before rinsing the samples in DI water and transferring them to a piranha etch (3:1 H₂SO₄:H₂O₂) solution for 10 minutes (5 minutes per side) to remove any organic contaminants. Samples are thoroughly rinsed in DI water at least 3 times to remove any traces of the piranha solution.

In order to obtain SiNWA samples suitable for testing as electrodes, it is more conducive to etch one surface of the Si substrate, whilst protecting the back so as to form a current conducting contact from the electrode at the back. Whilst spinning a protective etch-stop layer on the back could achieve this purpose, we opt to prepare samples in pairs; this enables us to have two samples back to back with the back surface of each sample protecting the other from the etch process. The samples are fixed together using a drop of PMMA between them and sticking them together, letting the ‘glue’ dry/cure for a few minutes before continuing. These samples can then be separated at the end of the etch process in an acetone bath to dissolve the PMMA.

Samples are initially dipped into the nucleation solution, composed of 0.005 M AgNO₃ and 5 M HF, for 2 minutes for the Ag particles to nucleate. After a rinse in DI water, they are transferred to the etch solution comprised of 0.1 M H₂O₂ and 4.9 M HF, where an etch time of 60 minutes will yield a SiNWA array of ~15 µm length for both p- and n-type Si substrates, with SiNW diameter ranging between 50-300 nm [1]. When the desired etch time (default of 60 minutes for this project) for the required length is reached, the samples are rinsed thoroughly in DI water to remove any trace of the etch solution. As a final step, we then transfer the samples into an oxidative solution of diluted nitric acid (1:1 HNO₃:H₂O) for 3-5 minutes so as to remove the Ag particles still present within the SiNWA.

As the final step is an oxidative step, any further process requiring an oxide strip would need the samples to be dipped in dilute HF (~5%) for 5 minutes in order to remove any oxide growth. The need for this would arise for subsequent fabrication steps such as further oxidations, and as a preference, we carry this out as a pre-step for doping to ensure a clear Si surface.
4.1.2. Spin-On Doping (SOD)

Whilst the initial substrate doping concentration is high enough to give good conductivity and ensure low resistance through the bulk, it has been useful to provide additional doping to the samples to boost this even further, especially at the surfaces. This can be useful at the contacts to mitigate contact resistance, or even to tune the nature of the active electrode, i.e. the SiNWA. A means to achieve this is the application of spin-on doping, where a dopant solution is spun onto the surfaces to ensure uniform coverage, before being annealed at high temperature so that the dopant atoms can diffuse into the Si.

SOD variants used throughout the project include Boron, Aluminium and Gallium for p-type, as well as Phosphorus for n-type. Spinning of the dopant solution was carried out followed by low temperature baking to evaporate the solvent. B and P dopant solutions are both spun at 2500 rpm onto the surface for 40 seconds, with an initial acceleration of 500 rpm·s⁻¹. Al and Ga dopants are spun on at 2000 rpm for 15 seconds with an initial acceleration of 400 rpm·s⁻¹. Low temperature baking on the hotplate was at 200 °C for 6 minutes for the B and P dopants, and 100 °C for 10 minutes for the Ga and Al dopants. Spinning and baking is often repeated on the other surface of the Si before the high temperature anneal if both top and back surfaces are intended to undergo SOD.

The high temperature anneal is carried out in a rapid thermal annealer (RTA) at a temperature of above 800 °C for 1 minute, preceded by 5 minutes of purging the RTA chamber with the atmospheric gas to be annealed in. This was in an inert Ar atmosphere for P, Al and Ga dopants, with an O₂ atmosphere chosen for the B dopant to prevent the formation of a boron rich layer [127, 6]. The high temperature anneal is followed by a 5 minute dip in dilute ~5 % HF to remove any oxides formed during the anneal process.

4.1.3. Nitric Acid Oxidation of Silicon (NAOS)

A key original development of this work is the adaptation of an oxidation method known as Nitric Acid Oxidation of Silicon (NAOS) for use as a thin, protective layer on the SiNWA electrode. The high reactivity of Si to most electrolytes, especially aqueous ones, necessitates the protection or passivation of Si to prevent its exposure to an environment in which its performance would degrade. Whilst the oxidation of Si is a well-known and established method capable of protecting the Si surface (as is the case with Si left in air), its disadvantage for an application with Si as an electrode material arises due to it being an insulator.

With conventional capacitances, an oxide layer can act as an insulating dielectric between the parallel plates of the capacitance, though whilst it adds a (small) dielectric constant, it also reduces the
effective capacitance by increasing the distance between the plates. This takes the capacitor out of
the realm of supercapacitors and places it more within the electrolytic capacitance range with a
significantly lower energy density. An oxide layer developed for the purposes of achieving a higher
capacitance would require being ultra-thin, whilst still retaining its properties as a well isolating and
insulating layer.

This was achieved with the growth of a highly dense, ultra-thin (~1.4 nm) layer of oxide with
concentrated (~68 %) nitric acid (see Section 5.4). The NAOS process was carried out by first stripping
the sample of any oxide with a dilute ~5 % HF dip for 5 minutes, followed by immediate transfer into
the heated nitric acid bath before any alternative oxide growth can occur. This was carried out at
temperatures of 90 °C and 120 °C for a duration of 10 minutes. Nitric acid was heated in a contained
oil bath, with a water-based condensing of the nitric acid vapours in a water-flushed extracted wet
bench environment.

4.1.4. Contact Formation

With the ‘top’ surface of our Si samples being used to develop the SiNWA electrodes, we require a
path from this electrode to form a circuit, for measurement and potential future application. Although
the highly doped Si substrate we begin with possesses a high conductivity and thus good current
carrying capability with low resistance from the electrode surface through the substrate, high
resistances may arise when making an external contact with the Si substrate. For that reason, we
would like to develop the unetched ‘back’ surface of the Si sample into a suitable current carrying
contact for measurement purposes; we would like to minimise any characteristics of the sample
measured unrelated to the SiNWA electrode area of interest.

For this purpose, we would like to develop a low-resistance Ohmic contact on the back surface. One
of the methods to achieve this would be to metallise the back surface, with low resistance between
the Si surface and the deposited metal [128], so that the metal can act as the external contact for the
back of our SiNWA electrode. For this, we employ a thermal evaporation method [129], with
Aluminium as our chosen metal, a suitable Ohmic contact metal for p-type (with Al a p-type dopant)
and highly doped n-type Si [130, 129]. The application of SOD to increase the dopant concentration at
the back surface as we have done is also a means of reducing the contact resistivity [131, 132].

In preparation for metallisation of the back surface, we want to make sure that the highly conductive
doped Si substrate is the surface material for the metal to contact, instead of any oxide growth. As we
do not want to cause any affectation on the electrode surface in the process of this, we avoid using a
wet HF dip to remove the oxide, but rather resort to a dry, anisotropic RIE oxide etch that affects only
the back surface. This is carried out with a plasma etch recipe of 25 sccm of CHF$_3$, 25 sccm of Ar and 2 sccm of O$_2$, with a power of 200 W for 5 minutes at a temperature of 20 °C.

Following the oxide strip, the sample is immediately transferred to the chamber of the evaporator, which is pumped down to vacuum. This prevents oxide formation before deposition of the Al. Thermal evaporation is carried out, with at least 100 nm of Al being deposited on the back surface of the Si sample. The sample is then transferred to a RTA be annealed for further improvement of the contact [133]. This is done in an inert environment of Ar, with the RTA purged for 5 minutes before a 1 minute anneal at 200 °C.

4.1.5. Materials

Si wafers used were <100>, double-sided polished 4-inch wafers of 525±25 µm thickness, purchased from Si-Mat. Boron (BDC1-2000) and Phosphorus (PDC1-2000) spin-on dopants (SODs) were purchased from Futurrex Inc., with Aluminium (Al100) and Gallium (Ga250) SODs purchased from Filmtronics. PMMA and the ionic liquids [Bmim][NTf$_2$] (BASF quality ≥ 98 %) and [Emim][HSO$_4$] are all purchased from Sigma-Aldrich. HF (50 %), HNO$_3$ (68 %), H$_2$O$_2$ (30 %), H$_2$SO$_4$ (95 %), IPA and acetone are all purchased from VWR International Ltd.

4.2. Characterisation

The fabrication and development of the electrode needs to be complemented by ways to measure, analyse and assess its performance. Evaluation of the SiNWA electrodes and comparisons were carried out primarily by electrochemical measurements in the configuration of a three electrode half-cell, a means of analysing a single electrode in isolation as opposed to a two electrode complete capacitor device. Multiple measurements are carried out on the electrode in the IL electrolyte, including cyclic voltammetry (CV), electrical impedance spectroscopy (EIS) and chronopotentiometry (CP, also known as galvanostatic charge/discharge (GCD) measurements).
Figure 4.2 – Structural formula of the ions comprising the IL, with the [Bmim]$^+$ cation (left) and [NTf$_2$]$^-$ anion (right) [134].

The chosen IL electrolyte used throughout the project, unless stated otherwise, was 1-Butyl-3-methylimidazolium bis(trifluoromethylsulfonyl)imide, i.e. [Bmim][NTf$_2$] (also known as [Bmim][TFSI]), as seen in Fig. 4.1. Features of this electrolyte that make it particularly suitable for this application include a low viscosity for an IL, primarily due to the [NTf$_2$]$^-$ anion [135, 136], hydrophobicity [136], the lack of any fluorinated ions such as BF$_4^-$ and PF$_6^-$ that may cause etching of Si with voltammetry [137, 138], and a wide EW of $\geq 3$ V in atmospheric conditions and up to 5 V after being vacuum dried [139, 140].

4.2.1. Three Electrode Half-Cell

The configuration used for all types of electrochemical measurements is a three electrode one, consisting of our electrode as the working electrode, a coiled platinum wire as counter electrode, and a silver wire as reference (pseudo-reference) electrode. This was carried out in custom built electrochemical cells constructed from PTFE. The initial stages of electrode development were first carried out in a cell with a larger projected surface area (area of working electrode exposed to the electrolyte assuming a perfectly flat electrode) of 2.8 cm$^2$. The external contact to the back was made with a Pt wire and silver paint. This was used in Sections 5.1 to 5.4. All other measurements were conducted with a more conveniently operable cell, shown in Fig. 4.3, with a projected surface area of 1.327 cm$^2$. 
A three electrode setup is the most commonly used one for electrochemical measurements [142, 143]. The presence of the additional electrode helps overcome a key weakness in a two electrode setup, i.e. the effects of any voltage drop due to the electrode that is not the working electrode. This is achieved by the control of the voltage and the current being separated, with the current drive and flow being effected through the counter electrode, whilst the potential is monitored by the reference electrode (Fig 4.4). With negligible current through the reference electrode, this mitigates any effects being caused by potential changes elsewhere than with respect to the working electrode, giving better analysis of it.

In preparation for measurements, the O-ring and PTFE section of the cell in contact with the electrolyte were cleaned by immersion in 7:3 H2SO4:H2O2 piranha solution diluted 50 %, followed by
a DI water and then ethanol rinse. As a water-free environment is desired, this was dried in an oven at 80 °C prior to measurement. The Pt counter electrode is cleaned by heating in a hydrogen flame, and the Ag wire was immersed in a 1:1 solution of concentrated nitric acid and water. The [Bmim][NTf₂] IL electrolyte was dried by heating at 80 °C with vacuum for 12 hours. Post-measurements, the SiNWA working electrodes would be kept in acetone overnight for the removal of any residual electrolyte present.

4.2.2. Cyclic Voltammetry (CV)

Cyclic voltammetry is one of the most established measurement techniques for electrochemical analyses. It is conducted by controlled scanning of the electrode potential – measured between the working and reference electrodes – at a constant rate with time, with the output being current flow measured through the counter electrode. In terms of evaluating capacitive performance, we are able to make useful observations and extract parameter values that can be used to evaluate performance, such as the capacitance and operating electrochemical window (EW).

![Figure 4.5 - Determination of electrochemical window (EW) and current (i) for CV measurement of capacitive quasi-rectangular shapes (a) and with redox peaks (b) [141].](image)

One of the more visibly apparent observances from the CV plot is the capacitive nature of the electrode and the presence/absence of any redox activity. A double layer capacitor without any faradaic reactions occurring would be expected to have a quasi-rectangular CV shape, whilst the presence of redox activity may be seen with the appearance of peaks in the CV plot (Fig. 4.5b). EW determination for the CV measurements is determined depending on this nature, with the EW for the quasi-rectangular CV determined as the points between the current values reaching 3x the value of current at the mid-window point of minimum current difference, whilst for samples with peaks, the window was evaluated in relation to the current values reaching the values of the peaks.
Equation 4.1 – Capacitance determination from current (i), scan rate (dV/dt) and projected area (A).

\[ C = \frac{i}{dV/dt \cdot A} \]

CV measurement also enables us to extract a capacitance value based on the current measured (i) and scan rate (dV/dt) used (Eq. 4.1). Where possible, as with most measurements, multiple scan rates and current measurements are used, with current plotted against scan rate and the gradient (scaled by the area, A) of this used to determine the CV extracted capacitance.

Figure 4.6 – Current vs scan rate for CV measurements. The linear gradient of the graph is fitted to extract a value of capacitance [3].

4.2.3. Electrical Impedance Spectroscopy (EIS)

Another useful technique to evaluate electrode performance is electrical impedance spectroscopy, conducted by frequency scanning of the electrode over a range of frequencies at a particular potential. The measurement is carried out by applying AC voltages of varying frequencies, measuring the current response, and obtaining the value of impedance as a function of frequency. With both magnitude and phase being analysed, the value of impedance, Z, is a complex one, and can be analysed in terms of its real and imaginary components. This enables us to characterise it in terms of equivalent circuit components, and extract device performance parameters such as capacitance and series resistance.
Equation 4.2 – Impedance equations for Electrical Impedance Spectroscopy.

\[ Z(j\omega) = \frac{V(j\omega)}{I(j\omega)} \]

\[ Z = Z_0 e^{j\theta} = Z' + jZ'' \]

\[ Z_{\text{resistor}} = R \]

\[ Z_{\text{capacitor}} = \frac{1}{j\omega C} = -\frac{j}{\omega C} \]

Having a picture of a device measured in terms of complex impedance vs frequency enables us to fit this to an equivalent circuit model, where an appropriate one can be found. For a near ideal capacitor device, this would be in the form of a simple, series RC circuit (Fig 4.7). This would appear on the Nyquist plot as a vertical line of infinite gradient, with the real-axis intercept being the ESR, and the capacitance easily extractable from the imaginary part of the impedance and frequency. This series resistance (\(R_s\)), in terms of an EDLC system, is likely to have its major contribution from the electrolyte or ‘solution’ resistance [144, 145]. The double layer capacitance is represented by the capacitor (\(C_{dl}\)) component.

![Figure 4.7 – Equivalent RC series (left) representing double layer capacitance (\(C_{dl}\)) and solution resistance (\(R_s\)), along with its Nyquist plot (right) from EIS measurements. Real impedance intercept is equal to \(R_s\), with complex impedance (from \(C_{dl}\)) increasing with lower frequencies.](image)

For electrochemical cells, such as with an EC, the equivalent system may not be quite as simple. The impedance character of an EC system may better be initially represented by the simplified Randles circuit (Fig 4.8) [146, 145, 147, 144], which adds an additional equivalent circuit resistance in parallel with the double layer capacitance.
This resistance, called the polarisation resistance ($R_p$, often also known as charge transfer resistance $R_{ct}$), and refers to the resistance towards a charge transfer process occurring at the electrode-electrolyte interface in opposition to the applied external potential as a means of restoring system equilibrium. This may be in the form of a redox reaction at the interface that results in the transfer of charge, or alternative leakage current at the surface. The restriction of charge transfer – such as from such a redox reaction – leads to a very low polarisation current and thus high polarisation resistance. A system with very low reactivity at the interface would yield a very high polarisation resistance, which is the case with some of the EDLC systems we’ve achieved. In this case, the Nyquist plot displays a more vertical character as with the simple RC circuit, as opposed to the semi-circular character of the Nyquist plot of a simplified Randles cell.

![Simplified Randles circuit](image)

**Figure 4.8 – Simplified Randles circuit (left) and its associated Nyquist plot (right) from EIS. Polarisation resistance ($R_p$) is introduced in addition to the solution resistance ($R_s$) and double layer capacitance ($C_{dl}$).**

Some of our systems have displayed the character of having a more complex equivalent circuit than the simplified Randles. This is often in the form of a much smaller second semi-circular observance on the Nyquist plot at higher frequencies [3]. We have found that this can be modelled with an additional parallel RC combination inserted in series with the simplified Randles circuit, and even though the effect of this is small, we use this modified Randles model for better circuit fitting and value extraction [3]. An explanation for this addition may be found on the other side of our SiNWA samples, i.e. the metal-semiconductor contact. If there are any parasitic capacitances, or if the character of the contact is not completely ohmic (as with the RC parallel equivalent seen in Schottky models [148, 149, 150, 151]). With this in mind, our equivalent circuit model fits well to the physical structure of our electrochemical cell measurement system (Fig 4.9). As such, this modified Randles circuit shall constitute the primary model we use for circuit fitting of our samples, with the double layer capacitance ($C_{dl}$) our primary parameter of interest.
4.2.4. Chronopotentiometry (CP)

Chronopotentiometry is another measurement technique useful for electrochemical analysis, especially in the context of electrical energy storage systems [152, 153, 154]. As the name suggests, it measures the potential as a function of time. This is done with a constant current driven in either direction – the technique is also known as galvanostatic charge/discharge (GCD) – cycling between two values of potential, i.e. an operating potential window.

The advantage of CP in terms of analysis the character and performance begin with the ability to extract yet another value of capacitance. Furthermore, compared to CV and EIS, it can provide us the added benefit of being able to extract a value for power density, which can be determined by the charge/discharge time and energy density extracted from the capacitance and EW between which the cycling occurs. In addition to performance parameters, repeated cycling of charging and discharging over a number of cycles enable us to determine the cyclability, lifetime and capacitance retention of the electrode.
Figure 4.10 – Chronopotentiometry trace, and determination of values of capacitance, energy and power from it.

We conduct CP on our samples with the three electrode setup, cycling them between the EW with a set of currents ranging from 0.1-1 mA. As the gradients of the trace give us a value of $dV/dt$ for each constant current value, we are able to determine a value of capacitance from this (Eq. 4.1) as with the CV measurements. Also, as with the CV, with a set of measurements available, the fitted linear slope of current vs potential-time gradient is preferred for this value.

\[
C = \frac{i}{dV/dt}
\]

\[
E = \frac{1}{2} CV^2
\]

\[
P = \frac{E}{t}
\]
5. ELECTRODE DEVELOPMENT

This chapter shall chronicle the development of the key achievement of this project, i.e. realising a viable and competitive high capacitance Si based electrode. It shall look into the initial phases of testing out the character of a MACE nanostructured SiNWA as an electrode, the limitations realised, improvements attempted and final successes in producing SiNWA based electrodes with supercapacitor performance.

5.1. Nanostructuration with SiNWA

As our aim was to begin exploring whether the use of nanostructured Si in the form of SiNWA could yield a significantly improved capacitance over bulk Si, the initial experiment involved the simple comparison of a SiNWA sample with a bulk Si sample.

Si bulk with a reasonably low resistivity of 0.01-0.02 Ω·cm was chosen to be our substrate, as our intentions were to maximise substrate conductivity. The use of Si substrates with lower resistivities (i.e. with higher dopant concentrations) is known to affect the MACE process and has a major effect on the morphology of the resulting SiNWA [155, 126]. The presence of a large concentration of doping atoms within the Si lattice offers more sites for etching to occur on the sidewalls of the nanowires. This results in an increased porosity of the wire, making the nanowires more prone to breakage. Despite the resistivity of 0.01-0.02 Ω·cm being low enough to cause nanowire porosity with solutions developed for the more ubiquitous 1-10 Ω·cm Si substrate, a two-step MACE process capable of producing stronger nanowires at the lower resistivity had previously been developed in-house [62], enabling the usage of samples with a higher conductivity for our investigation.

Single-sided SiNWA samples were fabricated from both n- and p-type substrates, with an etch time of 1 hour to give an approximate nanowire height of 15 µm. The samples were dipped in a solution of dilute HF (<5%) to remove any native oxide growth, followed by the deposition of a ~100 nm Al layer on the back (i.e. bulk) side of the sample as an Ohmic contact, providing a path for current conduction from the electrode substrate.
The choice of electrolyte and means of characterisation were decided by an expression of interest in collaboration with the Department of Chemistry at Imperial College London. The interest of exploring the usage of room temperature ionic liquids (RTILs or ILs), especially in a ‘green’, environmentally friendly context, coincided well with our aim of developing a high capacitance electrode with SiNWAs. ILs seemed to be an ideal choice for use as electrolyte, particularly for overcoming the key weakness of Si as an electrode material, its high reactivity. In addition to being non-aqueous, ILs have high chemical and thermal stability, and seemed promising for developing electrodes with a high operating potential window, and thus a high energy storage density. Furthermore, the characterisation of devices within this family (i.e. electrochemical capacitors (ECs)) is best done using electrochemical methods such as cyclic voltammetry (CV), and therefore doing measurements and analyses with the Department of Chemistry was an additional benefit. The measurements on the fabricated samples were carried out in collaboration with MRes student Lu Qiao [156].
CV measurements of the samples show clear differences between the bulk Si and SiNWA samples (Fig. 5.2), with both n- and p-type showing the same comparative contrasts in terms of current and voltage. As expected, with the increased surface area of the SiNWA providing a site for more charge storage, the current values of the CV scans for the SiNWA samples markedly exceed the values for the bulk Si.
With the capacitance being proportional to the current at identical scan rates, this demonstrates a successful increase in capacitance with the nanostructuration, as shown in Table 5.1. However, along with this, we observe that the nanostructuration has also resulted in a contraction of the operating potential window (or electrochemical window, EW) of approximately 0.35 V.

Table 5.1 – Current, Capacitance, and Electrochemical Window characteristics for n- and p-type SiNWA and bulk Si samples. Projected surface area of measurement cell is 2.8 cm².

<table>
<thead>
<tr>
<th></th>
<th>n-type</th>
<th>p-type</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>SiNWA</td>
<td>SiNWA</td>
</tr>
<tr>
<td>Current (µA)</td>
<td>0.77</td>
<td>4.27</td>
</tr>
<tr>
<td>Areal Capacitance (µF·cm⁻²)</td>
<td>5.52</td>
<td>30.50</td>
</tr>
<tr>
<td>Electrochemical Window (V)</td>
<td>0.85</td>
<td>0.50</td>
</tr>
</tbody>
</table>

These initial findings represent a partial success for the use of SiNWA in developing high capacitance Si-based electrodes. Despite a contraction of the EW indicating a reduction in electrode stability, an increase in capacitance of ~5x over bulk Si with SiNWAs of ~15 µm height was observed, demonstrating the expected utility of the large surface area achieved with nanostructuration in terms of the charge storage ability of the electrode. Further improvements made in order to increase the capacitance and stability of the electrode could result in the realisation of a competitive Si based high capacitance electrode.

5.2. Introducing Spin-On Doping (SOD)

One of the first improvements intended to be made upon the SiNWA electrode was to increase the surface conductivity via a doping process. The idea was that a higher amount of charge carriers at the surface could result in the ability a greater amount of charge at the electrode’s interface with the electrolyte. As the MACE process limits the carrier concentration we could begin with whilst still having robust NWs, a post-etch doping step was chosen to try and improve the conductivity.

A doping technique known as spin-on doping (SOD) was chosen to try and achieve this. SOD application on MACE SiNWA samples has been shown to drastically improve surface conductivity, with contact resistances on SiNWA samples for thermoelectricity being almost completely nullified with SOD [62, 157]. SOD involves the spinning of a dopant solution on the sample surface to ensure a uniform coating, followed by a high temperature anneal step to drive the doping atoms into the Si lattice (see Section 4.1.2 for process). This results in a high carrier concentration at the sample surface, with the concentration gradually decreasing with depth in the substrate (Fig. 5.3).
Figure 5.3 – Profile of doping concentrations of phosphorus dopant with boron doped Si substrates (bulk, pyramid, NWA, and pyramid-NWA hybrid) after an SOD step with similar processing, as simulated with Sentaurus [55].

SOD steps were carried out on SiNWA samples after the MACE process and an HF dip to remove any surface oxide growth. Boron was used as the dopant atom for the p-type sample, with Phosphorus for the n-type one. The SOD solutions BDC1-2000 (Boron) and PDC1-2000 (Phosphorus) were obtained from Futurrex Inc.
Figure 5.4 – CV measurements with $v = 50$ mV/s of n-type (top) and p-type (bottom) SiNW (black) and SOD treated SiNW (red) samples.

To gauge the effectiveness of the SOD application, the SOD treated SiNW samples were contrasted with the SiNW samples without SOD (Fig. 5.4). We can see that in both the n- and p-type samples that the SOD application has had a significant effect on the measured CV curves from the sample. The
most significant change seen is the one that was expected, i.e. an increase in the current values for
the SOD treated samples, translating into higher capacitances (see Table 5.2). In addition to this, we
observe that the EW has not reduced, but has rather had a marginal increase in value, bringing the
EWs of both n- and p-type samples up to 0.65 V.

Table 5.2 – Current, Capacitance, and Electrochemical Window characteristics for n- and p- type SiNWA
samples with and without SOD application. Projected surface area of measurement cell is 2.8 cm².

<table>
<thead>
<tr>
<th></th>
<th>n-type SiNWA</th>
<th>p-type SiNWA</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>no SOD</td>
<td>SOD</td>
</tr>
<tr>
<td>Current (µA)</td>
<td>4.27</td>
<td>13.10</td>
</tr>
<tr>
<td>Areal Capacitance (µF·cm⁻²)</td>
<td>30.50</td>
<td>93.57</td>
</tr>
<tr>
<td>Electrochemical Window (V)</td>
<td>0.50</td>
<td>0.65</td>
</tr>
</tbody>
</table>

Unlike with the initial nanostructuration step, we see marked differences between the effects on the
n- and p-type samples after SOD application. These differences are apparent both in the shape of the
CV curves (Fig. 5.4) and the extracted capacitance values. With regards to the CVs, whilst the n-type
SOD sample retains the expected quasi-rectangular shape of a double layer capacitor electrode, the
p-type SOD sample shows a CV curve that displays an additional feature in the middle of the scan, in
the form of a peak in both the negative (cathodic) and positive (anodic) scans. These peaks are typically
associated with oxidation (anodic peak) and reduction (cathodic peak) reactions occurring [158, 159].
With the current values even outside the peaks being of a considerably higher magnitude than those
for the non-SOD sample, the capacitance boost with SOD for the p-type sample is triple that of the n-
type sample, with capacitance boosts of 9.3x and 3.1x respectively.

From the exploration into the application into SOD, there are three points of note: the EW, the CV
peaks, and the current boost. We have observed a minor increase in the EWs of the samples after SOD
application, indicating an increased stability. This is likely to be due to a surface modification occurring
during the SOD process, such as the oxide grown during the high temperature anneal step. A residual
oxide or other protective layer may be left, even after the oxide removal step. In the p-type SOD
sample we have additionally observed anodic and cathodic peaks appearing on the CV curve. This was
conjectured to be potentially due to a boron layer being present at the surface, as previous
experiments with boron SOD have shown to result in the growth of a boron rich layer at the SiNWA
surface [127]. Finally, most importantly and most significantly, the application of SOD on the SiNWA
electrode samples has resulted in the desired effect of increased currents, leading to a capacitance
boost of 3-10x compared to before the SOD. A new best of a capacitance of 43x the bulk Si value was achieved with the SOD treated SiNWA.

5.3. Initial Surface Passivations

Our investigations thus far have shown that the surface area boost through nanostructuration and a surface carrier concentration boost through SOD can increase the charge storage ability of Si as an electrode. However, the merit of a capacitor electrode lies not only with its capacitance value, but also its operating potential window (EW). This has its most significant impact in the energy storage density, as the relation of energy (E) to the capacitance (C), also involves the potential difference (V), as shown in the equation \( E = \frac{1}{2} CV^2 \). Therefore, we know that for the same capacitance, an increase in the EW will quadratically increase the energy density.

Despite the use of an IL electrolyte with the aim of achieving better stability, our results have not demonstrated an improvement of the EW of Si compared to reported values with aqueous electrolytes (≤ 0.8 V [15, 17]). This may be attributed to a residual water trace present in the IL (possibly due to exposure to the environment before measurement), even though it is hydrophobic. Furthermore, the increased surface area of the SiNWA electrodes seem to have resulted in reducing the stability of the electrode-electrolyte system. The development of a practical and competitive Si-based high capacitance electrode would necessitate increasing the EW.

As the high reactivity is attributed to Si, protecting the Si surface and preventing its exposure could improve the stability of the electrode. This passivation of the Si surface could be done by the deposition a different material or other modification of the Si surface in order for Si to not be the material in contact with the electrolyte. A successful passivation has been reported [121] by electrochemically oxidising the surface of a nanostructured Si electrode. However, though a protective layer may improve stability, we also have to consider that it may reduce the performance of the electrode. The high capacitances obtained by double layer capacitors rely on minimal distances between electrode and electrolyte, and the introduction of a non-conductive layer between electrode and electrolyte would thus reduce the capacitance in proportion with the thickness of the layer. This would bring it more in line with conventional electrolytic capacitors rather that double layer supercapacitors.

Therefore, for passivating our Si surface without significantly compromising electrode performance it is important we place constraints on our passivation method. The passivation layer would need to either be a functional part of the electrode, or thin enough so that any potential reduction in
capacitance is minimal. For a material to be functional for double layer capacitance, we would require it to be both inert and conductive, as is the case with carbon materials generally used as electrodes.

In this section we shall explore two potential passivation methods. One shall involve the deposition of a thin layer of a carbon polymer used elsewhere in Si surface protection for etch processes \cite{160, 161}. We shall also attempt to replicate the electrochemical oxidation method used in \cite{121}, and assess whether we can employ it as effectively on our MACE SiNWA electrode as they did with SiNWs grown via chemical vapour deposition (CVD).

5.3.1. Fluorocarbon Polymer Deposition

An initial attempt to passivate the Si surface was carried out with depositing a thin polymer film derived from C\(_4\)F\(_8\) (octafluorocyclobutane) onto the surface using a Deep Reactive Ion Etching (DRIE) Bosch Process \cite{160, 161}. The Bosch Process involves an alternation of etch and polymer deposition steps, with the deposition of a fluorocarbon polymer film (such as polytetrafluoroethylene, PTFE) from a C\(_4\)F\(_8\) gas precursor acting as a passivation step to promote anisotropic etching. This polymer film has properties highly desirable for our application, with it being a relatively inert layer and being capable of being deposited with minimal thickness, <5 nm \cite{162}. Additionally, its hydrophobicity \cite{163, 164} may also aid our aim of reducing reactivity. With its high potential suitability and easy access to DRIE to carry out the process, we decided on the evaluation of a C\(_4\)F\(_8\) derived polymer film on Si as one of our first passivations to be explored.

C\(_4\)F\(_8\) deposition was carried out on n- and p- type SOD treated SiNWA samples for evaluation with two different thicknesses, based on deposition time. Deposition times of 30 and 90 seconds were used for a thinner and thicker layer comparison of the samples. The CV curves of the samples with polymer films deposited are shown in comparison to an equivalent sample without the polymer (Fig. 5.5).
Figure 5.5 – CV measurements with $v = 50 \text{ mV/s}$ of n-type (top) and p-type (bottom) SOD treated SiNWA samples with thin (red), thick (blue) and no (black) fluorocarbon polymer films deposited.
We can see variances between the samples from the CV curves, though perhaps with differences that are not as significant as seen with the previous steps of nanostructuration and doping. The n-type curves seem fairly similar in both size and shape, though we can see that the current magnitude increases with the polymer layer. Furthermore, the thicker polymer layer has shown to increase the EW by about 0.2 V, fulfilling our primary aim of improving electrode stability to an extent. This behaviour is not replicated with the p-type samples, though we observe that the current value for the thicker layer is significantly higher, indicating a higher capacitance value even with the lack of a stability improvement.

This is also quantified in Table 5.3 with the measured current and EW values. The 30 s deposition layer seems to have had very little effect on the samples, with sample variance possibly accounting for the minor differences. The EW values remain at ~0.65 V for both n- and p-type samples, with a minor increase/decrease in the current, and thus capacitance. With the thicker polymer layer, both n- and p- samples show a distinct current increase, giving capacitances of 1.8x and 2.1x respectively, an approximate doubling of the capacitance. Additionally, the n-type sample seems to benefit from a stability boost with the higher EW.

Table 5.3 – Current, Capacitance, and Electrochemical Window characteristics for n- and p-type SiNWA samples with SOD application and fluorocarbon film deposition. Projected surface area of measurement cell is 2.8 cm².

<table>
<thead>
<tr>
<th>Time of C₄F₈ deposition</th>
<th>n-type SiNWA</th>
<th>p-type SiNWA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current (µA)</td>
<td>no film</td>
<td>30 s</td>
</tr>
<tr>
<td></td>
<td>13.10</td>
<td>15.30</td>
</tr>
<tr>
<td>Areal Capacitance (µF·cm⁻²)</td>
<td>93.57</td>
<td>109.29</td>
</tr>
<tr>
<td>Electrochemical Window (V)</td>
<td>0.65</td>
<td>0.63</td>
</tr>
</tbody>
</table>

We can therefore conjecture that a fluorocarbon film deposition gives a performance improvement upon the SOD treated SiNWA, though that performance boost is marginal. The key factor of improvement is a doubling of the capacitance value. This, in fact, lines up well with the capacitance formula $C = \varepsilon A/d$, as with the same area $A$, an increase of the permittivity $\varepsilon$ greater than the distance $d$ would provide a capacitance boost. With regards to the distance, it is possible that the layer is ultra-thin, thus not affecting the capacitance significantly. An alternative explanation is that since thin layers of fluorocarbon polymer may have reasonable conductivities [165], the polymer film acts as an extension to the electrode surface, thus not contributing to an increasing distance. Assuming that the film deposition has a negligible effect on the distance of the electrode with the electrolyte,
the relative permittivity of a fluorocarbon layer such as PTFE being \( \varepsilon_r = 2.1 \) could fit well with the capacitance boost of up to 2.1x that we see.

Whilst a small capacitance boost may be obtained with the polymer deposition, it has failed to achieve its main aim, i.e. that of improving stability and expanding the EW. The n-type sample did show a marginal improvement, but this was much below the scale we had hoped for when deciding to investigate this method of improvement. The fluorocarbon polymer layer does not seem to have had a significant effect on the reactivity, despite its protective nature and observed hydrophobicity. An experimental limitation may be possible for this lack of improvement, with the absence of any residual or atmospheric water on the Si surface not sufficiently ensured. Water trapped between the fluorocarbon layer and SiNWA surface may be responsible for limiting the EW, such that there’s no significant improvement.

A partial success in improving SiNWA electrode performance with fluorocarbon polymer deposition may be claimed in light of the improved capacitance. However, with the improvement in EW being insignificant, we shall continue to look at alternative coatings to improve stability. A recommendation for any future studies regarding this method would be to ensure a dry surface with the complete removal of water immediately before polymer deposition, e.g. with sustained heating above boiling point \([166, 167]\) and maintaining a dry atmosphere until deposition is carried out.

5.3.2. Electrochemical Oxidation

A possible method to prevent the propensity of Si to oxidise – thereby limiting its operating potential window – is to pre-oxidise the Si so that further oxidation is limited. As with oxides such as aluminium oxide \([168, 169]\), an oxidised surface layer can perform the role of a protective coating for Si. This is especially relevant in this case, as the main reason attributed to the limitation of the Si potential window is the presence of water, even in trace amounts \([15, 17, 170]\). An investigation into the oxidation of nanostructured Si to improve electrode stability was carried out by Berton et al \([121]\) using an electrochemical method. The EW for chemical vapour deposition (CVD) grown SiNWs was shown to increase substantially (up to 4 V) after surface oxidation of the nanowires by cycling the electrode at successively higher anodic potentials.
We decided to attempt replicating this effect seen on CVD grown SiNWs with our MACE etched SiNWA samples. Samples of n- and p-type SOD treated SiNWAs underwent electrochemical oxidation for 20 cycles at a maximum anodic potential of 1.2 V (Fig. 5.6). We can see that the maximum current seen at 1.2 V decreases with successive cycling as the Si layers are oxidised, representing increased oxidation coverage of the Si accessible to the electrolyte. CV scans of these samples in comparison with unoxidised samples are shown in Figure 5.7.
Figure 5.7 – CV measurements with $v = 50 \text{ mV/s}$ of n-type (top) and p-type (bottom) SOD treated SiNW samples with (red) and without (black) electrochemical oxidation.

Two features are apparent in both doping types when comparing the oxidised and unoxidised electrodes. One is that the current magnitudes have increased, indicative of an increased capacitance. More importantly, the EWs appear to have widened, thus at least partially achieving the aim of the
electrochemical oxidation. Other observances to notice are the possible redox peaks in the middle of the CV scans, with the p-type sample showing more dominant peaks. The mid-scan redox peaks appear in both p-type scans, though the anodic and cathodic peaks seem to have moved further apart after oxidation.

When considering the numerical values extracted (Table 5.4), we can see that as also observed from the CV curves, the performance boost attained post-oxidation is greater with the p-type samples than with the n-type samples. The current and capacitance boost for n- and p-type is 1.17x and 1.62x respectively. The same can be said for the EW increase, with increases of 0.05 V and 0.31 V respectively. This indicates that the electrochemical oxidation process as carried out has had a bigger impact on the p-type sample than it has on the n-type. A possible explanation for this is that with the same process, a greater level of oxidation was realised on the p-type sample. This would account for the greater improvement in the EW of the electrode. It may also account for the greater capacitance boost, for the same reason as alluded to in the previous Section 5.3.1, with the oxidised surface layer acting as a dielectric to boost capacitance. Though the thickness of the electrochemically oxidised layer is unknown, it may be that the boost from the relative permittivity is greater than that of any decrease in capacitance caused by a greater electrode-electrolyte distance.

Table 5.4 – Current, Capacitance, and Electrochemical Window characteristics for n- and p- type SiNW samples with SOD application and electrochemical oxidation. Projected surface area of measurement cell is 2.8 cm².

<table>
<thead>
<tr>
<th>Electrochemical Oxidation</th>
<th>n-type SiNWA</th>
<th>p-type SiNWA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current (µA)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>No</td>
<td>13.10</td>
<td>17.60</td>
</tr>
<tr>
<td>Yes</td>
<td>15.30</td>
<td>28.50</td>
</tr>
<tr>
<td>Areal Capacitance (µF·cm²)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>No</td>
<td>93.57</td>
<td>125.71</td>
</tr>
<tr>
<td>Yes</td>
<td>109.29</td>
<td>203.57</td>
</tr>
<tr>
<td>Electrochemical Window (V)</td>
<td>0.65</td>
<td>0.65</td>
</tr>
<tr>
<td></td>
<td>0.70</td>
<td>0.96</td>
</tr>
</tbody>
</table>

We can make a few inferences from this exploration of electrochemical oxidation. The first is a partial affirmation of the effectiveness of an oxide layer grown on the SiNWA in improving stability, as evidenced by the improvements in the EW. However, this improvement is still much smaller than what we were hoping for, and what others have achieved with a similar process. Whether the difference lies in the process needing fine tuning for this electrode-electrolyte system or because MACE etched SiNWs are fundamentally different (e.g., rougher) from CVD grown SiNWs is unknown, and could be further investigated. We can also infer that we achieve a capacitance boost with electrochemical oxidation, though to a lesser extent than seen with the fluorocarbon polymer film coverage (Section
5.3.1). This is indicative of the oxide layer formed by electrochemical oxidation being of greater thickness than the polymer layer, especially if we account for a hypothesis where the dielectric constants of each contribute to the capacitance improvement. The realisation of a thinner yet more stable layer covering the SiNW should help us achieve an even better performance improvement.

5.4. Nitric Acid Oxidation of Silicon (NAOS)

Having achieved a measure of success in improving the stability of the electrode with an oxidation step done electrochemically, the desire to attempt an alternative means of oxidation persisted. A method that would achieve a more robust oxide for better stability should help us expand the EW further, and keeping the oxide layer thickness to a minimum would help with maintaining a high capacitance.

Though the most robust common method of oxidation is thermal oxidation [171], the time involved means that it yields oxide thicknesses of more than a few nanometres, which would strongly impact our capacitance. As one of the key strengths of our electrode development stems from the fabrication done in a low cost, chemical manner without the use of specialised equipment, the inspiration for seeking a similar simple chemical oxidation emerged. A known oxidation step that already existed during the processing was the immersion in diluted nitric acid to remove the silver particulates from NW etching (Section 4.1.1). Oxidation carried out in acid would fit well with our simple and low-cost approach. However, wet oxidation processes have been known to yield oxides of much lower quality than dry thermal oxidation, i.e. the oxide density is lower, with potential porosity and/or lack of full/uniform coverage [172, 173, 174].

However, research into oxidation using nitric acid returned an interesting finding. Nitric acid oxidation of Silicon (NAOS) has previously been carried out to yield high quality gate oxides [175, 176]. The nature of the oxide developed seemed promising for use on our electrodes. A good gate oxide requires a high oxide density to limit leakage currents. Additionally, with the focus on scaling down devices sizes, the ultrathin oxide layer of ~1.4 nm [175, 176] fits well with our desire to keep oxide thickness to a minimum. The key to maintaining a high oxide density with low leakage current lies in the use of the azeotrope of nitric acid (a.k.a. concentrated nitric acid) at 68 % by wt. concentration, as lower concentrations yield oxides of lower densities which can be porous. The tight packing of the oxide generated with concentrated acid ensures self-limiting of the oxide thickness; oxides of greater thickness can be generated by first doing a NAOS step with lower acid concentration before moving onto the azeotrope [177, 178].
Although the NAOS procedures are normally carried out at the boiling point of the respective concentrations, which is 120-121 °C for the azeotrope, the initial oxidations were carried out at the lower temperature of 90 °C due to the volatile nature of heated acid and the need for a more robust safety mechanism to be ensured before progression. The procedure was carried out on both n- and p-type SiNWA samples with post-etch P and B SODs, respectively. NAOS was carried out immediately after a dip in dilute HF (~5 %) to remove any existing oxide growth, ensuring that any grown oxide layer can be attributed to NAOS. Subsequently, the procedure was carried out at the boiling point of ~120 °C as well, as performed in literature [178, 175, 177]. The CV scans for the samples in comparison to the respective unoxidised SOD treated SiNWA is shown in Fig. 5.8.
Figure 5.8 – CV measurements with $v = 50$ mV/s of n-type (top) and p-type (bottom) SOD treated SiNW samples without (black) and with nitric acid oxidation (NAOS) at 90 °C (red) and 120 °C (blue).
We can clearly see from the CV scans that the NAOS procedure has had a profound effect on the samples, with the desired expansion of the EW realised along with a substantial increase in current. With the n-type samples, we can see that both temperatures of oxidation have yielded improved results, though the oxidation at ~120 °C has a wider EW and has seemed to be more effective than the 90 °C oxidation overall, with both having similar currents. Contrarily, for the p-type samples, the 90 °C oxidation seems to be the better result, with the wider EW and the larger, yet more stable, current. It should be noted that the small EW seen with the ~120 °C oxidised sample may in fact be misleading, as later CV scanning with larger potentials have shown that what was assumed a window at first is likely in fact a current spike associated with the anodic and cathodic mid-window peaks observed with the SOD treated p-type sample, though shifted greatly in potential. The actual EW realised by the oxide can be seen to be greater, approaching the value attained for the 90 °C oxidation. Further investigations into the phenomenon of the peaks shall be explored later in Chapter 6.

At this point, we shall take the relatively flat 90°C oxidised p-type and ~120 °C oxidised n-type samples to be our best performing electrodes. This is emphasised by the extracted values from the CV scans (Table 5.5), with the improvements in EW of 1 V and 0.85 V as well as capacitance improvements of 2.4x and 3x for the n- and p-type samples respectively. The areal capacitances for the SOD treated, HNO₃ oxidised SiNWA in comparison with our initial bulk Si samples has now reached values of 41x and 128x for the n- and p-type samples respectively. We see that the improvement for the p-type is around 3 times greater than that for the n-type, which follows on from the greater impact of the doping step on p-type as compared to n-type (Section 5.2).

Table 5.5 – Current, Capacitance, and Electrochemical Window characteristics for n- and p-type SiNWA samples with SOD application and nitric acid oxidation at two temperatures. Projected surface area of measurement cell is 2.8 cm².

<table>
<thead>
<tr>
<th>Oxidation Temperature (°C)</th>
<th>( \text{no oxide} )</th>
<th>90</th>
<th>120</th>
<th>( \text{no oxide} )</th>
<th>90</th>
<th>120</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current (µA)</td>
<td>13.10</td>
<td>23.80</td>
<td>31.60</td>
<td>17.60</td>
<td>52.00</td>
<td>54.30</td>
</tr>
<tr>
<td>Areal Capacitance (µF·cm²)</td>
<td>93.57</td>
<td>170.00</td>
<td>225.71</td>
<td>125.71</td>
<td>371.43</td>
<td>387.86</td>
</tr>
<tr>
<td>Electrochemical Window (V)</td>
<td>0.65</td>
<td>1.00</td>
<td>1.65</td>
<td>0.65</td>
<td>1.50</td>
<td>0.60</td>
</tr>
</tbody>
</table>

With the significant improvements in capacitance and EW seen with the SOD treated NAOS SiNWA samples, we wanted to further ascertain and confirm their performance with additional measurement techniques such as Electrochemical Impedance Spectroscopy (EIS) and Chronopotentiometry (CP),
also known as Galvanostatic Charge-Discharge (GCD). EIS measurements were performed on the samples with frequencies between 0.1 Hz and 100 kHz, with GCD measurements done at a constant current of 1mA within the EW.

Figure 5.9 – Zoomed-in Nyquist plots of actual (red) and fitted (blue) of best performing n-type (top left) and p-type (top right) SOD treated SiNWA samples with nitric acid oxidation (NAOS) with frequency ranging from 0.1 to 100k Hz. Fitting is carried out with equivalent circuit (bottom) showing series resistance ($R_s$), charge transfer resistance ($R_{CT}$), double layer capacitance ($C_{DL}$), and resistance and capacitance arising from the sample contact ($R_C$ and $C_C$).

On the larger scale, the resulting Nyquist plots from EIS show a fairly traditional capacitive picture, with near perpendicularity to the real impedance axis at the equivalent series resistance. This could be modelled with a simple RC series equivalent circuit, which is the simplified equivalent of real world conventional capacitors. Electrochemical interfaces are often modelled with additional elements, and for our expected electrode-electrolyte system we’ve adapted the simplified Randles circuit [145, 179, 180] with an interfacial charge transfer resistance in parallel to the double layer capacitance, along with the series resistance. This charge transfer resistance is observed to be very high – as expected for double layer capacitance – from the near perpendicularity of the graph towards lower frequencies; the larger semi-circle expected is not significantly observed. However, as the zoomed-in high frequency portion of the Nyquist plot (Fig. 5.9) demonstrates a small additional semi-circle at the high frequencies, we’ve added an additional parallel RC combination in series with
the simplified Randles circuit for our equivalent circuit model. This may be originating from the metallic contact at the back of the sample not being perfectly Ohmic, and thus having an associated capacitance and resistance.

Double layer capacitance values extracted from the equivalent circuit model fittings correspond well with the values extracted from the CVs, with capacitance values of 238 and 379 µF·cm⁻² respectively for the n- and p-type samples.

The charge/discharge curves (Fig. 5.10) also demonstrate good capacitive character, and the higher discharge time for p-type is reflective of the higher capacitance (as per Eq 4.1). Capacitances extracted from the GCD curve slopes are within the same region as the values obtained with CV and EIS, though slightly lower at 180 and 290 µF·cm⁻² for n- and p-type respectively. This could be accounted for by the observable IR drop due to series resistance being included in calculating the slope gradients. We can also extract power densities from the capacitance, EW and charge/discharge time, which turn out to be nearly identical at 291 and 293 µW·cm⁻² for n- and p-type respectively.

![GCD curves at 1 mA for the best performing n-type (black) and p-type (red) SOD treated SiNWA samples with nitric acid oxidation (NAOS).](image-url)
5.5. TiO$_2$ coatings on SiNWA

With the successful development and testing of a SiNWA electrode achieving a good capacitive character, with greatly improved capacitance through nanotexturing and stability through passivation, the appetite still remains to seek further improvement upon this. The coating material of Si oxide established in Section 5.4, though successful, remains to be an insulating material that can offer limited to no contribution in boosting the electrode capacitance.

An interest was developed in seeking alternative coatings that could be used in conjunction with the SiNWA electrode. Research into the more conventional carbon-based high surface area electrode materials have looked into surface coatings that can further boost their storage abilities. These include forming composite materials with surface coatings of transition metal oxide nanoparticles, such as Ru, Mn, Co, V, Ni, Ir, W, Mo, Ti, Sn, and Fe oxides [28, 181, 87, 182, 183, 184, 185, 186]. The combination of the carbon-based frame along with the nanoparticle coating form a constructive partnership; the good electrical and structural characteristics of carbon combined with the further increased surface area and/or faradaic nature for an additional dimension of charge storage of the nanoparticle coatings yield an appealing platform of improved capacitive performance.

Our SiNWA electrode offers similar benefits to the carbon platform for exploration of a composite electrode. A high surface area is achieved by the nanostructuration, and the SiNWA retains a robust mechanical character, with good conduction pathways, especially in a Si-based integrated system. The struggle that we face as opposed to carbon is, even with the use of a high stability IL electrolyte, unpassivated Si offers limited electrochemical stability. However, a sufficient nanoscale coating with a transition oxide material may allow for both passivation and capacitive performance improvement.

In line with our MACE etched SiNWAs, we look towards an available wet chemistry lab process without the use of any expensive vacuum equipment to coat our electrodes. A potential coating material to achieve this is TiO$_2$. TiO$_2$ nanoparticle coatings have been shown to provide electrode performance improvements on electrode materials such as multi-walled carbon nanotubes [187, 188, 189]. Therefore, with the ability to use wet, low temperature (<450 °C) processing, as well as additional advantages such abundance, low cost and environmental friendliness, we decided to explore the deposition of TiO$_2$ on our SiNWA electrodes for potential capacitance performance improvements.

5.5.1. Fabrication of TiO$_2$ coatings on SiNWA

Fabrication and testing of TiO$_2$ coatings was chosen to be done on the better performing p-type Si, with SiNWA samples etched as before, described in Chapter 4. Three different coating methods were attempted and investigated, with acknowledgement to the suggestions and guidance Dr Xiaoe Li. The
three methods involve differences in precursors, temperatures and mechanics, though with the same final step, and thus are expected to yield different results in both coverage and morphology.

Additional materials specific to the TiO₂ coatings include the Ti precursors of TiCl₄·2THF (97 %), Ti[OCH₂(CH₃)₂]₄ (97 %) and Ti foil (99.7 %, 0.25 mm thickness) purchased from Sigma-Aldrich, as well as acetylacetone purchased from Merck.

The three processes employed in coating the SiNWAs are:

- **TiCl₄ treatment [190, 191]:**
  - The sample (NW height of ~15 µm) was immersed in 10 ml of 0.04 M solution of titanium (IV) chloride tetrohydrofuran complex (TiCl₄·2THF) for 30 minutes in an oven at 70 °C, followed by a rinse with DI water and further baking at 450 °C for 30 minutes.
  - Elemental analysis using EDS yielded varying results of 0 - 0.12 %, 8 %, and 92 - 91.88 % for Ti, O and Si respectively.

- **Ti-dip procedure [192, 190]:**
  - The sample (NW height of ~10 µm) was immersed in a 10 ml solution of 0.2 M titanium (IV) isopropoxide (Ti[OCH₂(CH₃)₂]₄), 0.4 M acetylacetone and 12 M of ethanol absolute for 15 minutes. This was followed by immersion in DI water for 5 minutes before baking at 450 °C for 30 minutes.
  - The Ti-dip procedure was conducted 3 times on the sample to achieve better, more uniform, coverage of the SiNWA.
  - Elemental analysis using EDS for a single Ti-dip yielded values of 2 %, 10 %, and 88 % for Ti, O and Si respectively. The values for the 3x Ti-dip sample were 4.5 %, 13 %, and 82 % for Ti, O and Si respectively, indicating increased TiO₂ coverage.

- **Autoclave [193, 190]:**
  - The sample was immersed in a 30 ml solution of 0.1 M HCl containing a 0.1 g piece of Ti foil. This was placed into an autoclave, and heated at 180 °C for 4 hours, followed by a rinse with DI water and baking at 450 °C for 30 minutes.

A good initial look at the effects of the various coating processes on SiNWA can be provided with SEM imaging, shown in Fig. 5.11. A quick tells us immediately that all 3 samples have undergone a significant change in appearance from SiNWAs before coatings (see section 4.1.1). Although a low value of Ti is extracted from EDS measurements, we can see deposits of TiO₂ particles on the TiCl₄ treated samples. The sample is characterised by brittle and broken NWs, which are likely to a high packing quantity of the Ti cursor causing stress fractures on the NWs when expanded during the thermal process. Particle diameters vary between ~40 nm and ~550 nm. The 3x Ti-dip process shows
better survival of the original SiNWA structure, with small, circular TiO$_2$ nanoparticles (of ~135 nm diameter) distributed on the surface in an inhomogenous manner. The SEM of the autoclave sample displays the destructive effect of the high pressure of the autoclave process, with nearly all NWs being fractured and broken down to a significantly shortened height of no more than ~3 µm. This would cause a considerable reduction in the surface area advantage offered by the SiNWA. We do observe a discontinuous layer of TiO$_2$ covering the broken NWs; the layer is not in the form of nanoparticles and is less likely to provide a surface area advantage, especially with partial coverage blocking the NW surface area.
Figure 5.11 – SEM imaging of SiNWA samples coated with three TiO$_2$ processes of (a) TiCl$_4$ treatment, (b) 3x Ti-dip procedure and (c) autoclave. Inset of (a) shows a zoomed in portion highlighting TiO$_2$ particles amongst the broken NWs, whilst insets of (b) and (c) show top views of the TiO$_2$ nanoparticle and TiO$_2$ layer coverage respectively.
5.5.2. Results and Analysis

![Graph showing CV measurements]

Figure 5.1 – CV measurements at $v = 50$ mV/s of SiNWA electrodes coated with three TiO$_2$ coating processes of TiCl$_4$ treatment (black), 3x Ti-dip (red) and autoclave (blue).

CV scans of the samples conducted in the [Bmim][NTf$_2$] IL electrolyte are shown in Fig. 5.12. A clear observation is that the TiO$_2$ coating processes on the SiNWA do not yield similar results. This is as expected, especially with the differences seen in the SEM images (Fig 5.11). We observe wide EWs of >2 V for all samples, with widths of TiCl$_4$ < autoclave < 3x Ti-dip. The better coverage of the 3x Ti-dip sample seems to have resulted in better passivation of the SiNWA.

The current for the autoclave sample can be seen to be drastically lower than the others for the autoclave sample, as expected from the much lower surface area of the broken NWA. The 3x Ti-dip sample gives a very good quasi-rectangular shape as expected for a capacitor, along with its wide EW and largest minimum current value. This is indicative of a potentially strong capacitive performance. The TiCl$_4$ treated sample shows a non-standard shape with the appearance of apparent redox peaks. These peaks are associated with the presence and influence of deep level traps in the SiNWA surface, as covered in [1] and Chapter 6 of this thesis. Although the effect of these traps may add to improved extracted capacitances and energy storage ability by certain methods of measurement,
they have also demonstrated weaker cycling stability and capacitance retention, in addition to their non-standard charge-discharge character.

Table 5.6 – EWs and extracted capacitances of the SiNWA samples with TiO$_2$ coatings.

<table>
<thead>
<tr>
<th>Sample</th>
<th>EW (V)</th>
<th>Extracted Areal Capacitance (µf·cm$^{-2}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>CV</td>
<td>EIS</td>
</tr>
<tr>
<td>TiCl$_4$ treatment</td>
<td>2.0</td>
<td>484</td>
</tr>
<tr>
<td>3x Ti-dip</td>
<td>2.6</td>
<td>360</td>
</tr>
<tr>
<td>Autoclave</td>
<td>2.4</td>
<td>21</td>
</tr>
</tbody>
</table>

In addition to the minimum current difference values of CV scans, EIS measurements at the potential of minimum current difference and CP charge-discharge measurements were used to extract areal capacitance values for the samples, shown in Table 5.6. We can see that the non-standard shape of the TiCl$_4$ sample gives large disparities in the values measured, ranging from a low of 90 µf·cm$^{-2}$ to a high of 1281 µf·cm$^{-2}$, demonstrating the difficulty in accurately assessing its EDLC equivalent value. The autoclave sample has yielded consistent, yet very low values of capacitance across the measurements, being <10x higher than bulk Si capacitances we’ve measured; the desired high surface area effect of the SiNWA to boost capacitance has been negated.

The key achievement of the coatings has been realised by the 3x Ti-dip coated SiNWA electrode. Consistent and substantial areal capacitances of up to 386 µf·cm$^{-2}$ are measured, with a wide EW of 2.6 V. The near ideal quasi-rectangular shape with lack of any apparent redox activity gives good cyclability. Aims of a high capacitance with the increased surface area with the nanoparticle deposits as well as good passivation of the SiNWA has been achieved. It is well worth noting as well that the shorter NW height of ~10 µm yields better volumetric and gravimetric specific capacitances for the electrode compared to the top performing SiO$_2$ coated SiNWA electrode in [3], with values of 386 mF·cm$^{-3}$ and ~0.9 F·g$^{-1}$. This also yields us much improved extracted densities of energy and power, at 0.9 Wh·kg$^{-1}$ and 2228 W·kg$^{-1}$ respectively, placing it very well towards the frontier of the EC range of the Ragone plot (Fig. 1.1).
6. FURTHER ANALYSES

In the previous chapter, we explore the stages gone through in the initial development of the SiNWA electrode, with high capacitances comparable to expected EC or supercapacitor values being achieved in terms of both energy storage and power densities. SiNWA electrodes with post-etch spin-on doping (SOD) application and a thin oxide coating with nitric acid oxidation of silicon (NAOS) for stability proved to be our best performing electrode thus far, with capacitances of up to 404 µF·cm⁻² (~0.7 F·g⁻¹) [3]; the top performing sample yielding energy storage and power densities of 0.23 Wh·kg⁻¹ and 651 W·kg⁻¹ respectively.

Further to this, we decided that looking into further improvements based on the process parameters used could help us fine tune the electrode to achieve an even better performance. Parameter variations could be investigated in processes such as the doping and oxidation steps. This chapter explores the investigations into these, as well as further analysis and deductions based on the results found. Beginning with looking into various dopants with the aim of identifying the one yielding the best results, we begin to further observe, identify, and speculate upon the appearance of peaks present in the CV scans of the samples. This encompasses efforts into combating/removing them, looking into the nature and cause of them, and their impact on the capacitive performance of the SiNWA electrode.

6.1. Investigating Additional Parameters

6.1.1. Effects of Varied SODs

The first and seemingly most straightforward parameter to investigate was decided to be that of the doping involved in the electrode fabrication (Section 5.2). SOD application has shown to boost the capacitances of the electrodes, as well as making a major contribution into reducing the series and contact resistances. Along with having shown to respond better to the SOD process and yield higher capacitances, we choose to focus on p-type Si substrates for our electrode development for this stage as a variety of p-dopants are more commonly used (and are relatively safer to handle). In addition to boron, we have the subsequent Group III elements of aluminium and gallium suitable for SOD application. The process is described in Section 4.1.2.

6.1.1.1. Single SODs with NAOS at Boiling Point

Initial fabrications were carried out with the 3 p-type SODs on SiNWA samples from the same batch of fabrication, with a 4th sample from the batch acting as a control for comparison. These underwent the NAOS process at the boiling point of the azeotropic HNO₃ mixture, as found in literature (Section
The resulting samples were characterised in [Bmim][NTf2] electrolyte with CV, and the resulting scans are shown in Fig. 6.1.

Figure 6.1 – CV measurements at $v = 50$ mV/s of SOD and 120 °C NAOS treated SiNWA electrodes, with the SOD dopant atom of boron (red), aluminium (blue) and gallium (green) in comparison with an equivalent control sample without SOD (black).

It is observed that apart from the Ga doped sample, the 3 other samples scanned display what appears to be redox peaks on either side of the centre. This CV shape diverges from the classical quasi-rectangular shape expected from the CVs of electrostatic or double layer capacitors, where no faradaic processes are involved. This leads to difficulties in accurately assessing the double layer capacitance equivalent value for these electrodes.

In terms of CVs, a conservative estimate to take would be using the current minima – which can be seen to be located between the cathodic and anodic peak features – and using these values as our equivalent for the expected equivalent quasi-rectangular CV. Admittedly, this causes us to run the risk of underestimating the capacitance, though this is deemed to be safer than the converse of it. This point of extraction shall also be applied to conducting our EIS measurements, i.e. the potential at which this minimum current difference occurs. The limitation of this is that characterisation occurs at a single point, and as EIS at other potentials within the EW shall yield different results, this perhaps cannot be taken as completely representative of the electrode’s performance.
For this reason, and for providing us with additional information as well, it is useful for us to conduct chronopotentiometry – also known as galvanostatic charge/discharge – measurements on the sample. This measurement encompasses the full EW window, and thus is likely to provide us with an increased extracted capacitance value due to incorporation of any faradaic processes in the results. Therefore despite, or rather because of, the disharmony between the extracted values from the techniques employed, it is useful to look at the various techniques in order to form assessment on the sample.

Table 6.1 – EW and extracted areal capacitance measurements for SiNWA electrodes with single or no SOD treatments with various dopant atoms and NAOS coating at 120 °C.

<table>
<thead>
<tr>
<th>Sample</th>
<th>EW (V)</th>
<th>Extracted Areal Capacitance (µF·cm⁻²)</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>No SOD</td>
<td>2.8</td>
<td>799</td>
<td>198</td>
</tr>
<tr>
<td>B SOD</td>
<td>3.2</td>
<td>361</td>
<td>132</td>
</tr>
<tr>
<td>Al SOD</td>
<td>3.5</td>
<td>813</td>
<td>249</td>
</tr>
<tr>
<td>Ga SOD</td>
<td>3.5</td>
<td>776</td>
<td>645</td>
</tr>
</tbody>
</table>

With the results of extracted capacitances (Table 6.1), we can see a pattern, and note the differences between the samples with and without the peak features present. As anticipated for them, the EIS measurements yield a drastically lower value than the ones extracted for them by CP, as CP takes the full CV scan into account. The EIS readings taken from in between the peaks however, show even a lower capacitance extracted than the ones from the minimum current differences. Whether this is truly due to a low double layer capacitance for the sample, a cancelling out of the capacitance effect measured at the potential, or most likely, an unrepresentative equivalent circuit due to the processes involved in the peaks not being adequately represented.

Amongst the positive results that we can draw from the measurements is that in all cases, we continue to the significant effect of nanotexturing on the charge storage ability of the electrode, with even the lowest capacitance values extracted from the EIS measurements, with the capacitance boost being at least two orders of magnitude above bulk value. Another factor we see is that the EWs of the samples are all substantially boosted. This is especially true with the samples that have undergone SOD, as the EWs are approaching the value expected of the IL itself of ~4 V. This indicated that the NAOS oxide layer has provided additional stability for the Si electrode, and also perhaps that the electrolyte has been sufficiently dried to achieve this, giving good indication of promising real world device performance. The contrast between the windows of the SOD and non-
SOD samples (EW difference of 0.4-0.7 V) also indicates that the SOD process may be contributing to the passivation of the electrode.

To cap this all off, we see with the Ga doped sample not showing the presence of peaks, we have achieved a new best capacitance value, corroborated by closely corresponding CV and EIS extracted capacitance values. Even with the EIS value taken into account, this gives us an improved areal capacitance value of 645 µF·cm⁻² (≈1.6 F·g⁻¹), highly comparable with expected EDLC capacitances and with a wide (3.5 V) EW to accompany it. It should be noted that a repetition of the fabrication of this sample with similar conditions yielded peaks, and performance values within the range of the other samples showing peaks, most similar to the B SOD sample and thus still being less affected by peaks than the sample without SOD or the Al SOD sample.

6.1.1.2. Single SODs with NAOS at 90 °C

In our initial development and testing of NAOS coated SiNWA electrodes (Section 5.4), we made the observation that a sample oxidised at a lower temperature of 90 °C demonstrated near EDLC behaviour, with NAOS at boiling point on p-type Si leading to the appearance of the peaks. Therefore, our next iteration of testing was decided to be to fabricate the samples with the different p-type dopants (as in the previous section) at the lower oxidation temperature. Oxidation at the two temperatures occur with the slight difference of how vigorous the oxidation occurs; NAOS at 90 °C occurs with the nitric acid fuming but not bubbling, and the reaction is not as vigorous. Samples were fabricated as before, with B, Al and Ga doped SiNWA samples along with a sample without SOD being characterised.
Figure 6.2 – CV measurements at $v = 100 \text{ mV/s}$ of SOD and $90 \degree \text{C}$ NAOS treated SiNWA electrodes, with the SOD dopant atom of boron (red), aluminium (blue) and gallium (green) in comparison with an equivalent control sample without SOD (black).

The CV scans of these samples oxidised at the lower temperature are seen in Fig 6.2, and a number of apparent observations can be drawn from it. Firstly, the SOD application does seem to have an impact on the probability for the appearance of the peaks, as all 3 SOD samples show little to no redox features. The sample without SOD application again shows significant electrochemical activity, which is reflected in the extracted performance parameters in Table 6.2. It would also appear that oxidation at the lower temperature appears to have mitigated the appearance of peak features, with only the no SOD sample demonstrating significant peaks.

**Table 6.2 – EW and extracted areal capacitance measurements for SiNWA electrodes with single or no SOD treatments with various dopant atoms and NAOS coating at 90 °C.**

<table>
<thead>
<tr>
<th>Sample</th>
<th>EW (V)</th>
<th>Extracted Areal Capacitance ($\mu\text{F} \cdot \text{cm}^{-2}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>CV</td>
</tr>
<tr>
<td>No SOD</td>
<td>2.5</td>
<td>603</td>
</tr>
<tr>
<td>B SOD</td>
<td>2.7</td>
<td>192</td>
</tr>
<tr>
<td>Al SOD</td>
<td>3.8</td>
<td>197</td>
</tr>
<tr>
<td>Ga SOD</td>
<td>2.1</td>
<td>315</td>
</tr>
</tbody>
</table>
In terms of performance parameters, we can again observe a number of positives. All three samples demonstrate areal capacitance values of the same order, though not exceeding values previously reached. The Ga SOD sample again demonstrates strong capacitive performance, with current and capacitance values achieved being greater than that of the other two SOD types. However, the B and Al samples show greater consistency across the extraction techniques, with near identical CV and CP values. This could possibly be explained by the minimal faradaic activity observable on the Ga SOD sample but absent in the B and Al SOD ones. In terms of the EWs, we see that all the NAOS samples are still able to achieve values of over 2 V in the IL electrolyte, with the Al SOD sample reaching a particularly strong 3.8 V, very near the IL’s EW and thus possibly only limited by it.

Table 6.3 – Extracted areal capacitance measurements for repeat fabrications of SiNWA electrodes with single or no SOD treatments with various dopant atoms and NAOS coating at 90 °C.

<table>
<thead>
<tr>
<th>Sample</th>
<th>Extracted Areal Capacitance (µF·cm⁻²)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>CV</td>
</tr>
<tr>
<td>B SOD repeat</td>
<td>697</td>
</tr>
<tr>
<td>Al SOD repeat</td>
<td>671</td>
</tr>
<tr>
<td>Ga SOD repeat</td>
<td>331</td>
</tr>
</tbody>
</table>

As the repeated sample at the higher temperature yielded peaks, and as we wanted to ensure that the lower oxidation temperature has actually helped in mitigating them, we decided to fabricate another batch of the samples with the 3 types of SOD applied. This time, all 3 repeated samples demonstrated the presence of these peaks, with similar performances as has been seem with them before. The Ga SOD sample has again seemed to have not been affected as much by the peaks, though it has shown itself susceptible to it as well, albeit to a lesser extent.

In conclusion, we have been able to observe that faradaic peaks can occur with NAOS oxidised SiNWA electrodes, both at azeotropic nitric acid’s boiling point and at a lower oxidation temperature. Peaks can also be present with different dopant atoms, though it seems that all doping processes seem to contribute to mitigating the effect of the appearance of these peaks, and aid in moving towards a more conventional capacitive electrode character.

In terms of moving forwards there are three things to consider. Firstly, whether the doping steps can further aid mitigating the effect of the faradaic peaks that appear. Secondly, whether the oxidation temperature truly plays a role in mitigating them. And, most significantly, that continuing to work towards eliminating the faradaic peaks should enable us to hypothesise on the origin of these peaks, the cause of which is yet unknown in this instance.
6.1.1.3. Multiple SODs with NAOS

We have thus far been able to observe that the application of SOD on the electrodes seems to produce better capacitive performance on our SiNWA electrodes. This includes the apparent reasons such as lowering the series resistance (e.g. at the contacts), as well as the hypothesis that they are able to help mitigate the appearance of faradaic peaks that have been observed frequently with the SiNWA electrodes. Thus far, SOD applications have been carried out a single time on each side of the electrodes. Studies with Si based thermoelectric generators have shown that multiple SOD applications can provide additional benefit to performance [62]. We therefore decided to experiment on carrying out multiple SODs on our SiNWA electrodes before characterising their performance in the IL electrolyte, to see if any additional capacitance or stability benefits are attained.

Figure 6.3 – CV measurements at $v = 100$ mV/s of 3x SOD applied and NAOS treated SiNWA electrodes, with the SOD dopant atom of boron (red), aluminium (blue) and gallium (green).

SOD application is carried out as prior, with the exception being that the process was repeated 3 times. CV scans (Fig. 6.3) of the samples with all 3 types of dopants show a similar story; a wide EW is achieved without the appearance of any significant faradaic peaks. As with the 90 °C single SOD samples without peaks, the EW widths are in the order of Ga < B < Al, indicating that the type of dopant atom may have a minor effect on the stability, though all types have demonstrated high EWs approaching the IL's window. Extracted capacitance values (Table 6.4) show that a consistent set of values are achieved,
which are similar across all 3 samples, suggested that the dopant atom isn’t a main contributing factor in determining the capacitance. The capacitance values are similar to those previously achieved, though not exceeding them.

Table 6.4 – EW and extracted areal capacitance measurements for repeat fabrications of SiNWA electrodes with multiple SOD treatments with various dopant atoms and NAOS coating.

<table>
<thead>
<tr>
<th>Sample</th>
<th>EW (V)</th>
<th>Extracted Areal Capacitance (µF·cm⁻²)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>CV</td>
</tr>
<tr>
<td>3x B SOD</td>
<td>3.1</td>
<td>254</td>
</tr>
<tr>
<td>3x Al SOD</td>
<td>3.3</td>
<td>201</td>
</tr>
<tr>
<td>3x Ga SOD</td>
<td>2.5</td>
<td>225</td>
</tr>
</tbody>
</table>

We have observed that doping steps carried out multiple times can help with device character, in preventing the appearance of faradaic activity when cycling. However, a marked improvement in the capacitance value is not observed, with capacitances being similar to those achieved previously, indicating that multiple SOD application provides no additional benefit to capacitance.

The reason why multiple SOD applications can provide this sort of passivation leads us to a couple of ideas. It is possible that the presence of additional dopant atoms alters the character of the Si surface, changing its nature to eliminate or mitigate the cause of the peaks. Another explanation could be that repeated surface modification – with multiple oxidations and removals of that oxide – causes the removal of whatever feature was causing the peaks. What both these explanations would indicate, especially the latter, is that whatever causing the peaks lies within the nanowire surface layer on the electrode side.

At this point, our primary interest lies in identifying and analysing the nature and significance of the faradaic peaks occurring in our SiNWA high capacitance electrodes. Moving forwards, aspects to look at would include re-testing the effect of NAOS temperature on peak appearance, examining whether the root of it lies in the nanostructuration process, and looking into surface modifications that could help mitigate the appearance of these peaks.

6.1.2. Effect of Varied Oxidation Temperatures

Following prior investigations, a brief examination into whether the temperature has any significant effect on peak appearance was conducted. Samples were oxidised in NAOS at the investigated temperatures of the azeotropic boiling point and 90 °C, as well as at room temperature. The samples chosen are SiNWA samples which have not undergone SOD.
CV scans of the 3 samples indicate a similar character, with all 3 samples showing peaks and having roughly the same shape and width. The EW appears to be wider with NAOS at the higher temperature, though the peaks appear to be more prominent as well. The similarity of NAOS oxidised SiNWA at all three temperatures is further confirmed by the extracted capacitance values (Table 6.5), with the same patterns seen across all three temperatures, as well as similar values.

Table 6.5 – EW and extracted areal capacitance measurements for SiNWA electrodes with NAOS treatment at varied temperatures.

<table>
<thead>
<tr>
<th>Sample</th>
<th>EW (V)</th>
<th>Extracted Areal Capacitance (µF·cm⁻²)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>CV</td>
</tr>
<tr>
<td>Room Temp</td>
<td>2.6</td>
<td>707</td>
</tr>
<tr>
<td>90 °C</td>
<td>2.5</td>
<td>603</td>
</tr>
<tr>
<td>120 °C</td>
<td>2.8</td>
<td>199</td>
</tr>
</tbody>
</table>

6.1.3. Effect of Nanostructuration

The MACE process that that results in the formation of the SiNWA is the major process causing the structural change of Si in our electrodes. It involves chemically induced change to the structure, as

Figure 6.4 – CV measurements at $v = 50$ mV/s of SiNWA electrodes with NAOS treatment at varied temperatures of room temperature (red), 90 °C (blue) and 120 °C (black).
well as physical forces to a lesser extent. Thus, the MACE process is very likely to be responsible for the appearance of the faradaic peaks. A quick way to examine this to an extent would be to repeat the sample fabrications in which peaks were observed, but with no nanostructuration. We therefore fabricate a number of samples with the same cleaning and SOD processes, omitting just the MACE step. All three p-dopants used (B, Al and Ga) as well as a bulk sample without SOD are characterised in the electrolyte.

It can be clearly seen that all bulk samples tested demonstrate no peaks appearing in the CV scans (Fig 6.5). Similar EWs of >3 V are achieved (3.0-3.4 V), as well as capacitances of between 6-8 µF·cm⁻², as expected of bulk Si. The lack of any peaks appearing lends further credence to the MACE process having a causal link with them.

Figure 6.5 – CV measurements at \( v = 100 \text{ mV/s}\) of SOD and 120 °C NAOS treated bulk Si electrodes, with the SOD dopant atom of boron (red), aluminium (blue) and gallium (green) in comparison with an equivalent control sample without SOD (black).
A further aspect of this that was examined was to partially conduct the MACE process, but without the nucleation of Ag particles onto the surface. Thus, no mask for nanostructuration is laid, and also, there is no catalyst to carry out the faster etching. A bulk sample left in the etch bath for an hour as with other samples is tested, with all the same fabrication processes except the step for nucleation of Ag. The sample shows some visible signs of having been undergone processing; etching would have occurred at a slower rate.

The CV scan of this sample (Fig 6.6) shows a reasonably conventional pseudo-rectangular capacitive shape, with an EW of 2.4 V. The current and capacitance magnitude is substantially higher than the bulk samples without the etch step (~100 µF·cm$^{-2}$), which can be attributed to surface roughness caused by the etch step. Most notably, there is an absence of any substantial redox features appearing; the absence of nanowires without the metal Ag particles could have resulted in the lack of peaks.

6.1.4. Effect of Alternative Oxidation

Another attempted variation on process that could potentially alter the character of the electrode is a change in the oxidation process. So far, we have been mostly applying a chemical NAOS process, in
order to yield an ultrathin oxide of high density. A thermally grown oxide is usually the oxidation of choice for a highly dense, and well passivated oxide, but suffers from having a high minimum thickness when carried out conventionally in ovens. Though it may not be possible to achieve the approximately single nanometre thickness attainable with NAOS (except perhaps with a highly controlled low oxygen atmosphere such as in [194]), it is possible to achieve thicknesses of no more than a few nanometres (≤6 nm, possibly going down to as low as 2 nm [195, 196, 197, 198]) with a particular means of thermal oxidation. This would be to carry out the oxidation with Rapid Thermal Annealing, a process that we shall designate as Rapid Thermal Oxidation (RTO).

6.1.4.1. Single Rapid Thermal Oxidation (RTO)

RTO is carried out during the fabrication of a SiNWA electrode in place of the NAOS step by a quick high temperature anneal process inside a Rapid Thermal Annealer. The sample is oxidised in a purged oxygen atmosphere, with the temperature being rapidly ramped up to 800 °C and held just above for 1 minute before a rapid cooldown. The sample is characterised as usual in the IL electrolyte.

![Graph](image)

*Figure 6.7 – CV measurements at v = 100 mV/s of SiNWA electrodes with varied oxidations of RTO (red) and NAOS treatment at 120 °C (black).*
A comparison of the CV scans of the RTO oxidised sample with a NAOS oxidised sample is shown in Fig 6.7. There appears to be a marked difference in character, especially in terms of magnitude. The EW (2 V) and current values of the sample are both lower, with the lower current indicating lower capacitance as well. The lesser current/capacitance is as expected due to the greater thickness that even RTO would yield in comparison to NAOS. However, the capacitance values do not lag too far behind, with the values being of the same order of magnitude.

Table 6.6 – EW and extracted areal capacitance measurements for a SiNWA electrode with RTO.

<table>
<thead>
<tr>
<th>Sample</th>
<th>EW (V)</th>
<th>Extracted Areal Capacitance (µF·cm⁻²)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>CV</td>
</tr>
<tr>
<td>RTO</td>
<td>2.0</td>
<td>306</td>
</tr>
</tbody>
</table>

What is particularly interesting, is that even though with the smaller currents, and perhaps smaller magnitude of the features, that the redox peaks are still apparent in the CV scan. That the nature of these are similar is further confirmed in the character observed with the different measurement techniques (Table 6.6). The difference in oxidation technique and packing density does not seem to have prevented the appearance and effect of the peaks. This confirms that the origin of them does not lie with the chemically done NAOS process, but rather with a previous step in the fabrication.

6.1.4.2. Multiple RTOs with NAOS

Even though RTO has not shown to prevent the appearance of peaks, we thought it could potentially be useful in helping to eliminate them post-presence, as with the multiple SOD applications. If the multiple SOD applications primarily helped in terms of removing the top layers of the SiNWA surface through repeated oxidation and removal, carrying out multiple RTO oxidations and removing the grown oxide layer might allow us to strip a few nanometres off the surface. This could help eliminate the cause of the peaks, if present in this surface layer.

We fabricate a sample with RTO oxidation and subsequent removal of the oxide layer in dilute HF, carried out twice. This is expected to oxidise ~5 nm of the Si surface layer, which is removed. The samples are then oxidised with NAOS as the final step before being characterised with the electrolyte. This is so that the fabricated sample will end up with an ultrathin oxide layer, instead of the thicker RTO layer, and shall be comparable with other NAOS samples.
Figure 6.8 – CV measurements at $\nu = 100$ mV/s of SiNWA electrodes with 2x RTO and oxide strip followed by 90 °C NAOS (red), 3x B SOD followed by 90 °C NAOS (blue) in comparison with NAOS treatment at 90 °C (black).

We compare the sample with 2x RTO and removal followed by NAOS with a 3x SOD sample (hence having undergone multiple oxidation and removal steps), as well as the no SOD SiNWA sample oxidised in NAOS at high temperature (Fig 6.8). We note that the double RTO oxidation and removal has not resulted in the elimination of peaks. However, the magnitude of the peaks have reduced, which is more notable when comparing the ratio of peak to minimum current. The value is significantly smaller (1.6 as opposed to 2.4) compared to the single NAOS sample, indicating that the multiple oxidation is likely to have had a positive effect in mitigating the cause and presence of the peaks, though not completely eliminating them. Furthermore, the EW achieved (2.3 V) is not as high as most of the NAOS samples characterised.

6.1.5. Effect of Electrolyte

Though the hypothesis relates to the appearance of the peaks being electrode related, a brief investigation into the impact the electrolyte may have on the peaks was conducted. For this, a sample with known peaks was chosen, for observation of whether the appearance and nature of the peaks change with electrolyte. A supplementary benefit of this investigation is that it would also enable us to observe the suitability of our chosen electrolyte in comparison to others.
The sample chosen is a non-SOD SiNWA sample with NAOS treatment at the azeotropic boiling point. The measurements conducted with our [Bmim][NTf₂] electrolyte were contrasted with 3 others of 3 different natures: an aqueous, organic and another IL electrolyte. These are:

- **Aqueous:** 0.5 M Sodium Perchlorate (NaClO₄) solution
- **Organic:** 0.5 M Lithium Perchlorate (NaClO₄) in propylene carbonate (PC)
- **Ionic Liquid:** 1-Ethyl-3-methylimidazolium hydrogen sulphate ([Emim][HSO₄])

![Figure 6.9](image)

**Figure 6.9 – CV measurements at v = 50 mV/s of a SiNWA electrode with NAOS treatment at 120 °C with 4 different electrolytes: an aqueous 0.5 M NaClO₄ solution (red), organic 0.5 M NaClO₄ in PC solution (blue), [Emim][HSO₄] ionic liquid (green) and [Bmim][NTf₂] ionic liquid (black).**

The CV plot of measurements with the different electrolytes shows some notable features. Firstly, determining the nature and appearance of the peaks to be related to the electrolyte as opposed to the electrode can be ruled out. With all 4 electrolytes measured of different natures, the peaks are present and appear to be similar in nature.

A more interesting comparison between the electrolytes related to capacitive performance, especially in the character of electrode stability with the electrolyte and the EW achieved. With the exception of the [Emim][HSO₄] electrolyte, the electrolytes appear to achieve similar values of
current, with the extracted minimum current between the three ranging from 72-111 µA, as opposed to a lower value to 43 µA for [Emim][HSO₄]. The lower comparative current is especially notable considering the plot as a whole, including regions outside the minimum current point.

The unsuitability of [Emim][HSO₄] as an electrolyte becomes even more apparent when considering system stability, as along with having the lowest capacitive current by a significant margin, it also has a significantly lower EW of 1.6 V, just 0.1 V above the low EW achieved with the aqueous electrolyte (see Table 6.7). These factors may be attributed to higher system resistivity and water content, as [Emim][HSO₄] has higher viscosity (~31x at 25 °C [199, 200]) and tested hydrophilicity (~18x [156]) compared to our [Bmim][NTf₂] IL electrolyte.

Table 6.7 – Extracted EW measurements for a 120 °C NAOS treated SiNWA electrode with various electrolytes (see Fig. 6.9).

<table>
<thead>
<tr>
<th>Electrolyte</th>
<th>EW (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.5 M NaClO₄ (aqueous solution)</td>
<td>1.5</td>
</tr>
<tr>
<td>0.5 M LiClO₄ in PC (organic solution)</td>
<td>2.0</td>
</tr>
<tr>
<td>[Emim][HSO₄] (ionic liquid)</td>
<td>1.6</td>
</tr>
<tr>
<td>[Bmim][NTf₂] (ionic liquid)</td>
<td>2.8</td>
</tr>
</tbody>
</table>

The organic electrolyte achieves an improved EW by 0.5 V over the aqueous electrolyte, but is still significantly (0.8 V) lower than the EW of 2.8 V achieved by the hydrophobic [Bmim][NTf₂] IL electrolyte. With the current values achieved also showing no marginal gain with other electrolytes, and with its EW being the widest of the electrolytes investigated by a large margin, the use of [Bmim][NTf₂] continues to be justified for the SiNWA system, even after a protective coating layer is applied.

6.2. Analysing and Identifying Redox Peaks

6.2.1. Analysis of Potential Causes

Throughout the course of the investigations into additional parameters, we have observed the appearance of features present in our SiNWA electrodes in the form of redox peaks apparent in the CV scans. Though they are not universally present, their presence is frequent enough to become a significant issue in electrode utility. The presence of these peaks cause the electrodes to diverge from the traditional quasi-rectangular CV scan observed with EDLCs and conventional capacitors; they do not display the expected behaviour of capacitors. Peak presence results in difficulty in obtaining a truly objective value of the capacitance, due to the limitations in and differences in results seen with various measurement techniques.
With the multiple parameters looked into in Section 6.1 – many of them in order to try and eliminate or mitigate the appearance and effects of these peaks – we have also been able to draw a number of observations, conclusions and hypotheses that may allow us to understand, identify and potentially eliminate the appearance of the peaks if desired. These include being able to rule out a number of factors that may have resulted in the yet unknown appearance of them.

Amongst the processes and parameters involved in electrode fabrication, we have managed to rule out factors such as: 1) it being due to the substrate nature, as bulk Si does not exhibit the same behaviour even under similar processing and conditions, 2) it being caused by the NAOS process or its temperature, as it was observed at different temperatures and with an alternative thermal oxidation process, 3) it being subject to the conditions and chemicals of the etch bath of the MACE process, 4) it being a result of the dopant atom of post-etch SOD, and 5) it being a result of the SOD process itself, as evidenced by comparisons with and without SOD. If anything, the application of SOD has been seen to mitigate the appearance of the peak in certain cases, especially with multiple application.

This leaves us with the process of nanotexturing by MACE as being the most likely cause of the peaks. The involvement of the metal particles for it and the catalytic processes and effects involved have not been ruled out as potential causes. Also, in terms of mitigating it, we have seen results with some processes, which may give us an additional idea. Multiple processing steps such as oxidation and removal of the surface oxide layer – either as a standalone process or as part of SOD – has shown to help reduce the effect of peaks. This could be due to the removal of the cause in the surface layers of the SiNWs. Furthermore, post-etch doping seems to have an even more prominent effect on this, with multiple doping steps eliminating the peaks and even single doping steps contributing greatly towards that. This could indicate that a change in the semiconductor nature of the electrode could be contributing to the elimination of the peaks as well.

In light of this, it has been suggested that the cause of the peaks could lie with the presence of trap levels present within the bandgap of the Si surface in the electrode. MACE fabrication of SiNWAs can result in a considerable quantity of dangling bonds and surface defects, leaving them present in a high density especially with the greatly increased surface area [201, 202]. These can result in a high of energy trap levels on the SiNWAs surface, in contact with the electrolyte. Literature also shows that the MACE process, with involvement of metals, can introduce additional trap levels known as deep level traps (DLTs) [203, 204]. As our process involves the use of Ag within MACE, investigating this as a possibility was deemed prudent. The presence of a DLT centre within our SiNWA electrodes could potentially be sought out and established with the aid of low frequency noise measurements to identify the associated generation-recombination (G-R) centre.
6.2.2. Low Frequency Noise Analysis

Measurements of noise at low frequency were carried out with the aid of an SR770 FFT spectrum analyser, with the noise spectral density obtained between frequencies ranging from 1 mHz to 100 kHz. Measurement setup included the load resistor $R_L$ in series with the SiNWA electrode from which to measure the spectral density $S_V$, and the SiNWA electrode, using the custom built electrochemical cell as with the capacitance characterisation, placed in a Faraday cage. Contact was made with the NWA with a 3mm diameter spring loaded Au top probe sit onto a cell cap, with the back contact as normal, with the Cu back plate being in contact with the sample’s metallic back contact. A zero-bias setup was used to measure and deduct background noise from total noise for the results. For measurements, devices were biased with a battery at 1 V [205]. Noise spectral density of short circuit current fluctuations, $S_V$, was calculated using the load resistance and the sample’s differential resistance $R_D$ using Equation 6.1.

\[
S_I = S_V \left[ \frac{R_L + R_D}{R_L \times R_D} \right]^2
\]

Equation 6.1 – Calculation of noise spectral density for sample using load resistance

Results of the normalised noise spectral densities are shown in Fig. 6.9 with a sample with peaks being contrasted with a sample that has undergone multiple doping steps and does not display them. Both samples exhibit high levels of noise towards the lower frequencies, attributed to a near continuous distribution of trap levels in the bandgap of the NW surfaces. Whilst the $1/f^\alpha$ spectrum in Fig. 6.10b for the sample without peaks shows a single slope character with $\alpha=1$, the $1/f$ spectrum in 6.10a for the sample with peaks shows a clear difference, with a sharper slope of $\alpha=2$ at intermediate frequencies being an indication of a strong G-R centre. The peak in the inset allows us to identify the position of this G-R centre, with a lifetime of approximately 5 s being extracted, establishing that a strong trapping centre is present in the SiNWA.
Figure 6.10 – Normalised current noise spectral density vs frequency (log-log) for the NWAs showing peaks (a) and degenerately doped NWAs with no peaks (b). Dashed lines give spectrum slopes of 2 and 0.9 for (a) and 1 for (b). Inset of (a) gives normalised current spectral noise multiplied by frequency, with the peak position determining the characteristic trap level’s lifetime of ~5 s [1].

Confirmation of the presence of this G-R centre allows us to understand why multiple doping may have contributed to eliminating the appearance of the peaks. The influence of the centre can be lessened or even avoided by shifting the Fermi level away from this centre, which can be achieved by doping to an extent in which the Fermi level is shifted into the valence band, i.e. degenerately doping the sample. The absence of any significant redox activity with multiple doping steps, regardless of doping atom, as well as the absence of the G-R centre signal from the noise spectrum of these samples corroborates well with the hypotheses that the effects of the DLT is linked to the redox activity observed with the electrode-electrolyte system [206].

We can associate the presence of these DLT states with the presence of residual Ag particles left from the MACE process. It has also been reported [202] that low concentrations of Ag can cause DLT states in the Si bandgap. The use of Ag in MACE and the established presence of the DLT states in our SiNWA suggest the presence of residual Ag causing this.

The question of the electron transfer process involved in this is still unclear, as since the redox activity is observed within the EW, we cannot attribute the involvement of the IL electrolyte, as electron transfer to/from either cation or anion would occur outside this potential window. A suggested alternative explanation is the presence and involvement of adsorbed water on the SiNWA. Previous work [62] has shown the presence of water in the SiNWA, even in vacuum. This may be exacerbated in our system with the hydrophilic nature of the oxidised surface and presence of trace
amounts of water in the IL. This adsorbed water, rather than the IL, could provide the necessary donor and acceptor levels to equilibrate with the DLTs [207], with electron transfer via surface states.

\[
\begin{align*}
\text{Figure 6.11} & \quad \text{Energy band diagram sketch for SiNWAs with} \ a) \ \text{non-degenerate and} \ b) \ \text{degenerate doping.} \ 1, 2 \ \text{and} \ 3 \ \text{gives equilibrium, positive and negative bias respectively.} \ a \ \text{(acceptor)} \ \text{and} \ d \ \text{(donor)} \ \text{are the associated Ag related trap levels.} \ N_T \ \text{refers to trap density, with superscripts of} \ T \ \text{referring to a charge neutral donor trap either being filled with electrons (0) or empty (+)} [1].
\end{align*}
\]

Fig 6.11 shows energy band diagrams of the Si-electrolyte interface with adsorbed water (based on model proposed in [208]) for both degenerately and non-degenerately doped SiNWAs, with common Ag associated trap levels in Si of \(~0.56\) eV below the conduction band edge (acceptor state) and \(~0.23\) eV above the valence band edge (donor state) shown [209, 210]. The high density of surface states result in the pinning of the Fermi level [211], which in turn means that the external voltage shall primarily drop across the electrolyte, and the space charge region is independent of bias. Differences in the equilibrium space charge region are due to surface depletion of MACE etched p-Si SiNWAs [212], with less depletion seen with degenerate doping.

The position of the Fermi level is crucial to the involvement of the trap levels in the cycling process. With the Fermi level lying above the valence band for non-degenerate doping, we have an initial filled donor trap level at equilibrium, which releases its electrons into the electrolyte (water).
acceptor level under positive bias. Cycling back under opposite bias results in the transfer back of the electrons to this donor trap level. This can be linked to observing the related cathodic and anodic peaks. With the Fermi level in the degenerately doped SiNWA lying below the valence band, the donor trap level is unfilled at equilibrium. Thus, no transfer from the donor trap level to the electrolyte acceptor level can occur under positive bias, and no transfer into the donor level can occur under opposite bias conditions whilst the electrolyte acceptor states and donor trap levels still overlap. Thus, the trap level remains empty and no electron transfer occurs.

The explanation of residual Ag from the MACE process causing DLTs with which electron transfer with adsorbed water occurring during CV cycling allows us to explain the presence of redox peaks observed with our SiNWA electrodes. It also enables us to identify ways to mitigate and eliminate the effects of them. Surface layer removal via multiple oxidations and oxide strips have proven partially effective, likely due to removing the Ag residue containing surface layers resulting in the DLTs. Degenerate doping via multiple doping steps has shown to eliminate the effect of these trap states by pinning the Fermi level below them. This also provides us with an explanation to why these peaks were not observed with n-Si SiNWA electrodes (Chapter 5), as the Fermi level would be positioned far above the Ag associated trap levels.

6.2.3. Implications of Redox Peaks on Capacitive Performance

The presence and elimination of the redox peaks associated with DLTs in the SiNWAs has ramifications for the performance and stability of them as capacitor electrodes. We have consistently seen that samples exhibiting peaks have yielded high comparative current and capacitance values. This can be seen in Table 6.8, with the extracted capacitance value of an undoped SiNWA electrode with peaks being over 3x higher than that of a degenerately doped sample. This can be attributed to a capacitive effect contributed by the electron transfer dynamics of the trap levels with cycling.

Table 6.8 – EW and extracted areal capacitance measurement for NAOS treated SiNWA electrodes with degenerate (multiple SOD) and non-degenerate (no post-etch SOD) doping.

<table>
<thead>
<tr>
<th>Sample</th>
<th>EW (V)</th>
<th>Capacitance (µF·cm⁻²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>No SOD</td>
<td>2.8</td>
<td>799</td>
</tr>
<tr>
<td>3x B SOD</td>
<td>3.1</td>
<td>254</td>
</tr>
</tbody>
</table>

However, a higher initial capacitance does come at the cost of reduced cycling stability. Repeated cycling over 3000 cycles demonstrated a capacitance loss of nearly 3x higher for the sample with redox peaks than the one without, at 17.3 % and 6.5% respectively. Additionally, the sample without peaks
reaches a stable plateau earlier, with near constant capacitance retention from the 1500\textsuperscript{th} cycle. In contrast, the sample with peaks exhibits a sharper initial decline in capacitance retention and an approximately stable value over the last 800 cycles only. This degradation could potentially be attributed to the redox active sites causing and additional channel for current leakage. It also fits well with the conventional faradaic vs non-faradaic supercapacitor character, with the presence of redox activity demonstrating greater capacitance at the cost of reduced cycle lifetime.

Figure 6.12 – Capacitance retention over 3000 cycles for NAOS treated SiNWA electrodes with (red) and without (black) peaks. Retention percentage at the 3000\textsuperscript{th} cycle is shown.

We have managed to identify, provide an explanation for, and find ways to address the redox peaks appearing in our SiNWA electrode samples. This enables us more control in deciding the form and function of our electrode for performance. Allowing the presence of DLTs to contribute to the storage and discharge of charge, though unconventional, may allow us to achieve higher specific capacitances for certain applications, at the cost of reduced stability and capacity retention. In order to achieve a more conventional capacitive character with our high surface area capacitive electrodes, we can employ techniques such degenerate doping, which gives us a still high performing electrode with better stability and capacitance retention.
7. CONCLUSION

7.1. Summary of Key Outcomes

The key aim of this project was the development of a feasible alternative Si-based electrode for high capacitance electrical energy storage, utilising the high surface area of MACE etched SiNWAs. This dissertation chronicles the work done in achieving this, beginning with initial explorations into the development of a SiNWA electrode, step-by-step realisations of improvements required and made, and finally achieving the goal of a Si-based SiNWA capacitor electrode with performance in the realm of electrochemical capacitors, with high energy and power densities.

Development of the electrode began with using the low-cost MACE process to vastly increase the electrolyte-accessible surface area of Si by etching a high density of free-standing crystalline nanowires of high aspect ratio from a low resistivity Si substrate. An electrolyte to be used in a capacitance system with this was chosen in the form of an IL electrolyte, [Bmim][NTf₂]. This was deemed to be suitable for a number of reasons, most notably being the high chemical stability enabling the potential of achieving a high EW, allowing increased energy and power densities as well as a high operating electrode voltage. The high thermal stability and low volatility of ILs also contribute to their utility and ‘green’ credentials. Furthermore, the choice of this particular IL was underlined by it having a low viscosity for good conductivity, and hydrophobicity to prevent the Si being exposed to a reactive aqueous environment.

Initial evaluations of the SiNWA electrode in comparison to bulk did indeed yield higher current and capacitance values due to the increased surface area. However, even with the IL electrolyte, the EW remained limited to <1 V. Also, the improvement in areal capacitance of ~5x was far below expectations for values conceived to be achievable with the specific surface area boost. An improvement in the conductivity of the surface, boosting the concentration of charge carriers, was carried out by a post-etch SOD step. This greatly increased the attained current and capacitance values, with >40x bulk areal capacitance being realised.

The low EW emphasised the need for further improvements in electrode stability, in order to realise the potential capacity of reaching high EWs with the IL electrolyte. Passivating the exposed Si surface could allow this to be achieved, though the addition of the thickness of a surface layer could impair the capacitance by increasing the effective capacitive distance. A few passivations were investigated, before ending on the idea of utilising a process known as the nitric acid oxidation of silicon (NAOS) to grow an ultra-thin (~1.4 nm) layer of highly dense, stable oxide on the SiNWA surface. The high oxide density and stability of the layer enable good passivation to be reached – as evidenced by the boost
of the EW to values approaching that of the IL electrolyte – whilst the thinness allows the retention of the high capacitance, with no reduction in current and capacitance values caused by the oxide layer. Areal capacitance attained are two orders of magnitude (128x) higher for the SOD and NAOS treated SiNWA electrode as compared to bulk, and estimations of energy and power density place it well within the realm of ECs as per the Ragone plot (Fig. 7.1).

Figure 7.1 – Ragone plot showing a range of portable electrical energy storage mechanisms, contrasting energy density against power density [28]. Placement of a B SOD and NAOS treated sample [3] (yellow triangle) as well as 3x Ti-dip coated sample [2] (red star) on the plot is shown.

An alternative coating was explored in the form of a transition metal oxide (TiO₂) to further boost performance. Various coating methods were investigated, with a Ti-dip coating method conducted multiple times proving to provide a stable, high EW electrode with good capacitive character. This
attained a specific capacitance of \(~0.9 \text{ F·g}^{-1}\), as well as further improved energy and power densities of \(0.9 \text{ Wh·kg}^{-1}\) and \(2228 \text{ W·kg}^{-1}\) respectively. This places even better in the Ragone plot (Fig. 7.1), towards the frontier line of EC devices, and in line with commercially available supercapacitors [213].

Even with the successful realisation of electrodes with EC performance, attempts to improve upon this demonstrated the need for further analyses required due to the observance of the appearance of peaks in the CV plots of some of the SiNWA samples. This was contrary to the expected quasi-rectangular shape from conventional and double layer capacitors, though any chemical activity to cause this intermittent appearance was not apparent either. Additional investigations of various parameters were carried out to try and mitigate these; this also allowed us to rule out various potential causes. These peaks were eventually identified as being the result of deep level traps developed from the MACE process leaving behind residual Ag within the SiNWA surface. The presence of these DLTs, though yielding high values of areal capacitance, cause potential performance issues such as deviation from ideal capacitor charge/discharge character and reduced capacitance retention with cycling. A means to mitigate the effect of the DLTs (i.e. the peaks) was identified in the form of conducting multiple SOD steps. This resulted in the SiNWA surface being degenerately doped, pinning the Fermi level below the valence band, negating charge transfer to and from the trap states. The mitigation of peaks significantly improves capacitance retention with cycling, with a stable plateau of only 6.5% loss observed after 3000 cycles.

7.2. Future Work

This project has dealt with the initial stages of developing a MACE etched SiNWA based high capacitance electrode, leaving potential for further developments to be made upon this. This can be in the further improvement of electrode performance in general, or perhaps tuning the electrode for application purposes.

The key improvement brought by the SiNWA electrode is a high specific surface area (SSA) through nanostructuration. Whilst the surface area to volume ratio yielded is high, there is the possibility of scope for further improvement upon this. The MACE etch formula for the project was tuned to accommodate the relatively high doping concentration of the Si substrate in achieving robust NWs. Tuning the formula – for example by increasing oxidant concentrations – can lead to increased NW porosity. NW shell porosity may provide an additional boost to the SSA, though this would need to be optimised so as not severely degrade the mechanical robustness and electrical conductivity of the NWs.
In this project, the electrode has been investigated in the form of a half cell consisting of a single electrode, rather than the two electrodes of a device. Use of the electrode in device settings could be investigated, such as in a two electrode configuration with another SiNWA electrode, or even in hybrid configuration with other electrode materials. Developing the fabrication of device configurations such an interdigitated device structure from a Si substrate could also be considered.

Although we have identified the cause of peaks and a means to mitigate them, further investigations involving the negation as well as presence of them could be explored. Whilst degenerate doping is one way of negating the effect of the DLTs caused by the residual Ag, an alternative that was partially explored but could be consolidated is that of removing the root cause, i.e. the surface layer containing the Ag nanoparticles. Removing of the top surface layers of the SiNWA would also result in NW thinning, which could yield the added benefit of a higher SSA.

Another aspect of the peaks and trap levels is that, even though it produces non-ideal capacitance character and has a reduced cycling stability, it does provide a significant boost in energy charged and discharged. The potential exists of harnessing the charge transfer to and from the trap states as a means of charge storage, increasing the energy density where the application desires and allows for it.
REFERENCES


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