Silicon Nanowires for Single Electron Transistor Fabrication

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Declaration of Originality

I herewith certify that the research reported in this thesis is of the author’s own, conducted in the Optical and Semiconductor Device (OSD) Group, Department of Electrical and Electronic Engineering, Imperial College London from May 2011 to May 2015. Any other work mentioned in thesis has been properly referenced or acknowledged.

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To my wife, CHEN Si, my son, WANG Zonghan, and to my dear parents, WANG Hesheng and TIAN Jianying
Abstract

As the minimum feature sizes of current integrated circuits approach 10 nm, improvements in the speed, complexity and packing density are becoming increasingly difficult. In particular, at these scale, the operation of ‘classical’ complementary metal-oxide-semiconductor (CMOS) devices is expected to degrade unacceptably. Single-electron devices, where the Coulomb blockade effect can be used to control charge at the one electron level, provide a means to fabricate large scale integration (LSI) circuits with ultra-low power consumption, immunity from charge fluctuations, and high scalability at sub-10 nm dimensions. Single-electron devices are potentially a successor technology to conventional classical Si metal-oxide-semiconductor field effect transistors (MOSFETs), and will play an increasingly important role both in future CMOS and ‘beyond CMOS’ technologies.

In this thesis, we first introduce the history of single-electron (SE) effects and the previous work in both theory and practical fabrication. Subsequently, the theoretical operation of the single-electron transistor (SET) is discussed, followed by a brief introduction to the quantum dot (QD) and the multiple tunnel junction (MTJ) transistor. The fabrication process for SET devices in heavily doped, n-type silicon-on-insulator (SOI) material, using the electron-beam lithography (EBL), is then introduced. Two types of Si SET devices have been studied, the 1 μm nanowire (NW) SET and ‘point gate’ SET, which are both defined by EBL followed by reactive-ion etching (RIE) to create trench isolation of the devices, source, drain and nanowire regions. A thermal oxidation approach, was then used to reduce the Si core to the sub-10 nm scale in the NW. This passivates surface defects, creates charging ‘islands’ isolated by tunnel barriers and forms the SET. Variation in surface roughness, doping concentration and any disorder inherent at the nanoscale can form the tunnel barriers confining the charging island. The SiNW SETs fabricated in this work have been electrically characterised at temperatures from 8 - 300 K. Results obtained from
NWs with core widths from $\sim5$ nm to $\sim40$ nm with two different gate lengths of 1 $\mu$m to $\sim50$ nm have been compared. Here, detailed $I_{ds}$ vs. $V_{ds}$, $V_{gs}$ measurements have been performed at 8 K, and ‘Coulomb diamond’ characteristics have been observed. The 1 $\mu$m long NWs behave as MTJs, with $\sim40$ nm scale islands. Here, the width of the Coulomb diamond cannot be reduced to zero. The detailed temperature dependence of the $I_{ds}$ vs. $V_{ds}$ characteristics show that some SE effects persist even at 300 K. The reduction in NW gate length to 50 nm reduces the likelihood of quantum dots to only three dots, but increases their influence on the electrical characteristics. In the point contact device, QD behaviour with a combination of SE charging and quantum confinement effects is observed at 8 K. In a highly scaled point circuit Coulomb blockade and a single-electron oscillation are observed. Monte Carlo simulations have been used to further investigate the devices and their island configurations. The results of this thesis demonstrate explicitly the significance of quantum effects for the electrical performance of nominally ‘classical’ SiNW devices and highlight their potential for quantum effect ‘beyond CMOS’ devices.
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<th>Definition</th>
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<tr>
<td>MOSFET</td>
<td>metal oxide semiconductor field-effect transistor</td>
</tr>
<tr>
<td>LSI</td>
<td>large scale integration</td>
</tr>
<tr>
<td>SE</td>
<td>single-electron</td>
</tr>
<tr>
<td>SET</td>
<td>single-electron transistor</td>
</tr>
<tr>
<td>QD</td>
<td>quantum dot</td>
</tr>
<tr>
<td>MTJ</td>
<td>multiple tunnel junction</td>
</tr>
<tr>
<td>SOI</td>
<td>silicon-on-insulator</td>
</tr>
<tr>
<td>EBL</td>
<td>electron-beam lithography</td>
</tr>
<tr>
<td>RIE</td>
<td>reactive-ion etching</td>
</tr>
<tr>
<td>$I_{ds}$</td>
<td>source/drain current</td>
</tr>
<tr>
<td>$V_{ds}$</td>
<td>source/drain voltage</td>
</tr>
<tr>
<td>$V_{gs}$</td>
<td>gate voltage</td>
</tr>
<tr>
<td>CMOS</td>
<td>complementary metal-oxide-semiconductor</td>
</tr>
<tr>
<td>TFET</td>
<td>tunnel field effect transistor</td>
</tr>
<tr>
<td>$e$</td>
<td>elementary charge</td>
</tr>
<tr>
<td>$C_i$</td>
<td>island capacitance</td>
</tr>
<tr>
<td>$E_C$</td>
<td>charging energy</td>
</tr>
</tbody>
</table>
$k_B T$ \hspace{1cm} \text{thermal fluctuation}

$R_T$ \hspace{1cm} \text{tunnel resistance}

$R_K$ \hspace{1cm} \text{quantum resistance}
1. Introduction

Over the last 40 years, the improvements in the speed, complexity and packing density of integrated circuits, have been dramatically developed and delivered by reducing device dimensions and developing new device structures. These have required improvements in materials, lithography and fabrication processes. At present, manufacturers have adopted 14 nm node devices and minimum feature sizes < 10 nm being planned [1]. However, this has led to increasingly challenging barriers being encountered in both device physics and technology, e.g. from the fabrication prefecture, the transition well under way from the planar metal oxide semiconductor field-effect transistor (MOSFET) to non-planar FinFET [2] devices for the 14 nm and 10 nm devices nodes is occurring [3, 4].

While both silicon and non-silicon alternatives are being considered, such as III-V and III-V-silicon devices [5], hetero-junction tunnel field effect transistors TFETs [6, 7], graphene [8] and MoS$_2$ devices [9], there are likely to be significant manufacturing problems with the addition of non-silicon technologies. However, in addition to the major technological challenges posed by any successor ‘beyond CMOS’ technology at these scales (< 10 nm), quantum effects are increasingly likely to influence the behaviour of all these devices adversely, even those which are not specifically quantum-dot (QD) devices. For example, the operation of a Fin-FET, with a fin only ~4 nm wide, has been shown to be fundamentally limited by quantum confinement [4]. Fortunately silicon itself offers distinct attractions for quantum devices [10]. In addition to these technologies, at dimension < 10 nm single-electron (SE) devices [11–13] look increasingly attractive. Unlike ‘classical’ FETs, these devices inherently show performance improvements with reduction in size, but may require new approaches both for operation within circuits, and for lithographic and fabrication technologies at the sub-5 nm scale [14]. As highly scaled Si nanowires (SiNW) can be used as the basis for SE/QD transistors operating at room temperature [15–17], it is possible to
envision a direct transition from SiNW FETs to SE/QD devices. Si NWs may then inherently provide the basis for a quantum effect ‘beyond CMOS’ technology [14]. This thesis discusses the increasing influence of single-electron and quantum dot behaviour on the electron transferred in SiNWs, and their applications towards single-electron transistors. The uses Si NWs to study the transition to increasingly dominant quantum behaviour.

1.1. Literature

This section provides a brief introduction to single-electron effects. This comprises a short discuss of the literature background, the development of single-electron transistors (SETs) crystallines and nanocrystallines Si materials, and recent developments of SETs operating at room temperature. More detailed references to previous work will be provided at relevant points in later chapter in the thesis. Detailed reviews of single-electron effects can be found in references [11–13,18–20]

1.1.1. History of single-electron effects

Consider a nanoscale conducting region which can be made from any conducting material, coupled by insulating gaps to electrodes. The conducting region is typically referred to as the ‘island’ (Figure 1.1).

Figure 1.1.: Schematic diagram of single-electron charging of an island coupled by insulating gaps to electrodes.

When a source/drain voltage difference $V_{ds}$ is applied between the electrode regions,
electrons start to tunnel through the junction one at a time such that the charge of the island varies by $e$. If the capacitance of the island $C_i$ is small enough, the variation of the island potential due to the presence of an electron can be large enough such that the single electron charging energy $E_C$ of the island becomes larger than thermal fluctuation $k_B T$. With the presence of an extra electron on the island, the resulting increase in energy can prevent the charging of the island by a second electron, and block current flow across the island. This is the well-known ‘Coulomb blockade’ effect, where the single electron charging energy of the island is given by:

$$E_C = \frac{e^2}{2C_i}.$$

where $C_i$ has to be small enough such that $E_C$ is significantly greater than $k_B T$. For room temperature operation ($T = 300$ K), $E_C \gg k_B T = 26$ meV, corresponding to device dimensions in the nanoscale regime. The constraint of $E_C \gg k_B T$ has been recognised since the first identification of single-electron effects in the 1950s [21]. In the early work, single-electron effects were observed in the conduction and charging process in granular metal films, where the grain sizes were in the nanometer scale [21–26]. In these measurements, the capacitance of each grain was small such that $E_C$ was significantly large and Coulomb blockade could be observed. If this condition is not met, the thermal fluctuation in energy will suppress single-electron effects.

The second condition for observation of single-electron effects is a constraint on tunnel resistance $R_T$. Electrons are required to be localised on the island such that the tunnelling onto the island of an extra electron can be affected. Otherwise, electrons can tunnel through a delocalised states across the device without varying the number of electrons on the island [27–29]. Hence, $R_T$ is given as follows [11,12,18]:

$$R_T \gg \frac{h}{e^2} = 25.9 \, k\Omega.$$

The single-electron transistor (SET), fabricated by Fulton and Dolan [30] in 1987, allows a gate electrode to control single electron effects. Unlike those granular metal film system in the early stage, the SET was lithographically fabricated using Al/Al$_2$O$_3$ material, with an island capacitance $C_i$ of $\sim 1$ fF, leading to a $E_C$ of $\sim 100$ µeV. As this
$E_C \ll k_B T$ at 300 K (26 meV), the Coulomb blockade could only be observed at low temperature, $T = 1.1$ K. Figure 1.2 shows $I-V$ characterise Fulton and Dolan’s SETs with a strong central Coulomb blockade region. With the rapid development in advanced nano-lithography and semiconductor industry since Fulton and Dolan’s SETs, the dimensions of single-electron device have been greatly reduced and various types of SET devices with smaller dimensions have been fabricated, which will be discussed in detail in the next section.

![I-V characteristic at 1.1 K](image)

Figure 1.2.: $I-V$ characteristic at 1.1 K [30] where the center flat area is the Coulomb blockade region.

### 1.1.2. Si MOSFET SET

Since the first semiconductor SET was fabricated in Al/Al$_2$O$_3$ material by Fulton and Dolan in 1987, the first Si SET was demonstrated in a MOSFET type device [31] in 1989. Here, a periodic oscillation was observed at low temperature in the conductance of a one-dimensional channel in the Si SET. In this device, a $\sim 25$ nm $\times$ 1 $\mu$m channel was defined by using a stacked dual gate arrangement, with 27 nm trench used to isolate the gate to the channel. Figure 1.3 shows a plan view of the device in (a) and a cross-sectional view through the dashed line $A-B$ in (b).
The observed periodic oscillation was explained by van Houten et al [32] using a model where interface charges and/or an impurity potential along the channel, could form two or more tunnel barriers confining a charging island. In this system, with a total capacitance $C_T = 2C + C_g$, where $C_g$ is the gate capacitance coupled to island, the single-electron charging energy is given as $E_C = e^2/2C_i$ and the current $I$ across the island oscillations with gate voltage with a period of $e/C_g$. This is the so called ‘Coulomb oscillation’ effect. Figure 1.4 shows schematically how Coulomb oscillations of period $e/C_g$ occur as a function of gate bias. The energy band diagrams are shown in (a) and the correspondingly energy band diagrams are shown in (b) and (c). If a positive voltage $V_{gs} = V_{gs1}$, the positions of the edge of the charging levels $E$ in (b), will be lowered relative to the Fermi energy $E_F$. As $V_{gs}$ is increased to $V_{gs2}$. $E_1$ is pulled level with Fermi energy $E_F$ shown in (c). An electron then tunnels onto the island from the source, charging the island by one electron with the state $n = 1$. Further increases in $V_{gs}$ lead to increasing values of $n$ and all the states lying below Fermi energy $E_F$ are filled. The period of the oscillation is given as $\Delta V_g = e/C_g$. 
1.1.3. Si SETs in SOI material

The first silicon single-electron devices with lithographically defined islands were fabricated by using electron-beam lithography (EBL) in silicon on insulator (SOI) material, by Ali and Ahmed in 1994 [33,34]. This is a popular technique for SET fabrication and there are large number of demonstrations of silicon SETs with lithographically defined islands in SOI material. The SOI can be either the separation by implantation of oxygen (SIMOX) type [33] or the bonded oxide type [35]. Typically thin top Si layer $\sim 100$ nm or less has been used. This top layer could be n-type doped [33,36] or p-type doped to obtain single electron/hole operation [37]. In [33], the top Si layer was doped by phosphorous implantation to $10^{14}/\text{cm}^3$ but subsequent used heavily doped Si. Trench isolation techniques can be used to define the fine features i.e. (island, gate regions and source/drain regions) in the top Si layer. Usually, thermal oxidation of the Si is then used to further reduce the island dimensions and to passivate the surface. Any defects along the NW doping disorders as variation in the oxidation process can also be used to form tunnel barriers.

The scanning electron micrograph tilted at $40^\circ$ and schematic diagram of the device in [33] is shown in Figure 1.5. Here, a patterned island (usually cylindrical or other
similar shapes) was explicitly defined by EBL (with diameter of ∼100 nm), and connected to source/drain electrode regions via a narrow region in either side. As the entire region was defined by EBL followed by reactive ion etching (RIE) for trench isolation, the surface potential in these Si ‘neck’ regions is greater than in the island, which can be used to form the tunnel barrier and subsequently confine electrons on the island [33,36–44]. A side gate layout was used but not shown in the micrograph as this was 500 nm away from the island.

Figure 1.5.: Scanning electron micrograph (tilted at 40°) of the SET in [33]. SEM image of the island on the top and the corresponding schematic diagram at the bottom, with tunnel barriers labelled [33].

Alternatively, a gate can be fabricated on top of the island [37–39,43,44], or the substrate can be used as a back gate [36], can be used to provide a stronger bias. For a back-gate set up, as the BOX layer inherently exists in the SOI material, the substrate is much more straightforward to use as a gate. However, the thickness of BOX layer is 40 nm to 100 nm in most demonstrations, which is usually twice to 10 times thicker than devices using top gates. This means that more voltage is required to use the back gate. In addition, it is more likely that the BOX layer has more defects, especially in SIMOX material, due to the nature of SOI manufacture process. Hence, this implies that a back-gate can often be less effective than the top gate.

We now consider the single-island SET design of Ali and Ahmed [33]. A SIMOX SOI material with a top Si layer thickness of 50 nm, was thinned to ∼40 nm. Then, patterns for side-gate were first defined by EBL, directly written in 400 nm thick polymethylmethacrylate (PMMA) resist. The patterns in resist were then transferred in to Si by RIE in a 1:1 ratio of SiCl₄ and CF₄, at flow rate of 20 sccm at 300 W. Subsequently, two narrow regions were defined by using EBL followed by RIE, where the Si were thinned to form the tunnel barriers.
$I_{ds}$ vs. $V_{ds}$ characteristics of the device (Figure 1.5) at 0.3 K is shown in Figure 1.6 (a). Curves are offset by 0.5 nA for clarity. Figure 1.6 (b) shows the temperature dependence of (a), where clear Coulomb blockade can be observed. This effect was not smeared out until 4.8 K. With a Coulomb gap of $\Delta V = 1.6$ mV, shown in the inset of (b), the total capacitance of $C_T = 50$ aF ($\Delta V = e/2C_T$) was obtained. The rather low temperature for observation the single-electron effects with a narrow Coulomb gap width of 1.6 mV was due to the 100 nm diameter island such that the charging energy of the island $E_C = e^2/2C_T$ is not significant enough. Hence, a reduction in islands dimensions is necessary to reduce the total capacitance $C_T$.

![Figure 1.6.](image)

1.1.4. Si SETs in SOI material with patterned/unpatterned island

Regarding the shapes of lithographically defined islands, there are mainly two types of island, patterned or unpatterned. The patterned island refers to ‘cylindrical’ island connected by ‘neck’ regions, acting as tunnel barriers, e.g. the works done by [33,36–44].

Alternatively, in order to further reduce the island dimensions, unpatterned islands, where the island is not explicitly shaped by lithography, can be used. Here, the island is defined ‘implicitly’, e.g. in a nanowire (NW) any surface roughness, fluctuations in doping concentration and the disorder inherent at the nanoscale, can form tunnel barriers.

Figure 1.7 shows a schematic diagram (a) and SEM image (b) of a SiNW SET where line edge roughness in the fabrication process created islands and tunnel barriers [43].
Within the NW, multiple islands were formed by using EBL followed by RIE. The NW width was further reduced from 30 nm to 16 nm by thermal oxidation at 950°C, such that the smallest island was estimated as 12 nm in diameter with $C_T = 0.7 \text{ aF}$. The charging energy $E_C = \frac{e^2}{2C_T} \approx 130 \text{ meV}$ which is even greater than $k_B T \approx 26 \text{ meV}$ at room temperature.

$$E_C = \frac{e^2}{2C_T} \approx 130 \text{ meV}$$

(a) Schematic diagram of a unpatterned island (NW) SET and (b) SEM image of the $\sim 20 \text{ nm}$ NW [43].

### 1.1.5. Room temperature SETs

Following demonstrations of Si SETs with patterned/unpatterned islands in SOI material, a reduction in device size led to a dramatic improvement in these SETs operating temperature. The first single-electron devices operating at room temperature, were fabricated and characterised in 1995 by Takahashi [45] using pattern dependent oxidation of a NW, and Yano [46] using a nanocrystalline Si material. Both devices were fabricated with island dimensions of sub-10 nm, with a corresponding total capacitance of $< 1 \text{ aF}$, such that the charging energy was greater than thermal fluctuations at 300 K. We will discuss these two types of SET devices in detail in this section.

### 1.1.6. Pattern dependent oxidation

The first room temperature Si SET, fabricated by Takahashi in 1995, was defined by using EBL followed by RIE to create a NW in SIMOX material. A pattern-dependent oxidation (PADOX) approach, using thermal oxidation, was then used to reduce the Si core in the
NWs and passivate defects. The PADOX process provided a means to confine the island and reduce the Si core in the nanowire, relaxing the resolution requirements for lithography for ultra small SET devices. With increasing stress in Si from the growth of SiO$_2$, the oxidation process is self-limited, ensuring an ultra small island $\sim$10 nm or less in size. The PADOX, with its self-limited effect, has now been used to obtain room temperature operating in a number SETs [11, 45, 47–49].

The mechanism of PADOX has been investigated in detail by Horiguchi et al [50], by exploring the effect of stress on the band gap of the silicon along the NW and analysing the variation of the quantum confinement in the NW. It was shown that quantum confinement increased the energy of the bottom edge of the conduction band in the NW, whereas the stress in the centre of the NW decreased the energy. Hence, a potential well in the NW was formed and isolated by the tunnel barriers. The tunnel barriers height could be more than 0.1 meV [50].

Figure 1.8 (a) shows a schematic diagram of the PADOX SET device and (b) shows schematic diagram of the PADOX island with its corresponding potential [45, 48]. The devices consisted of a unpatterned 10 nm wide NW, fabricated in SIMOX material with a thinned top Si layer thickness of 30 nm. High resolution techniques i.e a combination of EBL, electron-cyclotron resonance (ERC) plasma oxidation and ECR plasma etching, were used to defined the devices. The PADOX was then followed to further reduce the island size to $\sim$10 nm within the NW. The tunnel barriers were also formed in the PADOX process to isolate the island from the source/drain electrode regions. The oxidation was in dry O$_2$ ambient at 1000$^\circ$C. The NW was then shielded by the top gate and remained intrinsic Si. The final device could be characterised by using a back and/or a top gate.
Room temperature operation, including Coulomb gap and Coulomb oscillation observed, can be achieved is a consequence of an island size \(\sim 10\) nm, with a further reduction in size by PADOX. In the device of [45], a \(\sim 70\) meV single-electron charging energy was obtained.

A more recent result of a Si quantum dot (QD) operating at room temperature [51] is shown in Figure 1.9 and Figure 1.10, where single electron transport through multiple quantum levels was demonstrated. The energy spacing within the QD was greater than three times of the thermal fluctuation, and high charge stability was obtained due to a ‘gate-all-around’ (GAA) structure [51].
Figure 1.9.: (a) Schematic diagram of the Si QD SET. (b) SEM image of the SiNW after wet-etching. (c) Cross-sectional transmission electron microscopy (TEM) image of the SiNW after fabricating the GAA structure. (d) Schematic diagram of potential profile in the conduction band along the SiNW [51].
A 3-D schematic diagram of the Si QD SET is shown in Figure 1.9 (a). The Si QD and the tunnel barriers, modified and fabricated from a Si nanowire-channel MOSFET, were self-formed by a volumetric undulation process [52–56]. A (110) oriented SiNW was defined by using EBL and helicon dry-etching, patterned on a semi-insulating (100) SOI material, where the substrate is $p$-type doped with doping concentration $\sim 10^{15}/\text{cm}^{-3}$. It was then followed by a subsequently isotropic wet-etching ($\text{NH}_4\text{OH}/\text{H}_2\text{O}_2/\text{H}_2\text{O}$) to further reduce the size of the SiNW to less than 10 nm (Figure 1.9 (b)). The nanowire-channel was then suspended by using HF etching to intentionally remove the BOX layer underneath nanowire-channel. The suspended nanowire-channel beam were supported by the large source/drain regions. Subsequently, a thermal oxidation was used to partially form the gate oxide (i.e. the suspended nanowire-channel). The Si core is further reduced to $< 5$ nm in size (Figure 1.9 (c)). The formation of the tunnel barriers were caused by large subband modulations of (110) oriented SiNW [52, 57, 58] within the Si core regions ($\sim 5$ nm), which are adjacent to the central ellipsoidal area. (Figure 1.9 (d)). A chemical vapour deposition process was used to fabricate the gate stacks of polycrystalline Si/SiO$_2$ in a GAA structure. Finally, a phosphorous ion implantation was carried out to create $n$-type source/drain electrode regions ($10^{20}/\text{cm}^{-3}$). A charging energy ($E_C > 140$ meV) and quantum level spacings ($\Delta E > 75$ meV) at room temperature were obtained in Lee et al’s device [51] due to the ultra small Si QD.

A room-temperature $I_D$ vs. $V_G$ characteristics of the device is shown in Figure 1.10 (a) where the Coulomb oscillation peaks can be clearly seen (CB$_1$, CB$_2$, CB$_3$ and CB$_4$). An aperiodic behaviour is observed in between Coulomb oscillations peaks, indicating that the electron transport is mediated through the discrete quantum states of a Si QD. This is because the Coulomb gap in a Si QD SET is a consequence of not only a single-electron charging energy but an unequally spaced quantum level of the QD [20, 51]. An in-depth analysis on the QD behaviour in Si will be discussed in Chapter 2. The temperature-dependent $I_D-V_G$ characteristics are shown in Figure 1.10 (b), where four Coulomb oscillation are observed in each current curve, as the temperature varies from 150 K to 300 K with a 50 K step. This is also a good agreement with the single dot structure because in a multidot system, a current peak will separate when the temperature is reduced as stochastic tunnelling would be unlikely to occur [58].
Figure 1.10.: (a) $I_D$ vs. $V_G$ characteristics of the QD SET at 300 K. The blue and red lines correspond to the logarithmic and linear scales, respectively. (b) Temperature-dependent $I_D$ vs. $V_G$ characteristics of the QD SET when $T$ varies from 150 to 300 K. (c) Contour plot of $I_D$ vs. $V_D, V_G$ characteristics at 300 K. (d) Contour plot of conductance $g_D = dI_D/dV_D$ vs. $V_D, V_G$ characteristics at 300 K [51].

The contour plot of $I_D$ vs. $V_D, V_G$ characteristics at 300 K, is shown in Figure 1.10 (c), where four clear Coulomb diamonds are observed, and the green area corresponds to CB$_1$, CB$_2$, CB$_3$ and CB$_4$ in Figure 1.10 (a), indicating a large charge stability area. The room temperature operation in Lee et al.’s device [51] is because of this charge stability area due to the ultra small QD in size. The capacitance ratio can then be extracted from the slopes $\alpha$ and $\beta$ of each Coulomb diamond (Figure 1.10 (c)) by using the equations $-\alpha = C_G/C_D$ and $\beta = C_G/(C_G + C_S)$ [53–56], where $C_D$ and $C_S$ are the source and drain capacitances, respectively. The contour plot of conductance $g_D = dI_D/dV_D$ vs. $V_D, V_G$ characteristics at 300 K, is shown in Figure 1.10 (d), where all of the Coulomb-blockade regions are tilted diagonally towards to higher $\pm V_D$. The electron transport through discrete quantum states can be seen from the multiple Coulomb blockade regions (A and -A). The evidence of Coulomb staircase occurrence is where $V_G = V_{g1}$ to $V_{g6}$ indicated by black dash line.
1.1.7. Nanocrystalline silicon nanowire SETs

The first room temperature SET in nanocrystalline silicon was fabricated by Yano [46]. Instead of using PADOX to reduce the islands, these devices used an ultra small island \( \sim 10 \) nm in diameter, defined ‘naturally’ by silicon nanocrystals in an ultra-thin \(< 5 \) nm width nanocrystalline silicon film [46].

The nature of the nanocrystalline silicon (nc-Si) material is such that as the crystalline silicon grains (\( \sim 10 \) nm in diameter) exist in the material, separated by oxide or amorphous regions [46, 59–69]. Those grains and the separation regions can be directly used as islands and tunnel barriers respectively to fabricated single-electron devices. Growth techniques can be used to precisely control the dimensions of islands and tunnel barriers, rather than PADOX or high-resolution lithographic techniques. Compared to those fabrication processes where a combination of high-resolution lithographic techniques, trench isolation and oxidation is used, nc-Si SET devices can be defined in both large grained polycrystallines [70] or in nc-Si films, \( \sim 50 \) nm or less in thickness [66,67]. For both types of materials, if the silicon nanocrystals can be less than 10 nm, the tunnel barriers can be \( \sim 100 \) meV or higher such that the single-electron charging energy and tunnel resistance is large enough for room temperature operation of SET devices [46,71]. Quantum confinement may also occur when the island dimension is sub-10 nm [72]. This means that it may be easier to realise room temperature SET in nc-Si.

A schematic diagram of Si SET, fabricated in an amorphous nc-Si material is shown Figure 1.11 [71], where a ‘point contact’ configuration is used to reduce the island dimensions. An SEM image of the island area is shown as a inset in Figure 1.11, where the island is 20 nm wide and 20 nm long, and the gap is 120 nm [71]. The fabrication process initiated with a 20 nm thick nc-silicon film prepared by a high frequency (100 MHz) low temperature plasma-enhanced chemical vapour deposition from a gas mixture of SiF\(_4\):H\(_2\):SiH\(_4\). The film was deposited at 300\(^\circ\)C on a 150 nm thick SiO\(_2\) layer, which was thermally grown on an \( n \)-type crystalline Si substrate in advance. Subsequently, the film was \( n \)-type doped to \( 10^{20} \)/cm\(^3\), leading to a typical grain size of 4 - 8 nm. The point contact SET devices, with in-plane gate electrodes on either side, were then defined by using EBL and RIE in SiCl\(_4\)/CF\(_4\) plasma. It was then followed by a low temperature oxidation (750\(^\circ\)C,
1 h)/high temperature annealing process (1000°C, 15 min) to oxidise the grain boundaries and simultaneously passivate the surface roughness.

Figure 1.11.: Schematic diagram with a SEM image of the point-contact device shown in the inset, where the point-contact island is 20 nm wide and 20 nm long, and the gap is 120 nm [71].

Figure 1.12 (a) shows temperature-dependent $I_{ds}$ vs. $V_{ds}$ characteristics of the device shown in Figure 1.11, where $V_{ds}$ is biased at 20 mV and $V_{gs}$ is swept from 0 to 9 V. The temperature dependence of $I_{ds}$ vs. $V_{gs}$ characteristics, is shown in Figure 1.12 (b), where the oscillations in $I_{ds}$ persists up to 300 K.
The capacitances in the device and the corresponding single-electron charge energy $E_C$ can then be extracted from the electrical results in Figure 1.11 and Figure 1.12. The Coulomb gap can be obtained as $V_C = e/C_\Sigma \approx 100 \text{ meV}$, leading to a total capacitance $C_\Sigma = 3.2 \text{ aF}$. The period of Coulomb oscillations in $I_{ds}$ can be exacted from Figure 1.12 (b) as $\Delta V_g = 3 \text{ V}$, leading to a gate capacitance $C_g = e/\Delta V_g = 0.05 \text{ aF}$. As the total capacitance $C_\Sigma = 2C_t + C_g$, the tunnel capacitance $C_t = 1.6 \text{ aF}$.

The conductivity of the point contact nc-Si SET device, outside the Coulomb gap is shown in Figure 1.13, where Arrhenius plots of the device conductivity as a function, are used to investigate the properties of the tunnel barriers. Here, the gradient of the plot corresponds to the highest potential barrier along the electron transport path, where the barrier height $E_a$ is 173 meV, extracted from this gradient. Here, $E_a$ is the energy gap between the conduction band and covalent band i.e. the change in the electrostatic charging energy for one electron added to the QD, which is also referred to as the ‘addition energy’ [20]. This significant barrier height in the SETs may be associated with the formation of oxide layers at the grain boundaries in the oxidation/annealing process.
1.1.8. Room temperature SET in FinFET structure

More recently an ultra small single-electron transistor has been fabricated by scaling the size of a FinFET structure down to the few nanometer regime, leading to a reliable formation of a sub-5 nm Coulomb island [73].

A schematic 3-D layout of the SET device is shown in Figure 1.14 (a) and (b) a cross-sectional view along the channel along the line $a$-$b$. The cross-sectional TEM images of the etched Si wires, along the line $c$-$d$ are shown in (c) and (d) for device A and B. Finally, a cross-sectional TEM image along the line $a$-$b$ in after the deposition of polycrystalline silicon (poly-Si) fin-gate is shown in (e) where the NW channel lies in the poly-Si forms the fin-gate and the tetraethyl-orthosilicate (TEOS) spacer profiles are used.
The devices were fabricated in SOI material with a 50 nm thick undoped top Si layer. The NW, 20 nm in width connected to the source/drain electrode regions, was defined by EBL followed by RIE in SF$_6$/CF$_4$/O$_2$ ambient. After deposition of a 100 nm TEOS layer, trenches 80 nm wide were etched across the NW using EBL with ZEP520A resist followed by RIE in CHF$_3$/O$_2$ ambient. The exposed Si area underneath was etched to a 30 nm depth by using RIE in SF$_6$/CF$_4$/O$_2$ ambient. The PADOX process was then used at 900°C for 50 min (SET A) and 40 min (SET B). The size of the islands was further reduced to $\sim$2 nm for SET A and $\sim$4 nm for SET B, respectively. A TEOS layer (20 nm in thickness) was then deposited into the trench to form spacers on the sidewalls of the source/drain electrodes. Doped poly-silicon was then deposited into the trench to form a
self-aligned fin-gate close to the Coulomb island.

Figure 1.15 shows the charge stability diagrams at room temperature for SET devices A and B, respectively. Three rhombic areas (Coulomb diamonds) can be seen in both devices. In the charge stability diagram, each of these areas corresponds to a stable charge configuration on the island, occupied with the number of $N$ electrons. The corresponding gate capacitance was then obtained as $C_g = 0.094$ aF, tunnel capacitance $C = 0.16$ aF and therefore the total capacitance $C_T = 0.42$ aF. The single-electron charging energy $E_C = 0.493$ eV due to the extremely small island size.

A more recent result of the impact on transistor performance of a single dopant atom at room temperature has been studied by investigating the influence of a single arsenic dopant atom on the off-state room-temperature behaviour of a short-channel Fin-FET [74].
Figure 1.16.: (a) Schematic diagram of the short-channel FET with a gate length of 30 nm, which is highlighted in red. (b) The plot of differential source/drain conductance versus gate and drain voltage at 4.2 K.
Figure 1.16 (a) shows the schematic diagram of the Fin-FET device with a gate length of 30 nm. The FET device was fabricated in 200 mm SOI wafers, followed by a stage of ion implementation to define the source/drain regions. A 200 nm × 20 nm × 50 nm (length/thickness/width) silicon nanowire was fabricated and covered by a 30 nm long polysilicon gate isolated by a 4 nm thick SiO$_2$ layer (shown in Figure 1.16 (a)). Figure 1.16 (b) shows the differential source/drain conductance versus gate and drain voltage at 4.2 K, where the top horizontal scale is the energy in the channel measured from the threshold voltage. The first peak occurs at the ionisation energy at -108 meV and the gate voltage $V_g = -1.3$ V (see Figure 1.16 (b)), corresponding to the first dopant with a high ionisation energy due to dielectric confinement near the buried oxide layer interface; the second (at $V_g = -1$ V) and third resonances (at $V_g = -0.7$ V) correspond to different electronic occupations of another donor. The negative differential conductance lines are resulted from local density of states fluctuations in the source/drain area. The positive differential conductance lines, however, are attributed to an excited state of the second peak. Figure 1.16 (c) is a magnified version of the peak in Figure 1.16 (b) at 100 mK. The lines of differential conductance parallel to edges of the diamond are observed due to the fluctuations of the local density-of-states (LDOS) in the source and drain [74]. Figure 1.16 (d) shows the second peak at $V_g = -1$ V and the third peak at $V_g = -0.7$ V in a magnified view, respectively. Because of the the single-electron effect and quantum confinement effect, the corresponding charging energy of the second peak is larger than the ionisation energy of another dopant i.e. arsenic atom, present in the channel. The second peak therefore corresponds to a second dopant located closer to the gate oxide. The third peak is related to the inelastic co-tunnelling, which will not be discussed in this thesis.

1.2. Summary

This chapter has provided a brief introduction to the history of single-electron effects. This comprises a short discussion of the background literature, the development of single-electron transistors from metallic material to Si SOI material (SIMOX or Bonded) with patterned/unpatterned island, the development of single-electron transistors in crystallines Si and nanocrystallines Si materials, and recent developments of SETs operating at room
temperature, including in FinFETs and QD SETs. A pattern-dependent oxidation (PA-DOX) approach for the further reduction of island dimensions has been discussed. Detailed references to previous work have been provided at relevant points.
2. Theory of single-electron effects

In this chapter, we will introduce the theory of single-electron effects in a SET in the double tunnel junction (DTJ) configuration. Here, we discuss the circuit diagram for the double tunnel junction SET, charge vs. electrostatic energy changes $\Delta E$, tunnelling rates as a function of $\Delta E$, the probability of the island in the electron number state $n$, $I$-$V$ curves calculation, Coulomb diamonds and the Coulomb staircase. This discussion follows the semiconductors model for a SET provided in [12, 13, 18, 75] Finally, a brief discussion of quantum dot (QD) behaviour and multiple tunnel junction (MTJ) system is provided.

2.1. Circuit diagram

The DTJ circuit schematic diagram is shown in Figure 2.1 (a), biased by a voltage supply $V_D$. The circuit consists of an island, where $ne$ corresponds to the charge due to $n$ electrons on the island, isolated by two tunnel junctions from source/drain voltage. The circuit diagram of an SET with double junctions is shown in (b). Note that the SET circuit can be obtained by introducing an additional gate voltage $V_G$ coupled to the island via a gate capacitance $C_G$. To simplify the analysis, voltage supply $V_D$ in (a) is often converted to two source/drain voltages $-V_D/2$ and $V_D/2$ respectively. Looking from the island in Figure 2.1 (c), capacitances $C_1$, $C_2$, $C_g$ are all in parallel to each other.
### Figure 2.1: Schematic diagram

- (a) DTJ
- (b) SET with double junctions
- (c) Capacitances $C_1$, $C_2$, $C_g$ of (b) are parallel to each other, looking from the island

#### 2.2. Electrostatic energy changes

As two junctions are presented in the SET, the electrons can ‘hop on/off’ the junction 1 and junction 2. This leads to two equations required to define the limits of the Coulomb blockade for $n$ extra electrons on the island [12]. The backward and forward tunnelling rates for each junction can then be determined by electrostatic energy changes. Using the net tunnelling rate, the device $I-V$ characteristics can be predicted. The current increases in a step-like manner, e.g. the current curves shown in [30,33,70], are caused by the mismatch of tunnelling rates across the two junctions, creating a Coulomb staircase characteristics. This is considered in the single-electron Monte Carlo simulations provided in Chapter 5, where very different resistance values are used to obtain Coulomb staircase.

We now consider the electrostatic energy changes when an electron tunnels through the junctions and the island. As capacitances $C_1$, $C_2$, $C_g$ in Figure 2.1 (b) are parallel, looking from the island, the island charge $-ne$, can be obtained as [13]:

$$-ne = Q_1 + Q_2 + Q_g$$  \hspace{1cm} (2.1)

Applying Kirchhoff’s voltage law, two equations can be obtained:

$$\frac{V_D}{2} + V_1 + V_{gi} - V_g = 0$$  \hspace{1cm} (2.2)

$$V_g - V_{gi} + V_2 - \frac{V_D}{2} = 0$$  \hspace{1cm} (2.3)
Rewrite the equations 2.2 and 2.3 in terms of charge \( Q \), gives:

\[
- \frac{V_D}{2} + \frac{Q_1}{C_1} + \frac{Q_g}{C_g} - V_g = 0
\]

(2.4)

\[
- \frac{V_D}{2} + \frac{Q_2}{C_2} - \frac{Q_g}{C_g} + V_g = 0
\]

(2.5)

Solving the equations 2.2 to 2.5 simultaneously, gives \( Q_1 \), \( Q_2 \) and \( Q_g \) in terms of \( ne \), \( V_g \) and \( V_D \):

\[
Q_1 = \frac{C_1}{C_\Sigma} ((C_2 + \frac{C_g}{2})V_D + C_g V_g + ne)
\]

\[
Q_2 = \frac{C_2}{C_\Sigma} ((C_1 + \frac{C_g}{2})V_D - C_g V_g - ne)
\]

\[
Q_g = \frac{C_g}{C_\Sigma} ((C_1 - C_2) \frac{V_D}{2} + (C_1 + C_2) V_g - ne)
\]

where \( C_\Sigma = C_1 + C_2 + C_g \). When an electron starts to tunnel through the junctions onto the island, the charge change due to a transition from \( n \) to \( n + 1 \) electrons as a consequence of tunnelling across the first junction, can be found [13]:

\[
\Delta Q_1 = Q_{1,n+1} - Q_{1,n} = \frac{C_1}{C_\Sigma} ((C_2 + \frac{C_g}{2})V_D + C_g V_g + (n+1)e) - \frac{C_1}{C_\Sigma} ((C_2 + \frac{C_g}{2})V_D + C_g V_g + ne)
\]

(2.6)

\[
\Delta Q_2 = -\frac{C_2}{C_\Sigma} e
\]

(2.7)

\[
\Delta Q_g = -\frac{C_g}{C_\Sigma} e
\]

(2.8)

We now consider the electrostatic energy change of Junction 1 when an electron tunnels on the island from \( n \) to \( n+1 \), which is the sum of the change in the electrostatic energy of
the island plus the work done by each voltage source and component in the system shown in Figure 2.1 (b) [12, 13, 18]. In a manner analogous to the charge changes, the energy change due to a transition from \( n \) to \( n + 1 \) electrons as a consequence of tunnelling through the first junction onto the island, can be found by using equations 2.6 to 2.8 [12,18]:

\[
\Delta E_1 = E_{1,n+1} - E_{1,n} + \text{work}
\]

\[
= \frac{(-n+1)e^2}{2C_\Sigma} - \frac{(-ne)^2}{2C_\Sigma} + \frac{V_D}{2} (\Delta Q_1 - e) + \frac{V_D}{2} \Delta Q_2 + V_g \Delta Q_g
\]

\[
= \frac{e}{C_\Sigma}(ne + \frac{e}{2} - V_D(C_2 + \frac{C_g}{2}) - C_g V_g)
\]

In a similar manner, the energy change due to a transition from \( n \) to \( n - 1 \) electrons as a consequence of tunnelling off the first junction, can also be obtained. Hence, the two equations of electrostatic energy changes are given as [12,18]:

\[
\Delta E_1 = \frac{e}{C_\Sigma}(ne + \frac{e}{2} - V_D(C_2 + \frac{C_g}{2}) - C_g V_g)
\]  

(2.9)

\[
\Delta E_2 = \frac{e}{C_\Sigma}(-ne + \frac{e}{2} + V_D(C_2 + \frac{C_g}{2}) + C_g V_g)
\]  

(2.10)

Here, by multiplying \( C/C \) to the right hand side of equation 2.9, gives:

\[
\Delta E_1 = \frac{e}{C}(\frac{C}{C_\Sigma} ne - \frac{C}{C_\Sigma} V_D(C_2 + \frac{C_g}{2}) - \frac{C}{C_\Sigma} C_g V_g + \frac{C}{C_\Sigma} e)
\]  

(2.11)

where \( C = C_1 + C_2 \), equation 2.9 can be rewritten in terms of average charge (\( Q_{ave} \)) and critical charge (\( Q_c \)) [18]:

\[
\Delta E_1 = \frac{e}{C}(Q_{ave} - Q_c)
\]  

(2.12)

where

\[
Q_{ave} = \frac{C}{C_\Sigma} ne - \frac{C}{C_\Sigma} V_D(C_2 + \frac{C_g}{2}) - \frac{C}{C_\Sigma} C_g V_g
\]

\[
Q_c = \frac{C}{C_\Sigma} \frac{e}{2}
\]

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Here, $Q_{\text{ave}}$ depends on the voltage supply $V_D$ and $Q_c$ is the so called critical charge of
the junction, which is less than $e/2$ and independent of $n$ [19,76]. Since a low impedance
environment is assumed here, the tunnelling rate $\Gamma$ is obtained as a function of $\Delta E_1$ [18,75],
given as follows:

$$\Gamma = \frac{1}{e^2 R_1} \frac{\Delta E_1}{1 - e^{\frac{\Delta E_1}{k_B T}}}$$

(2.13)

when temperature $T = 0$, the tunnelling rate can be given by:

$$\Gamma = \begin{cases} \frac{\Delta E_1}{e^2 R_1} & \text{if } \Delta E_1 > 0 \\ 0 & \text{if } \Delta E_1 < 0 \end{cases}$$

(2.14)

Equation 2.14 means that once the average charge $Q_{\text{ave}}$, determined by the voltage
supply, becomes greater than critical charge $Q_c$, an electron tunnels through one junction
onto the island. From equation 2.13, we can see that the tunnelling rate depends on
equation 2.9 which is determined by the change of equilibrium electrostatic energy of the
entire system, caused by the transition i.e. tunnelling event. Note that this is the case
when the tunnelling resistance $R_T \gg 26$ kΩ and the electromagnetic environment is of low
impedance $[18,19,75,77]$. For electrons tunnelling through the Junction 1 on to the island
from $n$ to $n+1$, equation 2.9 has to be positive, given by [18,77]:

$$\Delta E_1 = \frac{e}{C_2} \left( e(n + \frac{1}{2}) - V_D(C_2 + \frac{C_g}{2}) - C_g V_g \right) > 0$$

leading to

$$V_D(C_2 + \frac{C_g}{2}) + C_g V_g < e(n + \frac{1}{2})$$

(2.15)

In a similar manner, for electrons tunnelling off the island through the Junction 1, gives:

$$V_D(C_2 + \frac{C_g}{2}) + C_g V_g > e(n - \frac{1}{2})$$

(2.16)

Combining equations 2.15 and 2.16, the two edges of the Coulomb blockade region can
be defined by the following inequality [18]:
\( e(n - \frac{1}{2}) < V_D(C_2 + \frac{C_g}{2}) + C_g V_g < e(n + \frac{1}{2}) \)  

(2.17)

In a manner analogous to the transition of Junction 1, another inequality can be obtained to define the other two edges of the Coulomb blockade region, given by:

\( e(n - \frac{1}{2}) < -V_D(C_2 + \frac{C_g}{2}) + C_g V_g < e(n + \frac{1}{2}) \)  

(2.18)

Taking inequalities 2.17 and 2.18 together into account, the whole Coulomb blockade region is limited by tunnelling across any one of the two junctions. Within the area (rhombic regions (Figure 2.2 (a)) defined by the inequalities 2.17 and 2.18, the electron(s) on the island with number \( n \) is stable.

Figure 2.2.: (a) Charge stability diagram of Coulomb blockade regions defined by the edges using inequalities 2.17 and 2.18 (b) Slopes of the edges when \( n = 0 \).

The edges of the Coulomb blockade regions using inequalities 2.17 and 2.18 are shown in Figure 2.2 (a), where the area is a function of \( \frac{C_\Sigma V_D}{e} \) and \( \frac{C_g V_g}{e} \), for \( n = -1, 0 \) and 1. Here, each specific values of \( \frac{C_\Sigma V_D}{e} \) and \( \frac{C_g V_g}{e} \) with the rhombic areas corresponds to a stable state where the island is occupied by \( n \) electrons. Due to its rhombic shape, the charge stability regions are also called ‘Coulomb Diamonds’. The charge stability area when \( n = 0 \), is shown in Figure 2.2 (b), where the slopes of the Coulomb blockade regions, defined by the inequalities 2.17 and 2.18 are given [13,18].

From 2.14, if a SET device with gate capacitance \( C_g \) negligibly small compared with \( C_1 \) and \( C_2 \), all the terms with \( C_g \) are cancelled and the tunnelling rates remain as follows [13]:
\( \Gamma_1^+ \neq 0 \), gives 
\[ +ne + \frac{e}{2} - C_2 V_D - C_g V_g \approx +ne + \frac{e}{2} - C_2 V_D < 0 \] (2.19)

\( \Gamma_1^- \neq 0 \), gives 
\[ -ne + \frac{e}{2} + C_2 V_D + C_g V_g \approx -ne + \frac{e}{2} + C_2 V_D < 0 \] (2.20)

\( \Gamma_2^+ \neq 0 \), gives 
\[ -ne + \frac{e}{2} - C_2 V_D + C_g V_g \approx -ne + \frac{e}{2} - C_2 V_D < 0 \] (2.21)

\( \Gamma_2^- \neq 0 \), gives 
\[ +ne + \frac{e}{2} + C_2 V_D - C_g V_g \approx +ne + \frac{e}{2} + C_2 V_D < 0 \] (2.22)

where ‘+’ means the electron tunnels through the junction from left to right (forward) and ‘−’ means from left to right (backward). Then the shape of charge stability region, in a similar manner to the one in Figure 2.2 (b), is shown in Figure 2.3 (assuming \( C_1 < C_2 \)).

In comparison with Figure 2.2 (b), the top and bottom corners in Figure 2.3 are lying on the \( y \)-axis because \( C_g \) is negligible. The right and left corners are lying off the \( x \)-axis, leading to a ‘tilted’ shape because of the difference between \( C_1 \) and \( C_2 \).

![Figure 2.3: Charge stability region when \( n = 0 \)](image)

### 2.3. \( I-V \) characteristic calculation

In order to further investigate the single-electron effect, it is essential to understand the \( I-V \) characteristics. In the last section, we have seen that the tunnelling rates are a function of electrostatic single-electron energy determined by \( V_D, V_g \) and \( n \). Here, we will
discuss another parameter, \( p_n \), which is the probability of \( n \) electrons on the island. With a specific value of \( n \) and a constant bias of \( V_D \) and \( V_g \), neglecting correlated tunnelling processes, a master equation of the rate of changing probability \( p_n \) is given by [13]:

\[
\frac{dp_n}{dt} = \Gamma_{n,n+1}p_{n+1} + \Gamma_{n,n-1}p_{n-1} - \Gamma_{n+1,n}p_n - \Gamma_{n-1,n}p_n
\]

where the first two terms represents the rate of changing probability for the transition from \( n \) to the adjacent states \( n-1 \) and \( n+1 \). However, the last two terms give the rate of changing probability from \( n-1 \) and \( n+1 \) to \( n \). Taking 2.19 - 2.22 into account, the tunnelling rates for the transitions changing forward/backward can be obtained as follows [13]:

\[
\Gamma_{n+1,n} = \Gamma_{1,+}(n) + \Gamma_{2,-}(n) \quad (2.23)
\]

\[
\Gamma_{n-1,n} = \Gamma_{1,-}(n) + \Gamma_{2,+}(n) \quad (2.24)
\]

The solution of the master equation is given by [13]:

\[
\Gamma_{n,n+1}p_{n+1} = \Gamma_{n+1,n}p_n \quad (2.25)
\]

For state \( n \) and \(-n \) the probability are as follow:

\[
p_n = \prod_{m=0}^{m=n-1} \frac{\Gamma_{m+1,m}}{\Gamma_{m,m+1}} \quad (2.26)
\]

\[
p_{-n} = \prod_{m=n-1}^{m=0} \frac{\Gamma_{m-1,m}}{\Gamma_{m,m-1}} \quad (2.27)
\]

where

\[
\sum_{n=-\infty}^{n=+\infty} p_n = 1 \quad (2.28)
\]

Here \( \Gamma_{m,k} \) is the rate of transition from state \( m \) to \( k \). Equation 2.26 and 2.27 represent the possibilities for opposite directional transition. Equation 2.28 is from the normalisation of \( p_n \). By solving equations 2.26 - 2.28, \( p_0 \) and each \( p_n \) can be found out.
Since the current flowing through the whole system, is the product of the net tunnelling (the difference between forward and backward tunnelling rates), \( p_n \) and \( e \), adding the results for each value of \( n \), the current is given by:

\[
I = e \sum_{n=-\infty}^{n=+\infty} p_n (\Gamma_{1,+}(n) - \Gamma_{1,-}(n)) \\
= e \sum_{n=-\infty}^{n=+\infty} p_n (\Gamma_{2,+}(n) - \Gamma_{2,-}(n))
\]

Hence, the Coulomb staircase \((I_{ds} - V_{ds})\) and the Coulomb oscillation \((I_{ds} - V_{gs})\) can be calculated, respectively, by using different values of \( V_{ds} \) and \( V_{gs} \) to calculate the tunnelling rates and hence the probability \( p(n) \).

Using \( n=0 \) for equation 2.23 and \( n=1 \) for 2.24, gives

\[
\Gamma_{1,0} = \Gamma_{1,+}(0) + \Gamma_{2,-}(0) = \Gamma_{1,+}(0)
\]

\[
\Gamma_{0,1} = \Gamma_{1,-}(1) + \Gamma_{2,+}(1) = \Gamma_{2,+}(1)
\]

As \( p_0 + p_1 = 1 \), applying equation 2.26, this can be rewritten as follows:

\[
p_1 = \frac{\Gamma_{1,0}}{\Gamma_{2,0}} \frac{p_0 \Gamma_{1,0}}{p_0 \Gamma_{2,0}} = \frac{p_0 \Gamma_{1,0}}{\Gamma_{2,0}}
\]

leading to

\[
p_0 + p_1 = p_0 + p_0 \frac{\Gamma_{1,0}}{\Gamma_{2,0}} = 1
\]

Hence,

\[
p_0 = \frac{\Gamma_{2,0}}{\Gamma_{2,0} + \Gamma_{1,0}}
\]
\[ p_1 = \frac{\Gamma_{1,+}(0)}{\Gamma_{1,+}(0) + \Gamma_{2,+}(1)} \]

where as \( \Gamma_{1,+}(0) \) and \( \Gamma_{2,+}(1) \) are a function of \( V_D \). The current can be rewritten as follows:

\[ I = e\Gamma(V_D) \]

where \( \Gamma(V_D) \) is the net rate defined by:

\[ \frac{1}{\Gamma(V_D)} = \frac{1}{\Gamma_{1,+}(0, V_D)} + \frac{1}{\Gamma_{2,+}(1, V_D)} \]

Here, the net tunnelling rate \( \Gamma(V_D) \) depends on the smaller one of \( \Gamma_{1,+}(0, V_D) \) and \( \Gamma_{2,+}(1, V_D) \). As a consequence, if \( R_1 \) and \( R_2 \) are very different from each other, \( \Gamma_1 \) and \( \Gamma_2 \) are correspondingly different from each other according to equation 2.13. The current flowing through the junctions appears in a stepwise manner, referred to as the Coulomb staircase (Figure 2.4). Assuming \( R_1 < R_2 \), the slopes are given as:

\[ \frac{e}{2R_1(C_1 + C_2)} \text{ for ‘slope 1’ in each step} \]

\[ \frac{e}{2R_2(C_1 + C_2)} \text{ for ‘slope 2’ in each step} \]

Figure 2.4 shows a Coulomb staircase \( I - V \) characteristics using \( C_1 = C_2 = 2 \) aF, \( C_g = 0 \), \( R_1 = 200 \) kΩ, \( R_2 = 200R_1 \). The characteristics are obtained using simulation program ‘CAMSET’ [78] developed by Cambridge Hitachi laboratory. This allows both Monte Carlo simulations of single-electron system, and applications of the analytical model developed in this chapter. The slopes of stepwise manner in the \( I_{ds} \) vs. \( V_{ds} \) characteristic, caused by different tunnel resistances are labelled as ‘slope 1’ and ‘slope 2’, respectively.
Finally, the average current \( I_{av} \) (for \( R_1 < R_2 \)) is defined as

\[
I_{av}(V_D) = e\Gamma_{2,+} = \frac{1}{2R_2(C_1 + C_2)}(n_{max}e - \frac{e}{2} + (C_1 + C_2)V_D)
\]

which is dominated by the junction with lower tunnelling rate, and where \( n_{max} \) is the maximum possible integer for the number of electrons presenting on the island.

### 2.4. Quantum Dot

The influence of single-electron effects in metallic island were discussed in the Section 1.1. However, once the island dimensions are comparably small to the de Broglie wavelength of the electrons presented on the island, the discrete energy levels on the island can be filled with electrons. It is possible that the electrons can tunnel on and off the island when the energy spacing \( \Delta E_S \gg k_B T \) [13]. The island is then referred to as the ‘quantum dot’ (QD) [79–81]. In this section, we will only consider the Coulomb oscillations in a QD [72,82–84].

For simplicity we assume that energy levels in the QD are equally spaced and that the dimensions of the QD are small enough such that the single-electron charging energy \( E_C > \Delta E_S \gg k_B T \). The energy level is assumed to be independent of the number of electrons \( n \) and the total capacitance of the QD \( C_T = C_1 + C_2 + C_g \) [85].

A schematic diagram for a QD is shown in Figure 2.5, where we assume that the contacts are metallic. The Fermi energy of the source measured relative to the bottom of the conduction band is \( E_{FS} \). \( E_{FD} \) is the Fermi energy of the drain. We also assume a drain
voltage $V_D$ applied across the QD, which is just enough to enable the tunnelling rate from left to right. This leads to $E_{FS}$ being slightly greater than $E_{FD}$. Levels below the source Fermi energy $E_{FS}$ in the QD are filled by electrons. $E_a$ is the energy gap between the level, $E_{QD(n+1)}$ and $E_{QD(n)}$ i.e. the change in the electrostatic charging energy for one electron added to the QD, $E_{QD(n+1)} - E_{QD(n)}$, which is sometimes called ‘addition energy’ [20].

The electrostatic energy of the QD at a given gate voltage $V_g$ for $n$ electrons, is given by [20]:

$$E_{QD(n)} = E_n + \frac{e}{C_\Sigma}(ne - \frac{1}{2} - C_g V_g)$$

$E_n$ is the energy of $n^{th}$ confinement level and the last two terms are the electrostatic

Figure 2.5.: Energy band diagrams for a QD applied by a constant low $V_D$ when (a) $V_g = 0$. (b) $V_g > 0$ before the tunnelling of an electron, and (c) $V_g > 0$ after the tunnelling of an electron [20].
energy of the QD at a given gate voltage $V_g$ for $n$ electrons. The addition energy for state $n$ $E_a(n)$ can be rewritten as follows:

$$E_a(n) = E_{QD}(n+1) - E_{QD}(n) = \Delta E_S + \frac{e^2}{C_\Sigma}$$

In a manner analogous to the single electron effects, the gap at the Fermi energy in the QD caused by the addition energy $E_a$ corresponds to a Coulomb blockade effect in the QD. As shown in Figure 2.5, this Coulomb gap can be overcome by applying a gate voltage $V_g$. As $V_g$ increases, the energy level $E_{QD}(n+1)$ is pulled relative to the source Fermi energy $E_{FS}$. When $E_{QD}(n+1)$ is aligned with $E_{FS}$ (Figure 2.5 (b)), an electron tunnels onto the QD. For $V_g > 0$ in Figure 2.5 (c), the electrostatic energy of the QD is charged by one electron, filling the level $E_{QD}(n+1)$, all the levels above $E_{QD}(n+1)$ shift to higher energies by $e^2/C_\Sigma$. This behaviour repeats as $V_g$ increases. This is known as the Coulomb oscillation, and has the periodicity given by [20]:

$$\Delta V_g = \frac{C_\Sigma}{eC_g}(\Delta E_s + \frac{e^2}{C_\Sigma})$$

This $\Delta V_g$ implies an aperiodic Coulomb oscillation observed in the QD compared to the SET Coulomb oscillation period $\Delta V_{g,SET} = e/C_g$, and only when $\Delta E_s \ll e^2/C_\Sigma$, the aperiodic behaviour becomes less significant.

2.5. Multiple tunnel junction

We now turn our attention to a general single-electron Monte Carlo simulation for multiple tunnel junction (MTJ) consisting of a one-dimensional chain of nanoscale island and tunnel junctions, shown in Figure 2.6 (a) with a number of $N$ tunnel junctions and $N-1$ islands. The islands are coupled to each other by tunnel junctions with capacitance $C$, connected to the source/drain electrode regions. The islands are also coupled to a gate voltage by gate capacitances $C_g$. The Coulomb blockade, in such a system, can be influenced by any variation in the single electron charging energy of each island, and the polarisation changes of neighbouring tunnel junctions caused by the effect of an extra electron [77, 86–88]. The total capacitance of MTJ is also decreased as tunnel capacitance of each island are
connected in series. This leads to an increase in the charging energy of each island and hence an increase in the operating temperature.

![Circuit Diagram](image)

**Figure 2.6.** (a) A general simulation circuit diagram. (b) Circuit diagram looking from island \( m \). (c) The equivalent model of total capacitance \( C_T = 2C_h + C_g \). (d) The equivalent model of capacitance \( C_h^{-1} = (C_h + C_g)^{-1} + C^{-1} \) [13].

To further investigate the charging energy \( E_{C} \) of the MTJ, a simple approximation of an infinite long, homogeneous MTJ model [77, 89] is used, shown in Figure 2.6 (b). Looking from the middle island \( m \), each half of the MTJ can be seen as equivalent to a infinitely long capacitor array, with capacitance \( C_h \). The total capacitance of the MTJ may then be represented by \( C_T = 2C_h + C_g \) (Figure 2.6 (c)), where \( C_h^{-1} = (C_h + C_g)^{-1} + C^{-1} \).
If looking from the island $m$ again, due to the infinitely long MTJ $C_h$ is given by a combination of capacitors, where $C_h$ and $C_0$ are in parallel and then in series with $C$, shown in Figure 2.6 (d). Then $C_h$ is given by $C_h = \frac{1}{2}(\sqrt{C_0^2 + 4CC_0} - C_0)$, leading to $C_T = \sqrt{C_0^2 + 4CC_0}$. Therefore, the charging energy for a single electron within the MTJ can be obtained as follow:

$$E_C = \frac{e^2}{2C_T}.$$

A single electron Monte Carlo simulation of MTJ has been performed to further investigate the $I - V$ characteristics of our SET devices. These are presented in Chapter 5.

### 2.6. Summary

This chapter has discussed a theoretical model of double tunnel junction (DTJ) SET to explain the single-electron effects, from the circuit diagram for the double tunnel junction SET. This includes charge vs. electrostatic energy changes $\Delta E$, tunnelling rates as a function of $\Delta E$, the probability of the island in the electron number state $n$, $I-V$ curves calculation, Coulomb diamonds and the Coulomb staircase. The corresponding equations and inequalities were also derived to help explain the analytical model. The behaviour of quantum dots (QDs), especially the Coulomb oscillation in the current $I_{ds}$ as a function of gate voltage $V_{gs}$, has been discussed. Finally, the multiple tunnel junction (MTJ) system has been considered, including the total effective capacitance and the more complex electrical characteristics of the MTJ.
3. Fabrication of SiNW SET by using EBL

Since the development of the first single-electron transistors initially in Al/Al$_2$O$_3$ [30] in 1987, and subsequently in Si e.g. MOSFET type SET [31] in 1989 and first Si SET [90] in 1993, sub-micron lithographic techniques have been applied to the reduction of island dimension. This has significantly raised the possibility of observing single-electron effects in semiconductor devices at room temperature. In 1995, an important improvement was made in Si single-electron transistors by Takahashi et al [45, 46] with the fabrication of the first devices operating at room temperature. Silicon, demonstrated in the current semiconductor industry, has been used in a wide variety of SET devices.

SETs demonstrated in Si use high-resolution lithographic techniques, such as electron beam lithography (EBL), to define the nanoscale tunnel barriers and charging islands either ‘explicitly’ (e.g. by using a dot connected through two narrow regions forming tunnel barriers) or ‘implicitly’ (e.g. nanowire (NW) structure using material morphology). ‘Implicitly’ defined charging islands can rely on surface roughness, fluctuations in doping concentration and the disorder, inherent at this scale along the NW, to form tunnel barriers. In the following sections, a SiNW SET fabrication process defined by EBL in bulk-Si/SOI material will be introduced.

3.1. Electron-beam lithography

Lithographic techniques such as optical lithography where a mask is essential can be contrasted with direct writing techniques such as EBL, which do not require a mask. In standard optical lithography, the mask is normally made from chrome on quartz for a resolution typically for $\sim$1 $\mu$m. Over a lengthy period there has been a reduction in the UV
exposing wavelengths from the 435 nm (mercury arc ‘g’ line), through 405 nm ‘h’, 365 nm ‘i’ line to deep UV illumination systems at 248 nm (KrF excimer laser), 193 nm (ArF excimer laser) and 158 nm (F₂ laser) [91]. The shorter wavelengths require CaF₂ optics. And of course now to 13.4 nm EUV which requires reflection optics [92]). However, problems in EUV associated with cost, mask defects [93], and brightness of the light source remain to be overcome. EBL provides sub-micron lithography technique, capable of creating the fine features at the ∼5 nm scale [94]. In an electron beam lithography system, as a finely focused electron beam (sub-10 nm diameter) directly writes patterns on a thin film of electron sensitive material, controlled by a computer, it allows writing of arbitrary patterns in the resist with high resolution, high density and high reliability. This technology was first developed by Möllenstedt and Speidel [95] in 1960 and in the following a couple of years, it was demonstrated that the feature size could reach 150 nm [96] and that the single-beam diameter could be focused under 10 nm [97]. At present, EBL has demonstrated great potential for nanoscale fine structure linewidths/ gaps [96–99]. Nonetheless, EBL is limited by the need for ultra-high-resolution resist, slow sequential exposure rate and a complex pattern transfer processes, allowing the patterns to be transferred from the resist to the underlying substrate material. Very recently, the use of multiple beams has raised the possibility of high-resolution EBL [100]. The EBL process used for the fabrication of the SiNW SETs of this thesis will be discussed in the next section.

3.1.1. Beam formation and system interface

The SET patterns were exposed by electron beam lithography using a LEO 1450VP SEM, modified by the addition of a Xenos/XeDraw pattern generator. The schematic diagram of the SEM can be seen in Figure 3.1. In this system, the resist is exposed by a focused beam of electrons scanned across the writing field. The electron beam is formed from a source by a series of lenses, apertures and electrodes within the column, shown in Figure 3.1 below.

In Figure 3.1, the beam is emitted from the source, passing through two (or three) lenses to focus a demagnified image of the source onto a substrate on which the pattern is written. The beam deflection coils enable the beam to be moved across the writing field. The apertures are used to confine the beam diameter and limit the beam shape. The beam can also be blanked by inserting beam blanking electrodes before the final
The resist is exposed by the focused beam scanning the areas defined by the pattern data. The pattern is pre-designed and coded separately and then via the computer is used to control the movement of the beam accordingly.

The overview of EBL system used in this work is shown in Figure 3.2. The system consists of a XeDraw 2 pattern generator, connected by a ‘XeDraw PC’. A Keithley picoammeter is used to measure beam current from the Faraday cup mounted on the SEM stage. These three units interact with the computer (SEM PC) controlling the SEM to automate the control of the electron beam stage movement, deflection and the beam focusing. The explanation in details of the Xenox system and beam current measurement is given below:

- **XeDraw PC:**

  The XeDraw PC is used to design the program for e-beam patterns, and communicate with SEM PC for control of all SEM functionality, except beam deflection and the SEM image feed which are controlled by XeDraw 2 [103]. Many of the patterns in this thesis have been written without the use of a beam blanker in the system. This means the beam will not be completely blanked when moving over the writing field from one pattern to another.

- **XeDraw 2:**

  The XeDraw 2 is the pattern generator, controlling the electron beam deflection directly via BNC connections connected to a routing box to the SEM system. Xe-
Draw 2 has to be driven by the instructions from the XeDraw PC. The XeDraw 2 pattern generator and the XeDraw PC as a whole is the main body of the Xenox EBL system.

- Keithley Picoammeter:

  The Keithley picoammeter is used to measure and calibrate the electron beam current incident on the surface of the sample. A Faraday cup is used to perform this function, which is built in the sample holder and can be assembled with the SEM stage. When the beam current value is obtained, it is then used in the XeDraw PC for the exposure.

![Figure 3.2.: Overview of Xenos EBL system [103]](image)

### 3.1.2. Electron beam resist

EBL requires the use of a polymer or molecular resist layer [101], chemically sensitive to the electron beam. EBL has been performed in a wide range of resists, e.g. poly-methyl-methacrylate (PMMA) [104–107], hydrogen silsesquioxane (HSQ) [108], calixarene [109], ZEP [110,111] and other e-beam sensitive materials e.g. fullerene derivative [112,113] and TiO₂ [114], in either ‘positive’ or ‘negative’ tone. Here, a ‘positive’ tone resist such as PMMA, implies a material which becomes chemically soluble in a ‘developer’ solution. This is typically due to the breaking of the polymer molecular chains by the electron
beam [101]. In contrast, a negative tone resist such as HSQ, becomes less soluble in developer due to cross-links of polymer molecules [101, 108]. At high doses, it is possible to cross-link even positive tone resist and obtain negative tone behaviour [101, 115]. In this thesis, PMMA is adopted for SiNW SETs fabrication.

3.1.3. Sample preparation

The lithography and pattern transfer process was initially developed on bulk-Si material to investigate the limit of the resolution of the EBL system being used and determine process parameters. These processes were then directly transferred onto SOI material for actual device fabrication. Preceding EBL, samples required cleaning to remove surface contamination. The sample preparation process for this is outlined as follows:

- **Sample Cleaning**: Rinse a 1 cm $\times$ 1 cm chip first with acetone and then isopropanol (IPA, also known as 2-propanol or Isopropyl alcohol). This is followed by an oxygen plasma clean in a planar plasma to remove any organic contamination (flow rate: O$_2$ - 100 sccm, Ar - 10 sccm and power 200 W).

- **Prebake**: Bake at 150$^\circ$C in an oven for 30 min to dehydrate the chip, and allow good adhesion between the e-beam resist and the Si sample surface.

- **Resist spin-coating**: Spinning consists of two stages. The PMMA is initially spun on top of the chip at a speed of 500 rpm for 10 sec in a first stage. The spin speed is then instantly increased up to 5000 rpm for 50 sec in a second stage. The initial slow-rate spin is helpful in obtaining a uniform resist layer. The second stage is to further thin the layer, and the spin speed of 5000 rpm is the maximum speed of the spinner. The PMMA used here was 950k PMMA A6. This means that the PMMA is formulated with a molecular weight of 950k dissolved in an anisole solvent, with a 6% concentration of PMMA. With this concentration, the thickness of the PMMA film can be controlled using the spin speed from $\sim$400 nm to 1.5 $\mu$m.

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For a thinner layer of resist < 400 nm, the PMMA is diluted in anisole from 6% to 2%, leading to a ~100 nm thickness layer of resist. This was measured by using a stylus surface profiler, DekTak. This process was characterised and the relationship between film thickness and spin speed for different concentration can be seen in Figure 3.3. It is seen that decreasing the percentage dilution from 6% to 2% reduces the film thickness at a given spin speed. A 2% concentration of 950k PMMA, the film thickness can be controlled from sub-100 nm to 0.5 µm.

- Postbake: Bake the sample coated with PMMA at 170°C on a hot plate for 1 hour, to dehydrate and harden the PMMA and further improve adhesion. Although a bake of 5 - 15 min is regarded as sufficient, a longer baking time can help to create a stronger resist wall [107,116]. That makes the following lift-off process easier and more precise. Good hardness of the resist also prevents the patterned structure from being damaged in subsequent processes.

3.1.4. Electron-beam exposure

A writing field was defined before starting the beam exposure of the sample. In the XeDraw system, the writing field can be defined from 1 µm to 800 µm in accordance with
the number of pixels from 1000 to 200000. Here, a writing field of 100 µm × 100 µm was used by default, with 50000 × 50000 pixels, meaning that each pixel defined by the software is equally spaced by 2 nm, regardless of the spot size of beam itself, in both x and y directions. The software requires a pattern file and a control file to control the exposure, and these are explained in the following.

- **Pattern file:**

  A pattern file contains the data, is used to design the exposure pattern out of basic shapes. The essential shapes are dots, lines, rectangles and polygons (convex quadrilaterals). A circle is not definable by this program and a triangle can be only obtained by defining two corners of the quadrilateral at the same point.

  In the pattern file, the beam current is defined by measuring the current from the Faraday Cup using the pico-ammeter. This value is used to define beam ‘dwell time’ i.e. the time spent by the beam at each pixel, and separation of pixels in the pattern.

- **Control file**

  A control file is used to write multiple patterns in writing fields mapped to the chip area, and to define the stage movement necessary for this on the sample. For example, 9 patterns defined in a 100 µm by 100 µm writing field can be ‘stitched’ to form a different and bigger pattern in a writing field of 300 µm × 300 µm.

  In the control file, apart from the pattern files to be exposed, the beam dose per pixel for dot, line and area has to be defined respectively. The dose is also strongly related to the exposure time. For a traditional tungsten filament SEM, a compromise between the exposure time and the energy dose must be made as the filament may strongly degrade in long exposures e.g. > ∼2 hours or the beam drift away from its initial conditions.

  To balance the exposure time and energy exposed per pixel, the following parameters must be considered:

  - **Beam current step size**

    Step size defines the steps in movement of the e-beam in units of pixels. The minimum value is 2, meaning the e-beam exposes every other pixels for a given dimension.
of basic shapes. The maximum step size is 128. Figure 3.4 is used to explained step size in details. The beam spot is approximated as a Gaussian distribution seen from the top, with $\sigma$ as the beam diameter, shown in Figure 3.4 (a). The single-pass line starts from a black circle to another towards the right hand side. The grey circles are the unexposed pixels whereas the red ones are exposed in Figure 3.4 (b) and (c). The yellow regions are overlapping regions of two adjacent exposed spots and the red regions are overlapping region of a consecutive three exposed spot, shown in Figure 3.4 (c):

\[ \sigma = 10 \text{ nm} \]
\[ d_0 = 2 \text{ nm} \]
\[ L = 20 \text{ nm} \]
\[ n = 11 \]

(a) A sing-pass line consisted of 11 pixels with length of 20 nm, and the spot size of 10 nm

\[ d_1 = 4 \text{ nm} \]
\[ n_{\text{exp}}/d_s = 2 = 6 \]

(b) Every other pixel exposed in the line

\[ d_{\text{overlap}} = 6 \text{ nm} \]
\[ n_{\text{exp}}/d_s = 2 = 6 \]

(c) Superposition effect

Figure 3.4.: A schematic diagram to explain the step size in exposure

- The default writing field 100 $\mu$m $\times$ 100 $\mu$m with 50000 $\times$ 50000 pixels is used. => The distance between each pixel $d_0 = 100 \text{ $\mu$m} / 50000 = 2 \text{ nm}$.
- For a 20 nm single-pass line ($L = 20 \text{ nm}$) in the default writing field => The
number of pixels that the line requires \( n = \frac{L}{d_0} = \left(\frac{20}{2}\right) + 1 = 11 \).

- With a step size \( d_s \) of 2 \( \Rightarrow \frac{10}{2} = 5 \) out of 10 pixels will be exposed to form the line. \( \Rightarrow \) The separation between two exposed pixels \( d_1 = d_s \times d_0 = 4 \) nm

- Assuming that the best beam diameter can be obtained in the system is \( \sigma = 10 \) nm, as the beam diameter is greater than the step size, overlapping regions of \( d_{\text{overlap}} \) = 6 nm in width are formed between two adjacent exposed pixels. Overlapping regions of a consecutive three exposed pixels \( d_{\text{overlap2}} \) = 2 nm in width are also formed.

A Matlab simulation is used to investigate the effect of beam spot size and step size, shown in Figure 3.5. The contour plots with different step size are shown in Figure 3.5 (a) and (b). Here, the second beam scattering effect is ignored. The effective dose in the overlapping area can be simply regarded as the sum of each contributing exposed pixel. This superposition effect can cause a higher dose density than required, shown in Figure 3.5 (c) and (d), and will cause an overexposed pattern and increased feature size. However, if the pattern shown in Figure 3.4 (a) is written with step size \( d_s = 4 \), the beam exposes every four pixels i.e. three pixels will be exposed out of 11 shown in Figure 3.4 (b). The overlapping regions are therefore reduced to 2 nm in width for adjacent two exposed pixels and no contributions from three exposed pixels. The effective dose of the overlapping regions can be seen in Figure 3.5 (c) for step size = 2 and (d) for step size = 4. The effective dose therefore can be reduced by using a larger step size. Hence, those features with larger step size are more likely to have smaller width in the following processes.
Figure 3.5.: Simulation of the relationship between effective dose and step size.

(a) Step size = 2, dose = 1.5 nC/cm for each exposed excel
(b) Step size = 4, dose = 1.5 nC/cm for each exposed excel
(c) Step size = 2, effective dose = 7.5 nC/cm
(d) Step size = 4, effective dose = 4.5 nC/cm

However, the practical pattern size of the devices is often larger than expected because of scattering effects, shown in Figure 3.6. The beam will scatter before it arrives at the surface of the sample. Due to diffraction effects, the scattered electrons expose greater areas than defined region. This is the so called the ‘forward scattering’ [117]. In addition, reflected electrons from the interface of the substrate material and resist also expose the resist, leading to an overdeveloped result. This is referred to as ‘back scattering’ [117]. Forward scattering can be effectively reduced by limiting the electron dose and increasing the accelerating voltage (will be discuss later in this section). Back scattering, however, in our case helps the lift-off process in the fabrication flow due to its undercut profile in the developed resist, although a thinner layer of resist or a high accelerating voltage helps to alleviate this effect.
Figure 3.6: Schematic diagram of the actual size of beam diameter, where the beam diameter is consisted of the actual beam width and the scattering width.

- **Dwell time**

  ‘Dwell time’ defines the time, in units of nanoseconds, spent by the e-beam on each pixel. After the dwell time has passed, the beam moves to the next pixel with the distance defined by step size. The minimum value of dwell time is 200 ns, which is determined by the clock frequency of the SEM PC. The dwell time can be changed within a given exposure.

- **Accelerating voltage (EHT)**

  A voltage difference is established between the SEM filament (cathode) and the anode so that the working function of the filament material is overcome and the electrons are accelerated and drawn out of the emission gun toward the anode. This is 20 kV by default in the Xedraw system.

  A higher accelerating voltage confines the beam such as it is more concentrated and the scattering distribution within the substrate changes. The maximum value 30 kV of EHT is used to obtain the highest resolution patterns.

- **Spot size**

  The minimum spot size determines the highest resolution features exposed by the electron beam on the resist. The size is proportion to the emission current of the electron beam. Matlab simulation was used to provide an estimation of the spot size by comparison of the simulated exposure line width with actual obtained line width.
A spot size of \(~20\) nm was used for a beam current of 13 pA. The beam current was hence used to obtain the higher resolution features.

- **Working distance**

  The distance between the final lens and the specimen on the stage. Ideally, smaller values lead to high resolution pattern as the beam is in better focus. However, the distance must be a compromise due to the difficulty of focusing, the reduction of brightness and the danger of crashing the stage if moved. A working distance of \(~5\) mm was used to ensure high-resolution pattern with a good reproducibility.

- **Measured beam current**

  The current intensity from the emission gun can be tuned from the software interface. However, the current decreases while travelling through the lenses and apertures in the column. Therefore, the actual beam intensity used for EBL is the current at the specimen, which is measured from the Faraday cup, shown in Figure 3.7.

  Ideally, a smaller current intensity results in a smaller beam diameter. As the beam current is decreased to a range below 10 pA, even a small reduction of the beam diameter can cause a large reduction in brightness as the aberration limits of the column are approached [91]. The focus also becomes increasingly difficult to obtain. This is because only a reduced number of electrons can be collected in the SEM detectors due to the low beam current, and thereby difficulty in focusing the beam ensues. With difficulties of the viewing and recognition issues mentioned above, the beam current in the SEM software is set to be \(~18\) pA to allow a measured beam current of \(~13\) pA at the Faraday Cup.
Exposure time

Exposure time is the sum of the dwell time of the e-beam on each pixel, and the time for movement of the beam from one pixel to the next. This determined how much energy is deposited into the resist. As a small beam current with long exposure time can be equivalent to a large current with short time, a low beam current (i.e. small beam diameter) with long exposure time is often desirable for features at the nanoscale. Since the working distance, EHT and the spot size are fixed in each exposure, the measured beam current can therefore also be fixed for each exposure. Hence, the exposure time is also constant for one pattern. In our case, the exposure time is constrained to < 1 hour to ensure stability of exposure and also increase filament life.

3.1.5. Resist development and EBL results

Resist development immediately follows the e-beam exposure, and is typically performed by immersing the resist for 3 min (in our case) in a liquid developer to dissolve fragments (positive tone resist). The developer is a 20 ml combination of MIBK : IPA = 1 : 3 (MIBK : methyl isobutyl ketone). During development, the solvent penetrates through and selectively removes the exposed regions. Longer fragments molecular are less likely to be dissolved and removed, but more strongly bound to the unexposed resist. Exposure and development are interrelated, as a low exposure with long development can be equivalent to
an overexpose with short development [118]. To clarify the ambiguity between the terms underexposed and overexposed, or underdeveloped and overdeveloped, the relationship between the exposure dose and development time can be seen in the four-quadrant diagram shown in Figure 3.8.

![Figure 3.8: The relationship between exposure dose and development](image)

Here, the origin $O$ is where both exposure dose and developing time are ideal for the best resolution. Quadrant I leads to thick structures. Quadrant III leads to failure of lift-off in the subsequently steps. Underexposed pattern can be compensated by a slightly longer developing in quadrant II, and vice versa for quadrant IV.

Considering that the resist development time is a relative easy parameter to control, the exposure dose can be a varied to establish the best resolution. The dose for the best resolution can be found by exposing a group of lines with varying dose under the same development time of 3 min, shown in the Figure 3.9. Figure 3.9 (a) shows the pattern file of the layout, where the lines are divided into 5 groups with 5 different pitches for the minimum gap: $2 \mu m$, $1 \mu m$, $500 \text{ nm}$, $100 \text{ nm}$, $50 \text{ nm}$, from bottom to top. Each group has 10 single-pass lines to confirm repeatability of the linewidth. An ascending dose from $1 \text{nC/cm}$ to $10 \text{nC/cm}$ is used for the lines from the bottom to the top in each group. Then both the dose for nanoscale lines and the minimum line separation can be found. The optical image taken after the development is shown in the Figure 3.9 (b), where circular exposed regions 1 and 2 are caused by the absence of a beam blanker, and correspond to where the beam is parked by the software. Here, the PMMA was even converted to
negative tone due to the high electron dose. Beam optimisation, and necessity for a beam blanker will be discussed in following sections. Figure 3.9 (c) shows an SEM image of the two narrowest NWs taken after Si etching. The narrowest line for this test, found within 2 µm-spaced group, had a width of ~140 nm at 2 nC/cm at 30 kV EHT. Other lines either failed to develop as adjacent lines merged together, due to the narrow gaps in between, or the lines were so weak that damage in the follow steps, such as the metal lift-off process. Note that taking device fabrication into account, the actual dimensions are determined only when patterns are transferred from the resist to Si. That means that in our case the best exposure dose corresponds to when the transferred Si structure reaches its minimum size. In this case, the minimum transferred line widths was in the range of ~20 nm to 30 nm.

Figure 3.9.: Dose and grating test for single-pass line.
3.2. E-beam patterns fabrication

As PMMA is used in the positive tone as described above, a metal deposition followed by lift-off process is needed to transfer the nanoscale patterns to metal hard mask, typically using Al. A reactive ion etching (RIE) process is then used to transfer the pattern from metal to Si. Trench isolation of the devices, source, drain and nanowire regions can be also created when the device is fabricated in SOI material. The dimensions of the trenches in the etching process are expected to be $\sim 200$ nm in depth and $\sim 100$ nm in width. The process flow is described as follows:

- **Metal deposition:**
  The sample is loaded into the chamber of a thermal evaporator immediately after being developed. A 30 nm thick layer of Al is evaporated on top of the resist-coated sample at a chamber pressure $< 2.2 \times 10^{-6}$ mbar.

- **Lift-off:**
  The Al-coated sample is then immersed in acetone to dissolve the exposed areas and lift off the unwanted metal. Immersion in an ultra-sonic bath, typically for 2 min, can help to lift off metal films, which are difficult to remove only by immersion.

- **Reactive ion etching:**
  Following transfer of the pattern from resist to metal, an anisotropic reactive ion etching is used to transfer the pattern into Si using an Oxford Instrument System 80. It was operated at a power 100 W and pressure 100 mTorr for 1 minute under the flow rate: $\text{SF}_6$ - 30 sccm and $\text{O}_2$ - 10 sccm. This led to an etch depth of $\sim 200$ nm, shown in Figure 3.10 tilted at 30° from the horizontal.
Wet etching:

Following transfer of the pattern to silicon, the metal hard mask is removed by wet etching. The Al etchant used is a mixture of 1 - 5% HNO$_3$ for Al oxidation, 65 - 75% H$_3$PO$_4$ to dissolve the Al$_2$O$_3$, 5 - 10% CH$_3$COOH for wetting and buffering and H$_2$O for dilution.

### 3.3. Beam Optimisation

Figure 3.9 (c) shows initial SiNW fabrication following EBL and RIE before EBL process optimizations. The width of the SiNW $\sim 140$ nm. Following EBL process optimizations, the NW width was reduced to $\sim 30$ nm.

In this regards, first of all careful focusing is essential to define the beam diameter and thereby the NW width. The SEM beam spot size may be minimized by using the following techniques:

- Aperture alignment

A careful alignment of the final lens aperture is needed each time to shape the beam and improve the beam edges. A major change in the spot size are in column parameters, such as the EHT, beam current and the type of apertures. The SEM uses apertures from 100 $\mu$m to 30 $\mu$m, and for the highest resolution, the 30 $\mu$m aperture is required.
- **Stigmation**

As the electron beam should have a circular cross-section when it arrives at the specimen, any distortion resulting in focusing difficulties is not allowed during the travelling in the column. A stigmator is used to eliminate this problem. i.e. A stigmator, located in the objective lens, uses a magnetic field to reduce aberrations of the electron beam and adjust the shape of the beam and correct major lens distortions [119].

A large number of processing factors in EBL shown in Table 3.1 influence the dimensions of the final structure.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Influence</th>
</tr>
</thead>
<tbody>
<tr>
<td>Beam step size</td>
<td>The distance (nm) that the beam moves for one pixel</td>
<td>Exposure dose</td>
</tr>
<tr>
<td>Dwell time</td>
<td>The time (ns) spent on each pixel</td>
<td>Exposure dose</td>
</tr>
<tr>
<td>Beam current</td>
<td>The measured current (pA) is the beam current incident on the specimen</td>
<td>Beam diameter, exposure dose</td>
</tr>
<tr>
<td>Exposure dose</td>
<td>The dose per unit length/area (nC/Cm or µC/cm²), a function of above three parameters</td>
<td>Pattern resolution</td>
</tr>
<tr>
<td>Exposure time</td>
<td>The sum of dwell time for total exposed pixels</td>
<td>Filament life and feasibility</td>
</tr>
<tr>
<td>Exposure energy</td>
<td>The product of exposure time, and dose for a specific area</td>
<td>Pattern resolution</td>
</tr>
<tr>
<td>Pattern density</td>
<td>The integration level for patterns in a specific area</td>
<td>Pattern resolution</td>
</tr>
<tr>
<td>Resist thickness</td>
<td>N/A</td>
<td>Pattern resolution, resist sensitivity</td>
</tr>
<tr>
<td>Development time</td>
<td>N/A</td>
<td>Pattern resolution, resist sensitivity</td>
</tr>
</tbody>
</table>
### Table 3.2.: Optimal parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Optimal value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Aperture size</td>
<td>30 µm</td>
</tr>
<tr>
<td>Step size</td>
<td>24</td>
</tr>
<tr>
<td>Dwell time</td>
<td>3000 ns</td>
</tr>
<tr>
<td>EHT</td>
<td>30 kV</td>
</tr>
<tr>
<td>Working distance</td>
<td>5 mm</td>
</tr>
<tr>
<td>Beam current</td>
<td>13 nm</td>
</tr>
<tr>
<td>Exposure dose (Single-pass line)</td>
<td>1.85 nC/cm</td>
</tr>
<tr>
<td>Exposure dose (Polygon)</td>
<td>240 µC/cm²</td>
</tr>
<tr>
<td>Development time</td>
<td>3 min</td>
</tr>
</tbody>
</table>

### 3.4. SiNW SET fabrication on SOI material

EBL and trench isolation have been used to fabricate SETs devices in SOI material, based on heavily doped $n$-type oxidised Si nanowires (NWs), with dual in-plane side gates. The details of the fabrication steps are given below:

1. Sample

   A (100) oriented 8-inch diameter SOI wafer, supplied with a $p$-type doped ($\sim 10^{15}$ cm$^{-3}$) $\sim 120$ nm top Si layer, and a $\sim 130$ nm buried oxide layer, was cleaved into $\sim 1$ cm$^2$ chips. This is on top of an undoped substrate with thickness of $500 \pm 25$ µm.

2. Sample clean

   To remove both metallic and organic contamination and obtain a clean surface a 3-stage Piranha etch/RCA clean process is used:

   (i) Piranha etch: A mixture of $\text{H}_2\text{SO}_4(98\%) : \text{H}_2\text{O}_2(30\%) = 3:1$ (There may be many different mixture ratio used for piranha solution) is used to remove any ‘visible residues’.

   (ii) RCA1 clean: A typical recipe for RCA solutions is $\text{NH}_4\text{OH}(25\%) : \text{H}_2\text{O}_2(30\%) : \text{deionised water} = 1:1:5$. Soak in the solution at 60 - 80°C for 10 minutes.

   (iii) RCA2 clean: Soak in the solution of $\text{HCl}(37\%): \text{H}_2\text{O}_2(30\%) : \text{deionised water} = 1:1:6$ at 60 - 80°C for 10 minutes.

3. Top layer thinning
The cleaved chips were oxidised at 1100°C for 2 hours in oxygen, with a ramp time of 1 hour and natural cooling to room temperature, to form a ∼200 nm thick SiO$_2$ layer capping the top-Si. As the process consumed ∼100 nm of the top-Si, this resulted in a top Si layer as thin as ∼20 nm. An HF dip of 5 min was then used to remove the unwanted SiO$_2$ at an approximate rate of 25 nm/min, with an allowance made for a small over etch. Figure 3.11 shows a comparison between the original SOI material in (a) and thinned top layer SOI material in (b).

4. Spin-on doping

The nanowire SETs in this thesis were fabricated from a heavily doped $n$-type SOI (100) wafer (resistivity $\rho \sim 10^{-3}$ Ωcm). Unlike previous work on Si NWs doped by implantation, a novel process was used for Si nanowire doping by the application of a spin-on dopant (SOD) layer using phosphorus $n$-type dopant. The wafer SOD layer was applied at 2500 rpm for 50 sec, to form a layer ∼3.5 μm thick layer. This was followed by a bake at 200 °C for 30 min, to make the layer solid. A rapid thermal annealing (RTA) process in nitrogen ambient, lasting 2 min, at ∼950 - 1000 °C,
was used for dopant diffusion with the aim of producing a doping concentration of 
$\geq 10^{19}$/cm$^3$. This was confirmed using 4-point probe measurement of resistivity.

Figure 3.12 (a) shows one $I-V$ characteristic of the doped sample measured by 4-
point probe, where the slope of the curve is $V/I = 50$. As the thickness is only 
20 nm for the top Si layer of our SOI material, a thin layer resistivity function is 
applied as follows:

$$\rho = \frac{\pi}{\ln(2)} \frac{V}{I} = 4.532 \frac{V}{I}$$

subject to the layer thickness $t \leq s/2$, where $s$ is the probe spacing [120]. $\pi/\ln(2) = 4.532$ 
is the correction factor for thin layer resistivity. This gives a resistivity value of 
0.0005 $\Omega \cdot$ cm, corresponding to a doping concentration of $1.6 \times 10^{20}$/cm$^3$. Figure 3.12 
(b) shows the relationship between the doping concentration and doping times ob-
tained by 4-point probe measurement, where the initial undoped concentration was 
$\sim 10^{13}$. After first doping the concentration level increases to $\sim 10^{16}$. By doping 
twice, the concentration further increases to $\sim 10^{18}$. The concentration can eventu-
ally reach the level of $\sim 10^{19}$ or above by conducting SOD process three times. The 
highest concentration obtained is $1.6 \times 10^{20}$/cm$^3$ by doping three times, which is the 
last data point shown in figure 3.12 (b).
5. Fine feature patterning

Sample preparation, including resist (PMMA) spin-coating and baking, is the same as in the Section 3.1.3. The SET patterns were exposed by using EBL with parameters shown in Table 3.2. To study the characteristics of individual devices a circuit was designed to enable four devices to be investigated simultaneously. Here, devices with NW widths down to \( \sim 30 \text{ nm} \) and lengths to \( \sim 100 \text{ nm} \) were defined. A comparison was made specifically of the characteristics of NWs having nominal lengths of 1 \( \mu \text{m} \) and \( \sim 100 \text{ nm} \) respectively. Dual in-plane gates along the NWs were defined, using either a parallel gate structure (1 \( \mu \text{m} \) length wire) or as a ‘point gate’ (100 nm wire). The NW current could be controlled using one or both gates. A schematic diagram of the two device structures is shown in Figure 3.13 (a) (parallel side gate) and (b) (point-gate). Diagrams of EBL layout of two NW devices are shown in Figure 3.13 with parallel gate structures along a 1 \( \mu \text{m} \) NW (c), and ‘point gate’ structures along a \( \sim 100 \text{ nm} \) NW (d). A gradual transition was used where the NW meets the source/drain contact regions to minimise pattern dependent oxidation (PADOX) effects. Multiple devices were fabricated on each sample using the device layout shown in Figure 3.13 (e), which shows a group of four devices having

Figure 3.12.: (a) I-V characteristic of the doped sample measured by 4-point probe, where the slope can be used to obtain the resistivity/doping concentration. (b) Relationship of doping concentration over doping times
common gate and drain terminals.

Figure 3.13.: Device structure of NW SETs fabricated on a SOI chip, shown in schematic form, (a) 1 \( \mu \)m NW and (b) 100 nm point-gate device. (c) and (d) show EBL layout of 1 \( \mu \)m NW and 100 nm ‘point-gate’ device. (e) shows the whole layout of e-beam pattern.

6. Development

Resist development immediately followed the e-beam exposure, and was done by immersing the resist for 3 min in a liquid developer (MIBK : IPA = 1 : 3).

Figure 3.14 shows an optical image of the developed resist pattern in (a), and a magnified view in (b) for the SETs area. (c) and (d) show two 1 \( \mu \)m NW SETs and two ‘point-gate’ NW SETs, respectively. The surrounding 16 interconnect areas were also exposed using EBL to connect the fine features with the coarse features. The circular exposed regions in (a) are caused by the absence of a beam blanker when multiple writing fields were used with high beam current (> 300 pA).
Figure 3.14.: Optical image of development results for two types of NW SETs.

7. Metal deposition and lift off

A 30 nm thick layer of Al was evaporated on top of the resist-coated sample at a chamber pressure $< 2.2 \times 10^{-6}$ mbar. The Al-coated sample was then immersed overnight in acetone to lift off the unwanted metal films. A burst ultra-sonic bath was always used to help the lift-off process.

Figure 3.15 shows the metal hard mask for fine features in (a). A magnified view of for both types of NW SETs are shown in (b).
Figure 3.15.: Optical image of lift-off results (metal hard mask) for two types of NW SETs.

8. Coarse feature patterning

Optical photolithography was used to define the bond-pad regions in metal, aligned to the EBL patterns.

- Photoresist spin-coating

A 3.5 \( \mu \text{m} \) thick resist layer was formed on top of the metallised chip, using a positive resist S1828, which was spun coated, first at 500 rpm for 10 seconds followed by an acceleration to 4500 rpm over 40 seconds.

- Photoresist baking

The resist S1828 was baked on a hot plate for 1 minute each temperature of 65 °C, 85 °C and finally 115 °C, to dehydrate and harden the photoresist.

- Optical alignment by using photolithography

A light-field mask, shown in Figure 3.16, was used to pattern the photore sist with a fixed exposed energy, which is the product of a power density of 5.3 mW/cm\(^2\) and duration of 160 s. This step also required an alignment with the prepared metallised-NW pattern with a planar-offset error tolerance of 5 \( \mu \text{m} \) and a rotation error tolerance of 2°.
Development

MF319 was used to selectively remove the exposed regions. Figure 3.17 shows optical patterns following 2 min, 4 min and 6 min development. A development time of 4 min is a sensible choice to make, where the pink regions are the developed features and the orange region is covered by resist. In practice, a slight over-exposure is used, leading to a slight larger mesa and lead-in areas. This can reduce the difficulty of alignment when making ohmic contacts subsequently by optical lithography. An optical image of the whole pattern including the SETs pattern is shown in Figure 3.18. The green regions are the mesa and lead-in areas. The central yellow features are the metallised-NW pattern. The rest of area in Figure 3.17 is covered by S1828 resist.

Plasma descum

A 3 minute descum stage followed for residual ashing and edges trimming with flow rate: $O_2$ - 800 sccm, $Ar$ - 5 sccm and power 100 W.
9. Pattern transfer and thermal oxidation

- Metal deposition and lift-off

As the photoresist S1828 was 3.5 μm in thickness, an Al 100 nm can be easily removed by lift-off. The metal hard mask is formed, shown in Figure 3.19.

- RIE and thermal oxidation

The complete whole metal pattern, i.e. NW, lead-in and mesa areas, was transferred into the doped Si layer using RIE in SF₆, at the flow rate: SF₆ - 30 sccm
and O\textsubscript{2} - 10 sccm with pressure 100 mbar and power 200 W. This leads to a trench depth of \(~\sim\)200 nm with 1 min etching, to isolate the NW from the gates, shown in Figure 3.20 (a). The metal was then removed by wet etching in Al etchant solution for 1 min.

![SEM images](image)

Figure 3.20.: SEM images of the whole pattern after RIE (a) before thermal oxidation (b) after thermal oxidation (c) 1 \(\mu\)m NW SET after thermal oxidation (d) point-gate NW SET after thermal oxidation

The sample was then passivated by thermal oxidation at 1000\(^\circ\)C for 30 minutes followed by a natural cool-down to 300\(^\circ\)C lasting 2 hours until the sample could be removed. The Figure 3.22 shows the SEM images of the SiNW after RIE and wet etching before thermal oxidation in (a) and after in (b). This was used to grow an oxide layer \(~\sim\)10 nm thick, and would be reduced the Si core of the NW to an estimated range \(~\sim\)10 to 30 nm. The 1 \(\mu\)m NW and ‘point-gate’ NW SET devices are shown in a magnified view of (b) in Figure 3.20 (c) and (d), respectively. Figure 3.21 shows a cross-sectional schematic diagram of SiO\textsubscript{2} film growth (light blue) on a Si substrate (dark blue) by thermal oxidation at 1000\(^\circ\)C for 30 min, where \(W_1\) and \(W_2\) are the un-oxidised SiNW width and the Si core width after oxidation, respectively. \(d_1\) is the depth of consumed Si. The
sum of $d_1$ and $d_2$ is the thickness of the grown SiO$_2$ film. The ratio for $d_1 : (d_1 + d_2) = 0.44$ [121]

Figure 3.21.: Cross-sectional schematic diagram of thermal oxidation process before (left) and after (right)

For the device in Figure 3.22, the width of the un-oxidised NW $W_1 = 58$ nm. Using the oxidised NW width $W_2 + 2(d_1 + d_2) = 77$ nm from Figure 3.22, this gives us an unoxidised Si core diameter of $W_2 \sim 40$ nm, ignoring non-uniformity in the oxide layer. For device shown in Figure 3.20 (c), $W_1 = 88$ nm, $d_1$ and $d_2$ are remained due to the same parameter used for oxidation, leading to a Si core $W_2 \sim 39$ nm. Any variation in the NW Si core width/height can create tunnel barriers/islands along the NW, forming a MTJ device in NW or an SET with single or a couple of islands.

Figure 3.22.: SEM images of the ‘point-gate’ SiNW SET after thermal oxidation

10. Ohmic contact bond pads and wire bonding

The devices used Ohmic contacts, formed by deposition of a 200 nm Al on top of a 20 nm Cr layer. The Cr layer here was used to improve the adhesion between the Al and Si, and thereby reduce the possibility of damaging the pads in the wire-
bonding stage. These were defined by optical lithography using the same mask as for the mesa. As the mesa regions were overexposed during optical lithography, these were slightly larger (\(\sim 3\ \mu\text{m}\)) than the developed bond pad areas. This ensured that contact was made only to the doped silicon to prevent any leakage from the top layer to the substrate via misaligned contacts. Therefore a second alignment was required here with error tolerance even smaller, which resulted from the difference between the overexposure and normal exposure.

Figure 3.23 shows optical diagrams of second alignment to open windows on top of SiO\(_2\) for ohmic contact. The central area is shown in Figure 3.23 (a) and the lead-in and mesa areas are shown in (b). As the dark edges (photoresist) were inside/on the edge of the bright area (lead-in and mesa areas) shown in Figure 3.23 (b), the possibility of leaking for the subsequent bond pads were reduced.

The process flow for photolithography is the same as in the ‘Coarse feature patterning’. After that a burst buffered-HF dip was required for removing the SiO\(_2\) to open windows for subsequently ohmic contact on the bond pads. This was immediately followed by a Cr/Al evaporation/lift-off process. SETs were arranged as groups of four within a 100 \(\mu\text{m}\) square field, and connected to 16 bond pad regions surrounding the field. Finally, all the bond pads were bonded using Au wire in a small dual-in-line package, which could be inserted in a cryostat for electrical measurement.
Electrical characterisation was then performed in a Janis CTI-Cryogenics Model-22 closed cycle refrigeration cryostat, using an Agilent 4155B semiconductor parameter analyser to extract the device characteristics. Electrical measurements were performed at temperature from 8 - 300 K. These results will be discussed in Chapter 4.

3.5. $4 \times 4$ array of SiNW SETs fabrication on SOI material

The results to be discussed in the following chapters from individual devices were used to guide the development of a $4 \times 4$ array of transistors to allow multiple devices to be measured. The details of the fabrication steps are given in the following section. While the $4 \times 4$ array presented here retains the general factors of the fabrication process developed for individual devices, however in the future it is likely that this will evolve further. There were some changes to the process discussed below.

Figure 3.24 shows the layout for the $4 \times 4$ array. The work reported here was undertaken using square chips with 1.8 mm sides. There were 5 electrical contact pads per side, each 200 $\mu$m $\times$ 200 $\mu$m in area. Figure 3.24 (a) shows a 200 $\mu$m $\times$ 200 $\mu$m writing field superimposed on a grid of 10 $\mu$m. Figure 3.24 (b) shows the arrangement of 16 SET devices in a 100 $\mu$m $\times$ 100 $\mu$m writing field. In this circuit, only short NWs or point contacts between and source and drain have been used as these show clean single-electron operations. An optical image of the $4 \times 4$ array after alignment and metallisation is shown in Figure 3.24 (c). The chip is shown in low magnification in Figure 3.24 (d). The structure in (d) was defined using optical lithography. 16 devices are defined within the central 200 $\mu$m $\times$ 200 $\mu$m square, both the SET and interconnect areas were written using electron beam lithography.
The key design differentiator from the individual transistors discussed in Section 3.4 is given below:

1. Single side-gate configuration

The 16 transistors that form the $4 \times 4$ array are now gated on only one side of each NW. This has the advantage that there is a more compact, single-plane design with transistors sharing contacts, and the ability to address individual devices without interconnect cross-over.

2. New mask design:

Compared to the old mask with $4 \times 4$ surrounding bond pads, a new mask design was used (Figure 3.25). Here, there were $5 \times 5$ surrounding bond pads, allowing both coarse (optical) features patterning and precise alignment for ohmic contacts. The possible of requiring a slight over-exposure for the mesa areas was therefore elimi-
nated. The lead-in area pattern is shown in Figure 3.25 (a), and the 180 \( \mu m \times 180 \mu m \) bond pad area pattern is shown in (b). Each pattern, for example (a) shown in Figure 3.25 (c), is duplicated 16 times, forming a 1 cm\(^2\) area. This arrangement allows us to have a yield of SET devices of 16 \( \times \) 16 = 256 per 1 cm\(^2\) chip, providing that there are no failures in other process steps. The 180 \( \mu m \times 180 \mu m \) bond pad area pattern in the new mask shown in (b) has given an error tolerance of 20 \( \mu m \) in both \( x \) and \( y \) directions, leading to an easy optical alignment for ohmic contact. This not only speeds up the whole process but allows investigation of the reproducibility and reliability of SETs fabrication.

![Image](image1.png)

(a) Lead-in area  
(b) Bond pad area

(c) A block of patterns of (a)

Figure 3.25.: Layout of the new mask for 4 \( \times \) 4 array

SEM images of ‘point-contact’ SET devices are shown in Figure 3.26 with single side-gate structures along a \( \sim 50 \) nm NW. As defined, the width of the un-oxidised NW was
54 nm in Figure 3.26 (a). Follow oxidation the NW width was 115 nm, which left a nominal un-oxidised Si core of only \(\sim 5\) nm. For the device in Figure 3.26 (b), a narrower gap of \(\sim 50\) nm can be seen between the wire and gate. An overview of the \(4 \times 4\) array is shown in Figure 3.26 (c). Oxidation of the structure was used to reduce the Si core of the NW to \(\sim 20\) nm. Trenches \(\sim 200\) nm deep were used to electrically isolate the device.

(a) The devices with the smallest NW in width  
(b) The devices with the smallest trench in width

(c) Overview of the \(4 \times 4\) array

Figure 3.26.: SEM image of ‘point-contact’ SETs in the \(4 \times 4\) array, taken before the thermal oxidation for the smallest NW (a) and trench (b) in width, and overview in (c).

The fabrication process discussed in Section 3.4 and 3.5 can be concluded as ‘EBL patterns (fine features) defined first, followed by optical patterns (coarse features)’. The advantage in this approach is that if the NW structure defined by EBL has not reproduced as expected, the process can be repeated from ‘sample preparation’ for EBL and restarting
the subsequent steps with only the wasted effort in fabricating the ‘NW lift-off pattern’, which is relatively short. Since the NW’s lift-off process is most difficult step for the fine features fabrication, it is sensible to put this step in a relatively front position of the whole process flow.

3.6. Alternative SiNW SET fabrication process on SOI material

Compared to the process flow of ‘fine features defined first, followed by coarse features’, another process flow of ‘coarse features defined first, followed by fine features’ can be used as well. Alternatively, a mask-free SiNW SET fabrication process which completely relied on EBL was also used to investigate a reproducible and repeatable SiNW SET fabrication process. In this section, we will discuss two alternative fabrication processes.

3.6.1. ‘Coarse features first defined’ SiNW SET fabrication process

The process flow is summarised here for 10 mm × 10 mm SOI samples, with the top Si layer initially ∼100 nm in thickness, and the BOX layer ∼130 nm in thickness. We thinned the top-Si of this sample to ∼20 nm or less. The samples were initially p-type doped ∼10^{15} \text{ cm}^{-3}) and spin-on dopant (phosphorus) was used to heavily-dope the material n-type ∼10^{19} \text{ cm}^{-3}) or higher. If the new mask in Section 3.5 is used, a total of 256 SETs, arranged in 16 groups of 16, could be fabricated simultaneously by using EBL in a heavily n-type doped SOI material with 20 nm top layer thickness.

The process flow is outlined as follows (only step titles will be given if the processing parameters are the same as in previous sections):

1. Coarse feature patterning
   - Photoresist spinning
   - Photoresist Baking
   - Exposure
   - Development
• Metal deposition and lift-off
  
  A layer of Al was deposited to a thickness of ∼100 nm and the unwanted areas were then removed by lift-off.

2. Fine feature patterning

• Resist spin-coating
• E-beam exposure
  
  An EBL alignment is required here to connect the fine features (EBL pattern) to the coarse features (lead-in and mesa areas).
• Development
• Metal deposition and lift-off
  
  The metal hard mask of the whole pattern is formed.

3. Pattern transfer

• RIE
• Wet etching
• Thermal oxidation

4. Ohmic contact bond pads and wire bonding

  Compared to the process flow discussed in Section 3.4 and 3.5 where the alignment can only be done optically with very limited error tolerance and high possibility of misalignment, this process provides a means that enables the Xedraw system to align the fine features to the coarse feature.

  In this way, the advantages are given as follows:

i. Precise: The misalignment error will be minimised from optical level i.e. 5 µm to 0.1µm.

ii. Easy and fast: The whole alignment process is also automatic and pre-defined by programming. The program can also be combined with the EBL pattern program so that the EBL exposure and alignment can be done in one run.
However, due to the absence of beam blanker, the circular overexposed regions generated when picking the marks in the alignment stage, can short-circuit and ruin the whole chip. Subsequently, as the possibility of successful lift-off is not sufficiently high, once the NW structures fail to come up the whole process has to go back to the beginning where there are no EBL or optical patterns, which is quite waste of time.

In conclusion, the ‘Coarse feature first defined’ fabrication process will be used for large scale production in the near future, provided that the beam blanker is installed and a cleaner environment for both fabrication and evaporation is available.

3.6.2. ‘Mask-free’ SiNW SET fabrication process

The involvement of the optical lithography introduces more process steps and errors in the alignment of both the fine features and coarse features. The ‘mask-free’ SiNW SET fabrication process uses only EBL. Thus can complete the fabrication of both fine and coarse features in a heavily $n$-type doped SOI material with 20 nm top layer thickness.

The process flow is as follows:

1. Fine and coarse feature patterning
   - Photoresist spinning
   - Photoresist Baking
   - E-beam Exposure
   - Development
   - Metal deposition and lift-off

2. Pattern transfer
   - RIE
   - Wet etching
   - Thermal oxidation

3. Ohmic contact bond pads and wire bonding
Figure 3.27 shows SEM images of the fabrication results of 1 µm NW SET. The NW width after oxidation is \( \sim 50 \) nm in width shown in (a). The layout of four SiNW SET devices and the alignment between fine features and coarse features are shown in (b). A overview of the whole circuit with the dimension of mesa areas of 200 µm × 200 µ is shown in (c).
This process flow has the following advantages:

i. No alignment needed: As both fine and coarse features are defined by using EBL, there is no alignment issue because the displacement error is less than the beam step size which is 2 nm.

ii. No mask needed: As the mesa and lead-in area is defined by using EBL, the optical mask is no longer necessary. In the ‘Ohmic contact bond pads and wire bonding’ step, EBL can also be used to align and open the windows for ohmic contact precisely.

iii. Simple: As this process purely relies on EBL, all the optical related process steps are eliminated.

The disadvantages, however, are given as follows:

i. As the patterns are written by e-beam in one exposure, the exposure time will become tremendously long that the filament is very likely to blow up in the middle of the exposure.

ii. As the total written area, including lead-in and mesa areas, becomes very large, the focus during a large exposure time may degrade and for large scale production a consistent focus from the beginning to the end of the exposure cannot be guaranteed.

iii. Due to the absence of beam blanker and high beam current used for mesa areas, there were a lot of unwanted connections and circular unexposed regions (shown in Figure 3.27 (c)).

Because of these, even if the size of NW may be electrically small enough (shown in Figure 3.27 (a)), the devices still cannot be measured due to short-circuits.

3.7. Summary

This chapter has presented the electron-beam lithography (EBL) in detail, used for device fabrication based on the Xenos pattern generator system. Here, the beam formation, system interface, electron-beam resist, sample preparation, e-beam exposure and resist development have been discussed. In particular, the relationship between the EBL parameters and EBL results has been given in the Table 3.1. Furthermore, following experiments
for beam optimisation, the best parameters for lithography were provided in Table 3.2. A
detailed fabrication process flow is provided in Appendix A. The spin-on-doping (SOD)
and thermal oxidation results and have also been discussed. Here, the oxidation thickness
determines the dimensions of the device Si core and directly impacts on the electrical and
simulation results in Chapter 4 and 5.
4. Electrical characterisation: results and discussions

This chapter considers the electrical characteristics of Si nanowire SETs in detail. Drain-source current ($I_{ds}$) vs. drain-source voltage ($V_{ds}$) and gate-source voltage ($V_{gs}$) electrical measurements were performed on both 1 μm NW and point-gate devices at low temperature. We first report the characteristics of the 1 μm NW SET, and then the characteristics of the point-gate SET. In the latter case, a transition occurs to the observation of clear quantum dot behaviour in the $I$-$V$ characteristics. In a point-contact SET, single-electron effects were observed at room temperature. A $4 \times 4$ array of heavily oxidised SETs was also fabricated and characterised, to determine the percentage of devices with single-electron behaviour.

4.1. 1 μm NW SET devices

In this section, the source-drain characteristics of a 1 μm NW SET, are discussed as a function of temperature from 8 to 300 K. ‘Coulomb staircase’ $I_{ds}$ vs. $V_{ds}$ characteristics have been observed at 8 K, and the Coulomb gap modulated periodically by $V_{gs}$. The current steps thermally broaden into a non-linearity, which persists to 300 K.

Figure 4.1 shows the $I_{ds}$ vs. $V_{ds}$, $V_{gs}$ characteristics of the 1 μm NW device at 8 K. Here, a low current ‘Coulomb blockade’ region [18] is observed with a width varying from ±3 V to ±5.5 V. This very wide Coulomb gap is indicative of the formation of an MTJ along the NW [13, 122]. Single-electron oscillations [18] with a period ~3.75 V, can be seen in $I_{ds}$ (e.g. along the line $V_{ds} = -7$ V) as $V_{gs}$ is swept from 0 to 30 V. While the Coulomb gap cannot be reduced to zero, triangular regions corresponding to half-Coulomb diamonds are observed along the edges of the central Coulomb blockade region. This implies an effective
single-electron (SE) gate capacitance \( C_g \approx e/\Delta V_{gs} = 0.043 \text{ aF} \). The very small value of \( C_g \) is due to the wide NW-gate spacing in this device.

Figure 4.1: \( I_{ds} \) vs. \( V_{ds}, V_{gs} \) characteristics of the 1 \( \mu \text{m} \) NW device at 8 K

Selected \( I_{ds} \) vs. \( V_{ds} \) characteristics are shown in Figure 4.2 (a) with curves offset from each other in \( I_{ds} \) for clarity. Arrows mark the threshold voltage for current flow for positive and negative \( V_{ds} \), where \( V_{th1} \) and \( V_{th2} \) indicate the maximum and minimum range of threshold voltages. \( \log|I_{ds}| \) vs. \( V_{ds} \) are shown in Figure 4.2 (b). The current ratio \( I_{max}/I_{min} \), for points at twice the Coulomb gap and at the centre of the Coulomb gap is \( 5 \times 10^5 \). The Coulomb staircase is significant and stable.

Figure 4.2: Selected \( I_{ds} \) vs. \( V_{ds} \) curves of the 1 \( \mu \text{m} \) NW device (a) and in logarithmic scale (b)
Figure 4.3 shows the temperature dependence of the log|I_{ds}| vs. V_{ds} characteristics at gate voltage V_{gs} = 0 V of a 1 µm long NW SET, from 8 - 300 K. Temperature is varied in 20 K steps from 20 K to 300 K. For clarity the curves at each temperature are shown offset by 0.1 nA per temperature step.

Figure 4.3: I_{ds} vs. V_{ds} characteristics of the 1 µm NW device in logarithmic scale from 8 - 300 K

Figure 4.4 shows the data of the same device using a linear scale, with different limits to emphasise features at low temperature (8 K) in (a), and high temperature (300) in (b). These show a significant current staircase and low current Coulomb blockade regions at low temperatures < 220 K, shown in Figure 4.4 (a). This behaviour, corresponding to the Coulomb gap, also persists and can be observed at higher temperature. Traces of these effects persist even at room temperature, labelled by the arrow in Figure 4.4 (b). Here,
the single electron behaviour has been overcome progressively by thermal fluctuations.

Figure 4.4: $I_{ds}$ vs. $V_{ds}$ characteristics for the data of Figure 4.3, from 8 - 300 K range. Range of $V_{ds}$ is reduced from $\pm 10$ V (a) to $\pm 0.5$ V (b), Figure 4.5 (a) shows an Arrhenius plot of $\ln |I_{ds}|$ vs. inverse temperature $T^{-1}$ for the data, at $V_{ds} = 0.075$ V, and $V_{ds} = 0.5$ to 5 V in 0.5 V steps. For low $V_{ds} = 0.075$ V, a thermally activated current region is observed above 200 K. For $T < 200$ K, only a weakly-temperature dependent current is observed. The later corresponds to a region where Coulomb blockade effects are significant. The slope of the Arrhenius plot in the thermally activated region ($T > 200$ K) can be used to extract the activation energy, as follows:

$$E_a = k_B \frac{\Delta \ln |I_{ds}|}{\Delta T^{-1}}.$$ 

Figure 4.5 (b) shows a linear fit to the data in the temperature range 200 to 300 K, for
drain voltage $V_{ds} = 0.075$ V. The slope of the fit can be used to extract $E_a = 0.276$ eV $\pm 1.8 \times 10^{-3}$ eV (i.e. $\pm 0.66\%$).

Figure 4.5.: (a) Arrhenius plots of $\ln|I_{ds}|$ vs. $T^{-1}$, as $V_{ds}$ is varied from 0.075 V to 5 V. $V_{ds}$ varied in 0.5 V steps for $V_{ds} > 0.5$ V. (b) Linear fit (solid line) to Arrhenius plot of (a), for $V_{ds} = 0.075$ V for the data from 200 - 300 K. Error bars represent 1% error in the estimation of $\ln|I_{ds}|$.

We now discuss the formation of islands along the MTJ. Following the final oxidation stage for passivation, the Si core width of the NW is estimated to be $\sim 10$ - 20 nm. In these NWs, roughness of the SiO$_2$/Si interface, in combination with disorder in the interface state density or doping concentration variation, can pinch-off sections of the NW and
create a chain of tunnel barriers and conducting islands. In the 1 \( \mu \)m NW, the Coulomb gap is very large (see Figure 4.1), as this is a function of the combined charging energies of many islands along the NW. The Coulomb gap reduces with increasing temperature (Figure 4.3), implying a variation in island size, where because of their smaller charging energies, thermally activated currents overcome single-electron effects in the larger islands first. The maximum temperature for single-electron effects is determined, either by the size of the smallest island and/or by the heights of the tunnel barriers.

To further investigate and understand the electrical characteristics of 1 \( \mu \)m NW SET devices, a single-electron Monte Carlo simulation is used, which will be discussed in Chapter 5.

4.2. Point-gate SET devices

We now consider the electrical characteristics of the point-gate SET shown in Figure 3.20. The SET point-gate tips are \( \sim \)50 nm wide and this determines the length of the NW section which can be modulated.

Figure 4.6 shows strong Coulomb staircases in the \( I_{ds} \) vs. \( V_{ds}, V_{gs} \) characteristics at 8 K, as \( V_{gs} \) varies from 0 to 5 V. In comparison with the 1 \( \mu \)m NW device, the width of the Coulomb gap is significantly reduced, to between \( \sim \pm 0.2 \) V to \( \pm 0.8 \) V. This demonstrates that as the NW length is reduced, the number of islands in the MTJ is also reduced.

![Figure 4.6: \( I_{ds} \) vs. \( V_{ds}, V_{gs} \) characteristics of a point-gate SET at 8 K](image-url)
Figure 4.7 (a) shows the $I_{ds}$ vs. $V_{ds}$, $V_{gs}$ characteristics from the same device plotted on a linear (a) and log scale (b), as $V_{gs}$ varies between 1.375 V and 2.5 V in steps of 0.125 V. The Coulomb gap is 0.3 V wide and a regular multiple-step Coulomb staircase is seen. In the plot of log$|I_{ds}|$ vs. $V_{ds}$ (Figure 4.7 (b)), the Coulomb staircase is very stable, and modulated between two distinct curves (S1 and S2). Figure 4.7 (c) shows single-electron oscillations in the $I_{ds}$ vs. $V_{gs}$ characteristics for $V_{ds}$ values from -0.9 V to +0.9 V.
Figure 4.7.: Source-drain characteristics, $I_{ds}$ vs. $V_{ds}$, point SET, at 8 K (a) linear $I_{ds}$ scale, (b) log|$I_{ds}$| scale showing the reproducibility of the characteristics. (c) Selected curves from the plot of Figure 4.6, used to show the single-electron oscillations in the $I_{ds}$ vs. $V_{gs}$ characteristics for $V_{ds}$ values from -0.9 V to +0.9 V. Here, circles show the data points and the curves are interpolated fits through the points.
The region for $V_{gs} < 1.5$ V is shown in detail in Figure 4.8 (a) 3-D plot and (b) contour plot, using drain-source conductance $g_{ds}$ vs. $V_{ds}$, $V_{gs}$ characteristics extracted from the data of Figure 4.6. Large and small Coulomb diamond regions can be observed highlighted by white lines in 4.8 (b), centred at $V_{gs} \sim 0.6$ V and $0.125$ V respectively.

A contour plot of log $|I_{ds}|$ vs. $V_{ds}$, $V_{gs}$ from the same ‘point-gate’ SET device is given in Figure 4.9. It shows a complex structure with $V_{gs}$, creating current peaks/valleys (marked 1 - 9), some of which (3 - 9) are parallel to the $V_{ds}$ axis. For $V_{gs}$ values from 0 to 1.5 V, Coulomb diamond characteristics can be seen (e.g. highlighted by L1 and L2), and the Coulomb gap width is modulated between $\pm 0.5$ V. For $V_{gs} = 1.5$ to 5 V, the Coulomb gap modulation is relatively weak. The current valley lines in Figure 4.9 are arranged in groups, (group A: lines 1 - 2, group B: lines 3 - 5, group C: lines 6 - 8, and line 9). Lines 3 - 9 are parallel to the $V_{ds}$ axis, implying that the underlying electron levels are decoupled from $V_{ds}$. In contrast, lines 1 - 2 begin at Coulomb diamonds and shift in position with both $V_{ds}$ and $V_{gs}$, implying coupling to both drain and gate terminals.
As the NW length in this device is short $\sim 100$ nm, with only $\sim 50$ nm of this strongly coupled to the gate, the number of gated islands possible along the NW is limited. Furthermore, the observation of current lines in groups A - C may be associated with quantum confinement levels [18] in quantum dots formed in the NW.

The main features of the electrical characteristics of the point-gate NW device shown in Figure 3.20 (d), are as follows:

(i) A strong multiple-step Coulomb staircase is seen, implying very different values of tunnel resistances coupling the island(s). The observation of a staircase with uniform step widths shown in Figure 4.7 (a), reduces the likelihood of a many-island MTJ, where steps are weak or irregular.

(ii) The Coulomb gap is modulated by both $V_{ds}$ and $V_{gs}$ and Coulomb diamonds are observed in the region $0 < V_{gs} < 1.5$ V (highlighted by white lines, Figure 4.8). Coulomb diamond 1 (centred at $V_{gs} \sim 0.6$ V). This behaviour has been attributed theoretically to multiple tunnel junctions, e.g. two series, gate-coupled quantum dots can create major Coulomb diamonds with smaller, subsidiary diamonds intermediate to these [123]. Furthermore, as the Coulomb gap in Figure 4.8 cannot be reduced
to zero, there may be a third quantum dot, decoupled from the gate. This may be contrasted with SETs with a single quantum dot, where the Coulomb diamonds can be suppressed by increasing gate voltage due to an increasing channel current or a reduction in tunnel barrier resistance, such that the quantum dot becomes delocalised [11,124]. For the region $1.5 \, V < V_{gs} < 5 \, V$, there are only small variations in the Coulomb gap width.

(iii) When $V_{gs} > 1.5 \, V$, the edge of the Coulomb gap and the position of the current steps occurs at approximately the same value of $V_{ds}$. This implies that in this range of $V_{gs}$, the corresponding charging island(s) couples only to $V_{ds}$ and not to $V_{gs}$.

(iv) Lines 1 - 2 begin at Coulomb diamonds and shift diagonally across the plot, implying electrostatic coupling to both $V_{ds}$ and $V_{gs}$.

(v) Lines 3 - 9 are almost parallel to the $V_{ds}$ axis, implying that the corresponding energy levels couple strongly to $V_{gs}$ and only very weakly to $V_{ds}$. Furthermore, these lines exist in groups (3 - 5, 6 - 8) with a small line spacing within a group and a wider spacing between groups. This resembles the energy spectrum of a quantum dot including both charging and excited states [72].

(vi) Hexagonal regions of charge stability are not observed [123], precluding the possibility of electrostatically coupled quantum dots.

The patterns in Figure 4.9 may be compared to those typically observed in quantum dots [125]. In particular, our observation of lines parallel to the $V_{ds}$ axis (point (v)) is not typically seen in quantum dots. Furthermore, points (iii) and (v) are difficult to reconcile with a single quantum dot, as the Coulomb gap would need to couple only to $V_{ds}$ for point (iii), and lines 3 - 8 would need to couple only to $V_{gs}$ for point (v). However, it is possible to explain the characteristics using a model based on two quantum dots, where one quantum dot couples strongly to the source, but not to the gate, and another quantum dot couples strongly to the gate, but only weakly to the source. Decoupling of a quantum dot from the source electrode, by a strong intermediate potential barrier has been observed previously in single-electron transfer devices [126].
We investigate the characteristics of Figure 4.6 and Figure 4.9 by considering a circuit configuration of three independent quantum dots. The circuit diagram for this is shown in Figure 4.10 (a). QD0 is decoupled from the gate and tunnel couples to $V_s$. This prevents $V_{gs}$ from reducing the Coulomb gap completely to zero. QD1 tunnel couples to the intermediate section of the NW, and is coupled capacitively by $C_{g1}$ to $V_g$. QD2 tunnel couples to intermediate NW section and to the drain, and is coupled to capacitively by $C_{g2}$ to $V_g$. $C_{g1}$ is used in the model only when $V_{gs} < 1.5$ V. As we do not observe hexagonal charge stability regions [127] in Figure 4.9, we do not consider direct electrostatic or tunnel coupling between QD1 and QD2. Applying $V_{ds}$ pulls the Coulomb gaps in the relative to the source Fermi energy $E_{FS}$. However, QD2 is separated by its left-hand side tunnel barrier and by QD0 and QD1 from the source. Assuming the most of $V_{ds}$ drops across QD0 and QD1, e.g. due to tunnel barrier, this limits the shift in the potential of QD2 with $V_{ds}$. The energy levels in QD1 and QD2 at $V_{ds} = V_{gs} = 0$ V are shown in Figure 4.10 (a). The Coulomb gap and confinement levels in QD1 are $E_{C1}$ and $a - c$ respectively, and in QD2 are $E_{C2}$ and $\alpha - \gamma$ respectively. Applying $V_{ds}$ pulls the levels in QD1 down relative to the , due to strong coupling between QD1 and the source. Furthermore, QD2 is decoupled by QD1 from the source.

![Circuit diagram and energy diagrams](a) Circuit diagram for the point-gate SET of Figure 4.9. Schematic energy diagram for (b) $V_{ds} = V_{gs} = 0$ V, (c) for $V_{ds} = V_{d1} > 0$ V and $V_{gs} = V_{gs1} > 0$ V and (d) for $V_{gs2} > V_{gs1}$.

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The shapes of the diamonds in Figure 4.8 (a-b) with point ii, suggests that there are at least two gate coupled QDs (QD1 and QD2), and the persistence of a Coulomb gap at all values of $V_{gs}$ suggests the presence of a third QD (QD0) decoupled from the gate. Therefore, the formation of large and small Coulomb diamonds can be attributed to QD1 and QD2.

The region $V_{gs} > 1.5$ V in Figure 4.9 is now considered i.e. Figure 4.10 (a) excluding $C_{g1}$. As $V_{gs}$ increases, the tunnel barrier potentials are pulled down relative to the Fermi energy [124]. For a distribution of tunnel barrier heights, likely in our un-patterned NWs, a QD with relatively low tunnel barrier height may then become de-isolated and no longer contribute to the Coulomb blockade. In the model of Figure 4.10 (a), if QD1 is de-isolated, then only QD0 and QD2 remain significant. Figure 4.10 (b) shows the energy levels in QD0 and QD2 at $V_{gs} = V_{ds} = 0$ V, where the presence of both Coulomb gaps ($E_{C0}$ and $E_{C2}$) and quantum confinement levels $a - c$ and $\alpha - \gamma$ are assumed. Figure 4.10 (c) shows the situation when $E_{C0}$ is overcome by $V_{ds}$ at $V_{gs} = V_{gs1}$. Level ‘$a$’ aligns with $E_{FS}$ and current can flow across the QDs. This corresponds to line 3 in Figure 4.9. Increasing $V_{ds}$ charges QD0 with electrons one by one, leading to a Coulomb staircase in the $I_{ds} - V_{ds}$ characteristics.

When $V_{gs} > V_{gs1}$, energy levels $\alpha - \gamma$ are pulled down successively below level ‘$a$’ in QD0 and within the energy window $E_{FS} - E_{FD}$. Assuming the tunnelling rate for electrons leaving QD2 towards the drain is lower than for tunnelling onto QD2 from QD0, electrons can persist on QD2 and lead to a current valley [72]. This leads to lines 3 - 5 in Figure 4.9. When $V_{gs2}$ is reached, shown in Figure 4.10 (d), QD2 charges by one electron, filling level ‘$\alpha$’, and shifting levels $\beta - \gamma$ to higher energies. As $E_{C2}$ is greater than the energy level spacing $\Delta E$, the separation between lines 5 - 6 is greater than between lines 4 - 5, creating the groups of lines seen in Figure 4.9.

In the region, $0$ V $< V_{gs} < 1.5$ V, the presence of Coulomb diamonds and the diagonal shift in lines 1 - 2 implies that QD1 also couples to $V_{gs}$, via $C_{g1}$. As $V_{gs}$ increases $> 1.5$ V, the effect of $C_{g1}$ reduces. This behaviour can be caused by the possibility of stochastic tunnelling between charging levels on two QDs [128]. In this model, electrons tunnel across a junction intermediate to the two QDs, between ladders formed by charging states. Here, the corresponding conductance peaks can be grouped, with equal spacing within groups.
As we observe unequal spacing between lines within both group 1 and 2 (Figure 4.9), this suggests that the origin of the lines includes both charging and quantum confinement. However, in the stochastic tunnelling model, the QDs are tunnel coupled, which would lead to the formation of hexagonal charges stability regions. As we do not observe this in Figure 4.9, a model with independent QDs lying at different points along the NW is more likely.

4.3. 4 × 4 array of SiNW SETs

In order to determine the percentage of point-contact SETs fabricated simultaneously in the same process, where single-electron effects occurs, a 4 × 4 array of devices was characterised. In this section, the electrical characteristics of the array at 8 K are presented. Measurements are also presented for a SET with operating at room temperature. Here, Coulomb blockade and a current oscillation with gate voltage are observed.

The results of the characteristics of the 16 devices within the array are summarised in Table 4.1. The device numbers are labelled in the optical micrography of the 4 × 4 array shown in Figure 4.11.

<table>
<thead>
<tr>
<th>Device No</th>
<th>SET Type</th>
<th>Lithography Quality</th>
<th>Coulomb Blockade</th>
<th>Coulomb Staircase</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PC</td>
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<td>✓</td>
<td>✓</td>
<td>unpatterned island</td>
</tr>
<tr>
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<td>✓</td>
<td>✓</td>
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</tr>
<tr>
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<td>PC</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>unpatterned island</td>
</tr>
<tr>
<td>4</td>
<td>PC</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>unpatterned island</td>
</tr>
<tr>
<td>5</td>
<td>PC</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>unpatterned island</td>
</tr>
<tr>
<td>6</td>
<td>PC</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>unpatterned island</td>
</tr>
<tr>
<td>7</td>
<td>NW</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>unpatterned island</td>
</tr>
<tr>
<td>8</td>
<td>NW</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>unpatterned island</td>
</tr>
<tr>
<td>9</td>
<td>PC</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>unpatterned island</td>
</tr>
<tr>
<td>10</td>
<td>NW</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>unpatterned island</td>
</tr>
<tr>
<td>11</td>
<td>NW</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>unpatterned island</td>
</tr>
<tr>
<td>12</td>
<td>PC</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td>unpatterned island</td>
</tr>
<tr>
<td>13</td>
<td>PC</td>
<td>poor</td>
<td>n/a</td>
<td>n/a</td>
<td>unpatterned island</td>
</tr>
<tr>
<td>14</td>
<td>PC</td>
<td>✓</td>
<td>n/a</td>
<td>n/a</td>
<td>Influenced by SET13</td>
</tr>
<tr>
<td>15</td>
<td>PC</td>
<td>✓</td>
<td>n/a</td>
<td>n/a</td>
<td>Influenced by SET14</td>
</tr>
<tr>
<td>16</td>
<td>PC</td>
<td>✓</td>
<td>n/a</td>
<td>n/a</td>
<td>Influenced by SET15</td>
</tr>
</tbody>
</table>
As discussed in Chapter 3, the 16 SETs each have a single side gate, and some source/drain, and gate contacts are shared between different SETs to allow a reduction in the number of external contact terminals to 20. Because of the interconnections of this chip design and the inter-connectivity of the devices, any problem in a shared contact affects more than one SET. There are two ‘SET types’. One is point gate (PC) SET with a gate length 50 nm, the other is ‘NW’ SET device, with a NW length of $\sim 250$ nm (differentiated in column 2 of Table. 4.1). In the most case, a SET’s gate leakage can be rendered inoperable, e.g. can cause SETs 1-4 or 5-8 etc. to be inoperable. In the chip of Figure 4.11, sub-standard lithography (gate and nanowire were connected) affecting device 13 had a ‘knock-on’ effect and prevented characterisation not only of device 13, but also of devices 14, 15, and 16.

The performance of the 16 devices is summarised a follows:

(i) There was a lithographic error in device 13. This impacted on the three contacted devices, 14, 15 and 16, making them non-operational.

(ii) 4 devices, No.6, 8, 10 and 11, showed Schottky diode-like characteristics.

(iii) 8 out remaining 12 devices showed single-electron effects. In these devices, Coulomb staircase with multiple current steps was observed at low temperature.

(iv) The magnitude of the Coulomb gap varied between 0.3 V and 0.7 V

(v) There was a high degree of consistency in the behaviour of these SETs.
(vi) One device showed Coulomb oscillation at room temperature (300 K).

The $I_{ds}$ vs. $V_{ds}$ characteristics at 10 K, for devices 1 - 5, 7 and 9 are shown in Figure 4.12.

![Figure 4.12: $I_{ds}$ vs. $V_{ds}$ characteristics at 10 K, for devices 1 - 5, 7 and 9. The curves are offset by 10 pA for clarity. The curves were measured with a positive sweep of $V_{ds}$ from 0 V, and then a negative sweep of $V_{ds}$ from 0 V. This implies that the current step at $V_{ds} = 0$ V in some of the curves is a measurement artefact.](image1)

Figure 4.12: $I_{ds}$ vs. $V_{ds}$ characteristics at 10 K, for devices 1 - 5, 7 and 9. The curves are offset by 10 pA for clarity. The curves were measured with a positive sweep of $V_{ds}$ from 0 V, and then a negative sweep of $V_{ds}$ from 0 V. This implies that the current step at $V_{ds} = 0$ V in some of the curves is a measurement artefact.

The full $I_{ds}$ vs. $V_{ds}$, $V_{gs}$ characteristics of device 12 are shown in Figure 4.13 (a), where the gate oscillations in the central Coulomb blockade region can be seen. These oscillation can also be seen in the $I_{ds}$ vs. $V_{ds}$ curves in Figure 4.13 (b). However, these oscillations are relatively weak in comparison with the oscillations of devices discussed in Section 4.2. This is primarily attributed to the fact that the nanowires of the device 12 had a somewhat larger width of $\sim 70$ nm, which is wider than devices discussed in Section 4.2.
4.3.1. Room Temperature SET operation

Figure 4.14 shows room-temperature Coulomb blockade $I_{ds}$ vs. $V_{ds}$, $V_{gs}$ characteristics from device 9, with a heavily oxidised 50 nm × 50 nm NW. The SEM image of this device is shown in Figure 3.26 (a). These devices were heavily oxidised with an oxide thickness of 55.5 nm; it is estimated that the Si core of the device has a width of only 5 nm. In the 3-D plot shown in Figure 4.14 (a), a low current Coulomb blockade region is seen with Coulomb gap width $\Delta V_C = e/C_T = 1$ V, where $C_T$ is the total island capacitance. This implies $C_T = 0.16$ aF in the device. For larger values of $V_{ds}$, $I_{ds}$ increases in a non-linear manner and traces of a current step are visible, e.g. at $V_{ds} \approx -1$ in the $I_{ds}$ vs. $V_{ds}$ curves at $V_{gs} = 9$ V. A large current peak is observed in $I_{ds}$ as $V_{gs}$ increases, with a shift towards increasing values of $V_{gs}$ as $V_{ds}$ increases. Figure 4.14 (b) shows $I_{ds}$ vs. $V_{gs}$ as $V_{ds}$ is increased from -5 V to +4.6 V in 0.4 V steps. These characteristics may be attributed to room-temperature single-electron charging of an isolated island along the NW, with charging energy $E_C = e^2/2C = 0.5$ V $\gg k_B T = 26$ meV at 300 K. While multiple current peaks are not observed in this device within our $V_{gs}$ range, the behaviour is similar to other reported work on room-temperature Si SETs using patterned islands [73, 129, 130], where only a few peaks, or even a single peak [129], have been observed.
Figure 4.14: $I_{ds}$ vs. $V_{ds}$, $V_{gs}$ characteristics for a 50 nm NW SET at 300 K. Single-electron operation is observed, with Coulomb blockade in the $I_{ds}$ vs. $V_{ds}$ characteristics and a single-electron oscillation in the $I_{ds}$ vs. $V_{gs}$ characteristics. (a) Three-dimensional plot and (b) $I_{ds}$ vs. $V_{gs}$ characteristics as $V_{ds}$ is increased from -5 V to 4.6 V.

Figure 4.15 shows an SEM image of another SET device (SET7) before oxidation in the $4 \times 4$ array, where the NW length $L = 250$ nm and an un-oxidised width $W_1 = 80$ nm, leading to a Si core $\sim 30$ nm.

Figure 4.15.: SEM image of SET7 with a NW length of $\sim 250$ nm

In combination with two other room temperature $I_{ds}$ vs. $V_{ds}$ characteristics, Figure 4.16 (a) shows the $I_{ds}$ vs. $V_{ds}$ characteristics of three different types of SET devices, where the NW length and width ($L$, $W$) are also given as inset. From the slopes of curves
in (a), the resistivity $\rho$ for each device can be obtained by:

$$\rho = \frac{RA}{L}$$

where $R$ is the slope of the curve, $A = LW$ is the cross-section of the NW in each device, i.e. the product of NW length and width. This gives $\rho_1 = 0.02$ for 50 nm NW SET, $\rho_2 = 0.024$ for 250 nm NW SET and $\rho_3 = 0.032$ for 1 $\mu$m NW SET.

Figure 4.16.: (a) $I_{ds}$ vs. $V_{ds}$ characteristics for 50 nm/5 nm, 250 nm/30 nm and 1 $\mu$m/40 nm ($L/W$) NW SET at 300 K. (b) The resistivity $\rho$ as a function of the NW length $L$ for the three types of SET devices, with a linear fit.

This resistivity corresponds to a doping concentration of $\sim 8.57 \times 10^{18}$/cm$^3$, which is a good agreement with our spin-on-doping concentration. It also implies that the resistivity increase as the tunnel barriers are formed during the thermal oxidation, and decreases as the NW length reduces.

### 4.4. Summary

This chapter presented the electrical characteristics of scaled Si nanowires in the single electron/quantum confinement limit. Room temperature SET operation was observed in $\sim$50 nm long nanowires where the un-oxidised Si core was only $\sim$5 nm. Nanowires with
width \(\sim 30\) nm and length \(1\ \mu m\) to 50 nm, had in-plane parallel or point-gates. It was found that in the \(1\ \mu m\) long, uniform nanowires, strong single electron effects occurred up to \(\sim 220\) K, and traces of these effects persisted to \(\sim 300\) K. This was associated with the formation of a ‘natural’ 20-QD MTJ along the nanowire. The maximum island charging energy \(E_C = 0.2\) eV, was found to be in good agreement with the activation energy 0.276 eV extracted from Arrhenius plots. Scaling the nanowire gated length to \(\sim 50\) nm using a point-gate device reduced the number of quantum dots along the nanowire to only two and both single electron and quantum confinement effects were observed in the electrical characteristics. Comparison between the \(1\ \mu m\) nanowire and the point-contact two-quantum-dot device showed that as the nanowire length was scaled, quantum effects dominated the electrical characteristics. It was then shown how 16 transistors could be arranged as a \(4 \times 4\) array and were given examples of the single-electron characteristics measured on individual transistors. These results illustrate the significance of quantum effects towards the limits of CMOS at the sub-10 nm scale, and the potential of short Sinanowires for a quantum-effect ‘beyond CMOS’ technology.
5. Device simulation

The electrical characteristics of our devices have been investigated further, using a single-electron simulator, called ‘CAMSET’ [78]. This software utilises a Monte Carlo method for single-electron effects only and does not include quantum confinement effects. In the Monte Carlo method, the data is only output at the time of the first tunnelling event after the specified time. For example, if the step time is set to 1 µs, and tunnelling events happen at 0.5 µs, 0.7 µs, 1.1 µs, 1.4 µs, 1.9 µs, 2.2 µs, and 3.3 µs, then data is output to the plot file at the following times: 1.1 µs, 2.2 µs, and 3.3 µs. It is not possible to trace all of the tunnelling events when using the Monte Carlo method but using a small time parameter (by default 0.01 µs) is the best approach for capturing as many as possible.

5.1. Study of the single-electron effects vs. SET parameters

in Monte Carlo simulation

We first consider the single-electron Monte Carlo simulation for single island SET [30,131, 132]. The circuit diagram is shown in Figure 5.1, where the circuit consists of one island $n_1$, isolated by two tunnel junctions $t_1$ and $t_2$ from source/drain electrode regions. The island $n_1$ is also coupled to an additional gate voltage by a gate capacitor $C_g$. 
Figure 5.1.: The SET circuit diagram

Figure 5.2 shows a simulation of the $I_{ds}$ vs. $V_{ds}$ (Coulomb staircase in (a)) and $I_{ds}$ vs. $V_{gs}$ (Coulomb oscillation in (b)) characteristics of an SET at $T = 4.2$ K. We assume $C_1 = C_2 = 0.2 \text{ aF}$, $C_g = 0.12 \text{ aF}$, $R_1 = 100 \text{ G}\Omega$, $R_2 = 0.16 \text{ G}\Omega$. The curves in Figure 5.2 (a) show a step like manner, the so called Coulomb staircase, caused by significant tunnel resistance mismatch of $R_1/R_2 = 100$, with a step width of $\Delta V = e/C_1 = 0.8 \text{ V (±0.4 V)}$. The curves in Figure 5.2 (b) show that the $I_{ds}$ is a periodic function of $V_{gs}$ at each given $V_{ds}$. These are the Coulomb oscillations, which can be seen in the current $I_{ds}$. The current is also increased as $V_{ds}$ increases. The period of oscillation is $\Delta V_g = e/C_g = 1.33 \text{ V}$.

Figure 5.2.: (a) Coulomb staircase in $I_{ds}$ vs. $V_{ds}$ as $V_{gs}$ varies from 0 to 2 V in 0.05 V steps. (b) Coulomb oscillation in $I_{ds}$ vs. $V_{gs}$ as $V_{ds}$ varies from -2 to 2 V in 0.02 V steps. The curves in (b) and (c) are offset 10 pA from each other for clarity.
Figure 5.3 combining Figure 5.2 (a) and Figure 5.2 (b) to show the $I_{ds}$ vs. $V_{ds}$, $V_{gs}$ characteristics, where a series of rhombic areas, “Coulomb diamond” due to the superposition of Coulomb staircase and Coulomb oscillations, are consisted of a Coulomb gap in the middle. The gap width in $V_{ds}$ corresponds to the width of the charge stability region, where no electrons (current) flows through the island. As a gate voltage applied via a gate capacitor to the island increases from 0 V to $e/2C_g = 0.667$ V, the Coulomb gap width reduces from the maximum width of $\Delta V = 2 \times e/C_T = 0.8$ V to 0 V. Keeping increasing the gate voltage modulates the Coulomb gap from 0 V to 0.8 V periodically.

![3-D plot of Monte Carlo simulation of the $I_{ds}$ vs. $V_{ds}$, $V_{gs}$ at $T = 4.2$ K.](image)

Figure 5.3.: (a) 3-D plot of Monte Carlo simulation of the $I_{ds}$ vs. $V_{ds}$, $V_{gs}$ at $T = 4.2$ K.

Figure 5.4 (a) shows $I_{ds}$ vs. $V_{ds}$ curves at $V_{gs} = 0$ V with different tunnel resistance mismatch ratio, with other parameters unchanged in the last example (Figure 5.2). The curves in Figure reffig:DTJ+R+mismatch (a) are offset 10 pA from each other for clarity. Equal resistance leads to a flat Coulomb staircase curve, which can also be seen in Figure 5.4 (b). However, $R_1/R_2 = 10$ leads to a significant Coulomb staircase. This is because if $R_1 \gg R_2$, and $V_{ds} > \Delta V$, then the island charges up through first junction with a greater probability than the second, leading to a greater tunnel rate of the first junction than the rate of the second junction [133]. If the resistances are equal e.g. $R_1 = R_2 = 16$ GΩ (Figure 5.4 (b)) the oscillations become more symmetric [75] compared to Figure 5.3 because of the equal charge/discharge tunnelling rates of the island.
Figure 5.4.: (a) $I_{ds}$ vs. $V_{ds}$ curves at $V_{gs} = 0$ V for different tunnel resistance mismatch (b) 3-D plot of $I_{ds}$ vs. $V_{ds}$, $V_{gs}$ characteristic for equal resistance (16 GΩ).

Figure 5.5 (a) shows $I_{ds}$ vs. $V_{ds}$ curves at $V_{gs} = 0$ V with different $C_g$ values. The Coulomb gap width $\Delta V$ is affected by the variation of $C_g$, as the gap width $\Delta V = 2 \times \frac{e}{C_T}$, where $C_T = 2C + C_g$. If $C_g \ll C$, then $C_T = 2C$, a greater Coulomb gap arises is shown in Figure 5.5 (a) (blue curve). If $C_g$ becomes considerably large e.g. similar to $C$, the gap width is reduced. Figure 5.5 (b) ($e/C_g=0.012$ aF) and (c) ($e/C_g=0.6$ aF) show the variation of Coulomb oscillation period is $\Delta V_g$. As $\Delta V_g = e/C_g$ [133], the Coulomb oscillation period $\Delta V_g = 13.3$ V. However, in Figure 5.5 (c) the period is 0.267 V. Consequently, seven and half Coulomb diamonds can be seen.
Figure 5.5.: (a) \( I_{ds} \) vs. \( V_{ds} \) curves at \( V_{gs} = 0 \) V for different \( C_g \) values (b) 3-D plot for \( C_g = 0.012 \) aF. (c) 3-D plot for \( C_g = 0.6 \) aF.

Figure 5.6 (a) and (b) show the transition of the shape of Coulomb diamond from relatively symmetric to significantly asymmetric by changing the equal tunnel capacitances \( C_1 = C_2 = 0.2 \) aF to \( 2C_1 = C_2 = 0.2 \) aF. The slope of the diamond edge is determined by the tunnelling rate across the first and second tunnel junction. Equal capacitance leads to a rhombic shape, where the left and right corners lie on the \( x \)-axis, and top and bottom corner lies parallel to the \( y \)-axis, as shown in Figure 5.6 (a) (Ignoring the tiny offset caused by the presence of \( C_g \)). The diamond shape is tilted relative to the \( V_{ds} \) axis due to the capacitances mismatch, shown in Figure 5.6 (b). The capacitances can be derived by from the first intersection between diamond edges and \( x \)-axis, they are given by \( V_{g1} = e/2C_1 \).
and $V_{g2} = e/2C_2$ respectively [13].

Figure 5.6.: Contour plot of the data in Figure 5.3, where $C_1 = C_2 = 0.2 \text{ aF} = e/2C$ in (a) and $2C_1 = C_2 = 0.2 \text{ aF}$ in (b)

5.2. Single-electron effects vs. MTJ parameters in Monte Carlo simulation

To further investigate the $I_{ds}$ vs $V_{ds, V_{gs}}$ characteristics observed in Figure 4.1, the following SE Monte Carlo simulations were run. Figure 5.7 shows a single-electron Monte Carlo simulation of a MTJ at 8 K with all 10 islands coupled to the gate (a) and 50% of islands coupled to the gate. The parameters were used:

$$n = 10, C = C_g = 0.12 \text{ aF}, R_n = \begin{cases} 200 \text{ k}\Omega & \text{if } n \text{ is odd} \\ 20 \text{ M}\Omega & \text{if } n \text{ is even} \end{cases}$$

The Coulomb gap width in (a) is $\Delta V = e/2C = 0.67 \text{ V}$. Compared with (a), every other island is coupled to the gate in (b) i.e. 50% of island gated. Since not all of the islands within the MTJ are coupled to the gate voltage, the influence of the gate on the MTJ is reduced, leading to a wider gap of 10 V ($\pm 5 \text{ V}$) in the $I_{ds}$ vs $V_{ds, V_{gs}}$ characteristics shown in (b).
Figure 5.7: 3-D plot of simulation for all islands are fully coupled to the gate (a) and 50% islands are coupled to the gate (b).

Figure 5.8 shows a single-electron Monte Carlo simulation of a MTJ at 8 K with all 15 islands coupled to the gate (a) and 10 out of 15 islands coupled to the gate in (b) for $n_1$ to $n_{10}$ and (c) for $n_6$ to $n_{15}$. 
Figure 5.8.: 3-D plot of simulation for all islands are fully coupled to the gate (a), islands $n_1$ to $n_{10}$ are coupled to the gate (b) and $n_6$ to $n_{15}$ are coupled to the gate (c)

The parameters used in Figure 5.8 are:

\[ n = 15, \quad C = C_g = 0.12 \text{ aF}, \quad R_n = \begin{cases} 200 \text{ k}\Omega & \text{if } n \text{ is odd} \\ 20 \text{ M}\Omega & \text{if } n \text{ is even} \end{cases} \]

Even though the number of islands increases from 10 (Figure 5.7 (a)) to 15 (Figure 5.8 (a)), as long as they are all coupled to the gate, the Coulomb gap remains unchanged as $\Delta V = e/2C = 0.67 \text{ V}$. However, 5 out of 15 islands are not gated in (b) and (c), this corresponds to a 5 V Coulomb gap in Figure 5.8 (b) and (c) respectively. Additionally, 50% non-gated islands also corresponds to a 10 V gap width in $I_{ds}$ vs $V_{ds}$, $V_{gs}$ characteristics in Figure 5.7 (b).

Given that the Coulomb gap in Figure 4.1 is $\sim 9 \text{ V}$, we estimate that slightly over half of islands within the MTJ are not coupled to the gate.
A simulation using the same parameters used in Figure 5.8 is shown in the Figure 5.9, where only 5 islands coupled to the gate, \( n_1 \) to \( n_5 \) (a), \( n_6 \) to \( n_{10} \) (b) and \( n_{11} \) to \( n_{15} \) (c). The corresponding Coulomb gap in each case is \( \Delta V = 15 \) V with 10 out of 15 islands within the MTJ not coupled to the gate. However, the Coulomb oscillation in Figure 5.9 (a) appears to be the strongest when the first five islands are coupled to the gate. This is because when a voltage is applied to source/drain electrode, the voltage \( V_{ds} \) drops more across the first junction which is the closest to the voltage source, due to the presence of the stray capacitance at the first island [86]. The Coulomb gap is not determined by the way that the islands are coupled to the gate by the gate capacitance, but affected by the number of islands that are coupled.

Figure 5.9.: 3-D plot of simulation for 5 out of 15 islands coupled to the gate. \( n_1 \) to \( n_5 \) in (a) \( n_6 \) to \( n_{10} \) in (b) and \( n_{11} \) to \( n_{15} \) in (c)

Figure 5.10 shows that the Coulomb gap width is also a function of the number of islands coupled to the gate by gate capacitance. The curves are offset by 10 nA for clarity. The simulation used the same parameters as in Figure 5.8. The widest gap is obtained when none of the islands is affected to gate voltage source. It is then followed by the middle one island i.e \( n_8 \), middle five islands \( (n_6 \) to \( n_{10} \) and middle seven islands \( (n_5 \) to \( n_{11} \) coupled to the gate. To avoid the influence caused by the stray capacitance at the first junction [86], \( n_6 \) to \( n_{15} \) is then simulated. Finally, the top curve is the core of all islands fully coupled to the gate.
These wide gap widths are in good agreement with the gap width in Figure 4.1, and the estimation made that over 50% islands may not be coupled by the gate capacitance. This implies that the 1 μm NW SET device may contain 15 to 20 islands, where over 8 or 10 islands are not coupled to the gate.

### 5.3. Single-electron Monte Carlo simulation of 1 μm NW SET device

A circuit diagram shown in Figure 5.11, is used to explain qualitatively the electrical characteristics of Figure 4.1 (1 μm NW SET device). This simulation uses an MTJ formed by an array of tunnel capacitors $C_n$, with ‘islands’ regions coupled by gate capacitance $C_g$ to the gate voltage. The tunnel resistances may be varied to create a Coulomb staircase rather than a linear increase in current outside the Coulomb gap.
Figure 5.11.: (Circuit diagram of a 1 µm NW SET device, with \( n = 20 \) and with only the central 11 islands gated.

Here, the values of tunnel resistances and capacitances are given as follows:

\[
R_n = \begin{cases} 
1.5 \ \Omega & \text{if } n \text{ is odd} \\
15 \ \text{M}\Omega & \text{if } n \text{ is even}
\end{cases}
\]

\((C_n, C_g) = (0.2 \ \text{aF}, 0.042 \ \text{aF})\).

The tunnel resistances were varied alternatively to ensure a strong variation in the steps of Coulomb staircase as observed. The values of tunnel resistance were also estimated from the observed current in the electrical characteristics in Section 4.1. Since the maximum width of Coulomb gap observed in Figure 4.2 (a) is \( \sim \pm 8.4 \ \text{V} \), and the edge of Coulomb gap is a function of the tunnel capacitance \([13]\), the value \( C \) can be obtained by:

\[
V_{\text{threshold}} = \frac{ne}{2C_T} = 8.4 \ \text{V}.
\]

where \( n \) is the number of tunnel junctions within the NW. The number of islands \( n \) in the simulation was increased to 20 to obtain a Coulomb gap of \( \pm 3 \ \text{V} \) to \( \pm 5 \ \text{V} \). \( C_T \) is the total capacitance, and \( C_T = \sqrt{C_0^2 + 4CC_0} \) for MTJ system if the gate capacitance is negligible small. While the Coulomb gap cannot be reduced to zero in Figure 4.1, triangular regions corresponding to half-Coulomb diamonds are observed along the edges of the central Coulomb blockade region. This implies an effective single-electron (SE) gate capacitance \( C_g \approx e/\Delta V_{gs} = 0.043 \ \text{aF} \). A constant value of \( C_g = 0.043 \ \text{aF} \) is used for Monte Carlo simulation. The very small value of \( C_g \) is due to the wide NW-gate spacing in this device. This leads to a \( C_n = C = 0.2 \ \text{aF} \), corresponding to a total island capacitance \( C_T = \sqrt{C_0^2 + 4CC_0} \approx 0.2 \ \text{aF} \), leading to a charging energy:
\[ EC = \frac{e^2}{2CT} = 0.4 \text{ eV}. \]

This charging energy is in agreement with the activation energy \( E_a = 0.3 \text{ eV} \), extracted from the Arrhenius plot of Figure 4.5 (a).

The results of this simulation are shown in Figure 5.12 with the number of islands set to \( n = 20 \). The central 11 islands are coupled capacitively to the gate, as shown in Figure 5.11. This is also in good agreement with the estimation made in the end of Section 5.2. The simulation shows a wide Coulomb gap, modulated along the edges, and oscillations in \( I_{ds} \) as \( V_{ds} \) is varied, in a manner similar to the experimental characteristics of Figure 4.1. As a metallic island is assumed, we do not have the large modulation of \( I_{ds} \) outside the Coulomb gap observed in the experimental results of Figure 4.1.

![Figure 5.12.: Simulated \( I_{ds} \) vs. \( V_{ds}, V_{gs} \) characteristics at 8 K, for the circuit of Figure 5.11 (a) with \( n = 20 \). \( C_{gm} \) is applied only for \( n = 5 \) to \( n = 15 \).](image)

5.4. Single-electron Monte Carlo simulation of point-gate SET device

The single-electron behaviour of the point-gate device characteristics (Figure 4.8) is now modelled, while not considering the quantum confinement (lines 3 - 9). The circuit uses only three QDs with varying configurations of gate capacitance, see Figure 5.13. Simu-
lations were calculated with $C_{g1} \ (0 < V_{gs} < 1.5 \text{ V})$. The experimental characteristics of Figure 4.9 have been used to extract values for $C_1$ - $C_4$, $R_1$ - $R_4$ and $C_{g1}$ - $C_{g2}$. Here, $C_1$ - $C_4$ can be extracted from Figure 4.7, using the Coulomb diamonds in the region $0 < V_{gs} < 1.5 \text{ V}$, and Coulomb gap width in the region $V_{gs} > 1.5 \text{ V}$. As a strong Coulomb staircase is observed, unequal tunnel resistances are necessary. We use $R_1 = 200R_2$ and $R_2 = R_3 = R_4$. $C_{g1} = e/\Delta V_{g1}$ and $C_{g2} = e/\Delta V_{g2}$ can be determined from the period of the Coulomb diamonds in Figure 4.9, $\Delta V_{g1} = 1.2 \text{ V}$, and for the spacing between lines 3 - 6, $\Delta V_{g2} = 2 \text{ V}$, respectively.

![Circuit diagram with three quantum dots](image)

Using $C_1 = C_3 = C_4 = 0.2 \text{ aF}$, $C_2 = 2 \text{ aF}$, $R_1 = R_2 = R_3 = 0.8 \text{ G}\Omega$, $R_4 = 16 \text{ G}\Omega$, $C_{g1} = 0.13 \text{ aF}$, $C_{g2} = 0.08 \text{ aF}$, the Coulomb staircase plot shown in Figure 5.14 (a) and the contour plot shown in Figure 5.14 (b) were obtained. For $0 < V_{gs} < 1.5 \text{ V}$, both $C_{g1}$ and $C_{g2}$ are used. As the simulation does not include quantum confinement effects, Figure 5.14 does not show the lines 3 - 9, which have been observed experimentally in Figure 4.9.

The plot of Figure 4.8 (b) is shown in Figure 5.14 (c) with the addition of the black dotted lines to enable a comparison with the simulation result of Figure 5.14 (b). Furthermore, features corresponding to charge stability regions outside the central Coulomb blockade.
region, e.g. the region shown by the white dotted lines in Figure 5.14 (b) are also seen in Figure 5.14 (c).

Figure 5.14.: Simulated $I_{ds}$ vs. $V_{ds}$, $V_{gs}$ characteristics at 8 K, for the circuit of Figure 5.13 (b), excluding quantum confinement, (a) three dimensional plot and (b) contour plot. (c) Experimental Coulomb diamond of $g_{ds}$ vs. $V_{ds}$, $V_{gs}$ from Figure 4.8 (b)

$C_3$, $C_4$ and $C_{g2}$ in Figure 5.13 may be used to extract the charging energy of QD2, and hence estimate the energy level separation $\Delta E$ in QD2. Using total capacitances in QD2 of $C_{T2} = C_3 + C_4 + C_{g2} = 0.48 \text{ aF}$, the charging energy is found to be $E_{C2} = \frac{e^2}{2C_{T2}} = 0.16 \text{ eV}$. The ratio of the line separation is given below:

$$\frac{L_4 - L_3}{L_6 - L_3} = \frac{\Delta E_1}{E_{C2}}$$
The energy level separation is $\beta - \alpha = \Delta E_1 = 21$ meV. Similarly, the second energy level separation is $\gamma - \beta = \Delta E_2 = 31$ meV. These values may be used to estimate the width $W$ of QD2. A simple particle in a box approach, with energy levels given by:

$$E_n = \frac{n^2 \hbar^2}{8mW^2}$$

gives $W \approx 4.23$ nm, which fits very well with the estimated width of the Si core (5 nm) in the NWs.

5.5. Summary

This chapter has been studied the single-electron effect vs. SET, MTJ parameters in Monte Carlo simulation by using the software CAMSET, developed by Cambridge Hitachi Laboratory. Subsequently, the QD behaviour and single-electron effects observed in these SET devices have been simulated to further explain the electrical and physical characteristics results presented in this work.
6. Conclusions and Further Work

The chapter provides a brief discussion of the significance of the work described in this thesis, a summary of the thesis, and a discussion of further possible work.

We first consider our results with regards to the scaling of ‘classical’ SiNW FETs. The results show that single-electron effects associated with a MTJ can occur even where the NW diameter in relatively large (the Si core is \(~20\) nm wide in these devices). Single-electron effects can occur even in comparatively smooth, un-patterned NWs. While strong room temperature single-electron charging effects have been observed in MTJs formed by patterned NWs, the results also show that these effects can persist at room temperature even in uniform NWs. Here, the single-electron charging energy \(E_C = \frac{e^2}{2C_T} = 0.5\) eV for point-gate SET device, and 0.2 eV for 1 \(\mu\)m NW SET device respectively. Both \(E_C \gg k_BT = 26\) meV at room temperature. Reduction of the NW width would reduce the size of these QDs and further increase their influence on device properties. QDs in sections of the NW, which are not coupled to the gate, create a threshold voltage in the \(I_{ds}\) vs. \(V_{ds}\) curves. Furthermore, the gate and drain voltages needed to switch the drain on/off are < 0.5 V, implying that supply voltage scaling to this range is possible. It is significant that as the NW length is scaled, single-electron and quantum confinement effects become much clearer, e.g. the characteristics of the 1 \(\mu\)m NW device of Figure 4.1 may be compared to the point-gate device of Figure 4.6. Features such as the Coulomb staircase and quantised levels are much clearer in the scaled device. This demonstrates that the influence of quantum confinement effects on the electrical characteristics is increasingly significant not only as the NW width deceases, but also as the length in a SiNW FET is scaled to below \(~50\) nm.
6.1. Summary of Work

To summarise the thesis, a brief introduction to the history of single-electron effects has been provided in Chapter 1. This comprises a short discussion of the background literature, the development of single-electron transistors from metallic material to Si SOI material (SIMOX or Bonded) with patterned/unpatterned island, the development of single-electron transistors in crystallines Si and nanocrystallines Si materials, and recent developments of SETs operating at room temperature, including in FinFETs and QD SETs. A pattern-dependent oxidation (PADOX) approach for the further reduction of island dimensions has been discussed. Detailed references to previous work have been provided at relevant points.

In Chapter 2, the theoretical model of double tunnel junction (DTJ) SET has been used to explain the single-electron effects, from the circuit diagram for the double tunnel junction SET. This includes charge vs. electrostatic energy changes $\Delta E$, tunnelling rates as a function of $\Delta E$, the probability of the island in the electron number state $n$, $I-V$ curves calculation, Coulomb diamonds and the Coulomb staircase. The corresponding equations and inequalities were also derived to help explain the analytical model. The behaviour of quantum dots (QDs) behaviour, especially the Coulomb oscillation in the current $I_{ds}$ as a function of gate voltage $V_{gs}$, has been discussed. Finally, the multiple tunnel junction (MTJ) system has been considered, including the total effective capacitance and the more complex electrical characteristics of the MTJ.

In Chapter 3, the electron-beam lithography (EBL) has been studied in detail, based on the Xenos pattern generator system. Here, the beam formation, system interface, electron-beam resist, sample preparation, e-beam exposure and resist development have been discussed. In particular, the relationship between the EBL parameters and EBL results has been given in the Table 3.1. Furthermore, following experiments for beam optimisation, the best parameters for lithography were provided in Table 3.2. A detailed fabrication process flow is provided in Appendix A. The spin-on-doping (SOD) and thermal oxidation results have also been discussed in Chapter 3. Here, the oxidation thickness determines the dimensions of the device Si core and directly impacts on the electrical and simulation results in Chapter 4 and 5.
An investigation and characterisation of the electrical results of scaled SiNWs in the SE/quantum confinement limit has been described in Chapter 4. Room temperature SET operation was observed in ∼50 nm long NWs where the un-oxidised Si core was only ∼5 nm. NWs with width ∼30 nm and length 1 µm to 50 nm, had in-plane parallel or point-gates. It was found that in the 1 µm long, uniform NWs, strong SE effects occurred up to ∼220 K, and traces of these effects persisted to ∼300 K. This was associated with the formation of a ‘natural’ 20-QD MTJ along the NW. The maximum island charging energy $E_C = 0.2$ eV, was found to be in good agreement with the activation energy 0.276 eV extracted from Arrhenius plots. Scaling the NW gated length to ∼50 nm using a point-gate device reduced the number of QDs along the NW to only two and both SE and quantum confinement effects were observed in the electrical characteristics. Comparison between the 1 µm NW and the point-contact two-QD device showed that as the NW length was scaled, quantum effects dominated the electrical characteristics. We then went-on to show how 16 transistors could be arranged as a $4 \times 4$ array and give examples of the single-electron characteristics measured from individual transistors. These results illustrate the significance of quantum effects towards the limits of CMOS at the sub-10 nm scale, and the potential of short SiNWs for a quantum-effect ‘beyond CMOS’ technology.

In Chapter 5, the single-electron effect vs. SET, MTJ parameters in Monte Carlo simulation has been studied by using the software CAMSET, developed by Cambridge Hitachi Laboratory. Subsequently, the QD behaviour and single-electron effects observed in our SET devices have been simulated to further explain the electrical and fabrication results. Finally, conclusion, a summary of the thesis and a discussion of further work are provided in the present chapter (Chapter 6).

### 6.2. Future Work

Recognising that the research leading to these results has received funding from the European Union’s Seventh Framework Programme FP7/2007-2013 under grant agreement no. 318804 (SNM), one of the key objective of the SNM project is to develop technologies that are transferable and manufacturable. Work with project partners has already started to explore the fabrication of SET devices using alternative lithography techniques such as
scanning probe lithography (SPL). These collaborations will be actively developed during the next stage of this project, in the following year. Their status is reviewed here, not only for completeness, but also because it demonstrates the importance of this work and the project is appreciated.

i. Initial work has been undertaken in collaboration with the Techische Universität Ilmenau (TUIL). Here, the fabrication process flow that has been developed in Chapter 3 for the $4 \times 4$ device array has been modified to allow SPL. Very thin SOI layers will be used to reduce device dimensions. An Al metal mask determining the contact regions, navigation and alignment features will be defined at Imperial and etched at TUIL. A combination of EBL and SPL will be used to define SETs with Si channels $\sim 10$ nm in scale.

ii. Collaborative work has started which involves both IBM Zürich and the company Swiss Litho, with the overall objective being to fabricate a $4 \times 4$ SET array. Swiss Litho’s ‘NanoFrazor’ thermal scanning probe lithography system (www.swisslitho.com) will be used for the high-resolution structures. The substrates will be returned to Imperial for dicing, probing and measurement.

Our SET devices based on NW, defined in SOI material by using EBL and trench isolation, followed by thermal oxidation to further reduce the Si core to $\sim 5$ nm, have been fabricated and operated up to room temperature. It is proposed that the devices can be used as the basis of a RT integrated circuit SET system, e.g. single-electron memory and logic system [13].

Although fabrication of nanoscale devices, using EBL as a high resolution lithographic technique for nanoscale SET fabrication, can fabricate the SET $10$ nm to $5$ nm in size, a practical technology requires investigation of the reliability and yield of this process. Further work requires larger number of devices to be fabricated. Alternatively, SPL and nano-imprint lithography (NIL) approaches can be used for ‘beyond CMOS’ devices fabrication, which provide means to directly write lines defining NW at $\sim 10$ nm scale. A schematic layout of an SPL approach is shown in Figure 6.1, based on a development-less, positive-tone closed loop [134] exposure of calixarene-based molecular glass resists. Here, the same nanoprobe is used for both direct writing of features using spatially confined
low-energy electron emission from nano-tip, and AFM-imaging for pre- and post-imaging as well as for pattern overlay alignment. In addition, self-actuating and piezoresistive scanning probes can be applied, expanding the lithographic throughput capabilities by enabling cantilever array technology application for nanolithography [14,115].

![Lithography diagram](image)

Figure 6.1.: Schematic layout of the lithography system using a development-less, positive-tone closed loop [134] Scanning Probe Lithography (SPL) on calixarene-based molecular glass resists.

Finally, this work has led to the following publications:

**Journal Articles**    Chen Wang, Mervyn E. Jones, Zahid A. K. Durrani, “Single-electron and quantum confinement limits in length-scaled silicon nanowires”, submitted to the *Nanotechnology*

**Conference Papers**


3. Chen Wang, Mervyn Jones, Zahid Durrani, “Nanowire single-electron devices defined
A. Appendix

A.1. Fabrication process flow with a combination of electron-beam lithography and optical lithography

1. Sample

(100) oriented 8-inch diameter SOI wafer, p-type doped ($\sim 10^{15}$ cm$^{-3}$), $\sim 120$ nm top Si layer, and a $\sim 130$ nm buried oxide layer, undoped substrate with thickness of 500 $\pm$ 25 $\mu$m. Cleaved into $\sim 1$ cm$^2$ chips.

2. Sample clean

RCA/Piranha cleaning followed by an oxygen plasma clean (flow rate: $\text{O}_2$ - 100 sccm, Ar - 10 sccm, pressure 100 mTorr and power 200 W).

3. Top layer thinning

Oxidise the chips at 1100°C for 2 hours in oxygen, with a ramp time of 1 hour and natural cooling to room temperature, followed by an buffered HF (BHF, HF concentration 1%) dip for 5 min.

4. Spin-on doping

- Prebake
  
  Bake at 150°C in an oven for 30 min.

- Dopant spin-coating
  
  Spin the chip with the dopant (Phosphorous) at a speed of 500 rpm for 10 sec and then 2500 rpm with an accelerating rate of 500 for 50 sec ($\sim 3.5$ $\mu$m film thickness expected).
• Postbake

Bake the sample at 200°C on a hot plate for 30 min.

5. Fine feature patterning

• Sample Cleaning

Rinse a 1 cm × 1 cm chip with acetone and subsequently IPA. Oxygen plasma clean in a planar plasma (flow rate: O₂ - 100 sccm, Ar - 10 sccm and pressure 100 mTorr power 200 W).

• Prebake

Bake at 150°C in an oven for 30 min.

• Resist spin-coating

Spin the the e-beam resist, PMMA, on top of the chip at a speed of 500 rpm for 10 sec and then 5000 rpm with an accelerating rate of 500 for 50 sec (∼100 nm film thickness expected).

• Postbake

Bake the sample at 170°C on a hot plate for 1 hour

• Defined the SET patterns by using EBL

6. Development

Immerse the sample for 3 min in a liquid developer (MIBK : IPA = 1 : 3).

7. Metal deposition:

Deposit Al (30 nm thick) at a chamber pressure < 2.2 ×10⁻⁶ mbar. Subsequently, immerse the sample in acetone overnight.

8. Coarse feature patterning

• Photoresist spin-coating

Spin the resist S1828 on top of the chip at 500 rpm for 10 s, and then at 4500 rpm with an accelerating rate of 1000 for 40 s (∼3.5 µm film thickness expected).
• Photoresist baking

Bake the resist S1828 on a hot plate at 65 °C, 85 °C and finally 115 °C for 1 min each.

• Optical alignment by using photolithography

Pattern the photoresist with a fixed exposed energy (5.3 mW/cm² × 160 s).

• Development

Immerse the sample in a liquid developer (MF319) for 4 min.

• Plasma descum

Descum the sample by an oxygen plasma clean for 3 minute (flow rate: O₂ - 800 sccm, Ar - 5 sccm, pressure 100 mTorr and power 100 W).

9. Pattern transfer and thermal oxidation

• Metal deposition and lift-off

Deposit Al (100 nm thick) at a chamber pressure < 2.2 ×10⁻⁶ mbar. Subsequently, immerse the sample in acetone overnight.

• RIE:

Etch the Si in SF₆/oxygen plasma for 1 minute (flow rate: O₂ - 100 sccm, Ar - 10 sccm, pressure 100 mTorr and power 200 W, 200 nm etching depth expected).

• Wet etching:

Wet etch the metal hard mask by using the Al etchant used (1 - 5% HNO₃, 65 - 75% H₃PO₄, 5 - 10% CH₃COOH and H₂O for dilution).

• Thermal oxidation

Oxidise the sample at 1000°C for 30 minutes followed by a natural cool down process.

10. Ohmic contact bond pads and wire bonding

• Photoresist spin-coating
Spin the resist S1828 on top of the sample at 500 rpm for 10 s, and then at 4500 rpm with an accelerating rate of 1000 for 40 s (~3.5 µm film thickness expected).

- Photoresist baking
  Bake the resist S1828 on a hot plate at 65 °C, 85 °C and finally 115 °C for 1 min each.

- Optical alignment by using photolithography
  Pattern the photoresist with a fixed exposed energy (5.3 mW/cm² × 160 s).

- Development
  Immerse the sample in a liquid developer (MF319) for 4 min

- Plasma descum
  Descum the sample by an oxygen plasma clean for 3 minute (flow rate: O₂ - 800 sccm, Ar - 5 sccm, pressure 100 mTorr and power 100 W).

- HF dip
  An BHF dip for 1 min.

- Metal deposition and lift-off
  Deposit Cr (20 nm thick) and Al (200 nm thick) at a chamber pressure < 1 ×10⁻⁶ mbar. Subsequently, immerse the sample in acetone overnight.

- Wire bonding
References


