Integrated Electronics for Targeted Intraspinal Microstimulation

Song Luan

November 12, 2014

Supervised by Dr Timothy G. Constandinou

Submitted in partial fulfilment of the requirements for the degree of Doctor of Philosophy in Electrical and Electronic Engineering of Imperial College London and the Diploma of Imperial College London
Declaration of Originality

I hereby certify that all material in this dissertation which is not my own work has been properly acknowledged.

Song Luan
Copyright Declaration

The copyright of this thesis rests with the author and is made available under a Creative Commons Attribution Non-Commercial No Derivatives licence. Researchers are free to copy, distribute or transmit the thesis on the condition that they attribute it, that they do not use it for commercial purposes and that they do not alter, transform or build upon it. For any reuse or redistribution, researchers must make clear to others the licence terms of this work.

Song Luan
Acknowledgements

I would like to express my deepest gratitude to my supervisor Dr. Timothy G. Constantinou for offering me such an opportunity to pursue a PhD. His patient guidance has always saved me when I was overwhelmed by a problem. For four years, he has taught me not only how to undertake research, but also how to be (a) helpful (person) within the group. His sharp and insightful thought, patience and diligent personality had set a model for my future. It has been my honour to become your student since my master study.

I also wish to give special thanks to Amir, Virginia and Konstatin for teaching me the basics of electrophysiology and for helping with the experiments. To Yan, I would like to express my gratitude for guiding me through my first tape out even when he was busy finishing his PhD and for his continuous support for all these years on both academic and life in the UK. To Olive, I give thanks for her encouragement and guidance on my interest in RF design. It was a pleasure knowing her.

I thank my colleague and friend Ian who had finished writing up two weeks before me for sharing the stress throughout my PhD and for all the useful discussions. Furthermore, I am grateful for the language support he gave for every article I wrote. He is a kind person and I wish him all the best. I want to also thank my other friends working in the neural field, Sivylla, Onur, Deren, Lieuwe, Satoshi, for enlightening me with their knowledge everyday.

A very special thanks to Dora for proofreading my thesis. She is such a patient reader and surely will have a brilliant future!

To all the other people in this centre and in EEE, Pantelis, Melina, Yuanqi, Alex, Onur, Mohammadreza, Peter, Mohamed, Reza, Bassen, Paul, Emris, Tatiana, Themis, Iza, Wiesia, Gifty, Huan, Yufei, Jianxiong, Chuan, Chen and many other people whose name cannot be listed here as limited by the page size, I sincerely thank for all the support and encouragement they have provided. It would be a completely different world if I do not see their smiley face everyday. I am so lucky to be able to join such a group(family) full of love.

Special thanks to my friends, Shan, Chun, Kai, Yang, for giving me emotional support, sending me papers that are not subscribed by Imperial and tips on all sorts of academic questions outside of my field.

The final thanks go to my parents who never stopped loving me. I do not know how to express my gratitude even in Chinese, since no words would do it justice. I do not know how to pay back them since my love can never match theirs. Also to my wife who brings joy to my life and a lovely daughter. They are the biggest loves of my life and this thesis is dedicated to them.
Abstract

Intraspinal microstimulation (ISMS) is an emerging method that is applied to neuroprosthetic aims at individuals with spinal cord injury. Compared to traditional spinal stimulation or peripheral nerve stimulation methods, ISMS can activate muscle groups in organised synergies and thus can provide finer control of the generated force with reduced muscle fatigue.

As the spinal cord is the neural link between the central and peripheral nervous systems, it is convenient to use this in accessing neurons associated with limb movement within a small area. For example, the relevant length of the spinal cord controlling the lower limbs in humans is only 5 cm. However, this means that any implant surgery is limited to some extent, on the other hand, this means ISMS needs to use invasive electric neural stimulation (ENS) with microelectrodes to access the target motor neurons to achieve a higher spatial resolution. Similar to other implantable ENS systems, an ISMS system needs to be compact, safe and energy efficient (in addition to effectively provide the required therapy).

Although existing implantable neural stimulators fulfil these basic requirements, there is still much room for improvement. Depending on whether the stimulus is current or voltage controlled, the stimulator can be good for either safety and controllability or energy efficiency. Since the trend in the semiconductor industry is to reduce power consumption in integrated circuits, a current controlled stimulator is usually preferable by experimental neuroscientists. However, there is a new trend to combine these two control modalities, to enjoy the benefits of both.

Following this trend, this thesis starts by focusing on a third modality – charge controlled stimulation, which delivers the stimulus in charge packets. This eliminates the voltage headroom required for relatively high output resistances in current controlled stimulators whilst preserving the controllability over the total charge delivered. Charge controlled stimulation is thus proposed for having the potential to be as energy efficient as voltage controlled stimulation and as safe as current controlled stimulator. A novel circuit for charge mode stimulation is described based on a charge metering approach that has been adopted from nuclear engineering. Experimental results demonstrate the feasibility of this approach and also identify the key challenges.

This is then extended to a novel reconfigurable, multi-modal and multichannel stimulator circuit. This is the first integrated system to implement current, voltage and charge control stimulation within a reconfigurable channel architecture. This has been developed to investigate the effect of dynamic multipolar electrode reconfiguration with the aim of focusing or steering the stimulus. To this end, different stimulus delivery methods can be tested for multipolar spatial control.

The concept of multipolar stimulation is then investigated from a theoretical standpoint.
The ability to apply this in improving the spatial resolution in ISMS can be achieved by confining the stimulus spread (thus reducing destructive crosstalk). This method can also be used to shift the stimulus voltage field away from the delivering electrode so as to correct implant placement error during surgery. A theoretical computational model is developed to investigate the effect of dynamic multipolar electrode reconfiguration with the aim of focusing or steering the stimulus. It is intended, together with the developed multichannel stimulator, that this will be used in future to develop advanced multipolar strategies that can achieve spatial hyperacuity for ISMS, and more generally in ENS.
To my beloved family
# Contents

List of Abbreviations ........................................... 18

1. Introduction .................................................. 20
   1.1. Electrical Neural Stimulation .......................... 21
   1.2. Motivation ............................................... 22
   1.3. Research Aims ......................................... 24
   1.4. Outline of this Thesis .................................. 24

2. Intraspinal Microstimulation: Background and State-of-the-Art 28
   2.1. Introduction .............................................. 28
   2.2. Background on Physiology .............................. 28
      2.2.1. Organisation of spinal cord ...................... 28
      2.2.2. Motor neuron-muscle relationships ............... 29
      2.2.3. Biophysics of action potential generation ...... 32
   2.3. State-of-the-art Electrical Neural Stimulation .......... 33
      2.3.1. Stimulation electrodes ............................. 34
      2.3.2. Types and configurations .......................... 37
      2.3.3. Safety .............................................. 39
      2.3.4. Power consumption .................................. 43
      2.3.5. Size and programmability ......................... 43
      2.3.6. Targeted stimulation ................................ 44
   2.4. Current State of Intraspinal Microstimulation ......... 44
   2.5. Conclusions ............................................. 45

3. A New Method for Safe Electrical Neural Stimulation: Charge-metering 55
   3.1. Introduction ............................................. 55
   3.2. Principle and System Architecture ..................... 55
      3.2.1. Method of charge-metering ....................... 56
      3.2.2. Stimulus generation ................................ 56
      3.2.3. Circuitry ........................................... 58
      3.2.4. Evaluation methods ................................. 60
      3.2.5. Effects of electromagnetic interference, noise and drift 62
   3.3. Testing Results and Discussion ......................... 63
      3.3.1. Charge metering & balancing ...................... 63
      3.3.2. Ex-vivo test ...................................... 71
      3.3.3. Temporal control ................................... 71
<table>
<thead>
<tr>
<th>Section</th>
<th>Title</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3.4.</td>
<td>Power efficiency</td>
<td>73</td>
</tr>
<tr>
<td>3.3.5.</td>
<td>Procedure of calibration</td>
<td>74</td>
</tr>
<tr>
<td>3.4.</td>
<td>Conclusion and Future Work</td>
<td>74</td>
</tr>
<tr>
<td>4.</td>
<td>Multichannel Programmable Electrical Neural Stimulation Platform</td>
<td>78</td>
</tr>
<tr>
<td>4.1.</td>
<td>Introduction</td>
<td>78</td>
</tr>
<tr>
<td>4.2.</td>
<td>System Architecture</td>
<td>79</td>
</tr>
<tr>
<td>4.3.</td>
<td>Implementation</td>
<td>79</td>
</tr>
<tr>
<td>4.3.1.</td>
<td>Voltage and current stimulation</td>
<td>79</td>
</tr>
<tr>
<td>4.3.2.</td>
<td>Charge stimulation</td>
<td>82</td>
</tr>
<tr>
<td>4.3.3.</td>
<td>Calibration</td>
<td>83</td>
</tr>
<tr>
<td>4.3.4.</td>
<td>Charge imbalance monitor</td>
<td>85</td>
</tr>
<tr>
<td>4.3.5.</td>
<td>Digital control logic</td>
<td>85</td>
</tr>
<tr>
<td>4.3.6.</td>
<td>Top level support circuitry</td>
<td>86</td>
</tr>
<tr>
<td>4.4.</td>
<td>Test Results and Discussion</td>
<td>87</td>
</tr>
<tr>
<td>4.4.1.</td>
<td>Current mode stimulation</td>
<td>89</td>
</tr>
<tr>
<td>4.4.2.</td>
<td>Voltage mode stimulation</td>
<td>91</td>
</tr>
<tr>
<td>4.4.3.</td>
<td>Charge mode stimulation</td>
<td>91</td>
</tr>
<tr>
<td>4.4.4.</td>
<td>Charge imbalance monitor and active charge balancing</td>
<td>98</td>
</tr>
<tr>
<td>4.4.5.</td>
<td>Multi-channel stimulation capability</td>
<td>100</td>
</tr>
<tr>
<td>4.5.</td>
<td>Conclusion and Multi-channel stimulation capability</td>
<td>100</td>
</tr>
<tr>
<td>5.</td>
<td>Concept of Field Shaping for Improving Stimulation Focality</td>
<td>105</td>
</tr>
<tr>
<td>5.1.</td>
<td>Introduction</td>
<td>105</td>
</tr>
<tr>
<td>5.2.</td>
<td>Aims</td>
<td>105</td>
</tr>
<tr>
<td>5.3.</td>
<td>Methods</td>
<td>105</td>
</tr>
<tr>
<td>5.3.1.</td>
<td>Model of spinal cord</td>
<td>105</td>
</tr>
<tr>
<td>5.3.2.</td>
<td>Model of multi electrode array</td>
<td>106</td>
</tr>
<tr>
<td>5.3.3.</td>
<td>Stimulation protocols</td>
<td>106</td>
</tr>
<tr>
<td>5.4.</td>
<td>Results and Discussions</td>
<td>107</td>
</tr>
<tr>
<td>5.4.1.</td>
<td>Comparison between different stimulation modalities</td>
<td>107</td>
</tr>
<tr>
<td>5.4.2.</td>
<td>Influence of the distance to the electrodes</td>
<td>111</td>
</tr>
<tr>
<td>5.4.3.</td>
<td>Influence of the number of active electrodes</td>
<td>116</td>
</tr>
<tr>
<td>5.4.4.</td>
<td>Influence of electrode array grid spacing</td>
<td>121</td>
</tr>
<tr>
<td>5.4.5.</td>
<td>Influence of the stimulation amplitude</td>
<td>126</td>
</tr>
<tr>
<td>5.5.</td>
<td>Conclusion and Future Work</td>
<td>127</td>
</tr>
<tr>
<td>6.</td>
<td>Conclusion</td>
<td>130</td>
</tr>
<tr>
<td>6.1.</td>
<td>Original Contributions</td>
<td>130</td>
</tr>
<tr>
<td>6.2.</td>
<td>Recommendations for Future Work</td>
<td>131</td>
</tr>
<tr>
<td>6.3.</td>
<td>Concluding Remarks</td>
<td>132</td>
</tr>
<tr>
<td>A.</td>
<td>Appendices</td>
<td>133</td>
</tr>
<tr>
<td>A.1.</td>
<td>Neural signal recording system used in <em>ex-vivo</em> testing</td>
<td>133</td>
</tr>
</tbody>
</table>
A.2. Verilog Code Listing for Multichannel Stimulator ................. 134
A.3. State Diagram for Multichannel Stimulator .................. 173
A.4. Differential Nonlinearity of Current Mode Stimulation on Multichannel Stimulator System ............................................. 175
A.5. Integral Nonlinearity of Current Mode Stimulation on Multichannel Stimulator System .................................................. 179
A.6. Differential Nonlinearity of Voltage Mode Stimulation on Multichannel Stimulator System during Negative Output Phase ............... 183
A.7. Integral Nonlinearity of Voltage Mode Stimulation on Multichannel Stimulator System during Negative Output Phase ................ 187
A.8. Publications .......................................................... 191
## List of Tables

2.1. Charge-injection limits of electrode materials for stimulation. .................. 35
2.2. Main commercially available multielectrode arrays (MEAs) for *in-vivo* neural applications. Pictures are reproduced from the company websites. ........... 36
2.3. Qualitative comparison between three different ENS modalities ............... 39
2.4. Performance comparison .......................................................... 47
3.1. Evaluation matrix for each type of test. ..................................... 60
3.2. Simulated delivered and residual charges for different target charge stimulus. $V_{\text{ref}} = 920 \text{ mV}$ ................................................... 65
3.3. Performance comparison with existing work assuming 1 ms stimulation period. 74
4.1. Command list for controlling each channel ................................... 87
4.2. Summaries of tests performed on packaged integrated circuit (IC) samples . 89
4.3. Integral nonlinearity (INL) of current sourcing across all 4 output ranges . 90
4.4. INL of current sinking across all 4 output ranges .......................... 90
4.5. INL of voltage stimulation during negative phase ........................... 91
4.6. Average and maximum charge delivery error with corresponding target charge measured on channel 8 across chips 1,2,4,6,7,8,9,10 without calibration ... 92
4.7. Average and maximum charge delivery error with corresponding target charge measured on all the channels on chip 2 without calibration .............. 93
4.8. Average and maximum charge delivery error with corresponding target charge measured on all the channels on chip 9 without calibration .............. 94
4.9. Average and maximum residue charge error with corresponding target charge measured on channel 8 across chips 1,2,4,6,7,8,9,10 without calibration ... 94
4.10. Average and maximum residue charge error with corresponding target charge measured on all the channels on chip 2 without calibration ............ 95
4.11. Average and maximum residue charge error with corresponding target charge measured on all the channels on chip 9 without calibration ............ 96
5.1. Reported dimensions of the C5 cervical segment in the spinal cord ......... 106
5.2. Conductivities of the compartments in the inhomogeneous anisotropic model 106
5.3. Different stimulation configurations ............................................ 116
List of Figures

1.1. Concept of multi-channel intraspinal microstimulation with ability to shape the voltage fields ........................................ 24

2.1. An illustration of the spinal cord showing: (on left) a detailed cross section, and (on right) a list of corresponding spinally mediated functions. Adapted from [6] ................................................................. 29

2.2. An illustration of a typical neuron cell. Showing soma, dendrite, axon, node of Ranvier, myelin sheath. ................................................................. 30

2.3. Laminae of the spinal cord. Laminae I-VI forms the dorsal horn and VII-IX the ventral horn. ................................................................. 30

2.4. Cross section of human spinal cord (lumbar region, L1) showing motor neurons located below lateral horn (see inset in (b)). Astrocytes and oligodendrocytes are labelled ‘A’ and ‘O’, respectively. White intracellular structure are labelled ‘?’ in (b). The objective magnification used is 40x. (a) and (b) use different stains method [12]. Copyright belongs to Gregor Overney. ... 31

2.5. An illustration of a motor unit adapted from [6] ......................... 32

2.6. (a) The phospholipid cell membrane, ionic charges and an ion channel. (b) 4 phases during an AP generation: (i) stimulation causing depolarisation to above threshold, (ii) Na$^+$ channels open and Na$^+$ enters cell, (iii) K$^+$ channels are open and K$^+$ leaves cell, (iv) refractory period and ion pumps restore resting potential. Note that $I_{Na}$ and $I_K$ are caused by Na$^+$ influx and K$^+$ efflux respectively ................................................................. 32

2.7. Typical electrical model for the electrode-electrolyte interface used in the ENS design ................................................................. 37

2.8. Main electrode configurations for ENS: (a) monopolar configuration, with return electrode placed at a distance from the working electrode and with a larger surface area; (b) bipolar configuration; (c) multipolar configuration . 38

2.9. The three types of ENS ................................................................. 38

2.10. Typical current mode stimulation waveform with a zero net charge, i.e. the cathodic and anodic shaded areas should be equal (and opposite) ................................. 41

3.1. System architecture of the proposed charge-metering system. ($R_S$ represent the tissue spreading resistance and $C_{dl}$ the electrode-electrolyte-tissue double layer capacitance. $V_{ref}$ for the two comparators are the same. Both $V_{ref}$ and $V_{stim}$ are provided externally.) ................................................................. 55

3.2. Positions of the 6 switches during different phases of stimulus generation. . 57
3.3. Schematic of the comparator using a regenerative load .......................... 60
3.4. Schematic of the bi-directional counter (3-bits shown) .......................... 60
3.5. Chip microphotograph showing the core circuit fabricated in AMS 0.18µm 1P4M CMOS technology ................................................................. 61
3.6. (a) Test setup for charge-metering with lumped elements; (b) Test setup for measure stimulation current with lumped elements; (c) Saline tank test setup; (d) in-vitro setup with extracted Xenopus sciatic nerve; and (e) differential probe equivalent input model from manufacture datasheet .......................... 61
3.7. Geometry of the cuff electrode used. Made by IMTEK, University of Freiburg. The surface is coated with platinum black. Reproduced from the IMTEK catalogue ................................................................. 62
3.8. Simulation results show the overshoot of the voltage on the measuring capacitor due to control loop delay and offset of the comparator. The dashed line is $V_{\text{ref}}$ while the circled part shows extra charge injected at the end of the stimulation phase ................................. 63
3.9. Charging error showing the unit charge is comprised of two components. The variable portion is decreasing due to the reason stated in Section 3.3.1 .............. 64
3.10. Monte-Carlo analysis for: (a) charge delivered, and (b) residual charge .... 66
3.11. Measured results of 7 chips with RC EEI model and $V_{\text{ref}} = 920$ mV, $V_{\text{Stimulation}} = 1.8$ V for (a) the charge delivered; (b) the residue charge after active charge recycle. 100 measurements have been taken for each chip. The target charge is 10 nC. The box shows the interquartile range; with whiskers showing the minimum and maximum; and centre line showing the medium and central square is the average ........................................ 67
3.12. Measured results of 7 chips in the saline tank with platinum electrodes with $V_{\text{ref}} = 920$ mV, $V_{\text{Stimulation}} = 1$ V for (a) the charge delivered; (b) the residue charge after active charge recycle. 100 measurements have been taken for each chip. The target charge is 10 nC. The box shows the interquartile range; with whiskers shows the minimum and maximum; and centre line showing the median and central square is the average ........................................ 69
3.13. (a),(b) Single ended voltage on the two terminals of EEI model (c) Differential Voltage across the EEI model (derived from (a) and (b)); (d) Stimulation Current derived from the differential voltage accross the resistor in the EEI model; (e) Detail of (d) ..................................................... 70
3.14. NEURON® simulation results comparing an ideal constant current monopolar stimulation with the current profile simulated using the charge-metering system. The ripple on the action potential illustrates the propagation of the action potential over time. Each trace represents the membrane voltage at a specific location on the fibre model ..................................................... 72
3.15. Comparison of response between this work with $V_{\text{stim}}$=1.8 V and a conventional direct current stimulator using 500 µA with 500 µs pulse-width and zero inter-phasic delay ..................................................... 73
4.1. Concept of envisaged multichannel stimulation system

4.2. Block diagram of multichannel programmable electrical neural stimulation platform. The blocks contain bugs in the first tapeout are highlighted in red.


4.4. Schematic for switch used in DAC. Two of this make a single-pole-double-throw switch.

4.5. Current buffer with scaling output for stimulation.

4.6. Class AB voltage buffer.

4.7. Charge delivery using the same idea developed of charge-metering.

4.8. Schematic for circuitry used for generating comparison threshold for charge mode stimulation (T1 are selected when generating threshold for negative phase; T2 for positive phase).

4.9. (a) Schematic of the calibration circuit. (b) Calibration data output and its corresponding sampled threshold voltage.

4.10. Flowchart of calibration. Cal_data[5:0] is shown as the transition condition. “Pos” means calibration for positive phase; “Neg” means calibration for negative phase.

4.11. Data format of the 21-bit input serial data. Type 1 is for commands and type 2 is for data.

4.12. Micro-photograph of the stimulator fabricated using 0.35 µm HV CMOS process.

4.13. General setup for testing the multichannel programmable electrical neural stimulation platform.

4.14. Current stimulation with minimum duration (1 µs) on each data point and full scale change on Channel 8 of chip 7.

4.15. Electrode-electrolyte interface (EEI) model used during charge mode stimulation, the differential probe is connected monopolar side to measure the current.

4.16. Charge delivery measured on channel 8 across chips 1,2,4,6,7,8,9,10, the dash line represents the ideal case (Charge delivered = Target Charge).

4.17. Charge delivery measured across 8 channels on chip number 2, the dash line represents the ideal case.

4.18. Charge delivery measured across 8 channel on chip number 9, the dash line represents the ideal case.

4.19. Residue charge measured on channel 8 across chips number 1,2,4,6,7,8,9,10.

4.20. Residue charge measured across all 8 channels on chip number 2.

4.21. Residue charge measured across all 8 channels on chip number 9.

4.22. Voltage measured directly on the IC output of Channel 5 on chip 2 which always have a shorter charge recycling phase.
4.23. Simulation results of calibration. (a) negative phase calibration (b) positive phase calibration. These are two parts of a whole calibration process. Trace (i) is the signal for charging the unit capacitor $C_1$, (ii) control signal for sampling the electrode voltage, (iii) control signal for stimulating using the charge stored on unit capacitor $C_1$, (iv) threshold voltage (v) sampled electrode voltage (vi) – (xi) cal_data[5:0].

4.24. EEI model of the platinum electrode used inside normal ringer solution during the test. $R_1$ is an external resistor. $R_2$ and $C_1$ are measured values. (All parameters are measured using FLUKE PM6303A, automatic RCL meter).

4.25. Transient voltage measured across $R_1$ during charge mode stimulation with normal ringer solution delivering 16.384 nC. Noting that the voltage is not constant during charge delivery or recovery as the charge build up on the EEI.

4.26. Comparison between charge delivery measured with RC model and in normal ringer solution on channel 3 of chip 2 and channel 5 of chip 9.

4.27. Comparison between residue charge measured with RC model and in normal ringer solution on channel 3 of chip 2 and channel 5 of chip 9.

4.28. Passive shorting phase during charge imbalancing.

4.29. Error signal generated when the voltage on the electrode exceeds water window. C3 shows the electrode voltage; C2 shows the error signal. The spike on C3 is a stimulation cycle.

4.30. Active charge recycling in operation during imbalanced current stimulation. (a) the voltage on the electrode (b) comparator output on unit capacitor $C_1$ (c) comparator output on unit capacitor $C_2$.

4.31. Current stimulation between two stimulation channels without involving the reference electrode. (a) and (b), voltages on the two opposite terminals of the EEI model. (c) the differential results of traces in (a) and (b), presenting a constant current stimulation voltage profile.

4.32. Demonstration that different channel can be programmed individually. C1 shows the channel doing charge mode stimulation while C3 and C4 show the channel doing current stimulation synchronously.

5.1. Model of the spinal cord and electrode array built in COMSOL Multiphysics®.

5.2. Electrode configuration used during simulation.

5.3. Topview of electric field and voltage potential contour on a plane at 100 µm above the electrode tips for current mode stimulation (CMS). The coloured contours are voltage potential. The black lines are geometric boundaries and electric field streamlines.

5.4. Voltage potential along the Z-direction at $X = -2800 \mu m$ in Fig. 5.3. Blue-cross corresponds (a), green-circle (b) and red-circle (c).

5.5. Top view of electric field and voltage potential contours on a plane 100 µm above the electrode tips for voltage mode stimulation (VMS). The coloured contours are voltage potentials. The black lines are geometric boundaries and electric field streamlines.
5.6. Voltage potentials along the Z-direction at $X = -2800 \mu m$ in Fig. 5.5. Blue-cross corresponds (a), green-circle (b) and red-circle (c) (110).

5.7. Top view of electric field and voltage potential contours on a plane 10 $\mu m$ above the electrode tips for CMS. The coloured contours are voltage potentials. The black lines are geometric boundaries and electric field streamlines. (112).

5.8. Voltage potentials along the Z-direction at $X = -2800 \mu m$ in Fig. 5.7. Blue-cross corresponds (a), green-circle (b) and red-circle (c) (113).

5.9. Top view of electric field and voltage potential contours on a plane 10 $\mu m$ above the electrode tips for VMS. The coloured contours are voltage potentials. The black lines are geometric boundaries and electric field streamlines. (114).

5.10. Voltage potentials along the Z-direction at $X = -2800 \mu m$ in Fig. 5.9. Blue-cross corresponds (a), green-circle (b) and red-circle (c) (115).

5.11. Top view of electric field and voltage potential contours on a plane 100 $\mu m$ above the electrode tips for VMS using 5 electrodes. The coloured contours are voltage potentials while the black lines are geometric boundaries and electric field streamlines (117).

5.12. Voltage potential along the Z-direction at $X = -2800 \mu m$ and X-direction at $Z = -800\mu m$ in Fig. 5.11. Blue-cross represents Voltage Conf 1, green-circle Voltage Conf 2, red-circle Voltage Conf 3 (118).

5.13. Top view of electric field and voltage potential contours on a plane 100 $\mu m$ above the electrode tips for CMS using 5 electrodes. The coloured contours are voltage potentials while the black lines are geometric boundaries and electric field streamlines (119).

5.14. Voltage potential along the Z-direction at $X = -2800 \mu m$ and X-direction at $Z = -800\mu m$ in Fig. 5.11. Blue-cross represents Current Conf 1, green-circle Current Conf 2, red-circle Current Conf 3 (120).

5.15. Electric field and voltage potential contours on a plane 100 $\mu m$ above the electrode tips for CMS under a spacing of 200 $\mu m$. The coloured contours are voltage potentials. The black lines are geometric boundaries and electric field streamlines (122).

5.16. Electric field and voltage potential contours on a plane 10 $\mu m$ above the electrode tips for CMS under a spacing of 200 $\mu m$. The coloured contours are voltage potentials. The black lines are geometric boundaries and electric field streamlines (123).

5.17. Electric field and voltage potential contours on a plane 100 $\mu m$ above the electrode tips for VMS under a spacing of 200 $\mu m$. The coloured contours are voltage potentials. The black lines are geometric boundaries and electric field streamlines (124).

5.18. Electric field and voltage potential contours on a plane 10 $\mu m$ above the electrode tips for VMS under a spacing of 200 $\mu m$. The coloured contours are voltage potentials. The black lines are geometric boundaries and electric field streamlines (125).
5.19. Voltage potentials along the line at $X=-2400\,\mu m$ for field shaping in CMS 
((a),(b)) and VMS ((c),(d)) with changing amplitudes on planes at $100\,\mu m
((a),(c))$ and $10\,\mu m ((b),(d))$. ...................................................... 126

A.1. Neural signal recording system used in *ex-vivo* testing ........................ 133
A.2. State diagram for individual channel control FSM ................................ 173
A.3. State diagram for stimulation control FSM ........................................... 174
A.4. DNL of channel 1 to 4 of chip 4 to 7. Red circles represent sourcing current;
Blue circles represent sinking current ...................................................... 175
A.5. DNL of channel 5 to 8 of chip 4 to 7. Red circles represent sourcing current;
Blue circles represent sinking current ...................................................... 176
A.6. DNL of channel 1 to 4 of chip 8 to 11. Red circles represent sourcing current;
Blue circles represent sinking current ...................................................... 177
A.7. DNL of channel 5 to 8 of chip 8 to 11. Red circles represent sourcing current;
Blue circles represent sinking current ...................................................... 178
A.8. INL of channel 1 to 4 of chip 4 to 7. Red circles represent sourcing current;
Blue circles represent sinking current ...................................................... 179
A.9. INL of channel 5 to 8 of chip 4 to 7. Red circles represent sourcing current;
Blue circles represent sinking current ...................................................... 180
A.10. INL of channel 1 to 4 of chip 8 to 11. Red circles represent sourcing current;
Blue circles represent sinking current ...................................................... 181
A.11. INL of channel 5 to 8 of chip 8 to 11. Red circles represent sourcing current;
Blue circles represent sinking current ...................................................... 182
A.12. DNL of channel 1 to 4 of chip 1 to 2 and 4 to 6 .................................... 183
A.13. DNL of channel 5 to 8 of chip 1 to 2 and 4 to 6 .................................... 184
A.14. DNL of channel 1 to 4 of chip 7 to 11 .................................................. 185
A.15. DNL of channel 5 to 8 of chip 7 to 11 .................................................. 186
A.16. INL of channel 1 to 4 of chip 1 to 2 and 4 to 6 .................................... 187
A.17. INL of channel 5 to 8 of chip 1 to 2 and 4 to 6 .................................... 188
A.18. INL of channel 1 to 4 of chip 7 to 11 .................................................. 189
A.19. INL of channel 5 to 8 of chip 7 to 11 .................................................. 190
# List of Abbreviations

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>AP</td>
<td>action potential</td>
</tr>
<tr>
<td>ASIC</td>
<td>application-specific integrated circuit</td>
</tr>
<tr>
<td>CIC</td>
<td>charge injection capacity</td>
</tr>
<tr>
<td>CMOS</td>
<td>complementary metal-oxide-semiconductor</td>
</tr>
<tr>
<td>CMS</td>
<td>current mode stimulation</td>
</tr>
<tr>
<td>CNS</td>
<td>central nervous system</td>
</tr>
<tr>
<td>CNT</td>
<td>carbon nanotube</td>
</tr>
<tr>
<td>DAC</td>
<td>digital-to-analogue converter</td>
</tr>
<tr>
<td>DBS</td>
<td>deep brain stimulation</td>
</tr>
<tr>
<td>DC</td>
<td>direct current</td>
</tr>
<tr>
<td>DCC</td>
<td>dynamic current copying</td>
</tr>
<tr>
<td>DNL</td>
<td>differential nonlinearity</td>
</tr>
<tr>
<td>ECoG</td>
<td>electrocorticography</td>
</tr>
<tr>
<td>EEG</td>
<td>electroencephalography</td>
</tr>
<tr>
<td>EEI</td>
<td>electrode-electrolyte interface</td>
</tr>
<tr>
<td>EMG</td>
<td>electromyography</td>
</tr>
<tr>
<td>EMI</td>
<td>electromagnetic interference</td>
</tr>
<tr>
<td>ENS</td>
<td>electric neural stimulation</td>
</tr>
<tr>
<td>ESD</td>
<td>electrostatic discharge</td>
</tr>
<tr>
<td>FDA</td>
<td>U.S. Food and Drug Administration</td>
</tr>
<tr>
<td>FEA</td>
<td>finite element analysis</td>
</tr>
<tr>
<td>FEM</td>
<td>finite element model</td>
</tr>
<tr>
<td>FPGA</td>
<td>field-programmable gate array</td>
</tr>
<tr>
<td>FSM</td>
<td>finite state machine</td>
</tr>
<tr>
<td>HH</td>
<td>Hodgkin-Huxley</td>
</tr>
<tr>
<td>HPA</td>
<td>health protect agency</td>
</tr>
<tr>
<td>HV</td>
<td>high voltage</td>
</tr>
<tr>
<td>IC</td>
<td>integrated circuit</td>
</tr>
<tr>
<td>INL</td>
<td>integral nonlinearity</td>
</tr>
<tr>
<td>Acronym</td>
<td>Description</td>
</tr>
<tr>
<td>---------</td>
<td>--------------------------------------------------</td>
</tr>
<tr>
<td>IPD</td>
<td>interphasic delay</td>
</tr>
<tr>
<td>IrOx</td>
<td>iridium oxide</td>
</tr>
<tr>
<td>ISMS</td>
<td>intraspinal microstimulation</td>
</tr>
<tr>
<td>JTAG</td>
<td>join test action group</td>
</tr>
<tr>
<td>MEA</td>
<td>multielectrode array</td>
</tr>
<tr>
<td>MHRA</td>
<td>Medicines and Healthcare Products Regulatory Agency</td>
</tr>
<tr>
<td>MIM</td>
<td>metal-insulator-metal</td>
</tr>
<tr>
<td>MOSCAP</td>
<td>metal-oxide-semiconductor capacitor</td>
</tr>
<tr>
<td>MSB</td>
<td>most significant bit</td>
</tr>
<tr>
<td>PCB</td>
<td>printed circuit board</td>
</tr>
<tr>
<td>PEDOT</td>
<td>poly(ethylenedioxythiophene)</td>
</tr>
<tr>
<td>PNS</td>
<td>peripheral nervous system</td>
</tr>
<tr>
<td>QMS</td>
<td>charge mode stimulation</td>
</tr>
<tr>
<td>RAM</td>
<td>random-access memory</td>
</tr>
<tr>
<td>RC</td>
<td>resistor-capacitor</td>
</tr>
<tr>
<td>SC</td>
<td>switched capacitor</td>
</tr>
<tr>
<td>SCI</td>
<td>spinal cord injury</td>
</tr>
<tr>
<td>SCS</td>
<td>spinal cord stimulation</td>
</tr>
<tr>
<td>SIPO</td>
<td>serial in parallel output</td>
</tr>
<tr>
<td>SPDT</td>
<td>single pole, double throw</td>
</tr>
<tr>
<td>TMS</td>
<td>transcranial magnetic stimulation</td>
</tr>
<tr>
<td>VMS</td>
<td>voltage mode stimulation</td>
</tr>
</tbody>
</table>
1. Introduction

In recent years, the public has been exposed to the possibilities of neuroprosthetics. Putting aside science fiction, there is indeed more ongoing research and more products emerging. Research on neuroprosthetics has been conducted for years and progress is being made. In February 2013, the U.S. Food and Drug Administration (FDA) approved the first artificial retina for adults with advanced retinitis pigmentosa. In May 2014, the DEKA arm system became the first FDA approved hand prosthetic arm that is controlled by interpreting the electromyography (EMG) signal from patients. With the DEKA arm seeing its way to the clinic, current research is focusing on the next generation solutions for other diseases such as spinal cord injury (SCI) which does not have any existing treatment at the moment. Towards this goal, a number of applications in electric neural stimulation (ENS) have been investigated and amongst these, intraspinal microstimulation (ISMS) has been identified as a method for achieving better performance in terms of fatigue-resistance and stimulation power (i.e. efficiency). However, there remains several significant challenges. In this chapter, the impact of spinal cord injury and current state of rehabilitation are described, it is followed by the project motivation and overview of the entire thesis.

The spinal cord is an important part of the central nervous system (CNS) which forms the main pathway between the brain and the peripheral nervous system (PNS). SCI refers to damage of the spinal cord caused by trauma, as opposed to disease. It is the second most common cause of paralysis in the US according to the survey of Christopher & Dana Reeve Foundation [1]. Depending on the severity of the damage, the patient may have symptoms ranging from pain and/or numbness to paralysis. The scale of impairment has been categorised by the American Spinal Injury Association [2]. Severe SCI can result in paraplegia or tetraplegia which significantly affects the quality of life in patients. The life expectancy of the patient is reduced. The quality of life is also reduced with the ongoing complications, such as the loss of bladder control, skin sensation, chronic pain and depression. The average annual medical cost after injury per patient is about $15,000 – $30,000 and the estimated lifetime cost ranges from $500,000 to more than $3 million depending on injury severity. Across the world, SCI is prevalent and causes high mortality-rates in developing countries. In some sub-Saharan African countries, SCI is almost always fatal due to poor healthcare [3]. Although the first-year survival rate is higher in developed countries with modern healthcare and rehabilitation methods, the chances of full recovery is still low even with an incomplete injury. According to [4], only less than 1 % of the patients experience full neurological recovery by hospital discharge. The other 99 % of the patients have to live with different extent of paraplegia or quadriplegia.

Unfortunately, there is currently no “cure” or therapy for the SCI, so prompt treatments and neurosurgery after SCI are essential to the rehabilitation. The treatment usually starts
at the scene of injury. The injury site of the spine is usually fixed in position as to reduce further damage while being transported to the hospital. Then the surgeon will try to remove any fracture of bone, disk and ligaments when the patient is sedated and medicated to reduce further injury and inflammation. After emergency procedures, when the situation is stable, the patient will be referred to rehabilitation. The first 6 months after injury is viewed as the golden time for patients to maximise recovery. However, if the situation does not improve after 12 months, the remaining loss of function tends to become permanent.

Modern rehabilitation involves several steps and mainly focuses on the impaired functions that significantly reduce the quality of life, for example, bowel and bladder control and fertility. Fortunately, the spinal cord does not need to be fully reconstructed in order to partially restore these functions. Established research branches into two directions: regenerating damaged neural tissue or bypassing [5]. Although regeneration research is ongoing, there are currently no clinically viable methods. Regeneration could be achieved by counteracting the neurite outgrowth blocking proteins and/or using neurotrophic factors. The required chemicals can be externally introduced via medication or by grafting other cells. It can also be internally secreted by the remaining cells that have been genetically modified around the injury site. Replacing lost cells are realised by transplantation cells that have potential to be differentiated into spinal cord cells at a later stage. These cells can be neural precursor cells derived from brain, stromal cells from bone marrow and embryonic stem cells. However, there are remaining questions to be answered for each of these methods. For patients whose spinal neural connections cannot be partially restored, the quality of life can still be improved by transferring the control from other parts of the body. For example, for people with quadriplegia, a wheelchair can be controlled by the tongue by monitoring its movement using an electronic system [6]. Alternatively, the wheelchair can be controlled via electroencephalography (EEG). These methods do not involve any type of neural stimulation.

1.1. Electrical Neural Stimulation

In addition to the efforts in seeking a biological treatment for SCI, modern technologies are providing devices for at least partial rehabilitation thus helping to improve the quality of life of affected individuals. Neuroprosthetics uses electronic prosthetic devices to restore the lost or damaged motor pathway (and/or sensory pathway). This is showing real promise towards restoring voluntary locomotion. Unlike biological approaches, electrical stimulation aims to integrate the electronic system(s) within the biological, with ultimate goal being to control or replace the lost function. Currently, this is used mainly for pain control and bladder control (in clinical applications). There have in fact been decades of research aiming to apply ENS to restore the lost control of limbs due to SCI [7]. Recently, there has been much exciting research starting to demonstrate paralysed limbs that can be controlled via ENS in spinal cord thanks to the use of microelectrodes [8, 9]. However, the majority of this research is still based on animal models and there are significant challenges in transferring them to humans. For example, the different organisation of the spinal cord in human and
other mammalian species (monkey, cat and rat) and the impact on health due to chronic system operation. However, even if ENS is not used chronically, it could be used as a therapy to encourage re-connection of impaired neurolinks [10–12].

The successful use of ENS is based on the fact that the neural circuitry below the point of the injury remains intact. Therefore, in theory, an exact replication of the stimulation pattern from the brain by the stimulator would induce the same type of muscle movement. In existing applications, various methods can introduce stimulation pattern throughout different stage of the neural circuitry. For bladder control, the electrode is interfaced directly with the detrusor muscle [13] or the sacral anterior root ganglia of the spinal cord [14]. For support standing, the electrodes are placed under the dura matter of spinal cord [11]. This is contrary to those that believe the best and natural way to restore the lost function would be to stimulate the motor neurons inside the spinal cord and let the untouched circuitry take care of the rest [8]. This kind of stimulation is termed ISMS. It has been found to provide distinct benefits over traditional ways including less number of required electrodes [8], more fatigue resistant [15] and more graded force generation [16]. However, the challenges are also more obvious. The closer the interface electrode is to the neural circuitry, the harder it is to replicate the command from the brain. This is because it requires higher resolution for both the pattern from the brain and the neural stimulation so as to interface specific motor neurons. In the following section, the associated challenges are described together with the motivation.

1.2. Motivation

As ISMS is fundamentally based on ENS, it must comply with the general guidelines and requirements of implantable electrical neural stimulators. The first and foremost requirement is safety. As the implantation itself is invasive, placing a potentially unsafe device directly inside the human body must be avoided at all cost. This is fortunately, strictly regulated by the government (e.g FDA in the US, or Medicines and Healthcare Products Regulatory Agency (MHRA) in the UK). More specifically, safety means no toxic substances are generated during stimulation with minimal tissue damage. The second requirement is size/weight of the implanted device. A smaller size not only limits the damage to the tissue after implant, but also reduces the burden on the patient. However, the size/weight is generally a trade-off to all the other requirements. For example, the size and weight varies a lot with and without a battery implanted. The third requirement is the lifetime/energy. In the ideal case, the energy provided to the stimulator should support the whole lifetime of the patient. However, limited by charge density of the battery technology and constrained by size, stimulators with built-in battery needs to be replaced every several years. Stimulators with rechargeable batteries offers a better solution, but is still limited by the maximum number of charge cycles. Also, energy density of rechargeable batteries is not as high as non-rechargeable ones. The fourth requirement is functionality/programmability which is more application specific. The more programmable it is, the better it can be tuned to adapt personal therapies without changing to another stimulator. Apart from these general
requirements, ISMS also needs to consider interfacing resolution requirement for the reason described in the last section.

A successful design of a neural prosthetic device should meet the above five technical requirements which need collaboration among several fields including surgery, electronics, material and biology. The interpretation of these requirements on the electronic side requires a stimulator that is safe and reliable, compact in design, energy efficient, programmable and can support multiple highly targeted channels.

**Safety**  The safety of the stimulation is twofold. The first part is related to the material the implantable devices and electrodes are made in. The second part is associated with the stimulus which involves electrochemical reactions such as hydrolysis and others that will release toxic substances into the human body and reduce electrode lifetime. Therefore, the task of the electrical design is to ensure that chemical reactions are limited to only the necessary extent and are reversible. To do this, the charge/energy provided by the stimulator for stimulation must be well controlled within a safe range. Commercial products use large direct current (DC) blocking capacitors which are considered ultimately safe but sacrifice size and weight as well as the number of channels that can be implemented. In recent devices however, there has been a trend of using blocking-cap free stimulator which will be reviewed in detail in Chapter 2.

**Energy Efficiency**  Energy efficiency varies with the methods of stimulus delivery and is a trade-off over safe residue charge control. Most of today’s chronic implant stimulators like deep brain stimulation (DBS) and pacemaker still use voltage mode stimulation for the sake of power-saving. People are trying to preserve the safety capabilities of the current mode stimulation while exploring the possibilities for reducing the overhead of generating a current stimulus. Another trend is to combine the current and voltage mode so as to enjoy the benefits of both.

**Programmability**  The research trend of programmability is to provide the user controllability over all the parameters related to the stimulus waveform. This will allow the user to change the therapy without changing the stimulator or repositioning the lead. It has become a must for a useful stimulator. However, this type of stimulators may have some issues passing regulations for implantable devices.

**Interfacing Resolution**  Because of the conductive nature of the human body, electrical stimulation usually mis-triggers unwanted neural tissue causing unwanted effects, i.e. destructive crosstalk/interference. This affects the performance of the implant only. For example, in cochlear implants, due to the stimulus spread, the total number of functional channels is limited between to between 3 and 9 [17]. Some of the effects may put the patient into danger. For instance, the spreading over unwanted target in DBS could cause depression leading to suicide [18]. High resolution is however required for prosthetics applications such as like artificial retinas or those targeting finer graded muscle force [16, 19]. Although this is mostly deemed a task for finer (i.e. reduced pitch) electrode design, it would be
highly advantageous to tackle this problem independent of electrode manufacturing technology. In this way, misplaced electrode can be repositioned by simply re-programming the devices rather than surgery (as is routinely done in cochlear implantation).

1.3. Research Aims

The aim of this research is to build an advanced stimulator that further improves the current state-of-the-art on the five aspects shown above. Especially, the focus of this research is on safety, energy efficiency, programmability and interfacing resolution. Such stimulator design would also aid neuroscientists in more basic research.

An illustration of the concept is shown in Fig. 1.1. The multichannel stimulator delivers the stimulus via an implanted multielectrode array (MEA). Voltage fields generated at each individual electrode interact with each other and generate a combined voltage field with a shifted peak towards the target.

1.4. Outline of this Thesis

Chapter 2 provides the background and reviews the relevant state-of-the-art to this thesis. It starts by introducing the basics of electrodes and electric physiology behind ENS, as well as precautions that should be taken during the stimulation. The focus then moves onto the background of ENS, and state-of-the-art stimulator designs are reviewed and compared. In the last section within this chapter, the current state of ISMS is reviewed and associated challenges are highlighted.

In Chapter 3, a new method is introduced which provides charge control in voltage mode stimulation to improve safety. A mixed-signal integrated circuit (IC) is described with proof of concept results using a resistor-capacitor (RC) model, in-vitro and ex-vivo separately. It achieves comparable results with other traditional stimulators within a compact silicon footprint.

Chapter 4 further develops the method introduced originally in Chapter 3 to form a stimulus based on charge-packets. Combined with voltage and current controlled methods,
eight individually programmable channels have been integrated within a single IC to provide monopolar and multipolar stimulation.

Chapter 5 investigates the idea of field shaping to allow the peak of the generated electric field to be shifted (or focused) based on the settings in a multipolar environment. The idea is developed using a finite element model. At last, Chapter 6 concludes the thesis by summarising potential future work.
Bibliography


2. Intraspinal Microstimulation: 
   Background and State-of-the-Art

2.1. Introduction

The development of neuroscience has allowed us to understand the role of the spinal cord in more detail, in particular, how muscles are controlled by will or reflex [1]. However in the 1800s, any “hardware” used to provide electrical stimulations was extremely basic, and thus the theory of neuron stimulation was not put into useful practice in public other than in research. Then, with the development of electronics and the integrated circuit (IC), it became possible to implant electronic devices (like the pacemaker [2], cochlear implant and gait control [3]) into the human body to facilitate rehabilitation, therapy or restore function. Current research is focused on further developing such devices to target much more complex high-level functions such as artificial retinas [4] and upper-limb prosthetics [5].

For different target applications, different stimulation strategies are required which means electric neural stimulation (ENS) is not always the best solution. For instance, transcranial magnetic stimulation (TMS) is mainly used in functional brain mapping and neurological diagnostics because it is non-invasive. Even in ENS, except for the safety requirement which is a “hard” requirement, the other four requirements in Section 1.2 hold different weights in different applications. For example, artificial retina requests high stimulation resolution and multiple channels, but deep brain stimulation (DBS) needs lower energy consumption and programmability.

In this chapter, the electrophysiology basics of ENS and intraspinal microstimulation (ISMS) are first introduced. Then different state-of-the-art design techniques for meeting the aforementioned requirements on ENS are reviewed. The chapter concludes by reviewing the current state of intraspinal microstimulators.

2.2. Background on Physiology

2.2.1. Organisation of spinal cord

The human spinal cord (shown in Fig. 2.1) nests in the vertebral column and is covered by meninges. It consists of various types of neural tissue and support cells. The column comprises 33 articulating vertebrae/segments for support and protection, forming 5 regions. The first region is called cervical which consists of 7 vertebrae that controls breathing, heart rate and forelimbs. The second region is the thoracic, typically consisting of 12 vertebrae which controls sympathetic tone, e.g. temperature regulation and trunk stability.
The next region is the lumbar which typically includes 5 vertebrae that controls hip motion and hindlimbs. The other two regions are the sacrum and coccyx which usually consist of 5 and 4 vertebrae respectively. They control sex and bladder functions. During spinal cord injury (SCI), the damaged region will lose its connection with the peripheral nervous system (PNS) fully or partially, whilst blocking the signal to and from the regions below despite maybe being intact.

A typical neuron is shown in Fig. 2.2 which has a soma, axon and dendrite. In vertebrates, an axon may be covered with the myelin sheath which increases the propagation speed of electrical neural signal and guide regrowth in damaged parts. In spinal cord, the soma of neurons forms grey matter at the central area of the spinal cord as shown in the left of Fig. 2.1. The grey matter is categorised into 10 laminae based on cellular structure of the cell as shown in Fig. 2.3 [7]. The axons of all spinal cord neurons form the white matter which encloses the grey matter. Some axons run along the rostral-caudal axis in the spinal cord to relay information in different segments while some form mixed spinal nerve that exits the spinal cord to connect to other organs in the body. Sensory information from organs is sent to the spinal cord via afferent nerves in the dorsal root that connects to the dorsal horn (laminae I-VI). On the other hand, the motor commands generated by the motor neurons in the ventral horn (laminae VII-IX) exit the spinal cord via nerves in ventral root to the target muscle.

2.2.2. Motor neuron-muscle relationships

Motor neurons not only exist in the spinal cord but also in the brain (upper motor neurons). However, only those in the spinal cord (lower motor neurons) control the skeletal muscle contractions. Neurons that control different muscles are located at different segments of the spinal cord. This location mapping between target muscle and origin motor neurons is studied extensively [8, 9].
Figure 2.2: An illustration of a typical neuron cell. Showing soma, dendrite, axon, node of Ranvier, myelin sheath.

Figure 2.3: Laminae of the spinal cord. Laminae I-VI forms the dorsal horn and VII-IX the ventral horn.
Each motor neuron innervates a single muscle fibre (a single muscle consists of several muscle fibres). All the motor neurons that innervate a single muscle form a rod-shaped cluster called motor neuron pool that extends over several spinal segments [6, 8]. As an example, mean and standard error values for the medial-lateral, dorsal-ventral and rostral-caudal extents of the triceps surae/plantaris activation pool in cat were on average $0.6 \pm 0.05 \text{mm}$, $1.0 \pm 0.1 \text{mm}$, and $11.4 \pm 0.3 \text{mm}$, respectively [10]. The sizes of such pool also change depending on the number of muscle fibres it controls.

Within each motor neuron pool, there are two types of motor neurons. The first type is $\alpha$ motor neuron which has a large soma (diameter is 50–100 $\mu\text{m}$ [11]). Fig. 2.4 shows the size of the motor neurons in at the lumbar region (L1) of human spinal cord [12]. $\alpha$ motor neuron directly controls the force generated by a muscle fibre. The second type is the $\gamma$ motor neuron, which is typically smaller in size. These innervate intrafusal fibres which are important for proprioception. In this research, this type of neuron is not important.

![Figure 2.4. Cross section of human spinal cord (lumbar region, L1) showing motor neurons located below lateral horn (see inset in (b)). Astrocytes and oligodendrocytes are labelled ‘A’ and ‘O’, respectively. White intracellular structure are labelled ‘?’ in (b). The objective magnification used is 40x. (a) and (b) use different stains method [12]. Copyright belongs to Gregor Overney.](image)

The $\alpha$ motor neurons, together with the fibres they innervate is called a motor unit (Fig. 2.5). Skeletal muscle contraction is a result of the combined action of these motor units. There are two types of motor units. One is fast motor units which react fast but is prone to fatigue. This type is good for fast reaction such as raising up a hand. The other type is the slow motor units which react slowly but are resistive to fatigue. These are good for holding a posture over a long time, such as standing. A single muscle can contain both types of motor units but each fibre can only belong to one type.

These motor units are different in size as well. Large motor units have large $\alpha$ motor neurons and larger fibres, whereas small motor units have smaller neurons and fibres. As reported by Elwood Henneman, the size principle dictates that motor neurons are recruited from small sizes to large sizes [13]. This means that motor neurons within a pool are not activated simultaneously but progressively depending on the required force. It is thus rare for all motor neurons to be active simultaneously [14].
2.2.3. Biophysics of action potential generation

This relationship lays the fundamentals of spinal cord stimulation. Depending on the location of the stimulation, different muscle contraction/extension pattern can be achieved. For all the neurons, not only the spinal cord neurons, a successful stimulation would generate an action potential (AP) which is an electric pulse. The whole generation originates from the interactions among different types of ion-channels in the neuron’s membrane and is briefly described below.

![Motor Neuron Pool](image)

Figure 2.5: An illustration of a motor unit adapted from [6]

![Motor Neuron Pool](image)

Figure 2.6: (a) The phospholipid cell membrane, ionic charges and an ion channel. (b) 4 phases during an AP generation: (i) stimulation causing depolarisation to above threshold, (ii) Na⁺ channels open and Na⁺ enters cell, (iii) K⁺ channels are open and K⁺ leaves cell, (iv) refractory period and ion pumps restore resting potential. Note that $I_{Na}$ and $I_K$ are caused by Na⁺ influx and K⁺ efflux respectively

An illustration of the cell membrane, ionic charges and an ion channel is shown in Fig. 2.6. Before stimulation, the neuron maintains a low concentration of Na⁺ and a high concentration of K⁺ inside the cell. K⁺ is allowed to leak outside, but an influx of Na⁺ is blocked. Therefore, the voltage across the membrane ($V_m$) is close to the potassium equilibrium.
voltage $E_K \sim 75\,\text{mV}$, giving a rest potential of around $-70\,\text{mV}$. This means there are more positive charges on the extracellular side of the membrane and more negative charges on the intracellular side as shown in Fig. 2.6(a). When a neuron is being stimulated, typically the sodium ion channels are opened which allows an influx of $\text{Na}^+$ that rises $V_m$ which is called depolarisation (phase (i) in Fig. 2.6(b)). However, as this influx needs to counteract the efflux of $\text{K}^+$, a threshold of $V_m$ is created around $-60\,\text{mV}$ above which more and more sodium channels are open due to positive feedback of $\text{Na}^+$ influx until they are fully open. Now as the $V_m$ reaches its peak which is approximately the sodium equilibrium voltage $E_{\text{Na}} \sim 65\,\text{mV}$ (phase (ii) in Fig. 2.6(b)), the channels are then gradually closed while the voltage gated potassium channels are still increasing the efflux of $\text{K}^+$ because of longer reaction time-constant. This causes a re-polarisation of the membrane towards $E_K$ (phase (iii) in Fig. 2.6(b)). Due to the momentum of the potassium influx, there will be an undershoot towards $E_K$ which is termed hyperpolarisation (phase (iv) in Fig. 2.6(b)). During this undershoot, if the sodium ion channels remain inactive, it is called an absolute refractory period during which the neuron cannot generate another AP under stimulation. Otherwise, it is called the relative refractory period as only opened potassium channels are counteracting the depolarisation. An AP can still be initiated during the relative refractory period provided the stimulus is large enough. The refractory period is responsible for uni-directional propagation of the AP. Then at last, the neuron is restored to the rest state by the ion pumps. The generated AP propagates to the connected neurons via chemical or electrical synapses.

In brief, what a stimulus should do is to open sodium ion-channels and the rest is a built-in biophysics process of a neuron. The ion-channels can be opened chemically or electrically. Chemical stimulus is called neurotransmitter which binds to target receptors on the cell membrane and control the ion channels. Because the neurotransmitter needs to diffuse to the targets, it is usually slower than the electrical stimulus. As the cell membrane is a good insulator, a rise of external voltage at a point closer to the neuron will consecutively increase the intracellular voltage at that point. Therefore, an intracellular current will be created causing charge redistribution at nearby points that causes $V_m$ to rise thus opening the voltage gated sodium ion-channels. Because of kinetics of the membrane and ion channels, there are other methods that can cause charge redistribution such as change of temperature or mechanical deformation of membrane [15].

2.3. State-of-the-art Electrical Neural Stimulation

A simple (and typical) ENS system consists of only the electrodes and their driving circuit. However, with challenging safety requirements (as those imposed by the U.S. Food and Drug Administration (FDA)), high stimulation efficiency and other more advanced functions, more and more circuits must be added to the system. In the following section, the basics are first introduced, and then state-of-the-art ENS systems are reviewed based on requirements stated in Section 1.2. Finally, generic approaches to overcome current spread in various ENS applications are reviewed.
2.3.1. Stimulation electrodes

In order to change the extracellular voltage of the target neuron, an electrode must be placed in proximity to that neuron to deliver the charge from the circuitry. In ENS, at least two electrodes are used. The one delivering the stimulus is called the working electrode and the one closing the circuit is called the return electrode.

**Electrode materials**

The properties (e.g. size, maximum charge capacity) of electrode material determines whether the electrode is suitable and safe for the target application. For ENS stimulation, the most important two factors are charge per phase and charge density [16]. Charge per phase is the total of charges delivered to the tissue during the stimulation phase. It is presented as the shaded area in the cathodic phase of Fig. 2.10. Charge density is defined as charge per phase divided by the geometric surface area of the electrode. The safety range for not inducing neural damage depends on the target neural tissue. For ISMS, no significant damage is reported for rats at charge per phase up to \(48 \text{nC}, 7000 \mu\text{C/cm}^2\) density [17].

On the other hand, charge density is also limited by the maximum charge injection capacity (CIC) determined by electrode material and surface roughness. Exceeding this limit means the charge injected is not recoverable due to chemical reactions which generate gas and/or changing pH. The CIC for commonly used electrode material (with possibly different manufacture treatment) is listed in Table 2.1, together with its charge injection mechanism. The charge injection mechanism is the way charge is exchanged between the electrode and the solution. Faradaic and capacitive charge injection are differentiated by the involvement of redox reactions which offer relatively large injection capability at the risk of damaging neural tissue and/or the electrodes. For such reasons, capacitive charge injection is desirable but may not be able to provide enough charge for stimulation. On the other hand, Faradaic charge injection needs to be applied carefully to avert damage. These two mechanisms are modelled in the electrode-electrolyte interface (EEI) model later in Section 2.3.1.

For ISMS, the threshold for generating AP is reported to be \(\sim 8.5–12.8 \text{nC/phase}, 1195.6–2601.2 \mu\text{C/cm}^2\) [17, 23]. The material can then be selected by the threshold value against the CIC value from Table 2.1 to ensure safety. However, it must be noted that these values are measured under different pulse widths and conditions (i.e. *in-vivo* or *in-vitro*) thus vary case by case. For instance, the value of the maximum CIC for a platinum electrode is found to be \(0.3–0.35 \text{mC/cm}^2\) when using a pulse width greater than 0.6 ms for evaluation but \(0.05–0.15\) with a pulse width of 0.2 ms.

Note that there are some materials used by researchers such as tungsten and stainless steel [23, 24] may not be considered suitable for chronic stimulation due to dissolution when exposed in an oxidising environment [18, 25, 26]. However, they are still useful for acute recording or stimulation and have been used intensively as the base for depositing other material onto the electrode because of their mechanical strength [22].

Beside the requirements shown above, the electrode also needs to show low impedance to allow better charge injection rate. In addition, the material needs to have enough mechanical
Table 2.1.: Charge-injection limits of electrode materials for stimulation.

<table>
<thead>
<tr>
<th>Material</th>
<th>Charge injection mechanism</th>
<th>Max. CIC (mC/cm²)</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pt &amp; PtIr alloys</td>
<td>Capacitive/Faradaic</td>
<td>0.05 – 0.54¹</td>
<td>[18–20]</td>
</tr>
<tr>
<td>Mesoporous Pt</td>
<td>Capacitive/Faradaic</td>
<td>~ 3</td>
<td>[18, 19]</td>
</tr>
<tr>
<td>Iridium smooth</td>
<td>Capacitive/Faradaic</td>
<td>0.1 – 0.6</td>
<td>[21]</td>
</tr>
<tr>
<td>Iridium oxide²</td>
<td>Faradaic</td>
<td>1 – 5</td>
<td>[18, 20]</td>
</tr>
<tr>
<td>Tantalum/Ta₂O₅</td>
<td>Capacitive</td>
<td>~ 0.5</td>
<td>[18]</td>
</tr>
<tr>
<td>TiN</td>
<td>Capacitive</td>
<td>~ 1</td>
<td>[18, 20]</td>
</tr>
<tr>
<td>PEDOT</td>
<td>Faradaic</td>
<td>~15</td>
<td>[18, 19]</td>
</tr>
<tr>
<td>CNT</td>
<td>Capacitive</td>
<td>1 – 1.6</td>
<td>[18, 19]</td>
</tr>
<tr>
<td>PEDOT coated CNT</td>
<td>Faradaic/Capacitive</td>
<td>392 – – 1400</td>
<td>[19, 21, 22]</td>
</tr>
</tbody>
</table>

¹ The theoretical capacity is around 0.3 – 0.35 µC/cm², but Pt dissolution starts as low as 20 – 50 µC/cm² in vitro and the potential would exceed water window at ~100 mV/cm².
² Depends on the method the iridium oxide electrode is manufactured and post-processed (i.e. conditioned), the CIC can be increased to ~5 mC/cm².

strength so that it will not break during implantation and be biocompatible so that it will not cause severe immune reaction during chronic stimulation. These general requirements can be found in [18, 19].

Microelectrode array

Although single microelectrode with a tip on the micrometer scale is usually used in research for single neuron access, multielectrode array (MEA) allows a compact and multiple access to a small region via only one implantation. Also, its manufacture controlled structure is good for studying neural dynamics as the locations of the neurons can be estimated.

Current MEAs are grouped into three main categories by [22]: microwire arrays, micromachined arrays and flexible arrays. Each has its own advantages and disadvantages as summarised in Table 5 in [22]. Microwire array is still preferred for chronic recording and neuron locating. However, since it is bendable during insertion, it is hard to place the tip accurately for neuron stimulation. Micromachined array can be better controlled during insertion and also provides better spatial resolution. However, it is hard to fix its position relative to the neural tissue. Therefore it may damage the tissue if any relative displacement happens. Flexible array is more used for surface recording, such as electrocorticography (ECoG) recording, because it is hard to implant the array deep inside the neural tissue. Most MEAs can be used for both recording and stimulation as long as the safety requirements are met.

In terms of commercially availability of these MEAs, Table 2.2 summaries the main MEAs sold by 4 companies. Note that not all these probes are approved for clinical use. For different applications, the electrode must have the correct geometry. For example, in ISMS, to access the target motor neurons in ventral horn, the length of the electrode needs to be greater than 5 mm when accessing from the dorsal side, and have a contact spacing (pitch) less than 500 µm so that at least one electrode will be inside the motor neuron pool. Then, it is clear that the Utah MEA is not a choice in this case.
Table 2.2: Main commercially available MEAs for *in-vivo* neural applications. Pictures are reproduced from the company websites.

<table>
<thead>
<tr>
<th>Manufacture</th>
<th>MicroProbes(^\circ)/Plexon(^\circ)(^1)</th>
<th>Blackrock Microsystems(^\circ)</th>
<th>Neuronexus(^\circ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Name</td>
<td>FMA</td>
<td>MEA</td>
<td>MWA</td>
</tr>
<tr>
<td>Category</td>
<td>micro-machined</td>
<td>micro-machined</td>
<td>microwire</td>
</tr>
<tr>
<td>Contacts Material</td>
<td>Pt/Ir, IrOx</td>
<td>Tungsten, Pt/Ir, IrOx</td>
<td>Stainless steel, Pt/Ir</td>
</tr>
<tr>
<td>Chronic/Acute</td>
<td>Both</td>
<td>Chronic(^3)</td>
<td>Both</td>
</tr>
<tr>
<td>Length (mm)</td>
<td>0.5 – 10</td>
<td>1.0 – 40</td>
<td>5 – 23</td>
</tr>
<tr>
<td>Contacts Spacing (μm)</td>
<td>250, 400</td>
<td>100 – 1000</td>
<td>multiples of 250</td>
</tr>
<tr>
<td>Contacts diameter (μm)</td>
<td>1 – 6</td>
<td>1 – 6</td>
<td>25, 50</td>
</tr>
<tr>
<td>Max. # of Contacts</td>
<td>36+</td>
<td>128</td>
<td>64</td>
</tr>
<tr>
<td>Impedance values (MΩ)</td>
<td>0.01 – 5</td>
<td>0.01 – 5</td>
<td>0.2 – 0.8</td>
</tr>
</tbody>
</table>

\(^1\) Plexon manufactures FMA and MWA under the same specification

\(^2\) Most of Neuronexus probes are customised

\(^3\) Pt/Ir or IrOx is recommended for chronic application

\(^4\) 65 mm is for extending the array to deep target
Electrode-electrolyte interface

EEI is formed on the surface wherever an electrode contacts an electrolyte. It is used to model the electrode properties using circuitry so that it can be used during the ENS design. These properties are complex, time-variant and non-linear. A lot of studies have been done in electrochemistry in order to understand and model them [18, 27–31]. Typical equivalent circuit models of EEI for ENS system design include only three components as shown in Fig. 2.7. The Warburg impedance due to mass transfer by diffusion in solution is not included because its value reduces at higher frequencies. For neural stimulation, it was experimentally determined to be insignificant. $Z_{CPA}$ is a constant phase angle component representing the capacitive charge transfer via the interface capacitance with the inhomogeneous surface [31]. $R_{ct}$ represents the Faradaic charge transfer and $R_S$ is the electrolyte spreading resistance between the working and return electrodes. Usually, capacitive charge transfer is more preferable as it will not involve any redox reactions. However, some extent of Faradaic reactions are allowed provided they are reversible.

2.3.2. Types and configurations

Based on the size, location and number of working and return electrode, ENS configurations can be grouped as monopolar, bipolar and multipolar (tripolar and more). An illustration of these three configurations is shown in Fig. 2.8. In the monopolar configuration, the return electrode has a much larger surface area than the working electrode and is placed at a distance. Therefore, in Fig. 2.7, $Z_{CPA}$ of the return electrode can be ignored. Moreover, no irreversible Faradaic reactions happen during normal operation. This is true as such Faradaic operation must be avoided for any stimulator. Therefore, $R_{ct}$ of both electrodes can be ignored. At last, assuming the surface of the electrode is smooth, $Z_{CPA}$ would represent a pure capacitor which is called double-layer capacitance ($C_{dl}$) [29]. This simplified model is more commonly used [32–37].

In bipolar and multipolar configuration, all electrodes are comparable in size and are placed at closer proximity than in monopolar stimulation. Therefore, $Z_{CPA}$ of all electrodes are comparable and cannot be ignored but can still be simplified to pure capacitors. As a result of the spacing between electrodes, the stimulus in monopolar stimulation has a radiative profile and a confined area in the other two configurations. Moreover, the multipolar configuration is capable of shaping the electric field generated by the stimulus since several working and returning electrodes are used simultaneously.

The electrical stimulus can be voltage, current or charge which can all achieve the same desired effect to depolarise the membrane. Corresponding to the three forms of stimulus,
there are three types of ENS system: current mode stimulation (CMS), voltage mode stimulation (VMS) and charge mode stimulation (QMS). Illustrations of their generic circuits are shown Fig. 2.9. In CMS, VMS and QMS, the current, voltage and charge are controlled respectively. Each has its own pros and cons and has been experimentally studied in [38].

**Current mode stimulation**

In CMS, the current flowing through the tissue is controlled, and therefore the total charge delivered is easily defined by timing. This is of great importance as excessive charge not only increases power consumption but also causes tissue damage (more details on safety are discussed in Section 2.3.3). However, a relatively high supply voltage is required to design the stimulator so as to accommodate a larger output range. This is because the required effective stimulation amplitude changes with the tissue impedance which is based on electrode placement, electrode age, or be patient specific. For instance, a stimulation current of 500 µA will cause 5V drop across the tissue (for an electrode-tissue impedance of 10 kΩ). This supply voltage requires a high voltage module for complementary metal-oxide-semiconductor (CMOS) IC fabrication with extra cost. In addition, this limits the maximum current that can be delivered as a sufficient voltage headroom must be preserved for the current source to work properly. As a result, when the maximum current is not used, power is wasted on the current source.

**Voltage mode stimulation**

In VMS, the voltage across the tissue is controlled instead of the current. Thus the ability to directly control the charge is lost as the tissue impedance is non-linear, time variant and at

![Monopolar Configuration](image1)

(a) Monopolar Configuration

![Bipolar Configuration](image2)

(b) Bipolar Configuration

![Multipolar Configuration](image3)

(c) Multipolar Configuration

**Figure 2.8.:** Main electrode configurations for ENS: (a) monopolar configuration, with return electrode placed at a distance from the working electrode and with a larger surface area; (b) bipolar configuration; (c) multipolar configuration

![Current Mode Stimulation](image4)

(a) Current Mode Stimulation

![Voltage Mode Stimulation](image5)

(b) Voltage Mode Stimulation

![Charge Mode Stimulation](image6)

(c) Charge Mode Stimulation

**Figure 2.9.:** The three types of ENS
unknown at design time. However, from a circuit design point of view, there is no need for this voltage headroom, thus simplifying the design and improving stimulation efficiency. Even though high voltage modules are unnecessary, they are typically used to enable a higher stimulation current.

**Charge mode stimulation**

In QMS, the charge is controlled directly. A typical implementation first charges a bank of capacitors to a predefined voltage and then discharge the charged capacitors through the tissue [36]. However, because of charge sharing, only part of the charge will be delivered to the tissue. The capacitors can be topped up after the stimulation. The charge delivered can be calculated through monitoring the residual voltage on the storage capacitor. In order to make sure most of the charge is injected into the tissue, large storage capacitors in the order of nanofarad are required. This unfortunately prevents a fully integrated design for QMS.

<table>
<thead>
<tr>
<th>Table 2.3.: Qualitative comparison between three different ENS modalities</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Stimulation efficiency</strong></td>
</tr>
<tr>
<td><strong>Main/Potential applications</strong></td>
</tr>
<tr>
<td><strong>Engineering challenges</strong></td>
</tr>
<tr>
<td><strong>References</strong></td>
</tr>
</tbody>
</table>

### 2.3.3. Safety

Safety is of crucial importance in the design of any ENS system and before deployment has to be regulated tightly through regulatory bodies such as FDA. It is required to be implemented in several aspects of the design. For example, system packages need to be made of biocompatible material to eliminate any rejection from the body in addition to not being harmful. Comprehensive reviews have been published on this topic [16, 45]. The main focus here is IC design techniques used to comply with the safety requirements which include charge balancing, fail-safe protection, thermal dissipation and size. Note that the important safety requirements on charge density and charge per phase are limited by the electrode rather than the stimulator as mentioned above and cannot be improved via better circuit design.

**Charge balancing** Charge balancing means the removal of any injected charge used for stimulation to give a zero residue charge after each stimulation. This is because residue charge will induce a direct current (DC) level across the EEI causing redox reactions. The resultant water electrolysis or toxic substance (chlorine) generation will reduce the electrode
lifetime as well as damage the surrounding tissue. For example, the maximum allowed residue DC current level is 100 nA for cochlear implant\(^1\) and 10 nA for retinal implant [47, 48].

One way of benchmarking the charge imbalance is residue DC level \(I_{DC,\text{res}}\) defined as

\[
I_{DC,\text{res}} = \frac{Q_{\text{res}}}{T_{\text{short}}}
\]

(2.1)

where \(Q_{\text{res}}\) is residue charge and \(T_{\text{short}}\) is shorting time. Equivalently, it means an imbalanced stimulation includes one perfectly balanced part and a DC stimulation part at a level of \(I_{DC,\text{res}}\). This equation can be further transformed by introducing charge mismatch factor \(\mu\) thus

\[
I_{DC,\text{res}} = \frac{Q_{\text{target}} \cdot \mu}{T_{\text{short}}}
\]

(2.2)

where \(Q_{\text{target}}\) is the total charge required. In this equation, \(I_{DC,\text{res}}, Q_{\text{target}}\) are determined by application while \(\mu\) is a design parameter. It is shown that for a high \(\mu\), the requirement on \(I_{DC,\text{res}}\) can still be met by tweaking the stimulation protocol, such as using a longer shorting time. On the other hand, a lower \(\mu\) gives more choices on stimulation protocol. Therefore, instead of using \(I_{DC,\text{res}}\), charge mismatch factor \(\mu\) highlights the quality of the design.

One traditional way to remove the charge is called passive charge balancing which shorts the working electrode and the returning electrode through a resistive path after each stimulation [49]. This method is intuitive and safe as it essentially shorts the two ends of EEI. However, because of the impedance of EEI, the discharging time constant is relatively large (several hundred of microseconds), limiting the repetition rate (speed) of the stimulation. Nevertheless, this method is usually applied at the end of each stimulation for extra safety. A slight variation of this is to use a buffer to provide a potential (usually the mid-rail voltage) and shorting all the electrode to this voltage [43, 50]

Active charge balancing means the injected charge is recycled via active circuitry. The simplest way is to use bi-phasic stimulus which is widely used nowadays. A typical CMS bi-phasic stimulus comprises two phases as shown in Fig. 2.10. The first phase is called the cathodic phase during which charge is injected to the tissue to activate the target neural tissue. The second phase is called the anodic phase during which the charge is recycled. Between the two phases, there is an interphasic delay (IPD) which is important in preventing the anodic phase suppressing the AP recruited by the cathodic phase [42, 51]. This asymmetric waveform is good for continuous stimulation by maintaining the same stimulation threshold. The shaded regions in the cathodic and anodic phases (Fig. 2.10) are designed to be equal in area in order to achieve zero residual charge. However, in practice this is challenging to achieve due to a mismatch between the current source (anodic phase) and the current sink (cathodic phase).

To avoid or improve the matching, several techniques have been proposed. [42, 46, 52] use a single current source for both delivery and recycling phases with the help of H-bridge.

\(^1\)A more strict requirement of 25 nA is used by [33, 46]
Ideally, if the biphasic waveform is symmetric, the mismatch of two phases of this type of design is very close to zero because the only limitation is the mismatch of the switches in the H-bridge and output impedance of the current source. For example, [46] uses symmetric stimulus and is able to achieve 5.6 fC for 140 nC charge delivery. However, for asymmetric waveform, the mismatch of the current source dominates as the reported charge mismatch ($\mu$) is around 0.5% for current source implemented using current mirrors and with good layout [42]. Ian Williams manages to further reduce $\mu$ to 0.05–0.15% over a series of 4 stimulations [52]. The asymmetric waveform is constructed by using all 4 current mirror outputs for charge delivery but only one for recycling. All the four outputs are cycled through so that a better matching is eventually achieved over 4 cycles.

Lam and Lee proposed a method to self-calibrate the digital-to-analogue converters (DACs) for generating biphasic current pulses which achieves $\mu = 0.06\%$ [53]. During IPD, the DAC used for charge balancing is calibrated by introducing an offset equal to the mismatch to the DAC used for charge delivery. A similar method, dynamic current balancing (using dynamic current copying (DCC)) is used by [4, 33, 54]. Instead of introducing an offset, the required gate driving voltage on the transistor working as the current source is sampled and held during calibration that precedes each stimulation. Although [54] gives $\mu = 0.012\%–0.035\%$ in simulation, the measurement results from [33] and [4] show $\mu = 0.4\%$ and $\mu = 0.5\%$ respectively.

Other than trying to balance the charge from the source, it can also be actively corrected afterwards. Ortman et al have developed a method that monitors the residual voltage caused by the charge across the electrode pair after each stimulation cycle [32]. For any value falling outside the safety window, an offset current or small current pulses would be applied to the tissue to reduce long term or short term residual charge respectively. For the reported system in [32], $\mu = 0.01\%$. Similarly Jiang et al use an extra current source to compensate the imbalance caused by the rounding problem of DAC when generating the scaled current output during active charge recycling [55]. The measured results is around $\mu = 0.01\%$. Alternatively, Fang et al monitor the stimulation current to estimate the total charge delivered rather than the voltage across the electrode resulting $\mu = 0.2\%$ [35].

**Fail safe protection** Even if perfect charge balancing can be achieved during normal operation, blocking capacitors are still used to protect the user in case of system failure. Otherwise, a direct DC path could form through the tissue, causing the same damage as
charge imbalance. But note that this is only true for systems using electrodes made of material that involves Faradaic charge transfer. Systems using electrodes made of capacitive charge transfer only material, e.g. Tantalum, can avoid the blocking capacitor [56]. However, these kind of electrodes are usually very large so as to meet the charge delivery requirement.

A typical value for these capacitors is in the order of $100 \text{nF}$ or $1 \mu \text{F}$ making them unsuitable for on-chip integration which has become a major issue for multichannel stimulators [55, 57]. There are designs aim to replace the capacitors with other fail-safe protection methods including monitoring the electrode-tissue impedance [43, 58], charge [35] and voltage [32]. Although these can achieve a certain level of protection, the operation of blocking capacitor depends only on the passive response of the device (e.g. the large shunt impedance) rather than an active monitoring. Hence it is challenging to be replaced. Instead of removal, high frequency current-switching provides a means of reducing its value to the pF range making integration possible [59].

Apart from the physical protections, system failure should always be avoided from the circuit design point of view. As a result, data integrity checks and correction are a standard procedure in most ENS systems [4, 55, 57, 60, 61].

**Thermal dissipation** Thermal dissipation from the circuit to the surrounding tissue is not a significant issue for external stimulators but is crucial for implantable microstimulators. The main heat sources on the chip include the implantable battery, power converters and high speed digital circuitry. If the implanted device receives data and power through a wireless link, the electromagnetic energy will also have an effect on heating tissue. Fortunately, it is within the safe range set by IEEE [62] in the US and health protect agency (HPA) in the UK [63]. The heat generated by the device itself is regulated by FDA in the US (ISO 14708-1:2013) and Medicines and Healthcare Products Regulatory Agency (MHRA) in the UK (BS ISO 14708-1:2013). They state that the temperature of the outer surface of a device must not rise more than $2^\circ\text{C}$ above body temperature [64]. The influence of power dissipation on tissue temperature elevation for retina prosthetic devices is investigated in [65] using a computer model. It is argued that the total power dissipation of a 16-electrode system must be kept below $12.4 \text{mW}$, (area $4 \text{mm} \times 4 \text{mm}$) which translates to a power density of $77.5 \text{mW/cm}^2$. The result obtained from *in-vivo* experiment using Utah electrode array implanted in the brain is about $57 \text{mW/cm}^2$ (13 mW; area is $7.88 \text{mm} \times 7.53 \text{mm}$; temperature increase 0.38) [66], which is 30% lower than the widely accepted value of $80 \text{mW/cm}^2$ [67]. Excessive heat must be taken away actively as done in [64].

The heat generated is directly proportional to the circuit power consumption which should be minimised. In the mean-time, the power efficiency of the system should be increased so as to reduce the power wasted and will be reviewed in Section 2.3.4. In [61], the total power of the implanted device is monitored and fed back to the external power transmitter. Therefore, the power transmitted can be adjusted to a proper level as required by the implanted system resulting in a higher power efficiency.
As a protection method, from a circuit design perspective, the system should be able to monitor the temperature of the surrounding tissue and limit the power consumption when there is a danger of overheating. This has been implemented in \[68\] and \[4\] for an in-vitro MEA used with cultured cells and retinal prosthesis respectively.

### 2.3.4. Power consumption

The power consumption of a system can be split into quiescent power $P_Q$ and dynamic power $P_D$. $P_Q$ does not vary with the stimulation protocol (i.e. stimulus profile and stimulation rate) but $P_D$ does.

Regarding the efficiency of the system, it can be defined as

$$\eta = \frac{P_{EEI}}{(P_D + P_Q)}$$

where $P_{EEI}$ is the power consumed on the tissue.

From the above equation, it is clear that $\eta$ can be improved if $P_Q$ and $P_D$ can be reduced. $P_Q$ is mainly limited by the analogue part of the system. Because of the presence of DAC, current mirror and other biasing circuit, $P_Q$ is on the order of $10 \sim 100 \mu W$ per channel for most designs \[4, 35, 42, 69\]. \[46, 54, 68\] achieves $P_Q < 10 \mu W$ by disabling the analogue front-end outside stimulation time. However, \[59\] hits the higher end of $P_Q$ (200 $\mu W$) because of higher switching frequency used in the front-end.

The dynamic power consumption per channel $P_D$ is in the same order as $P_Q$ and can also be reduced. It has two contributors. The first one is the system overhead which controls the stimulation and ensures safety. So, simple designs with blocking capacitors would give a better result on this factor. The second part is the power consumed in stimulation path excluding all the useful power for stimulation ($P_{EEI}$). Ghovanloo et al introduces stimulation efficiency to quantify this factor based on stimulation type and found CMS is the least efficient while VMS is the most efficient. Nevertheless, CMS is still the most favourable method. \[40, 52, 70\] manages to saving around 50 $\sim$ 60% wasted power by using dynamic power supplies.

### 2.3.5. Size and programmability

As discussed in Section 1.2, smaller and lighter system is better for implantation and free-behaving animal experiments. And this is not a problem for the design as long as the system is fabricated on silicon chips and without power supply implanted. However, for fully implanted system, it is system is often limited by the size of the battery. Hence, wireless microstimulator is the best solution \[43, 51, 57, 61, 71\]. Although wireless technology is a hot topic both for neurostimulation and neurorecording, it is not a focus in this thesis. Typical whole system sizes are in the order of centimetre. An in depth review can be found in \[72\].

Programmability is an important aspect for the stimulator to be useful in clinical and research applications. Most stimulator would provide programmability on stimulus amplitude, inter-phasic delay, stimulation frequency and active channel \[4, 57\]. Some also provide more than one stimulation type and arbitrary waveform programming \[43, 73–75\].
2.3.6. Targeted stimulation

The current spreading problem is a fundamental challenge in all ENS applications. For example, although MEA can provide more physical channels for the cochlear implant (up to 22 in commercial devices), the effective number of channels has been limited to just 8 due to current spread [76]. The same challenge has been faced in retina prosthetics which has become one of the main limitations [37].

Existing works aimed at addressing this can be classified into three main categories: (1) manipulating the position of the MEA; (2) employing regenerative electrodes; (3) manipulating the configuration of the stimulating electrodes [77]. For the first category, the MEA is placed closer to the target neurons in order to reduce the stimulation current thus reducing the spreading effect. For the second method, neurotrophic electrodes are employed to enable the dendrites grow on the electrodes reducing the distance between the electrodes and neurons. Although this is excellent for an in-vitro platform, developing this towards an implantable device is expected to be challenging. The third method dynamically reconfigures the MEA such as to explore its maximum achievable resolution. For example, using adjacent electrodes in an array to provide the current return path for a single stimulation electrode to confine the stimulus current [37]. Although this does provide some improvement, the main issue tends to be increased power consumption due to shunting currents increasing, thus reducing stimulation efficiency. Another method is to use phased-array techniques [78] to further improve the stimulation resolution based on the interference of the electromagnetic wave in the far field [79, 80]. Therefore GHz signal needs to be used which makes it is hard to generate using a standard CMOS process and consumes a huge amount of power.

2.4. Current State of Intraspinal Microstimulation

Spinal cord stimulation (SCS) is mainly used to treat the chronic pain based on the gate theory published in 1965 [81]. It has matured to the extent that commercial FDA-approved SCS systems are available through Medtronic, Inc. and several other medical device companies. These systems are typically implemented using integrated technology and are therefore fully implantable, with the electrodes implanted into the epidural space. These systems also use inductive power transfer to recharge an implantable battery. The charge interval is usually more than 24 hours [82].

Different from SCS, ISMS is still at the research phase. Experimental neurologists tend to use bulky, external equipment to generate the stimulus that is then delivered through an implanted microelectrode (array) [10, 23, 83, 84]. Although there are many published ENS systems, commercial products may not provide configuration flexibility for ISMS.

ISMS generally aims to stimulate specific motor neuron pools with typical stimulation current around 100 µA for a duration of 100 ~400 µs. Within this field, there has recently been a great surge in interest within the neuroscience community. The key drive is to apply this method towards restoring motor function in fore-/hind- limbs.

Prosthetics of hindlimb control have been mainly studied and tested on cats [24, 85–87].
Overall results indicate that ISMS is possible to innervate muscles that are needed for standing [85] and closed-loop stepping [24, 86]. For forelimb, Zimmermann et al have demonstrated that grasp and release function of the hand can be achieved through ISMS with only 2 electrodes [23]. They also showed that models designed based on ISMS can provide predictable and chronic stimulation.

These results do provide a good motivation for using ISMS to restore lost spinal cord function, but the aforementioned stimulus spread problem remains. Current spread range in the spinal cord grey matter is predicted to be of 0.5 to 0.7 mm for 70 \( \mu \text{A} \) and 0.6 to 0.8 mm for 100 \( \mu \text{m} \) in cats [88]. Although this value will not cause misfiring of the motor neurons in a neighbourhood pool as tested in the same paper, this will limit the control of the muscle fibres within the pool. Therefore, it is not good for gradual control of the force of a single muscle or better fatigue resistive stimulation.

In addition, movement of microelectrodes can pose further challenges, for example in [24], one electrode tip is shifted slightly after implantation, resulting in activation of both the knee extensors and ankle flexors and produced a contralateral response. In such cases it is highly undesirable to explant and re-implant due to the risk of infection and to avoid any additional damage to the tissue.

These two problems can be resolved if stimulus focusing can be achieved, meaning the stimulus be confined to a smaller area and steered towards a specific direction. An effective implementation would bring ISMS closer to the level of flexibility provided by the traditional ENS methods. As a result, finer control of the skeletal muscle can be achieved and a displacement of the electrodes can simply be re-calibrated. Now the problems have shifted to finding a method(s) for limiting the current spread effect and focusing the stimulus. Unfortunately, the methods proposed for ENS in Section 2.3.6 have not been applied to ISMS [71].

2.5. Conclusions

In this chapter, the basic theory of neural stimulation is introduced as well as basic modelling of EEI. Published systems are reviewed from different aspects with an emphasis on stimulation safety. A summary table is shown in Table 2.4. It is shown that there are various methods for achieving charge balancing and designers are trying to replace the non-integratable blocking capacitors with active monitoring system. Some proposed systems also monitor the temperature and power condition of the system. Power consumption keeps shrinking as researchers are reducing the quiescent power on the analogue part and power wasted on the stimulation path (e.g in CMS). Size requirement has pushed system to utilise wireless technology for power transfer. Programmability is nearly a standard for ENS stimulators. Targeted neural stimulation has become a major limitation on the effective number of stimulation channels. Various methods have been proposed ranging from electrode re-design to voltage field shaping. Each has its own challenges. At last, the current state of ISMS is discussed. Although general ENS system is normally applicable, researchers still prefer to use bench-top equipments because commercial stimulators for other applications...
has configurations that cannot be overridden. Moreover, designing an application-specific integrated circuit (ASIC) stimulator needs more effort and collaboration with IC engineers. Also, ISMS requires better spatial resolution which may not be possible with off-the-shelf stimulators.
Table 2.4.: Performance comparison

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Year</th>
<th>Process</th>
<th>Application</th>
<th>Q mismatch (method)</th>
<th>Full scale</th>
<th>Power (Quiescent)</th>
<th>Area (mm²)</th>
<th>No. of Ch.</th>
<th>Electrode conf.</th>
<th>Improved res.</th>
</tr>
</thead>
<tbody>
<tr>
<td>[4]</td>
<td>2014</td>
<td>65 nm</td>
<td>Retina</td>
<td>0.5% (DCC)</td>
<td>465 µA</td>
<td>33 mW (10 mW)</td>
<td>2.76 × 2.91</td>
<td>256</td>
<td>Multipolar</td>
<td>Current-steering</td>
</tr>
<tr>
<td>[52]</td>
<td>2013</td>
<td>0.18 µm HV</td>
<td>PNS</td>
<td>0.46% (H-Bridge)</td>
<td>504 µA</td>
<td>(185 µW)</td>
<td>2 × 2.7</td>
<td>8</td>
<td>Bipolar</td>
<td></td>
</tr>
<tr>
<td>[70]</td>
<td>2012</td>
<td>0.35 µm</td>
<td></td>
<td></td>
<td>450 µA</td>
<td>1.12 × 0.52 †</td>
<td>1</td>
<td></td>
<td>Bipolar</td>
<td></td>
</tr>
<tr>
<td>[46]</td>
<td>2012</td>
<td>Discrete</td>
<td></td>
<td>0.04 ppm (H-Bridge)</td>
<td>1.4 mA</td>
<td>(25 µW)</td>
<td></td>
<td></td>
<td>Mono/Bi-polar</td>
<td></td>
</tr>
<tr>
<td>[55]</td>
<td>2011</td>
<td>0.6 µm HV</td>
<td></td>
<td>0.01% (Compen.)</td>
<td>1 mA</td>
<td>6.77 mW (1.1 mW)</td>
<td>2.27 †</td>
<td></td>
<td>Bipolar</td>
<td></td>
</tr>
<tr>
<td>[40]</td>
<td>2011</td>
<td>1.5 µm</td>
<td></td>
<td></td>
<td>±2.5 V</td>
<td>2.18 mW (335 µW)</td>
<td>4.76</td>
<td></td>
<td>Bipolar</td>
<td></td>
</tr>
<tr>
<td>[80]</td>
<td>2011</td>
<td>DBS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Phase array</td>
<td></td>
</tr>
<tr>
<td>[49]</td>
<td>2011</td>
<td>0.35 µm</td>
<td>Cortical</td>
<td>(Passive)</td>
<td>94.5 µA</td>
<td>375 µW*</td>
<td>3.3 × 3.3</td>
<td>4</td>
<td>Bipolar</td>
<td></td>
</tr>
<tr>
<td>[32]</td>
<td>2010</td>
<td>Discrete</td>
<td></td>
<td>0.01% (Compen.)</td>
<td>10 mA</td>
<td>135 mW*</td>
<td>7.5 × 6.1</td>
<td>126</td>
<td>Multipolar</td>
<td></td>
</tr>
<tr>
<td>[68]</td>
<td>2010</td>
<td>0.6 µm</td>
<td>in-vitro</td>
<td></td>
<td>255 µA</td>
<td>25 mW</td>
<td>4.6 × 5.4</td>
<td>100</td>
<td>Bipolar</td>
<td></td>
</tr>
<tr>
<td>[51]</td>
<td>2009</td>
<td>0.6 µm Bi-CMOS</td>
<td></td>
<td>&lt; 0.35% (DCC)</td>
<td>1 mA</td>
<td>0.04 †</td>
<td></td>
<td></td>
<td>Bipolar</td>
<td></td>
</tr>
<tr>
<td>[37]</td>
<td>2009</td>
<td>0.35 µm HV</td>
<td>Retina</td>
<td>&lt; 2.6% (Shorting)</td>
<td>600 µA</td>
<td>9.81 mW (152.3 µW)</td>
<td>2.8 × 4.6</td>
<td>14</td>
<td>Multipolar</td>
<td>Guarding</td>
</tr>
<tr>
<td>[59]</td>
<td>2008</td>
<td>1 µm SOI</td>
<td>Retina</td>
<td>0.012% (Passive)</td>
<td>1 mA</td>
<td>8.54 mW (200 µW †)</td>
<td>1.52 †</td>
<td>4</td>
<td>Bipolar</td>
<td></td>
</tr>
<tr>
<td>[35]</td>
<td>2008</td>
<td>0.18 µm</td>
<td></td>
<td></td>
<td>1.8 V</td>
<td>50 µW</td>
<td></td>
<td></td>
<td>Monopolar</td>
<td></td>
</tr>
<tr>
<td>[42]</td>
<td>2008</td>
<td>0.35 µm</td>
<td>Bi-CMOS</td>
<td>0.5% (H-Bridge)</td>
<td>735 µA</td>
<td>(65.5 µW)</td>
<td>1.5 × 0.9</td>
<td>3</td>
<td>Bipolar</td>
<td></td>
</tr>
<tr>
<td>[53]</td>
<td>2007</td>
<td>0.7 µm HV</td>
<td></td>
<td>0.4% (DCC)</td>
<td>1 mA</td>
<td>647 µW</td>
<td>2.3 × 2.3</td>
<td>16</td>
<td>Monopolar</td>
<td></td>
</tr>
<tr>
<td>[53]</td>
<td>2007</td>
<td>0.7 µm HV</td>
<td></td>
<td>0.06% (Cal-DAC)</td>
<td>3.2 mA</td>
<td>67 µW</td>
<td>1.7 × 0.31</td>
<td></td>
<td>Monopolar</td>
<td></td>
</tr>
<tr>
<td>[61]</td>
<td>2007</td>
<td>0.18 µm</td>
<td>Cortical</td>
<td></td>
<td>140 µA</td>
<td>880 µW</td>
<td>3.2 × 2.8</td>
<td>16</td>
<td>Mono/Bi-polar</td>
<td></td>
</tr>
<tr>
<td>[43]</td>
<td>2007</td>
<td>1.5 µm</td>
<td>Cortical</td>
<td>(Shorting)</td>
<td>270 µA</td>
<td>8.25 mW</td>
<td>4.6 × 4.6</td>
<td>32</td>
<td>Bipolar</td>
<td></td>
</tr>
<tr>
<td>[50]</td>
<td>2006</td>
<td>0.8 µm Bi-CMOS</td>
<td>ISMS</td>
<td></td>
<td>63.5 µA</td>
<td>4.5 × 4.5</td>
<td>16</td>
<td></td>
<td>Bipolar</td>
<td></td>
</tr>
<tr>
<td>[57]</td>
<td>2001</td>
<td>2 µm</td>
<td>Retinal</td>
<td>(Passive)</td>
<td>1.3 mA</td>
<td>4.6 × 6.8</td>
<td>100</td>
<td></td>
<td>Bipolar</td>
<td></td>
</tr>
<tr>
<td>[60]</td>
<td>1999</td>
<td>1.2 µm</td>
<td></td>
<td></td>
<td>6.3 mA</td>
<td>0.04</td>
<td></td>
<td>4</td>
<td>Bipolar</td>
<td></td>
</tr>
</tbody>
</table>

† Active area
* Including recording system
‡ Simulated
Info that is not provided by the associated publication left blank
Bibliography


[75] K. Sooksood, E. Noorsal, J. Becker, and M. Ortmanns, “A neural stimulator front-end with arbitrary pulse shape, HV compliance and adaptive supply requiring 0.05 mm2 in 0.35um HVCMOS,” in *Proc. IEEE ISSCC*, vol. 4, no. 3. IEEE, 2011, pp. 306–308.


3. A New Method for Safe Electrical Neural Stimulation: Charge-metering

3.1. Introduction

This chapter presents a novel technique for charge-metered voltage mode stimulation (VMS) that achieves good charge balancing using two small fully integrated capacitors. This technique was adopted from an application in nuclear science for charge monitoring [1]. It has also been applied in a mixed signal integrator design [2]. Following the preliminary work [3], an application-specific integrated circuit (ASIC) is manufactured as a proof of concept. The methodology and system architecture are detailed below and evaluation was performed using resistor-capacitor (RC) electrode-electrolyte interface (EEI) model, buffered saline solution and ex-vivo Xenopus sciatic nerve.

3.2. Principle and System Architecture

The system architecture is shown in Fig. 3.1. It can be divided into two sub-systems: an analogue front-end for the charge sensing, and a digital back-end for the charge measuring and system control. $R_S$ and $C_e$ represents the EEI described in Section 2.3.1. The required charge quantity is set by the controller which sequences the switches to deliver the stimulation current via two paths formed by $C_{unit1}$ and $C_{unit2}$ alternatively. The two comparators and one counter will track the number of times these paths were taken, hence the total amount of charge injected/recycled. The method will be explained in detail in Section 3.2.1 and 3.2.2. Its integrated circuit implementation and evaluation setup are described in Section 3.2.3 and 3.2.4 respectively.

![System Architecture Diagram](image)

Figure 3.1.: System architecture of the proposed charge-metering system. ($R_S$ represent the tissue spreading resistance and $C_{dl}$ the electrode-electrolyte-tissue double layer capacitance. $V_{ref}$ for the two comparators are the same. Both $V_{ref}$ and $V_{stim}$ are provided externally.)
3.2.1. Method of charge-metering

The essence of charge-metering is integration of the current over the stimulation/recycling period. One straightforward method would be to use a capacitor. To measure 10 nC charge is the same as measuring 10 V across the two plates of a 1 nF capacitor. However, integrating 1 nF on-chip is generally unfeasible due to area requirements. Therefore, a small value capacitor must be used. A simple analogy is measuring a large quantity of water using only a small measuring cup. The method presented here measures a small quantity of charge each time with a small measuring capacitor and using a digital counter to record the number of the total measurements made. A similar architecture is used to measure the current in the frequency domain [4].

The circuit operates as follows. In Path 1 (Fig. 3.1), \( C_{\text{unit1}} \) is charged until the comparator tells the controller to start discharging it. Ideally, the maximum amount of charge that can be stored before discharging is \( C_{\text{unit1}} \times V_{\text{ref}} \). This amount will hereon be referred to as the unit charge. This charge and discharge sequence is repeated continuously using a controller. It should be noted that Path 1 will be broken during the discharge of \( C_{\text{unit1}} \) to prevent the stimulation current bypassing \( C_{\text{unit1}} \). However, the break is undesirable as its physiological effect is unknown. Therefore, the circuit is replicated such that a second current path (Path 2) operates in a complementary fashion such as to maintain a continuous current flow.

If \( V_{\text{ref}} = 1 \text{V} \), the unit charge quantitatively equals the value of \( C_{\text{unit1}} \) and \( C_{\text{unit2}} \). From hereon, these two capacitors will be referred as the unit capacitors (\( C_{\text{unit}} \)) as they have the same value and good manufacture tolerance. Each unit charge delivered to the electrode is counted and thus the total charge (\( Q_{\text{total}} \)) delivered can be determined by:

\[
Q_{\text{total}} = \sum_{i}^{N} C_{\text{unit}} \times V_{\text{ref}}
\]

where \( N \) is the output of the counter.

The system comprises 6 switches: \( SW_1 \) enables both paths; \( SW_{2-3} \) determine the polarity of the stimulus and are used to short the electrodes; \( SW_{4-5} \) are used to discharge the unit capacitors; \( SW_6 \) steers the stimulation current between Path 1 and Path 2.

3.2.2. Stimulus generation

The system generates a biphasic stimulus (similar to Fig. 2.10) using five phases as described below. The detailed current path and switch positions are shown in Fig. 3.2.

**Phase 1 – Initial/Shorting Phase** The system is reset and the \( C_{\text{unit}} \) are discharged. The stimulation path is broken and the electrodes are shorted. \( SW_6 \) can be at either \( T_1 \) or \( T_2 \). This phase can also be used for shorting after a stimulation cycle to further reduce the residual charge.

**Phase 2 – Cathodic Phase** The stimulation path is established and current is integrated on \( C_{\text{unit}} \). The charge is delivered by continuously alternating between Path 1 and Path 2.
Figure 3.2: Positions of the 6 switches during different phases of stimulus generation.
as described in Section 3.2.1. During this phase, the counter counts upwards till the target value is reached.

**Phase 3 – Inter-phasic Delay**  A short delay is introduced between the cathodic and anodic phases to avoid blocking the propagation of the induced action potential (AP) [5].

The stimulation path is broken and the switches are set as for the anodic phase.

**Phase 4 – Anodic Phase**  The charge delivered previously is recycled in this phase. The operation is similar to that of the cathodic phase, with SW2, SW3 and SW6 inverted and the counter counts down until it reaches zero. Note that the positions of T1 and T2 determine the polarity of the stimulation.

At the end of the anodic phase, the system will cycle back to the Initial/Shorting Phase to further reduce the residual charge and wait for the new stimulation cycle to start.

The stimulus parameters can be programmed as follows: the quantity of charge needs to be delivered is set by the controller; the stimulation duration is coarsely tuned by $V_{\text{stim}}$; the inter-phasic delay is defined externally via an RC delay network.

### 3.2.3. Circuitry

The circuit has been implemented in AMS 0.18μm 1P4M CMOS technology. This section details specific design aspects of the circuit implementation.

**Switch Design**

All the switches are implemented using transmission gates with equal device sizes ($W/L = 10\mu m/0.18\mu m$) for both NMOS and PMOS. The widths are designed to be the same so as to mitigate the charge injection effect during switching. Calculated turn-on resistance is between 80 $\Omega$ and 330 $\Omega$ with associated gate capacitance of 28 fF. Parametric simulations confirm that the drop-out voltage on the switch does not change significantly by further increasing their width for the required stimulation current. Each single pole, double throw (SPDT) switch (SW2,3,6) is implemented using two transmission gates. Switch charge injection is not expected as a challenge because: (1) transmission gates significantly reduce any switch-related charge injection; (2) matching between switches in Path 1 and Path 2 ensures any injected charge is recycled.

**Unit Capacitor Selection & Comparison threshold ($V_{\text{ref}}$)**

The value of $C_{\text{unit}}$ and $V_{\text{ref}}$ are crucial design parameters. They first define the measurement resolution ($V_{\text{ref}} \times C_{\text{unit}}$) but also set the scale and power requirements of the system.

For a fixed $V_{\text{ref}}$, a smaller $C_{\text{unit}}$ is preferable for a finer resolution and reduced area. However, this is at the expense of an extended counter range (for a fixed target charge quantity). In addition, this requires the counter to operate at a higher frequency as $C_{\text{unit}}$ is charged and discharged faster. Moreover, the smaller the capacitor the greater the effect of mismatch. Therefore, there is a power/area/resolution/mismatch trade-off. To allow
multiple stimulation channels on a single chip, both the power consumption and silicon area should be minimised. Initially, \( C_{\text{unit}} = 1 \text{pF} \) was used as this has two desirable effects: increasing the stimulation resolution and also reducing the silicon area. However, this also increases the operating frequency (Eq. 3.2) to 100 MHz, which is comparable to the delay of the continuous time comparator designed (Section 3.2.3). Therefore, a \( C_{\text{unit}} = 10 \text{pF} \) has been selected (using \( 10 \times 1 \text{pF} \) capacitors) to relax timing constraints and provide a charge resolution of 10 pC. With a 10-bit counter, a maximum charge of 10.24 nC can be delivered, meeting the requirement for intra-cortical stimulation for human vision prosthetics [6] and intraspinal microstimulation [7]. For other applications, such as retinal stimulation using an iridium oxide (IrOx) electrode requiring a stimulus of 800 nC (800-200 \( \mu \)A within 1-4 ms) [8], the counter needs to extend its range from 10-bit to 13-bit. The time constant for charging \( C_{\text{unit}} \) is:

\[
\tau \approx R_s \times (C_{\text{dl}}^{-1} + C_{\text{unit}}^{-1})^{-1}
\]  

(3.2)

Where \( C_{\text{dl}} \) is in the order of 10-100 nF and \( R_s \) the order of 10s of k\( \Omega \). Therefore the overall capacitance is determined by \( C_{\text{unit}} \). This sets the time constant \( \tau \) to be approximately 100 ns and the operating frequency of the digital controller to be approximately 10 MHz. Note that the capacitor is not charged to the stimulation voltage so that it is faster than \( 2.2 \times \tau \).

On the other hand, \( V_{\text{ref}} \) also affects the resolution. It however, also sets the common mode of the comparator and it is preferable to set this to around half the supply voltage (0.9V). To simplify the design, \( V_{\text{ref}} \) is set to 1 V so that the stimulation resolution is numerically equal to \( C_{\text{unit}} \). However, because of the control loop delay, \( V_{\text{ref}} \) is actually smaller than 1 V (see Section 3.3.1) and is determined via simulation so that the \( C_{\text{unit}} \) will be discharged when its voltage reaches 1 V.

**Comparator**

A continuous time comparator is designed (Fig. 3.3). A regenerative load is used to increase the gain. The strength of positive feedback formed by M5 and M6 is given by \( \alpha = \frac{(W/L)_5}{(W/L)_6} = 1 \). This means the comparator works as a latch. Since the load of the comparator is an OR gate whose input capacitance is \( \approx 2 \text{fF} \), the delay is limited mainly by the parasitic capacitance observed at the drains of M1 and M2. In order to minimise this parasitic capacitance and thus reduce power consumption, \( (W/L)_{1-6} = 1 \mu \text{m}/1 \mu \text{m}, (W/L)_{7,10} = 0.4 \mu \text{m}/1 \mu \text{m} \). This is at the cost of introducing larger input offset voltage. However, this offset voltage can be compensated by tuning the threshold voltage \( V_{\text{ref}} \). The bias current is set to 6\( \mu \)A (determined through simulation) such that the delay is around 10 ns. This delay cannot be improved much further without significantly increasing power consumption or changing to synchronous comparator. Although the output swing of the comparator is limited by the headroom of the output transistors, a full swing can be achieved at the output of the OR gate.
Controller & Counter

The controller is implemented using a finite state machine (FSM) coded in Verilog Hardware Description Language to achieve the operating sequence described in Section 3.2.2. A 10-bit up/down binary counter is used to record the charge delivered. The circuit comprises 10 flip-flops with supporting combinational logic. Fig. 3.4 shows the least significant 3-bits. The counter operates synchronously and counts upwards when Direction is HIGH and downwards when LOW. Calculated from the specifications of the standard cells provided by the foundry, the counter consumes between 360 nW to 840 nW (varies with load and input transition time) at 10 MHz with a stimulation period of 1 ms and a duty cycle of 20%. This power is negligible compared to that of the comparator.

3.2.4. Evaluation methods

The system has been tested using 4 different methods to evaluate its performance on charge-metering, charge-balancing, process variation, mismatch, and its physiological effect. The evaluation matrix is shown in Table 3.1.

The circuit is simulated using Cadence IC 5.1.41ISR2 with foundry-supplied PSP (Penn

<table>
<thead>
<tr>
<th>Test Name</th>
<th>Simulation</th>
<th>RC Model</th>
<th>Saline Tank</th>
<th>Ex-vivo†</th>
</tr>
</thead>
<tbody>
<tr>
<td>Charge metering</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>Charge balancing</td>
<td>✓</td>
<td>✓</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>Process variation &amp; mismatch</td>
<td>✓</td>
<td></td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>Nerve Stimulation</td>
<td>✓</td>
<td></td>
<td></td>
<td>✓</td>
</tr>
</tbody>
</table>

†only one chip is tested.
Figure 3.5.: Chip microphotograph showing the core circuit fabricated in AMS 0.18µm 1P4M CMOS technology.

Figure 3.6.: (a) Test setup for charge-metering with lumped elements; (b) Test setup for measure stimulation current with lumped elements; (c) Saline tank test setup; (d) in-vitro setup with extracted Xenopus sciatic nerve; and (e) differential probe equivalent input model from manufacture datasheet.

State-Philips) models. \( C_{dl} \) and \( R_s \) of the EEI model are set to 100 nF and 10 kΩ respectively, based on values modelled for a platinum electrode with a diameter of 430 µm [9].

The fabricated circuit (core) is shown in Fig. 3.5. \( C_{\text{unit}} \) are implemented using \( 10 \times 1 \) pF metal-insulator-metal (MIM) capacitors, each with a dimension of 22.2 µm \( \times \) 22.2 µm. The capacitor arrays are interleaved. One important point to note is that in the fabricated design, the target charge is hard-wired to 10 nC with the inter-phasic delay and stimulation voltage controlled externally.

Test configuration with RC EEI model is shown in Fig. 3.6(a). The measurements were taken from 7 randomly selected chips (within the same wafer/batch). \( V_{\text{Ref}} \) is 920 mV, which is the same as in the simulations. To calculate how much charge is delivered, a 8.2 Ω resistor (\( R_0 \)) is connected in series between \( V_{\text{stim}} \) and the chip. A differential probe (Lecroy AP034) is used so as to minimise the offset between the two channels of the oscilloscope (LeCroy WaveSurfer 434). This configuration is aimed to minimise the parasitic capacitance on the EEI model. Additional parasitic capacitance of printed circuit board (PCB) tracks have been removed by soldering the EEI model directly onto the pins of the chip. The remaining dominating parasitics are from the electrode (Fig. 3.6(e)) and chip package (around 1 pF). However, these do not affect the measurement of charge as they are not directly connected.
Figure 3.7.: Geometry of the cuff electrode used. Made by IMTEK, University of Freiburg. The surface is coated with platinum black. Reproduced from the IMTEK catalogue.

Therefore, the charge can be obtained by integrating the voltage across $R_0$ over time and divide by $8.2 \, \Omega$. To monitor the stimulation current more clearly, the probes are placed across the resistor ($10 \, \text{k}\Omega$) in the EEI model as shown in Fig. 3.6(b) to provide an increased signal-to-noise ratio. However, this introduces the capacitance of the probes to the stimulation path. Therefore, this configuration is not used to measure the charge.

In saline tank tests, two end-exposed platinum wire electrodes are used. The working electrode has a diameter of $200 \, \mu\text{m}$ while the counter electrode has a diameter of $1 \, \text{mm}$. Fig. 3.6(c) shows the configuration for saline tank test. The tank is shielded from interferences. Other setups are the same as the measurement using lumped elements, except $V_{\text{stim}}$ is $1 \, \text{V}$ as the impedance of the electrodes is lower than the $\text{RC}$ model.

The $\text{ex-vivo}$ experiment was conducted using $\text{Xenopus}$ sciatic nerve within 6 hours of its extraction. The setup is shown in Fig. 3.6(d). The stimulation and recording electrodes are both cuff electrode ($1 \, \text{mm}$ diameter) provided by IMTEK, University of Freiburg\(^1\) as shown in Fig. 3.7. The effective cathode area is $0.01 \, \text{cm}^2$ considering a surface factor of 2.53 for platinum black coating [10]. The extracted nerve was bathed in normal ringer solution within a tank which is enclosed by a Faraday cage which is connected to ground. The recording amplifier has been realised using off-the-shelf components and configured to have a total gain of 2000 with output bandwidth from 500 to 2000 Hz. It also provides an unfiltered output to confirm the genuine nerve response. As a reference point, a standard current stimulator with an amplitude of $500 \, \mu\text{A}$ is used.

3.2.5. Effects of electromagnetic interference, noise and drift

Other factors such as electromagnetic interference (EMI)/drift/noise will also affect the charge measurement. The EMI may cause a sudden voltage change on the electrode which

\(^1\)http://www.imtek.de/en
provides an extra path for the charge. Depending on whether the magnitude of the voltage interference is higher or lower than the solution voltage, the comparator will either flip more frequently or less frequently. This means the charge is not accurately measured. Therefore, in the tests presented in Section 3.2.4, the tank has been shielded to minimise external EMI. However, internal EMI caused by the switching activities (e.g. SW6 in Fig. 3.2) are not shielded. Although their amplitudes are limited by the power supply, they are expected to inject error during charge measurement. However, this effect is hard to quantify without modelling the whole chip using electromagnetic wave analysis software.

Unlike in neural recording, noise is not a concern for electric neural stimulation (ENS). But this will affect the resolution of charge measurement because the input of the comparator is connected to the electrode. According to [11], the noise power spectra density at 10 kHz is \( \sim 15 \text{nV}_{\text{RMS}}/\sqrt{\text{Hz}} \) for a platinum wire with an exposed area of \( \pi \times 38^2 \mu \text{m}^2 \). This can be used as a worst case estimation for the noise floor of the current system because the cathode area of the cuff electrode used is 10000 \( \mu \text{m}^2 \) which means a lower noise floor [12]. Thus, the worst case noise for an operational bandwidth from 0 to 10 MHz is about 47 \( \mu \text{V}_{\text{RMS}} \), corresponding to 0.47 fC RMS error with each 10 pC charge packet delivered which is negligible.

The drift of the electrode with respect to ground of the circuit can cause similar problems as the sudden interference. However, drift occurs at a larger time scale (seconds) than each stimulation (milliseconds), therefore the electrode potentials are reset to the circuit ground during each shorting phase.

3.3. Testing Results and Discussion

In this section, the results are provided along with discussion. Error analysis is presented for charge measurement. Limitations on temporal control and power efficiency are also discussed.

3.3.1. Charge metering & balancing

Simulation

The delivered and residual charge are calculated by integrating the stimulation current. Simulation results are shown in Table 2. For 10 nC target charge, which is the hard-wired setting for the fabricated chip, the delivered and residual charge is calculated to be 10.04 nC and -70.33 pC respectively. Note the difference in charge delivery increases with the target
charge quantities but reduces for the 10 nC run. This is caused by both the control loop delay and the charge accumulated on $C_{dl}$ in the EEI model as explained below.

Note that the results are simulation results obtained and presented with a resolution of 10 pC for charge delivery and 10 fC for residual charge. However, these are not necessarily the measurement accuracy as it is hard to make such accurate measurements within an environment full of noise and EMI. These resolutions are chosen to show what the capability of the circuits in an ideal environment. However, note that such 10 pC resolution may be an overkill for the requirements of neuroscientists. But this could provide neuroscientists tools to explore new fields with high accuracy stimulation charge control.

Because the digital circuits are clocked by the comparator output (comparison of the $V_{C_{unit}}$ and $V_{ref}$), it is essentially an asynchronous circuit and is therefore sensitive to timing. During the time from $V_{C_{unit}} = V_{ref}$ to the time the current path is steered away, extra charge is injected, as shown in Fig. 3.8. This also happens at the end of each phase (the circled portion in Fig. 3.8). This delay is caused by the offset of the comparator and the inherent delay in the system and introduces two errors.

The first is the difference between the target and actual quantities of charge delivered. In detail, without considering the error injected by EMI, unit charge comprises a fixed part set by $V_{ref}$ and a variable part set by the control loop delay ($\Delta t$) and stimulation current ($I_{stim}$) as well as the system offset (Fig. 3.9). The fixed part is given by

$$Q_{\text{Unit Charge, fixed}} = V_{\text{ref}} \times C_{\text{unit}}$$

while the variable part is given by

$$Q_{\text{Unit Charge, variable}} = (I_{\text{stim}} \times \Delta t) + (V_{\text{offset}} \times C_{\text{unit}})$$

Here, $\Delta t$ and $V_{\text{offset}}$ are only affected by the temperature of the system and process variation. They can be treated as fixed during the stimulation period (on a scale of 100 of $\mu$s. However,

$$I_{\text{stim}} = (V_{\text{stim}} - V_{C_e})/|Z_{\text{EEI}}|$$

where $V_{C_e}$ is the voltage on $C_{dl}$ and $|Z_{\text{EEI}}|$ is the time varying EEI impedance that is assumed to be constant within one stimulation cycle. Therefore, with $V_{C_e}$ increasing as the
Table 3.2: Simulated delivered and residual charges for different target charge stimulus. $V_{ref} = 920 \text{ mV}$

<table>
<thead>
<tr>
<th>Target Charge (nC)</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0.01</th>
</tr>
</thead>
<tbody>
<tr>
<td>Delivered Charge (nC)</td>
<td>10.04</td>
<td>9.072</td>
<td>8.067</td>
<td>7.061</td>
<td>6.054</td>
<td>5.047</td>
<td>4.039</td>
<td>3.031</td>
<td>2.021</td>
<td>1.011</td>
<td>0.0104</td>
</tr>
<tr>
<td>Residual Charge (pC)</td>
<td>-70.33</td>
<td>-56.91</td>
<td>-45.32</td>
<td>-34.25</td>
<td>-25.05</td>
<td>-17.25</td>
<td>-10.887</td>
<td>-5.94</td>
<td>-2.4</td>
<td>-0.3057</td>
<td>0.3011</td>
</tr>
<tr>
<td>Delivery Difference (nC)</td>
<td>0.04</td>
<td>0.072</td>
<td>0.067</td>
<td>0.061</td>
<td>0.054</td>
<td>0.047</td>
<td>0.039</td>
<td>0.031</td>
<td>0.021</td>
<td>0.11</td>
<td>0.0004</td>
</tr>
<tr>
<td>Delivery Error (%)</td>
<td>0.40</td>
<td>0.80</td>
<td>0.84</td>
<td>0.87</td>
<td>0.90</td>
<td>0.94</td>
<td>0.97</td>
<td>1.03</td>
<td>1.05</td>
<td>1.10</td>
<td>4</td>
</tr>
</tbody>
</table>
stimulation carries on and \( V_{\text{stim}} \) fixed, \( Q_{\text{Unit Charge}} \) decreases as shown in Fig. 3.9. Also note that here, an error \( \delta \) is defined:

\[
\delta = Q_{\text{Unit Charge}} - Q_{\text{Unit Charge, target}}
\]

(3.6)

where, \( Q_{\text{Unit Charge, target}} = 10 \, \text{pC} \) as designed. The accumulation of \( \delta \) introduces the charge delivery difference.

The second error is in the residual charge. This is a result of charge delivery difference between the stimulation and recycling phases. As identified in the above, the charge delivery difference depends on the initial value of \( V_{C_e} \). Since the initial values are different for the stimulation and recycle phases, the charge is not perfectly recycled.

For a positive \( \delta \) at the beginning of stimulation and a negative \( \delta \) at the end, the charge delivery difference will first increase and then decrease as observed in the simulation (delivery difference in Table 2).

To reduce the errors, the ideal solution is to design an adaptive system that can compensate any control loop delay rising from either tissue impedance changes or \( V_{C_e} \) changes. Such a system would give a \( \delta \) close to (but not equal to) zero. The predictive comparator [13] may be used for such a task. A simpler solution is to calibrate \( V_{\text{ref}} \) before stimulation.

A Monte-Carlo simulation was done for 10 nC target charge. The results for delivered and residual charge are shown Fig. 3.10. Although this shows a small variation, in practice, it is not the case as will be shown.

### Lumped element RC model test

The results are post processed to removed the direct current (DC) offset from the probe and shown in Fig. 3.11. The average charge delivered for the whole test is 10.96 nC which is higher than the simulation, which is the result of three factors.

Firstly, the absolute value of \( C_{\text{unit}} \) has a 10% error according to the manufacturer specification. Secondly, parasitic capacitance are added by the electrostatic discharge (ESD) protection and chip package. Thirdly, the overshoot error \( \delta \) is different from the simulation. The first two factors are process limitation while the third one can be tuned as the value of the RC EEI model is externally controlled. Considering only the first two factors, the actual \( C_{\text{unit}} \) is between 10.06 pF and 12.45 pF with a typical value of 11.3 pF based the layout dimensions and measured package pin capacitance. This means an error of ±10%. Therefore, any result between 10.06 pF and 12.45 pF is valid. Since this error is process
Figure 3.11: Measured results of 7 chips with RC EEI model and $V_{\text{ref}} = 920 \text{ mV}$, $V_{\text{stimulation}} = 1.8 \text{ V}$ for (a) the charge delivered; (b) the residue charge after active charge recycle. 100 measurements have been taken for each chip. The target charge is 10 nC. The box shows the interquartile range; with whiskers showing the minimum and maximum; and centre line showing the medium and central square is the average.
limited, it cannot be improved unless the capacitor can be built more accurately on chip or \( \delta \) is tuned to compensate after fabrication. The latter one can be done by changing \( V_{\text{ref}} \) or \( V_{\text{stim}} \). If assuming the mean charge delivered is tuned to 10 nC, the maximum measured spread of the charge delivered is 328.6 pC, corresponding to a delivery error of 3% which cannot be further reduced after fabrication.

The measured residue charge shows a mean value below 100 pC but a larger spread than the simulation. For 1 ms stimulation period, this translates to a mean DC error of 52.54 nA and maximum 290 nA using only active charge recycling. This is not safe for neural stimulation without further passive shorting phase. However, the result is comparable to the published active recycling systems without including their passive shorting phase as shown in Table 3.3. To reduce the DC error, the electrodes need to be shorted. The required shorting time depends on the impedance of the EEI. In this test, the time constant is \( \tau_{\text{short}} = 10 \, \text{k}\Omega \times 100 \, \text{nF} = 1 \, \text{ms} \). The shorting time required in this test for reaching a DC error of 25 nA is 0.77 \( \tau_{\text{short}} \) (maximum 4.27 \( \tau_{\text{short}} \) for a maximum 290 nA DC error).

Saline tank test

The results for the saline tank test is shown in Fig. 3.12. For charge delivery, the mean value is lower than the results using RC EEI model because \( V_{\text{stim}} \) is 1 V rather than 1.8 V. But, it presents a similar charge delivery error of 3.4% to that of using RC EEI model. The residue charge also gives similar results which has a mean DC current error of 77.19 nA and maximum 311 nA. This corresponds to a required shorting phase of 1.14 \( \tau_{\text{short}} \) (maximum 4.58 \( \tau_{\text{short}} \)) after active charge recycling.

Using the configuration in Fig. 3.6(b), the stimulation current is measured as shown in Fig. 3.13(d). Note that the envelope of the current seems to be constant. However, this “constant” envelope is made of very small ripples (Fig. 3.13(e)) that resemble the current waveform of constant voltage stimulations. The ripples are caused by switching between the two stimulation paths. A similar current profile can be found in [8].

Nevertheless, the neuron can still be stimulated as confirmed by both computer simulation using NEURON® [14] and ex-vivo setup shown later. NEURON® is a simulation environment for modelling individual neurons and networks of neurons. The simulated stimulation current is imported into the software and is modelled as a point source at 0.1 cm from fibre with no electrode model used. Fibre model consists only of \( N a^+ \), \( K^+ \) and leak currents with Hodgkin-Huxley (HH) model and axonal diameter = 36 um. Firstly, an ideal current stimulation is used to identify the model’s threshold. Then a DC offset is added to the recorded stimulation current to find out whether the neuron’s behaviour is affected by the ripple.

The results shown in Fig. 3.14 demonstrates that the ripple caused by the testing system do not affect the behaviour of the fibre model. For ideal current monopolar stimulus, the fibre has a threshold around 1.4 mA. Fig. 3.14(c) shows a constant current stimulus of 1.35 mA is not able to initiate an AP, but 1.4 mA can (Fig. 3.14(f)). The same property reserves while the simulated current stimulus is raised to these values (Fig. 3.14(a) and Fig. 3.14(d)). The reason is that the ripple has a much smaller time constant (90 ns) than
Figure 3.12: Measured results of 7 chips in the saline tank with platinum electrodes with $V_{ref} = 920 \text{ mV}, V_{stimulation} = 1 \text{ V}$ for (a) the charge delivered; (b) the residue charge after active recycle. 100 measurements have been taken for each chip. The target charge is 10 nC. The box shows the interquartile range; with whiskers shows the minimum and maximum; and centre line showing the median and central square is the average.
Figure 3.13: (a), (b) Single ended voltage on the two terminals of EEI model (c) Differential Voltage across the EEI model (derived from (a) and (b)); (d) Stimulation Current derived from the differential voltage across the resistor in the EEI model; (e) Detail of (d).
that required for sodium channel activation (100-200 µs) [15].

3.3.2. Ex-vivo test

The aim of the ex-vivo test is to demonstrate that the nerve can be successfully stimulated as predicted. A comparison between this work and a direct current stimulator with 500 µA amplitude, 500 µs pulse width and zero inter-phasic delay is shown in Fig. 3.15. The stimulator (based on Keithley 6221 AC and DC Current Source) and the response recording system (see appendix A.1) is designed and tested by Dr Amir Eftekhar in the group. The charge injected by the current stimulation is 250 nC giving a charge density of 9.88 µC/cm². The proposed system delivers 10 nC charge resulting in a charge density of 0.4 µC. Note that the two stimulation charge quantities differ by 25 times, however their charge densities are in the range for recruiting mainly the fast nerve fibres, Aα and Aβ, according to the experiments by [16]. The focus of this experiment is to verify the proposed stimulator can stimulate a nerve. More work needs to be done to see if there is a difference in stimulus threshold in comparison to the traditional current stimulation.

The conduction velocity of Aα and Aβ (large nerve fibre as identified in the experiment) is between 14~38 m/s [17]. Therefore, for 5 cm distance, the compound action potential composed of potentials from Aα and Aβ should be observed within 1.32~3.57 ms after stimulation. Fig. 3.15 confirms that both the current stimulator and the proposed stimulator recruit Aα and Aβ fibres. The large stimulation artefact here is a result of direct voltage stimulation. Therefore, the system is able to induce action potentials as predicted by the NEURON® package.

3.3.3. Temporal control

Temporal control of the stimulus is an important aspect of ENS as it affects the neural stimulation efficacy [18, 19]. In the presented system, the ability of temporal control is limited and empirical as the user has to change the stimulation voltage and check if the stimulation time meets the requirement. For example, in the saline tank test (Section 3.3.1), \( V_{\text{stim}} = 1 \) V is used to prolong the stimulation time.

The temporal resolution can be described as

\[
\text{Temporal Resolution} = \frac{V_{\text{ref}} \times C_{\text{unit}} \times Z(t)}{V_{\text{stim}}} \tag{3.7}
\]

where \( Z(t) \) is the time-varying impedance of the EEI interface. As a result, the temporal resolution improves with smaller \( V_{\text{ref}}, C_{\text{unit}} \) and \( Z(t) \). However, \( V_{\text{ref}} \) and \( C_{\text{unit}} \) are limited by the common mode voltage of the comparator and process variation respectively (Section 3.2.3). \( Z(t) \) complicates the equation by making it time dependant. Therefore, to make the temporal resolution more controllable, the charge can be set to be delivered discretely within a predefined period larger than is required. In this way, the temporal resolution becomes time-independent. Nevertheless, the present system can deliver asymmetric waveform by setting different stimulation voltage for charge/discharge phase.
Figure 3.14.: NEURON® simulation results comparing an ideal constant current monopolar stimulation with the current profile simulated using the charge-metering system. The ripple on the action potential illustrates the propagation of the action potential over time. Each trace represents the membrane voltage at a specific location on the fibre model.
3.3.4. Power efficiency

As introduced in Section 2.3.3, power consumption of a stimulator can be split into three portions and the Eq. 2.3 is reproduced here for convenience

\[ \eta = \frac{P_{\text{EEI}}}{P_{\text{Q}} + P_{\text{D}}} \]  

(3.8)

Where \( P_{\text{Q}} \) is the power measured from the system power supply which is 45 \( \mu \)W (averaged over the stimulation cycle, 220.5 \( \mu \)s). Note that \( P_{\text{D}} \) is calculated by averaging the integrated product of the current across the EEI model and the maximum voltage level recorded at the stimulation terminal over one stimulation cycle (the voltage across the EEI and \( C_{\text{unit}} \) but not \( SW_1 \) in Fig. 3.1). The result is 177.5 \( \mu \)W. Similarly, \( P_{\text{EEI}} \) is calculated by averaging the integrated product of the voltage and current across the EEI model over one stimulation cycle. The result is 94.23 \( \mu \)W. Therefore the power efficiency (\( \eta \)) is 42.35\% when delivering a 10 nC biphasic pulse. (If \( P_{\text{D}} \) includes the power consumed on the switches in the stimulation path. The result is 36.4\%.) This is the result of connecting a capacitor in the stimulation path for charge-metering. The voltage drop across this measuring capacitor cannot be avoided thus reducing the power efficiency.

For traditional current stimulators, the power efficiency is closely related to the stimulation current used. The voltage drop across the current sinking/sourcing transistor reduces with increased stimulation current when EEI impedance does not change. Therefore, the power efficiency increases. For example, with 1 V across the transistor using a 10V stimulation power supply, the efficiency is 90\%. However, if it is 7V across the transistor, the efficiency is 30\%. In comparison, the stimulator presented here has a fixed voltage drop which does not scale with the stimulation current. Also, the higher the stimulation voltage, the higher the efficiency. For a 10V supply, \( \sim 90\% \) efficiency can also be achieved.

However, compared to the other voltage stimulation system with charge metering capability, this 1 V voltage drop across the measuring capacitor is large. For example, the method proposed in [20, 21] only requires 200 mV drop across their measuring resistor. Therefore, the overall efficiency is \( \sim 95\% \) for a 10 k\( \Omega \) EEI impedance.
Table 3.3: Performance comparison with existing work assuming 1 ms stimulation period.

<table>
<thead>
<tr>
<th></th>
<th>This work&lt;sup&gt;a&lt;/sup&gt;</th>
<th>[22]</th>
<th>[23]</th>
<th>[21]&lt;sup&gt;b&lt;/sup&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC current error (nA)</td>
<td>77.19 (Max 311)</td>
<td>120</td>
<td>Not state, $\propto C_{dl}$</td>
<td>160</td>
</tr>
<tr>
<td>Stimulation mode</td>
<td>Voltage</td>
<td>Current</td>
<td>Current</td>
<td>Voltage</td>
</tr>
<tr>
<td>Full-scale Stimulus</td>
<td>-</td>
<td>10 mA</td>
<td>1 mA</td>
<td>-</td>
</tr>
<tr>
<td>Charge Delivery Error</td>
<td>5.2%</td>
<td>-</td>
<td>-</td>
<td>0.5%</td>
</tr>
<tr>
<td>Voltage Rails (V)</td>
<td>1.8</td>
<td>+6, -9</td>
<td>3.3, 22.5</td>
<td>1.8/3.3</td>
</tr>
<tr>
<td>Power</td>
<td>$45 \mu W$</td>
<td>$47 \mu W$</td>
<td>$198 \mu W$</td>
<td>$50 \mu W$</td>
</tr>
<tr>
<td>Technology</td>
<td>$0.18 \mu m$</td>
<td>$0.7 \mu m$ HV</td>
<td>$0.35 \mu m$ HV</td>
<td>$0.18 \mu m$</td>
</tr>
<tr>
<td>Area&lt;sup&gt;c&lt;/sup&gt;</td>
<td>0.037 mm$^2$</td>
<td>1.44 mm$^2$</td>
<td>0.15 mm$^2$</td>
<td>-</td>
</tr>
</tbody>
</table>

<sup>a</sup>Saline tank test  
<sup>b</sup>Simulated value  
<sup>c</sup>Core area of single channel only

3.3.5. Procedure of calibration

In order to use this system in practice, the reference voltage ($V_{\text{ref}}$) must be calibrated first following the procedure below:

1. Measure the EEI impedance and build a lumped element RC model to represent it.
2. Connect the stimulator as shown in Fig. 3.6 and set the target charge quantity.
3. Set $V_{\text{ref}}$ to 900 mV and capture one cycle of stimulation current using an oscilloscope.
4. Adjust the $V_{\text{stim}}$ to achieve required stimulation period. (The higher $V_{\text{stim}}$, the shorter the stimulation period.)
5. Run several stimulations and adjust $V_{\text{ref}}$ such that the total charge quantity calculated by integrating the stimulation current equals the required value.

In some cases, after calibrating $V_{\text{ref}}$, $V_{\text{stim}}$ needs to be re-adjusted slightly to meet the requirement on the stimulation period. Also note that if the EEI impedance is so low that $V_{\text{stim}}$ has to be very close to $V_{\text{ref}}$, a small resistor must be connected in series in the stimulation path to prolong the stimulation period. Otherwise, the stimulation efficiency is too low and operating frequency of the comparator is too high for proper operation. Also, $V_{\text{ref}}$ cannot be too low as it sets the operating point of the comparators.

3.4. Conclusion and Future Work

This chapter has presented a novel method for charge-balanced VMS using charge-metering with the first reported experimental results. The system architecture and circuit implementation have been presented with the key design considerations. The concept and system viability have been demonstrated through measured experimental results using the discrete RC EEI model and platinum electrodes within normal ringer solution as well as ex-vivo. The results show a max charge delivery error of 5.2% (on chip 3) with a typical DC current error of 77.19 nA for 1 ms stimulation period. The total power consumption is $45 \mu W$ with an efficiency around 36.4% with a stimulation power supply of 1.8 V. The core area is
110 \mu m \times 339 \mu m in a 0.18 \mu m CMOS technology. The circuit performance is compared to the state-of-the-art charge balancing and charge metering systems in Table 3.3.

Although the basic principle has been demonstrated, there are several limitations that need to be highlighted and require future work. As pointed out in the discussion (Section 3.3), the temporal controllability is limited. Users have to set the stimulation speed by tuning the stimulation voltage \(V_{\text{stim}}\) by trial and error in practice. In addition, because the voltage current across the capacitor used for charge metering is approximately 1 V, the power efficiency is limited even when the stimulation voltage is only slightly higher than 1 V (e.g. 1.8 V). Moreover, as one panel of the measuring capacitors \(C_{\text{unit}}\) is connected to a pad, the charge measurement is affected by any charge discharged from the environment, for example from EMI. In the end, the calibration is based on trial and error thus needs manual tuning and the tuning range of \(V_{\text{stim}}\) and \(V_{\text{ref}}\) are limited by the system speed and operating point of the comparators respectively.

These limitations point out the directions for future work. One is to reduce the process limited error by introducing on-chip calibration. This will also eliminate the requirement of manual calibration before use. Another direction for improvement would be to reduce the static power consumption (currently is about 60% of the total power consumption). In addition, it is also useful to extend the common mode input range of the comparator so as to extend the tuning range of \(V_{\text{ref}}\).
Bibliography


4. Multichannel Programmable Electrical Neural Stimulation Platform

4.1. Introduction

As mentioned previously, a key requirement for a next generation electric neural stimulation (ENS) system is a multichannel operation. This will provide simultaneous access to multineurons, thus enabling coordinate stimulation of neurons. This type of stimulation is core to the complex study of neuron behaviour. Such systems need to also be programmable to allow researchers to investigate how these neurons respond to different stimulation parameters.

Fig. 4.1 shows the idea of the proposed system. The stimulator integrated circuits (ICs) are connected in series on a printed circuit board (PCB) under the commands of a field-programmable gate array (FPGA) or microprocessor which receives commands from the computer via USB connection. The required low voltage and high voltage power supplies are also provided via USB by a discrete DC-DC converter. Each stimulation channel can be individually configured and controlled. Therefore, it can support mono-, bi- or multipolar stimulation. Inside each channel, it could be configured to three different stimulation modalities: current mode stimulation (CMS), voltage mode stimulation (VMS) and charge mode stimulation (QMS). The stimulation waveform and the target quantity of charge delivery can be user programmed.

Figure 4.1.: Concept of envisaged multichannel stimulation system
4.2. System Architecture

Based on the conceptual system, the detail block diagram of the implemented system is shown in Fig. 4.2. This system comprises 8 stimulation channels and distribution systems for analogue biasing, clock, data and command. The system operates on two pairs of balanced (split) voltage supplies: ±1.65 V for low voltage circuits (both analogue and digital), and ±10 V for current and voltage mode stimulation. The Hamming(27,21) encoded data is input via the serial port and used for control and programming. All inputs are synchronised via a 1 MHz external clock.

Each stimulation channel has a local finite state machine (FSM) so that it can be independently addressed and controlled. The FSM has access to in-channel 16×16 bits static random-access memory (RAM) which stores the waveform for voltage and/or current stimulation. The control parameters for the charge stimulation and other settings, however, are stored within the FSM. The FSM controls a 5-bit current steering binary weighted digital-to-analogue converter (DAC) that plays back the stored waveform and supplies the threshold voltage ($V_{th}$) for charge stimulation. A current buffer and voltage buffer are implemented to provide voltage compliance in current mode and current driving ability in voltage mode respectively. A water window comparator is also included to detect the charge imbalance after long-term stimulation to ensure safety. Depending on the configuration of stimulation: monopolar, bipolar or multipolar, the input of comparator is adjusted accordingly.

4.3. Implementation

4.3.1. Voltage and current stimulation

The main components for the voltage- and current-mode stimulation are a DAC, a current and a voltage buffer. Designs are detailed below.

Digital-to-analogue converter

A DAC is used to generate the stimulation waveform with specifications derived from the stimulation requirements. For intraspinal microstimulation (ISMS), there is no need for mA current ranges. Based on previously reported systems for spinal cord stimulation (see Chapter 2), the range has been set to $-511 \mu A$ to $512 \mu A$. The resolution of the DAC is 5-bit. Another 2 bits are used to select between 4 different current output ranges: $-63 \mu A$ to $64 \mu A$, $-127 \mu A$ to $128 \mu A$, $-255 \mu A$ to $256 \mu A$, $-511 \mu A$ to $512 \mu A$. Another 1 bit is used to set the output polarity. The temporal resolution of the DAC is designed to be 1 µs but can be changed by adjusting the clock frequency.

A current steering DAC (schematic shown in Fig. 4.3.) is chosen so that it can be easily buffered as a current output. This uses a binary-weighted structure (instead of unary coding) for less area, power and complexity. However, this must be designed carefully to ensure monotonicity and reduce glitches and nonlinearity. All unused terminals at the output are connected to either VSS or GND.
Figure 4.2: Block diagram of multichannel programmable electrical neural stimulation platform. The blocks contain bugs in the first tapeout are highlighted in red.
Figure 4.3.: Schematic for 5-bit binary-weighted current steering DAC

All the switches are designed to minimise the voltage drop while the charge injection is mediated by using dummy metal-oxide-semiconductor capacitors (MOSCAPs) (i.e. half sizes transistors) at the drain and source controlled by complimentary clock phases (Fig. 4.4).

Figure 4.4.: Schematic for switch used in DAC. Two of this make a single-pole-double-throw switch.

**Current buffer**

A current buffer is used to increase the output current level while increasing the voltage compliance to ±10 V. This has a 2-bit control, ranging from 10x to 40x scaling. In the schematic shown in Fig. 4.5, the high voltage transistors used at the input and biasing are placed to protect the low voltage transistors from the DAC. The cascoded transistors at the output are to ensure high output voltage swing. To ensure better current mirror matching, each mirror branch is cascoded, in addition to careful selection of device sizing to provide similar V$_{DS}$ on the low voltage mirrors.

In order for smooth transition between current levels when the scaling is not changing, any current dumped from the DAC should be ideally interfaced to the same impedance as the output branch. This is achieved by the input cascoding protection high voltage (HV) transistor and the diode connected transistor.

**Transimpedance amplifier**

This converts the output current from the DAC using a polysilicon resistor in the feedback loop. The schematic is shown in Fig. 4.6. The output can source/sink 0.5 mA with a static power consumption of 613 $\mu$W (6.13% the peak output). Most of the static power is consumed on the branches using a 20 V power supply (539.4 $\mu$W).

The design of the transimpedance amplifier is adapted from low-voltage super class AB CMOS OTA cells [1]. However, changes have been made such that it can accept a low voltage input signal and convert to a high output voltage domain.
Figure 4.5.: Current buffer with scaling output for stimulation.

The input terminals are thin oxide 20V drain voltage devices adaptively biased by flipped voltage follower in the low voltage domain. The resistor at the bottom provides the dynamic gain during amplification. Note that the sizes of the transistors on the two high voltage branches are different such that the static current through the non-output branch is limited to around 100 nA. Such configurations, however, increase the system mismatch at the drain of the two NMOS middle oxide transistors.

4.3.2. Charge stimulation

In charge-mode stimulation, the design from Chapter 3 has been modified so as to support multichannel stimulation. As shown in Fig 4.7, the charge metering is now performed from the stimulating side other than the receiving side. Switches S1–S4 are controlled by the stimulation FSM based on the results of Comp_C1 and Comp_C2. They operate in a complementary fashion. Switch S0 determines the polarity of the charge stimulation. S5 and S6 are used for calibrating the comparison threshold. Because C1 and C2 are interlaced in layout, only C1 is used during calibration, so that S6 actually shorts C2, and Comp_C2 is not valid.

A similar type of stimulation is switched capacitor (SC) stimulation, but there is a major difference. In SC stimulation, the total charge is set using a discrete capacitor and an one-off charging voltage, with the charge transfer being incomplete. Here, the capacitor is charged repetitively and the charge-transfer is divided into packets.

Here, the output of the DAC is converted to voltage via resistors and a current mirror to provide comparison threshold voltages for positive and negative charge stimulation. Fig. 4.8
shows the circuit schematic. T1 and T2 are selected when the voltage is recycled from the tissue (unit capacitors, C1 and C2, are positively charged) and delivered (unit capacitors are negatively charged) to the tissue respectively. This tunable threshold voltage is essential for calibration so that the overshooting due to the control loop delay can be mitigated.

**Figure 4.6.** Class AB voltage buffer.

**Figure 4.7.** Charge delivery using the same idea developed of charge-metering

All the three outputs from current, voltage and charge modules are multiplexed to the output as shown in Fig. 4.2.

### 4.3.3. Calibration

The aim of calibration is to compensate the over-delivered charge due to the control loop delay as described in Section 3.2.3. Calibration is achieved by sweeping the comparison threshold $V_{th}$ in Fig. 4.7 and sampling the voltage on C1 via S5 at the moment of switching from unit capacitor discharging to charging. C2 on the other hand is always shorted by S6. In order to avoid using an additional ADC solely for calibration, six comparators have been used to inform the FSM the position of the sampled threshold voltage. The schematic
Figure 4.8.: Schematic for circuitry used for generating comparison threshold for charge mode stimulation (T1 are selected when generating threshold for negative phase; T2 for positive phase)

Figure 4.9.: (a) Schematic of the calibration circuit. (b) Calibration data output and its corresponding sampled threshold voltage.

Figure 4.10.: Flowchart of calibration. Cal_data[5:0] is shown as the transition condition. “Pos” means calibration for positive phase; “Neg” means calibration for negative phase.
is shown in Fig. 4.9. The default calibration process targets 1.5 V drop across the unit capacitors, but it can be overwritten using externally provided calibration voltages.

The decision process is shown in Fig. 4.10. For example, the default process is as follows: the initial threshold voltage is set up via a setup command and will be close to the charge delivery voltage – 0 V for negative phase, 3.3 V for positive phase. Then the real $V_{th}$ at the moment of switching is sampled by the comparators. Then 3 different situations will happen.

1. $1.8 V < V_{th} < 1.805 V$ for positive phase, $1.495 V < V_{th} < 1.5 V$ for negative phase.
   The sampled $V_{th}$ is closer to the ideal range (see 2nd situation below) and keeps increasing $V_{th}$.

2. $1.795 V < V_{th} < 1.8 V$ for positive phase, $1.5 V < V_{th} < 1.505 V$ for negative phase.
   The sampled $V_{th}$ is in the ideal range so that the calibration ends and the value of $V_{th}$ is saved.

3. $1.505 V < V_{th} < 1.795 V$ for either positive or negative phase.
   The sampled $V_{th}$ is outside the ideal range so that $V_{th}$ is decreased by one step to put it back to the situation close to the ideal range (1st situation).

Note that the initial $V_{th}$ cannot be too large, otherwise the sampled $V_{th}$ will be in the range of 1.505 V–1.795 V. This will cause the FSM to issue a calibration error.

4.3.4. Charge imbalance monitor

This is used to compare the residue voltage across the stimulation and returning electrode within a predefined water window, which is $-0.6 V$ to $0.8 V$ after each stimulation cycle. In monopolar stimulation, the returning electrode is the reference electrode. The mid-rail voltage (GND) is always connected to the reference electrode in this case so that stimulation can happen within the correct range. In multipolar stimulation, the working electrode for comparison is the reference electrode while the returning electrode is actually the potential at half of the battery. This is because in multipolar stimulation, the working electrodes are shorting to one another in addition to the reference electrode. Therefore, if there is any imbalance after shorting, the reference electrode, which is at the same potential as the fluid would drift away from the mid-point of the battery where it was initially. Once the drifting exceeds the water window, the stimulation is stopped.

4.3.5. Digital control logic

All the digital control logic is implemented using Verilog (full code and state flow chart in appendix A.2). On the top level, the incoming data stream is first verified and decoded. Then the data are parallely loaded onto the address and data bus which the local FSM inside each channel continuously monitors.

The local FSM consists of two parts: the first part is in charge of monitoring the bus and configuring each channel. Once the configuration is done and the stimulation start
command is received, a dedicated module for stimulation will take control and it can only be interrupted during the shorting phase. Also this makes the code more hierarchical.

![General Data Format Diagram](image)

**TYPE 1. Commands:**

Address / Command

<table>
<thead>
<tr>
<th>20</th>
<th>15</th>
<th>10</th>
<th>5</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Command</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type 1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Channel Flag Bits</th>
</tr>
</thead>
<tbody>
<tr>
<td>(0 - inactive, 1-active)</td>
</tr>
</tbody>
</table>

**TYPE 2. Data:**

<table>
<thead>
<tr>
<th>Address / Command</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
</tr>
<tr>
<td>0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Type 2</th>
</tr>
</thead>
</table>

**Cmd/Data Identifier**

(16-bit, allows maximum charge-mode stimulation of $64\text{nC}$ at a resolution of $10\text{pC}$)

**Address / Command**

20 15 10 5 0

**Command**

0 - inactive, 1-active

**Calibration:**

<table>
<thead>
<tr>
<th>NIU</th>
<th>Positive Threshold</th>
<th>Negative Threshold</th>
<th>NIU</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td></td>
<td></td>
<td>0</td>
</tr>
</tbody>
</table>

**Figure 4.11:** Data format of the 21-bit input serial data. Type 1 is for commands and type 2 is for data.

The formats of input data are listed in Fig. 4.11. The input data frame is 21-bit long and sorted into two types indicated by the most significant bit (MSB). The first type is commands where the MSB is ‘1’. The next 4-bit is a command identifier with the following 16-bit flags indicating which channel should accept this command. The available commands are shown in Table. 4.1.

Depending on the commands received, the selected channel will receive further setup for the chosen stimulation type. The local FSM will monitor the address field (bit 19 to 16) of TYPE 2 input and looking for a match. In current/voltage stimulation, the amplitude of each 16 stored data point is set first. Then the timing information is set including total repetition number and the duration of the shorting phase. The interphasic delay (IPD) is achieved by user-customised programming. For charge mode stimulation, the target charge quantity and duration of the IPD is set within one command. The timing setup command is the same as for the current/voltage stimulation mode. For calibration, it is channel independent and sets the initial positive and negative comparison threshold.

### 4.3.6. Top level support circuitry

The functions of the top level supporting circuitry are to distribute bias currents and voltages as well as multiplexing the error outputs from each channel. The bias currents are
Table 4.1.: Command list for controlling each channel

<table>
<thead>
<tr>
<th>bit 19-16</th>
<th>commands</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 0 0</td>
<td>IDLE</td>
</tr>
<tr>
<td>0 0 0 1</td>
<td>Not in use</td>
</tr>
<tr>
<td>0 0 1 0</td>
<td>Not in use</td>
</tr>
<tr>
<td>0 0 1 1</td>
<td>Not in use</td>
</tr>
<tr>
<td>0 1 0 0</td>
<td>Not in use</td>
</tr>
<tr>
<td>0 1 0 1</td>
<td>Current stimulation with active charge recycling</td>
</tr>
<tr>
<td>0 1 1 0</td>
<td>Voltage stimulation with active charge recycling</td>
</tr>
<tr>
<td>0 1 1 1</td>
<td>Charge stimulation with active charge recycling</td>
</tr>
<tr>
<td>1 0 0 0</td>
<td>Calibration</td>
</tr>
<tr>
<td>1 0 0 1</td>
<td>Current stimulation with passive charge recycling</td>
</tr>
<tr>
<td>1 0 1 0</td>
<td>Voltage stimulation with passive charge recycling</td>
</tr>
<tr>
<td>1 0 1 1</td>
<td>Charge stimulation with passive charge recycling</td>
</tr>
<tr>
<td>1 1 0 0</td>
<td>Start stimulation</td>
</tr>
<tr>
<td>1 1 0 1</td>
<td>Stop stimulation</td>
</tr>
<tr>
<td>1 1 1 0</td>
<td>Low impedance</td>
</tr>
<tr>
<td>1 1 1 1</td>
<td>Reset</td>
</tr>
</tbody>
</table>

distributed to each channel using cascode current mirrors. The bias voltages can be generated internally using resistor chains or provided externally. These are mainly used for the comparators during charge mode stimulation, calibration and charge imbalance monitoring. The inputs of error multiplexing module from each channel are error flags indicating malfunction during channel setup, stimulation or calibration. To reduce the pin count, only one pin is used for error indication with 3 pins for channel selection and 2 pins for error type selection.

### 4.4. Test Results and Discussion

![Micro-photograph of the stimulator fabricated using 0.35µm HV CMOS process](image)

Figure 4.12.: Micro-photograph of the stimulator fabricated using 0.35µm HV CMOS process
The application-specific integrated circuit (ASIC) is fabricated using AMS 0.35 \( \mu m \) HV process (Fig. 4.12) including 8 channels. The total area is 3.2 mm \( \times \) 3.4 mm\(^1\). It is the first and only tapeout of the system which contains several bugs as highlighted in red in Fig. 4.2. These bugs affect the testability of the system although some of them can be fixed temporally. Below is a list with the temporary fixing methods:

1. The hamming code decoder has one bit mistakenly flipped in the code during decoding. This is temporally fixed by manually injecting an error bit so that the hamming code will do auto correction and output the correct information.

2. Serial in parallel output (SIPO) holds its output value whilst reading the serial input, rather than giving an idle pattern, which causes FSM to be programmed wrongly. This is also temporally fixed by changing the communication protocol between the FPGA and the chip.

3. The last data point of the programmed waveform that is stored on-chip cannot be programmed because the FSM directly proceed to timing setup after programming the last second data point.

4. The waveform generation part of the FSM does not hold the polarity and scale of the current data point as it does for the amplitude, so that whenever the polarity or scale need to be changed, the duration of the last data point has to be 1 \( \mu s \).

5. The polarity of one switch controlling the switching between monopolar stimulation and multipolar stimulation are swapped, causing the mid-rail supply (1.65 V) to be always shorted to the reference electrode during multipolar stimulation. This prevents the testing of the charge imbalance monitor during multipolar stimulation.

6. The control signal of the switch pair (S1 – S3, S2 – S4 in Fig. 4.7) overlaps as a result of digital synthesis without timing constraints. Therefore, the stimulation may stop because of a possible short between the reference electrode and stimulation supply during the stimulation. It also prevents proper threshold calibration.

The general test setup is shown in Fig. 4.13. Bias currents and power supplies are provided by Keithley 2602 and Agilent N6705. The chip is configured and controlled via FPGA while time domain measurement is captured by an oscilloscope. The measurement is automated using MATLAB. Note that the centre of the supply rails is 1.65 V rather than 0 V because the logic level from the FPGA is 0–3.3 V.

There are 11 packaged ICs available, that have all been tested to establish the impact of process variation and thus yield. The tested samples are summarised in Table 4.2

During these tests, the reference electrode is always connected to the mid-rail supply (1.65 V) unless otherwise stated. All channels are programmed at the same time but tested individually. Idle channels receive all the setup data except for the start stimulation command.

\(^1\)The right portion of the design in Fig. 4.12 contains unrelated test circuits.
4.4.1. Current mode stimulation

The main target of this test is to evaluate performance of the 5-bit current steering DACs. The output current is measured using a 9089.8 Ω resistor connected between the output terminal and the reference electrode terminal which is shorted to 1.65 V. The waveform generated is averaged over 100 trials before being stored and then used to evaluate non-linearity. The integral nonlinearity (INL) and differential nonlinearity (DNL) are defined in Eq. 4.1

\[
\text{DNL}_i = \frac{I_{out,i+1} - I_{out,i} - I_{\text{ideal},\text{LSB}}}{I_{\text{ideal},\text{LSB}}} \quad (4.1)
\]

\[
\text{INL} = \max_i \left( \frac{I_{out,i} - I_{out,0} - I_{\text{linear},i}}{I_{\text{ideal},\text{LSB}}} \right) \quad (4.2)
\]

\[
I_{\text{linear},i} = i \cdot \frac{I_{out,N} - I_{out,0}}{N} \quad (4.3)
\]

where \( N = 2^{\text{total number of bits}} \). The full results of DNL is presented in Appendix A.4. To summarise the findings, all tested channels are monotonic except channel 5 on chip 7 which shows a DNL of -1.121 LSB during sinking current at MSB of input code switches. The INL results are shown in Table 4.3 and Table 4.4 and deviation at each input code can be found in Appendix A.4. Note that the definition of INL represents end-of-point non-linearity that excludes gain-error and offset-error that can be potentially calibrated if required. It is shown that channel 5 on chip 7 shows the biggest INL and channel 7 on chip 4 shows the lowest.

\^2\text{Measured with RCL meter, FLUKE PM6303A at room temperature around 23 degree. The last digit is not accurate as the resistor has a temperature coefficient of ±50 ppm.}
The transient properties have been evaluated with a resistor-capacitor (RC) electrode-electrolyte interface (EEI) model with $R = 10 \, \text{k}\Omega$ and $C = 470 \, \text{nF}$. The stimulation channel is programmed so that each waveform data point has a minimum duration (1 $\mu$s) with full scale change. In Fig. 4.14, it can be seen that the full scale step can be generated within 1 $\mu$s with a little overshoot when entering charge recycling. This 1 $\mu$s response also holds for other RC values provided that the output transistor of the current source/sink does not enter the linear region.
4.4.2. Voltage mode stimulation

When evaluating the voltage buffer, the output terminal is loaded by a 20Ω resistor to directly provide the maximum current at the maximum output voltage. Following the definition of INL and DNL in Eq. 4.1, the results on INL for the voltage stimulation of the negative phase is summarised in Table 4.5, and more details on each channel can be found in Appendix A.7.

Considering that the DAC is also used in CMS, the linearity error should be similar to that reported in Section 4.4.1. The end-of-point DNL and INL are still bounded within ±1 LSB. Note that the worst INL is still from channel 5 on chip 7. However it is observed that channel 7 on chip 4 does not give the smallest value although it is still a relatively smaller value compared to the average. This difference originates from the extra distortion of the transimpedance amplifier.

<table>
<thead>
<tr>
<th>Chip 1</th>
<th>Ch. 2</th>
<th>Ch. 3</th>
<th>Ch. 4</th>
<th>Ch. 5</th>
<th>Ch. 6</th>
<th>Ch. 7</th>
<th>Ch. 8</th>
</tr>
</thead>
<tbody>
<tr>
<td>-0.25</td>
<td>-0.49</td>
<td>-0.33</td>
<td>-0.25</td>
<td>-0.34</td>
<td>-0.19</td>
<td>-0.15</td>
<td>0.30</td>
</tr>
<tr>
<td>-0.27</td>
<td>-0.22</td>
<td>-0.31</td>
<td>-0.33</td>
<td>0.24</td>
<td>-0.31</td>
<td>-0.47</td>
<td>-0.19</td>
</tr>
<tr>
<td>-0.14</td>
<td>0.13</td>
<td>-0.39</td>
<td>-0.36</td>
<td>-0.30</td>
<td>-0.41</td>
<td>-0.21</td>
<td>-0.36</td>
</tr>
<tr>
<td>-0.27</td>
<td>-0.31</td>
<td>-0.42</td>
<td>-0.40</td>
<td>-0.26</td>
<td>-0.37</td>
<td>-0.31</td>
<td>-0.42</td>
</tr>
<tr>
<td>-0.17</td>
<td>-0.39</td>
<td>-0.31</td>
<td>-0.47</td>
<td>-0.34</td>
<td>-0.47</td>
<td>-0.40</td>
<td>-0.36</td>
</tr>
<tr>
<td>-0.36</td>
<td>-0.47</td>
<td>0.17</td>
<td>-0.46</td>
<td>-0.57</td>
<td>-0.35</td>
<td>-0.22</td>
<td>-0.39</td>
</tr>
<tr>
<td>-0.32</td>
<td>-0.34</td>
<td>-0.45</td>
<td>-0.26</td>
<td>-0.36</td>
<td>-0.31</td>
<td>-0.40</td>
<td>0.45</td>
</tr>
<tr>
<td>-0.41</td>
<td>-0.44</td>
<td>-0.38</td>
<td>-0.39</td>
<td>-0.40</td>
<td>-0.30</td>
<td>-0.34</td>
<td>-0.44</td>
</tr>
<tr>
<td>-0.24</td>
<td>-0.27</td>
<td>-0.19</td>
<td>-0.33</td>
<td>-0.36</td>
<td>-0.44</td>
<td>-0.31</td>
<td>-0.40</td>
</tr>
<tr>
<td>-0.40</td>
<td>-0.30</td>
<td>-0.32</td>
<td>-0.39</td>
<td>-0.18</td>
<td>-0.35</td>
<td>-0.40</td>
<td>-0.25</td>
</tr>
</tbody>
</table>

4.4.3. Charge mode stimulation

Using lumped elements

![EEI model](image)

Figure 4.15.: EEI model used during charge mode stimulation, the differential probe is connected monopolar side to measure the current

During charge stimulation, EEI model comprises a capacitor and 3 resistors on each side (Fig. 4.15). The resistor values are chosen based on reported platinum electrodes value [2]. The capacitor value may not be realistic for microelectrode but used here to make sure the maximum charge delivery will not introduce significant voltage build-up even with the maximum target charge delivered. Terminal “Ref” is connected to the middle of the supply. Terminal “Ex” is connected to the output of the stimulator (x = 1..8). The differential probe is connected on to the two terminals of R1 to measure the stimulation current. The probe cannot be connected at another node as the input capacitance of the probe will introduce
Figure 4.16: Charge delivery measured on channel 8 across chips 1,2,4,6,7,8,9,10, the dash line represents the ideal case (Charge delivered = Target Charge).

extra paths for the stimulation current which is picked up by the probe. While one terminal is tied to "Ref", the current input capacitances and leakage path via input resistance are limited to only one probe terminal.

The programme cycles the target charge from 20 pC to 16.384 nC in passive charge stimulation mode without calibration. Fig. 4.16 shows the measured charge delivery on channel 8 for all measured chips. The actual charge delivered is always above the ideal line and does not deviate too much. Average charge delivery error can be calculated as:

$$\frac{1}{20\,\text{pC} \leq Q_{\text{target},n} \leq 16384\,\text{pC}} \sum Q_{\text{delivery},n} - Q_{\text{target},n}$$  \hspace{1cm} (4.4)

The results are given in Table 4.6. This shows that the maximum charge delivery error can be up to 23.20% (channel 8 of chip 6). However that is associated with a charge delivery of 30 pC in which case a small absolute error gives a large relative error in percentage. Actually, the average error even on channel 8 of chip 6 is still comparable to the other chips. The average error of all channel 8 on all the measured chips is between 5.05% and 10.42%. This result is comparable to the reported value in Figure 3.11(a) in Chapter 3 where the charge delivery is also uncalibrated.

<table>
<thead>
<tr>
<th>Chip No.</th>
<th>1</th>
<th>2</th>
<th>4</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
<th>10</th>
</tr>
</thead>
<tbody>
<tr>
<td>Average error(%)</td>
<td>7.97</td>
<td>5.79</td>
<td>9.43</td>
<td>10.42</td>
<td>7.16</td>
<td>10.12</td>
<td>7.16</td>
<td>5.12</td>
</tr>
<tr>
<td>Max Error(%)</td>
<td>9.72</td>
<td>7.40</td>
<td>23.20</td>
<td>16.20</td>
<td>11.36</td>
<td>17.32</td>
<td>6.41</td>
<td>12.57</td>
</tr>
<tr>
<td>Target Charge(nC)</td>
<td>82.93</td>
<td>82.85</td>
<td>0.03</td>
<td>0.03</td>
<td>0.08</td>
<td>0.02</td>
<td>1.68</td>
<td>0.02</td>
</tr>
</tbody>
</table>

The charge delivery of all 8 channels on chip 2 and 9 is characterised as representative examples. The results are shown in Fig. 4.17 and Fig. 4.18 and are as expected. The average and maximum charge delivery errors are also presented in Tables 4.7 and 4.8. The smaller target charge still tends to give a large relative error. The average error is still below 10.42% as reported on channel 8 of chip 6. Without an exhaustive test, it is inconclusive as
to whether 10.42% is the maximum percentage error, but it would be a typical value.

Figure 4.17.: Charge delivery measured across 8 channels on chip number 2, the dash line represents the ideal case

Figure 4.18.: Charge delivery measured across 8 channel on chip number 9, the dash line represents the ideal case

Table 4.7.: Average and maximum charge delivery error with corresponding target charge measured on all the channels on chip 2 without calibration

<table>
<thead>
<tr>
<th>Channel No.</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
</tr>
</thead>
<tbody>
<tr>
<td>Average error(%)</td>
<td>7.88</td>
<td>7.62</td>
<td>6.96</td>
<td>2.37</td>
<td>7.90</td>
<td>3.26</td>
<td>3.78</td>
<td>5.79</td>
</tr>
<tr>
<td>Max Error(%)</td>
<td>9.49</td>
<td>15.19</td>
<td>12.13</td>
<td>4.65</td>
<td>9.18</td>
<td>5.24</td>
<td>8.78</td>
<td>7.48</td>
</tr>
<tr>
<td>Target Charge(nC)</td>
<td>47.40</td>
<td>4.82</td>
<td>0.06</td>
<td>0.10</td>
<td>89.70</td>
<td>0.15</td>
<td>0.06</td>
<td>82.85</td>
</tr>
</tbody>
</table>

The residue charge (after stimulation before shorting) is also measured with results shown in Fig. 4.19. The average and maximum errors are shown in Table 4.9. The average residue charge error has a similar definition as average charge delivery error:

\[
\sum_{20 \text{pC} \leq Q_{\text{target},n} \leq 16384 \text{pC}} \frac{Q_{\text{residue},n}}{Q_{\text{target},n}}
\] (4.5)

For channel 8 on all measured chips, the residue charge before passive shorting is bounded within 13 nC. The average error as a percentage is within 8.34%. For maximum error in percentage, it is obvious that smaller target charge tends to give a bigger error in percentage.
Table 4.8: Average and maximum charge delivery error with corresponding target charge measured on all the channels on chip 9 without calibration

<table>
<thead>
<tr>
<th>Channel No.</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
</tr>
</thead>
<tbody>
<tr>
<td>Average error(%)</td>
<td>5.34</td>
<td>3.86</td>
<td>4.50</td>
<td>4.81</td>
<td>8.15</td>
<td>1.84</td>
<td>2.52</td>
<td>5.12</td>
</tr>
<tr>
<td>Max Error(%)</td>
<td>6.05</td>
<td>4.40</td>
<td>5.44</td>
<td>5.53</td>
<td>11.09</td>
<td>3.23</td>
<td>3.50</td>
<td>6.41</td>
</tr>
<tr>
<td>Target Charge(nC)</td>
<td>83.95</td>
<td>39.68</td>
<td>52.30</td>
<td>0.28</td>
<td>4.27</td>
<td>95.04</td>
<td>48.20</td>
<td>1.68</td>
</tr>
</tbody>
</table>

Figure 4.19: Residue charge measured on channel 8 across chips number 1,2,4,6,7,8,9,10.

Table 4.9: Average and maximum residue charge error with corresponding target charge measured on channel 8 across chips 1,2,4,6,7,8,9,10 without calibration

<table>
<thead>
<tr>
<th>Chip No.</th>
<th>1</th>
<th>2</th>
<th>4</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
<th>10</th>
</tr>
</thead>
<tbody>
<tr>
<td>Average error(%)</td>
<td>-3.32</td>
<td>-3.14</td>
<td>7.16</td>
<td>8.34</td>
<td>5.00</td>
<td>-4.45</td>
<td>3.50</td>
<td>3.54</td>
</tr>
<tr>
<td>Max Error(%)</td>
<td>-10.65</td>
<td>-5.78</td>
<td>25.58</td>
<td>11.22</td>
<td>25.50</td>
<td>15.54</td>
<td>19.40</td>
<td>34.59</td>
</tr>
<tr>
<td>Target Charge(nC)</td>
<td>0.03</td>
<td>2.29</td>
<td>0.03</td>
<td>0.03</td>
<td>0.08</td>
<td>0.02</td>
<td>0.03</td>
<td>0.02</td>
</tr>
</tbody>
</table>
Chips 2 and 9 are again measured to characterise different channels on a single chip. The results are shown in Fig. 4.20 and Fig. 4.21. The average and maximum residue charge errors are shown in Table 4.10 and Table 4.11. Note that channel 5 on chip 2 malfunctioned as the charge recycling phase is always shorter than the charge delivery phase (shown in Fig. 4.22). There could be two reasons for this. Firstly, $V_{th}$ for the recycling phase could be quite different from that for charge delivery. Secondly, the FSM controlling the system does not function as expected.

![Figure 4.20: Residue charge measured across all 8 channels on chip number 2](image1)

![Figure 4.21: Residue charge measured across all 8 channels on chip number 9](image2)

<table>
<thead>
<tr>
<th>Channel No.</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
</tr>
</thead>
<tbody>
<tr>
<td>Average error(%)</td>
<td>7.41</td>
<td>4.21</td>
<td>7.83</td>
<td>1.28</td>
<td>30.07</td>
<td>0.29</td>
<td>0.70</td>
<td>-3.14</td>
</tr>
<tr>
<td>Max Error(%)</td>
<td>15.45</td>
<td>15.31</td>
<td>21.87</td>
<td>32.72</td>
<td>40.56</td>
<td>-12.86</td>
<td>18.67</td>
<td>-5.78</td>
</tr>
<tr>
<td>Target Charge(nC)</td>
<td>0.04</td>
<td>4.82</td>
<td>0.06</td>
<td>0.58</td>
<td>8.47</td>
<td>0.15</td>
<td>0.04</td>
<td>2.29</td>
</tr>
</tbody>
</table>

Table 4.10.: Average and maximum residue charge error with corresponding target charge measured on all the channels on chip 2 without calibration

Considering the digital circuitry is more prone to process variations if not all process corners are simulated (which unfortunately is the case here), FSM should be the cause
Table 4.11.: Average and maximum residue charge error with corresponding target charge measured on all the channels on chip 9 without calibration

<table>
<thead>
<tr>
<th>Channel No.</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
</tr>
</thead>
<tbody>
<tr>
<td>Average error(%)</td>
<td>9.75</td>
<td>9.98</td>
<td>4.61</td>
<td>2.84</td>
<td>9.58</td>
<td>-0.47</td>
<td>8.88</td>
<td>3.50</td>
</tr>
<tr>
<td>Target Charge(nC)</td>
<td>0.05</td>
<td>0.02</td>
<td>0.03</td>
<td>0.03</td>
<td>0.02</td>
<td>0.03</td>
<td>0.02</td>
<td>0.03</td>
</tr>
</tbody>
</table>

which may not generate non-overlapping control signals for charging and discharging each unit capacitor. The voltage measured in Fig. 4.22 is an actual reflection of the threshold voltage. As it shows, the two channels have a similar tripping voltage during charge recycling indicating that the FSM is counting more pulses than there actually are. More severely, as the non-overlapping requirement on the switch pair (S1 – S3, S2 – S4 in Fig. 4.7) are not strictly met, there will be a short between the reference electrode and stimulation supply which stops the stimulation completely.

![Figure 4.22](image_url)

Figure 4.22.: Voltage measured directly on the IC output of Channel 5 on chip 2 which always have a shorter charge recycling phase

This issue can also be observed on the other channels on chip 2 and 9. For these channels, the maximum average error measured is 9.98% on channel 2 of chip 9. The maximum error on the other hand is as high as 32.72% (channel 4 of chip 2) when delivering sub-nC charge.

It is also noticeable that some traces become wider as the target charge increases (channel 6 of chip 9) and some even have large spikes or sudden changes (channel 9 of chip 9). These indicate the existence of other influence factors. These include the system errors as explained in Section 3.3.1, charge injection during switching activities and measurement errors. Some of them are hard to locate without accessing the internal signal inside the chips. However, the highlight of the results here is that the circuit can achieve charge mode stimulation by delivering a fixed amount of charge set by the user and achieve charge balancing.
Threshold calibration

As a result of the aforementioned non-overlapping control signal issue, the calibration does not operate on the chip as intended. Therefore, simulation results have been presented in Fig. 4.23. Please note, this is a purely functional simulation involving no timing properties.

\[
\begin{align*}
&\text{(i) V (V)} \\
&\text{(ii) V (V)} \\
&\text{(iii) V (V)} \\
&\text{(iv) V (V)} \\
&\text{(v) V (V)} \\
&\text{(vi) V (V)} \\
&\text{(vii) V (V)} \\
&\text{(viii) V (V)} \\
&\text{(ix) V (V)} \\
&\text{(x) V (V)} \\
&\text{(xi) V (V)}
\end{align*}
\]

Figure 4.23.: Simulation results of calibration. (a) negative phase calibration (b) positive phase calibration. These are two parts of a whole calibration process. Trace (i) is the signal for charging the unit capacitor C1, (ii) control signal for sampling the electrode voltage, (iii) control signal for stimulating using the charge stored on unit capacitor C1, (iv) threshold voltage (v) sampled electrode voltage (vi) – (xi) cal_data[5:0]

It can be seen that the threshold voltage steps away from the stimulation voltage as expected. It finishes when the sampled tripping voltage (sampled_Vth) on unit capacitors meets the requirement.

Worth noting that in Fig. 4.23(a), the charge control signal (trace (i)) remains fixed between 25 and 50 µs because Vth (trace (v)) is so low that comparator (in Fig. 4.7 cannot flip. To compare, during the positive calibration phase (Fig. 4.23(b)), no such blank out is observed as the threshold does not start from the stimulation voltage but 1 V lower.

Using saline solution with platinum electrode

Two platinum electrodes of the same size are used for testing the system – one is connected directly to 1.65 V (the mid-rail between the supplies). The end exposed area of each electrode is 12.56 mm². The solution is normal ringer (NaHCO₃: 2.4 mmol/L, NaCl: }
112 mmol/L, KCl: 2 mmol/L, CaCl₂·2H₂O: 2.4 mmol/L). The equivalent RC model of the EEI is shown in Fig. 4.24. All parameters are measured using FLUKE PM6303A, automatic RCL meter. \( R_1 \) is an external resistor used to measure the current and its value is used to match the total resistance in series as used in Section 4.4.3 so that the charge delivery speed is similar as well. Otherwise, it may cause malfunction of the FSM due to timing constraints (as \( R_2 = 640.8 \Omega \) would cause a higher operating frequency). The smaller value of \( C_1 \) compared to that in the RC model does cause voltage built up and slows down the charge delivery as can be seen from Fig. 4.25. Measurements have only been taken on channel 3 of chip 2 and channel 5 of chip 9 to check the similarities between results of this test and those using lumped elements. The results are shown in Fig. 4.26 and Fig. 4.27. It can be concluded that the saline test does not show significant differences from the previous RC measurements.

![EEI model of the platinum electrode used inside normal ringer solution during the test. \( R_1 \) is an external resistor. \( R_2 \) and \( C_1 \) are measured values. (All parameters are measured using FLUKE PM6303A, automatic RCL meter)](image)

### 4.4.4. Charge imbalance monitor and active charge balancing

Fig. 4.28 clearly shows the passive shorting phase during imbalanced current stimulation. An error signal will be generated if the voltage on the electrode exceeds the water window after shorting. Since passive discharge cannot be disabled, the electrode is driven to ground manually to test the imbalance monitor as shown in Fig. 4.29. C3 shows the voltage on the electrode where a stimulation can be seen in the second division. C2, the error signal turns high when the electrode is forced to zero.

Active charge balancing is also tested using a single phase waveform. Fig. 4.30 shows the active charge recycling in operation when the residue voltage is out of the predefined water window. However, due to the issue with non-overlapping charge/discharge control signal, the comparator outputs remain fixed at times so that it is not completely working.
Figure 4.26.: Comparison between charge delivery measured with RC model and in normal ringer solution on channel 3 of chip 2 and channel 5 of chip 9

Figure 4.27.: Comparison between residue charge measured with RC model and in normal ringer solution on channel 3 of chip 2 and channel 5 of chip 9

Figure 4.28.: Passive shorting phase during charge imbalancing
4.4.5. Multi-channel stimulation capability

The multichannel stimulation is the basis of multipolar stimulation and later introduced field shaping. This cannot be properly tested with current IC design because of a design bug which shorts the reference electrode to 1.65 V at all times in a multipolar configuration. Therefore, the charge imbalance monitor will always see the voltage on the stimulation electrode within the water window after shorting, thus never giving an error. Nevertheless, by connecting the RC EEI model between only two stimulation circuits, it can be demonstrated that the design is capable of multipolar stimulation. Fig. 4.31 presents two stimulation channels: one sourcing and one sinking with the same amplitude but opposite polarity settings. The reference electrode is left unconnected (not possible in an in-vitro test). The differential result on the EEI model is a constant current stimulation.

Moreover, Fig. 4.32 shows that each channel can be programmed individually into different modes. However, interference from other channels into the charge simulation channel is also clearly visible (spikes on trace C1).

4.5. Conclusion and Future Work

In this chapter, an 8-channel fully integrated programmable stimulator IC is presented. The idea is that each channel can be independently programmed into different stimulation
Figure 4.30: Active charge recycling in operation during imbalanced current stimulation. (a) the voltage on the electrode (b) comparator output on unit capacitor C1 (c) comparator output on unit capacitor C2

Figure 4.31: Current stimulation between two stimulation channels without involving the reference electrode. (a) and (b), voltages on the two opposite terminals of the EEI model. (c) the differential results of traces in (a) and (b), presenting a constant current stimulation voltage profile
Figure 4.32: Demonstration that different channel can be programmed individually. C1 shows the channel doing charge mode stimulation while C3 and C4 show the channel doing current stimulation synchronously with different parameters. Charge balancing is designed to be achieved via passive and active methods and safety is enforced by monitoring the stimulation electrode voltage. However, in this first and only tapeout, several design bugs prevent a thorough test.

For the tested parts, the results show that the DAC used in voltage and current stimulation is monotonous and has a maximum INL of -0.88 LSB across all the packaged chips tested. In charge mode stimulation, the charge measuring capacitor ($C_{\text{units}}$ in Chapter 3) is moved from the common return path to the stimulation path such that multipolar stimulation is feasible. The target charge delivery range is also extended. The results on charge mode stimulation agree with the results in the Chapter 3: maximum average charge delivery error of 10.42% (chip 6 channel 8), maximum average residue charge error of 9.98% (chip 9 channel 2) on all measured channels. The system also shows the ability of multichannel stimulation. Unfortunately, voltage mode stimulation, threshold calibration and active charge recycling cannot be tested properly.

Nevertheless, in this chapter, it is shown that within an area of 338 $\mu$m x 2200 $\mu$m, a fully programmable stimulation module can be implemented using 0.35 $\mu$m process. Several stimulation modules can be connected in parallel and receive commands and data from common buses to enable multi-channel operation. This allows designers to build fully integrated programmable stimulation system very easily by cascading this design. In addition, it can serve as a reference design for future integrated stimulators as an estimation on area requirement.

All the bugs are planned to be fixed in the next iteration of the design. More importantly,
the digital implementation needs to be carefully verified using equivalent logic checking, timing constraint checking. **Join test action group (JTAG)** interface needs to be implemented for post-fabrication debugging.

The first version of the chip must be software patched to function, nevertheless the proposed design provides a platform for verifying the field shaping idea presented in the next chapter.
Bibliography


5. Concept of Field Shaping for Improving Stimulation Focality

5.1. Introduction

To ultimately improve the dimensionality and fidelity of information, future stimulation systems need to increase the channel count per area to increase spatial resolution. However, the problem of stimulus spread has been present since the early work in the field [1]. This is a fundamental limit for increasing the total number of effective channels. The use of a multichannel system could herein give the possibility to confine the electric voltage field from spreading. Whilst most reported systems utilise current controlled field shaping [2–4], this chapter additionally studies voltage based field shaping, as voltage stimulation provides better stimulation efficiency [5].

The work presented in this chapter is based on finite element analysis (FEA), which is a numerical technique for approximating the results of a series of problem-defined differential equations under given boundary conditions. This is extensively used in the neural engineering community to analyse voltage fields during neuron/axon stimulation [6–8]. This method can be further extended to analysing neural response by integrating with neural modelling software, such as NEURON®, or by modelling the neuron directly with a finite element model (FEM). An extensive protocol has been recently presented by Joucla and Yvert [9].

5.2. Aims

This chapter aims to investigate the feasibility of developing multipolar stimulation strategies within the context of a multielectrode array to improve the spatial resolution. This is achieved by replicating the geometry of a multielectrode array (MEA) (potentially can be used for intraspinal microstimulation (ISMS)) within a FEA package, COMSOL Multiphysics®.

5.3. Methods

5.3.1. Model of spinal cord

Table 5.1 summarises key features within the human spinal cord. The dimension of the 5th segment of cervical spinal cord (C5), in addition to the diameters of the sagittal and transverse planes have been established from literature. The variations in the measurements are from different myelography methods used. The internal structure of the spinal cord
model (white and grey matter) has been calculated proportionally based on histology images found at C5 level. The length of C5 is modelled as 2 mm \([10]\). For ISMS, the other structures surrounding the spinal cord are not important. Also, dura matter, pia matter and arachnoid are reported not to influence the electric field potential distribution within the spinal cord \([8]\). The electrical properties are obtained from \([8, 11]\) where the conductivity of the white matter is anisotropic (Table 5.2), representing the fact that axons are mainly distributed along the rostral-caudal axis.

<table>
<thead>
<tr>
<th>Reference</th>
<th>Average Sagittal Diameter (SD)</th>
<th>Average Transverse Diameter (SD)</th>
</tr>
</thead>
<tbody>
<tr>
<td>[12]</td>
<td>8.3 mm (0.9 mm)</td>
<td>13.9 mm (1.0 mm)</td>
</tr>
<tr>
<td>[10]</td>
<td>7.5 mm</td>
<td>13.0 mm</td>
</tr>
<tr>
<td>[13]</td>
<td>7.7 mm</td>
<td>13.2 mm</td>
</tr>
<tr>
<td>[14]</td>
<td>9.5 mm</td>
<td></td>
</tr>
<tr>
<td>[15]</td>
<td>6.2 mm (1.15 mm)</td>
<td>11.8 mm (1.35 mm)</td>
</tr>
<tr>
<td>[16]</td>
<td>7.1 mm</td>
<td>13.8 mm</td>
</tr>
<tr>
<td>[17]</td>
<td>7.1 mm</td>
<td>13.8 mm</td>
</tr>
<tr>
<td>[18]</td>
<td>6.9 (0.5)</td>
<td></td>
</tr>
</tbody>
</table>

Table 5.2: Conductivities of the compartments in the inhomogenous anisotropic model

<table>
<thead>
<tr>
<th>Structure</th>
<th>Conductivity (S/m)</th>
</tr>
</thead>
<tbody>
<tr>
<td>grey matter (longitudinal)</td>
<td>0.255</td>
</tr>
<tr>
<td>grey matter (transversal)</td>
<td>0.195</td>
</tr>
<tr>
<td>white matter (longitudinal)</td>
<td>0.797</td>
</tr>
<tr>
<td>white matter (transversal)</td>
<td>0.0988</td>
</tr>
<tr>
<td>cerebrospinal fluid</td>
<td>1.79</td>
</tr>
</tbody>
</table>

Longitudinal, Z-direction in the model; transversal, X,Y-direction in the model

### 5.3.2. Model of multi electrode array

The electrode array has been modelled based on a 4-by-4 MEA (by MicroProbes©). The spacing between electrodes is 400 \(\mu\)m with a tip diameter of 2-3 \(\mu\)m and base diameter of 75 \(\mu\)m. The contact at the tips is made by exposing the top 2 mm from the enclosing insulation to achieve a target resistance of 10 k\(\Omega\). The total length is 5.5 mm which positions the tips around the ventral horn and the bases inside the cerebrospinal fluid. The finished 3D model is shown in Fig. 5.1. The insulation and electrode are made of Parylene C and 30%/70% Pt/Ir alloys with electric conductance of 10 fS/m and 28,571 kS/m respectively.

### 5.3.3. Stimulation protocols

The configuration uses 16 terminals at the base of the electrodes to provide static stimulation voltage and current. Although this has been modelled as 16 individual electrodes, the simulations were only performed on a subset of the total electrodes. Unused electrodes are configured as high impedance at the terminal. Electrodes have been labelled as in Fig. 5.2.
The used 3-by-3 portion is labelled from 1 to 9 (on the bottom right), with the least used electrodes being labelled from 10 to 16.

Within this 3-by-3 subset, electrode number 5 is either biased using a negative voltage or sinking current (neural tissue is 0 V). Other electrodes are biased based on the simulation requirements.

The model has been meshed to 1,206,693 elements with extra fine setting by COMSOL Multiphysics®. Local refinement has been done within the volume around the tip. The minimum element quality is 0.006037 and average quality is 0.7195. Meshing with pre-defined settings was found to be consistent and faster to solve than meshing with individual settings of element size for each different part of the model. Current conservative boundary conditions are set to be over all the conductive volume. The outer boundaries of the model are set to electric insulation such that it will not serve as a voltage source. The iterative linear solver is chosen based on modelling scale with a relative tolerance of 0.001.

5.4. Results and Discussions

5.4.1. Comparison between different stimulation modalities

Field shaping with current controlled stimulation

Current controlled stimulation has recently been reported in deep brain stimulation (DBS) to shift the voltage profile [2]. In this simulation, channels 4–6 are configured as described below to show the voltage field shifting:

1. \( I_4 = 0 \mu A, I_5 = -100 \mu A, I_6 = 100 \mu A \)
2. \( I_4 = 50 \mu A, I_5 = -100 \mu A, I_6 = 50 \mu A \)
3. $I_4 = 100 \mu A, I_5 = -100 \mu A, I_6 = 0 \mu A$

The simulation results are shown in Fig. 5.3. These results are similar to those of two point charges on a single plane. Note that some of the electric field streamlines are shown as broken because at that point the streamline leaves the plotting plane. To further illustrate the field shifting, the voltage along the Z-direction at $X = -2800 \mu m$ in Fig. 5.3 is plotted separately in Fig. 5.4. Although not shown, other current sourcing/sinking combinations between channels 4 and 6 can be interpolated between these lines.

**Field shaping with voltage controlled stimulation**

In comparison to field shaping using current controlled stimulation, voltage controlled stimulation can offer control of the voltage potentials directly at the electrodes, rather than leaving them to be determined by the impedance of the electrode-electrolyte interface (EEI) interface. This can be shown by comparing Fig. 5.6 with Fig. 5.4. Fig. 5.6 shows a much larger voltage variation between the electrodes that are 100 $\mu m$ away. The top view at a height of 100 $\mu m$ away from the electrode is shown in Fig. 5.5.

Another difference between the two modes is that in CMS the total current flowing out the electrode must be the same as that flowing into the electrode and can be manually set easily. In VMS this requirement is fulfilled automatically provided there is no other uncontrolled voltage source. This can be seen by comparing Fig. 5.6 and Fig. 5.4. Because current stimulation controls the current directly, the total sourcing/sinking current is maintained during shifting. As a result, the minimum voltage in Fig. 5.4 are similar. In voltage stimulation, the total current is not maintained, therefore showing a large variation when the voltage is changed on only one electrode.
Figure 5.3: Topview of electric field and voltage potential contour on a plane at 100 µm above the electrode tips for current mode stimulation (CMS). The coloured contours are voltage potential. The black lines are geometric boundaries and electric field streamlines.

Figure 5.4: Voltage potential along the Z-direction at $X = -2800 \mu m$ in Fig. 5.3. Blue-cross corresponds (a), green-circle (b) and red-circle (c)
Figure 5.5: Top view of electric field and voltage potential contours on a plane 100 µm above the electrode tips for voltage mode stimulation (VMS). The coloured contours are voltage potentials. The black lines are geometric boundaries and electric field streamlines.

Figure 5.6: Voltage potentials along the Z-direction at $X = -2800$ µm in Fig. 5.5. Blue-cross corresponds (a), green-circle (b) and red-circle (c)
In summary, for both voltage and current controlled stimulation, when 2 electrodes (channels 4 and 5) are used to guard the working electrode (channel 5), the peak of the voltage field is able to shift by around \(100 \mu m\) at a distance of \(100 \mu m\) away from the electrodes. The next step is to identify the controllable factors that determine the field shaping ability.

5.4.2. Influence of the distance to the electrodes

In Section 5.4.1, the plots have been observed at a plane \(100 \mu m\) away from the electrode. If the observation plane is moved to \(10 \mu m\), it can be observed that the peak of the voltage potential becomes closer to the electrode. The results for CMS and VMS are shown in Fig. 5.7, Fig. 5.8 and Fig. 5.9, Fig. 5.10 respectively.

In this case, the peak voltage shifts are not observable in either of the stimulation modes. Therefore, there appears to be a certain range from the electrode within which the relative peak voltage cannot be shifted. However, there is also a certain range beyond which the difference between the voltages above the electrodes is not sufficient to achieve stimulation. For example, comparing Fig. 5.9(b) and Fig. 5.5(b), it can be seen that the absolute voltage directly above electrode 5 increases from around -0.24 V at 10 \(\mu m\) above to around 0.43 V at 100 \(\mu m\) and the peak-to-peak difference between voltages decreases from 1.16 V to 0.37 V resulting in a smaller potential gradient. This is also true for CMS.
Figure 5.7.: Top view of electric field and voltage potential contours on a plane 10 μm above the electrode tips for CMS. The coloured contours are voltage potentials. The black lines are geometric boundaries and electric field streamlines.
Figure 5.8: Voltage potentials along the Z-direction at $X = -2800 \mu m$ in Fig. 5.7. Blue-cross corresponds (a), green-circle (b) and red-circle (c).
Figure 5.9: Top view of electric field and voltage potential contours on a plane 10 µm above the electrode tips for VMS. The coloured contours are voltage potentials. The black lines are geometric boundaries and electric field streamlines.
Figure 5.10.: Voltage potentials along the Z-direction at $X = -2800 \mu m$ in Fig. 5.9. Blue-cross corresponds (a), green-circle (b) and red-circle (c)
5.4.3. Influence of the number of active electrodes

In the simulations shown above, only 3 electrodes in a line were used. More controllability is expected if the number of electrode used was increased. In this simulation, 5 electrodes: 2,4,5,6,8 were used to form a cross shape. The test configurations are shown below:

<table>
<thead>
<tr>
<th>Configuration</th>
<th>Electrode 2</th>
<th>Electrode 4</th>
<th>Electrode 5</th>
<th>Electrode 6</th>
<th>Electrode 8</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage Cfg. 1</td>
<td>1.65 V</td>
<td>1.65 V</td>
<td>-1.65 V</td>
<td>1.65 V</td>
<td>1.65 V</td>
</tr>
<tr>
<td>Voltage Cfg. 2</td>
<td>0 V</td>
<td>0 V</td>
<td>-1.65 V</td>
<td>1.65 V</td>
<td>1.65 V</td>
</tr>
<tr>
<td>Voltage Cfg. 3</td>
<td>0 V</td>
<td>1.65 V</td>
<td>-1.65 V</td>
<td>1.65 V</td>
<td>1.65 V</td>
</tr>
<tr>
<td>Current Cfg. 1</td>
<td>0 μA</td>
<td>0 μA</td>
<td>-120 μA</td>
<td>60 μA</td>
<td>60 μA</td>
</tr>
<tr>
<td>Current Cfg. 2</td>
<td>0 μA</td>
<td>40 μA</td>
<td>-120 μA</td>
<td>40 μA</td>
<td>40 μA</td>
</tr>
<tr>
<td>Current Cfg. 3</td>
<td>30 μA</td>
<td>30 μA</td>
<td>-120 μA</td>
<td>30 μA</td>
<td>30 μA</td>
</tr>
</tbody>
</table>

When testing these configurations, the results shown are measured at 100 μm above the electrode plane, presented in Fig. 5.11 and Fig. 5.13 for VMS and CMS respectively.

In “Voltage Cfg. 1” the voltage from the central electrode (electrode 5) is more constrained within the space defined by the surrounding electrodes compared to the 3-electrode configuration (electrode 4,5,6) in Fig. 5.5(b). In “Voltage Cfg. 2”, the voltage is shifted by approximately 25 μm along both X and Z direction as shown in Fig. 5.12. In “Voltage Cfg. 3”, the voltage is only shifted along the X-direction. In the Z-direction, the voltage presents a similar pattern as the green-circle trace in Fig. 5.6.

The significance of the results shown above is that by adding two further electrodes on the orthogonal direction of the original 3-electrode configuration, the voltage peaks can be shifted in 2-Dimension space. Although this is only shown in “Voltage Cfg. 2”, it is expected that the location of the peak could be modulated by varying the voltages of the surrounding electrodes based on the superposition theorem.

Similar results are observed for the three current configurations in Table 5.3 (Fig. 5.13 and Fig. 5.14).

Although increasing the total number of electrodes can offer increased spatial control of the induced voltage field, this is at a cost of more area and a complex stimulation protocol. In other words, compared to using a single electrode inside a MEA at a spacing of 300 μm, using the 5-electrode configuration for the same stimulation target would require a spacing of 100 or 150 μm depending on whether the surrounding electrodes can be shared.
Figure 5.11: Top view of electric field and voltage potential contours on a plane 100 µm above the electrode tips for VMS using 5 electrodes. The coloured contours are voltage potentials while the black lines are geometric boundaries and electric field streamlines.
Along the line formed by electrode 4, 5, 6

Along the line formed by electrode 2, 5, 8

Figure 5.12.: Voltage potential along the Z-direction at $X = -2800 \mu m$ and X-direction at $Z = -800 \mu m$ in Fig. 5.11. Blue-cross represents Voltage Conf 1, green-circle Voltage Conf 2, red-circle Voltage Conf 3
Figure 5.13: Top view of electric field and voltage potential contours on a plane 100µm above the electrode tips for CMS using 5 electrodes. The coloured contours are voltage potentials while the black lines are geometric boundaries and electric field streamlines.
Along the line formed by electrode 4,5,6

Along the line formed by electrode 2,5,8

Figure 5.14: Voltage potential along the Z-direction at $X = -2800 \mu m$ and X-direction at $Z = -800 \mu m$ in Fig. 5.11. Blue-cross represents Current Conf 1, green-circle Current Conf 2, red-circle Current Conf 3
5.4.4. Influence of electrode array grid spacing

Following the idea of using more channels/area to stimulate a single target, it is important to understand how the field shaping ability changes with reduced spacing. In these simulations, an electrode pitch of 200 $\mu$m is used, which is larger than the minimum spacing offered by MicroProbes® (100 $\mu$m). The results on CMS and VMS observed at 100 and 10 $\mu$m planes are shown in Fig. 5.15, Fig. 5.16, Fig. 5.17 and Fig. 5.18. The corresponding electrode configurations are given in the corresponding captions.

Because of the small spacing, the dynamic range for CMS of the induced voltage field is reduced – the maximum value reduced and the minimum value raised. This compression is more visible at an observation plane of 100 $\mu$m rather than at 10 $\mu$m, indicating a reduced range of the voltage field. The plots on the transverse lines (Fig. 5.15(e) and Fig. 5.16(e)) shows that the field shaping on the orthogonal direction would not affect the relative value, i.e. spatial derivative, on the current direction.

For VMS, a similar compression range is observed. However, here it is mainly due to the increase of the minimum value as a result of superimposition and having a fixed voltage value at the electrodes. In the orthogonal direction of field shaping, similar to that of CMS, the shape of the voltage field is similar across the three different stimulation protocols.
(a) $I_4 = 0$, $I_5 = -100 \mu A$, $I_6 = 100 \mu A$

(b) $I_4 = 100 \mu A$, $I_5 = -100 \mu A$, $I_6 = 0$

(c) $I_4 = 50 \mu A$, $I_5 = -100 \mu A$, $I_6 = 50 \mu A$

(d) Along the line at $X=-2400 \mu m$. Blue-cross represents (a), green-circle (b), red-circle (c)

(e) Along the line at $Z=-1200 \mu m$. Blue-cross represents (a), green-circle (b), red-circle (c)

Figure 5.15: Electric field and voltage potential contours on a plane 100 $\mu m$ above the electrode tips for CMS under a spacing of 200 $\mu m$. The coloured contours are voltage potentials. The black lines are geometric boundaries and electric field streamlines.
(a) $I_4 = 0$, $I_5 = -100 \mu A$, $I_6 = 100 \mu A$

(b) $I_4 = 100 \mu A$, $I_5 = -100 \mu A$, $I_6 = 0$

(c) $I_4 = 50 \mu A$, $I_5 = -100 \mu A$, $I_6 = 50 \mu A$

(d) Along the line at X=−2400 μm. Blue-cross represents (a), green-circle (b), red-circle (c)

(e) Along the line at Z=−1200 μm. Blue-cross represents (a), green-circle (b), red-circle (c)

Figure 5.16: Electric field and voltage potential contours on a plane 10 μm above the electrode tips for CMS under a spacing of 200 μm. The coloured contours are voltage potentials. The black lines are geometric boundaries and electric field streamlines.
Figure 5.17: Electric field and voltage potential contours on a plane 100 µm above the electrode tips for VMS under a spacing of 200 µm. The coloured contours are voltage potentials. The black lines are geometric boundaries and electric field streamlines.
Figure 5.18: Electric field and voltage potential contours on a plane 10 µm above the electrode tips for VMS under a spacing of 200 µm. The coloured contours are voltage potentials. The black lines are geometric boundaries and electric field streamlines.
5.4.5. Influence of the stimulation amplitude

In this series of simulations, 3-electrode configurations were used and voltage/current values on channel 4 and channel 6 were fixed. The voltage potential on the observation line across electrodes 4, 5 and 6 is shown in Fig. 5.19 for both CMS and VMS on 10 and 100 µm planes.

(a) Blue-cross: $I_4 = 1 \mu A$, $I_5 = -2 \mu A$, $I_6 = 1 \mu A$ Green-circle: $I_4 = 1.5 \mu A$, $I_5 = -3 \mu A$, $I_6 = 1.5 \mu A$

(b) Blue-cross: $I_4 = 1 \mu A$, $I_5 = -2 \mu A$, $I_6 = 1 \mu A$ Green-circle: $I_4 = 1.5 \mu A$, $I_5 = -3 \mu A$, $I_6 = 1.5 \mu A$

(c) Blue-cross: $V_4 = 1.65 V$, $V_5 = -5 V$, $V_6 = 1.65 V$ Green-circle: $V_4 = 1.65 V$, $V_5 = -10 V$, $V_6 = 1.65 V$

(d) Blue-cross: $V_4 = 1.65 V$, $V_5 = -5 V$, $V_6 = 1.65 V$ Green-circle: $V_4 = 1.65 V$, $V_5 = -10 V$, $V_6 = 1.65 V$

Figure 5.19.: Voltage potentials along the line at $X=-2400 \mu m$ for field shaping in CMS ((a),(b)) and VMS ((c),(d)) with changing amplitudes on planes at 100 µm ((a),(c)) and 10 µm ((b),(d))

It is shown that VMS and CMS have similar voltage field shapes when observed from a plane that is the same distance from the electrodes (Fig. 5.19). Both have a change on the dynamic range of the voltage field. But for CMS, the increased sinking current on electrode 5 has to be compensated by increasing the sourcing currents on electrodes 4 and 6. For VMS, the voltage potential on electrode 4 and 6 can remain the same. This allows independent control on each electrode voltage during VMS.
5.5. Conclusion and Future Work

This chapter has investigated the effects of basic field shaping in a uniform MEA towards increasing the spatial resolution of neural stimulation. Both VMS and CMS have been compared alongside by varying various parameters such as electrode pitch, multipolar configuration, observation height and stimulus amplitude. It is intended that these stimulation protocols can be later configured using the application-specific integrated circuit (ASIC) designed in Chapter 4.

The results indicate that both current and voltage field shaping can be achieved at a certain distance away from the electrode. The findings are summarised below.

- **Stimulation modalities** Both CMS and VMS can shape the voltage field using more than one electrode. The fundamental physics behind these results is voltage superposition.

- **Distance to the electrodes** The shift in voltage peak increases with distance. However, the longer the distance, the less likely a neuron will be stimulated.

- **Number of active electrodes** More electrodes can provide more spatial controllability at a cost of more complex stimulation protocol and less stimulation resolution if the pitch is not changed.

- **Pitch of electrode array** The voltage field gets more confined with a finer pitch. For CMS, the dynamic range of the voltage field decreases as well, but it remains the same for VMS.

- **Stimulation amplitude** The dynamic range of the voltage field will increase. For CMS, the increased value must be compensated by recycling an equal sum of current from other electrodes.

In the presented work, the conclusion is that the voltage field can be shaped. However, the voltage field that has been obtained was not imported to NEURON® for evaluation of the activation volume as suggested by [9]. This is certainly an area for further work. It would also be beneficial to compare simulation results with in-vitro/in-vivo measurement. However, this requires constructing a recording platform which can be observed at micrometer scale to sample the voltage between electrodes on MEA. Moreover, a method needs to be found for field shaping using charge mode stimulation (QMS) as there is limited temporal control on this method which makes synchronisation hard to achieve.
Bibliography


6. Conclusion

This thesis has developed methods and circuits for neural stimulation. It is intended these will be applied specifically to intraspinal microstimulation (ISMS). Even with a very limited number of stimulation channels, relatively good control on muscle activation has already been demonstrated by other researches. Furthermore, ISMS has been shown to provide a more graded control of muscle force in addition to fatigue resistance compared to the spinal cord and peripheral nerve stimulation methods (e.g. epidural and direct muscle stimulation). This work aims to provide a platform for neuroscientists to further exploit these benefits.

Chapter 2 introduces the basic knowledge which explains how electrical neural stimulation is able to innervate a muscle. It also compares three different modalities for electric neural stimulation (ENS) and highlights the engineering considerations for designing an ENS system. Based on these requirements, the state-of-the-art ENS systems are reviewed. The problem of stimulus spread and the potential methods is also introduced in the end.

6.1. Original Contributions

This thesis has made original contributions in 3 key areas: (1) a novel charge-metering method and circuit for voltage mode stimulation (VMS); (2) a multipolar, multichannel reconfigurable architecture and integrated circuit for investigating advanced stimulation strategies; and (3) establishing the effect of varying stimulus and configuration parameters within a uniform, multipolar electrode array by simulation.

Chapter 3 has proposed a new method and circuit for voltage mode stimulation based on charge metering. This uses a small, integrated capacitor that is charged and discharged rapidly to monitor the overall charge delivery and thus ensuring safety. This can achieve VMS and also charge mode stimulation (QMS) within a compact silicon footprint requiring only small integrated capacitors, a comparator and digital logic. This is the first fully integrated circuit that can provide QMS-based charge delivery. The integrated circuit realisation has been validated through circuit simulation, measured results (both using a lumped RC model and saline solution) and experimentally (ex-vivo).

Chapter 4 has detailed a novel architecture for a multi-channel stimulator that can provide a user-defined multipolar stimulus using either current mode stimulation (CMS), VMS or QMS. The system is based on a scalable channel architecture that each contains a stimulus generation circuit and finite state machine (FSM). Each channel contains an independent DAC that can be used to generate an arbitrary waveform for CMS and VMS. The method proposed in chapter 3 has been adapted to provide QMS by using the unit capacitance to generate the stimulus rather than metering the delivery. The system uses a custom protocol
interpreted by a central FSM that receives stimulus commands from an external device. This allows channels to be independently configured and triggered in synchronisation. This system has been validated through circuit simulations and measured results. However, in the first and only tapeout, some functions of the design (including VMS, self calibration, active charge balancing and multipolar stimulation) cannot be tested correctly because of mistakes made at design time as mentioned in Chapter 4.

Chapter 5 has investigated the effect of using multipolar stimulation strategies with a uniform multi electrode array. Through computational simulations, the effect on the potential field was established and compared for compared between CMS and VMS. The study focused on the design of stimulation strategies given an available electrode geometry rather than the electrode design itself. Within the results reported, the effects of varying parameters such as electrode pitch, distance from the target, stimulus magnitude and electrode configuration were established. Preliminary COMSOL® results show that advanced multipolar strategies can be used to reshape the potential field which can lead to improved spatial resolution in stimulation.

6.2. Recommendations for Future Work

For the technical contributions described in this thesis, the specific improvements and related further work are presented at the end of each chapter. There are also some flaws in the design that need to be fixed in future tapeouts. This section is thus focused on possible future directions towards a useful spinal cord injury (SCI) therapy.

The catastrophic impact caused by SCI is that the neural connections are broken and cannot be effectively re-established. Apart from the site of injury, other parts of the spinal cord would typically remain functionally intact. However, without supraspinal control, the spinal cord below the injury site would develop spasticity and spasms and causes muscle atrophy in the future.

Although a stimulating system can be used in open loop to help restore lost function and prevent muscle atrophy, this is a sub-optimal solution. The system can be integrated with a neural recording subsystem to provide the possibility of building a neural bridge by bypassing the site of injury. Although there remain several challenges (for example, spatial resolution in stimulation), a prototype system with several channels that have been carefully selected could result in a therapeutic benefit.

The recording site could also be integrated more locally to the stimulation target such that it can monitor the stimulation efficacy. Such close-loop stimulation can be used to tune stimulus parameters towards a near optimal level. In addition to potentially prolonging electrode (and battery) lifetime, it can dynamically adjust these parameters over chronic use and provide increased robustness. Other complex signal processing can be used to generate stimulation pattern based on the analysis result of the recorded signal so that an artificial reflex arc may be built to replace the impaired one. However, the close proximity between recording and stimulation would raise the problem of stimulation artefact.

To tackle this issue of stimulus artefact and selectivity, there are two approaches that can
be employed. More directly, a computational model together with an appropriate front-end could be applied in order to “filter” out the artefact. Alternatively, different stimulation and recording modalities could be combined such that the underlying mechanisms are decoupled. For example, optogenetics (for either stimulation or recording) could be combined with electrical techniques. This would allow concurrent stimulation and recording – perhaps even direct feedback to adjust each stimulus pulse in real-time.

6.3. Concluding Remarks

ENS is an important method for interfacing to the nervous system. This has already been successfully used in improving the quality of life for individuals suffering from hearing loss (cochlear implant), chronic pain (transcutaneous electrical nerve stimulation) and Parkinson’s diseases (deep brain stimulation (DBS)). Although there exist several emerging methods claiming benefits over ENS, this is still the most widely used. This is for the following reasons: first and foremost, the track record of having been used effectively and safely places alternative methods under increased scrutiny. Secondly, very few emerging methods have shown the sub-millisecond response time that is achievable with ENS.

ISMS is still a neurotechnology in its infancy. Experimental neuroscience has recently reported encouraging results demonstrating the opportunities. However, key advances will inevitably require multidisciplinary efforts in electrode design, materials technology, biocompatible and robust packaging, microsurgery for precise implantation, neuroscience, and of course electronic design.

The work reported in this thesis tackles only a very small portion of the bigger question: how the electronic design can be used to improve stimulation selectively in partial isolation of the previously mentioned disciplines. This will in the first instance, be useful as a research tool for the neural engineering community. It will only be after such methods are applied that we will know what is possible.
A. Appendices

A.1. Neural signal recording system used in _ex-vivo_ testing

Figure A.1: Neural signal recording system used in _ex-vivo_ testing
A.2. Verilog Code Listing for Multichannel Stimulator

Listing A.1: Serial in parallel output

```
module SIPO(clk, rst, we, data_in, data_out, de, sec);

input clk;
input rst;
input data_in;
input we;

output reg [20:0] data_out;
output reg de, sec;
reg inv_clk;
reg [26:0] tmp_in;
reg [20:0] tmp_out;
reg [4:0] index;
reg [5:0] synd;
reg data_ready;

always @(clk) begin
    inv_clk =~ clk;
end

always @(negedge inv_clk or negedge rst) begin
    if (!rst) begin
        // reset
        tmp_in <= 27'b000_0000_0000_0000_0000_00_00000_0;
        index <= 5'b00000;
        data_ready <= 1'b0;
        data_out <= 21'b1_0000_0000_0000_0000_0000;
        sec <= 1'b0;
        de <= 1'b0;
    end
    else begin
        if (we && !data_ready) begin
            tmp_in[index] <= data_in;
            if (index == 5'b11010) begin
                index <= 5'b00000;
                data_ready <= 1'b1;
            end
            else begin
                index <= index + 5'b00001;
            end
        end
        else if (data_ready) begin
            data_out <= tmp_out;
            if (synd==6'b000000) begin
                // no error
                sec <= 1'b0;
                de <= 1'b0;
            end
            else if (synd[5]==1'b1) begin
                // single error corrected. Odd errors is causing problem!
                sec <= 1'b1;
                de <= 1'b0;
            end
            else if ((synd[5]==1'b0) && (synd[4:0]! =5'b00000)) begin
                sec <= 1'b1;
                de <= 1'b0;
            end
        end
    end
endmodule
```
Listing A.2: Individual channel control FSM

```vhdl
module channel_fsm (clk, rst, cdi, addr, addr_set, data_in, stim_finish, 
memory_ergodic, data_out, data_check, errflag, read_setup, stim_mode, 
rst_stim, stim_ready, data_ready, set_charge, calibration, cal_done, 
lowz_state, set_cal);

input clk, rst;
input cdi;
input [3:0] addr, addr_set;
input [15:0] data_in;
output reg errflag;
output reg lowz_state;
```

```vhdl
70 always @(tmp_in, data_ready) begin
71     synd[0] = ^(tmp_in & 2^7 'b010_1010_1011_0101_0110_11_0_00001);
72     synd[1] = ^(tmp_in & 2^7 'b100_1100_1101_1001_1011_01_0_00010);
73     synd[2] = ^(tmp_in & 2^7 'b000_1111_0001_1110_0011_10_0_00100);
74     synd[3] = ^(tmp_in & 2^7 'b111_0000_0001_1111_1100_00_0_01000);
75     synd[4] = ^(tmp_in & 2^7 'b111_1111_1110_0000_0000_00_0_10000);
76     synd[5] = ^(tmp_in);
77     tmp_out = tmp_in[26:6];
78     if (data_ready & synd[5]==1'b1) begin
79         case (synd[4:0])
80             5'b11010: tmp_out[20]=~tmp_out[20];
81             5'b11001: tmp_out[19]=~tmp_out[19];
82             5'b11000: tmp_out[18]=~tmp_out[18];
83             5'b10111: tmp_out[17]=~tmp_out[17];
84             5'b10110: tmp_out[16]=~tmp_out[16];
85             5'b10101: tmp_out[15]=~tmp_out[15];
86             5'b10100: tmp_out[14]=~tmp_out[14];
87             5'b10011: tmp_out[13]=~tmp_out[13];
88             5'b10010: tmp_out[12]=~tmp_out[12];
90             5'b01111: tmp_out[10]=~tmp_out[10];
91             5'b01110: tmp_out[9]=~tmp_out[9];
92             5'b01101: tmp_out[8]=~tmp_out[8];
93             5'b01100: tmp_out[7]=~tmp_out[7];
94             5'b01011: tmp_out[6]=~tmp_out[6];
95             5'b01010: tmp_out[5]=~tmp_out[5];
96             5'b01001: tmp_out[4]=~tmp_out[4];
97             5'b00111: tmp_out[3]=~tmp_out[3];
99             5'b00101: tmp_out[1]=~tmp_out[1];
100            5'b00011: tmp_out[0]=~tmp_out[0];
101         endcase
102     end else begin
103         tmp_out = 2^1'b1_0000_0000_0000_0000_0000;
104     end
105 end
106 endmodule
```
input stim_finish, stim_ready, cal_done;
output reg [2:0] stim_mode;
output reg read_setup, set_charge, set_cal;
output reg rst_stim, calibration;

input memory_ergodic;
reg mem_ergodic;
output data_check, data_ready;
output reg [15:0] data_out;

reg [3:0] state, next_state;
always @ (addr_set) begin
    case(addr_set)
        4'b0000: CHID = 16'h0000000000000000;
        4'b0001: CHID = 16'h0000000000000001;
        4'b0010: CHID = 16'h0000000000000010;
        4'b0011: CHID = 16'h0000000000000011;
        4'b0100: CHID = 16'h0000000000000100;
        4'b0101: CHID = 16'h0000000000000101;
        4'b0110: CHID = 16'h0000000000000110;
        4'b0111: CHID = 16'h0000000000000111;
        4'b1000: CHID = 16'h0000000000010000;
        4'b1001: CHID = 16'h0000000000010001;
        4'b1010: CHID = 16'h0000000000010010;
        4'b1011: CHID = 16'h0000000000010011;
        4'b1100: CHID = 16'h0000000000010100;
        4'b1101: CHID = 16'h0000000000010101;
        4'b1110: CHID = 16'h0000000000010110;
        4'b1111: CHID = 16'h0000000000010111;
        default: CHID = 16'h0000;
    endcase
end

always @(posedge clk or negedge rst) begin
    if (!rst) begin // reset is hard reset!
        // Channel Identifier
        reg [15:0] CHID;
        // State variables
        parameter RESET=4'b0000, IDLE=4'b0001, STIM=4'b0111, LowZ=4'b0110, ERR=4'b0011, PRGAV=4'b0100, PRGTIM=4'b0101, PRGCHG=4'b0111, CAL=4'b1000, PRGCAL=4'b1011;
        // Stimulation modes
        parameter I_STIM=3'b001, V_STIM=3'b010, C_STIM=3'b011, I_STIM_a=3'b101, V_STIM_a=3'b110, C_STIM_a=3'b111;
        // Command codes
        parameter c_START=4'b1100, c_STOP=4'b1101, c_RESET=4'b1111, c_LowZ=4'b1110, c_CAL=4'b1000, c_I_STIM=4'b1110, c_V_STIM=4'b1010, c_C_STIM=4'b1111, c_I_STIM_a=4'b0110, c_V_STIM_a=4'b0110, c_C_STIM_a=4'b0111;
        reg [3:0] state, next_state;
        // Convert binary channel ID to one-hot channel ID.
        always @(addr_set) begin
            case(addr_set)
                4'b0000: CHID = 16'h0000000000000000;
                4'b0001: CHID = 16'h0000000000000001;
                4'b0010: CHID = 16'h0000000000000010;
                4'b0011: CHID = 16'h0000000000000011;
                4'b0100: CHID = 16'h0000000000000100;
                4'b0101: CHID = 16'h0000000000000101;
                4'b0110: CHID = 16'h0000000000000110;
                4'b0111: CHID = 16'h0000000000000111;
                4'b1000: CHID = 16'h0000000000010000;
                4'b1001: CHID = 16'h0000000000010001;
                4'b1010: CHID = 16'h0000000000010010;
                4'b1011: CHID = 16'h0000000000010011;
                4'b1100: CHID = 16'h0000000000010100;
                4'b1101: CHID = 16'h0000000000010101;
                4'b1110: CHID = 16'h0000000000010110;
                4'b1111: CHID = 16'h0000000000010111;
                default: CHID = 16'h0000;
            endcase
        end
        // Sequential logic, synchronous state transfer
        always @(posedge clk or negedge rst) begin
            if (!rst) begin // reset is hard reset!
            end
        end
    end
end
state<= RESET;
tmp_stim_mode <= 3'b000;
end else begin
  // state transfer
  state<= next_state;
  if (state==IDLE && (cdi==1'b1) && (data_in & CHID)==CHID)
  begin
    case (addr)
      c_I_STIM: begin
        if (stim_ready) begin
          tmp_stim_mode <= I_STIM;
        end else begin
          tmp_stim_mode <= 3'b000;
        end
      end
      c_V_STIM: begin
        if (stim_ready) begin
          tmp_stim_mode <= V_STIM;
        end else begin
          tmp_stim_mode <= 3'b000;
        end
      end
      c_C_STIM: begin
        if (stim_ready) begin
          tmp_stim_mode <= C_STIM;
        end else begin
          tmp_stim_mode <= 3'b000;
        end
      end
      c_I_STIM_a: begin
        if (stim_ready) begin
          tmp_stim_mode <= I_STIM_a;
        end else begin
          tmp_stim_mode <= 3'b000;
        end
      end
      c_V_STIM_a: begin
        if (stim_ready) begin
          tmp_stim_mode <= V_STIM_a;
        end else begin
          tmp_stim_mode <= 3'b000;
        end
      end
      c_C_STIM_a: begin
        if (stim_ready) begin
          tmp_stim_mode <= C_STIM_a;
        end else begin
          tmp_stim_mode <= 3'b000;
        end
      end
    endcase
  end
always @(cdi, data_in, CHID, addr_set, addr) begin
  if (((cdi==1'b1) && (data_in & CHID)==CHID)) || ((cdi==1'b0) && (addr==addr_set)) begin
    ch_selected = 1'b1;
  end else begin
    ch_selected = 1'b0;
  end
always @(posedge clk or negedge rst) begin
  if (!rst) begin
    // reset
    reg_mem_ergodic <= 1’b0;
  end
  else begin
    reg_mem_ergodic <= memory_ergodic;
  end
end

always @((state, cdi, addr, data_in, channel_set, reg_mem_ergodic, stim_ready,
          tmp_stim_mode[1:0], stim_finish, CHID, errflag, cal_done, set_charge,
          read_setup, set_cal)
begin
  if ((cdi==1’b1) && (addr==c_RESET) && ((data_in & CHID)==CHID))
    begin // soft reset can be triggered within any state
      next_state=RESET;
    end else begin
      case (state)
        IDLE: begin
          if ((cdi==1’b1) && ((data_in & CHID)==CHID) && !
            errflag) begin
            case (addr)
              c_START: begin
                if (channel_set==1’b1 && stim_ready) begin
                  next_state=STIM; // only start stimulation
                  when the channel is properly set.
                end else begin
                  next_state=IDLE;
                end
              end
              c_STOP: begin
                next_state=IDLE;
              end
              c_LowZ: begin
                next_state=LowZ;
              end
              c_RESET: begin
                next_state=RESET;
              end
              c_CAL: begin
                next_state=PRGCAL;
              end
              c_I_STIM: begin
                if (stim_ready) begin
                  next_state=PRGWAV;
                end else begin
                  next_state=IDLE;
                end
              end
              c_V_STIM: begin
                if (stim_ready) begin
                  next_state=PRGWAV;
                end else begin
                  next_state=IDLE;
                end
              end
              c_C_STIM: begin
                if (stim_ready) begin
                  next_state=PRGCHG;
              end
end
end else begin
    next_state=IDLE;
end

c_I_STIM_a: begin
    if (stim_ready) begin
        next_state=PRGwav;
    end else begin
        next_state=IDLE;
    end
end
c_V_STIM_a: begin
    if (stim_ready) begin
        next_state=PRGwav;
    end else begin
        next_state=IDLE;
    end
end
c_C_STIM_a: begin
    if (stim_ready) begin
        next_state=PRGChg;
    end else begin
        next_state=IDLE;
    end
end
default: next_state=ERR;
endcase
end else begin
    next_state = IDLE;
end
end

STIM: begin
if (((cdi==1'b1) && ((data_in & CHID)==CHID) && (addr == c_STOP)) || (stim_finish==1'b1)) begin
    // only stop stimulation when a stop command is received.
    // OR stop stimulation when the number of stimulation reached set value
    next_state=IDLE;
end else if (tmp_stim_mode[1:0]!=2'b00 && stim_finish ==1'b0) begin
    next_state=STIM; // otherwise, stay within the current state.
end else begin
    next_state=ERR;
end
end

LowZ: begin
if (((cdi==1'b1) && ((data_in & CHID)==CHID) && (addr == c_STOP)) || (stim_finish==1'b1)) begin
    // only stop stimulation when a stop command is received.
    // OR stop stimulation when the number of stimulation reached set value
    next_state=IDLE;
end else begin
    next_state=LowZ;
end

RESET: next_state=IDLE;
CAL: begin
if (cal_done == 1'b0) begin
    next_state = CAL;
end else begin
next_state = IDLE;
end
end

PRGCAL: begin
if (set_cal == 1'b0) begin
next_state = PRGCAL;
end else begin
next_state = CAL;
end
end

PRGWAV: begin
if (reg_mem_ergodic==1'b1) begin
next_state=PRGTIM;
end else begin
next_state=PRGWAV;
end
end

PRGCHG: begin
if (set_charge) begin
next_state=PRGTIM;
end else begin
next_state=PRGCHG;
end
end

PRGTIM: begin
if (read_setup) begin
next_state=IDLE;
end else begin
next_state=PRGTIM;
end
end

ERR: next_state=IDLE;
default: next_state=ERR;
endcase
end

always @(posedge clk or negedge rst) //sequential logic, determine the outputs
begin
if (!rst) begin
// hard reset all the outputs
data_out<=16'h0000;
data_check <= 1'b0;
errflag <= 1'b0;
set_charge <= 1'b0;
read_setup <= 1'b0;
channel_set <= 1'b0;
rst_stim <= 1'b1;
data_ready <=1'b0;
stim_mode <= 3'b000;
calibration <= 1'b0;
lowz_state <= 1'b0;
set_cal <= 1'b0;
end else begin
case (state)
IDLE:begin
data_out <= 16'h0000;
set_charge <= 1'b0;
read_setup <= 1'b0;
rst_stim <= 1'b1;
data_ready <=1'b0;
end
stim_mode <= 3'b000;
calibration <= 1'b0;
lowz_state <= 1'b0;
end

STIM: begin
  data_out <=16'h0000; //High-Z state
  stim_mode <= tmp_stim_mode;
calibration <= 1'b0;
lowz_state <= 1'b0;
case (tmp_stim_mode)
  I_STIM: begin
    set_charge <= 1'b0;
    read_setup <= 1'b0;
    rst_stim <= 1'b1;
    data_ready <=1'b0;
  end
  V_STIM: begin
    set_charge <= 1'b0;
    read_setup <= 1'b0;
    rst_stim <= 1'b1;
    data_ready <=1'b0;
  end
  C_STIM: begin
    set_charge <= 1'b0;
    read_setup <= 1'b0;
    rst_stim <= 1'b1;
    data_ready <=1'b0;
  end
  I_STIM_a: begin
    set_charge <= 1'b0;
    read_setup <= 1'b0;
    rst_stim <= 1'b1;
    data_ready <=1'b0;
  end
  V_STIM_a: begin
    set_charge <= 1'b0;
    read_setup <= 1'b0;
    rst_stim <= 1'b1;
    data_ready <=1'b0;
  end
  C_STIM_a: begin
    set_charge <= 1'b0;
    read_setup <= 1'b0;
    rst_stim <= 1'b1;
    data_ready <= 1'b0;
end
case
end
endcase

LowZ: begin
  data_check <= 1'b1;
  set_charge <= 1'b0;
  read_setup <= 1'b0;
  rst_stim <= 1'b1;
  data_ready <=1'b0;
  stim_mode <= 3'b000;
calibration <= 1'b0;
lowz_state <= 1'b1;
end

CAL: begin
  calibration <= 1'b1;
lowz_state <= 1'b0;
end
RESET: begin
// hard reset all the outputs

data_out <= 16'h0000;
data_check <= 1'b0;
errflag <= 1'b0;
set_charge <= 1'b0;
read_setup <= 1'b0;
channel_set <= 1'b0;
rst_stim <= 1'b0;
data_ready <= 1'b0;
stim_mode <= 3'b0000;
calibration <= 1'b0;
lowz_state <= 1'b1;
end

ERR: begin
  errflag <= 1'b1;
end

PRGWAV: begin
  data_check <= 1'b0;
data_out <= data_in;
read_setup <= 1'b0;
set_charge <= 1'b0;
rst_stim <= 1'b1;
if (ch_selected) begin
  data_ready <= 1'b1;
  end else begin
  data_ready <= 1'b0;
end
  calibration <= 1'b0;
lowz_state <= 1'b0;
end

PRGCAL: begin
  data_check <= 1'b0;
data_out <= data_in;
read_setup <= 1'b0;
if (ch_selected && !set_cal) begin
  set_cal <= 1'b1;
  end else begin
  set_cal <= 1'b0;
end
  rst_stim <= 1'b1;
data_ready <= 1'b0;
calibration <= 1'b0;
lowz_state <= 1'b0;
end

PRGCHG: begin
  data_check <= 1'b0;
data_out <= data_in;
read_setup <= 1'b0;
if (ch_selected && !set_charge) begin
  set_charge <= 1'b1;
  end else begin
  set_charge <= 1'b0;
end
  rst_stim <= 1'b1;
data_ready <= 1'b0;
calibration <= 1'b0;
lowz_state <= 1'b0;
  // active_chg_bal <= 1'b0;
end

PRGTIM: begin
  data_check <= 1'b0;
  if (ch_selected && !read_setup) begin
    read_setup <= 1'b1;
  end
end else begin
    read_setup <= 1'b0;
end // generate a pulse on read_setup for other stimulation
      FSMs to get the timing setup.
channel_set <= 1'b1;
data_out <= data_in;
set_charge <= 1'b0;
rst_stim <= 1'b1;
data_ready <= 1'b0;
calibration <= 1'b0;
lowz_state <= 1'b0;
end
dencase
end
endmodule

Listing A.3: Stimulation control FSM
inv_pos_x2;

// interface to active charge balancing
input p_chg_balance, n_chg_balance;
// output check balance
wire chg_balance;

assign chg_balance = p_chg_balance & n_chg_balance;

// interface to charge sensing
input Cmp_C1, Cmp_C2;
output reg C1_Charge, Inv_C1_Chg, C1_Stim, Inv_C1_Stim;
output reg C2_Charge, Inv_C2_Chg, C2_Stim, Inv_C2_Stim;
output reg Pos_CSTIM, Neg_CSTIM;
wire charge_clk;

// interface to DAC mux
output reg Voltage_Sel, Inv_Vol_Sel;
output reg Charge_Sel, Inv_Chg_Sel;

// switch control signals
output reg Short_Sel, Inv_Shrt_Sel;
output reg Sample_Sel, Inv_Sample_Sel;

// interface to 3 window comparators for calibration threshold voltage
input [5:0] cal_data;
output reg cal_err;
reg data_ready, dly_Cmp_C1;

// internal variables
reg [2:0] state, next_state;
reg token_IDLE, token_STIM, token_SHORT, token_ERR, token_IPD, token_CSTIM,
   token_PCIE, token_NCAL;
reg cycle_finish, charge_finish, delay_finish, waveform_finish;
reg [7:0] dur_cnt;
reg [5:0] short_cnt;
reg [9:0] rpt_cnt;
reg [13:0] charge_cnt;
reg [7:0] duration;
reg [1:0] delay_cnt;
reg [9:0] rpt_number;
reg [5:0] short_length;
reg [2:0] reg_stim_mode;
wire [2:0] stim_mode;
reg [1:0] ipd_duration;
reg [13:0] target_charge;
reg vth_saved;
reg [7:0] clk_cnt;
reg threshold_ready, dur_finish;
reg [5:0] p_threshold, n_threshold;
reg send_charge;
reg p_cal_done, n_cal_done, sampled, ovfl_status, ideal_status;
wire enable;
input rst;
input clk; //1 MHz, used for waveform generation.
assign charge_clk = Cmp_C1 | Cmp_C2;

// State Variables
parameter [2:0] IDLE='b000, STIM='b010, SHORT='b011, ERR='b001, IPD='b110, CSTIM='b111, P_CAL='b100, N_CAL='b101;

// Starts read out the data from the RAM
assign enable = stim_mode_in[1] | stim_mode_in[0];

always @(posedge clk or negedge rst) begin
    if (!rst) begin
        // RST
        state <= IDLE;
    end
    else begin
        state <= next_state;
    end
end

always @(posedge clk or negedge rst) begin
    if (!rst) begin
        // RST
        state <= IDLE;
    end
    else begin
        state <= next_state;
    end
end

always @(posedge clk or negedge rst) begin
    if (!rst) begin
        // RST
        state <= IDLE;
    end
    else begin
        state <= next_state;
    end
end

// Calculate the next states
always @(state, chg_balance, stim_finish, waveform_finish, charge_finish, cycle_finish, delay_finish, enable, calibration, cal_done, p_cal_done, n_cal_done, errflag, cal_err, reg_stim_mode[1:0]) begin
    case (state)
        IDLE: begin
            if (!errflag) begin
                if (enable & !calibration) begin
                    next_state = STIM;
                end
                else if (calibration & !cal_done) begin
                    next_state = N_CAL;
                end
                else begin
                    next_state = IDLE;
                end
            end
            token_IDLE = 1'b1;
            token_STIM = 1'b0;
            token_SHORT = 1'b0;
            token_ERR = 1'b0;
            token_IPD = 1'b0;
            token_CSTIM = 1'b0;
            token_PCAL = 1'b0;
            token_NCAL = 1'b0;
        end
        STIM: begin
            if (waveform_finish & (reg_stim_mode[1:0]==2'b10 || reg_stim_mode[1:0]==2'b01)) begin
                next_state = SHORT;
            end
            end else
if (charge_finish && reg_stim_mode[1:0]==2'b1) begin
  next_state = IPD;
end else begin
  next_state = STIM;
end

token_IDLE = 1'b0;
token_STIM = 1'b1;
token_SHORT = 1'b0;
token_ERR = 1'b0;
token_IPD = 1'b0;
token_CSTIM = 1'b0;
token_PCAL = 1'b0;
token_NCAL = 1'b0;
end

SHORT: begin
  if (calibration) begin
    if (cycle_finish) begin
      if (!p_cal_done) begin
        next_state = P_CAL;
      end else if (cal_done) begin
        next_state = IDLE;
      end else begin
        next_state = SHORT;
      end
    end else begin
      next_state = SHORT;
    end
  end else if (cycle_finish && !enable && chg_balance) begin
    next_state = IDLE;
  end else begin
    if (cycle_finish) begin
      if (chg_balance && !stim_finish) begin
        // charge is NOT balanced when the cycle finished, as well as the stimulation
        next_state = ERR;
      end else begin
        next_state = SHORT;
      end
    end else begin
      next_state = SHORT;
    end
  end
  token_IDLE = 1'b0;
token_STIM = 1'b0;
token_SHORT = 1'b1;
token_ERR = 1'b0;
token_IPD = 1'b0;
token_CSTIM = 1'b0;
token_PCAL = 1'b0;
token_NCAL = 1'b0;
end
IPD: begin
    if (delay_finish) begin
        next_state = CSTIM;
    end else if (!delay_finish) begin
        next_state = IPD;
    end else begin
        next_state = ERR;
    end
    token_IDLE = 1'b0;
    token_STIM = 1'b0;
    token_SHORT = 1'b0;
    token_ERR = 1'b0;
    token_IPD = 1'b1;
    token_CSTIM = 1'b0;
    token_PCAL = 1'b0;
    token_NCAL = 1'b0;
end
CSTIM: begin
    if (charge_finish) begin
        if (reg_stim_mode[1:0] == 2'b11) begin
            next_state = SHORT;
        end else begin
            next_state = ERR;
        end
    end else begin
        next_state = CSTIM;
    end
    token_IDLE = 1'b0;
    token_STIM = 1'b0;
    token_SHORT = 1'b0;
    token_ERR = 1'b0;
    token_IPD = 1'b1;
    token_CSTIM = 1'b0;
    token_PCAL = 1'b0;
    token_NCAL = 1'b0;
end
ERR: begin
    next_state = IDLE;
    token_IDLE = 1'b0;
    token_STIM = 1'b0;
    token_SHORT = 1'b0;
    token_ERR = 1'b1;
    token_IPD = 1'b0;
    token_CSTIM = 1'b0;
    token_PCAL = 1'b0;
    token_NCAL = 1'b0;
end
P_CAL: begin
    // rebalancing the charge after calibration
    if (!cal_err) begin
        if (p_cal_done) begin
            next_state = SHORT;
        end else begin
            next_state = P_CAL;
        end
    end else begin
        next_state = ERR;
    end
    token_IDLE = 1'b0;
    token_STIM = 1'b0;
    token_SHORT = 1'b0;
    token_ERR = 1'b0;
```verilog
// rebalancing the charge after calibration
if (!cal_err) begin
  if (n_cal_done) begin
    next_state = SHORT;
  end
  else begin
    next_state = N_CAL;
  end
end else begin
  next_state = ERR;
end
```

```verilog
always @(posedge clk or negedge rst)
begin : CLK_GEN //"Generate reference clock for shorting and inter phase delay, 16us"
  if (!rst) begin
    // rst
clock_cnt <= 8'h00;
  end
  else if (token_SHORT || token_IPD) begin
    if (clock_cnt != 8'b1111_1111) begin
      clock_cnt <= clock_cnt + 8'h01;
    end
    else begin
      clock_cnt <= 8'h00;
    end
  end
end
```
clk_cnt <= 8'h00;

end

end

///////////////////////////////////////////////////////////////////////////////////////////////
// END - Generate Different Clock signals
///////////////////////////////////////////////////////////////////////////////////////////////

///////////////////////////////////////////////////////////////////////////////////////////////
// Read stimulation setup from the Channel FSM
///////////////////////////////////////////////////////////////////////////////////////////////

reg time_saved, charge_saved;
always @(posedge clk or negedge rst)
begin : SET_TIME //"Read timing setup"
if (!rst) begin
  // rst
  rpt_number <= 10'b00_0000_0000;
  short_length <= 6'b00_0000;
  time_saved <= 1'b0;
end else
begin
  if (!calibration && read_setup) begin
    if (!time_saved) begin
      rpt_number <= setup_in[15:6];
      short_length <= setup_in[5:0];
      time_saved <= 1'b1;
    end
  end else if (calibration) begin
    // setting the shorting phase for calibration.
    // longest shorting duration is used.
    rpt_number <= 10'b00_0000_0000;
    short_length <= 6'b111111;
    time_saved <= 1'b0;
  end else begin
    time_saved <= 1'b0;
  end
end

end // read charge setup
always @(posedge clk or negedge rst)
begin : SET_CHG //"read charge setup"
if (!rst) begin
  // rst
  target_charge <= 14'h0000;
  ipd_duration <= 2'b00;
  charge_saved <= 1'b0;
end else
begin
  if (set_charge) begin
    if (!charge_saved) begin
      target_charge <= setup_in[15:2];
      ipd_duration <= setup_in[1:0];
      charge_saved <= 1'b1;
    end
  end else begin
    charge_saved <= 1'b0;
  end
end

end
always @ (posedge clk or negedge rst)
begin : OUTPUTS_DAC
  // "Generate the data feed for DAC"
  if (!rst) begin
    // rst
    waveform_n <= 5'b00000;
    waveform <= 5'b11111;
    duration <= 8'h00;
    addr <= 4'b0000;
    threshold_ready <= 1'b0;
    last_one <= 1'b0;
  end
  else begin
    if (token_STIM && (reg_stim_mode[1:0]==2'b10 || reg_stim_mode [1:0]==2'b01)) begin
      if (dur_finish) begin
        if (!last_one || one_cycle_end) begin
          addr <= addr + 4'b0001;
        end
        waveform_n <= data_in[12:8];
        waveform <= ~data_in[12:8];
        duration <= data_in[7:0];
      end
      else begin
        if (!one_cycle_end) begin
          if (addr == 4'b1111 && dur_finish & & !waveform_finish) begin
            last_one <= 1'b1;
          end
          end else if (waveform_finish) begin
          last_one <= 1'b0;
        end
        end
      else begin
        if (addr == 4'b1110 & & dur_finish & & !waveform_finish) begin
          last_one <= 1'b1;
        end
        end else if (waveform_finish) begin
          last_one <= 1'b0;
        end
        end
      end
    else if (((token_STIM || token_CSTIM || token_IPD) &&
      reg_stim_mode[1:0]==2'b11) || (token_NCAL || token_PCAL))
    begin
      if (token_STIM || token_NCAL) begin
        waveform_n <= n_threshold [4:0];
        waveform <= ~n_threshold [4:0];
      end
      else if (token_CSTIM || token_PCAL || token_IPD) begin
        waveform_n <= p_threshold [4:0];
        waveform <= ~p_threshold [4:0];
      end
      threshold_ready <= 1'b1;
duration <= 8'h00;
else if (token_SHORT) begin
    if (!p_chg_balance) begin
        waveform_n <= p_threshold [4:0];
        waveform <= ~ p_threshold [4:0];
        threshold_ready <= 1'b1;
    end
    else if (!n_chg_balance) begin
        waveform_n <= n_threshold [4:0];
        waveform <= ~ n_threshold [4:0];
        threshold_ready <= 1'b1;
    end
    else if (chg_balance) begin
        if (calibration & n_cal_done & !p_cal_done) begin
            waveform_n <= p_threshold [4:0];
            waveform <= ~ p_threshold [4:0];
            threshold_ready <= 1'b0;
        end
        else if (reg_stim_mode[1:0]==2'b11) begin
            waveform_n <= n_threshold [4:0];
            waveform <= ~ n_threshold [4:0];
        end
        else begin
            waveform_n <= 5'b00000;
            waveform <= 5'b11111;
            threshold_ready <= 1'b0;
        end
    end
else if (token_STIM) begin
    if (reg_stim_mode[1:0]==2'b01 || reg_stim_mode [1:0]==2'b10) begin
        if (dur_cnt == duration) begin
            dur_cnt <= 8'h00;
        end
        else begin
            dur_cnt <= dur_cnt + 8'h01;
        end
    end
end
always @(posedge clk or negedge rst)
begin : OUTPUTS_WAV_DUR
    //"Controls the duration of each waveform"
    if (!rst) begin
        dur_cnt <= 8'h00;
    end
else begin
    if (token_STIM & (reg_stim_mode[1:0]==2'b01 || reg_stim_mode [1:0]==2'b10)) begin
        if (dur_cnt == duration) begin
            dur_cnt <= 8'h00;
        end
        else begin
            dur_cnt <= dur_cnt + 8'h01;
        end
    end
end
always @(dur_cnt,duration,last_one,one_cycle_end)
begin
    if (dur_cnt == duration) begin
        dur_finish = 1'b1;
end else begin
  dur_finish = 1'b0;
end
if (last_one) begin
  if ((dur_cnt == (duration - 8'h01)) && !one_cycle_end) begin
    waveform_finish = 1'b1;
  end
  else if (one_cycle_end && (dur_cnt == duration)) begin
    waveform_finish = 1'b1;
  end
  else begin
    waveform_finish = 1'b0;
  end
end else begin
  waveform_finish = 1'b0;
end
always @(posedge clk or negedge rst)
begin : OUTPUTS_SWITCH // "scale and polarity control to DAC"
if (!rst) begin
  neg_stim <= 1'b0;
  neg_x1 <= 1'b0;
  neg_x2 <= 1'b0;
  pos_stim <= 1'b1;
  pos_x1 <= 1'b1;
  pos_x2 <= 1'b1;
  inv_neg_stim <= 1'b1;
  inv_neg_x1 <= 1'b1;
  inv_neg_x2 <= 1'b1;
  inv_pos_stim <= 1'b0;
  inv_pos_x1 <= 1'b0;
  inv_pos_x2 <= 1'b0;
end else begin
  if (reg_stim_mode[1:0]!=2'b11 && reg_stim_mode[1:0]!=2'b00 &&
    token_STIM) begin
    case (data_in[14:13])
    2'b00: begin // Iz stimulation
      case (data_in[15])
      1'b0: begin
        neg_stim <= 1'b1;
        neg_x1 <= 1'b0;
        neg_x2 <= 1'b0;
        pos_stim <= 1'b1;
        pos_x1 <= 1'b1;
        pos_x2 <= 1'b1;
        inv_neg_stim <= 1'b0;
        inv_neg_x1 <= 1'b1;
        inv_neg_x2 <= 1'b1;
        inv_pos_stim <= 1'b0;
        inv_pos_x1 <= 1'b0;
        inv_pos_x2 <= 1'b0;
      end
      1'b1: begin
        neg_stim <= 1'b0;
        neg_x1 <= 1'b0;
        neg_x2 <= 1'b0;
        pos_stim <= 1'b0;
        pos_x1 <= 1'b1;
        pos_x2 <= 1'b1;
        inv_neg_stim <= 1'b1;
      end
      default: begin
        waveform_finish = 1'b0;
      end
    end
    2'b01: begin
      neg_stim <= 1'b1;
      neg_x1 <= 1'b1;
      neg_x2 <= 1'b1;
      pos_stim <= 1'b1;
      pos_x1 <= 1'b1;
      pos_x2 <= 1'b1;
      waveform_finish = 1'b1;
    end
    2'b10: begin
      waveform_finish = 1'b1;
      neg_stim <= 1'b1;
      neg_x1 <= 1'b1;
      neg_x2 <= 1'b1;
      pos_stim <= 1'b1;
      pos_x1 <= 1'b1;
      pos_x2 <= 1'b1;
    end
    default: begin
      waveform_finish = 1'b0;
    end
  end
  else begin
    waveform_finish = 1'b0;
  end
end
inv_neg_x1 <= 1'b1;
inv_neg_x2 <= 1'b1;
inv_pos_stim <= 1'b1;
inv_pos_x1 <= 1'b0;
inv_pos_x2 <= 1'b0;
end

default: begin
  neg_stim <= 1'b0;
neg_x1 <= 1'b0;
neg_x2 <= 1'b0;
  pos_stim <= 1'b1;
pos_x1 <= 1'b1;
pos_x2 <= 1'b1;
  inv_neg_stim <= 1'b1;
inv_neg_x1 <= 1'b1;
inv_neg_x2 <= 1'b1;
inv_pos_stim <= 1'b0;
inv_pos_x1 <= 1'b0;
inv_pos_x2 <= 1'b0;
end
endcase

2'b01: begin // 2x stimulation
  case (data_in[15])
    1'b0: begin
      neg_stim <= 1'b1;
neg_x1 <= 1'b1;
neg_x2 <= 1'b0;
      pos_stim <= 1'b1;
pos_x1 <= 1'b1;
pos_x2 <= 1'b1;
      inv_neg_stim <= 1'b0;
inv_neg_x1 <= 1'b0;
inv_neg_x2 <= 1'b1;
inv_pos_stim <= 1'b0;
inv_pos_x1 <= 1'b0;
inv_pos_x2 <= 1'b0;
end
    1'b1: begin
      neg_stim <= 1'b0;
neg_x1 <= 1'b0;
neg_x2 <= 1'b0;
      pos_stim <= 1'b0;
pos_x1 <= 1'b0;
pos_x2 <= 1'b0;
      inv_neg_stim <= 1'b1;
inv_neg_x1 <= 1'b1;
inv_neg_x2 <= 1'b0;
inv_pos_stim <= 1'b1;
inv_pos_x1 <= 1'b1;
inv_pos_x2 <= 1'b0;
end
    default: begin
      neg_stim <= 1'b0;
neg_x1 <= 1'b0;
neg_x2 <= 1'b0;
      pos_stim <= 1'b0;
pos_x1 <= 1'b1;
pos_x2 <= 1'b1;
      inv_neg_stim <= 1'b1;
inv_neg_x1 <= 1'b1;
inv_neg_x2 <= 1'b1;
inv_pos_stim <= 1'b0;
end
endcase
inv_pos_x1 <= 1’b0;
inv_pos_x2 <= 1’b0;
endcase
end: begin // 3x stimulation
case (data_in[15])
1’b0: begin
  neg_stim <= 1’b1;
  neg_x1 <= 1’b0;
  neg_x2 <= 1’b0;
  pos_stim <= 1’b1;
  pos_x1 <= 1’b1;
  pos_x2 <= 1’b1;
  inv_neg_stim <= 1’b0;
  inv_neg_x1 <= 1’b1;
  inv_neg_x2 <= 1’b0;
  inv_pos_stim <= 1’b0;
  inv_pos_x1 <= 1’b0;
  inv_pos_x2 <= 1’b0;
end
1’b1: begin
  neg_stim <= 1’b0;
  neg_x1 <= 1’b0;
  neg_x2 <= 1’b0;
  pos_stim <= 1’b1;
  pos_x1 <= 1’b1;
  pos_x2 <= 1’b1;
  inv_neg_stim <= 1’b1;
  inv_neg_x1 <= 1’b1;
  inv_neg_x2 <= 1’b1;
  inv_pos_stim <= 1’b1;
  inv_pos_x1 <= 1’b0;
  inv_pos_x2 <= 1’b0;
end
default: begin
  neg_stim <= 1’b0;
  neg_x1 <= 1’b0;
  neg_x2 <= 1’b0;
  pos_stim <= 1’b1;
  pos_x1 <= 1’b1;
  pos_x2 <= 1’b1;
  inv_neg_stim <= 1’b1;
  inv_neg_x1 <= 1’b1;
  inv_neg_x2 <= 1’b1;
  inv_pos_stim <= 1’b0;
  inv_pos_x1 <= 1’b0;
  inv_pos_x2 <= 1’b0;
end
endcase
end: begin // 4x stimulation
case (data_in[15])
1’b0: begin
  neg_stim <= 1’b1;
  neg_x1 <= 1’b1;
  neg_x2 <= 1’b1;
  pos_stim <= 1’b1;
  pos_x1 <= 1’b1;
  pos_x2 <= 1’b1;
  inv_neg_stim <= 1’b0;
  inv_neg_x1 <= 1’b0;
  inv_neg_x2 <= 1’b0;
end
endcase
end: begin // 2x stimulation
case (data_in[15])
1’b0: begin
  neg_stim <= 1’b1;
  neg_x1 <= 1’b1;
  neg_x2 <= 1’b1;
  pos_stim <= 1’b1;
  pos_x1 <= 1’b1;
  pos_x2 <= 1’b1;
  inv_neg_stim <= 1’b0;
  inv_neg_x1 <= 1’b0;
  inv_neg_x2 <= 1’b0;
end
endcase
end
inv_pos_stim <= 1'b0;
inv_pos_x1 <= 1'b0;
inv_pos_x2 <= 1'b0;
end

1'b1: begin
neg_stim <= 1'b0;
neg_x1 <= 1'b0;
neg_x2 <= 1'b0;
pos_stim <= 1'b0;
pos_x1 <= 1'b0;
pos_x2 <= 1'b0;
inv_neg_stim <= 1'b1;
inv_neg_x1 <= 1'b1;
inv_neg_x2 <= 1'b1;
inv_pos_stim <= 1'b1;
inv_pos_x1 <= 1'b1;
inv_pos_x2 <= 1'b1;
end
default: begin
neg_stim <= 1'b0;
neg_x1 <= 1'b0;
neg_x2 <= 1'b0;
pos_stim <= 1'b1;
pos_x1 <= 1'b1;
pos_x2 <= 1'b1;
inv_neg_stim <= 1'b1;
inv_neg_x1 <= 1'b1;
inv_neg_x2 <= 1'b1;
inv_pos_stim <= 1'b0;
inv_pos_x1 <= 1'b0;
inv_pos_x2 <= 1'b0;
end
default: begin // no stimulation
neg_stim <= 1'b0;
neg_x1 <= 1'b0;
neg_x2 <= 1'b0;
pos_stim <= 1'b1;
pos_x1 <= 1'b1;
pos_x2 <= 1'b1;
end
else begin
neg_stim <= 1'b0;
neg_x1 <= 1'b0;
neg_x2 <= 1'b0;
pos_stim <= 1'b1;
pos_x1 <= 1'b1;
pos_x2 <= 1'b1;
inv_neg_stim <= 1'b1;
inv_neg_x1 <= 1'b1;
inv_neg_x2 <= 1'b1;
inv_pos_stim <= 1'b0;
inv_pos_x1 <= 1'b0;
inv_pos_x2 <= 1'b0;
end
end

// deliver charge during Charge stimulation

reg cstim_clk, cstim_start, cstim_on;
always @(end_charge, Cmp_C1, Cmp_C2, cstim_start, cstim_on, calibration, data_ready, dly_Cmp_C1) begin
  if (!calibration) begin
    if (cstim_start && !cstim_on) begin
      cstim_clk = 1'b1;
    end
    else if (!cstim_start) begin
      cstim_clk = 1'b0;
    end
    else begin
      cstim_clk = Cmp_C1 | Cmp_C2;
    end
  end
  else begin
    if (send_charge && !cstim_on) begin
      cstim_clk = 1'b1;
    end
    else if (!send_charge) begin
      cstim_clk = 1'b0;
    end
    else if (dly_Cmp_C1) begin
      cstim_clk = data_ready;
    end
    else begin
      cstim_clk = Cmp_C1;
    end
  end
end

always @(posedge clk or negedge rst) begin
  if (!rst) begin
    // reset
    dly_Cmp_C1 <= 1'b0;
  end
  else begin
    dly_Cmp_C1 <= Cmp_C1;
  end
end

always @(posedge clk or negedge rst) begin
  if (!rst) begin
    // reset
    cstim_start <= 1'b0;
  end
  else begin
    if (Charge_SEL && !calibration) begin
      cstim_start <= 1'b1;
    end else begin
      cstim_start <= 1'b0;
    end
  end
end

always @(posedge cstim_clk or negedge rst) begin
  if (!rst) begin
    // rst
    C1_Charge <= 1'b1;
    Inv_C1_Chg <= 1'b0;
    C1_Stim <= 1'b0;
    Inv_C1_Stim <= 1'b1;
    C2_Charge <= 1'b1;
    Inv_C2_Chg <= 1'b0;
    C2_Stim <= 1'b0;
  end
end
Inv_C2_Stim <= 1'b1;
cstim_on <= 1'b0;
Sample_Sel <= 1'b0;
Inv_Sample_Sel <= 1'b1;
end
  if (Cmp_C1) begin
    // if unit cap 1 needs recharge
    C1_Charge <= 1'b1;
    Inv_C1_Chg <= 1'b0;
    C1_Stim <= 1'b0;
    Inv_C1_Stim <= 1'b1;
    C2_Charge <= 1'b0;
    Inv_C2_Chg <= 1'b1;
    C2_Stim <= 1'b1;
    Inv_C2_Stim <= 1'b0;
  end else if (Cmp_C2) begin
    // if unit cap 2 needs recharge
    C1_Charge <= 1'b0;
    Inv_C1_Chg <= 1'b1;
    C1_Stim <= 1'b1;
    Inv_C1_Stim <= 1'b0;
    C2_Charge <= 1'b1;
    Inv_C2_Chg <= 1'b0;
    C2_Stim <= 1'b0;
    Inv_C2_Stim <= 1'b1;
  end
else begin
  // this happens to kick off the stimulation by start stimulation using C1.
  C1_Charge <= 1'b0;
  Inv_C1_Chg <= 1'b1;
  C1_Stim <= 1'b1;
  Inv_C1_Stim <= 1'b0;
  C2_Charge <= 1'b1;
  Inv_C2_Chg <= 1'b0;
  C2_Stim <= 1'b0;
  Inv_C2_Stim <= 1'b1;
cstim_on <= 1'b1;
end
  C1_Charge <= 1'b1;
  Inv_C1_Chg <= 1'b0;
  C1_Stim <= 1'b0;
  Inv_C1_Stim <= 1'b1;
  C2_Charge <= 1'b1;
  Inv_C2_Chg <= 1'b0;
  C2_Stim <= 1'b0;
  Inv_C2_Stim <= 1'b1;
cstim_on <= 1'b0;
Sample_Sel <= 1'b0;
Inv_Sample_Sel <= 1'b1;
end
else if (calibration) begin
  // in calibration state, the charging is triggered via control
  if ((Cmp_C1 || Cmp_C2) && !data_ready) begin
if one charge is send, stop sending charge.

// Cmp_C1 and Cmp_C2 will return to zero.
C1_Charge <= 1'b0;
Inv_C1_Chg <= 1'b1;
C1_Stim <= 1'b0;
Inv_C1_Stim <= 1'b1;
C2_Charge <= 1'b1;
Inv_C2_Chg <= 1'b0;
C2_Stim <= 1'b0;
Inv_C2_Stim <= 1'b1;
Sample_SEL <= 1'b1;
Inv_Sample_SEL <= 1'b0;
end
else if (data_ready) begin
C1_Charge <= 1'b1;
Inv_C1_Chg <= 1'b0;
Sample_SEL <= 1'b0;
Inv_Sample_SEL <= 1'b1;
cstim_on <= 1'b0;
end
else begin
// this happens to kick off the stimulation by start stimulation using C1.
// I am trusting matching between C1 and C2, therefore calibration will only be done on C1.
C1_Charge <= 1'b0;
Inv_C1_Chg <= 1'b1;
C1_Stim <= 1'b1;
Inv_C1_Stim <= 1'b0;
C2_Charge <= 1'b1;
Inv_C2_Chg <= 1'b0;
C2_Stim <= 1'b0;
Inv_C2_Stim <= 1'b1;
Sample_SEL <= 1'b1;
Inv_Sample_SEL <= 1'b0;
cstim_on <= 1'b1;
end
end begin

else begin
cstim_on <= 1'b0;
end
end

// save stim_mode once stimulation starts, trigger by the stimulation clock in I/V mode and start command in C mode.
always @(posedge clk or negedge rst) begin
if (!rst) begin
// rst
reg_stim_mode <= 3'b000;
end
else if (token_STIM && reg_stim_mode == 3'b000) begin
reg_stim_mode <= stim_mode_in;
end else if (token_IDLE) begin
reg_stim_mode <= 3'b000;
end
end
assign stim_mode = reg_stim_mode | stim_mode_in;

// determine the outputs for other states.
always @(posedge clk or negedge rst) begin
if (!rst) begin
// Current_SEL <= 1'b0;

end
// Inv_Cur_Sel <= 1'b1;
Voltage_Sel <= 1'b0;
Inv_Vol_Sel <= 1'b1;
Charge_Sel <= 1'b0;
Inv_Chg_Sel <= 1'b1;
stim_ready <= 1'b1;
Short_Sel <= 1'b0;
Inv_Shrt_Sel <= 1'b1;
Pos_CSTIM <= 1'b0;
Neg_CSTIM <= 1'b1;
errflag <= 1'b0;
end else
if (token_ERR) begin
errflag <= 1'b1;
end
else if (token_STIM) begin
  case (reg_stim_mode[1:0]) // stim_mode is not registered yet.
    2'b00: begin
      Voltage_Sel <= 1'b0;
      Inv_Vol_Sel <= 1'b1;
      Charge_Sel <= 1'b0;
      Inv_Chg_Sel <= 1'b1;
      stim_ready <= 1'b0;
      Short_Sel <= 1'b0;
      Inv_Shrt_Sel <= 1'b1;
    end
    2'b01: begin
      Voltage_Sel <= 1'b0;
      Inv_Vol_Sel <= 1'b1;
      Charge_Sel <= 1'b0;
      Inv_Chg_Sel <= 1'b1;
      stim_ready <= 1'b0;
      Short_Sel <= 1'b0;
      Inv_Shrt_Sel <= 1'b1;
    end
    2'b10: begin
      Voltage_Sel <= 1'b1;
      Inv_Vol_Sel <= 1'b0;
      Charge_Sel <= 1'b0;
      Inv_Chg_Sel <= 1'b1;
      stim_ready <= 1'b0;
      Short_Sel <= 1'b0;
      Inv_Shrt_Sel <= 1'b1;
    end
    2'b11: begin
      Voltage_Sel <= 1'b0;
      Inv_Vol_Sel <= 1'b1;
      Charge_Sel <= 1'b1;
      Inv_Chg_Sel <= 1'b0;
      stim_ready <= 1'b0;
      Short_Sel <= 1'b0;
      Inv_Shrt_Sel <= 1'b1;
    end
  endcase
else if (token_CSTIM) begin
  if (reg_stim_mode[1:0] == 2'b11) begin
    Voltage_Sel <= 1'b0;
    Inv_Vol_Sel <= 1'b1;
    Charge_Sel <= 1'b1;
    Inv_Chg_Sel <= 1'b0;
  end
end
stim_ready <= 1'b0;
ShortSel <= 1'b0;
InvShrtSel <= 1'b1;
PosCSTIM <= 1'b1;
NegCSTIM <= 1'b0;

else if (token_IDLE) begin
    if (lowz_state) begin
        ShortSel <= 1'b1;
        InvShrtSel <= 1'b0;
    end else begin
        ShortSel <= 1'b0;
        InvShrtSel <= 1'b1;
    end
    VoltageSel <= 1'b0;
    InvVolSel <= 1'b1;
    ChargeSel <= 1'b0;
    InvChgSel <= 1'b1;
    stim_ready <= 1'b1;
    PosCSTIM <= 1'b0;
    NegCSTIM <= 1'b1;
end
else if (token_SHORT) begin
    if (calibration) begin
        ChargeSel <= 1'b0;
        InvChgSel <= 1'b1;
        if (n_cal_done && !p_cal_done) begin
            PosCSTIM <= 1'b1;
            NegCSTIM <= 1'b0;
        end else begin
            NegCSTIM <= 1'b1;
            PosCSTIM <= 1'b0;
        end
    end
    else begin
            if (!p_chg_balance) begin
                ChargeSel <= 1'b1;
                InvChgSel <= 1'b0;
                PosCSTIM <= 1'b0;
                NegCSTIM <= 1'b1;
            end else if (!n_chg_balance) begin
                ChargeSel <= 1'b1;
                InvChgSel <= 1'b0;
                PosCSTIM <= 1'b1;
                NegCSTIM <= 1'b0;
            end
        end
    end
else begin
    ChargeSel <= 1'b0;
    InvChgSel <= 1'b1;
    PosCSTIM <= 1'b0;
    NegCSTIM <= 1'b1;
end
VoltageSel <= 1'b0;
InvVolSel <= 1'b1;
stim_ready <= 1'b0;
ShortSel <= 1'b1;
InvShrtSel <= 1'b0;
end
else if (token_IPD) begin
Voltage_Sel <= 1'b0;
Inv_Vol_Sel <= 1'b1;
Charge_Sel <= 1'b0;
Inv_Chg_Sel <= 1'b1;
stim_ready <= 1'b0;
Short_Sel <= 1'b0;
Inv_Shrt_Sel <= 1'b1;
Pos_CSTIM <= 1'b1;
Neg_CSTIM <= 1'b0;
end
else if (token_PCAL) begin
Voltage_Sel <= 1'b0;
Inv_Vol_Sel <= 1'b1;
Charge_Sel <= 1'b1;
Inv_Chg_Sel <= 1'b0;
stim_ready <= 1'b0;
Short_Sel <= 1'b0;
Inv_Shrt_Sel <= 1'b1;
Pos_CSTIM <= 1'b1;
Neg_CSTIM <= 1'b0;
end
else if (token_NCAL) begin
Voltage_Sel <= 1'b0;
Inv_Vol_Sel <= 1'b1;
Charge_Sel <= 1'b1;
Inv_Chg_Sel <= 1'b0;
stim_ready <= 1'b0;
Short_Sel <= 1'b0;
Inv_Shrt_Sel <= 1'b1;
Pos_CSTIM <= 1'b0;
Neg_CSTIM <= 1'b1;
end
else begin
Voltage_Sel <= 1'b0;
Inv_Vol_Sel <= 1'b1;
Charge_Sel <= 1'b0;
Inv_Chg_Sel <= 1'b1;
stim_ready <= 1'b0;
Short_Sel <= 1'b0;
Inv_Shrt_Sel <= 1'b1;
Pos_CSTIM <= 1'b0;
Neg_CSTIM <= 1'b1;
end
end

always @(posedge clk or negedge rst) begin : CTRL_SHORT
// Controls the duration of shorting phase
if (!rst) begin
short_cnt <= 6'b00_0000;
cycle_finish <= 1'b0;
end
else begin
if (token_SHORT && clk_cnt == 8'b1111_1111) begin
if (short_cnt == short_length) begin

end
short_cnt <= 6'b00_0000;
end
else begin
short_cnt <= short_cnt + 6'b00_0001;
end
end
if (short_cnt == short_length && clk_cnt == 8'b1111_1111)
begin
cycle_finish <= 1'b1;
end else begin
cycle_finish <= 1'b0;
end
end

// determine when the inter-phase delay finish
always @(posedge clk or negedge rst) begin
if (!rst) begin
// rst
delay_cnt <= 2'b00;
delay_finish <= 1'b0;
end else begin
if (token_IPD && clk_cnt == 8'b1111_1111) begin
if (delay_cnt == ipd_duration) begin
delay_cnt <= 2'b00;
end else begin
delay_cnt <= delay_cnt + 2'b01;
end
end
if (token_IPD && delay_cnt == ipd_duration && clk_cnt == 8'b1111_1111) begin
delay_finish <= 1'b1;
end else begin
delay_finish <= 1'b0;
end
end

// determine when the whole stimulation finish
always @(posedge clk or negedge rst)
begin : CTRL_RPT //"Controls the repetition of the stimulation"
if (!rst) begin
// rst
rpt_cnt <= 10'b00_0000_0000;
stim_finish <= 1'b0;
end else begin
if (token_SHORT && cycle_finish) begin
if (rpt_number != 10'b11_1111_1111) begin // rpt_number = 8'hff for infinite loop.
if (rpt_cnt == rpt_number) begin
rpt_cnt <= 10'b00_0000_0000;
end else begin
rpt_cnt <= rpt_cnt + 10'b00_0000_0001;
end
end else if (token_IDLE) begin
rpt_cnt <= 10'b00_0000_0000;
end
if (rpt_cnt == rpt_number && token_SHORT && !calibration)
begin
  stim_finish <= 1'b1;
end else begin
  stim_finish <= 1'b0;
end
end

// determine when the charge delivery finish
reg charge_rst;

always @(posedge charge_clk or negedge charge_rst) begin
if (!charge_rst) begin
  // rst
  charge_cnt <= 14'b0000_0000_0000_00;
end else begin
  if (((token_STIM || token_CSTIM) && (reg_stim_mode[1:0]==2'b11)
    && !charge_finish)
    begin
    charge_cnt <= target_charge;
  end else begin
    charge_cnt <= charge_cnt + 14'b0000_0000_0000_01;
  end
end
always @(charge_cnt, target_charge) begin
if (charge_cnt == target_charge) begin
  charge_finish = 1'b1;
end else begin
  charge_finish = 1'b0;
end
end
always @(posedge clk or negedge rst) begin
if (!rst) begin
  // reset
  charge_rst <=1'b1;
end else begin
  if (!token_STIM && !token_CSTIM) begin
    charge_rst <= 1'b0;
  end else begin
    charge_rst <= 1'b1;
  end
end

// END - Generate signals to detect a phase finish
// Calibration the threshold voltage
// find the NEGATIVE and POSITIVE threshold voltage by decreasing from
the desired value
always @(posedge clk or negedge rst) begin
if (!rst) begin
  // rst threshold voultag to it's maximum value and calibration to a low value
  n_threshold <= 6'b010001;
p_threshold <= 6'b010001;
p_cal_done <= 1'b0;
n_cal_done <= 1'b0;
send_charge <= 1'b0;
data_ready <= 1'b0;
cal_err <= 1'b0;
cal_done <= 1'b0;
out_cal_done <= 1'b0;
sampled <= 1'b0;
nvfl_status <= 1'b0;
ideal_status <= 1'b0;
vth_saved <= 1'b0;
end
else begin
  if (set_cal) begin
    if (!vth_saved) begin
      p_threshold <= setup_in[15:10];
n_threshold <= setup_in[9:4];
vth_saved <= 1'b1;
    end
  end
  else begin
    vth_saved <= 1'b0;
    if (!cal_err && (token_PCAL || token_NCAL)) begin
      if (data_ready) begin
        data_ready <= 1'b0;
send_charge <= 1'b0;
sampled <= 1'b0;
      end
    end
    else if (send_charge && dly_Cmp_C1 && !sampled) begin
      if ((token_PCAL && !p_cal_done) || (token_NCAL && !n_cal_done)) begin
        if (p_threshold[5] || n_threshold[5]) begin
          cal_err <= 1'b1;
        end
      end
    end
    else begin
      case (cal_data)
        6'b101_011: begin
          if (token_PCAL) begin
            ideal_status <= 1'b1;
p_threshold <= p_threshold + 6'b000001;
          end
        end
        6'b111_011: begin
          if (token_PCAL) begin
            p_cal_done <= 1'b1;
            ideal_status <= 1'b1;
          end
        end
        6'b001_011: begin
          if (token_PCAL) begin
            if (token_PCAL)
          end
end
end
end
ovfl_status <= 1'b0;
ideal_status <= 1'b0;
p_threshold <= p_threshold + 6'b000001;
end else begin
cal_err <= 1'b1;
end
end

6'b110_011: begin
if (token_PCAL) begin
p_cal_done <= 1'b1;
ovfl_status <= 1'b1;
ideal_status <= 1'b0;
if (ovfl_status && ideal_status)
begin
p_threshold <= p_threshold - 6'b000001;
end
end
else if (token_NCAL) begin
n_cal_done <= 1'b1;
ovfl_status <= 1'b1;
ideal_status <= 1'b0;
if (ovfl_status && ideal_status)
begin
n_threshold <= n_threshold - 6'b000001;
end
end else begin
cal_err <= 1'b1;
end
end

//===================================NCAL=====================================
6'b110_101: begin
if (token_NCAL) begin
ideal_status <= 1'b1;
n_threshold <= n_threshold + 6'b000001;
end else begin
cal_err <= 1'b1;
end
end

6'b110_111: begin
if (token_NCAL) begin
n_cal_done <= 1'b1;
ovfl_status <= 1'b1;
ideal_status <= 1'b0;
end else begin
cal_err <= 1'b1;
end
end

6'b110_100: begin
if (token_NCAL) begin
ovfl_status <= 1'b0;
ideal_status <= 1'b0;
n_threshold <= n_threshold + 6'b000001;
end else begin
cal_err <= 1'b1;
end
end

default: begin
cal_err <= 1'b1;
endcase
end
end

else if (sampled) begin
data_ready <= 1'b1;
end

else if (!send_charge && !data_ready && !n_cal_done && token_NCAL && !p_cal_done && token_PCAL && threshold_ready) begin
send_charge <= 1'b1;
end

end

end

cal_done <= p_cal_done & n_cal_done;
out_cal_done <= cal_done & token_IDLE;
end
end

// END - Calibration the threshold voltage

// Generate power gating signal

always @(posedge clk or negedge rst) begin
if (!rst) begin
  // reset
  Current_mode <= 1'b0;
  Inv_Cur_mode <= 1'b1;
  Voltage_mode <= 1'b0;
  Inv_Vol_mode <= 1'b1;
  Charge_mode <= 1'b0;
  Inv_Chg_mode <= 1'b1;
  Cal_mode <= 1'b0;
  Inv_Cal_mode <= 1'b1;
  Channel_on <= 1'b0;
  Inv_Channel_on <= 1'b1;
end
else begin
  if (stim_mode != 3'b000 || calibration) begin
    Channel_on <= 1'b1;
    Inv_Channel_on <= 1'b0;
    if (!calibration) begin
      case (stim_mode[1:0])
        2'b01: begin
          // Current Stimulation
          Current_mode <= 1'b1;
          Inv_Cur_mode <= 1'b0;
          Voltage_mode <= 1'b0;
          Inv_Vol_mode <= 1'b1;
          if (stim_mode[2] == 1'b1) begin
            Charge_mode <= 1'b1;
            Inv_Chg_mode <= 1'b0;
          end else begin
            Charge_mode <= 1'b0;
            Inv_Chg_mode <= 1'b1;
          end
        end
      endcase
    end
  end
end
end

2'b10: begin
   // Voltage Stimulation
   Current_mode <= 1'b0;
   Inv_Cur_mode <= 1'b1;
   Voltage_mode <= 1'b1;
   Inv_Vol_mode <= 1'b0;
   if (stim_mode[2] == 1'b1) begin
      Charge_mode <= 1'b1;
      Inv_Chg_mode <= 1'b0;
   end else begin
      Charge_mode <= 1'b0;
      Inv_Chg_mode <= 1'b1;
   end
   end

2'b11: begin
   // Charge Stimulation
   Current_mode <= 1'b0;
   Inv_Cur_mode <= 1'b1;
   Voltage_mode <= 1'b0;
   Inv_Vol_mode <= 1'b1;
   Charge_mode <= 1'b1;
   Inv_Chg_mode <= 1'b0;
   end

default: begin
   Current_mode <= 1'b0;
   Inv_Cur_mode <= 1'b1;
   Voltage_mode <= 1'b0;
   Inv_Vol_mode <= 1'b1;
   Charge_mode <= 1'b1;
   Inv_Chg_mode <= 1'b0;
   end
endcase

   Cal_mode <= 1'b0;
   Inv_Cal_mode <= 1'b1;
end
else begin
   Current_mode <= 1'b0;
   Inv_Cur_mode <= 1'b1;
   Voltage_mode <= 1'b0;
   Inv_Vol_mode <= 1'b1;
   Charge_mode <= 1'b1;
   Inv_Chg_mode <= 1'b0;
   Cal_mode <= 1'b1;
   Inv_Cal_mode <= 1'b0;
end
end
else begin
   Channel_on <= 1'b0;
   Inv_Channel_on <= 1'b1;
   Current_mode <= 1'b0;
   Inv_Cur_mode <= 1'b1;
   Voltage_mode <= 1'b0;
   Inv_Vol_mode <= 1'b1;
   Charge_mode <= 1'b0;
   Inv_Chg_mode <= 1'b1;
   Cal_mode <= 1'b0;
   Inv_Cal_mode <= 1'b1;
end
end

always @(Charge Sel, Inv_Chg Sel, Current mode, Inv Cur mode,
Voltage_mode, Inv_Vol_mode, Charge_mode, Inv_Chg_mode, stim_mode,
calibration, threshold_ready) begin
  if (!calibration) begin
    if (stim_mode[1:0] != 2'b11 && stim_mode[1:0] != 2'b00) begin
      // voltage and current mode
      if (stim_mode[2]) begin
        // active recycling
        Current_Mux = (Current_mode & Inv_Chg_Sel & ~threshold_ready);
        Inv_Cur_Mux = ~((Current_mode & Inv_Chg_Sel & ~threshold_ready));
        Voltage_Mux = (Voltage_mode & Inv_Chg_Sel & ~threshold_ready);
        Inv_Vol_Mux = ~((Voltage_mode & Inv_Chg_Sel & ~threshold_ready));
        Charge_Mux = Charge_Sel | threshold_ready;
        Inv_Chg_Mux = Inv_Chg_Sel & ~threshold_ready;
      end
      else if (stim_mode[1] | stim_mode[0]) begin
        // passive recycling
        Current_Mux = Current_mode;
        Inv_Cur_Mux = Inv_Cur_mode;
        Voltage_Mux = Voltage_mode;
        Inv_Vol_Mux = Inv_Vol_mode;
        Charge_Mux = Charge_mode;
        Inv_Chg_Mux = Inv_Chg_mode;
      end
      else begin
        Current_Mux = 1'b0;
        Inv_Cur_Mux = 1'b1;
        Voltage_Mux = 1'b0;
        Inv_Vol_Mux = 1'b1;
        Charge_Mux = 1'b0;
        Inv_Chg_Mux = 1'b1;
      end
    end
    else if (stim_mode[1:0] == 2'b11) begin
      // charge mode
      Current_Mux = 1'b0;
      Inv_Cur_Mux = 1'b1;
      Voltage_Mux = 1'b0;
      Inv_Vol_Mux = 1'b1;
      Charge_Mux = 1'b1;
      Inv_Chg_Mux = 1'b0;
    end
    else begin
      Current_Mux = 1'b0;
      Inv_Cur_Mux = 1'b1;
      Voltage_Mux = 1'b0;
      Inv_Vol_Mux = 1'b1;
      Charge_Mux = 1'b0;
      Inv_Chg_Mux = 1'b1;
    end
  end
  else begin
    Current_Mux = 1'b0;
    Inv_Cur_Mux = 1'b1;
    Voltage_Mux = 1'b0;
    Inv_Vol_Mux = 1'b1;
    Charge_Mux = 1'b1;
    Inv_Chg_Mux = 1'b0;
  end
end
Listing A.4: Bidirectional RAM

```verilog
module bidirectional_ram (data_in, data_ready, data_check, memory_ergodic,
                       data_out, rst, addr, one_cycle_end);
  input [15:0] data_in;
  input data_ready, data_check;
  input [3:0] addr;
  output reg memory_ergodic, one_cycle_end;
  output reg [15:0] data_out;
  input rst;
  reg [15:0] memory [15:0];
  reg [3:0] index;
  always @(posedge data_ready or negedge rst) begin
    if (!rst) begin
      index <= 4'0000;
      memory_ergodic <= 1'b0;
      one_cycle_end <= 1'b0;
    end else begin
      if (!data_check) begin
        memory[index] <= data_in;
        index <= index + 4'0001;
        if (index == 4'b1110) begin
          memory_ergodic <= 1'b1;
        end else begin
          memory_ergodic <= 1'b0;
        end
      end
      if (memory[15][7:0] == 8'h00) begin
        one_cycle_end <= 1'b1;
      end else begin
        one_cycle_end <= 1'b0;
      end
    end
  end
  always @(addr, data_ready) begin
    if (!data_ready) begin
      data_out = memory[addr];
    end else begin
      data_out = 16'h0000;
    end
  end
endmodule
```

Listing A.5: Top level connection

```verilog
module top_fsm(clk, rst, data, errflag, p_chg_balance, n_chg_balance, Cmp_C1,
               Cmp_C2, neg_stim, neg_x1, neg_x2, pos_stim, pos_x1, pos_x2, inv_neg_stim,
               inv_pos_stim, inv_neg_x1, inv_neg_x2, inv_pos_x1, inv_pos_x2, C1_Charge,
               Inv_C1_Chg, C1_Stim,
               Inv_C1_Stim, C2_Charge, Inv_C2_Chg, C2_Stim,
               Inv_C2_Stim, Voltage_SEL, Inv_Vol_SEL, Charge_SEL, Inv_Chg_SEL,
               Pos_CSTIM, Neg_CSTIM, Short_SEL, Inv_Shrt_SEL, Sample_SEL, Inv_Sample_SEL,
               waveform, waveform_n, cal_data, stim_err, cal_err, addr_set, Current_mode,
               Inv_Cur_mode, Voltage_mode, Inv_Vol_mode, Charge_mode, Inv_Chg_mode,
               Cal_mode, Inv_Cal_mode, Channel_on, Inv_Channel_on, Current_MUX,
               Inv_Cur_MUX, Voltage_MUX, Inv_Vol_MUX, Charge_MUX, Inv_Chg_MUX);
```
input clk, rst;
input [20:0] data;
input [3:0] addr_set;
wire stim_finish;
wire [15:0] data_out;
wire data_check, data_ready, read_setup, set_charge;
output errflag;
wire rst_stim, stim_ready, write_enable;
wire [3:0] ram_address;
wire [2:0] stim_mode;
wire memory_ergodic, cal_done;
output Current_mode, Inv_Cur_mode, Voltage_mode, Inv_Vol_mode, Charge_mode,
Inv_Chg_mode, Cal_mode, Inv_Cal_mode, Channel_on, Inv_Channel_on,
Current_Mux, Inv_Cur_Mux, Voltage_Mux, Inv_Vol_Mux, Charge_Mux,
Inv_Chg_Mux;
wire calibration, lowz_state, set_cal;
channel_fsm U0 (
    .clk (clk),
    .rst (rst),
    .cdi (data[20]),
    .addr (data[19:16]),
    .addr_set (addr_set),
    .data_in (data[15:0]),
    .stim_finish (stim_finish),
    .memory_ergodic (memory_ergodic),
    .data_out (data_out),
    .data_check (data_check),
    .errflag (errflag),
    .data_ready (data_ready),
    .read_setup (read_setup),
    .set_charge (set_charge),
    .stim_mode (stim_mode),
    .rst_stim (rst_stim),
    .stim_ready (stim_ready),
    .calibration (calibration),
    .cal_done (cal_done),
    .lowz_state (lowz_state),
    .set_cal (set_cal)
);

// wire memory_empty, memory_full;
wire [15:0] waveform_data;
wire one_cycle_end;

bidirectionalram U1 (
    .data_in (data_out),
    .data_ready (data_ready),
    .data_check (data_check),
    .memory_ergodic (memory_ergodic),
    // .memory_full (memory_full),
    // .memory_empty (memory_empty),
    .data_out (waveform_data),
    .rst (rst),
    .addr (ram_address),
    .one_cycle_end (one_cycle_end)
);

input p_chg_balance, n_chg_balance;
input Cmp_C1, Cmp_C2;
output neg_stim, neg_x1, neg_x2, pos_stim, pos_x1, pos_x2, inv_neg_stim, inv_pos_stim, inv_neg_x1, inv_pos_x1, inv_neg_x2, inv_pos_x2;

output C1_Charge, C1_Stim, C1_Chg, C2_Charge, C2_Stim, Voltage_SEL, Inv_C1_Chg, Inv_C1_Stim, Inv_C2_Chg, Inv_C2_Stim, Pos_CSTIM, Neg_CSTIM, Short_SEL, Inv_Shrt_SEL, Sample_SEL, Inv_Sample_SEL, Inv_Cmp_C1, Inv_Cmp_C2;

output [4:0] waveform, waveform_n;

input [5:0] cal_data;
output stim_err;
output cal_err;

ivc_fsm U2 (stim_mode, read_setup, waveform_data, data_out, waveform, waveform_n, neg_stim, neg_x1, neg_x2, pos_stim, pos_x1, pos_x2, p_chg_balance, n_chg_balance, rst_stim, clk, stim_ready, set_charge, C1_Charge, C1_Stim, C1_Chg, C2_Charge, C2_Stim, C2_Chg, Voltage_SEL, Inv_Vol_SEL, Charge_SEL, Inv_Cmp_C1, Inv_Cmp_C2, ram_address, cal_data, cal_done, Pos_CSTIM, Neg_CSTIM, Short_SEL, Inv_Shrt_SEL, one_cycle_end, stim_err, cal_err, Sample_SEL, Inv_Sample_SEL, inv_neg_stim, inv_pos_stim, inv_neg_x1, inv_pos_x1, inv_neg_x2, inv_pos_x2,
.inv_neg_x2 (inv_neg_x2),
.inv_pos_x2 (inv_pos_x2),
.Current_mode (Current_mode),
.Inv_Cur_mode (Inv_Cur_mode),
.Voltage_mode (Voltage_mode),
.Inv_Vol_mode (Inv_Vol_mode),
.Charge_mode (Charge_mode),
.Inv_Chlg_mode (Inv_Chlg_mode),
.Channel_on (Channel_on),
.Inv_Channel_on (Inv_Channel_on),
.Cal_mode (Cal_mode),
.Inv_Cal_mode (Inv_Cal_mode),
.Current_Mux (Current_Mux),
.Inv_Cur_Mux (Inv_Cur_Mux),
.Voltage_Mux (Voltage_Mux),
.Inv_Vol_Mux (Inv_Vol_Mux),
.Charge_Mux (Charge_Mux),
.Inv_Chg_Mux (Inv_Chg_Mux),
.lowz_state (lowz_state),
.set_cal (set_cal)
);
endmodule
A.3. State Diagram for Multichannel Stimulator

Figure A.2: State diagram for individual channel control FSM
Figure A.3: State diagram for stimulation control FSM
A.4. Differential Nonlinearity of Current Mode Stimulation on Multichannel Stimulator System

Figure A.4. DNL of channel 1 to 4 of chip 4 to 7. Red circles represent sourcing current; Blue circles represent sinking current.
Figure A.5: DNL of channel 5 to 8 of chip 4 to 7. Red circles represent sourcing current; Blue circles represent sinking current.
Figure A.6: DNL of channel 1 to 4 of chip 8 to 11. Red circles represent sourcing current; Blue circles represent sinking current.
Figure A.7: DNL of channel 5 to 8 of chip 8 to 11. Red circles represent sourcing current; Blue circles represent sinking current.
A.5. Integral Nonlinearity of Current Mode Stimulation on Multichannel Stimulator System

Figure A.8: INL of channel 1 to 4 of chip 4 to 7. Red circles represent sourcing current; Blue circles represent sinking current.
Figure A.9: INL of channel 5 to 8 of chip 4 to 7. Red circles represent sourcing current; Blue circles represent sinking current.
Figure A.10: INL of channel 1 to 4 of chip 8 to 11. Red circles represent sourcing current; blue circles represent sinking current.
Figure A.11: INL of channel 5 to 8 of chip 8 to 11. Red circles represent sourcing current. Blue circles represent sinking current.
A.6. Differential Nonlinearity of Voltage Mode Stimulation on Multichannel Stimulator System during Negative Output Phase

Figure A.12: DNL of channel 1 to 4 of chip 1 to 2 and 4 to 6
Figure A.13: DNL of channel 5 to 8 of chip 1 to 2 and 4 to 6.
Figure A.14: DNL of channel 1 to 4 of chip 7 to 11
Figure A.15.: DNL of channel 5 to 8 of chip 7 to 11
A.7. Integral Nonlinearity of Voltage Mode Stimulation on Multichannel Stimulator System during Negative Output Phase

Figure A.16: INL of channel 1 to 4 of chip 1 to 2 and 4 to 6
Figure A.17: INL of channel 5 to 8 of chip 1 to 2 and 4 to 6
Figure A.18: INL of channel 1 to 4 of chip 7 to 11.
Figure A.19: INL of channel 5 to 8 of chip 7 to 11.
A.8. Publications


Other work (not related to topic of this thesis)
