Single-electron effects in side-gated point contacts fabricated in low-temperature deposited nanocrystalline silicon films

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Single-electron effects have been observed up to 60 K in a side-gated point contact device fabricated in nanocrystalline silicon films. The films were phosphorus-doped and deposited at 300 °C by plasma enhanced chemical vapor deposition. Using transmission electron microscopy and Raman spectroscopy, the grain size, crystalline volume fraction, and grain boundary thickness are determined. The single-electron effects are associated with islands formed by crystalline silicon grains ~4 nm in size, isolated by amorphous silicon regions ~0.5 nm in thickness. The structural characteristics of the nc-Si film are correlated to the electrical behavior. The electrical transport mechanism at high temperatures is attributed to percolation conduction across a distribution of tunnel barriers with a maximum height of 40 meV. © 2001 American Institute of Physics.

Nanocrystalline silicon (nc-Si) is a chemically-tailored material where crystalline silicon grains <10 nm in size are embedded in an oxide or amorphous silicon matrix. These nanoscale grains can form isolated charging islands which show single-electron effects, raising the possibility of room temperature single-electron devices fabricated in silicon. Several large-area nc-Si devices have been demonstrated, such as the nanodot memory structure of Tiwari and co-workers and the tunneling diode of He and co-workers. An atomic force microscope has been used to characterize individual nc-Si grains embedded in SiO2 by Fukuda and co-workers and Otobe and co-workers. Resonant tunneling and single-electron effects have been observed at room temperature in these systems.

Nc-Si can be prepared using a low-temperature plasma-enhanced chemical vapor deposition (PECVD) process. Typically, a plasma of SiH4 or SiF4 at temperatures ≈300 °C is used. The nc-Si can be deposited on glass or silicon-on-insulator substrates for faster device operation and better electrical isolation. The low process temperature reduces fabrication costs and makes large-area fabrication easier. This raises the possibility of device applications such as quantum devices fabricated on flexible plastic sheets.

In this letter, we report the observation of single-electron effects up to a temperature of 60 K in an in-plane, side-gated, point contact device fabricated in phosphorus-doped nc-Si. Our nc-Si film is deposited by PECVD at 300 °C. We structurally characterize the nc-Si film and correlate this to the electrical characteristics. We attribute electron transport in our device to a thermally-assisted single-electron tunneling process in the low-temperature range and percolation conduction through a distribution of barriers heights in the high-temperature range.

We prepared 30 nm thick nc-Si films using very high frequency (VHF) PECVD from a SiF4:H2:SiH4 gas mixture. The films were deposited on a 150 nm thick silicon oxide layer thermally grown on top of n-type crystalline silicon. The flow rates of the SiF4, H2, and SiH4 were 30, 40 and 0.25 sccm. The films were doped in situ with PH3 (1% diluted with H2) where the concentration of PH3 in SiH4 was 2%. The VHF frequency was 100 MHz, the VHF power was 40 W and the reactor pressure was 200 mTorr. The carrier concentration and electron mobility, measured at room temperature by Hall measurements, were 3×1020 cm−3 and 1.8 cm2/Vs, respectively.

Our silicon point contact structures were defined using electron-beam lithography in polymethyl methacrylate resist and reactive-ion etching in a mixture of SiCl4 and CF4 gases (20 sccm each) at 13.56 MHz, 300 W, and 20 mTorr. The point contact has a width of 20 nm. Ohmic contacts were formed to the structure by first wet etching the surface oxide on the nc-Si film in SILOX (Laporte proprietary chemical) and then depositing aluminum contact pads. Figure 1 shows

FIG. 1. Scanning electron micrograph of the side-gated point contact device. The inset shows an enlarged view of the source–drain point contact.
a scanning electron micrograph of the structure.

We have characterized the structure of the nc-Si films using transmission electron microscopy (TEM). We used a Philips CM 300 FEG with an accelerating voltage of 300 kV. Figure 2 shows a TEM image of uniformly distributed nc-Si grains embedded in an amorphous silicon matrix. The grain sizes range from 4–8 nm. The diffraction rings shown in the inset demonstrate that the film contains crystalline silicon and not entirely amorphous. Additional high-resolution TEM analysis using Fresnel contrast indicated that the grain boundaries were decorated with fine layers of amorphous silicon less than 1 nm thick.

We have also characterized the structure of the nc-Si films with Raman spectroscopy, using an argon–ion beam with an excitation wavelength of 514.5 nm. The film structure was analyzed by fitting the Raman spectra with a combination of the correlation length model for the crystalline silicon peak at ~521 cm⁻¹ and a Gaussian function for the amorphous silicon peak at ~480 cm⁻¹. The results demonstrated that the average grain size in the nc-Si film is 4 nm and the crystalline volume fraction is 70%. Assuming spherical nc-Si grains with a radius of 2 nm, uniformly encapsulated by an amorphous silicon layer of thickness D, we estimate D = 0.25 nm from the crystalline volume fraction of 70%. Therefore, the average thickness of the grain boundary region is d = 2D = 0.5 nm.

We have electrically characterized the point contact devices at temperatures ranging from 4.2 to 300 K. Figure 3(a) shows the drain–source current–voltage (I_d–V_d) characteristics of the device at 8 K as the gate voltage V_g is varied from −2 to 2 V in 50 mV steps. A Coulomb gap V_C, strongly modulated by V_g, is observed at low V_d. The maximum width of V_C is ~40 mV. Periodic peaks separated by ~20 mV are observed in the differential conductance characteristic (not shown). A nonlinearity in the I_d–V_d characteristics corresponding to the Coulomb gap is observed up to a temperature 70 K.

Figure 3(b) shows oscillations in I_d as V_g is swept from −1 to 1 V and V_g is varied from −44 to −4 mV and from 4 to 44 mV in 4 mV steps. A dominant oscillation with a period ΔV_g of 500 mV for the superimposed minor oscillations. This behavior can be attributed to single-electron conductance oscillations in a multiple tunnel junction (MTJ).

![FIG. 3. (a) I_d–V_d characteristics at 8 K. V_g is varied from −2 to 2 V in steps of 50 mV. Each I–V curve is displaced by 20 pA for clarity. (b) I_d–V_g characteristic at 4.2 K. V_d is varied from −44 to 44 mV in steps of 4 mV.](image-url)

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The variation in the amorphous silicon tunnel barrier height may be explained by considering the dopant distribution in the nc-Si film. A nc-Si grain of 4 nm diameter contains on average thirty phosphorous atoms while a 0.5 nm thick amorphous silicon grain boundary contains on average only six phosphorous atoms. This implies that the grain boundaries would be strongly influenced by any fluctuation in the doping concentration, leading to a variation in the energy difference between the conduction band edge and the Fermi level in the amorphous silicon, and a variation in the depletion width at the crystalline silicon/amorphous silicon interface. We note that if the tunnel barrier on average is 40 meV high and 0.5 nm wide, the tunnel resistance is \( \sim 10 \, \text{k}\Omega \), which is less than the quantum resistance \( R_0 = 25.8 \, \text{k}\Omega \) and Coulomb blockade effects are not possible.\(^{11}\) However, in our measurements there must be a wider than average grain boundary because of statistical fluctuations in the grain boundary width together with additional depletion regions on either side. This would create a wider tunnel barrier with a higher tunnel resistance, for example if the barrier is 40 meV high and 2 nm wide, the tunnel resistance is \( \sim 10R_0 \) and Coulomb blockade effects would occur.

We have also fabricated up to 60 nm wide devices which exhibit a maximum tunnel barrier height from 16–22 meV. In these devices a larger number of percolation paths may exist for electron transport and a lower tunnel barrier height is more likely observed. Even in the point contact device of Fig. 4, the maximum barrier height of 40 meV is relatively low for electronic confinement at higher temperatures closer to room temperature. At temperatures \( > T_1 \), single-electron effects disappear and there is a transition to percolation conduction.

In conclusion, we have observed single-electron effects in nc-Si point contacts up to a temperature of 60 K. We have shown that the charging islands are nc-Si grains as small as \( \sim 4 \) nm, isolated by amorphous silicon regions \( \sim 0.5 \) nm thick. Electron transport is attributed to a thermally assisted single-electron tunneling process at low temperature and percolation conduction at high temperature. Our work is funded by the Japan Science and Technology Agency CREST program.