Ultra-low power design strategy for two-stage amplifier topologies

L.B. Leene and T.G. Constantinou

A novel two-stage amplifier topology and ultra-low power design strategy for two-stage amplifiers that utilises pole zero cancellation to address the additional power requirements for stability are presented. For a 288 nA total bias, the presented amplifier achieves a 1.07 MHz unity gain frequency with a $\$560 \text{pF} \text{MHz}/\text{mA}$ figure of merit.

Introduction: Power-efficient amplifier topologies are fundamental for analogue processing both in the continuous and discrete time domains. The feasibility of a system is often established using a relevant figure of merit (FOM) that quantifies performance. The prevalence of limited power budgets in medical sensors indicates that advances in low-power analogue amplifiers are critical for the future of implantable biomedical systems that are constrained through battery life and wireless telemetry [1, 2]. An ultra-low-power analogue design is best motivated through aggressively maximising a FOM that indicates how effectively power is used to achieve a desired performance characteristic such as noise, speed or linearity in order to reveal the underlying limitation.

Take the differential pair in Fig. 1, for example, to illustrate the driving motivation behind sub-threshold operation. The FOM with all input transistor pairs and evaluated as

\[
\text{FOM}_{\text{fi}} = \frac{10^3}{4\pi \cdot \eta U_T}
\]

where \(\eta\) and \(U_T\) being the sub-threshold slope factor and thermal voltage, respectively. With \(V_{\text{cm}}\) usually being 200 mV, operation in weak inversion can be reduced to a single operational parameter:

\[
\text{FOM}_{\text{fi}} = \frac{10^3}{2\pi U_{\text{ov}}}
\]

where \(U_{\text{GF}}, C_{\text{i}}, L_{\text{cm}}\) and \(V_{\text{cm}}\) are the unity gain frequency, load capacitance, total bias current and overdrive voltage of the input transistors, respectively. With the input transistors biased in weak inversion, however, the FOM is derived as

\[
\text{FOM}_{\text{ab}} = \frac{10^3}{2\pi U_{\text{ov}}}
\]

with \(\eta\) and \(U_T\) being the sub-threshold slope factor and thermal voltage, respectively. With \(V_{\text{cm}}\) usually being 200 mV, operation in weak inversion can directly improve the FOM by six times. In addition to sub-threshold biasing, a number of current recycling techniques can be applied to further gain in FOM [3]. By coupling the input signal to biasing transistors \(M_{\text{fi}}\) for instance, a larger transconductance can be achieved with the same bias current. This allows a simple reduction in power by a factor of two for single-stage systems, but a second stage is often required in switched capacitor (SC) applications for high gain and wide output swing. The constraint of the second stage lies with the non-dominant pole at the output that needs to lie beyond the UGF. The output load capacitance dictates the minimum transconductance of the second stage and will often result in the second stage dissipating significantly more power than the first stage. In this Letter, we propose zero cancellation of this non-dominant pole in order to minimise power dissipation in the second stage. Secondly, we identify appropriate scaling factors for the FOM such as to make this applicable to two-stage amplifiers.

**Proposed amplifier:** The circuit configuration is shown in Fig. 2. This differential topology extends the complementary input stage with a current conveyor (CC) structure to achieve high gain and wide output swing. The high open-loop gain is provided by the cross-coupled PMOS devices \(M_{1,14}\) in addition to the traditional gain stage \(M_{19,22}\) that also allows for a rail-to-rail output swing. The circuit is configured to drain the same amount of current in the output branch as in the input transistor pair such that the transistors \(M_{1,6}\) and \(M_{19,22}\) have a transconductance \(g_{m1}\). The cross-coupled PMOS branch drains a fraction \((1/M = 0.25)\) of this same current such that the total current dissipated by the amplifier is \(2I_{\text{ab}}(2 + 1/M)\). The NMOS current mirror \(M_{15,18}\) implements a wideband positive feedback loop with a ratio of \(1/N = 1\), where \(N = 1.5\) to boost the bandwidth of the structure. Note that transistors \(M_{23,24}\) bias the input stage through common mode feedback and transistors \(M_{19,18}\) bias the output stage. The input transistors \(M_{1,6}\) are biased with a drain current \(I_{\text{in}}\) of 50 nA with a 1.2 V supply. This biasing current in addition to the ratio \(M\) determines the observed single-ended slew rate (SR) at the output as it is limited by the low-gain path in the NMOS current mirror. In the step response scenario, the current drained by \(M_{23}\) sources entirely into \(M_{15}\) \((M_{18})\) which is multiplied to \(M_{8,9}\) \((M_{50})\) by a factor \(M\), that is

\[
\text{SR} = M \cdot 2I_{\text{in}} / C_L
\]

For preliminary design considerations, it is useful to assess the dependence of different component parameters through the open-loop gain, UGF, pole and zero locations with simple approximations. First, it should be noted that the bandwidth product is twice as large as a conventional amplifier although current recycling in the complementary input transistor pairs and evaluated as

\[
\text{UGF} = \frac{g_{m1}}{\pi C_F}
\]

where \(C_F\) is a 500 fF compensation capacitor that couples the output to the input stage via a low impedance node in the NMOS differential pair utilising split length indirect compensation, thus avoiding the right-hand plane pole [4]. With \(\lambda\) as the channel length modulation parameter, the open-loop DC gain is evaluated as

\[
A_{\text{dc}} \approx N M \left( \frac{1}{\eta U_{TA}} \right)^2
\]

Furthermore, in the mid-band frequencies, the Miller capacitor \(C_T\) performs pole splitting both poles in the CC stage through the feedback loop. This will move the pole at the cross-coupled PMOS outside the UGF, more specifically \(a_{\text{p2}}\), and move the pole due to \(C_T\) towards

\[
a_{\text{p1}} \approx \frac{2M \cdot g_{m1}}{C_L + C_T}
\]

If \(g_{m1}\) is kept small this pole will remain inband of the amplifier. For an adequate phase margin that is larger than 65°, to prevent excess ringing at the output, we use pole zero cancellation. With \(a_{\text{p1}} = a_{\text{p2}}, C_i\) is determined according to

\[
a_{\text{p1}} \approx \frac{g_{m1}M \cdot (2 - N)}{C_i}
\]

Past the zero location, the signal path loads into the diode-connected
NMOS $M_{4}$ that now drives both $M_{23}$ and $M_{19}$ pushing out the UGF. With $C_{m}$ as the total gate capacitance from both NMOS and PMOS current mirrors and taking $C_{z}$ as a short circuit, the pole location $\omega_{12}$ can be confirmed to lie outside the UGF

\[
\omega_{12} = \frac{2g_{m2}}{C_{m}}
\]

\[
FOM = \frac{10^{6} \frac{C_{2}}{4\pi \eta U/2} + 1/M} = 3.56 \times FOM_{m1}
\]

As a result, when the FOM is reformulated (see above) for this particular configuration, it can be observed that this is increased, compared with the conventional single-stage topology. A significant contribution of this improvement in FOM naturally comes from the factor $C_{2}/C_{m}$, as a reduction in the dominant capacitive load allows an overall reduction in bias current to achieve a given bandwidth. This also illustrates that relative to a single stage, a two-stage configuration may trade off noise for a better FOM by adjusting the $C_{2}/C_{m}$ ratio. As the total input-referred integrated thermal noise ($\epsilon_{in}$) for a single pole system is related to the capacitor $(C)$ that introduces the dominant pole of the system through

\[
\epsilon_{in}^{2} = \frac{KT \text{NEF} I_{\text{input}}}{C} \frac{\eta \Delta C_{\text{total}}}{C}
\]

which is directly derived from the definition of the noise efficiency factor (NEF) [5] by substituting the expression for bandwidth as the closed-loop gain ($A_{cl}$) multiplied by UGF.

**Fig. 3** Simulation results

<table>
<thead>
<tr>
<th>Fig. 3 Simulation results</th>
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<tbody>
<tr>
<td>a</td>
</tr>
<tr>
<td>b</td>
</tr>
<tr>
<td>c</td>
</tr>
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**Simulation results:** Preliminary validation of the proposed implementation has been achieved using schematic level simulations in the Cadence IC 6.1.5 Design Environment using industry provided transistor models for the commercially available 6 Metal 0.18 μm CMOS technology (AMS/IBM C18A6/7SF). Fig. 3 shows the key simulation results, including small signal, transient and noise characteristics. The common mode feedback configuration used in these simulations is a conventional differential difference amplifier with a current mirror to drive both $M_{23}$ and $M_{24}$ transistors biasing the input stage simultaneously. To normalise performance with respect to requirements on the common mode feedback circuit, its 45 nW power contribution is excluded in FOM calculations. The simulated frequency characteristics were close to the analytical expectation achieving a 1.07 MHz UGF and a phase margin of 64°. The step response indicates settling of the output to <0.1% within 10 μs with the feedback configuration illustrated in Fig. 1. The configuration also demonstrates good noise performance as the input transistors have a larger transconductance than the first active load by a factor of $M$ for a smaller input referred noise figure. The 60 nV/√Hz input-referred thermal noise floor from 100 kHz to 1 MHz is good for auto-zeroing SC topologies that reject the flicker noise and low-frequency aggressors.

**Table 1: Performance summary**

<table>
<thead>
<tr>
<th>References</th>
<th>[6]</th>
<th>[7]</th>
<th>[8]</th>
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<tr>
<td>Year</td>
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<td>2010</td>
<td>2010</td>
<td>2013</td>
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<td>Tech. (nm)</td>
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<td>180</td>
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<td>Power (W)</td>
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<td>345 n</td>
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<td>Supply voltage(V)</td>
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<td>1.5</td>
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<td>1.2</td>
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<tr>
<td>DC gain (dB)</td>
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<td>59</td>
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<td>UGF (MHz)</td>
<td>450</td>
<td>111</td>
<td>20</td>
<td>1.07</td>
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<tr>
<td>SR (V/μs)</td>
<td>–</td>
<td>233</td>
<td>8</td>
<td>0.12</td>
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<td>Load/Miller (pF)</td>
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<td>5, 0/2/500</td>
<td>2/0.5</td>
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<td>Phase margin</td>
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<td>80°</td>
<td>72°</td>
<td>64°</td>
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<td>Noise floor (V/√Hz)</td>
<td>–</td>
<td>125 n</td>
<td>–</td>
<td>60 n</td>
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<tr>
<td>FOM (MHz pF/mA)</td>
<td>295</td>
<td>1267</td>
<td>8333</td>
<td>8560</td>
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</table>

**Conclusion:** The application of pole zero cancellation for achieving ultra-low power in a two-stage amplifier has been demonstrated. In addition, the Miller to load capacitor ratio and current recycling have been discussed as techniques to improve the FOM with the respective trade-off. The overall performance characteristics are summarised in Table 1. This demonstrates comparable performance to state-of-the-art three-stage nested Miller systems in terms of FOM in addition to a 345 nW power budget that is well within the power constraints of many biomedical analogue processing applications. The proposed topology achieves a 3.56 times improvement in FOM over conventional single-stage structures.

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One or more of the Figures in this Letter are available in colour online.

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**References**


