Coherent states in a coupled quantum dot nanocrystalline silicon transistor

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We investigate the coherent coupling of electronic states in a nanocrystalline silicon quantum dot transistor. The device consists of a nanometer-scale point-contact containing only a few silicon grains. The grains form quantum dots, tunnel-coupled across thin silicon sub-oxide grain boundaries. At 4.2 K, we observe a pattern of single-electron conductance peaks versus two gate voltages, caused by electrostatic coupling between the quantum dots. Additional peaks are observed when the energy levels from two adjacent quantum dots are resonant, which may be associated with "quasi-molecular" states formed by coherent coupling of the levels. The tunnel splitting obtained from the peak separation is ~ 0.4 meV, which is from a few times to an order-of-magnitude larger than reported previously in GaAs/AlGaAs quantum dots. © *2004 American Institute of Physics*. [DOI: 10.1063/1.1795974]

Nanocrystalline silicon (nc-Si) devices are promising candidates for the development of quantum-dot (QD) and single-electron transistors (SETs) compatible with large-scale integration processes.[1–3] These devices use nanocrystalline silicon materials where nanometer-scale crystalline silicon grains "naturally" form large numbers of silicon QDs, isolated by tunnel barriers formed at thin amorphous silicon or silicon oxide grain boundaries (GBs). The small grain size leads to large electron-confinement and single-electron charging energies,[4] raising the possibility of room-temperature operation of QDs and SETs.[2,5] The densely packed nature of the QDs is also of interest for quantum information processing in silicon.[6]

The close proximity of the nc-Si QDs suggests that strong electrostatic "Coulomb" interactions, and electron wave function interactions, may occur between multiple grains. Electrostatic interactions have been investigated in great detail at milli-Kelvin temperatures in tunnel-coupled double QDs defined in GaAs/AlGaAs two-dimensional electron gas materials.[7–9] There are comparatively few investigations of these effects in silicon.[6,10,11] These various experiments use two or more gates to change the QD potentials and a plot of the conductance versus the two gate voltages traces out hexagonal regions of constant electron number on the QDs, associated with single-electron interactions between the QDs. This forms a "charge stability" diagram where the electron number changes by one between neighboring hexagons.[7] Electron wave function interactions can also occur, forming coherent "quasi-molecular" states. These states have been observed below 50 mK in conductance measurements on GaAs/AlGaAs double QDs.[12] At the "triple-points" where three charge stable regions meet on the double QDs charge stability diagram, two discrete states (one from each QD) are resonant in energy, and the interdot tunnel coupling forms two "valance" states consisting of bonding-

like and antibonding-like levels. Resonant tunneling through these states leads to additional peaks in the device conductance.

In this letter, we investigate the formation of coherent states in strongly coupled nc-Si QDs embedded within point-contact transistors (Fig. 1). The point-contact is 30 nm $\times$ 30 nm $\times$ 40 nm in size, with two gates ~ 200 nm away on either side. The nc-Si grains are ~ 5 to ~ 25 nm in size, creating QDs far smaller than those in GaAs/AlGaAs systems. The grains are separated by ~ 1-nm-thick SiO_x GBs, and only a few grains exist within the point-contact [Fig. 1(b)]. The electrostatic potential of these grains can be controlled by the gate voltages. A plot of the device conductance at 4.2 K versus both the gate voltages shows single-electron conductance peaks arranged in lines, partially tracing out the charge stability diagram for two electrostatically coupled QDs. Additional conductance peaks are observed when the energy levels in two QDs are in resonance, which may be associated with the formation of coherent quasi-molecular states, due to the strong tunnel coupling between the QDs. The tunnel splitting between these states is ~ 0.4 meV,
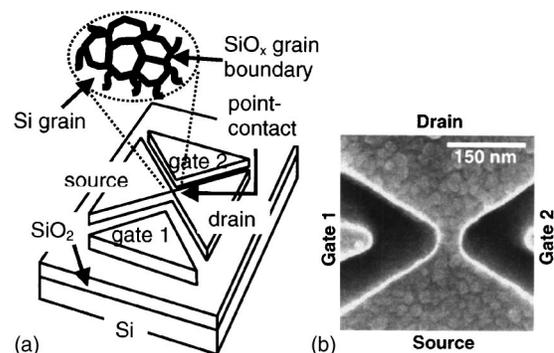

FIG. 1. (a) Schematic diagram of a nanocrystalline silicon point-contact transistor with two side gates. (b) Scanning electron micrograph of a nanocrystalline silicon point-contact transistor.

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which is from a few times to an order-of-magnitude greater than the splitting observed in previous work in GaAs/AlGaAs double QDs.[12] Our large tunnel splitting leads to the observation of quasi-molecular states even at 4.2 K, and is a consequence of tunnel coupling across GB barriers only ~1 nm thick, two orders-of-magnitude narrower than those in GaAs/AlGaAs double QDs. In addition, our "naturally" formed nc-Si QDs and tunnel barriers inherently cover large chip areas, and have the potential to be used for a quantum information processing system in silicon.

We fabricated our point-contact transistors in a ~40-nm-thick, heavily doped (n-type, phosphorous, doping concentration ~1×10^{19} cm^{-3}) nc-Si film, deposited by low-pressure plasma-enhanced chemical vapor deposition on a 100-nm-thick SiO$_2$ layer grown thermally on a Si substrate. The room temperature resistivity of the film was 0.1 Ω cm. The point-contact transistor was defined using high-resolution electron-beam lithograph in polymethyl methacrylate resist, followed by reactive-ion etching of the nc-Si film in 1:1 SiCl$_4$/CF$_4$ plasma to trench-isolate the point-contact and the gates (Fig. 1). The device was oxidised in dry O$_2$ at 750 °C for 30 min. This oxidizes the GBs (originally amorphous silicon) into SiO$_x$ and passivates the surface and GB defect states. In our previous work on room temperature nc-Si SETs,[2] we used Ar annealing to obtain GB SiO$_x$ tunnel barriers ~170 meV high. Our present devices are not annealed and the tunnel barriers remain narrow and low (~tens of meV), leading to strong tunnel coupling between the QDs.

Figure 2 shows the source-drain conductance (dI_{ds}/dV_{ds}) in a point-contact transistor at 4.2 K, as a function of the voltage on gate 1(V_{g1}) and gate 2(V_{g2}) and at source-drain voltage $V_{ds} = -2$ mV. The conductance is plotted in grey scale [Fig. 2(a)] and as a three-dimensional graph [Fig. 2(b)]. The measurement uses a preamplifier and an ac lock-in amplifier, at an excitation frequency and voltage of 30 Hz and 820 μV, respectively. The Coulomb gap voltage, measured from the I_{ds}-V_{ds} characteristic, was $V_{gap} = 7.5$ mV. This corresponds to a total QD capacitance $C_t = 2e/V_{gap} \approx 40$ aF. In Fig. 2, the maximum conductance is only 3×10^{-10} S, due to the small value of $V_{ds} < V_{gap}$ and due to high resistance nc-Si source/drain lead regions associated with a reduced carrier concentration at 4.2 K. The capacitance between either gate and the various grains in the point-contact is different due to the different location of each grain [Fig. 1(b)]. Therefore, V_{g1} and V_{g2} can shift the energy levels in different QDs past the source/drain Fermi level and past each other, resulting in the observation of single-electron conductance peaks. These peaks form a complex arrangement of lines with two main slopes which can split near the intersection points to define partially the boundaries of electron stability regions associated with two electrostatically coupled QDs. The stability region shapes are irregular and vary from the ideal hexagonal shapes. This may be caused by a complicated QD-gate capacitance network, or a change in the coupling between the grains at different gate voltages.[10,11]

In region "I" (dashed circle), two peak lines ["a" and "b", shown schematically in Fig. 2(c)] intersect. The lines tend to split due to electrostatic coupling between two QDs, and form a set of two triple points [points "1" and "2", Fig. 2(c)] where the energy levels are resonant. From the stability region widths along $V_{g1}(\Delta V_{g1} \sim 3$ V) and $V_{g2}(\Delta V_{g2} \sim 1.5$ V) axis, we can estimate the gate capacitances $C_{g1} \sim 0.05$ aF and $C_{g2} \sim 0.1$ aF. Therefore, the energy level
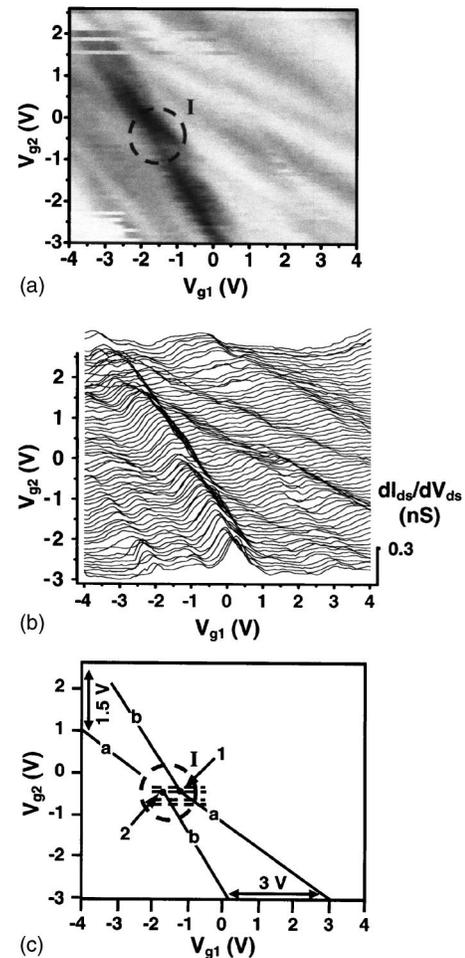

FIG. 2. (a) Grey-scale image of the source-drain conductance dI_{ds}/dV_{ds} in a point-contact transistor at 4.2 K, as a function of the voltage on gate 1(V_{g1}) and gate 2(V_{g2}). The source-drain voltage $V_{ds} = -2$ mV. (b) Three-dimensional graph of the same data. (c) Schematic showing two of the lines formed by the conductance peaks, which intersect and split in region "I."

separation corresponding to the peak lines is ~$eC_{g1}\Delta V_{g1}/C_t \sim 4$ meV, which compares well to the single-electron level separation. We also observe a finite conductance along the stability region boundaries, either suggesting two parallel QDs,[11] or series QDs with an off-resonance current due to strong coupling between the QDs, and to the source and drain.[12] In both cases, at the triple points the QD energy levels are resonant.

We observe an additional conductance peak in region "I," between the two triple points. This is investigated by sweeping V_{g1} for fixed values of V_{g2} [dashed lines, Fig. 2(c)], and is seen to consist of four subpeaks (Fig. 3). Our data (300 points) can be fitted using a sum of four Lorentzian peaks, implying that the subpeaks may correspond to resonant tunneling through strongly coupled energy levels.[13] The two outer subpeaks are higher than the two intermediate subpeaks. The height of the various peaks varies with V_{g2} in a complex manner, which may be associated with changes in the tunnel coupling of the energy levels to the source and drain region. The subpeaks disappear away from region "I," and further along lines "a" and "b" only a single Lorentzian peak is seen.

Coherent coupling of the wave functions of the resonant states near the two triple points can form "valance" states at different energies. In the vicinity of these triple points, the
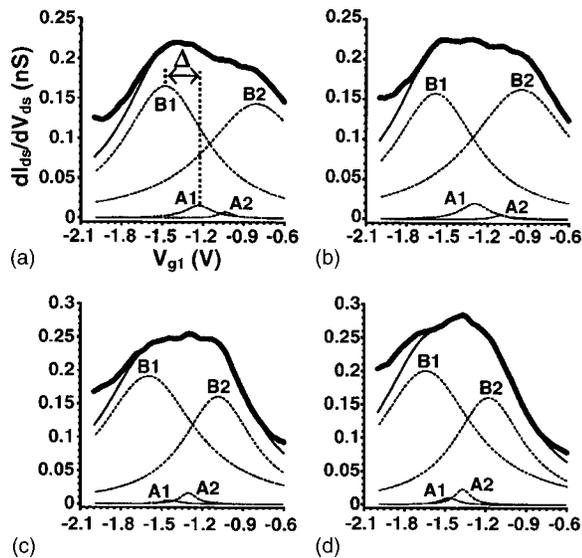
FIG. 3. Drain-source conductance (circles) at 4.2 K, in the point-contact transistor as a function of V_{g1} and $V_{ds} = -2$ mV, for V_{g2} equal to (a) −0.75 V, (b) −0.65 V, (c) −0.45 V, and (d) −0.35 V. The traces are measured along the dashed lines in Fig. 2(c). The data (300 points) can be fitted (solid line) using the sum of four Lorentzian peaks, A1, A2, B1, and B2 (dashed lines).

discrete charge states in adjacent dots split into bonding and antibonding states. Resonant tunneling through these levels may explain the peak structure in Fig. 3. The two additional antibonding states lead to two small current peaks along the shoulder of the main current peaks.[12] The four Lorentzian peaks can then be associated with bonding (outer peaks B1 and B2) and antibonding (intermediate peaks A1 and A2) levels. The energy separation between the states "A1" and "B1" in Fig. 3(a) can be estimated as $\Delta = e C_{g1} V_s / C_t$ ~0.4 meV, where V_s ~0.3 V is the horizontal separation, C_t ~40 aF and C_{gl} ~0.05 aF. By contrast, the level separation in a 10 nm QD with parabolic potential bafflers is ~10 meV. Our results may be compared with coherent states observed at milli-Kelvin temperatures in GaAs/AlGaAs double QDs, which have large QD and tunnel baffler dimensions ~100 nm, and long wave function coherence lengths

~1 μm. The coherence length in silicon is much shorter, e.g., the inelastic scattering mean free path in bulk Si at 300 K is ~10 nm,[14] although this may be longer locally and at low temperature. In nc-Si with ~10 nm grain size, the macroscopic mean free path is likely to be determined by GB scattering, i.e., by the grain size. However, our QDs are only ~10 nm in size and are separated by very narrow GBs only ~1 nm in width. Wave function coupling of the states in adjacent QDs can then occur locally across the intermediate GB tunnel barrier, leading to the formation of coherent quasi-molecular states even in silicon.

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