A Partial-Current-Steering Biphasic Stimulation Driver for Neural Prostheses

Timothy G. Constandinou*,†, Julius Georgiou*, and Chris Toumazou†

*Holistic Electronics Research Lab, ECE Department, University of Cyprus, Nicosia 1678, Cyprus
†Institute of Biomedical Engineering, Imperial College of Science, Tech. & Medicine, London SW7 2AZ, UK

Email: t.constandinou@ucy.ac.cy, julio@ucy.ac.cy, c.toumazou@imperial.ac.uk

Abstract—This paper describes a novel partial-current-steering stimulation drive for implantable neural prosthetics. The drive hardware momentarily delivers a charge-balanced asymmetric stimulus to a dummy load before steering towards the stimulation electrodes. In this fashion, power is conserved whilst still gaining from the benefits of current steering. The circuit has been designed to be digitally programmable as part of an implantable vestibular prosthesis. The hardware has been implemented in AMS 0.35μm 2P4M CMOS technology.

Index Terms—electrical stimulation, prosthesis, biphasic pulse, continuous interleave sampling, current steering

I. INTRODUCTION

Artificial electrical stimulation, a methodology becoming increasingly accepted in the medical community is providing engineers and medical professionals a reliable method to interface to neural tissue. Neural prostheses are already benefitting those with profound hearing loss, cardiac arrhythmia’s, loss of muscular function, hand grasp, foot drop, in bladder control and soon those with loss of vision. A key component in such systems is the neural interface and stimulation drive hardware. Reliability and robustness are paramount, and ensuring good efficiency and minimising neural fatigue ensure long-lasting rehabilitation.

Typically, in electrical neural stimulation, a minimum of two electrodes are used to produce a nerve activation current. The pair can be used in a monopolar or a bipolar configuration. The bipolar scheme (active and reference electrode are placed close to the nerve) is preferred as it allows greater activation selectivity because each pair generates a more localised field (compared to monopolar) [1].

Stimulus pulse parameters include frequency, amplitude and duration. The former affects the smoothness of perceived sensation and needs to be adjusted to prevent neural fatigue. The latter two parameters affect the strength of the neural response and alter the charge injected. As established by [2], in order to avoid harmful electrochemical processes, the stimulus waveform has to be biphasic. In such a waveform the first pulse causes activation, followed by a second one with opposite polarity to balance the charge delivered by the first [3]. However, it has been reported [4] that two opposite pulses back to back could act to prevent the generation of an action potential, or could require more energy to produce an action potential. To overcome this, a short time delay needs to be introduced between the pulses. Additionally, using an extended anodic pulse with reduced amplitude can compensate for charge distribution and thus reduce fatigue.

This paper presents a novel CMOS-based integrated circuit for artificial neural stimulation as part of an implantable vestibular prosthesis. Section II outlines the system architecture, section III describes the implementation at circuit level and section IV presents simulated results. Finally, section V summarises and discusses the various features of the presented work.

II. SYSTEM OVERVIEW

This system implements a complete, 3-channel biphasic stimulation drive with digitally programmable signal conditioning for a fully-implantable vestibular prosthesis [5] using a bipolar electrode configuration. Due to the close proximity between adjacent stimulation sites, the system incorporates a continuous interleave sampling (CIS) strategy to minimise crosstalk. Furthermore, we have chosen to implement an asymmetric (but charge-balanced biphasic) waveform profile, to match natural neurophysiological response, thus reducing fatigue of neural tissue. Additionally, the system includes a short-duration current steering phase, to avoid charge-buildup, and therefore glitching at turn-on and turn-off, whilst reducing...
power consumption compared to traditional current-steering systems. As an added precaution, once each CIS cycle, all the stimulation electrodes are grounded, such that any residual charge that may have accumulated is removed.

The target stimulation profile and current-steering methodology used is illustrated in Fig. 1. For one clock cycle before and after each stimulation phase, the current is steered towards a dummy load, such to achieve a smooth transition, thus minimising charge buildup and spiking. Additionally, the current magnitude is scaled with ratio 4:1 between cathodic and anodic pulses. Conversely, the pulse lengths are scaled 1:4 respectively, to maintain charge balance. The corresponding current paths flowing through the drive switches are also shown (circuit details given later). Another feature is that there exists a short pause between cathodic and anodic pulses.

### III. CIRCUIT IMPLEMENTATION

The top-level system schematic is shown in Fig. 2. This shows the 3-channel stimulation drive incorporating a continuous-interleave-sampling (CIS) strategy [6] based on a modular design architecture, similarly to [7]. The implementation and purpose of the various sub-blocks will be discussed in the following sub-sections.

#### A. Stimulus Conditioning

For each stimulation channel, this includes digital settings for: (i) offset, (ii) gain, and (iii) threshold. These are intended to (i) remove any static (operating point) offset caused by process variation and/or device mismatch in preceding hardware, (ii) amplify the input stimulus such that the dynamic range is maximised for a particular channel/patient, and (iii) provide a baseline stimulation to match the onset of sensation of the patient, such that any additional increment in stimulus will perceive a sensation. Collectively, these settings ensure the full content of the signal is most efficiently mapped onto the available dynamic range of the artificially-evoked neural response (including the entire stimulation chain). The circuit implementation for the current-mode signal conditioning is shown in Fig. 3.

#### B. Patient Tuning/Programmability

In order to implement a feasible totally-implantable prosthesis, the requirement for digitally programmability is paramount. One challenge in achieving such functionality is the scheme used for data transmission and recovery. Typically, medical implants use inductive schemes whereby patient settings data is encoded onto a carrier signal that is inductively coupled through the skin, to the subcutaneously implanted device where the data can be recovered [8]. Implementing robust
hardware to extract patient settings data from a continuous bitstream requires: (i) a temporary settings (shift) register and method to precisely align the incoming bitstream to patient settings register, (ii) a method to reliably initiate a parallel load from serial input to patient settings register, and (iii) data redundancy and error correction. The design implemented in this system is shown in Fig. 4. This work however, does not include hardware for data redundancy and error correction. It is envisaged that this can be implemented using standard coding techniques, eg. hamming coding, parity check-bits, etc.

The hardware for loading the patient tuning data is split into two sections; the registers that are specific to each channel, and the state machine for determining when a parallel-register-load occurs. In Fig. 4, the first portion is illustrated in subfigures (a) and (b). These registers are repeated (and cascaded) for each channel, for example- within a 3-channel system, each register would be of \( 3 \times (3+6+3)=24 \)-bit length. The state machine, appended to the end of the combined shift-register is shown in Fig. 4 (c) and (d). In (c), the incoming bitstream is interrogated to match a multi-bit START-SEQUENCE chosen to be: 111010101011. Finally, in (d), a ripple counter increments for every “0” received, and reset whenever a “1” is received, thus checking for the occurrence of 64 successive 0’s. This effectively flushes (initialises) the shift register each time patient settings are streamed in. The LOAD-DATA signal is therefore asserted when both these conditions are met, i.e. the patient settings bitstream starts with 64 0’s followed by the START-SEQUENCE.

C. Biphasic Waveform Generation

The waveform shown previously in Fig. 1 is generated using a state machine; requiring a clock \( 32 \times \mu \) higher than the CIS clock. The state machine is based on a 32-bit serial shift register, with RS-latches arranged to capture the individual phases. This is shown in Fig. 5. For example, the anodic phase has been predefined to start on clock cycle 12 and end after clock cycle 31.

These digital control signals, (after being level-shifted/buffered to stimulation supply voltage- see Fig. 7), feed the current control switches to form the H-bridge, shown in Fig. 6, the functioning of which has been previously illustrated in Fig. 1. In this, Q1 and Q7 drive the cathodic pulse, devices Q3 and Q5 drive the anodic pulse, devices Q2 and Q6 drive the dummy load (steering), and devices Q4 and Q8 are used to ground the stimulation electrodes, during the short/reset phase.

D. Integrated Circuit

The circuit has been designed and fabricated in AMS 0.35\( \mu \)m 2P4M CMOS technology. The chip microphotograph is shown in Fig. 8.

IV. SIMULATION RESULTS

The circuit was simulated using the Cadence Spectre (5.1.41isr1) simulator with foundry supplied BSIM3v3 models.

Transient simulations taking static (stimulation) input currents \( (I_{IN1}=5\mu A, I_{IN2}=10\mu A, \text{ and } I_{IN3}=15\mu A- \text{ before gain}) \), and loading (maximum) patient settings registers have been performed (with \( I_{LSB-THRESHOLD}=15\mu A \text{ and } I_{LSB-OFFSET}=0 \)). The results show the bipolar waveform being correctly generated, are presented in Fig. 9. The effect of the current steering can be clearly seen to minimise...
the turn-on and turn-off glitches. Also, the SHORT phase (Fig. 9(c)) can be seen to remove any residual charge. As expected, the power consumption is mostly dominated by the stimulation supply (largely depending on patient settings). The static current consumption is on average 20 μA.

V. CONCLUSION

In this paper we have presented an integrated circuit for use in artificial electrical stimulation of neural tissue within the peripheral nervous system. The system designed provides three stimulation channels, each with full digital programmability, sequenced using the CIS stimulation strategy. We have focused on achieving good reliability and robustness, specifically to ensure long-term stability, be minimally invasive and guaranteeing that patient calibration settings are uploaded in a safe manner. To this goal, we have implemented a novel current-steering scheme to avoid charge-buildup-related stimulation artifacts. This has designed to ensure all stimulation transitions are smooth but sharp whilst maintaining good power efficiency, compared to traditional current-steer systems. Moreover, the system has been designed to generate an asymmetric, charge-balanced waveform to maximise neural response to electrical stimulus whilst minimising fatigue of neural tissue.

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