Fault Models of Inverter-Interfaced Distributed Generators: Experimental Verification and Application to Fault Analysis

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Abstract—This paper investigates the fault behaviour of inverter-interfaced distributed generators in stand-alone networks. It is shown that the rapid transient response of the inverter control system allows its fault behaviour to be characterised by quasi steady-state equivalent fault models. The choice of inverter control strategy, control reference frame and the method of active current limiting dominate the fault response, especially in case of unbalanced faults. The proposed fault models can be directly incorporated in conventional fault analysis methods of which an example is given for a faulty islanded microgrid. Model validation is carried out by comparing experimental measurements with results of analytical fault analysis using the developed fault models and PSCAD time domain simulations.

Index Terms—inverter, fault response, island, fault model, distributed generation

I. Introduction

The integration of DG into the utility grid faces a number of technical issues such as their impact on feeder voltage profiles and the distribution network existing protection system. In contrast to conventional generators, no tried-and-tested analytical fault models exist for inverters, forcing protection engineers to employ complex and time consuming full time domain models of the inverter and its control systems [3], [4]. The fault response of an inverter is dominated by its control system which actively limits the available fault current to safeguard the semiconductor switches [5], [6]. This limit can be increased by over-engineering the inverter hardware and is typically set at twice the nominal current rating [5]. If a substantial amount of conventional generation is replaced by IIDG, or indeed if the IIDG is the only power source as in the case of an islanded network, the resulting low fault level can interfere with the proper operation of the incumbent over-current based protection system [7], [8], [9].

To facilitate the anticipated rise in DG connections, it is imperative to develop and test inverter fault models that can be used in conventional fault analysis techniques yet reflect the inverter's control strategy and current limiting method. In [4] an attempt is made by considering a grid-connected IIDG. An approximated model based on observation of the

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inverter's response during simulations in EMTP is developed for use in loadflow based methods. This approach is not analytically rigorous and ignores the effect of the control system. The analysis presented in [10] does not provide an efficient method or insight into inverter fault response as it relies on the numerical solution of a state-space representation of the complete system including inverters. In [11] the test results of subjecting commercially available inverters to faults are presented, without providing details on the inverter control system. Analytical fault models based on a popular grid-connected inverter control strategy are presented in [19] together with their application in loadflow based fault studies including an experimental validation. The presented models do, however, not apply to islanded or stand-alone operation.

To date, there are no reported studies on the fault behaviour of islanded IIDG sources. This paper aims to develop analytical models that characterise islanded IIDG sources under fault conditions. The paper is organized as follows. In Section 2 the control of inverters operating in islanded-mode is described. Two different inverter fault models are developed and their characteristics described in Section 3. An islanded microgrid supplied by an IIDG unit has been modelled in PSCAD and recreated in an experimental setup to back the proposed models and illustrate their application. Section 4 illustrates the application of the fault models to fault analysis and then compares the analytical results with the experimental and time-domain simulation results.

II. Stand Alone Inverter Control

The presence of DG can provide a supply to customers in a network where the utility connection is unavailable due to unplanned or planned islanding [12]. A typical IIDG unit and its control structure for islanded-mode operation is shown in figure 1. The primary source produces DC power which is stored in the DC bus and then converted to AC power by the inverter. For the purpose of analyzing the inverter fault response, the primary source is considered as ideal and the DC bus dynamics are neglected [10], [4].

The control of a single inverter operating in islanded mode is focused on regulating output voltage magnitude and frequency. The multi-loop control structure in figure 1 is popular because it provides good dynamic performance and disturbance rejection and the presence of an explicit current reference facilitates inclusion of a current limit [12]. The inverter is
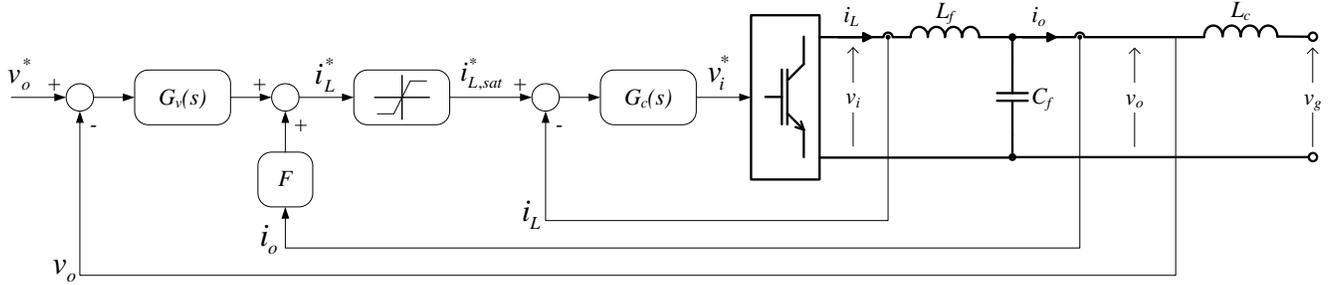
Figure 1: Multi-loop control of a stand-alone inverter.

interfaced to the network through a low pass filter (L_f and C_f) and a coupling inductance (L_{cc}). The inner loop regulates the inductor current i_L and is usually designed to have a high bandwidth (e.g. here around 1.6kHz). The outer loop regulates the output voltage v_o across the filter capacitor by setting a current demand for the inner loop and is designed with a slower bandwidth (e.g. 400Hz). Blocks $G_v(s)$ and $G_c(s)$ contain the transfer functions of the voltage and current regulators and F is a feed-forward transfer function chosen to attenuate output current disturbances. In case of a single inverter, it is sufficient to hold the output voltage reference v_o^* constant (in magnitude and frequency). For a system with multiple inverters, frequency and voltage droops might be applied for power sharing [14].

The multi-loop control structure in figure 1 can be implemented in various reference frames. A popular choice of reference frame [12], [14], is the Synchronous Reference Frame (SynRF or $dq0$ coordinates). The new variables result from the Clarke and Park transformation of the original phase variables. If only the Clarke transformation is applied [15], then the control is implemented in the Stationary Reference Frame (StatRF or $\alpha\beta0$ coordinates). If no transformation is involved, the control is implemented in the Natural Reference Frame (NatRF or abc coordinates), as described in [16]. The control in the SynRF is popular because the DC signals resulting from the Park transformation can be regulated to zero steady-state error by PI compensators. However, with the advent of P+R (proportional + resonant) compensators, the use of the NatRF has been gaining popularity for control of islanded inverters [17], grid-connected inverters [18], [19] and in particular where there is a need for good synchronization during unbalanced operation [20]. As a result, in this paper, control in both reference frames is considered and analyzed for four-leg three-phase inverters. This is necessary if single phase loads are to be supplied. The fourth leg also provides a return path for any fault current. How to orderly resume power export once a fault has been cleared is considered out of scope. All calculations have been performed in actual values rather than in per unit as the paper considers a network with only one voltage level.

III. INVERTER FAULT MODELS

An understanding of inverter fault behaviour can be developed by starting with the equivalent model of the multi-loop inverter control in figure 1 and then by analyzing how

it changes in the event of a fault. This general fault model can then be adapted to the two control schemes under study (SynRF and NatRF) to yield specific fault models.

A. Multi-loop controlled inverter during a network fault

It is common practice to summarise the control strategy by expressing the relation between the output voltage v_o, the reference v_o^* and the load current i_o. The relationship can be expressed in the complex frequency domain by replacing the current control loop in figure 1 with its closed-loop transfer function $G_{cc}(s)$ [12]:

$$V_o(s) = G(s)V_o^*(s) - Z_o(s)I_o(s) \qquad (1)$$

where

$$G(s) = \frac{G_v(s)G_{cc}(s)}{sC_f - G_v(s)G_{cc}(s)} \qquad (2)$$

is the inverter voltage gain and

$$Z_o(s) = -\frac{FG_{cc}(s) - 1}{sC_f + G_v(s)G_{cc}(s)} \qquad (3)$$

is the output impedance. The inverter is therefore modelled as an equivalent two-terminal circuit as shown in figure 2a. A design objective for $G_v(s)$ would be to make $G(s)$ close to unity in the low frequency range.

Under fault conditions, the current limit of the inverter will be applied using a saturation function on the inductor current reference i_L^*, as shown in figure 1. In the event of a fault, the current in the network increases and as saturation is reached, the voltage feedback loop is broken. This break in the loop reduces the two-loop control of the inverter to a single current loop control. The output voltage is then determined by the current injected into the filter capacitor and the following relationship applies:

$$V_o(s) = \left(G_{cc}(s)I_{L,sat}^* - I_o(s)\right)\frac{1}{sC_f} \qquad (4)$$

where $i_{L,sat}^*$ is the reference maximum inductor current. Rearranging (4):

$$I_o(s) = G_{cc}(s)I_{L,sat}^* - sC_fV_o(s) \qquad (5)$$

At the operating frequency, the transfer function $G_{cc}(s)$ has a gain close to unity and so the inverter behaves like a constant current source with a parallel impedance as shown in figure 2b. There will also be an initial transient resulting from the dynamics of the current control loop. However, because of the

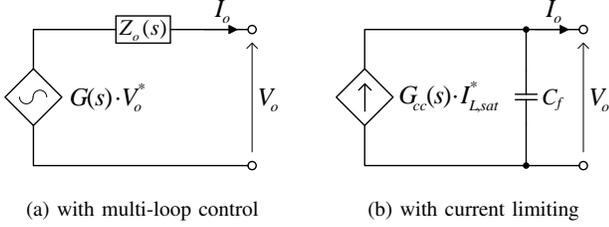(a) with multi-loop control   (b) with current limiting

Figure 2: Equivalent two-terminal circuit of a stand-alone inverter

high bandwidth of this loop, the settling time of this transient can be assumed near-instantaneous. The general model shown in figure 2b, must now be adapted to the particular response of the inverter controllers according to the employed reference frame and the type of fault.

B. Fault model of an inverter controlled in the SynRF

The control of an islanded inverter using $dq0$-coordinates requires three loops identical to the one in figure 1, one for each coordinate [12]. The saturation blocks are placed in the each of the three current loops to limit I_{Ld}^*, I_{Lq}^* and I_{L0}^*. The current limits latch and hold the current to a limited value (i.e. $I_{L,sat,d}^*$, $I_{L,sat,q}^*$ and $I_{L,sat,0}^*$) until the fault clears. Without such a provision, the saturation would be applied to the instantaneous values which can lead to harmonic distortion (clipping). From figure 1 and applying the current saturation, (4) can be written for each coordinate as:

$$v_{od} = \left(G_{cc}(s)I_{L,sat,d}^* - I_{od} + \omega C_f v_{oq}\right)\frac{1}{sC_f}$$

$$v_{oq} = \left(G_{cc}(s)I_{L,sat,q}^* - I_{oq} + \omega C_f v_{od}\right)\frac{1}{sC_f} \qquad (6)$$

$$v_{o0} = \left(G_{cc}(s)I_{L,sat,0}^* - I_{o0}\right)\frac{1}{sC_f}$$

It is apparent that during a fault the inverter becomes equivalent to a balanced, three-phase, positive sequence current source parallel to the filter capacitor, the equivalent single-line diagram of which is shown in figure 2b. The appearance of the coupling terms stems from the application of the Park transformation to the capacitor voltages and represent the capacitor's conductance at the grid frequency. Assuming the closed current loop transfer function has a unity gain at the system operating frequency and deals with the capacitive coupling, the inverter fault model in abc-coordinates can be found by applying inverse Park and Clarke transformations to (6):

$$v_{oa} = \left(I_{L,sat,a}^* - I_{oa}\right)\frac{1}{sC_f}$$

$$v_{ob} = \left(I_{L,sat,b}^* - I_{ob}\right)\frac{1}{sC_f} \qquad (7)$$

$$v_{oc} = \left(I_{L,sat,c}^* - I_{oc}\right)\frac{1}{sC_f}$$

The three-phase, positive sequence equivalent current source with parallel filter capacitor described by (7) is shown in figure

3a. The values of the current sources can be calculated from $I_{L,sat,d}^*$ and $I_{L,sat,q}^*$ as follows:

$$I_{L,sat,a}^* = \sqrt{2/3}I_{L,sat,dq}^* e^{j\phi_{dq}}$$
$$I_{L,sat,b}^* = \alpha^2 I_{L,sat,a}^* \qquad (8)$$
$$I_{L,sat,c}^* = \alpha I_{L,sat,a}^*$$

where $\alpha = -0.5 + j0.5\sqrt{3}$ is the Fortescue operator, $I_{L,sat,dq}^* = \sqrt{I_{L,sat.d}^{*2} + I_{L,sat,q}^{*2}}$, $\phi_{dq} = \arctan\frac{I_{L,sat,q}^*}{I_{L,sat,d}^*}$ and $I_{L,sat,0}^* = 0A$.

C. Fault model of an inverter controlled in the NatRF

Control of an islanded inverter in the NatRF again requires three multi-loop controllers [16], one for each phase coordinate. The key differences between control in the NatRF and in the SynRF are the ability of the NatRF controller to regulate the voltage of each phase independently and the possibility to limit the inductor phase currents separately. Latching current limits are used which apply a sinusoidal reference current of amplitude equal to the maximum inverter current to the phases that experienced an over-current until the fault clears. The healthy phases continue to operate in voltage control mode. As a consequence, the equivalent fault model of the inverter depends on the type of fault. For example, for a single phase-to-ground (A-G) fault on phase a, only phase a is current limited and the equivalent circuit of figure 2b applies while phases b and c are voltage controlled and the Thevenin equivalent circuit of figure 2a applies. The resulting equivalent fault model of the inverter in phase coordinates is shown in figure 3b. In the circuit corresponding to phase a, the current source is given by $G_{cc}(s)I_{L,sat,a}^*$, where $I_{L,sat,a}^*$ is the maximum inverter current and the parallel impedance $Z_{c,a}(s)$ is equal to $Z_{C_f}(s) = \frac{1}{sC_f}$. The closed loop transfer function of the current loop can be expressed as:

$$G_{cc}(s) = \frac{G_c(s)N(s)}{1 + G_c(s)N(s)} \qquad (9)$$

where $N(s)$ is the LC filter transfer function, as explained in Appendix A, and defined as follows:

In the circuits corresponding to phases b and c in figure 3b, the voltage sources are given by $G(s)V_{0_b}^*$ and $G(s)V_{0_c}^*$ where $G(s)$ is the inverter voltage gain and V_{0b}^* and V_{0c}^* are the nominal reference phase voltage values. The inverter voltage gain is calculated as in (2) and the series connected output impedances are given by:

$$Z_{0b(s)} = Z_{0c(s)} = Z_0(s) = -\frac{FG_{CC}(s) - 1}{sC_f + G_V(s)G_{CC}(s)} \qquad (11)$$

In order to use the same form of model for each phase, the Thevenin models of the healthy phases can be transformed to their Norton equivalents as shown in figure 3c. The Norton equivalent source current is given by:

$$I_{Norton}(s) = \frac{G(s)}{Z_o(s)}V_o^* \qquad (12)$$

The models in figure 3a and figure 3c refer to different control methods but are presented in the same form. This common representation helps in understanding the different fault response

$$N(s) = \frac{I_L(s)}{v_i(s) - v_o(s)} = \frac{s\left(L_f + 2L_n\right) + R_f + 2R_n}{s^2\left(L_f^2 + 3L_fL_n\right) + s\left(2R_fL_f + 3R_fL_n + 3R_nL_f\right) + R_f^2 + 3R_fR_n} \tag{10}$$

(a) Model for any type of fault with control in SynRF

(b) Model for a single phase fault with control in NatRF

(c) Model for a single phase fault with control in NatRF (Norton equivalent)
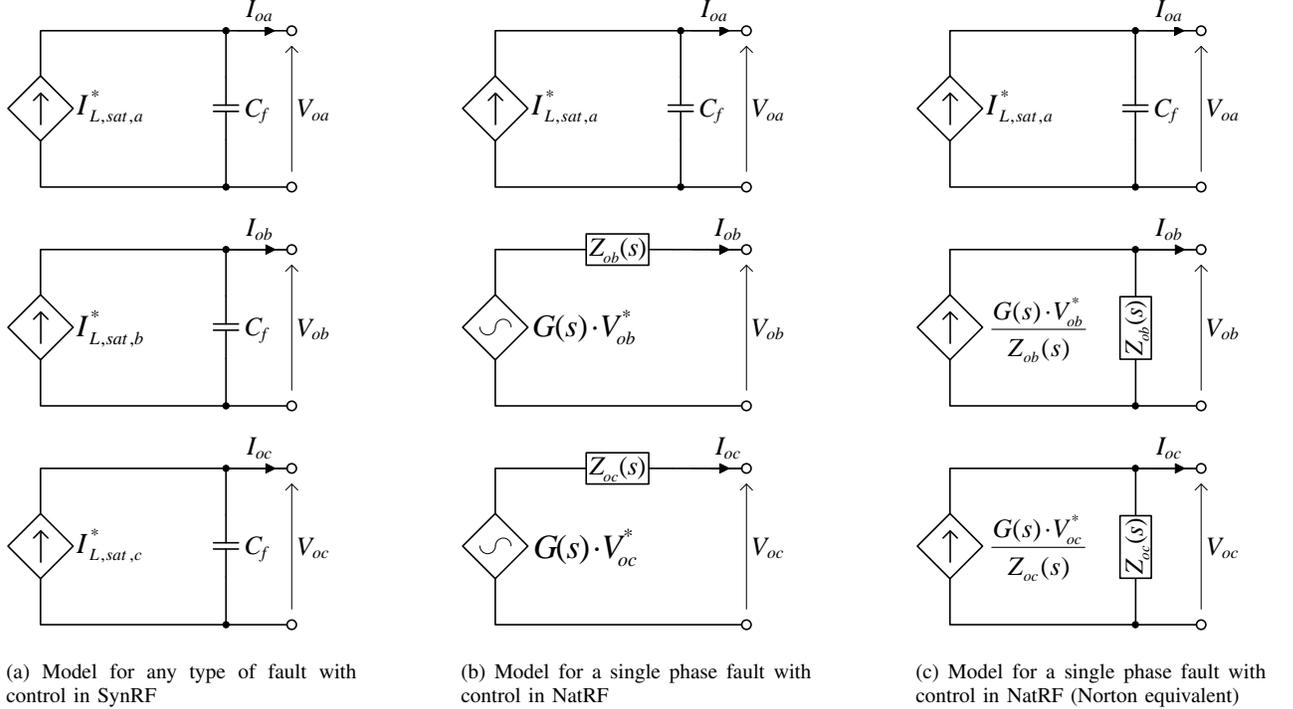
Figure 3: Equivalent phase networks of a three-phase inverter

given by the two control methods. In particular, it should be noted that in figure 3a the impedances are physical but in figure 3c two impedances are equivalent output impedances determined by the control of the inverters. Moreover, the amplitude and transfer functions of the current sources also differ.

IV. SIMULATION AND EXPERIMENTAL RESULTS

To validate the models developed in the previous section, an experimental set-up has been created in which a single $3kVA$ inverter feeds a single $1.7kW$ load through a $300V_{rms,l-l}$ distribution line. At $t = 0s$ a fault is applied in the middle of the line. A per-phase representation of the test network is illustrated in figure 4 showing the inverter parallel impedances Z_c, the coupling impedances Z_{cc}, the line impedances Z_{line}, the fault impedances Z_{fault}, and the load impedances Z_{load}. The inverter AC front end is connected to the terminals labelled a, b, c and n. Due to practical restrictions, there is no impedance in the neutral return path. The fault impedances are connected between nodes 7,8,9 and 0, and can be arranged so as to recreate any type of fault. The inverter is controlled using the TRIPHASE rapid prototyping software suite [22] which allows MATLAB SIMULINK control programs to be run on a real-time Linux PC as inverter controller. Current and voltage measurements are downloaded back into MATLAB for immediate plotting and analysis. The parameters
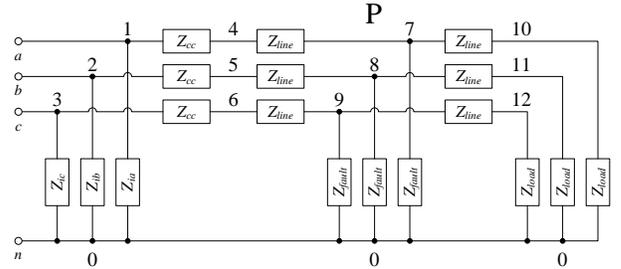

Figure 4: Test network

of the test network components have been given in table I. The quasi steady-state fault models will now be used to quantify the fault currents and voltages for comparison with the experimental results. Traditional fault analysis based on symmetrical components is difficult to apply in the case of an inverter under NatRF control facing an asymmetric fault. In this case, the inverter presents unbalanced phase impedances, while the use of symmetrical components is normally based on a single point of unbalance, being the fault itself. Nevertheless, the behaviour of the two example microgrid models in the event of a fault can still be assessed using circuit analysis if an equivalent direct phase coordinate representation of the network is constructed as shown in figure 4. This circuit can be represented by an equivalent bus impedance matrix

Table I: Test Network Parameters

Symbol	Value	Unit
L_f	2.3	mH
R_f	0.01	Ω
C_f	26.4	μF
ESR	0.05	Ω
L_n	1.15	mH
R_n	0.01	Ω
L_{cc}	0.93	mH
R_{cc}	0.01	Ω
L_{line}	0.35	mH
R_{line}	0.2	Ω
R_{load}	52.9	Ω
R_f	2	Ω
$I_{L,sat,dq}^*$	$15 + j0$	A
$|v_o^*|$	300	$V_{rms,l-l}$

Table II: Inverter controller realisations

SynRF	$G_v(s)$	$G_c(s)$	F
d & q	$0.05\left(1 + \frac{1000}{s}\right)$	$23\left(1 + \frac{1600}{s}\right)$	0.7
0	$0.05 + 200\frac{s}{s^2 + \omega_s^2}$	$30\left(1 + \frac{1600}{s}\right)$	0.7

NatRF	$G_v(s)$	$G_c(s)$	F
a,b & c	0.12	17	1

Z_{BUS} based on an explicit representation of every node in the network. After Z_{BUS} is determined, the system behaviour is described by the relationship:

$$V = Z_{BUS}I \qquad (13)$$

where V are the node voltages referred to the reference node and I are the currents entering the nodes from the current sources. Voltages and currents are expressed in phase quantities because the bus impedance matrix is built by considering each single node in the network. In the event of a fault, the original Z_{BUS} of (13) can be replaced by $Z_{BUSfault}$ which incorporates the modifications introduced by the fault impedance and the appropriate inverter parallel output impedances. The node voltages can be determined by applying the injected currents corresponding to the models in figures 3a and 3c. The fault analysis using (13) is completely general and can be extended to multiple inverters. The analytical process to find the fault currents and voltage in the microgrid consists of the following steps:

1) Include fault impedances in the network of figure 4 to represent the desired type of fault. A three phase to ground fault is shown.
2) Based on the quasi steady state models developed in this paper choose the right value for the parallel impedances Z_{ia}, Z_{ib} and Z_{ic}:
   a) If the inverter is controlled in the SynRF, then the parallel impedances are physical and equal to the filter capacitor impedance:

   $$Z_{ia}(s) = Z_{ib}(s) = Z_{ic}(s)$$
   $$= Z_{C_f}(s) = \left(ESR + \frac{1}{j\omega_s C_f}\right)\Omega$$

   b) If the inverter is controlled in the NatRF, then only the faulty phase will go into current limiting mode and the healthy phases remain in voltage control mode. For the faulty phases, the parallel impedance is again given by the filter capacitor impedance:

   $$Z_{i,faulty}(s) = Z_{C_f}(s)$$

   and for the healthy phases the parallel impedance is given by the Norton equivalent output impedance of (3). It is thus a virtual impedance which depends on physical impedances as well as control system parameters:

   $$Z_{i,healthy}(s) = Z_o(s) = -\frac{FG_{cc}(s) - 1}{sC_f + G_v(s)G_{cc}(s)}$$

3) Construct the bus impedance matrix $Z_{BUSfault}$ corresponding to the faulty microgrid.
4) Determine the current vector representing the currents injected into each node of the test network. Only nodes connected to the inverter will have non-zero values:
   a) If the inverter is controlled in the SynRF, then for any type of fault the inductor currents are given by (8) and the current vector I is given by

   $$I = \begin{bmatrix} I_{L,sat,a}^* & I_{L,sat,b}^* & I_{L,sat,c}^* & 0 & \cdots & 0 \end{bmatrix}^T$$

   b) If the inverter is controlled in the NatRF, then the inductor currents in the faulty phase are given by the corresponding inductor phase current in (8):

   $$I_{L,faulty}^* = \alpha^n \sqrt{2/3} I_{L,sat,dq}^* e^{j\phi_{dq}}$$

   where $n = 3, 2, 1$ for phases a, b and c, respectively. The healthy phases maintain voltage control and are replaced with their Norton equivalent circuits as shown in figure 3c. The Norton equivalent source current is given by (12):

   $$I_{Norton}(s) = \frac{G(s)}{Z_o(s)} V_o^*$$

   and the current vector I for e.g. a single phase to ground fault (A-G) is given by:

   $$I = \begin{bmatrix} \frac{G(s)}{Z_{oa}(s)} V_{oa}^* & I_{L,sat,b}^* & I_{L,sat,c}^* & 0 & \cdots & 0 \end{bmatrix}^T$$

5) Compute $V = Z_{BUS}I$ to find the nodal voltages. Line currents can be obtained from the nodal voltages and line impedances.

In the same manner, inductor currents and output voltages have been calculated for inverters under both SynRF and NatRF control for no fault, three phase, single phase, and phase-phase faults. The results have been shown in table III. The fault response of an inverter operating in islanded-mode is almost instantaneous. Indeed, the only dynamic process involved is that of the current loop which is designed with a high bandwidth. It is therefore possible to represent the islanded inverter, in the event of a fault, with quasi stead-state models like the ones in figure 2. The models are considered valid until the fault clears or until the inverter is disconnected because the fault has not cleared within an expected time.

	NatRF			
	no fault	$3\phi - g$	$1\phi - g$	$\phi - \phi$
$\hat{I}_{L_a}[A]$	$5.0\angle23.4°$	$12.2\angle-3.8°$	$12.2\angle-3.8°$	$12.2\angle-3.8°$
$\hat{I}_{L_b}[A]$	$5.0\angle-96.6°$	$12.2\angle-123.8°$	$5.0\angle-101.2°$	$12.2\angle-123.8°$
$\hat{I}_{L_c}[A]$	$5.0\angle143.4°$	$12.2\angle116.2°$	$5.0\angle138.8°$	$5.0\angle138.8°$
$\hat{v}_{o_a}[V]$	$244.9\angle0°$	$26.6\angle5.8°$	$26.6\angle5.8°$	$290.0\angle-85.2°$
$\hat{v}_{o_b}[V]$	$244.9\angle-120°$	$26.6\angle-114.2°$	$245.2\angle-124.6°$	$309.6\angle-89.1°$
$\hat{v}_{o_c}[V]$	$244.9\angle120°$	$26.6\angle125.8°$	$245.2\angle115.4°$	$245.2\angle115.4°$
	SynRF			
$\hat{I}_{L_a}[A]$	$5.0\angle23.4°$	$12.2\angle-3.8°$	$12.2\angle-3.8°$	$12.2\angle-3.8°$
$\hat{I}_{L_b}[A]$	$5.0\angle-96.6°$	$12.2\angle-123.8°$	$12.2\angle-123.8°$	$12.2\angle-123.8°$
$\hat{I}_{L_c}[A]$	$5.0\angle143.4°$	$12.2\angle116.2°$	$12.2\angle116.2°$	$12.2\angle116.2°$
$\hat{v}_{o_a}[V]$	$244.9\angle0°$	$26.6\angle5.8°$	$26.6\angle5.8°$	$290.0\angle-85.2°$
$\hat{v}_{o_b}[V]$	$244.9\angle-120°$	$26.6\angle-114.2°$	$597.3\angle-147.2°$	$307.6\angle-89.1°$
$\hat{v}_{o_c}[V]$	$244.9\angle120°$	$26.6\angle125.8°$	$597.3\angle92.8°$	$597.3\angle92.8°$

Table III: Fault currents and voltages

Focusing now only on the islanded microgrid, the results of two experiments are presented: in the first one the inverter is controlled in the SynRF, in the second one the NatRF control is used. Each plot in figure 5 shows the measured output voltage (top) and inductor current (bottom) as thick solid sinusoidal lines. The analytical results from table III have been plotted as thin black dotted horizontal lines for direct comparison with the peak values of the experimental measurements. The envelope created by these analytical results has been plotted as a thick horizontal black line. Results from time domain simulations in PSCAD have been plotted underneath the measured variables where appropriate, as thin grey solid lines to show where the experimental measurements deviate from the ideal results. This is only visible when the inverter voltage clips due to a limited DC link voltage.

Figures 5a, 5c and 5e show the response of the inverter controlled in the SynRF to a three-phase, single-phase and phase-to-phase fault applied at point P in figure 4 at time $t = 0s$. Voltages v_{oa}, v_{ob} and v_{oc} represent the phase voltages at the output of the filter while $I_{L,a}$, $I_{L,b}$ and $I_{L,c}$ are the controlled inductor currents.

It is clear that, following the fault, the inverter quickly establishes a new set of currents and voltages. As the inverter attempts to inject balanced set of fault currents, the network voltages are dependent on fault type. The balanced fault leads to uniform under-voltage whereas the single phase fault produces a large over-voltage on the healthy phases. This can lead to a current controller voltage demand which exceeds the maximum available DC-link voltage. This then results in the clipping observed in figures 5c and 5e. The thin grey lines indicate the bridge voltage trajectory that the current controller was attempting to follow. This clipping introduces harmonic distortion and causes the current control loop to be broken, leading to distortion of the inductor current.

Turning now to NatRF control, figures 5b, 5d and 5f show the response to a three-phase fault, a single phase fault and a phase-phase fault. The response to the three-phase fault is very similar to that for SynRF control because the fault model is similar (i.e., figure 3a). In contrast, the response to the single phase-to-ground fault is very different. Under NatRF control, the injection of fault current occurs only for the faulted phase a, whereas the healthy phases b and c remain uder voltage control and do not experience a voltage rise.

This ability of the control in NatRF to regulate the voltage of each phase independently can be considered an advantage. In the event of a fault, the supply of power is kept unchanged in the healthy phases while the current is only actively limited in the faulty phases. This behaviour could be particularly advantageous when the number of disrupted single-phase customers has to be kept to a minimum. Finally, from figures 5b, 5d and 5f it is confirmed that, under control in the NatRF the transient response of the inverter is again very rapid.

It can be seen that, except for the case where voltage limiting occurs, the analytical results from table III match the experimental results from figure 5 very well i.e. the calculated voltage and current magnitudes agree with the measurements. This proves that with simple analytical models, fault currents and voltages can be calculated for single inverter-fed microgrids with relative ease. It also provides a case against current limiting in the $dq0$-reference frame as it a) can lead to harmonic distortion due to a limited DC-link voltage and b) it means the inverter fault current is actively pushed through healthy phases, and therefore through the loads connected to them. This can lead to adverse side effects in load operation.

V. CONCLUSION

As the number of inverter-interfaced DG sources increases, it is important to understand and visualise how these sources respond in the event of a fault and how they contribute
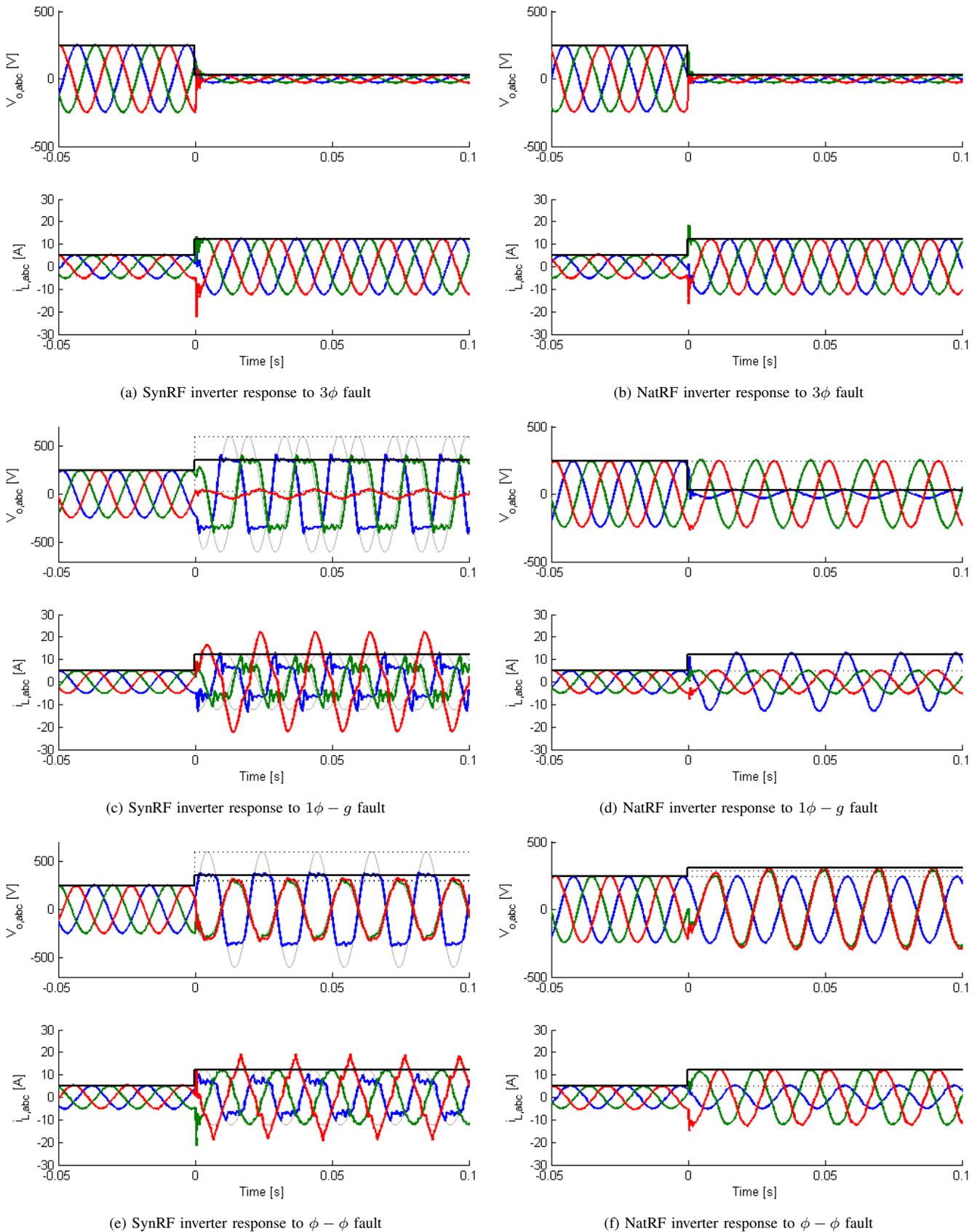
Figure 5: Matlab plots of experimental (thick dark grey solid sinusoidal), analytical (thin black horizontal dotted) & simulation (thin light grey solid sinusoidal) results

to system fault behaviour. This paper has outlined the development of analytical fault models for inverter-interfaced DG sources that can be integrated into traditional impedance models of faulted networks. The focus is placed on capturing and illustrating the inverter control loops and their reference frame implementation as these are the main factors responsible for shaping the response of the inverter in the event of a fault.

To validate the developed models, a laboratory scale islanded microgrid has been built and subjected to various types of fault. Measurements from the experiments for different faults are shown to be in good agreement with numerical results from the analytical faults studies of the example system. The experimental results also highlight the comparatively small fault currents but fast transient response characterising inverter-interfaced sources. The difference in fault response due to choice of reference frame is shown by representing both cases in a per-phase coordinate representation. It is shown that current limiting in the synchronously rotating reference frame can lead to overvoltages and harmonic distortion and is thus undesirable. Finally, the paper gives an example on how to include these models in quasi steady-state fault analysis based on a per-phase coordinate representation of the network.

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