High-performance Zinc Oxide Thin-Film Transistors For Large Area Electronics

By

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I hereby declare that this thesis is the result of my own investigations, which have been carried out by me, between October 2007 and November 2010 in the Experimental Solid State Physics group of Imperial College London, under the supervision of Dr Thomas D. Anthopoulos. The results quoted from other workers have properly been referred to. I further declare that this thesis as a whole or any part thereof has not been submitted by me for the award of any research degree, to this university or any other University or Institution.

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Abstract

The increasing demand for high performance electronics that can be fabricated onto large area substrates employing low manufacturing cost techniques in recent years has fuelled the development of novel semiconductor materials such as organics and metal oxides, with tailored physical characteristics that are absent in their traditional inorganic counterparts such as silicon. Metal oxide semiconductors, in particular, are highly attractive for implementation into thin-film transistors because of their high charge carrier mobility, optical transparency, excellent chemical stability, mechanical stress tolerance and processing versatility.

This thesis focuses on the development of high performance transistors based on zinc oxide (ZnO) semiconducting films grown by spray pyrolysis (SP), a low cost and highly scalable method that has never been used before for the manufacturing of oxide-based thin-film transistors. The physical properties of as-grown ZnO films have been studied using a range of techniques. Despite the simplicity of SP, as-fabricated transistors exhibit electrical characteristics comparable to those obtained from ZnO devices produced using highly sophisticated deposition processes. In particular, electron mobility up to 25 cm^2/Vs has been achieved in transistors based on pristine ZnO films grown at 400 °C onto Si/SiO_2 substrates utilising aluminium source-drain (S-D) electrodes. A strong dependence of the saturation mobility on the work function of S-D electrodes and the transistor channel length (L) has been established. Short channel transistors are found to exhibit improved performance as compared to long channel ones. This was attributed to grain boundary effects that tend to dominate charge transport in devices with $L < 40$ μm.

High mobility, low operating voltage (<1.5 V) ZnO transistors have also been developed and characterised. This was achieved through the combination of SP, for the deposition of ZnO, and thermally stable solution-processed self-assembling monolayer gate dielectrics.

Detailed study of the temperature dependence of the operating characteristics of ZnO transistors revealed a thermally activated electron transport process that was described by invoking the multiple trapping and release model. Importantly, ZnO transistors fabricated by SP are found to exhibit highly stable operating characteristics with a shelf lifetime of several months. The simple SP-based fabrication paradigm demonstrated in this thesis expands the possibilities for

the development of advanced simple as well as multi-component oxide semiconductors far beyond those accessible by traditional deposition methods such as sputtering. Furthermore, it offers unprecedented processing scalability hence making it attractive for the manufacturing of future ubiquitous oxide electronics.

Contents

List of figures 9
Acknowledgments 12
List of symbols and acronyms 13

1. Introduction to transparent electronics 15
1.1 Background 15
1.2 Motivation 19
1.3 Thesis overview 20
References 23
2. Current status of transparent oxide based electronics 24
2.1 Introduction 25
2.2 Review of prior work 27
References 37
3. Theoretical background 41
3.1 Electronic properties of transparent oxide semiconductors (TOS): introduction 42
3.2 Electronic structure and carrier generation 42
3.3 Conduction pathways and characterising models 45
3.3.1 Band like charge transport 46
3.3.2 Hopping transport and simple model 46
3.3.3 Charge trapping: Multiple trapping and release model 48
3.3.4 Grain boundary limited charge transport 51
3.4 Thin film transistors 52
3.4.1 Device architecture and fundamental operation . . 52
3.4.2 Gradual channel approximation model for thin film transistors 54
3.4.3 Thin film transistor operation: parameter calculation 56
3.4.4 The role of dielectric-semiconductor interface in thin film transistors 59
3.4.5 Trap density estimation 61

3.4.6 Metal semiconductor junctions: role of contact resistance in thin film transistors 63
3.5 Ambipolar thin film transistors 66
3.5.1 Device operation 66
3.5.2 Ambipolar thin film transistors based on semiconductor heterostructures 68
3.6 Voltage inverter: The NOT gate 68
References 71
4. Experimental methods 78
4.1 Material fabrication and characterisation 79
4.1.1 Thermal analysis of zinc precursor 79
4.1.2 ZnO thin film deposition by spray pyrolysis 79
4.1.3 X-ray diffraction 82
4.1.4 Atomic force microscopy (AFM) 83
4.1.5 Ultraviolet-visible optical spectroscopy 84
4.1.6 Surface energy analysis 85
4.2 Device fabrication 86
4.2.1 Substrates 86
4.2.2 Metal contact deposition 87
4.2.3 Self assembly of organic molecules on metal electrodes 87
4.2.4 Spin coating 88
4.3 Electrical characterization 88
4.3.1 Current-voltage characteristics and circuit measurements 88
4.3.2 Capacitance-voltage measurements 90
References 92
5. High performance ZnO transistors by spray pyrolysis 94
5.1 Introduction 95
5.2 Characterization of ZnO thin films deposited by spray pyrolysis 98
5.2.1 Thermal analysis of precursor compounds 98
5.2.2 X-ray diffraction characterisation of ZnO films 99
5.2.3 Atomic force microscopy of ZnO films 100

5.2.4 Optical transmission spectroscopy of ZnO films . . 102
5.3 ZnO transistors using SiO_2 as gate dielectric 103
5.3.1 Device fabrication 103
5.3.2 Current voltage characteristics of ZnO transistors . . 103
5.3.3 Effect of metal electrodes on parasitic contact resistance 107
5.3.4 Unipolar voltage inverters based on ZnO transistors 110
5.4 Low voltage ZnO transistors based on self assembled nano dielectrics 112
5.4.1 Introduction 112
5.4.2 Self assembled monolayer dielectrics and transistor fabrication 113
5.4.3 Metal insulator semiconductor capacitors based on ZnO and SAM dielectric 115
5.4.4 Low voltage ZnO transistors based on SAM Dielectric 118
5.4.5 Low voltage unipolar ZnO transistors based inverters 120
5.5 Top gate ZnO transistors and effect of plasma treatment 121
5.5.1 Device fabrication 121
5.5.2 Top gate ZnO transistors based on CYTOP dielectric 122
5.5.3 Dual gate ZnO transistors 124
5.6 Summary 127
References 129
6. Solution processed hybrid thin film transistors 136
6.1 Introduction 137
6.2 Experimental 139
6.2.1 Material systems used and device fabrication 139
6.2.2 Film characterisation 141
6.3 Hybrid ambipolar thin film transistors 143
6.3.1 Air stability of hybrid ambipolar transistors 147

6.4 Inverters based on hybrid ambipolar transistors 148
6.5 Summary 149
References 150
7. Charge transport in ZnO thin-film transistors 153
7.1 Introduction 154
7.2 Temperature dependent field-effect measurements 155
7.2.1 Temperature dependent current-voltage characteristics 156
7.2.2 Temperature dependence of electron mobility In ZnO transistors. 157
7.2.3 Meyer Neldel rule and multiple trapping 158
7.3 Electron transport in polycrystalline ZnO films 160
7.3.1 Grain boundary scattering: Levinson plot for ZnO transistors 161
7.3.2 Trap density comparison 162
7.3.3 Evaluation of density of states in the band gap 163
7.4 Summary 164
References 165
8. Ambient and bias stress stability of ZnO transistors 169
8.1 Introduction 170
8.2 Experimental details 171
8.3 Temporal evolution of ZnO transistor characteristics 171
8.4 Bias stress characteristics of ZnO transistor 173
8.4.1 Electrical characteristics of ZnO transistors under gate bias 174
8.5 Summary 177
References 179
9. Summary of results and future outlook 181
A List of publications 186

List of figures

1.1 Past, present and future of transparent electronics 18

1.2 Examples of transparent electronics 20

2.1 Glass substrates coated with a conductive layer of ITO 26

2.2 Organic light-emitting diode (OLED) display 26

2.3 Output electrical characteristics of a ZnO TFT 28

2.4 Transfer curves for zinc tin oxide TFT 30

2.5 Schematic of bottom gated ZnO TFT fabricated 32

2.6 Frequency and propagation delay as a function 33

2.7 Ouput characteristics of Indium zinc oxide 35

3.1 Energy gap formation in TOS 43

3.2 Schematic band structure of TOS 44

3.3 Energy levels in a disordered semiconductor 45

3.4 Potential barrier and potential well for grain 51

3.5 Thin film transistor model 53

3.6 The transfer characteristics of an ideal TFT 56

3.7 The Metal dielectric semiconductor band structure 60

3.8 Energy band diagram of a metal semiconductor 64

3.9 Calculated operating characteristics of an ambipolar transistor . . 67

3.10 Schematic Inverter circuits 69

4.1 Schematic representation of the spray pyrolysis 81

4.2 Bragg's law 82

4.3 Schematic representation of an atomic force microscope 84

4.4 Contact angles between liquid and a solid surface 85

4.5 Chemical structure of the octadecylphosphonic acid 88

4.6 Schematic semiconductor analyser 89

4.7 Schematic for capacitance measurements 90

5.1	An array of transparent thin-film transparent	96
5.2	Chemical structure of Zn Ac	97
5.3	Thermo gravimetric analysis of Zn Ac	98
5.4	X-ray diffraction patterns, and average ZnO crystal size	100
5.5	AFM of ZnO films	101
5.6	Optical transmission spectra of ZnO films	102
5.7	BG-TC Transfer and output characteristics	104
5.8	BG-BC Transfer and output characteristics	104
5.9	Electron mobility against deposition temperature	106
5.10	Contact resistance data obtained from ZnO TFTs	108
5.11	Ratio of R_C to R_T as a function of L	108
5.12	Contact resistance (R_C) for Au, Al and Ca	109
5.13	Output characteristics of unipolar inverter	111
5.14	Contact angle measurements	114
5.15	Current density as a function of voltage	115
5.16	C-V characteristics of low voltage MIS capacitors	116
5.17	Normalised C-V characteristics of ZnO MIS	117
5.18	Low voltage Transfer and output characteristics	119
5.19	Low voltage unipolar inverter	121
5.20	Chemical structure of CYTOP	122
5.21	Transfer characteristics of a top gate ZnO TFT	123
5.22	Comparison of BG and TG characteristics	125
5.23	Transfer characteristics of a dual gate ZnO TFT	126
6.1	Chemical structures of the solution processible materials	139
6.2	Energy levels of Au with ZnO	140
6.3	AFM and microscopic image of	141
6.4	Transmission spectrum of ZnO/organic layer	142

6.5 Cross-section of the dual-gate hybrid ambipolar transistor . . . 143

6.6 Output characteristics of hybrid ambipolar transistor 144

6.7 Transfer characteristics of hybrid ambipolar transistor 145

6.8 P-type characteristics 146

6.9 N-type characteristics 146

6.10 Air stability of channel on and off currents 147

6.11 Transfer characteristics of the hybrid voltage inverter 148

7.1 Transfer characteristics for ZnO TFT against temperature 156

7.2 Arrhenius plots of the average mobility at all temperature . . . 158

7.3 Arrhenius plots of the average electron mobility 159

7.4 Activation energy (E_a) of electron transport 160

7.5 Levinson plots of data measured from a ZnO TFT 162

7.6 Estimation of the density of states below the conduction 164

8.1 Transfer characteristics of a ZnO TFT over 20 months 172

8.2 Evolution of the parameters overtime 172

8.3 Transfer characteristics under stress and recovery 175

8.4 Time evolution of the threshold voltage shift 176

8.6 Mobility under stress and recovery 177

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List of symbols and acronyms

TOS	Transparent oxide semiconductor
MOSFET	Metal oxide semiconductor field effect transistor
TFT	Thin Film Transistor
ICs	Integrated circuits
TTFT	Transparent Thin Film
AMLCD	Active-matrix liquid crystal displays
OLED	Organic Light Emitting Diode
SP	Spray pyrolysis
ZnO	Zinc oxide
CBM	Conduction band minimum
VBM	Valence band maximum
O	Oxygen
M	Metal
DOS	Density of States
E_F	Fermi energy (J or eV)
V_O	Oxygen vacancies
I_M	Metal interstitials
μ	Charge carrier mobility (cm2/Vs)
T	Temperature (K or ^oC)
K	Boltzmann's constant (J/K)
Q	Charge on an electron (C)
μ_{FE}	Field effect carrier mobility (cm^2/Vs)
Ci	Geometric capacitance (nF/cm^2)
V_G	Gate voltage (V)
V_D	Drain voltage (V)
k	Dielectric constant
MTR	Multiple Trapping and Release
E_T	Transport energy level (J or eV)
Nt	Areal trapped charge density (cm^{-2})
Nt(E)	Density of trap states ($eV^{-1}cm^{-2}$)
μ_{AVE}	Average charge carrier mobility (cm^2/Vs)
E_A	Activation energy (J or eV)
EMN	Meyer-Neldel energy (J or eV)

I_D	Drain current (A)
I_G	Gate current (A)
I_S	Source current (A)
W	Channel width (m)
L	Channel length (m)
Rc	Contact resistance (Ω)
R_{ch}	Channel resistance (Ω)
R_T	Total resistance (Ω)
V_T	Threshold voltage (V)
Von	Onset voltage (V)
Ion	Drain current in the transistor on-state (A)
Ioff	Drain current in the transistor off-state (A)
SS	Subthreshold slope ($Vdec^{-1}$)
SAM	Self Assembled Monolayer
V_{IN}	Input voltage (V)
V_{OUT}	Output voltage (V)
V_{DD}	Supply voltage (V)
NM	Noise margin
XRD	X-ray diffraction
AFM	Atomic Force Microscopy
UV-Vis	Ultraviolet-Visible Absorption Spectroscopy
TGA	Thermo gravimetric analysis
DSC	Differential scanning calorimetry

Chapter 1

Introduction to transparent electronics

1.1 Background

The modern era of semiconductor electronics owes its existence to the development of the metal oxide semiconductor field effect transistor (MOSFET). MOSFETs are at the heart of nearly every integrated circuit (IC) where up to several billions of discrete devices can be integrated in a single crystalline silicon (Si) chip. This extreme downscaling has enabled a range of new applications in the areas of telecommunications, personal entertainment, data processing and many more. A close relative of the traditional MOSFET is the thin-film transistor (TFT). The first TFT was demonstrated by P. K. Weimer (1) in 1965. Unlike MOSFETs, TFTs can be manufactured onto insulating large-area substrates without the need of a single-crystal wafer-type substrate. Because of this unique advantage thin-film transistors have now become the "staple" of the large-area electronics industry and have enabled the development of novel devices such as flat-panel liquid crystal displays (LCDs) where several million TFTs are usually incorporated in a single display.

Despite the various similarities between the two technologies however the technological requirements, as defined by the targeted applications, are rather different. For example, MOSFETs are used in microprocessors where extreme size

downscaling is typically required. State-of-the-art microchips are made of MOSFETs with channel length typically <50 nm. This nano-scale dimension allows fabrication of MOSFETs with extremely fast operating frequencies to be achieved that typically exceeds >100 GHz. On the other hand, the performance requirements for TFTs are very different. A representative example is the use of TFTs in optical displays where each transistor needs neither to be extremely small nor to be fast but instead to be cheap, reliable and easy to process onto large substrates that are typically the size of the optical display i.e. from 2" inches over 50" inches diagonally.

Apart from these rather extreme "high-end" applications, however, other technologies such as radio-frequency integrated circuits and various wireless networking applications demand TFTs to fulfil the combined requirements for high performance and large-area processability. As a result research efforts are increasingly focussed on developing and investigating alternative semiconductors with improved physical characteristics including; mechanical flexibility, manufacturability, optical transparency and higher carrier mobilities than those obtained from conventional Si technologies such as amorphous and polycrystalline silicon (a-Si, poly-Si).

This ever increasing demand for alternative semiconductor technologies has led to the development of a number of material systems that can potentially outperform Si for certain applications. For example, the 1980s marked the debut of a new class of TFTs based upon organic semiconductors (2, 3). Use of organic materials offers the prospect of low manufacturing cost combined with some desirable physical characteristics such as ease of processing and extreme mechanical flexibility. Since then, organic TFTs (OTFTs) are being exploited for integration onto flexible plastic substrates primarily for use in advanced lightweight and flexible optical displays. Despite the impressive progress achieved in recent years, however, a number of obstacles, especially poor air-stability and relatively low device performance, have still to be overcome before the advantageous manufacturability and hence the economic benefits associated with organic semiconductors, can be fully exploited.

While research in the area of organic semiconductors and devices has been intensifying, a different class of semiconducting materials, namely metal oxides,

has recently emerged as a possible alternative technology (4, 5). Metal oxides incorporate important qualities that are currently absent from organic-based semiconductors. For instance, they generally exhibit higher carrier mobilities which are already sufficient for use in optical displays, such as current-driven organic light-emitting diode (OLED) based displays. Furthermore, metal oxides can be made conductive, semiconductive as well as insulating depending on their chemical composition. An important advantage of oxide semiconductors which is relevant to many electronic applications is the high (>80%) optical transparency resulting from their wide bandgap (typically > 3 eV). The combination of these unique properties makes metal oxides particularly interesting for use in transparent microelectronics (6) as well as in backplanes for the next generation current-driven optical displays (7, 8).

Figure 1.1 displays the degree of expected impact of transparent electronics on the electronic industry with time. As can be seen the impact is expected to increase with time and is characterised by three technology waves. The first wave in transparent electronics already began with the utilization of transparent electrodes based on metal oxides in the 1970s (9, 10). Today oxide materials such as indium tin oxide (ITO) are key components in a range of technologies including; optical displays, touch panels and solar cells. Because of the scarcity and high cost of indium (In), however, alternative transparent oxides such as the fluorine-doped tin oxide (FTO) have been proposed, developed and are now slowly entering the market.

The second wave was initiated recently with the demonstration of the first transparent TFTs based on oxide semiconductors. The long term goal of this new technology is to enable the development of novel device concepts that are currently not accessible through the use of conventional Si-based technologies. The third wave, on the other hand, depends on the progress that will be achieved during the second wave. A key technology that is at the heart of this third wave is the availability of hole-transporting (p-type) oxide semiconductors with performance characteristics comparable to those achieved in n-type oxides (11, 12). The combination of n- and p-type oxide semiconductors is expected to enable the development of key opto-/electronic devices such as microelectronics, photovoltaics and optical sensors. In the area of microelectronics p- and n-type oxide transistors will be combined to form complementary logic circuits and hence

lead to a variety of high performance transparent electronics. In the area of optoelectronics, the availability of both p- and n-type oxides will enable the demonstration of a diverse range of devices for a host of applications including semi-transparent solar cells for smart-window applications, ultraviolet light emitting diodes (LEDs) for lighting and water purification systems and ultraviolet photodetectors.

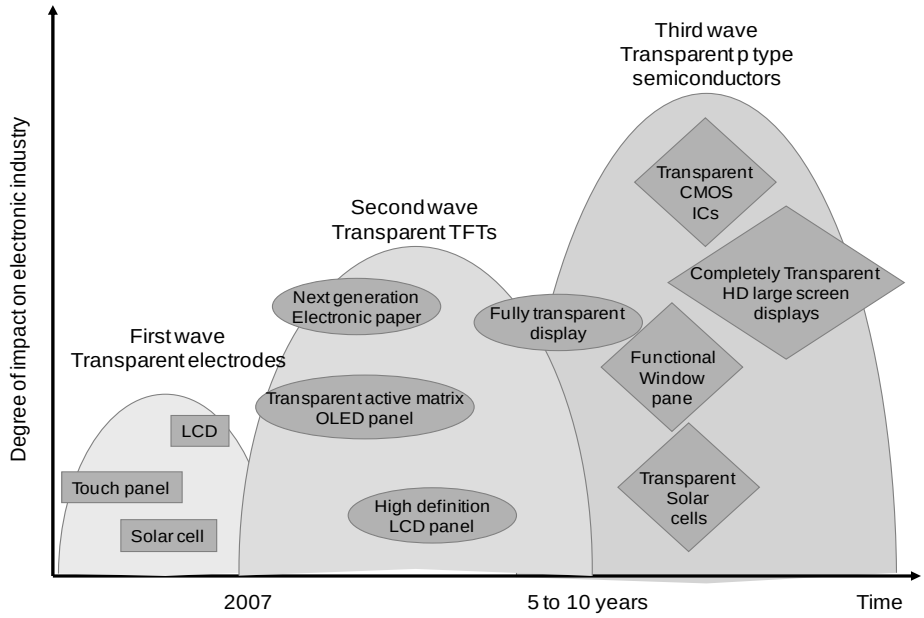

Figure 1.1: Past, present and future of transparent electronics (TE). The first wave in TE was using transparent electrodes. A number of key products such as LCD and touch panel were made possible. Transparent transistors together with electrodes are expected to lead to next generation of optical displays (13).

The ultimate target for oxide based electronics is the development of fully transparent products with performance characteristics superior to current state-of-the-art technologies. Such developments are driven by the industry's current and continuing demand for novel materials that are optically transparent, exhibit superior electrical characteristics (e.g. charge carrier mobility, ambient stability etc), are environmentally-friendly, as compared to the state-of-the-art, and less expensive to manufacture. It is now widely anticipated that such developments will create a new era of ubiquitous electronics that current semiconductor technologies cannot bring about.

1.2 Motivation

The combination of desirable physical characteristics and availability makes metal oxide highly competitive to existing thin-film transistor technologies based on more conventional semiconductors such as organics and silicon. Because of this, a range of metal oxide semiconductors are already commercially available in large quantities and at a very low cost. Most of the early work on oxides has been focussed on the development of materials and device optimization with particular emphasis on improving the charge carrier mobilities and device operating stability as well as processability.

The combination of optical transparency and the ability to drive high currents (because of the high charge mobility), metal oxide TFTs are expected to enable a number of new applications where current technologies (i.e. a-Si, poly-Si and organics) are inadequate or too expensive to implement. A good example is the polycrystalline Si (poly-Si) TFT backplanes used in various LCD displays where the fabrication of the backplane alone accounts for nearly 60% of the overall display cost (14). A few examples of potential future applications include; high refresh rate, high-definition (HD) 3D active-matrix liquid crystal displays (AMLCDs), current driven HD active-matrix organic light emitting displays (AMOLEDs), full-colour electronic paper (E-paper) based displays and a host of transparent electronics. A few of these envisioned applications are shown in Figure1.2.

In the case of high value products such as 3D-HD optical displays, oxide TFTs are also expected to enable low-cost manufacturing without compromising the device performance. This is because unlike Si, oxide TFTs can be processed using a diverse range of techniques including vacuum as well as solution based methods. To date, vacuum based techniques, such as sputtering, pulsed-laser deposition (PLD) and metal-organic chemical vapour deposition (MOCVD), yield the best performing devices. Despite the extraordinary performance, however, vacuum methods suffer from high manufacturing cost and their incompatibility with large area deposition. In order to overcome this technology bottleneck recent research has been directed to alternative deposition methods based on solution processing such as spin casting, dip coating and spray pyrolysis (SP).

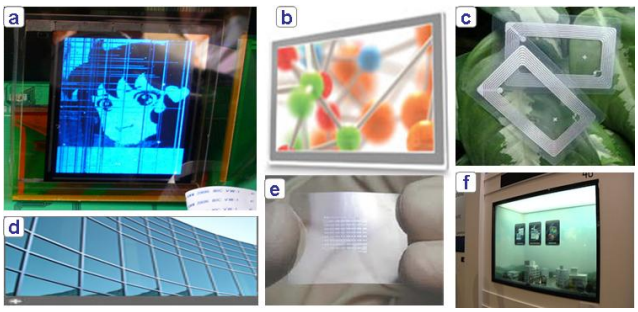

Figure1.2: Examples of transparent electronics: a) an OLED display driven by ZnO based TFTs (15). b) TOs promise to make flat-panel displays faster and sharper than today's silicon standby (16). c) Transparent radio-frequency ID (RFID) tags (17). d) Transparent oxides can be used in energy efficient windows (18). e) Low temperature processability makes transparent oxides fabrication compatible with flexible substrates (19). f) Prototype by Samsung of a see-through flat-panel screen intended to be used as high-tech windows (20).

Solution processing offers a number of advantages that are well known from the area of organic electronics with the most important being the prospect of easy deposition on large-area substrates. In most cases, however, control over the morphology of solution-processed films is difficult, and typically leads to low device yield and hence increased manufacturing cost. Therefore, the promise of solution processed oxide devices as an enabling technology is only likely to be realized when a combination of simple processing and high performance can be achieved. It was the aim of this work to develop and evaluate high performance oxide devices using simple and large-area compatible fabrication paradigms combined with novel materials and device concepts.

1.3 Thesis overview

In this work we have studied and evaluated the application of an alternative processing technique, namely spray pyrolysis (SP), for the deposition of ZnO films and the fabrication of high mobility electron transporting (n-channel) thin-film transistors and integrated circuits. As soluble precursors we have employed a range of commercially available high purity compounds such as acetates the properties of which will be discussed later in the thesis. Based on these materials optimised deposition procedures have been developed and implemented for device and circuit fabrication. Particular emphasis is placed on the effect of growth temperature on the optical and electronic properties of the as-grown ZnO films. A further

interesting development has been the utilisation of molecular self-assembled nano-dielectrics in combination with spray pyrolysis technique for the fabrication of low-voltage, low-power thin-film transistors and logic circuits such as NOT gates.

A further important achievement is the development of organic-inorganic hybrid heterostructures and the demonstration of high mobility, air-stable hole-transporting, electron-transporting as well as ambipolar thin-film transistors and NOT gates based on the much sought complementary circuitry. The latter work has been motivated by the distinct lack of p-type oxide semiconductors with comparable performance characteristics to those obtained from their n-type relatives. To overcome this problem we have employed solution processible phase-separated organic blends, as the p-type films, in combination with ZnO as the n-type layers integrated in a dual-gate device architecture utilising a common set of source-drain electrodes. The stability and reliability of these devices and circuits has also been evaluated.

Optimised ZnO TFTs have also been used to study the electron transport characteristics at the dielectric/ZnO interface of these devices and their dependence on important device processing parameters such as ZnO growth temperature. It is established that as-deposited films are polycrystalline and contain a large number of defects which act as electron traps. Measurements of the transistor transport characteristics as a function of temperature have also been utilised to study the different charge transport regimes in optimised ZnO TFTs. Finally the issue of device stability against bias and time is also addressed.

The thesis is divided into nine chapters. Chapter 2 provides an overview of the current status of oxide based semiconductors and electronics. Chapter 3 reviews the relevant theories underlying the electronic transport in oxide semiconducting materials and transistors. Chapter 4 reviews the experimental procedures and techniques used throughout this thesis for the manufacturing and study of the ZnO films and the various devices. Chapter 5 presents the results obtained from ZnO transistors manufactured at different substrate temperatures utilising three different dielectrics. Chapter 6 discussed the fabrication and characterisation of a novel type of hybrid TFTs based on organic-inorganic semiconducting heterostructures and their utilisation in high performance integrated complementary logic circuits. Chapter 7 examines the charge transport characteristics of ZnO TFTs with

particular emphasis on the effect of charge trapping. Chapter 8 reports on the ambient and operating stability of ZnO transistors under bias-stress and storage in ambient for a prolonged period of time. Lastly, Chapter 9 summarises the main conclusions of this work and some suggestions for future research direction in the area of oxide electronics.

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Chapter 2

Current status of transparent oxide based electronics

Abstract

Thin-film transistors (TFTs) based on metal oxide semiconductors are currently being studied as potential alternatives to silicon based technologies for electronic applications where low-cost, mechanical flexibility, large-area processing and optical transparency are required. Despite their relatively brief history, the charge carrier mobilities of state-of-the-art ZnO TFTs now exceeds those obtained from mainstream technologies such as hydrogenated amorphous silicon (a-Si:H) transistors, making metal oxide semiconductor technology a strong candidate for a whole host of future electronic applications. This chapter reviews the recent progress in the field of oxide semiconductor electronics with particular emphasis on materials and TFT performance.

2.1 Introduction

In recent years transparent electronics have emerged as one of the most promising technologies for a host of opto-electronic applications (1). The key constituents of this technology are wide band gap materials comprised primarily of binary, ternary and quaternary metal oxides systems. This family of materials can be utilised for both passive components (conductors, optical filters, insulators etc) as well as active components (i.e. semiconductors). Importantly, the electronic properties of metal oxide semiconductors are similar to those of conventional electroactive materials such as silicon. However, due to their wide band gap (>3 eV), metal oxides exhibit two normally mutually exclusive properties typically absent in traditional semiconductors such as Si, namely optical transparency and high electrical conductivity (2). This unique combination of physical properties makes metal oxide material systems very promising candidates for a host of future optoelectronic applications.

Although transparent metal oxides are some of the earliest investigated semiconducting materials, they could not be exploited to their full potential owing to a lack of recognised processing techniques and basic knowledge in the first three quarters of the past century. However, during the last three decades a range of growth methods suitable for the production of high quality oxides have been developed. This has triggered significant volume of research focussing on the development and application of a range of transparent oxide conductors and semiconductors (e.g. ZnO, SnO_2 and In_2O_3) (3-7). Many of these compounds have already been employed successfully in a range of applications, mainly as passive components e.g., transparent electrodes (Figure 2.1) for liquid crystal displays (LCDs), organic light emitting diodes (OLED), solar cells and optical detectors among others. In addition to optical transparency and conductivity, transparent oxides can also be synthesised using a variety of chemical elements, enabling the fabrication of a wide range of materials with diverse electronic/crystal structures, and in turn making them particularly attractive for use in a diverse range of applications beyond simple passive components (8).

Following the recent demonstration of the first transparent oxide based thin-film transistor (TTFT) in 2003, recent research has been focussing on the development and exploration of improved transparent oxide semiconductors based

primarily on ZnO. Some successful examples include zinc tin oxide (ZTO), zinc indium oxide (ZIO), and indium gallium zinc oxide (IGZO).

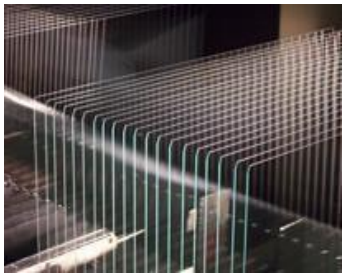


Figure 2.1: Glass substrates coated with a conductive layer of indium tin oxide (9).

These materials have successfully been used as active components in a range of semiconducting devices and electronic circuits (10-15). Although research focusing on ZnO dates back many decades, the interest has been renewed due to the availability of high quality materials, novel deposition methods and above all the appearance of the so-called "killer applications" requiring high carrier mobilities and alternative low temperature processing paradigms (16-19). These characteristics have qualified transparent oxides as ideal candidates for application in future ubiquitous electronics (e.g. flexible optical displays). Figure 2.2 shows a display prototype based on oxide TFT switching backplane. For this particular application, oxide TFTs offer a better ability to drive electrical current and improve the lifetime and stability of the driving electronics used in organic light-emitting diode (OLED) displays.

Figure 2.2: Organic light-emitting diode (OLED) display based on mixed oxide TFTs developed by Arizona State University (20).

2.2 Review of prior work

Over the past five years countless examples of TTFTs based on a range of oxide semiconductors have been reported in the literature. The primary focus of these studies has been the enhancement of the electronic properties in these oxide semiconductors and in particular the charge carrier mobility. Not surprisingly, this effort led to the development of materials and devices with properties tailored to specific technological applications with unusual requirements. The same activity has also led to the development of alternative processing methodologies that unlike conventional deposition techniques (sputtering etc), are compatible with large-area processing and hence low cost manufacturing. This section reviews some of the most relevant work that has enabled the impressive developments we see today in the field of oxide electronics.

In 2003, the groups of Masuda et al, Hoffman et al, and Carcia et al independently reported on the fabrication of ZnO TFTs manufactured using vacuum based deposition techniques (10-12). Some representative data reported in these papers are shown in Figure 2.3. These early devices were fabricated using bottom-gate staggered device architecture, utilising Si wafers and glass as the substrates. The transistors exhibited good operating characteristics with electron mobilities over 2 cm^2/Vs and current on-off ratios exceeding 10^6. The most intriguing aspect of this early work was the demonstration of an alternative low-temperature processing TFT technology compatible with low-cost flexible substrates. In the same year Nishii et al. were able to demonstrate improved ZnO TFT processed below 150 °C using PLD (21). Soon after several other articles reporting ZnO TTFTs were published. Some examples include the work by Nomura et al, which reported the fabrication of a single crystal TTFT with very high electron mobility of ~80 cm^2/Vs (13). Unlike the ZnO TTFTs reported previously, the device structure used here was coplanar with a top-gate employing an $InGaO_3(ZnO)_5$ channel layer grown at 600 °C by PLD. The performance characteristics of these TTFTs were excellent, including an optical transmittance of >80%, enhancement-mode operation with V_T ~ 3 V, channel current on-off ratio of ~10^6 and negligible photo response. This superior performance was attributed to the high quality of the mixed oxide layer hence demonstrating the enormous potential of the metal oxide technology for TFT applications.

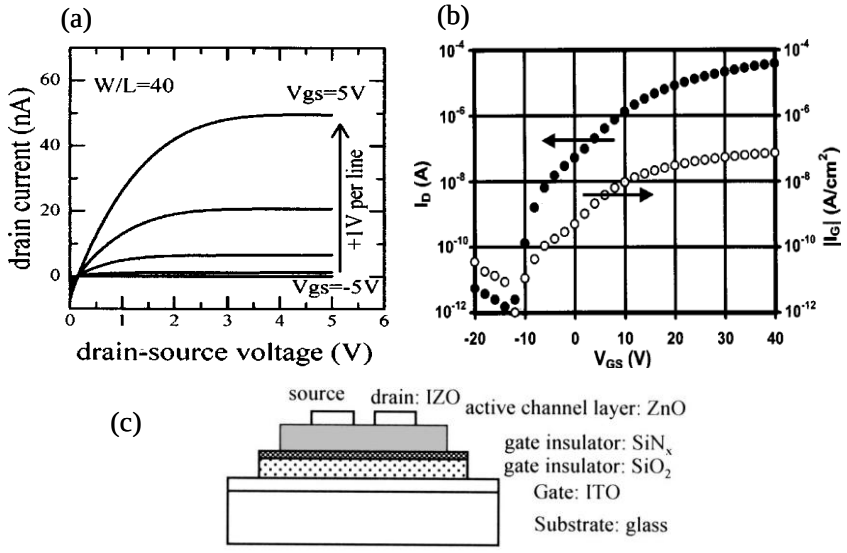


Figure 2.3: (a) Output electrical characteristics of a ZnO TFT with a double layer gate insulator employed by Masuda et al. Mobility achieved is 0.031 cm^2/Vs.(12) (b) Transfer and gate leakage characteristics of a completely transparent ZnO TFT reported by Hoffmann and the group (11). He used ITO for gate and source drain electrodes while ATO was employed as an insulator. (c) Device architecture employed by Masuda et al.

The work by Hoffman et al., in 2004 (22) is also of great significance for the history of transparent electronics, as it was the first to demonstrate the applicability of existing theoretical models that in turn has allowed parameter extraction through experimental TFTs measurements. One of these parameters is the so-called average carrier mobility (μ_{AVE}), or measured mobility, which corresponds to the mobility of all charge carriers in the conducting channel. This represents the most important figure-of-merit for both materials and device evaluation (23).

In the same year (i.e. 2004) Fortunato et al., reported the first ZnO TFT fabricated entirely at room temperature using RF magnetron sputtering for the deposition of all device components (24). In the latter work, indium tin oxide (ITO) was used as a bottom-gate electrode combined with silicon oxynitride as the gate dielectric. The reported performance of these transparent ZnO TTFTs was very promising and exhibited an average optical transmission of ~84%, n-channel enhancement mode operation with a threshold voltage V_T of ~ 1.8 V, an electron mobility of 70 cm^2/Vs, a sub-threshold voltage swing of 0.68 V/decade, and a current on-off ratio of 10^5. The key experimental condition that enabled the

development of such high performance devices was the use of oxygen-free deposition conditions, with the aim of avoiding defects at channel-insulator interface. Minimising such defects was found to be necessary for the growth of transparent low carrier concentration ZnO films. Worth noticing however, is that in their subsequent publications a lower mobility on the order of ~20 cm^2/Vs was reported for the same device configuration (6, 25). The reason for this discrepancy is not known.

Also in 2004, Nomura et al., were the first to demonstrate a novel amorphous mixed oxide semiconductor (i.e. a-InGaZnO) suitable for use in TFTs (26). In their paper they demonstrated a-InGaZnO based TFTs on plastic (i.e. polyethylene terephthalate - PET) substrates fabricated at room temperature. The devices were found to exhibit electron mobility in the range 6-9 cm^2/Vs and offered excellent mechanical stability. Furthermore, the transistors were found to be electrically stable for temperatures up to 120°C. Since then a large number of papers reporting on TFTs based on amorphous mixed oxide semiconducting systems have been published.

Based on their earlier work (10) Carcia et al., also reported on low temperature processed ZnO thin-films fabricated on flexible kapton substrates (27). Devices were constructed using Al as the source, drain and gate electrodes, and utilising a sputtered ZnO layer as the semiconductor and an electron beam evaporated Al_2O_3 layer as the gate dielectric. Importantly, the entire device fabrication was performed at room temperature. The transistors exhibited high electron mobility on the order of ~50 cm^2/Vs. This work provided further evidence of the potential of oxide semiconductors for application in flexible electronics where low-temperature processing is a prerequisite.

In 2006 Hoffman et al., investigated how the oxide stoichiometry and processing temperature influence the performance of mixed oxides such as zinc tin oxide (ZTO) based TFTs (28). The main highlight of this work was the effect of a post deposition annealing step (400-600 °C) on the intermediate cation concentrations (i.e. $Zn/(Zn+Sn) \approx 0.3$-0.7) in the ZTO layers and its relevance to TFT applications since optimised films resulted in a high carrier mobility (25-30 cm^2/Vs). Some findings of this work are represented in Figure 2.4.

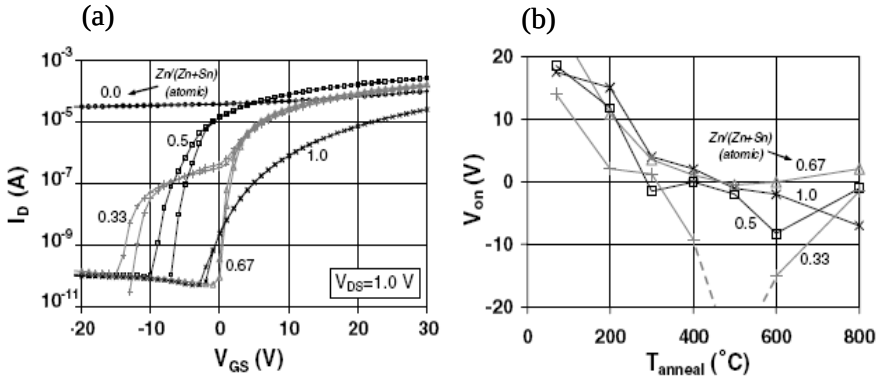


Figure 2.4: (a) Transfer curves for zinc tin oxide channel TFT structures with varying Zn:Sn ratio (as per sputter target composition) and with a 600 °C post-deposition anneal. Stoichiometry is quantified as the atomic ratio of Zn to total metals (Zn + Sn), depicted in the graph. (b) Turn-on voltage (Von) is plotted against channel anneal temperature (Tanneal), corresponding to Zn/(Zn + Sn) (atomic). It is reported that the dotted lines between 400 and 600 °C, for the Zn/(Zn + Sn) = 0.33 curve, indicate a device that could not be turned off within the applied V_G range (28).

Relevant theoretical work was carried out by Hossain et al., who performed the first two-dimensional device simulations of ZnO TFTs assuming a polycrystalline ZnO layer (29). The model asserts that the polycrystalline ZnO layer possesses three properties which can be held responsible for the measured TFT characteristics. These are: (i) the grain size, (ii) the electron concentration within each grain, and (iii) the density of grain boundary traps. It was concluded that low temperature grown ZnO films are characterised by dense grains that result in degradation of the carrier mobility due to the presence of energy barriers and electron traps associated with grain boundaries. In later publications it was confirmed that the electron mobility in polycrystalline ZnO TFTs does indeed depend on the average size of the crystallites comprising the ZnO films (18, 30-32).

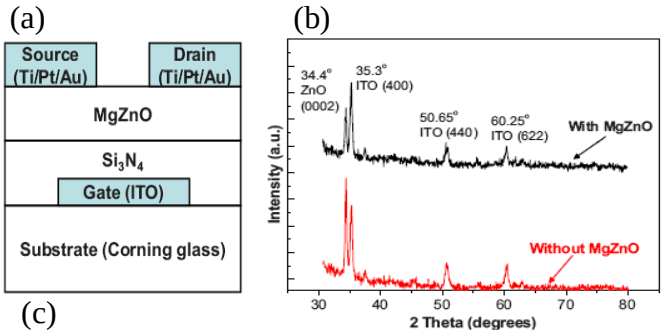
To date, sputtering is the most widely used deposition method due mainly to its relative simplicity and ability to produce high quality ZnO films. One of the main disadvantages however is the limited controllability over the deposited film elemental composition. Although the latter characteristic does not represent a serious issue for the growth of basic oxides such as ZnO, it is a significant problem when considering the growth of complex mixed oxides such as a-InGaZnO, particularly when considering large area substrates. One way of circumventing this problem is through the use of alternative deposition techniques such as metal

organic chemical vapour deposition (MOCVD) (33). The method offers the advantage of high controllability over film elemental composition, along with deposition of uniform high quality films over large areas and good prospects for processing scalability. In a recent paper Remashen et al. (32) demonstrated high mobility TFTs based on films of ZnO grown by MOCVD. The bottom-gated TFTs were built on glass using ITO as the gate electrode. For the source and drain electrodes, metallic layers comprised of Ti/Pt/Au were employed. One significant development reported in this work was the insertion of a 5 nm thick MgZnO interlayer [Figure 2.5(a)] between ZnO and insulator (i.e. Si_3N_4). The incorporation of this thin interlayer was found to enhance the electrical characteristics of ZnO TFTs as compared to control samples fabricated without the interlayer, as shown in Figure 2.5(c). The findings were attributed to the increased ZnO grain size upon insertion of the interlayer. The latter assumption was confirmed by AFM measurements. The interlayer was found not only to improve the electron mobility of the TFTs (9 cm^2/Vs), but also the on-off ratio (10^8) as well as the subthreshold swing and the distribution of trap states when compared to TFTs without the MgZnO interlayer [see Figure 2.5(c)].

It is now established that the nature of the gate dielectric determines, to a large extent, the operating characteristics of a TFT. One could therefore assume that the device performance could in principle be improved through modification of the gate dielectric. The idea was pursued by Kim et al., Lee et al., and Wang et al., in 2006 when they explored the use of alternative dielectric materials with the primary objective of improving the transistor performance (34-36). Kim et al. used $Bi_{1.5}Zn_{1.0}Nb_{1.5}O_7$, with a relative dielectric constant $\varepsilon_r \sim 55$ (at 1 kHz) as the gate dielectric in ZnO TFTs. Unfortunately the only improvement achieved at the time was the lowering of the operating voltage since the electron mobility was found to be low (<1 cm^2/Vs) (34). In a similar effort, Lee et al. investigated the use of a polymer/high-k oxide double layer gate insulator comprising a solution processed poly-4-vinylphenol layer and a mixed SiO_2/CeO_2 (65/35 %) oxide layer with a combined $\varepsilon_r \sim 9.8$. This hybrid gate dielectric led to improved TFT performance as compared to control devices based on polymer only dielectrics.

More recently Wang et al. were able to demonstrate In_2O_3 TFTs with excellent performance characteristics including electron mobilities >120 cm^2/Vs, V_T of ~ 0 V, subthreshold swings of 90 mV/decade, and current on-off ratios of

~10^5 when solution processed self-assembled monolayer (SAM) gate dielectrics were employed (36).



(c)

Comparison of device parameters of the ZnO TFTs without and with the MgZnO layer.

TFTs	μ(sat) cm²/Vs	SS (V/dec)	On-off ratio	VON (V)
Without MgZnO	2.3	0.78	$6.4x10^7$	-6.75
With MgZnO	9.1	0.38	$2.3x10^8$	-2.75

Figure 2.5: (a) Schematic of bottom gated ZnO TFT fabricated by MOCVD by Remashen and group. (32) (b) XRD spectra of ZnO films grown with and without a MgZnO layer. (c) Effect of MgZnO interlayer on electrical performance of ZnO TFT is tabulated. An improvement is observed with MgZnO insertion.

These devices however show high gate leakage currents as evident from non-zero drain current measured at low drain voltage in the output characteristics. On the contrary, the SAM-based ZnO TFTs reported in this thesis (see Chapter 5) show very low leakage currents and V_T of ~ 0 V, although the electron mobility is not as high as 120 cm^2/Vs reported by Wang and group (36). To date a range of oxide dielectrics suitable for use in ZnO TFTs have been demonstrated including; HfO_2, Al_2O_3, SiN, SiO_2, Gd_2O_3, MgO, La_2O_3 as well as a several organic polymeric compounds (19, 32, 37-42). From the work on dielectrics to date it appears that the optimum material combination depends not only on the individual materials used, but also on the nature of the dielectric-semiconductor interface and the deposition methods employed.

In addition to discrete oxide based TFTs a range of integrated circuits based on metal oxide semiconductors have also been demonstrated. Recently, Mourey et al., have reported the fabrication of high mobility ZnO TFTs and fast

integrated circuits (43, 44). The devices were fabricated on glass using Al_2O_3 as the gate insulator and ZnO as the active layer deposited by plasma enhanced atomic layer deposition (PEALD). Discrete devices showed very promising characteristics with electron mobility ~20 cm^2/Vs and current on-off current ratio $>10^9$. The key technological development that enabled the demonstration of such high performance circuits [Figure 2.6(a)] was the use of a backside exposure protocol (taking advantage of the transparency of the oxide semiconductor) which enabled the fabrication of transistors and circuits with self-aligned gate architecture (44). The latter resulted in reduced parasitic capacitance and a significant reduction in the propagation delay (i.e. switching speed) to <10 ns/stage for L = 2.8 μm based transistors. The latter work demonstrated for the first time the potential of oxide microelectronics for applications requiring operating speed >1 MHz.

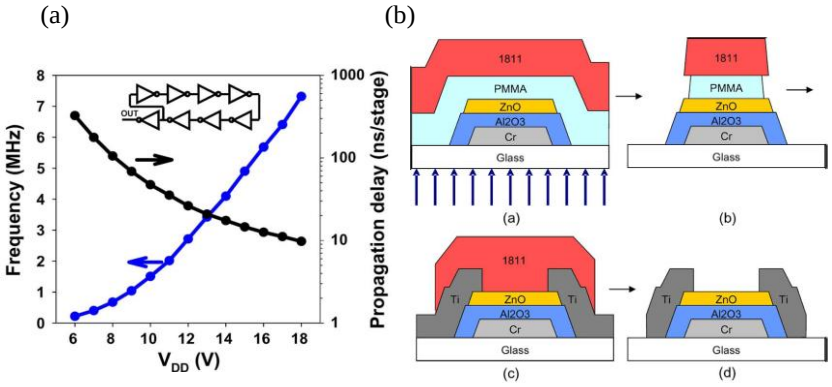


Figure 2.6: (a) Frequency and propagation delay as a function of the supply voltage reaching a minimum propagation delay < 10 ns/stage, obtained from ZnO TFTs fabricated by plasma enhanced atomic layer deposition by Mourey (44). (b) Backside exposure process used to fabricate gate-self-aligned TFTs.

Recently our group at Imperial College has reported the fabrication of high performance oxide TFTs where both the oxide semiconductor and an oxide high-k dielectric (ZrO_2) were processed by spray pyrolysis in ambient air (45). Using this simple deposition technique facile chemical doping of the ZnO with Lithium (Li) has also been achieved through physical blending of two parent precursor solutions. Li-ZnO devices were found to exhibit electron mobility over 85 cm^2/Vs and on-off ratio around 10^6. Because of the high-k characteristics of the ZrO_2 dielectric operating voltages under 6 V were also achieved. Using the same

methodology, Adamopoulos et al., have successfully extended this early work to other dielectric systems including Y_2O_3 and Al_2O_3 and implemented these into low operating voltage ZnO TFTs (46). The devices exhibit excellent characteristics with no hysteresis and mobilities up to 34 cm^2/Vs. This work illustrates the flexibility that oxide materials offer, whilst also demonstrating a significant step towards the development of low-cost, large-area oxide electronics.

It is now widely acknowledged that the ability to grow oxides through solution processing routes expands the possibilities for low-cost transparent oxide electronics, while at the same time enables the rapid synthesis of new materials that are difficult to obtain through conventional deposition techniques. The interest in solution processed oxides was initiated by the first demonstration of solution grown oxide ZnO based TFTs in 2003 by Norris et al. (47). In this work ZnO films was formed via spin coating using a zinc nitrate precursor solution that was converted to ZnO by baking in air at 600°C, followed by a 700°C rapid thermal annealing step in oxygen. The performance characteristics of these early transistors were rather poor when compared to earlier reported data for TFTs grown by vacuum based methods. Despite this the work attracted a great deal of attention from various research groups working on solution processable oxide materials. More recently, Redinger and Li employed chemical bath deposition and drop casting respectively, and were able to demonstrate TFTs with electron mobilities >3 cm^2/Vs (48, 49). Based on this early work in the area of solution processed oxides, our group at Imperial College has recently demonstrated for the first time the applicability of an alternative processing method, namely spray pyrolysis, for the growth of high quality films of ZnO suitable for transistor applications (50). The development and adaptation of this technique to the area of oxide microelectronics is at the heart of this thesis and will be discussed in later chapters.

Despite the impressive progress that has been achieved in recent years in the area of n-type oxide semiconductors, the synthesis and demonstration of p-type oxide materials and devices with comparable performance characteristics have yet to be realised. This distinct lack of p-type oxides represents a serious technology bottleneck as the majority of modern electronic applications demand the use of both p and n-type semiconductors. Attempts to produce p-type ZnO have usually involved doping with Group I and V elements (51). Despite a great deal of research, the production of p-type compounds has been difficult, with most

materials exhibiting poor performance or no field-effect characteristics. In order to circumvent this lack of p-type oxide semiconductors, recent attempts have been made to combine n-type oxide semiconductors with p-type organic semiconductors in a bilayer configuration (52). In particular, Nakanotani et al. reported high-performance ambipolar TFTs based on an organic–inorganic hybrid structure (Figure 2.7) containing IZO as the n-type layer and pentacene as the p-type layer. This heterostructure was found to exhibit ambipolar transistor characteristics (52) with hole and electron mobilityies of 0.14 and 13.8 cm^2/Vs respectively. An IZO film was deposited by RF magnetron sputtering at room temperature followed by annealing step at 300°C, whilst the pentacene layer was thermally evaporated under high vacuum.

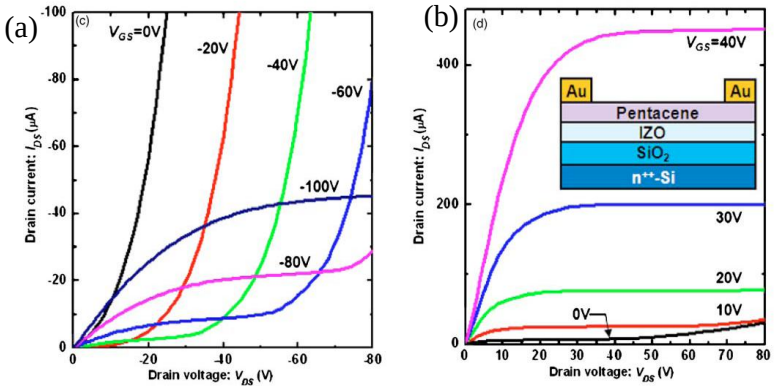


Figure 2.7: Ouput characteristics of Indium zinc oxide IZO/Pentacene heterostructure based transistor. (a) and (b) represent p-type and n-type operations respectively. Inset is a schematic of a transistor with a bilayer based on organic-inorganic heterostructure. The work was reported by Nakanotani et al. (52).

The same approach was adopted by different groups focussing on balanced electron and hole mobility devices. Recently, Yang et al., have investigated the effect of a dodecanoic acid (DA) self-assembled monolayer (SAM) inserted between the pentacene and ZnO layer grown by atomic layer deposition (ALD) (53). The SAM layer was found to improve the morphology of the evaporated pentacene resulting in a well-balanced ambipolar charge transport with hole and electron mobilities of 0.34 and 0.38 cm^2/Vs respectively.

From this short introduction it is clear that despite the great deal of research carried out over the past 10 years, there are still many questions and

technology bottlenecks that would need to be addressed before full scale commercial exploitation of the oxide semiconductor technology becomes a reality. A number of these questions are fundamental in their nature and relate to the transport physics in crystalline, and also polycrystalline oxide materials and devices. For example, the effects of sub-gap density of states on the transistor characteristics, bias instability, the defect physics is virtually unknown. In this thesis we try to address some of these key questions, while at the same time provide practical solutions to technological bottlenecks, such as the absence of p-type oxide semiconductors and the inability to produe high performance circuits based on key technologies such as complementary logic architectures.

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Chapter 3

Theoretical Background

Abstract

Transparent oxide materials have emerged as promising materials for applications in a host of optoelectronic and microelectronic applications. This chapter reviews the basic material properties including the energy band structure, charge transport mechanisms and the various device applications and particularly thin-film transistors and integrated circuits. Device related effects such as parasitic contact resistance and charge trapping are also discussed.

3.1 Electronic properties of transparent oxide semiconductors (TOS): introduction

The electronic structure of transparent oxide semiconductors (TOS) varies greatly from conventional inorganic semiconductors, but does not render altogether a different behaviour on a macroscopic scale (1). This characteristic allows already developed charge transport models to be employed in TOS if necessary modifications are done, but only a few studies are available as developments in TOS are still underway. Basic carrier transport properties in crystals are often discussed based on band theory whereby electrons and holes experience phonon scattering while moving in delocalised bands.

TOS can be regarded as a disordered system due to inherent defects, which give rise to localised states in the system (2). It gives rise to another conduction mechanism in which the charge carrier transport is via hopping from one localised state to the other with the help of phonons (3). But these conduction mechanisms cannot be accounted for using a single model (4), as is the case for other disordered systems. The polycrystalline nature of TOS induces grain boundary limited transport which fortunately can be well described using the models devised for poly Si (5). This chapter will give an idea of how the electronic structures of TOS are different from other inorganic semiconductors as well as how carriers are generated and how the existing models can help in understanding their various charge transport characteristics.

3.2 Electronic structure and carrier generation

For understanding conduction pathways in n type TOS, e.g. ZnO, In_2O_3, SnO_2 which share similar chemical and electronic properties, one has to be able to comprehend the origin of electronic band structure in these materials. The electronic structure of oxides varies significantly not only from organic but also from their inorganic counterparts. In covalent materials such as Si, for example, out of sp^3 hybridized orbitals the anti bonded states (sp^3 σ^*) make up the conduction band minimum (CBM) while the valence band maximum (VBM) results from bonded states (sp^3 σ). The band gap is formed by the energy splitting of the σ–σ^* levels [Figure 3.1(a)] (6). In many oxides, metal (M) atoms and oxygen (O) atoms, when brought closer, are ionized due to charge transfer [Figure 3.1 (b)]. This occurs due to large differences in electron affinity and ionization

potential of the two species. Consequently the ionized states in the crystal are stabilized by the Madelung potential [Figure 3.1(c)]. In ideal stoichiometric materials the bonding and nonbonding O 2p states form the valence band while the conduction band arises from the antibonding Ms–Op interaction states (1, 6).

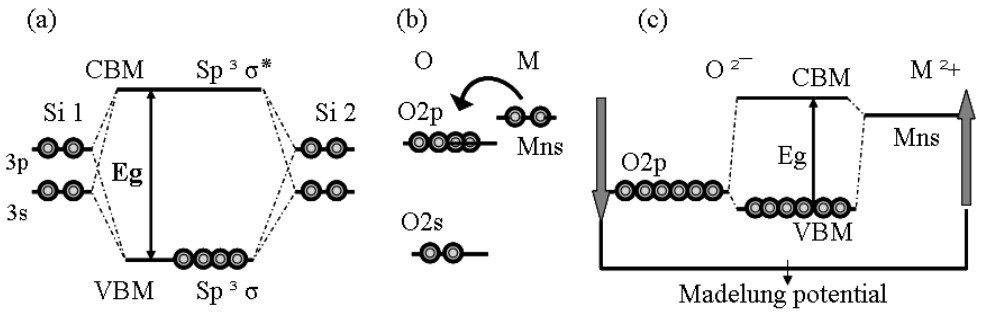

Figure 3.1: Energy gap formation in (a) covalent semiconductor, Si and (b) energy levels of metal and oxygen neutral atoms in vacuum, (c) large band gap arises from large Madelung potential due to ionized atoms. Courtesy of (1)

The Ms-Op overlap determines the energy dispersion of the CB, in TOS materials. It is worth noting that this overlap is minimal at CBM and once away from this point it becomes greater thereby rendering a parabolic shape to the CB, as indicated in the density of states plot in Figure 3.2. Uniquely, the dispersion with a spherical symmetry in the heavy metal cations (Zn, In, Sn) is much larger than that in light metal cations such as Al, leading to a wider CB (7). The high dispersion of the band contributes to a small electron effective mass (8, 9) and a high mobility, which differ from light metal oxides such as MgO and Al_2O_3 which are typical insulators (7).

Moreover, the large orbital of metal extended states do not vary under local structural distortions or bond stretching in the M-O-M bonds; in other words the mobility of TOS remains less sensitive, or immune, to the structural disorder because of such ionic bonding (1, 7). The latter is another feature differentiating oxides from Si in which charge transport is hindered via carriers being trapped at localised states created due to distortions in its chemical bonds.

The origin of electrons in unintentionally doped TOS is far from clear. However native defects are considered responsible for carrier generation and hence

positioning of the Fermi level E_F near or within CB, in case of n-type conduction (8). Such defects include oxygen vacancies (V_O), metal vacancies, interstitial sites occupied by metals I_M, and in some cases hydrogen (2, 10). How these defects contribute to carrier concentration is discussed briefly next.

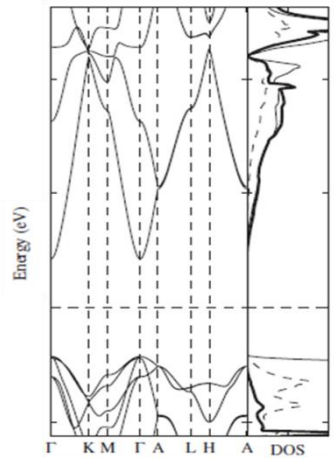

Figure 3.2: Electronic band structure showing VB separated from CB and density of states DOS for undoped wurtzite ZnO. The thick, dashed, and the thin lines in DOS plots represent the metal s, metal p, and oxygen p states respectively (11).

Upon removal of an O atom from the crystal left behind are two electrons; one or both of them become free or remain localised at the vacancy site depending upon the oxide free energy of formation. In conventional TOS the low formation energy produces large O deficiencies even under equilibrium conditions (12, 13). Free carriers densities can thus be adjusted between 10^{17}–10^{20} cm^{-3}, for ZnO and In_2O_3 (8, 14). Electronic structure studies of reduced oxides have predicted that the neutral oxygen vacancy, V^0_O functions as a deep level (15). Only when the vacancy is excited i.e. $V^0_O \rightarrow V^+_O + e$ and $V^+_O \rightarrow V^{2+}_O + e$, does it contribute to the observed conducting nature of the material through electron population of the conduction band (16).

ZnO has often been characterised by a significant V_O concentration; Zn interstitial defect has formation energy too high to let it occur spontaneously on its own, though could contribute significantly to conductivity upon sufficient concentration. Hydrogen has also been found to be a strong contender for donating carriers but high carrier concentration has still been observed in samples with minimal amount of hydrogen (10, 12, 17). It is only recently that defect interactions

have been theoretically, shown to be necessary for contributing to high carrier concentration (18). This is due to the strong attractive interaction between deep donor V_O and shallow donor I_{Zn} driven by the quantum mechanical hybridization of the two states. This interaction lowers the system's total energy by lowering the energy of the electronic orbital of V_O, as the distance between the two defects decreases. The latter leads to an increase in I_{Zn} concentration to a high enough value that can produce high carrier concentration in O deficient ZnO, even when E_F is close to CB.

Lastly, high carrier density achieved either by external doping or by reduction leads to perturbation in the electron energy bands of TOS which results in a blue shift in the high-energy absorption edge known as the Burstein–Moss effect. For example, when ZnO is doped n-type by introducing gallium into the structure, defect levels are introduced near the bottom of the conduction band thereby leading to an increase in the bandgap energy (19).

3.3 Conduction pathways and characterising models

Electrical conductivity in polycrystalline TOS can proceed through variety of mechanisms. Intrinsic defects together with extrinsic impurities give rise to impurity conduction phenomenon at low temperature and band conduction near and above room temperature (20).

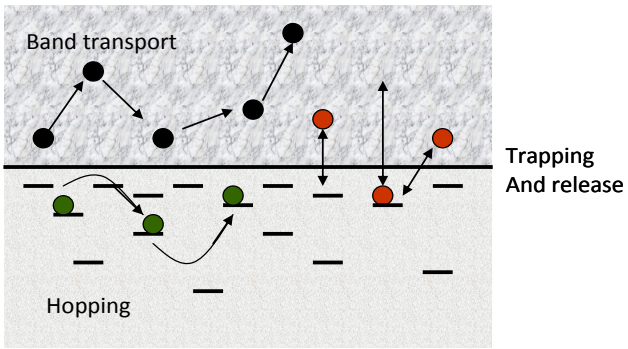

Figure3.3: Energy levels in a disordered semiconductor. This schematic diagram illustrates the band transport, trapping and release of the carriers as well as hopping conduction between localised states.

A schematic of these mechanisms is shown in Figure3.3. In addition, the grain boundaries act as charge carrier traps and therefore affecting electrical

conduction through band bending and potential barriers around grains (21). Moreover scattering of carriers at ionised impurities has also been found to be inevitable for these materials (22). For TOS like ZnO, ITO, and SnO, these mechanisms are found in different temperature regimes as well as under various carrier concentrations (5, 23). The following sections provide a short introduction on mechanisms and the respective models employed.

3.3.1 Band like charge transport

Like other inorganic systems, in TOS too at finite temperature the carriers are present in CB, which are ready to be transported once any stimulus is present. Mobility of the carriers, μ, has been determined to vary with absolute temperature T as $\mu \propto T^{-3/2}$ due to lattice vibration scattering (24, 25). But due to degeneracy present in majority of TOS, the incorporation of a Fermi-Dirac distribution has given an inverse temperature dependence i.e. $\mu \propto T^{-1}$ (22). The latter is a characteristic of band like transport in many TOS.

3.3.2 Hopping transport and simple model

Carriers can be activated to an energy above which they can be transported by hopping. Hopping occurs in the vicinity of the Fermi level which requires localized states within kT around the Fermi level. The activation energy is then a typical barrier height separating the localised neighbouring states (26).

It has been found that conduction in many TOS is a combination of band and hopping like transport where the latter is caused by the localised states arising from inherent defects and ionic interactions (27). Therefore many models developed for disordered or organic semiconductors for hopping conduction have equally been applied to TOS and found useful to understand the otherwise complicated charge transport processes in these materials. Following is a brief introduction to some of these models.

In a system where carriers are more or less localized at defect sites, we would expect to observe activation energy behaviour, i.e. an energy barrier that a carrier has to cross when jumping from one site r_i to another r_j. Though a classical electron would remain trapped at r_i, the wavefunctions on the two sites decay exponentially in the barrier and the overlap between them results in a finite

probability P_{ij} of tunnelling. In a common approach to find a simple hopping model, this probability includes not only the spatial separation $|r_i-r_j|$ but the energetic mismatch E_i-E_j of the two sites (28) and is given as

$$P_{ij} \propto \exp\left(-2\frac{|r_i - r_j|}{a_o}\right).\exp\left(-\frac{E_i - E_j}{kT}\right); \qquad E_i-E_j>0 \qquad 3.1$$

where a_o represents the decay of the squared wavefunction in the barrier and is called the localisation length. The Boltzmann factor accounts for the activation energy of charge carrier before tunnelling.

Hopping amongst nearest neighbour defect states, described under nearest-neighbour hopping mechanism (NNH) (27, 29) is observed by the exponential temperature dependence of the mobility given as

$$\mu_{NN} = B.\exp\left[-\left(\frac{E_1 - E_2}{kT}\right)\right]; \qquad E_1-E_2 << kT \qquad 3.2$$

where B is a temperature independent constant. At extremely low temperatures, T $\leq 50\ ^0$K, when both phonons and energy decrease and impurity density is high, the hopping between states that are almost similar or closer in energy (even if they are wider spaced) becomes more preferable than that between the nearest neighbours whose energies differ substantially (30). This mechanism is the so called variable range hopping (VRH) conductivity or Mott's conductivity and is governed by both; 1) the most probable hopping distance which depends upon the overlap of the wave functions and 2) the average hopping energy between initial and final state (26, 30, 31). Mott modified the model considering that VRH is also weakly dependent on the density of localised states around the Fermi energy. The mobility, evaluated in 3-dimensional space, thus arrives at the following expression (rather than an Arrhenius temperature dependence).

$$\mu = \mu_o \exp\left[-\left(\frac{T_o}{T}\right)^{\frac{1}{4}}\right] \qquad 3.3$$

where $kT_o = \dfrac{1}{N(E_F)a_o^3}$ is the average energy level spacing in volume a_o^3 and $N(E_F)$ is the density of states DOS at Fermi energy. The DOS here are chosen to be

constant in the energy range considered. A different DOS would lead to a different temperature dependence as shown by Efros and Shklovskii (ES-VRH), also taking into account the Coulomb interactions between different sites which are ignored in Mott VRH (32). ES-VRH gives mobility the inverse square root temperature dependence i.e. $\mu \propto \exp\left(-\sqrt{\frac{T_o}{T}}\right)$.

Mott VRH is a general feature of disordered systems. An oxide lattice with impurities is one case. More generally this is seen in amorphous materials but is still found appropriate and applicable to polycrystalline TOS such as ZnO.

3.3.3 Charge trapping: Multiple trapping and release model (MTR)

For almost all inorganic semiconductors the localised states which result from structural disorder such as grain boundaries, point defects and external impurities are characterised as trap states, being able to hold the carrier over some period of time depending on trap energy level as well as temperature. Therefore these states require thermal activation to release the carrier to a transport level E_T. E_T is nothing more than a band edge or mobility edge of an inorganic semiconductor i.e. E_c for n type and is defined as the energy level the carrier finds it more likely to escape to (33). The trapping and release of carriers at localized states result in a thermally activated behaviour of the mobility, which also depends on the gate voltage V_G. It is often interpreted in terms of multiple trap and release (MTR) model, devised for Si based electronics (34) but applied to organics too (35). In this model, finding DOS holds the main importance and here it is shown very briefly how to evaluate that.

The MTR model assumes that the charge transport occurs solely in extended states i.e. above E_T but under the influence of trapping and release of the carriers in states below E_T. Another important assumption is that the charge induced by the gate voltage not only lies in the first few monolayers of the semiconductor insulator interface but consists of both trapped σ_t and free charge σ_f, though the former being much greater than the latter, $\sigma_t >> \sigma_f$. The average mobility μ_{AVE} of a thin film transistor TFT, being averaged over all carriers whether free or trapped, will simply be a ratio of free to total charge densities:

$$\mu_{AVE} = \mu_o \frac{\sigma_f}{\sigma_f + \sigma_t} \approx \mu_o \frac{\sigma_f}{\sigma_t}; \qquad \sigma_t >> \sigma_f \qquad 3.4$$

where μ_o is the mobility in perfectly delocalised bands. For a discrete trap, the mobility is lowered due to reduced ratio of free to total charge as majority is captured at trap sites. It also becomes temperature dependent but remains bias independent. The mobility then takes the following form:

$$\mu_{AVE} \approx \mu_o \frac{N_c}{N_t} \exp\left(-\frac{E_A}{kT}\right) \qquad 3.5$$

Where N_c and N_t are the density of states for transporting carriers at band edge and for traps respectively. In this case E_A the activation energy represents how far is the trap level from the transport level. If the traps are distributed over some energy levels then appropriate evaluation of N_t is very important. Due to localised states lying within the bandgap, it seems plausible here to employ the exponential distribution for trap states as (34):

$$N_t(E) = N_t^o \exp\left(-\frac{E_T - E}{kT_o}\right) \qquad 3.6$$

where kT_o accounts for the width of the trap distribution and N_t^o is the total surface density of states. The average mobility is now modified to

$$\mu_{AVE} = \mu_o \frac{N_c}{N_t^o} \exp\left(-\frac{E_A}{kT} + \frac{E_A}{kT_o}\right). \qquad 3.7$$

The activation energy and the mobility are V_G dependent, as observed e.g. in Zinc Tin Oxide TFT (36), since an increase in V_G fills the traps thereby shifting the Fermi level E_F towards the band edge. Keeping this dependence and abundance of traps (distributed in energy) in mind, the expression can be visualised as a general form of the Meyer Neldel rule (MNR) (37-39) with prefactor μ_{oo} increasing exponentially with activation energy as depicted in Equation 3.8.

$$\mu_{oo} \approx \mu_o \exp\left(\frac{E_A}{kT_o}\right). \qquad 3.8$$

MNR is best described by the Meyer Neldel energy kT_o (or trap distribution width) with T_o termed as the isokinetic temperature. T_o is a temperature where bias

dependence of mobility disappears and can be determined from a single crossing point of different activation energies. In other words, it is that point where ln(μ), for various gate voltages, converge when plotted against inverse temperature. Thus average mobility in Equation 3.7 with the prefactor has Arrhenius form i.e.

$$\mu_{AVE} = \mu_{oo} \frac{N_c}{N_t^o} \exp\left(-\frac{E_A}{kT}\right). \qquad 3.9$$

Also, the activation energy measured from Arrhenius plot depends upon the bias in the following way

$$E_A(V_G) = kT_o \ln\left(\frac{q.N_t^o}{C_i(V_G - V_T)}\right) \qquad 3.10$$

where C_i, the geometrical gate capacitance and V_T, threshold voltage are explained in the following sections. It is to be noted that activation energy of mobility depends upon the parameters of trap distribution width and bias, despite revealing the depth of the trap level.

The next step is to find a general form for the DOS for the MTR model, using temperature dependent transistor data. First it is assumed that gate voltage induced charge contributes the most to total charge density and the most voltage drop occurs across the insulator then $\sigma_{TOTAl} = \sigma_{TRAP} = C_i V_G$. Free charge density, σ_f, can be evaluated using well known Boltzmann statistics and is $qN_C\ exp\left[-\left(\frac{E_C - E_F}{kT}\right)\right]$. Inserting these charge densities in Equation 3.4, we arrive at the following expression

$$E_T - E_F = kT \ln\left(\frac{q\mu_o N_c}{\mu_{AVE} C_i V_G}\right). \qquad 3.11$$

In the case of a slowly varying trap distribution, the Fermi distribution can be approximated to a step function and the DOS can be found from the derivative of the trapped charge density with respect to energy given as Equation 3.12:

$$\sigma_t = \int_{-\infty}^{E_F} N_t(E)dE \Rightarrow N_t(E) = \frac{d\sigma_t}{dE}. \qquad 3.12$$

Although the MTR model has successfully been applied to organic and inorganic TFTs (35, 40) but its use in transparent TFTs (41) has been very limited.

The only flaw it carries is its inability to give an account of particularly low temperature dependence of mobility. It is therefore valuable if grain boundaries effect on charge transport is taken into account. It is discussed briefly next.

3.3.4 Grain boundary limited charge transport

In polycrystalline TOS, grain boundary limiting electron transport is one of the most important mechanisms, which is sometimes useful to explain two or more thermally activated processes competing with each other. As far as the grain itself is concerned it offers delocalised charge transport. But grain boundaries due to incomplete atomic bonding and defects are highly disordered regions and that is why they are assumed to contain all the traps. These traps immobilize the charge carriers by trapping them and create a potential barrier which impedes the carrier motion from one grain to other. This is schematically shown in Figure 3.4 (a) with energetically distributed traps at the boundary.

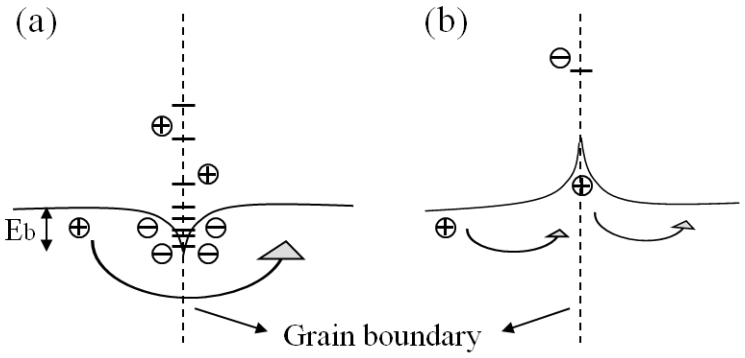

Figure 3.4: (a) Potential well and (b) potential barrier for grain boundary trapping model. Carriers can tunnel as well as cross it depending upon temperature and carrier concentration.

It should be noted that the MTR model is applicable if grain sizes are small compared to the boundary width having spatially uniformly distributed traps. Moreover the potential well model for grain boundary trapping also exists whereby acceptor-like trap states give rise to local band bending, shown in Figure 3.4(b). Seto was the first to study grain boundary effects in poly Si films (42) and his model is still found applicable in other polycrystalline systems. It was modified to include Fermi Dirac statistics in order to be applied to transparent oxides. The average mobility of polycrystalline medium can be written as:

$$\mu^{-1} = \mu_b^{-1} + \mu_g^{-1} \qquad 3.\ 13$$

where μ_b and μ_g stand for mobility in the grain boundary and in the grain, respectively. Both energetic barrier height and width are functions of carrier concentration but the former also varies with gate voltage. For TOS with n ~ 10^{20} cm^{-3}, the barrier width is quite small and the mobility is governed by thermionic carrier jumps across the grain boundaries at high temperatures but tunnelling at low temperatures (22).

3.4 Thin-film transistors

Having described the fundamental physics of charge transport in TOSs, the following sections discuss the operation of thin film transistors (TFTs) and how the field effect mobilities together with some important parameters prerequisites for many TFT applications are extracted.

The concept of the field-effect transistor (FET) dates back to 1930 (43), even earlier than the bipolar junction transistor's invention, and still is a key component of contemporary device technology. The most common and unique design of FET known as the thin-film transistor (TFT) was developed by Weimer in 1962 (44). Since then TFTs based on a wide variety of materials including amorphous and polycrystalline Si have been demonstrated. It is only recently that the development of the transparent oxide based TFT revolutionised research with a new spark of invisible electronics (45). The transparent TFTs used as the driving circuitry in active matrix optical displays have presented the advantage of a higher aperture ratio for the transmission of backlight, unlike Si based TFTs. The latter due to the in opacity blocks the light from part of the pixel and also requires shielding to avoid generation of carriers, from light. The potential for simple, large-area fabrication makes TOS an ideal choice for use in TFTs and therefore research regarding developments and utilization of TOS in TFTs is booming.

3.4.1 Device architecture and fundamental operation

The basic TFT structure consists of a semiconducting active layer i.e. the channel separated from gate (G) electrode by an insulating layer. Voltage applied across the gate, through electrostatic coupling, modulates the current flow between source (S) and drain (D) electrodes. The source and drain, as the names suggest, provide carrier injection into and extraction from the semiconductor respectively.

The operating principles of a TFT are not much different from a typical MOSFET device and as all the induced charge is necessarily close to semiconductor- dielectric interface therefore a typical charge-voltage relation can be applied.

$$Q(x) = (V_G - V(x))C_i \qquad 3.\ 14$$

where Q(x) and V_x are the surface charge density and voltage at any point x in the channel between source and drain [Figure 3.5(a)]. V_G is the gate voltage and C_i represents the dielectric capacitance per unit area.

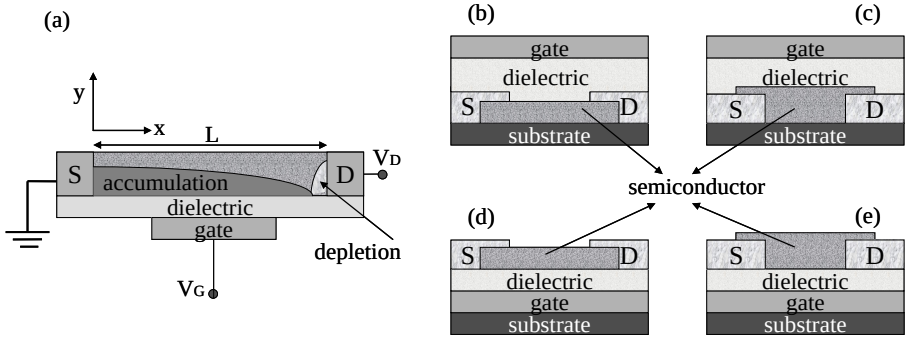

Figure 3.5: (a) Thin film transistor model showing the source (S), drain (D) and gate (G) contacts, dielectric layer and semiconductor with a schematic representation of the charge accumulation and depletion regions. The device is shown in the saturation regime with $V_{DSAT} = V_G - V_T$. Four general TFT configurations, including: (b) coplanar top-gate, (c) staggered top-gate, (d) staggered bottom-gate, and (e) coplanar bottom-gate.

With source grounded, the applied gate voltage V_G develops an electric field at the gate-dielectric interface which accumulates or depletes the semiconductor-dielectric interface of charged carriers. The applied drain voltage V_D drives the carriers through the channel to get drain current I_D. When V_D is close to zero the channel is modelled as a resistor due to the linear variation of I_D with V_D. Further increase in V_D decreases the accumulation in a region close to drain until that region begins to deplete of carriers as shown in Figure 3.5 (a). When the region is fully depleted or in other words pinched off, the respective voltage V_D is termed as the saturation voltage V_{DSAT}. So application of $V_D > V_{DSAT}$ results in no further increase in drain current I_D which then saturates.

There are several possible TFT architectures that can be used as shown in Figure 3.5. Two of them are termed as the coplanar type with either a top gate or bottom gate [Figure 3.5 (b, e)] and the others as the staggered [Figure 3.5 (c, d)] type. These structures are distinguished by the placement of electrodes. In the coplanar structure, electrodes are placed on the same side of semiconductor insulator interface while they are on the opposite side of the interface for staggered structures. The latter configuration results in minimal contact resistance due to large contact area and significant charge accumulation under the contact. Performance of a TFT is highly architecture dependent due to different gate dielectric interfaces and contact configurations. Also process integration related issues can motivate the use of different structures.

3.4.2 Gradual channel approximation model for thin-film transistor

It is relatively easy to show that the equation for currents in a MOSFET is also applicable to the TFT. This section formalizes the basic theory to calculate the drain current I_D in a TFT. It is considered that the charge density varies from one electrode (source, x=0) to the other (drain, x=L), as shown in Figure 3.5(a) while the thickness of the channel remains constant. From principles of elementary theory of electricity, it can be understood that the local current $I_x(x)$ at any point x along the channel length would be a multiple of local induced charge density Q(x), channel width W, mobility and local electric field E(x). Before putting this expression into appropriate form for a TFT, two assumptions are made. 1) Mobility (μ) is constant along the channel so does not vary with either x or V(x) (the voltage at any point x along the channel). 2) The lateral change in electric field E_x is considered to be negligible when compared with its perpendicular component E_y (46). The latter is very well known as the gradual channel approximation and is valid only for long channels and a narrow range of V_D. Now the current at point x in the channel, as mentioned above, is written as:

$$I_x(x) = Q(x)W\mu E_x(x) \qquad 3.\ 15$$

where $E_x(x)$ is the electric field felt by the small element dx in the channel such that $E_x(x)=dV(x)/dx$. Though both gate voltage V_G and V(x) (caused by V_D) can alter the magnitude of Q(x) there also exists an offset that accounts for the flat-band potential, bulk charges present when there is no electric field, and states

acting as traps for injected charges. A single term i.e. the so called threshold voltage V_T comprises all these effects and so modifies Equation (3.14) to;

$$Q(x) = (V_G - V_T - V(x))C_i. \qquad 3.16$$

By knowing the geometric capacitance C_i, surface charge density can be evaluated using Equation (3.16). Current can then be written as;

$$I_x(x) = C_i W \mu [V_G - V_T - V(x)] \frac{dV(x)}{dx}. \qquad 3.17$$

For all x, $I_x(x) = I_D$, which can be evaluated by integrating the above equation along the channel length, L, using the boundary conditions V(0) =0 and V(L) = V_D.

$$\int_0^L dx.I_D = W\mu \int_0^{V_D} C_i [V_G - V_T - V(x)] dV(x) \qquad 3.18$$

Simplification of equation (3.18) results in the following form of I_D.

$$I_D = \frac{W}{L} C_i \mu \left[(V_G - V_T) V_D - \frac{V_D^2}{2} \right]. \qquad 3.19$$

It is to be noted that Equation (3.19) is not valid in the cut off region, i.e. when $V_G < V_T$ or in the saturation regime when $V_D \geq V_G - V_T$. This expression can further quantify the two regions of operations of a TFT, mentioned briefly above. In the linear regime ($V_D << V_G - V_T$) the charge density is uniform along the channel because V_D is so small that I_D varies linearly with it. This condition yields the expression for I_D in linear operating regime, given in Equation 3.20:

$$I_{DLIN} = \frac{W}{L} C_i \mu (V_G - V_T) V_D. \qquad 3.20$$

In the saturation regime ($V_D \geq V_G - V_T$) complete pinching at the region near the drain electrode occurs and I_D becomes independent of V_D. The channel current in saturation can then be obtained using $V_D = V_G - V_T$ in Equation 3.19, as:

$$I_{DSAT} = \frac{W}{2L} C_i \mu [(V_G - V_T)^2] \qquad 3.21$$

These equations 3.19-3.21 are central for the analysis of a TFT and will be used throughout this thesis.

3.4.3 Thin-film transistor operation: parameter calculation

It is common practice to develop 'figures of merit' which allow comparison between different materials, devices, and technologies. Electrical characterization of a TFT device includes the measurement of its transfer and output characteristics which are used to calculate some key device parameters. Transfer characteristics are graphical representation of drain current against gate voltage while output characteristics represent drain current as a function of drain voltage. Figure 3.6 shows an ideal form of these characteristics calculated using Equation 3.19.

Important parameters that can be obtained are (i) threshold voltage V_T, (ii) switch on voltage V_{on}, (iii) ratio of on current to off current (I_{on}/I_{off}), (iv) subthreshold slope/swing SS, and the most important (v) the charge carrier mobility, μ. Following is a brief overview of these key parameters.

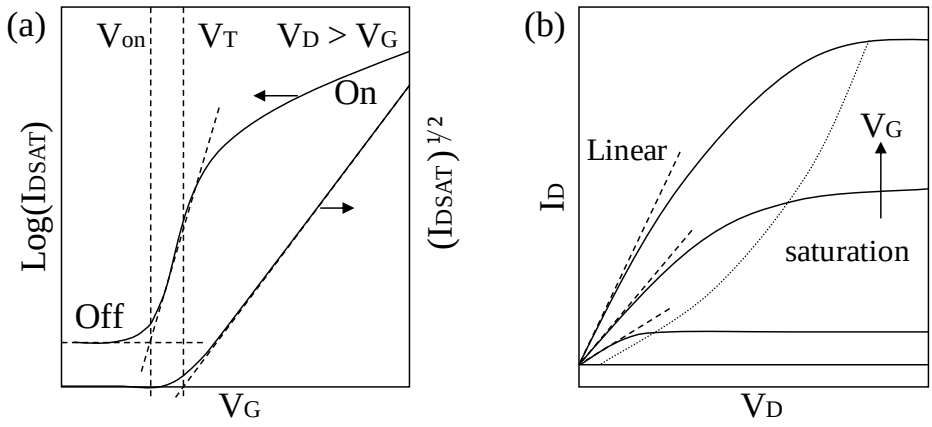

Figure 3.6: (a) The transfer characteristics of an ideal TFT calculated using gradual channel approximation (Equation 3.19). It shows how the V_T and V_{on} can be found out using I_D and square root of I_D. (b) The output characteristics of an ideal device showing linear and saturation regimes for several gate voltages. The output is approximately linear for low V_D but beyond the pinch-off point (indicated by the thin line) the device saturates.

THE THRESHOLD VOLTAGE (V_T)

For a conventional MOSFET, there is a physical meaning for V_T. It is the gate voltage marking the transition between weak inversion and strong inversion. Since there is no such identified mechanism in a TFT, V_{on} is sometimes preferred over V_T. V_{on} is the gate voltage at which conduction in the channel begins to increase

and can easily be determined from the transfer curve where I_D starts to rise exponentially, above the noise floor/leakage current as shown in the Figure 3.6(a).

ON-OFF RATIO (I_{on}/I_{off})

Another performance metric is the I_{on}/I_{off} ratio discussed earlier. The higher the ratio the better is the switching capability of the TFT. The latter can be assessed from the transfer curve with V_G swept through an appropriate voltage range. The off current translates into how much power is lost when the device is off so an extremely low value is desirable. The off current is determined from one or more current leakage mechanisms such as gate dielectric leakage and source-drain leakage. These currents depend upon the size of the device and therefore can be effectively minimised by the channel dimensions and also with efficient patterning of the semiconductor. The on current indicates the maximum current that the device can drive and is determined by the charge carrier mobility and device dimensions.

SUBTHRESHOLD SWING (SS)

In the subthreshold region of operation i.e. below V_T, a TFT is in a switching transition from off to on and I_D changes exponentially from a low off current (10^{-12}–10^{-8} A) to a high on current. For $V_G < V_T$, most of the induced charge goes into deep states in the semiconductor bandgap and semiconductor insulator interface so only a small number of electrons participate in conduction. As V_G increases, a higher density of electrons leads to an exponential increase of current until switch on is achieved. This operating regime is characterised by a subthreshold slope, S, defined as the gate voltage required to increase the drain current by an order of magnitude. Inverse of this slope is termed as the subthreshold swing (SS). The latter can be extracted from the TFT transfer characteristics in subthreshold regime using the following equation:

$$S = \frac{\partial V_G}{\partial(\log_{10} I_D)}. \qquad 3.22$$

A small value of S indicates the speediness of the device in changing between off and on states and how efficiently the conduction channel is formed. It is therefore a very important figure of merit for comparing different TFTs.

MOBILITY (μ)

Channel mobility, μ, is a critical parameter for all TFTs. It determines TFT performance in terms of current drive and frequency response and it is discussed in detail by Hoffman (47). Details relevant to the present work are presented here briefly.

Mobilities in linear and saturation regimes can easily be calculated by differentiating Equation 3.19, for the linear and the saturation regimes. In the linear regime, mobility is given as:

$$\mu_{LIN} = \frac{L}{WC_i V_D}\left(\frac{\partial I_{DLIN}}{\partial V_G}\right) \qquad 3.\ 23$$

while in saturation regime, the mobility is:

$$\mu_{SAT} = \frac{L}{WC_i}\left(\frac{\partial^2 I_{DSAT}}{\partial V_G^2}\right) = \frac{2L}{WC_i}\left(\frac{\partial \sqrt{I_{DSAT}}}{\partial V_G}\right)^2 . \qquad 3.\ 24$$

It is common practice, and also evident from Equation 3.24, that plotting $\sqrt{I_{DSAT}}$ against V_G results in a straight line. The slope when squared yields the saturation mobility while the x- intercept with the V_G axis gives V_T.

These methods for calculating mobility are commonly employed but are subjected to errors when mobility is gate voltage dependent. This dependence is due to interface roughness scattering, velocity saturation, electron trapping etc. It has led to the definition of several different kinds of mobilities, which are distinguished by the procedure employed for their estimation from measured data. One of them is the average mobility, μ_{AVE}, extracted from the channel conductance measured in the linear regime of operation and physically corresponds to the average mobility of all carriers in the channel whether above or below V_T. The defining relation for average mobility is given by Equation 3.25:

$$\mu_{AVE} = \frac{L}{WC_i V_D}\left(\frac{I_{DLIN}}{V_G - V_{on}}\right). \qquad 3.\ 25$$

It is nearly identical to the commonly used expression of effective mobility μ_{EFF}, in MOSFET. The primary difference is the use of V_{on} in the place of V_T. In the case of multiple trapping and release models (3.3.3) this gives a physically

meaningful gate voltage dependent mobility since it is the average over both trapped and free carriers.

3.4.4 The role of dielectric-semiconductor interface in thin-film transistors

The dielectric-semiconductor interface, in a TFT, is where the conducting channel is formed allowing carriers to flow between source and drain terminals. The voltage required to create this channel is determined in large part by the capacitance C_i of the dielectric which is related to its dielectric constant, k, by $C_i = \frac{k.\varepsilon_o}{d}$; with d and ε_o, the dielectric thickness and permittivity of free space, respectively. The conducting path covers only a few nanometres of the interface of the semiconductor and dielectric (48). The quality of this channel is the most important for device performance and is easily influenced by interface roughness, surface energy, impurities and trap states at this interface (46, 49).

Interface roughness impedes carrier flow through the channel, thereby limiting the carrier mobility. Moreover high interface trap density can increase the threshold voltage and the operating hysteresis characteristic. Figure 3.7 gives energy band diagrams of this interface for n type semiconductor, which demonstrates the effect of interface states on the bands. In the case of no interface states gate voltage comparable to flat band voltage or V_{on} is sufficient enough to form an accumulation layer and further increase results in band bending which depends upon carrier concentration of semiconductor too. However, the presence of interfacial states may result in additional band bending, which varies as the density of these surface states. V_G beyond V_{on} is then required to fill the traps up to the Fermi level until V_T is reached. It is followed by conduction as the carriers can now drift through accumulation layer.

The poor quality gate dielectric may also contribute to excessive interface states and leakage current hence limiting the range of TFT applications. Furthermore, it plays a role in determining the microstructure of the first few nano-meter layer of the semiconductor (in cases where semiconductor is grown on top of the dielectric). The structure of these layers is considered to be critical to the performance of organic semiconductors based TFTs (50). Here are some important

film features and performance metrics for an optimal gate dielectric, the choice of which is very critical.

A dielectric should possess high dielectric constant, ensure small leakage currents and have a smooth surface with no cracks and minimum impurities (8). It should maintain its structure at processing temperatures and during its operating life. Further a dielectric should exhibit environmental stability, easy processability without deterioration and interference with other materials, i.e. materials compatibility.

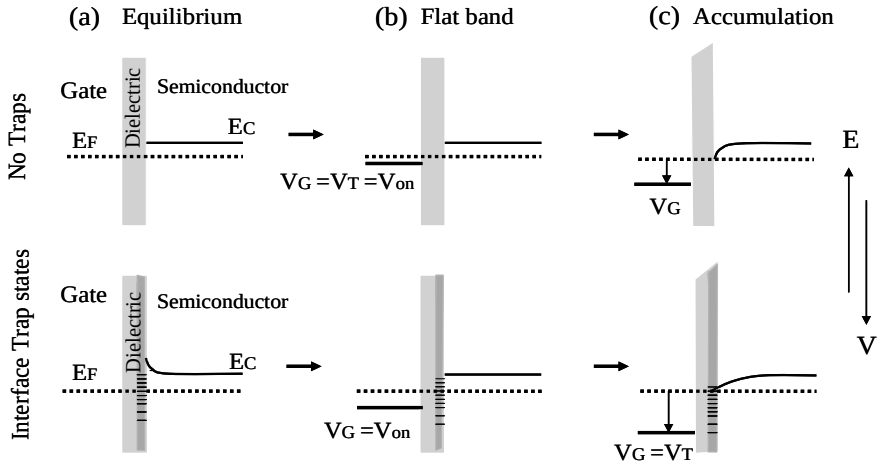

Figure 3.7: The metal dielectric semiconductor band structure for n type semiconductor in the absence and presence of interfacial trap states, between CB and VB. VB and vacuum level are not shown here. (a) Equilibrium condition when no bias is applied even though trapping states give rise to band bending. (b) Flat band condition to be met requires a higher voltage due to trapping of carriers at the interface. (c) The conduction band curvature is negative, consistent with a build-up of negative electron accumulation layer charge which is localized very near the insulator-channel interface.

The most commonly employed dielectric is silicon dioxide, SiO_2, which is thermally grown on highly doped Si. As a benchmark, SiO_2 has excellent insulating properties due to its large bandgap (8.9 eV) and high thermodynamic stability. The prime importance of SiO_2 stems from its ability to passivate Si surface and its small surface roughness i.e. 0.5 nm, under controlled preparation. But even SiO_2 needs to be passivated as surface – OH groups play an important role on the surface chemical properties since they can work as effective adsorptive or reactive sites (51). The most commonly employed material is hexamethyl disilazane (HMDS)

($[(CH_3)_3Si]_2NH$) (52). Also the activity of – OH groups has been effectively altered by doping SiO_2 with metals e.g. Al, T_i, and Z_r (53).

Organic dielectrics are another class which has gained much attention, especially for the family of flexible devices. They offer simple solution processing with high degree of optimization, to meet device requirements. Moreover they allow the fabrication of top gate devices if the dielectric solvent is not deteriorative for the layers underneath. The charge induced in the semiconductor for any given dielectric is given by $Q = \frac{k.\varepsilon_o.A}{d}V$ where A is the area. This implies that increasing the capacitance, C_i, through increasing the dielectric constant, k, or reducing the film thickness, d, would reduce the voltage required to induce the same amount of charge in the semiconductor. Low operating voltages TFT eventually lead to battery powered applications. This has been achieved by minimizing dielectric thickness through several approaches. Thinning of inorganic dielectrics such as SiO_2 < 10 nm however has rendered TFT with high leakage currents due to drastic increase in tunnelling current, making it incompatible for low mobility semiconductors (54). In order to achieve the thinnest dielectric films, great attention must be devoted to self-organization of the molecular film. This has been achieved by using ultrathin self-assembled monolayer (SAM) (55-59) as well as multi-layers (60) in gate dielectrics. In commonly used SAMs, the aliphatic chains effectively insulate the gate, after bonding to oxidized aluminium gate electrodes. The SAM molecules employed usually consist of a functional group which bonds to the gate and an alkyl chain which presents a large tunnelling barrier for the charge carriers. Like organic polymers, SAMs can be chemically tailored to optimize material compatibility and device performance. In this way transistors operating at < 2 V have also been demonstrated (55), using metal/transparent oxides as the semiconductor (61).

3.4.5 Trap density estimation

It is clear that trap states at the insulator semiconductor interface affect the device performance by capturing the free carriers. Not all of the accumulated charge carriers will therefore be available for conduction. Improvement in device performance for future applications thus relies heavily on estimation of trap density employing the transistor characteristics.

Here we present some commonly employed methods of calculating the density of traps. It is well known that these traps can be considered as an additional capacitance per unit area, (C_{it}) acting in series with the geometric capacitance of the dielectric, (C_i) per unit area. From elementary theory of MOSFET, subthreshold slope relates the two by the following relation (62):

$$S = \frac{kT\ln(10)}{q}\left(1+\frac{C_{it}}{C_i}\right). \qquad 3.26$$

For the ideal situation of no traps, the room temperature subthreshold slope turns out to be kTln(10)/q $\approx$60mV/dec. The density of traps (D_{it}) expressed in units of [energy]$^{-1}$[length]$^{-2}$, is related to C_{it} as D_{it}= C_{it}/q^2 and therefore can be obtained using equation (3.26) as:

$$D_{it} = \frac{C_i}{q^2}\left(\frac{qS}{kT\ln(10)}-1\right). \qquad 3.27$$

However this method is not always accurate as the subthreshold operation of the transistor is also under the influence of bulk charges (63, 64) which can arise from traps or incomplete ionized defects. These bulk states, when close to the band edge, give rise to high film conductivity and hence high off currents. Therefore for this method to be valid, high on-off ratio is required. As mentioned earlier, the interface states trap the free carriers thereby increasing the threshold voltage necessary for carrier accumulation in the channel. V_T can therefore serve as a measure of number of traps N_t ([length]$^{-2}$) that have to be filled up to V_T. Hence it provides another method for evaluating the trap density using the following relation:

$$N_t = \frac{C_i\left|V_T - V_{on}\right|}{q}. \qquad 3.28$$

It is interesting to note that upon cooling higher trap density results from the shift of the Fermi level towards the CB edge. This demands for more and more carriers to fill in the states before any thermal activation for conduction in the channel can occur. This effect is clearly manifested in V_T as it becomes temperature dependent. If this dependence is linear the energy distribution of traps (i.e D_{it}) becomes energy independent within few kT. The energy distribution of traps then can be calculated using the following expression (65):

$$D_{it} = \frac{\partial N_t}{\partial E} = \frac{C_i}{qk}\frac{\partial V_T}{\partial T}. \qquad 3.\ 29$$

Although these methods provide an easy way of calculating the trap density, they may lead to different values of D_{it} since the energy regions probed are different in the two cases.

There are other methods developed particularly for polycrystalline devices such as Levinson's model (66) that could in principle be used. The latter accurately models the drain current at higher gate biases but not the turn-on behaviour of the TFT as it assumes a uniform charge distribution induced by V_G. The drain current in a polycrystalline TFT evaluated using the Levinson model has the following form:

$$I_D = \frac{W}{L}\mu_b V_D C_i V_G \exp\left(-\frac{q^3 N_t^2 t}{8\varepsilon kTC_i V_G}\right) \qquad 3.\ 30$$

where t, and ε are semiconductor thickness and permittivity respectively while all other terms have their usual meanings. Values of μ_b and N_t can be obtained by plotting $\ln(I_D/V_G)$ against $1/V_G$ for small V_D. After performing a straight line fit, N_t and μ_b are proportional to the slope (m) and y-axis intercept (c) respectively:

$$\mu_b = \frac{\exp(c)L}{WV_D C_i} \qquad 3.\ 31$$

and

$$N_t^2 = -m\frac{8\varepsilon kTC_i}{q^3 t}. \qquad 3.\ 32$$

The model has been found applicable in the majority of polycrystalline TFTs including ZnO based devices (67-70).

3.4.6 Metal semiconductor junctions: role of contact resistance in thin-film transistors

During the development of transparent oxide TFT, metal to semiconductor contact effects have become noticeable. These are considered to be major obstacles in realizing long life time operation of the devices. Charge carrier injection and

extraction into and out of the semiconductor is very crucial for any metal electrodes chosen for a TFT.

When a contact is made between a metal and semiconductor, Figure 3.8(a), the Fermi levels of both sides line up as charge transfer takes place. This results in the formation of an energy barrier (φ_{Bn}). This energy barrier is a function of the electron affinity of the semiconductor (χ), and the metal work function (φ_m), as expressed y Equation (3.33) and depicted in Figure 3.8(c).

$$\varphi_{Bn} = \varphi_m - \chi + \Delta \qquad 3.33$$

where Δ represents the potential across the unavoidable interfacial layer between metal and semiconductor.(71) Moreover the presence of interface trap states also alters the barrier height through additional band bending, not shown here. For an n-type semiconductor with work function $\varphi_s < \varphi_m$, the contact is rectifying and allows current flow in one direction only. Δ=0 is referred to as the vacuum level alignment on either side or the Mott-Schottky limit for carrier injection (72).

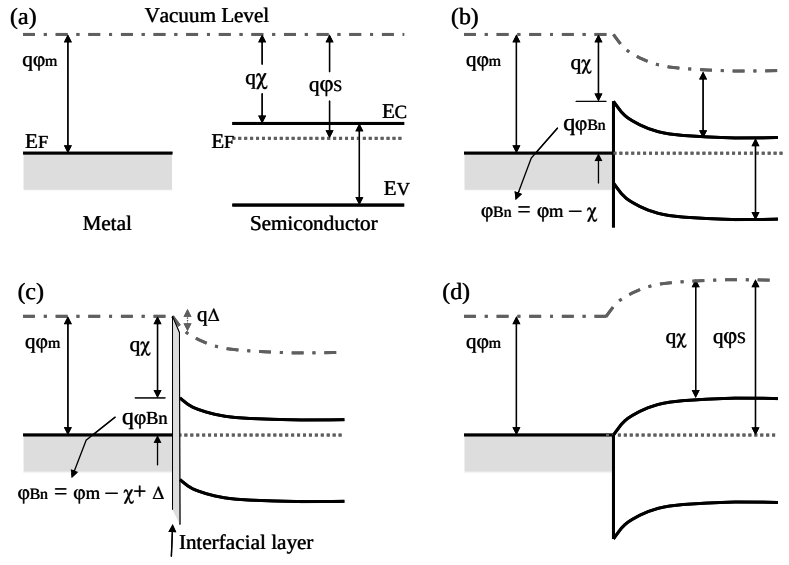

Figure 3.8: Energy band diagram of (a) an isolated metal adjacent to an isolated *n*-type semiconductor under thermal non equilibrium condition. (*b*) metal semiconductor contact in thermal equilibrium without interfacial layer, (c) metal semiconductor contact in thermal equilibrium with interfacial layer, difference in band bending is evident. (d) an ideal equilibrium diagram of an ohmic contact between a metal and semiconductor

The Schottky barriers few tenths of angstroms in thickness, through which majority carriers can tunnel in either direction are termed as ohmic contacts. Ohmic contacts can also be formed if $\varphi_m < \varphi_s$, as shown in Figure 3.8(d). This leads to a linear relation in I-V characteristics. The major loss of device performance is often caused by high-resistance metal-semiconductor Ohmic contacts through thermal stress and/or contact failure (73).

Thermally stable and reliable low resistance ohmic contacts can be achieved either by performing surface preparation to reduce the metal-semiconductor barrier height or by increasing the effective carrier concentration at the surface (74, 75). With wide band gap semiconductors, thermal annealing produces low contact resistance but is also associated with various disadvantages such as surface roughness and structural degradation at the interface (76, 77). To avoid annealing low specific resistance non alloyed metals are often preferred (74, 78-80).

A quantitative measure of the ohmic contact quality is the contact resistance (R_c) also called parasitic series resistance. Among various methods the most common way to determine R_c is by using the scaling Law method (81, 82). In this method, the operating characteristics of identical transistors but of different channel lengths are analyzed. Total resistance (R_T) of each device in linear operating regime can be written as:

$$R_T = \frac{\partial V_{DLIN}}{\partial I_{DLIN}} = R_{ch} L + R_c . \qquad 3.\ 34$$

where R_{ch} is the channel resistance per channel-length unit (L). The determination of these parameters involves plotting of R_T *(*at low V_D) for different V_G against L, then fitting the experimental values with linear curves for each V_G. R_c and R_{ch} can then be calculated from the intercept with the y-axis of each fitting and slope respectively.

Very little work has been published on the effect of contact resistance in TFTs fabricated with wide-bandgap semiconductors such as metal oxides. In a recent report (83), on a-InGaZnO based TFT, plasma exposure of S/D bulk region has produced very low contact resistance leading to gate overlap independent transfer characteristics unlike for a-Si:H based TFTs (84). Also a-InGaZnO TFTs

with short channels require precise control of the contact resistance as it decreases the mobility in short channel TFTs (85).

3.5 Ambipolar thin-film transistors

It is well known that complementary metal oxide semiconductor (CMOS) technology dominate all modern digital electronics as it can deliver high speed, low power dissipation and an excellent noise margin. For the design of efficient transparent integrated circuits, there is an urgent need to find ways towards transparent semiconductors which are p-type so they complete the wide range of n-type oxide semiconductors. In recent years great effort has been focussed towards the development of p-type oxides but with little success (86). Therefore the idea of hybridization of inorganic TOS with organic seems to be a viable alternative towards complementary integrated circuits. The following section provides a brief overview of ambipolar transistors that could be fabricated using hybrid semiconducting systems.

3.5.1 Device operation

An ambipolar transistor can be biased into the linear regime of operation for either electrons or holes. The amount of charge induced at any point x in the channel is a function of the effective gate voltage V_{eff} which is merely a difference of V(x) and V_G. For $|V_D|<|V_G-V_T|$ with V_D and V_G having the same sign, unipolar transport occurs for either of the carriers depending upon the applied voltage sign (87, 88). For $|V_G-V_T|>0$, electron accumulation in the channel leads to n- type current conduction and correspondingly, for negative V_G-V_T, holes accumulate in the channel making it p-type. When $|V_D|=|V_G-V_T|$, the effective gate potential at the drain is zero and the channel becomes pinched. If now $|V_D|\geq|V_G-V_T|>0$ is applied the effective gate potential becomes negative at the drain, increasing the pinch-off region for *n*-type conduction. The opposite situation holds true when $|V_D|\leq|V_G-V_{T,h}|<0$. Therefore, when $|V_D|>|V_G-V_T|$ a sign inversion in the effective gate potential yields ambipolar transport and both type of current conduction with TFT operating in saturation.

Note that if V_D has the opposite sign with respect to V_G-V_T the transistor operates as a unipolar TFT, with source and drain inverted. In both p- and n-type operations, high on-off current ratios at low V_D are possible. At higher V_D the contribution of "opposite" sign carriers in the unipolar region in the off-region,

where V_G-V_T and V_D have opposite sign, significantly decrease the on-off current ratios. Their ability to operate at both positive and negative V_G makes possible to build complementary like circuits using the same number of TFTs.

In an ambipolar transistor the total channel length comprises of an electron accumulation region as well as a hole accumulation region and therefore the total drain current, derived from the gradual channel approximation in the saturation regime, is given as:

$$I_D = \frac{W}{2L} C_i \left[\mu_e \left(V_G - V_{T,e} \right)^2 + \mu_h \left(V_D - \left(V_G - V_{T,h} \right) \right)^2 \right] \qquad 3.\ 35$$

The ambipolar transfer curve represents the channel current for both positive and negative V_G, as a manifestation of both electron and hole accumulation, depending upon V_D as shown in Figure 3.9 (a). The output curves [Figure 3.9 (b)] show the normal saturated behaviour for one charge carrier, j, at $|V_D|>|V_G-V_{T,j}|$ but as soon as the other charge carrier is injected superlinear current increase is observed for small gate voltages and large drain-source voltages.

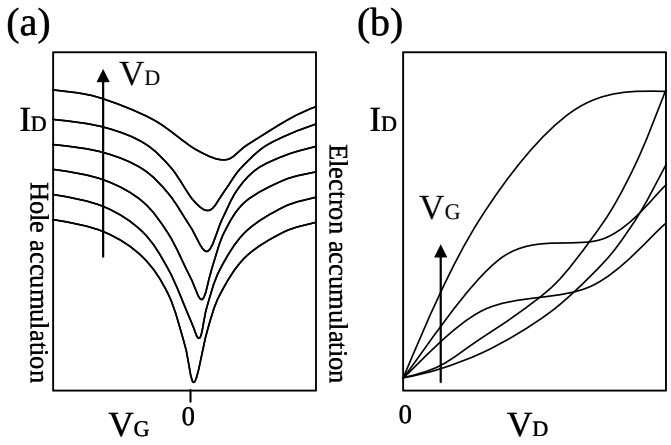

Figure 3.9: Calculated operating characteristics of an ambipolar transistor. (a) Transfer curves in V-shape representing both electron and hole accumulation at different V_D. (b) Output curves for various gate voltages.

It is also important to mention that at the meeting point of two accumulation layers in the channel, there exists the likelihood of recombination of holes and electrons which can lead to light emission if the material is electroluminescent (89, 90). Due to the fact that both types of charges can be induced in the transistor, fabrication of complementary like logic for inverters is possible. The latter has been found to be

superior to the unipolar logic due to reduced complexity of device fabrication and good performance characteristics (91, 92).

3.5.2 Ambipolar thin-film transistors based on semiconductor heterostructures

In organic electronics, ambipolar TFTs have been demonstrated using various types of bilayer structures (93, 94) as well as single component materials (87, 95). In layered heterostructures, n- and p- type thin films are successively built up though an energy barrier keeps charge carriers from moving across the materials. Therefore there exist two separate channels for carrier conduction. High performance circuit applications demand the use of TFTs with comparable n- and p- type mobilities. However, the carrier mobility is found to be low for n type organic TFTs. To circumvent this problem, the concept of organic/inorganic hybrid ambipolar inverters has been successfully employed by Dodabalapur (96-98). The recent addition of n-type oxide semiconducting compounds to the family of electro-active materials has opened up new areas of research with the introduction of oxide-organic hybrid systems. Nakanotani has reported high-performance ambipolar TFTs based on hybrid structures containing an indium zinc oxide IZO and pentacene bilayer, which exhibit ambipolar TFT characteristics (99). This combination with inclusion of a SAM layer has further led to balanced electron and hole mobilities (100). In another report (101), Pentacene was hybridized with an n-channel InGaZnO and the combination has shown promising properties for future circuit applications. A similar approach has been used in this thesis and will be discussed in chapter 6.

3.6 Voltage Inverters: The NOT gate

TOS have not only been used for the development of high performance discrete TFTs but also in integrated microelectronic circuits. The voltage inverter is the simplest logical operation to implement and can be cascaded into more complex logic circuits. In this section, a brief introduction of the inverter circuit with particular features affecting its operation is provided.

An inverter is a series combination of a drive transistor (operating as a switch) and a load, which is often another transistor as shown in Figure 3.10. Their function is to provide an output that is the NOT to the input. For instance, if a high

voltage (a "one") is placed on the input of an inverter, it returns a low voltage (a "zero") and vice versa.

There are several different configurations for inverters where various logics are exploited using a variety of circuit arrangements and transistor types. Here we will focus on complementary logic and unipolar logic circuits only. The complementary metal oxide semiconductor CMOS circuits employ both n- and p-type devices to effectively implement two switches controlled by a single input, one to pull the output up (the p-type transistor) and other to pull the output down (the n-type transistor). However, in the present state of TOS-based TFTs, this is just not possible due to the absence or low performance of p- type TOS. Thus, a transistor load of the same polarity as the control transistor must be used. Typical circuit diagrams for both logics are shown in Figure 3.10 (a, b, c).

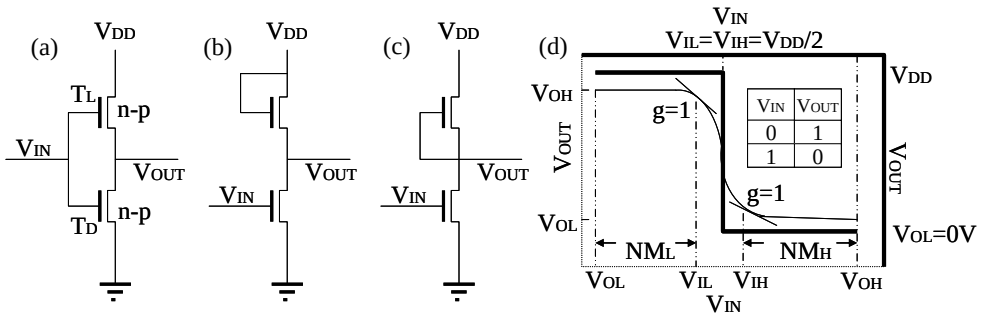

Figure 3.10: Schematic Inverter circuits, V_{DD} is supply voltage (a) complementary using ambipolar transistors, (b) unipolar diode-connected load logic (c) unipolar "$V_G = 0$" logic. (d) A representative voltage transfer characteristic (VTC) for an inverter, bold line shows an ideal form. At input voltages below V_{IL}, the control transistor is on and negligible current flows through the inverter, hence the output voltage is at a relatively constant high level, V_{OH}. As the input voltage increases beyond V_{IL}, the control transistor turns on causing an increase in the voltage drop across the load. Once the input exceeds V_{IH}, the inverter has reached a steady state in both the current and output voltage. The gain of an inverter is defined as the maximum change in output voltage with respect to a change in the input voltage; this corresponds to the slope of the VTC between V_{IL} and V_{IH}. The inset shows the truth table for an inverter.

It is clear from the Figure 3.10(a) that in complementary logic both transistors, whether ambipolar or discrete n- and p- type, are biased from the same supply which keeps one transistor off all the time (98, 102). The latter implies that power dissipation is limited only to the switching time between the two inverter states. This case is just opposite to that seen in unipolar logic where one of the

transistors always has to be on and thus power dissipation remains higher for both states (96, 98, 103).

For unipolar logic with similar transistors, either a difference in I_{on} or a difference in V_T between the drive and load transistors is essential for inversion to take place. An approach called ratio'd logic is commonly applied to alter I_{on} exploiting the transistor channel width, (W). It allows the load transistor to be connected in two ways in the circuit. Load transistor's gate is either connected to the supply voltage V_{DD} just like a diode as shown in Figure 3.10(b) or to the source (known as "Vg= 0" logic) as shown in Figure 3.10(c). Moreover, the most ideal same-polarity load in "$V_G = 0$" logic is a depletion load (104). Its default on-state, with the gate tied to the source, allows conduction to occur until V_{OUT} reaches the V_{DD} voltage.

Quantification of the inverter function can be given from its voltage transfer curve (VTC) (105). The latter is shown in Figure 3.10(d). The real inverter exhibit a transition range where the inverter switches from high to low level. The slope of this range ($g = \partial V_{OUT}/\partial V_{IN}$) equals the voltage gain of the inverter obtained if it was used as a voltage amplifier. The noise margin is another important characteristic representing voltage ranges recognised as either "on/high" or "off/low" shown in Figure 3.10(d) and defined as:

$$NM_L = V_{IL} - V_{OL}, \qquad NM_H = V_{OH} - V_{IH}, \qquad 3.36$$

where V_{IL} and V_{IH} are the input low and input high voltages for which the output level is clearly high V_{OH} and low V_{OL} respectively. For several inverter stages the signal can propagate without attenuation only if gain is above unity. The noise margin on the other hand gives an account of the circuit's tolerance to signal fluctuations i.e. noise.

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Chapter 4

Experimental methods

Abstract

This chapter reviews the experimental methods used throughout this thesis for the growth and study of the optical, electrical and structural properties of zinc oxide (ZnO) thin films and thin-film transistors (TFTs). The methods used for the surface functionalization of metal gate electrodes with self-assembling monolayer (SAM) dielectrics and the study of the solid surface energy characteristics are also described in detail.

4.1 Material fabrication and characterization

4.1.1 Thermal analysis of zinc precursor

Thermal methods of investigations are generally preferred for characterizing a system (element, compound or a mixture) using heat to force reactions and physical changes. Two of these methods are a) thermo-gravimetric analysis (1) (TGA) and b) differential scanning calorimetry (DSC) (2). TGA provides quantitative measurement of mass change in materials associated with transition and thermal degradation, e.g. dehydration, decomposition, and oxidation, with time and temperature. Mass is lost if the substance contains a volatile fraction. This can be very useful to investigate the thermal stability of a material, or to investigate its behaviour in different atmospheres (e.g. inert or oxidizing).

DSC measures the change of the difference between the heat flow rate to the material (sample) and to a reference sample while they are subjected to a controlled temperature program. The reference is an inert material such as alumina, or just an empty aluminium pan. The temperature of both the sample and reference are increased at a constant rate. The result of DSC is a curve of heat flux versus time or temperature and is therefore used also for determination of the enthalpy, specific heat etc.

In the present work, we have performed both TGA and DSC to understand the thermal behaviour of the zinc acetate precursor. TGA was conducted under air at a scan rate of 10 °C/min with a TA Instruments Q500e. DSC measurements were conducted under nitrogen at a scan rate of 10 °C/min with a Mettler Toledo DSC822 instrument using medium pressure steel pans.

4.1.2 ZnO thin film deposition by spray pyrolysis

In recent years there has been a great deal of interest in ZnO and its application in transparent thin film transistors (TFTs) (3) primarily due to its optical transparency (i.e. wide bandgap), high charge carrier mobility and its exceptional photostability when compared with traditional inorganic semiconductor based devices such as poly-Si TFTs. A further important advantage associated with ZnO is that high-quality crystalline films can be grown at relatively low deposition temperatures on various substrates including glass as well as commoditised substrates such as low-cost plastic. Because of this a large number

of studies have already been published describing the use of ZnO in various electronic applications including TFTs (4-9). In the vast majority of these studies ZnO films were grown by traditional vacuum based methods such as sputtering, pulsed laser deposition, atomic layer deposition etc. Unfortunately, vacuum based technologies are intrinsically complex and expensive but above all incompatible with large area substrates. For this reason in recent years there has been significant effort towards the development of alternative deposition paradigms based on solution processing due to the simplicity and huge potential for ultra low cost, particularly for large area deposition. Next we describe the simple and highly scalable method, namely spray pyrolysis (SP), used for the deposition of ZnO films used throughout this thesis.

SP relies on the spraying of a carefully formulated precursor solution onto a heated substrate. Upon contact of the aerosol (precursor plus solvent) with the substrate, the precursor molecules [e.g., Figure 4.1(a)] react to form a stable compound the properties of which depend on the chemical composition of the precursor formulation (10). Under optimised conditions the method ensures stoichiometric invariance from the very solution composition as each atomized droplet results in single submicron sized particle (11, 12). The substrate/deposition temperature is critical and determines the morphology, crystallinity, porosity as well as the optical and electrical properties of the deposited film (11, 12).

Unlike conventional oxide deposition techniques the process is simple, scalable and requires very low capital investment. A further intriguing aspect of the proposed approach is the extraordinary control over the chemical composition and thickness of the deposited layers. For example, by controlling the composition of the precursor solution likewise, the stoichiometry of the pyrolysed films can easily be controlled. The molarity of the precursor solution and the feed-speed to the spraying nozzle can be used to control the film thicknesses down to 10 nm with great accuracy.

Figure 4.1(a) shows the precursor material, namely zinc acetate dihydrate used for the deposition of the ZnO films in this work. Figure 4.1(b) displays the schematic of the spray pyrolysis set up developed and used in this thesis. The latter comprises a commercially available handheld air brush shown in Figure 4.1(c), for

the spraying of a methanolic precursor solution (0.1M concentration) onto heated substrates [T = 200-500°C].

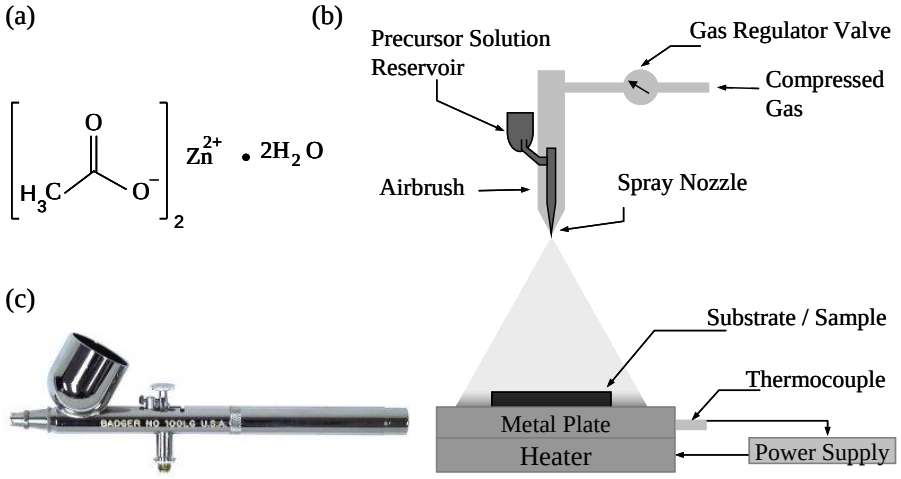

Figure 4.1: a) Chemical structure of the precursor zinc acetate dihydrate.
b) Schematic representation of the spray pyrolysis system developed.
c) Picture of the actual Badger 100 air brush.

Upon contact of the aerosol with the heated substrate the following chemical reaction takes place (13):

$$Zn(CH3COO)_2 \cdot 2H_2O + 2CH_3 - OH \rightarrow ZnO + 2CH_3 - CO - CH_3 + 3H_2O \quad 4.1$$

Using the SP setup, uniform, homogeneous and highly reproducible films were grown by following the deposition procedure described next. It is to be noted that the latter is the result of tedious optimisation carried out on both the material combination and the various experimental conditions. In brief, deposition consisted of a set of 5 spraying cycles carried out in ambient air i.e. no controlled atmosphere. In each cycle the precursor solution was sprayed intermittently onto substrates for approximately 12 s followed by an intermediate waiting step of 48 s. The latter step was introduced in order to ensure that the droplets adsorb to the surface of the substrate and fully convert to ZnO. Following the film spraying sequence and before any further device processing, the samples were allowed to cool down to room temperature by gradual cooling lasting approximately 5 minutes.

4.1.3 X-ray diffraction

The X-ray diffraction (XRD) measurements can provide valuable information about the microstructure of different forms of solid state materials (e.g. powders, films, bulk crystals etc) down to the nm scale. The interaction of electromagnetic waves, such as X-rays, with the periodic lattice produces diffraction effects provided that the wavelength and periodicity of the lattice are comparable. For instance, X-rays with wavelengths on the order of ~1 Å incident on the surface of a crystal will be scattered by the atoms/ions lying on crystal lattice. The reflected waves can interfere constructively to produce diffraction patterns only when Bragg's law [Figure 4.2] is satisfied:

$$2d \sin\theta = n\lambda \,. \qquad 4.2$$

In this equation n is the reflection order (1, 2, 3...) and d is the atomic interplanar spacing.

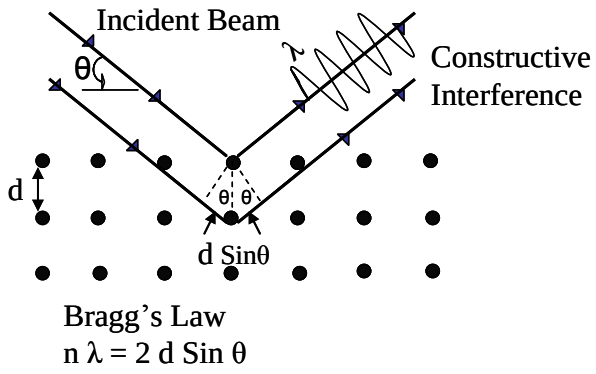

Figure 4.2: Bragg's law: A simple expression relating the wavelength (λ) of the incident X-ray, interplanar spacing (*d*), and angle (θ) of diffracted beam. If the Bragg's law is not satisfied, the interference will be non constructive yielding very low intensity diffracted beam.

Since no crystal is perfect as it is not infinitely extended in all directions, such a deviation from perfect crystallinity leads to broadening of the diffraction peak. Moreover, distribution of lattice spacing, crystal domain size and orientation contribute to crystal disorder and hence peak broadening. In polycrystalline material the crystallites may have a random or non random distribution of orientation. A solid sample is called "textured" if its grains are aligned in a preferred orientation along certain lattice planes. Crystallite size is a measure of the size of a coherently diffracting domain. The Scherrer formula (14) (Equation 4.3) is

often used to analyse the average crystal size (K_o) with peak broadening, assuming that the sample consists of sub micrometer domains (15). The crystallite size can by determined once the Bragg angle is known using:

$$R_o = \frac{K\lambda}{\beta_W \cos\theta} \qquad 4.3$$

where R_o is the averaged dimension of crystallites; K is the Scherrer constant, somewhat arbitrary value that falls in the range 0.87-1.0 (it is usually assumed to be 1); λ is the wavelength of the X-ray used and β_W is the integral breadth of the diffraction width at half maximum.

In this work the structural properties of ZnO films grown by SP at different substrate temperatures (T_S) in air were examined by wide angle X-ray diffraction measurements performed using an Oxford Diffraction Xcalibur^{TM} XP instrument employing a Mo Kα graphite monochromatic radiation with λ = 0.71073 Å. The average size of the crystallites comprising the film was calculated using Scherrer formula (Equation 4.3).

4.1.4 Atomic force microscopy (AFM)

The AFM technique is a powerful tool often used to investigate the surface characteristics of thin solid films with nanometre resolution. AFM measurements can provide extraordinary topographic contrast, direct height measurements and unobstructed views of the surface's nanoscopic features, both morphological as well as electronic. A typical AFM system has different modes of operation depending upon the nature of the contact between the sharp cantilever's tip and the sample that is being imaged. For example, whether the tip comes in close contact or oscillates in very close proximity to the sample, the respective modes are known as contact and tapping mode. The motion of the tip is controlled by a feedback loop and piezoelectric scanners. A semiconductor diode laser is bounced off the back of the cantilever onto a position-sensitive photodiode detector. This detector measures the bending of the cantilever during scanning over the sample. The measured cantilever deflections are used to generate a map of the surface topography. The schematic layout of an AFM system is shown in Figure 4.3.

For this work a Pacific Nanotechnology Nano-R2 AFM system was employed. The system has allowed imaging of the as-prepared samples over surface areas up to 60×60 μm with a vertical resolution of the order of 1 nm. Using

the AFM measurements the root mean square (r.m.s.) and peak-to-peak roughness of the film's surfaces was calculated.

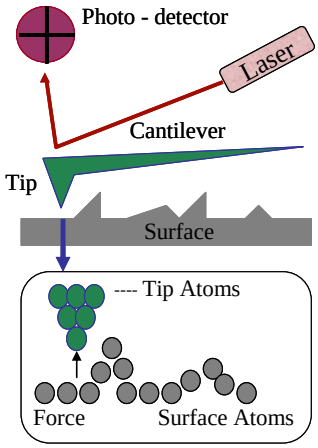

Figure 4.3: Schematic representation of an atomic force microscope (AFM). A laser beam is deflected off from the surface of a scanning cantilever. The deflection is converted to distance allowing mapping the surface topography.

4.1.5 Ultraviolet-visible optical spectroscopy

Absorption spectra measurements were carried out using a Varian Cary 05E spectrophotometer in Ultraviolet-Visible (UV-Vis) to near-infrared range of the electromagnetic spectrum. The principle of the instrument is straight forward. A monochromatic beam generated using a visible/UV light source is split into two equal intensity beams. One of the beams is passed through the sample (substrate/ZnO film) while the other through a reference sample i.e. a blank substrate. The two beam intensities, defined as I and I_o, respectively, are measured by high sensitivity optoelectronic detectors. After scanning the entire available wavelength range, a plot between Absorbance ($A = \log (I/I_o)$) and wavelength (λ) can be obtained. Substrates used for this study were based on borosilicate glass and are commonly known as spec-B substrates. ZnO thin films were deposited by spray pyrolysis directly onto spec-B substrates while organic materials were spin casted from solution in nitrogen. The film thickness of the as-deposited films was determined using Dektak profilometer.

4.1.6 Surface energy analysis

The physical characteristic of a solid surface on which film deposition from solution occurs is critical and can determine the optical as well as electronic quality of the solid-surface/film interface. Surface energy analysis is therefore an important characterisation tool and can determine how well a liquid will wet the surface of a substrate as shown in Figure 4.4. The surface energy (γ) is the energy required for new surface formation from the bulk material and occurs as the continuity in bonding at that interface is broken. A common method for determining the surface energy of a solid involves measuring the contact angles (θ) of several liquids, with known surface energy characteristics, on the solid surface (16).

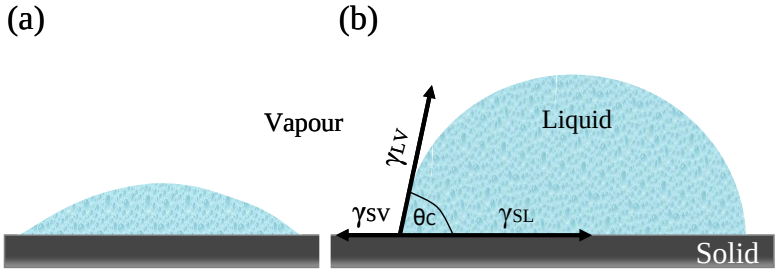

Figure 4.4: Droplets of liquid are shown on a solid surface. a) Solid surface with high surface energy. Such surfaces exhibit good wetting characteristics. b) Solid surface with low surface energy. This type of surface exhibit poor wetting and a high contact angle (θ_C). The definition of θ_C and surface energy components are also shown. γ is the interfacial energy and L, S, and V stand for liquid, solid, and vapour respectively

This approach is also particularly relevant for solution processing of organic materials since wetting can be defined as the point at which $\theta \rightarrow 0$. Figure 4.4 demonstrates the three surface energies that must be balanced out to produce Young's equation for contact angle given as:

$$Cos\theta_C = \frac{\gamma_{SV} - \gamma_{SL}}{\gamma_{LV}} \qquad 4.4$$

where S, L and V refer to solid, liquid and vapour respectively. Because the method excludes the solid-liquid interactions it was modified by Owens, Wendt and Kaelble (OWK) (17) in order to account for these interactions. In this case the surface energy has a polar component, arising due to polar interactions, and a

dispersive component which is associated with the van der Waals type interactions. In the OWK model the solid surface energy is given as:

$$\gamma_{LV}\frac{(Cos\theta_C+1)}{2\sqrt{\gamma_{LV}^D}}=\sqrt{\gamma_{SV}^P}\sqrt{\frac{\gamma_{LV}^P}{\gamma_{LV}^D}}+\sqrt{\gamma_{SV}^D}. \qquad 4.5$$

Here the superscripts D and P refer to the dispersive and polar components. Using this equation in combination with the experimental data, the solid surface energy (γ_{SV}) can be determined from the slope of the straight line between:

$$\gamma_{LV}\frac{(Cos\theta_C+1)}{2\sqrt{\gamma_{LV}^D}} \qquad 4.6$$

and

$$\sqrt{\frac{\gamma_{LV}^P}{\gamma_{LV}^D}}. \qquad 4.7$$

In this work, the method was employed to study the wetting properties of solid surfaces of gate electrodes functionalised with self assembled monolayers (SAM) dielectrics. The three test liquids employed were; i) deionised water, ii) diiodomethane and iii) ethylene glycol. It is important to mention that the same surface analysis method can also be employed to determine the surface energy characteristics of semiconductor (or precursor) solutions using liquid pendant drop analysis (18).

4.2 Device fabrication

4.2.1 Substrates

Discrete devices were fabricated on either thermally grown SiO_2 on heavily doped Si^{++} wafers or on glass. Silicon wafers were highly p-doped with 200 or 400 nm of SiO_2 oxide. Glass substrates were usually alkaline-earth boro-aluminosilicate sheet glass (Corning EAGLE2000) and microscope slides. The standard cleaning procedure consisted of sonication of the substrates in acetone and then isopropyl alcohol (IPA) followed by washing with IPA and drying with nitrogen.

4.2.2 Metal contact deposition

Different types of metal contact were evaporated in high vacuum (10^{-6} mbar) using a thermal evaporator. To avoid contamination and degradation, the evaporator is integrated into a nitrogen glove box. Different metal shadow masks were used to pattern the source-drain and gate electrodes. Dimensions of channel lengths (L), and width (W), were in the range of 20-100 μm and 0.5-2 mm, respectively. The evaporation rate used for all metals (Au, Al, Ca) was approximately 0.1 nm/sec. The typical electrode thickness was around 25-50 nm. These evaporation conditions / parameters were found to yield the best performing devices.

4.2.3 Self-assembly of organic molecules on metal electrodes

In recent years molecular self-assembled monolayers (SAMs) have received significant attention for a host of applications in the field of organic electronics. This is mainly because SAMs can provide many functions including; modification of the surface work function, modification of the surface wetting characteristics, and desirable interface chemistry (19-21). More recently, SAMs have also been used as molecular dielectrics in low-voltage, low-power organic electronics (22-24). Typically, SAM molecules are soluble and comprise a functional group which bonds to a metal or metal-oxide surface. For this work the widely known octadecylphosphonic acid (ODPA) was employed as the SAM dielectric [Figure 4.5].

The ODPA was functionalised onto oxidised Al gate electrodes and used as the SAM nanodielectric. The exact procedure used is as follows. Aluminium gate electrodes 30 nm thick were thermally evaporated under high vacuum employing shadow masks. The gate electrodes were subsequently oxidised in oxygen plasma (the power and duration of the plasma exposure were typically 80-100 W and 30 s - 5 min, respectively) and/or thermally oxidised and then ODPA SAM dielectric was deposited by drop casting using 1mM concentrated solution. Substrates were sonicated in ethanol followed by thermal annealing at 140°C for several hours to ensure optimal bonding of the phosphonic acid groups to the oxide surface. Finally, all adsorbed residues of non-bonded organic molecules were rinsed away with ultrasonic bath using pure IPA. The presence of the ODPA on the

gate electrode surfaces was confirmed using contact angle and electrical measurements.

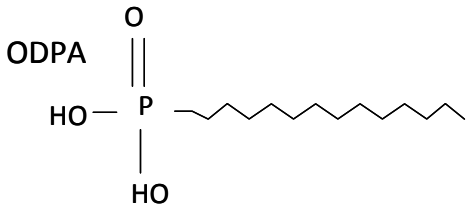

Figure 4.5: Chemical structure of the octadecylphosphonic acid (ODPA) used as SAM dielectric

4.2.4 Spin coating

All organic layers used throughout this work were processed by spin coating from solution. Spin coating is carried out by applying enough volume of solution, typically around 100 μL, to the surface of the substrate so it is fully covered. The final film thickness is determined by the spin speed (revolutions per minute or r.p.m.) and the solution viscosity. Surface reactions and premature solvent evaporation is controlled by minimising the time between solution application and the start of spinning. In addition to simple spin coating, multistage spin regimes can also be used. For example, a single spin coating recipe may consist of different stages i.e. 500 rpm for 10 sec followed by 2000 rpm for 20 sec. The latter procedure was used for the processing of acene:polymer organic blend films employed for the fabrication of hybrid devices. In the case of more viscous material solutions such as the fluoropolymer CYTOP (25) dielectric, films were spin coated at 2000 rpm for 60 sec. This high spin speed ensured good film uniformity across the entire sample.

4.3 Electrical characterization

4.3.1 Current-voltage characteristics and circuit measurements

The electrical characteristics of a thin-film transistor are virtually identical to these obtained from a conventional metal oxide semiconductor field effect transistor (MOS-FET). For both types of devices two main measurements are usually performed. The first one is the measurement of the output curves. Here, the source-drain current (I_D) is monitored as a function of drain voltage (V_D) while

keeping the gate voltage (V_G) fixed. The same measurement is then repeated for different V_G bias. The V_G chosen typically represent all operating regimes of the device i.e. depletion, accumulation and saturation. The second type of measurements relates to the evaluation of the so-called transfer characteristics. Here, I_D is monitored over a range of gate voltages with drain voltage fixed at a constant value. The same measurements are then repeated at a different fixed drain voltage. From these measurements important information can be extracted including; the carrier mobility, the transistor on/off current ratio, and the gate leakage current.

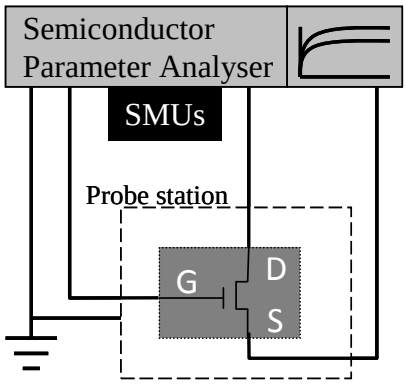

Figure 4.6: Schematic representation of the apparatus used for electrical characterisation of ZnO thin-film transistors.

Figure 4.6 shows a simple schematic of the apparatus and the device configuration used for the electrical characterisation of ZnO TFTs. A semiconductor parameter analyser (Keithley 4200) equipped with four source measuring units (SMUs) was used to monitor the currents and apply the voltages across the source, drain and gate terminals. Connection between the transistor contacts and the analyser were made through electrical microprobes mounted onto specially designed micro-positioning stages. Electrical measurements were performed in air or under N_2 containing less than 0.5 p.p.m. of oxygen. The electrical characteristics of the transistors as a function of temperature were also measured using a Janis cryogenic probe station under high vacuum. In this case all measurements were obtained under vacuum of $\sim 10^{-5}$ mbar. The electrical characteristics were then analysed to obtain various transistor parameters including; charge carrier mobility, sub threshold voltage swing, channel on-off ratio and the threshold voltage.

Electrical characterisation of integrated circuits such as the logic voltage inverter, or NOT gate, was performed using the same semiconductor parameter analyser in a quasi-static mode using all four SMUs. Specifically, the first SMU was used for applying the input voltage (V_{IN}), the second SMU for monitoring the output voltage signal (V_{OUT}), the third SMU for supplying the power to the circuit (V_{DD}), and the fourth SMU was used as the ground terminal. The transfer characteristics of the circuit were then evaluated by measuring V_{OUT} as a function of V_{IN} at different voltage ranges at a fixed V_{DD}. The obtained data was then analysed to extract important circuit parameters such as noise margins and differential signal gain.

4.3.2 Capacitance-voltage measurements

Evaluation of the charge carrier mobility using the transfer characteristics of a transistor requires a prior knowledge of the geometrical capacitance (F/m^2) of the gate dielectric employed. In this work the geometrical capacitance (C_i) of the different dielectrics used were measured using an impedance analyser (Solartron 1260) connected to the two terminal metal-dielectric-metal capacitor device as shown in Figure 4.7.

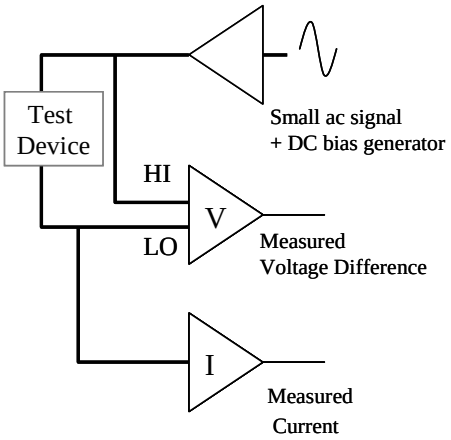

Figure 4.7: Schematic representation of the apparatus used for measuring the capacitance-voltage characteristics of sandwich type structures.

A small amplitude (50 mV) ac signal was then superimposed over a dc voltage and applied across the device. From the phase and amplitude change the real and imaginary parts of the impedance (Z) were calculated and used for the analysis of the dielectric properties of the insulator materials under investigation. The geometric capacitance of the device was then estimated using:

$$C_i = \frac{1}{A\omega \,\mathrm{Im}(Z)} \qquad 4.8$$

where A is the device area (cm^2) and ω is the angular frequency of the applied ac signal.

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Chapter 5

High-performance ZnO transistors by spray pyrolysis

Abstract

In this chapter a very simple solution deposition method, namely spray pyrolysis (SP), is used for the first time to fabricate thin-film transistors employing ZnO as the transparent semiconductor. The role of the substrate temperature on the structural, optical, and electronic properties of ZnO thin films deposited by spray pyrolysis using a zinc acetate precursor solution is described. Both high and low voltage operation is demonstrated for ZnO based transistors utilising conventional (i.e. SiO_2) and unconventional (self-assembled organic monolayers), dielectrics, respectively. The electron mobility in these devices is found to increase with increasing deposition temperature across the range of 200-500°C. The maximum mobility and current on/off ratio is obtained from transistors fabricated using ZnO films deposited at > 400°C and are on the order of 25 cm^2/Vs and 10^6, respectively. Finally, dual-gate transistor operation is successfully demonstrated through the use of a solution-processed top-gate dielectric (i.e. CYTOP) in combination with a second gate electrode at the top. By combining these ZnO TFTs unipolar voltage inverters with maximum gain exceeding 25 are demonstrated.

5.1 Introduction

Research on solution-processible semiconducting materials is rapidly progressing towards the goal of providing viable alternatives to silicon-based technologies for applications where lower-cost manufacturing and new product features, such as mechanical flexibility and optical transparency, are desired. Organic semiconductors have been the subject of intense research over the past 20 years (1) and offer the prospect of low manufacturing cost combined with some desirable physical characteristics such as ease of processing and mechanical flexibility. Despite the impressive progress achieved in recent years, a number of obstacles including poor air-stability, device performance insufficient for a variety of applications and device-to-device variability, have to be overcome before the advantageous manufacturability and the economic benefits associated with organic semiconductors can be fully exploited.

While research in the area of organic materials and devices has been intensifying, a different class of semiconducting materials, namely metal oxide semiconductors also know as transparent oxide semiconductors (TOS), has emerged as possible alternative technology (2). Metal oxides incorporate important qualities that are currently absent from organic-based semiconductors. For instance, they generally exhibit higher carrier mobilities which are already sufficient for use in optical displays, such as current-driven organic light-emitting diode (OLED) based displays. An additional advantage of TOS relevant to many electronic applications is the superb optical transparency resulting from their wide bandgap. The latter makes oxide semiconductors particularly interesting for use in transparent electronics (3) as well as in backplanes for the next generation of current-driven displays (4, 5). However, for application in novel device concepts such as see-through electronics, transparent TFTs with higher switching speeds and low power consumption are required [Figure 5.1] (6).

So far, the opacity of amorphous silicon and the insufficient performance of organic semiconductors have impeded the development of high switching speed transparent TFTs (6). In this respect, TOS materials simultaneously fulfil the requirements for high optical transparency and high charge-carrier mobilities. In addition, they provide excellent chemical stability combined with superior mechanical robustness i.e. flexibility (7).

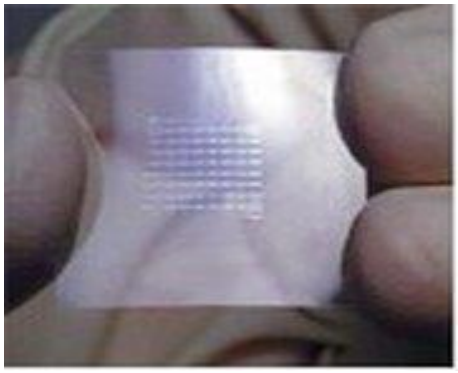

Figure 5.1. An array of transparent thin-film transparent fabricated on a flexible substrate (8).

A further advantage associated with TOS is the diverse range of techniques that can be employed for thin-film deposition (7). TOS are usually processed by vacuum based techniques such as molecular beam epitaxy (MBE) (9), sputtering (10-12), chemical vapour deposition (13), ion-assisted deposition (14-16) and pulsed laser deposition (PLD) (17). In recent years, vacuum based techniques have successfully been employed for the demonstration of indium oxide and indium-doped ZnO-based TFTs with electron mobilities of up to 140 cm^2/Vs (16) [31 cm^2/Vs for pristine ZnO TFTs (14)]. Despite the extraordinary device performance, however, vacuum based techniques suffer from high manufacturing cost and incompatibility with large area processing. In order to overcome this significant technology bottleneck research effort in recent years has been focussed on the development of alternative solution processing deposition methods including spin casting, dip coating and spray pyrolysis (18-23). Using these techniques TOS such as ZnO (18, 24-27), zinc tin oxide (ZnSnO) (28), indium zinc oxide (ZnO:In) (29-31), have been synthesised and used as the active layer in TFTs. A common and highly attractive aspect of solution-based approaches is that they combine simple and large-area compatible processing with potentially very high device performance.

Among the numerous metal oxide materials, ZnO (group II–VI) has attracted the most interest due to its exceptional physical properties. For example, it is a non-toxic semiconductor (32) and exhibits high electron mobility, excellent environmental stability and superior optical transparency (22) (bandgap ~3.3 eV, at

room temperature). Importantly, ZnO films can be prepared using various soluble precursor compounds with the most common one being the zinc acetate (ZnAc) shown in Figure 5.2. ZnAc is a widely available acetic salt with relatively low decomposition temperature that is highly soluble and capable of producing high quality polycrystalline ZnO films (24, 25, 33). This is rather important, since purity, size/size-distribution of the ZnO grain /crystals as well as the incorporation of organic species (i.e. contaminants) can lead to poor performance e.g. low carrier mobility (34).

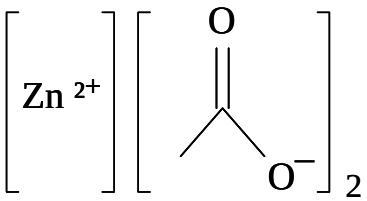

Figure 5.2: Chemical structure of the commonly used metal oxide precursor zinc acetate (ZnAc).

In this chapter the structural, optical and electronic properties of ZnO films grown by spray pyrolysis (SP) of a zinc acetate solution at different substrate temperatures, is studied using a range of techniques. The primary aim of this work is the elucidation of the growth mechanism of ZnO films and its impact on the electronic properties of thin-film transistors based on these films. To achieve this, a series of ZnO films were deposited at different substrate temperatures in ambient air. The film microstructure was investigated using a wide range of characterization techniques including AFM, X-ray diffraction, and UV-Vis spectroscopy. Finally, the electron mobility of the as-grown ZnO films was investigated using a carefully optimised bottom-gate (BG), top-contact (TC) as well as bottom-gate (BG), bottom-contact (BC) transistor architectures.

Another key finding of this work is the compatibility of SP with a number of solution-processible self-assembled monolayer (SAM) dielectrics. By combining SP with soluble SAM dielectrics, we are able to demonstrate ZnO transistors operating at voltages below |1.5| V and exhibit mobilities comparable to those obtained from SiO_2 based devices (24, 25, 33). Finally dual gate operation is also demonstrated by combining a solution processed organic dielectric CYTOP with the conventional SiO_2 gate dielectric at the bottom. Dual-gate transistors are then

combined to produce unipolar inverters with excellent operating characteristics that include high signal gain and wide noise margins.

5.2 Characterization of ZnO thin films deposited by spray pyrolysis

This section describes the results obtained from ZnO film characterization, employing different techniques. For these studies, ZnO thin films were deposited at various deposition temperatures by spray pyrolysis following an optimized deposition procedure, detailed in chapter 4. The films were deposited on SiO_2/Si and quartz/glass substrates for AFM and XRD measurements, respectively. Detailed descriptions of the experimental procedures are given in Chapter 4.

5.2.1 Thermal analysis of the precursor compound

The thermal properties of the zinc acetate were investigated using thermal gravimetric analysis (TGA) and differential scanning calorimetry (DSC) (Figure 5.3). Loss of surface-adsorbed and intercrystalline water molecules was found to occur at temperatures of about 100 °C. This resulted in negligible mass loss given the water free nature of the zinc acetate precursor used for this study.

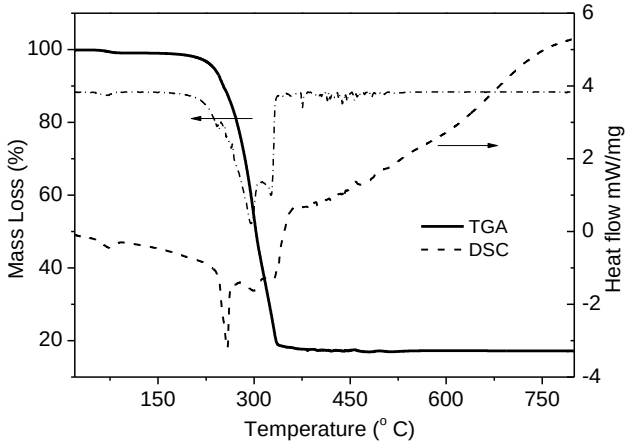

Figure 5.3. Thermo gravimetric analysis (left axis: weight loss% (solid line) and weight loss rate (dotted line) with temperature and differential scanning calorimetry (right axis) of 15 mg zinc acetate powder. TGA and DSC runs conducted under air and nitrogen respectively at a scan rate of 10 ° C/min. Courtesy of George Adamapolous.

In the temperature range of 180-350 °C a more pronounced weight loss is observed. The latter is attributed to the collapse of the intra-layer structure that

releases a variety of products that include acetic acid, acetone generated via ketonisation of acetic acid, water which may be generated via dehydroxylation of Zn-OH linkages, as well as carbon dioxide resulting from thermo oxidation of organic species (35-38). The evolution of CH_3CO_2H begins at about 205 °C and peaks at around 295 °C suggesting that the second stage of decomposition is mainly due to the loss of the acetate groups. This observation is further supported by differential scanning calorimetry (Figure 5.3, left y-axis) that also indicates that the precursor is fully decomposed at 350 ^oC resulting in polycrystalline ZnO. Earlier studies performed on similar acetic zinc salts using in-situ monitoring of the evolved gaseous products as well as ex-situ characterization of the residues showed similar evolution and precursor thermal behaviour (39-41).

5.2.2 X-ray diffraction characterisation of ZnO films

The XRD technique is commonly used to determine the crystalline quality and preferential orientation of the ZnO films. Figure 5.4(a) shows the X-ray diffraction patterns of room temperature, spray coated zinc acetate and spray pyrolysed ZnO films deposited on glass substrates at different temperatures. The pattern illustrates all the pronounced diffraction peaks for zinc acetate as well as for ZnO. The broad band that appears between 14.5^o and 38.5^o corresponds to the underlying glass substrate. The diffraction pattern of the film deposited at room temperature shows the (002) diffraction peak of the zinc acetate at 12°. However, the absence of any (00l) zinc acetate reflections at deposition temperatures above 100°C implies that zinc acetate phase in solution is thermally unstable even at temperatures as low as 100°C, probably due to the rearrangement of the acetate anions in the lattice sites. However, no ZnO is detected by X-ray diffraction in films grown below 200°C. Deposition of the precursor at temperatures above 200°C yields polycrystalline ZnO films. Deposition at temperatures in the range of 300-500°C yields the wurtzite structure as the dominant polycrystalline phase with preferential orientation along the (002) direction. Moreover, no peak for ZnO-related compound such as ZnO_2 could be identified, indicating that the crystalline parts of these films consist of the pure ZnO.

The evolution of the average size of the ZnO crystallites, determined from the width of the (002) reflection at 34.5° using the Scherrer formula, as a function of deposition temperature is displayed in Figure 5.4(b).

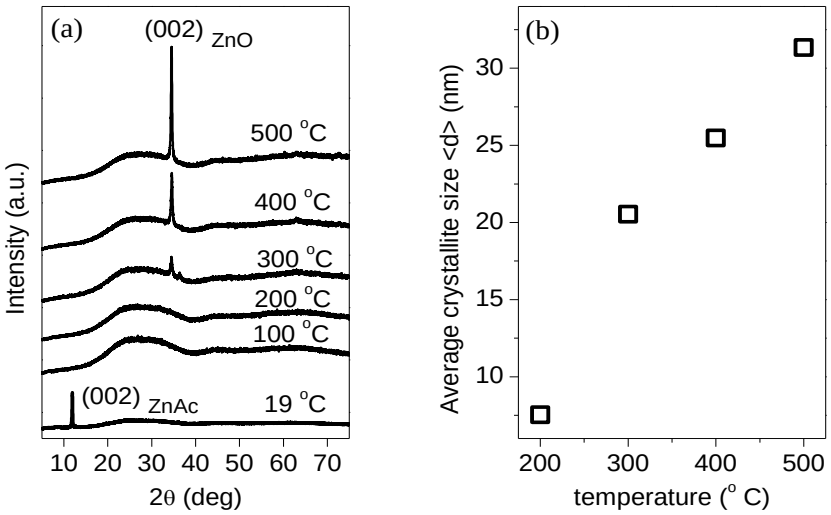

Figure 5.4: a) X-ray diffraction patterns, and b) average ZnO crystal size calculated from the (002) diffraction peak of ZnO films sprayed on glass substrates using zinc acetate solutions at substrate temperature in the range of 19-500 °C. Courtesy of Mohamed Bakler.

The crystallite size increases with temperature from 7.5 nm to 32 nm within the temperature range between 200-500 °C. Relative intensities of the (002) ZnO reflection exhibit a propensity for growth in the < 002 > lattice direction, perpendicular to the substrate. Preferential growth of ZnO along the < 002 > lattice direction has also been reported previously using other deposition methods (22, 42).

5.2.3 Atomic force microscopy of ZnO films

The surface properties of zinc acetate/ZnO films fabricated on Si/SiO_2 substrates were investigated by AFM. The recorded phase and topography images are depicted in Figure 5.5. The images presented are the tip dilation effects processed images obtained over 1 μm × 1 μm scanning range. AFM images reveal good quality smooth films when grown by spray pyrolysis at temperatures above 300 °C. The surface roughness of the ZnO thin film was calculated in terms of root mean square (rms) using appropriate AFM software (43). The latter is estimated to increase monotonously from 0.5 nm to 2.9 nm for deposition temperatures between

200-500 °C. However, a disordered grain and mixed phase material unevenly distributed was found for films deposited at substrate temperature of 200 °C. Both phase and topography images indicate an increase of the grain size with deposition temperature. The grain sizes that are shown inset the AFM images were obtained by processing (44) the phase images. Such a trend has been previously reported for ZnO films deposited by pulsed laser deposition (PLD) (45, 46) and is believed to be related to the mobility and diffusion of the ad-atoms on the substrate surface. At low deposition temperatures (100-200 °C) the diffusion and mobility of ad-atoms on the substrate surface is low preventing the ad-atoms arriving at the correct lattice site resulting in the formation of an amorphous structure.

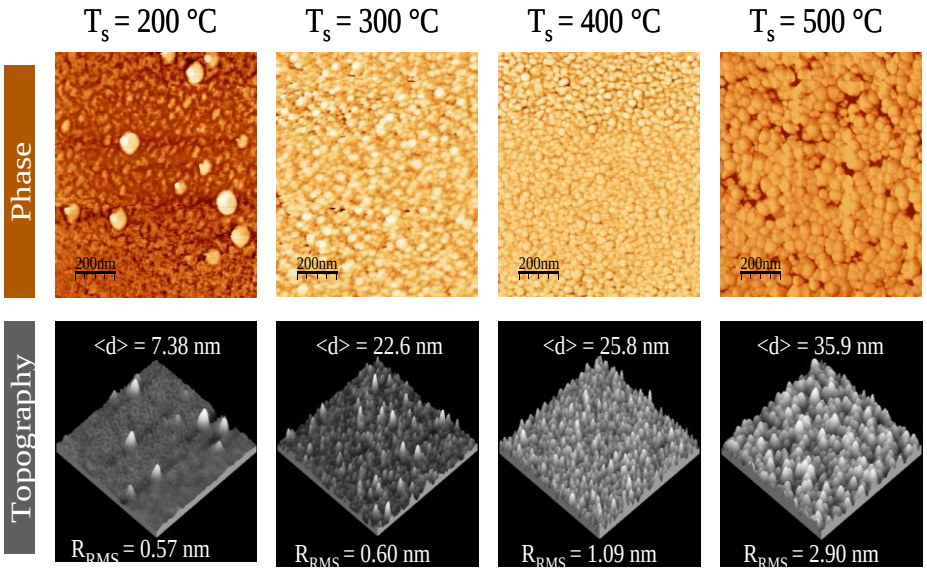

Figure 5.5: AFM phase (top) and topography (bottom) images of ZnO films deposited at substrate temperatures in the range of 200-500 °C. Here T_s indicates the substrate temperature during deposition, < d > the average size of the ZnO crystallites, and R_{RMS} the surface roughness of the film. Both are evaluated from AFM measurements. Courtesy of Jeremy Smith.

As the substrate temperature increases (300-500 °C) the mobility and diffusion of the ad-atom increases and hence prevents ZnO agglomeration into large amorphous particles. The latter leads to the formation of larger crystalline domains with enhanced preferential crystallographic orientation.

5.2.4 Optical transmission spectroscopy of ZnO films

The UV-Vis transmission spectra of zinc acetate/ZnO films grown on quartz are shown in Figure 5.6. The spectra clearly demonstrate that the optical transmittance near the band edge of the onset of the optical transitions of the sprayed films decreases with increasing the deposition temperature. Moreover, appearance of excitonic features i.e. small peak near the band gap energy for films deposited at 400-500 ^{o}C also confirms the excellent quality of the films at higher temperatures.

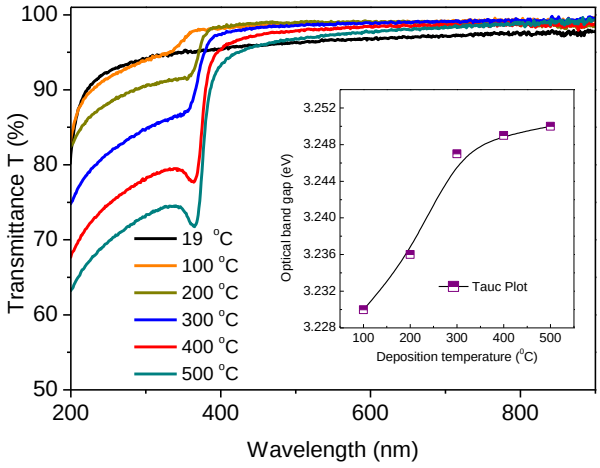

Figure 5.6: Optical transmission (%) spectra of ZnO films (30–40 nm) sprayed onto quartz substrates at temperatures in the range of 19–500 ° C. Inset: Evolution of the optical bandgap of ZnO films, grown at different temperatures, obtained using Tauc plots.

The graph inset shows the optical band gap obtained independently by the Tauc plots (47) and clearly indicates that the change in deposition temperature slightly affects the film's optical band gap. Note that the values for the optical band gap obtained here differ from the 3.37 eV optical band gap at room temperature of polycrystalline ZnO. There are two reasons for that. 1) The values are obtained from a linear fit so the excitonic effects or low energy absorption/transmittance are excluded which may pose an error in the analysis. 2) This can also be attributed to the valence band-donor transition at 3.15 eV which contributes to the absorption spectrum (48). Also, We note that the band gap dependence on crystal size shows the opposite trend when compared to some earlier data (49, 50) reported for grain sizes > 20 nm.

5.3 ZnO transistors using SiO_2 as gate dielectric

5.3.1 Device fabrication

To investigate the suitability of the SP method for the fabrication of functional devices, we have fabricated a number of ZnO transistors employing different device architectures. First, ZnO TFTs fabricated on doped silicon (S_i^{++}) wafers, also acting as the common gate electrode, incorporating thermally grown layer of SiO_2 as the gate dielectric. The bottom-gate, top-contact (BG-TC) transistor architecture was completed with the evaporation of Al S-D electrode by thermal sublimation under high vacuum using a shadow mask. For the bottom-gate, bottom-contact (BG-BC) transistors, Au S-D contacts were patterned using standard photolithographic techniques directly onto SiO_2. The SiO_2 surface was passivated using vapour deposited hexamethyldisilazane (HMDS). Films of ZnO were then deposited by SP at different substrate temperatures (T_s). The schematic structures of these transistors are presented along with their respective device characteristics in the Section 5.3.2. Electrical characterization was performed in air at room temperature (~20°C) and in the dark.

5.3.2 Current-voltage characteristics of ZnO transistors

A representative set of the transfer and output characteristics for an optimised BG-TC transistor with L = 20 μm and W = 1000 μm, based on ZnO film sprayed at 400°C is shown in Figure 5.7. The TFT architecture is shown as an inset in Figure 5.7(b). The transistor operates in the n-type mode and exhibits hard saturation. It is noticed that drain currents of 1 μA can be achieved with voltages substantially below 10 V. Furthermore the TFT exhibits high on-off current ratio that approaches 10^6. In the saturation mode, an electron mobility of ~23 cm^2/Vs and a threshold voltage V_T ~ 3 V, are extracted using the saturation current equation derived in Section 3.4.2. From log I_D versus V_G plot, the subthreshold slope (SS) is estimated to be approximately 3.2 V/decade. A similar set of characteristics obtained from a BG-BC transistor based on ZnO film deposited at T_S = 400°C employing gold S-D electrodes, is presented in Figure 5.8. It should be noted that transistor operation is not only observed for ZnO films grown at 400°C but also for temperatures in the range 200-500°C. Table 5.1 summarizes the performance parameters of these ZnO transistors.

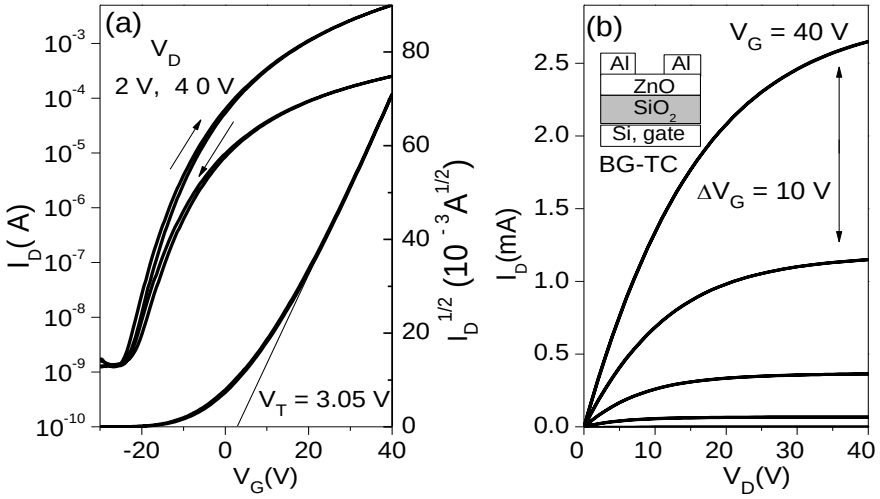

Figure 5.7: (a) Transfer and (b) output characteristics obtained from a BG–TC (see inset) transistor (L/W = 20/1000 μm). The ZnO layer was deposited by SP in air at T_S = 400 ^oC. Hysteresis free characteristics are evident.

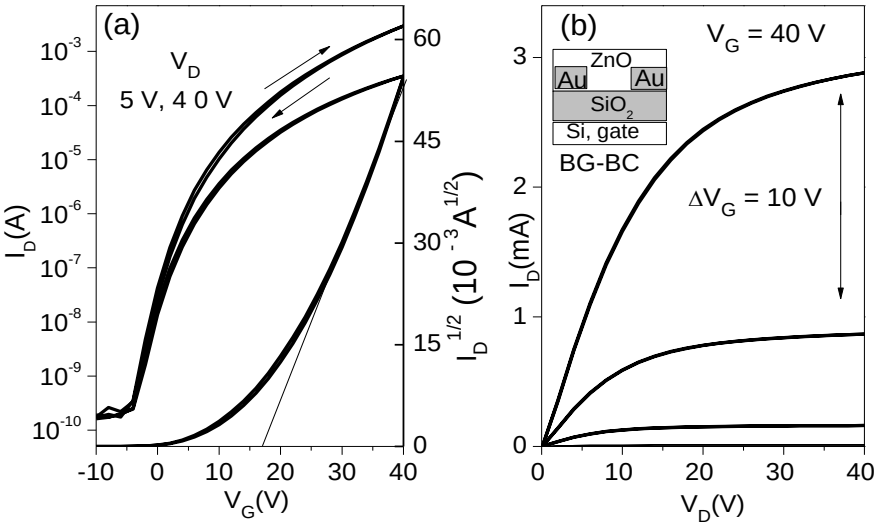

Figure 5.8. (a) Transfer and (b) output characteristics obtained from a BG–BC (see inset) transistor (L/W = 15/10000). The ZnO layer was deposited by SP in air at T_S = 400 ^oC. Excellent hysteresis free characteristics are evident.

In general, all devices exhibit hysteresis free characteristics with current on/off ratios and threshold voltages in the range of 10^3-10^7 and 2-20 V, respectively. A further general observation is that the electron mobility (extracted

in the saturation regime for both transistor configurations), increases with increasing deposition temperature, in agreement with earlier reports (51, 52). Such an increase can be attributed to the improved crystallinity of ZnO films, (23) and is consistent with the increased surface roughness seen in the AFM images (Figure 5.5). Improved crystallinity is expected to yield larger domains and fewer grain boundaries in the ZnO films, both of which should lead to an increase in electron mobility with increasing processing temperature.

Another interesting observation is the lower mobility values obtained from the BG-BC ZnO TFTs for all channel dimensions. The effect is attributed partly to the significant energy offset present between the Fermi level of the gold S/D electrodes (E_F = 5.1 eV) and the conduction band of ZnO (~ 4.4 eV) (this offset is much less pronounced in BG-TC devices, where aluminium with a work function of 4.2 eV is employed), and partly to the different injection electrode geometry between the BG-BC and BG-TC device architectures.

T_S (^oC)	V_T (V)	μ_{SAT} (cm^2 /Vs)	On-off ratio	S (V/ dec)
BG-TC using Aluminium S/D electrodes (L= 20- 60 μm, W= 1000 – 2000 μm)				
200	15.5	0.34	10^3	4.19
300	11.4	7.85	10^4	4.72
400	3.05	23.4	10^6	3.17
500	12.5	25	10^6	3.58
BG-BC using gold S/D electrodes (L= 10- 15 μm, W= 10000 – 20000 μm)				
200	16.4	0.15	10^5	1.28
300	14	1.08	10^6	1.87
400	17.6	1.65	10^7	1.92
500	17.7	1.31	10^7	1.41

Table 5.1. Summary of the performance parameters of BG-TC and BG-BC ZnO transistors based on SiO_2 dielectric for different T_S. These are typical values representative of characteristics of a group of ~ 100 devices prepared for each set of conditions.

In addition to the energy offset, Gopel et al. also demonstrated that the Schottky barrier at the nonreactive Au-ZnO interface is qualitatively different from

that of the rather reactive Al-ZnO interface (53). In the latter case, Al could affect the stoichiometry of ZnO at the interface and hence the charge-transport/-injection mechanisms. Further work related to the injection mechanism, for each device geometry and material combination is presented in Section 5.3.3.

As can be seen (Table 5.1) the highest mobility of approximately 25 cm^2/Vs is obtained from BG-TC ZnO TFTs fabricated at 500°C. Both the mobility and the current on-off ratio (~10^6) obtained here compares favourably with some of the highest mobility values reported in the literature for ZnO transistors prepared by sophisticated deposition methods such as sputtering, (3, 14, 16, 54), PLD, (55) ink-jet printing, (56) ALD (57) and MOCVD (13). It is to be noted that the set of values given in Table 5.1 represent typical device characteristics out of a group of ~100 devices measured for each set of deposition temperatures. Each of the evaluated parameters exhibited a distribution in values for both BG-TC and BG-BC configurations and also at all deposition temperatures. It can be attributed to the manual spray deposition of ZnO film.

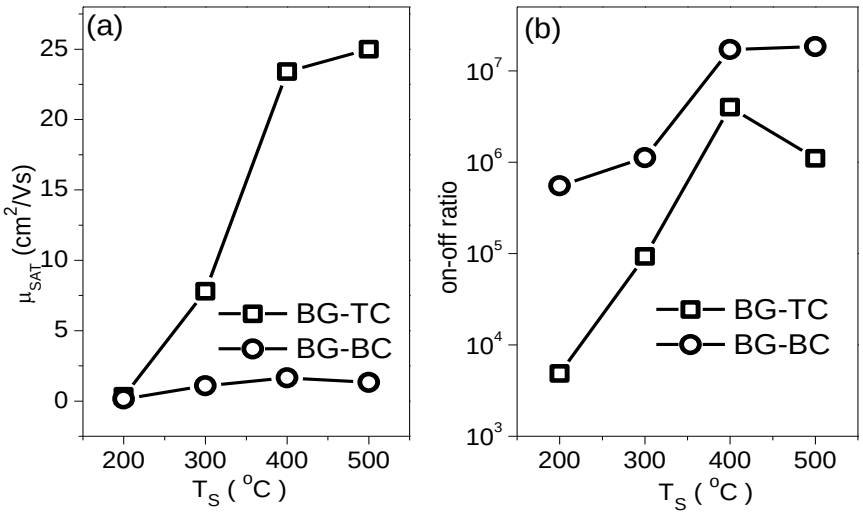

Figure 5.9. a) Electron mobility calculated in saturation, and b) current on/off ratio as a function of deposition temperature (T_S), obtained from ZnO TFTs (BG-TC and BG-BC) prepared at different substrate temperatures (200-500°C).

Mobility and threshold voltage for BG-TC exhibited a spread of 0.01-0.34 cm^2/Vs and 12-16 V for devices fabricated at 200 ^oC. At 300 ^oC, the former varied between 4-7.8 cm^2/Vs and the latter between 10-13V. For higher deposition

temperatures such as 400 ^{o}C and 500 ^{o}C, the spread in these values was less pronounced and was found to be only 20-23 cm^2/Vs, 3-5V and 22-25 cm^2/Vs, 11-13 V respectively. While the current on-off ratio and SS were quite consistent from device to device for all deposition temperatures. BG-TC transistors also showed similar trend.

The evolution of the electron mobility and current on/off ratio obtained from a number of ZnO TFTs prepared at different temperatures are displayed in Figure 5.9. From this figure a drastic improvement in the device performance coinciding with increasing deposition temperature is evident. Finally, despite the indication of the formation of some crystalline ZnO at temperatures as low as 100°C (from UV-Vis data), we have been unable to find a working transistor based on ZnO films grown at or below 100°C.

5.3.3 Effect of metal electrodes on parasitic contact resistance

A thorough analysis on ZnO TFT should include the extraction of TFT source/drain series resistance, the contribution of which cannot easily be separated from TFT characteristics. The total series resistance (R_T) is a combination of contact resistance (R_C) due to the metal semiconductor interface and the channel resistance, particularly for a staggered TFT where the carriers need to travel through the bulk of the semiconductor layer to the channel region. This section focuses on the analysis of the parasitic contact resistance utilising the scaling law method described in Chapter 3, Section 3.4.6. Specifically, we have systematically studied the effect of S-D electrode work function and its relation to R_C, which was determined by analysing a series of TFTs with the same channel width (1 mm) and varying channel lengths (20-100 μm) fabricated simultaneously under the same conditions. For this analysis we have chosen ZnO transistors fabricated at T_S = 400°C on Si^{++} substrates employing the BG-TC architecture and utilising three different metal electrodes (Al, Au, Ca) as the S-D electrodes.

The calculated R_T is plotted as a function of various channel lengths (L) for different V_G, and then linear fitting of the data is performed. Figure 5.10(a) illustrates the evolution of R_T against L as a function of V_G, extracted for ZnO TFTs based on Au S/D electrodes. It is shown that as V_G increases, R_T decreases due to the increase of the channel carrier density. The extracted R_C and channel

resistance (R_{ch}) are shown in Figure 5.10(b). It is evident that R_C is strongly V_G dependent.

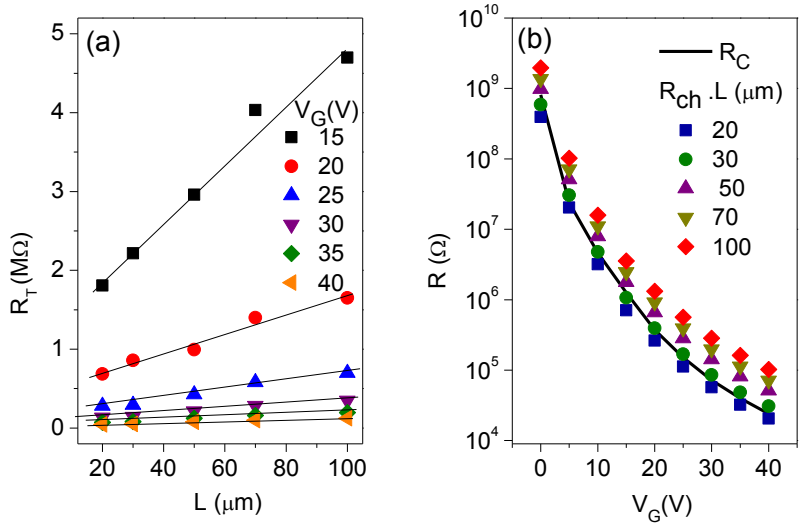

Figure 5.10. Contact resistance data obtained from ZnO TFTs based on Au S-D electrodes. a) Total resistance (R_T) versus channel length (L) extracted from the linear output curves (W is kept constant). b) Contact and channel resistance is plotted against V_G.

Figure 5.11 displays the ratio of R_C to R_T, clearly demonstrating the significant role of the R_C. In particular, the R_C /R_T at V_G = 10 V increases from 23% to 54%, when channel length decreases from 100 μm to 20 μm. The same trends of R_C/R_T at other V_G are observed.

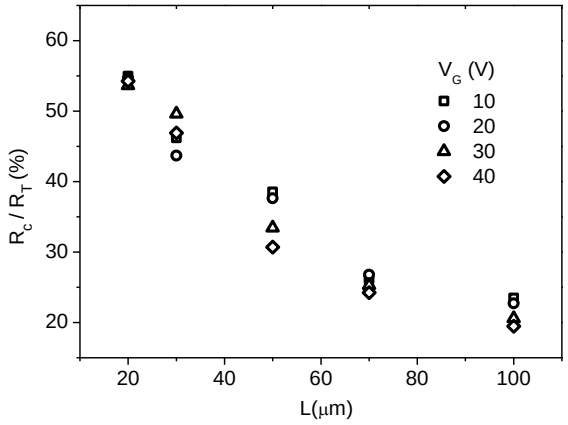

Figure 5.11: Ratio of R_C to R_T as a function of L evaluated at different V_G.

Due to the increasing portion of R_C as the channel length decreases, it is clear that a significant part of the externally applied voltage (V_D) drops across the contact regions rather than the transistor channel itself thereby affecting, in a negative way, the carrier mobility i.e. the transistor performs worse. The effect is pronounced for short channel devices since smaller R_{CH} makes the voltage drop across the contacts larger (58, 59).

Following the same procedure the contact resistance for ZnO TFTs based on three different metal S-D materials namely Al, Au, and Ca, has been calculated. These data are shown in Figure 5.12(a) (24). As can be seen, Ca yields the lowest contact resistance while Au yields the highest. Using the work functions values for Au ~ 5 eV, Al ~ 4.2 eV, and Ca ~ 3 eV from the literature, and assuming a value for the conduction band (CB) of ZnO at 4.3 eV, the R_C trend can be explained on the basis of the simplified energy diagram shown in the inset of Figure 5.12(b).

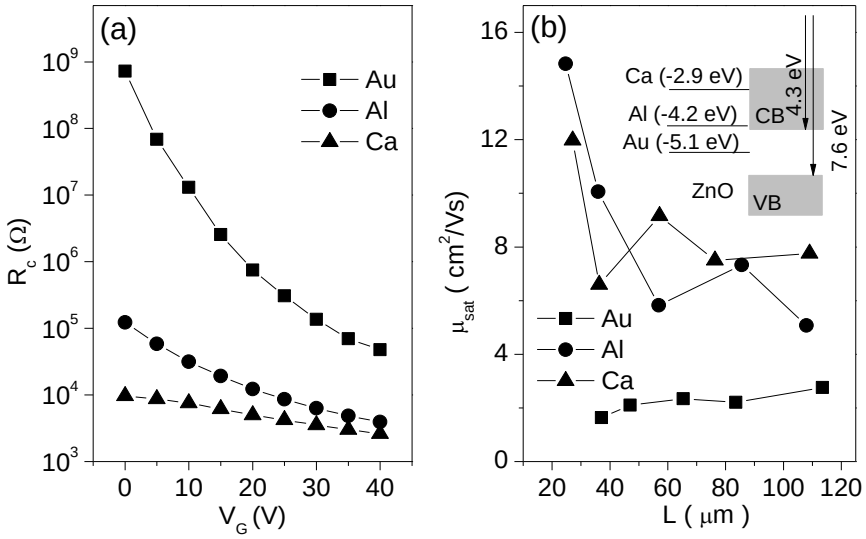

Figure 5.12. a) Contact resistance (R_C) as a function of gate bias for ZnO TFTs employing three different materials namely Ca, Al, Au as S-D electrodes. Inset: Simplified energy diagram between Au, Al, Ca, and ZnO. b) Electron mobility calculated in saturation is plotted against channel length (L) for Ca, Al and Au S-D electrodes. All measurements were performed in nitrogen due to the sensitivity of Ca electrodes to atmospheric oxidants.

Evidently Au results in a large energy barrier ~0.7 eV for electron injection to the CB of ZnO. This is possibly the reason for the large contact resistance,

particularly at low V_G. In the case of Al the potential barrier is close to 0 eV if one neglects surface states at the surface of ZnO and possible oxidation of the Al electrode upon contact with ZnO. ZnO Transistors based on Ca S/D electrodes exhibit the lowest contact resistance, which is weakly dependent on V_G. The latter observation is in agreement with the expected behaviour from the energy diagram of Figure 5.12 (b).

The electron transport in ZnO TFTs has also been studied as a function of transistor channel length (L) under N_2. Figure 5.12(b) displays the dependence of the electron mobility obtained from several ZnO TFTs, calculated in saturation, versus L. Two interesting features can be identified. The first is the positive dependence of electron mobility with increasing *L* for TFTs comprised of injection limiting Au S/D electrodes. This effect is attributed to the large R_C that tends to dominate charge transport at short channel lengths [see Figure 5.11]. As L increases, R_C becomes smaller than the channel resistance [Figure 5.10(b)] and the effective mobility increases. Hence charge transport is dominated by electron transport in the ZnO film rather than electron injection from Au. The situation is different for ZnO TFTs based on Al and Ca S/D electrodes. In both cases short channel TFTs exhibit improved performance as compared to long channel devices. The latter observation is attributed to grain boundary effects that tend to dominate charge transport in TFTs with $L > 40$ μm. The shorter the channel the fewer grain boundaries the charges have to cross and hence the larger the effective mobility. As L increases the number of grain boundaries encountered by the electrons increases, and since they introduce states that can trap electrons hence reduction in the effective carrier mobility is observed. One interesting implication of this finding is that fabrication of ZnO transistors with Ohmic contacts (i.e., Al or Ca), and $L < 20$ μm could eventually yield devices with even higher electron mobilities.

5.3.4 Unipolar voltage inverters based on ZnO transistors

In order to demonstrate the potential of this technology for practical electronic applications we have fabricated unipolar voltage inverters, commonly known as the logic NOT gate, utilising n-channel ZnO TFTs (60-63). It should be noted that fabrication of complementary logic is currently very challenging because of the unavailability of p-type oxide semiconductors. Instead, unipolar logic based solely on n-type channel TFTs is one strategy for building oxide circuits. Currently,

significant effort has been focussed on optimisation of the performance of such unipolar inverters. For example, the V_T of the driver and load TFTs or the channel resistance of the load TFT have been studied as important adjustable parameters for the n-channel inverter due to the fact that such adjustments can accurately determine the transition voltage of the voltage transfer characteristics (VTC) of an inverter (63-65). Currently, choosing different width-to-length (W/L) ratios for load and driver TFTs (60-62) is the most commonly employed approach to control the transition voltage.

To demonstrate functional logic inverters we have integrated two n-channel ZnO TFTs with different V_T, chosen from different substrates but fabricated under similar conditions, to fabricate high gain NOT gates employing the depletion load configuration shown in Figure 3.10 (c). Figure 5.13(a) represents the static VTC performance of the inverter. The circuit is fully functional at supply voltages of V_{DD} = 40, 50, and 60 V and exhibits negligible operating hysteresis. The voltage gain, given by $-dV_{OUT}/dV_{IN}$, is high with maximum values close to 25 measured at V_{DD} = 60 V [Figure 5.13(b)]. The trip voltage at this V_{DD} is 40 V, slightly higher than the ideal value of $V_{DD}/2$ = 30 V.

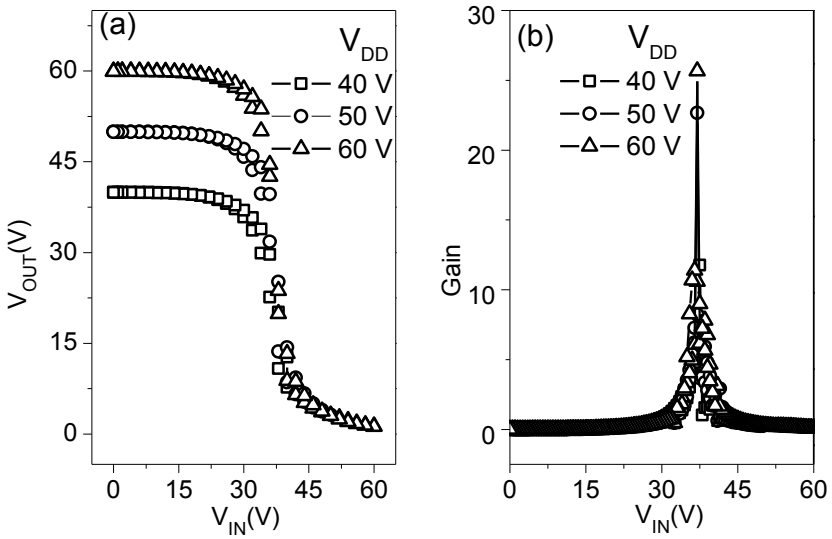

Figure 5.13: a) Output characteristics of unipolar voltage inverter constructed of ZnO TFT. Load TFT were chosen to has V_T = 13.5 V which was less than that of driver TFT with V_T = 23 V. The two TFTs belonged to different substrates but fabricated under similar conditions. b) Signal gain during inverter operation.

Another important circuit parameter is the noise margin (NM). A high NM is usually required as it makes the inverter more tolerant to signal fluctuations in circuit applications. The inverter's NM depends on the V_T and SS of the individual transistors used. Using the data from Figure 5.13 the NM of the inverter was calculated yielding a value close to 19 V (V_{DD} = 60 V). The latter is very high as compared to previous reports and represents 63% of the maximum limit achievable i.e. $V_{DD}/2$.

Similar unipolar circuits have been reported by Ofuji et al. (61) using IGZO based TFTs. They reported a gain of - 1.7 measured at a V_{DD} = 18 V. Similarly, Presley et al. (60) reported a gain of 1.5 V/V at V_{DD} = 30 V for an IGO based inverter circuit. More recently, and employing a depletion load unipolar inverter circuit based on ZTO TFTs, Wager et al. reported a signal gain of 10 at the much reduced supply voltage of V_{DD} = 10 V. Despite the fact that the unipolar NOT gates realised here exhibit high gain at relatively high V_{DD}, our results demonstrate the potential of this simple manufacturing technology for application in high performance electronic circuits.

5.4 Low-voltage ZnO transistors based on self-assembled nano-dielectrics

5.4.1 Introduction

The vast majority of the reported transistors/circuits based on transparent semiconductors whether organic or inorganic operate at relatively high voltages which typically exceed 20 V. This appears to be a drawback when it comes to the battery powered and/or portable applications that require much reduced operating voltages e.g. below 5 V. A possible solution to the problem is to use thinner gate dielectrics since the capacitance of the gate dielectric (C_i) is inversely proportional to the dielectric thickness (d) given as:

$$C_i = \frac{k.\varepsilon_o}{d}. \qquad 5.1$$

This idea has been successfully implemented by employing ultra thin layers of molecular self-assembled monolayers (SAMs) as gate dielectrics. The high geometrical capacitance of the SAM layers makes the accumulation of high charge carrier densities possible at significantly reduced gate voltages. Here, we

have employed octadecylphosphonic acid (ODPA) as a SAM gate dielectric (66). The ODPA SAM was functionalized onto oxidized aluminium gate electrodes following the well-established procedures reported elsewhere (66). As already mentioned the majority of reports on ODPA SAMs relate to organic TFT (67-70). It is only recently that oxide semiconductors have been combined with SAM layers in order to produce low operating voltage TFTs (71, 72).

In our effort to reduce the operating voltage and hence the overall power consumption of our ZnO TFTs fabricated by SP, we have incorporated the ODPA SAM dielectric to produce low voltage, high mobility transistors. The effect of deposition temperature on the SAM integrity and device performance was also analysed. By combining two low voltage ZnO TFTs, low-voltage unipolar inverters have also been demonstrated.

5.4.2 Self-assembled monolayer dielectrics and transistor fabrication

Aluminium gate electrodes (30 nm) were thermally evaporated onto precleaned glass substrates using shadow masks followed by oxidation in oxygen plasma. The ODPA SAM dielectric was deposited by drop casting. Details of the procedure are given in Chapter 4. The molecular structure of ODPA is displayed in Figure 5.14(a). Contact angle measurements were performed on Al- AlOx surfaces before and after SAM treatment. Figure 5.14(b) displays images of a water droplet on the oxidized aluminium surface. Upon treatment of the Al-AlO_X electrode with the ODPA SAM [Figure 5.14(a)], the water contact angle (θ_C) changes from <40° to >105°, clearly indicating the presence of the hydrophobic ODPA layer. Water contact angles in excess of 100° are typical for methyl-terminated SAMs (66, 73). Moreover annealing the sample at 400°C does not appear to remove ODPA as confirmed by the contact angle measurements [Figure 5.14(a)]. This implies that the SAM dielectrics can be employed for high temperature deposition as the phosphonic acid groups binds very strongly onto AlOx while the insulating alkyl chain does not decompose upon annealing.

Finally, the surface energy characteristics of the Al-AlO_X-ODPA surface were also analysed by surface energy measurements using three liquids with known polar and dispersive components. Contact angles of distilled water, diiodomethane, and ethylene glycol were calculated to be 107°, 68° and 85°, respectively. The Al-AlO_X-ODPA surface exhibits a low polar and highly

dispersive surface energy as evident from the low polar (0.24 mN/m) component and the large dispersive component (23 mN/m).

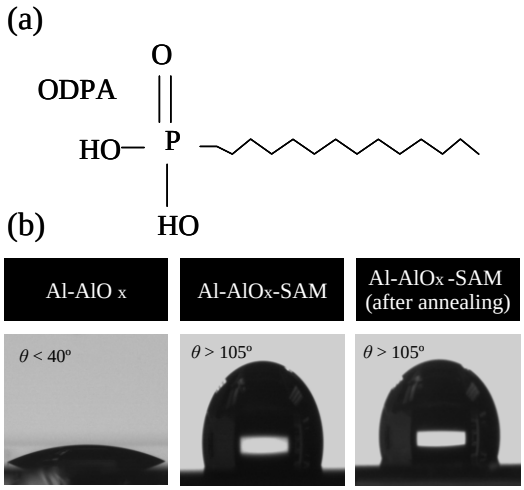

Figure 5.14: a) Molecular structure of octadecylphosphonic acid (ODPA). (b) Water contact angle on Al-AlO_X electrode before and after treatment with ODPA and finally after thermal annealing at 400°C. Annealing was performed for 5 min in N_2 atmosphere and did not induce any change in the contact angle.

The presence of the SAM layer was also confirmed by current-voltage (J-V) measurements using metal-insulator-metal (MIM) structures. The corresponding data is shown in Figure 5.15. It can be seen the current density (J) between the two metal electrodes reduces dramatically upon SAM functionalization (~10^{-7} A/cm^2 measured at ±1 V). The latter corresponds to an electric field of >1 MV/cm assuming an overall thickness (i.e. AlO_X + ODPA) of <10 nm. For comparison, similar leakage current densities at a similar electric field strength have been reported for 50 nm thick polymer dielectrics (74) as well as 100 nm SiO_2 on Si (75).

The geometric capacitance of the SAM dielectric was measured to be in the range of 500-700 nF/cm^2. These results are in good agreement with data reported in the literature (66, 69). This value for C_i is orders of magnitude higher than the one obtained from the 200 nm thick SiO_2 (17 nF/cm^2) and the 1 μm thick CYTOP (2 nF/cm^2) dielectrics. The latter is discussed later. It is therefore expected to have a dramatic effect on the operating voltages of the ZnO transistors.

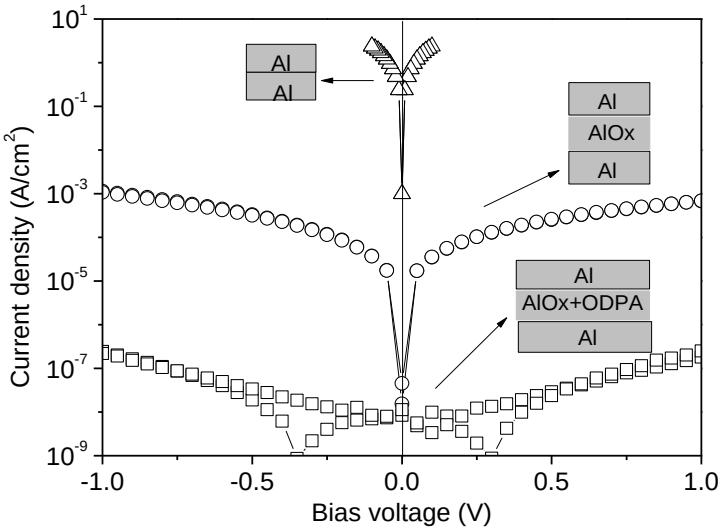

Figure 5.15: Current density as a function of voltage measured at different stages of the device fabrications. Significant reduction in leakage current can be observed when SAM layer is introduced.

5.4.3 Metal-insulator-semiconductor capacitors based on ZnO and SAM dielectric

Once the insulating properties and the exceptional thermal stability of ODPA SAMs have been established, we attempted to fabricate low-voltage metal-insulator-semiconductor (MIS) capacitors in order to further evaluate the dielectric properties of ODPA as well as investigate the electronic characteristics of the ODPA/ZnO interface employing the capacitance-voltage (C-V) method. To achieve this, MIS capacitors were fabricated employing spray pyrolysed ZnO films and ODPA monolayers as the semiconductor and the dielectric layer onto glass substrates. The schematic structure of the device is shown as an inset in Figure 5.16(b). The ZnO film was deposited by SP at 400°C. The C-V measurements were performed with devices under nitrogen atmosphere using a Keithley semiconductor parameter analyser, and by applying a small (30 mV peak-to-peak) oscillating ac voltage superimposed onto a DC voltage with frequency in the range 3-100 kHz. The DC bias voltage was applied across the bottom and top Al electrodes and was swept from -2 V to +2 V.

The geometric capacitance (C) as a function of applied bias and frequency is shown in Figure 5.16(a). The C-V curves clearly exhibit the high and low capacitance values for positive and negative DC bias i.e. for accumulation and depletion regions, respectively. These measurements confirm the n-type behaviour of the ODPA/ZnO interface. Moreover a single value for the minimum capacitance (C_{min}) could not be found within the DC voltage range investigated.

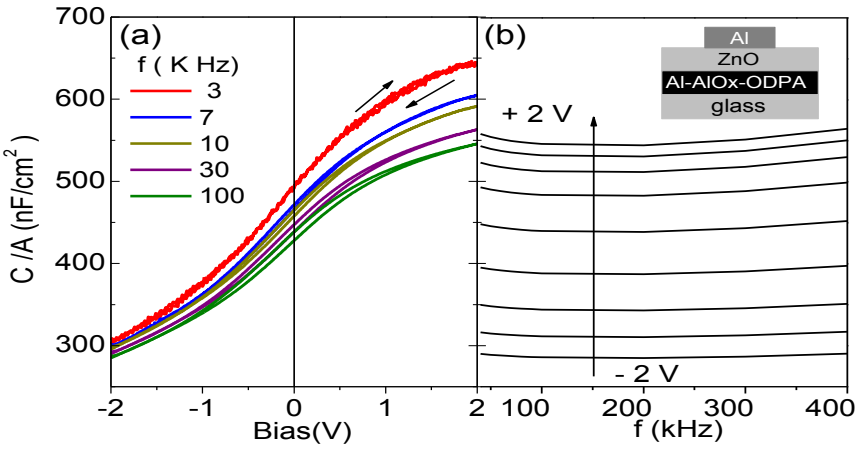

Figure 5.16. a) C-V characteristics of ZnO based low voltage MIS capacitor using SAM as a dielectric. Area (A) of the capacitor is 0.0025 cm^2. b) C-*f* characteristics of the same device are shown, with the inset representing the device architecture. Frequency is swept from 3 kHz to 400 kHz.

The C-V curves were stretched out along the voltage axis which implies a rather large interface state density but show no hysteresis with increasing frequency. Hysteretic behaviour in C-V curves is typically caused by slow charge trapping of injected charges and/or migration of mobile ions into the insulator. The exact origin of such hysteretic behaviour is usually speculated by its direction where for the n-type capacitors, a clockwise hysteresis implies that the dominant origin is mobile ions within ZnO.

The frequency dispersion in accumulation is usually attributed to the formation of an inhomogeneous layer at the interface. The capacitance of such a layer acts in series with the insulator capacitance causing frequency dispersion of capacitance in the accumulation. Moreover, the contacts in this MIS structure were not patterned so lateral contribution to the conduction at the electrode edge due to parasitic effects particularly for bottom contacts may also be responsible for this

dispersion (76). The effect is more pronounced at low frequencies and can be eliminated with a proper choice of mesa structure for contact alignment with patterned semiconductors (76). The frequency dispersion in depletion region is due to the presence of interface traps (77). In order to understand better the nature of the ODPA/ZnO interface, the density of trap states (N_t) at the interface was calculated directly from the data in Figure 5.16(a) using the relationship:

$$N_t \approx \left[C_i \left(\frac{\Delta V}{q} \right) \right]. \qquad 5.2$$

Here, C_i is the gate insulator capacitance, q the elementary charge and ΔV the width of hysteresis. The value of charge trapping for this MIS capacitor is calculated to be approximately 2.81×10^{10} cm^{-2}. This value is an order of magnitude lower than the values reported for ZnO interfaces with other insulators. The origin of such traps could be the plasma ashing performed as part of fabricating SAM layer (77) and/or interface damage induced during the ZnO deposition by spray pyrolysis. Figure 5.17(a) shows the normalized *C-V* characteristics relative to the accumulation capacitance values of the MIS capacitors shown above. C_{min}/C_{max} in the depletion region is approximately equal to 0.51 and is slightly smaller than the recently reported value 0.86 and 0.7 for the same ZnO thickness (40 nm) employing AlO_x as the insulator (78, 79).

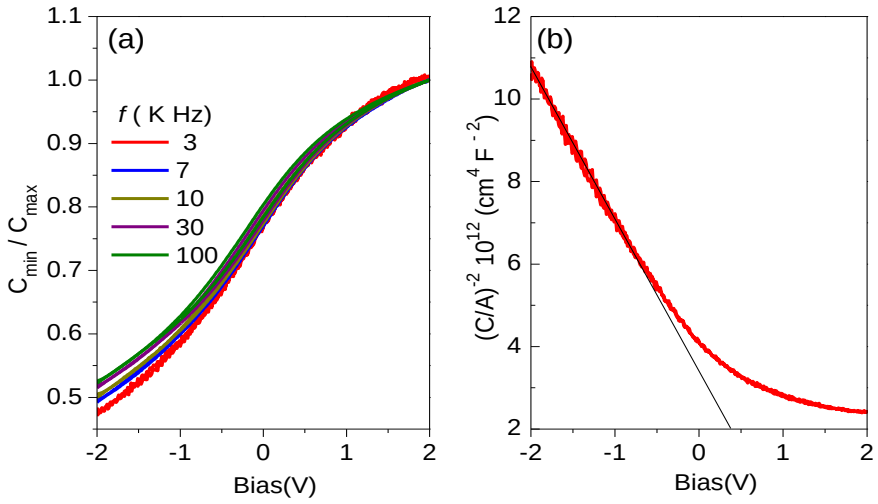

Figure 5.17. a) Normalised C-V characteristics of ZnO MIS capacitor at various frequencies. b) $1/C^2$ plot for calculating carrier density in the depletion region of ZnO taken at 3 kHz.

This smaller value can be attributed to the following factors: i) hybrid nature of the insulator (AlOx+ODPA) employed in this work, ii) exact thickness of the AlO_x along with its capacitance was not possible to evaluate, and iii) accumulation capacitance (C_{max}) is quite high when compared to other insulators. Since the C_{max} of the MIS capacitors corresponds to the gate-insulator properties, the MIS device resulted in the same maximum capacitance as measured from the MIM structures previously. In the depletion region of a MIS capacitor, effective capacitance results from a series combination of gate-insulator capacitance (C_i) and capacitance of the semiconductor depletion layer (C_{SD}). Therefore, the capacitance in the depletion region for an MIS capacitor with active area (A) can be used to calculate the carrier density in semiconductor using the MOSFET equation given as:

$$\frac{d\left(\frac{C}{A}\right)^{-2}}{dV} = \frac{2}{q\varepsilon_s\varepsilon_o N_D} \qquad 5.3$$

here, ε_0, ε_S are the permittivity of free space and semiconductor respectively. N_D is the carrier concentration of the semiconductor, respectively. The C^{-2} versus applied bias plot for a frequency of 3 kHz is shown in Figure 5.17(b). From the slope of this curve we can calculate a value of $N_D = 4.6 \times 10^{17}$ cm^{-3}. The latter is in good agreement with the carrier density of ZnO thin films. Moreover the flat band voltage found from the C-V curve is approximately 0.37 V. The latter can be correlated with V_T obtained from low-voltage ZnO TFTs discussed in the following section.

5.4.4 Low-voltage ZnO transistors based on SAM dielectrics

Low-voltage ZnO transistors based on ODPA SAM dielectrics have also been fabricated in order to evaluate the suitability of this technology for practical electronic applications. The typical device schematic employed is shown in the inset of Figure 5.18(b). A set of representative transfer and output characteristics is also shown in the same figure. The characteristics presented correspond to a TFT (L/W = 20/500 μm), based on ZnO films deposited at 400°C. As can be seen the transistor exhibits excellent operating characteristics with negligible hysteresis and clear channel current saturation for $V_G > 0.5$ V.

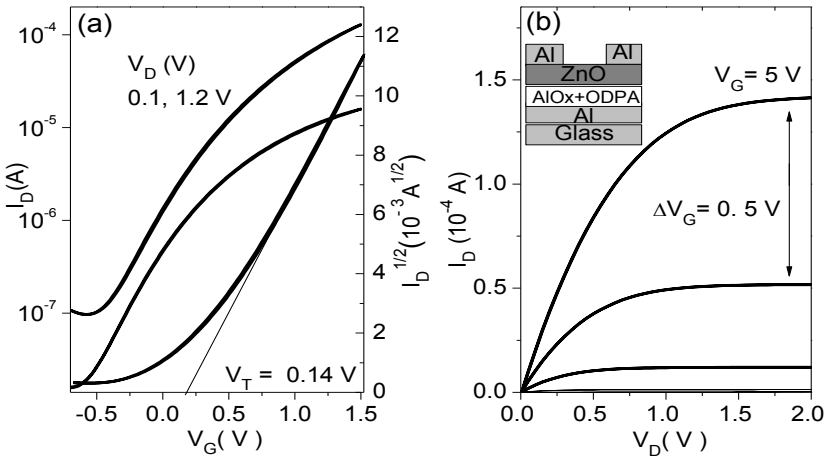

Figure 5.18. Transfer (a) and output (b) characteristics measured from a low-voltage ODPA-based ZnO TFT. Inset in (b) shows the BG-TC transistor architecture employed (L = 20 μm, *W* = 500 μm). ZnO was deposited by spray pyrolysis in air at T_S = 400°C.

From these measurements it appears that high temperature deposition of ZnO does not damage the SAM dielectric (at least not to a significant degree) and functional ZnO TFTs can be realised. Table 5.2 summarises the performance parameters of these ODPA-based ZnO TFTs fabricated at different T_S ranging between 200-500°C. These are typical values representing nearly 50 devices for each set of deposition temperature. The current on-off ratio and SS were observed to exhibit only small variations from device to device and maintained the respective order of magnitude for all substrate temperatures. On the other hand mobility and V_T were found to vary when measured from different devices though prepared under similar conditions. The distribution in these values are 0.25-0.37 cm^2/Vs, 0.23-0.42V; 8.56-10.8 cm^2/Vs, 0.26-0.32V; 12.15-14.3cm^2/Vs, 0.14-0.24V; 7.5-8.37 cm^2/Vs, 0.34-0.32V; for devices prepared at substrate temperature of 200 ^oC, 300 ^oC, 400 ^oC and 500 ^oC respectively. The extracted electron mobilities are comparable to values obtained from BG-TC transistors employing SiO_2 gate dielectric (see Table 5.1). The mobility trend with T_S is also similar to that found for SiO_2 based devices. Therefore, it can be assumed that crystallinity and hence the electronic properties of ZnO with an ODPA layer on top has not changed.

T_S (°C)	V_T (V)	μ_{SAT} (cm^2 /Vs)	On-off ratio	S (mV/ dec)
200	0.42	0.37	10^3	383
300	0.31	10.8	10^3	409
400	0.14	14.3	10^3	392
500	0.3	8.3	10^3	290

Table 5.2.Performance parameters of low-voltage BG-TC ZnO transistors based on AlOx-SAM dielectrics. The channel length of the TFTs was 20-30 μm while the width was 500 μm. These values represent the typical device parameters.

In order to prove that the ODPA layer plays a key role in reducing the leakage current to the gate electrode, we have also fabricated ZnO TFTs employing bare Al–AlOx gates. Surprisingly, operational transistors can be obtained even when functionalization of the Al–AlOx gate with ODPA is omitted (data not shown). We attribute this to the unique matching of the two important chemical processes: i) conversion of the zinc acetate solution to ZnO and ii) further oxidization of the surface of the aluminium gate electrode to AlOx. However, we note that low-voltage ZnO transistors without ODPA exhibit significantly higher gate-leakage currents, significantly lower on/off ratios ($<10^2$), and reduced electron mobilities as compared to ODPA-based ZnO TFTs.

5.4.5 Low-voltage unipolar ZnO transistors based inverters

SAM-based ZnO TFTs demonstrated in the previous section were employed to realise low-voltage unipolar logic NOT gates. The latter were obtained by choosing suitable transistors from different substrates though prepared under similar deposition conditions. Figure 5.19 represents the output curves of a unipolar voltage inverter measured in air, with the inset displaying the inverter configuration comprising two low voltage ODPA based ZnO TFTs with L = 60 μm.

The circuits represents the desired logic function with signal gain >1 and operates at voltages below 2 V. These results clearly demonstrate the potential of combining simple and low-cost deposition techniques for the fabrication of high performance transistors and logic circuits.

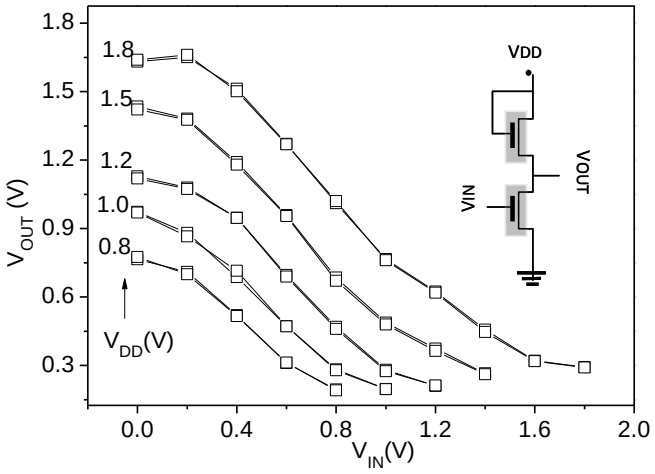

Figure 5.19. Transfer characteristics of a unipolar voltage inverter comprising two low-voltage ODPA-based ZnO transistors measured at different V_{DD}. Inverter characterization was performed in ambient atmosphere. The inset shows the circuitry of the unipolar inverter (L = 60 μm as the design rule).

It is also worth noting that the SAM-based ZnO transistors and circuits operate at low voltages comparable to that of state-of-the-art amorphous silicon TFTs and could arguably be considered as an alternative to amorphous and polycrystalline silicon for a host of ubiquitous electronic applications.

5.5 Top gate ZnO transistors and the effect of oxygen plasma treatment

5.5.1 Device fabrication

So far the work described in this thesis focused on bottom gate TFTs. However, alternative transistor architectures such as top-gate ones are usually required for implementation in commercial electronic products. In order to investigate the possibility of fabricating such alternative device structures utilising the processing paradigms discussed in earlier sections, we have attempted to realise top-gate TFTs utilising an organic dielectric namely CYTOP [Figure 5.20].

Top-gate ZnO transistors were fabricated on glass substrates using ZnO thin films deposited by SP at 400°C in ambient air followed by the evaporation of the Al S-D electrodes through a shadow mask under high vacuum.

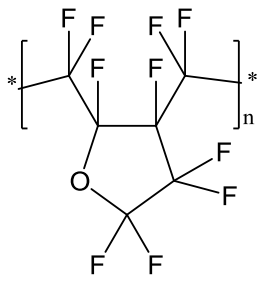

Figure 5.20. Chemical structure of the solution processable organic dielectric CYTOP.

CYTOP was then spin cast (see Chapter 4) followed by the evaporation of the Al top gate electrodes. Prior to the deposition of the S-D electrodes (Al) the surface of the ZnO films were exposed to an oxygen plasma treatment for 5-10 minutes at 80 W. Finally, dual gate transistors were fabricated utilising the usual Si^{++}/SiO_2 wafers employing spray pyrolysed ZnO layers, Al S-D electrodes and CYTOP/Al as the top dielectric and gate electrode, respectively.

5.5.2 Top-gate ZnO transistors based on CYTOP dielectric

The operating characteristics of top-gate ZnO transistors are displayed in Figure 5.21. The devices exhibit hysteresis-free operation with on-off ratio on the order of 10^3 and a maximum electron mobility of ~0.155 cm^2/Vs. Although the electron mobility is much lower than obtained from BG-TC devices, the overall performance is reasonable when compared to recent results reported for top gate ZnO TFT employing poly (4-vinylphenol) (PVP) as the gate dielectric (80). In the latter study an electron mobility of ~6.4×10^{-3} cm^2/Vs and on-off ratio of only 30, were reported.

The low device performance may be a result of the different ZnO surface morphology and/or the slightly different surface stoichiometry as compared to the SiO_2/ZnO interface. In order to modify the elemental composition of the ZnO surface, and in particular to improve the oxygen content, ZnO films were subjected to oxygen plasma treatment (81-83). Fabrication of the ZnO TFTs was then completed with the deposition of the Al S-D electrodes and the CYTOP/Al dielectric/gate electrode, respectively. Obtained results were quite consistent with

previously reported studies of plasma treated ZnO thin film as well as TFTs (81-84).

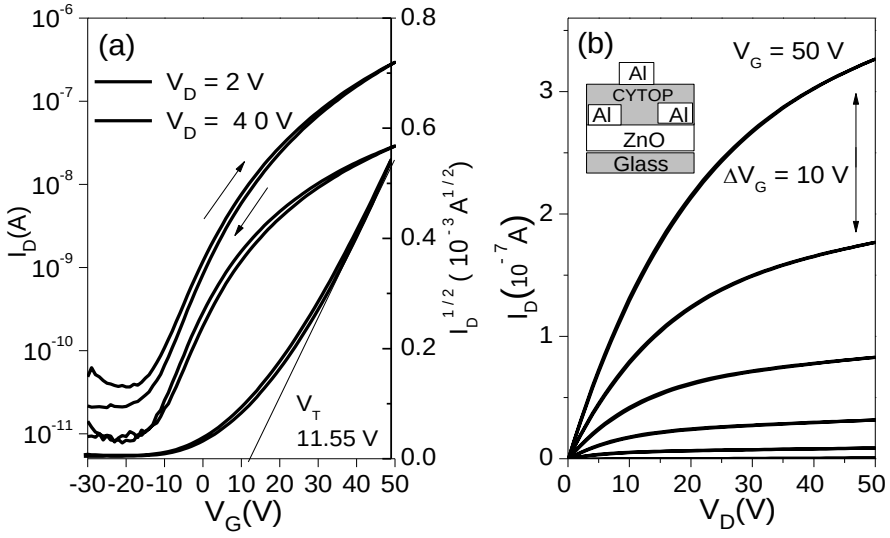

Figure 5.21. (a) Transfer characteristics of a top gate ZnO TFT using CYTOP as a gate dielectric with a saturation mobility < 1 cm^2 /Vs and channel L/W of 100 μm/1000 μm. (b) Output characteristics of the same device. Inset: The top-gate, top - contact architecture used for this device.

Table 5.3 summarises the processing and transistor parameters including oxygen plasma exposure time, V_T, μ_{SAT}, on-off ratio and SS. The positive shift in V_T from 8 V to 11 V with increasing exposure time indicates both reduction of free carriers and increase in donor like trap states. This is also confirmed by the reduction in the off currents from 2×10^{-10} A to 3.6×10^{-11} A, and saturation current from 5.4×10^{-7} A to 3×10^{-7} A. Exposure of ZnO to oxygen plasma seems to improve the transistor's on-off ratio (Table 5.3). The improved SS is attributed to the reduction in the total trap density at the ZnO/CYTOP interface. It is to be noted that each parameter in Table 5.3 represents typical device characteristics out of 15 devices measured for each set of plasma conditions. The dispersion in these parameters was too small to be negligible.

From these results it can be concluded that the plasma exposure time increases the absorbed oxygen and hence reduces the oxygen vacancies at the surface of the ZnO films. Since oxygen is highly electronegative it attracts electrons from the ZnO resulting in a reduced electron density which

is manifested in the drop of the channel current both in saturation and linear operating regime.

	Transistor parameter			
Plasma exposure(min)	V_T (V)	μ_{SAT} (cm^2 /Vs)	On-off ratio	SS (V/ dec)
5	8.2	0.140	$2x10^3$	11
10	11.5	0.135	$8x10^3$	9.2

Table 5.3. Operating parameters of top-gate ZnO transistors measured for different oxygen plasma exposure time of the ZnO thin film (T_S = 400°C). For each set, the parameters are representative of typical device characteristics.

Since ZnO films deposited at 400°C are polycrystalline, electron transport is limited by the energy barriers present between the grain boundaries. The barrier height is proportional to the square of the density of surface trap states at the grain boundaries (N_t) and inversely proportional to the free electron density. Therefore the observed decrease in charge carrier mobility can be associated either with a decrease in charge carrier density or an increase in surface trap density. The adsorbed oxygen at the grain boundaries increases the trap density which would also increase the barrier height thus reducing the average electron mobility (83, 85).

5.5.3 Dual-gate ZnO transistors

Dual-gate ZnO transistors based on the device structure shown in Figure 5.22(a) have been fabricated. This type of device allows the direct comparison of the electronic properties of the top and bottom ZnO channels within the same device thus negating any significant structural variations.

By fixing the potential in the top gate (V_{TG}) and measuring the transfer characteristics of the bottom-channel, typical dual-gate operation was observed [Figure 5.22(b)]. As can be seen the threshold voltage of the transistor can be modulated at will by controlling the V_{TG} potential. This effect is a consequence of the effects of the electrostatic interactions between the two gates and the resulting channels (86).

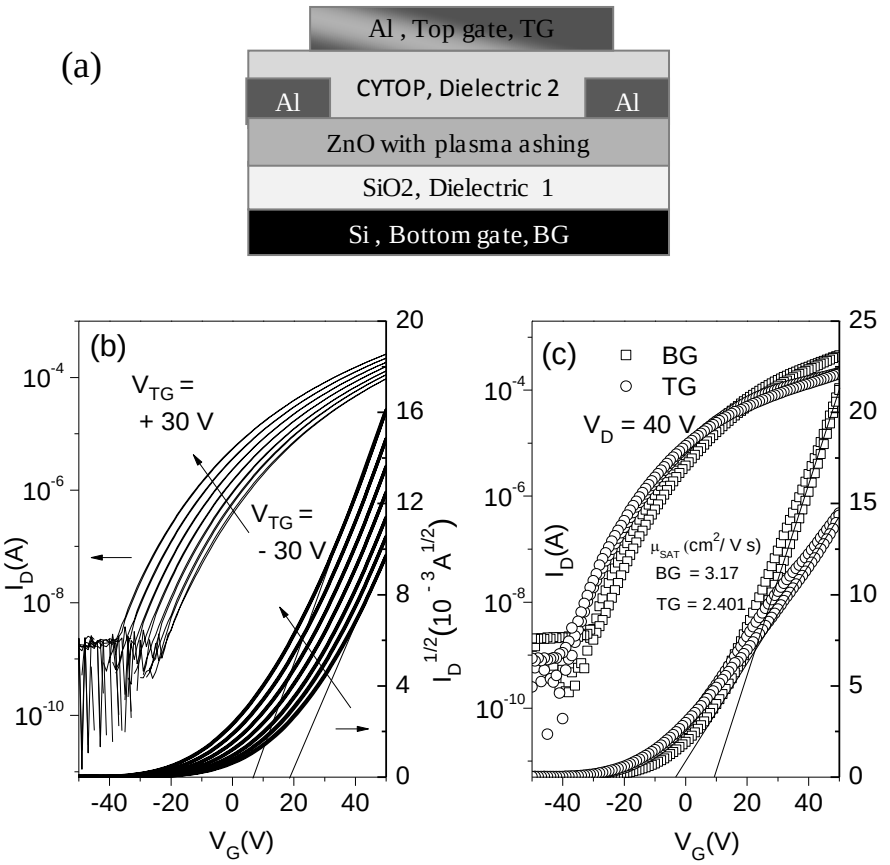

Figure 5.22. a) Schematic representation of the dual-gate device structure. SiO_2 and CYTOP were employed as the gate dielectrics and ZnO layer was treated with oxygen plasma ashing for two minutes prior to CYTOP deposition. b) Transfer characteristics measured for the bottom SiO_2/ZnO interface obtained at different top-gate potentials. c) A comparison of top and bottom channel transfer characteristics and the extracted mobilities and threshold voltages.

Despite the V_T change, the electron mobility within the bottom-channel remains approximately constant and independent of the V_{TG} while it is slightly higher than the value obtained from the top-gate channel. The transfer characteristics for both channels are shown in Figure 5.22(c). The two channels exhibit slightly different on/off ratio and negligible hysteresis between forward and reverse scans. This difference in performance could partly originate from the different device architecture of the two channels as well as from the nature of dielectric interface. The dual gate ZnO transistors were also studied by connecting the two gates together, i.e. single gate (SG) configuration. The resulting circuitry is shown in the inset of Figure 5.23(a). The latter configuration allows an increase in

the effective width of the conducting channel and hence the enhancement of the current-driving capabilities of the transistor. Figure 5.23 displays the transfer and output characteristics of the dual-gate ZnO transistor connected in the SG configuration. The characteristics exhibit a clear pinch-off voltage, current saturation and hysteresis-free operation.

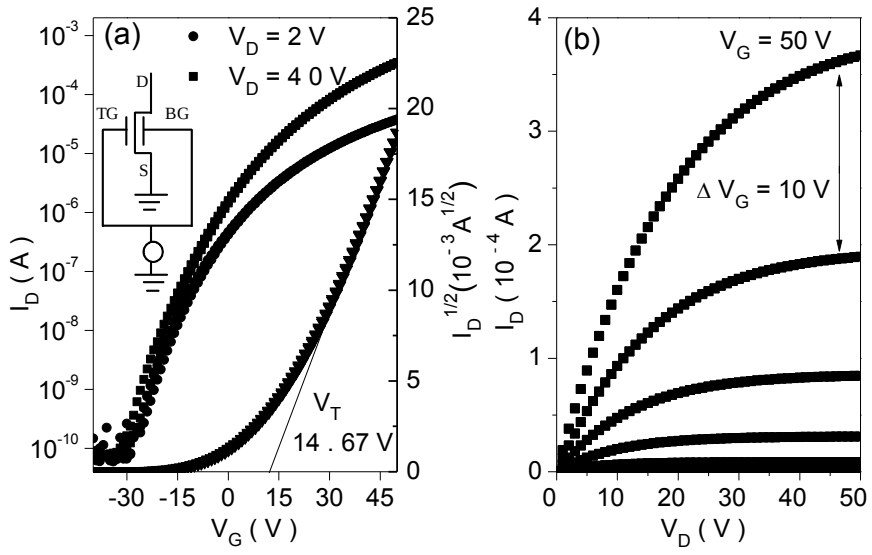

Figure 5.23. (a) Transfer characteristics of a dual gate ZnO TFT, measured with both gate shorted as shown in the inset. Mobility is obtained using capacitance for parallel combination of two dielectrics. Device dimensions are L/W = 50 μm/500 μm. (b) Output characteristics of the same device.

Table 5.4 summarises the data obtained from the dual-gate devices for all three different measuring configurations i.e. dual-gate (DG) using the bottom-gate (BG) channel, DG with the top-gate (TG) channel and DG with the single-gate (SG) channel configuration. As can be seen the effective mobility of the device calculated for the DG-SG configuration is high and of the order of 9.5 cm^2/Vs. Although not very clear, this significant mobility enhancement is probably due to an enhanced channel conduction which also results in high on-off current ratio. It can thus be concluded that shorting the two gates in dual gate device architecture can improve the device by a factor of three hence making the DG-SG configuration attractive for practical applications (87). However, integration of the second top-gate electrode is found to be negatively affecting the performance characteristics of the bottom channel device as evident by the reduction in its electron mobility.

	Transistor parameter			
TFT Structure	V_T (V)	μ_{SAT} (cm^2 /Vs)	On-off ratio	SS (V/ dec)
DG/BG	8.1	3.17	10^6	3.5
DG/TG	-4.9	2.4	10^6	4.2
DG/SG	11.5	9.5	4×10^6	4.7

Table 5.4. Summary of the Dual gate (DG) ZnO TFT characteristics for different architectures (TG = top-gate, BG = bottom-gate, SG = single-gate). These values are representative of typical device characteristics.

From these measurements it can be concluded that the dual-gate ZnO TFTs demonstrated in this section represents an advantageous device architecture that can lead to the formation of transistor channels with improved electrical characteristics when the two gates are combined.

5.6 Summary

The role of the growth temperature on the structural, optical and electrical properties of ZnO films processed by spray pyrolysis has been investigated. Optical and structural measurements revealed that the onset for the formation of ZnO can be as low as 100°C. Increase of the substrate deposition temperature to 500°C resulted in films with enlarged crystal size up to 32 nm. Transistors based on ZnO films grown at temperatures in the range of 200-500°C exhibit the highest electron mobilities with maximum values in the range 20-25 cm^2/Vs. The present results demonstrate the possibility of depositing high optical and electronic quality ZnO films onto large area substrates using the rather simple technique of spray pyrolysis. Furthermore, spray pyrolysis can be combined with simple processing of solution processed organic SAM dielectrics for the fabrication of high-performance transistors and integrated circuits with operating voltages below 2 V. These low-voltage transistors exhibit excellent operating characteristics with high electron mobilities (~10 cm^2/Vs). Top gate ZnO transistors have also been demonstrated and the effect of O_2 plasma treatment of the semiconductor surface has been investigated. An improvement of device characteristics in terms of on-off ratio upon treatment was observed. The latter was attributed to a reduction in the free electron density resulting from adsorbed oxygen on ZnO surface. Finally, dual gate

operation was also successfully demonstrated and transistors with improved operating characteristics have been realised. The use of spray pyrolysis for the large-area deposition of high quality metal oxide semiconducting films, discrete devices and integrated circuits can be considered a major step toward low-cost, high-performance transparent electronics.

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Chapter 6

Solution-processed hybrid thin-film transistors

Abstract

There are still a few important technology bottlenecks that would need to be addressed before the technology of oxide based transistors can be fully exploited. These are associated mainly with material processability, poor environmental stability and above all the unavailability of hole-transporting (p-type) oxide semiconductors. Development of large-scale oxide integrated circuits demands the development of p-type oxide semiconductors with equivalent electrical characteristics or alternative/compatible semiconductor technologies. In this chapter we explore an alternative method for the fabrication of high performance transistors based on ambipolar like hybrid heterostructures. The latter consists of a phase separated organic semiconducting blend as the p-type layer, and transparent ZnO as the n-type layer. By combining these heterostructures with novel device architectures we are able to demonstrate p-/n-type hybrid transistors with balanced carrier mobilities as well as integrated circuits based on complementary circuitry.

6.1. Introduction

Organics and transparent oxide semiconductors are two families of materials that are currently being investigated as potential alternatives to silicon (Si) technology for use in existing and new electronic device applications (1-3). Oxide compounds are a relatively new addition to the family of electroactive materials but the field of oxide microelectronics has been advancing rapidly and within only a few years has managed to outperform (i.e., in terms of charge carrier mobility—a commonly used figure of merit) established technologies such as amorphous Si (a-Si) and organic semiconductors (4, 5). This rapid development is reflected both in the increased number of scientific publications and by the demonstration of the first product prototypes i.e., optical displays using oxide TFTs based switching backplanes (6-8). Despite their impressive track record, however, oxide semiconductors suffer from one main drawback which is the distinct lack of hole-transporting compounds with appreciable charge mobilities. Part of this problem lies in the fact that for most oxide semiconductors the valence band (VB) edge is inaccessible (i.e., very deep and typically of the order of –7 eV) and part in the localised nature of the hole transport states (comprising of the oxygen 2p orbitals) (9). In an effort to address this problem a number of different approaches have been reported including new materials systems as well as different doping protocols. Unfortunately, to date the success of these approaches has been limited with only few exceptions (10-15).

A great deal of interest in the development of organic semiconductors stems from their potential for low temperature processing using low cost printing techniques. In recent years, impressive progress has also been made in terms of their performance and particularly charge carrier mobility and stability. Despite this, however, there have been relatively few examples of solution processible n-type organic semiconductors that exhibit carrier mobility and environmental stability comparable to those achieved by their p-type counterparts. Because of this the majority of organic TFTs reported to date in the literature are based on p-type compounds (16). The unavailability of stable n-type organics has hindered the development of low cost, large-scale integrated circuits based on complementary logic, a key technology that could enable the development of robust integrated circuits.

In this chapter we report on an alternative approach toward the development of high-performance ambipolar transistors based on existing materials systems comprising high mobility p-type organic and n-type transparent oxide semiconductors. There have been several reported examples of organic-inorganic hybrid systems with the aim of combining the advantageous features of each material (17), making complementary logic inverter and ring oscillator circuits (18-20), or creating ambipolar bilayer structures (21, 22). However, these have either had low mobilities, separate p- and n-channel transistors, or were not fully solution processible. In this respect, our approach is unique because it combines key features of organic semiconductors, that include air-stable hole transport and solution processability, with highly complementary features found only in oxide semiconductors which include air-stable electron transport, solution processability and optical transparency.

By combining hybrid bilayers with a novel dual-gate transistor architecture (23, 24) we are able to achieve, within a single device, both unipolar (hole or electron) as well as ambipolar transport. This is achieved by depositing an organic layer composed of a polymer-small molecule blend, acting as the hole transporting medium (25), directly onto a solution deposited zinc oxide (ZnO) layer, acting as the electron transporting material (26, 27). Integrating these hybrid layers within a dual-gate transistor structure, we are able to realise air-stable transistors with hole (μ_h) and electron (μ_e) mobilities of over 2 cm^2/Vs. Depending on the applied biasing configuration the hybrid TFTs can be operated either in a p-channel, n-channel or ambipolar mode. By integrating several of these rather versatile devices we are able to realise hybrid logic gates with operating characteristics closely resembling those of truly complementary circuits i.e. circuits that combine hole and electron transporting TFTs. The work described in this chapter is a significant step towards high-performance, large-area microelectronics fabricated by solution processing (i.e. a combination of spin-casting and spray pyrolysis) a large-area compatible and potentially low manufacturing cost deposition method.

6.2. Experimental

6.2.1. Material Systems used and device fabrication

The precursor and organic materials employed in this work were: Zn-acetate dihydrate used for the deposition of electron transporting ZnO layers; for the hole transporting layer, 2,8-difluoro-5,11-bis(triethylsilylethynyl) anthradithiophene (diF-TESADT) which was admixed with a matrix polymer, poly(triarylamine) (PTAA), to form the polymer-small molecule blend. The soluble perfluoropolymer CYTOP (Asahi Glass) was used as the top-gate dielectric. Molecular structures of these materials are shown in Figure 6.1.

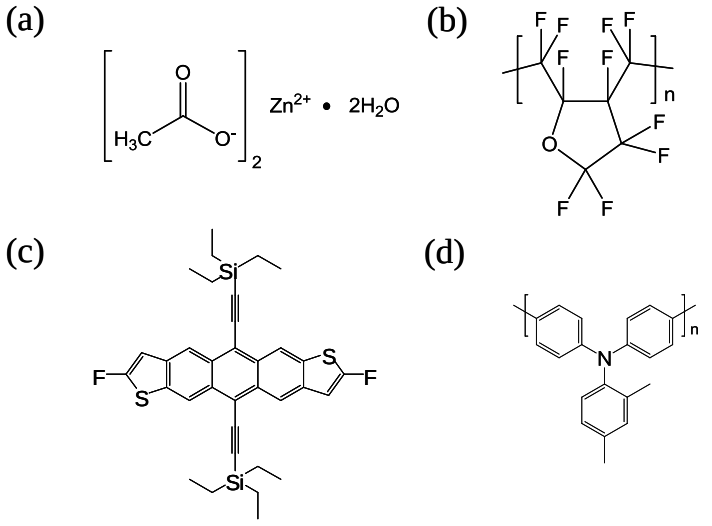

Figure 6.1: Chemical structures of the solution processible materials employed for the development of the hybrid transistors. (a) Zinc acetate dihydrate [n-type ZnO films], (b) the p-type diF- TESADT molecule, (c) CYTOP fluoropolymer gate dielectric, (d) the p-type polytriarylamine (PTAA) matrix polymer. (b) and (d) are blended to form the phase separated p-type organic semiconducting layer.

Doped silicon (Si^{++}) wafers employing a 400 nm thermally grown layer of SiO_2 as the bottom gate electrode were used. Discrete hybrid transistors on Si substrates were fabricated according to the following procedure. A film of ZnO with a thickness of ~35 nm was deposited by spray pyrolysis from a solution of zinc acetate in methanol (26, 27), as described in Chapter 4. The substrate temperature was maintained at 400°C in ambient air. The choice of the semiconducting materials in combination with the injecting electrodes is crucial for

the demonstration of high performance TFT. Therefore gold was chosen for source-drain (S-D) electrodes, which were thermally evaporated through shadow masks under high vacuum (10^{-6} mbar). The channel lengths and widths were in the range of 20-70 μm and 1-2 mm, respectively. Gold was chosen because it provides low injection barriers for both holes into the HOMO of diF-TESADT (~0.3 eV) and electrons into the conduction band (CB) of ZnO (~0.8 eV) without having to resort to bilayer or asymmetric-contact metal electrodes. The energy levels that come into play are schematically depicted in Figure 6.2.

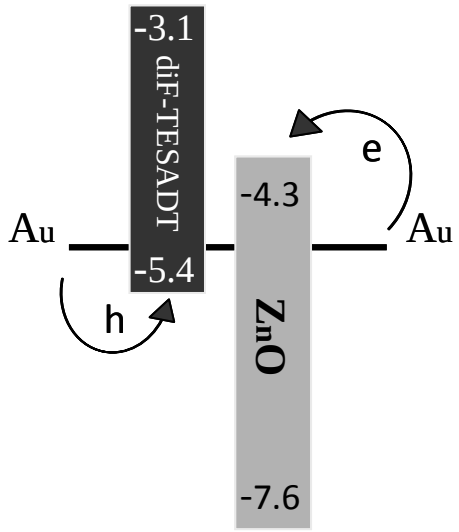

Figure 6.2: Energy levels of Au S-D electrodes and for the n- and p-type semiconducting materials used. For simplicity, the energy levels are drawn as straight lines

The hole transporting semiconducting layer was then spin coated from a solution containing diF-TESADT (28) and the conjugated polymer matrix PTAA (29), 1:1 by weight at 4 wt% concentration of solids in tetralin. Spin casting was carried out in two steps; 1) at 500 rpm for 10 sec, followed by step 2) 2000 rpm for 20 sec and a drying step at 100°C for 3 min in N_2 to obtain organic layers with a thickness of 60-70 nm. Finally, CYTOP acting as the second gate dielectric, was spin coated at 2000 rpm for 60 sec and dried at 100°C for 15 min before the second gate electrode (Al) was evaporated through a shadow mask. Electrical characterisation was performed under nitrogen or ambient air (section 6.3.1) employing a Keithley 4200 semiconductor parameter analyser. Hole and electron

mobilities were calculated from the transfer characteristics in both linear and saturation regimes from the model as discussed in Chapter 3. Geometric capacitances of the gate dielectrics used were $C_{i(CYTOP)}$ ~ 2.1 nFcm^{-2} and $C_{i(SiO2)}$ ~ 8.5 nFcm^{-2}.

6.2.2. Film characteristics

The surface morphology and crystallinity of the ZnO films deposited on Si were examined by atomic force microscopy (AFM) [Figure 6.3(a)] and XRD measurements. The films are found to be polycrystalline in nature with a typical crystallite size of around 25 nm (calculated from both the AFM and XRD data). As can be seen from Figure 6.3(a) the surface is very smooth with r.m.s surface roughness of ~2 nm. The organic blend comprising PTAA:diF-TESADT was then spin cast onto the ZnO films at room temperature.

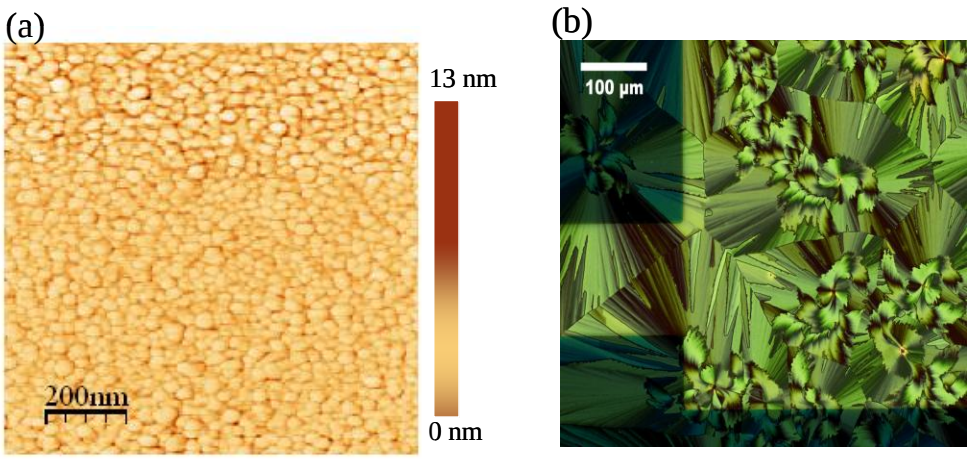

Figure 6.3: (a) AFM image of a ZnO film deposited by spray pyrolysis, representing a smooth surface with an rms roughness of ~2 nm. (b) Polarised light microscopy image of the ZnO/PTAA:diF-TESADT bilayer showing crystallisation of the diF-TESADT blend. Courtesy of Jeremy Smith.

Figure 6.3(b) shows a polarised light optical micrograph of the bilayer film revealing a polycrystalline microstructure that is very similar to that seen in blend organic films fabricated directly onto glass substrates (25, 30). The only difference is the slight increase in the variation of grain sizes, which is probably induced by the different surface roughness/surface energy of ZnO when compared to the

smooth glass substrate used in earlier studies. These large crystalline domains are the result of a distinct phase separation occurring between the small-molecule organic and the polymer matrix (25). The latter leads to the formation of a film consisting of a highly crystalline top surface that is capable of hole transport. Hence, the ZnO/ PTAA:diF-TESADT bilayer films can be considered as a single semiconductor where its top surface is capable of conducting holes while its bottom surface electrons, both with very high charge carrier mobilities.

Figure 6.4 shows the optical transmission spectra for both the pristine ZnO and ZnO/organic bilayer film deposited on quartz substrate (inset). Transmission was measured between 380-780 nm. As can be seen, both films are highly transparent in the optical range 420–800 nm with transmission values exceeding 80%.

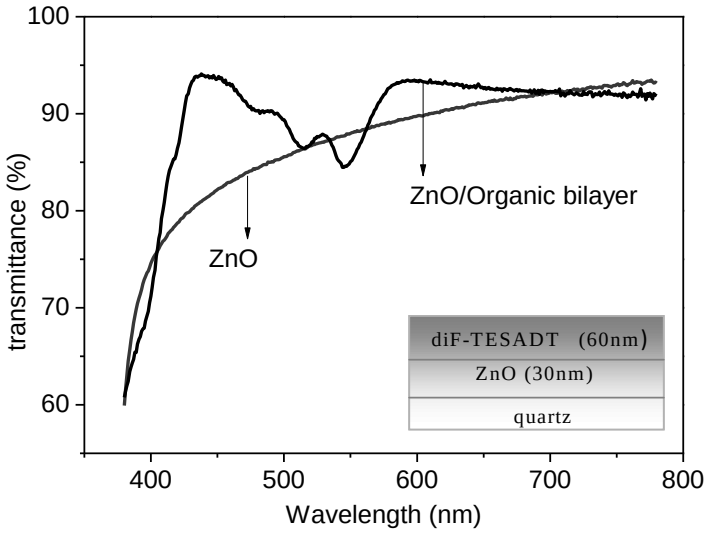

Figure 6.4: Transmission spectrum of ZnO film alone and ZnO/PTAA: diF-TESADT bilayer, deposited onto a glass substrate. Inset: cross section of bilayer structure used. Courtesy of Jeremy Smith.

Such high optical transparency qualifies the hybrid ZnO/PTAA:diF-TESADT heterostructure as a candidate for use in future transparent electronics. It should be noted that the use of hybrid semiconductor films comprising a phase separated organic layer has not been reported previously in the literature.

6.3. Hybrid ambipolar thin-film transistors

The electronic properties of hybrid transistors utilising ZnO as the n-type bottom layer and the organic semiconducting blend PTAA: diF-TESADT as the top layer, have been investigated in dual-gate field-effect transistor architectures utilising a common set of gold S-D electrodes. A schematic cross section of the bilayer transistor is shown in Figure 6.5(a). Such transistors can operate in three different regimes, listed below:

i) Unipolar n-channel regime (electron accumulation)
ii) Unipolar p-channel regime (hole accumulation)
iii) Ambipolar regime (electron & hole accumulation)

The ambipolar transport regime can be achieved by connecting the bottom-gate (BG) and top-gate (TG) terminals together as shown in the circuit in Figure 6.5(b). Under such biasing configuration the device is capable of conducting holes and electrons, provided that the hybrid semiconductor film can facilitate transport of both carriers. The type of accumulated carriers depends on the magnitude and polarity of V_G and V_D (31).

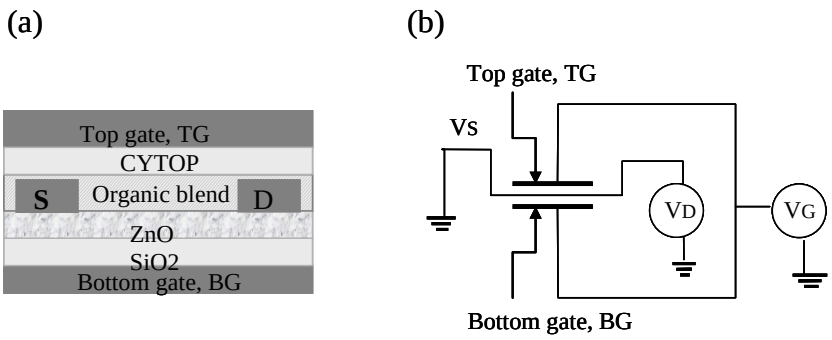

Figure 6.5: a) Cross-section of the dual-gate hybrid transistor fabricated. b) Equivalent circuit for a dual-gate transistor with the two gates (i.e. TG and BG) interconnected and the common source electrode grounded (V_S).

Figure 6.6 displays a set of the output characteristics measured from a ZnO/PTAA:diF-TESADT hybrid transistor biased in hole [Figure 6.6(a)] and electron [Figure 6.6(b)] accumulation. For high negative V_G the transistor operates in the hole enhancement mode and its performance is identical to a unipolar

transistor based on pristine diF- TESADT. The hole mobility calculated directly from the transfer characteristics shown in Figure 6.7(a) is in the range of 1.5-2.4 cm^2/Vs. For low V_G the channel current shows a pronounced increase with increasing V_D [see Figure 6.6(a)]. The latter is a typical characteristic of ambipolar transistor operation and is not present in unipolar devices.

When a positive V_G is applied, the transistor operates in the electron-enhancement mode [Figure 6.6(b)] with electron mobility, measured in saturation, in the range 2-4.5 cm^2/Vs. At low V_G and high V_D the channel current increases. The latter is attributed to ambipolar transport and is not observed in unipolar n-channel transistors based on pristine ZnO. Close examination of the output curves (Figure 6.6) at low drain voltages reveals Ohmic-like injection characteristics for both p- and n-channel operation, suggesting that the common Au S-D electrodes provide suitable ambipolar injecting contact.

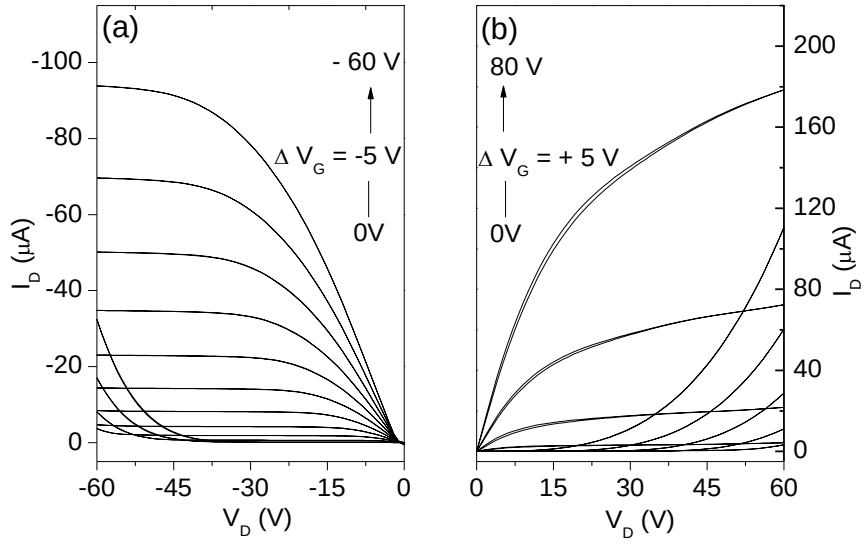

Figure 6.6: Output characteristics measured from a ZnO/PTAA:diF-TESADT based ambipolar hybrid transistor with channel length (L) and width (W) of 30 μm and 1 mm, respectively. The transistor operates both in hole (a) and electron (b) enhancement mode.

Figure 6.7 displays a set of typical transfer characteristics measured for the same hybrid TFT. From this figure it can be seen that devices connected in the common-gate configuration exhibit excellent ambipolar transport characteristics with high on-off current ratios (10^4-10^6) and negligible hysteresis between forward

and reverse V_G sweeps. It is to be noted that the hole and electron mobilities obtained from these hybrid TFTs are the highest mobilities reported for any solution processed hybrid devices to date.

A further intriguing characteristic of these hybrid transistors is that they may also be employed for the realisation of unipolar high-mobility devices. For example, by applying negative voltage at TG and V_D potentials and maintaining a floating bottom-gate terminal, holes can be accumulated and transported at the diF-TESADT:PTAA/CYTOP interface. Figure 6.8 displays the transfer and output p-channel operating characteristics measured from such a transistor. In this figure both the linear and saturation operating regimes can clearly be seen.

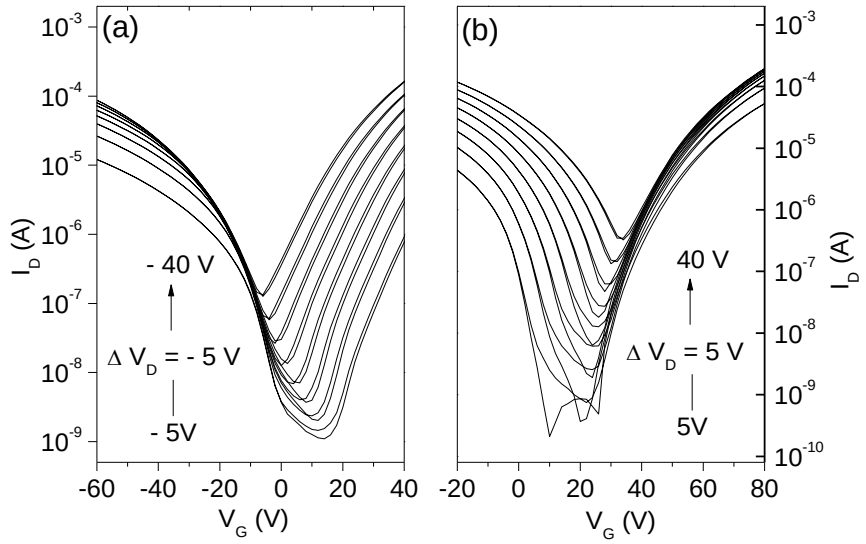

Figure 6.7: Ambipolar transfer characteristics measured from a dual-gate hybrid transistor with channel length and width of 30 μ m and 1 mm, respectively. Transistor operation under; (a) hole-accumulation and (b) electron-accumulation.

Finally, by biasing the bottom-gate of the same transistor with a positive V_G and keeping the top-gate terminal floating, the transistor can be operated as an n-channel device. Figure 6.9 displays the transfer and output characteristics for the same hybrid transistor biased in electron accumulation (n-channel) regime. Unlike p-channel operation, however, the electron conducting channel in this operating mode is formed at the bottom interface of the hybrid semiconducting heterostructure i.e. the interface between SiO_2 and ZnO [see Figure 6.5(a)].

The hole and electron mobilities, calculated in the saturation regime, are balanced and high and typically >2 cm^2/Vs while the threshold voltage for the electron $V_{T(e)}$ and hole $V_{T(h)}$ channels are ~ 40 V and -17 V respectively.

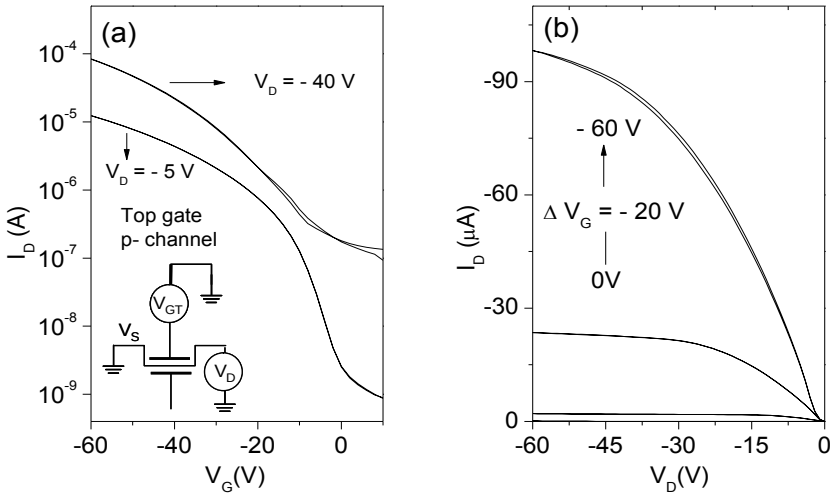

Figure 6.8: (a) Transfer characteristics measured for a top-gate, p-channel hybrid transistor with channel length and width of 30 μ m and 1 mm, respectively. Insets: Schematic of the active device biasing regime. (b) Output characteristics obtained from the same TFT operating in truly unipolar p-channel mode.

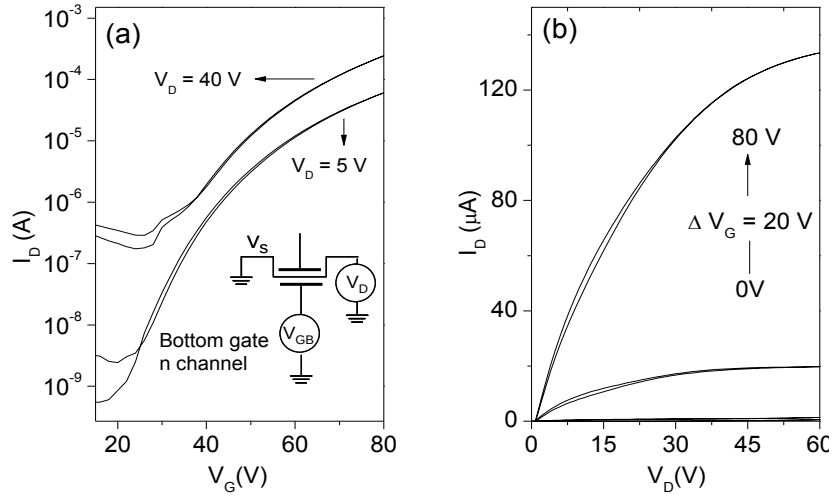

Figure 6.9: (a) Transfer and (b) output characteristics measured for a top-gate n-channel of hybrid transistor with channel length and width of 30 μ m and 1 mm, respectively, operating in truly o channel mode. Insets: Schematic of the active device biasing regime.

Importantly, both operating regimes exhibit nearly ideal unipolar operation with negligible operating hysteresis, hence making the devices ideal for application in truly complementary integrated circuits.

6.3.1 Air-stability of hybrid ambipolar transistors

In addition to the performance characteristics such as carrier mobility and channel current modulation, the operational and environmental stability of the functional devices across a range of ambient oxidants is very important for any future application. One important advantage associated with the solution processed hybrid TFTs described here is the superior environmental stability of both the hole and electron channel. To demonstrate this we have exposed freshly prepared hybrid TFTs to ambient air and monitored the p- and n-channel activity as a function of exposure time. The relative humidity of the ambient atmosphere during testing was fluctuating within the range 45-65%. Figure 6.10 displays the on- and off-currents as well as mobility for both the hole (top interface) and electron (bottom-interface) channels over a period of several weeks.

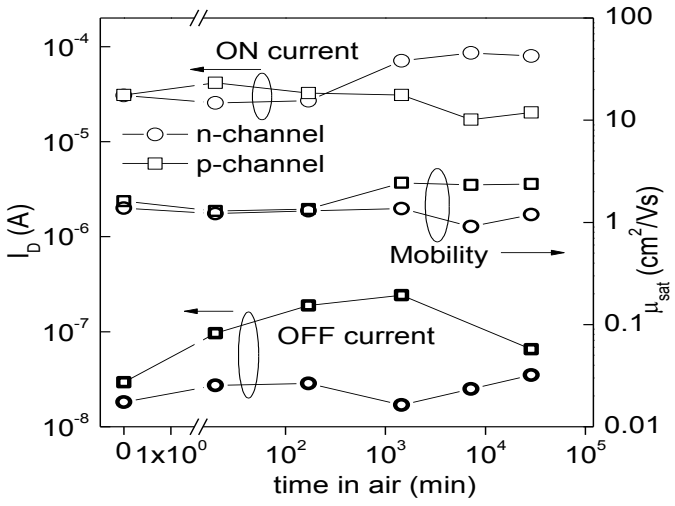

Figure 6.10: Evolution of the channel on and off currents and hole and electron mobilities under p- and n-channel operation as a function of exposure time to ambient air over a period of three weeks. P-channel characterisation was performed at V_D = -40 V, and V_G = -60 V, while n-channel at V_D = 40 V, and V_G = 60 V. Devices were stored in the dark and in air with a relative humidity in the range 45-65%.

From this figure it can be seen that transport of both holes and electrons remains largely unaffected by the ambient air with small variations observed mainly in the off-currents of both channels. Although noticeable, these changes do not significantly affect the operation of the hybrid TFT and are mainly attributed to the damage of the device during repeated electrical probing and testing. Similarly, the hole and electron mobility remains largely unaffected by the presence of ambient air with only a slight decrease in μ_e and a small increase in μ_h. Such superb stability is not surprising since both ZnO and diF-TESADT are known to exhibit environmentally stable n- and p-channel operation, respectively (25, 27).

6.4. Inverters based on hybrid ambipolar transistors

Using these high-performance hybrid TFTs one could, in principle, construct logic circuits. To demonstrate this we have used two hybrid TFTs to realise voltage inverters (i.e., NOT gates) based on complementary logic circuitry. It should be noted that the two TFTs were chosen from different substrates but prepared under same conditions.

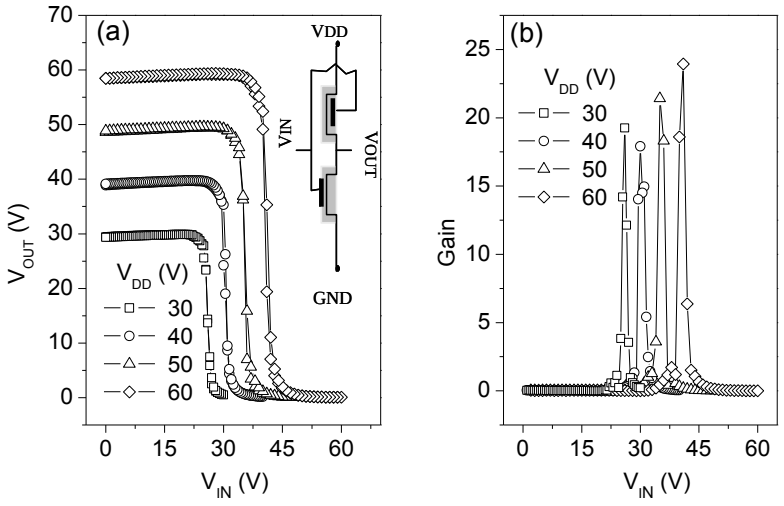

Figure 6.11: a) Transfer characteristics of the hybrid voltage inverter measured at different supply voltages (V_{DD}) ranging from 30 V to 60 V. Inset: Schematic of the inverter circuit employed. b) Differential gain as a function of input voltage (V_{IN}). The channel length and width of the transistors used were 50 μm and 1 mm, respectively.

To achieve truly complementary functionality one TFT was biased as the n-channel device using the bottom-gate, and the other as the p-channel device

using the top-gate. The circuitry of the inverter along with its transfer curves and signal gain, measured at different supply voltages (V_{DD}), are shown in Figure 6.11(a.b). The inverter exhibits hysteresis-free operating characteristics [Figure 6.11(a)] that resemble closely those obtained from truly complementary integrated voltage inverters (32). The average switching voltages (or trip voltages) are slightly shifted from the theoretical value of (V_{DD}/2) mainly due to the threshold voltage mismatch between the two transistor channels. The complementary like nature of this circuit combined with its high differential gain >17 [see Figure 6.11(b)] and wide noise margins (~30% at V_{DD} = 60 V), renders the technology suitable for large-scale circuit integration. Importantly, the hybrid circuits exhibit excellent environmental stability, a prerequisite for successful implementation in future large-volume ubiquitous electronics.

6.5. Summary

In summary, solution processed air stable hybrid transistors that can operate in either unipolar or ambipolar mode have been demonstrated. These model devices are based on a single or a dual-gate transistor architecture comprising optimised hybrid bilayer semiconductor films. Importantly, the semiconductor layers are processed in ambient atmosphere using simple and large-area compatible solution based methodologies. The hybrid transistors have been found to yield electron and hole transporting channels with carrier mobilities exceeding 2 cm^2/Vs, negligible operating hysteresis and excellent environmental stability. This allows the fabrication of high performance NOT gates with operating characteristics closely resembling those of truly complementary circuits. These features make the proposed hybrid heterostructure system a strong candidate for application in versatile, high-performance, large-area electronics.

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Chapter 7

Charge transport in ZnO based thin-film transistors

Abstract

The gate bias (V_G) and temperature dependence of the electron field-effect mobility in polycrystalline ZnO based TFT was investigated in order study the charge transport mechanism at the dielectric/semiconductor interface in these devices. Measurements were performed across the relatively large temperature range of 100-415 K. The electron mobility was found to exhibit a thermally activated Arrhenius like behaviour and increased with increasing gate voltage. Furthermore, the threshold voltage (V_T) was found to become more negative with increasing temperature hence verifying thermally activated conduction. Two thermally competing transport regimes were identified from the dependence of the electron mobility on temperature and the corresponding activation energies were derived using the Arrhenius model. It is found that the observations could only be well interpreted by invoking a multiple trapping model that takes into account the grain boundary trapping effects. The density of trap states below the mobility edge was also evaluated using the multiple trapping model as well as the Levinson model.

7.1 Introduction

In recent years zinc oxide (ZnO) thin-film transistors have emerged as a candidate technology for use in a host of ubiquitous large volume electronic applications (1-4). Interestingly, metal oxide semiconductors are transparent in the visible part of the electromagnetic spectrum making them very attractive for novel device applications. Additionally, they can be deposited uniformly over large areas using a range of techniques that includes relatively simple solution processing. Despite their relatively short history transparent oxide based TFTs have already been shown to exhibit high carrier mobilities as well as excellent on-off ratios, (5, 6) i.e. two key technology requirements for successful implementation in numerous areas. This progress has mainly been achieved through developments in both materials processing as well as the basic understanding of charge transport processes in oxide semiconductors and the role of the device architectures.

The operating parameters of state-of-the-art transparent oxide thin film transistors are strongly dependent on the conduction mechanisms and the electronic structure [e.g. the density of localized gap states (DOS)] of the oxide semiconductor. Hence, elucidation of these fundamental material/system properties is of critical importance to the understanding and hence further development of novel materials with improved performance characteristics. Although the extraction and characterisation of sub-gap DOS (7-10) and its effect of the charge transport characteristics of oxide semiconductors (11-13) has been reported in the literature, the vast majority of these studies have been focused on TFTs based on doped rather than pristine ZnO.

Furthermore, unlike crystalline inorganic semiconductors where charge transport in extended states (i.e. band transport) is limited by scattering due to phonons, in polycrystalline materials such as ZnO the carrier transport is controlled by localized trap states (14) that result from structural imperfections and/or unintentional defects/impurities (15). Hence, the growth conditions such as temperature, deposition rate and pressure, renders the resulting films sensitive to various structural imperfections (16-19). For these reasons, a range of transport characteristics for polycrystalline ZnO thin films have been reported in the literature (20-24). For example, it has been suggested that classic hopping conduction is prevailing at low temperatures in both doped as well as undoped ZnO

films (11-13, 20, 25, 26), while at higher temperatures electron conduction is believed to be via thermally activated band conduction mechanism (12, 27). Schottky emission and tunnelling have also been proposed in order to understand the temperature dependent conductivity (28, 29). Despite the volume of work, however, very few of these early reports focused on the temperature dependence of critical transistor parameters such as the electron mobility and threshold voltage (V_T). As a consequence, the electron transport in ZnO TFTs has not yet been fully explored although a great deal is now known about the role of structural disorder and defects in oxide materials.

In this chapter we show that the electron transport in polycrystalline ZnO TFTs fabricated by spray pyrolysis is thermally activated and invokes the influence of inter-grain boundary trapping. In particular, we use the temperature-dependent electrical characteristics of ZnO TFTs to study important physical parameters such as activation energies, scattering mechanisms and compensation effects, all of which govern the overall carrier conduction. The activation energy reflects the energy separation between the Fermi level and the mobility edge. The former can be determined from the Arrhenius plots of the temperature dependence of the electron field effect mobility (in the case of ZnO).

In this part of the thesis we have investigated the temperature-dependent characteristics of ZnO TFTs in the range 100-415 K. It is established that the average mobility of these TFTs obeys the Meyer Neldel (MN) rule for temperatures in the range 200-400 K and inverse MN rule for temperatures <200 K. This implies that two distinct thermally competing transport regimes exist. The former can be explained using multiple trap and release (MTR) model by invoking the grain boundary trapping. Moreover, the density of trap states was successfully extracted in the sub-gap region using both the MTR as well as the Levinson model. Both models have been discussed in Chapter 3.

7.2 Temperature dependent field-effect measurements

Temperature dependent field-effect measurements were performed on inverted staggered ZnO TFTs fabricated on Si/SiO_2 substrate using Al as S-D contacts, as shown in Figure 7.1. Thin films of ZnO were deposited at 400°C using the spray pyrolysis method discussed in Chapter 4. Electrical characterisation was

performed in high vacuum (10^{-6} mbar) and in the dark using a Keithley 4200 semiconductor parameter analyser. The device temperature was regulated by a temperature controller with a precision of ±1 K. Before each measurement, the TFTs were placed on the heated chuck, set at the desired measurement temperature, for 15 min in order to allow for thermal equilibrium to be reached. At each temperature the drain current (I_D) was recorded as a function of the gate current (V_G) across the temperatures range of 100-400 K. Measurements were obtained for several ZnO TFTs with channel width (W) of 1 mm and channel length (L) in the range 70-100 μm.

7.2.1. Temperature dependent current-voltage characteristics

The transfer characteristics for a ZnO TFT measured in the linear operating regime (V_D = 2 V) at different temperatures are shown in Figure 7.1. It can be seen that as temperature increases the conductivity of the ZnO film increases.

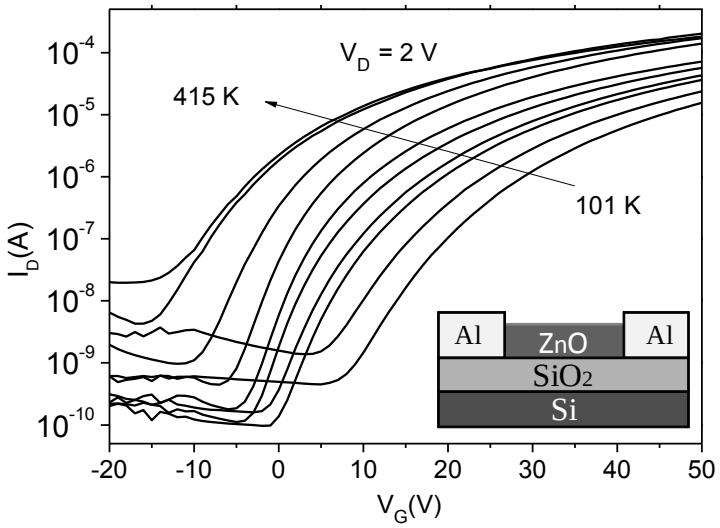

Figure 7.1: The transition of the transfer characteristics for ZnO TFT with W/L = 1000/70 μm, depending on various temperatures measured. There is a consistent shift in these characteristics to the negative direction with increasing temperature from 100K to 415K. The V_T of pristine ZnO TFTs is decreased by approximately 20 V, i.e. from 31.5 V to 11.5 V. It is caused by increasing of thermally activated electrons with rise in measured temperature. The inset shows the device structure used for these measurements.

The switch-on voltage also is found to shift towards more negative gate voltages. From these measurements it can be concluded that I_D is thermally activated as it increases by one order of magnitude. The only exception is the small drop observed at T > 400°K. The latter is most likely attributed to band like transport and will be discussed in the next section. The increase in conductivity with temperature can be accounted for by rise in carriers contributed from the donor states. These thermally activated electrons then reduce the threshold voltage of the device.

7.2.2. Temperature dependence of electron mobility in ZnO transistors

In order to understand the temperature dependence of the average electron mobility (μ_{ave}) i.e. the average value between free and trapped carriers as discussed in Chapter 3, transfer characteristics were measured in the linear operating regime (i.e. V_D = 2 V where the in-plane electric field is much smaller than the applied V_G, which results in an approximately uniform density of charge carriers in the active channel) at different temperatures. Figure 7.2 displays the ln(μ_{ave}) versus 1000/T for various gate voltages. These characteristics are clearly indicative of thermally activated electron transport having two different conduction regimes. For temperatures > 400 K (region C) a fall in the electron mobility is observed marking the onset of band like transport. The latter implies that electrons above the mobility edge are transported in the delocalized states forming the conduction band. As temperature increases phonon scattering becomes dominant and the electron mobility reduces.

For lower temperatures the average electron mobility reduces and exhibit two different regimes: regime A for T < 200 K and Regime B for 200 K < T < 400 K. The latter observation possibly suggests two different competing mechanisms with different activation energies. In both temperature regimes electron transport is dominated by recurrent trapping into localised trap states below the mobility edge followed by thermal activation into delocalised states above the mobility edge, as discussed in Chapter 3. In order to better understand and interpret this data the Multiple Trap and Release (MTR) model has been employed. These results are discussed next.

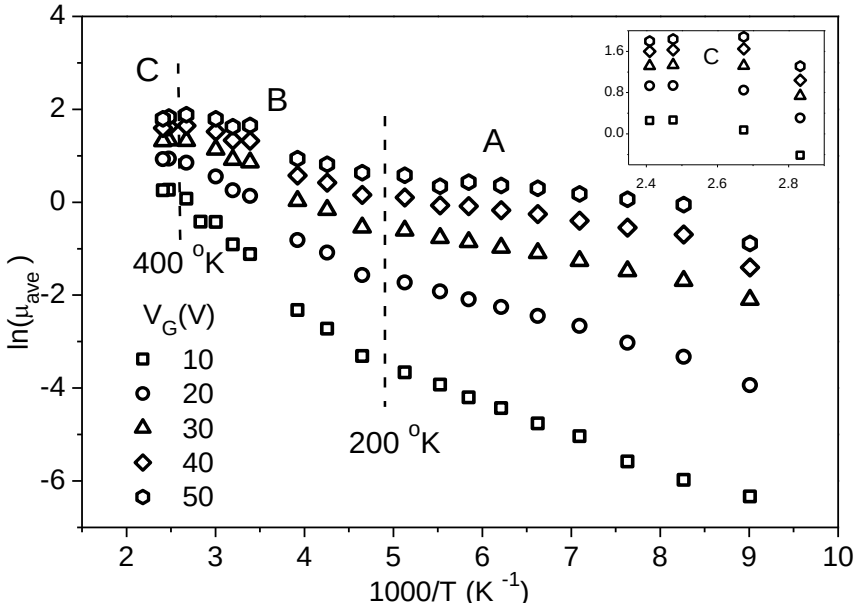

Figure 7.2: Arrhenius plots of the average electron mobility at different gate voltages measured from a ZnO transistor. The dashed lines demarcate the different transport regimes. A and B correspond to thermally activated transport under different mechanisms and region C corresponds to band like transport. Inset is a magnified view of region C.

7.2.3. Meyer Neldel rule and multiple trapping

The variable range hopping (VRH) model predicts a linear relationship between ln(μ) and $T^{1/4}$ (11-13). Thus, the Arrhenius relationship shown in Figure 7.3 excludes the possibility of a classic hopping type transport in our sample. These Arrhenius fits for two regions are separately shown in Figure 7.3(a-b). Upon extrapolation of the linear part of the plots (200 K < B < 400 K) to high temperatures we find a common crossing point as depicted in Figure 7.3(a). This indicates that the Meyer Neldel Rule (MNR) is possibly applicable to ZnO based TFTs. To this end it has been shown that the multi trapping and release type transport always exhibit NMR (30). Hence the appearance of NMR provides additional evidence that the MTR is the dominant transport mechanism in these ZnO based devices.

The trap distribution width can be estimated directly from the Meyer-Neldel energy (MNE) (see Equation 3.8) assuming an exponential distribution of trap states. The latter is found to be kT_o = 123 (±3) meV. Since the Meyer Neldel behaviour is related to both the spatial distribution of defects in the active layer and to the density of sub-gap states, it has often been used to quantify the quality of the

semiconductor layer in TFTs (31, 32). From our measurements, the high values of kT_o are most likely associated with large trap density and the high degree of disorder within the ZnO layer. In the lower temperatures regime (A; < 200 K) no such values could be extracted since the linear fits did not intersect at a common point [Figure 7.3(b)]. The latter observation most likely suggests that a different charge transport process may be occurring in this part of the temperature region.

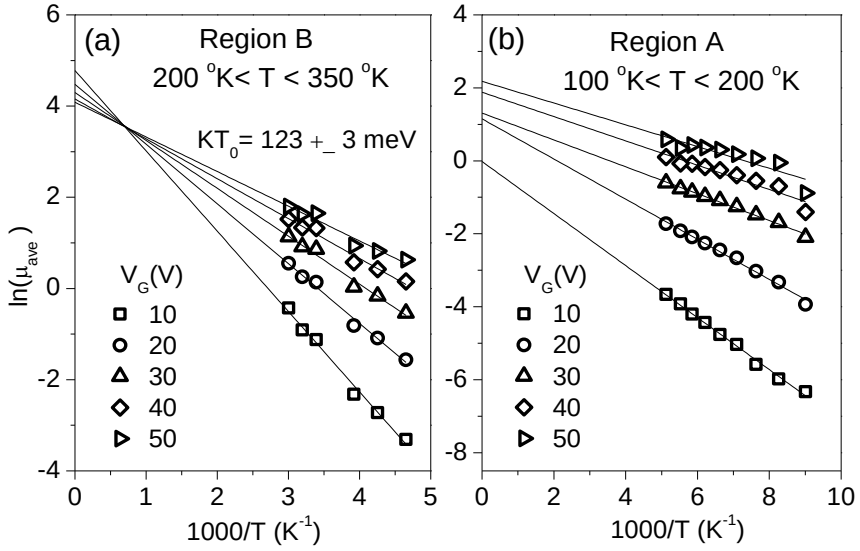

Figure 7.3: Arrhenius plots of the average electron mobility of ZnO TFT at various gate voltages for; (a) high temperature region B, and (b) low temperature region A. Linear fits are intersecting at a single point only for region B from which the Meyer-Neldel energy (kT_o) can be estimated.

From the slopes of the Arrhenius plots, the activation energy (E_a) for the electron mobility was calculated. These data are displayed in Figure 7.4(a). This evolution of E_a with V_G, for both temperature regimes, reflects the distribution of DOS in the sub-band gap region. Specifically, the decreasing trend of E_a indicates that as V_G increases the energy distance between the filled trap states and the band/mobility edge reduces due to shifting of the Fermi level (27). The derived activation energies of 25-61 meV and 65-151 meV correspond to the shallow donors as well as the defect states in ZnO. Both values are in agreement with those reported literature for ZnO prepared by different deposition methods (33-36). Finally, the activation energy can be fitted using Equation 3.10, hence providing further confirmation on the validity of the trapping model for describing electron transport in ZnO transistors fabricated by spray pyrolysis.

Further evidence of the trap states controlled transport can be obtained from the evolution of V_T versus T shown in Figure 7.4(b). In this figure, V_T increases linearly with temperature all the way from 31.5 V to 11.5V. The temperature coefficient (KV_T) calculated from this set of data is found to be approximately -60mV/ K. This relatively high value suggests that the variation of V_T with temperature is the result of a thermally activated transport process and may be explained in terms of trapping and thermal activation of free electrons.

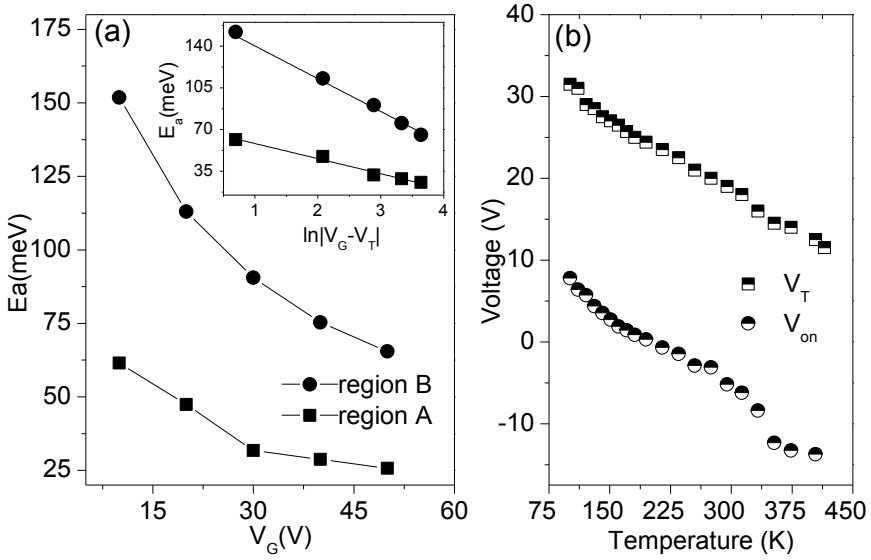

Figure 7.4: (a) Activation energy (E_a) of electron transport as a function of V_G in both low (region A; < 200°K) and high (region B; > 200°K) temperature regimes. Inset shows the same data fitted using Eq. 3.10 using a value for V_T = 12 V. (b) V_T and V_{on} as a function of measuring temperature.

At higher temperatures, more electrons can escape from the localized states, because of the increased emission rates and/or shorter trapping. This is manifested in smaller value for V_T i.e. the potential at which electron accumulation begins. Almost similar temperature dependence is observed for V_{on}. It is worth noting that the measured temperature dependences of μ and V_T are similar to those observed for poly-Si TFTs and commonly explained by invoking trapping and thermal activation of free carriers (37).

7.3 Electron transport in polycrystalline ZnO films

Polycrystalline semiconducting films are usually characterised by a large concentration of grain boundaries (GBs) the value of which depends on the mean

size of the crystalline domain which in turn depends on the material and the processing conditions during film growth. These GBs are commonly associated with potential barriers that tend to impede charge transport between the crystalline domains. Furthermore, GBs give rise to the formation of trap states within the band gap of semiconductors. For this reason charge transport is often described by charge trapping models that take into account the trap states; including their spatial and energy distributions. In the case of TOS, however, additional intrinsic defects such as oxygen vacancies and metal interstitials make charge transport analysis much more complex than in conventional polycrystalline semiconductors.

The two thermally activated mechanisms observed in the ZnO TFTs in Figure 7.4 requires the incorporation of a charge trapping process occurring predominantly at GBs, since the simple MTR model employs only a single thermal activation process (38). Several different transport regimes such as thermally activated transport, band like transport, and hopping through localised states have been observed in ZnO based materials whether polycrystalline or amorphous (11-13, 20, 25-27). In the case of polycrystalline metal oxide semiconductors, GBs induced potential barriers as well as ionised impurity scattering centres are the most likely scattering effects that dominate charge transport across devices based on these materials. However, the exact nature of the trap distributions and densities is difficult to evaluate as they strongly depend on the carrier concentration (39, 40) which in turn depends on the growth conditions. Given the polycrystalline nature of the spray pyrolysed ZnO films investigated in this work, it is reasonable to assume that the GB models can indeed be used to explain and analyse the different temperature regimes observed. In particular, in the high temperature regime it is suggested that de-trapping of carriers by thermionic emission dominates whereas at lower temperatures the dominant process becomes the thermally assisted tunnelling from the spatially narrow distribution of grain boundary trap states (41). Next we discuss the grain boundary scattering mechanism in detail.

7.3.1 Grain boundary scattering: Levinson plot for ZnO transistors

To elucidate the GB trapping our experimental data, measured at room temperature, have been analysed within the framework of the Levinson model. The latter model is an extension of Seto's model (42) for transport within polycrystalline materials that incorporate the gate-voltage dependence of the trap filling. In this model it is assumed that scattering at the GBs dominates inter-grain

transport but charges within the grains can reduce the GBs barrier and lead to higher average mobility values. As mentioned in Chapter 3, the model predicts that the plot of $\ln(I_D/V_G)$ versus $1/V_G$ results in a straight line. Although the Levinson plots of the high voltage appear to be in agreement with the theoretical fits [Figure 7.5], the low voltage data deviate from the ideal straight line behaviour. For this reason only the experimental data measured above V_T were used in order to calculate the trap density yielding a value on the order of $10^{12}/cm^{-2}$. The latter is in good agreement with values reported previously in the literature (39, 43-45).

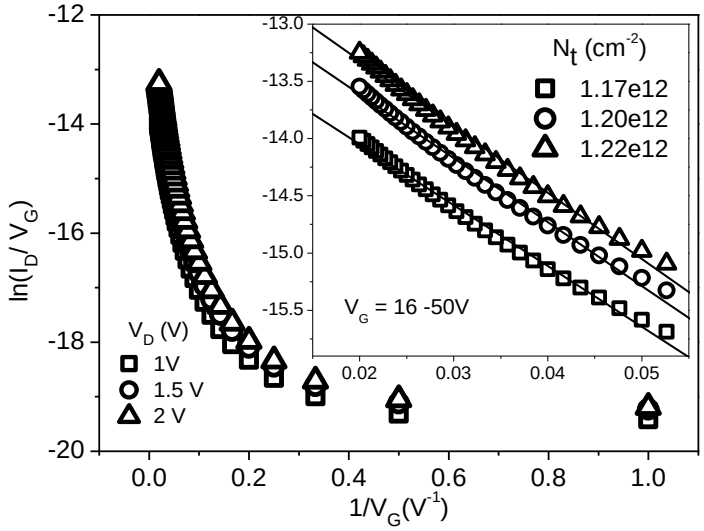

Figure 7.5: Levinson plots of data measured from a ZnO TFT with W/L= 1 mm/70 μm for three different V_D voltages in the linear regime. Data measured at 300 K. The inset shows linear fitting at V_G > 15 V. The calculated trap density is of the order of 10^{12} cm^{-2}.

7.3.2 Trap density comparison

To further understand GB trapping, trap densities were estimated from the evolution of V_T and subthreshold slope (SS) with temperature using Equations 3.29 and 3.27. From the slope of V_T against T plot, measured from the same ZnO TFT, the density of shallow trap states was estimated to be approximately 7.43×10^{13} eV^{-1} cm^{-2}. Additionally, evaluation of the trap density at 111 K using SS analysis yields a trap concentration on the order of 1.98×10^{13} eV^{-1} cm^{-2}. The latter value reduces to 4.79×10^{12} eV^{-1} cm^{-2} at 333 K. Both of these values are within the range of previously reported data for ZnO (46). At higher temperatures the applicability of the SS analysis becomes inaccurate due to the high transistor channel off-current. The variation between the trap concentrations calculated using the V_T and SS

approaches is attributed to the different trap energy regime being probed in each case.

7.3.3 Evaluation of the density of states in the band gap

Using the MTR model, the DOS [$N_t(E)$] within the band gap can be estimated from the temperature dependence of the electron field-effect mobility data. Following from Section 3.3.3, the density of trap states below the transport level/mobility edge can be estimated by differentiating V_G with respect to energy E_C–E_F (calculated using Equation 3.11) given as:

$$N_t(E) = \frac{C_i}{q}\frac{\partial V_G}{\partial E}. \qquad 7.1$$

In this case $\mu_o N_c$ is the parameter to be adjusted for consistent density of states over all temperatures. As shown in Figure 7.6, experimental data could not be fitted using a single value for $\mu_0 N_C$. In particular, for T < 200 K $\mu_0 N_C$ was found to be around 3.9×10^{13} V^{-1} s^{-1} while for temperatures >200 K, $\mu_0 N_C$ was slightly higher and equal to 5.1×10^{13} V^{-1} s^{-1}. Even then the data could not be fitted accurately for either temperature regime. It should also be noted that a double exponential distribution of states was observed similar to those observed in other polycrystalline systems (47).

Both shallow and deep level traps are characterised by broader distributions having widths of ~ 47 meV and ~ 76 meV, respectively. The density of shallow states is equal to 6.73×10^{13} eV^{-1} cm^{-2} at around $3kT$ from the mobility edge and is comparable to the one found employing V_T analysis. It can thus be concluded that the model for the temperature dependence of V_T is valid, at least for this particular case. Deeper trap states have a lower density in agreement with the previous values obtained using the SS analysis.

The trap distribution widths calculated earlier using the Meyer-Neldel energy assumed a single exponential distribution which resulted in a wider trap distribution than both the shallow and deep values of kT_0 calculated here. However, since the trap distribution could not be fitted across the entire temperature range investigated (i.e. failed at higher temperatures), the mobility edge model does not seem to be appropriate for this case. Instead, GB trapping with two thermally

activated charge transport mechanisms and hence two different fits for $\mu_0 N_C$ are required.

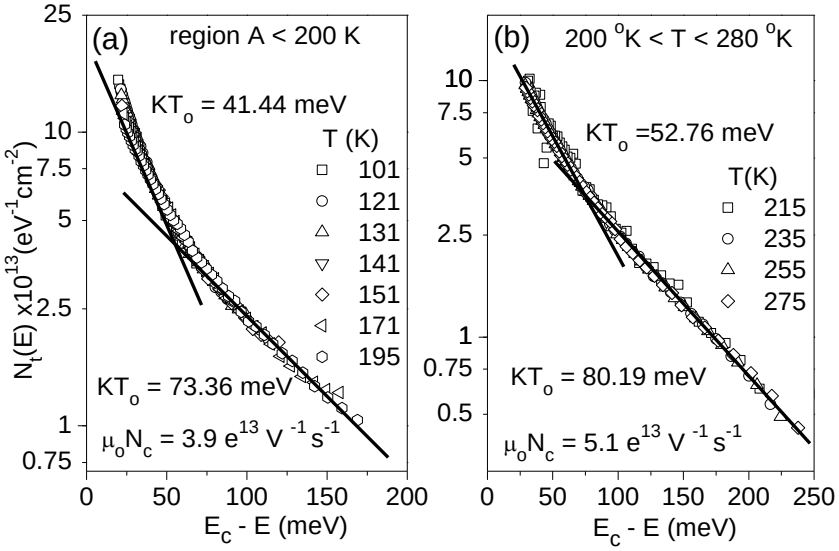

Figure 7.6: Estimation of the density of states below the conduction band edge E_c for a ZnO TFT fabricated by spray pyrolysis. The data are fitted using a mobility edge model. The best fits for $\mu_o N_c$ are shown for low (a), and high (b) temperatures. A double exponential distribution is observed with different distribution widths (kT_o). No consistent fit could be found out for temperatures higher than 275°K.

7.4 Summary

In summary, we have fabricated transistors based on ZnO films grown by spray pyrolysis at 400°C. The electrical properties of the devices (i.e. V_T and average electron mobility), have been studied as a function of temperature. By increasing the temperature from 101 K to 415 K, the ZnO transistor threshold voltage was found to shift towards more negative V_G bias. This was attributed to an increasing concentration of thermally activated electrons. The activation energy E_a for these electrons has been calculated to be on the order of ~61.45 meV and 151.81 meV for two different thermally competing transport regimes. These findings have been explained by invoking a grain boundary trapping process incorporated into the multiple trapping and release model. The two models were also used to calculate, independently, the density of shallow and deep electron trap states. The values obtained ~ 10^{12} and 10^{13} $cm^{-2}eV^{-1}$ are in good agreement with values reported previously for ZnO films grown by different methods.

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Chapter 8

Ambient and bias-stress stability of ZnO transistors

Abstract

As already discussed, ZnO shows great promise as the active layer in thin-film transistors for a host of future electronic applications, offering the possibility for high performance as well as simple and scalable processing. Implementation of the technology in large scale electronics, however, will depend a great deal on the reliability of these ZnO devices. Therefore, the ambient and electrical stability of devices is considered to be one of the key issues for the successful development of any future ZnO based electronics. This chapter presents a study concerning the influence of storage time (in air) as well as bias-stressing on the electrical characteristics of thin-film transistors based on ZnO films grown by spray pyrolysis at 400 °C in ambient air.

8.1 Introduction

Following recent breakthroughs in the field of transparent oxide semiconductors, a change in the future direction of electronic display technology and optoelectronic devices is highly anticipated (1). Recent reports of TFTs utilising ZnO based semiconductors have already shown promising electrical and optical properties, including high transparency (>80%), high charge carrier mobility (>20 cm^2/Vs) as well as excellent I_D on-off ratios (>10^7), utilising both opaque and transparent substrates (2-8). Of particular note is the insensitivity of ZnO to visible light, which typically causes degradation in silicon (Si) based devices through photo generation of defects. However, ZnO based devices with their many advantages will still need to demonstrate a level of reliability and stability comparable to that of conventional amorphous Si (a-Si) TFTs before they can be utilised in the next generation optical displays as well as various other opto-/electronic applications.

At present there are only few reports in the literature evaluating the electrical stability of ZnO based devices. Early investigations into devices fabricated by magnetron sputtering and bias-stressed with a gate bias (V_G) of 50 V for 10^4 s, show a shift in threshold voltage (V_T) of approximately 40 V. This shift is attributed to trap states arising from bond breaking at the lattice mismatched ZnO/SiO_2 interface when the gate bias voltage is applied (9). Recently Seokhwan *et al* have suggested that incorporation of an additional processing step, such as a thermal annealing following oxide growth, can significantly reduce the V_T shift during electrical stressing (10). This improvement is believed to be due to an incorporation of oxygen species, improving the semiconductor structure in terms of stoichiometry and also altering the quality of the semiconductor/dielectric interface. In another study by Ahn *et al.*, doping of ZnO with Al has also been found to improve device stability through microstructural changes in the active film (11).

In the case of solution processed ZnO TFTs, it has recently been demonstrated that the bias-stability may be significantly influenced by the type and relative concentration of the defects present in the semiconducting layer (9, 12). Therefore, studying, understanding and improving the operating stability of TFTs is of paramount importance and key to any future developments. In this chapter we

study; (i) the impact of storage time of the devices in ambient air, and (ii) the effect of prolonged bias-stress on the performance characteristics of ZnO transistors fabricated by spray pyrolysis.

8.2 Experimental details

The devices used for this study utilise a bottom-gate staggered structure fabricated on Si^{++} wafer, using ZnO as the semiconductor layer deposited by spray pyrolysis (SP) at temperatures around 400°C. Aluminium was deposited as source and drain (S-D) contacts by thermal evaporation under high vacuum. To evaluate the effect of time dependent stressing, measurements were performed in dark conditions at room temperature (RT) directly after fabrication and at set intervals across a 20 month period. Devices were stored in a storage box in ambient air, whilst no encapsulation was used to protect the devices from environmental factors such as humidity and various other atmospheric oxidants. For electrical stressing, similarly structured ZnO TFTs were tested in the dark and under vacuum, with a constant gate bias for up to 60 kilo-seconds (ks). Subsequently, the relaxation behaviour of the TFTs was also monitored under vacuum and over the same period of time.

8.3 Temporal evolution of ZnO transistor characteristics

Figure 8.1 displays the transfer characteristics of a ZnO TFT measured immediately after fabrication (Day 1) and after 20 months of exposure to ambient air (the relative humidity, RH, was in the range 30-60 % but was not monitored). It is to be noted that the devices were not encapsulated and no protective coating was used.

All electrical measurements were performed with the devices biased in the saturation regime (drain voltage, V_D = 40 V) in order to avoid any parasitic contact effects. The operating characteristics of the TFTs were measured at regular time intervals to allow the evolution of the various device parameters including, saturation mobility (μ_{SAT}), V_T, current on/off ratio and subthreshold swing (SS), to be monitored as a function of exposure time. A representative set of these results are shown in Figure 8.2. It can be seen that apart from the observed drop in the current on/off ratio the rest of the device parameters seem to improve with exposure time. Specifically, the conductivity of the transistor channel increases, as

evident by the increase of I_D at $V_G = 0$ V, leading to an improvement in μ_{SAT} as well as a negative shift in V_T. The former was found to increase from below 2 V to approximately 10 cm^2/Vs, while the latter has shifted from 25 V to 13 V over the exposure period of 20 months.

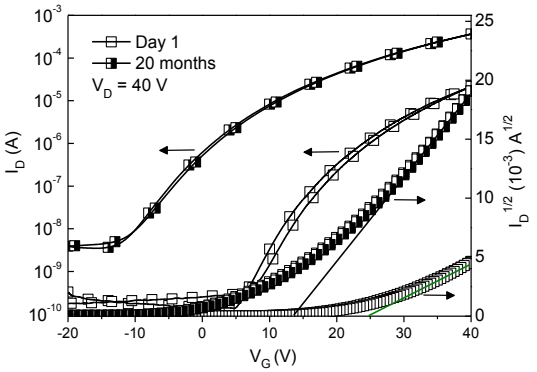

Figure 8.1: Transfer characteristics of a ZnO TFT (W/L = 20) fabricated by SP at 400°C. The TFT was measured immediately after fabrication and after 20 months storage in ambient air.

The increase in conductivity can be attributed to the ZnO film not being passivated/ encapsulated, leading to possible incorporation of defects/impurities caused by various compounds adsorbed from the ambient air. Moreover, it can be seen in Figure 8.2(a) that the current on/off ratio of the transistor increases during the initial ~ 30 days of exposure, but then decreases by an order of magnitude to nearly its initial value. This is possibly due to increase in on current as a result of increased conductivity but after 30 days of exposure the off current becomes

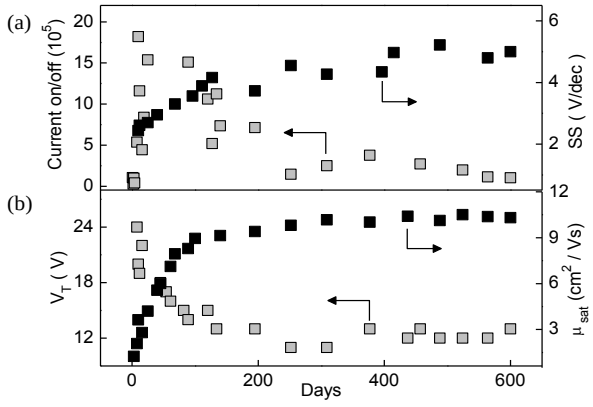

Figure 8.2. a) Evolution of the current on/off ratio and SS with exposure time. b) Evolution of electron mobility (measured in saturation), and V_T with exposure time.

worse and worse thereby degrading the on-off ratio. A possible explanation is that exposure time to air leads to physisorption of various molecules present in the air (water etc.) which may be responsible for the observed rise in the off -current of the transistor, hence leading to a deterioration in the current on/off ratio. Elucidation of the exact origin of this effect however will require further work on the effects of individual oxidants on the transport characteristics of ZnO and is beyond the scope of this work.

A further interesting feature is the increase in the SS from 2.44 V/dec to 5 V/dec [Figure 8.2(a)] with increasing exposure time, possibly indicating an increase in the trap density at the semiconductor-insulator interface. The latter was calculated directly from the SS using Equation 3.27 and was found to increase from 2.1×10^{12} $cm^{-2}eV^{-1}$ to 4.3×10^{12} $cm^{-2}eV^{-1}$. This is not surprising since similar behaviour has been observed previously for ZnO based devices (13, 14).

The increase in μ_{SAT}, on the other hand, could be due to trap screening (i.e. trap filling) by extra electrons induced by desorption of various atmospheric molecules possibly leading to a reduction in the barrier height between grain boundaries across the ZnO film. Consequently, V_G induced electrons are free to drift across the ZnO channel faster since they encounter much fewer scattering centres (i.e. traps). A summary of the extracted transistor parameters for different periods of exposure is presented in Table 8.1.

Testing conditions	μ_{SAT} (cm^2/Vs)	V_T (V)	SS (V/dec)	Current on/off ratio
Initial state	1.2	25	2.44	1×10^5
10 months	9.8	11	3.73	1.4×10^5
20 months	10.4	13	5	1×10^5

Table 8.1. Influence of exposure time on the electrical parameters of ZnO transistors fabricated using spray pyrolysis before exposure (initial state) and after 10 and 20 months of exposure to air.

8.4 Bias-stress characteristics of ZnO transistor

The observed shift in V_T is often used to quantify the electrical instability of thin-film transistors. Such shift is often observed in devices subjected to bias stress (i.e. constant voltage/current conditions) for extended periods of time. For

example, during constant gate bias, a decrease in channel conductance can be observed, or in other words a decrease in the drain current. The lesser the shift, the more stable the device is considered to be. Likewise, recovery of V_T in the off state i.e., under no bias conditions, holds equal importance for assessing device stability/stress-reversibility.

In order to assess the bias stability of the devices we have studied the effect of continuous gate bias stress on the transfer characteristics of ZnO TFTs fabricated by spray pyrolysis. The bias stress method requires a voltage be applied only to the gate, while source and drain contacts are kept grounded to ensure a uniform electric field across the transistor channel interface. The transfer characteristics are then recorded at V_D = 10 V at set times, during which the gate bias stressing is interrupted. This is carried out over a period of 60 ks. The relaxation characteristics (recovery) of the transistor are then measured after the stressing period, and after all three terminals (i.e. G, S, D) have been grounded. The following section presents and discusses the results obtained from these bias-stress studies.

8.4.1 Electrical characteristics of ZnO transistors under gate bias

Figure 8.3 displays the transfer characteristics for a ZnO TFT obtained before (initial state) and after (60 ks) bias-stress at V_G = 40 V. Clearly, bias-stress results in a pronounced shift in the V_T towards more positive values followed by a reduction in the current on-off ratio. However, the decrease in on current is much less in magnitude when compared to the increase in the off current. During recovery, the transfer curve shifts back to its original state, but only after 30 ks. For longer recovery times (60 ks) a small negative shift, as compared to initial state, in V_T is observed. Therefore, it can be concluded that the device fully recovers to its initial pre-stress electrical state. The same is true for SS which is found to shift from 3.2 V/dec to 2.4 V/dec. The latter however occurs at even shorter time scales than other parameters (it fully recovers after 20 ks of recovery time).

In order to quantify the stress/recovery process observed in our spray pyrolysed ZnO TFTs, the time dependent behaviour of ΔV_T was studied. Figure 8.4 shows the stress-recovery of ΔV_T for time periods up to 60 ks. A significant increase in ΔV_T during the initial stressing period is observed, followed by a subsequent plateau with further stressing. The same is true for the post stress

relaxation phase. The initial shift in V_T decreases rapidly, but then recovers relatively slowly toward its initial state after 35 ks.

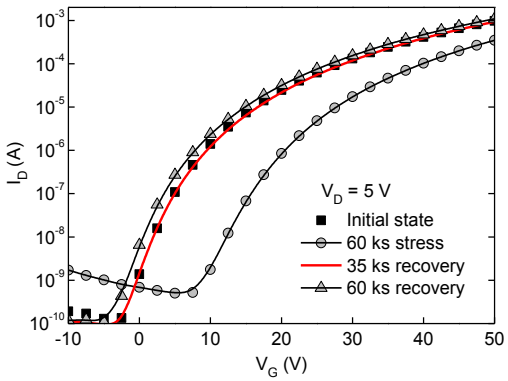

Figure 8.3: Transfer characteristics measured immediately after fabrication (initial state), after stressing (using V_G = 40 V for 60 ks) and after relaxation (recovery) for 30 ks and 60 ks. Relaxation is achieved by biasing the device at V_G = 0 V. The device dimensions used in this experiment are L/W= 70/2000 µm.

The instability mechanism can best be studied through the use of stretched exponential equations (Equations. 8.1, 8.2 below) which are often employed to provide some understanding of relaxation phenomena in disordered semiconductors (15). The applicability of the latter approach to various metal oxides as well as organic semiconductor based transistors has been demonstrated in recent years by many groups (16, 17). The model can provide an account of defect creation and charge trapping mechanisms, during both bias-stressing as well as relaxation i.e. recovery. These stretched exponential equations are given as:

$$\Delta V_T = \Delta V_{T\infty}\left[1-\exp\left(-\left(\frac{t}{\tau}\right)^{\beta}\right)\right] \qquad 8.1$$

$$\Delta V_T = \Delta V_{T,M}\left[\exp\left(-\left(\frac{t}{\tau}\right)^{\beta}\right)\right]. \qquad 8.2$$

Here, $\Delta V_{T\infty} = [V_T\ (t = \infty) - V_T\ (t = 0)]$ and $\Delta V_{T,\,M}$ represent threshold variation at the maximum and at the beginning of relaxation phase, respectively. The parameter β ($0 < \beta \leq 1$) is known as a dispersion parameter and accounts for the width of the involved trap distribution, or the distribution of time constants that characterize the charge trapping process. The distribution (time constants) are narrower when $\beta \sim 1$

and broader if $\beta < 1$. Accordingly, ΔV_T follows an exponential function or a trend slower than the exponential function. Finally, τ is the thermally activated trapping time of charge carriers.

Figure 8.4 shows the time evolution of the threshold voltage shift (ΔV_T) for gate bias-stress values of 40 V during stressing and recovery phases. It can clearly be seen that the experimental results are in good agreement with the stretched-exponential equations 8.1 and 8.2. The fitting parameters β and τ are shown as inset in Figure 8.4 for both stress and recovery, phases. The value of τ is calculated to be approximately 19 ks and 13 ks, for stress and recovery, respectively. It can therefore be concluded that de-trapping of carriers is faster when compared to the trapping process. These trapping and de-trapping processes may also be associated with adsorption and desorption of ambient oxygen, and/or other atmospheric molecules, into the ZnO film. To this end, it has been suggested that a more oxygen rich environment during bias-stressing would result in higher de-trapping times, since without a catalyst (i.e. no gate bias), the desorption of oxygen becomes more difficult and slower (18).

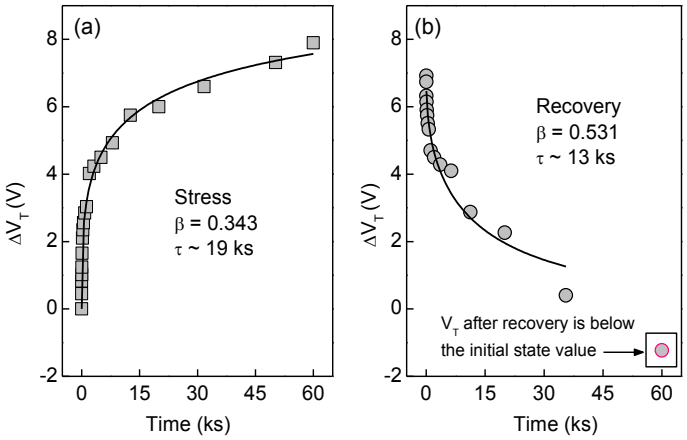

Figure 8.4: Time evolution of the threshold voltage shift (ΔV_T) for gate bias stress values of 40 V during; (a) stressing and (b) recovery. The solid lines show the fitting to the stretched exponential function (Eqs. 8.1, 8.2).

Since all measurements reported here were performed under high vacuum, the ZnO transistors exhibit relatively short recovery time possibly because of the low oxygen concentration. The same measurements also suggest that injected electrons are not localised in energetically deep states and can easily be activated back to the transport energy level. The value of β obtained is also found to be less

than unity, both for stress and recovery phases, depicting a slower exponential for ΔV_T. Finally, the instability in electron mobility with stressing time is also found to be reversible, as illustrated in Figure 8.5. Interestingly, the mobility value continues to decrease with increasing stress time but is found to recover to its initial value after approximately 35 ks of relaxation period.

It is important to note that in previous bias-stress studies performed on ZnO transistors fabricated by sputtering, Equations 8.1-8.2 were applied using a logarithmic dependence of ΔV_T with time (16, 19). Furthermore, these earlier studies reported irreversible bias-stressing (16, 18) or some degree of recovery was achieved through the use of a post-processing step such as annealing or chemical doping (10, 11, 20, 21). It can therefore be concluded that in the present work the fitting of a stretched exponential on a linear scale reflects a much better quality fit. The latter is most likely attributed to smaller energetic/spatial disorder within the spray pyrolysed ZnO film, which may also be the reason for the high carrier mobilities measured in these devices.

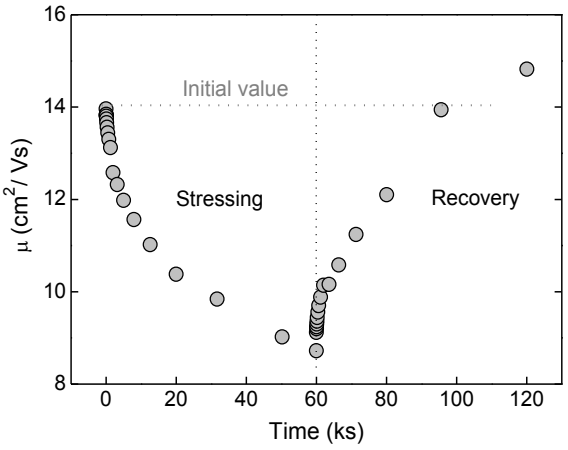

Figure 8.5: Electron mobility for a ZnO transistor measured as a function of bias stressing (V_G = 40 V) and recovery (V_G = 0 V) time. All measurements were obtained at a V_D = 10 V.

8.5 Summary

In this chapter we have presented and discussed preliminary results on the ambient and bias-stress stability of transparent ZnO TFTs fabricated by spray pyrolysis in ambient air. The transistors exhibited excellent performance characteristics for exposure times to ambient air up to 20 months, even though no encapsulation or any passivation layers were employed. Electrical parameters such

as carrier mobility and threshold voltage were found to improve with an exception of the current on/off ratio of the device which reduced. These effects were attributed to the increased conductivity (i.e. increased free electron concentration) of the ZnO films resulting, possibly, from physisorption of atmospheric chemicals such as water and oxygen onto ZnO films.

We have also shown, through stress-recovery experiments, that a positive shift in the threshold voltage of the transistors is predominantly due to charge trapping at the semiconductor-dielectric interface, resulting from adsorbed negatively charged oxygen molecules present in ambient air. However, the recovery behaviour of V_T without any thermal annealing, i.e. thermal activation, excludes the possibility of charge injection and trapping into the gate dielectric (SiO_2). The time dependence of the shift of V_T was found to follow a stretched exponential model under gate bias stressing conditions. Moreover, the devices exhibit faster recovery behaviour, possibly due to less oxygen being present in the atmosphere (i.e. vacuum) during testing. This also suggests that defect creation is not the dominant process. We conclude that ZnO TFTs prepared by spray pyrolysis have a promising outlook with regards to their environmental stability as well as bias-stress induced stability.

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Chapter 9

Summary of results and future outlook

In this thesis the applicability of a simple solution-based deposition technique, namely spray pyrolysis (SP), for the fabrication of high performance ZnO semiconducting films, is demonstrated. The core part of the work describes the growth and application of solution processed ZnO films in optimised discrete thin-film transistors as well as microelectronic applications such as logic gates. Importantly, it is the first study to demonstrate working transistors prepared by spray pyrolysis and one of the first to investigate other important device properties such as charge carrier transport, shelf lifetime and bias-stress stability. Because of the holistic approach adopted in this work (i.e. from unconventional processing methodologies and materials development all the way to device and circuit fabrication) the thesis represents an important step towards the development of a high performance, scalable and simple to fabricate thin-film transistor technology based on oxide semiconductors. Important findings reported in this thesis include:

- First demonstration of the use of spray pyrolysis for the fabrication of metal oxide thin-film transistors, and particularly ZnO transistors, and integrated circuits such as unipolar voltage inverters.
- First demonstration of low-voltage, low-power thin-film transistors and unipolar logic gates through a combination of thermally stable solution-

processed self-assembled monolayer (SAM) nano-dielectrics and spray pyrolysed ZnO semiconducting films.

- First demonstration of novel high mobility n-channel, p-channel as well as ambipolar hybrid transistors based on a phase separated organic blend layer as the p-type material and a spray pyrolysed ZnO layer as the n-type material. By integrating two of these hybrid heterostructure transistors, complementary logic inverters with high noise margin and signal gain have also been demonstrated.
- Study of the temperature dependence of electron transport in ZnO based transistors. These measurements helped elucidating the electron trapping processes and particularly the role of grain boundaries.

The main findings reported in this thesis are summarised next. Chapter 5 demonstrated the applicability of spray pyrolysis for the fabrication of high quality ZnO films in ambient air. As-grown films in the temperature range 200-500°C, are found to be highly transparent (>85 %) as well as polycrystalline in nature thus confirming the possibility of depositing high quality films onto large area substrates using this low cost and scalable deposition method. A detailed material study of as-prepared ZnO films was conducted aiming at elucidating the effect of deposition temperature on the film's microstructure and electronic properties. Higher deposition temperatures were found to produce ZnO films with larger crystalline domains and better performing transistors. The latter was attributed to fewer grain boundaries present in films with larger crystalline domains. Using these spray pyrolysed ZnO films, high mobility (25 cm^2/Vs) thin-film transistors were also demonstrated further confirming the applicability of SP for the growth of high performance oxide electronics. The maximum electron mobility measured from these devices is amongst the highest values reported to date for ZnO transistors processed by either solution or vacuum-based techniques.

Another important issue addressed in this work is the prevailing high operating voltage characteristics of the vast majority of metal oxide transistors reported to date. This technological bottleneck was successfully addressed through the use of solution processable phosphonated self-assembled monolayers (SAMs) as ultra thin (<3 nm) gate dielectrics. The superior thermal stability of this family of SAMs enabled the use of spray pyrolysis for the growth of polycrystalline ZnO

films directly onto the organic monolayer. Using a combination of contact angle and current-voltage measurements it was established that phosphonic SAMs are stable to processing temperatures up to 450°C. Optimised SAM based ZnO transistors were found to operate at biases in the range 1-2 V and exhibit mobilities comparable to devices based on SiO_2. Similar to SiO_2 based ZnO transistors, an increase in electron mobility with increasing processing temperature was observed. By integrating two such low-voltage ZnO transistors, the first low-voltage unipolar inverter based on ZnO has also been demonstrated. These developments clearly demonstrate the applicability of our technology for practical device applications.

The use of spray pyrolysis for realising alternative device configurations, such as top-gate (TG) and dual-gate transistors has also been investigated. By utilising an organic solution processable fluoropolymer, namely CYTOP, as the top-gate dielectric, the effect of the different surface nanomorphology of the ZnO, as compared to the bottom SiO_2/ZnO interface, has been investigated. Top-gate ZnO transistors are found to exhibit reduced electron mobility as compared to bottom-gate devices. The introduction of an additional oxygen plasma treatment step of the top ZnO surface, prior to CYTOP deposition, was found to induce significant changes to the electrical characteristics of TG ZnO transistors. The latter observation was attributed to the altered stoichiometry of ZnO surface following oxygen plasma treatment. Based on the same material combination, dual gate ZnO transistors have also been demonstrated. The devices exhibit improved operating characteristics when biased in dual-gate mode (i.e. the two gates connected together). Such advantageous device architectures could one day be explored for the manufacturing of transistors with high current driving capabilities (e.g. current-driven organic light-emitting diode (OLED) displays).

Chapter 6 described the development of ambipolar hybrid heterostructures and their use in p-channel, n-channel, as well as ambipolar transistors with balanced carrier mobilities. This was achieved by realising a novel device architecture consisting of an organic semiconducting blend as the p-type layer and a ZnO film as the n-type layer. Importantly, this versatile hybrid heterostructure can be processed from solution in ambient air. The maximum hole and electron mobilities extracted from optimised hybrid transistors were approximately equal and over 2 cm^2/Vs. Most importantly, the hybrid devices are stable when stored in air without noticeable degradation in either hole or electron accumulation regimes.

By integrating two such hybrid transistors, logic inverters based on complementary circuitry have also been demonstrated. The hybrid circuits exhibit near ideal operating characteristics such as wide noise margins and high signal gain. Importantly, the inverter characteristics resemble closely those of truly complementary circuits hence making these hybrid devices an excellent candidate technology for application in future large-area electronics.

In Chapter 7 the charge transport processes in optimised spray pyrolysed ZnO based thin-film transistors have been investigated using temperature dependence current-voltage measurements. Thermally activated electron transport was observed and was found to exhibit two distinct temperature regimes separated at around 200 K. Electron transport in the high-temperature regime was modelled using the multiple trapping and release (MTR) model by invoking the effects of grain boundaries. The latter, enabled calculation of the trap distribution widths, trap energy levels and trap densities. The low temperature regime exhibited lower activation energies when compared to high temperature regime. Electron transport in this regime could not be modelled by a simple MTR model. It was proposed that at low temperatures some form of thermally assisted tunnelling process at grain boundaries is dominating over a purely thermal activation mechanism. This important grain boundaries influence was further confirmed by invoking the Levinson model. The density of states calculated using this model was in good agreement with values reported in the literature for ZnO films grown by different methods.

Finally, Chapter 8 presented some preliminary results on the ambient and bias-stress stability of ZnO transistors fabricated by spray pyrolysis. Surprisingly, the performance of the devices is found to improve upon exposure to ambient air for up to 20 months as evident by the increased electron mobility over this period. Upon electrical stressing the threshold voltage (V_T) of the transistors was found to shift towards more positive gate voltages. The latter was attributed to the creation of electron traps at the semiconductor/SiO_2 interface. These results suggest that ZnO TFTs prepared by spray pyrolysis represent a promising technology that is able to deliver devices with high carrier mobilities as well as promising environmental and bias stability.

Future Research Directions

Undoubtedly successful development of ubiquitous electronics based on oxide semiconductors that are processed by spray pyrolysis would require an improved understanding of the film growth dynamics and its effect on the film's microstructure, the various charge transport processes and the effects of ambient oxidants on the electrical stability of discrete devices as well as integrated systems. Although this thesis addresses some of these key issues, significant work would still be required before spray pyrolysis can be fully exploited for real device applications. A few critical areas on which further research would be required are listed below.

- Development of fully automated spray pyrolysis systems. The latter would enable scaling of oxide film processing over large areas with high reproducibility.
- Study of the film growth dynamics during spray pyrolysis and the role of the various processing parameters including; concentration of the precursor in the solution, substrate temperature, deposition angle, nozzle speed, feed flow rate of the precursor solution into the nozzle and the effect of the propellant gas on the electronic properties of the deposited oxide layer.
- Development of hole transporting metal oxide semiconductors with performance characteristics comparable to those of n-type oxides. Hole transporting oxides is a key enabling technology for the development of high performance complementary circuits for a host of applications.
- Development of low processing temperature precursors for the growth of semiconducting and insulating oxides. Availability and combination of such materials would enable the manufacturing of all-oxide electronics on low cost, flexible substrates such as plastic. To date low temperature oxides processed from solution have proven difficult and exhibit marginal performance.

Appendix A

List of publications

Journal articles

George Adamopoulos, Aneeqa Bashir, William P. Gillin, Stamatis Georgakopoulos, Maxim Shkunov, Mohamed A. Baklar, Natalie Stingelin, Donal D. C. Bradley, and Thomas D. Anthopoulos. '*Structural and Electrical Characterization of ZnO Films Grown by Spray Pyrolysis and Their Application in Thin-Film Transistors'* Advanced Functional Materials 21, 525 (2011).

George Adamopoulos, Aneeqa Bashir, Stuart Thomas, William P. Gillin, Stamatis Georgakopoulos, Maxim Shkunov, Mohamed A. Baklar, Natalie Stingelin, Robert C. Maher, Lesley F. Cohen, Donal D. C. Bradley, and Thomas D. Anthopoulos. '*Spray-Deposited Li-Doped ZnO Transistors with Electron Mobility Exceeding 50* cm^{2}/Vs*'* Advanced Materials 22, 4764 (2010).

Jeremy Smith, Aneeqa Bashir, George Adamopoulos, John E. Anthony, Donal D. C. Bradley, R. Hamilton, Martin Heeney, Iain McCulloch, and Thomas D. Anthopoulos. '*Air-Stable Solution-Processed Hybrid Transistors with Hole and Electron Mobilities Exceeding 2* $cm^{2} V^{-1} s^{-1}$*'* Advanced Materials 22, 3598 (2010).

George Adamopoulos, Aneeqa Bashir, Paul H. Wöbkenberg, Donal D. C. Bradley, and Thomas D. Anthopoulos. '*Electronic properties of ZnO field-effect transistors*

fabricated by spray pyrolysis in ambient air' Applied Physics Letters 95, 133507 (2009).

Aneeqa Bashir, Paul H. Wo¨bkenberg, Jeremy Smith, James M. Ball, George Adamopoulos, Donal D. C. Bradley, and Thomas D. Anthopoulos. '*High-Performance Zinc Oxide Transistors and Circuits Fabricated by Spray Pyrolysis in Ambient Atmosphere'* Advanced Materials 21, 1 (2009).

Patents

Thomas Anthopoulos, Donal Bradley, Aneeqa Bashir, Paul Henrich Wobkenberg, US Patent Application US/2011/0113859 A. Low voltage thin-film field effect transistors.

Conference presentations

Aneeqa Bashir, Paul H. Wöbkenberg, George Adamopoulos, Donal D.C. Bradley and Thomas D. Anthopoulos. Solution-Processed ZnO Films for Transistor Applications (poster), at The 7th International thin-film transistor Conference, Cambridge, UK, 2011.

Aneeqa Bashir, George Adamopoulos, Stuart Thomas, Donal D. C. Bradley, and Thomas D. Anthopoulos. Spray-deposited Li-doped ZnO thin-film transistors with electron mobility exceeding 50 cm^2/Vs (Oral), at The Society for Information Display (SID) conference, London, UK, 2010.

Aneeqa Bashir, Paul H. Wöbkenberg, Jeremy Smith, James Ball, George Adamopoulos, Donal D.C. Bradley, Thomas D. Anthopoulos. ZnO Transistors and Circuits Fabricated by Spray Pyrolysis (poster) at E-MRS spring meeting Symposium F: Advances in Transparent Electronics: From Materials to Devices, Strasbourg France, 2009.