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Quantum Corrections to the 'Atomistic' MOSFET Simulations

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We have introduced in a simple and efficient manner quantum mechanical corrections in our 3D 'atomistic' MOSFET simulator using the density gradient formalism. We have studied in comparison with classical simulations the effect of the quantum mechanical corrections on the simulation of random dopant induced threshold voltage fluctuations, the effect of the single charge trapping on interface states and the effect of the oxide thickness fluctuations in decanano MOSFETs with ultrathin gate oxides. The introduction of quantum corrections enhances the threshold voltage fluctuations but does not affect significantly the amplitude of the random telegraph noise associated with single carrier trapping. The importance of the quantum corrections for proper simulation of oxide thickness fluctuation effects has also been demonstrated.

Keywords: Doping; Fluctuations; MOSFET; Device simulation; Silicon devices; Threshold; Quantum; Density-gradient

1. INTRODUCTION

The scaling of MOSFETs in integrated circuits is reaching the stage where the granularity of the electric charge and the atomicity of matter start to introduce substantial variation in the characteristics of the individual devices and has to be included in the device simulations. The variation in number and position of dopant atoms in the active region of the decanano MOSFETs introduces significant variations in the device characteristics [1]. At the same time the thickness of the gate oxide becomes equivalent to several atomic layers with a typical interface roughness of the order of 1–2 atomic layers [2]. This will introduce more than 50% variation in the oxide thickness within an individual transistor and will make the transistors microscopically different in terms of oxide thickness pattern as well. The trapping/detrapping of individual charges at the interface also will have a dramatic effect on the current in such devices [3].

The statistical variations in the decanano devices shift the paradigm of the numerical device simulations. It is no longer sufficient to simulate a single device with continuous doping distribution, uniform oxide thickness and unified dimensions to represent one macroscopic design. Each device is microscopically different at the level of dopant

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distribution, oxide thickness and gate pattern, so an ensemble of macroscopically identical but microscopically different devices must be characterised. The simulation of a single device with random dopants, oxide thickness and gate pattern variation requires essentially a 3D solution with fine grain discretisation. The requirement for statistical interpretation transforms the problem into a four dimensional one where the fourth dimension is the size of the statistical sample [4].

At the same time the increase in doping concentration and the reduction in the oxide thickness in decanano MOSFETs results in a strong quantization in the inversion layer and a corresponding threshold voltage shift and oxide capacitance degradation [5]. However traditionally the 3D simulation studies of random dopant fluctuation effects [4, 6–8] use drift-diffusion (DD) approximation and do not take into account quantum effects. Until recently [9] it was unclear to what extent the quantum effects may enhance or reduce the variations in the device characteristics associated with random dopant, and oxide thickness fluctuation and the effects associated with trapping/detrapping of individual interface charges.

In this paper we study the influence of the quantum effects in the inversion layer on the parameter fluctuations in decanano MOSFETs. The quantum mechanical (QM) effects are incorporated in our previously published 3D 'atomistic' simulation approach [4] using a 3D implementation of the density gradient (DG) formalism. This results in a 3D, QM picture which incorporates the vertical inversion layer quantization, lateral confinement effects associated with the current filamentation in the valleys of the potential fluctuation, and eventually tunnelling through the sharp potential barriers associated with individual dopants.

2. IMPLEMENTATION OF DG APPROACH IN 3D 'ATOMISTIC' SIMULATIONS

The DG model is an approximate approach for introducing quantum mechanical corrections into the macroscopic drift-diffusion approximation by considering a more general equation of state for the electron gas, depending on the density gradient. It has been demonstrated in [10] that, to lowest order, the quantum system behaves as an ideal gradient gas for typical low-density and high-temperature semiconductor conditions. Quantum corrections have been included in the DD simulations by introducing an additional term in the carrier flux expression:

$$F_n = n\mu_n \nabla\psi - D_n \nabla n + 2\mu_n \nabla\left(b_n \frac{\nabla^2\sqrt{n}}{\sqrt{n}}\right) \quad (1)$$

where $b_n = \hbar/(12qm_n^*)$, and all other symbols have their usual meaning. One possible approach [12] to avoid the discretisation of fourth order derivatives when using (1) in multidimensional numerical simulations is to introduce a generalised electron quasi-Fermi potential ϕ_n, as follows:

$$F_n = n\mu_n \nabla\phi_n \quad (2)$$

Thus the unipolar DD system of equations with QM corrections, which in many cases is sufficient for MOSFET simulations, becomes:

$$\nabla\cdot(\varepsilon\nabla\psi) = -q(p - n + N_D^+ - N_A^-) \quad (3)$$

$$2b_n \frac{\nabla^2\sqrt{n}}{\sqrt{n}} = \phi_n - \psi + \frac{kT}{q}\ln\frac{n}{n_i} \quad (4)$$

$$\nabla\cdot(n\mu_n\nabla\phi_n) = 0 \quad (5)$$

where ψ, ϕ_n and $\sqrt{n}$ are independent variables. Compared to the conventional DD simulations the DG approach increases the number of equations by one for each type of carriers. However we have restricted our simulations to low drain voltage which allows us to disentangle Eqs. (3) and (4) from Eq. (5) by considering a quasi-constant quasi-Fermi level. First we solve self-consistently the 3D Poisson equation (3) for the potential and Eq. (4), which can be considered as a DG approximation of Schrödinger's equation, for the electron concentration. Standard boundary

conditions are used for the potential in the Poisson equation (3) with zero bias applied at the source and drain contacts. Dirichlet boundary conditions are applied to the electron concentration in the DG equation (4) at the contacts and Si/SiO_2 interface introducing charge neutrality and vanishing small values respectively, and Neumann boundary conditions are applied at all other boundaries of the solution domain.

Knowing the electron concentration from the selfconsistent solution of Eqs. (3) and (4), and following the procedure described in [4] we extract the current from the resistance of the MOSFET by solving the drift approximation of Eq. (5):

$$\nabla \cdot \mu_n n \nabla V = 0 \tag{6}$$

in a thin slab near the Si/SiO_2 interface engulfing the inversion layer charge. Dirichlet boundary conditions are applied for the 'driving' potential V at the source and drain contacts with $V=0$ and $V=V_D$ respectively and Neumann boundary conditions are applied at all other boundaries of the slab. We have demonstrated in [4] that at low drain voltage this approach is in excellent agreement with the full self-consistent solution of the DD equations.

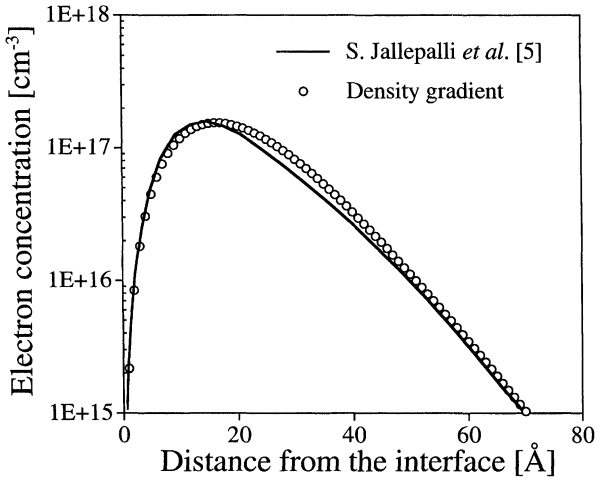

FIGURE 1 Comparison of the 1D charge distribution obtained from DG and full band Poisson–Schrödinger simulations for acceptor concentration $N_A = 5 \times 10^{17} cm^{-3}$, oxide thickness $t_{ox} = 4$ nm, inversion charge density $1.67 \times 10^{11} cm^{-2}$ and vertical field 3.05 V/cm.

Before moving to 3D atomistic simulations the DG approach has been carefully calibrated for continuous doping against rigorous 1D full band Poisson–Schrödinger simulations presented in [5]. By using effective mass $m^* = 0.19\, m_O$ an excellent agreement has been achieved between the DG simulations and the comprehensive Poisson–Shrödinger solution in respect of the QM threshold voltage shift [9]. Even more important for this study is the good agreement between the electron distributions in the inversion layer obtained using the two simulation techniques and illustrated in Figure 1.

3. EXAMPLES

We illustrate the fruitfulness of the DG approach in several 3D 'atomistic' simulation examples including random dopant fluctuation, single charge trapping at the Si/SiO_2 interface and oxide thickness fluctuation in ultrathin gate oxides.

3.1. Random Dopant Fluctuations

A typical result of the atomistic simulation of a $30 \times 50\,nm^2$ n-channel MOSFET with oxide thickness $t_{ox} = 3$ nm and a junction depth $x_j = 7$ nm is outlined in Figure 2. The uniform doping concentration in the channel region $N_D = 5 \times 10^{18}\,cm^{-3}$ is resolved down to individual dopants using fine grain discretisation. The number of dopants in the random dopant region of each individual transistor follows a Poisson distribution. The position of dopants is chosen at random and each dopant is assigned to the nearest gridnode. More complex doping profiles in the random dopant region of the device may be introduced using a rejection technique.

Current criterion $I_T = 10^{-8}\, W_{eff}/L_{eff}$ [A] is used to estimate the threshold voltage. Typically, samples of 200 microscopically different transistors are simulated for each combination of macroscopic design parameters, in order to extract the average threshold voltage and its standard deviation σV_T. The corresponding

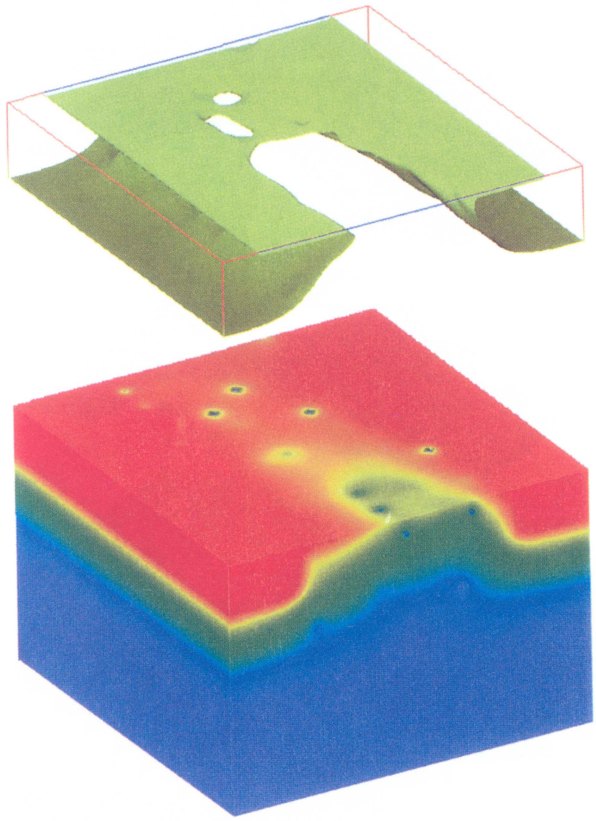

FIGURE 2 Potential (bottom) and one electron equiconcentration contour (top) at threshold voltage obtained from the atomistic DG simulation of 30 × 50 nm MOSFET with oxide thickness $t_{ox}=3$ nm, junction depth $x_j=7$ nm and channel acceptor concentration $N_A=5\times10^{18}\,\mathrm{cm}^{-3}$. (See Color Plate I).

relative standard deviation of the extracted σV_T is 5% for all results presented in this paper.

The dependencies of the threshold voltage standard deviation σV_T as a function of the oxide thickness, extracted from classical and from quantum atomistic simulations, are compared in Figure 3 for $50\times50\,\mathrm{nm}^2$ MOSFETs. In the classical simulations σV_T scales linearly to zero with the corresponding scaling of t_{ox} within the accuracy of the statistical estimations. This derives from the fact that Dirichlet boundary condition was applied at the gate electrode during the simulations, keeping constant the value of the potential on top of the gate insulator. Such 'metal gate' boundary condition completely screens/flattens the potential fluctuations at the Si/SiO_2

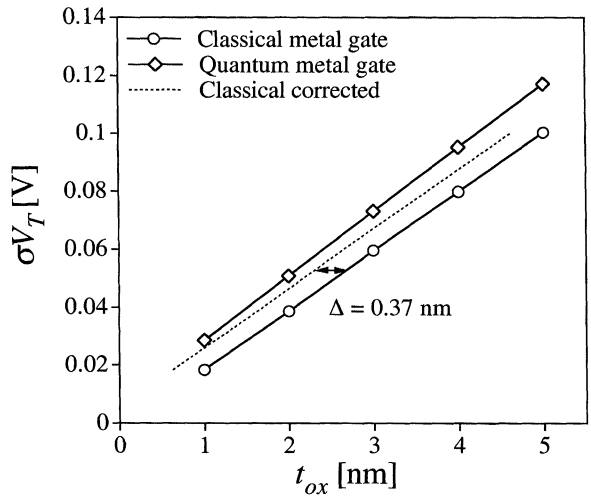

FIGURE 3 Threshold voltage standard deviation as a function of the oxide thickness for 50 × 50 nm MOSFETs with channel doping concentration $N_A=5\times10^{18}\,\mathrm{cm}^{-3}$. Comparison of classical and DG simulations.

interface when the oxide becomes infinitesimally thin. This in turns kills the threshold voltage fluctuations since the maximum of the classical inversion layer charge distribution and channel current density occur at the interface. The values of σV_T corresponding to the quantum simulations are shifted up in respect to the classical simulations and the shift slightly increases with the increase in the oxide thickness. The shift can be partially explained by the fact that the inversion layer centroid in the quantum simulations is below the interface and results in an effective increase in the oxide thickness. This can be taken into account simply by shifting the straight line approximating the classical dependence of σV_T on the oxide thickness along the oxide thickness axis by:

$$\Delta = \varepsilon_{ox} z_i / \varepsilon_{Si} \tag{7}$$

where z_i is the inversion layer centroid. According to [12] at doping concentration $N_A=5\times10^{18}$ cm^{-3} the inversion layer centroid is $z_i=1.12$ nm which corresponds to a shift of $\Delta=0.37$ nm. The shifted by this value classical σV_T dependence lies below the values of σV_T obtained from the quantum mechanical simulations and the difference increases for larger oxide thicknesses. This

confirms the fact that only part of the quantum enhancement of the threshold voltage fluctuations can be attributed to the effective increase in the oxide thickness. Other factors like the lateral confinement effects in the current channels and the quantum mechanical spreading of the inversion layer charge may be responsible for the rest of the quantum enhancement. The quantum mechanical enhancement of the fluctuations becomes important when the oxides are scaled to thicknesses below 2 nm.

3.2. Interface Charge Trapping

Current fluctuations, caused by trapping of single carriers at the Si/SiO_2 interface and related local modulation in carrier density and/or mobility [13, 14], are becoming increasingly important. Corresponding random telegraph signals (RTS) with amplitudes larger than 60% have been reported already at room temperature in very narrow channel devices [3]. Current fluctuations on such a scale will become a serious issue, not only in analogue circuits, but also in mixed-mode and digital applications.

In the following simulation example we use a continuous doping charge and only the trapped electron is introduced in the simulations as a discrete localised charge. We position the trapped electron at the Si/SiO_2 interface in the middle of the channel where its influence on the current flow is maximal. The potential distribution and a pair of electron equiconcentration contours, one corresponding to classical and the second corresponding to DG simulations are illustrated in Figure 4 for a $30 \times 30\,nm^2$ MOSFET with continuous doping and one discrete electron trapped exactly in the middle of the channel. The simulations presented in Figure 4 are carried out at gate voltage equal to the threshold voltage. The dependence of the relative RTS amplitude on the drain current (varied by changing the gate voltage) for a wide range of square decanano MOSFETs with oxide thickness 3 nm is presented in Figure 5. The continuous lines represent classical simulations.

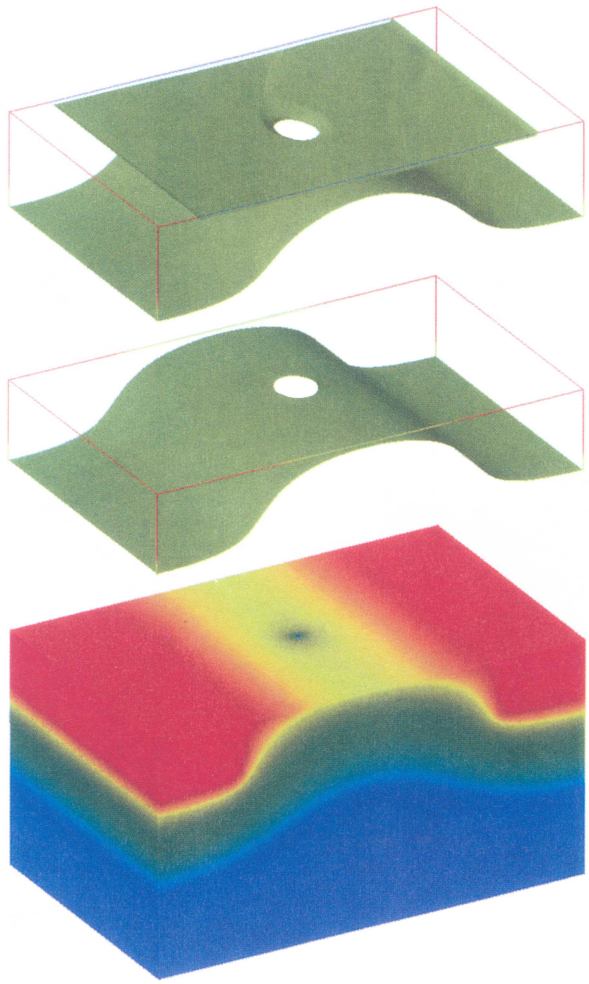

FIGURE 4 Potential distribution in a 30×30 nm MOSFET with continuous doping and one electron trapped in the middle of the channel (bottom). Equiconcentration contours calculated classically and using DG approach (top). (See Color Plate II).

DG simulations were carried out for the $30 \times 30\,nm^2$ MOSFET and plotted as dots in the figure. To avoid misleading conclusions the DG results are presented only in the subthreshold region where the assumption for low density of the electron gas holds. Disappointingly for the purposes of this study no significant difference between the classical and the quantum results were observed in respect to the RTS amplitudes. We believe that the effective increase in the oxide thickness in the QM simulation, and the corresponding reduction of the gate screening at

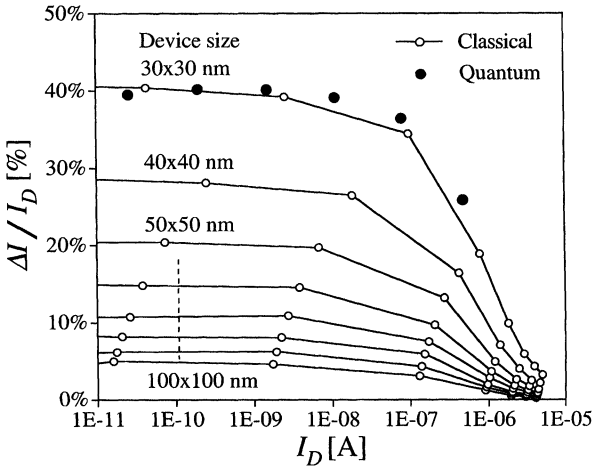

FIGURE 5 Relative RTS amplitude as a function of the drain current for a set of square MOSFETs with oxide thickness $t_{ox} = 3$ nm, junction depth $x_j = 7$ nm and channel acceptor concentration $N_A = 5 \times 10^{18}\,\mathrm{cm}^{-3}$.

the position of the charge centroid, is offset by the fact that the trapped electron itself is at the interface. It is, however, important to point out that the RTS amplitude in the 30×30 nm MOSFET reaches more than 40% in the subthreshold region and remains larger than 5% in strong inversion, even assuming continuous doping in the simulations.

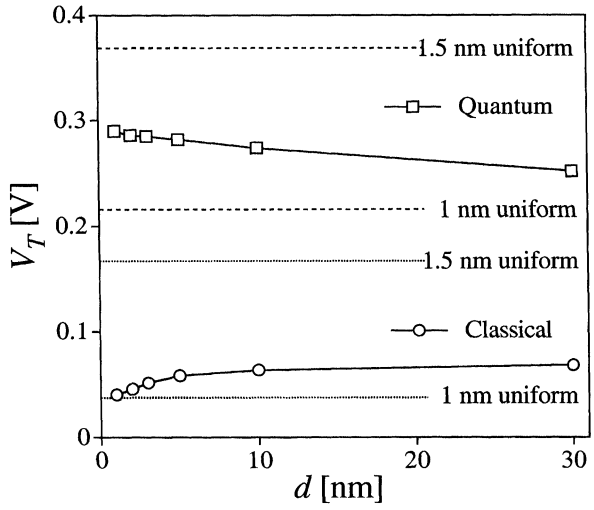

FIGURE 6 Threshold voltage in a 30×30 nm MOSFET as a function of the period of a superlattice formed by oxide thickness variations aligned with the direction of the channel.

3.3. Oxide Thickness Fluctuations

In order to illustrate the importance of the QM corrections in respect to the simulation of oxide thickness fluctuation effects a simulation experiment was carried out in a $30 \times 30\,\mathrm{nm}^2$ MOSFET with gate oxide forming a lateral superlattice of

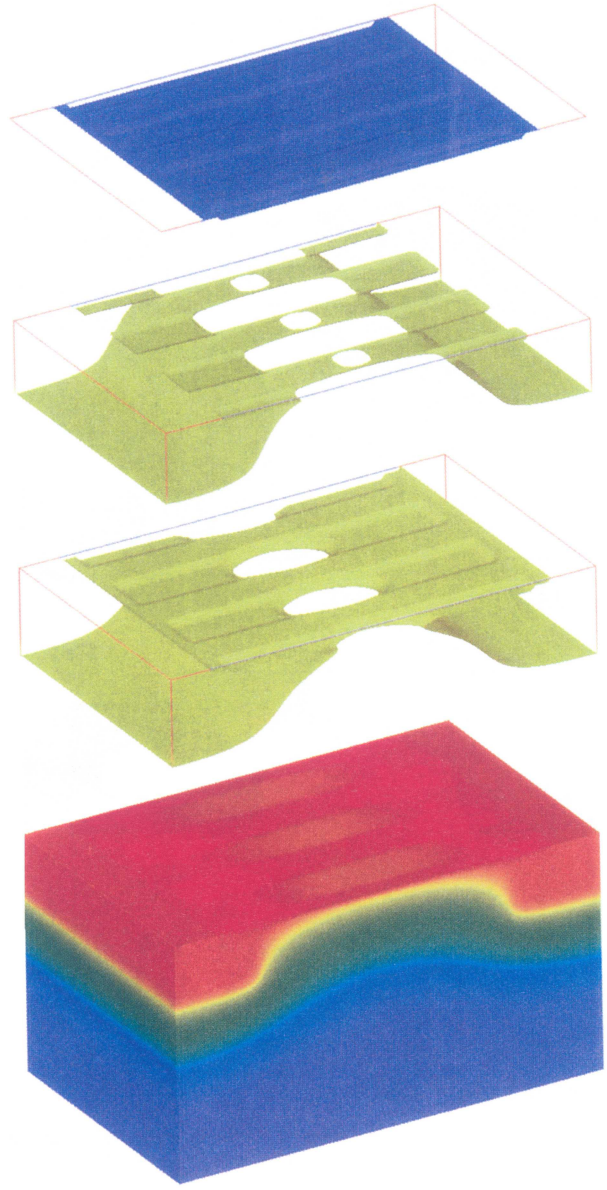

FIGURE 7 The profile of the Si/SiO_2 interface in a 30×30 nm MOSFET (top) followed by two equiconcentration contours obtained from classical and DG simulations and the potential distribution (bottom). (See Color Plate III).

thin (1 nm) and thick (1.5 nm) oxide strips in the direction parallel to the channel. The whole change in the oxide thickness occurs at the Si/SiO_2 interface. The threshold voltage dependence on the period d of the superlattice, calculated classically and with QM corrections, is illustrated in Figure 6. Completely opposite behaviour is observed with the two types of simulations. The classical results show reduction in the threshold voltage with the reduction of d while the quantum mechanical results show an increase in the threshold voltage. Figure 7 offers the explanation of the observed behaviour. The top of the figure illustrates the Si/SiO_2 interface followed by two equiconcentration contours obtained from classical and DG simulations and the potential distribution at the bottom. In the classical simulations there is an increase in the carrier concentration near the edges of the well associated with the increase of the potential there. Such increase in the potential near the corners is well known in such geometries and is the origin of the inverse narrow channel effect in trench isolated devices. The increasing contribution to the current from the corners, when the period of the superlattices decreases, results in a reduction of the threshold voltage in the classical case. However, due to the small depth of the trenches (0.5 nm) the QM charge distribution can not follow the local increase in the potential in the corners and the QM maximum in the charge concentration is in the middle of the wells. This is causing an increase in the threshold voltage when d becomes smaller.

4. CONCLUSION

The DG approach provides relatively simple means to include quantum correction in the 3D DD 'atomistic' MOSFET simulation. Applicable at relatively low carrier density it can be used in the DD framework to simulate the QM threshold voltage shift and to investigate the effect of the dopant and oxide thickness fluctuations on the variation of the threshold voltage. We have found that the inclusion of the QM corrections enhances the random dopant induced threshold voltage fluctuations in decanano MOSFETs. The enhancement is more than 50% in devices with gate oxide below 5 nm. In the same time we have not observed significant impact of the QM corrections on the RTS amplitudes in similar devices. We have demonstrated that the QM corrections may affect the simulations of effects associated with oxide thickness fluctuations in MOSFETs with ultrathin gate oxides and further investigations in this area are in progress.

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