AIP | Applied Physics Letters

High ON/OFF ratio and multimode transport in silicon nanochains field effect transistors

M. A. Rafiq, K. Masubuchi, Z. A. K. Durrani, A. Colli, H. Mizuta et al.

Citation: Appl. Phys. Lett. **100**, 113108 (2012); doi: 10.1063/1.3694046
View online: http://dx.doi.org/10.1063/1.3694046
View Table of Contents: http://apl.aip.org/resource/1/APPLAB/v100/i11
Published by the American Institute of Physics.

Related Articles

Analytic potential and charge model for III-V surrounding gate metal-oxide-semiconductor field-effect transistors
J. Appl. Phys. 112, 084512 (2012)

Oxygen plasma post process to obtain consistent conductance of carbon nanotubes in carbon nanotube field-effect transistors
Appl. Phys. Lett. 101, 173104 (2012)

Impact of universal mobility law on polycrystalline organic thin-film transistors
J. Appl. Phys. 112, 084503 (2012)

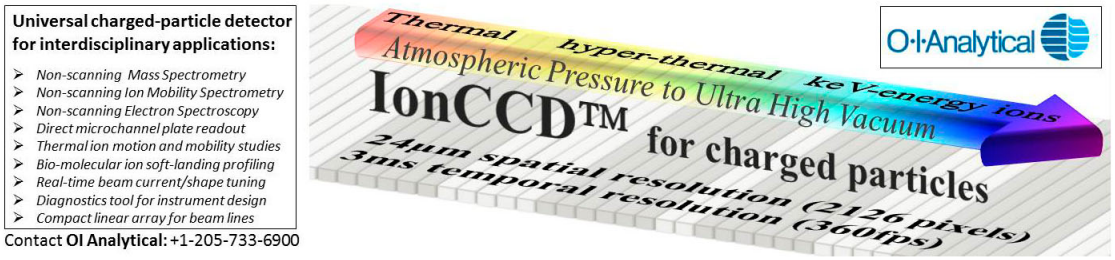
Influence of the surface morphology on the channel mobility of lateral implanted 4H-SiC(0001) metal-oxide-semiconductor field-effect transistors
J. Appl. Phys. 112, 084501 (2012)

Photoresponsivity enhancement of pentacene organic phototransistors by introducing C60 buffer layer under source/drain electrodes
Appl. Phys. Lett. 101, 163301 (2012)

Additional information on Appl. Phys. Lett.

Journal Homepage: http://apl.aip.org/
Journal Information: http://apl.aip.org/about/about_the_journal
Top downloads: http://apl.aip.org/features/most_downloaded
Information for Authors: http://apl.aip.org/authors

ADVERTISEMENT



Downloaded 24 Oct 2012 to 155.198.134.249. Redistribution subject to AIP license or copyright; see http://apl.aip.org/about/rights_and_permissions

High ON/OFF ratio and multimode transport in silicon nanochains field effect transistors

M. A. Rafiq,[1,2,3,a)] K. Masubuchi,[1] Z. A. K. Durrani,[2,4] A. Colli,[5] H. Mizuta,[2,6] W. I. Milne,[2,7] and S. Oda[1,2]

[1]*Quantum Nanoelectronics Research Centre, Tokyo Institute of Technology, O-Okayama, Meguro-ku, Tokyo 152-8552, Japan*
[2]*SORST JST, Japan*
[3]*Micro and Nano Devices Group, Department of Metallurgy and Materials Engineering, Pakistan Institute of Engineering and Applied Sciences, Islamabad, Pakistan*
[4]*Department of Electrical and Electronic Engineering, Imperial College London, South Kensington Campus, London SW7 2AZ, United Kingdom*
[5]*Nokia Research Centre C/O Nanoscience Centre, Cambridge CB30FF, United Kingdom*
[6]*Nanoscale Systems Integration Group, School of Electronics and Computer Science, University of Southampton, Southampton SO171BJ, United Kingdom*
[7]*Department of Engineering, University of Cambridge, 9 J. J. Thomson Avenue, Cambridge CB3 0FA, United Kingdom*

(Received 31 January 2012; accepted 27 February 2012; published online 14 March 2012)

We have observed multimode transport and high ON/OFF ratio in silicon nanochain devices. Silicon nanochains grown by thermal evaporation of SiO solid sources consisted of chains of silicon nanocrystals ~10 nm in diameter, separated by SiO_2 regions. The devices were fabricated using electron beam lithography on SiO_2 thermally grown on silicon substrate. These devices exhibited high ON/OFF current ratio up to 10^4. The inverse subthreshold slope as small as ~500 mV/decade was observed in these devices. Therefore, we believe silicon nanochains hold great potential to be used in field effect transistors. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.3694046]

One-dimensional nanostructures are attractive components of future nanoelectronic devices such as field effect transistors (FETs).[1–11] For this reason, semiconductor nanowires and carbon nanotubes have been used as channel material in FETs. Cui *et al*. studied high performance FETs based on silicon nanowires prepared by nanocluster-mediated growth method.[1] More recently, silicon nanowires grown by Au-catalyzed vapor-transport method have been utilized to fabricate top-gated FETs.[2] Heinze *et al*. demonstrated operation of carbon nanotube transistors as Schottky barrier transistors.[3] ZnO nanowires and graphene have also been used in fabrication of FETs.[5,12] The device concepts based on band to band tunnelling[4] have also been demonstrated in silicon and InAs nanowire FETs.[5,6] However, silicon based one-dimensional nanostructures are of considerable interest due to their compatibility with present industry. In view of this, we investigate possibility of silicon nanochains to be used in FETs. Silicon nanochain is a unique necklace like structure where a nanowire takes the form of silicon nanocrystals (SiNCs) separated and covered by SiO_2.[13–18] Silicon nanochains have attracted some attention recently.[13–18] Kohno *et al*. reported tunnelling electron transport in silicon nanochains during *in situ* scanning electron microscopy.[13] Tang *et al*. investigated the microstructure and field emission properties of boron doped silicon nanochains.[19] It has also been demonstrated that silicon nanochains have great potential to fabricate room and low temperature single electron transistors.[16–18] However, there are no studies on potential use of silicon nanochains as functional components of field effect transistors.

To explore the possibility of use of silicon nanochains in field effect transistor, we investigate electron transport in multiple silicon nanochain devices. We fabricate back gated devices, where multiple nanochains were present as channel between source and drain contacts. The silicon nanochains were prepared by thermal evaporation of silicon monoxide.[20] The silicon nanochains consisted of a chain of SiNCs ~10 nm in diameter separated and covered by SiO_2. Clear indication of multimode transport during electrical characterisation of silicon nanochain devices was observed. These devices exhibited subthreshold slope as small as ~500 mV/decade. High ON/OFF current ratio ~10^4 was also observed in these devices. The characteristics of the silicon nanochain FETs can be improved by reducing the gate oxide thickness and doping the nanochains.

The silicon nanochains were synthesised by thermal evaporation of 99.99% pure silicon monoxide powder, at 1400 °C in a quartz tube furnace. Argon gas was used to carry the vapour through the tube. Silicon nanochains were synthesised in a cooler part of the furnace at 900 °C–950 °C, and the nanochains were undoped. In addition, nanowires were also present in the grown samples. Depending on the growth conditions, 50%–90% of the final product takes the form of silicon nanochains. The nanochains may be considered as chains of SiNCs, separated by SiO_2 regions. Figure 1(a) shows a transmission electron micrograph of a silicon nanochain. The SiNC diameter varies from <10 nm to ~30 nm, and the separation varies from ~15 nm to 40 nm. SiNC is covered by a thin SiO_2 layer, ~1 nm–3 nm thick. The separation between

a)Electronic mail: fac221@pieas.edu.pk.

 © 2012 American Institute of Physics

Downloaded 24 Oct 2012 to 155.198.134.249. Redistribution subject to AIP license or copyright; see http://apl.aip.org/about/rights_and_permissions

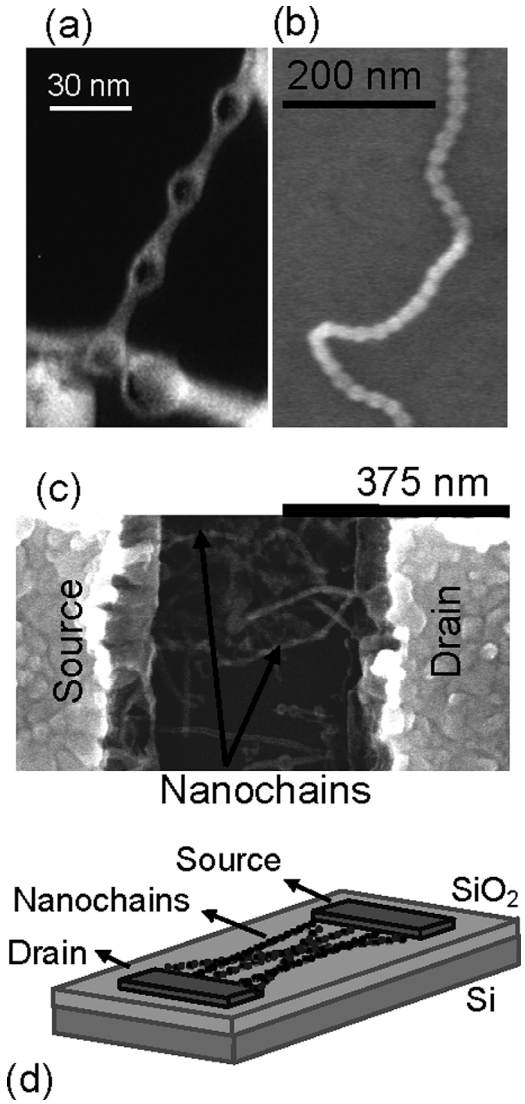


FIG. 1. (a) Transmission electron micrograph of Si nanochains, prepared by thermal evaporation of SiO. The image is slightly under-focused to emphasize diameter variations. A JEOL 200CX transmission electron microscope was used. (b) Scanning electron micrograph of a Si nanochain deposited on SiO_2. (c) Scanning electron micrograph of a Si nanochain device. (d) Schematic of a Si nanochain device.

the SiNCs varies from approximately the diameter of the SiNCs, to well below this value. Figure 1(b) shows a scanning electron micrograph of a silicon nanochain deposited on SiO_2.

The silicon nanochain devices were fabricated by defining aluminium contacts to silicon nanochains, using electron-beam (e-beam) lithography in poly methyl methacrylate resist. The devices were defined on silicon substrate covered with a ~200 nm thick thermally grown SiO_2. The silicon was doped *n*-type to a concentration of $1 \times 10^{19}/cm^3$ and it formed a global back-gate. Initially, an array of Cr/Au alignment marks was fabricated by e-beam lithography on the SiO_2 layer. The array of alignment marks was used for alignment purpose during successive lithography steps. Next, the surface of the top SiO_2 layer was treated with hexamethyldisilizane vapour treatment to improve the adhesion between nanochains and SiO_2. 0.1 mg of silicon nanochains were then dissolved in 3 ml isopropyl alcohol (IPA) using ultrasonic tip agitation for 5 min. The silicon nanochains were then spun onto the sample at 5000 rpm. Finally, aluminium contacts were evaporated on to the silicon nanochains, after wet etching of the SiO_2 layer around the silicon nanochains in the contact regions.

Figure 1(c) shows top view of a silicon nanochain device, respectively. Figure 1(d) shows a schematic diagram of the nanochain device. The I_D-V_{DS} characteristics of the devices were then measured in vacuum ($\sim 10^{-6}$ mBar) using a needle prober (BCT-43MDC, Nagase & Co. Ltd.) and an Agilent 4156C parameter analyser. The source-drain separation was ~350 nm and few silicon nanochains were present between source and drain contacts in this device (Fig. 1(c)).

Figure 2(a) plots the room temperature output curves (I_D-V_{DS}) for device A at $V_{GS} = -10$ V, -5 V, 0 V, and $+5$ V.

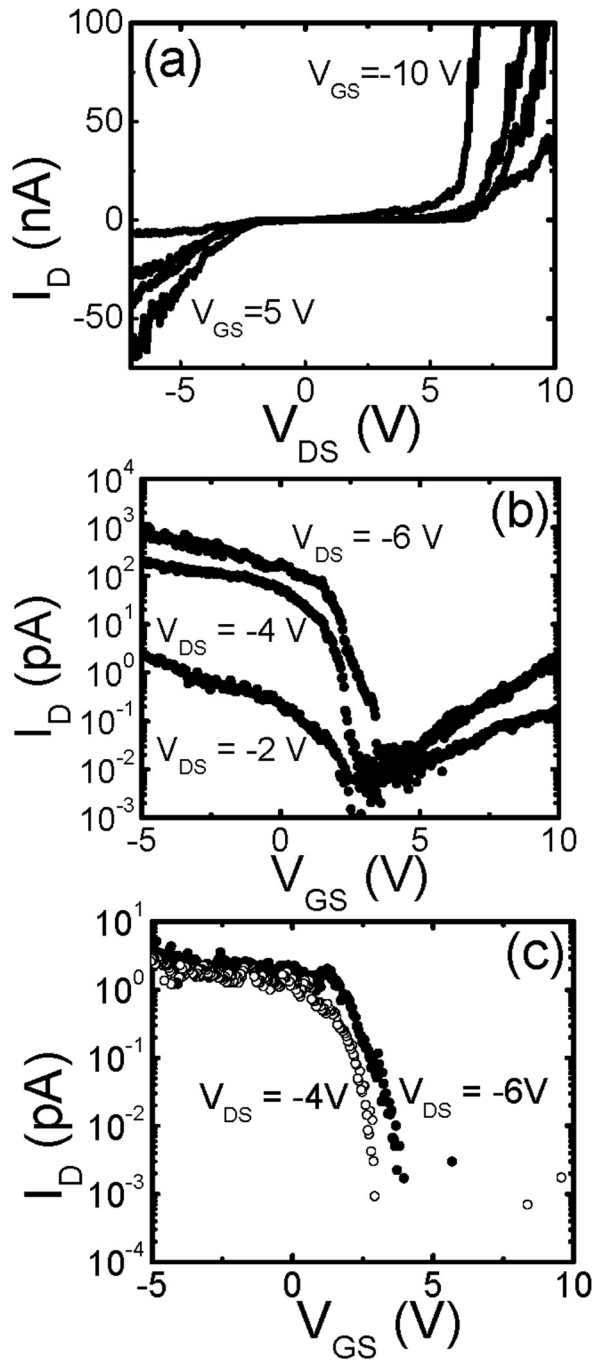


FIG. 2. (a) I_D-V_{DS} characteristics of a Si nanochain device (device "A") at 300 K. (b) Log-linear plot of I_D-V_{GS} characteristics of device "A." (c) I_D-V_{GS} characteristics of a Si nanowire device (device "B") at 300 K.

Downloaded 24 Oct 2012 to 155.198.134.249. Redistribution subject to AIP license or copyright; see http://apl.aip.org/about/rights_and_permissions

The curves are nonlinear indicating that the contacts between nanochains and metal leads are not ohmic, but rather a Schottky barrier is present.[21] Typical total device resistance in the ON state is ~25 GΩ. The high device resistance is expected due to undoped nature of nanochains. We note, however, that the output curves are non-symmetric indicating that contacts are in general nonequivalent. A wide distribution of contact resistances may exist for a single fabrication process, leading to a situation where only a few nanochains are dominating the electrical transport for an individual device.

Figure 2(b) shows the transfer characteristics of the same device A. The gate leakage I_G remains within the noise level, <0.1 pA (not shown). The values of I_D, I_S, and I_G confirm that the current flows through the silicon nanochains and not via the gate. I_D is low in value because of the small size and undoped nature of the SiNCs. In this device, strong dependence of I_D on V_{GS} is observed. I_D increases as the V_{GS} is decreased and I_D is blocked when V_{GS} is increased. This indicates that the nanochain transistor behaves as *p*-type transistor. The behaviour is similar to previous reports, where it has been demonstrated that undoped nanowire FETs usually behave as *p*-type transistor.[20,22] The nanochain FETs exhibits ambipolar behaviour. The current due to electrons, however, always shows a lower subthreshold slope compared to holes as can be seen from Figure 2(b). All nanochain devices exhibited similar characteristics. The transconductance ~0.1 pS was determined for this device. The value is low because of undoped nature of the nanochains. The value can be improved by doping the nanochains. Further, reduction in gate oxide will also improve the transconductance value.[23] The inverse subthreshold slopes S of the device A at $V_{DS} = -6$, -4, and -2 V are 500 mV/decade, 500 mV/decade, and 1000 mV/decade, respectively, was extracted from Figure 2(b). The obtained values of the S are not close to ideal value of S at room temperature, i.e., 60 mV/decade. However, these values are better than the values of S obtained for silicon nanowire tunnelling FETs.[5] However, the values of S can be further reduced by decreasing the gate oxide thickness.[24] In our devices, we used gate oxide thickness ~200 nm. Therefore, there is great potential to improve the value of S in our devices by reducing the gate oxide thickness below 50 nm. The ON/OFF current ratio of this device increases from 10^2 at $V_{DS} = -2$ V to 10^4 at $V_{DS} = -4$ V and it remains 10^4 at $V_{DS} = -6$ V. Figure 2(c) shows the transfer characteristics of a device B with source drain separation ~500 nm. The inverse subthreshold slopes S of the device at $V_{DS} = -6$, -4 volts is ~600 mV/decade. The ON/OFF current ratio of this device is 10^3.

Figure 3(a) shows the presence of step-like features in the I_D-V_{GS} characteristics of the device A. This may be due to stepwise increase of current carrying 1D modes in the nanochains when V_{GS} is increased, i.e., made more negative in present case (*p*-type FET). Appenzeller *et al.* observed similar step-like behaviour in carbon nanotube FETs.[25] They argued that such steps can be made visible by introducing scattering sites such as doping the nanotube. Here, in present case, the scattering sites may be present at the silicon nanocrystal/SiO_2 interface. They further argued that multimode transport can appear for small diameter nanotubes, where the

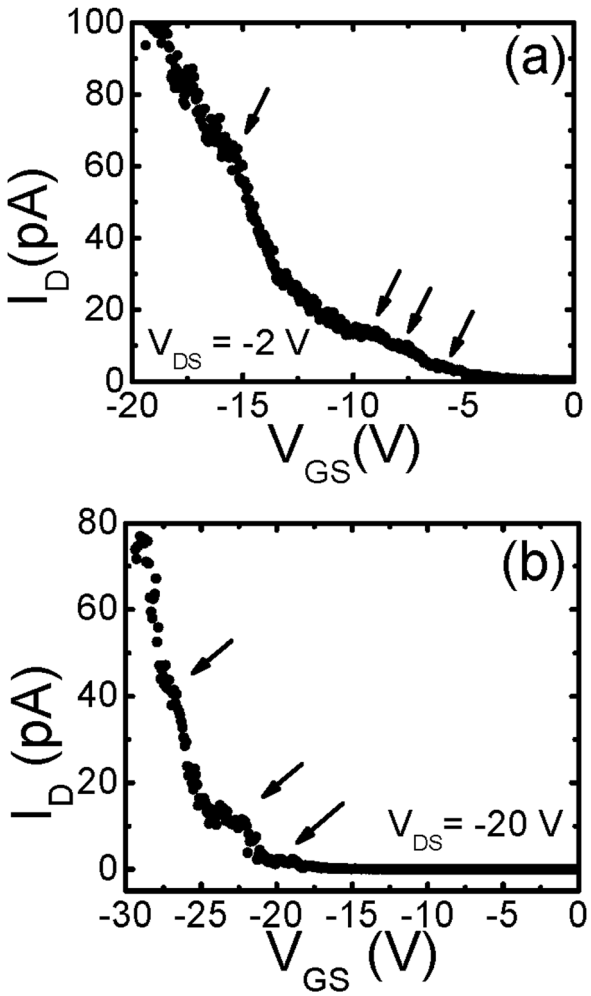


FIG. 3. (a) Linear-linear plot of I_D-V_{GS} characteristics of device "A" at $V_{DS} = -2$ V and (b) device "C" at $V_{DS} = -20$ V showing step-like behaviour.

current through one subband saturates when current level reaches the current level associated with the quantized conductance $4e^2/h$. In our nanochains, the silicon nanocrysals forming the nanochain are of very small diameter (large separation between subbands) and, therefore, it is expected that multimode transport may be visible in nanochains at room temperature. Many silicon nanochain devices exhibited such step-like behaviour. Figure 3(b) shows the multimode transport in another silicon nnaochain device C.

In conclusion, we have observed large ON/OFF ratio and multimode transport in silicon nanochain FETs. Si nanochains were grown by thermal evaporation of SiO solid sources. The nanochains consisted of chains of SiNCs ~10 nm in diameter, separated by SiO_2 regions. High ON/OFF current ratio up to 10^4 has been observed in these devices. Further, the inverse subthreshold slope S ~500 mV/decade is observed in these devices. ON/OFF current ratio and S can be improved by reducing the gate oxide thickness and doping the nanochains. Therefore, we believe silicon nanochains hold great potential to be used in fabricating FETs.

The work was supported by Grant-in-Aid for scientific research from the Japan Society for Promotion of Science (JSPS) Nos. 22246040 and 19-07107. M.A.R. would like to acknowledge the support from JSPS.

Downloaded 24 Oct 2012 to 155.198.134.249. Redistribution subject to AIP license or copyright; see http://apl.aip.org/about/rights_and_permissions

[1]Y. Cui, Z. Zhong, D. Wang, W. U. Wang, and C. M. Lieber, Nano Lett. **3**, 149 (2003).
[2]A. Colli, A. Tahraoui, A. Fasoli, J. M. Kivioja, W. I. Milne, and A. C. Ferrari, ACS Nano **3**, 1587 (2009).
[3]S. Heinze, J. Tersoff, R. Martel, V. Derycke, J. Appenzeller, and Ph. Avouris, Phys. Rev. Lett. **89**, 106801 (2002).
[4]J. Appenzeller, Y.-M. Lin, J. Knoch, and Ph. Avouris, Phys. Rev. Lett. **93**, 196805 (2004).
[5]M. T. Björk, J. Knoch, H. Schmid, H. Riel, and W. Riess, Appl. Phys. Lett. **92**, 193504 (2008).
[6]K. Tomioka and T. Fukui, Appl. Phys. Lett. **98**, 083114 (2011).
[7]A. L. Vallett, S. Minassian, P. Kaszuba, S. Datta, J. M. Redwing, and T. S. Mayer, Nano Lett. **10**, 4813 (2010).
[8]D. Kazazis, P. Jannaty, A. Zaslavsky, C. Le Royer, C. Tabone, L. Clavelier, and S. Cristoloveanu, Appl. Phys. Lett. **94**, 263508 (2009).
[9]W. M. Reddick and G. A. J. Amaratunga, Appl. Phys. Lett. **67**, 494 (1995).
[10]S. H. Ko, I. Park, H. Pan, N. Misra, M. S. Rogers, C. P. Grigoropoulos, and A. P. Pisano, Appl. Phys. Lett. **92**, 154102 (2008).
[11]M. Radosavljevic, J. Appenzeller, Ph. Avouris, and J. Knoch, Appl. Phys. Lett. **84**, 3694 (2004).
[12]F. Xia, D. B. Farmer, Yu. Lin, and Ph. Avouris, Nano Lett. **10**, 715 (2010).
[13]H. Kohno, S. Takeda, and T. Akita, Appl. Phys. Lett. **89**, 233124 (2006).
[14]H. Kohno and S. Takeda, Nanotechnology **18**, 395706 (2007).
[15]T. Nogami, Y. Ohno, S. Ichikawa, and H. Kohno, Nanotechnology **20**, 335602 (2009).
[16]Z. Z. Sun, X. R. Wang, R. Q. Zhang, and S. T. Lee, J. Appl. Phys. **103**, 103719 (2008).
[17]D. D. D. Ma, K. S. Chan, D. M. Chen, and S. T. Lee, Chem. Phys. Lett. **484**, 258 (2010).
[18]M. A. Rafiq, Z. A. K. Durrani, H. Mizuta, A. Colli, P. Servati, A. C. Ferrari, W. I. Milne, and S. Oda, J. Appl. Phys. **103**, 053705 (2008).
[19]Y. H. Tang, X. H. Sun, F. C. K. Au, L. S. Liao, H. Y. Peng, C. S. Lee, and S. T. Lee, Appl. Phys. Lett. **79**, 1673 (2001).
[20]A. Colli, A. Fasoli, P. Beecher, P. Servati, S. Pisana, Y. Fu, A. J. Flewitt, W. I. Milne, J. Robertson, C. Ducati *et al.*, J. Appl. Phys. **102**, 034302 (2007).
[21]S. W. Chung, J. Y. Yu, and J. R. Heath, Appl. Phys. Lett. **76**, 2068 (2000).
[22]K. Byon, D. Tham, J. E. Fischer, and A. T. Johnson, Appl. Phys. Lett. **90**, 143513 (2007).
[23]M. Choe, G. Jo, J. Maeng, W. Hong, M. Jo, G. Wang, W. Park, B. H. Lee, H. Hwang, and T. Lee, J. Appl. Phys. **107**, 034504 (2010).
[24]S. Heinze, M. Radosavljevic, J. Tersoff, and Ph. Avouris, Phys. Rev. B **68**, 235418 (2003).
[25]J. Appenzeller, J. Knoch, M. Radosavljevic, and Ph. Avouris, Phys. Rev. Lett. **92**, 226802 (2004).

Downloaded 24 Oct 2012 to 155.198.134.249. Redistribution subject to AIP license or copyright; see http://apl.aip.org/about/rights_and_permissions