Coprime Polynomial Based Dual-circulant Modulation for Inherent Submodule Voltage Balancing in MMDC

Shiyuan Fan, Xin Xiang, *Member, IEEE*, Chushan Li, *Member, IEEE*, Yunjie Gu, *Senior Member, IEEE*, Huan Yang, Wuhua Li, *Member, IEEE*, Xiangning He, *Fellow, IEEE*, Timothy C. Green, *Fellow, IEEE*

***Abstract*—The modular multilevel dc-dc converters (MMDCs) have attracted much interest in medium voltage dc applications, but have to face the main issue of balancing submodule (SM) capacitor voltages. This paper proposes a dual-circulant modulation and proves it possessing the inherent balancing capability for arbitrary operation cases. High-speed communication for real-time sensor data transfer could be avoided, which reduces implementation costs and also enhances the system reliability. Two sets of circular switching patterns are preset and combined to complete the full constrains on SM voltages. The associated polynomial of circulant matrix is introduced and the coprime of polynomials demonstrates the full-rank feature of the extended switching matrix that promises the inherent balancing for any operation cases. Then the switching patterns are reallocated and optimized to keep the SM uniformity and reduce the capacitor voltage ripple at the same time. Full-scale simulations on MMDC models and down-scaled experiments on prototypes are both presented, which validates the inherent voltage balancing capability and the optimization of SM capacitor voltage ripple with the proposed dual-circulant modulation.**

***Index Terms*—Modular multilevel dc converter, inherent submodule voltage balancing, dual-circulant modulation, circulant matrix, coprime associated polynomial.**

I. Introduction

Modular multilevel dc-dc converters (MMDCs) have shown its superiority of flexibility and reliability in interfacing low voltage dc (LVdc) layers with medium voltage dc (MVdc) systems for renewable energy integration, large-scale energy storage and electric vehicle charging station [1],[2]. The balancing of submodule (SM) capacitor voltage is the basic requirement for an MMDC like that for all kinds of modular converters [3]. One of the most common ways to realize the balancing is allocating the switching patterns according to the real-time order of SM voltages. This relies on the voltage sensors of each SM, the high-speed communication with central controller and the high-performance computing for complex sorting process [4]-[6].

Instead, inherent balancing of SM voltage is an attractive property that avoids real-time sensor data transfer thereby curtailing implementation costs, reducing control burden and also enhancing reliability [7],[8]. Switching patterns of the SMs are preset enabling the open-loop control for voltage balancing. The patterns of the arm stack can be expressed by an n-column switching matrix where n is the SM number in one stack, and the inherent balancing condition has be concluded as the full-rank feature of switching matrix [9]-[12], which indicates n linear independent row vectors in the matrix that provides complete constrains on n SMs.

Studies have been conducted on switching pattern design for self-balanced modulation. In [9], a full-rank switching matrix extraction method based on recursion is proposed for modular multilevel converter (MMC) in dc-ac applications. However, with the extension of SM number, the complexity of matrix extraction process grows rapidly, and it would be very difficult to create the matrix and justify the matrix rank [10]. Furthermore, the switching frequency of each SM will be higher than ac fundamental frequency, which is not suitable for the high-frequency operation of MMDC. Another approach is provided in [11] that full-permutated switching patterns are combined to generate a full-rank switching matrix specifically for a MMDC with 4 SMs. However, strict proof is not provided for the effectiveness of permutation with arbitrary SM number, and massive data dilemma still exists resulting in a huge matrix when SM number increases.

Circulant modulation discussed in [12] directs that each SM shares the same switching patterns with the later SM lagging behind the former one. This would equally distribute the voltage and current stresses, switching and conduction losses among SMs for better uniformity, and further benefit to specify a tighter SM design limit with reduced overall costs [13]. The circulant matrix [14] is introduced to capture the circular feature, then the full-rank condition can be simplified as the coprime criterion that effectively justifies the inherent balancing capability for circulant modulation regardless of the expansion of SM number [15]. However, unbalanced cases cannot be avoided since the coprime criterion strictly relates to both SM total number and conversion ratio, which could not satisfy for all the operations cases [16].

To date, an inherently balanced modulation that adapts both SM number expansion and arbitrary voltage conversion demands is still unrevealed for MMDC. This paper proposes and optimizes a dual-circulant modulation for MMDC and proves its inherent

Manuscript received 15 July 2022; revised 17 October 2022; accepted 12 November 2022. This work was supported in part by the National Key Research and Development Program of China under Grant 2022YFE0101900 and in part by the National Natural Science Foundation of China under Grant 52107214 and 52061635101. (*Corresponding author: Xin Xiang.*)

S. Fan, X. Xiang, H. Yang, W. Li, and X. He are with the College of Electrical Engineering, Zhejiang University, Hangzhou 310027, China (e-mail: shiyuan_fan@zju.edu.cn; xiangxin@zju.edu.cn; yanghuan@zju.edu.cn; woohualee@zju.edu.cn; hxn@zju.edu.cn).

C. Li is with the Zhejiang University–University of Illinois at Urbana-Champaign Institute, Zhejiang University, Hangzhou 310058, China (e-mail: chushan@intl.zju.edu.cn).

Y. Gu is with the Department of Electronic and Electrical Engineering, University of Bath, Bath BA2 7AY, U.K. (e-mail: yg934@bath.ac.uk).

T. C. Green is with the Department of Electrical and Electronic Engineering, Imperial College London, London SW7 2AZ, U.K. (e-mail: t.green@imperial.ac.uk).

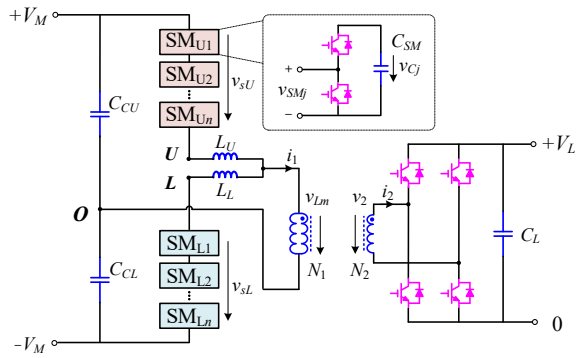


Fig. 1 Schematics of DAB-based MMDC.

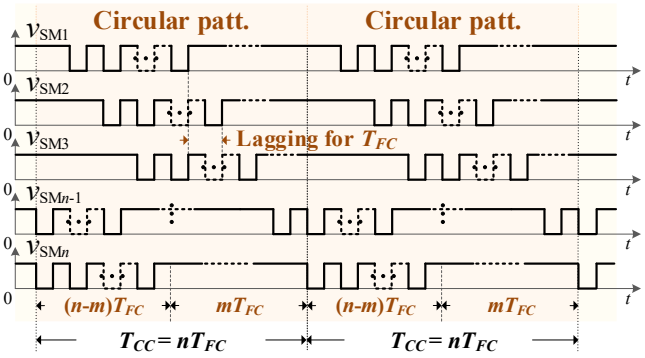


Fig. 2 Switching patterns of basic circulant modulation (denoted as $\boldsymbol{S}$).

balancing capability for arbitrary SM number including non-coprime cases, which could fill the last building block for inherent SM voltage balancing in MMDC. Firstly, the operating principles of MMDC and inherent balancing conditions under the basic circulant modulation are briefly summarized, indicating that non-coprime unbalanced cases would be unavoidable. In order to solve this, dual-circulant modulation is proposed that extends the switching patterns to complete the constrains on SM voltages. Then the associated polynomial of circulant matrix is introduced to prove the full-rank feature of the extended switching matrix for dual-circulant modulation. The switching patterns are then reallocated to inherit the advantages of SM uniformity and further optimized to reduce the SM capacitor voltage ripple. Full-scale simulations and down-scaled experiments are both conducted, which validates the effectiveness of the proposed dual-circulant modulation with both inherent voltage balancing and SM ripple optimization.

II. Inherent Balancing Capability and the Limitation of Basic Circulant Modulation

A DAB-based MMDC is illustrated in Fig. 1, and its operating principles are discussed in detail referring [12], [16].

Different kinds of MMDCs similarly share the SM-based stack structure and rely on the alternation of inserted SM number in upper and lower stacks to generate a high-frequency ac voltage then stimulate the internal passive stage [15]-[20]. A fundamental ac cycle, denoted as T_{FC}, can be equally divided into two stages, the positive stage and negative stage, according to the voltage between mid-points of dc-link capacitors and arms. For the negative stage, all of the n SMs in upper stack are inserted, while only m SMs ($0 < m < n$) are inserted in lower stack with $n - m$ SMs bypassed. For the positive stage, m SMs in upper stack and n SMs in lower stack are inserted [1],[16],[17]. This modulation highly satisfies the demand of voltage amplitude conversion in MMDCs, since the choice of m can be utilized as an effective control degree of freedom for voltage regulation [16], namely, a larger m provides a higher step-down ratio and vice versa [1],[18]. And with this modulation considered for design, it also helps to specify the demanded SM number in the MMDC, since the medium-side dc bus voltage would be supported by $n + m$ SMs rather than n SMs in the typical MMC modulation [21].

Circulant modulation is applied to decide which specific SMs switches for each fundamental cycle. As shown in Fig. 2, the switching patterns of each SM refer that of the former one with one T_{FC} lagging, and the first SM refers back to the last. Thus, it takes n steps to fully rotate a switching pattern among n SMs within one stack. On the other hand, the driving signal of a specific SM would fulfill a circulation every n fundamental cycles. Hence, the circulant cycle is defined as $T_{CC} = nT_{FC}$, and each SM shares the same switching frequency $f_{SW} = \frac{n-m}{n} f_{FC}$ that is lower than the ac fundamental frequency f_{FC}.

SM capacitor voltages are then constrained by the circulant switching patterns and the MVdc bus. For the voltage loop of the upper arm, the voltage equation can be written as

$$\boldsymbol{s} \cdot \boldsymbol{v_C^T} = v_{CCU} - v_{LU} - v_{Lm} \tag{1}$$

where $\boldsymbol{v_C^T}$ and $\boldsymbol{s}$ are both n-dimensional vectors, whose elements indicate the instantaneous capacitor voltages and the switching states of each SM in the upper stack. v_{CCU}, v_{LU} and v_{Lm} are the instantaneous voltage respectively of the upper dc-link capacitor C_{CU}, arm inductor L_U and the internal transformer L_m. Considering the voltage-second balance of the inductors and eliminating the capacitor voltage fluctuation within fundamental cycles in steady state, a set of linear equations constraining SM capacitor voltages is derived [12] as

$$\boldsymbol{S} \cdot \bar{\boldsymbol{v}}_{\boldsymbol{C}}^{\boldsymbol{T}} = \begin{bmatrix} \overbrace{11\cdots11}^{m}\overbrace{00\cdots00}^{n-m} \\ 01\cdots1110\cdots00 \\ \vdots \quad\quad \vdots \\ 11\cdots1000\cdots01 \end{bmatrix} \cdot \begin{bmatrix} \bar{v}_{C1} \\ \bar{v}_{C2} \\ \vdots \\ \bar{v}_{Cn} \end{bmatrix} = \begin{bmatrix} 2V_M - V_{CS} \\ 2V_M - V_{CS} \\ \vdots \\ 2V_M - V_{CS} \end{bmatrix} \tag{2}$$

where $\boldsymbol{S}$ is a circulant matrix that is defined as the switching matrix of circulant modulation. The element of "1" in $\boldsymbol{S}$ denotes that the SM capacitor is inserted into the conducting circuit for the whole fundamental cycle without any switching actions, and the element "0" in $\boldsymbol{S}$ represents that the SM capacitor is bypassed during the positive stage and inserted back to the circuit during the negative stage with a switching action in the fundamental cycle. Each column vector of $\boldsymbol{S}$ describes the switching patterns of one SM for T_{CC}, thus the switching frequency can be calculated for each SM as the number of "0" elements divided by the total element number in the column vector. Each row vector represents the switching patterns of all the n SMs in the stack within one T_{FC}. It decides how the SM capacitors are inserted in the circuits and clamped by the dc bus, which could be considered as a constrain determining the SM capacitor voltages. $\bar{\boldsymbol{v}}_{\boldsymbol{C}}^{\boldsymbol{T}}$ is the vector of averaged SM capacitor voltages for T_{CC}. V_M is the steady-state dc-link capacitor voltage and $2V_M$ would be the

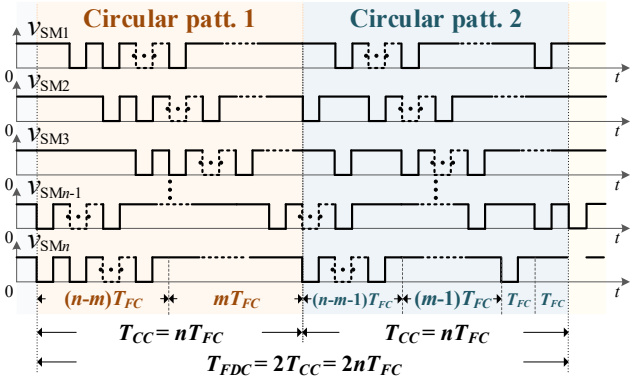


Fig. 3 Switching patterns for all n SMs under direct dual-circulant modulation with switching set alternation (denoted as $\boldsymbol{DS}$).

MVdc bus voltage. $V_{CS} = [\overbrace{11\cdots11}^{n}] \cdot \bar{\boldsymbol{v}}_{\boldsymbol{C}}^{\boldsymbol{T}} = \sum_{i=1}^{n} \bar{v}_{Ci}$ depicting the negative stages as a whole that all the n SMs are inserted into the circuits. Since $\bar{v}_{C1}$, $\bar{v}_{C2}$, ⋯, $\bar{v}_{Cn}$ should be constants (but not necessarily equal) in steady state, $2V_M - V_{CS}$ will be also a constant.

The steady-state inherent balancing of SM capacitor voltages will be promised if $\boldsymbol{S}$ is a full-rank matrix that provides n linear-independent constrains and results in the unique solution. It could be considered as the switching patters providing a complete rotation of the SMs, and thus the SM capacitors are equally and separately clamped by the dc bus capacitor in steady state. Then so long as the dc bus voltage is stable and the switching patterns follow the full-rank switching matrix, the steady-state SM capacitor voltages would be always inherently and finally balanced with the consideration of dynamic process, circulation components and harmonic components [15],[22]. By calculating the determinant of $\boldsymbol{S}$, equivalent condition has been deduced in [12] that n and m should be coprime.

However, the SM number in stack n is decided by the MVdc bus voltage and power devices used in SMs, and m is relevant to the internal ac voltage amplitude and governed by the dc voltage conversion demand. The cases of n and m being non-coprime is unavoidable in practical design and operation, and it will lead to unbalanced SM voltages [11], [23], which will be discussed and solved in next sections.

III. Direct Dual-Circulant Modulation

In this section, the dual-circulant modulation is proposed with associated polynomial of circulant matrix introduced for checking matrix rank and inherent balancing capability.

A. Direct dual-circulant modulation

Incomplete constrains provided by the single set of circular switching patterns is the root cause of unbalanced SM voltages in non-coprime cases, and the non-full rank feature of switching matrix can be viewed as the mathematical expression of the incompleteness. Thus, additional set of switching patterns is demanded to be combined with the original set, which could help to complete the constrains and promise the inherent balancing capability for non-coprime cases.

As shown in Fig. 3, an additional set of circular switching patterns is added with blue shade illustrated. The additional set is designed as follow: For the first fundamental cycle, m SMs including SM_1, SM_3, ⋯, SM_{m+1} are inserted during positive stage while the rest $n-m$ SMs in stack are bypassed, and all the n SMs are inserted during negative stage, which can be represented by the first row vector of $\boldsymbol{S'}$ in (3). Then for the following $n-1$ fundament cycles, the later SM still refers the former one with one T_{FC} lagging. It is presented by the circulant switching matrix $\boldsymbol{S'}$ that each row vector has the same elements sequence, but the later row lags one bit behind the former one. Thus, this additional set of circular switching patterns can be represented by the circulant matrix $\boldsymbol{S'}$ as

$$\boldsymbol{S'} = \begin{bmatrix} 1\,0\ \overbrace{111\cdots111}^{m-1}\ \overbrace{000\cdots000}^{n-m-1} \\ 0\,1\ 011\cdots111\ 100\cdots000 \\ \vdots \qquad\qquad \vdots \\ 1\,1\ 111\cdots100\ 000\cdots010 \\ 0\,1\ 111\cdots110\ 000\cdots001 \end{bmatrix} \tag{3}$$

Similarly with that in $\boldsymbol{S}$, each column vector of $\boldsymbol{S'}$ describes the switching patterns of one SM for T_{CC}, and each row vector represents the switching patterns of all the n SMs in the stack within one T_{FC}.

Then the dual-circulant modulation can be directly obtained by alternating these two sets of circular switching patterns. The full dual-circulant cycle, denoted as T_{FDC}, contains two circulant cycles, namely $T_{FDC} = 2T_{CC} = 2nT_{FC}$. Considering that each SM switches $n-m$ times within each circulant cycle, the SM switching frequency is still $f_{SW} = \frac{n-m}{n} f_{FC}$ that is lower than the fundamental frequency.

The switching matrix of the dual-circulant modulation can be derived by combining $\boldsymbol{S}$ and $\boldsymbol{S'}$ as

$$\boldsymbol{DS} = \begin{bmatrix} \boldsymbol{S} \\ \boldsymbol{S'} \end{bmatrix} \tag{4}$$

$\boldsymbol{DS}$ is a $2n \times n$ matrix with $2n$ rows indicating that the full dual-circulant cycle contains $2n$ fundamental cycles, and thus $2n$ switching patterns regulates the SMs in stack providing more constrains on SM voltages.

B. Coprime associated polynomial for inherent balancing

The additional circular switching patterns set brings more constrains on SM voltages, but the expanded switching matrix is not necessary to be full-rank to promise the inherent balancing. A new issue arises that how to justify the full-rank feature of the $2n \times n$ matrix that is not a typical $n \times n$ circulant matrix. In order to solve this, the associated polynomial is introduced, then the polynomial coprime is presented to evaluate the rank of expanded $2n \times n$ switching matrix.

For a circulant matrix $\boldsymbol{C}$ with first row being $[a_0\ a_1 \cdots a_{n-1}]$, the associated polynomial of $\boldsymbol{C}$ is defined as

$$p(x) = \sum_{i=0}^{n-1} a_i x^i \tag{5}$$

***Lemma* 1**. The rank of an n-order circulant matrix $\boldsymbol{C}$ is $n-d$, where d is the degree of the greatest common divisor of $1-x^n$ and the associated polynomial of $\boldsymbol{C}$. [24]

***Lemma* 2.** For n-order circulant matrixes $\boldsymbol{C_1}$ and $\boldsymbol{C_2}$ respectively with associated polynomials $p_1(x)$ and $p_2(x)$, if $p_1(x)$ and $p_2(x)$ are coprime, the rank of the combined $2n \times n$ matrix $\boldsymbol{C} = [\boldsymbol{C_1^T}\ \boldsymbol{C_2^T}]^T$ would *be* n. [25]

***Lemma* 3**. The necessary and sufficient condition for $f(x)$ and $g(x)$ being coprime is the existence of $u(x)$ and $v(x)$ that satisfy $f(x)u(x) + g(x)v(x) = 1$. [26]

For the basic circulant modulation with circulant switching

matrix $\boldsymbol{S}$ in (2), the associated polynomial of $\boldsymbol{S}$ is denoted as $f(x)$ and shown in (6). Since $x = 1$ is apparently not the solution of $f(x) = 0$, $f(x)$ can be further expressed as

$$f(x) = 1 + x + x^2 + \cdots + x^{m-1} = \frac{x^m - 1}{x - 1} = \frac{\prod_{k=0}^{m-1}(x - e^{i\cdot 2\pi\frac{k}{m}})}{x - 1} \quad (6)$$

Expanding by the roots of unity, $1 - x^n$ can be rewritten as

$$1 - x^n = -\prod_{k=0}^{n-1}(x - e^{i\cdot 2\pi\frac{k}{n}}) \quad (7)$$

Combining (6) and (7), it can be derived that if n and m are coprime with the greatest common factor equaling $z = 1$, $f(x)$ and $1 - x^n$ would have no common divisor other than 1. The constant 1 is irrelevant to x and its degree d can be considered as 0. Thus, the rank of $\boldsymbol{S}$ is n, which promises the inherent balancing capability of circulant modulation. On the contrary, if n and m are not coprime with their greatest common factor equaling $z > 1$, the greatest common divisor of $1 - x^n$ and $f(x)$ would be $\prod_{k=1}^{z-1}(x - e^{i\cdot 2\pi\frac{k}{z}})$ whose degree is $z - 1$. Thus, the rank of $\boldsymbol{S}$ could be specified as $n - z + 1 < n$ indicating that the basic circulant modulation cannot provide complete constrains and leads to unbalanced SM voltages. In all, the coprime of m and n is the sufficient and necessary condition of the $f(x)$ and $1 - x^n$ being coprime, which is also the sufficient and necessary condition of inherent SM balancing under the basic circulant modulation.

In order to inherently balance the SM voltages for non-coprime cases, dual-circulant modulation should be applied with the additional set $\boldsymbol{S'}$ alternating with the basic one. According to (3), the associated polynomial of $\boldsymbol{S'}$ would be

$$g(x) = 1 + x^2 + x^3 + \cdots + x^{m-1} + x^m \quad (8)$$

Using the extended Euclidean algorithm [27], $g(x)$ and $f(x)$ can be represented as

$$g(x) = xf(x) + (1 - x) \quad (9)$$

$$f(x) = -\sum_{k=1}^{m-1} k \cdot x^{m-k-1}(1 - x) + m \quad (10)$$

Then substituting (9) in (10) with $1 - x = g(x) - xf(x)$,

$$\begin{aligned} m &= f(x) + \sum_{k=1}^{m-1} k \cdot x^{m-k-1}\,[g(x) - xf(x)] \\ &= f(x) \cdot \left(1 - \sum_{k=1}^{m-1} k \cdot x^{m-k}\right) + g(x) \cdot \sum_{k=1}^{m-1} k \cdot x^{m-k-1} \end{aligned} \quad (11)$$

Dividing m on each side of (11) considering $m \neq 0$, it shows that $u(x)$ and $v(x)$ can be always found as (12) satisfying $f(x)u(x) + g(x)v(x) = 1$.

$$u(x) = \frac{1 - \sum_{k=1}^{m-1} k \cdot x^{m-k}}{m}, v(x) = \frac{\sum_{k=1}^{m-1} k \cdot x^{m-k-1}}{m} \quad (12)$$

Thus, $f(x)$ and $g(x)$ should be coprime, and the $2n \times n$ switching matrix $\boldsymbol{DS}$ is proved to be full-rank. The dual-circulant modulation can always possess the inherent balancing capability regardless of n and m being coprime or not.

C. Illustration Example

The inherent balancing feature of an MMDC with 4 SMs in one stack is analyzed as an illustration example as below. For $n = 4$ and $m = 2$, the switching matrix $\boldsymbol{S}$ and $\boldsymbol{S'}$ are shown in (13) representing two sets of circular switching patterns.

$$\boldsymbol{S} = \begin{bmatrix} 1\,1\,0\,0 \\ 0\,1\,1\,0 \\ 0\,0\,1\,1 \\ 1\,0\,0\,1 \end{bmatrix} = \begin{bmatrix} \boldsymbol{S_1} \\ \boldsymbol{S_2} \\ \boldsymbol{S_3} \\ \boldsymbol{S_4} \end{bmatrix}, \boldsymbol{S'} = \begin{bmatrix} 1\,0\,1\,0 \\ 0\,1\,0\,1 \\ 1\,0\,1\,0 \\ 0\,1\,0\,1 \end{bmatrix} = \begin{bmatrix} \boldsymbol{S'_1} \\ \boldsymbol{S'_2} \\ \boldsymbol{S'_3} \\ \boldsymbol{S'_4} \end{bmatrix} \quad (13)$$

The first row vector of $\boldsymbol{S}$, denoted as $\boldsymbol{S_1}$, represents the switching patterns of the 4 SMs in upper stack during the first fundamental cycle that the first two SMs keep insertion for the whole T_{FC} and the other two SMs switch with their capacitors bypassed during positive stage. Similarly, $\boldsymbol{S_2}$~$\boldsymbol{S_4}$ and $\boldsymbol{S'_1}$~$\boldsymbol{S'_4}$ represent the switching patterns in the 2nd ~ 4th and the 1st ~ 4th T_{FC} of the basic and the additional circular set respectively. Furthermore, for the first column vector of $\boldsymbol{S}$, it represents the switching patterns of SM_1 for 4 fundamental cycles within one circulant cycle that it keeps insertion in the 1st and 4th T_{FC} and switches in the 2nd and 3rd T_{FC}. Thus the switching frequency of SM_1 can be calculated as $\frac{1}{2}f_{FC}$. All the column vectors have the same sequence of elements with the later column moving backward one bit referring to the former column. This indicates that all SMs share the same switching patterns with the later one lagging behind the former one for one T_{FC}.

The associated polynomials of $\boldsymbol{S}$ and $\boldsymbol{S'}$ are respectively denoted as $f(x)$ and $g(x)$ that are

$$f(x) = 1 + x,\ g(x) = 1 + x^2 \quad (14)$$

Considering that the greatest common divisor of $1 - x^4$ and $f(x)$ is $1 + x$ with degree being 1, and the greatest common divisor of $1 - x^n$ and $g(x)$ is $1 + x^2$ with degree being 2, according to *Lemma* 1, $\boldsymbol{S}$ and $\boldsymbol{S'}$ are not full rank. The inherent balancing capability is absent with the single set based basic circulant modulation, and the SM capacitor voltages cannot inherently converge with the switching patterns of $\boldsymbol{S}$ or $\boldsymbol{S'}$.

Dual-circulant modulation should be applied to promise the inherent balance capability. As derived in (12), since $u(x) = \frac{1-x}{2}$ and $v(x) = \frac{1}{2}$ can be find for $f(x)$ and $g(x)$, these two associated polynomials are coprime according to *Lemma* 3 due to the existence of polynomials allowing

$$\tfrac{1-x}{2} \cdot f(x) + \tfrac{1}{2} \cdot g(x) = 1 \quad (15)$$

Thus, the switching matrix $\boldsymbol{DS}$ as (16) would be full-rank indicating that the combined switching patterns would provide complete constrains to inherently balance the SM capacitor voltages.

$$\boldsymbol{DS} = \begin{bmatrix} \boldsymbol{S} \\ \boldsymbol{S'} \end{bmatrix} = \begin{bmatrix} \boldsymbol{S_1} \\ \boldsymbol{S_2} \\ \boldsymbol{S_3} \\ \boldsymbol{S_4} \\ \boldsymbol{S'_1} \\ \boldsymbol{S'_2} \\ \boldsymbol{S'_3} \\ \boldsymbol{S'_4} \end{bmatrix} = \begin{bmatrix} 1\,1\,0\,0 \\ 0\,1\,1\,0 \\ 0\,0\,1\,1 \\ 1\,0\,0\,1 \\ 1\,0\,1\,0 \\ 0\,1\,0\,1 \\ 1\,0\,1\,0 \\ 0\,1\,0\,1 \end{bmatrix} = [\boldsymbol{S_{SM1}}\ \boldsymbol{S_{SM2}}\ \boldsymbol{S_{SM3}}\ \boldsymbol{S_{SM4}}] \quad (16)$$

where $\boldsymbol{S_{SM1}}, \boldsymbol{S_{SM2}}, \boldsymbol{S_{SM3}}, \boldsymbol{S_{SM4}}$ are the column vectors in $\boldsymbol{DS}$, which denotes the switching patterns of each SM within one full-

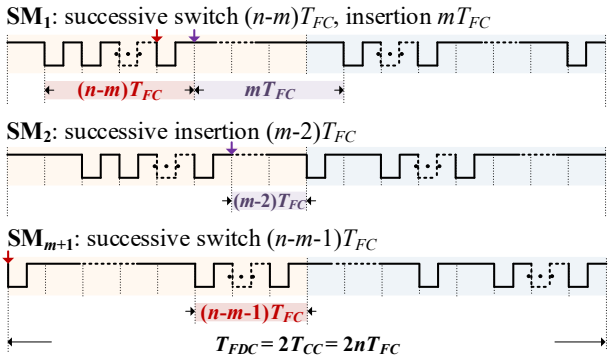


Fig. 4 Various switching patterns for SM_1, SM_2 and SM_{m+1} indicating the absence of uniformity in direct dual-circulant modulation.

dual circulant cycle. According to each column vector of $\boldsymbol{DS}$, each SM switches 4 times within 8 fundamental cycles in this case, and the switching frequency keeps $f_{SW} = \frac{2(n-m)}{2n} f_{FC} = \frac{1}{2} f_{FC}$ for the dual-circulant modulation, which is same with that of $\boldsymbol{S}$ or $\boldsymbol{S}'$.

IV. Optimization of Dual-Circulant Modulation

The direct dual-circulant modulation promises the inherent SM balancing in MMDC, but the direct alternation of two switching sets results in the patterns of each SM varying, which may result in the absence of SM uniformity, the difference of SM lifespan and the difficulty of refined design. This issue will be solved and further optimized in this section.

A. Reallocated dual-circulant modulation

For each SM, the two circular pattern sets are cut off at different breakpoints and then combined forming various switching patterns. As shown in Fig. 4, switching patterns of SM_1, SM_2 and SM_{m+1} are illustrated in detail as a clear example to show their difference. Within the full dual-circulant cycle for $2nT_{FC}$, SM_1 successively switches $n-m$ times in maximum, which inherits from the basic circular set. Following that, the maximum insertion duration of SM_1 keeps mT_{FC} that appears around the breakpoint of two circular set. For SM_2, the successive insertion around the breakpoint reduces to mT_{FC}. For SM_{m+1}, it would successively switch only $n-m-1$ times in the first circular set before the breakpoint, then a continued insertion period for only $(m-1)\,T_{FC}$ inheriting from the additional circular set follows. Switching patterns of SM_1, SM_2 and SM_{m+1} are all different, indicating that the uniformity of SM is absent. This brings the difficulties of predicting the SM capacitor voltage ripples and thermal distribution, and further spreads the difference of operating condition and lifespan of each SM.

Thus, the switching patterns need to be reallocated to keep the SM uniformity. As shown in Fig. 5(a), the reallocated pattern of SM_1 is generated by alternatively extracting from two circular sets. Within the full dual-circulant cycle for $T_{FDC} = 2nT_{FC}$, the switching patterns of 1st, 3rd, 5th, ⋯, (2n-1)th T_{FC} accordingly refer that of 1st, 2nd, 3rd, ⋯, nth ones in the basic circular pattern set, and 2nd, 4th, 6th, ⋯, 2nth T_{FC} refer the patterns in the additional set in sequence. All SMs would equally share the same circular switching patterns as illustrated in Fig. 5(b). The latter SM action lags behind the former one for $2T_{FC}$, and each SM repeats the patterns for every $2nT_{FC}$.

The switching matrix of the reallocated patterns is denoted as $\boldsymbol{DS_A}$, and it can be considered as the combination of the alternated row vectors from $\boldsymbol{S}$ and $\boldsymbol{S}'$ as

$$\boldsymbol{DS_A} = [\boldsymbol{S_1^T}\ \boldsymbol{S'^T_1}\ \boldsymbol{S_2^T}\ \boldsymbol{S'^T_2}\ \boldsymbol{S_3^T}\ \boldsymbol{S'^T_3}\ \cdots\ \boldsymbol{S_n^T}\ \boldsymbol{S'^T_n}]^T \qquad (17)$$

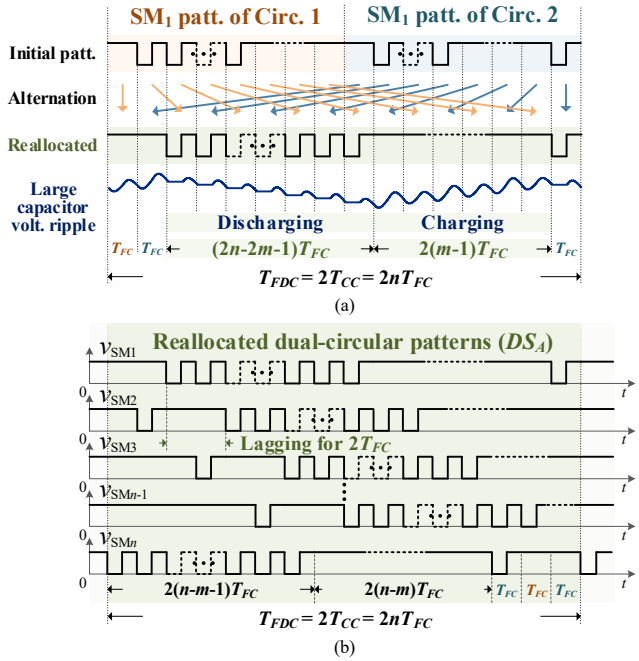


Fig. 5 Reallocated dual-circulant modulation with switching pattern alternation. (a) Switching patterns of SM1 with switching patterns from two sets alternated, which results successive charging and discharging periods and large SM capacitor voltage ripple. (b) Unified switching patterns for all n SMs (denoted as $\boldsymbol{DS_A}$).

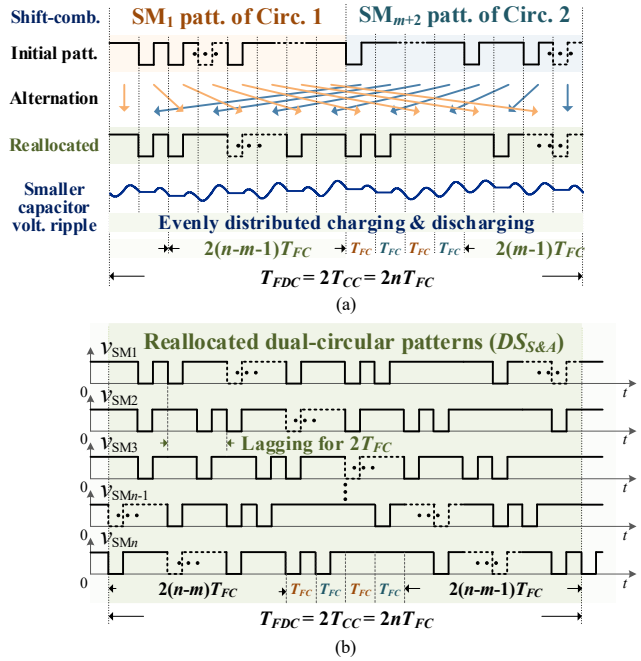


Fig. 6 Optimized dual-circulant modulation with switching pattern shift-combination and alternation. (a) Switching patterns of SM_1 with patterns from additional circular set shifted, charging and discharging periods are evenly distributed and SM capacitor voltage ripple is reduced. (b) Unified and optimized switching patterns for all n SMs (denoted as $\boldsymbol{DS_{S\&A}}$).

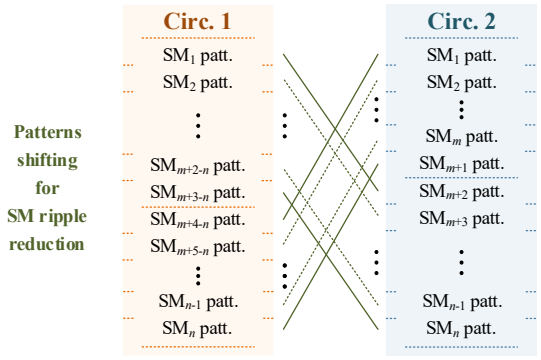


Fig. 7 Couples of switching patterns for combination with the patterns from the additional circular set shifting $(m+1)T_{FC}$.

where $\boldsymbol{S_1}, \boldsymbol{S_2}, \boldsymbol{S_3}, \cdots, \boldsymbol{S_n}$ and $\boldsymbol{S'_1}, \boldsymbol{S'_2}, \boldsymbol{S'_3}, \cdots, \boldsymbol{S'_n}$ are the row vectors in $\boldsymbol{S}$ and $\boldsymbol{S'}$, which denote one of the n stack switching states in a circular set. Since elementary row operations of the matrix including row interchange would not change the matrix rank [28], the rank of $\boldsymbol{DS_A}$ should be same with $\boldsymbol{DS}$. Thus, $\boldsymbol{DS_A}$ would be still a full-rank matrix that always promises the inherent balancing for dual-circulant modulation.

B. Optimized dual-circulant modulation

The reallocated dual-circulant modulation resolves the absence of SM uniformity in direct dual-circulant modulation, but it enlarges the SM capacitor voltage ripple because the successive charging and discharging periods are doubled. As shown in Fig. 5(a), the fundamental cycles with switching actions (corresponding to the "0" elements in switching matrix, called action cycles for short) and the fundamental cycles without switching actions (corresponding to the "1" elements in switching matrix, called insertion cycles for short) from two circular sets would be gathered. According to the operating principles of the MMDC, the SM capacitor would be discharged in each action cycle and charged in each insertion cycle. Compared with dual-circulant modulation without reallocation process, the SM capacitor voltage ripple would be almost doubled since $2n-2m-1$ discharging-action cycles and $2(m-1)$ charging-insertion cycles from two circular cycles are assembled. Considering that the SM voltage ripple has to be suppressed within a reasonable range, a larger SM capacitor is demanded resulting in the increase of costs and volume.

The switching patterns need to be reordered and optimized for SM capacitor ripple reduction. Noting that the SM uniformity can be obtained so long as the patterns are alternately extracted from two circulant sets in sequence, it is not necessary to choose the first pattern from the additional circulant set inserting behind the first pattern from the basic set as (17). Each pattern can be considered as the beginning of the alternation to generate different switching matrixes, and the generated patterns with evenly distributed charging and discharging cycles would be chosen and applied. Focusing on the switching sequence of each SM, it can be noticed as Fig. 6(a) that SM_1 begins the successive switching actions from the 2nd T_{FC} for the first basic circular set, and SM_{m+2} begins the successive switching actions from the 2nd T_{FC} for the second additional circular set. Alternating the switching patterns from these two different SMs, a new switching pattern is generated. The charging-insertion cycles from the second sequence are interspersed into the discharging-action cycles from the first one. The charging and discharging periods are evenly distributed, and the SM capacitor voltage ripple can be reduced. Similarly for all the other SMs, the couples of switching patterns can be obtained following the map in Fig. 7. The second circular set is shifted $m+1$ fundamental cycles, and then alternatively combined with the patterns from the first set. The patterns of SM_2 in the first circular set would be combined with that of SM_{m+3} in the second one, following that until SM_{m+3-n} in the first set combines with SM_n in the second set. Then SM_{m+4-n} in the first set reverses back to combine with SM_1 in the second set, and SM_n in the first set would couple with SM_{m+1} in the second set.

Considering that the patterns are still alternatively extracted from the two circular sets, the uniformity of SM action is kept as shown in Fig. 6(b), and the smaller capacitor voltage ripple has been also achieved thanks to the evenly distributed charging and discharging cycle, which both benefit to reduce the overall costs of MMDC. The switching matrix of the optimized dual-circulant modulation with patterns shift-combined and alternated is denoted as $\boldsymbol{DS_{S\&A}}$, and it can be also considered as the combination of row vectors from $\boldsymbol{S}$ and $\boldsymbol{S'}$ as (18) at the bottom of the page. $\boldsymbol{DS_{S\&A}}$ should be also full-rank like $\boldsymbol{DS}$ that always promises the inherent balancing capability.

C. Illustration Example and Comparison

Following the analyses for the 4-SM MMDC in former section, it can be observed that each column vector of $\boldsymbol{DS}$ in (16) has different element sequence indicating the various switching patterns for each SM with direct dual-circulant modulation. The reallocation should be applied in order to keep the uniformity of SMs. As shown in (19), $\boldsymbol{DS_A}$ is obtained by directly alternating the vector from $\boldsymbol{S}$ and $\boldsymbol{S'}$. Each row vector from $\boldsymbol{S}$ follows with the corresponding row vector from $\boldsymbol{S'}$. For $\boldsymbol{DS_{S\&A}}$, it can be viewed as that $\boldsymbol{S'}$ is firstly shifted $m+1=3$ times by rows, then row-alternatively combined with $\boldsymbol{S}$.

$$\boldsymbol{DS_A}=\begin{bmatrix}\boldsymbol{S_1}\\ \boldsymbol{S'_1}\\ \boldsymbol{S_2}\\ \boldsymbol{S'_2}\\ \boldsymbol{S_3}\\ \boldsymbol{S'_3}\\ \boldsymbol{S_4}\\ \boldsymbol{S'_4}\end{bmatrix}=\begin{bmatrix}1&1&0&0\\ 1&0&1&0\\ 0&1&1&0\\ 0&1&0&1\\ 0&0&1&1\\ 1&0&1&0\\ 1&0&0&1\\ 0&1&0&1\end{bmatrix},\boldsymbol{DS_{S\&A}}=\begin{bmatrix}\boldsymbol{S_1}\\ \boldsymbol{S'_4}\\ \boldsymbol{S_2}\\ \boldsymbol{S'_1}\\ \boldsymbol{S_3}\\ \boldsymbol{S'_2}\\ \boldsymbol{S_4}\\ \boldsymbol{S'_3}\end{bmatrix}=\begin{bmatrix}1&1&0&0\\ 0&1&0&1\\ 0&1&1&0\\ 1&0&1&0\\ 0&0&1&1\\ 0&1&0&1\\ 1&0&0&1\\ 1&0&1&0\end{bmatrix} \quad (19)$$

All the four column vectors in $\boldsymbol{DS_A}$ and $\boldsymbol{DS_{S\&A}}$ are respectively have the same sequence of elements with the later one moving backward two bits referring to the former one, which indicates that all SMs share the same switching patterns after the reallocation with the later one lagging behind the former one for two T_{FC}. Considering that there are only elementary row interchanges among them, the rank of $\boldsymbol{DS_A}$ and $\boldsymbol{DS_{S\&A}}$ are same with $\boldsymbol{DS}$ as 4, which indicates the inherent balancing capability of reallocated and optimized dual-circulant modulation.

The features of above-mentioned modulation methods for SM voltage balancing are listed and compared in TABLE I. Circulant modulation shows its superiority that it inherently balances the SM capacitor voltages, which could omit high-speed centralized

$$\boldsymbol{DS_{S\&A}}=[\boldsymbol{S_1^T}\ \boldsymbol{S'^T_{m+2}}\ \ \boldsymbol{S_2^T}\ \boldsymbol{S'^T_{m+3}}\ \cdots\ \boldsymbol{S^T_{m+3-n}}\ \boldsymbol{S'^T_n}\ \ \boldsymbol{S^T_{m+4-n}}\ \boldsymbol{S'^T_1}\ \ \boldsymbol{S^T_{m+5-n}}\ \boldsymbol{S'^T_2}\ \cdots\ \boldsymbol{S^T_n}\ \boldsymbol{S'^T_{m+1}}]^T \quad (18)$$

TABLE I Comparison of Modulation Methods for SM Capacitor Voltage Balancing

	Sensorless inherent balancing capability	Non-coprime case adaptability	SM patterns uniformity	SM capacitor voltage ripple
Traditional sample-sort based balancing	×	√	×	Small
Basic circulant modulation ($\boldsymbol{S}$)	√	×	√	Medium
Direct dual-circulant modulation with switching set alternation ($\boldsymbol{DS}$)	√	√	×	Medium
Reallocated dual-circulant modulation with switching pattern alternation ($\boldsymbol{DS_A}$)	√	√	√	Large
Optimized dual-circulant modulation with switching pattern shift-combination and alternation ($\boldsymbol{DS_{S\&A}}$)	√	√	√	Small

TABLE II Simulation and Experiment Parameters

Parameters	Descriptions	Simulation	Experiment
n	SM number per stack	4 or 10	4 or 6
m	Positive stage inserted SMs	2 or 5	2 or 3
$2V_M$	MV side bus voltage	11 kV	800 V
C_{CU}, C_{CL}	DC-link capacitance	550 μF	550 μF
L_U, L_L	Arm inductance	3.4 mH	330 μH
L_m	Magnetizing inductance	60.8 mH	460 mH
C_{SM}	SM capacitance	400μF (±10%)	60 μF (±10%)
r_T	Transformer turns-ratio	5:2	5:2
T_{FC}	Fundamental cycle	1/3000 s	1/3000 s

communication and computation. Dual-circulant modulation extents the inherent balancing capability under non-coprime cases, and optimized scheme keeps SM uniformity and reduces the ripple with the pattern alternation and shift-combination.

V. Simulation and Experiment Verification

In order to validate the theoretical analysis for the inherent balancing capability of dual-circulant modulation, a full-scale DAB-based MMDC model is built in the MATLAB/Simulink environment, and a down-scaled prototype is also implemented with parameters both shown as TABLE II. It should be noted that the SM capacitances are set with 10% variation and the initial voltages of each SM capacitor are set to be unbalanced in simulation, and the SM capacitances also have 10% variation due to manufacturing tolerances in experiment, which validates the independence of inherent balancing capability with hardware uniformity and initial state.

A. Simulation verification

The simulation results of the 4-SM case are shown in Fig. 8. During each fundamental cycle, there are two SMs inserted and the other two bypassed in the positive stage as $m = 2$, and all SMs inserted in the negative stage.

Basic circulant modulation is applied as Fig. 8(a). All SMs shares the same circular switching patterns with the latter SM lagging behind the former one for one T_{FC}. Each SM repeats the switching patterns every circulant cycle $T_{CC} = 4T_{FC}$, during which the SM switches twice resulting in the average switching frequency equaling $f_{FC}/2$. Considering the non-coprime of n and m, the rank of switching matrix $\boldsymbol{S}$ is 3<4, the SM voltages tend to unbalanced. The capacitor voltage is about 1.3kV for SM_2 and SM_4, while the voltage reaches 2.3kV for SM_1 and SM_3 that is 78% higher than the other two. The inherent balancing capability is absence in basic circulant modulation.

Direct dual-circulant modulation is applied as Fig. 8(b) referring the switching matrix $\boldsymbol{DS}$ in (16) to rebalance the SM voltages. The basic circular switching set is dashed by pale orange and the additional circular switching set is marked by blue. With the two sets alternation, the SM voltages tend to converge at 1.8kV, which verifies the inherent balancing capability of the dual-circulant modulation. However, the SM uniformity is absent in direct dual-circulant modulation with switching patterns being different among SMs.

Reallocated and optimized dual-circulant modulations are conducted as Fig. 8(c) and (d) following the switching matrix $\boldsymbol{DS_A}$ and $\boldsymbol{DS_{S\&A}}$ in (19), respectively. Each SM share the same switching sequence with the later SM lagging behind the previous one for $2T_{FC}$. The inherent balancing capability is kept that each SM capacitor voltage equals about 1.8kV.

The 4-SM case above is clear for showing the switching patterns and inherent balancing capability of the dual-circulant

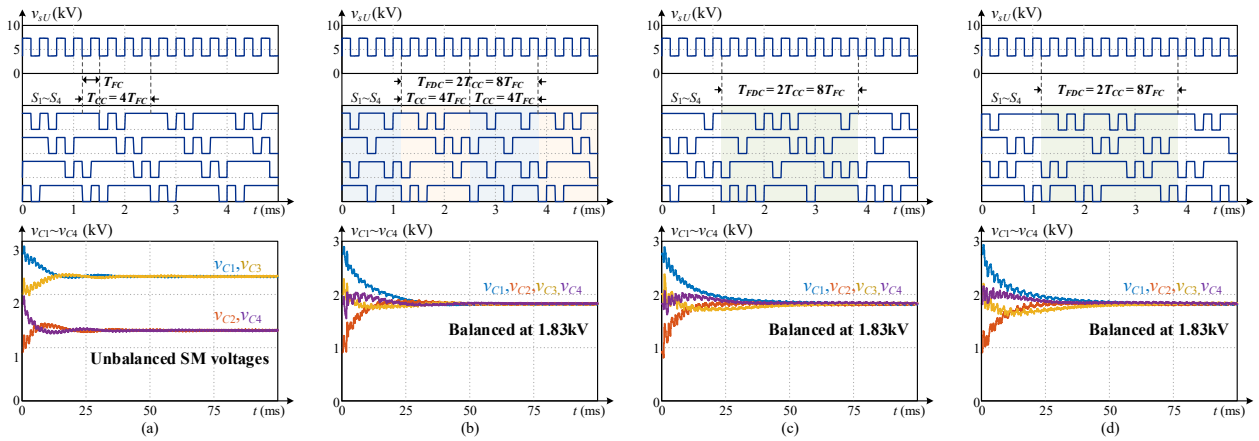


Fig. 8 Upper stack voltage and SM driving signals, and dynamic SM capacitor voltages of $n = 4, m = 2$ case. (a) Basic circulant modulation ($\boldsymbol{S}$), SM unbalanced. (b) Direct dual-circulant modulation ($\boldsymbol{DS}$) with switching set alternation, SM balanced but patterns varied. (c) Reallocated dual-circulant modulation ($\boldsymbol{DS_A}$) with switching pattern alternation, SM balanced and patterns unified. (d) Optimized dual-circulant modulation ($\boldsymbol{DS_{S\&A}}$) with switching pattern shift-combination and alternation, SM balanced and patterns unified.

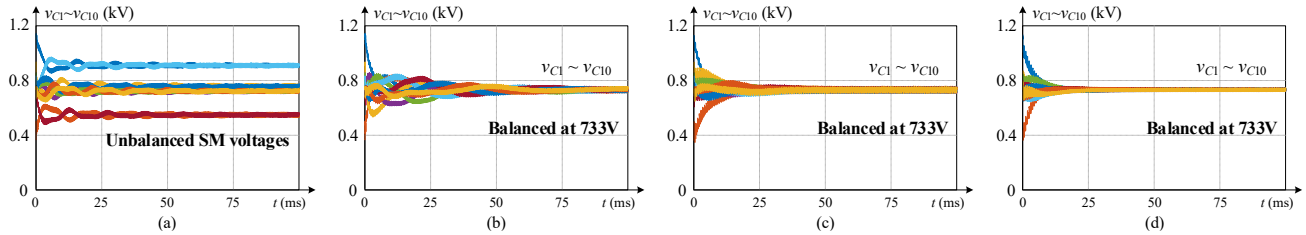


Fig. 9 Dynamic SM capacitor voltages of $n = 10, m = 5$ case. (a) Basic circulant modulation ($\boldsymbol{S}$), SM unbalanced. (b) Direct dual-circulant modulation ($\boldsymbol{DS}$), SM balanced. (c) Reallocated dual-circulant modulation ($\boldsymbol{DS_A}$), SM balanced. (d) Optimized dual-circulant modulation ($\boldsymbol{DS_{S\&A}}$), SM balanced.

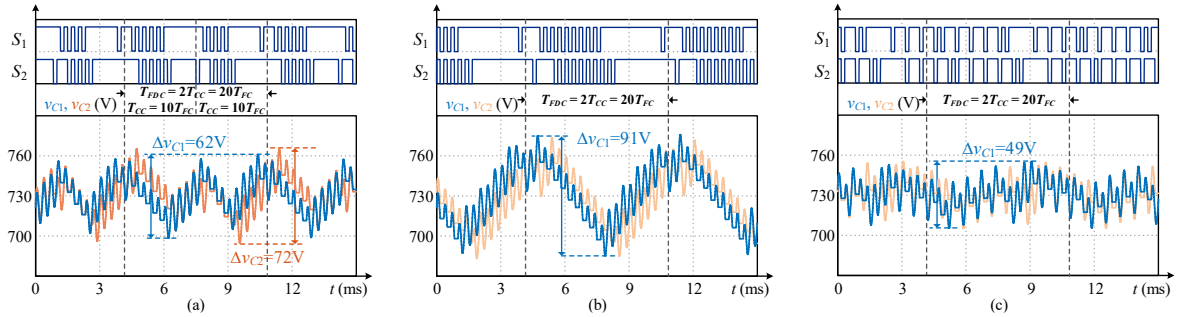


Fig. 10 Switching patterns and SM capacitor voltage ripples of $n = 10, m = 5$ case. (a) Different ripple under direct dual-circulant modulation. (b) Identical but large ripple under reallocated dual-circulant modulation. (c) Identical and reduced ripple under optimized dual-circulant modulation.

modulation, but the SM voltage ripples under different switching patterns are quite similar. The ripple reduction effectiveness of the optimized dual-circulant modulation is not apparent in the case with less SMs.

Expanding the SM number in one stack, the switching patterns and SM voltage ripples of the 10-SM case ($m = 5$) are recorded to provide a clearer comparison for dual-circulant modulations with the inherent balancing capability being double-checked. It illustrates in Fig. 9 that the basic circulant modulation results in the unbalanced SM capacitor voltages with the maximum one being 63% higher than the minimum one, and the dual-circulant modulations help to balance the SM voltages at 733V as desired. For the direct dual-circulant modulation with switching patterns alternated by set as shown in Fig. 10(a), the switching patterns of each SM are different from each other. Different charging and discharging sequences are assigned to each SM resulting that the SM capacitor voltage ripples vary. The ripple of SM_1 and SM_2 are about 72V and 62V respectively with 17% difference. The reallocated dual-circulant modulation alternatively extracts patterns from two circular sets, which unifies the SM patterns and results in the same capacitor voltage ripple for each SM. But as shown in Fig. 10(b), the ripple is larger than the former direct set-alternation one. The charging-insertion periods and discharging-action periods are gathered, which leads to successive charging and discharging periods almost doubled compared with the set-alternation case, and the common ripple value is enlarged to be 91V that is 34% higher than the averaged ripple in set-alternation case. Thus, the optimized dual-circulant modulation should be applied to reduce the ripple that the circular patterns in the second set is firstly shifted by $m + 2 = 7$ fundamental cycles, then alternatively combined with that in the first set. As shown in Fig. 10(c), the action cycles and the insertion cycles are distributed evenly, and the successive charging and discharging periods are avoided. The capacitor voltage ripple is significantly reduced to 49V for all the SMs. It is not only almost the half of the former reallocated one, but also 28% lower than the averaged ripple of direct dual-circulant modulation.

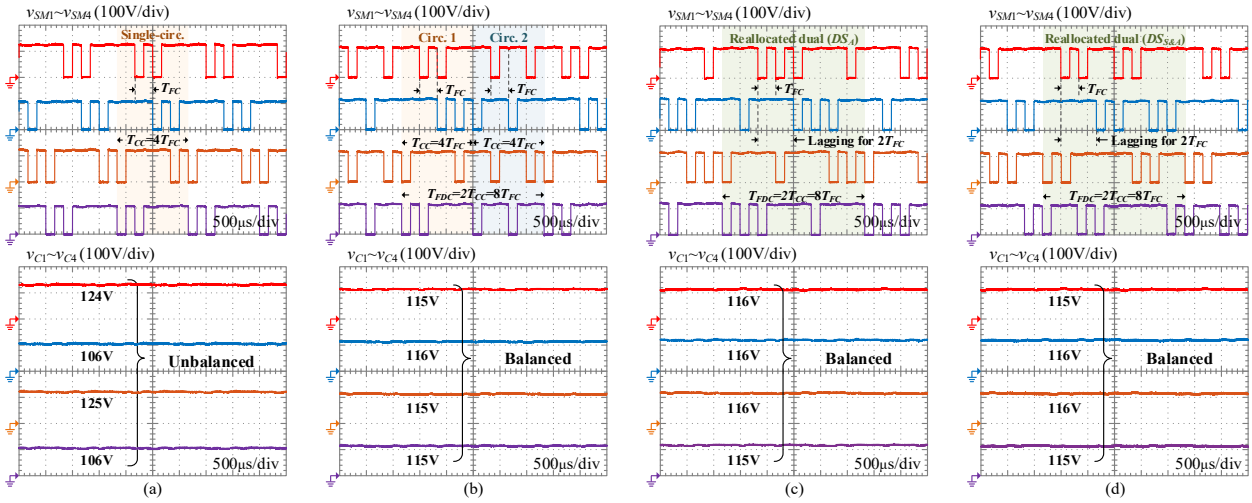


Fig. 11 Experimental results for n=4, m=2 case. (a) SM output voltages with unbalanced SM capacitor voltages under basic circulant modulation. (b) SM output voltages with balanced SM capacitor voltages under direct dual-circulant modulation. (c) SM output voltages with balanced SM capacitor voltages under reallocated dual-circulant modulation. (d) SM output voltages with balanced SM capacitor voltages under optimized dual-circulant modulation.

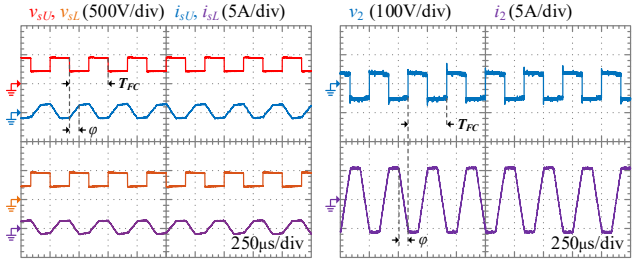


Fig. 12 Experimental results of n=4, m=2 under balanced cases. (a) Voltages and currents of upper and lower stacks. (b) Voltages and currents of output side of ac passive stage.

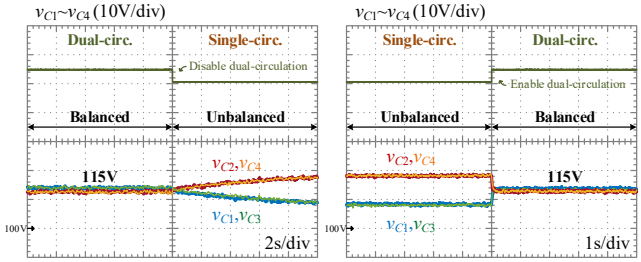


Fig. 13 Dynamic responses of SM capacitor voltages after enabling or disabling the dual-circulant modulation.

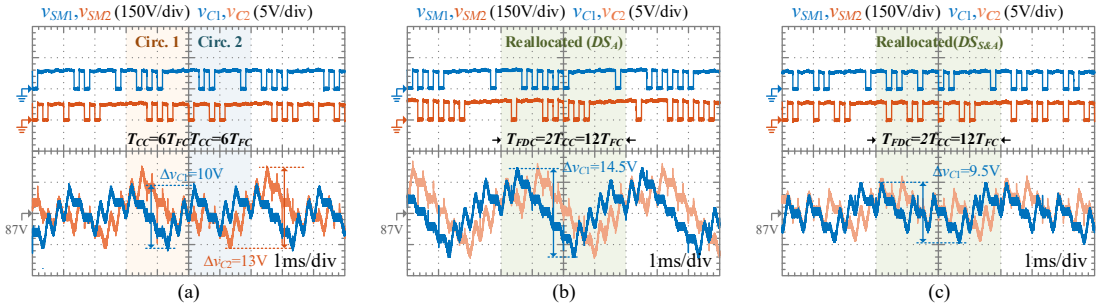


Fig. 14 Experimental results of SM output voltages and capacitor voltages for $n = 6, m = 3$ under dual-circulant modulations. (a) Different ripple under direct dual-circulant modulation with switching set alternation ($\boldsymbol{DS}$). (b) Identical but large ripple under reallocated dual-circulant modulation with switching pattern alternation ($\boldsymbol{DS_A}$). (c) Identical and reduced ripple under optimized dual-circulant modulation with switching pattern shift-combination and alternation ($\boldsymbol{DS_{S\&A}}$)

B. Experimental Verification

Experiments are firstly conducted on the 4-SMs prototype with n=4, m=2 operating condition as a typical non-coprime case. Similarly with the simulation results, SM capacitor voltages are unbalanced with over 20% variation under basic circulant modulation as shown in Fig. 11(a), but balanced at about 115V under three kinds of dual-circulant modulation as Fig. 11(b)~(d).

The complemental operation of upper and lower stack is shown in Fig. 12(a) with stack voltages and currents presented. And the secondary-side voltage and current of internal transformer are illustrated in Fig. 12(b) depicting that the phase-shift angle φ is set as $\pi/2$ for the maximum power output as that in classical DAB converters

The dynamic responses of SM capacitor voltages for switching between dual-circulant modulation and basic circulant modulation are shown in Fig. 13. Fig. 13(a) shows that all the SM capacitor voltages are well balanced at about 115V with dual-circulant modulation at beginning. After disabling the dual-circulation and using the basic circulant modulation, the SM voltages tend to split with over 20% variation. The reverse process is provided in Fig. 13(b), showing that the SM voltages are immediately rebalanced after applying the dual-circulant modulation, which verifies its inherent balancing capability for converging SM capacitor voltages.

In order to further compare the SM capacitor ripples under three kinds of dual-circulant modulation, experiments are conducted on an extended 6-SM prototype. With direct dual-circulant modulation ($\boldsymbol{DS}$), the switching patterns of SM_1 and SM_2 are different resulting in various SM capacitor voltage ripples as Fig. 14(a). The ripple of SM_1 and SM_2 are about 10V and 13V respectively with 33% difference. Then the reallocation ($\boldsymbol{DS_A}$) is applied as shown in Fig. 14(b), which unifies the SM patterns and the capacitor voltage ripple, but it enlarges the SM ripple to 14.5V that is 26% higher than the averaged ripple with $\boldsymbol{DS}$. Finally, the optimized dual-circulant modulation ($\boldsymbol{DS_{A\&S}}$) helps to evenly distribute the charging and discharging periods, then the capacitor voltage ripple is reduced to 9.5V for all SMs as Fig. 14(c). It is not only 34% lower than the former reallocated one, but also 17% lower than that of set-alternation case.

VI. Conclusion

This paper proposes the dual-circulant modulation for the MMDC that promises the inherent balancing capability of SM capacitor voltages for arbitrary SM number including non-prime cases. The switching matrix is extended to complete constrains on SM voltages with two sets of circular switching patterns preset and combined. The associated polynomial of circulant matrix is introduced providing a new perspective on coprime criterion of basic circulant modulation, and the coprime of polynomials further proves the full-rank feature of dual-circulant modulation that promises the inherent balancing capability under any operation cases. The switching patterns are then reallocated to keep the SM uniformity and further reordered to optimize the SM capacitor voltage ripple. Simulations and experiments are conducted corresponding to the theoretical analysis, which verifies the effectiveness of the proposed dual-circulant modulation with both inherent voltage balancing and SM ripple optimization.

References

[1] X. Zhang and T. C. Green, "The Modular Multilevel Converter for High Step-Up Ratio DC–DC Conversion," *IEEE Trans. Ind. Electron.*, vol. 62, no. 8, pp. 4925-4936, Aug. 2015.

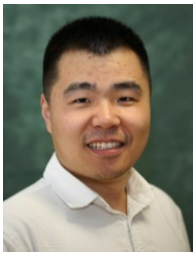
[2] S. Dey and T. Bhattacharya, "A Transformerless DC–DC Modular Multilevel Converter for Hybrid Interconnections in HVDC," *IEEE Trans.*

Ind. Electron., vol. 68, no. 7, pp. 5527-5536, July 2021.
[3] E. Solas, G. Abad, J. A. Barrena, S. Aurtenetxea, A. Cárcar and L. Zając, "Modular Multilevel Converter With Different Submodule Concepts—Part I: Capacitor Voltage Balancing Method," *IEEE Trans. Ind. Electron*., vol. 60, no. 10, pp. 4525-4535, Oct. 2013.
[4] S. Shao, M. Jiang, J. Zhang and X. Wu, "A Capacitor Voltage Balancing Method for a Modular Multilevel DC Transformer for DC Distribution System," *IEEE Trans. Power Electron.*, vol.33, no.4, pp.3002-3011, 2018.
[5] X. Xiang, X. Zhang, T. Luth, M. M. C. Merlin and T. C. Green, "A Compact Modular Multilevel DC–DC Converter for High Step-Ratio MV and HV Use," *IEEE Trans. Ind. Electron*., vol. 65, no. 9, pp. 7060-7071, Sept. 2018.
[6] H. Yang and M. Saeedifard, "A Capacitor Voltage Balancing Strategy with Minimized AC Circulating Current for the DC–DC Modular Multilevel Converter," *IEEE Trans. Ind. Electron*., vol. 64, no. 2, pp. 956-965, Feb. 2017.
[7] W. van der Merwe, "Natural Balancing of the 2-Cell Modular Multilevel Converter," *IEEE Trans. Ind. App.*, vol. 50, no. 6, pp. 4028-4035, 2014.
[8] T. Zheng et al., "A Novel High-Voltage DC Transformer Based on Diode-Clamped Modular Multilevel Converters With Voltage Self-Balancing Capability," *IEEE Trans. Ind. Electron*., vol. 67, no. 12, pp. 10304-10314, 2020.
[9] Y. Liu and F. Z. Peng, "A Modular Multilevel Converter With Self-Voltage Balancing Part I: Mathematical Proof," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 8, no. 2, pp. 1117-1125, June 2020.
[10] Y. Liu and F. Z. Peng, "A Modular Multilevel Converter With Self-Voltage Balancing Part II: Y-Matrix Modulation," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 8, no. 2, pp. 1126-1133, June 2020.
[11] Y. Qiao, X. Zhang, X. Xiang, and et al., "Trapezoidal Current Modulation for Bidirectional High-Step-Ratio Modular DC–DC Converters," *IEEE Trans. Power Electron.*, vol. 35, no. 4, pp. 3402-3415, April 2020.
[12] X. Xiang, Y. Qiao, and et al., "Analysis and Criterion for Inherent Balance Capability in Modular Multilevel DC–AC–DC Converters," *IEEE Trans. Power Electron.*, vol. 35, no. 6, pp.5573-5580, June 2020.
[13] N. Lin and V. Dinavahi, "Dynamic Electro-Magnetic-Thermal Modeling of MMC-Based DC–DC Converter for Real-Time Simulation of MTDC Grid," *IEEE Trans. Power Delivery*, vol. 33, no. 3, pp. 1337-1347, 2018.
[14] P. Davis, *Circulant Matrices*, 2nd ed. Providence, RI, USA: Amer. Math. Soc., 2012.
[15] X. Xiang, Y. Gu, K. Chen, A. Astolfi and T. C. Green, "On the dynamics of inherent balancing of modular multilevel DC–AC–DC converters," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 34–40, Jul. 2021
[16] S. Shao, Y. Li, J. Sheng, C. Li, W. Li, J. Zhang and X. He, "A Modular Multilevel Resonant DC–DC Converter," *IEEE Trans. Power Electron.*, vol. 35, no. 8, pp. 7921-7932, Aug. 2020.
[17] P. A. Gray, Z. C. Ma and P. W. Lehn, "A High-Frequency MMC for DC–DC Applications Using a Three-Winding Transformer With DC Flux Cancellation," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 3, no. 3, pp. 647-657, July 2022.
[18] C. Pineda, J. Pereda, F. Rojas, C. Cerda, X. Zhang and A. J. Watson, "Asymmetrical Triangular Current Mode (ATCM) for Bidirectional High Step Ratio Modular Multilevel Dc–Dc Converter," *IEEE Trans. Power Electron.*, vol. 35, no. 7, pp. 6906-6915, July 2020.
[19] S. Du, B. Wu, K. Tian, D. Xu and N. R. Zargari, "A Novel Medium-Voltage Modular Multilevel DC–DC Converter," *IEEE Trans. Ind. Electron*., vol. 63, no. 12, pp. 7939-7949, Dec. 2016.
[20] Q. Song, B. Zhao, J. Li, and W. Liu, "An improved DC solid state transformer based on switched capacitor and multiple-phase-shift shoot-through modulation for integration of LVDC energy storage system and MVDC distribution grid," *IEEE Trans. Ind. Electron.*, vol. 65, no. 8, pp. 6719–6729, Aug. 2018.
[21] P. D. Judge, G. Chaffey, M. M. C. Merlin, P. R. Clemow and T. C. Green, "Dimensioning and Modulation Index Selection for the Hybrid Modular Multilevel Converter," *IEEE Trans. Power Electron.*, vol. 33, no. 5, pp. 3837-3851, May 2018.
[22] X. Yuan, H. Stemmler, and I. Barbi, "Investigation on the clamping voltage self-balancing of the three-level capacitor clamping inverter", in *30th Annual IEEE Power Electronics Specialists Conference*, pp. 1059–1064, Jul. 1999.
[23] S. Fan et al., "Inherent SM Voltage Balance for Multilevel Circulant Modulation in Modular Multilevel DC–DC Converters," *IEEE Trans. Power Electron.*, vol. 37, no. 2, pp. 1352-1368, Feb. 2022.
[24] A. W. Ingleton, "The Rank of Circulant Matrices," *J. London Mathematical* Society, vol. s1-31, no. 4, pp. 445–460, Oct. 1956.
[25] Y. Fan and H. Liu, "Double circulant matrices," *Linear and Multilinear Algebra*, vol. 66, no. 10, pp. 2119–2137, Oct. 2017.
[26] V. V. Prasolov, "Irreducible Polynomials," in *Polynomials*, 2th ed. Berlin, Germany: Spring, 2001, pp. 60-61.
[27] T. H. Cormen, C. E. Leiserson, R. L. Rivest, et al., "Greatest common divisor," in *Introduction to Algorithms*, 2nd ed. Cambridge, MA: MIT Press and McGraw-Hill, 2001, pp. 859-861.
[28] D. C. Lay, S. R. Lay and J. J. McDonald, *Linear Algebra and Its Applications*, 5th ed. London, England: Pearson, 2016, pp. 6-7.

Shiyuan Fan received the B.Sc. degree in electrical engineering and its automation from North China Electric Power University, Beijing, China, in 2018. She is currently working toward the Ph.D. degree in electrical engineering with Zhejiang University, Zhejiang, China.

Her research interests include topology, modulation and control of modular multilevel converters.

Xin Xiang (S'17-M'18) received the B.Sc. degree from Harbin Institute of Technology, China in 2011, the M.Sc. degree from Zhejiang University, China in 2014 and the Ph.D. degree from Imperial College London, UK in 2018, all in Electrical and Electronic Engineering. He has received the Eryl Cadwaladr Davies Prize for the Best Ph.D. Thesis of Electrical and Electronic Engineering Department in Imperial College London, and he was also the recipient of the Best Ph.D. Thesis Award from IEEE PELS UK and Ireland Chapter. From 2018 to 2020, he was a Research Associate with Imperial College London, UK. He is currently a tenure-track Associate Professor in the College of Electrical Engineering, Zhejiang University, China. His research interests include the analysis and control of power electronics converters for power system applications.



Chushan Li (S'11-M'17) received the B.E.E. degree and Ph.D. degree in electrical engineering from the Department of Electrical Engineering, Zhejiang University, Hangzhou, China, in 2008 and 2014, respectively. Currently, he is an assistant professor in Zhejiang University – University of Illinois at Urbana-Champaign Institute, Zhejiang, China.

From April to September in 2008, he was an internship student with the Power Application Design Center in National Semiconductor (Hong Kong) Co.Ltd. From December 2010 to October 2011, he was a visiting scholar with the Freedm Center in North Carolina State University. From December 2013 to June 2014, he was a research assistant in Hong Kong Polytechnic University. From July 2014 to July 2017, he was a postdoctoral fellow in Department of Electrical and Computer Engineering, Ryerson University, Canada. His research interest includes high power density power converter design and Transportation Electrification.

Yunjie Gu (M'16- SM'20) received the B.Sc. and the Ph.D. degree in Electrical Engineering from Zhejiang University, Hangzhou, China, in 2010 and 2015 respectively. He was a Consulting Engineer with General Electric Global Research Centre, Shanghai, China, from 2015 to 2016. After that, he joined Imperial College, UK, under the sponsorship of the UKRI Innovation Fellowship. He is currently a Lecturer (Assistant Professor) with the University of Bath, UK, and an Honorary Lecturer at Imperial College. His research focuses on the fundamental theories and computational tools for analyzing power system dynamics, as well as the algorithms and software for power conversion control.

Huan Yang (M'09) received the B.Sc. and Ph.D. degrees in Electrical Engineering & its Automation and Electrical Engineering from Zhejiang University, Hangzhou, China, in 2003 and 2008, respectively.

From January 2009 to March 2011, he was a Postdoctoral Fellow at Zhejiang University. In March 2011, he became a faculty member in Zhejiang University as a Research Associate. In December 2012, he became an Associate Professor of Electrical Engineering at Zhejiang University. From April 2012 to April 2013, he conducted joint research in Fuji Electric Co., Ltd. as the Oversea Researcher of New Energy and Industrial Technology Development Organization (NEDO), Tokyo, Japan. His research interests include distribution generation and Microgrids, high performance motor systems and smart power distribution equipment. Dr. Yang has published more than 50 papers and holds over 10 issued/pending patents.

Wuhua Li (M'09) received the B.Sc. and Ph.D. degree in Power Electronics and Electrical Engineering from Zhejiang University, Hangzhou, China, in 2002 and 2008, respectively.

From 2004 to 2005, he was a Research Intern, and from 2007 to 2008, a Research Assistant in GE Global Research Center, Shanghai, China. From 2008 to 2010, he joined the College of Electrical Engineering, Zhejiang University as a Post doctor. In 2010, he was promoted as an Associate Professor. Since 2013, he has been a Full Professor at Zhejiang University. From 2010 to 2011, he was a Ryerson University Postdoctoral Fellow with the Department of Electrical and Computer Engineering, Ryerson University, Toronto, ON, Canada. He is currently the Executive Deputy Director of the National Specialty Laboratory for Power Electronics and the Vice Director of the Power Electronics Research Institute, Zhejiang University. His research interests include power devices, converter topologies and advanced controls for high power energy conversion systems. Dr. Li has published more than 300 peer-reviewed technical papers and holds over 50 issued/pending patents.

Due to his excellent teaching and research contributions, Dr. Li received the 2012 Delta Young Scholar from Delta Environmental & Educational Foundation, 2012 Outstanding Young Scholar from National Science Foundation of China (NSFC), 2013 Chief Youth Scientist of National 973 Program, 2014 Young Top-Notch Scholar of National Ten Thousand Talent Program, 2019 Distinguished Young Scholar from National Science Foundation of China. He serves as the Associated Editor of Journal of Emerging and Selected Topics in Power Electronics, IET Power Electronics, CSEE Journal of Power and Energy Systems, CPSS Transactions on Power Electronics and Applications, Proceedings of the Chinese Society for Electrical Engineering, Guest Editor of IET Renewable Power Generation for Special Issue "DC and HVDC system technologies", Member of Editorial Board for Journal of Modern Power System and Clean Energy.

He received one National Natural Science Award and four Scientific and Technological Achievement Awards from Zhejiang Provincial Government and the State Educational Ministry of China. He was appointed as the Most Cited Chinese Researchers by Elsevier since 2014.

Xiangning He (M'95--SM'96--F'10) received the B.Sc. and M.Sc. degrees from Nanjing University of Aeronautical and Astronautical, Nanjing, China, in 1982 and 1985, respectively, and the Ph.D. degree from Zhejiang University, Hangzhou, China, in 1989.

From 1985 to 1986, he was an Assistant Engineer at the 608 Institute of Aeronautical Industrial General Company, Zhuzhou, China. From 1989 to 1991, he was a Lecturer at Zhejiang University. In 1991, he obtained a Fellowship from the Royal Society of U.K., and conducted research in the Department of Computing and Electrical Engineering, Heriot-Watt University, Edinburgh, U.K., as a Post-Doctoral Research Fellow for two years. In 1994, he joined Zhejiang University as an Associate Professor. Since 1996, he has been a Full Professor in the College of Electrical Engineering, Zhejiang University. He was the Director of the Power Electronics Research Institute, the Head of the Department of Applied Electronics, the Vice Dean of the College of Electrical Engineering, and he is currently the Director of the National Specialty Laboratory for Power Electronics, Zhejiang University. His research interests are power electronics and their industrial applications.

Dr. He is a Fellow of The Institute of Electrical and Electronics Engineers (IEEE) and was appointed as IEEE Distinguished Lecturer by the IEEE Power Electronics Society 2011--2015. He is also a Fellow of the Institution of Engineering and Technology (formerly IEE), U.K.

Timothy. C. Green (M'89–SM'02–F'19) received a B.Sc. (Eng) (first class honours) from Imperial College London, UK in 1986 and a Ph.D. from Heriot-Watt University, Edinburgh, UK in 1990. He is a Professor of Electrical Power Engineering at Imperial College London, and Director of the Energy Futures Lab with a role of fostering interdisciplinary energy research across the university. His research is focused on using the flexibility of power electronics to further the decarbonisation of electricity systems by easing the integrations of renewable sources and EV charging. In HVDC, he has contributed converter designs that strike improved trade-offs between power losses, physical size and fault handling. In distribution systems, he has pioneered the use of soft open points and the study of stability of grid connected inverters. Prof. Green is a Chartered Engineering in the UK and a Fellow of the Royal Academy of Engineering.