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Towards a Bionic Neural Link for Implantable Prosthetics

Xiaoying Li*, Timothy G. Constandinou†, Amir Eftekhar*†, Pantelis Georgiou*† and Chris Toumazou†
*Department of Electrical and Electronic Engineering, †Institute of Biomedical Engineering
Imperial College London, South Kensington Campus, London, SW7 2AZ, United Kingdom
Email: {xiaoying.li, t.constandinou, amir.eftekhar, pantelakis.georgiou, c.toumazou}@imperial.ac.uk

***Abstract*—This paper presents a biologically-inspired 'silicon neural link', encompassing a neurochemical sensor array, an asynchronous artificial-neural bus and an interleaved biphasic stimulus generator. The proposed system is intended for neuroprosthetic application; employing an array of ISFET-based spiking neurons to convey measured neuronal data across a damaged neural pathway to a target stimulation site. A 48dB dynamic range is achieved by encoding the neural signal in the time-domain, using accumulating address-events to modulate the biphasic waveform. The electrical stimulation is delivered via a bipolar electrode configuration in a continuous interleave sampling strategy. This has been implemented in a commercially available 0.35μm CMOS technology.**

I. Introduction

Neural prostheses (or neuroprosthetics) is a term generally used to refer to an artificial device, engineered to bypass a dysfunctional element in the neural pathway. This idea was originally expressed in the 1960's, when functional electrical stimulation (FES) was first proposed [1]. Since then, this discipline has progressed to develop several devices for the rehabilitation of both sensory and motor neuron pathways [2]. Some examples include the treatment of foot-drop, orthotics, hand grasp, problems with diaphragm pacing, bladder and bowel control, cochlear and retinal diseases, pain relief, epilepsy and to stimulate bone growth and repair.

It is recent advances in microelectronic technology that have mainly contributed to the massive surge in neuroprosthetic research. Pacemakers and cochlear implants are two prime examples of neuroprosthetic devices that have now become mainstream, proving the benefits, long term biocompatibility and safety of this technology in general. In such examples, the neural rehabilitation has been unidirectional, with a single human/prosthetic-device interface point. This has tended to be either using an external device to bypass a damaged sensory organ, or using artificially generated stimuli to trigger or otherwise modulate a damaged motory action.

A new wave in neuroprosthetic research is now emerging; aiming to develop medical devices to reconnect damaged nerves, measuring activity at a healthy node and providing the necessary stimulus at a target site [3]. Such examples could include restoration of partial lower body motor functioning in spinal cord injury (SCI) patients, where both the input and output of the prosthetic device would interface to different neural targets. We have chosen to call such a device a 'neural link', as the prosthetic device would only serve to bridge the damaged nerve fibres, aiming to restore some functionality.

For such applications, a single integrated circuit may be inadequate, due to the physical proximity between the source and target (neural) sites. For instance, a single-chip solution would be to have the device implanted close to the neural source, to minimise signal degradation due to noise, and thus the stimulation electrode would be connected via relatively long (and therefore lossy) wires.

This work presents a neural link incorporating a 'single-chip' transceiver, designed to be used in pairs; one chip configured as the transmitter and the other as the receiver. By using an asynchronous event-address-representation (AER) [4] to communicate the neural data between devices, the robustness of digital representation can be exploited without the complexity and power requirements of using an ADC and DAC. Furthermore, this adopted representation can be readily interfaced to a low-power, short range RF transceiver to realise a wireless neural link in cases that wiring may be undesirable.

The paper is organised as follows: Part I has introduced neural prostheses and explained the motivation behind this work, Part II describes the philosophy behind the adopted system architecture and outlines the design and implementation for each of the main sub-blocks. Finally, Part III presents block- and system-level simulated results, with target design specification and future work discussed in Part IV. Circuit implementation details are not included in the scope of this paper.

II. System Overview

The system integrates a number of essential stages in establishing the neural link described. In the following sections we will see how these stages function. They include potassium ion (K^+) front-end sensing, sensing level to spike frequency integrate-and-fire and address encoding and communication. This is finally followed by the second in the pairing and includes the address receiver with spike frequency to biphasic current stimuli of proportional magnitude. The complete system architecture is illustrated in Fig. 1.

A. Neural Sensing

Typical methods used in measuring neural activity are based on two main techniques: transmembrane measurements of the action potential using the patch or voltage clamp technique [5] and extracellular recordings using microelectrodes [6]. Although, the former yields high-accuracy information about the electrophysiological properties of the cell, it is an invasive method non-suitable for long-term monitoring. Thus extracellular measurement is preferable, measuring the magnetic field (using cuff electrodes) or electrical field directly (using microelectrodes positioned in close proximity).

This work adopts a different approach; to measure neural activity by extracellular measurement of ion-concentration using chemical microsensors. As modelled by Hodgkin and Huxley [7], the generation of an action potential follows well-defined dynamics involving K^+ and Na^+ ion channels opening within the cellular membrane. As a result, an extracellular chemical microsensor sensitive to K^+ or Na^+ can detect the onset of an action potential. One such sensor is the ion-sensitive field effect transistors (ISFET) [8], which can be made sensitive to potassium ions (K^+). This has the added advantage of being implementable in standard CMOS technology with minimal post-processing (to modify the sensing membrane for K^+ ion selectivity), therefore also allowing for monolithic integration.

The sensor array readout current is subsequently translated to be used as a stimulus current for spike generation at the following stage.

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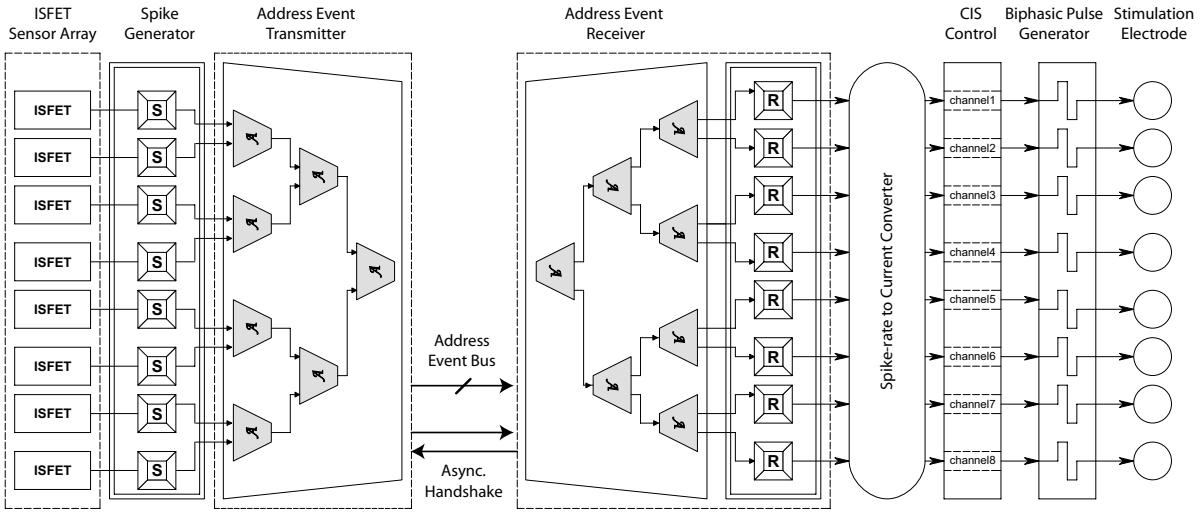

Fig. 1. Top-level system architecture of the bionic neural link, consisting of seven main blocks (shown from left to right): chemical sensor (1×8 array), spiking neuron (1×8 array), AER transmitter, AER receiver, spike-rate converter (1×8 array), CIS controller and biphasic waveform generator (1×8 array)

A spike-domain representation is desired to translate the analogue current magnitude to a stream of discrete pulses, with data encoded in the time-domain. This overcomes signal degradation issues and makes it directly compatible for subsequent address-event encoding. The spike generation stimulus current is obtained by scaling the sensor current using the translinear H-cell topology [9], achieving a linear relation with ionic concentration and also reducing temperature dependance.

B. Spike Encoding

This converts the sensory current-magnitude to a spike train with varying spike density to follow an event-based representation; necessary for the AER communication.

One method to achieve this is to use a neuromorphic silicon neuron. These emulate the electrophysiological behavior of biological neurons. Typically, there are two main neuron types that can be implemented in silicon: conductance-based and integrate-and-fire models. Although conductance-based models typically provide a better representation of biological neurons, we have chosen to implement a leaky integrate-and-fire neuron, to achieve a compact yet versatile design. Specifically, the model proposed in [10] was adapted for this application. This has the following characteristics: (i) tunable threshold value, (ii) tunable refractory period, (iii) explicit leakage current and (iv) well-defined pulse-width, also operating with micropower consumption. The readout of the spike encoder is modulated by the stimulation current (obtained from the H-cell output), the spike frequency of which is designed to be linearly proportional (to the stimulus). Details on circuit design and implementation are provided in [11].

C. Address Event Communication

As the spike train that has been generated is both asynchronous and data-driven in nature, it is ideally suited to an event driven output. One such protocol is the Address Event Representation [4]; used especially in the vision chip arena. The principle behind this data-transmission mechanism is that each pixel has a unique identifier (i.e. its co-ordinate) and when a pixel registers an event this identifier is asserted onto a digital bus. The data is then communicated off-chip through means of an asynchronous handshake. On the receiving end, these address-events are decoded to reconstruct the original spatiotemporal pattern.

AER offers several advantages over alternative methods (such as scanning or multiplexing): (i) the binary address provides the flexibility of mapping from a single pre-synaptic signal to multiple post-synaptic targets, (ii) it explicitly separates the temporal and spatial information, and it is also capable of decoding any address ordering in the receiver chip and (iii) It exhibits the closest resemblance to the action potential representation.

Each element in the array has an *event latch* that locks an elements state on an event until the data has been transmitted off-chip. The event latch initially sends an arbitration request to the *arbitration tree* (Fig. 2). The role of the arbitration tree is to select a single output in case of multiple colliding events. On arbitration (selection of a single event), the chip sends a bus request signal off-chip to the receiving device. The address is read off the bus and then a bus acknowledge signal is relayed back to reset the event latch and reinitialise the transmitter. This selection/arbitration process is repeated for all events waiting to be transmitted. On the receiver end, all incoming events are decoded by means of a binary demultiplexer tree. Subsequently, an acknowledge signal is generated once the event is reconstructed.

D. Pulse-rate to Current Converter

The next stage is to convert the reconstructed pulse train into a current magnitude; required to modulate the charge delivered per stimulation phase. This is achieved using a decimation filter, to effectively downsample the pulse train to a pulse code modulated (PCM) representation, which is then converted to a current using a DAC. The decimation filter is implemented using an 8-bit counter, reset at the stimulation rate and PCM-to-current conversion is using a binary-weighted current-steering structure. Details on circuit design and implementation are provided in [12].

E. Interleaved Biphasic Stimulus Generator

The artificial electrical stimulation is conducted through a bipolar electrode configuration scheme using a continuous interleave sampling (CIS) strategy. These have been chosen to focus the stimuli and thus minimise cross-talk. Moreover, the stimulation profile is designed to take a balanced biphasic waveform; to ensure no overall charge buildup, with refractory period inserted between the inverted

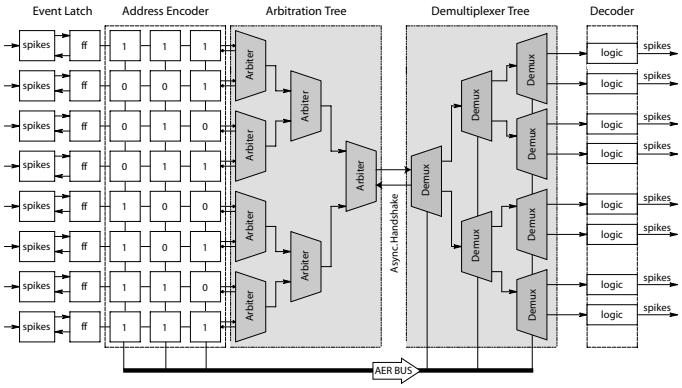

Fig. 2. Asynchronous address-event sender and receiver architecture, based an AER protocol. The sender (shown on left) consists of: event-capture latches, address encoder and arbitration tree. The receiver (shown on right) consists of: demultiplexer tree (address decoder) and event-decoding logic.

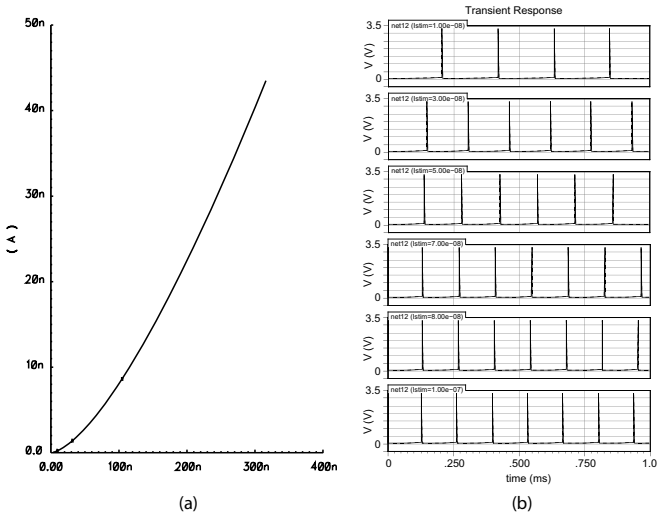

Fig. 3. Front-end simulation results showing: (a) The ISFET sensor H-cell characteristics (I_{isfet} vs. $I_{stim} = h-cell\ o/p$) and (b) The spiking neuron characteristics ($V_{out} = spike\ o/p$ transient behaviour for different values of $I_{stim} = neuron\ i/p$)

phases; to reduce fatigue and thus improve efficiency [13]. The channel interleaving and waveform profile generation is implemented using a custom state-machine design to derive the phases required. In turn, these are used to switch the stimulus current into the stimulation electrodes using an H-bridge configuration, such that the current direction can be reversed, thus driving a reverse current. Details on circuit design and implementation are provided in [12].

III. Simulation Results

The general functionality of the system is verified through both system and circuit-level simulation using Matlab 2006b and Cadence Spectre 5.1.41. The system input functionality is verified by using an ISFET macromodel [14], providing the input current the H-cell module and subsequently to the silicon I&F neuron. Fig. 3(a) illustrates the sensor output current is a linear relation with ionic concentration, with the centre operating point measured is at pH 6.7. Fig. 3(b) shows the neuron firing frequency as a linear function of the ISFET sensor output current, the maximum frequency is 8.9kHz, which corresponds to 50nA stimulation current from the ISFET output.

The system output functionality is verified by using an address-event input stream and monitoring the electrode current outputs, shown in Fig. 4.

The CIS cycle frequency (set to 1KHz) and current gain (set to provide a maximum of 2mA) are made tunable to adapt use to different applications. Fig. 5 illustrates complete front- and back-end system simulations, demonstrating input ionic concentration to event-rate, and event-rate to biphasic stimulus respectively. The input characteristic exhibits a logarithmic relationship between pH input and event-rate output (and thus a linear relationship between ion concentration and event-rate). The output characteristic exhibits a linear relationship between event-rate and output stimulus.

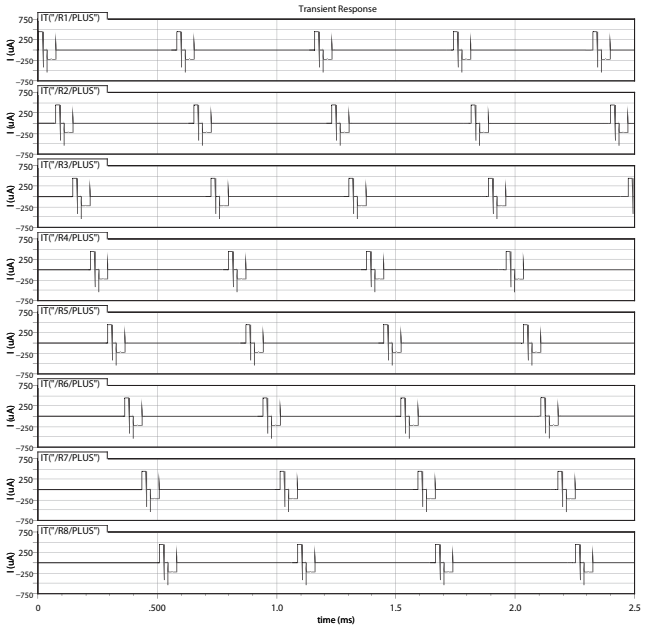

Fig. 4. Transient analysis of the system output for a uniform input, illustrating the 8-channel CIS biphasic current waveform (into a 1kΩ load)

IV. Discussion

A design prototype of a generic AER-based Neural Link, implemented in CMOS technology has been presented, target specifications summarised in Table I. This is the first system reported to encode and communicate multi-channel chemically sensed signals via an address event bus to an artificial electrical stimulator. The fabricated device includes the complete transceiver architecture on a $3mm^2$ die. The system layout and floorplan are shown in Fig. 6.

The novelty of implementing the neural link in this manner is the versatility, i.e. programmability of the structure. By simply intercepting the address event bus, either hard-wired or wirelessly, any form of processing can be implemented using pulse stream arithmetic [15]. For example, non-linear relationships between chemical input and artificial stimulus magnitude can be easily implemented, extending the applicability of this neural link to more realistic neural algorithms. If implemented in hardware, such algorithms would typically increase chip area, power consumption and thus compromise the implantability of sensing systems as described in this paper. Being able to wirelessly implement these algorithms using event-interception-processing overcomes such limitations.

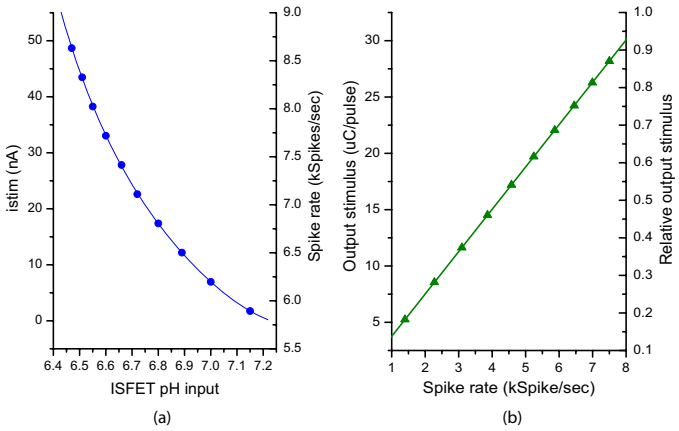

Fig. 5. System simulations of the entire front- and back-end sub-systems. Shown are: (a) pH to spike-rate dynamics and (b) spike-rate to stimulation charge characteristics

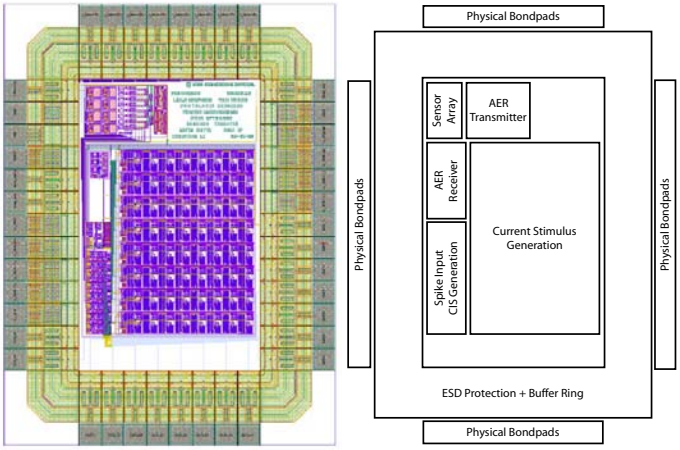

Fig. 6. Designed system layout and corresponding floorplan of the neural link. Chemical sensor and stimulation microelectrode arrays are implemented off-chip.

TABLE I
TARGET SYSTEM SPECIFICATIONS

Technology	AMS 0.35μm (C35B4C3) CMOS
Supply voltage	3.3V
Die size	1.5mm x 2mm
System device count	2490 (transmitter), 4106 (receiver)
AER dynamic range	48dB
AER bandwidth	10Mspikes/sec
K^+ sense range	pK 1 to pK 9
Max. firing frequency	8.9kHz (@50nA, tunable)
Power: I&F Neuron	4.07μW per channel (Ibias=10nA)
Power: AER transmitter	355μW (Iaer=50μA)
Power: AER receiver	180μW

Furthermore, the use of address-event encoding is ideally suited for sparse data sets. As this system has a maximum theoretical throughput of 2.05Mspikes/sec (i.e. CIS-rate $\times$ 8-channels $\times$ 2$\hat{8}$-bits) and the AER bus bandwidth (for the given bias) is 10Mspikes/sec, any temporal skew in data transmission is negligible.

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