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Design of Resonant Converters for High Frequency Wireless Power Transfer Applications

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Declarations

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Abstract

High frequency inductive wireless power transfer is a promising solution that can enable the true potential of many technological applications. The Class EF and Class Φ inverters have properties that make them ideal candidates for primary coil drivers, but designing such circuits with accuracy is difficult using traditional first order methods due to their complexity. A generalised design method is proposed in this work, that can be applied to any Class E type inverter, and includes non-linear and parasitic effects that become prevalent at high frequency operation. A 13.56 MHz 50 W Class EF₂ inverter is developed using this method with 97 % efficiency, and no additional manual re-tuning, whilst maintaining all of the other design requirements. In addition, several circuit configurations are introduced to enable high power operation using GaN technology, including a single common choke push-pull Class DE topology. A demonstration of a 3.39 MHz 3 kW DC/DC inductive power system with 95 % efficiency, using a parallel push-pull Class E inverter, is shown to confirm the theoretical findings. Furthermore, the typical one-to-one wireless link design is generalised to a one-to-many resonant system through a custom iterative method, which expands the application space of inductive power transfer systems. Then, an implicit method for characterising links at high frequency where measurement instruments fail to produce accurate results is proposed and demonstrated through experiments, by using resonant converters. The limitations of Class E type inverter operation at fixed loads are investigated and overcome by introducing various potential active control schemes, which can even absorb the negative effects of reactive reflections to the primary while maintaining output regulation. Finally, an analytic design method for Class Φ resonant gate drivers is presented and a detailed performance comparison with an equivalent half-bridge driver is conducted, where the resonant gate driver despite the slightly lower efficiency displays better switching characteristics.

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List of Abbreviations

AC Alternating Current

DC Direct Current

EM Electromagnetic

EMI Electromagnetic Interference

EV Electric Vehicle

FEM Finite Element Method

FO First Order

GaN Gallium Nitride

GND Ground

HEMT High Electron Mobility Transistor

HF High Frequency

IGBT Insulated Gate Bipolar Transistor

IMS Insulated Metal Substrate

IPT Inductive Power Transfer

ISM Industrial, Scientific and Medical

KCL Kirchhoff's Current Law

KVL Kirchhoff's Voltage Law

MAE Mean Absolute Error

MIMO Multiple-Input Multiple-Output

MOSFET Metal Oxide Semiconductor Field Effect Transistor

MSE Mean Squared Error

PA Power Amplifier

PC Phase Controlled

PCB Printed Circuit Board

PFC Power Factor Correction

PP Push-Pull

PPCC Push-pull Common Choke

PWM Pulse Width Modulation

RF Radio Frequency

RFC Radio Frequency Choke

RK Runge-Kutta

RMS Root Mean Square

RMSE Root Mean Squared Error

Rx Receiver

SE Single Ended

Si Silicon

SiC Silicon Carbide

SRF Self Resonance Frequency

SS State Space

THD Total Harmonic Distortion

Tx Transmitter

VNA Vector Network Analyser

WBG Wide Bandgap

WPT Wireless Power Transfer

ZVDS Zero Voltage Derivative Switching

ZVS Zero Voltage Switching

List of Symbols

Φ	Magnetic flux
$\vec{B}$	Magnetic field density
$\vec{E}$	Electric field
$\vec{F}$	Lorentz force
q	Electric charge
$\mathcal{E}$	Electromotive force
$\vec{r}$	Position vector
t	Time
μ	Permeability
π	Ratio of a circle's circumference to its diameter
L	Self inductance
M	Mutual inductance
k	Coupling factor
Q	Quality factor
C	Capacitance
I	Constant current
V	Constant voltage
i	Time varying current
v	Time varying voltage
S	Surface area
$\vec{s}$	Surface area vector
$\vec{l}$	Loop vector
$\vec{v}$	Velocity
$\vec{r}$	Distance vector

f	Frequency
R	Resistance
$\overline{Z}$	Complex impedance
ω	Angular frequency
$\mathbb{R}$	Set of real numbers
η	Efficiency
X	Reactance
i	Imaginary unit
θ	Angle
D	Duty Cycle
P	Power
c	Speed of light in vacuum
T	Temperature
e	Euler's number

Preface

There are five main technical chapters in this thesis and seven chapters in total, organised as follows:

- **Chapter 1** is a brief, general introduction to inductive wireless power transfer systems.
- The main core of this work is presented in **chapter 2**, where a design process for Class EF and Class Φ inverters is proposed.
- **Chapter 3** investigates the potential of operating high frequency inductive power transfer systems at high power and several candidate solutions are introduced.
- A link design method for inductive power transfer systems with a single transmitter to many receivers is proposed in **chapter 4**. In addition, an implicit inductive link estimation method based on converter measurements is introduced.
- Potential solutions for real time adjustments of Class E type inverters to load variations are given in **chapter 5**.
- **Chapter 6** contains an analytic design method for Class Φ resonant gate drivers.
- **Chapter 7** concludes the thesis.

Chapter 1

Introduction

1.1 Wireless Power Transfer Techniques and Applications

As technology advances, a rising number of applications in various fields are revealed where wireless transmission of power can either enhance their capabilities and performance, or is even essential for their core function. An indicative example where Wireless Power Transfer (WPT) is beneficial compared to current solutions is in recharging biomedical implants, where we can substantially decrease the size of the battery required to be implanted, increase its lifespan, and reduce the number of consecutive surgeries needed for battery replacement [2, 3]. As we make improvements in miniaturisation and robustness of WPT systems and the transfer efficiency becomes comparable to traditional connectors, WPT systems are strong candidates for replacing connections that are sensitive to exposure to environmental elements (humidity, dust, etc.) [4]. Furthermore, WPT can increase the autonomy of systems, for example by dynamically charging vehicles while they are on the move and thus reducing their battery sizes and minimising the amount of time needed for stationary charging [5]. Space based solar power, which is the concept of capturing solar power in outer space and delivering it to the earth through microwaves, is also a highly popular research topic with large interest lately [6, 7].

Historically, even though Faraday and Maxwell had already worked on the fundamental physical concepts enabling WPT, it was Tesla who first experimented with transmitting power over a distance [8]. Since then, and especially after World War II, research on several types of WPT has been conducted, initially focused more on far field technologies, but with near field catching

up later on, too [9]. The latest advances in Wide Band Gap WBG devices in recent years have accelerated even further the interest and effort put into developing WPT systems for real-world applications [10].

Electromagnetic field power transfer can be split into two subcategories: near field (coupled) and far field (uncoupled) WPT [11]. Near field WPT is based on electromagnetic induction and is used for distances from mm to m, whereas far field transmits energy using radiation and can transfer power even across km. Far field WPT can be further distinguished between Radio Frequency (RF) and microwave, operating at MHz to GHz, and optical (laser) power transmission, at THz frequencies. Near field WPT can be achieved either with the electric field (capacitive) or with magnetic field (inductive), and operating frequencies typically range from low kHz to low MHz.

Radiative systems can inherently achieve power transfer over longer range compared to closed coupled ones, but their efficiency is poorer [7]. The efficiency and range of strongly coupled systems can be further improved by utilising resonance at the operating frequency [12]. Also, closed coupled systems are generally safer compared to far field technology [11, 13]. Radiative WPT systems can effectively deliver up to MW of power, whereas near field have so far achieved efficient transfer of up to tens of kW [14].

Due to the directional nature of the electric field, the negative effects of the stray fields in capacitive WPT are less disruptive compared to Inductive Power Transfer (IPT). However, capacitive systems are inherently operating at extremely low coupling for useful applications, which requires very high frequency and high voltage to achieve high transfer efficiency. In order to reach the high magnitude of electric field required, multiple stages of impedance transformation networks are used, which increase the losses and the size of the primary driver circuitry.

Regarding WPT systems using magnetic coupling, there are two main approaches when it comes to operating frequency. The most popular approach is using kHz frequencies, such as the Qi standard which is widely used in low power consumer electronics, or the SAEJ2954 standard (85 kHz) for electric vehicle charging [15]. The design of the power electronics in these kHz frequencies is relatively conventional and based on proven and well-established half-bridge topologies. However, the magnetic link is bulky and requires a lot of copper and ferrite for efficient power transmission.

On the other hand, the alternative approach uses low MHz frequencies for the link, such as the Airfuel Alliance (6.78 MHz). Operating at high frequency has the potential of significantly reducing the size and cost of the magnetic link, while still maintaining high quality factors [16]. In addition, high frequency enable the operation of the link at low couplings without the need of ferrite materials. However, switching losses increase with frequency, which makes the design of the converters a challenging task for high frequency high power applications [17]. In order to fully benefit from the advantages that high frequency IPT offers, we need to accurately design appropriate resonant soft-switching converters to enable efficient operation and be able to precisely integrate them into the magnetic link, which is the main topic of this thesis.

1.2 Electromagnetic Theory of Induction

The magnetic flux Φ at time t caused by a magnetic flux density $\vec{B}$ through a surface area S is defined by the relation

$$\Phi(t) := \int_{S(t)} \vec{B}(\vec{r}, t) \cdot d\vec{s}, \quad (1.1)$$

where $\vec{r}$ is the position vector and $d\vec{s}$ is the infinitesimal surface area vector. Consequently, the rate of change of Φ through a moving loop area S is

$$\frac{d\Phi}{dt} = \frac{d}{dt} \int_{S(t)} \vec{B}(\vec{r}, t) \cdot d\vec{s}. \quad (1.2)$$

The Maxwell-Faraday equation describes the interaction between a varying magnetic and electric field $\vec{E}$ and its integral form is given by [18]

$$\oint_{\partial S(t)} \vec{E}(\vec{r}, t) \cdot d\vec{l} = - \int_{S(t)} \frac{\partial \vec{B}}{\partial t} \cdot d\vec{s}, \quad (1.3)$$

where ∂S is the boundary of S and $d\vec{l}$ is a segment of that loop. In the special case of ∂S being a conductive loop as shown in Figure 1.1, the right-hand side of (1.2) combined with (1.3) in the macroscopic view produces

$$\frac{d}{dt} \int_{S(t)} \vec{B}(\vec{r}, t) \cdot d\vec{s} = - \oint_{\partial S(t)} \left[\vec{E}(\vec{r}, t) + (\vec{v}(t) \times \vec{B}(\vec{r}, t)) \right] \cdot d\vec{l}, \quad (1.4)$$

where $\vec{v}$ is the velocity of $d\vec{l}$.

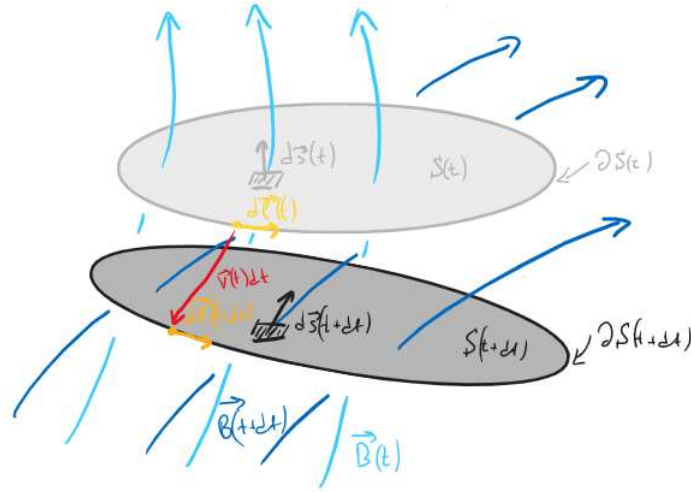


Figure 1.1: A varying conductive loop ∂S in the presence of a changing magnetic field $\vec{B}$ resulting in a time changing magnetic flux $d\Phi/dt$.

The Lorentz force $\vec{F}$ is defined by an empirical axiom that describes the combined forces to a test charge q due to the presence of electromagnetic fields [18] and its differential form is

$$d\vec{F} := \left[\vec{E}(\vec{r}, t) + \left(\vec{v}(t) \times \vec{B}(\vec{r}, t) \right) \right] dq. \quad (1.5)$$

The electromotive force $\mathcal{E}$ is defined by the line integral of $\vec{F}$ per unit charge [18]:

$$\mathcal{E}(t) := \oint_{\partial S(t)} \frac{d\vec{F}}{dq} \cdot d\vec{l}. \quad (1.6)$$

The differential form of Faraday's law occurs by combining all of the above:

$$\mathcal{E}(t) = -\frac{d\Phi}{dt}, \quad (1.7)$$

and it states that a changing magnetic flux through a closed conductive path induces an $\mathcal{E}$ in that loop.

According to the Biot-Savart law, a constant current line I along ∂S produces constant a magnetic field at $\vec{r}$ [18]:

$$\vec{B}(\vec{r}, t) = I(t) \frac{\mu_0}{4\pi} \int_{\partial S(t)} \frac{d\vec{l} \times \hat{\vec{r}}(\vec{r}, t)}{|\vec{r}(\vec{r}, t)|^2}, \quad (1.8)$$

where μ_0 is the permeability of free space and $\vec{r}$ is the vector from $d\vec{l}$ to $\vec{r}$. Since $\vec{B}$ in (1.8) is

proportional to I so is the Φ generated by it, and by using (1.1) we get:

$$L := \frac{\Phi(t)}{I(t)}, \quad (1.9)$$

where the proportionality factor L is the self-inductance of ∂S and it is a geometry depended quantity.

If I is varying quasi-statically so that (1.8) still applies, we get the relation of the voltage across an inductor with the current through it, by combining (1.7) with (1.9):

$$\mathcal{E}(t) = -L \frac{dI}{dt}, \quad (1.10)$$

which means that a varying current through a loop induces an $\mathcal{E}$ in itself.

According to (1.8), the magnetic field in Figure 1.1 can be generated by a current around another loop in vicinity, as shown in Figure 1.2. In such configuration, the flux through S_2 is

$$\Phi_2(t) = \int_{S_2} \vec{B}_1(\vec{r}, t) \cdot d\vec{s}_2 = M I_1(t), \quad (1.11)$$

where the proportionality constant M is the mutual inductance of the two loops. Using Stoke's theorem on the configuration of Figure 1.2, M is given by the general formula [18]

$$M = \frac{\mu_0}{4\pi} \oint_{\partial S_1} \oint_{\partial S_2} \frac{d\vec{l}_1 \cdot d\vec{l}_2}{|\vec{r}|}, \quad (1.12)$$

where $\vec{r}$ is the distance between $d\vec{l}_1$ and $d\vec{l}_2$. Based on (1.12), the value of M is independent of which of the two coils carries the current and it is a purely geometrical quantity.

If I_1 is changing with t , it causes a changing magnetic flux through ∂S_2 according to (1.11), which in turn produces an $\mathcal{E}$, as shown in (1.7):

$$\mathcal{E}_2(t) = -M \frac{dI_1}{dt}. \quad (1.13)$$

Since ∂S_2 is conductive in Figure 1.2, a current I_2 flows through it because of the induced $\mathcal{E}_2$, which in turn produces a $\vec{B}_2$ based on (1.8). This effect will result in an induced $\mathcal{E}_1$ in ∂S_1

$$\mathcal{E}_1(t) = -M \frac{dI_2}{dt}. \quad (1.14)$$

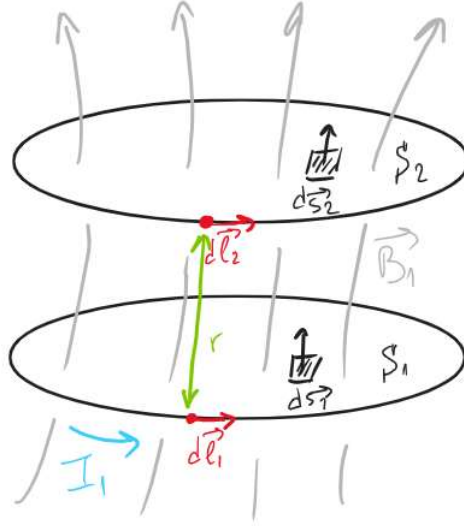


Figure 1.2: The current I_1 around the loop ∂S_1 generates the magnetic field $\vec{B}_1$, resulting in the magnetic flux Φ_2 through the area S_2 .

The total effect of I_1 on both ∂S_1 and ∂S_2 is derived from the combination of (1.10) on each loop individually with (1.13) and (1.14). Substituting the arbitrary conductive loops in Figure 1.2 with the coupled coils in Figure 1.3, the relation of the voltages across the coils with the currents through them is described by the following system of equations:

$$\begin{cases} v_1(t) = L_1 \frac{di_1}{dt} + M \frac{di_2}{dt} \\ v_2(t) = L_2 \frac{di_2}{dt} + M \frac{di_1}{dt} \end{cases} \quad (1.15)$$

The coupling factor k in Figure 1.3 is a description of the part of the magnetic flux produced by L_1 that flows through L_2 and is defined by [19]

$$k := \frac{M}{\sqrt{L_1 L_2}}. \quad (1.16)$$

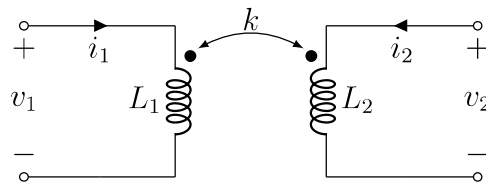


Figure 1.3: Circuit diagram of two mutually coupled inductors.

1.3 Inductive Power Transfer System Fundamentals Overview

A high level overview of a conventional IPT system, from alternating current (AC) mains to the remote load being charged, is shown in Figure 1.4 [20]. The mains rectifier (typically a full bridge) as well as the DC/DC (direct current) converters in both the transmitter (Tx) and receiver (Rx) sides are independent of the IPT operation of the system and are not discussed in detail in this work. The primary side DC/DC converter usually includes an active power factor correction (PFC) function and provides the required DC input voltage for the primary coil driver. The secondary side DC/DC converter adjusts the voltage to the specifications of the load and can also act as a voltage regulator. However, the power regulation can also be performed through special high frequency (HF) rectifier topologies [21], and thus the extra DC/DC conversion stage in the Rx may be omitted in some cases.

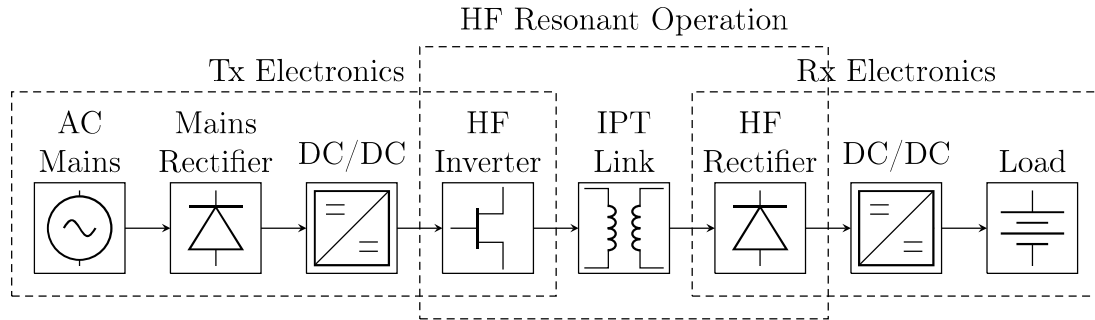


Figure 1.4: High level block diagram of the various power conversion stages in a typical IPT system.

Along with the coupled coils, the parts of the circuitry in Figure 1.4 that perform the WPT operation are the inverter, which acts as the driver of the primary coil, and the HF rectifier, that turns the HF signal of the secondary back to DC, so that it has a usable form for the subsequent receiver electronics [5]. Typically, the two coupled coils are part of respective resonant tanks, to achieve higher power throughput especially at low coupling instances [17]. In addition, as the frequency of the inductive link rises and the switching losses of the devices become a limiting factor, the preferred inverter and rectifier topologies of the IPT link are also resonant converters [22]. Depending on the application, an impedance matching network may be needed between the resonant tank and the HF converters for optimal compatibility [23].

Each of the resonant tanks of the coupled coils can be connected either in series or in parallel with the corresponding coils [24]. The most widely used inverter circuits for WPT are usually series tuned, since they are voltage driven, whereas the type of the secondary resonance depends

on the equivalent input AC resistance of the HF rectifier; with parallel tuning used for high resistance and series tuning for low [19]. Using first order (FO) approximation the output of the inverter can be modelled as an AC source at the driver frequency. A non-resonant rectifier can be approximated with just an equivalent input AC resistor. A resonant rectifier is modelled as a complex impedance at the IPT link resonance frequency, which consist of a combination of capacitance or inductance and resistance, series connected for current driven topologies and parallel connected for the voltage driven counterparts [25].

An AC approximation of a series-series resonant link is shown in Figure 1.5 along with the equivalent circuit reflected to the primary side. The inverter is modelled as the sinusoidal voltage source v_{s1} , $C_{s1,2}$ and $L_{s1,2}$ are the primary and secondary series tuning capacitors and coils accordingly, k is the coupling coefficient, R_{ac} is the equivalent input AC resistance of the rectifier, and $\bar{Z}_{eq}$ is the secondary impedance reflected to the primary side. The series resistances $R_{s1,2}$ represent the quality factors (Q) of the coils at the primary driver output frequency f_s . C_{s2} also includes the effect of any potential residual reactance of the rectifier.

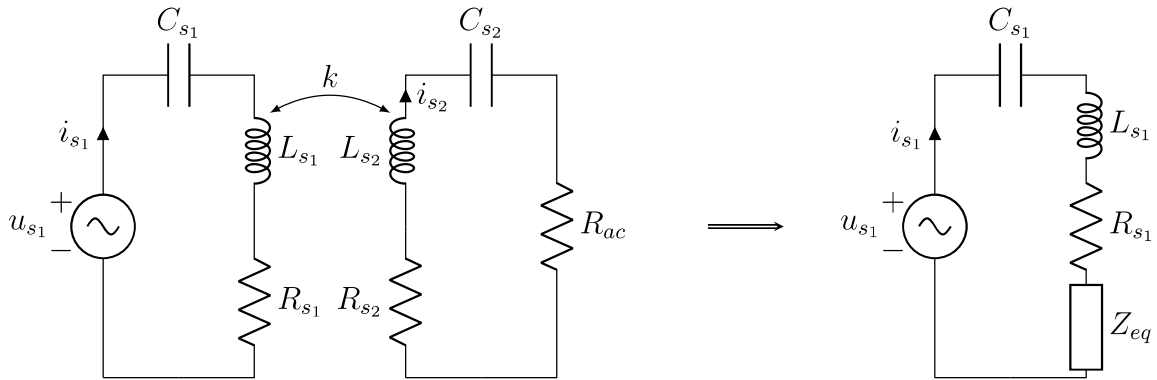


Figure 1.5: FO AC model of the HF converters of the IPT link (left) and the equivalent primary side circuit with the reflected secondary impedance (right).

The total link efficiency in Fig.1.5 is defined as the product

$$\eta_s := \eta_{s1} \eta_{s2}, \quad (1.17)$$

where η_{s1} is the primary link efficiency

$$\eta_{s1} = \frac{R_{eq}}{R_{eq} + R_{s1}}, \quad (1.18)$$

η_{s_2} is the secondary link efficiency

$$\eta_{s_2} = \frac{R_{ac}}{R_{ac} + R_{s_2}}. \quad (1.19)$$

The only degree of freedom for maximising link efficiency, for given AC load, coupling, frequency and coil Q factors is through the reflected resistance $R_{eq} \equiv \text{Re}(\bar{Z}_{eq})$ [19]:

$$\bar{Z}_{eq} = \frac{k^2 X_{L_{s_1}} X_{L_{s_2}} [(R_{ac} + R_{s_2}) + i(-X_{C_{s_2}} - X_{L_{s_2}})]}{(R_{ac} + R_{s_2})^2 + (-X_{C_{s_2}} - X_{L_{s_2}})^2}, \quad (1.20)$$

where

$$X_{L_{s_{1,2}}} := \omega L_{s_{1,2}}, \quad (1.21)$$

$$X_{C_{s_2}} := -\frac{1}{\omega C_{s_2}}, \quad (1.22)$$

and ω is the angular frequency

$$\omega := 2\pi f. \quad (1.23)$$

Maximising (1.20) naturally leads to secondary resonance at f_s , i.e.

$$\eta_s(C_{s_2}) = \max \Rightarrow \omega_s = \frac{1}{\sqrt{L_{s_2} C_{s_2}}}. \quad (1.24)$$

In the case that the secondary is designed to be resonant at the frequency of v_{s_1} , the equivalent reflected impedance is [19]

$$\bar{Z}_{eq}|_{f=f_s} = R_{eq}|_{f=f_s} = \frac{(\omega_s k)^2 L_{s_1} L_{s_2}}{R_{s_2} + R_{ac}}. \quad (1.25)$$

The first observation than can be made from (1.25) is that $\bar{Z}_{eq} \in \mathbb{R}$ at f_s , regardless of changes in k and R_{ac} . This is important for stable inverter operation, especially the Class E type ones [26], since in a real WPT systems both the coupling and the load are not fixed constants. Another noteworthy property of (1.25) is that $R_{eq} \propto f_s^2$. Subsequently, by combining (1.25) with (1.18) we conclude that higher operating frequency leads to higher link efficiencies. Although, in reality the above statement only holds true for a specific limited bandwidth depending on the geometry of L_{s_1} , as the coil Q factor is also frequency dependent [27], it still applies for IPT systems as they generally operate in a narrow bandwidth [19].

1.4 Inverter Topologies

As explained in section 1.3, for efficient operation of WPT systems the primary coil needs to be driven with a HF AC current. This HF signal is provided by a power amplifier, which is a DC/AC inverter [19].

A generic block diagram of a single ended (SE) power amplifier (PA), adjusted for IPT applications, is given in Figure 1.6. A DC power supply feeds the block with the power transistors through an input filter. The output of the transistors can be shaped through a series of resonant filters before it reaches the Tx coil. Many times, the transistors are paired with shunt capacitors for ZVS operation [28]. Depending on the total required output reactance that the inverter needs to drive, the coil inductance is usually countered with either a series or parallel capacitor. For IPT applications specifically, series tuned output tanks are preferred since the series load can be naturally modelled in the case of coupled inductors, as shown in Figure 1.5. When both series and parallel tuning capacitors are used, the inverter is at semi-resonant operation which effectively results in an output equivalent impedance increase [29]. Impedance matching networks can also be used before the output stage of the inverter.

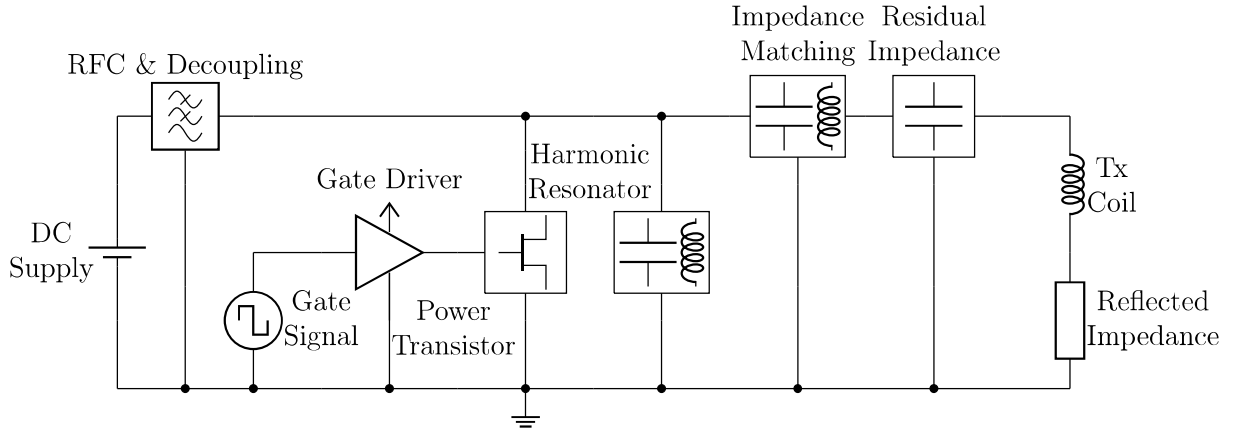


Figure 1.6: Circuit diagram showcasing some of the potential operating blocks of a single ended inverter.

PA's that use the device in the linear region, i.e. Class A, Class B and their derivatives, are suboptimal for IPT applications because they exhibit low ideal drain efficiencies ($50\% \leq \eta_{DS} < 80\%$) [28]. Class F power amplifiers also have losses with an ideal drain model [28]. Class C amplifiers at saturating mode can have 100% drain efficiency, but are unsuitable for IPT applications because of their sensitivity to coupling variations [19]. A more thorough theoretical

examination of the relation between the various types of PA's through drain waveform harmonic content can be found in [30].

Instead, the primary coil drivers are typically not linear inverters, where the device acts like a switch and the gate is driven with pulses, effectively transforming the energy from the DC power supply into a HF signal, which enables high efficiency performance [19]. Depending on their architecture and principle of operation they are usually either Class D type, or Class E type inverters.

In addition, these topologies are also frequently used in a differential or Push-Pull (PP) configuration for improved output Total Harmonic Distortion (THD), increased output power for given device stresses, and reduced demands in input filtering [31]. A PP inverter consists of two individual identical SE inverters with a common supply, shared output network, and driven with 180° phase difference, as shown in Figure 1.7.

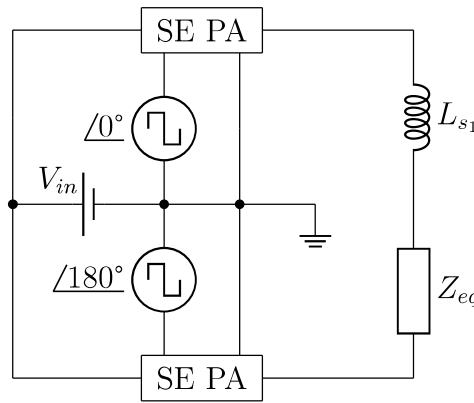


Figure 1.7: PP inverter configuration for IPT applications consisting of two identical generic SE inverters.

1.4.1 Class E Type Inverters

The Class E type inverter uses the drain voltage of a low side switch, filtered through the resonant output tank, to drive the Tx coil with a sinusoidal current at the switching frequency [32]. As shown in Figure 1.8, the supply current is filtered through the input choke inductor (L_{rfc}) before reaching the switching network. There, the shunt capacitor (C_p) along with the duty cycle and the residual impedance of the output tank, provide the conditions necessary for ZVS and ZVDS operation.

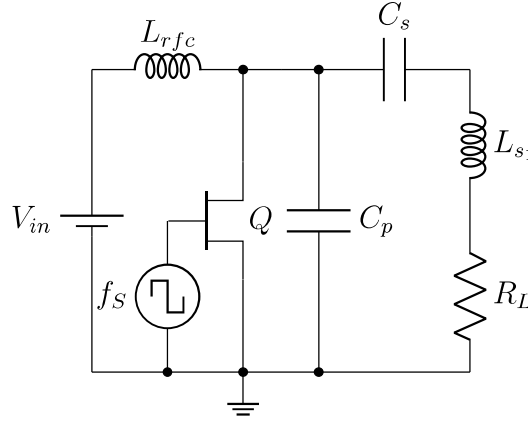


Figure 1.8: Generic circuit diagram of a SE Class E ZVS inverter.

Depending on the inductance value of the L_{rfc} , the Class E inverters are split into infinite and finite choke topologies [33]. High (infinite) input inductance has the advantage of low input current ripple which results in minimal input filtering requirements and simple supply circuits. However, when the impedance of the input choke is comparable to the rest the resonant components, this provides another degree of freedom, which in turn gives more design capabilities. One of the advantages of introducing a finite choke is load independence [34], which means having a constant output current across a large range of reflected resistive loads to the primary side while at the same time maintaining ZVS.

Class E inverters exhibit high efficiency operation and can operate at high frequencies, depending on the output capacitance of the transistor, however in the expense of high device voltage stresses ($v_{DS}^{\max} > 3 \times V_{in}$) for a given output power level. This drawback can be improved by adding additional resonant branches parallel to the switching network, as shown in Figure 1.9. Again, depending on the impedance value of the input choke, these circuits are called Class EF (infinite choke) or Class Φ (finite choke), and the voltage stresses in these ones are significantly reduced ($v_{DS}^{\max} \sim 2 \times V_{in}$) [35]. In addition, Class EF/ Φ inverters provide further degrees of freedom during the design process due to their higher complexity, e.g. load independence with infinite choke [1], but practical circuit tuning at high frequencies becomes a more complicated task.

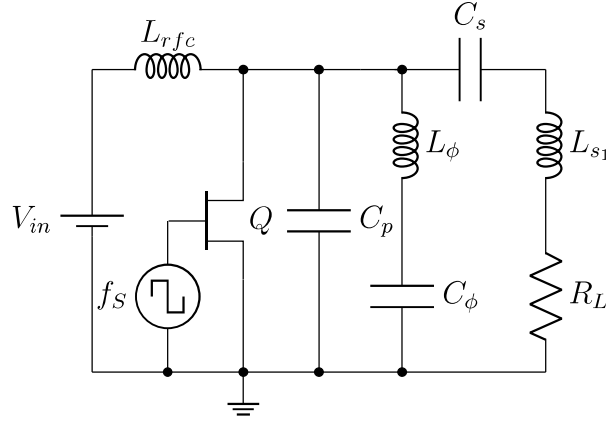


Figure 1.9: Generic circuit diagram of a SE Class EF/ Φ ZVS inverter.

1.4.2 Class D Type Inverters

Another popular topology for primary coil drivers in WPT applications is the Class D inverter and the circuit diagram of the half bridge instance of it is shown in Figure 1.10 [36]. At optimal operation, the high and low side transistors are driven with a 50 % duty cycle signal at the output tank resonance frequency, at 180° phase difference. The fundamental component of the square drain voltage of the low side transistor is filtered through the output tank to provide the sinusoidal current for the primary coil.

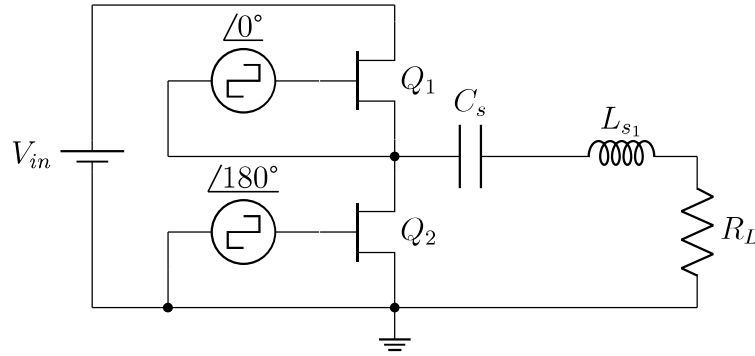


Figure 1.10: Generic circuit diagram of a half-bridge Class D series resonant inverter.

Contrary to the Class E type counterparts which operate at a fixed frequency, the output power of the Class D inverter can be modulated by varying the switching frequency, without causing significant changes in efficiency [36]. It must be noted that the Class D primary coil driver is not a pulse width modulation (PWM) converter, and the duty cycle is kept fixed to achieve a sinusoidal output current. Also the Class D topology is inherently more immune to reactive load changes, whereas the Class E inverters lose ZVS and efficiency drops rapidly under non ideal reflected load conditions [19]. Also, because of the hard switching square shape of the

u_{DS} , the device voltage stresses are equal to the supply voltage.

However, abrupt voltage transitions during hard switching on real devices with parasitic capacitances and lead inductances result in ringing and overall switching losses. In addition, as the switching interval becomes non trivial, a dead time between the signals of the two transistors is required to avoid shorting the switching node directly to ground. Also, the internal output capacitance of the transistors practically limits the upper frequency limit of operation of such inverters. Another drawback is the need for high side gate driver circuit, which can be a challenging task especially at high power, high frequency applications. Finally, the supply current is effectively the high side switching current, which creates the need for additional supply decoupling and filtering.

The frequency limitation of the Class D inverter can be overcome by combining it with the Class E operation, resulting in reduced switching losses. This is realised by introducing a shunt capacitor across the transistors, which also absorbs the effect of the output capacitance of the device, and operating at duty cycle below 50 %, resulting in the Class DE inverter in Figure 1.11. In this operation, a substantial dead time between switching the devices is introduced, carefully timed along with the shunt capacitance and the residual output impedance, so that ZVS and even ZVDS conditions are achieved. This topology combines the low device voltage stresses of the Class D along with the soft switching advantages of the Class E. It also manages to minimise the effect of the non-linearity of the output capacitances of the transistors. However, it loses the frequency modulation and load independence characteristics of the Class D circuit. The maximum theoretical switching frequency of the Class DE for a given duty cycle inverter is when the required shunt capacitance equals the effective output capacitance of the transistors.

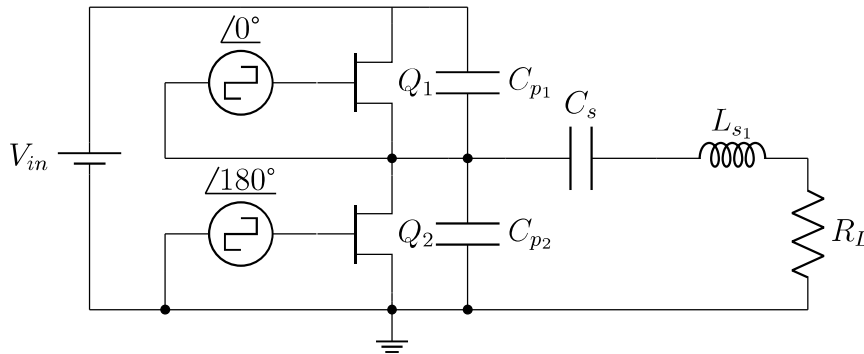


Figure 1.11: Generic circuit diagram of a half-bridge Class DE ZVS inverter.

Chapter 2

Class EF/ Φ Inverter Design

2.1 Introduction

Transmitting power using HF induction offers numerous benefits for WPT systems as the link can be realised with miniaturised and lightweight air core coils with high Q that can transmit power efficiently over low coupling [37, 38, 27]. Advances in WBG devices make the realisation of HF IPT systems operating at MHz frequency range more feasible, where the Class E type single switch resonant converter circuits demonstrate benefits over the Class D type drivers [17, 19, 39].

The properties of the basic Class E inverter can be enriched and the design possibilities can be expanded by adding resonant networks in parallel and in series with the series load network [33, 40, 41, 1, 42]. These topologies have been given different names in the literature based on the resonant frequency of the filters and the degree that the input choke is involved to the rest of the resonant circuit of the inverter. In this work we use the term “Class EF_n” when referring to a design with an infinite choke and “Class Φ_n ” when the finite input choke is part of the resonant circuit, where “n” is the ratio of the resonance frequency of the single parallel filter branch (ϕ -branch) over the switching frequency. The two additional degrees of freedom for defining the behaviour of the inverter that the ϕ -branch provides, enable the Class EF/ Φ inverters to achieve better device power capability utilisation by shaping the drain voltage and to decrease THD by filtering the output current, compared to the typical Class E converters. These features expand the design possibilities with more control over the properties

and behaviour of the circuit operation [1]. For example, load independent operation can be achieved with a Class E converter using a finite DC feed inductor [1, 43, 44], but Class EF can do the same with a infinite choke [1], which can be preferable in cases where a low ripple input current is required. Load independent Class Φ_2 operation can be achieved using the design method proposed in [45].

Because of the high number of design variables combined with the low component value tolerances of the Class EF inverter, it is typical that additional manual retuning is required, which is an iterative procedure based on trial and error [1, 46, 47, 48]. This process is not trivial and requires high level of insight and experience [48, 46, 49], especially at high operating frequency and power level. Most importantly though, after such alterations to the original design, it is not guaranteed that the final experimental setup will still remain true to the initial design requirements [26].

The main motivation leading to this work is to eliminate the need of manual retuning of Class EF/ Φ inverters, by developing a robust and reproducible design method, which can be fully automated and produces reliable results with high accuracy. In addition, our method is able to cater for designs based on specification of several different properties of the converter circuit such as, the DC to AC current gain, the slope of the drain voltage at turn on while maintaining ZVS at the specified Φ -branch resonance frequency. Finally, the proposed method is by definition generally applicable and can provide results that are able to satisfy any combination of required operating conditions and circuit properties, as long as such demands do not exceed the physical limitations of the topology itself. The scope of this work is to explain the details of the proposed design algorithm rather than propose specific inverter designs.

Our proposed algorithm provides different levels of precision, depending on the amount of information that is available about the system. Different complexities of models from ideal FO approximations to SS models with a non-linear switching device are used. Furthermore, in order to take full advantage of the design degrees of freedom that the Class EF/ Φ inverter provides, this algorithm regularly ensures during its progression that the required properties of the circuit are maintained until the end, with no external supervision from the user being needed. Such a high level of design precision and control over the design parameters of the inverter is practically impossible to be achieved with traditional manual retuning techniques.

2.2 Background

The circuit diagram of an ideal Class EF/ Φ inverter is shown in Figure. 2.1. In this work we implement the Class EF/ Φ inverter as a primary coil driver in WPT applications. In the diagram of Figure 2.1, L_{s1} is the Tx coil inductance and R_{sL} is the series combination of the primary coil resistance (R_{s1}) with the equivalent resistance of the secondary reflected to the primary (R_L), since the inductive link is running at the primary resonance frequency and there is no reflected reactance as explained in section 1.3. The final component of the series load network is the C_s capacitor. The input RF choke inductance (L_{rfc}) can be either finite (Class Φ) or infinite (Class EF) depending on its value relative to the rest of the energy storing components of the inverter. V_{in} is the DC input supply voltage; C_p is the shunt capacitor to the switching device (S) and L_ϕ in series with C_ϕ form the added resonant ϕ -branch network parallel to the load network, which is absent in the Class E inverter.

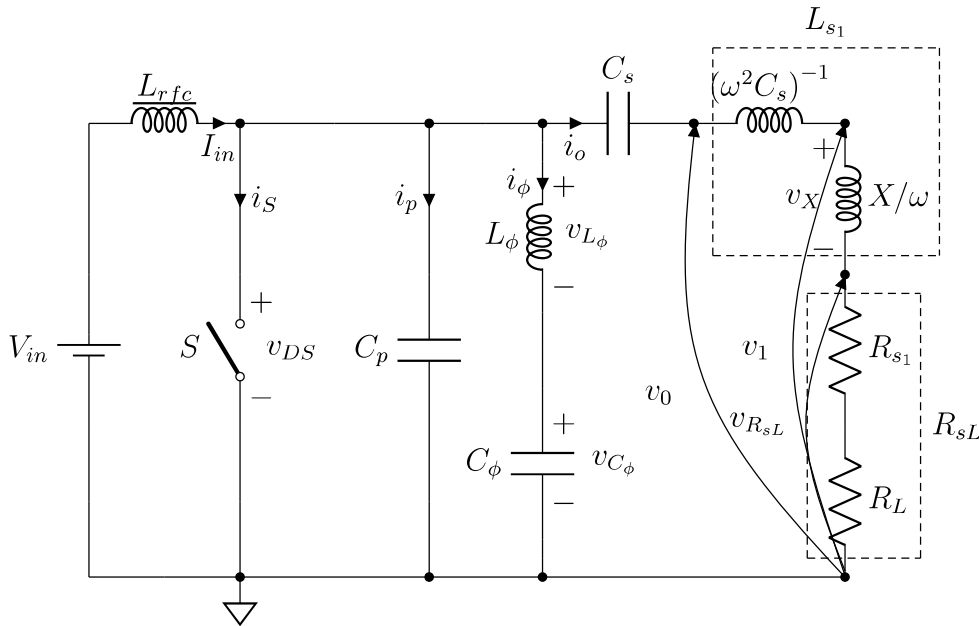


Figure 2.1: Circuit diagram of Class EF/ Φ inverter using the FO formulation.

Various Class E inverter design methods for optimal operation have been thoroughly developed in the literature with ideal FO analytic expressions for both exact [50, 51] and high Q approximations [32, 26, 19] of load network. An alternative approach of deriving design equations based on fitting datasets is presented in [46]. The potential advantages and disadvantages of using a finite choke inductor have also been investigated [52, 53].

Similar design equations based on the FO analysis of the Class E inverter have been derived for the Class EF [35] and the Class Φ [54, 55] inverters. Search optimisation algorithms based on the more accurate linear SS simulation of the circuit have also been used for defining the passive component values of the inverter [56, 40, 57], with the downside that such numerical approaches provide very limited insights and control of the tuning process to the user, do not provide a broad range of design input parameters, are relying on random initial parameters to run and are usually computationally demanding, and provide no guarantee of a practically realisable design output. An extension to traditional first order design methods is proposed in [58] using higher order analysis but some of the design component values need to be set initially, which may be problematic.

The above mentioned theoretical approaches to optimally tune real world circuits with such sensitivity to component variations have always been a practical challenge because of parasitics and non-linearities, whose effect becomes even more prevalent as frequency and power levels increase. This issue is typically resolved by performing additional manual retuning [49, 47], even though efforts to compensate for the output capacitance of the device during the design procedure have been made both for the Class E [59] and the Class Φ [60]. The manual retuning steps are usually based on empirical observation and provide more qualitative instead of quantitative and precise guidelines [26, 46, 1] and tend to require multiple repetitive incremental adjustments based on trial and error. An attempt to develop an automated design method for Class EF inverters in WPT applications that aims to minimise the requirement for manual retuning by incorporating the output capacitance of the switching device using a combination of FO and SS formulations is presented in our previous work in [61], but only an outline of the proposed tuning method is provided with a very brief description and the theoretical results are not supported with experimental measurements.

2.3 Overview

The inverter design process flow chart is illustrated in Figure 2.2. It consists of four main, interdependent steps executed in sequence, which are further explained in the corresponding sections. Depending on the desired accuracy of simulation to experimental matching requirements, the tuning process can be terminated at the end of any of the specified steps of the

procedure.

The first step of the design algorithm (section 2.4) is based on FO analysis of the circuit. It is the least accurate part of the proposed tuning process. However, it is the only one that uses analytic expressions, and its main contribution is that it provides a good starting point for the iterative methods that follow, ensuring speed and convergence. Typically, the component values that this part of the design algorithm produces are not very accurate, mainly due to its inherent simplification, as explained in subsection 2.4.2. The accuracy of the outputs can be evaluated by an LTspice simulation, which will determine whether the subsequent steps of the algorithm need to be applied.

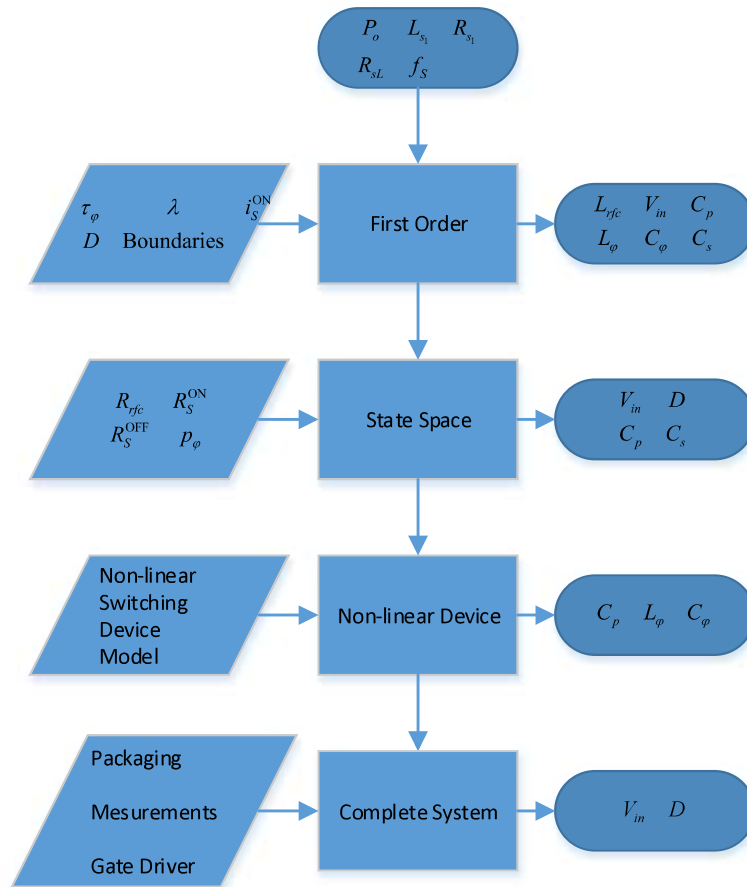


Figure 2.2: Class EF/ Φ inverter design flowchart diagram.

The second tuning part, analysed in section 2.5, is based on SS representation of the circuit and resolves any approximation and simplification errors caused by the first part. The accuracy of the outcome of this algorithm step should be practically enough when the switching frequency is low enough so that the shunt capacitor value (circuit diagram details given in subsection

2.4.2) is substantially higher than the effective output capacitance of the device (for a given power level). This is due to the fact that the values of the energy storing components are related to the operating frequency. Usually, when this is the case, the effect of the rest of the parasitic capacitances of the device along with the stray package inductances and gate driver imperfections are negligible, too. If any of the two first steps of the algorithm fail to converge or produce a realistic result, it is an indication that the operation requirements cannot be met with the given input conditions.

The third part introduces a more representative non-linear model of the switching device and compensates for the changes caused by the parasitics of the device, and is discussed in section 2.6. Proceeding to this part of the algorithm is required at higher switching frequencies, as the theoretical speed threshold of the converter is approached. If this part doesn't converge, it means that the parasitics of the transistor of choice cannot be absorbed in the circuit.

The fourth part includes effects caused by the unavoidable mismatch between the theoretical optimal component values and their actual experimental measurements and is given in section 2.7. This stage is essential when this mismatch becomes substantial, mostly due to limitations of off the shelf passive component values. The last two parts also include the effects of the packaging of the device and gate drive signal shaping resistances. Convergence failure during the last part of our algorithm shows that the circuit design cannot be realised with preferred values.

The description of the experimental setup and circuit examples used for the verification of the performance of our proposed method are given in section 2.8. Measurements are taken across a variety of operating conditions and the evaluation of the accuracy and contribution of each tuning step is performed.

2.4 First Order Approximation

2.4.1 Background

The first section of the proposed tuning algorithm uses a FO approximation. The derivation of the design equations and the corresponding assumptions they are based on have been extensively

described in [19, 32, 26, 36, 28] for infinite choke Class E, in [52, 53] for the finite choke Class E, in [33, 54, 55] for the Class Φ , and in [35, 1] for the Class EF inverter. Second order approximations for the simulation of Class E inverters have been applied in [62]. In this work we formulate the problem using a combination of the analytic methods mentioned above in a way that provides both control and insight to the user about the tuning of the resulting circuit. This part of the design algorithm is the only one that is based on analytical synthesis; the rest use iterative optimisation. As stated previously, the design algorithm uses the FO approach as an initial point for the iterative procedures that follow in the next steps, for faster and more controlled convergence.

2.4.2 Design and Simulation Equations

Switching Network

Since S in Figure 2.1 is modelled as an ideal switch, there is no voltage drop across it when turned on and no current flows through it during turn-off. Also, the current through C_p during turn-on is considered to be zero. By applying Kirchhoff's Voltage Law (KVL) to the ϕ -branch during the part of the period that the device is on we get:

$$\omega L_\phi \frac{di_\phi(\theta)}{d\theta} + v_{C_\phi}(\theta_{\text{ON}}^+) + \frac{1}{\omega C_\phi} \int_{\theta_{\text{ON}}^+}^{\theta} i_\phi(u) du = 0 \quad (2.1)$$

where i_ϕ is the current through the ϕ -branch, v_{C_ϕ} is the voltage across C_ϕ , $\theta_{\text{ON}}^+ = 0$ is the right-hand side boundary of the turn-on angle. The angular switching frequency and angular time are defined as follows:

$$\omega = \theta_{\text{ON}}^- f_s \quad (2.2)$$

$$\theta = \omega t \quad (2.3)$$

where $\theta_{\text{ON}}^- = 2\pi$ is the left-hand side boundary of the turn-on angle, f_s is the switching frequency and t is the time. The input choke is regarded as infinite and consequently I_{in} is considered purely DC. By solving (2.1) using the Laplace transform we get:

$$\left. \frac{i_\phi(\theta)}{I_{in}} \right|_{\theta_{\text{ON}}^+ \leq \theta \leq \theta_{\text{OFF}}^-} = A_1 (i_\phi(\theta_{\text{ON}}^+)) \cos(\tau_\phi \theta) + B_1 (v_{C_\phi}(\theta_{\text{ON}}^+)) \sin(\tau_\phi \theta) \quad (2.4)$$

where A_1 and B_1 are coefficients dependent on boundary conditions and τ_ϕ is the resonant frequency of the ϕ -branch normalised to the switching frequency:

$$\tau_\phi = \frac{1}{\omega \sqrt{L_\phi C_\phi}}. \quad (2.5)$$

The turn-off angular time is defined as:

$$\theta_{\text{OFF}} = \theta_{\text{ON}}^- D \quad (2.6)$$

where D is the duty cycle of the switching signal.

We assume that the load network Q is high enough, i.e., $\omega L_{s1}/R_{sL} > 15$ [19], so that the current through the coil can be approximated as sinusoidal at f_s [32]:

$$\frac{i_o(\theta)}{I_{in}} = \lambda \sin(\theta + \phi) \quad (2.7)$$

where ϕ is the output current phase relative to the gate signal of the switching device [36] and λ is the peak output current (I_m) to input current ratio of magnitudes:

$$\lambda = \frac{I_m}{I_{in}}. \quad (2.8)$$

During the part of the period which the device is not conducting, the current flowing through it is zero. By applying KVL and Kirchhoff's Current Law (KCL) we get:

$$\begin{cases} v_{DS}(\theta) = \omega L_\phi \frac{di_\phi(\theta)}{d\theta} + v_{C_\phi}(\theta_{\text{OFF}}^+) + \frac{1}{\omega C_\phi} \int_{\theta_{\text{OFF}}^+}^{\theta} i_\phi(u) du \\ i_\phi(\theta) = I_{in} - \omega C_\phi \frac{dv_{DS}(\theta)}{d\theta} - i_o(\theta) \end{cases} \quad (2.9)$$

By solving the system of equations in (2.9) we get the ϕ -branch current equation during turn-off:

$$\begin{aligned} \left. \frac{i_\phi(\theta)}{I_{in}} \right|_{\theta_{\text{OFF}}^+ \leq \theta \leq \theta_{\text{ON}}^-} &= A_2 (i_\phi(\theta_{\text{OFF}}^+)) \cos(\tau_2 \theta) + B_2 (v_{C_\phi}(\theta_{\text{OFF}}^+)) \sin(\tau_2 \theta) - P_1 \sin(\theta + \phi) \\ &+ K_1 \end{aligned} \quad (2.10)$$

where again A_2 and B_2 are coefficients dependent on boundary conditions and

$$\tau_2 = \frac{\tau_\phi}{\sqrt{K_2}} \quad (2.11)$$

$$P_1 = \frac{p\tau_2^2}{\tau_2^2 - 1} \quad (2.12)$$

$$K_1 = \frac{p}{\lambda} \quad (2.13)$$

$$K_2 = 1 - K_1. \quad (2.14)$$

The loading factor p [56] and the capacitance ratio k of the shunt capacitor to the ϕ -branch capacitor are defined below:

$$p = \frac{\lambda}{k + 1} \quad (2.15)$$

$$k = \frac{C_p}{C_\phi}. \quad (2.16)$$

By applying KCL while the device is not conducting and incorporating (2.7) and (2.10), the normalised current through C_p is given by:

$$\left. \frac{i_p(\theta)}{I_{in}} \right|_{\theta_{\text{OFF}}^+ \leq \theta \leq \theta_{\text{ON}}^-} = K_2 + P_2 \sin(\theta + \phi) - A_2 \cos(\tau_2 \theta) - B_2 \sin(\tau_2 \theta) \quad (2.17)$$

where

$$P_2 = P_1 - \lambda. \quad (2.18)$$

The voltage across the device during the part of the period in which it is turned off is directly derived from (2.17):

$$v_{DS}(\theta) = \frac{1}{B_C} \int_{\theta_{\text{OFF}}^+}^{\theta} i_p(u) du \quad (2.19)$$

where B_C is the normalised C_p capacitance:

$$B_C = \omega C_p. \quad (2.20)$$

Solving (2.19) results in the relation:

$$v_{DS}(\theta) = \frac{I_{in}}{B_C} \beta(\theta) \quad (2.21)$$

where

$$\beta(\theta) = K_2\theta - P_2 \cos(\theta + \phi) - \frac{A_2}{\tau_\phi} \sin(\tau_\phi\theta) + \frac{B_2}{\tau_\phi} \cos(\tau_\phi\theta) + C, \quad (2.22)$$

$$C = \frac{A_2}{\tau_2} \sin(\tau_2\theta_{\text{OFF}}) - \frac{B_2}{\tau_2} \cos(\tau_2\theta_{\text{OFF}}) - K_2\theta_{\text{OFF}} + P_2 \cos(\theta_{\text{OFF}} + \phi). \quad (2.23)$$

The input voltage is equal to the mean of the drain voltage:

$$V_{in} = \frac{1}{\theta_{\text{ON}}^-} \int_{\theta_{\text{ON}}^+}^{\theta_{\text{ON}}^-} v_{DS}(\theta) d\theta. \quad (2.24)$$

By combining (2.21) and (2.24) we get:

$$V_{in} = a \frac{I_{in}}{B_C} \quad (2.25)$$

where a is calculated from the relation:

$$\begin{aligned} \theta_{\text{ON}}^- a = & K_2 (\theta_{\text{OFF}} - \theta_{\text{ON}}^-)^2 + P_2 [\sin(\theta_{\text{OFF}} + \phi) + (\theta_{\text{ON}}^- - \theta_{\text{OFF}}) \cos(\theta_{\text{OFF}} + \phi) - \sin \phi] \\ & + \frac{A_2}{\tau_2} \left[\frac{1}{\tau_2} (\cos(\tau_2\theta_{\text{ON}}^-) - \cos(\tau_2\theta_{\text{OFF}})) + (\theta_{\text{ON}}^- - \theta_{\text{OFF}}) \sin(\tau_2\theta_{\text{OFF}}) \right] \\ & + \frac{B_2}{\tau_2} \left\{ \frac{1}{\tau_2} [\sin(\tau_2\theta_{\text{ON}}^-) - \sin(\tau_2\theta_{\text{OFF}})] - (\theta_{\text{ON}}^- - \theta_{\text{OFF}}) \cos(\tau_2\theta_{\text{OFF}}) \right\}. \end{aligned} \quad (2.26)$$

Then, combining (2.21) with (2.25), the normalised drain voltage during turn-off is given by:

$$\frac{v_{DS}(\theta)}{V_{in}} \bigg|_{\theta_{\text{OFF}}^+ \leq \theta \leq \theta_{\text{ON}}^-} = \frac{1}{a} \beta(\theta). \quad (2.27)$$

Applying KCL while the switching device is conducting, by combining (2.4) and (2.7), gives the normalised current through the device:

$$\frac{i_S(\theta)}{I_{in}} \bigg|_{\theta_{\text{ON}}^+ \leq \theta \leq \theta_{\text{OFF}}^-} = 1 - A_1 \cos(\tau_\phi\theta) - B_1 \sin(\tau_\phi\theta) - \lambda \sin(\theta + \phi). \quad (2.28)$$

By taking the derivative of (2.4) and (2.10) and normalising using (2.25) we get:

$$v_{L_\phi}(\theta) = \omega L_\phi \frac{di_\phi(\theta)}{d\theta} \quad (2.29)$$

$$\frac{v_{L_\phi}(\theta)}{V_{in}} = \frac{\omega B_C L_\phi}{a} \begin{cases} \tau_\phi [B_1 \cos(\tau_\phi \theta) - A_1 \sin(\tau_\phi \theta)], & \theta_{ON}^+ \leq \theta \leq \theta_{OFF}^- \\ \tau_2 [B_2 \cos(\tau_2 \theta) - A_2 \sin(\tau_2 \theta)] - P_1 \cos(\theta + \phi), & \theta_{OFF}^+ \leq \theta \leq \theta_{ON}^- \end{cases} \quad (2.30)$$

and integrating them in the same manner results in:

$$v_{C_\phi}(\theta) = \begin{cases} v_{C_\phi}(\theta_{ON}^+) + \frac{1}{\omega C_\phi} \int_{\theta_{ON}^+}^{\theta} i_\phi(u) du \\ v_{C_\phi}(\theta_{OFF}^+) + \frac{1}{\omega C_\phi} \int_{\theta_{OFF}^+}^{\theta} i_\phi(u) du \end{cases} \quad (2.31)$$

$$\frac{v_{C_\phi}(\theta)}{V_{in}} = \frac{k}{a} \begin{cases} \frac{A_1}{\tau_\phi} \sin(\tau_\phi \theta) - \frac{B_1}{\tau_\phi} \sin(\tau_\phi \theta), & \theta_{ON}^+ \leq \theta \leq \theta_{OFF}^- \\ \frac{A_2}{\tau_2} \sin(\tau_2 \theta) - \frac{B_2}{\tau_2} \sin(\tau_2 \theta) + P_1 \cos(\theta + \phi) + K_1 \theta + E, & \theta_{OFF}^+ \leq \theta \leq \theta_{ON}^- \end{cases} \quad (2.32)$$

where

$$E = P_1 \left[\frac{\cos \phi}{K_2 \tau_2} - \cos(\theta_{OFF} + \phi) \right] - K_1 \theta_{OFF} + \frac{B_2}{\tau_2} \left[\cos(\tau_2 \theta_{OFF}) - \frac{1}{K_2} \right] - \frac{A_2}{\tau_2} \sin(\tau_2 \theta_{OFF}). \quad (2.33)$$

Load Network

The voltage across R_{sL} is:

$$u_{R_{sL}}(\theta) = R_{sL} i_o(\theta) \quad (2.34)$$

where the reflected load and coil resistances are related by the equation:

$$R_{sL} = R_{s1} + R_L. \quad (2.35)$$

By following the convention proposed in [32], we define v_X as the fictitious voltage across the residual series reactance X of the load network at f_S (X is assumed to be infinite at any other frequency), since C_s and L_{s1} are not exactly at resonance:

$$v_X(\theta) = X \frac{di_o(\theta)}{d\theta} \quad (2.36)$$

where

$$X = \omega L_{s1} - \frac{1}{\omega C_s}. \quad (2.37)$$

Consequently, the part of L_{s1} that resonates with C_s is $(\omega^2 C_s)^{-1}$, as shown in Figure 2.1. We define the voltage v_1 as the combined effect of $v_{R_{sL}}$ and v_X :

$$v_1(\theta) = v_{R_{sL}}(\theta) + v_X(\theta). \quad (2.38)$$

Using (2.7), (2.34), (2.36) and (2.38), we have:

$$v_1(\theta) = \rho I_m \sin(\theta + \phi_1) \quad (2.39)$$

where

$$\rho = R_{sL} \sqrt{1 + \tan^2 \psi}, \quad (2.40)$$

$$\phi_1 = \phi + \psi, \quad (2.41)$$

$$\psi = \arctan\left(\frac{X}{R_{sL}}\right). \quad (2.42)$$

The magnitude of v_1 is equal to the Fourier component of v_{DS} at f_S :

$$\rho I_m = \frac{1}{\pi} \int_{\theta_{ON}^+}^{\theta_{ON}^-} v_{DS}(\theta) \sin(\theta + \phi_1) d\theta. \quad (2.43)$$

Solving (2.43) gives the relation:

$$\pi B_C \lambda \rho(\psi) = K_2 f_1(\psi) + P_2 f_2(\psi) + \frac{A_2}{2\tau_2} f_3(\psi) + \frac{B_2}{2\tau_2} f_4(\psi) \quad (2.44)$$

where ψ is the phase difference between i_o and v_1 , and

$$f_1(\psi) = \sin(\phi_1(\psi)) - (\theta_{ON}^- - \theta_{OFF}) \cos(\phi_1(\psi)) - \sin(\theta_{OFF} + \phi_1(\psi)), \quad (2.45)$$

$$f_2(\psi) = \frac{\cos(\phi_1(\psi) + \phi)}{4} - \pi(1 - D) \sin \psi + \frac{\cos(2\theta_{OFF} + \phi_1(\psi) + \phi)}{4} \\ - \frac{\cos(\theta_{OFF} - \psi)}{2} + \frac{\cos \psi}{2} - \frac{\cos(\theta_{OFF} + \phi_1(\psi) + \phi)}{2}, \quad (2.46)$$

$$f_3(\psi) = \frac{\sin((\tau_2 + 1)\theta_{ON}^- + \phi_1(\psi))}{\tau_2 + 1} + \frac{\tau_2 \sin((\tau_2 + 1)\theta_{OFF} + \phi_1(\psi))}{\tau_2 + 1} \\ - \frac{\sin((\tau_2 - 1)\theta_{ON}^- + \phi_1(\psi))}{\tau_2 - 1} + \frac{\tau_2 \sin((\tau_2 - 1)\theta_{OFF} - \phi_1(\psi))}{\tau_2 - 1} \\ - \sin(\tau_2 \theta_{OFF} + \phi_1(\psi)) - \sin(\tau_2 \theta_{OFF} - \phi_1(\psi)), \quad (2.47)$$

$$\begin{aligned}
f_4(\psi) = & \frac{\tau_2 \cos((1 - \tau_2)\theta_{\text{OFF}} + \phi_1(\psi))}{1 - \tau_2} - \frac{\cos((1 - \tau_2)\theta_{\text{ON}}^- + \phi_1(\psi))}{1 - \tau_2} \\
& - \frac{\tau_2 \cos((\tau_2 + 1)\theta_{\text{OFF}} + \phi_1(\psi))}{\tau_2 + 1} - \frac{\cos((\tau_2 + 1)\theta_{\text{ON}}^- + \phi_1(\psi))}{\tau_2 + 1} \\
& - \cos(\tau_2\theta_{\text{OFF}} - \phi_1(\psi)) + \cos(\tau_2\theta_{\text{OFF}} + \phi_1(\psi)).
\end{aligned} \tag{2.48}$$

The output power is:

$$P_o = \frac{I_m^2 R_L}{2}. \tag{2.49}$$

Since the only losses incorporated in the circuit are in the Tx coil, the input power is:

$$P_{in} = \frac{I_m^2 R_{sL}}{2}. \tag{2.50}$$

By combining 2.8 and 2.50 we get the following relation for the input voltage:

$$V_{in} = \frac{\lambda I_m R_{sL}}{2}. \tag{2.51}$$

The output voltage, i.e. the voltage across the loaded coil, is the series combination of the voltage across L_{s1} and R_{sL} . Using (2.7) and (2.34) and normalising with (2.25), we have:

$$\frac{v_o(\theta)}{V_{in}} = \frac{B_C \lambda}{a} (\omega L_{s1} \cos(\theta + \phi) + R_{sL} \sin(\theta + \phi)). \tag{2.52}$$

The minimum impedance value of the input choke must be substantially higher than the input resistance of the inverter [28] and its inductance can be calculated by combining (2.8) with (2.50):

$$L_{rfc} \gg \frac{R_{in}}{\omega} \tag{2.53}$$

where

$$R_{in} = \frac{\lambda^2 R_{sL}}{2}. \tag{2.54}$$

For the special case of the inverter with a finite DC-feed inductance and 50% duty cycle the input inductance value can be calculated using the expression proposed in [63] combined with (2.54). In this work, the case for the finite input choke is addressed in subsection 2.5.5.

Boundary and Soft-switching Conditions

If we were to derive the exact waveform expressions of the inverter in 2.1, we should be solving a 6th degree differential equation (which is the approach we follow in the 2nd part of this proposed design algorithm). However, doing so results in overly complex analytical expressions of very limited practical use, since they would no longer provide meaningful insight of the circuit behaviour, which defies the main purpose of the FO approach. Even the approximation of infinite L_{rfc} and high Q output network still requires solving a 3rd order differential equation with two boundary conditions (device turned-off and on). For comparison, the Class E inverter requires solving just one FO differential equation [32].

To overcome this, we made one more simplification, which despite introducing another source of error, results in more manageable expressions with a good trade-off between accuracy and complexity: we treat the ϕ -branch independently of the shunt capacitor network during turn-off. This is also obvious from the formulation of (2.4) and (2.10), which incorporates only four boundary dependent parameters ($A_{1,2}, B_{1,2}$) instead of six, which effectively reduces the degree of the differential equation from three to two. This results in simpler and more compact analytic waveform expressions. The choice of the ϕ -branch specifically is also based on the fact that during turn-on it is already independent of the shunt capacitor, since the device is shorting it. It should be mentioned that this approach is fairly typical in the existing literature [35, 1]. The additional source of error introduced by this approach is eliminated by the more accuracy-based iterative tuning process of the subsequent algorithmic stage in section 2.5, which simulates the circuit using the full sixth degree state space differential equation solution.

Given the above reasoning, the on-off boundary conditions of the ϕ -branch-shunt network can involve any combination of two signals among v_{DS} , i_ϕ and v_{C_ϕ} . Since the equivalent of v_{DS} expressed at the ϕ -branch is the sum of v_{L_ϕ} and v_{C_ϕ} , the simplified boundary condition expressions can incorporate any two signals among i_ϕ , v_{L_ϕ} and v_{C_ϕ} . Different combinations of boundary conditions will provide different inverter designs, for the same inputs. The designer can choose the preferred boundaries based on the component values that they provide and the focus of the modelling accuracy of the FO approximation, since the parts of the circuit that the boundaries are applied will be simulated with more precision.

As an example, we derive the exact equations satisfying the switching continuity conditions for

the i_ϕ and v_{C_ϕ} boundaries. The same methodology can be applied for any other two signals mentioned above, by using the corresponding equations. By using (2.4), (2.10) and (2.32) to satisfy the boundary continuity conditions we get:

$$\begin{bmatrix} i_\phi(\theta_{\text{ON}}^-) \\ v_{C_\phi}(\theta_{\text{ON}}^-) \\ i_\phi(\theta_{\text{OFF}}^-) \\ v_{C_\phi}(\theta_{\text{OFF}}^-) \end{bmatrix} = \begin{bmatrix} i_\phi(\theta_{\text{ON}}^+) \\ v_{C_\phi}(\theta_{\text{ON}}^+) \\ i_\phi(\theta_{\text{OFF}}^+) \\ v_{C_\phi}(\theta_{\text{OFF}}^+) \end{bmatrix}. \quad (2.55)$$

Equation (2.55) is a system of four linear equations with the four boundary coefficients as unknowns and its solution is given by:

$$\begin{bmatrix} A_1 & B_1 & A_2 & B_2 \end{bmatrix}^T = \mathbf{B}^{-1} \mathbf{a} \quad (2.56)$$

where

$$\mathbf{a} = \begin{bmatrix} K_1 - P_1 \sin(\theta_{\text{OFF}} + \phi) \\ K_1 - P_1 \sin \phi \\ \frac{P_1 \cos \phi}{\sqrt{K_2}} \\ P_1 \left[\cos(\theta_{\text{OFF}} + \phi) - \left(1 + \frac{1}{\tau_2 K_2} \right) \cos \phi \right] \\ + (\theta_{\text{ON}}^- - \theta_{\text{OFF}}) K_1 \end{bmatrix}, \quad (2.57)$$

$$\mathbf{B} = \begin{bmatrix} \cos(\tau_\phi \theta_{\text{OFF}}) & \sin(\tau_\phi \theta_{\text{OFF}}) & -\cos(\tau_2 \theta_{\text{OFF}}) \\ 1 & 0 & -\cos(\tau_2 \theta_{\text{ON}}^-) \\ \sin(\tau_\phi \theta_{\text{OFF}}) & -\cos(\tau_\phi \theta_{\text{OFF}}) & 0 \\ 0 & \frac{1}{\tau_\phi} & \frac{\sin(\tau_2 \theta_{\text{ON}}^-) - \sin(\tau_2 \theta_{\text{OFF}})}{\tau_2} \\ & & -\sin(\tau_2 \theta_{\text{OFF}}) \\ & & -\sin(\tau_2 \theta_{\text{ON}}^-) \\ & & \frac{1}{\sqrt{K_2}} \\ & & \frac{\cos(\tau_2 \theta_{\text{OFF}}) - \cos(\tau_2 \theta_{\text{ON}}^-) - \frac{1}{K_2}}{\tau_2} \end{bmatrix}. \quad (2.58)$$

Applying the ZVS condition through (2.27) results in the equation:

$$C(p, \phi) = P_2(p, \phi) \cos \phi + \frac{A_2(p, \phi)}{\tau_2(p)} \sin(\theta_{\text{ON}}^- \tau_2(p)) - \theta_{\text{ON}}^- K_2(p) - \frac{B_2(p, \phi)}{\tau_2(p)} \cos(\theta_{\text{ON}}^- \tau_2(p)). \quad (2.59)$$

The drain current is equal to i_p at turn-on, because of the discharge of the shunt capacitor. Hence, we can apply the condition of the drain current at turn-on by using (2.17):

$$\frac{i_S^{\text{ON}}}{I_{in}} = K_2(p) + P_2(p) \sin \phi - A_2(p, \phi) \cos(\theta_{\text{ON}}^- \tau_2(p)) - B_2(p, \phi) \sin(\theta_{\text{ON}}^- \tau_2(p)) \quad (2.60)$$

where i_S^{ON} is the drain current at turn-on.

2.4.3 Component Values

As shown in Fig. 2.2, the FO design process of the inverter begins by determining the requirements of the IPT system, namely the output power P_o and switching frequency f_S . Then, we define the desired characteristics of the circuit, i.e., the frequency of the ϕ -branch normalised to f_S (τ_ϕ), the duty cycle (D), the ratio λ of the peak output current (I_m) to the input current (I_{in}) (which represents the DC to AC current gain), and the current through S at turn-on (i_S^{ON}). R_{sL} is defined according to the inductive link properties and the corresponding choice of L_{s1} , while R_{s1} is an intrinsic property of L_{s1} . All the above parameters are the inputs to the design algorithm.

R_L is computed from (2.35), followed by I_m using (2.49). Then I_{in} is derived from (2.8), so that next, V_{in} can be calculated from (2.51). If it is preferable to design with the input voltage set as condition, then (2.51) needs to be solved for λ instead.

After choosing the preferred pair of waveforms for the computation of the boundary continuation conditions, as described in section E, we can apply (2.56), along with (2.4), (2.10), (2.11), (2.12), (2.13) and (2.14), to calculate the boundary coefficients. The parameters p and ϕ are derived by solving the system of equations formed by (2.22) and (2.60), with the incorporation of (2.18) and (2.23). In this work, we solve the combined system of (2.56), (2.59) and (2.60), since the boundary parameters are interconnected, using the trust-region-dogleg algorithm described in

[64, 65].

Next, we compute B_C from (2.25) and (2.26), followed by C_p from the combination of (2.2) and (2.20). Then, C_ϕ is directly calculated from (2.16) and L_ϕ from (2.5). Numerically solving (2.44), along with (2.40), (2.41), (2.45), (2.46), (2.47) and (2.48), gives ψ . The iterative scheme that we use to solve the equation above is a combination of bisection, secant, and inverse quadratic interpolation methods described in [66, 67]. Thus, C_s can then be calculated from (2.37) and (2.42).

2.4.4 Measurements and Numerical Example

The application of the FO tuning equations is presented in the numerical example below. This example is further developed and improved in the following chapters of this paper. The inputs that were chosen to define the circuit properties are given in Table 2.1, along with the corresponding outputs of the algorithm. An analysis of the sensitivity of a Class E inverter to its component values has been conducted in [26]. The waveforms across various parts of the circuit shown in Figure 2.1 are given in Figure 2.3.

Table 2.1: Inputs and outputs of first order tuning example

	Quantity	Value	Unit
Inputs	P_o	50	W
	τ_ϕ	2	—
	λ	5	—
	i_S^{ON}	0	A
	R_{sL}	8.6	Ω
	R_{s1}	346	m Ω
	L_{s1}	1.24	μH
	f_S	13.56	MHz
	D	30	%
	Boundaries	$\{i_\phi, v_{C_\phi}\}$	—
Outputs	V_{in}	78.835	V
	C_p	228.971	pF
	L_ϕ	536.941	nH
	C_ϕ	64.141	pF
	C_s	150.317	pF

The complete WPT system of the experimental setup is shown in Figure 2.4 [68]. The inverter is represented as a current source connected to the Tx coil and the Rx coil (L_{s2}) is connected

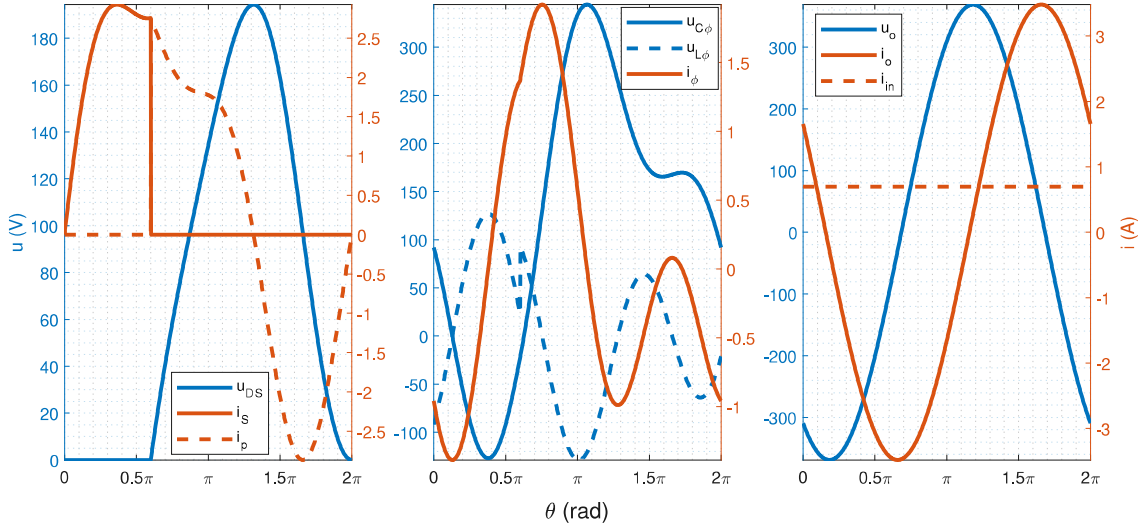


Figure 2.3: Inverter waveforms of the numerical example given in Table 2.1. The voltages are shown in blue on the left-hand side vertical axes of the graphs and the currents in orange on the left-hand side. The parts of the circuit each individual waveform corresponds to is given in Figure 2.1. The left-hand side graph shows the shunt network waveforms, the middle graph represents the phi-branch and the right-hand side graph has the input-output waveforms.

to an AC load (R_{ac}) via a series tuning capacitor (C_{s2}). The two coils are coupled together forming the WPT link, where k_s is the coupling factor and $R_{r1/2}$ is the radiation resistance of the Tx and Rx, respectively.

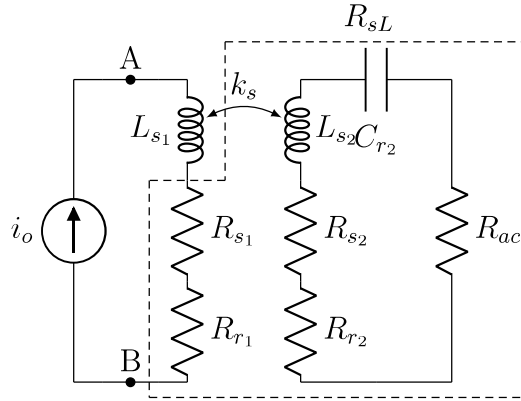


Figure 2.4: WPT link with a current source as inverter, series secondary tuning capacitor and AC load.

R_{ac} consists of 12 LTO100F100R0JTE3 AC resistors [69] in parallel. Because of the relatively low value of R_{ac} we opt for a series-tuned secondary [19], where the theoretical value of the tuning capacitor is derived from the resonance condition at the switching frequency:

$$C_{s2} = \frac{1}{\omega^2 L_{s1}} \quad (2.61)$$

since the two coupled coils are identical in our setup, whereas the generalised computation of the tuning capacitors is given in [70]. The WPT link coils consist of two planar spiral turns made of FR-4 printed circuit board (PCB) with maximum outer radius $r_o = 10.5$ cm, minimum inner radius $r_i = 6.75$ cm, track width of 1 cm, across distance $d_s = 12$ cm with zero lateral misalignment and angle. An estimation of the order of magnitude of the radiation resistances of the coils based on the size and geometry mentioned above can be calculated with [71]:

$$R_{r_{1/2}} \approx 320\pi^6 \left[\frac{f_s}{c} (r_o + r_i) \right]^4 = 1.137 \text{ m}\Omega \quad (2.62)$$

where c is the speed of light in vacuum.

Impedance measurements of the fully loaded ($k_S = k_S^{\max}$) and unloaded ($k_S = 0$) IPT link were taken both with an impedance analyzer (E4990A Impedance Analyzer from Keysight Technologies) and a Vector Network Analyzer (VNA) (ZNB 4 from Rohde & Schwarz) across the points A and B in Figure 2.4 and compared with each other. According to [72], for measuring the quality and coupling factors of the IPT link for the frequency and Q factor value range of our case study, the impedance analyser is preferable. Both the inductance and series resistance values measurements with the VNA were higher compared to the ones from the impedance analyser, as expected from [72]. The impedance measurements of the tuned resonant link using the E4990A with the Keysight 42941A Impedance Probe Kit connected to the pin probe are shown in Figure 2.5, where the fitting function of the Φ -branch reactance is

$$X_{\phi}^{\text{fit}}(f) = \frac{2\pi f L_{\phi} C_{\phi} - 1}{2\pi f C_{\phi}}. \quad (2.63)$$

The value of C_{s_2} was manually adjusted using the tuning method described in [20] from the starting theoretical value of (2.61). The measurements were taken from the empty inverter board with only the Tx coil soldered in place. This way, the adjustment of C_{s_2} , which in our setup are 3 kV C0G capacitors [73], naturally incorporates the stray inductances and capacitances of the PCB and the rest of the passive components, and the measurements represent the effective values of the circuit components. If a parasitic extraction tool is available, the incorporation of their effect can be done a posteriori in the calculations with the individual component values, however the above mentioned method of measurements gave the most accurate results when compared to the theoretical predictions. Also, if we want accurate impedance

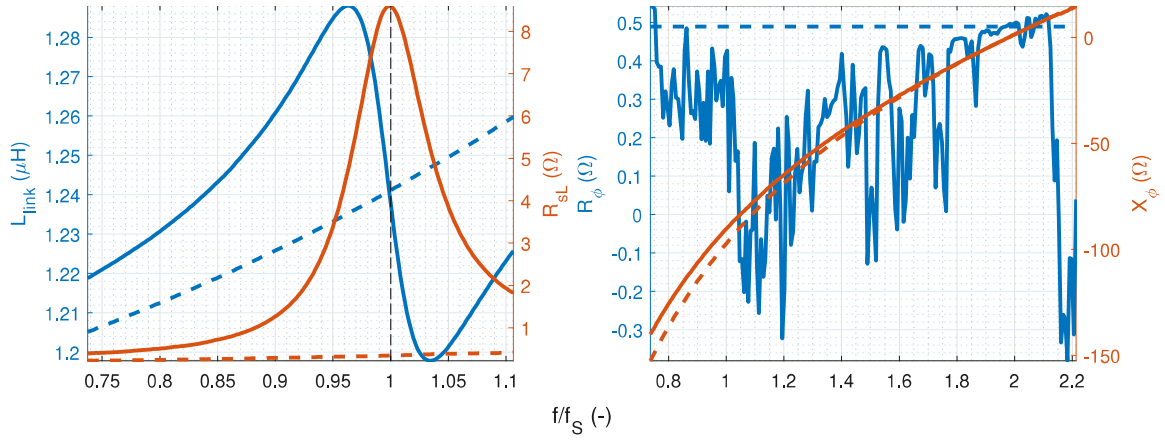


Figure 2.5: Inductance and series resistance measurement of the fully loaded (solid line) and unloaded (dashed line) IPT link (left), and total series resistance and reactance measurements (solid line) and fitting curves (dashed line) of the Φ -branch, with impedance analyser.

representation during operation with a current probe attached, we should perform the above measurement method with the current probe in place. However, the coupling of the current probe with the IPT link is minimal [74], so it can be omitted.

The numerical values of the equivalent series resistances in the measurements of Figure 2.5 and Table 2.1 are several orders of magnitude larger than the radiation resistance estimation of (2.62), and thus its effect can be considered negligible. An analytical approximation of the Tx inductance can be derived by [75]:

$$L_{s1} \approx 9.84 \times 10^{-6} \frac{n_s^2 (r_o + r_i)^2}{15r_o - 7r_i} = 1.062 \mu\text{H} \quad (2.64)$$

where n_s is the number of turns of the coil. The estimation in (2.64) agrees with the measurements of Figure 2.5, if we take into consideration and add the effects of the stray inductances of the SMA connectors. The coupling factor can be calculated using the formula in [20] and the experimental measurements as inputs:

$$k_s^{\max} = \frac{\sqrt{R_L (R_{ac} + R_{s1})}}{\omega L_{s1}} \approx 8.011 \%. \quad (2.65)$$

It must be noted at this point that the link was not optimised neither for radiation [71], nor for gain [76], since this procedure is irrelevant from the inverter design and thus beyond the scope of this study.

The aim of this inverter circuit example is to achieve high efficiency. The switching frequency of

choice is one of the commonly used lower ISM bands [77] both to reduce electromagnetic interference and increase the link efficiency by increasing the Q of the Tx and Rx coil, while resulting in realistic values of capacitances. In order to be able to measure AC current accurately, we limit the output power within the capabilities of the current probe at these frequencies, namely Keysight N2783B [74]. The order of the harmonic content of the output current is inversely related to its contribution in its THD in the case of the Class E inverter, according to [19, 78], so we set the ϕ -branch to resonate at double the switching frequency. We minimise the ohmic losses by reducing the currents and increasing the voltages in the circuit through a high λ value. Additionally, we minimise the switching device losses by applying zero derivative voltage switching (ZVDS), despite that this condition will result in non load independent operation, as defined in [1]. The duty cycle was chosen based on [1]. The output power capability and distribution of device stresses are mainly determined by λ and D ; high λ and low D increase the current demands and decrease the voltage requirements, and vice versa. The boundaries were selected according to the signals that we want to simulate more accurately.

By comparing the input requirements in Table 2.1 with the waveforms in Figure 2.3 we can verify that all the desired properties of the inverter are met. The limitation of the applied boundary conditions is revealed through the discontinuity during switching of $v_{L\phi}$.

2.5 State Space Tuning

2.5.1 Background

The second tuning step of the proposed algorithm uses a piece-wise SS representation for the formulation of the problem, similar to [40, 56]. However, instead of using a predefined optimisation tool for the design process, we developed a custom Newton based iterative method, starting from the solution of the previous step. The SS simulation resolves the approximation errors of the FO analysis and the aim of the numerical optimisation is to fine-tune the inverter while maintaining the required design properties. The advantages in modelling accuracy of the SS approach compared to FO approximations in Class E converters are demonstrated in [79, 80].

2.5.2 Simulation Equations

At this part of the algorithm, we replace the infinite choke with its actual measured value, and we model the switching device as a variable resistance $R_S^{\text{ON/OFF}}$, which represents the resistance of the switching device during turn-on/off. Also, as shown in Figure 2.6, we incorporate the series resistance R_{rfc} of the input choke, and the series resistance of L_ϕ , through the parameter p_ϕ , since it is proportionate to the windings of the inductor:

$$R_\phi = p_\phi L_\phi \quad (2.66)$$

where

$$p_\phi \equiv \frac{\tau_\phi \omega}{Q_{L_\phi}(f)|_{f=\tau_\phi f_S}}. \quad (2.67)$$

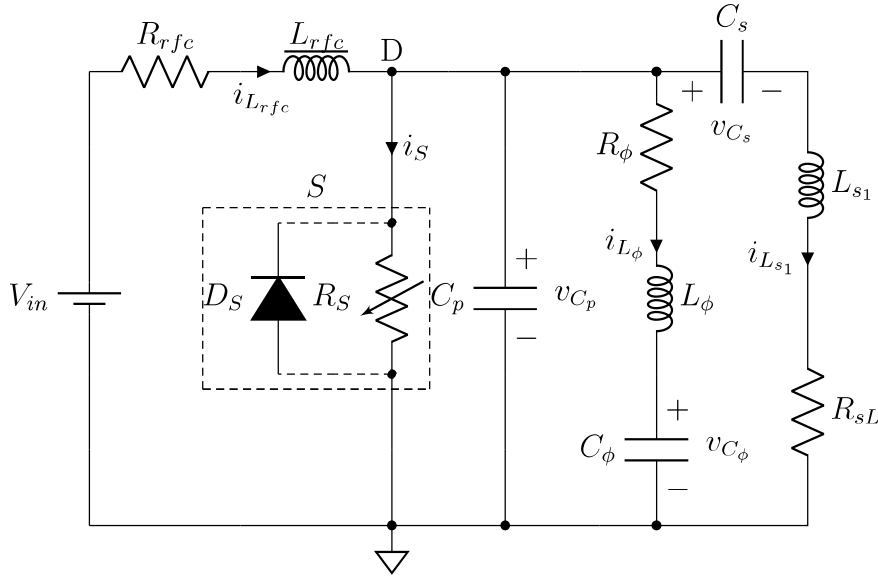


Figure 2.6: Circuit diagram of Class EF/ Φ inverter using the State Space formulation.

The 6th order system of linear SS differential equations of the inverter is given by:

$$\frac{d\mathbf{q}(\theta)}{d\theta} = \mathbf{A}\mathbf{q}(\theta) + \mathbf{b}u(\theta) \quad (2.68)$$

where u is the unit step function and the state vector is defined as follows:

$$\mathbf{q}(\theta) = \begin{bmatrix} i_{L_{rfc}}(\theta) & v_{C_p}(\theta) & i_{L_\phi}(\theta) & v_{C_\phi}(\theta) & v_{C_s}(\theta) & i_{L_{s1}}(\theta) \end{bmatrix}^T. \quad (2.69)$$

The rest of the parameters of the differential equation (2.68) are:

$$\mathbf{A}_{\text{ON/OFF}} = \frac{1}{\omega} \text{diag}^{-1}(L_{rfc}, C_p, L_\phi, C_\phi, C_s, L_{s1}) \cdot \begin{bmatrix} -R_{rfc} & -1 & 0 & 0 & 0 & 0 \\ 1 & \frac{-1}{R_S^{\text{ON/OFF}}} & -1 & 0 & 0 & -1 \\ 0 & 1 & -R_\phi & -1 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 1 & 0 & 0 & -1 & -R_{sL} \end{bmatrix}, \quad (2.70)$$

$$\mathbf{b} = \frac{V_{in}}{\omega L_{rfc}} \mathbf{e}_1. \quad (2.71)$$

where $\mathbf{e}_i$ is the single entry column vector whose i^{th} element is one and the rest are zero.

Equation (2.68) is solved separately for the part of the period that device is turned-on and off, in a piece-wise linear manner, hence the dual nature of (2.70). The solution of (2.68) is given by:

$$\begin{aligned} \mathbf{q}(\theta)|_{\theta_{\text{ON/OFF}}^+ \leq \theta \leq \theta_{\text{OFF/ON}}^-} &= e^{(\theta - \theta_{\text{ON/OFF}}^+) \mathbf{A}_{\text{ON/OFF}}} \mathbf{q}(\theta_{\text{ON/OFF}}^+) \\ &+ \mathbf{A}_{\text{ON/OFF}}^{-1} \left(e^{(\theta - \theta_{\text{ON/OFF}}^+) \mathbf{A}_{\text{ON/OFF}}} - \mathbf{I} \right) \mathbf{b} \end{aligned} \quad (2.72)$$

where $\mathbf{I}$ is the identity matrix. The boundary continuation conditions when the switching device is turning on and off during one period are described by the relation:

$$\begin{bmatrix} \mathbf{q}(\theta_{\text{ON}}^-) \\ \mathbf{q}(\theta_{\text{OFF}}^-) \end{bmatrix} = \begin{bmatrix} \mathbf{q}(\theta_{\text{ON}}^+) \\ \mathbf{q}(\theta_{\text{OFF}}^+) \end{bmatrix}. \quad (2.73)$$

By combining (2.72) with (2.73) we get:

$$\begin{bmatrix} \mathbf{q}(\theta_{\text{ON}}) \\ \mathbf{q}(\theta_{\text{OFF}}) \end{bmatrix} = \mathbf{C}^{-1} \mathbf{E} \quad (2.74)$$

where

$$\mathbf{C} = \begin{bmatrix} \mathbf{I} & -e^{(\theta_{\text{ON}}^- - \theta_{\text{OFF}}^-) \mathbf{A}_{\text{OFF}}} \\ -e^{\theta_{\text{OFF}}^- \mathbf{A}_{\text{ON}}} & \mathbf{I} \end{bmatrix} \quad (2.75)$$

$$\mathbf{E} = \begin{bmatrix} \mathbf{A}_{\text{OFF}}^{-1} \left(e^{(\theta_{\text{ON}}^- - \theta_{\text{OFF}})} \mathbf{A}_{\text{OFF}} - \mathbf{I} \right) \mathbf{b} \\ \mathbf{A}_{\text{ON}}^{-1} \left(e^{\theta_{\text{OFF}}} \mathbf{A}_{\text{ON}} - \mathbf{I} \right) \mathbf{b} \end{bmatrix}. \quad (2.76)$$

The inverse of (2.75) can be calculated by applying the Schur complement [81]:

$$\mathbf{C}^{-1} = \begin{bmatrix} \left[\mathbf{I} - e^{(\theta_{\text{ON}}^- - \theta_{\text{OFF}})} \mathbf{A}_{\text{OFF}} e^{\theta_{\text{OFF}}} \mathbf{A}_{\text{ON}} \right]^{-1} & \mathbf{0} \\ \mathbf{0} & \left[\mathbf{I} - e^{\theta_{\text{OFF}}} \mathbf{A}_{\text{OFF}} e^{(\theta_{\text{ON}}^- - \theta_{\text{OFF}})} \mathbf{A}_{\text{OFF}} \right]^{-1} \end{bmatrix} \cdot \begin{bmatrix} \mathbf{I} & e^{(\theta_{\text{ON}}^- - \theta_{\text{OFF}})} \mathbf{A}_{\text{OFF}} \\ e^{\theta_{\text{OFF}}} \mathbf{A}_{\text{ON}} & \mathbf{I} \end{bmatrix} \quad (2.77)$$

where $\mathbf{0}$ is the zero matrix. The current through the switching device is given by the relation:

$$i_S(\theta)|_{\theta_{\text{ON/OFF}}^{+/-} \leq \theta \leq \theta_{\text{OFF/ON}}^{+/-}} = \frac{v_{C_p}(\theta)}{R_s^{\text{ON/OFF}}}. \quad (2.78)$$

Simulating the inverter with (2.72) gives a more accurate and realistic representation of the operation of the circuit (Figure 2.7) compared to the FO formulation, since the assumptions and simplifications that are incorporated in the FO equations are no longer present in the SS approach. By comparing the waveforms in Figure 2.3 with the equivalent part of Figure 2.7, neither the required design properties of Table 2.1 nor the soft switching conditions are met, and further tuning is required.

The additional input parameters needed for the SS simulation in Figure 2.7 along with the ones in Table 2.1, are given in Table 2.2. I_m is calculated in the previous tuning step, as described in subsection 2.4.3, and the rest of the input values are based on the component selection of the experimental setup, which are more thoroughly presented and justified in subsection 2.5.5. Specifically for the input choke, according to (2.53) the impedance value chosen in Table 2.2 is around 57 times higher than the FO input resistance of the inverter, which practically acts as an infinite choke. The input component values for this stage of the algorithm are not limited only to the ones produced by our proposed first tuning step, but can be derived by any arbitrary design algorithm for Class EF inverters that needs additional correction, as long as the formulation of input conditions matches, such as the special cases discussed in [1].

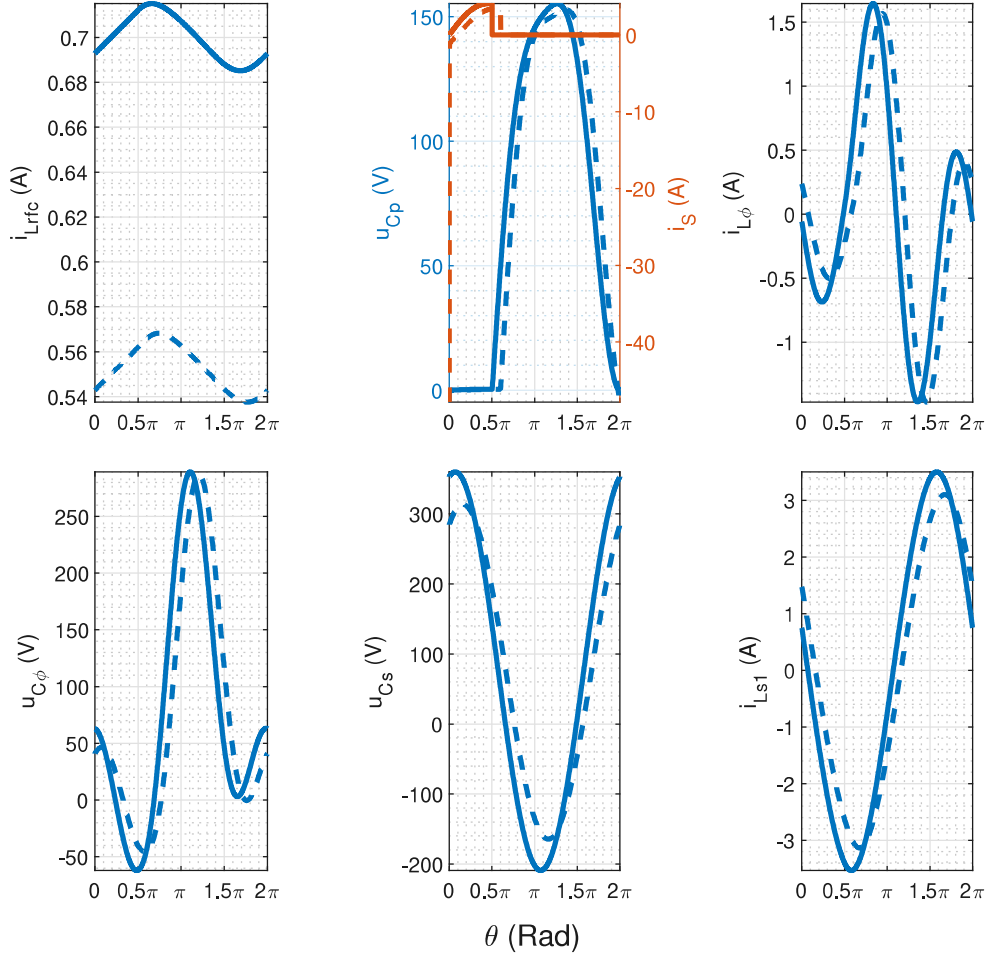


Figure 2.7: Simulation of the Class EF₂ inverter waveforms using state-space formulation. The dashed line is used to represent the design that occurs from the FO tuning method and the solid line shows the state-space tuned inverter.

2.5.3 Iterative Tuning Process

In this section we introduce a tuning method using the SS representation in order to correct the inaccuracies caused by the FO formulation. We choose to keep the ϕ -branch unaltered and adjust the rest of the control parameters accordingly to reassure that the circuit is operating as defined by the input parameters in Table 2.1. This corresponds to readjusting P_o , λ , $v_{C_p}(\theta_{ON}^-)$ and i_s^{ON} at their desired values by optimising for V_{in} , D , C_p and C_s .

The input voltage determines the output power, which basically is the amplitude of the output current, since the load is regarded as constant. C_s sets the load network impedance, which primarily defines λ but also shapes the drain voltage waveform. C_p and D also shape the drain voltage, with the first one mainly contributing to the value at turn-on and the latter mostly

Table 2.2: Inputs and outputs of state space Class EF₂ tuning example

	Quantity	Value	Unit
Inputs*	I_m	3.481	A
	L_{rfc}	72	μH
	R_{rfc}	500	$\text{m}\Omega$
	R_S^{ON}	100	$\text{m}\Omega$
	R_S^{OFF}	650	$\text{M}\Omega$
	p_ϕ	10^6	ΩH^{-1}
Outputs	V_{in}	75.7	V
	D	25.169	%
	C_p	284.559	pF
	C_s	143.166	pF
Relative Change	$\delta(V_{in})$	-3.977	%
	$\delta(D)$	-16.103	%
	$\delta(C_p)$	21.277	%
	$\delta(C_s)$	-4.757	%

*The inputs given in this table are in addition to the data of Table 2.1.

affecting the derivative. Changing the combination of L_ϕ - C_ϕ while keeping τ_ϕ constant also affects the drain voltage shape, however including them as independent variables in the iterative scheme impacted the convergence negatively and made it uncontrollable.

The state vector formulation in (2.72) is defined in terms of matrix exponentials which is not a convenient form for dealing with the output current characteristics. By approximating the output current waveform using the sine wave fit algorithm proposed in [82] we can solve for peak output current as well as minimise the THD. The sine coefficients of the fitted waveforms are defined as:

$$y_n = z_1 \cos \theta_n + z_2 \sin \theta_n + z_3 \quad (2.79)$$

where $n = 1, 2, \dots, N$, N is the waveform discretisation number, and

$$\mathbf{z} = [\mathbf{D}^T \mathbf{D}]^{-1} \mathbf{D}^T \mathbf{y}, \quad (2.80)$$

$$\mathbf{D} = \begin{bmatrix} \cos \theta_1 & \sin \theta_1 & 1 \\ \cos \theta_2 & \sin \theta_2 & 1 \\ \vdots & \vdots & \vdots \\ \cos \theta_n & \sin \theta_n & 1 \end{bmatrix}, \quad (2.81)$$

$$\mathbf{y} = \begin{bmatrix} i_{L_{s1}}(\theta_1) & i_{L_{s1}}(\theta_2) & \dots & i_{L_{s1}}(\theta_N) \end{bmatrix}^T, \quad (2.82)$$

$$\theta_n = (n-1) \frac{2\pi}{N-1}. \quad (2.83)$$

We define the following system of non-linear equations in the form of a vector function:

$$\mathbf{f}(\mathbf{x}) = \begin{bmatrix} v_{C_p}(\theta_{\text{ON}}; \mathbf{x}) & i_{C_p}(\theta_{\text{ON}}^-; \mathbf{x}) - i_S^{\text{ON}} & \sqrt{z_1^2(\mathbf{x}) + z_2^2(\mathbf{x})} - I_m & z_3(\mathbf{x}) \\ \frac{\max_{\theta} |i_{L_{s1}}(\theta; \mathbf{x})|}{I_{L_{rfc}}(\mathbf{x})} - \lambda \end{bmatrix}^T \quad (2.84)$$

where

$$\mathbf{x} = \begin{bmatrix} C_p & D & V_{in} & C_s \end{bmatrix}^T. \quad (2.85)$$

The current through C_p and the DC input current in (2.84) are:

$$i_{C_p}(\theta_{\text{ON}}^-; \mathbf{x}) = i_{L_{rfc}}(\theta_{\text{ON}}; \mathbf{x}) - \frac{v_{C_p}(\theta_{\text{ON}}; \mathbf{x})}{R_S^{\text{OFF}}} - i_{L_{\phi}}(\theta_{\text{ON}}; \mathbf{x}) - i_{L_{s1}}(\theta_{\text{ON}}; \mathbf{x}), \quad (2.86)$$

$$I_{L_{rfc}}(\mathbf{x}) = \frac{1}{\theta_{\text{ON}}^-} \int_{\theta_{\text{ON}}^+}^{\theta_{\text{ON}}^-} i_{L_{rfc}}(\theta; \mathbf{x}) d\theta. \quad (2.87)$$

The peak output current in the fifth element of (2.84) can be calculated by setting the derivative of (2.72) to zero:

$$\frac{d\mathbf{q}_{\text{ON/OFF}}(\theta; \mathbf{x})}{d\theta} = e^{(\theta - \theta_{\text{ON/OFF}}^+(\mathbf{x}))\mathbf{A}_{\text{ON/OFF}}(\mathbf{x})} (\mathbf{A}_{\text{ON/OFF}}(\mathbf{x}) \mathbf{q}(\theta_{\text{ON/OFF}}; \mathbf{x}) + \mathbf{b}(\mathbf{x})). \quad (2.88)$$

The solution to (2.87) can be obtained either arithmetically e.g., through the trapezoidal rule [83], or by analytically integrating (2.72):

$$\begin{aligned} \int_{\theta_{\text{ON/OFF}}^+(\mathbf{x})}^{\theta_{\text{OFF/ON}}^-(\mathbf{x})} \mathbf{q}_{\text{ON/OFF}}(\theta; \mathbf{x}) d\theta &= \mathbf{A}_{\text{ON/OFF}}^{-1}(\mathbf{x}) \left\{ \left(e^{(\theta_{\text{OFF/ON}}^-(\mathbf{x}) - \theta_{\text{ON/OFF}}^+(\mathbf{x}))\mathbf{A}_{\text{ON/OFF}}(\mathbf{x})} \right. \right. \\ &\quad \left. \left. - \mathbf{I} \right) \mathbf{q}(\theta_{\text{ON/OFF}}; \mathbf{x}) + \left[\mathbf{A}_{\text{ON/OFF}}^{-1}(\mathbf{x}) \right. \right. \\ &\quad \left. \left. \cdot \left(e^{(\theta_{\text{OFF/ON}}^-(\mathbf{x}) - \theta_{\text{ON/OFF}}^+(\mathbf{x}))\mathbf{A}_{\text{ON/OFF}}(\mathbf{x})} - \mathbf{I} \right) \right. \right. \\ &\quad \left. \left. + \left(\theta_{\text{ON/OFF}}^+(\mathbf{x}) - \theta_{\text{OFF/ON}}^-(\mathbf{x}) \right) \mathbf{I} \right] \mathbf{b}(\mathbf{x}) \right\}. \end{aligned} \quad (2.89)$$

An alternative to the above tuning scheme would be the combination of (2.84) and (2.85), but

without the last element of each vector. This version is computationally lighter and easier to converge compared to the full scheme because the inverter behaviour is very sensitive to C_s . The drawback of such objective function would be that the occurring design would no longer satisfy the condition for λ .

The circuit design resulting from the solution of (2.84) corresponds to the required conditions for ideal tuned operation of the Class EF/ Φ inverter, based on the inputs in Table 2.1. More specifically, the first component of (2.84) is the ZVS condition, the second one sets the slope of the drain voltage at turn-on to the desired value, the third condition sets the output current amplitude according to P_o and the fifth component controls λ . The fourth component of (2.84) is the DC part of $i_{L_{s1}}$ and combined with the third component result in reducing THD, when satisfied.

We solve (2.84) using the combined gradient-descent and Newton's method iterative algorithm mentioned in [84]:

$$\mathbf{x}^{(m+1)} = \mathbf{x}^{(m)} - \left\{ \gamma \left(a_N [\mathbf{J}_f^T(\mathbf{x}^{(m)}) \mathbf{J}_f(\mathbf{x}^{(m)})]^{-1} - a_{GD} \mathbf{I} \right) + a_{GD} \mathbf{I} \right\} \mathbf{J}_f^T(\mathbf{x}^{(m)}) \cdot \mathbf{f}(\mathbf{x}^{(m)}) \quad (2.90)$$

where m denotes the iteration index, γ is the mixing parameter of Newton's and gradient-descent methods, a_N and a_{GD} are the respective converging coefficients and $\mathbf{J}_f$ is the Jacobian matrix of $\mathbf{f}$ with respect to $\mathbf{x}$. We define the condition that needs to be satisfied for the termination of the iterative process in (2.90) as follows:

$$\frac{\|\mathbf{x}^{(m)} - \mathbf{x}^{(m-1)}\|_\infty}{\|\mathbf{x}^{(m)}\|_2} < \epsilon \quad (2.91)$$

where ϵ is the error tolerance.

2.5.4 Jacobian Computation

The components of the Jacobian in (2.90) are given by the relation:

$$\frac{\partial \mathbf{f}(\mathbf{x})}{\partial x_i} = \left[\begin{array}{c} \frac{\partial v_{C_p}(\theta_{\text{ON}}; \mathbf{x})}{\partial x_i} \quad \frac{\partial i_{C_p}(\theta_{\text{ON}}^-; \mathbf{x})}{\partial x_i} \quad \frac{z_1(\mathbf{x}) \frac{\partial z_1(\mathbf{x})}{\partial x_i} + z_2(\mathbf{x}) \frac{\partial z_2(\mathbf{x})}{\partial x_i}}{\sqrt{z_1^2(\mathbf{x}) + z_2^2(\mathbf{x})}} \quad \frac{\partial z_3(\mathbf{x})}{\partial x_i} \\ \frac{1}{I_{L_{rfc}}^2(\mathbf{x})} \left(I_{L_{rfc}}(\mathbf{x}) \frac{\partial \max_{\theta} |i_{L_{s1}}(\theta; \mathbf{x})|}{\partial x_i} - \max_{\theta} |i_{L_{s1}}(\theta; \mathbf{x})| \frac{\partial I_{L_{rfc}}(\mathbf{x})}{\partial x_i} \right) \end{array} \right]^T \quad (2.92)$$

where i is the index of $\mathbf{x}$.

The first two elements of (2.92) are computed from (2.74):

$$\frac{\partial}{\partial x_i} \begin{bmatrix} \mathbf{q}(\theta_{\text{ON}}; \mathbf{x}) \\ \mathbf{q}(\theta_{\text{OFF}}; \mathbf{x}) \end{bmatrix} = \mathbf{C}^{-1}(\mathbf{x}) \frac{\partial \mathbf{E}(\mathbf{x})}{\partial x_i} - \mathbf{C}^{-1}(\mathbf{x}) \frac{\partial \mathbf{C}(\mathbf{x})}{\partial x_i} \mathbf{C}^{-1}(\mathbf{x}) \mathbf{E}(\mathbf{x}). \quad (2.93)$$

Equation (2.93) with respect to the input voltage gives:

$$\frac{\partial}{\partial V_{in}} \begin{bmatrix} \mathbf{q}(\theta_{\text{ON}}; \mathbf{x}) \\ \mathbf{q}(\theta_{\text{OFF}}; \mathbf{x}) \end{bmatrix} = \frac{1}{\omega L_{rfc}} \mathbf{C}^{-1}(\mathbf{x}) \begin{bmatrix} \mathbf{A}_{\text{OFF}}^{-1}(\mathbf{x}) \left(e^{(\theta_{\text{ON}}^- - \theta_{\text{OFF}}(\mathbf{x})) \mathbf{A}_{\text{OFF}}(\mathbf{x})} - \mathbf{I} \right) \mathbf{e}_1 \\ \mathbf{A}_{\text{ON}}^{-1}(\mathbf{x}) \left(e^{\theta_{\text{OFF}}(\mathbf{x}) \mathbf{A}_{\text{ON}}(\mathbf{x})} - \mathbf{I} \right) \mathbf{e}_1 \end{bmatrix}. \quad (2.94)$$

The partial derivatives of the third and fourth elements of (2.92) are given by:

$$\frac{\partial \mathbf{z}(\mathbf{x})}{\partial x_i} = [\mathbf{D}^T \mathbf{D}]^{-1} \mathbf{D}^T \frac{\partial \mathbf{y}(\mathbf{x})}{\partial x_i}. \quad (2.95)$$

The right-hand side of (2.95) differentiated with respect to the input voltage can be calculated using the corresponding partial derivative of (2.72):

$$\begin{aligned} \frac{\partial \mathbf{q}_{\text{ON/OFF}}(\theta; \mathbf{x})}{\partial V_{in}} &= e^{(\theta - \theta_{\text{ON/OFF}}^+(\mathbf{x})) \mathbf{A}_{\text{ON/OFF}}(\mathbf{x})} \cdot \frac{\partial \mathbf{q}(\theta_{\text{ON/OFF}}; \mathbf{x})}{\partial V_{in}} + \frac{1}{\omega L_{rfc}} \mathbf{A}_{\text{ON/OFF}}^{-1}(\mathbf{x}) \\ &\quad \cdot \left(e^{(\theta - \theta_{\text{ON/OFF}}^+(\mathbf{x})) \mathbf{A}_{\text{ON/OFF}}(\mathbf{x})} - \mathbf{I} \right) \mathbf{e}_1. \end{aligned} \quad (2.96)$$

The fifth element of (2.92), with respect to V_{in} , can be calculated by combining (2.96) at the

angle of maximum output current with the following term:

$$\begin{aligned}
 \frac{\partial \int_{\theta_{\text{ON/OFF}}^+(\mathbf{x})}^{\theta_{\text{OFF/ON}}^-(\mathbf{x})} \mathbf{q}_{\text{ON/OFF}}(\theta; \mathbf{x}) d\theta}{\partial V_{in}} &= \mathbf{A}_{\text{ON/OFF}}^{-1}(\mathbf{x}) \\
 &\cdot \left\{ \left(e^{(\theta_{\text{OFF/ON}}^-(\mathbf{x}) - \theta_{\text{ON/OFF}}^+(\mathbf{x}))} \mathbf{A}_{\text{ON/OFF}}(\mathbf{x}) - \mathbf{I} \right) \right. \\
 &\cdot \frac{\partial \mathbf{q}(\theta_{\text{ON/OFF}}; \mathbf{x})}{\partial V_{in}} + \frac{1}{\omega L_{rfc}} \left[\mathbf{A}_{\text{ON/OFF}}^{-1}(\mathbf{x}) \right. \\
 &\cdot \left(e^{(\theta_{\text{OFF/ON}}^-(\mathbf{x}) - \theta_{\text{ON/OFF}}^+(\mathbf{x}))} \mathbf{A}_{\text{ON/OFF}}(\mathbf{x}) - \mathbf{I} \right) \\
 &\left. \left. + \left(\theta_{\text{ON/OFF}}^+(\mathbf{x}) - \theta_{\text{OFF/ON}}^-(\mathbf{x}) \right) \mathbf{I} \right] \mathbf{e}_1 \right\}. \tag{2.97}
 \end{aligned}$$

The partial derivatives in (2.93) when differentiated with respect to the duty cycle can be directly calculated using (2.75) and (2.76):

$$\frac{\partial \mathbf{E}(\mathbf{x})}{\partial D} = \theta_{\text{ON}}^- \begin{bmatrix} -e^{(\theta_{\text{ON}}^- - \theta_{\text{OFF}}(\mathbf{x}))} \mathbf{A}_{\text{OFF}}(\mathbf{x}) \mathbf{b}(\mathbf{x}) \\ e^{\theta_{\text{OFF}}(\mathbf{x})} \mathbf{A}_{\text{ON}}(\mathbf{x}) \mathbf{b}(\mathbf{x}) \end{bmatrix} \tag{2.98}$$

$$\frac{\partial \mathbf{C}(\mathbf{x})}{\partial D} = \theta_{\text{ON}}^- \begin{bmatrix} \mathbf{0} & \mathbf{A}_{\text{OFF}}(\mathbf{x}) e^{(\theta_{\text{ON}}^- - \theta_{\text{OFF}}(\mathbf{x}))} \mathbf{A}_{\text{OFF}}(\mathbf{x}) \\ -\mathbf{A}_{\text{ON}}(\mathbf{x}) e^{\theta_{\text{OFF}}(\mathbf{x})} \mathbf{A}_{\text{ON}}(\mathbf{x}) & \mathbf{0} \end{bmatrix}. \tag{2.99}$$

The right-hand side of (2.92) differentiated with respect to the duty cycle can be calculated using the following equation:

$$\begin{aligned}
 \frac{\partial \mathbf{q}_{\text{ON/OFF}}(\theta; \mathbf{x})}{\partial D} &= e^{(\theta - \theta_{\text{ON/OFF}}^+(\mathbf{x}))} \mathbf{A}_{\text{ON/OFF}}(\mathbf{x}) \frac{\partial \mathbf{q}(\theta_{\text{ON/OFF}}; \mathbf{x})}{\partial D} \\
 &+ \frac{\partial e^{(\theta - \theta_{\text{ON/OFF}}^+(\mathbf{x}))} \mathbf{A}_{\text{ON/OFF}}(\mathbf{x})}{\partial D} \mathbf{q}(\theta_{\text{ON/OFF}}; \mathbf{x}) + \mathbf{A}_{\text{ON/OFF}}^{-1}(\mathbf{x}) \\
 &\cdot \frac{\partial e^{(\theta - \theta_{\text{ON/OFF}}^+(\mathbf{x}))} \mathbf{A}_{\text{ON/OFF}}(\mathbf{x})}{\partial D} \mathbf{b}(\mathbf{x}) \tag{2.100}
 \end{aligned}$$

where

$$\frac{\partial e^{(\theta - \theta_{\text{ON/OFF}}^+(\mathbf{x}))} \mathbf{A}_{\text{ON/OFF}}(\mathbf{x})}{\partial D} = \begin{cases} \mathbf{0}, & \theta_{\text{ON}}^+ \leq \theta \leq \theta_{\text{OFF}}^- \\ -\theta_{\text{ON}}^- \mathbf{A}_{\text{OFF}}(\mathbf{x}) e^{(\theta - \theta_{\text{OFF}}(\mathbf{x}))} \mathbf{A}_{\text{OFF}}(\mathbf{x}), & \theta_{\text{OFF}}^+ \leq \theta \leq \theta_{\text{ON}}^- \end{cases}. \tag{2.101}$$

The fifth element of (2.92), with respect to D , can be calculated by combining (2.100) at the

angle of maximum output current with the following equation:

$$\begin{aligned}
\frac{\partial \int_{\theta_{\text{ON/OFF}}^+(\mathbf{x})}^{\theta_{\text{OFF/ON}}^-(\mathbf{x})} \mathbf{q}_{\text{ON/OFF}}(\theta; \mathbf{x}) d\theta}{\partial D} = & \pm \theta_{\text{ON}}^- e^{(\theta_{\text{OFF/ON}}^-(\mathbf{x}) - \theta_{\text{ON/OFF}}^+(\mathbf{x}))} \mathbf{A}_{\text{ON/OFF}}(\mathbf{x}) \\
& \cdot \mathbf{q}(\theta_{\text{ON/OFF}}; \mathbf{x}) + \mathbf{A}_{\text{ON/OFF}}^{-1}(\mathbf{x}) \\
& \cdot \left[\left(e^{(\theta_{\text{OFF/ON}}^-(\mathbf{x}) - \theta_{\text{ON/OFF}}^+(\mathbf{x}))} \mathbf{A}_{\text{ON/OFF}}(\mathbf{x}) - \mathbf{I} \right) \right. \\
& \cdot \frac{\partial \mathbf{q}(\theta_{\text{ON/OFF}}; \mathbf{x})}{\partial D} \pm \theta_{\text{ON}}^- \\
& \cdot \left. \left(e^{(\theta_{\text{OFF/ON}}^-(\mathbf{x}) - \theta_{\text{ON/OFF}}^+(\mathbf{x}))} \mathbf{A}_{\text{ON/OFF}}(\mathbf{x}) \mp \mathbf{I} \right) \mathbf{b}(\mathbf{x}) \right].
\end{aligned} \tag{2.102}$$

The partial derivatives in (2.93) with respect to C_p and C_s are given by:

$$\begin{aligned}
\frac{\partial \mathbf{E}(\mathbf{x})}{\partial C_{p/s}} = & \left[\left[\frac{\partial \mathbf{A}_{\text{OFF}}^{-1}(\mathbf{x})}{\partial C_{p/s}} \left(e^{(\theta_{\text{ON}}^- - \theta_{\text{OFF}}(\mathbf{x}))} \mathbf{A}_{\text{OFF}}(\mathbf{x}) - \mathbf{I} \right) \right. \right. \\
& \left[\mathbf{A}_{\text{ON}}^{-1}(\mathbf{x}) \frac{\partial e^{\theta_{\text{OFF}}(\mathbf{x})} \mathbf{A}_{\text{ON}}(\mathbf{x})}{\partial C_{p/s}} \right. \\
& \left. \left. + \mathbf{A}_{\text{OFF}}^{-1}(\mathbf{x}) \frac{\partial e^{(\theta_{\text{ON}}^- - \theta_{\text{OFF}}(\mathbf{x}))} \mathbf{A}_{\text{OFF}}(\mathbf{x})}{\partial C_{p/s}} \right] \mathbf{b}(\mathbf{x}) \right] \\
& \left. + \frac{\partial \mathbf{A}_{\text{ON}}^{-1}(\mathbf{x})}{\partial C_{p/s}} \left(e^{\theta_{\text{OFF}}(\mathbf{x})} \mathbf{A}_{\text{ON}}(\mathbf{x}) - \mathbf{I} \right) \mathbf{b}(\mathbf{x}) \right]
\end{aligned} \tag{2.103}$$

$$\frac{\partial \mathbf{C}(\mathbf{x})}{\partial C_{p/s}} = \begin{bmatrix} \mathbf{0} & -\frac{\partial e^{(\theta_{\text{ON}}^- - \theta_{\text{OFF}}(\mathbf{x}))} \mathbf{A}_{\text{OFF}}(\mathbf{x})}{\partial C_{p/s}} \\ -\frac{\partial e^{\theta_{\text{OFF}}(\mathbf{x})} \mathbf{A}_{\text{ON}}(\mathbf{x})}{\partial C_{p/s}} & \mathbf{0} \end{bmatrix} \tag{2.104}$$

where

$$\frac{\partial \mathbf{A}_{\text{ON/OFF}}^{-1}(\mathbf{x})}{\partial C_{p/s}} = -\mathbf{A}_{\text{ON/OFF}}^{-1}(\mathbf{x}) \frac{\partial \mathbf{A}_{\text{ON/OFF}}(\mathbf{x})}{\partial C_{p/s}} \mathbf{A}_{\text{ON/OFF}}^{-1}(\mathbf{x}). \tag{2.105}$$

The partial derivatives of $\mathbf{A}$ in (2.105) are given by:

$$\frac{\partial \mathbf{A}_{\text{ON/OFF}}(\mathbf{x})}{\partial C_{p/s}} = -\frac{1}{C_{p/s}} \mathbf{J}^{2/6, 2/6} \mathbf{A}_{\text{ON/OFF}}(\mathbf{x}) \tag{2.106}$$

where $\mathbf{J}^{i,j}$ is the single entry matrix where the element $J^{i,j}[i, j]$ is one and the rest are zero.

The right-hand side of (2.95) differentiated with respect to C_p and C_s can be calculated using

the corresponding partial derivatives of (2.72):

$$\begin{aligned}
\frac{\partial \mathbf{q}_{\text{ON/OFF}}(\theta; \mathbf{x})}{\partial C_{p/s}} &= \frac{\partial e^{(\theta - \theta_{\text{ON/OFF}}^+(\mathbf{x})) \mathbf{A}_{\text{ON/OFF}}(\mathbf{x})}}{\partial C_{p/s}} \mathbf{q}(\theta_{\text{ON/OFF}}; \mathbf{x}) \\
&+ e^{(\theta - \theta_{\text{ON/OFF}}^+(\mathbf{x})) \mathbf{A}_{\text{ON/OFF}}(\mathbf{x})} \frac{\partial \mathbf{q}(\theta_{\text{ON/OFF}}; \mathbf{x})}{\partial C_{p/s}} + \left[\frac{\partial \mathbf{A}_{\text{ON/OFF}}^{-1}(\mathbf{x})}{\partial C_{p/s}} \right. \\
&\cdot \left(e^{(\theta - \theta_{\text{ON/OFF}}^+(\mathbf{x})) \mathbf{A}_{\text{ON/OFF}}(\mathbf{x})} - \mathbf{I} \right) + \mathbf{A}_{\text{ON/OFF}}^{-1} \\
&\cdot \left. \frac{\partial e^{(\theta - \theta_{\text{ON/OFF}}^+(\mathbf{x})) \mathbf{A}_{\text{ON/OFF}}(\mathbf{x})}}{\partial C_{p/s}} \right] \mathbf{b}(\mathbf{x}). \tag{2.107}
\end{aligned}$$

The fifth element of (2.92), with respect to $C_{p/s}$, can be calculated by combining (2.107) at the angle of maximum output current with the following equation:

$$\begin{aligned}
\frac{\partial \int_{\theta_{\text{ON/OFF}}^+(\mathbf{x})}^{\theta_{\text{OFF/ON}}^-(\mathbf{x})} \mathbf{q}_{\text{ON/OFF}}(\theta; \mathbf{x}) d\theta}{\partial C_{p/s}} &= \frac{\partial \mathbf{A}_{\text{ON/OFF}}^{-1}(\mathbf{x})}{\partial C_{p/s}} \mathbf{A}_{\text{ON/OFF}}(\mathbf{x}) \\
&\cdot \int_{\theta_{\text{ON/OFF}}^+(\mathbf{x})}^{\theta_{\text{OFF/ON}}^-(\mathbf{x})} \mathbf{q}_{\text{ON/OFF}}(\theta; \mathbf{x}) d\theta \\
&+ \mathbf{A}_{\text{ON/OFF}}^{-1}(\mathbf{x}) \left\{ \left[\frac{\partial \mathbf{A}_{\text{ON/OFF}}^{-1}(\mathbf{x})}{\partial C_{p/s}} \right. \right. \\
&\cdot \left(e^{(\theta_{\text{OFF/ON}}^-(\mathbf{x}) - \theta_{\text{ON/OFF}}^+(\mathbf{x})) \mathbf{A}_{\text{ON/OFF}}(\mathbf{x})} - \mathbf{I} \right) \\
&+ \mathbf{A}_{\text{ON/OFF}}^{-1}(\mathbf{x}) \\
&\cdot \left. \frac{\partial e^{(\theta_{\text{OFF/ON}}^-(\mathbf{x}) - \theta_{\text{ON/OFF}}^+(\mathbf{x})) \mathbf{A}_{\text{ON/OFF}}(\mathbf{x})}}{\partial C_{p/s}} \right] \mathbf{b}(\mathbf{x}) \\
&+ \frac{\partial e^{(\theta_{\text{OFF/ON}}^-(\mathbf{x}) - \theta_{\text{ON/OFF}}^+(\mathbf{x})) \mathbf{A}_{\text{ON/OFF}}(\mathbf{x})}}{\partial C_{p/s}} \\
&\cdot \mathbf{q}(\theta_{\text{ON/OFF}}; \mathbf{x}) \\
&+ \left(e^{(\theta_{\text{OFF/ON}}^-(\mathbf{x}) - \theta_{\text{ON/OFF}}^+(\mathbf{x})) \mathbf{A}_{\text{ON/OFF}}(\mathbf{x})} - \mathbf{I} \right) \\
&\cdot \left. \frac{\partial \mathbf{q}(\theta_{\text{ON/OFF}}; \mathbf{x})}{\partial C_{p/s}} \right\}. \tag{2.108}
\end{aligned}$$

The partial derivatives of the Jacobian components in (2.92) that cannot be directly computed,

i.e. the exponential derivatives in (2.103), (2.104), (2.107) and (2.108) with respect to C_p and C_s , can be calculated by any combination of the methods described in [85, 86]. The method described in [85] uses the complex step derivative approach and is simpler to implement as well as less computationally demanding compared to the one in [86]. However, the approach of [86], which is based on matrix diagonalisation, provides a better insight on the actual analytic equation of the derivative. We provide bellow the exact equations of these terms for both approaches, where the subscripts “ CS ” and “ MD ” denote the complex step and the matrix diagonalisation derivatives, respectively:

$$\left. \frac{\partial_{CS} e^{(\theta - \theta_{\text{ON/OFF}}^+(\mathbf{x})) \mathbf{A}_{\text{ON/OFF}}(\mathbf{x})}}{\partial C_{p/s}} \right|_{\mathbf{x}=\mathbf{x}^{(m)}} = \frac{\text{Im} \left(e^{(\theta - \theta_{\text{ON/OFF}}^+(\mathbf{x}^{(k)})) \mathbf{A}_{\text{ON/OFF}}(\mathbf{x}^{(m)} + j h \mathbf{e}_{1/4})} \right)}{h}, \quad (2.109)$$

$$\frac{\partial_{MD} e^{(\theta - \theta_{\text{ON/OFF}}^+(\mathbf{x})) \mathbf{A}_{\text{ON/OFF}}(\mathbf{x})}}{\partial C_{p/s}} = \mathbf{X}_{\text{ON/OFF}}(\mathbf{x}) \mathbf{V}_{p/s}^{\text{ON/OFF}}(\mathbf{x}; \theta) \mathbf{X}_{\text{ON/OFF}}^{-1}(\mathbf{x}) \quad (2.110)$$

where j is the imaginary unit and h is an infinitesimal positive number [85]. $\mathbf{X}_{\text{ON/OFF}}$ is the matrix whose i^{th} column is a right eigenvector corresponding to the eigenvalue $d_i^{\text{ON/OFF}}$ of $\mathbf{A}_{\text{ON/OFF}}$:

$$\mathbf{A}_{\text{ON/OFF}}(\mathbf{x}) = \mathbf{X}_{\text{ON/OFF}}(\mathbf{x}) \mathbf{D}_{\mathbf{A}}^{\text{ON/OFF}}(\mathbf{x}) \mathbf{X}_{\text{ON/OFF}}^{-1}(\mathbf{x}) \quad (2.111)$$

$$\mathbf{D}_{\mathbf{A}}^{\text{ON/OFF}}(\mathbf{x}) = \text{diag} \left(d_1^{\text{ON/OFF}}(\mathbf{x}), \dots, d_6^{\text{ON/OFF}}(\mathbf{x}) \right) \quad (2.112)$$

where $\mathbf{X}_{\text{ON/OFF}}$ and $\mathbf{D}_{\mathbf{A}}^{\text{ON/OFF}}$ can be calculated using the QZ decomposition method [87]. The individual entries of $\mathbf{V}_{p/s}^{\text{ON/OFF}}$ are given by:

$$V_{p/s}^{\text{ON/OFF}}[i, j](\mathbf{x}; \theta) = \begin{cases} G_{p/s}^{\text{ON/OFF}}[i, j](\mathbf{x}) \left(e^{(\theta - \theta_{\text{ON/OFF}}^+(\mathbf{x})) d_i^{\text{ON/OFF}}(\mathbf{x})} - e^{(\theta - \theta_{\text{ON/OFF}}^+(\mathbf{x})) d_j^{\text{ON/OFF}}(\mathbf{x})} \right) / \left(d_i^{\text{ON/OFF}}(\mathbf{x}) - d_j^{\text{ON/OFF}}(\mathbf{x}) \right), & i \neq j \\ G_{p/s}^{\text{ON/OFF}}[i, i](\mathbf{x}) \left(\theta - \theta_{\text{ON/OFF}}^+(\mathbf{x}) \right) \cdot e^{(\theta - \theta_{\text{ON/OFF}}^+(\mathbf{x})) d_i^{\text{ON/OFF}}(\mathbf{x})}, & i = j \end{cases} \quad (2.113)$$

where

$$\mathbf{G}_{p/s}^{\text{ON/OFF}}(\mathbf{x}) = \mathbf{X}_{\text{ON/OFF}}^{-1}(\mathbf{x}) \frac{\partial \mathbf{A}_{\text{ON/OFF}}(\mathbf{x})}{\partial C_{p/s}} \mathbf{X}_{\text{ON/OFF}}(\mathbf{x}). \quad (2.114)$$

2.5.5 Inverter Design Examples

Class EF₂ Tuning Example

In this subsection we further improve the numerical example of the Class EF₂ inverter presented in subsection 2.4.4 of this work by using the SS formulation. The additional inputs needed for the computational process, to the ones given in Table 2.1, as well as the resulting adjusted component values with their relative change to the previous tuning step, are given in Table 2.2. The inductance of the choke [88] was measured using the method described in subsection 2.4.4 at f_S and its series resistance was measured with a multimeter (Keysight 34465A Digital Multimeter), since the input current is mostly DC. Based on the peak of the drain voltage and current waveforms in Figure. 2.3 as well as the switching frequency requirements, the switching device of choice is the GS66504B from GaN Systems [89], which is where the ON and OFF resistances in Table 2.2 were derived from. The value of p_ϕ was based on the properties of the air-core inductors [90] at $\tau_\phi f_S$ used in the ϕ -branch, since the requirement of the combination of the relatively low inductance with low HF Q makes cored inductors unsuitable for this application [27]. The waveforms of the improved design are shown in Figure. 2.7 displayed in solid line, compared to the ones from the FO tuning method, shown with dashed lines. It is clear from Table 2.3 that after the SS tuning procedure improvement, the operating conditions described in (2.84) are met.

In this example, we calculated (2.89) numerically and used the pure Newton version of (2.90). For the Jacobian computation we implemented the approach in (2.109). The iterative progression of the solution convergence of (2.84) is shown in Figure 2.8 and the final conditions that terminated the iteration, along with the corresponding algorithm parameters, are given in Table 2.3. Apart from I_m , which was calculated in the previous tuning step, the choice of the component values in Table 2.2 are based on their experimental measurements and datasheets.

Class Φ_2 Tuning Example

As mentioned in the Introduction, in this section we show the design of a Class Φ_2 inverter in order to demonstrate the versatility and the design possibilities that the proposed SS tuning method can provide. In the previous numerical example in subsection 2.5.5, the inductance of

Table 2.3: State space tuning algorithm parameters and outputs

	Quantity	Value	Unit
Parameters	N	1000	points
	γ	1	—
	a_N	1	—
	a_{GD}	0	—
	ϵ	10^{-6}	—
	h	10^{-20}	—
EF_2	$ v_{C_p}(\theta_{ON}) $	0.253	nV
	$ i_{C_p}(\theta_{ON}^-) - i_S^{ON} $	0.128	nA
	$ \max(i_{L_{s1}}) - I_m $	0.912	nA
	$i_{L_{s1}}^{DC}$	40.864	μA
	$\left \frac{\max(i_{L_{s1}})}{I_{L_{rfc}}} - \lambda \right $	2.284×10^{-10}	—
Φ_2	$ v_{C_p}(\theta_{ON}) $	52.03	pV
	$ i_{C_p}(\theta_{ON}^-) - i_S^{ON} $	97.158	pA
	$ \max(i_{L_{s1}}) - I_m $	0.211	nA
	$i_{L_{s1}}^{DC}$	27.061	μA
	$\left \frac{\max(i_{L_{s1}})}{I_{L_{rfc}}} - \lambda \right $	3.57×10^{-12}	—

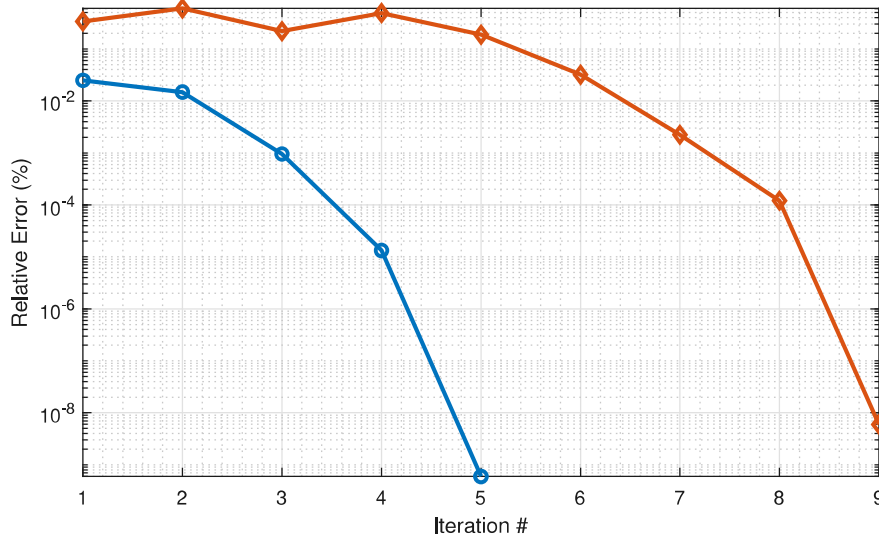


Figure 2.8: Convergence progression of (2.91). The blue circles correspond to the Class EF_2 and the orange diamonds to the Class Φ_2 inverter examples presented in this paper.

the input choke is large enough so that its involvement on the resonance of the rest of the circuit is minimal around f_S which is confirmed by the small amplitude of the AC compared to the DC part of the input current waveform. However, by reducing the value of the choke inductance, relative to the inverter input resistance, we get closer to the Class Φ_2 operation. Compared

to the Class EF inverter, the Class Φ inverter has higher limits of operating frequency, since reducing the input choke results in higher values of shunt capacitance, for a given inverter design. In addition, lower input choke inductance values can results in more compact circuits.

The inputs and outputs for the Class Φ_2 inverter design example are given in Table 2.4, in addition to the component values required from Table 2.1 and Table 2.2. Here, the impedance of the input choke is half of the input resistance and the condition for infinite input choke operation in (2.53) does not apply. The algorithm parameters used for this example are the same with the ones in subsection 2.5.5 and are given in Table 2.3. The progress of the convergence procedure is shown in Figure 2.8. The FO inverter design that is used as an initial point for the iterative process is again the one mentioned in subsection 2.4.4. The waveforms of the SS variables in Figure 2.6 before and after the application of the SS tuning method are shown in Figure 2.9.

Table 2.4: Inputs and outputs of state space Class Φ_2 tuning example

	Quantity	Value	Unit
Inputs*	L_{rfc}	600	nH
Outputs	V_{in}	77.068	V
	D	20.817	%
	C_p	515.532	pF
	C_s	142.641	pF
Relative Change	$\delta(V_{in})$	-2.368	%
	$\delta(D)$	-30.61	%
	$\delta(C_p)$	125.152	%
	$\delta(C_s)$	-5.107	%

*The inputs given in this table are in addition to the data of Table 2.1 and Table 2.2.

As expected, the FO method is even more inaccurate when using a finite input choke, since it is based on an infinite input choke assumption. This limitation is reflected in the difference of the waveforms shapes before and after tuning in Figure 2.9 as well as the mismatch of the corresponding parts of Figure 2.3 and Figure 2.9. Also, the tuning process was slower compared to the Class EF₂, as shown in Figure 2.8, mostly because the FO initial point of the iterative method is by definition less suitable for the Class Φ inverter design. However the algorithm still manages to produce an inverter design that complies with (2.84), which can be proven from Table 2.3.

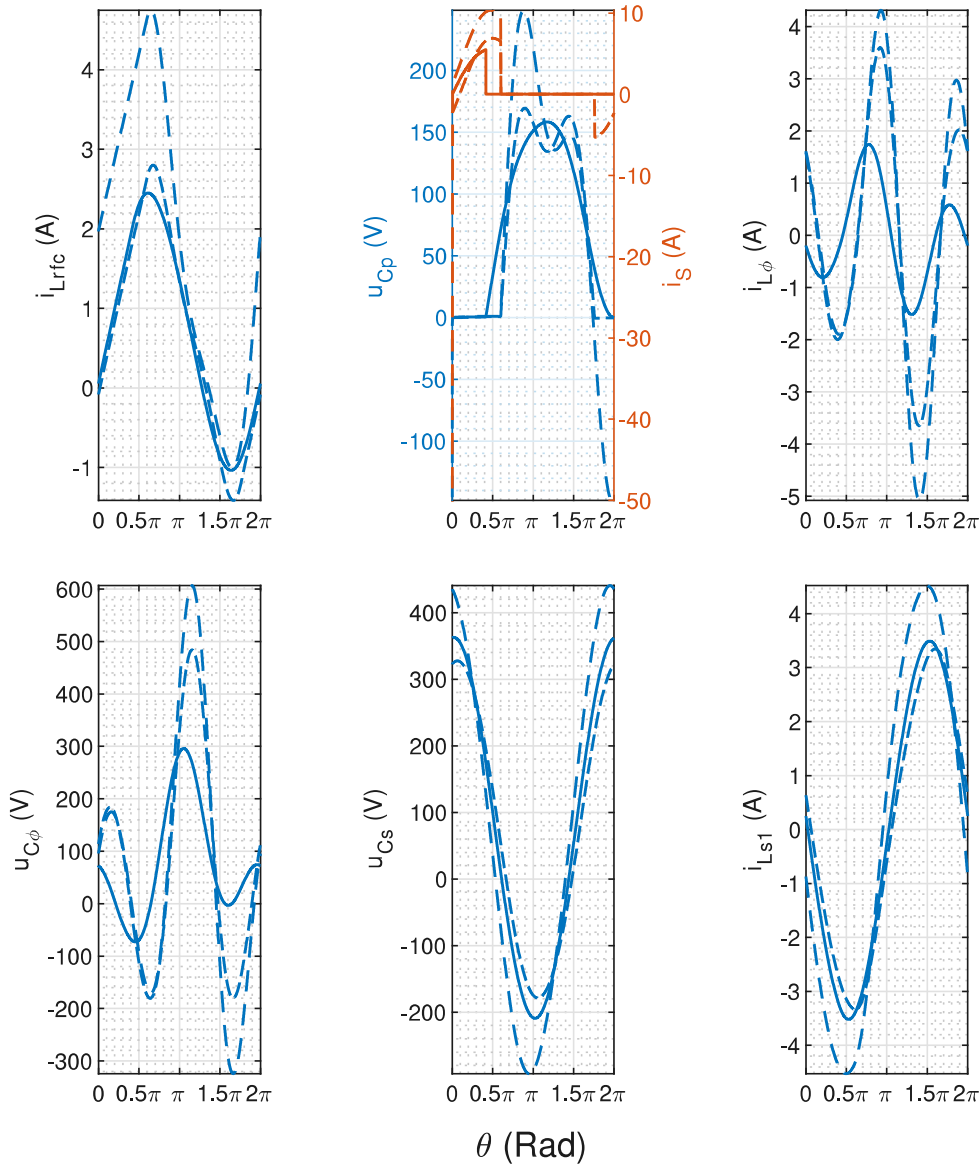


Figure 2.9: Simulation of the Class Φ_2 inverter waveforms using state-space formulation. The dashed line is used to represent the design that occurs from the FO tuning method, the dashed-dotted line shows the FO design with an antiparallel diode incorporated into the device and the solid line shows the state-space tuned inverter. The negative limit of the i_s overshoot in the graph is not shown to its full amplitude for improved readability and scaling, since it doesn't provide any meaningful information.

A comment that could be made is that for the Class Φ inverter designs, it would be more suitable to use the RMS formula in (2.87), instead of the DC, since the AC component in the input current is not negligible anymore. Actually, the RMS value of the input current would be the generally most applicable measure, but it would complicate the computation for the Jacobian even more. However, that part of (2.84) mostly affects the value of C_s , and by comparing the capacitor values in Table 2.2 and Table 2.4, we see a difference that is practically

not important.

Class EF₂ Reduced Tuning Example

As mentioned in subsection 2.5.3, we can alternatively apply a reduced version of tuning process in the SS part of the design algorithm. The difference between the complete and the reduced version is that the latter does not further adjust C_{s1} from the FO step and does not incorporate the input condition for λ . As an example, we apply this design approach to a 150 W 13.56 MHz Class EF₂ inverter based on the equivalent experimental setup in [1].

The inputs and outputs of the FO tuning step are given in Table 2.5, and the corresponding waveforms both in FO and SS simulation are given Figure 2.10. Again, although the FO simulation in Figure 2.10 seems to successfully apply the input conditions, the more accurate SS simulation of the FO design reveals that neither the soft switching nor the power and loading conditions are met.

Table 2.5: Inputs and outputs of first order reduced tuning example

	Quantity	Value	Unit
Inputs	P_o	150	W
	τ_ϕ	2	—
	λ	5	—
	i_S^{ON}	0	A
	R_{sL}	6	Ω
	L_{s1}	1.14	μH
	f_S	13.56	MHz
	D	30	%
	Boundaries	$\{i_\phi, v_{C_\phi}\}$	—
Outputs	V_{in}	106.066	V
	C_p	328.19	pF
	L_ϕ	91.935	nH
	C_ϕ	374.61	pF
	C_s	150.68	pF

Then, we apply the reduced SS tuning to the output of the FO design of Table 2.5, by using the parameters in Table 2.3. The component values and the waveforms of the reduced SS optimised inverter are given in Table 2.6 and Figure 2.11, respectively. The SS design does maintain both voltage and current soft switching conditions, while delivering the desired output power to the

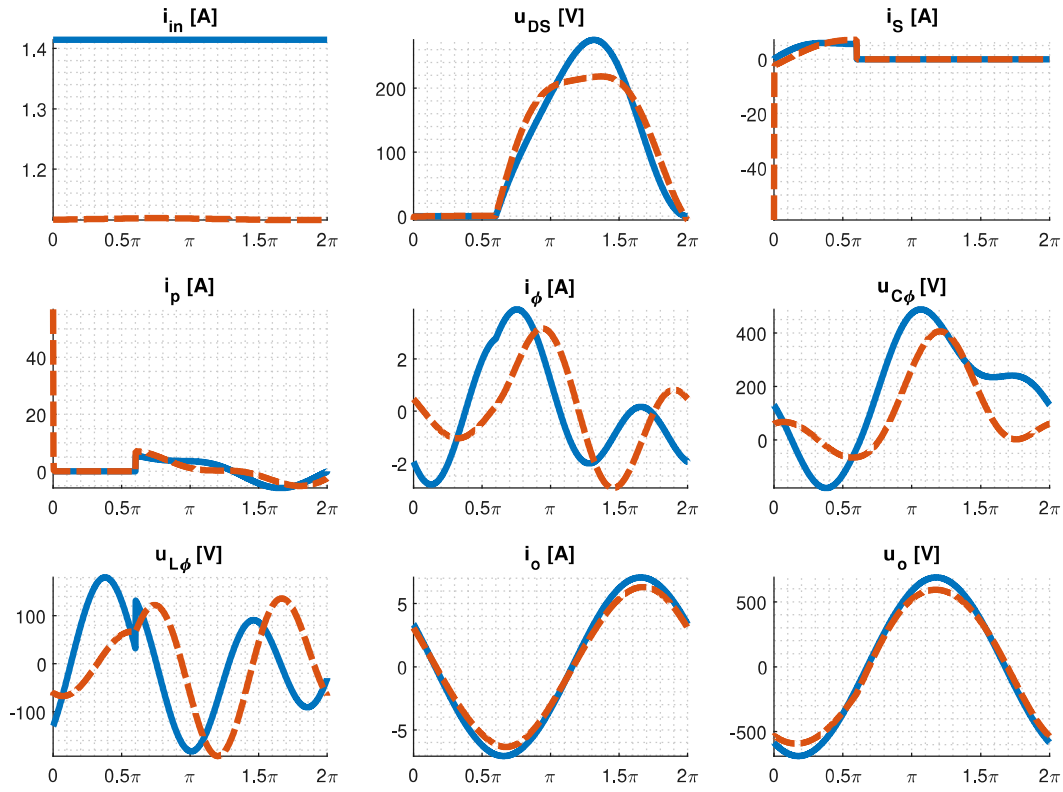


Figure 2.10: Comparison between first order waveforms calculation (solid blue line) and state space solution (dashed orange line) using the components derived from the first order analysis.

load with low output THD, as can be confirmed by the shape of v_{DS} and i_S , and the amplitude and shape of i_o in Figure 2.11. The THD is quantified experimentally in section 2.8. However, the DC to AC current gain of the output design is higher than expected, since $\lambda \approx 5.7$, which is the predicted shortcoming of the reduced tuning method. It must also be noted that it took 5 iterations for the algorithm to converge, same as the complete Class EF_2 example, which is expected since fundamentally the two inverters do not differ significantly.

2.5.6 A Note on Load-Independent Operation

In this work, the circuit design conditions that we choose to incorporate are focused on direct low level waveform shaping as shown in (2.84), instead of more abstract properties. We prefer this approach because it is more general and produces greater variety and control over the behaviour of the resulting circuits.

Table 2.6: Inputs and outputs of state space Class EF₂ reduced tuning example

	Quantity	Value	Unit
Inputs*	I_m	7.701	A
	L_{rfc}	1	mH
	R_S^{ON}	100	m Ω
	R_S^{OFF}	650	M Ω
Outputs	V_{in}	122.869	V
	D	24.28	%
	C_p	359.267	pF
Relative Change	$\delta(V_{in})$	15.842	%
	$\delta(D)$	-19.067	%
	$\delta(C_p)$	9.469	%
Termination Limit	$ v_{C_p}(\theta_{ON}) $	146.4	pV
	$ i_{C_p}(\theta_{ON}^-) - i_S^{ON} $	261.87	pA
	$ \max(i_{L_{s1}}) - I_m $	-5.699	nA
	$i_{L_{s1}}^{DC}$	-73.19	μ A

*The inputs given in this table are in addition to the data of Table 2.5.

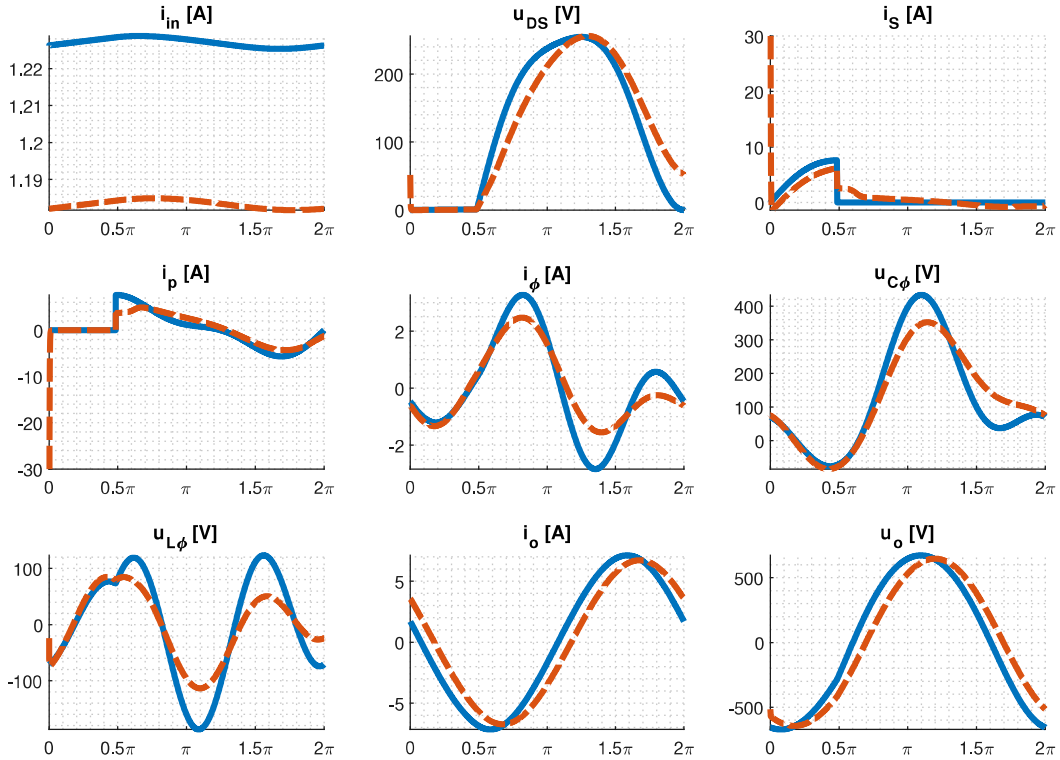


Figure 2.11: Comparison between the iteratively optimised state space solution (solid blue line) and the same circuit with the inclusion of a voltage dependent switch capacitor (dashed orange line).

Such example of a more complex design property is the load-independent operation mentioned in [1], where the FO design equations are used to mathematically produce the formulation of the invariance of some specific waveforms over changes in the resistive reflected load. However, the FO approach, apart from the accuracy issues it inherently has as shown in Figure 2.7, it is also not convenient for the direct computation of the partial derivatives with respect to the reflected load that are required.

The above mentioned shortcomings of the FO equations for achieving Load Independent Class EF/ Φ inverter designs can be overcome by using the SS tuning method we propose in this section. One possible way of defining the load independent conditions, i.e. ZVS and constant output current respectively, is given below:

$$\left. \frac{\partial v_{C_p}(\theta_{\text{OFF}}; \mathbf{x})}{\partial R_L} \right|_{R_L \in [0, R_L^{\text{max}}]} = 0, \quad (2.115)$$

$$\left. \frac{\partial}{\partial R_L} \int_{\theta_{\text{ON}}^+}^{\theta_{\text{ON}}^-} i_{L_{s1}}^2(\theta; \mathbf{x}) d\theta \right|_{R_L \in [0, R_L^{\text{max}}]} = \frac{\theta_{\text{ON}}^- I_m}{\sqrt{2}}. \quad (2.116)$$

The partial derivatives in (2.115) and (2.116) and their respective terms in the Jacobian can be calculated according to subsection 2.5.4. However, in order to ensure convergence of the iterative tuning algorithm, similar adjustments in the selection of the tuning parameters in (2.85) must also be made. Nonetheless, this kind of investigation is beyond the scope of this paper and could be implemented as possible future work.

2.5.7 Simulation of the Device Anti-parallel Diode

As shown in Figure 2.7 and Figure 2.9, simulating the circuit in Figure 2.6 using (2.72) and (2.73) doesn't incorporate the effect of the reverse conducting diode, which is an intrinsic property of power MOSFETs [91] and HEMTs [89], since the device is blocking both positive and negative current when turned off. The impact of the antiparallel diode to the behaviour of the circuit can be included by adding to the a priori known switching boundary conditions in (2.73) the points in time where v_{C_p} changes polarity during turn-off. However, the process of figuring out the parts of the period during which the reverse diode is conducting is not straight forward and requires a dynamic calculation approach. In this subsection, we propose

an iterative scheme, which is broken down in the flowchart in Figure 2.12, for the calculation of the time points within a period where the reverse diode turns on and off.

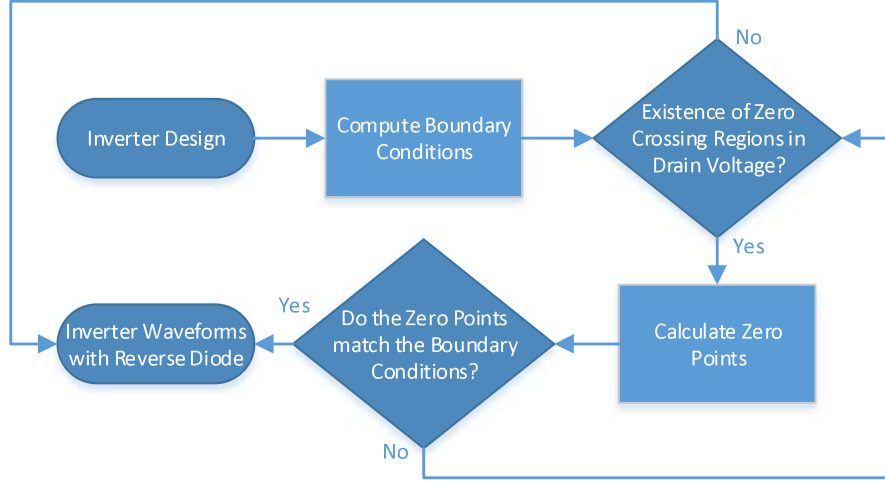


Figure 2.12: Flowchart of the algorithm proposed in subsection 2.5.7 for simulating the effect of the intrinsic reverse conducting diode of the switching device to the waveforms of the Class EF/ Φ inverter using the state space formulation.

The algorithm begins by setting the inverter design with the corresponding component values and computing the state vector waveforms, as described in subsection 2.5.2. The next step involves figuring out whether and when the drain voltage during turn-off changes polarity. Solving for the zeros of v_{C_p} is achieved first by splitting the waveform in a predefined number of equal pieces and checking forward in time if the boundaries of a part have opposing signs. If a waveform part crosses zero, we solve for that point using the Two-Point Newton method in [92], starting the iteration from the edge points. If, however, no such point exists in the entirety of the drain voltage during turn-off, the reverse diode is not conducting and the simulation process is terminated. Once we have solved for all the potential zero crossing points with the current boundary conditions, we readjust the boundary conditions accordingly for the next iteration. At every boundary condition, the conducting state of the device is switched.

The iterative process has converged once the boundary conditions have reached a steady equilibrium. One way to express this can be by:

$$\left\| \boldsymbol{\theta}_S^{(m+1)} - \boldsymbol{\theta}_S^{(m)} \right\|_{\infty} < \epsilon \quad (2.117)$$

where $\boldsymbol{\theta}_S$ is the vector with the boundary points in angular time and ϵ is the tolerance, given that the two vectors have the same dimension. The length of $\boldsymbol{\theta}_S$ is n , $\theta_1 = 0$ and $\theta_n = \theta_{\text{OFF}}$. Another way to set the termination condition without the requirement of the consecutive boundary points vectors having the same length is by using the normwise backward error for linear equations [93]:

$$\frac{\|\mathbf{d} - \mathbf{A}_{n-1}\mathbf{c}\|_\infty}{\|\mathbf{A}_{n-1}\|_\infty \|\mathbf{c}\|_1 + \|\mathbf{d}\|_\infty} < \epsilon, \quad (2.118)$$

where

$$\mathbf{c} = \mathbf{q}(\theta_1) - e^{(\theta_n - \theta_{n-1})\mathbf{A}_{n-1}} \mathbf{q}(\theta_{n-1}), \quad (2.119)$$

$$\mathbf{d} = (e^{(\theta_n - \theta_{n-1})\mathbf{A}_{n-1}} - \mathbf{I}) \mathbf{b}. \quad (2.120)$$

As an example for the demonstration of the algorithm in Figure 2.12 we use the FO design with finite choke of subsection 2.5.5, since the diode conduction part of the period is substantially larger compared to the corresponding Class EF₂ design. We used the condition in (2.117) for termination with tolerance 10^{-6} . The resulting waveforms are shown in Figure 2.9 and it took 4 iterations for the scheme in Figure 2.12 to converge. The need for the iterative scheme in order to determine the reverse diode conducting regions becomes clear from Figure 2.9, since the actual point in time that the antiparallel diode of the device begins to conduct does not match exactly the zero crossing point of the non diode drain waveform.

2.6 Tuning with a Non-Linear Device

2.6.1 Background

In section 2.4 and section 2.5 we simulate the device behaviour as an ideal switch and a variable resistor, respectively. However, power MOSFETs have non-linear parasitic capacitances [91] which not only introduce delays but also, specifically C_{oss} for the cases of Class E [59] and Class EF inverters [60], are part of the shunt resonant network and their effect should be taken into account in the tuning calculations in order to get accurate results. As we've already shown in section 2.5, the FO approach is not suitable for Class EF/ Φ inverter designs, which means that the method proposed in [59] is not ideal for this case, and [60] is based on manual tuning and fitting of the waveforms along with experimental measurements. A numerical design

procedure for Class E inverters at 50% duty cycle is presented in [44], however it is not directly applicable to Class EF inverters. If a detailed and extensive model of the parasitics of the device is not available, the iterative tuning method in our previous work [61] is a powerful option. However it doesn't incorporate the gate drive signal in the calculations and focuses only on maintaining ZVS, while the other properties of the circuit may be altered during the tuning process.

In this section we propose an iterative tuning method, that will further adjust the design produced in section 2.5 so that it absorbs the unwanted effects of the device parasitics and the non-ideal gate drive signal, while maintaining all the required input design properties. The circuit model of the device as well as the simulation equations derived in this section are generally applicable to any transistor. The same applies to the tuning methodology proposed, which is universal. However, since we are dealing with non-linear effects uniquely defined by the specific semiconductor device used, the exact functions of the parasitics behaviour need to be defined accordingly for each individual transistor model.

2.6.2 System Modelling

The circuit diagram of the Class EF inverter topology that is used for simulation in this chapter is, for the most part, the one shown in Figure 2.6 with a different, more thorough and realistic, transistor model. The switching device [89] is modelled as a non-linear voltage-dependent current source along with a network of non-linear voltage-dependent capacitances [94, 95, 10] and temperature-dependent resistors, as shown in Figure 2.13. The stray inductances caused by the packaging of the device are incorporated in the computations as inductors at the pins of the device.

Since the three capacitors in Figure 2.13 form a delta network, only the voltages across two of them are considered independent SS variables. In this work we choose $v_{C_{gd}}$ to be the dependent one, which is related to the other two device capacitor voltages by the relation:

$$v_{C_{gd}}(\theta) = v_{C_{gs}}(\theta) - v_{C_{ds}}(\theta). \quad (2.121)$$

The same principle applies for the currents through the package inductances, which form a star network connected at a hypernode. The dependent variable of choice is i_{L_s} , which is given by

the relation:

$$i_{L_s}(\theta) = i_{L_g}(\theta) + i_{L_d}(\theta). \quad (2.122)$$

In line with (2.68), applying KVL and KCL to the inverter with the non-linear device model in Figure 2.13 leads to the non-linear 10th order differential equation of the system given below:

$$\omega \mathbf{M}(\mathbf{v}) \frac{d\mathbf{v}(\theta)}{d\theta} = \mathbf{U}(\mathbf{v}, v_{GS}, T) \mathbf{v}(\theta) + \mathbf{e}_1 V_{in} + \mathbf{n} v_{GS}(\theta) + \mathbf{m}(\mathbf{v}) i_S(\mathbf{v}, T) \quad (2.123)$$

where T is the temperature of the device and

$$\mathbf{U} = \begin{bmatrix} -R_{rfc} & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & -1 & 0 & 0 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & -R_\phi & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & -1 & -R_{sL} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 & 0 & 0 & -n_{ds}R_s - (n_{ds} + 1)R_{gate} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & n_{gs} + 1 & 0 & 0 & 0 & 0 & R_{gate} - n_{gs}R_s & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & m_{ds} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ & & & & & & & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ & & & & & & & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ & & & & & & & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ & & & & & & & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ & & & & & & & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ & & & & & & & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ & & & & & & & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ & & & & & & & -n_{gs}(R_d + R_s) - R_d & 1 & -n_{gs} - 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ & & & & & & & -m_{dg} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ & & & & & & & m_{gs} & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \quad (2.124)$$

$$\mathbf{v} = \begin{bmatrix} i_{L_{rfc}} & v_{C_p} & i_{L_\phi} & v_{C_\phi} & v_{C_s} & i_{L_{s1}} & i_{L_g} & i_{L_d} & v_{C_{gs}} & v_{C_{ds}} \end{bmatrix}^T \quad (2.125)$$

$$\mathbf{M}(\mathbf{v}) = \text{diag}(L_{rfc}, C_p, L_\phi, C_\phi, C_s, L_{s1}, L_{gds}, L_{gds}, C_{gds}(\mathbf{v}), C_{gds}(\mathbf{v})) \quad (2.126)$$

$$\mathbf{n} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & n_{ds} + 1 & -1 & 0 & 0 \end{bmatrix}^T \quad (2.127)$$

$$\mathbf{m}(\mathbf{v}) = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & m_{dg}(\mathbf{v}) & -m_{gs}(\mathbf{v}) \end{bmatrix}^T \quad (2.128)$$

$$L_{gds} = (n_{ds} + 1) L_g + L_d \quad (2.129)$$

$$C_{gds}(\mathbf{v}) = m_{gs}(\mathbf{v}) \frac{\partial Q_{C_{ds}}(\mathbf{v})}{\partial u_{C_{ds}}} + \frac{\partial Q_{C_{gs}}(\mathbf{v})}{\partial u_{C_{gs}}} + \frac{\partial Q_{C_{gs}}(\mathbf{v})}{\partial u_{C_{ds}}} \quad (2.130)$$

$$n_{gs} = \frac{L_g}{L_s} \quad (2.131)$$

$$n_{ds} = \frac{L_d}{L_s} \quad (2.132)$$

$$R_{\text{gate}}(v_{GS}) = R_G(v_{GS}) + R_g \quad (2.133)$$

$$m_{ds}(\mathbf{v}) = \frac{\partial_{u_{C_{ds}}} Q_{C_{ds}}(\mathbf{v})}{\partial_{u_{C_{gd}}} Q_{C_{gd}}(\mathbf{v})} + 1 \quad (2.134)$$

$$m_{dg}(\mathbf{v}) = \frac{\partial_{u_{C_{ds}}} Q_{C_{gs}}(\mathbf{v})}{\partial_{u_{C_{gd}}} Q_{C_{gd}}(\mathbf{v})} - 1 \quad (2.135)$$

$$m_{gs}(\mathbf{v}) = \frac{\partial_{u_{C_{gs}}} Q_{C_{gs}}(\mathbf{v})}{\partial_{u_{C_{gd}}} Q_{C_{gd}}(\mathbf{v})} + 1. \quad (2.136)$$

$Q_{C_{gs}}$, $Q_{C_{ds}}$ and $Q_{C_{gd}}$ are the electrical charges in of the corresponding capacitors of the circuit in Figure 2.13 and R_G is the resistance for shaping the rise and fall of the gate signal of the switching device.

The input gate signal is determined by the characteristics of gate driver circuit used in the experimental setup, which in our case is [96], and is modelled as an ideal pulse wave:

$$v_{GS}(\theta) = \begin{cases} 5 \text{ V}, & 0 \leq \theta < \theta_{\text{OFF}} \\ 0 \text{ V}, & \theta_{\text{OFF}} \leq \theta < \theta_{\text{ON}}^- \end{cases} \quad (2.137)$$

The above mentioned choice of gate driver may not be ideal efficiency-wise for this switching device because, according to [89], the lowest $R_{DS(\text{on})}$ is achieved at 6 V and the bias voltage during turn-off can be as low as -3 V . However, the main purpose of this work is to demonstrate the accuracy of the proposed modelling and optimisation techniques under given operating conditions, hence the choice of optimal components is beyond the scope of our study.

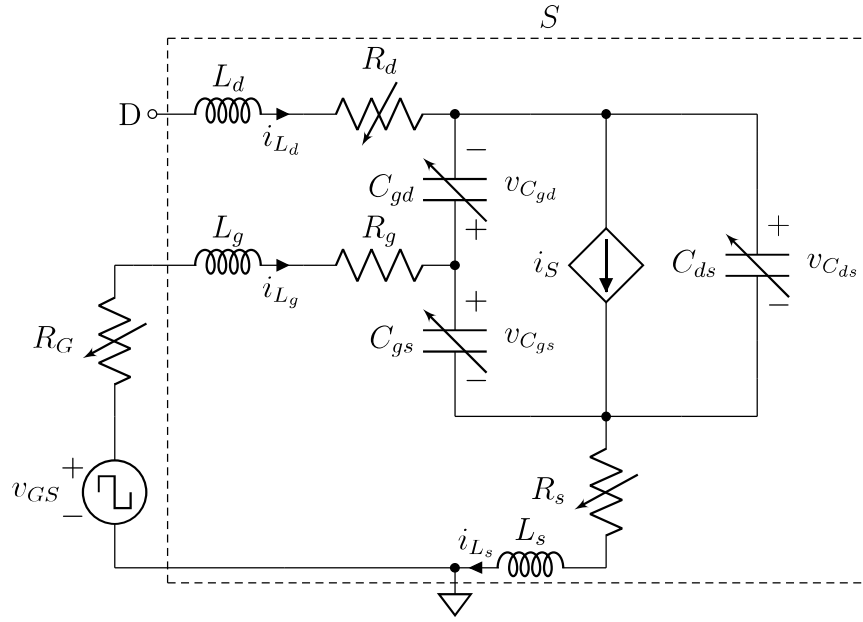


Figure 2.13: Circuit diagram of a non-linear model of the switching device in the Class EF/ Φ inverter, including parasitic capacitances and resistances, stray package inductances and input gate signal with ON/OFF resistors.

The effect of the temperature on the device operation was emulated by the internal drain and source temperature dependent resistances $R_{d/s}(T)$, which are modelled using the linear FO approximation [97]. The equations of the capacitances and the current source in Figure 2.13 are defined based on the small signal and DC MOSFET models described in [98]. The fitting of the drain and source resistances, the drain current, and the internal capacitors of the device on the datasheet curves was performed using the Levenberg-Marquardt damped least-squares method, described in [99] combined with information from reverse engineering the LTspice model provided by the manufacturer. The exact details of applying the fitting algorithm are skipped, since it is a complicated procedure very specific to our case study and with little potential for generalisation and out of the scope of the inverter design method.

A demonstration of the visual fitting and comparison between some specially selected data from the datasheet measurements of the device [89] and the above mentioned internal device component models is given in Figure 2.14. The chosen data curves are the ones quantitatively closest to our case study. The numerical values of metrics for the evaluation of the accuracy of fitting are shown in Table 2.7. Specifically, the Mean Absolute Error (MAE), which represents the average of the absolute difference between the actual and predicted values in the data set, the Mean Squared Error (MSE) which represents the average of the squared difference between the original and predicted values in the data set and the Root Mean Squared Error (RMSE)

which measures the standard deviation of residuals [100], have been calculated. A more detailed investigation of C_{oss} losses in a device level approach is presented in [54, 101], however such characterisation is beyond the scope of this work and this kind of behaviour could further enrich the data in Figure 2.14 to produce even more accurate transistor models.

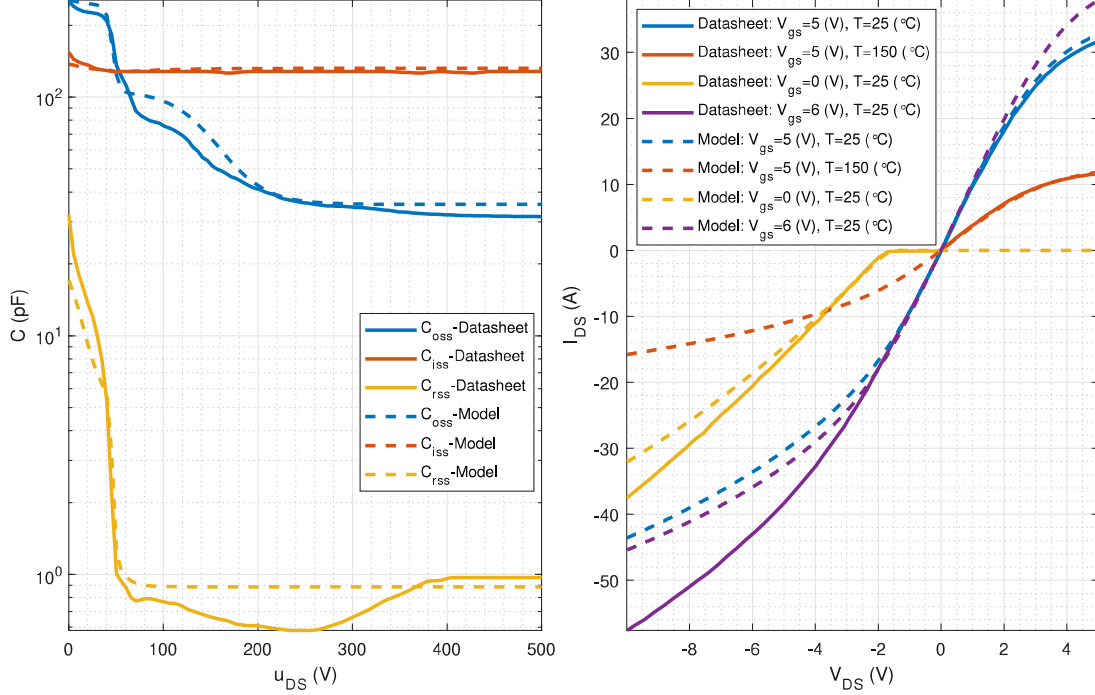


Figure 2.14: Visual comparison of the dependence of the internal non-linear capacitances (left) and the drain current (right) on the drain voltage between the datasheet and the fitted model curves. For the case of the drain current, the choice of gate bias and temperature were chosen so that they reflect as closely as possible the numerical example of our experimental setup operation. For the top graph we set $v_{GS} = 0$ V and $T_n = 27^\circ\text{C}$ for the bottom one.

Table 2.7: Performance evaluation metrics of the fitting curves in Figure 2.14

Curve	MAE	MSE	RMSE
$C_{oss}(v_{DS})$	6.98	97.28	9.863
$C_{iss}(v_{DS})$	3.844	18.4	4.289
$C_{rss}(v_{DS})$	0.6164	3.795	1.948
$I_{DS}(V_{DS}) _{5\text{V}, 25^\circ\text{C}}$	0.8123	0.7172	0.8469
$I_{DS}(V_{DS}) _{5\text{V}, 150^\circ\text{C}}$	0.12	0.01852	0.1361
$I_{DS}(V_{DS}) _{0\text{V}, 25^\circ\text{C}}$	1.708	5.932	2.436
$I_{DS}(V_{DS}) _{6\text{V}, 25^\circ\text{C}}$	6.799	60.12	7.754

The fitting equations used in Figure 2.14 are given bellow:

$$R_d(T) = 8.518 \times 10^{-2} [1 + 1.35 \times 10^{-2} (T - T_n)] \quad (2.138)$$

$$R_s(T) = 4.69 \times 10^{-3} [1 + 1.35 \times 10^{-2} (T - T_n)] \quad (2.139)$$

$$i_s(\mathbf{v}, T) = \frac{1.83}{|0.003333T + 0.8267|^{2.7}} \frac{\ln(s_1(\mathbf{v}))}{s_2(\mathbf{v})} \quad (2.140)$$

$$\frac{\partial Q_{C_{gs}}(\mathbf{v})}{\partial v_{C_{gs}}} = \frac{6.465 \times 10^{-11}}{e^{-4.027v_{C_{gs}}} + 0.2988} \quad (2.141)$$

$$\frac{\partial Q_{C_{gs}}(\mathbf{v})}{\partial v_{C_{ds}}} = \frac{-2.023 \times 10^{-11}}{1 + e^{2.333 \times 10^{-2} v_{C_{ds}} - 7.7 \times 10^{-2}}} \quad (2.142)$$

$$\frac{\partial Q_{C_{gd}}(\mathbf{v})}{\partial v_{C_{ds}}} = \frac{3.851 \times 10^{-11}}{e^{-0.1v_{C_{gd}}} + 2.246} + \frac{66.9}{e^{-0.6735v_{C_{gd}}} + 1.547 \times 10^{13}} \quad (2.143)$$

$$\frac{\partial Q_{C_{ds}}(\mathbf{v})}{\partial v_{C_{gd}}} = \frac{2.335 \times 10^{-8}}{e^{0.04v_{C_{ds}}} + 330.3} + \frac{0.0004331}{e^{0.3333v_{C_{ds}}} + 3.269 \times 10^6} \quad (2.144)$$

where T_n is the reference temperature and

$$s_1(\mathbf{v}) = \begin{cases} 2.524 \times 10^{-10} e^{13v_{C_{gs}}} + 1, & v_{C_{ds}} > 0 \\ 9.686 \times 10^{-8} e^{9.5v_{C_{gd}}} + 1, & v_{C_{ds}} \leq 0 \end{cases} \quad (2.145)$$

$$s_2(\mathbf{v}) = \begin{cases} v_{C_{ds}}^{-1} + 0.2, & (v_{C_{ds}} > 0) \wedge (0.255v_{C_{gs}} + 1.356 \leq 0.2) \\ 0.255v_{C_{gs}} + v_{C_{ds}}^{-1} + 1.356, & (v_{C_{ds}} > 0) \wedge (0.255v_{C_{gs}} + 1.356 > 0.2) \\ v_{C_{ds}}^{-1} - 0.2, & (v_{C_{ds}} \leq 0) \wedge (0.255v_{C_{gd}} + 1.866 \leq 0.2) \\ 0.255v_{C_{gd}} + v_{C_{ds}}^{-1} + 1.866, & (v_{C_{ds}} \leq 0) \wedge (0.255v_{C_{gd}} + 1.866 > 0.2). \end{cases} \quad (2.146)$$

The input, output and reverse transfer capacitances of Figure 2.13 are defined below, respectively:

$$C_{iss}(\mathbf{v}) = \frac{\partial Q_{C_{gd}}(\mathbf{v})}{\partial u_{C_{gd}}} + \frac{\partial Q_{C_{gs}}(\mathbf{v})}{\partial u_{C_{gs}}} + \frac{\partial Q_{C_{gs}}(\mathbf{v})}{\partial u_{C_{ds}}} \quad (2.147)$$

$$C_{oss}(\mathbf{v}) = \frac{\partial Q_{C_{ds}}(\mathbf{v})}{\partial u_{C_{ds}}} + \frac{\partial Q_{C_{gd}}(\mathbf{v})}{\partial u_{C_{gd}}} \quad (2.148)$$

$$C_{rss}(\mathbf{v}) \equiv \partial_{v_{C_{gd}}} Q_{C_{gd}}(\mathbf{v}). \quad (2.149)$$

Since (2.123) is a non-linear system of differential equations, it cannot be solved analytically as (2.68) is in subsection 2.5.2. For this reason, we approximate the solution of (2.123) using the numerical approach described in [102]. We define the application of the implicit Crank-Nicolson discretisation formula via an arithmetic mean to (2.125) as follows:

$$\mathbf{v}_{n+\frac{1}{2}}(\mathbf{v}_{n+1}) := \frac{\mathbf{v}_{n+1} + \mathbf{v}_n}{2} \quad (2.150)$$

where $\mathbf{v}_n \equiv \mathbf{v}(\theta_n)$. Substituting (2.125) with (2.150) in (2.123), approximating the derivative with the FO terms of the Taylor series and rearranging the terms appropriately results in the following equation:

$$\mathbf{g}(\mathbf{v}_{n+1}) = \mathbf{H}(\mathbf{v}_{n+1}) \mathbf{v}_{n+1} - \mathbf{h}(\mathbf{v}_{n+1}). \quad (2.151)$$

where

$$\mathbf{H}(\mathbf{v}_{n+1}) = \frac{\omega}{\Delta_n \theta} \mathbf{M}(\mathbf{v}_{n+\frac{1}{2}}) - \frac{1}{2} \mathbf{U}(\mathbf{v}_{n+\frac{1}{2}}, u_{GS}(\theta_{n+1})) \quad (2.152)$$

$$\begin{aligned} \mathbf{h}(\mathbf{v}_{n+1}) = & \left(\frac{1}{2} \mathbf{U}(\mathbf{v}_{n+\frac{1}{2}}, u_{GS}(\theta_{n+1})) + \frac{\omega}{\Delta_n \theta} \cdot \mathbf{M}(\mathbf{v}_{n+\frac{1}{2}}) \right) \mathbf{v}_n + \mathbf{e}_1 V_{in} + \mathbf{n} u_{GS}(\theta_{n+1}) \\ & + \mathbf{m}(\mathbf{v}_{n+\frac{1}{2}}) i_S(\mathbf{v}_{n+\frac{1}{2}}). \end{aligned} \quad (2.153)$$

The time discretisation parameter is given by:

$$\Delta_n \theta = \theta_{n+1} - \theta_n. \quad (2.154)$$

The converged value of $\mathbf{v}_{n+1}$ is produced by the following iterative scheme:

$$\mathbf{v}_{n+1}^{(m+1)} = \mathbf{v}_{n+1}^{(m)} - r \mathbf{J}_{\mathbf{g}}^{-1}(\mathbf{v}_{n+1}^{(m)}) \mathbf{g}(\mathbf{v}_{n+1}^{(m)}) \quad (2.155)$$

where r is the relaxation parameter. The individual entries of the Jacobian matrix in (2.155) are defined as:

$$J_{\mathbf{g}}[i, j](\mathbf{v}_{n+1}) = H_{i,j}(\mathbf{v}_{n+1}) + \gamma \left(\sum_{l=1}^{N_{\mathbf{v}}} \frac{\partial H_{i,l}(\mathbf{v}_{n+1})}{\partial v_{n+1}[j]} v_{n+1}[l] - \frac{\partial h_i(\mathbf{v}_{n+1})}{\partial v_{n+1}[j]} \right) \quad (2.156)$$

where $N_{\mathbf{v}}$ is the size of the state vector. The mixing parameter in (2.156) refers to the Newton ($\gamma = 1$) and Picard ($\gamma = 0$) iterations. The inverse of $\mathbf{J}_{\mathbf{g}}$ can be calculated either directly or by applying the bad Broyden method [103]:

$$\mathbf{J}_{\mathbf{g}}^{-1}(\mathbf{v}_{n+1}^{(m)}) = \mathbf{J}_{\mathbf{g}}^{-1}(\mathbf{v}_{n+1}^{(m-1)}) + \frac{\Delta_m \mathbf{v}_{n+1} - \mathbf{J}_{\mathbf{g}}^{-1}(\mathbf{v}_{n+1}^{(m-1)}) \Delta_m \mathbf{g}_{n+1}}{\|\Delta_m \mathbf{g}_{n+1}\|_2^2} \Delta_m \mathbf{g}_{n+1}^T \quad (2.157)$$

where

$$\Delta_m \mathbf{v}/\mathbf{g}_{n+1} = \mathbf{v}/\mathbf{g}_{n+1}^{(m)} - \mathbf{v}/\mathbf{g}_{n+1}^{(m-1)} \quad (2.158)$$

However, even when using (2.157) there is still the need for either an explicit computation

or an approximation of the inverse of (2.156) for the initial iteration, since every subsequent calculation depends on the value of the previous iteration.

The termination condition used in (2.155) is the equivalent of (2.91) adjusted to $\mathbf{v}_{n+1}$:

$$\frac{\|\Delta_m \mathbf{v}_{n+1}\|_\infty}{\|\mathbf{v}_{n+1}^{(m)}\|_2} < \epsilon_v \quad (2.159)$$

where ϵ_v is the relative error tolerance for the state vector approximation. The initial boundary conditions of (2.123) mainly affect the convergence speed of the differential equation solution until it reaches steady state and in this work we propose three different ways. The first and simpler possible approach is to start off with a zero state vector and let it evolve until convergence. Another approach, which is by default used in LTspice transient simulations [104], is to treat the inductors as short circuits and the capacitors as open circuits. Then, the currents through the inductors and the voltages across the capacitors are determined by the independent current and voltage sources in the circuit topology, accordingly. The third suggested approach for defining the initial conditions of the differential equation is to use the state vector values from the previous tuning step, i.e. the linear SS model. The simulation is considered to have reached steady state when the state vector behaviour over a period is not evolving anymore and the process has converged. The condition that we use to determine the termination of the computations is based on the relative error of the DC component of the inverter input current between the last two periods:

$$\frac{|I_{L_{rfe}}^{(m_T)} - I_{L_{rfe}}^{(m_T-1)}|}{I_{L_{rfe}}^{(m_T)}} < \epsilon_T \quad (2.160)$$

where $I_{L_{rfe}}$ is calculated using the trapezoidal method for numerical integration [83], m_T is the iteration index of complete periods computations and ϵ_T is the corresponding error tolerance.

2.6.3 Tuning Method

A tuning algorithm for adjusting the drain voltage and slope at turn-on using the shunt and series load capacitors for the Class E inverter is proposed in [105]. However, changes in the value of C_s result in changes in the output power of the inverter, and further tuning of the input voltage, Tx coil inductance and load is required to maintain the desired circuit properties. The higher dimension of degrees of freedom in the Class EF/ Φ inverter, compared to the Class E

counterpart, enables the absorption of the unwanted effects of the switching device on the shape of the drain waveform using the combination of the shunt and the Φ -branch capacitors, which introduce minimum effects on the output power of the circuit. Instead of the Φ -branch capacitor, we could also adjust the duty cycle to control the drain voltage slope at turn-on, however this would result in changes in λ , which corresponds in deviation of the inverter behaviour from the input design requirements.

The proposed tuning process is explained in the flowcharts shown in Figure 2.15a and Figure 2.15b. It is composed of two parts, the “master” and the “slave” tuning methods, similar to the master-slave D flip-flop terminology. The master tuning method (Figure 2.15a) dictates the results of the slave tuning method (Figure 2.15b) and the algorithm terminates when the conditions of both processes are satisfied. Both methods are based on the same principle: first set appropriate boundaries in such way that a solution exists within the resulting range, and then search for the solution in it.

The goal of this algorithm is to set the value of the drain voltage at turn-on to zero, by adjusting the value of C_p , as well as the drain current to i_S^{ON} at turn-on, using C_ϕ . Any adjustments to C_ϕ are followed by the corresponding alterations of L_ϕ according to (2.5), and R_ϕ is based on (2.66), so that the resonant frequency of the Φ -branch filter remains constant. The order in which the two tuning requirements, the drain voltage and current values, will be assigned to the master and slave iterative schemes is up to the designer to choose and affects primarily the convergence but could also lead to different results. For example, the EF₂ example that we use in this work uses the C_ϕ tuning as the master scheme and the C_p as the slave, as it is discussed in the following subsection. However, tuning the inverter design proposed in the experimental section of [1] with this method required the implementation of the opposite master-slave assignment order, compared to the example mentioned above, in order to achieve convergence. The requirement for the tuning process to be repeated iteratively originates from the fact that the effects of C_p and C_ϕ are interconnected and not independent and their adjustments must be treated simultaneously. Instead of the actual drain voltage, we track the $v_{C_{ds}}(\theta_{\text{ON}}^-)$ state variable, since it is the internal signal of the device that controls i_S . As for the drain current, we use the combination of the shunt capacitor current and the output capacitor current of the device:

$$i_{C_p}(\theta_{\text{ON}}^-) + i_{C_{oss}}^*(\theta_{\text{ON}}^-) = i_{L_{r_{fc}}}(\theta_{\text{ON}}) - i_{L_\phi}(\theta_{\text{ON}}) - i_{L_{s_1}}(\theta_{\text{ON}}) - i_S^*(\theta_{\text{ON}}^-) \quad (2.161)$$

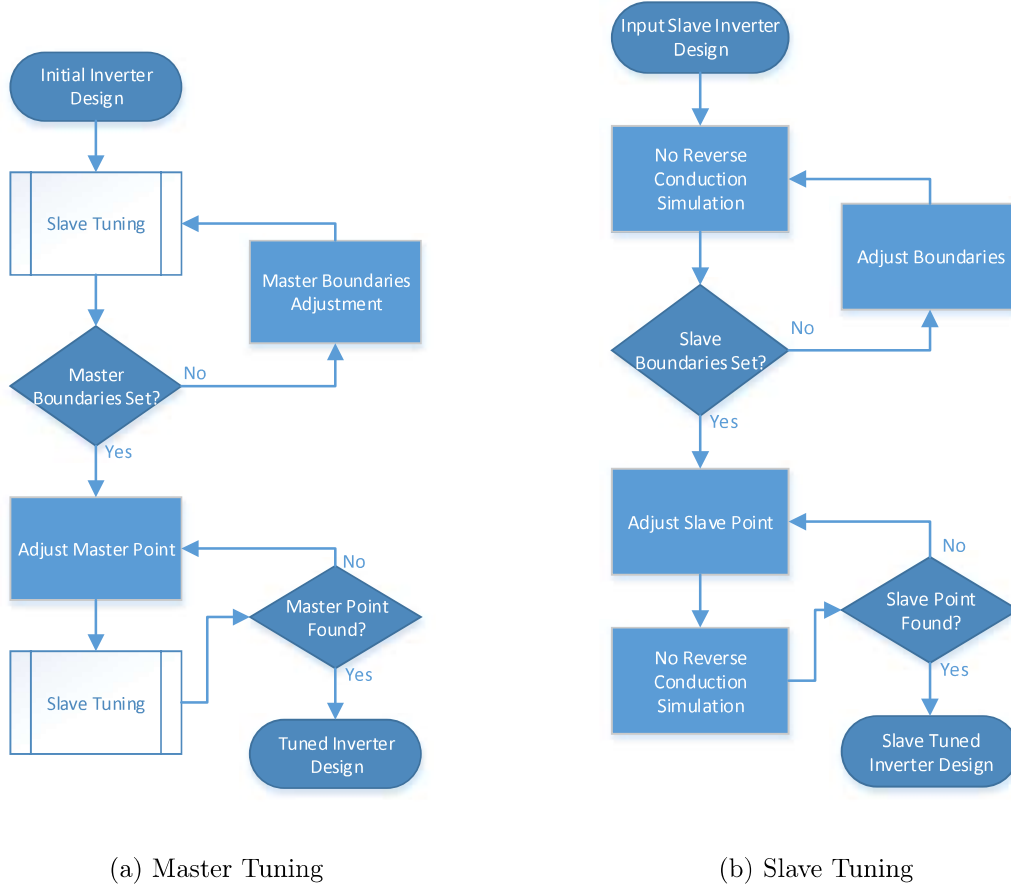


Figure 2.15: High level flowchart diagrams of the "master" and "slave" tuning processes for adjusting the drain voltage characteristics of the non-linear switching device in a given Class EF inverter design. The subprocess of the "slave" tuning algorithm in (a) is explained in more detail in (b).

where i_S^* is the current of the dependent source in Figure 2.13 without reverse conduction during turn-off.

The "Initial Inverter Design" in Figure 2.15a can be defined with one of the ways proposed in subsection 2.6.2. The "Inputs Slave Inverter Design" in Figure 2.15b is always set to the state vector of the previous iteration, since this approach achieves convergence faster as the iterations advance.

The "No Reverse Conduction Simulation" block in Figure 2.15b begins with a simulation according to subsection 2.6.2 until steady state is achieved. The property of reverse conduction during turn-off in the device is modelled through the behaviour of i_S and controlled by the sign of $v_{C_{ds}}$. To simulate the device as if it was not reverse conducting we first need to locate the zero crossing point of $v_{C_{ds}}$ and then extend with the evolution of i_S^* from that point until

$\theta = \theta_{ON}^-$. The search of the zero crossing point can be done either by looking for $v_{C_{ds}}(\theta) < 0$ forward in time or for $v_{C_{ds}}(\theta) > 0$ backwards in time, with the choice of the search direction affecting the speed of the algorithm. The reason for calculating the electrical signals in the circuit without the property of reverse conduction is because this way we can achieve a better estimation of how far from the solution the current state is during the iterative tuning process and adjust the solver accordingly with more precision, since during reverse conduction both conditions will be close to zero, regardless of how detuned the circuit is.

The block for computing the limits of the boundaries uses the same methodology for both the master and the slave part of the tuning algorithm. First we check whether the existing design constitutes the upper or the lower boundary, based on the sign of the corresponding termination condition. Then, the opposite boundary is updated iteratively until the required sign condition is satisfied. This approach ensures that the resulting range contains a solution since the boundaries are of opposing signs and the transfer function of the inverter is continuous. The update of the component for the opposing boundary limit is computed using the following relation:

$$C_{p/\phi}^{(m+1)} = \left(1 \pm t_{C_{p/\phi}}\right) C_{p/\phi}^{(m)} \quad (2.162)$$

where $t_{C_{p/\phi}} \in (0, 1)$ is a parameter that determines the extent of the update. High values of $t_{C_{p/\phi}}$ will require fewer iterations to converge, however low values will result in smaller range, hence better solution approximations for the following steps of the algorithm. One more way to control the speed and accuracy of the boundaries computations, and differentiates the master block to its slave counterpart, is to update the slave parameter mentioned above before each "Slave Tuning" block:

$$t_{C_{p/\phi}}^{(m_M+1)} = (1 + t_C^S) t_{C_{p/\phi}}^{(m_M)} \quad (2.163)$$

where m_M is the iteration index of the "Master Tuning" block and $t_C^S \in (-1, 1)$ is a parameter that determines the incremental update of the slave boundary update parameter in (2.162) and can have an effect on the speed of the process by taking advantage of the fact that as the algorithm evolves the approximation of the solution improves.

Once the range and limits of the boundaries are well defined, we use the algorithm proposed in [106] to find the roots of the condition functions within. This algorithm uses a combination of inverse quadratic interpolation and bisection methods for locating the zero of the function in a computationally efficient way, depending on its properties. In this paper we follow the same

formulation and notation as in [106], wherever we refer to this method.

The slave tuning block tries to follow the changes introduced by the master tuning method, since every time the master block updates, the slave block needs to re-adapt accordingly. The procedure converges after enough iterations are performed and the algorithm terminates after the two conditions are satisfied simultaneously and the final inverter design is defined.

2.6.4 Simulation and Tuning Example

Instead of using the full model in Figure 2.13, at this point of the tuning algorithm (3rd part of the flowchart in Figure 2.2) we use a reduced model by omitting the effects of the package parasitic inductances and the rise/fall gate resistances. Reducing the accuracy and level of detail of the model is acceptable in this case, since [89] introduces relatively low stray package inductance and its effect does not affect significantly the overall behaviour of the circuit. The reduced accuracy of simulation is counterbalanced by a significant increase in computational speed, both because the SS model has fewer degrees of freedom (8 instead of 10) and the discretisation number is not required to be as large compared to the full device model, since there is no need for capturing the HF oscillations caused by the packaging stray inductance. Mathematically, this process is equivalent to equating R_{gate} to R_g , omitting the 7th and 8th rows and columns in (2.123), and replacing with the following expressions in the corresponding places:

$$i_{L_d} = \frac{u_{C_p} - u_{C_{ds}} + \frac{R_s}{R_g + R_s} (u_{GS} - u_{C_{gs}})}{R_d + R_s + \frac{R_s^2}{R_g + R_s}} \quad (2.164)$$

$$i_{L_g} = \frac{u_{GS} - u_{C_{gs}} - R_s i_{L_d}}{R_g + R_s}. \quad (2.165)$$

The simulated waveforms of the inverter SS variables before and after tuning are shown in Figure 2.16. The design and algorithm inputs, in addition to the ones used in the previous tuning steps of the algorithm, as well as the output component values and performance metrics of the iterative process are presented in Table 2.8. The use of the last four tolerance criteria in the “Parameters” section of the table is explained in [106]. As expected, the adjustment of the shunt capacitor value is the most prevalent ($\sim 60\%$ decrease from the value of the linear SS tuning in Table 2.2), mainly to compensate for the effect of the output capacitance of the switching

device. Also, from Table 2.8 we can confirm that the accuracy of the termination conditions agrees with the tolerance demands. This fact can also be confirmed from the corresponding waveforms at the bottom right corner in Figure 2.16, where both the soft switching as well as the slope of the drain voltage requirements at turn-on have been restored. Also, by comparing the tuned waveforms in Figure 2.7 with Figure 2.16 we can confirm that no additional stresses were introduced on the transistor by the non-linearities of the device, and the tuning algorithm successfully absorbed any potential unwanted effects.

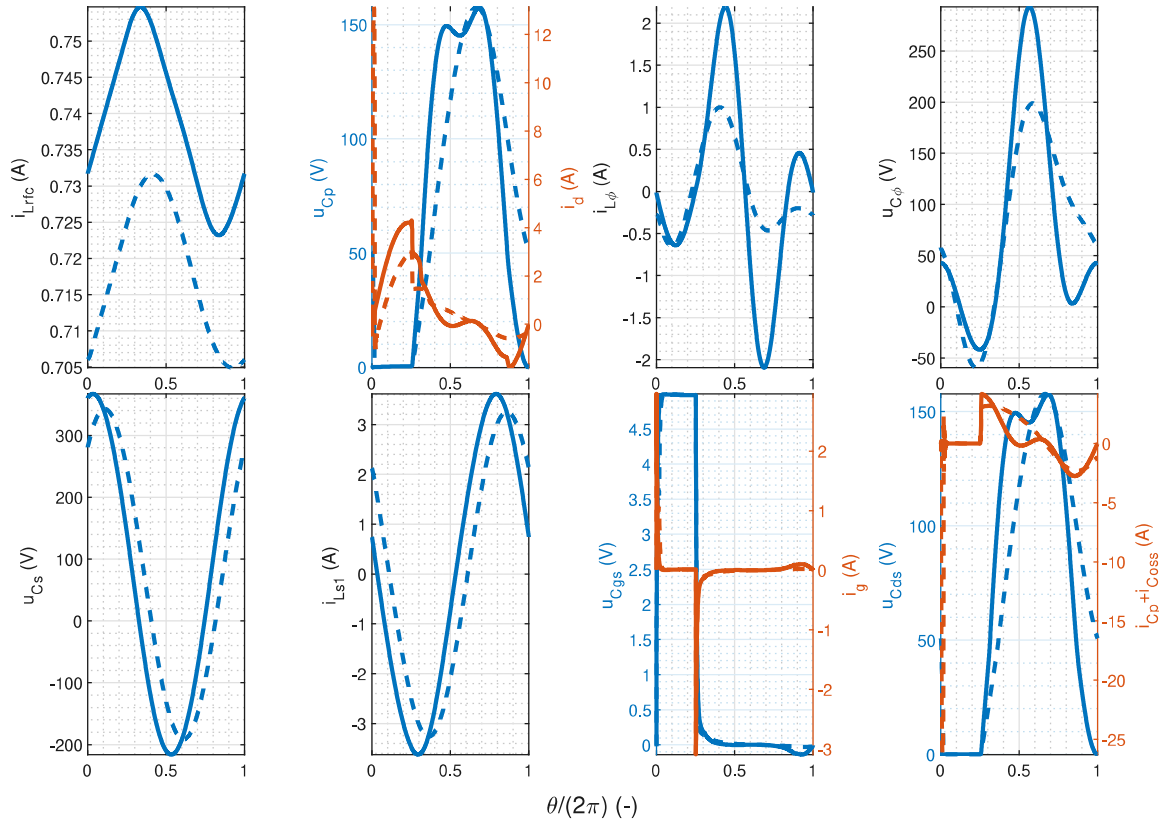


Figure 2.16: Simulation of the Class EF inverter using the numerical simulation with the non-linear switching device model. The dashed waveforms correspond to the linear State Space design and the solid ones represent the tuned version.

A characteristic visual demonstration of the output of the process represented by the “No Reverse Conduction Simulation” block in Figure 2.15 and further explained in subsection 2.6.3 is shown in Figure 2.17. Without this process the magnitude and direction of the incremental adjustment of the shunt and ϕ -branch capacitors would be inaccurate, since the drain voltage and current waveform values at turn-on during reverse conduction are not representative of the extend of the detuning.

The figures that follow display the convergence properties of the simulation method (Fig-

Table 2.8: Inputs, outputs, algorithm parameters, and performance data of the Class EF inverter tuning example with a non-linear device model

	Quantity	Value	Unit
Inputs *	T_n	27	$^{\circ}\text{C}$
	T	27	$^{\circ}\text{C}$
	Device	GS66504B	—
	Gate Driver	LMG1020	—
Parameters	t_C^S	-0.2	—
	Master→Slave	$C_\phi \rightarrow C_p$	—
	Reverse Conduction	Forward Search	—
	$t_{C_p}^{(1)}$	0.5	—
	$t_{C_\phi}^{(1)}$	0.5	—
	$\mathbf{J}_g^{-1}$	Gaussian Elimination	—
	ϵ_T	1×10^{-6}	—
	ϵ_v	1×10^{-6}	—
	Initial Conditions	LTspice	—
	r	1	—
	γ	1	—
	Root Finding	Method in [106]	—
	$\left i_{C_p}^* \right _{\min}^{\text{bisection}^{**}}$	1	mA
	$\left u_{C_{ds}}(\theta_{\text{ON}}) \right _{\min}^{\text{bisection}}$	1	mV
	e_A	1×10^{-5}	—
	e_R	1×10^{-10}	—
Outputs	C_p	108.196	pF
	C_ϕ	88.374	pF
	L_ϕ	389.703	nH
	R_ϕ	389.703	m Ω
Relative Change	$\delta(C_p)$	-61.978	%
	$\delta(C_\phi)$	37.781	%
	$\delta(L_\phi)$	-27.422	%
	$\delta(R_\phi)$	-27.422	%
Performance	$i_{C_p}^*(\theta_{\text{ON}}) - i_S^{\text{ON}^{**}}$	-279.397	μA
	$u_{C_{ds}}(\theta_{\text{ON}})$	233.925	μV
	Cycle Iterations	1740	—
	Newton Iterations	4.0963×10^6	—
	Slave Iterations	23	—
	Master Iterations	4	—
	Algorithm Iterations	26	—

*The inputs given in this table are in addition to the data of Table 2.1, Table 2.2 and Table 2.3.

** $i_{C_p}^*$ refers to (2.161).

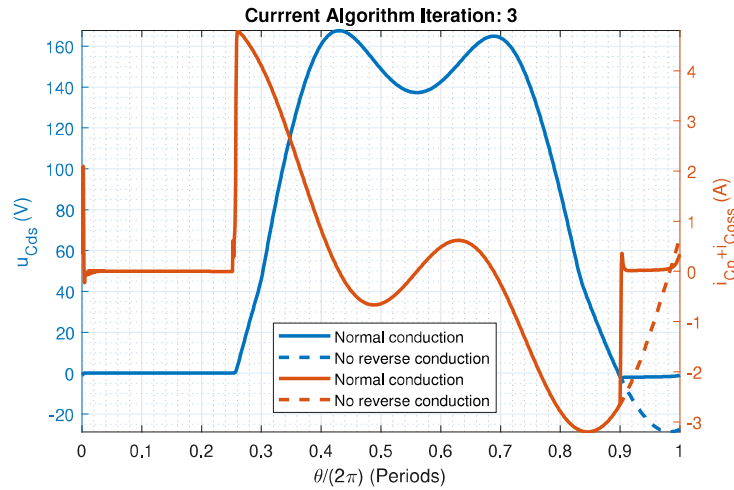


Figure 2.17: Example of the output of the "No Reverse Conduction Simulation" block in Figure 2.15b, as described in subsection 2.6.3.

ure 2.18) and tuning algorithm (Figure 2.19) described in subsection 2.6.2 and subsection 2.6.3, respectively. The relation between the choice of the initial conditions and the computational speed and efficiency of the simulation process is demonstrated in Figure 2.18. By using the state vector at turn-on from the previous iteration as initial conditions for the current step during the evolution of the Slave Tuning block in Figure 2.15a, the required number of iterations for convergence is reduced drastically, as shown by comparing the graphs in Figure 2.18 from left to right. A four dimensional phase space representation of the evolution of the tuning algorithm is given in Figure 2.19. The spiral shape of the reflection of the path to the plane defined by the C_p and C_ϕ axes proves that the scheme in (2.163) does accelerate the search to convergence.

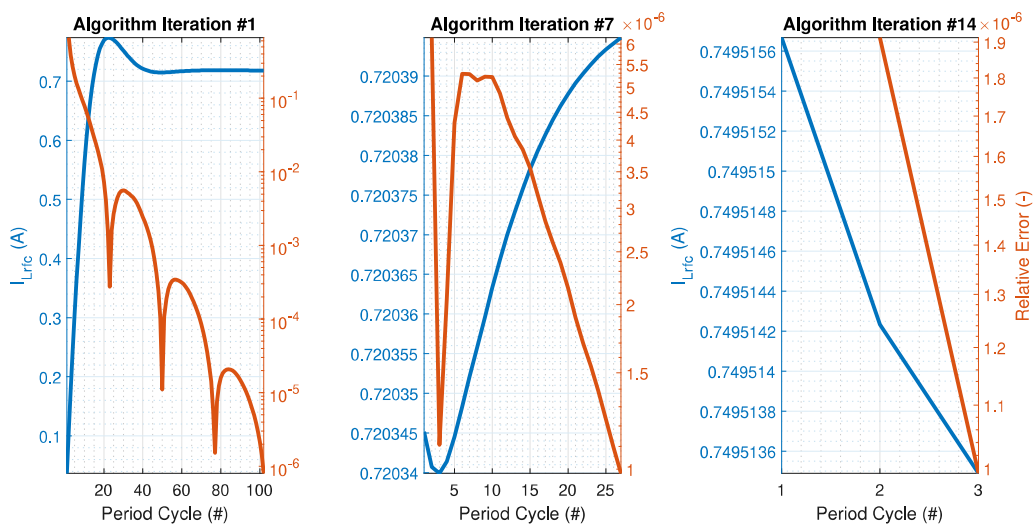


Figure 2.18: Convergence of the input current value and its relative error of the Class EF simulation with a non-linear device model for various indicative stages of the tuning algorithm.

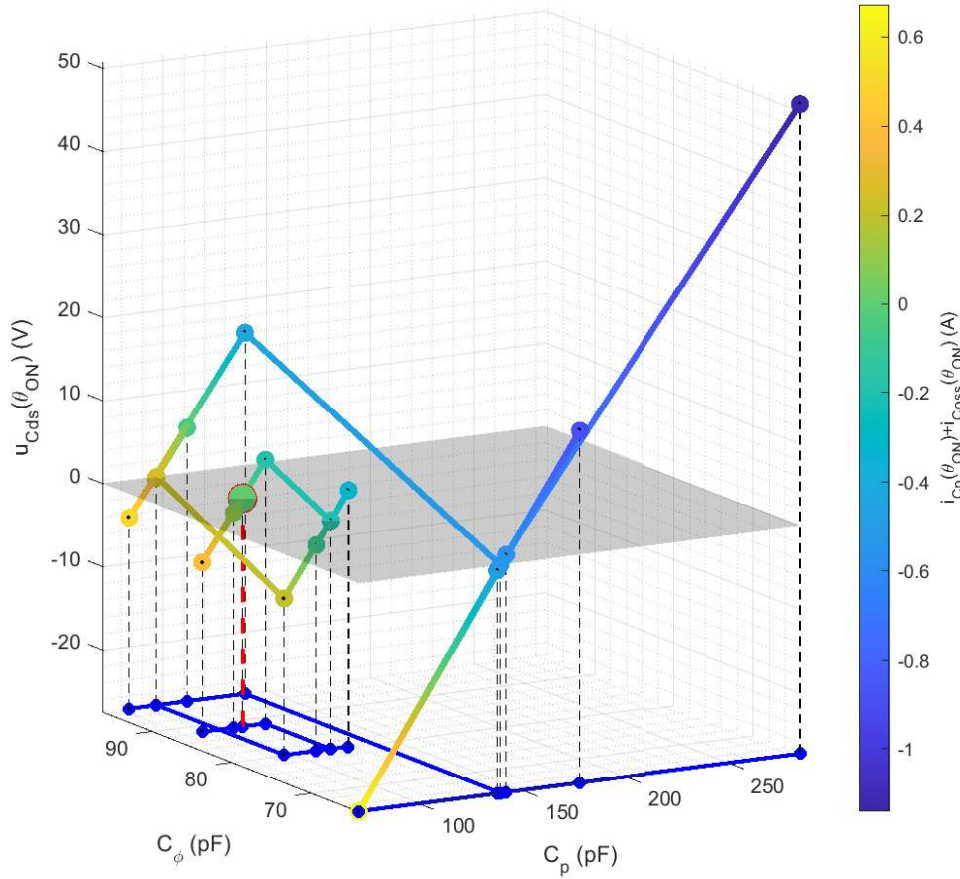


Figure 2.19: Four dimensional phase space representation of the tuning algorithm evolution using the non-linear switching device model. The blue line is the two dimensional reflection on the input plane of the higher level convergence path.

2.6.5 Reduced Non-linear Tuning

Background

In some cases, the information for reproducing the full device model in Figure 2.13 is either not available or the implementation of the modelling described in subsection 2.6.2 along with the tuning method in subsection 2.6.3 may be too complicated and time consuming. In this section we propose an alternative tuning method that requires much less detail and information about the intrinsic properties of the device while still managing to capture the effects of the non-linearities to a comparable degree and maintain ZVS.

Simulation

The circuit model that we use for this design method, shown in Figure 2.20, is based on Figure 2.6 with the inclusion of a non-linear drain voltage dependent output capacitance C_{oss} in parallel with the variable switch resistor. The behaviour of C_{oss} is approximated with the following scaled sigmoid function:

$$C_{oss}^S(v_{DS}) = L + \frac{U - L}{1 + e^{-r(v_{DS} - x_0)}}, \quad (2.166)$$

where L, U, r and x_0 are fitting parameters. The fitting of (2.166) was performed with the combination of [107] and [108] and both the fitted and datasheet C_{oss} shapes of [89] are shown in Figure 2.21.

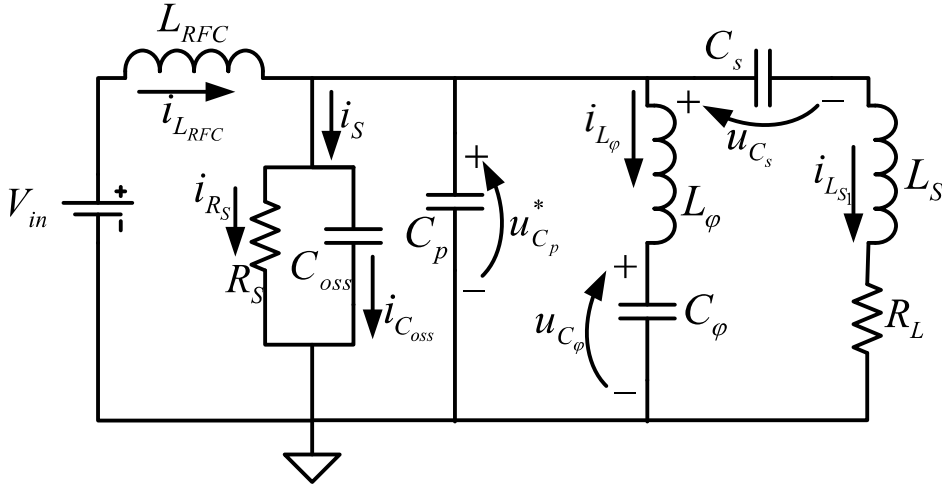


Figure 2.20: Class EF inverter with the state space variables shown and the switch modelled as variable resistance in parallel to a voltage dependent capacitance.

The differential equation that describes the evolution of the behaviour in time of the circuit in Figure 2.20 is:

$$\omega \mathbf{M}(\mathbf{q}^*) \frac{d}{d\theta} \mathbf{q}^*(\theta) = \mathbf{A}_{ON/OFF} \mathbf{q}^*(\theta) + \mathbf{b}, \quad (2.167)$$

where

$$\mathbf{M}(\mathbf{q}^*) = \text{diag} \left(L_{rfc}, C_p + C_{oss}^S(v_{C_p}^*), L_\phi, C_\phi, C_s, L_{s1} \right), \quad (2.168)$$

$$\mathbf{q}^*(\theta) = \begin{bmatrix} i_{L_{rfc}}(\theta) & v_{C_p}^*(\theta) & i_{L_\phi}(\theta) & v_{C_\phi}(\theta) & v_{C_s}(\theta) & i_{L_{s1}}(\theta) \end{bmatrix}^T, \quad (2.169)$$

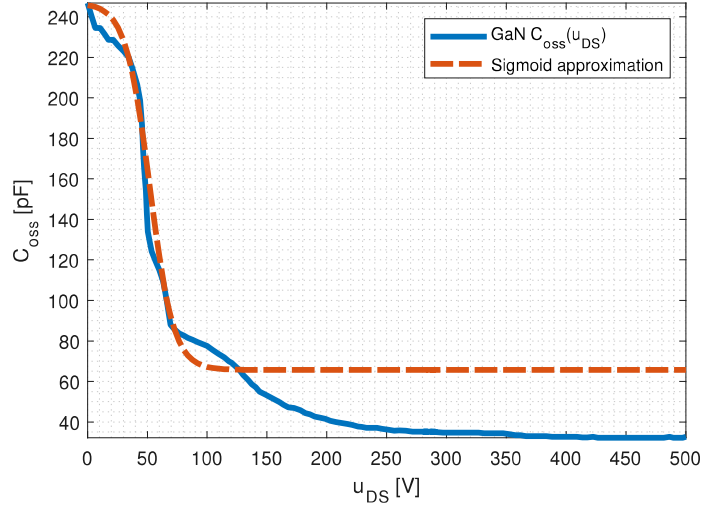


Figure 2.21: $C_{oss}(v_{DS})$ of GaN Systems GS66504B transistor (solid blue line) compared to the sigmoid function with the best fitting results (dashed orange function).

$$\mathbf{A}_{\text{ON/OFF}} = \begin{bmatrix} 0 & -1 & 0 & 0 & 0 & 0 \\ 1 & \frac{-1}{R_s^{\text{ON/OFF}}} & -1 & 0 & 0 & -1 \\ 0 & 1 & 0 & -1 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 1 & 0 & 0 & -1 & -R_{sL} \end{bmatrix}, \quad (2.170)$$

$$\mathbf{b} = V_{in} \mathbf{e}_1. \quad (2.171)$$

Since Equation (2.167) is non-linear and there is no direct analytical solution, it is solved numerically by using the 4th order Runge-Kutta (RK) iterative method [109]. It is repeatedly solved during one period, until the boundary conditions are satisfied to the required tolerance (ϵ_{RK}), which is defined below:

$$\max_{\{\theta_{\text{ON}}, \theta_{\text{OFF}}\}} \|\mathbf{q}^{*(k_{RK})}(\theta^-) - \mathbf{q}^{*(k_{RK})}(\theta^+)\|_2 < \epsilon_{RK}, \quad (2.172)$$

where k_{RK} is the iteration index.

Figure 2.11 shows the effect in the operation that the inclusion of the switch capacitor introduces. It is clear that the circuit is no longer in the desired tuning state when the effect of the switch capacitance is taken into account, and the device is hard switching at over 50 V, according to Table 2.9. The rest of the circuit components are identical to the ones derived

from the iterative tuning method of subsection 2.5.5. The initial condition for the RK method was the final state vector during turn on at the iterative SS tuning method. The inputs and outputs of the calculations are given in Table 2.9. The waveforms of the currents through the switch and the parallel capacitor are given by:

$$i_p^*(\theta) = \frac{C_p}{C_p + C_{oss}(q_2^*)} \left(q_1^*(\theta) - \frac{q_2^*(\theta)}{R_S} - q_3^*(\theta) - q_6^*(\theta) \right), \quad (2.173)$$

$$i_s^*(\theta) = \frac{q_2^*(\theta)}{R_S} + \frac{C_{oss}(q_2^*)}{C_p} i_p^*(\theta). \quad (2.174)$$

Table 2.9: Input, outputs and parameters used in the reduced tuning method in subsection 2.6.5.

	Quantity	Value	Unit
Parameters	U	65.713	pF
	L	246.75	pF
	r	0.1	V^{-1}
	x_0	51.913	V
	ϵ_{RK}	10^{-3}	—
	ϵ_B	10^{-3}	V
RK Inputs* $k_B = 0$ $k_{RK} = 0$ $\theta = \theta_{ON+}$	q_1	1.226	A
	q_2	146.217	pV
	q_3	-0.47	A
	q_4	71.038	V
	q_5	656.117	V
	q_6	1.696	A
Bisection Inputs* $k_B = 0$ $k_{RK} = 606$ $\theta = \theta_{ON+}$	q_1	1.182	A
	q_2	51.79	V
	q_3	-0.611	A
	q_4	75.753	V
	q_5	567.496	V
	q_6	3.554	A
	C_p^-	112.517	pF
	C_p^+	359.267	pF
Outputs $k_B = 16$	$q_2(\theta_{ON}^+)$	0.535	mV
	C_p	253.712	pF
	$\delta(C_p)$	29.38	%
	THD($i_{L_{s1}}$)	1.195	%

*The inputs given in this table are in addition to the data of Table 2.5 and Table 2.6.

Tuning

The tuning of the non-linear model of the circuit is performed by implementing a modified Bisection method [110], by adjusting C_p until ZVS is achieved. The high limit of the range is the value of C_p from the previous SS tuning step, i.e. Table 2.6, since it will always produce a value of C_p higher than required because it does not include the effect of the output capacitance of the device. The lower limit of C_p is produced by subtracting from the previously described high limit the value of $C_{oss}(v_{DS} = 0)$, since C_{oss} is monotonically decreasing [91] and the effective constant output capacitance of the transistor is typically around the supply voltage level [1].

Apart from the range of the shunt capacitor, the rest of the component values are directly derived from the previous SS tuning step in Table 2.6. The initial conditions of the state vector for the RK simulation are also taken from the SS tuned state vector at θ_{ON} . Once the RK solver has converged, the bisection method is applied to further adjust C_p , and this scheme repeats iteratively until the final termination criterion is satisfied:

$$|q_2^*(\theta_{ON})| < \epsilon_B, \quad (2.175)$$

where ϵ_B is the tolerance of the ZVS in the Bisection method.

Finally, we evaluate our model with an LTspice simulation, using the final component values that occurred after the non-linear tuning part of the design algorithm, and the device model provided by the manufacturer. The resulting waveforms of both the LTspice simulation and the design algorithm are plotted in Figure 2.22. Our model has successfully incorporated the effect of the actual switching device and the two sets of waveforms highly agree.

The results from the Fourier analysis performed on the output current and voltage waveforms from the state space solution of the final model are given in Figure 2.23. The reduced 2nd harmonic confirms that the inverter design is a Class EF₂ and the output THD remains low for both the Tx coil voltage and current. However, we can notice from Figure 2.22 that although the ZVS condition is met, P_o is slightly higher than expected, λ is lower and ZVDS is not exactly achieved. Though in practice, all the final operating conditions are quite close to the design inputs, and the inverter would still be suitable for application.

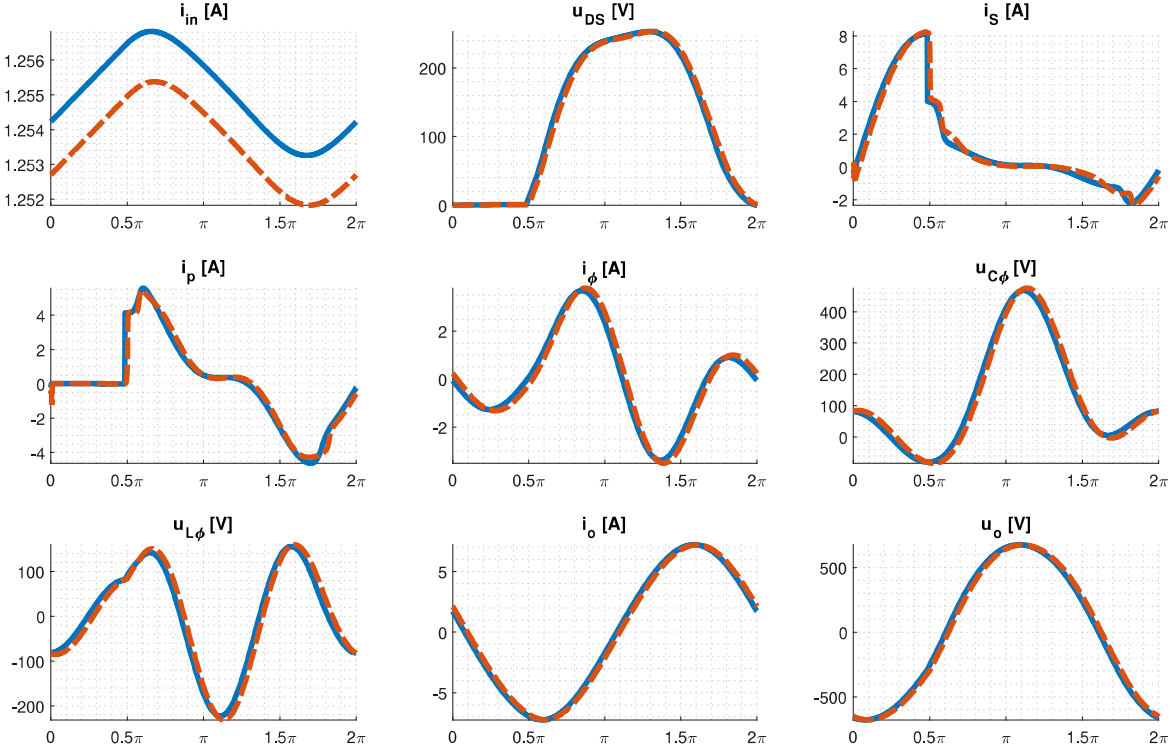


Figure 2.22: State space solution with components from iterative tuning including the effect of C_{oss} (solid blue line) and corresponding LTspice simulation with the actual switching device model (dashed orange line).

2.7 Measurements and Tuning of the Experimental Setup

2.7.1 Background

In this section of the paper we explain the mechanisms involved in the last tuning step of Figure 2.2, i.e. the “Complete System” process block. The theoretical design procedure for defining the component values of the circuit has been completed in the previous tuning steps, and the resulting values are used as guidelines for populating the PCB accordingly. However the actual measured values of the components in the final topology will almost certainly deviate from the ideal case, due to limited off-the-shelf component selection and tolerances.

This issue is typically resolved by performing additional manual retuning [49, 47]. The manual retuning steps are usually based on empirical observation and provide more qualitative instead of quantitative and precise guidelines [26, 46, 1] and tend to require multiple repetitive incremental adjustments based on trial and error. Here, we propose a post-measurement iterative scheme to readjust the operation of the inverter to the actual components using only the pro-

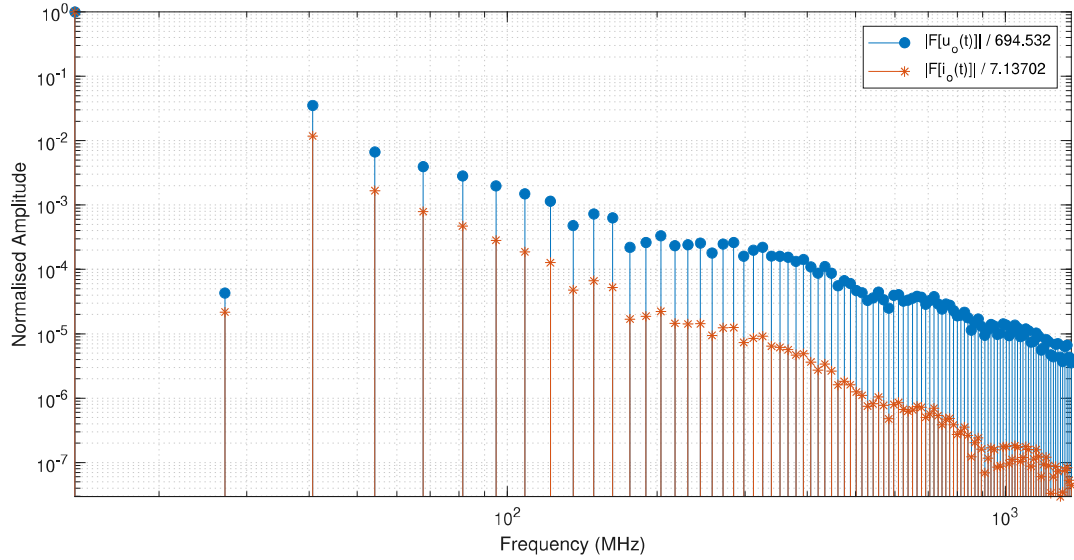


Figure 2.23: Fourier analysis of the output waveforms of the reduced non-linear finalised model.

vided electrical signals of the board, while still maintaining the desired behaviour based on the input features.

2.7.2 Component Measurement and Simulation

For simulating the inverter and computing the corresponding waveforms we used the full switching device model along with the method described in subsection 2.6.2 and the values of the component measurements used are given in Table 2.10. As initial boundary conditions for the simulation calculations we use the SS vector values from the previous tuning step along with (2.164) and (2.165). This choice results in the fastest computational speed, since the gate shaping resistance and stray package inductance along with the relatively minor deviations of actual components from the ideal values (ranging from 0.12% to 2.59%) results in the initial point not being far from the final solution.

The ON and OFF gate signal shaping resistances are measured individually using the TTI LCR400 Precision LCR Bridge and the package inductances are derived by reverse engineering the LTspice model of [89], since the datasheet does not provide quantitative stray inductance information. It must be mentioned at this point that the above measurements may deviate when applied at MHz frequencies because of instrument and Spice model limitations, however their overall effect to the operation of the circuit is not crucial in terms of optimal tuning.

Table 2.10: Inputs, outputs, algorithm parameters, and performance data of the Class EF₂ inverter tuning example with a complete non-linear system model

	Quantity	Value	Unit
Inputs*	T	40	$^{\circ}\text{C}$
	C_p	111	pF
	L_{ϕ}	391	nH
	R_{ϕ}	489	m Ω
	C_{ϕ}	90	pF
	C_s	142	pF
	R_G^{ON}	5.3	Ω
	R_G^{OFF}	2.2	Ω
Parameters**	N	2000	points
	Initial Conditions	Previous Tuning Step	—
	$ V_{in} _{\min}^{\text{bisection}}$	1	mV
	D Search Range	[15.169, 35.169]	%
Outputs	V_{in}	73.055	V
	D	24.93	%
Relative Change	$\delta(C_p)$	2.592	%
	$\delta(L_{\phi})$	0.333	%
	$\delta(R_{\phi})$	25.48	%
	$\delta(C_{\phi})$	1.84	%
	$\delta(C_s)$	-0.814	%
	$\delta(V_{in})$	-3.494	%
	$\delta(D)$	-0.95	%
Performance	P_o	49.93	W
	η_{inverter}	97.583	%
	$I_{L_{s1}}$	510.766	μA
	THD ($i_{L_{s1}}$)	1.907	%
	V_{in} Iterations	8	—
	D Iterations	15	—
	Algorithm Iterations	25	—

*The inputs given in this table are in addition to the data of Table 2.1, Table 2.2 and Table 2.8.

**The parameters given in this table are in addition to the data of Table 2.8.

Also, the ON and OFF gate resistances selection is based on the guidelines of the transistor manufacturer and were measured experimentally in situ, rather than derived from theoretical optimisation, since this kind of investigation is out of the scope of this work.

The shunt and series load capacitors [73] are measured while soldered in place at f_S , as described in subsection 2.4.4. Another option could be to measure the impedance of the fully populated series load branch, i.e. C_s and fully coupled Tx and Rx coils, and fit a series damped resonant model on the measurement point at switching frequency. This is the approach that we use

for the ϕ -branch components values derivation, which is based on fitting on the curves of the total resistance and impedance around the frequencies f_S and $\tau_\phi \times f_S$, as shown in Figure 2.5. It must be noted that the resistance measurement is unreliable (existence of sections with negative value) because of the high Q factors [72] of the inductors [90] and capacitors [73] used. Also, for the case of C_p and ϕ -branch the probes are connected during measurements to compensate for their additional capacitance to the system. If PCB board and component parasitics, either obtained through impedance measurements or by software extraction, are to be included separately, they can be directly added to the formulation of (2.124). This applies for both linear and non-linear components. Linear board parasitics can also be simulated in the second part of the algorithm through (2.70).

The resulting waveforms of the inverter simulation are given in Figure 2.24, based on the inputs shown in Table 2.10. As previously, input data that has already been mentioned in previous parts of this work and have not been altered are ignored. The effects of the ON and OFF gate resistances and the package inductances can be noticed when comparing $v_{C_{gs}}$ with the current through the drain of the device between Figure 2.16 and Figure 2.24. Specifically, the softer voltage level transitions of $v_{C_{gs}}$ are caused by R_G and the HF ringing oscillations of i_{L_d} after turn-off are driven by the stray package inductances. The ringing of i_{L_d} would be more pronounced across the whole period if the design did not have ZVDS. According to subsection 2.6.4, in order to successfully capture these HF ringing transitions in simulation, a finer discretisation is required, which is confirmed since the value of N in Table 2.10 is double that of Table 2.3.

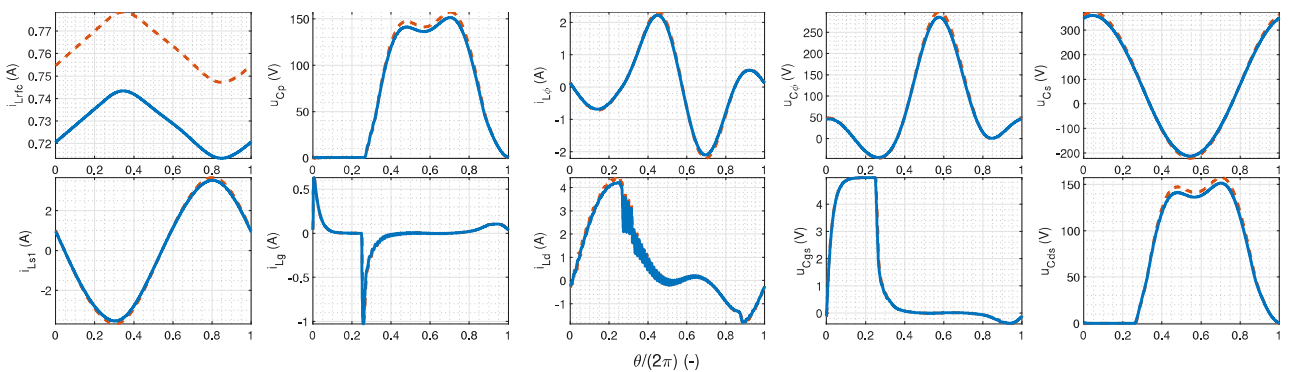


Figure 2.24: Waveforms of the state space vector in (2.125) before (dashed orange line) and after (solid blue line) adjusting the electrical input signals of the inverter for absorbing the undesired effects of the measurement mismatch with the ideal theoretical design component values.

2.7.3 Explanation and Results of the Tuning Method

This last part of the tuning process consists of two separate and independent iterative schemes that aim to optimise the operation of the final experimental evaluation of the inverter board by adjusting the input voltage and duty cycle in order to achieve the desired power output level with maximum possible efficiency. If we had perfectly ideal components, i.e. linear as in section 2.5, we would expect that the input voltage would only affect the magnitude of the electrical signals of the inverter proportionally, without disturbing the soft switching conditions and desired operation properties of the circuit. However, the non-linear output capacitance of the device results in loss of ZVS when the input voltage deviates from its optimal value. Also, the duty cycle has an impact on the power throughput of the system, since it changes the equivalent input resistance of the circuit. The above stated reasons basically mean that although we defined the optimisation of each parameter independently, their effect is interconnected, and hence the proposed tuning method should be applied repeatedly until the desired accuracy level is reached. In our case, since the mismatch of the components is low, as mentioned in the previous subsection, and the GS66504B device has low package inductance [89], a single iteration of the algorithm gave satisfactory level of accuracy and was enough for practical application. Another detail worth mentioning is that optimising the duty cycle for efficiency in general and not strictly to achieve ZVS may be more beneficial in practice and lead to better designs, since with real, non-ideal parts in the circuit ZVS does not always translate to better overall performance [47].

The tuning of the input voltage follows the flowchart shown in Figure 2.15b, with the differentiation that instead of using simulation results with no reverse conduction, we use simulation results of the normal device operation. The condition for the boundaries definition is that the two boundary values of the input voltage define a range that includes the desired output power level, by using (2.162) but adapted to V_{in} . If more than one repetitions of the full algorithm are applied, we can use (2.163) to speed up the process, which is not the case of our example. The rest of the algorithm evolution follows exactly the description in subsection 2.6.3. The convergence progression of the algorithm is shown in Figure 2.25 and the algorithm parameters and outputs are presented in Table 2.10.

After the input voltage is defined, we proceed by optimising the duty cycle in order to maximise the total efficiency (η) of the inverter. We apply a combined minimisation algorithm comprised

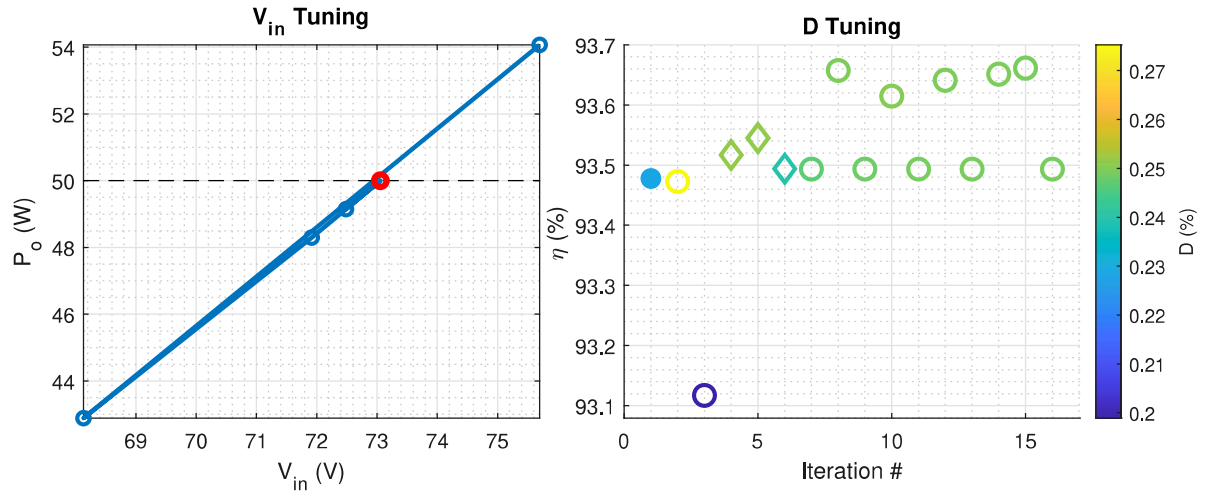


Figure 2.25: Tuning progress of the input voltage to achieve the desired output power level (left), which is indicated with the dashed line, and the optimisation search of the duty cycle for maximum efficiency (right). The blue circles on the left graph indicate the intermediate points during the solving process and the red one is the final result. On the left graph, the full circle represents the initial point, the rhombuses are points found with golden section search, and the circles are derived using parabolic interpolation.

of golden section search and parabolic interpolation methods, which are explained in more detail in [67, 66] to find the local minimum of $-\eta$ within a predefined range. The progression of the duty cycle search of the minimiser is given in Figure 2.25 and the corresponding algorithm parameters used for our example are shown in Figure 2.10.

The SS waveforms of the final design of the Class EF₂ inverter model are given in Figure 2.24, and the resulting adjusted parameters and performance metrics of the tuning algorithm are shown at the bottom section of Table 2.10. At this point, it must be clarified that the efficiency on the vertical axis of the right graph in Figure 2.25 includes the losses of the link due to the Q factor of the primary coil, whereas the efficiency value stated in Table 2.10 corresponds to the efficiency of the inverter only (which is the most common way of defining efficiency in the literature). In both cases the provided power from the gate drive signal is incorporated in the calculations. The efficiency of the real world setup is expected to be lower due to the losses of the gate drive circuit, which the model of an ideal signal generator cannot capture, however the power consumption of the gate drivers for GaN devices can be regarded as negligible compared to the losses of the power components, because of their relatively low input capacitance.

A clearer picture of the percentage distribution of the losses, including the losses of the Tx coil, are given in the pie chart in Figure 2.26. The aim of a low current design, as mentioned

in subsection 2.4.4, results in relatively low heat dissipation of the passive components. The ZVDS condition and low duty cycle design also contributes to achieving low conduction and switching losses on the device. Also, the correct frequency tuning of the ϕ -branch to the desired frequency is confirmed from the Fourier coefficients distribution of the output current in the left graph of Figure 2.26, where the amplitude of the 2nd harmonic is suppressed. The contribution of tuning the ϕ -branch to the second harmonic is also reflected in the low THD value of the output current (Table 2.10).

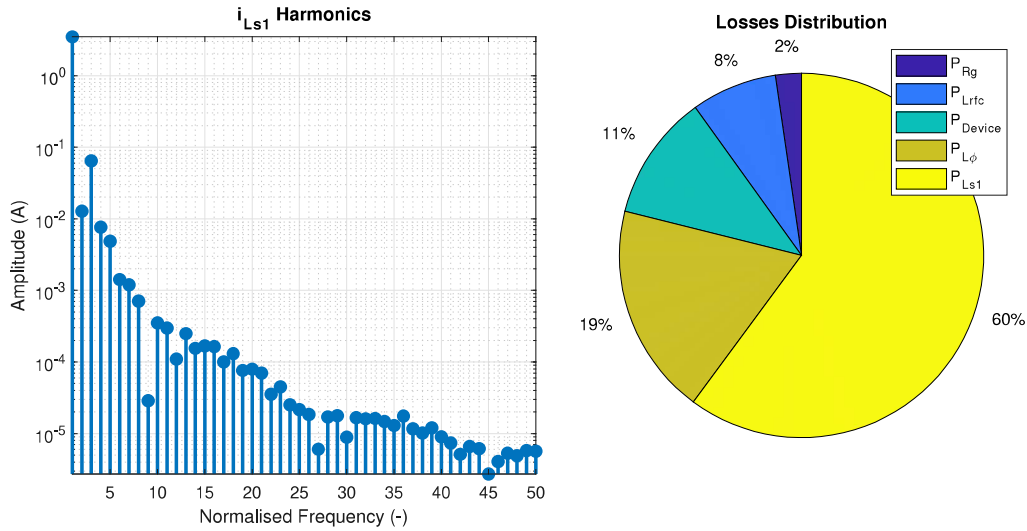


Figure 2.26: Amplitude of the output current Fourier series coefficients (left) and relative distribution of the total losses of the Class EF₂ inverter (right).

2.8 Experimental Verification of the Inverter Performance

2.8.1 Overview

A photograph of the experimental setup of the Class EF inverter board, IPT link, and AC load board connected to the Tektronix MSO58 mixed signal oscilloscope is shown in Figure 2.27. In addition, we use the Fluke Ti400 infrared camera for monitoring the temperatures of various components on the inverter board and the Yokogawa WT310 digital power meter for measuring the inputs of the system. A more detailed image of the inverter board is shown in Figure 2.28, where the top and bottom view of the 3D populated PCB model is presented. The switching signal for the gate driver can be generated either directly from an external signal generator (TTi 100MHz Arbitrary Waveform Generator TGA12104) or a frequency divider formed by a

crystal oscillator (SG-210STF from Seiko Epson Corporation) and a flip-flop (NC7SV74 from ON Semiconductor), using a potentiometer at the RC stage for duty cycle control. The gate driver signal and input DC voltage were provided with external power supplies (U8032A from Keysight and N8741A from Agilent Technologies, respectively).

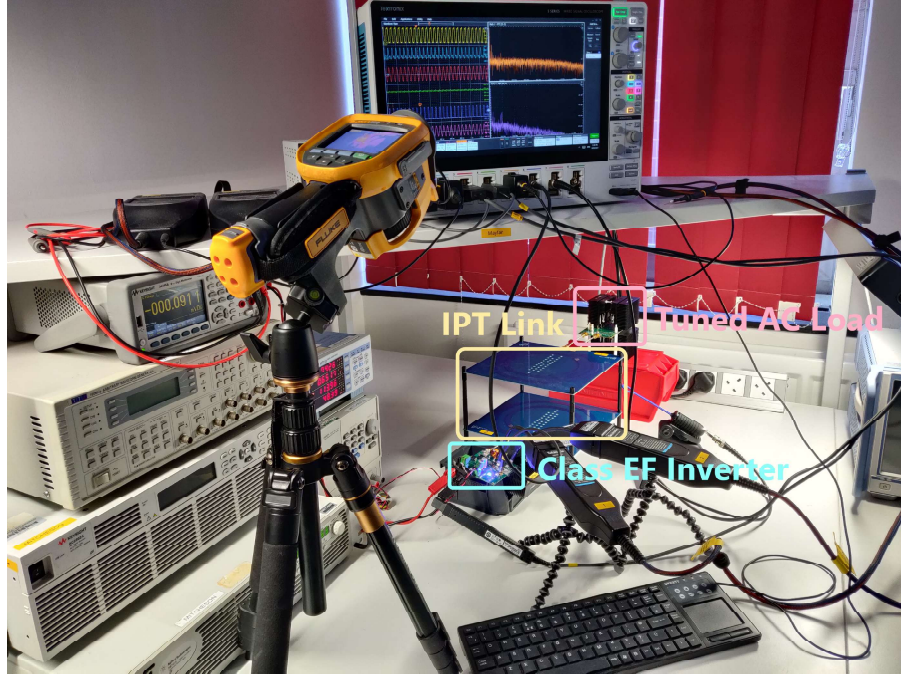


Figure 2.27: Photograph of the final experimental setup during operation connected to the oscilloscope for performance verification. The individual parts of the system are highlighted accordingly.

The measured waveforms of the inverter board over a range of various loading situations are shown in Figure 2.29. Measurements across indicative loading situations over the entire possible load variation range are taken, for more accurate post-measurement characterisation of the inverter and evaluation of the degree of precision of the tuning algorithm and simulation methods. The measurements of v_{C_p} and v_{C_ϕ} are done using the Tektronix TIVH08 probe with the SQPIN 500X sensor tip cable, since they provide accuracy over a combination of high bandwidth and high voltage [111]. For tracking $i_{L_{rfc}}$ and $i_{L_{s1}}$ we use the current probes in [74], because their coupling with the IPT link is minimal. The input voltage to the gate of the GaN device is measured with a Tektronix TPP1000 probe. The power meter measurements are presented in Table 2.11, along with the duty cycle, input voltage and equivalent reflected load for each case.

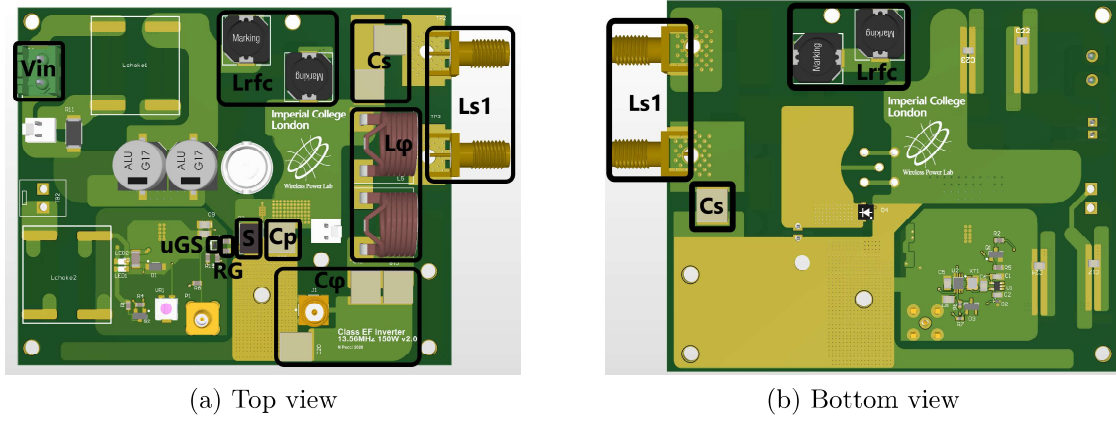


Figure 2.28: 3D model of the Class EF/ Φ inverter PCB. The common mode choke tracks as well as the capacitor voltage dividers are shorted in the real board and the anti-parallel diode is removed. The Tx coil is connected to the SMA connectors.

Table 2.11: Experimental measurements and Tx impedance error correcting parameters for the LTspice simulation

		Unloaded	Semi-loaded	Optimal	Overpowered
R_{sL}	(Ω)	0.346	2.5	8.6	8.6
V_{in}	(V)	75.25	75.25	75.25	125.09
D	(%)	25.17	25.17	25.17	30.85
P_{in}	(W)	5.52	18.05	48.58	153.58
R_{in}	(Ω)	1025.6	313.86	116.57	101.89
$p_{L_{s1}}^*$	(%)	1	1	1	1
$p_{R_{sL}}^{**}$	(%)	30	0	-3	-3

$$^*L_{s1}^{LTspice} = (1 + p_{L_{s1}}) L_{s1}^{E4990A}.$$

$$^{**}R_{sL}^{LTspice} = (1 + p_{R_{sL}}) R_{sL}^{E4990A}.$$

2.8.2 Error Analysis

The corresponding LTspice simulations to the measurements are also given for comparison in Figure 2.29. For the simulation, we use some correction parameters to compensate for the possible Q factor measurement errors of the IPT link, which are given in the last rows of Table 2.11. These parameters are set to achieve the best matching to the experimental waveforms. As expected, the inductance measurement of the Tx coil, as well as the equivalent series resistance for the link instances with higher coupling are extremely accurate, given the HF measurement condition. However, a 30% adjustment was required for the real part of the impedance of the Tx coil when uncoupled, which is in agreement with the limitations of the measuring instrument, according to [72].

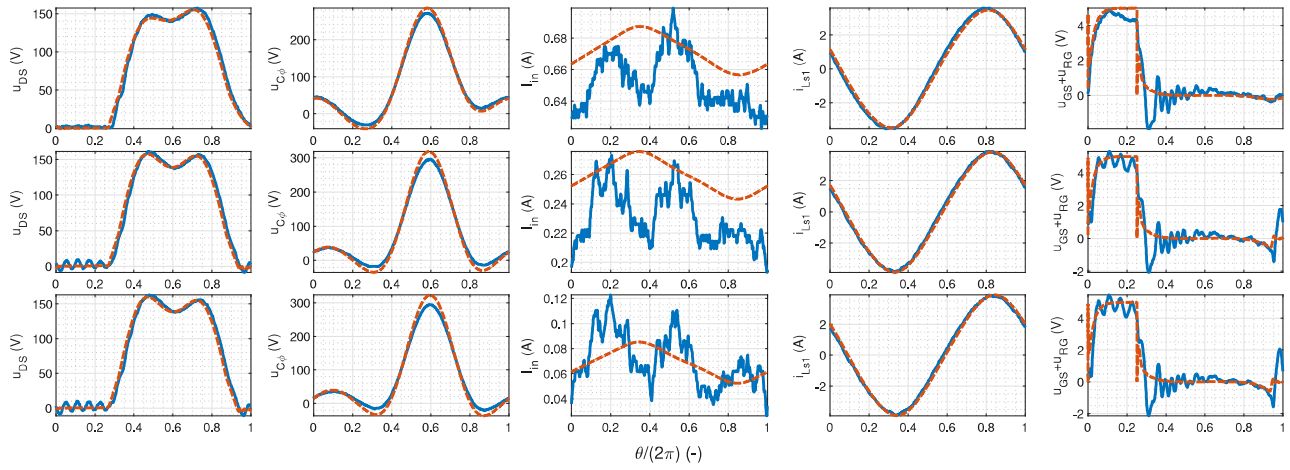


Figure 2.29: Comparative display of the experimental waveforms of the inverter extracted from the oscilloscope (blue) over the corresponding outputs of the LTspice model, with 75 V input voltage along different coupling ranges. The first row shows the fully loaded system, as described in (2.65), the second row shows the results for the same load coupled over a larger gap ($R_{sL} = 2.5 \Omega$), and the third row is the completely uncoupled case.

Some of the errors between simulation and measurements can be attributed to measurement artifacts. The mismatch of the voltage across the ϕ -branch is due to the error introduced by the high attenuation of the probe ($2 \times 500X$) combined with offset accuracy limitations of the oscilloscope. The main cause of the noise on the input current measurement is that the choke inductors chosen have an SRF below the switching frequency of the inverter. The placement of the probe used for the measurement of the input gate voltage resulted in it being affected by the magnetic field of the IPT link as well as introducing parasitics to the gate path, which results in noise on the gate signal and a slight delay to the measured drain voltage compared to the simulation.

Other errors between the theoretical expectations and measurements can be attributed to inaccurate modelling. For example, the higher amplitude oscillations of the real drain voltage, which are more prevalent when ZVDS is not achieved, are due to an underestimation of the stray inductance of the GS66504B packaging combined with PCB track inductances in the drain path. The spikes during transition of the LTspice input gate voltage are a simulation phenomenon caused by the switching of different turn-on and turn-off resistance values. In addition, as shown in Figure 2.14, the behaviour of the simulation model of the GS66504B is not in complete agreement with its datasheet. However, the most important limitation of the simulation method is that the behaviour of the passive elements in the inverter can be more accurately approached to capture a larger range of frequencies if a more complex network of

passive elements is used to model them. A demonstration of this fact is shown in the existence of higher frequency harmonics of the Tx current present in Figure 2.30, compared to Figure. 2.26. Although this modelling complexity can be easily incorporated to our proposed simulation method so that the tuning of the inverter does compensate for the resonant effects of the passive components, it increases the computational requirements disproportionately to the advantages it offers. This is further supported by the practically insignificant level of deviation between the waveforms of Figure. 2.24 and Figure. 2.29 which show the primary voltages and currents in the circuit.

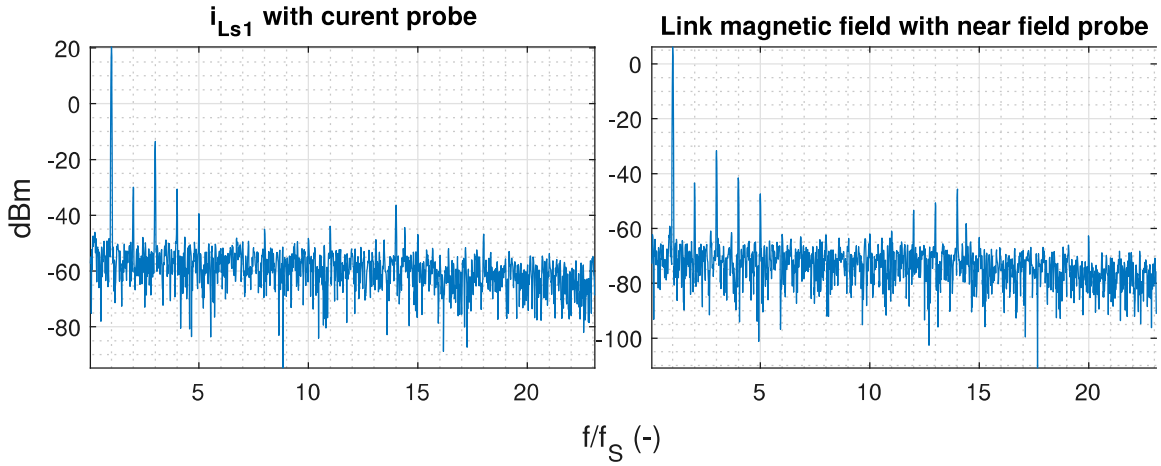


Figure 2.30: Spectrum view from the oscilloscope of the output current measurement using a current probe (left) and a qualitative representation of the magnetic field close to the IPT link using a near field probe. The relative positioning of the link and the near field probe is shown in Figure 2.27.

The tracking of the progression of specific error metrics with regards to the experimental measurements as the algorithm transitions between its various stages is displayed in Figure 2.31. The normalised deviation of both the components values and waveforms matching is provided. The general form of the error metric we use for evaluating the accuracy of simulation waveforms is the normalised MAE

$$\frac{\text{MAE}(u)}{U} = \frac{\sum_{i=1}^N |u_i^s - u_i^e|}{UN}, \quad (2.176)$$

where u is the waveform, U is the normalisation parameter, N is the discretisation number, the superscript s refers to simulation data, and the superscript e refers to experimental measurements. Since the DC component of v_{DS} and v_{C_ϕ} is set by V_{in} , we normalise the MAE of

these waveforms accordingly. The MAE of $i_{L_{s1}}$ is normalised using its measured RMS value. The rest of the absolute error metrics are normalised using the corresponding experimental measurement.

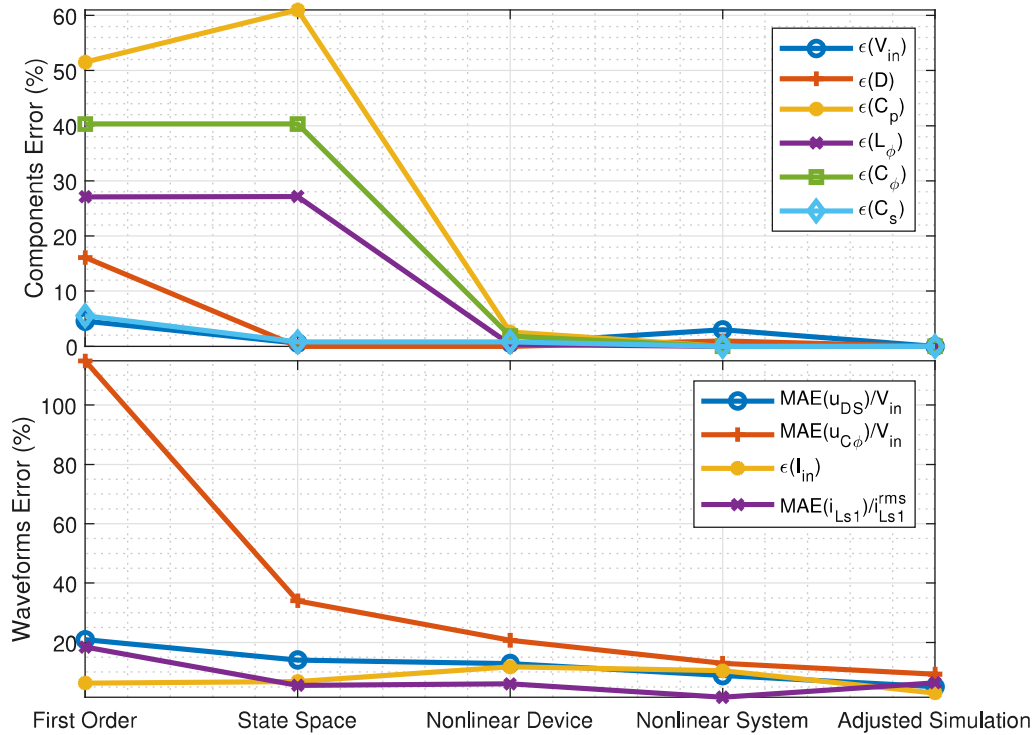


Figure 2.31: Progressions of error metrics regarding the component values and the waveforms fitting between the tuning algorithm stages and the experimental data. The percent error (ϵ) is based on the absolute change and the fitting metrics of the waveforms are normalised using experimental data. For the case of the input current we used the DC values of the waveforms, to filter out the noise of current probe measurements.

Overall, for our Class EF₂ example, we observe that stopping the design procedure at the FO stage produces component values that are between 5 % and 50 % away from the true experimental values. After the final part of the algorithm, the component errors have been eliminated and the accuracy of the waveform simulations has been improved two to twelve times, depending on the case. Furthermore, the limitations of the first order modelling due to the boundary definition in Figure 2.3 is reflected to the fitting error of v_{C_ϕ} in Figure 2.31, and the accurate predictions of v_{C_ϕ} are crucial for reflected load estimation techniques [112]. It must be noted that the computational penalty for achieving these results is insignificant compared to the benefits, since the total computation only takes a couple of minutes to run on an Intel Xeon E5-2630 v3 CPU using Matlab R2020b.

As mentioned before and verified by Figure 2.31, the FO stage is only used to provide an initial

estimation to be used as starting point for the iterative tuning schemes that follow, and none of the component values that are derived from this stage remains unaltered as the algorithm progresses. The SS stage contributes mainly to the adjustment of V_{in} , D and C_s , whereas the third step corrects the ϕ and shunt networks. The last part of the algorithm acts as a final fine tuning stage, which in our case turned out to be unnecessary because of precise selection of passive components and low parasitics of the device.

2.8.3 Verification through Implicit Measurements

We use the spectrum view option that the MSO58 offers to derive the graphs in Figure 2.30. The magnitude, i.e. the vertical axes, can only be measured in dBm, assuming a 50Ω impedance, which makes the data in Figure 2.30 useful only in a qualitative way. For the near field measurements of the magnetic field created by the inductive link we use the 25 mm Aaronia RF Near Field Probe. Both measurements include the filtering effect of the second harmonic on the output of the inverter, which verify the simulated model in Figure 2.26. Since the effect of the ϕ -branch is tested indirectly, we conduct two different kinds of measurements to avoid any room for error.

The thermal performance of the inverter is shown in Figure 2.32 across a variety of operating conditions. The images were captured after the inverter was running long enough to achieve steady state temperature. No active cooling is used and the heatsink only attaches to the bottom part of the board where the GaN device is located. The components that tend to be stressed the most, according to Figure 2.32, are in agreement with the power distribution predicted in Figure 2.26. The small form factor of the transistor makes its thermal dissipation challenging and this is reflected in the measurements. The inductor in the ϕ -branch also is a significant cause of loss because of its finite Q factor. The final component that undergoes significant heating is the series load capacitor, because of the high output current, as shown in Figure 2.24. In Figure 2.26 the ohmic losses of the capacitors are included in the corresponding series inductances, so high temperatures of C_s were expected.

Since the design procedure is defined so that the inverter is optimised for a single operating point, we expect maximum efficiency to be achieved when the full load is connected, which is confirmed from Figure 2.32c. As the distance between the two coils increases, decreasing the

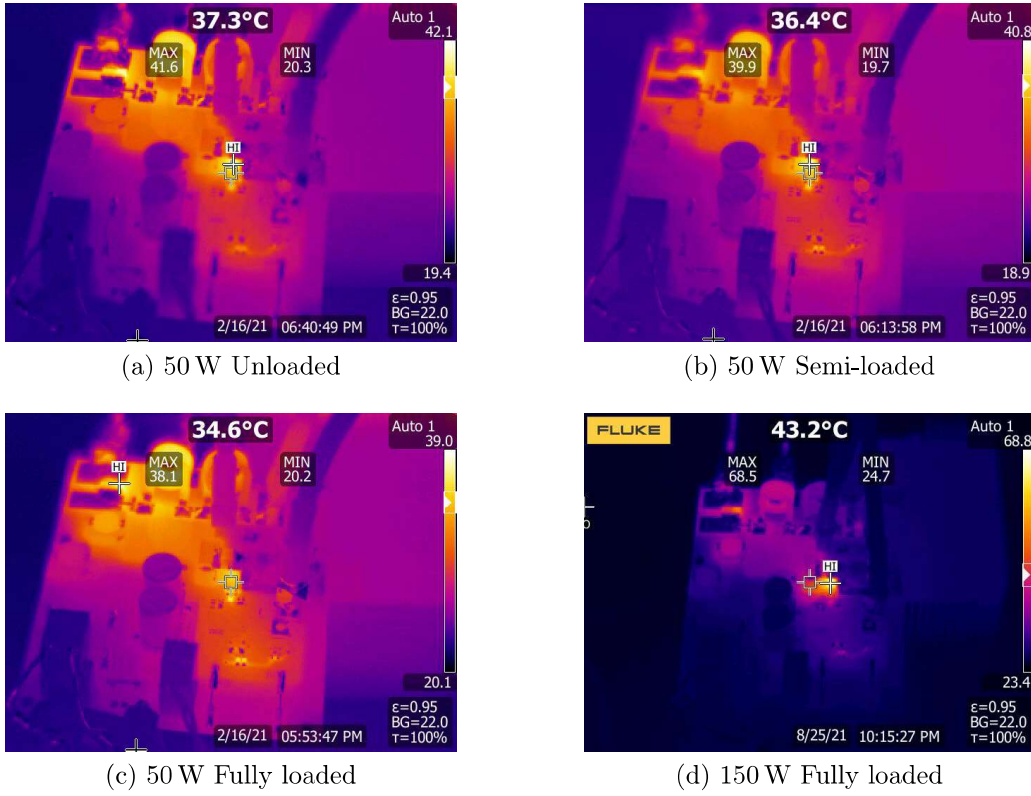


Figure 2.32: Thermal image of the inverter board during operation using the infrared camera for four different loading and powering scenarios. As we deviate from the optimal operating point (c), the thermal stresses on the components rise. The safe thermal limit of the design with the given passive cooling solution is shown in (d).

coupling, the efficiency starts to drop and temperatures rise. The worst case scenario is when the Tx coil is completely decoupled from the load, which is confirmed in Figure 2.32a. For this reason, the power consumption of the freewheeling inverter in Table 2.11 is higher than the expected losses in the board when running under full load. Combined with the Tx Q factor correction in Table 2.11, the theoretical efficiency statement in Table 2.10 holds. However, these temperature deviations are very subtle and the inverter can in practise operate safely across the full range of possible couplings.

The inverter is supposed to be capable of operating not only among a range of coupling factors but also with various power levels supplied. The descending nature of C_{oss} while the drain voltage increases (Figure 2.14) and its direct correlation with the effective value of C_p , combined with the fact that efficiency-wise, reverse conduction is a much more preferable operation condition compared to hard switching, makes the optimal input voltage the lower bound of supplied power level. The upper limit of V_{in} , for the given thermal solution used in our experimental setup, is also given in Table 2.11, which corresponds to three times the optimal

power. A comparative presentation of the v_{DS} and v_{GS} waveforms from measurement and LTspice simulation is given in Figure 2.33, and the accuracy of the simulation method and measurements is confirmed again. The thermal image of the inverter for this operation instance is shown in Figure 2.32d, where now the switching device clearly becomes the limiting factor. It should be noted that by increasing the input voltage from the optimal value, with the optimal load connected, the device starts reverse conducting, and thus the overall efficiency drops because of increased conduction losses. We compensate for this effect by increasing the duty cycle manually, until ZVS is achieved.

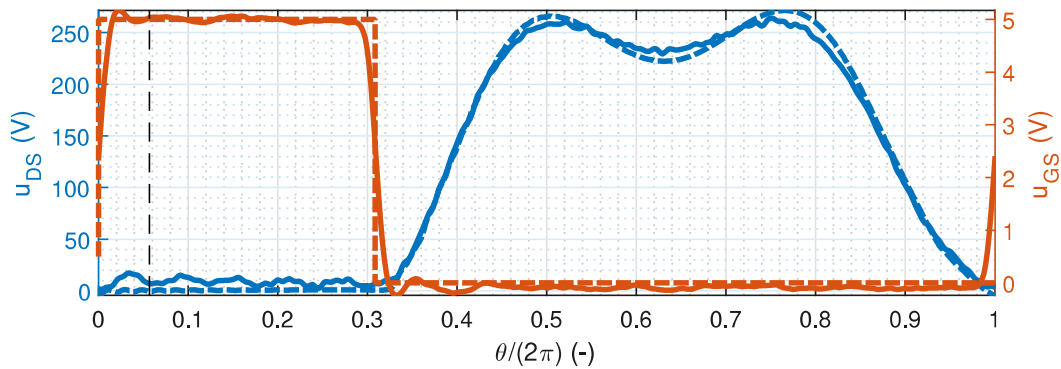


Figure 2.33: Drain voltage and gate signal from experimental measurement (solid line) and LTspice simulation (dashed line) for Class EF₂ inverter with the maximum input voltage that the given thermal dissipation setup allows for safe operation. The duty cycle is manually adjusted to avoid reverse conduction and decrease the power consumption of the switching device, with the dashed black line representing the turn-on time point of the non-adjusted duty cycle.

2.8.4 Load-independent Design Experiment

In order to further showcase the capabilities of our proposed design method, we apply it to the load independent Class EF inverter introduced in [1]. We use the same inductive link, load, power level and transistor as in the main body of this chapter, however the circuit design inputs are completely different to the Class EF₂ example, as can be confirmed from Table 2.12. This way a direct comparison between the two can be made, since the application remained the same.

The final component values of the experimental setup as well as measurements are given in Table 2.12 and Figure 2.34. The level of agreement between experimental and simulated waveforms in Figure 2.34 again confirms the high accuracy of our tuning method. The change in

Table 2.12: Inputs, outputs and measurements of the load independent Class EF inverter example.

	Quantity	Value	Unit
Inputs*	τ_ϕ	1.7	—
	λ	4	—
	i_S^{ON}	−4	A
Outputs	V_{in}	57.33	V
	D	34.82	%
	C_p	65.252	pF
	L_ϕ	320.01	nH
	C_ϕ	147.521	pF
	C_s	126.79	pF
Measurements*	P_{in}	50.19	W
	R_{in}	65.487	Ω

*Including the data of previous relevant Tables.

simulation accuracy when comparing the first step of the algorithm to the last can exceed 120 % and component values can be off by more than 300 %. The output capacitance from Figure 2.14 of the device at input voltage for our two experimental examples is quite similar, however the change in C_p in Figure 2.31 and Figure 2.35 is different by seven-fold. This observation confirms that the widely accepted technique in the literature of using the mean of the drain voltage to calculate the effective output capacitance of the device is oversimplified and unreliable. Interestingly, after the efficiency maximisation during the fourth step of our algorithm, the final design was slightly hard switching, as can be seen in Figure 2.34, which although being seemingly unusual agrees with the definition of "optimal operation" in [49]. Indeed, slight hard switching, reduces device stresses and increases power capability, which is even more effective in non ZVDS conditions.

The THD of the Class EF₂ example is below 1 %, whereas on the load independent one is 9 %. This is visually noticeable from the output current waveforms in Figure 2.29 and Figure 2.34 and is a consequence of the ϕ branch resonant frequency of the two instances. Although the load independent design has significantly larger duty cycle than the EF₂, the latter has over 40 % higher power capability, assuming equal output power. Notwithstanding that precise efficiency measurements on an AC load can be challenging at MHz frequencies, since the two setups share the same link, we can calculate their efficiency ratio using only input power and output current measurements. The Class EF₂ example is 16 % more efficient overall. By combining

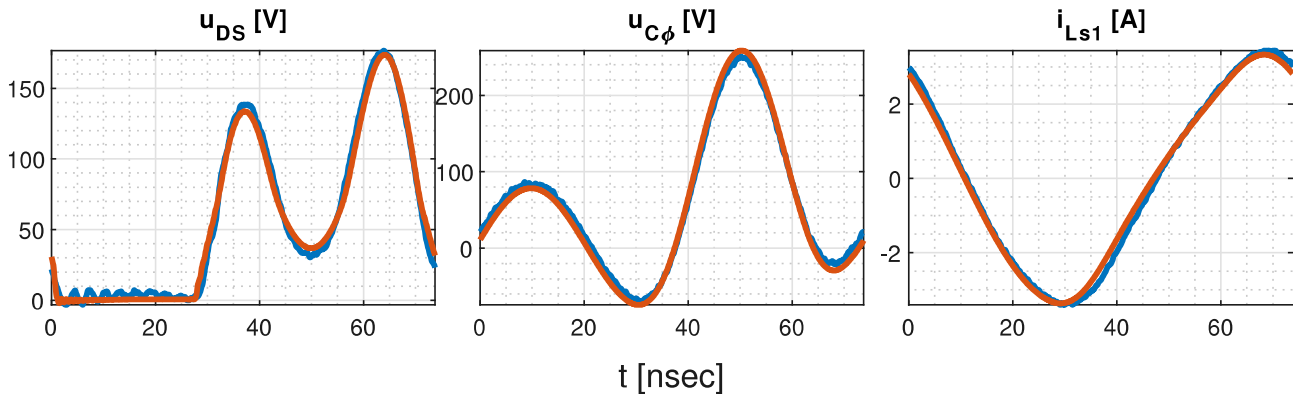


Figure 2.34: Simulated (orange) and measured (blue) waveforms of the the voltage across the drain and the ϕ capacitor and output current of the load independent Class EF inverter example.

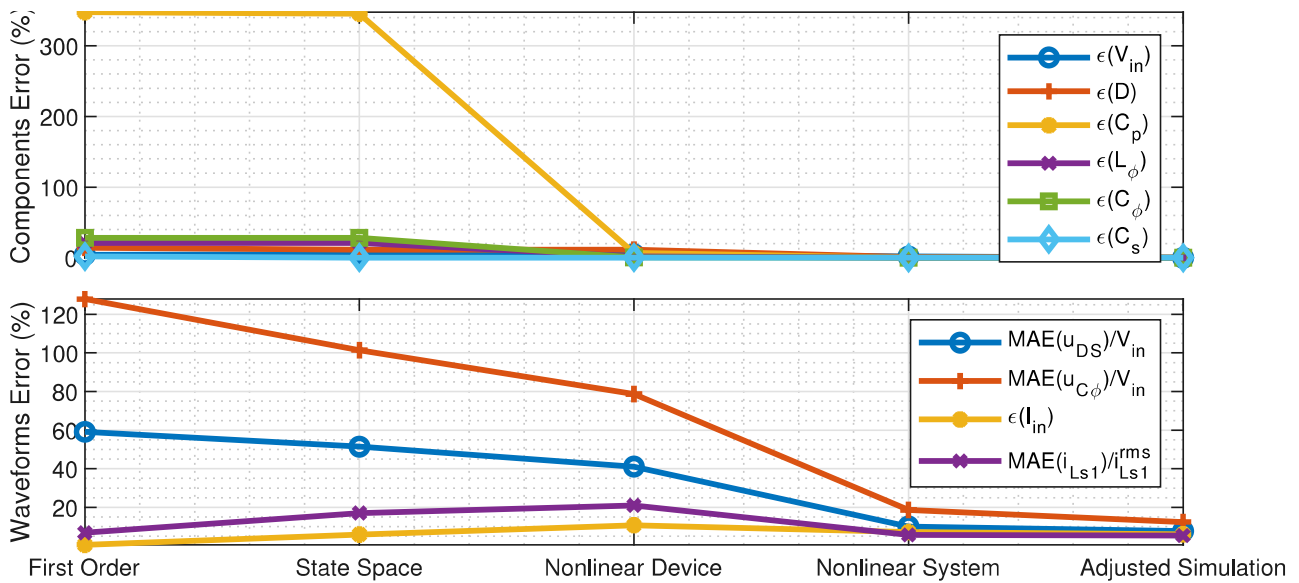


Figure 2.35: Progression errors of the tuning algorithm in correspondence to Figure 2.31 for the load independent Class EF example.

the simulated ϕ branch current and the corresponding Q factor, the losses on L_ϕ on the load independent example are roughly three times higher than its counterpart. Lastly, the device temperature on the EF₂ is half of that on the load independent.

2.9 Conclusion

A detailed and thorough description and application of a novel proposed algorithm, along with the underlying mathematical expressions, is presented for designing Class EF/ Φ inverters. The algorithm can easily be implemented in computer code and offer an automated solution for

determining the component values of the circuit with high accuracy. All design equations and calculation details are provided in order to make this work completely reproducible.

The design procedure offers to the user the ability to determine a variety of operating parameters (loading factor, Φ -branch frequency, drain current at turn-off), according to the requirements of the application. The algorithm is general and covers both finite and infinite choke topologies. The proposed method is divided into four subroutines, where each consecutive one offers higher accuracy compared to the subsequent one, and can be terminated after any of these four stages, depending on the level of detail of available measurements.

The algorithm is then applied to design a Class EF/ Φ inverter and the experimental results match the simulation without the requirement of manual retuning. This example includes the effects of both linear networks for simulating passive components as well as non-linear semiconductor modelling. The level of accuracy achieved from this work is demonstrated and verified with experiments. Having the level of control that this algorithm provides over the behaviour of HF resonant systems, as in the case of HF-WPT applications, can enable us to confidently define the safe operation limits of the system. This is also confirmed experimental. The work in this chapter has been published in [61, 113].

Chapter 3

High Power Designs

3.1 Introduction

3.1.1 Background

In general, components suitable for high frequency applications tend to be physically small, since smaller structures naturally have less parasitic energy storing capabilities, and thus exhibit higher resonant frequencies. On the other hand, devices capable of handling high power tend to be physically large, since this property enables them to dissipate heat more effectively and thus avoid being damaged during operation. This fundamental and unavoidable contradiction, however, is the core reason that makes building high power HF IPT systems an engineering challenge.

As explained in chapter 1, the inverter topology with the highest power capability is the Class D full-bridge. High power IPT applications at switching frequencies in the order of 10's of kHz have been demonstrated using silicon MOSFET [114] and IGBT [115] in the literature. However, at MHz switching frequencies the effect of the parasitic inductances of the PCB layout combined with the increase in switching losses and severity of EMI issues because of hard switching [116], make this kind of inverters impractical for HF IPT applications.

Even though Class E type inverters are capable of operating efficiently at higher frequencies, the upper limit is set by the output capacitance of the device. For this reason, granted that Si power

MOSFET and IGBT modules can handle high currents and voltages, their large C_{oss} , combined with the high gate charge requirements and large parasitic inductances because of their typical packages [37], makes these power transistor technologies unsuitable at MHz frequencies.

GaN devices overcome all of the above mentioned issues, with low input and output parasitic capacitances and compact dies that can fit in low inductance packages [10, 117]. The power capability of Class E type inverters is bound by the high drain voltage requirements, which depending on the specific topology can be several times over the DC bus level [28]. At the moment, commercially available GaN transistors typically have a maximum drain voltage of 650 V [89], which is a major limiting factor when attempting to scale up the power of a Class E inverter, and reduces efficiency as we are forced to use designs with high currents and low voltages. There are some devices based on GaN that state drain voltages up to 0.9 kV [118], however these are based on a cascode structure with a Si MOSFET and lose the reverse conduction properties of a pure GaN device.

SiC technology offers higher breakdown voltages than GaN, with commercial devices going as high as 1.7 kV [119], and can withstand higher operating temperatures. A high power IPT DC/AC system has been demonstrated at 3 MHz [120], based on a push-pull Class E inverter. A comparison of two Class Φ_2 2 kW WPT inverters was conducted at 6.78 MHz in [121], one being a single ended design with a custom 1.2 kV SiC for reduced parasitics, and the other a push-pull with GaN. The inverter with the GaN still had higher operating efficiency, despite having twice the amount of components. In addition, the gate requirements of GaN are very simple, whereas SiC devices usually need both positive and negative gate levels, and have a high gate charge. The effect of the SiC package on the inverter losses is demonstrated in a 13.56 MHz 2 kW Class Φ_2 design in [122].

3.1.2 SiC - GaN Comparison

As an illustrative comparison example we run LTspice simulations using GaN and SiC devices with around 30 A current rating on a 3 kW push-pull Class EF_2 inverter, at two switching frequencies, 3.39 MHz and 6.78 MHz. The gate is an ideal voltage source without gate resistors, to eliminate non-ideal gate driving effects on the overall circuit. We use the inductance values of coils shown in Figure 4.13. The Rx is a resonant 50 Ω AC load with impedance transformation

to achieve the desired reflected resistance value of $15\ \Omega$.

The circuit diagram of the system is shown in Figure 3.1. The GaN device is the GS66508B from GaN Systems and no reverse diode is used, since GaN transistors have practically no reverse recovery charge. The commercial SiC device is the 1.2 kV C3M0075120J combined with the C4D10120H diode, both in TO packages. The custom SiC device has the UJ3N120065K3S transistor with the UJ3D1210K2 diode in a single QFN package for low inductance. The gate and drain waveforms of the devices are given in Figure 3.2, where the drain voltage is kept below 650 V for a fair comparison between GaN and SiC. All the examples are tuned to achieve both ZVS and ZVDS.

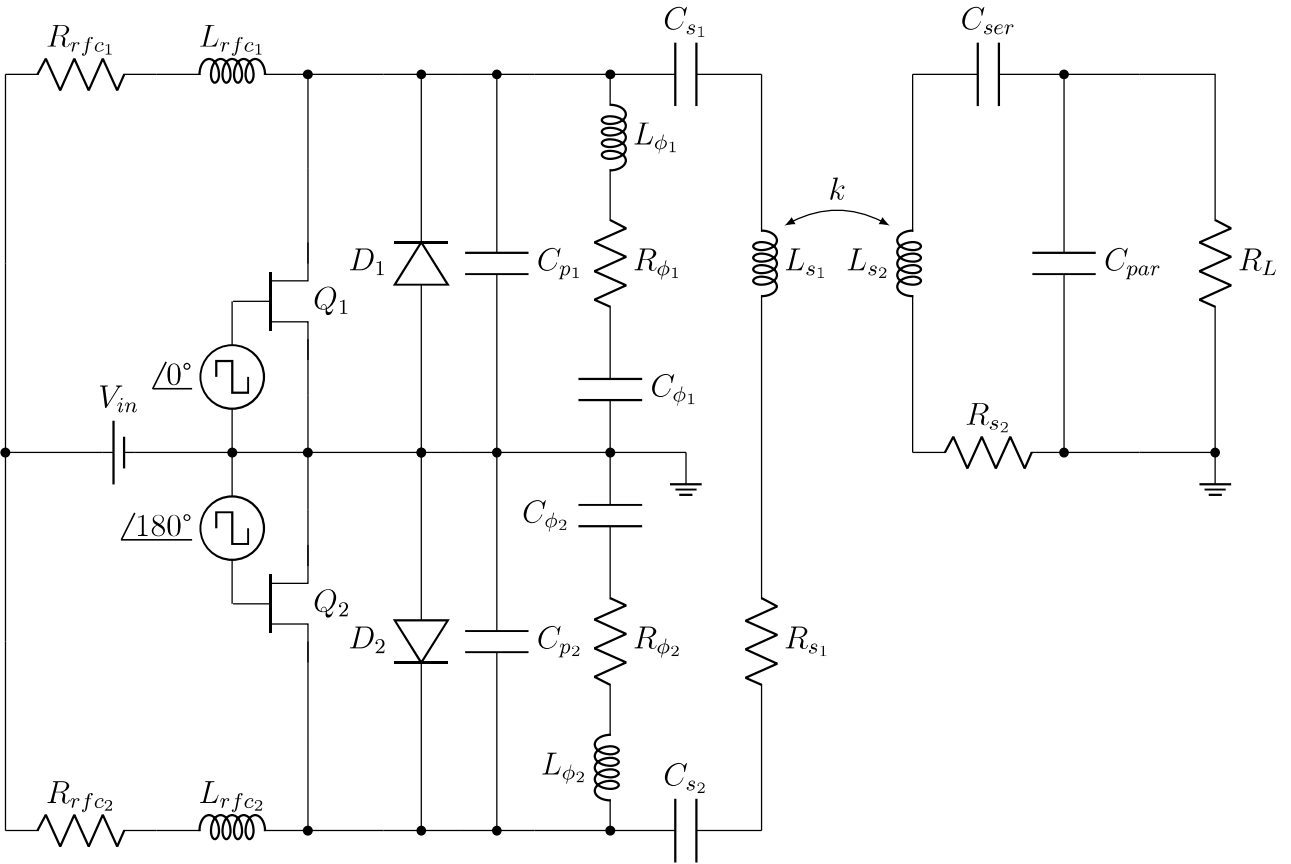


Figure 3.1: DC/AC system used to compare GaN and SiC performance in an HF IPT system. The system consists of a push-pull Class EF inverter with an AC load on the Rx side.

Measurements on inverter efficiency, device losses and gate requirements are given in Figure 3.3. Here, we also include measurements from designs with 1.2 kV drain voltage, in order to investigate the benefits of having SiC devices operating at their full potential. Overall, The GaN based inverter has the highest efficiency, lowest power losses and lowest gate power required.

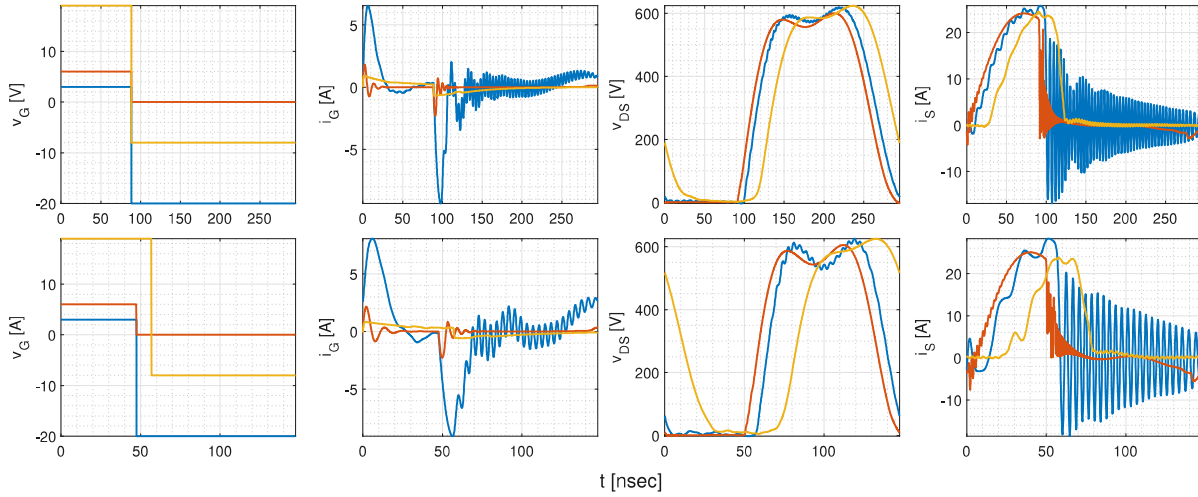


Figure 3.2: Gate and drain waveforms of the voltages and currents of the GaN and SiC devices in the system shown in Figure 3.1. The blue waveforms are from the UJ3N120065K3S, the orange are from the GS66508B, and the yellow ones are from the C3M0075120J device.

When comparing the effect of the drain voltage limit across designs with the same device and at the same frequency, the 1.2 kV designs have higher efficiencies, which was expected. The SiC device from Wolfspeed is too slow even for operation at 3.39 MHz, which can be confirmed both from the switching delays in Figure 3.2 and the high device consumption at Figure 3.3. The main reason for the slow switching speed is the high gate resistance of the device ($9\ \Omega$ according to [123]), which limits the gate current, as shown in Figure 3.2. On the other hand, the custom QFN packaged SiC achieves fast switching speeds, without lagging significantly from the overall efficiency figures of the GaN examples. The ringing in Figure 3.2 can be reduced with an external gate resistance, in the expense of switching losses, and can be further improved with lower stray inductances in the package.

An experimental prototype of the GaN version using the GS-065-030-2-L transistor was built but could not maintain efficient operation above 2.16 kW, because of the coil characterisation difficulties explained in section 4.2. The experimental inverter PCB is shown in Figure 3.4 and the drain and primary coil current waveforms at maximum power are shown in Figure 3.5.

The benefits of the Class EF over the Class E when it comes to power capability have been discussed in chapter 2, and it is the main reason that the Class EF/ Φ topology is generally preferred for high power, high frequency applications in the literature. A 600 W DC/DC WPT system has been developed using a push-pull load independent Class EF inverter with GaN devices at 6.78 MHz [124]. Alternative configurations of the Class Φ_2 push-pull topology have

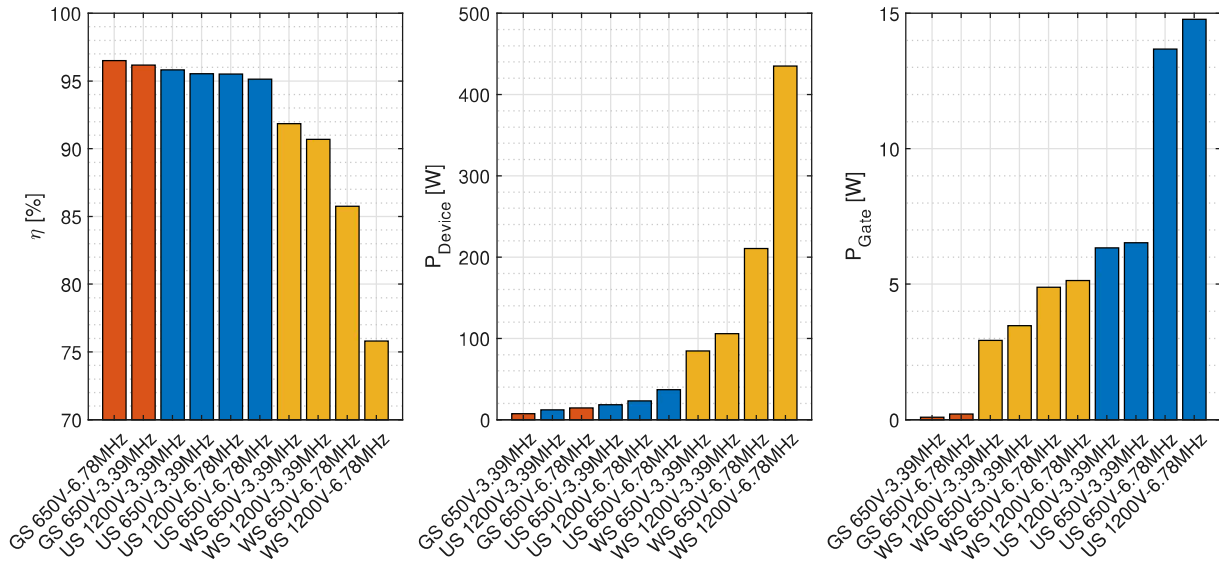


Figure 3.3: Bar charts with measurements of efficiency, device losses, and gate requirements for various design examples of the system in Figure 3.1. The GaN devices are in orange, the commercial SiC devices are in yellow, and the custom SiC devices are represented with blue.

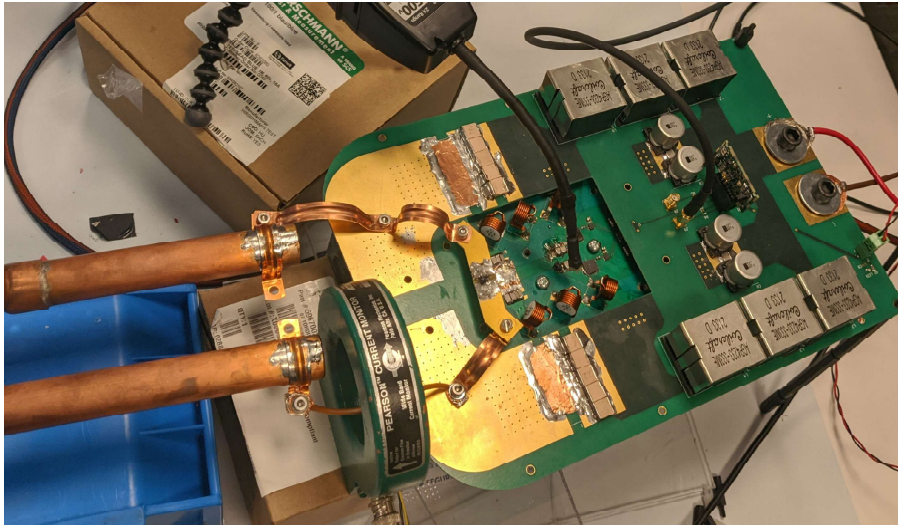


Figure 3.4: Push-pull GaN based inverter driving the coil shown in Figure 4.13a.

been proposed in the literature, with even lower device voltage stresses by combining the ϕ -branch in [125], and center-tapped choke and single ϕ -branch inductor in [48].

However, the conduction losses on the ϕ -branch inductors scale up with power, which makes achieving high efficiency challenging at high power applications. This is not the case for switching losses, so it is preferable to increase the amount of switching devices to scale up the power. In addition, it is also preferred to use GaN, despite its limited drain voltage limit. Furthermore, as the current on the coil increases, the heating on the output capacitors also needs to be taken into account. In this chapter we propose a circuit configuration of paralleling push-pull

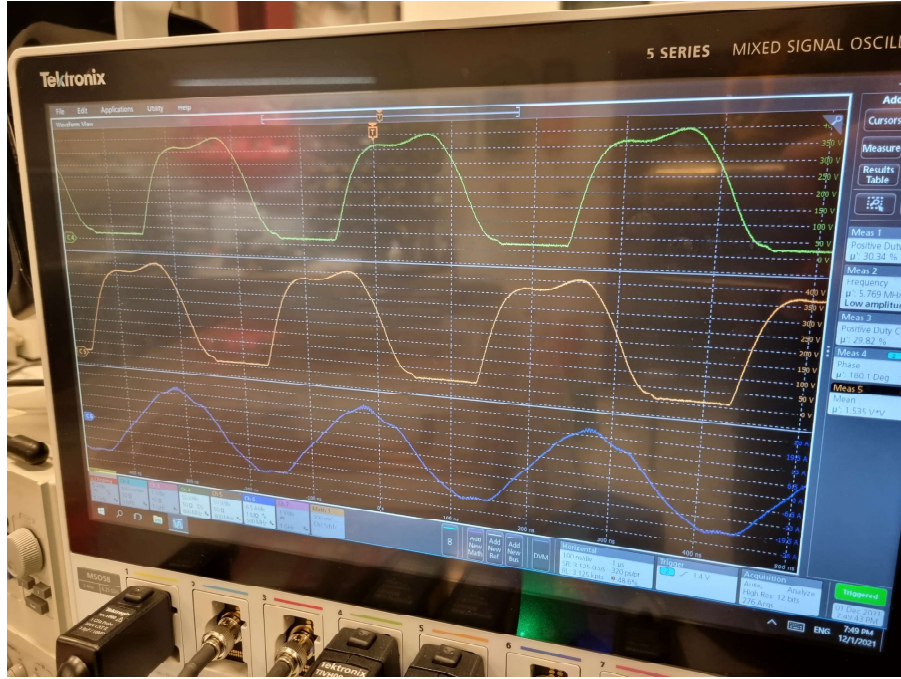


Figure 3.5: Drain (orange and green) and primary coil current (blue) waveforms of the inverter board in Figure 3.4. The non ideal shape of the output current is due to the noise floor and distortion caused by the Rogowski current probe, since the measured amplitude is relatively low for the sensitivity of the instrument.

inverters to increase the power output, while keeping the individual component stresses low. Such approach enables us to overcome the power capability limitations of the Class E topology combined with GaN devices, while benefiting from the high efficiency. We also introduce a modified differential Class DE topology with a single input choke, which maintains the benefits of a Class DE inverter without the need of input filtering.

3.2 Parallel Inverter Combination

3.2.1 Outphasing Modulation

The concept of combining the AC outputs of two resonant inverters (can be either the current or the voltage [36]) into a common load to create a fixed frequency, phase controlled (PC) converter was first introduced in the literature in [126], and has been used both with Class D [127, 128, 129] and Class E [130, 131] topologies. Apart from output power modulation, the phased controlled topology also has the advantage of delivering to the load double the maximum power of each individual inverter, whilst keeping the component stresses to the equivalent of

half the output power. This latter feature is the one that is of interest in this chapter, since we investigate ways of increasing the output power of a HF-IPT system, beyond the electrical limitations of the transistors and the rest of the passive components.

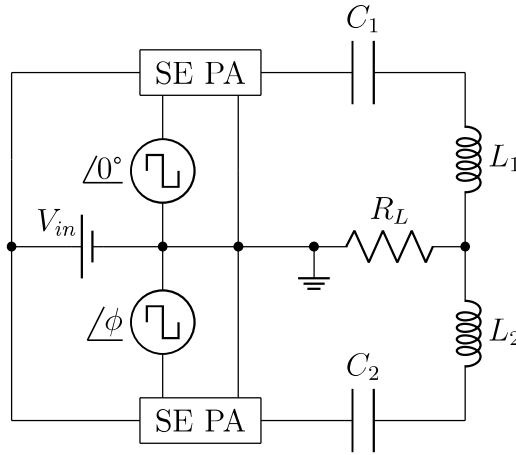
The high level block circuit diagram of a generic resonant PC inverter is shown in Figure 3.6. The main difference between the PP configuration in Figure 1.7 and the PC configuration in Figure 3.6a is that the the output inductor in the PC case is not part of the common load. So, even though both the PP and the PC topologies provide to the load double the power of each individual stage, only the PP is suitable for IPT applications. A possible but suboptimal way of adjusting the circuit in Figure 3.6a to drive a primary coil would be to fully resonate the coil at the switching frequency and connect it as the output load, as shown in Figure 3.6b. This approach, however, negates the benefits of using the primary coil inductance as part of the output resonant tank of the inverter, and has reduced efficiency because of the additional large output inductors required.

3.2.2 Circuit Analysis

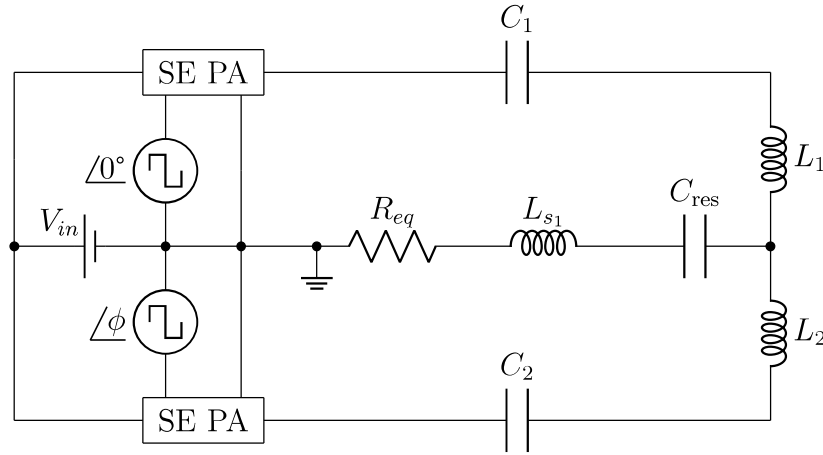
Parallel Push-pull Configuration

Our objective in this section is to increase the power throughput of the PP configuration even further by combining it with the PC approach, with the resulting topology still being applicable for IPT systems. This can be achieved by setting the phase of the PC configuration to zero and replacing the SE inverters with differential ones. The output coil can now be connected in parallel with the PP inverters and by applying a specific impedance transformation, it can also maintain resonance with the individual output branches of the PP inverters. This setup obviously loses the PC property, but achieves the power combination of multiple PP stages, and is not limited to just two.

A visual example of such a parallel push-pull configuration based on two Class E inverters (but can be any kind of resonant topology) driving a single Tx coil is shown in Figure 3.7. There are four discrete points of connection in this topology: A, B, C, and GND. The common power supply is connected between points A and GND, and the primary coil is connected between points B and C. The input of each PP inverter is connected to point A and the outputs are



(a) Typical PC inverter not suitable for IPT



(b) Suboptimal PC inverter suitable for IPT

Figure 3.6: Circuit block diagrams of a current driven PC inverter, where ϕ is the phase modulating the output power to the load R_L , $C_{1/2}$ and $L_{1/2}$ form the output resonant tank, and C_{res} is fully resonating with the primary coil at the switching frequency.

connected to B and C. It is important that each of the points B and C is only connected to the same phase branch of the PP part. As already known, the PP topology has twice the power output of the equivalent SE one. In turn, the parallel PP topology of Figure 3.7 has twice the power capability of a single PP stage, i.e. quadruple the power of a SE inverter. Of course, this kind of configuration is not limited to only two PP stages as shown in Figure 3.7.

The design method for a parallel push-pull topology is similar to the simple push-pull case, with some key modifications. For a given primary coil loaded impedance $\bar{Z}_{sL}$ and output power P_o of each SE stage, the corresponding PP configuration has $2\bar{Z}_{sL}$ loaded primary coil impedance and $2P_o$ total output power. In turn, a parallel PP configuration of N stages using the above SE design has a loaded output impedance of $2\bar{Z}_{sL}/N$ and total output power $2NP_o$. The rest of the inverter components, including the input power remain unchanged from the SE stage.

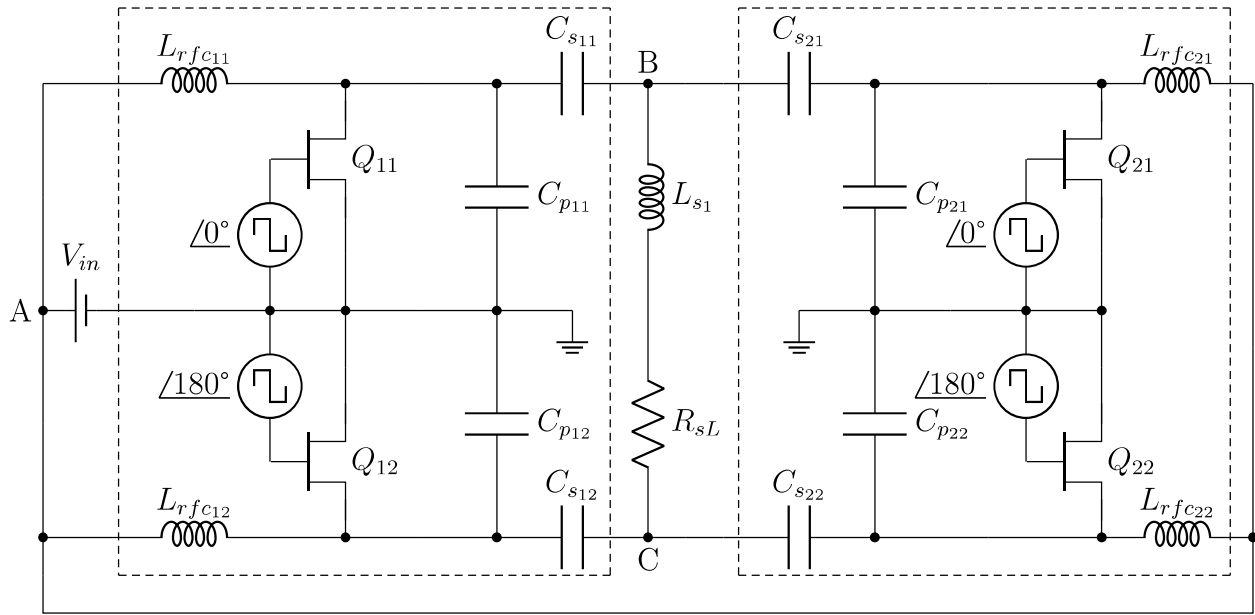


Figure 3.7: Parallel connection of two push-pull Class E inverters on a common loaded primary coil, supplied by a common voltage source, to form a parallel push-pull configuration.

An interesting observation for the special case when $N = 2$, as in Figure 3.7, is that both for the discrete SE inverters as well as for the whole parallel PP system, the output impedance is identical, which simplifies the design process, as well as the dynamic analysis of the inverter behaviour under varying load.

Parallel Single-ended Configuration

This type of parallel combination of the outputs of inverters to a single Tx coil is not limited only to PP topologies, but can also be similarly applied to SE converters. The equivalent version of the inverter in Figure 3.7 but with SE circuits is shown in Figure 3.8. Again, the supply voltage is connected between points A and GND, but the Tx coil is now connected between points B and GND. Obviously, this means that the output current is not differentially driven in the parallel SE case and the topology does not exhibit the even harmonic cancellation effect of its PP counterpart. In addition, the input current ripple also is additive among the individual stages and not cancelled out as in the PP case. The total output power is MP_o , where M is the number of total SE stages, and it is equivalent to the parallel PP topology. The loaded coil impedance however now is $\bar{Z}_{sL}/M$, which is significantly lower compared to the parallel PP.

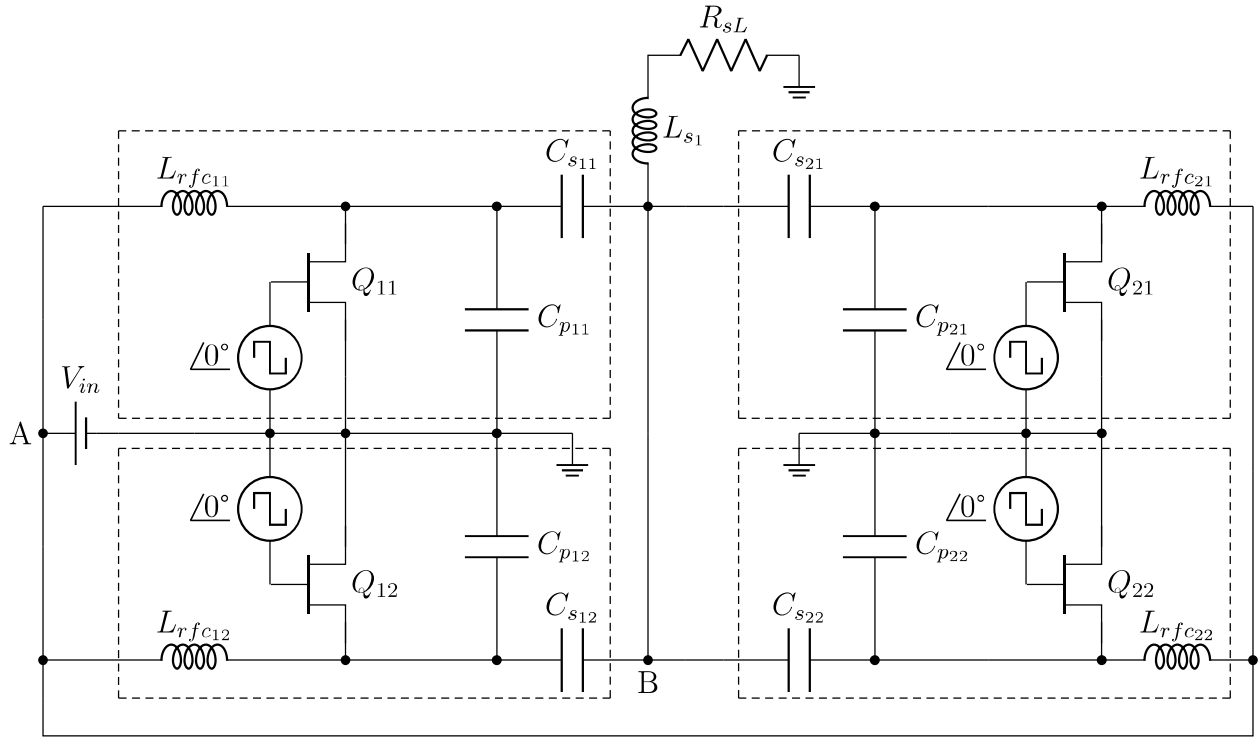


Figure 3.8: Parallel connection of four single-ended Class E inverters on a common loaded primary coil, supplied by a common voltage source, to form a parallel single-ended configuration.

Comparison of Component Stresses

A thorough comparison of the component values and stresses between the different topologies is shown in Table 3.1. The data in Table 3.1 are general and the overall outcomes are applicable to any resonant converter topology, in an analogous way. Table 3.1 has four inverter configurations: single-ended, push-pull, parallel single-ended, and parallel push-pull. All of the inverters are driving the same primary coil and reflected resistance, and provide the same output power, to give a fair and representative comparison. The data in Table 3.1 are all normalised to the values of the single-ended case, so that the results are relative to a specific standard.

Overall, the configuration showcasing the best performance and lowest component stresses from Table 3.1 is the parallel PP topology. It combines the reduced voltage stresses and input current ripple of the PP with the reduced current stresses of the parallel SE. A more common way of reducing device stresses in converters is by either paralleling transistors to share the current, or connecting them in series to share the voltage drop. This technique, however requires very precise switching timing, otherwise there is risk of uneven loading of the devices, which can cause failure. The parallel PP configuration is relatively resilient to small phase differences in the switching signals, or component imbalances among the individual branches.

Table 3.1: Comparison of component stresses and impedance values among various combined inverter configurations, relative to the simple case of the SE inverter.

	PP	M -parallel SE	N -parallel PP
V_{in}	1/2	1	1/2
R_{in}^{total}	1/4	1	1/4
$R_{in}^{\text{individual}}$	1/2	M	$N/2$
i_{in}^{pp}/I_{in}	1/8	$2M$	1/8
$I_{L_{rfc}}$	1	$1/M$	$1/N$
v_{DS}^{max}	1/2	1	1/2
i_S^{max}	1	$1/M$	$1/N$
$i_{C_{s1}}^{\text{rms}}$	1	$1/M$	$1/N$
$v_{C_{s1}}^{\text{rms}}$	1/2	1	1/2

Also, paralleling transistors increases the effect of the non-linear C_{oss} , and connecting them in series requires high side switching. In addition, this approach does not reduce the stresses on the passive components, which become crucial as the power scales up and conduction losses become significant.

3.3 Current Reduction Techniques

In a resonant inverter, adding extra capacitors between specific points on the circuit can result in reducing the overall current stresses in the topology. For example, in a push-pull configuration that is achieving ZVS through shunt capacitors, the addition of a differential shunt capacitor results in further reduction of the peak transistor current [132, 133]. However, this technique has some limitations in real world operation that have not been addressed in the literature. In a single ended resonant inverter, adding parallel resonance to the primary coil, after the series resonance of the converter, results in impedance transformation of the load, that can also reduce the current stresses in the circuit [19]. Once the topology becomes more complex, e.g. push-pull, parallel push-pull, etc., the exact methodology of applying this kind of impedance transformation is not defined in the literature.

3.3.1 Differential Shunt Capacitor

The circuit diagram of a push-pull Class E inverter incorporating a differential shunt capacitor is shown in Figure 3.9. The parameter r determines the effect of peak current reduction that occurs due to the presence of the differential shunt capacitor. To investigate deeper the benefits and drawbacks of including a differential shunt capacitor we run simulations on a 6.78 MHz, 1 kW push-pull Class E inverter, driving a 2 μ H primary coil with full reflected load of 4 Ω . We include simulation results both for the ideal case, and with the GS66516B transistor, to highlight potential differences when a real transistor model is used. The input voltage is 42 V, the choke is 70 μ H, the duty cycle is 50 % the original shunt capacitance is 2.1 nF, and the series capacitance is 583 pF. For the real device model, the duty cycle is adjusted to 88 % of the ideal case, the shunt capacitance is reduced by 45 %, and a 3 Ω gate resistor is added in order to maintain the same effective drain voltage shape and minimise ringing.

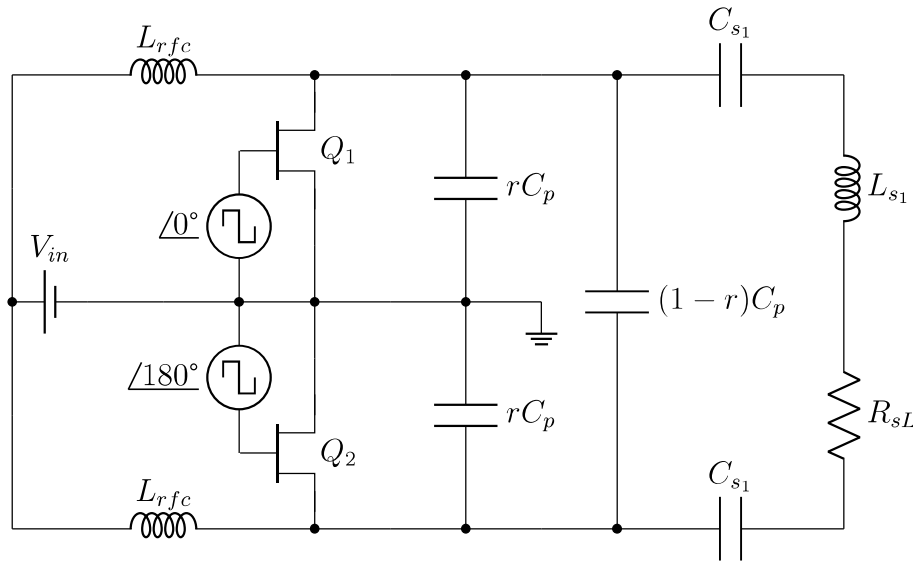


Figure 3.9: Push-pull Class E inverter with a differential shunt capacitor to reduce device current stresses. The value of r ranges from 0 to 1 and controls the effect of the differential shunt capacitance.

The benefit of including a differential shunt capacitor is shown in the drain current waveforms in Figure 3.10. For the ideal case the peak current has been reduced by 29.4 %, which is a significant reduction and can enable us to use a lower rating transistor, such as the GS66508B, which is a 30 A device, instead of the 60 A one currently used. The reduction in the non-ideal case is noticeably less (13.9 %), and is mainly because of the limiting effect that the parasitic output capacitance has to the differential shunt capacitance. However, the shape of the drain

current does not change its mean value, which remains constant around 12 A in all cases. Since the combination of the single ended and differential shunt capacitors form effectively a current divider, the total shunt capacitor current is shared between the two, resulting in reduction of current stresses in those passive elements as well, as shown in Figure 3.11.

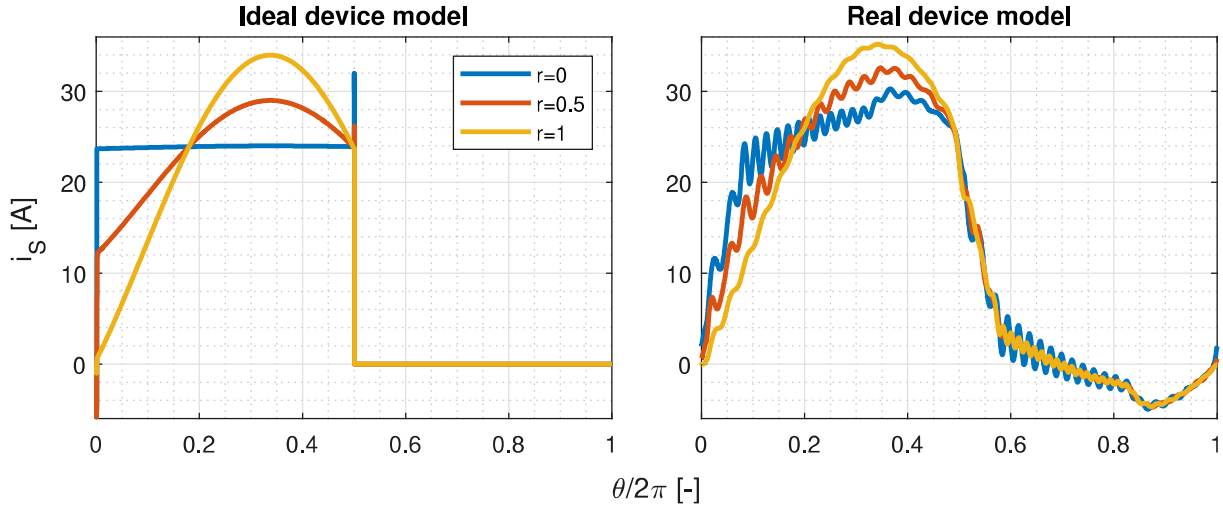


Figure 3.10: Drain current waveforms from the circuit in Figure 3.9, for various values of r . The data on the left are from simulations with an ideal switching device and on the right using the model of the GS66516B GaN transistor. The current spikes on the ideal case are caused from a simulation artifact due to the low R_{DS}^{ON} .

In theory, the addition of the differential shunt capacitor should not alter the overall behaviour of the circuit, with the drain voltage and output current waveforms remaining the same. However, depending on the value of the differential shunt capacitor, the turn on slope of the drain current increases, which combined with the parasitic inductances in the device (and potentially the PCB traces) result in significant ringing on the corresponding waveforms, as shown in Figure 3.10 and Figure 3.11. This ringing even negatively affects the noise level on the drain voltage waveform, as shown in Figure 3.12. But, according to the data in Figure 3.13, reducing the peak drain current with a differential shunt capacitor reduces the power dissipation on the device, with the extreme case of no single-ended shunt capacitor having 5.5 % less power losses compared to the traditional topology, which is in line with the findings in [132].

The main drawback of the differential shunt topology is the strict requirement of a 50 % duty cycle. If the duty cycle deviates from 50 %, either by reverse conduction due to dynamic changes in the load or by design such as the Class EF topology that typically has lower duration of conduction during the period, the current reduction benefits no longer apply. This is because once the drain is shorted to the ground, the differential shunt becomes an open and all of the

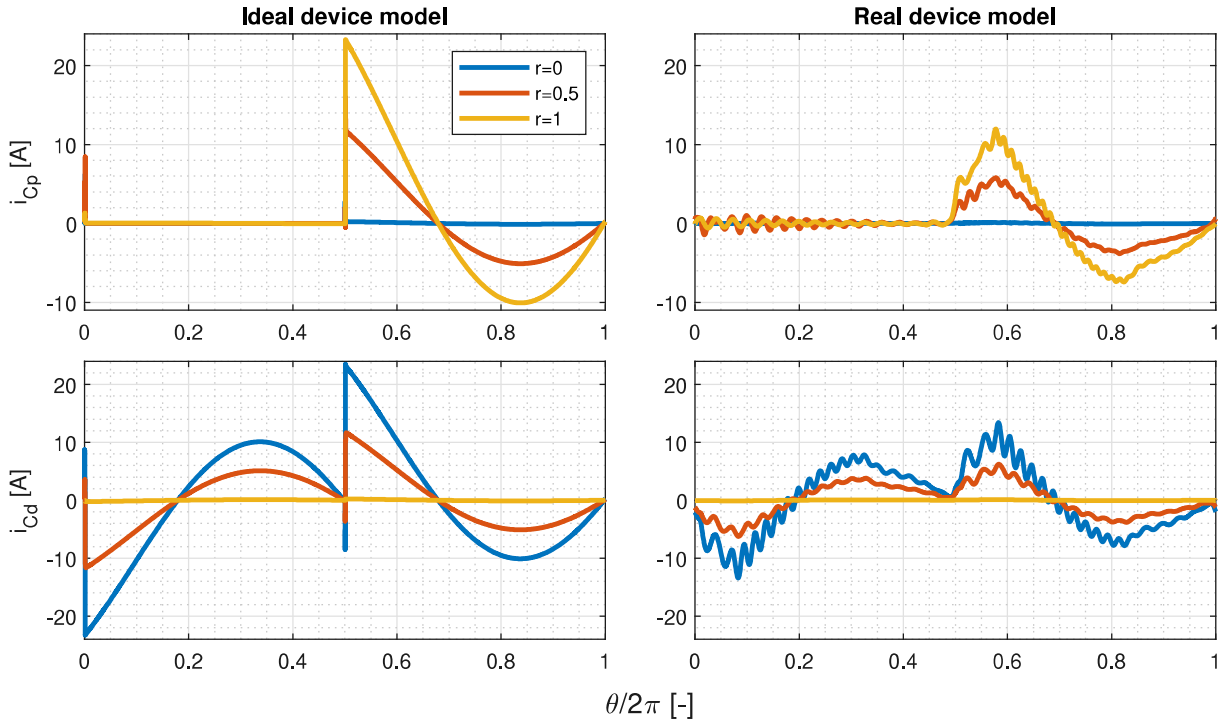


Figure 3.11: Single ended (top) and differential (bottom) shunt capacitor current waveforms from the circuit in Figure 3.9, for various values of r . The data on the left are from simulations with an ideal switching device and on the right using the model of the GS66516B GaN transistor. The current spikes on the ideal case are caused from a simulation artifact due to the low R_{DS}^{ON} .

residual current flows immediately through the drain. This effect is shown in the waveforms in Figure 3.14, where the circuit in Figure 3.9 is simulated with half the nominal reflected resistance, resulting in reverse conduction of the transistors. When the parasitics of the switching devices are taken into account, the ringing in the differential shunt circuit can even surpass the peak transistor current of the traditional topology, which negates the purpose of the differential shunt capacitor in the first place. So, unless the inverter is load-independent with 50 % duty cycle, the differential shunt capacitor technique is not recommended.

3.3.2 Semi-resonance

The performance of weakly coupled IPT systems can be improved in terms of efficiency by connecting a capacitor in parallel to the primary coil, so that it resonates with it slightly above the switching frequency, as explained in [19]. We showcase the effect of semi-resonance by applying capacitors of various values across the primary of the IPT link used in chapter 2, and measuring with the impedance analyser. The results, for a distance between the coils of

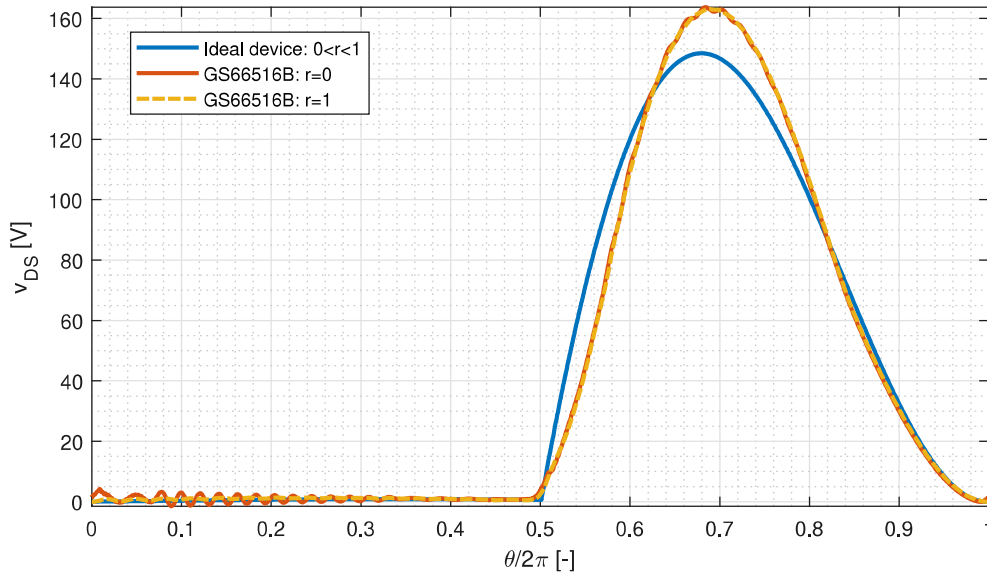


Figure 3.12: Drain voltage waveform of the circuit in Figure 3.9 with an ideal device (blue) for any value of r , and with the GS66516B GaN HEMT for no differential shunt capacitance (yellow), and no single ended shunt capacitors (orange). The difference in the peak value between the ideal and non-ideal case is due to the effect of C_{oss} .

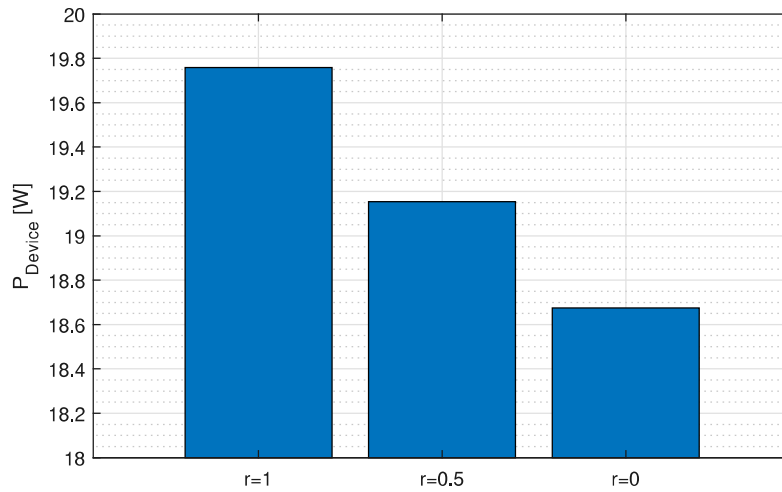


Figure 3.13: Power dissipation on a single device in the circuit in Figure 3.9 for various values of r .

11.3 cm is shown in Figure 3.15. The lowest frequency resonance is from the AC load on the secondary, which is at 13.56 MHz. The three higher frequency resonances are caused by the parallel capacitors connected to the primary coil. The closer the external capacitor resonance is to the secondary resonance, the higher the impedance transformation.

The concept of the impedance transformation that takes place with the inclusion of a parallel

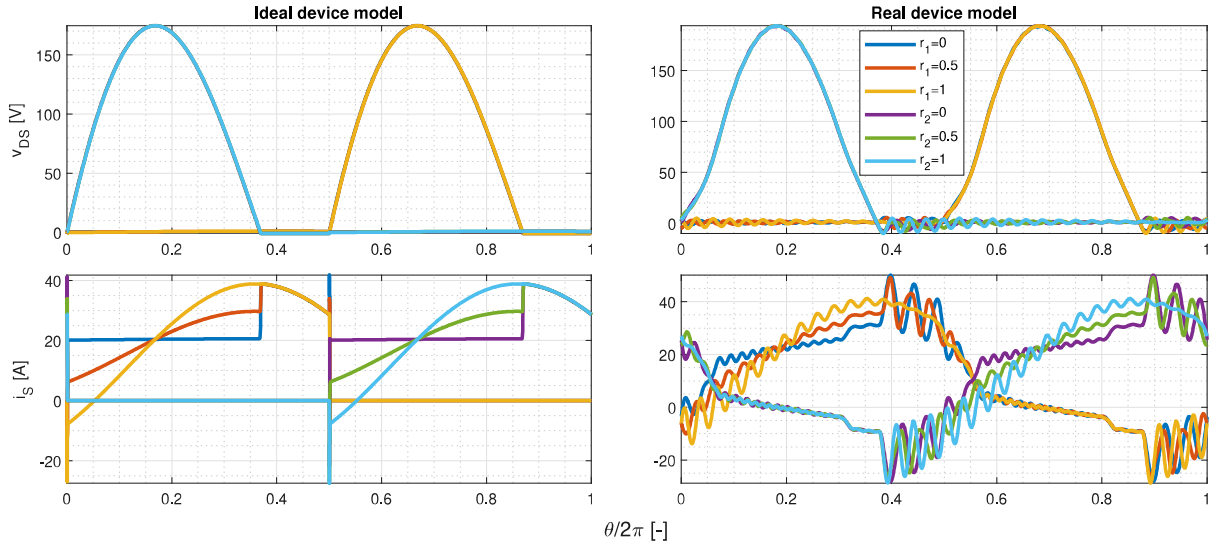


Figure 3.14: Drain voltages (top) and drain currents (bottom) for ideal devices (left) and the GS66516B (right), of the circuit in Figure 3.9 with duty cycle less than 50 %.

capacitor to the Tx coil is shown through the equivalent circuits in Figure 3.16. The process begins by choosing the resonant frequency f_0 of the parallel combination of the loaded primary and C_{sr} , where

$$f_0 = n f_S, \quad (3.1)$$

with $n > 1$. The lower the value of n the larger the impedance increase, according to 3.15. Then, the value of the resonant capacitor is calculated by the relation

$$C_{sr} = \frac{L_{s1}}{R_{sL}^2 + (nX_{L_{s1}})^2}, \quad (3.2)$$

where

$$X_{L_{s1}} = \omega_S L_{s1}. \quad (3.3)$$

The effective value of the impedance of the loaded primary at the switching frequency is given by the equations:

$$R_{sr}(f_S) = \frac{R_{sL} X_{C_{sr}}^2}{R_{sL}^2 + (X_{L_{s1}} + X_{C_{sr}})^2} \approx \frac{R_{sL}}{\left(1 - \frac{1}{n^2}\right)^2}, \quad (3.4)$$

$$L_{sr}(f_S) = \frac{X_{sr}(f_S)}{\omega_S} \approx \frac{L_{s1}}{1 - \frac{1}{n^2}}, \quad (3.5)$$

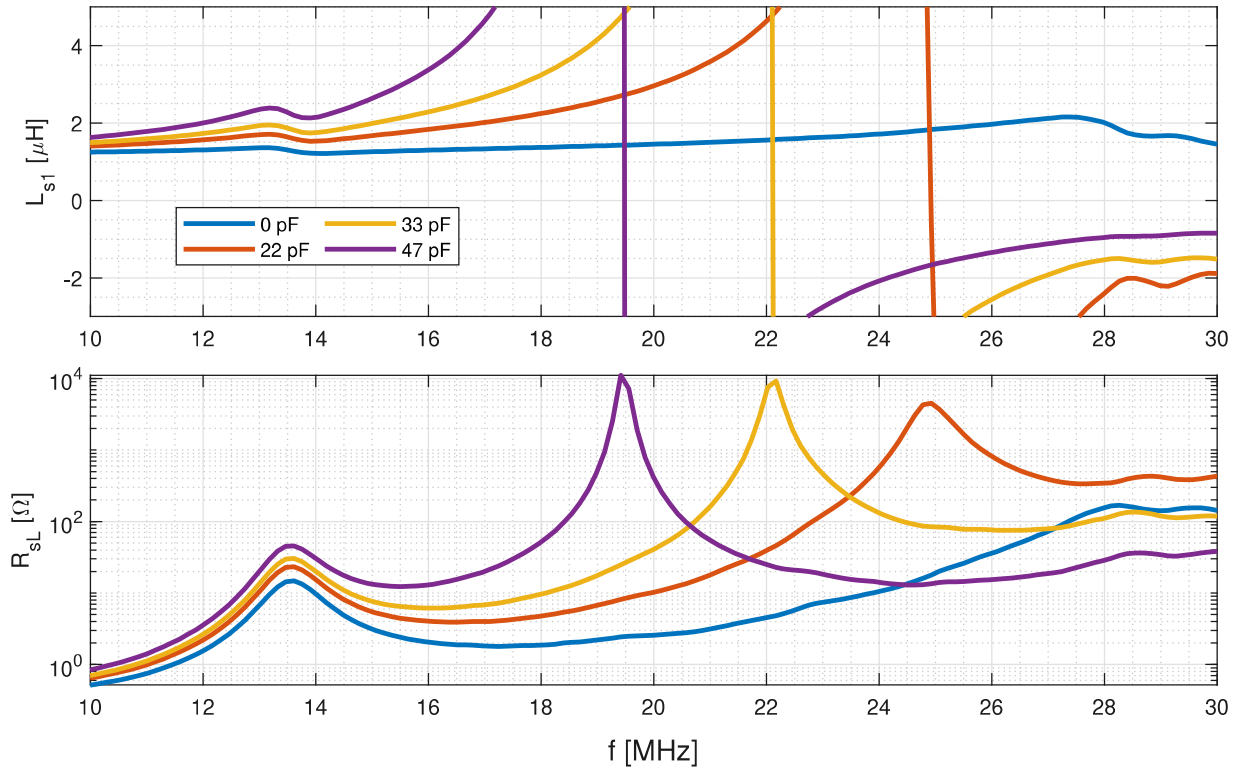


Figure 3.15: Equivalent inductance (top) and series resistance (bottom) measurements, using the impedance analyser on the IPT link and AC load combination used in chapter 2, with various parallel resonant capacitors to the primary coil.

where

$$X_{sr}(f_S) = \frac{X_{C_{sr}} [R_{sL}^2 + X_{L_{s1}} (X_{L_{s1}} + X_{C_{sr}})]}{R_{sL}^2 + (X_{L_{s1}} + X_{C_{sr}})^2}, \quad (3.6)$$

$$X_{C_{sr}} = \frac{-1}{\omega_S C_{sr}}. \quad (3.7)$$

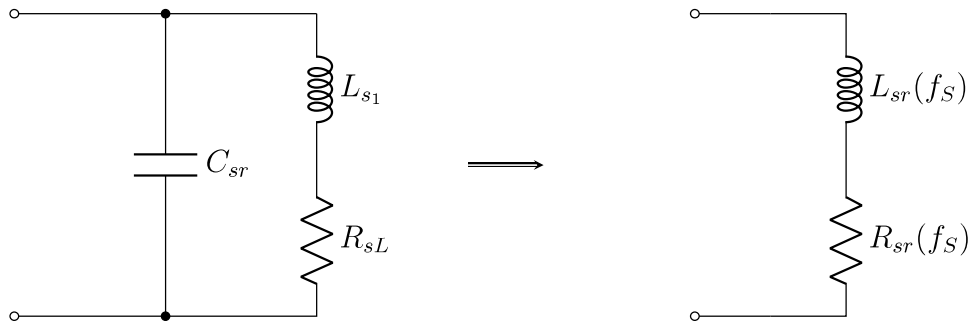


Figure 3.16: Equivalent circuit of the impedance transformation that occurs with the inclusion of a parallel capacitor to the Tx coil.

In a power combining configuration, such as the push-pull and the rest proposed in section 3.2, there are two ways of connecting capacitors to achieve semi-resonant operation, shown in Figure 3.17. The first type of connection is shown in Figure 3.17a and it is the typical configuration

extended to the push-pull topology. The second type is achieved by splitting the resonant capacitor to each branch of the push-pull and connecting them to ground, i.e. Figure 3.17a. Both configurations have the same effect, however the calculation of the value of the capacitors is different in each case.

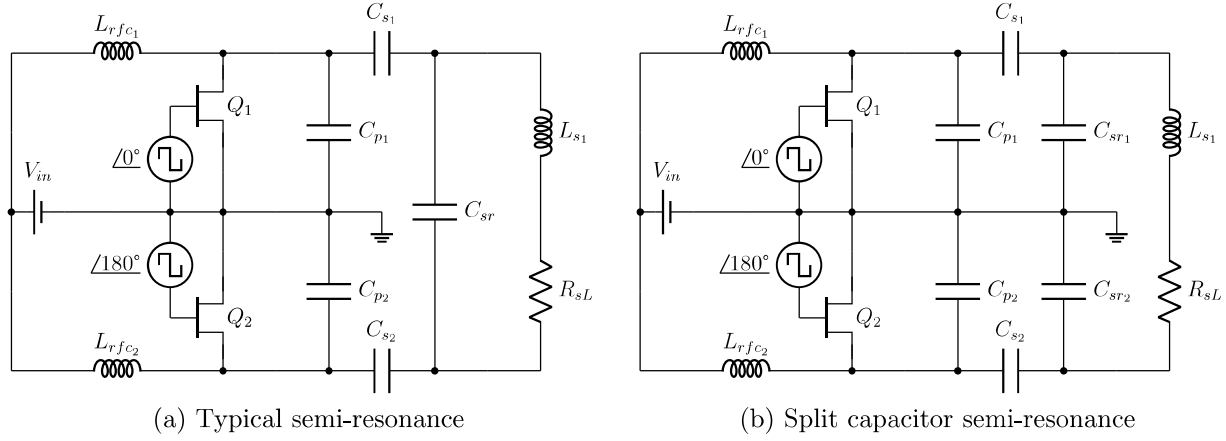


Figure 3.17: Push-pull Class E semi-resonant inverter topology with two variations on the connection type of the resonant parallel capacitors.

For the typical semi-resonant connection type, we follow the process of calculating the value of C_{sr} and the resulting effective impedance of the loaded primary as we would do for a single-ended inverter. Then, we design the single-ended parts of the push-pull inverter based on the equivalent transformed primary loaded impedance. For the case of the split resonant capacitor to ground of Figure 3.17b, the process is the opposite of the traditional connection. First we perform the impedance transformation from the push-pull to the each single ended side, and then we apply the corresponding resonant capacitance value to the effective loaded primary impedance of each side. The values of the resonant capacitor are generally different between the two cases of Figure 3.17, apart from the case of a two stage parallel push-pull inverter, where the real primary loaded impedance matches exactly the equivalent impedance that each single-ended side receives.

To better showcase the properties of the semi-resonant operation, we provide three push-pull Class E inverter simulations with various values of n . All the inverters provide 1 kW on the same primary and reflected load combination. The component values of each case are shown in Table 3.2 with the corresponding waveforms shown in Figure 3.18. Adding semi-resonance effectively reduces the loaded Q factor of the output branch, which in turn results in higher voltages and lower currents in the circuit components. However the voltage across the series

output capacitors and the current on the primary remains the same, since all of the examples have the same power and load.

Table 3.2: Component values of the semi-resonant push-pull Class E inverter examples.

Parameter	$n \rightarrow +\infty$	$n = 3$	$n = 2$	Unit
V_{in}	31.23	35.13	41.65	V
L_{rfc}	70	70	70	μH
f_S	6.78	6.78	6.78	MHz
D	44	44	44	%
R_g	3	3	3	Ω
Q	GS66516B	GS66516B	GS66516B	—
C_p	2.566	1.968	1.157	nF
C_s	765.8	684.32	582.6	pF
C_{sr}^{diff}	-	40.812	91.811	pF
C_{sr}^{split}	-	81.624	183.62	pF
L_{s1}	2	2	2	μH
R_{sL}	4	4	4	Ω

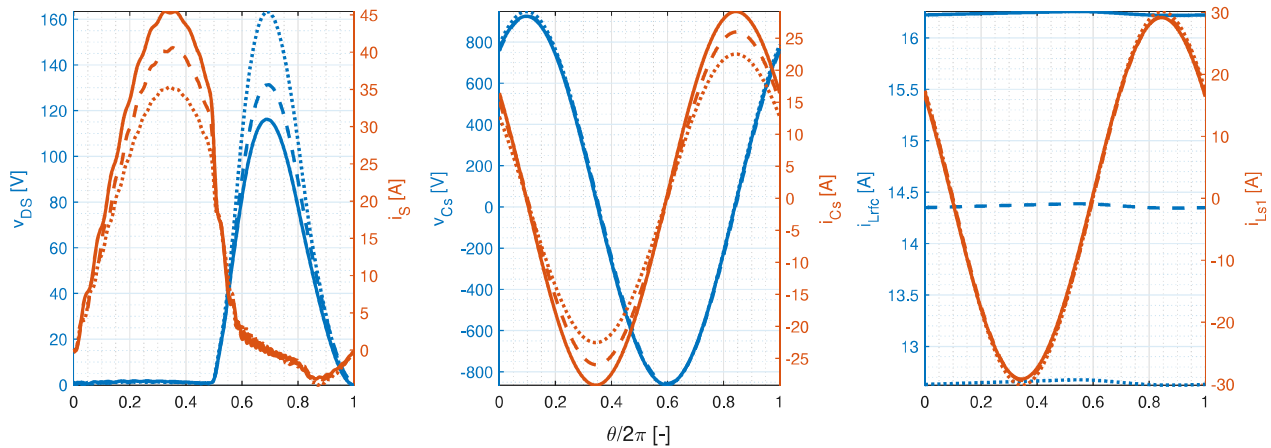


Figure 3.18: Waveforms showcasing the voltage and current stresses of a Class E inverter with various semi-resonance capacitance values. The solid line represents no semi-resonance ($n \rightarrow +\infty$), the loosely dashed line is semi-resonance with $n = 3$, and the densely dashed line is semi-resonance with $n = 2$.

We also compare the current and voltage stresses on the resonant capacitors between the differential connection of Figure 3.17a and the split connection in Figure 3.17b. The split capacitor connection requires lower voltage rating on the components, which is expected since the two split capacitor form a voltage divider. The current however is the same in both cases. Another benefit of the split capacitor over the typical differential connection is that any potential noise because of mismatch between the two branches is absorbed through the ground.

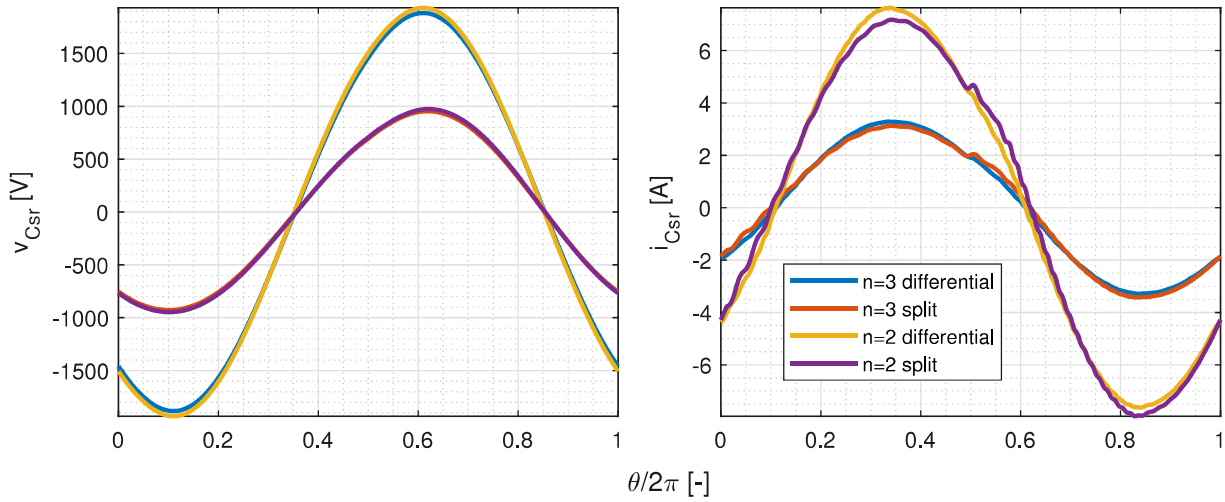


Figure 3.19: Voltage and current waveforms of the semi-resonant capacitors for $n = 2$ and $n = 3$, both for the typical connection across the coil as well as the split connection to ground.

3.4 Common Infinite Choke Push-pull Class DE Topology

As already explained in chapter 1, the Class D topology (Figure 1.10) has the highest power capability, but the hard switching operation suffers from switching losses and EMI issues as the operating frequency rises. The peak drain voltage on the Class DE topology (Figure 1.11) is also capped at the supply voltage, since there is no input choke. The lack of input choke however creates high current pulses, which are parts of the output current, through the supply, which requires additional input filtering.

In this section we propose a push-pull Class DE topology with a common input choke (PPCC Class DE inverter), the circuit diagram of which is shown in Figure 3.20. The circuit diagram of a the single common infinite choke push-pull Class DE inverter topology is the same as of a typical differential Class DE inverter, with the inclusion of a choke inductor between the supply voltage and the top drain. This topology can be easily scaled up to provide more power with a parallel combination, as explained in section 3.2.

The high side transistors can be driven either through a high speed, high voltage diode in a bootstrap configuration, such as the C3D1P7060Q SiC Schottky diode in a QFN package from Wolfspeed, or with an isolated supply, such as the high voltage PV15-27B15R3 fly-back converter from Mornsun America combined with the TLP2767 high speed opto-coupler from Toshiba for the gate signal. If the transistors are based on GaN technology, the low sides can be both driven with a single two channel gate driver, such as the 2EDN7524G from Infineon.

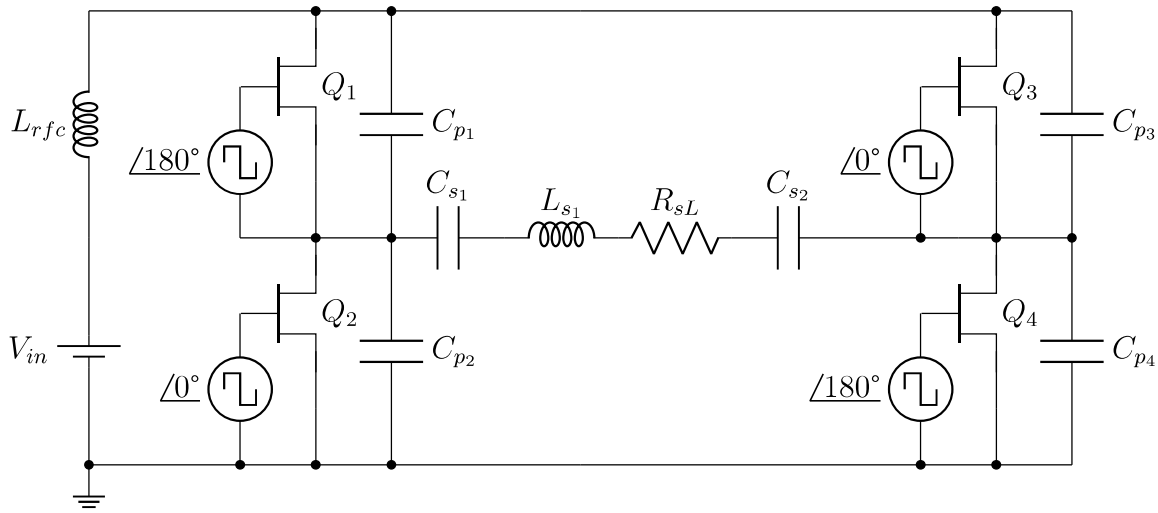


Figure 3.20: Single common infinite choke push-pull Class DE inverter topology.

The total number of individual gate signals is two, just like any Class E type push-pull inverter, and if the gate drivers have inverted driving capability (such as the UCC27512 from TI) and the duty cycle is 50 %, it can even be driven just with a single signal.

The design process for the inverter in Figure 3.20 begins by designing a single ended Class DE inverter [36], with the corresponding output power, frequency, equivalent primary coil, and reflected load for the full push-pull topology. In the examples below we use the IPT link, secondary AC load, output power, and switching devices that are mentioned in the experimental example in subsection 3.1.2. The complete list of the component values is provided in Table 3.3. For the traditional Class DE topology we choose 25 % duty cycle, as it provides the highest power capability. Once the circuit with ideal switches has been established, we make adjustments to accommodate for the actual transistor model. First we add the minimum gate resistance that minimises the drain current ringing, especially at turn-off. Then we decrease the duty cycle in order to absorb the switching delays caused by the input capacitance of the device, which for the Class DE example is -11% . Finally, the value of the external shunt capacitance is reduced to absorb the effect of the output capacitance of the device. The Class DE topology by design almost eliminates the non-linear part of the C_{oss} [36], which vastly simplifies this part of tuning.

The design process to achieve a PPCC Class DE inverter design begins from the ideal transistor PP Class DE stage and adding the input choke of choice. Then, we increase the duty cycle while simultaneously decreasing the shunt capacitance to achieve the required switching conditions, which in our example are both ZVS and ZVDS. Once the PPCC Class DE inverter design with

Table 3.3: Component values of the Class DE inverter examples.

Parameter	PP Class DE	PPCC Class DE	Unit
V_{in}	474	377.11	V
L_{rfc}	-	100	μH
f_S	6.78	6.78	MHz
D	22.25	38.36	%
R_g	2	2	Ω
Q	GS66508B	GS66508B	—
C_p	329.64	197.93	pF
C_s	117	117.59	pF
L_{s1}	10	10	μH
R_{s1}	200	200	$\text{m}\Omega$
R_L	15	15	Ω

ideal transistors has been finalised, we include the non-ideal transistor model. Again, at this stage, we decrease the duty cycle to absorb the turn-off delay of the transistor and decrease the external shunt capacitance to absorb the effect of C_{oss} . Unlike the traditional Class DE inverter, the PPCC Class DE topology does not have the property of absorbing the non-linearity of the output capacitance, so adjustments on the output series resonant capacitors may be needed to achieve the desired switching conditions, especially if the loaded output Q factor is relatively low. Finally, the input voltage should be decreased accordingly to match the expected output current value. In our example, the ideal PPCC Class DE inverter had -25.5% change in shunt capacitance, 65% increase in duty cycle, and 22% decrease in input voltage, compared to its PP Class DE counterpart. It must be noted at this point that the dynamic behaviour of the PPCC Class DE inverter to load changes is similar to that of a typical Class E configuration.

The voltage and current waveforms of the two 3 kW Class DE inverter designs are shown in Figure 3.21. The main observation from the input current waveforms is that the PPCC Class DE design has a constant DC current with amplitude only 39% of the peak of the PP Class DE, which was the main objective of creating this inverter design. The output current of the two designs has a phase difference, which means that the equivalent impedance of the two inverter is different, since the series resonant capacitances are the same. However, the peak drain voltage on the PPCC Class DE inverter is no longer limited to the supply voltage, because of the back $\mathcal{E}$ of the input choke during turn-off. But, because of the inherently larger duty cycle of the PPCC Class DE design, the peak source current is lower than the traditional Class DE, which effectively disconnects the typically large output current from the current through the device,

as well as the input current. The peak device current of the PPCC Class DE inverter example is so much lower than the PP Class DE, that a lower rating transistor can be used, such as the GS66504B 15 A device.

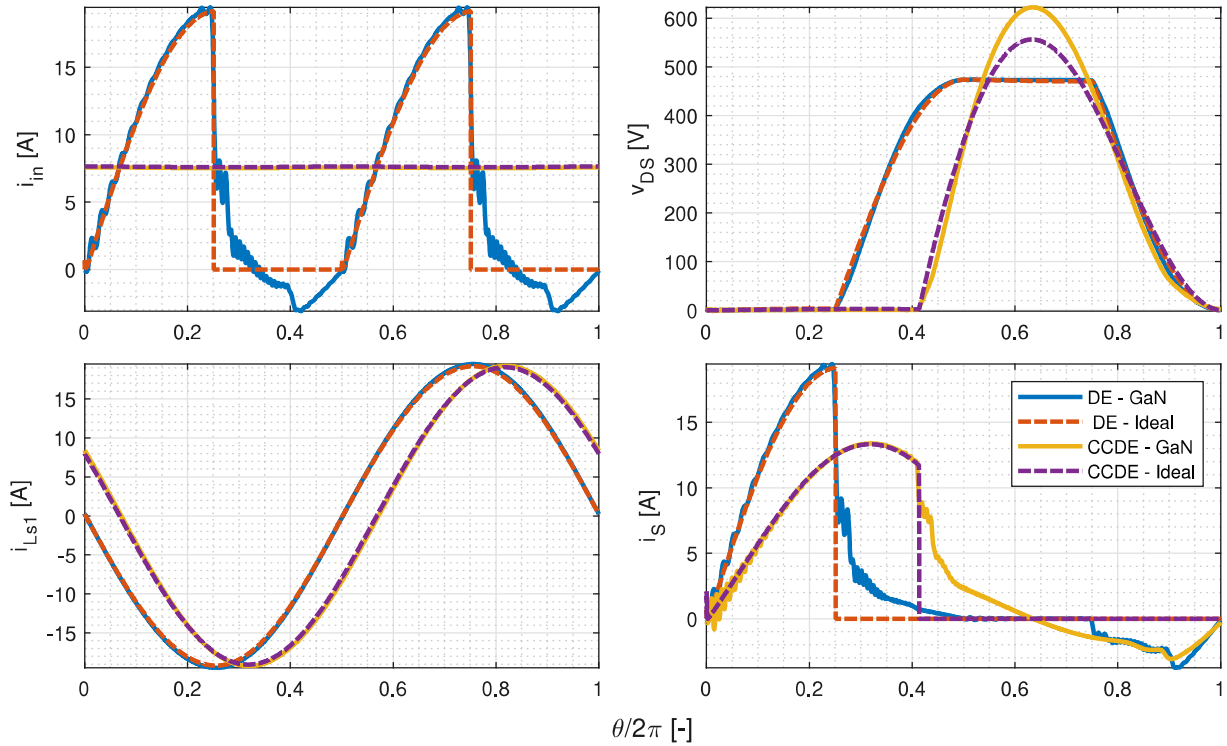


Figure 3.21: Voltage and current waveforms of the PP Class DE and the PPCC Class DE 3 kW inverter simulation examples, for both an ideal transistor model and the GS66508B.

Another, not so obvious benefit of having an input choke is that it eliminates voltage overshoot during turn-off due to parasitic trace inductances, especially when there is no ZVDS condition. The peak voltage of the PPCC Class DE design example with the ideal transistor is 1.68 times the supply voltage, which is lower both than the Class E, that is around 4, and the Class EF_2 , which is around 2. Even taking into account that the PPCC Class DE topology has twice the number of transistors compared to the PP Class E inverter, it still has relatively lower voltage stresses on the devices, while having half the number of individual choke inductors, which drastically increases the power density of the circuit.

3.5 Inverter - Magnetic Link - Rectifier Integration

In this section we present in detail the design process, development and finally experimental testing of a high power DC/DC HF IPT system. This experiment serves the purpose of proving

the concept of the parallel PP topology introduced in section 3.2. The switching frequency is limited to 3.39 MHz by the capabilities of the SiC Schottky diodes (C4D20120H from Cree) used in the rectifier circuit.

3.5.1 Magnetic Link Measurements

We begin with the coil impedance measurements, using the E4990A impedance analyser from Keysight, with the coils connected to their respective PCB's. Photos of the Tx and Rx coils are shown in Figure 3.22, with details about their dimensions in the description. The Tx coil has 3 turns for high inductance, and large gap between turns to keep the SRF high. The secondary coil has two turns, which enables lower gap between turns, while keeping the inductance low enough to be able to absorb the capacitive reactance of the rectifier. Screenshots of the results of the impedance measurements for the two coils are shown in Figure 3.23, based on which we determine the inductances and Q factors used in the design procedure of the converters. The measured inductance values agree with the analytic low frequency approximations from [75], where $L_{s_1} = 4.11 \mu\text{H}$ and $L_{s_2} = 3.44 \mu\text{H}$. Another noteworthy observation from Figure 3.23 is that the SRF of both coils is well above the operating frequency (around 20 MHz), which makes them well suited for the application.

The next step involves determining the distance between the two coils and accurately measuring the coupling factor. For an IPT system design with high link efficiency it is important that the combination of coil distance and AC equivalent secondary load result in high enough reflected resistance to the primary at the switching frequency. We performed three kinds of coupling factor measurements: impedance measurements from the primary with a resonant secondary AC load, open-short measurements, and coupling estimation with a frequency sweep, as explained in [19, 134]. For the case of the resonant secondary coupling measurement method, we used two different values of resistance.

A photo of the final coil configuration is shown in Figure 3.24, where the distance is 11 cm and the reflected resistance at the switching frequency is around 8Ω with a 42Ω AC secondary load, according to the impedance measurement in Figure 3.25. These measurements correspond to a coupling factor in the range of 20 % to 30 % which is too low to be estimated accurately with the open-short method and too high for the AC resonant load method, leaving the frequency

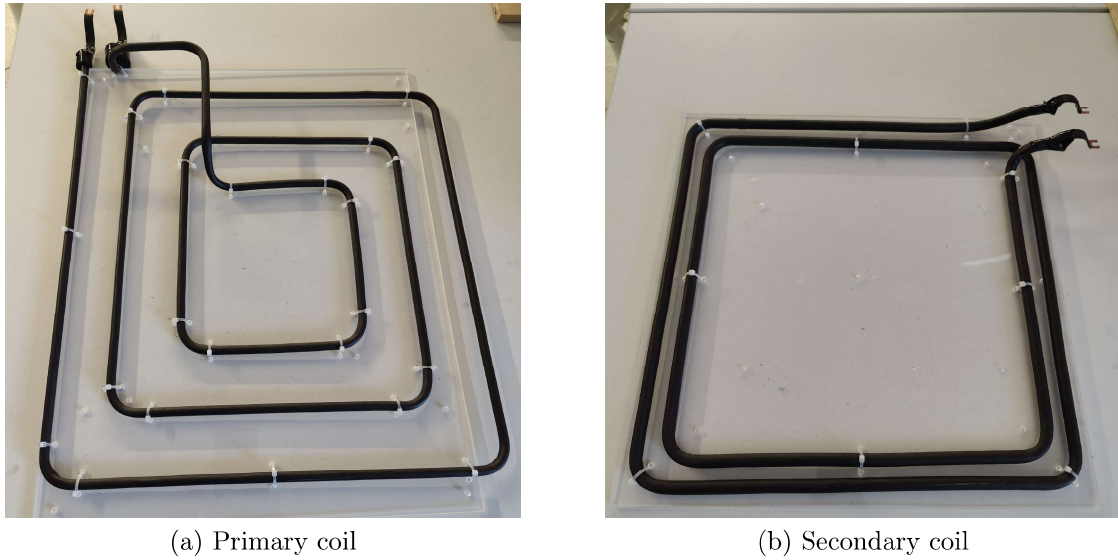


Figure 3.22: Photos of the primary and secondary coils used in the high power IPT DC/DC system example. Both coils are square planar made with copper tube. The outer dimension of the 3-turn Tx coil is 43 cm, with 6 cm distance between turns and 8 mm tube diameter. The outer length of the 2-turn Rx coil is 37 cm, the distance between turns is 1 cm, and the tube diameter is 10 mm.

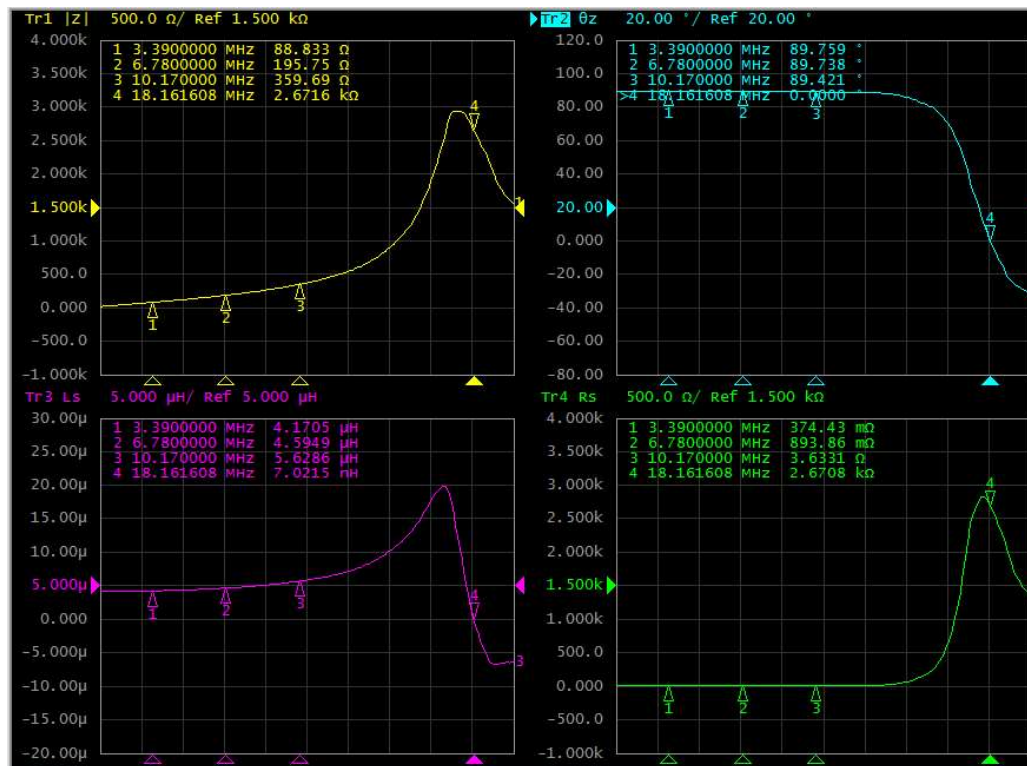
sweep method as the preferred estimation approach.

The results of the frequency sweep measurements for coupling factor estimation are shown in Figure 3.26. The signal source is the 50 MHz Aim-TTi function generator and the voltage measurements across the coils are performed using the optical probes from Tektronix, to minimise the capacitive loading on the coils, although this measurement method inherently absorbs the effect of the coil capacitance. The range of the frequency sweep is from 100 kHz to the resonant frequency of the coils. The voltage measurements are performed by stimulating first the primary and then the secondary, while measuring both sides of the IPT link. The coupling factor k and the transformer ratio n are given by

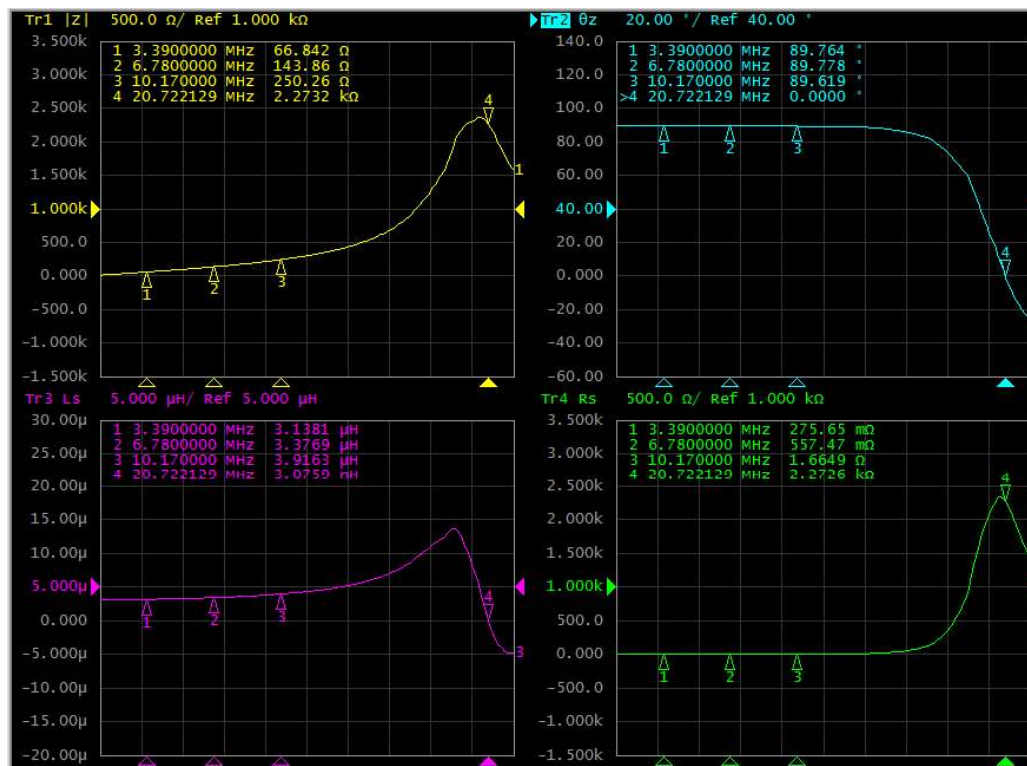
$$k = \sqrt{\frac{V_{L_{s1}}^{\text{out}} V_{L_{s2}}^{\text{out}}}{V_{L_{s1}}^{\text{in}} V_{L_{s2}}^{\text{in}}}}, \quad (3.8)$$

$$n \equiv \sqrt{\frac{L_{s2}}{L_{s1}}} = \sqrt{\frac{V_{L_{s2}}^{\text{in}} V_{L_{s2}}^{\text{out}}}{V_{L_{s1}}^{\text{in}} V_{L_{s1}}^{\text{out}}}}. \quad (3.9)$$

The transformer ratio value matches the individual impedance measurements of the two coils, which is a confirmation of valid results. The exact estimation value of the coupling factor using



(a) Primary coil



(b) Secondary coil

Figure 3.23: Impedance measurements of the coils in the IPT DC/DC system experimental example. In yellow is the impedance amplitude, in cyan is the phase, in purple is the inductance, and in green is the resistance. The first three frequency marks correspond to the first three harmonics of the IPT system and the fourth mark is at the resonance frequency of the coil.

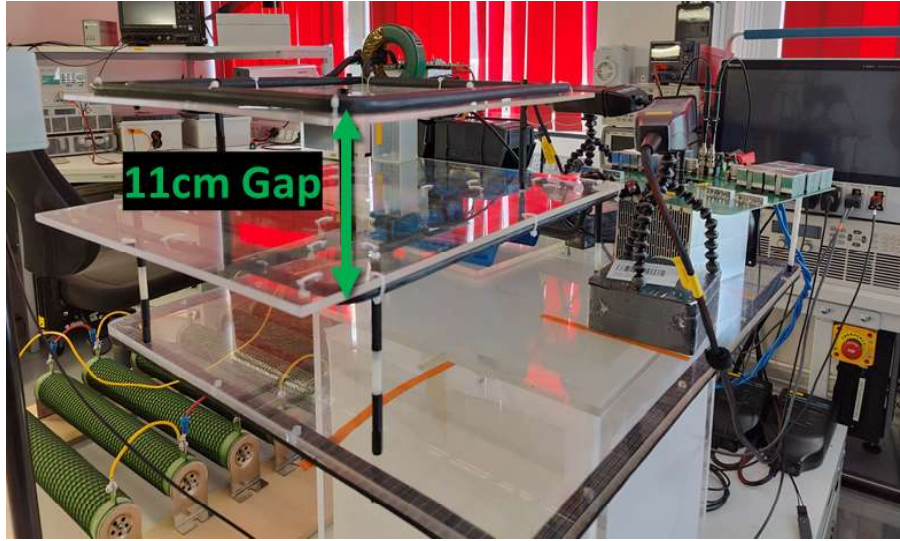


Figure 3.24: Photo of the IPT of the experimental setup.

the frequency sweep method is 24.5 %. The open-short method gave an underestimation of the coupling factor, and the two measurements with the resonant Rx loads gave an overestimation, with significant deviation between the two instances, which is an indicator of unreliable estimations for these two measurement methods in our example.

3.5.2 Design of High Frequency Converters

Once the IPT link has been established and well characterised we continue to designing the HF rectifier. We choose the current driven Class DE rectifier topology, for the high power capability, resonant operation with soft switching, absorption of the non-linearities of the diode capacitances, and lack of inductors [36, 135, 136, 137]. Also, the current driven topologies are in general preferred for IPT applications, since they are series tuned and changes in the equivalent AC load of the rectifier do not affect the equivalent reactance [25]. The objectives are 8 kW peak power using the C4D20120H SiC Schottky diodes with a full-bridge configuration equivalent to a $40\ \Omega$ AC load.

The component values are determined by the design process of the half-bridge version with half the equivalent AC resistance and 30 % duty cycle, in order to remain within the voltage and current limits of the diodes. The full-bridge equivalent version has the same shunt capacitances but half the DC load of the half-bridge. The voltage and current waveforms for both versions are the same, as long as the the DC load is transformed accordingly. Both the half-bridge and

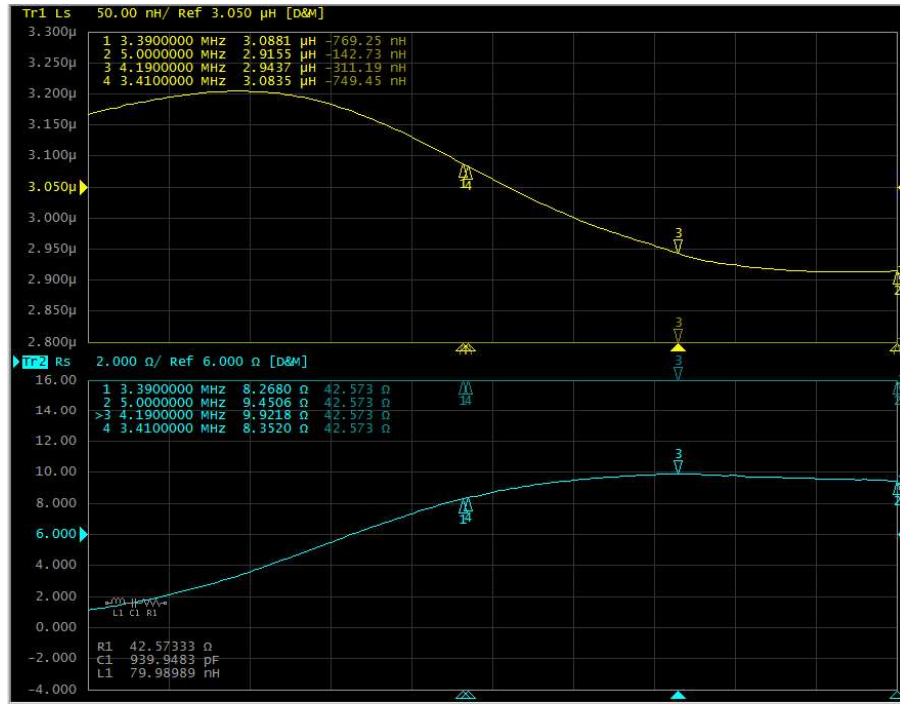


Figure 3.25: Impedance measurement from the primary side of the IPT link in Figure 3.24 with a resonant secondary. The primary inductance and reflected resistance values at the switching frequency are given at the first frequency mark and the secondary AC resistance value is at the bottom left corner.

full-bridge Class DE rectifier circuit diagrams are shown in Figure 3.27. Then we replace the ideal diodes in the simulation with the real diode model, and reduce the value of the shunt capacitors until the current and voltage waveforms match, as displayed in Figure 3.28. In our example it is 70 % of the ideal case, and it practically does not affect the equivalent reactance of the rectifier, since the Class DE topology inherently absorbs the non-linearities of the parasitic capacitance of the diodes.

The top and bottom views of the rectifier PCB are shown in Figure 3.29. The exact values of NP0 shunt capacitors and the DC resistance are measured, and the ideal components in the LTspice simulation are replaced accordingly. The first order equivalent input impedance of a resonant current driven rectifier is a capacitance in series with a resistance, as shown in Figure 3.30. The exact value of the equivalent impedance of the rectifier is calculated by driving it with an AC input current source at the nominal amplitude deriving the first harmonic of the voltage across it. Then, the series resonant capacitor can be computed using the relation

$$C_{s2} = \frac{C_r}{\omega_s^2 L_{s2} C_r - 1}. \quad (3.10)$$

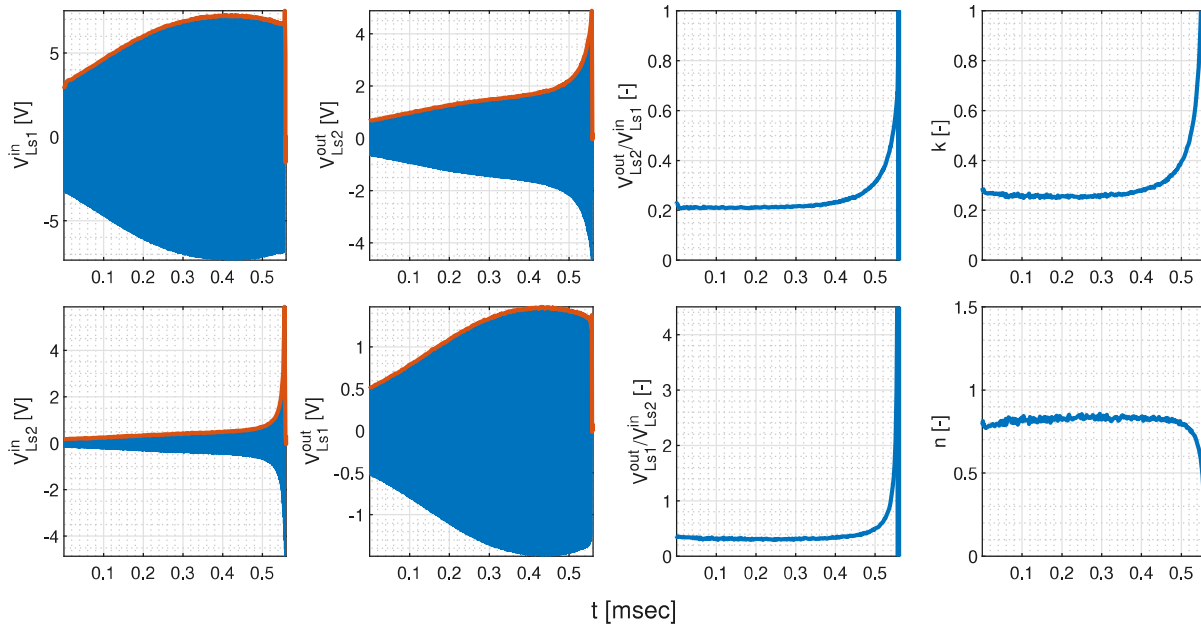


Figure 3.26: Frequency sweep measurement results for the IPT link in Figure 3.24. In the first two columns the waveforms are in blue and the envelopes of the waveforms are in orange. The curves in the last two columns are derived using the envelope data of the first two. The final values of the coupling factor and transformer ratio are derived from the flat part of the respective curves.

Once the Rx side is fully defined, the next objective is to calculate the reflected resistance to the primary, while minimising the reflected reactance. A close initial approximation of the amplitude of the primary coil current is given by

$$I_{L_{s1}} = \frac{I_{L_{s2}}(R_{s2} + R_r)}{\omega_S k \sqrt{L_{s1} L_{s2}}}. \quad (3.11)$$

Then, we simulate the complete secondary coupled to the Tx coil, driven by the current from (3.11). If needed, we fine tune the primary current amplitude to achieve the required output power, and the series secondary capacitance to minimise the reflected reactance to the primary. Specifically, in our example the primary current was increased by 3 % and the secondary resonant capacitor was increased by 2 %. Now, the value of the reflected resistance can be approximated by the real part of the first harmonic of the voltage across the Tx coil divided by the primary current.

Now that the objectives for the primary driver are determined, we proceed with the design of the inverter. We choose a parallel push-pull Class E inverter topology, because the lack of ϕ -branch provides superior efficiency (lower conduction losses) at high power over the Class EF

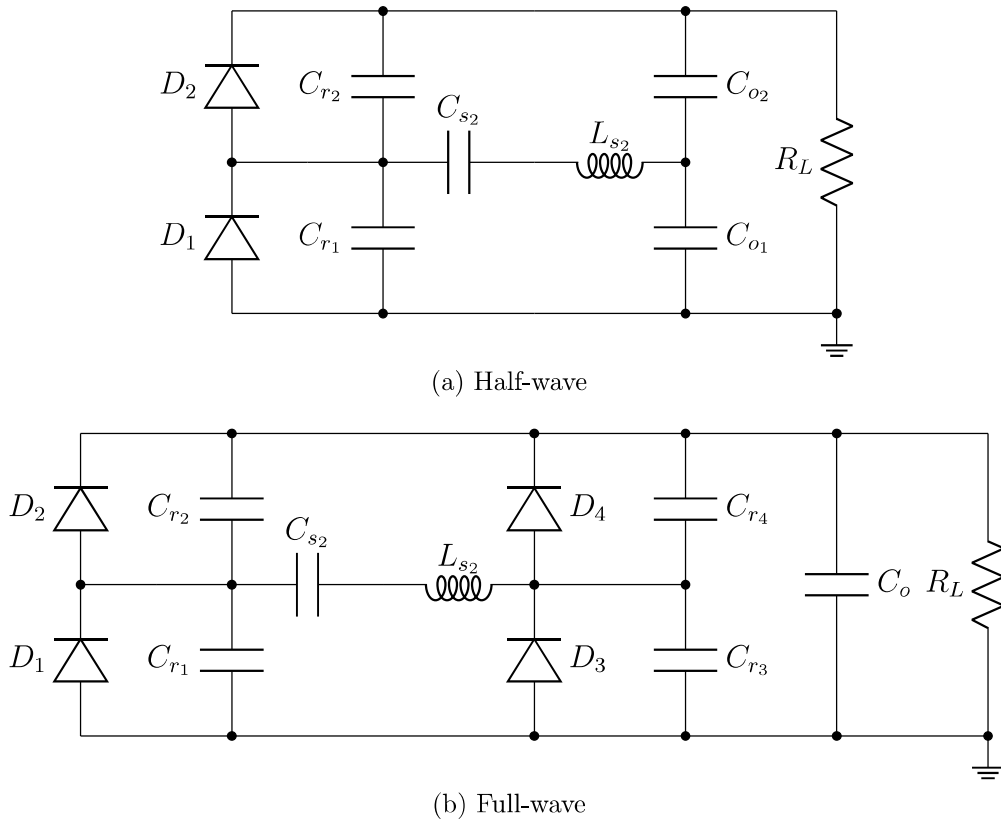


Figure 3.27: Circuit diagrams of the half-wave and full-wave current driven Class DE rectifier for IPT applications.

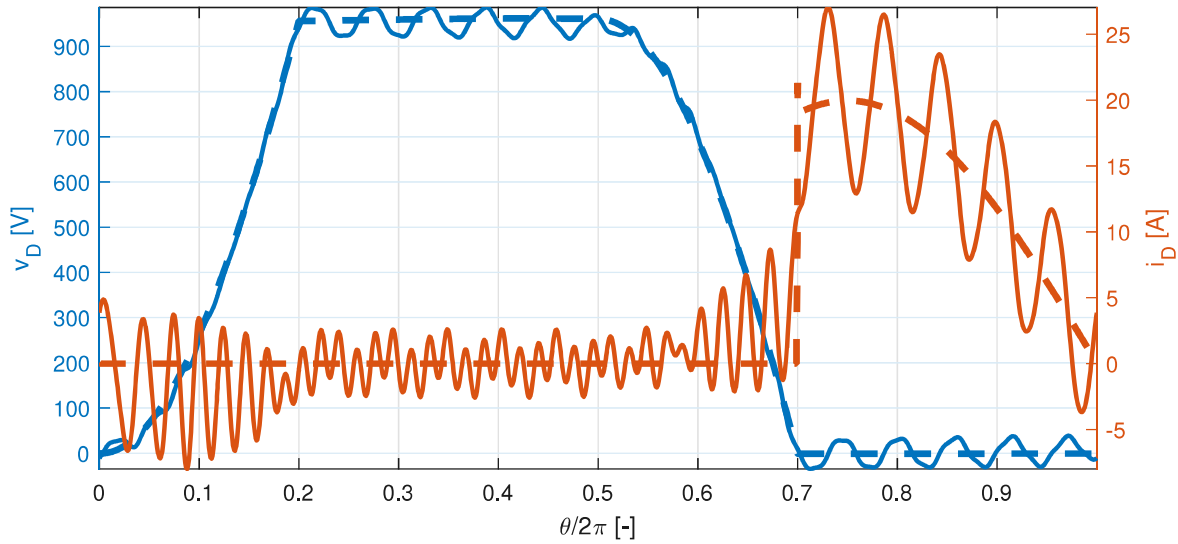


Figure 3.28: Voltage and current on the diodes of the current driven full-bridge Class DE example at 8 kW operation. The dashed line represents the ideal diode waveforms and the solid line is for the waveforms of the C4D20120H SiC Schottky diode. The ringing is caused by the resonance of the stray inductance of the TO-247-2 package with the parasitic capacitance of the diode.

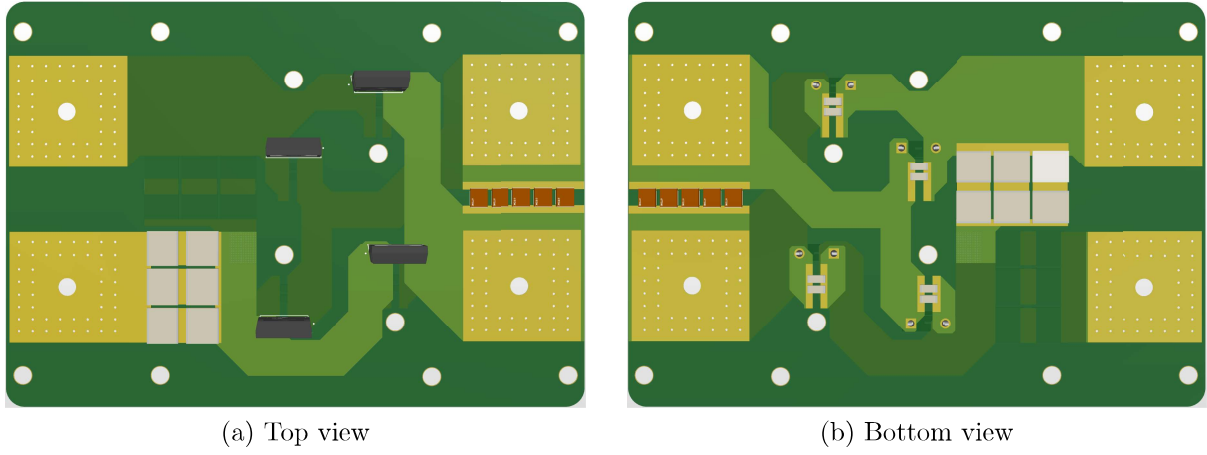


Figure 3.29: PCB of the full bridge current driven Class DE circuit. The parallel impedance transformation capacitor is left unpopulated in the experimental setup.

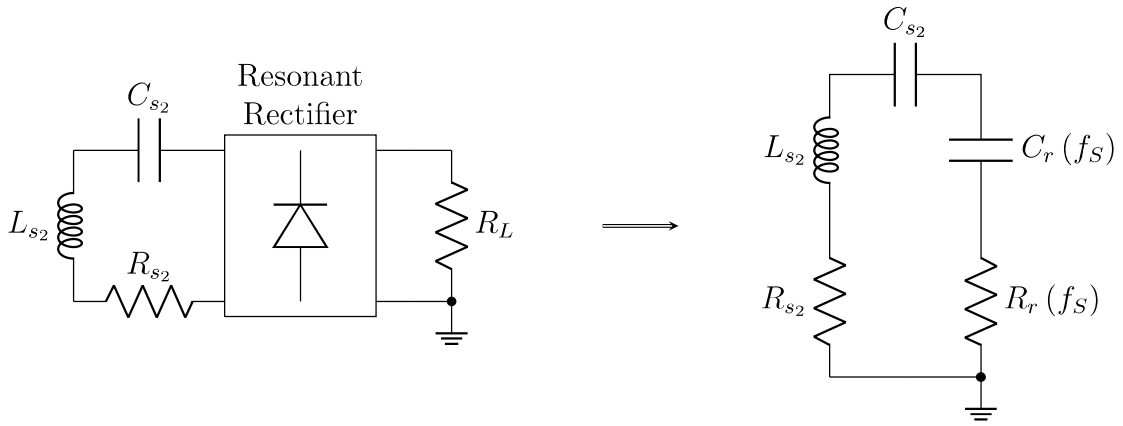


Figure 3.30: AC equivalent input impedance of a capacitive current driven resonant rectifier at the operating frequency.

topology, with 50% duty cycle for maximum power capability [32] and 7 kW nominal power output. The design procedure is based on the method proposed in chapter 2, adjusted to the simpler Class E configuration, combined with the impedance transformation required for the parallel PP connection.

The PCB's of the inverter are shown in Figure 3.31. It consists of two individual boards: an IMS daughter PCB with the Ventec VT-4B7 SP material containing the switching network for improved thermal performance, and a FR4 motherboard with the rest of the components. The transistors are the GS66516B from GaN Systems and the gate drivers are the UCC27512 from TI. Some indicative waveforms from the simulation of the full IPT system at nominal power are given in Figure 3.32.

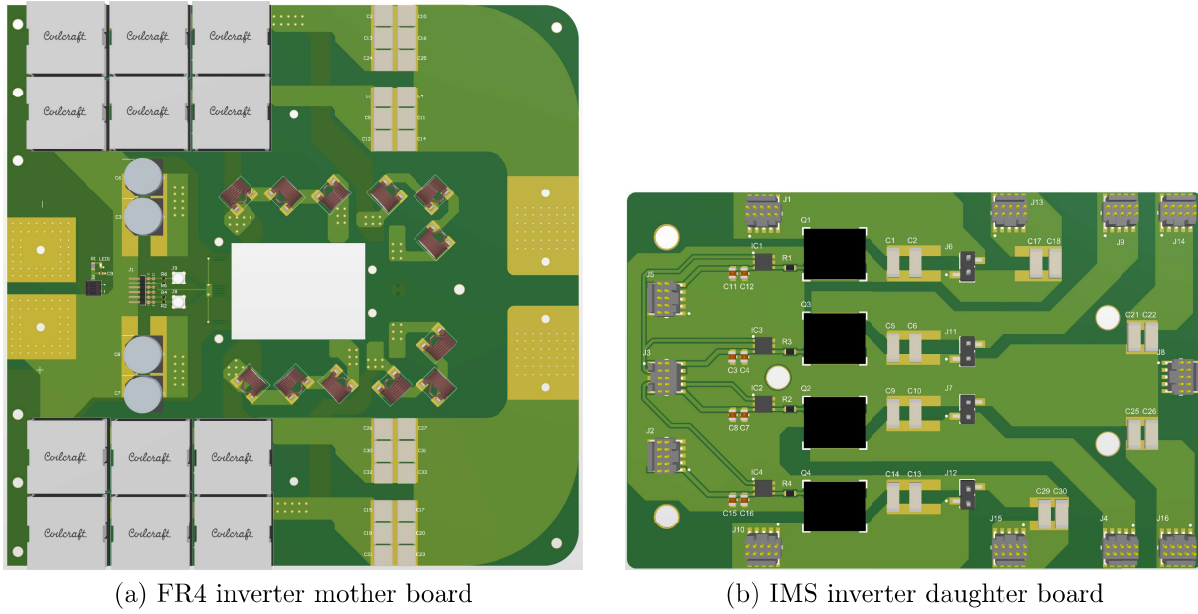


Figure 3.31: PCB's comprising the parallel push-pull Class E inverter. The boards are capable of providing both Class E and Class EF configurations. The daughter board is connected to the bottom of the mother board under the cutout.

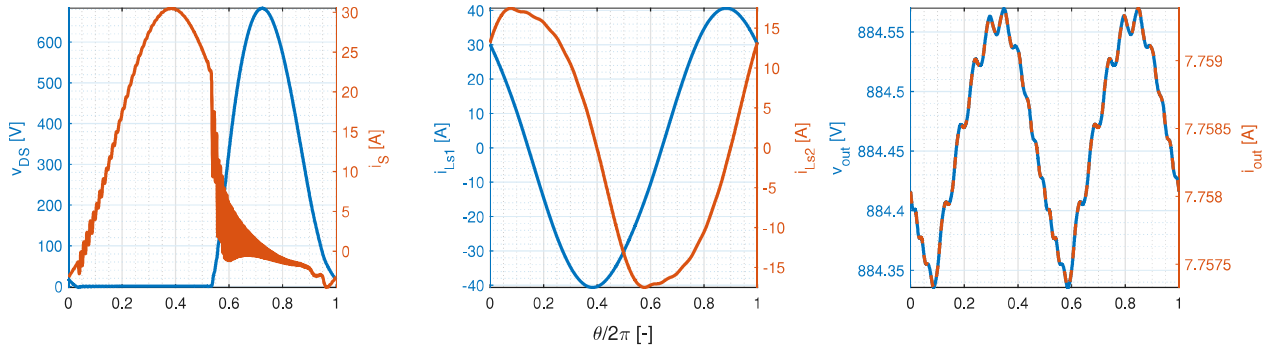


Figure 3.32: Waveforms of the transistor drain voltage and current (left), currents through the coils (middle), and output load power (right). The Rx coil has distortion from the third harmonic, which is an artifact of the Class DE rectification.

3.5.3 Experimental Results

Both the inverter and the rectifier use 7.2kV 3838 NP0 ceramic capacitor from Kyocera AVX for resonance with the coils, and the shunt capacitors are 2kV 2225 NPO from TDK. The input chokes are the AGP4233-333ME from Coilcraft, and the output stabilising capacitors of the rectifier are 1.5kV X7R ceramics. The input stabilising capacitors comprise of a combination of electrolytic and ceramic, both X7R and NP0. The signal generating circuit is the same as the one used in the experimental examples in chapter 2. The exact measured component values are given in Table 3.4 and a photo of the complete IPT system is shown in Figure 3.33.

Table 3.4: Component values of the high power IPT system

Parameter	Value	Unit
$V_{in}^{\max}$	180	V
L_{rfc}	100	μH
f_S	3.39	MHz
D	48.5	%
R_g	0	Ω
G	UCC27512	—
V_{dd}	6	V
Q	GS66516B	—
C_p	678	pF
C_{s1}	611	pF
L_{s1}	4.17	μH
k	24.5	%
L_{s2}	3.14	μH
C_{s2}	1.916	nF
D	C4D20120H	—
C_r	236	pF
C_o	2.24	μF
R_L	114	Ω

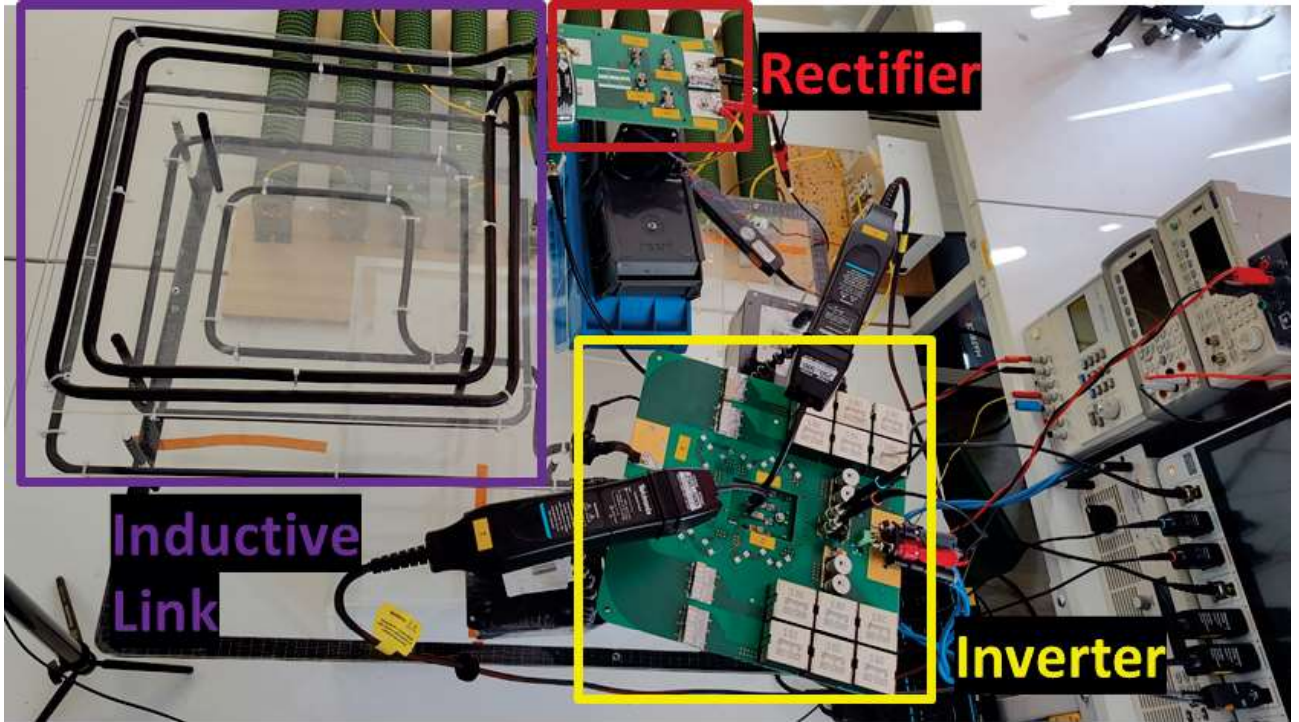


Figure 3.33: Photo of the complete high power IPT experimental setup.

The waveforms of the experimental setup in Figure 3.33 are given in Figure 3.34. The gate signals are measured with 50Ω coaxial cables, the secondary coil current is measured with

the Pearson 6585 current monitor, the primary coil current is measured with the N7041A Rogowski probe from Keysight, the drain voltage is measured with the TVIH08 isolated probe and WSQPIN1000X tip from Tektronix, the voltage across the diode is measured with the N2891A differential probe from Keysight, the output voltage is measured with a high voltage passive PMK probe, and the output current is measured with the N2893A current clamp from Keysight.

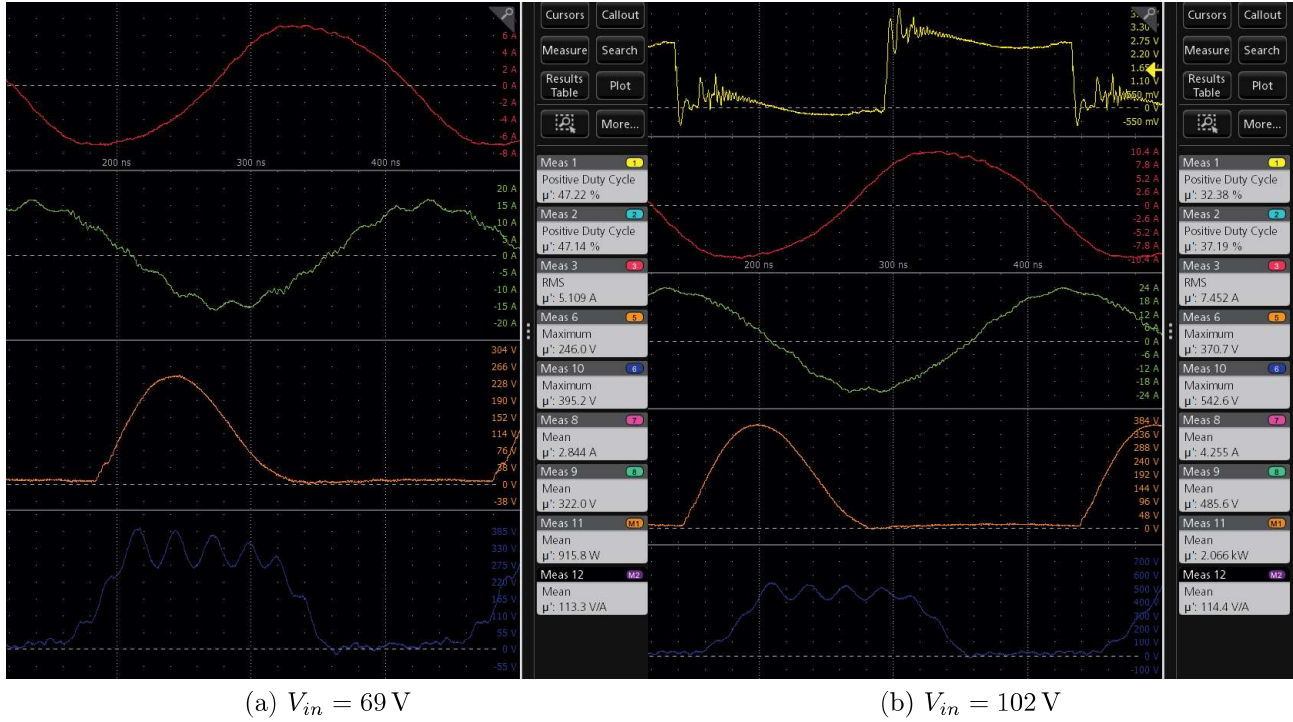


Figure 3.34: Measured waveforms of the IPT system in Figure 3.33 at two supply voltage values. The gate signal to one of the two pairs of gate drivers is yellow, the Rx coil current is red, the Tx coil current is green, v_{DS} is orange, the voltage across one of the diodes is blue. The first two measurements are the duty cycles of the gate signals, the third measurement is the RMS value of the Rx coil, "Meas 6", is the peak of the drain voltage, "Meas 10" is the peak of the voltage across the diode, "Meas 8" and "Meas 9" are the DC output current and voltage, respectively, "Meas 11" is the output power, and "Meas 12" is the DC load. The ripple of the L_{s1} is noise from the Rogowski probe.

The rectifier measurements match the simulations, but the inverter is reverse conducting more than expected, due to the large, non-predictable parasitic capacitance of the IMS board. At 69 V input voltage the inverter is soft switching with both ZVS and ZVDS, and the output power is 916 W. At 102 V input voltage the inverter is reverse conducting and the load is consuming over 2 kW power at over 91% DC/DC efficiency. The highest output power achieved was around 3 kW at 95% efficiency. Throughout the testing of the system the devices remained below 40 °C and the coils were around 30 °C at maximum power.

Several issues that limited the performance of the system had to be addressed. First, the 1.5 kV X7R capacitors at the output are not suitable for such application, since their temperature was increasing unexpectedly high. The reason lies in the voltage dependent behaviour of their capacitance as well as the lower SRF compared to NP0. This problem was easily resolved by adding extra NP0 ceramic capacitors to the output. Next, the metal substrate of the IMS board should not be left floated, but instead should be connected to ground. This intervention would make the parasitic capacitance of the IMS board more controllable and provide a return path through an uninterrupted plane to the signals. The cross-talk noise on the gate signal, which is caused by the supply of the gate and the drain node current, was dramatically decreased by grounding the metal substrate.

In addition, the mother board has unnecessarily long traces, which introduce parasitic inductances. Also, the transistors should be connected in a star configuration with a common solid ground plane, to minimise interference from the return path of the drain node. Finally, the gate signal traces should be shielded and kept as short as possible, to minimise coupling with the strong fields present on the power board. A parallel push-pull semi-resonant Class E inverter PCB with improved layout that addresses all the above issues is shown in Figure 3.35.

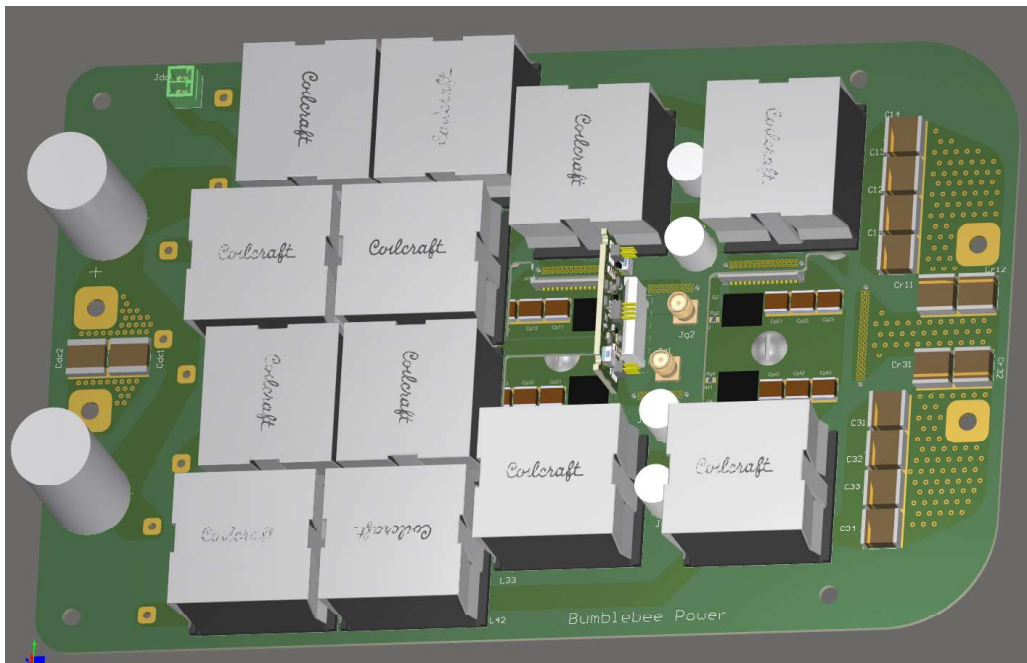


Figure 3.35: Parallel push-pull semi-resonant Class E inverter with improved layout to minimise EMI issues and ensure signal integrity.

3.6 Summary

The difficulty of operating high frequency IPT systems at high power is explained and the benefits of using GaN technology for such applications, despite its limitations, are justified. Two versions of a novel parallel configuration for resonant inverters and rectifiers is proposed, that increases the power throughput of IPT systems without being limited by the device and component stresses. Next, the pros and cons of a differential shunt capacitance in a push-pull Class E type inverter are investigated, and an alternative for semi-resonance operation for push-pull topologies is introduced. Then, a common input choke Class DE inverter topology is proposed that combines the benefits of both the Class E and the Class DE inverter. Finally, a complete and detailed process of designing and testing a 3 kW, 3.39 MHz DC/DC IPT system is provided, which achieved 95 % DC/DC conversion efficiency over an 11 cm gap.

Chapter 4

Magnetic Link Design and Characterisation

4.1 Single Transmitter - Multiple Receivers System

4.1.1 Background

Traditionally, an IPT system consists of a single Tx powering just one Rx, as shown in Figure 1.5, since a single IPT link minimises the dynamic variables of such systems. However, there is interest for applications and practical benefit in realising IPT systems with more than one receiver, such as air-core DC/DC converters [138, 70] and WPT systems [139, 140]. Having multiple coils in vicinity results in cross-coupling among every possible pair in the system, which complicates the optimal design procedure for resonant HF IPT operation.

Efforts have been made in the literature towards building IPT systems with multiple receivers whose cross-coupling has been minimised [141, 142, 143]. This approach, successfully reduces the complexity of the problem, but simultaneously introduces physical limitations to the setup of the IPT link. In principle, it is possible to design a Multiple-Input Multiple-Output (MIMO) IPT system with high efficiency despite the existence of cross-coupling, as proven theoretically for a first order model [144].

In this chapter, we present an IPT link design method for a single Tx and multiple Rx's accord-

ing to the configuration shown in the block diagram in Figure 4.1. Our analysis includes the effects of the rectifiers on the receivers and achieves maximum power throughput while eliminating the reflected reactance to the primary, which is crucial for maintaining high efficiency in a dynamic IPT system. This way we manage to further extend the work in the existing literature providing results that are more beneficial to the requirements of optimal operation of practical IPT systems.

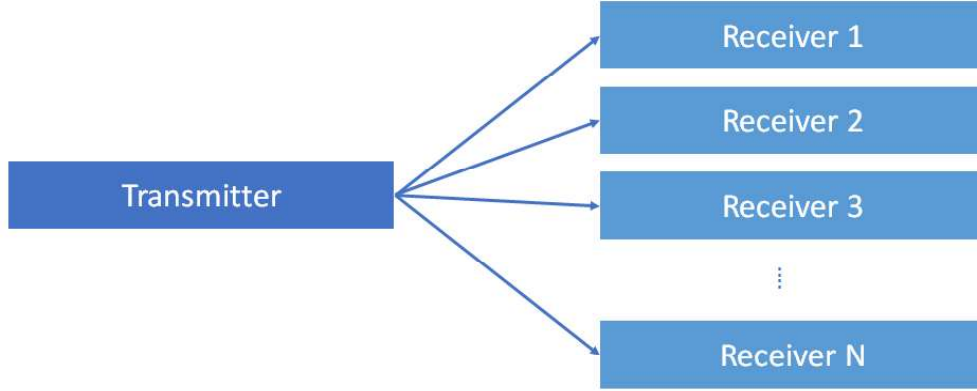


Figure 4.1: Block diagram of a generalised inductive WPT system with a single Tx and multiple Rx's.

4.1.2 System Analysis

As explained in section 1.3 and shown in Figure 1.5, a first order equivalent approximation of the IPT system can be obtained by modelling the inverter as an AC voltage source and the rectifier as an equivalent impedance at the switching frequency. The inverter is typically series tuned whereas the connection type of input resonant capacitor of the rectifier depends both on the type of rectifier and the value of its equivalent AC resistance [19]. In our analysis we use a half bridge current driven rectifier, shown in Figure 4.2, which is series tuned [36], but the mathematical derivation can be adjusted to any rectifier topology, series or parallel tuned to the corresponding Rx coil.

The equivalent input impedance that the secondary coil current sees is given by [19]

$$R_{ac}(i_{L_{s2}}) = \frac{2}{\pi^2} \left(R_{dc} + \frac{2V_d}{I_{dc}(i_{L_{s2}})} \right), \quad (4.1)$$

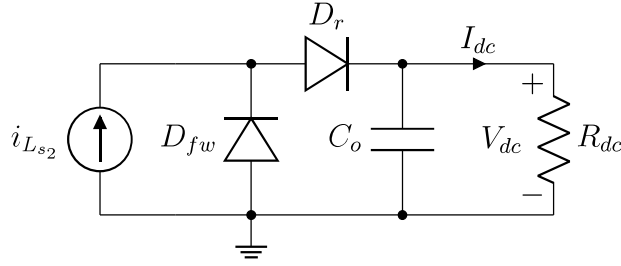


Figure 4.2: Circuit diagram of a half bridge current driven rectifier.

where V_d is the voltage drop of the diodes, and the relation of the input to output current is

$$I_{dc}(i_{L_{s2}}) = \frac{|\bar{I}_{L_{s2}}|}{\pi}. \quad (4.2)$$

From (4.1) we can see that the input impedance of the half bridge topology heavily relies on the input current, which is a significant obstacle for the efficient operation of dynamic IPT systems, but such analysis is beyond the scope of this chapter, as we use it only as an example. A more suitable rectifier topology would be the semi-resonant Class E introduced in [21], which can easily replace the Class D in the analysis that follows.

Under the above conditions, the FO circuit diagram of the multi-coil system in Figure 4.1 is the one shown in Figure 4.3. The AC input equivalent load of the rectifier in Figure 4.2 is purely resistive (R_{ac}), assuming no significant parasitic capacitance in the diodes, so there is no need to compensate for its reactance with the series tuning secondary capacitor. Our objective in Figure 4.3 is to obtain a closed form equation for the total reflected impedance on the primary as a function of the series tuning capacitors on the receivers.

As depicted in Figure 4.3, we define the angles of all the phasors with respect to the primary coil current, hence the phase of I_1 can be set to zero. The real and imaginary parts of the total reflected impedance to the primary $\bar{Z}_R$ in matrix form are:

$$R_R \equiv \text{Re} [\bar{Z}_R(\mathbf{x}_C)] = \mathbf{x}_b^T \mathbf{U}^{-1}(\mathbf{x}_C) \mathbf{x}_b, \quad (4.3)$$

$$X_R \equiv -\text{Im} [\bar{Z}_R(\mathbf{x}_C)] = \mathbf{x}_b^T \mathbf{R}_A^{-1}(\mathbf{x}_C) \mathbf{X}_A(\mathbf{x}_C) \mathbf{U}^{-1}(\mathbf{x}_C) \mathbf{x}_b, \quad (4.4)$$

where by incorporating the complex matrix inversion scheme in [145] we get

$$\mathbf{U} = \mathbf{R}_A + \mathbf{X}_A \mathbf{R}_A^{-1} \mathbf{X}_A. \quad (4.5)$$

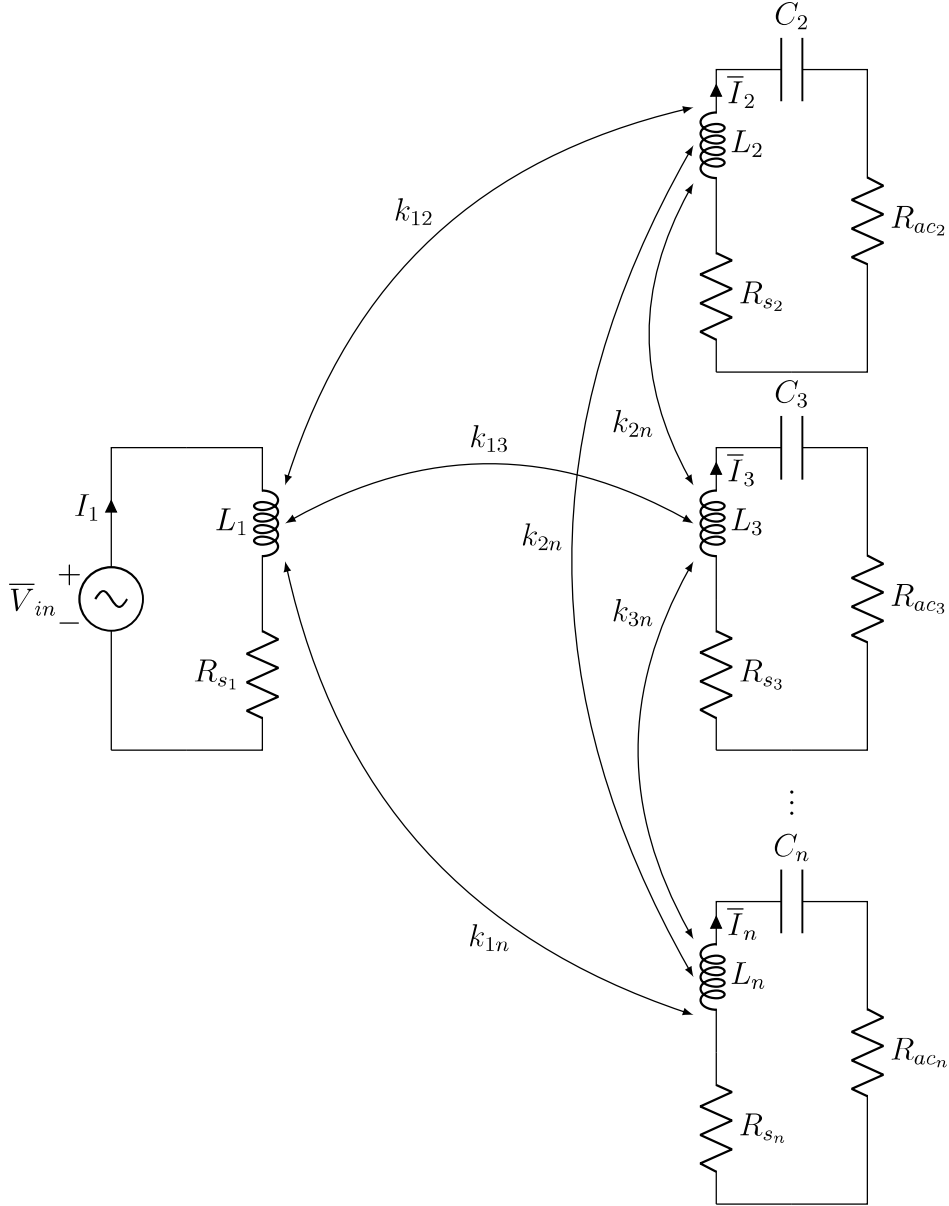


Figure 4.3: FO AC equivalent circuit of the single Tx powering multiple cross-coupled Rx's.

The real and imaginary parts input of the currents on the receiver coils are

$$\text{Im} [\bar{\mathbf{i}}] = -I_1 \mathbf{U}^{-1} \mathbf{x}_C, \quad (4.6)$$

$$\text{Re} [\bar{\mathbf{i}}] = \mathbf{R}_A^{-1} \mathbf{X}_A \text{Im} [\bar{\mathbf{i}}], \quad (4.7)$$

where the receiver input current phasor vector is

$$\bar{\mathbf{i}} = \begin{bmatrix} \bar{I}_2 & \bar{I}_3 & \dots & \bar{I}_n \end{bmatrix}. \quad (4.8)$$

The reactance vector $\mathbf{x}_C$ of the secondary series capacitances is

$$\mathbf{x}_C = \begin{bmatrix} X_{C_2} & X_{C_3} & \dots & X_{C_n} \end{bmatrix}^\top, \quad (4.9)$$

where $n - 1$ is the total number of receivers in the system and

$$X_{C_i} = \frac{-1}{\omega C_{s_i}}, \quad i = 2, 3, \dots, n. \quad (4.10)$$

The mutual reactance vector with the primary is

$$\mathbf{x}_b = \begin{bmatrix} X_{12} & X_{13} & \dots & X_{1n} \end{bmatrix}^\top, \quad (4.11)$$

where

$$X_{ij} = k_{ij} \sqrt{L_i L_j}, \quad i, j = 1, 2, \dots, n. \quad (4.12)$$

The combined AC secondary resistance matrix is

$$\mathbf{R}_A = \text{diag}(\mathbf{r}_s + \mathbf{r}_{ac}), \quad (4.13)$$

where

$$\mathbf{r}_s = \begin{bmatrix} R_{s_2} & R_{s_3} & \dots & R_{s_n} \end{bmatrix}, \quad (4.14)$$

$$\mathbf{r}_{ac} = \begin{bmatrix} R_{ac_2} & R_{ac_3} & \dots & R_{ac_n} \end{bmatrix}. \quad (4.15)$$

The combined secondary reactance matrix is

$$\mathbf{X}_A = \text{diag}(\mathbf{x}_C) + \mathbf{X}_M, \quad (4.16)$$

where

$$\mathbf{X}_M = \begin{bmatrix} X_{22} & X_{23} & \dots & X_{2n} \\ X_{32} & X_{33} & \dots & X_{3n} \\ \vdots & \vdots & \ddots & \vdots \\ X_{n2} & X_{n3} & \dots & X_{nn} \end{bmatrix}. \quad (4.17)$$

The formulation of $\overline{Z}_R$ in (4.3) and (4.4) is a higher order extension and generalisation of the simple case of a single Tx and a single Rx described by (1.20). It can be easily confirmed that

by reducing the number of receivers to one, (4.3) and (4.4) converge to (1.20), which proves and validates our proposed equations.

A visual example of the simple case using (1.20) is shown in Figure 4.4, which is also equivalent to the measurements in Figure 2.5. A more complex surface plot of the reflected impedance to the primary when two cross-coupled receivers are in place is shown in Figure 4.5. In both cases the optimal series capacitance values are calculated from (2.61). By comparing the two above mentioned cases, it is clear that once the number of receivers is more than one and they are cross-coupled, as shown in Figure 4.3, the simple secondary resonance method does not produce the highest possible reflected reactance, which reduces the overall link efficiency according to section 1.3, and introduces unwanted reflected reactance, which causes sub-optimal operating conditions for the primary coil driver.

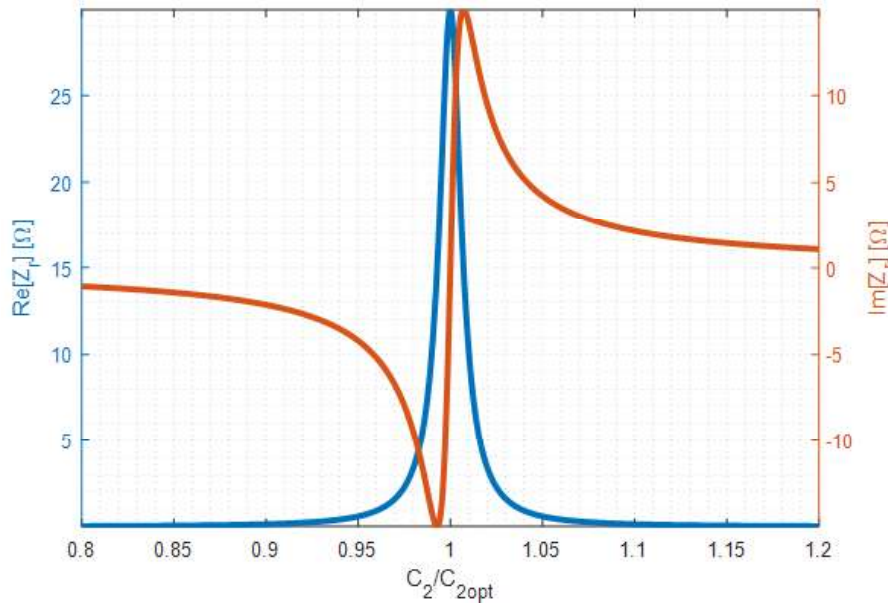


Figure 4.4: Total reflected resistance (blue) and reactance (orange) of a system with one transmitter and one receiver. The independent variable is the ratio between the series secondary tuning capacitance and its optimal value. In this simple case the evaluation of the highest efficiency operating point is straight forward and well documented in the literature.

4.1.3 Link Optimisation for a Given Power Level

As already established, once the load, rectifier topology, and physical characteristics of the link are decided, the only degree of freedom for link efficiency optimisation is the choice of secondary tuning capacitances. By setting (4.3) as our objective function, such optimisation scheme for

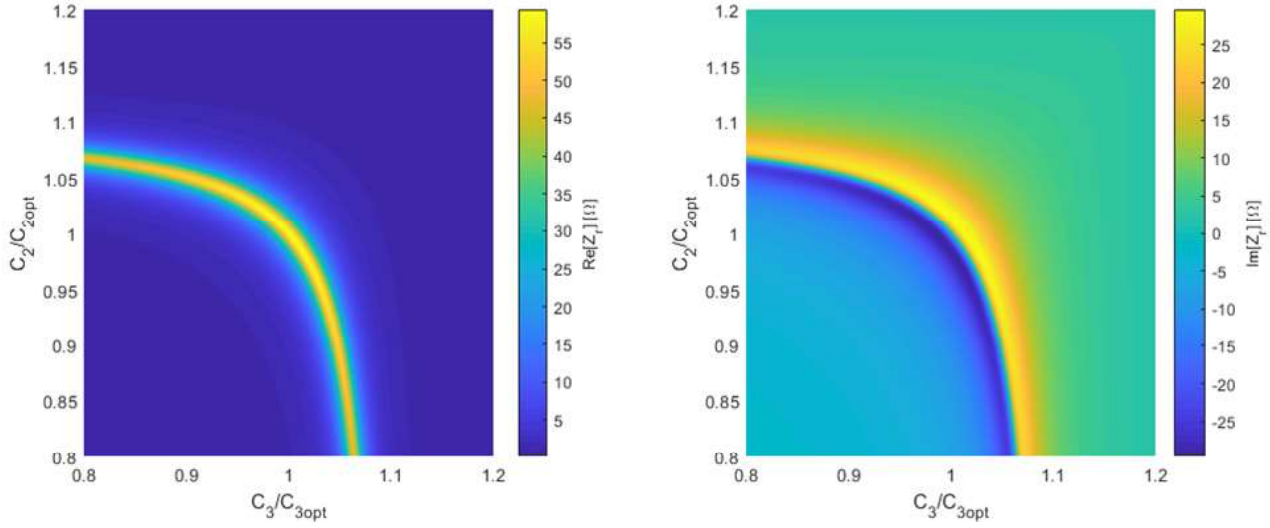


Figure 4.5: Extension of Figure 4.4 by having two receivers. It is obvious that in higher than one dimension the optimization problem becomes complex and the solution of the 1D case does not apply anymore.

an IPT system would try to maximise the value of (4.3) while keeping (4.4) at zero, searching for the solution in a multi-dimensional space such as Figure 4.5. Here, we implement a modified Newton scheme as follows [146, 147]:

$$\nabla^2 R_R(\mathbf{x}_C^{[k]}) \Delta \mathbf{x}_C^{[k]} = -\gamma \nabla R_R(\mathbf{x}_C^{[k]}), \quad (4.18)$$

where k is the iteration index, γ is a relaxation parameter, and

$$\Delta \mathbf{x}_C^{[k]} = \mathbf{x}_C^{[k+1]} - \mathbf{x}_C^{[k]}. \quad (4.19)$$

In order to speed up the above iterative scheme and simultaneously ensure convergence we set the initial guesses of R_{ac_i} and C_i , $i = 2, 3, \dots, n$ to

$$R_{ac_i}^{[0]} = \frac{2R_{dc}}{\pi^2} \left(1 + \frac{2V_d}{V_{dc_i}} \right), \quad (4.20)$$

$$X_{C_i}^{[0]} = -\lambda \sum_{j=2}^n \text{Im}(Z_{ij}), \quad (4.21)$$

where V_{dc_i} is the target output voltage of each rectifier, Z_{ij} are the z-parameters of the IPT link, and λ is a deviation parameter. These initial conditions ensure that we start close to the solution and our method will stop at a maximum point, without deviating to an unwanted local

minimum. The iterative procedure terminates either if $X_R^{[k]}$ is close to zero or if the relative iterative step is too small, described by:

$$\frac{\|\Delta \mathbf{x}_C^{[k]}\|_\infty}{\|\mathbf{x}_C^{[k]}\|_2} < \epsilon, \quad (4.22)$$

where ϵ is the tolerance.

The complete process flow diagram of the secondary series capacitances optimisation for a given input current is shown in Figure 4.6. For a given input current value to the primary coil, this method produces the correct secondary tuning capacitances, which then can be used to calculate the output power of each individual Rx. This routine can run iteratively until the desired output power is achieved. We also included an extra step to speed up the convergence, which involves a heuristic based on the shape of the reflected impedance in Figure 4.4 and Figure 4.5 that either adds or subtracts the value of (4.19), depending on its effect to the change of the reflected resistance (represented by the "Ascend" and "Descend" blocks in Figure 4.6).

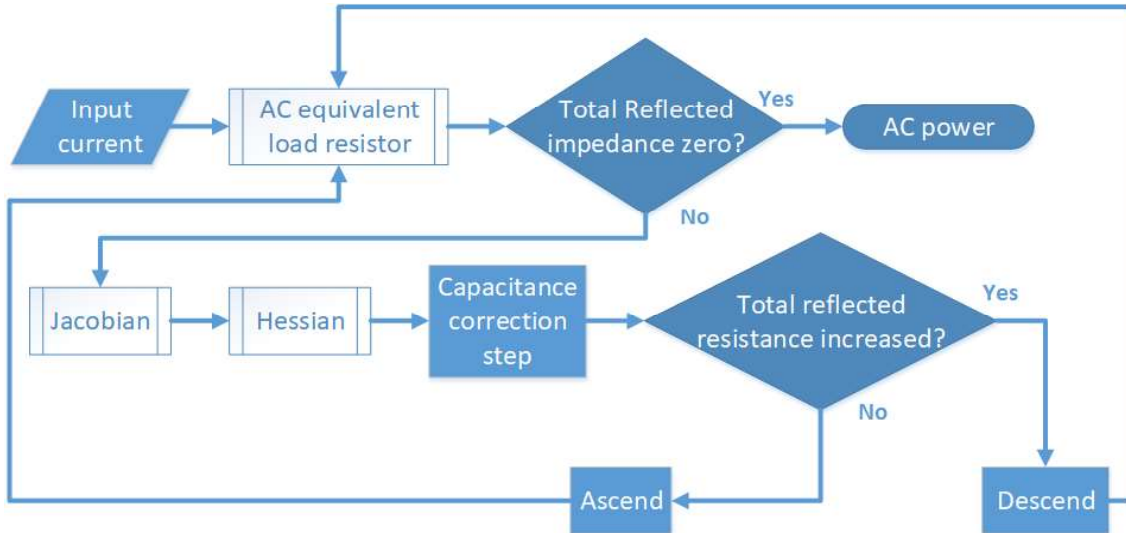


Figure 4.6: Flow process of the optimisation of the secondary series tuning capacitances. It is a specially modified Newton optimization method that adjusts the next step direction based on the current state of the system. The subroutines shown in the figure include their independent iterative computation schemes.

Formulation of the Gradient and the Hessian

By definition, the gradient vector and the Hessian matrix in (4.18) are, respectively:

$$\nabla R_R^{[k]} = \begin{bmatrix} \frac{\partial R_R^{[k]}}{\partial X_{C_2}} & \frac{\partial R_R^{[k]}}{\partial X_{C_3}} & \cdots & \frac{\partial R_R^{[k]}}{\partial X_{C_n}} \end{bmatrix}^\top, \quad (4.23)$$

$$\nabla^2 R_R^{[k]} = \begin{bmatrix} \frac{\partial^2 R_R^{[k]}}{\partial X_{C_2}^2} & \frac{\partial^2 R_R^{[k]}}{\partial X_{C_2} \partial X_{C_3}} & \cdots & \frac{\partial^2 R_R^{[k]}}{\partial X_{C_2} \partial X_{C_n}} \\ \frac{\partial^2 R_R^{[k]}}{\partial X_{C_3} \partial X_{C_2}} & \frac{\partial^2 R_R^{[k]}}{\partial X_{C_3}^2} & \cdots & \frac{\partial^2 R_R^{[k]}}{\partial X_{C_3} \partial X_{C_n}} \\ \vdots & \vdots & \ddots & \vdots \\ \frac{\partial^2 R_R^{[k]}}{\partial X_{C_n} \partial X_{C_2}} & \frac{\partial^2 R_R^{[k]}}{\partial X_{C_n} \partial X_{C_3}} & \cdots & \frac{\partial^2 R_R^{[k]}}{\partial X_{C_n}^2} \end{bmatrix}, \quad (4.24)$$

where

$$\frac{\partial R_R^{[k]}}{\partial X_{C_i}} = -\mathbf{x}_b^\top [\mathbf{U}^{[k]}]^{-1} \frac{\partial \mathbf{U}^{[k]}}{\partial X_{C_i}} [\mathbf{U}^{[k]}]^{-1} \mathbf{x}_b, \quad (4.25)$$

$$\begin{aligned} \frac{\partial^2 R_R^{[k]}}{\partial X_{C_i} \partial X_{C_j}} &= \mathbf{x}_b^\top [\mathbf{U}^{[k]}]^{-1} \left(\frac{\partial \mathbf{U}^{[k]}}{\partial X_{C_i}} [\mathbf{U}^{[k]}]^{-1} \frac{\partial \mathbf{U}^{[k]}}{\partial X_{C_j}} - \frac{\partial^2 \mathbf{U}^{[k]}}{\partial X_{C_i} \partial X_{C_j}} + \frac{\partial \mathbf{U}^{[k]}}{\partial X_{C_j}} [\mathbf{U}^{[k]}]^{-1} \frac{\partial \mathbf{U}^{[k]}}{\partial X_{C_i}} \right) \\ &\quad \cdot [\mathbf{U}^{[k]}]^{-1} \mathbf{x}_b. \end{aligned} \quad (4.26)$$

The partial derivatives of $\mathbf{U}$ in (4.25) and (4.26) are

$$\begin{aligned} \frac{\partial \mathbf{U}^{[k]}}{\partial X_{C_i}} &= \text{diag} \left(\frac{\partial \mathbf{r}_{ac}^{[k]}}{\partial X_{C_i}} \right) + \mathbf{J}^{ii} [\mathbf{R}_A^{[k]}]^{-1} \mathbf{X}_A^{[k]} \\ &\quad + \mathbf{X}_A^{[k]} [\mathbf{R}_A^{[k]}]^{-1} \left[\mathbf{J}^{ii} - \text{diag} \left(\frac{\partial \mathbf{r}_{ac}^{[k]}}{\partial X_{C_i}} \right) [\mathbf{R}_A^{[k]}]^{-1} \mathbf{X}_A^{[k]} \right], \end{aligned} \quad (4.27)$$

$$\begin{aligned} \frac{\partial^2 \mathbf{U}^{[k]}}{\partial X_{C_i} \partial X_{C_j}} &= \text{diag} \left(\frac{\partial^2 \mathbf{r}_{ac}^{[k]}}{\partial X_{C_i} \partial X_{C_j}} \right) + \mathbf{J}^{ii} [\mathbf{R}_A^{[k]}]^{-1} \left[\mathbf{J}^{jj} - \text{diag} \left(\frac{\partial \mathbf{r}_{ac}^{[k]}}{\partial X_{C_j}} \right) [\mathbf{R}_A^{[k]}]^{-1} \mathbf{X}_A^{[k]} \right] \\ &\quad + \left[\mathbf{J}^{jj} - \mathbf{X}_A^{[k]} [\mathbf{R}_A^{[k]}]^{-1} \text{diag} \left(\frac{\partial \mathbf{r}_{ac}^{[k]}}{\partial X_{C_j}} \right) \right] [\mathbf{R}_A^{[k]}]^{-1} \\ &\quad \cdot \left[\mathbf{J}^{ii} - \text{diag} \left(\frac{\partial \mathbf{r}_{ac}^{[k]}}{\partial X_{C_i}} \right) [\mathbf{R}_A^{[k]}]^{-1} \mathbf{X}_A^{[k]} \right] + \mathbf{X}_A^{[k]} [\mathbf{R}_A^{[k]}]^{-1} \\ &\quad \cdot \left[\left(\text{diag} \left(\frac{\partial \mathbf{r}_{ac}^{[k]}}{\partial X_{C_i}} \right) [\mathbf{R}_A^{[k]}]^{-1} \text{diag} \left(\frac{\partial \mathbf{r}_{ac}^{[k]}}{\partial X_{C_j}} \right) - \text{diag} \left(\frac{\partial^2 \mathbf{r}_{ac}^{[k]}}{\partial X_{C_i} \partial X_{C_j}} \right) \right) \right. \\ &\quad \left. \cdot [\mathbf{R}_A^{[k]}]^{-1} \mathbf{X}_A^{[k]} - \text{diag} \left(\frac{\partial \mathbf{r}_{ac}^{[k]}}{\partial X_{C_i}} \right) [\mathbf{R}_A^{[k]}]^{-1} \mathbf{J}^{jj} \right], \end{aligned} \quad (4.28)$$

where $\mathbf{J}^{ii}$ is an $n - 1 \times n - 1$ matrix where the (i, i) element is one and all the rest are zero.

All the above equations for the gradient and the Hessian are generally applicable to any system of the kind in Figure 4.3. The only thing missing to complete the Newton method computations at this point is the derivation of $\mathbf{r}_{ac}$ and its derivatives, which are dependent on the rectifier. Here, we show the final equations for the half bridge in Figure 4.2, which is based on (4.1).

We can observe from (4.1) that the equivalent input AC resistance of the half bridge rectifier is dependent on the corresponding receiver coil current. The input current of each receiver, however, is set by the combination series tuning capacitances. Since the optimisation scheme in Figure 4.6 defines the values of the resonant capacitances, the corresponding value of the equivalent impedance of the rectifier must be computed iteratively until it converges for every step of the optimisation algorithm. This internal iteration, which is independent of the Newton iteration denoted with k in the above equations, is performed in the white subroutine blocks in Figure 4.6, which also involve the computation of the gradient and Hessian.

The input AC resistance of the rectifier and its derivatives are

$$R_{ac_m}^{[k,l+1]} = \frac{2R_{dc_m}}{\pi^2} + \frac{4V_d}{\pi |\bar{I}_m^{[k,l]}|}, \quad (4.29)$$

$$\frac{\partial R_{ac_m}^{[k,l+1]}}{\partial X_{C_i}} = -\frac{4V_d}{\pi |\bar{I}_m^{[k,l]}|^2} \frac{\partial |\bar{I}_m^{[k,l]}|}{\partial X_{C_i}}, \quad (4.30)$$

$$\frac{\partial^2 R_{ac_m}^{[k,l+1]}}{\partial X_{C_i} \partial X_{C_j}} = \frac{4V_d}{\pi |\bar{I}_m^{[k,l]}|^2} \left(\frac{2}{|\bar{I}_m^{[k,l]}|} \frac{\partial |\bar{I}_m^{[k,l]}|}{\partial X_{C_i}} \frac{\partial |\bar{I}_m^{[k,l]}|}{\partial X_{C_j}} - \frac{\partial^2 |\bar{I}_m^{[k,l]}|}{\partial X_{C_i} \partial X_{C_j}} \right), \quad (4.31)$$

where l denotes the inner iteration index of the subroutines in Figure 4.6. The amplitudes of secondary coil currents and their derivatives are

$$|\bar{I}_m^{[k]}| = \sqrt{\text{Re} [\bar{I}_m^{[k]}]^2 + \text{Im} [\bar{I}_m^{[k]}]^2}, \quad (4.32)$$

$$\frac{\partial |\bar{I}_m^{[k]}|}{\partial X_{C_i}} = \frac{1}{|\bar{I}_m^{[k]}|} \left(\text{Re} [\bar{I}_m^{[k]}] \frac{\partial \text{Re} [\bar{I}_m^{[k]}]}{\partial X_{C_i}} + \text{Im} [\bar{I}_m^{[k]}] \frac{\partial \text{Im} [\bar{I}_m^{[k]}]}{\partial X_{C_i}} \right), \quad (4.33)$$

$$\begin{aligned} \frac{\partial^2 |\bar{I}_m^{[k]}|}{\partial X_{C_i} \partial X_{C_j}} &= \frac{1}{|\bar{I}_m^{[k]}|} \left(\frac{\partial \operatorname{Re} [\bar{I}_m^{[k]}]}{\partial X_{C_i}} \frac{\partial \operatorname{Re} [\bar{I}_m^{[k]}]}{\partial X_{C_j}} + \frac{\partial \operatorname{Im} [\bar{I}_m^{[k]}]}{\partial X_{C_i}} \frac{\partial \operatorname{Im} [\bar{I}_m^{[k]}]}{\partial X_{C_j}} - \frac{\partial |\bar{I}_m^{[k]}|}{\partial X_{C_i}} \frac{\partial |\bar{I}_m^{[k]}|}{\partial X_{C_j}} \right. \\ &\quad \left. + \operatorname{Re} [\bar{I}_m^{[k]}] \frac{\partial^2 \operatorname{Re} [\bar{I}_m^{[k]}]}{\partial X_{C_i} \partial X_{C_j}} + \operatorname{Im} [\bar{I}_m^{[k]}] \frac{\partial^2 \operatorname{Im} [\bar{I}_m^{[k]}]}{\partial X_{C_i} \partial X_{C_j}} \right). \end{aligned} \quad (4.34)$$

The real and imaginary parts of the secondary currents required for the above computations are

$$\frac{\partial \operatorname{Im} [\bar{\mathbf{i}}^{[h,k]}]}{\partial X_{C_i}} = I_1^{[h]} [\mathbf{U}^{[h,k]}]^{-1} \frac{\partial \mathbf{U}^{[h,k]}}{\partial X_{C_i}} [\mathbf{U}^{[h,k]}]^{-1} \mathbf{x}_b^{[h,k]}, \quad (4.35)$$

$$\begin{aligned} \frac{\partial \operatorname{Re} [\bar{\mathbf{i}}^{[k]}]}{\partial X_{C_i}} &= [\mathbf{R}_A^{[k]}]^{-1} \\ &\cdot \left(\mathbf{X}_A^{[k]} \frac{\partial \operatorname{Im} [\bar{\mathbf{i}}^{[k]}]}{\partial X_{C_i}} - \frac{\partial \mathbf{R}_A^{[k]}}{\partial X_{C_i}} [\mathbf{R}_A^{[k]}]^{-1} \mathbf{X}_A^{[k]} \operatorname{Im} [\bar{\mathbf{i}}^{[k]}] + \frac{\partial \mathbf{X}_A^{[k]}}{\partial X_{C_i}} \operatorname{Im} [\bar{\mathbf{i}}^{[k]}] \right), \end{aligned} \quad (4.36)$$

$$\begin{aligned} \frac{\partial^2 \operatorname{Im} [\bar{\mathbf{i}}^{[h,k]}]}{\partial X_{C_i} \partial X_{C_j}} &= I_1^{[h]} [\mathbf{U}^{[h,k]}]^{-1} \left(\frac{\partial^2 \mathbf{U}^{[h,k]}}{\partial X_{C_i} \partial X_{C_j}} - \frac{\partial \mathbf{U}^{[h,k]}}{\partial X_{C_i}} [\mathbf{U}^{[h,k]}]^{-1} \frac{\partial \mathbf{U}^{[h,k]}}{\partial X_{C_j}} \right. \\ &\quad \left. - \frac{\partial \mathbf{U}^{[h,k]}}{\partial X_{C_j}} [\mathbf{U}^{[h,k]}]^{-1} \frac{\partial \mathbf{U}^{[h,k]}}{\partial X_{C_i}} \right) [\mathbf{U}^{[h,k]}]^{-1} \mathbf{x}_b^{[h,k]}, \end{aligned} \quad (4.37)$$

$$\begin{aligned} \frac{\partial^2 \operatorname{Re} [\bar{\mathbf{i}}^{[k]}]}{\partial X_{C_i} \partial X_{C_j}} &= \frac{\partial^2 [\mathbf{R}_a^{[k]}]^{-1}}{\partial X_{C_i} \partial X_{C_j}} \mathbf{X}_A^{[k]} \operatorname{Im} [\bar{\mathbf{i}}^{[k]}] + \frac{\partial [\mathbf{R}_a^{[k]}]^{-1}}{\partial X_{C_i}} \left(\frac{\partial \mathbf{X}_A^{[k]}}{\partial X_{C_j}} \operatorname{Im} [\bar{\mathbf{i}}^{[k]}] + \mathbf{X}_A^{[k]} \right. \\ &\quad \left. \cdot \frac{\partial \operatorname{Im} [\bar{\mathbf{i}}^{[k]}]}{\partial X_{C_j}} \right) + \frac{\partial [\mathbf{R}_a^{[k]}]^{-1}}{\partial X_{C_j}} \left(\frac{\partial \mathbf{X}_A^{[k]}}{\partial X_{C_i}} \operatorname{Im} [\bar{\mathbf{i}}^{[k]}] + \mathbf{X}_A^{[k]} \frac{\partial \operatorname{Im} [\bar{\mathbf{i}}^{[h,k]}]}{\partial X_{C_i}} \right) \\ &\quad + [\mathbf{R}_a^{[k]}]^{-1} \left(\frac{\partial \mathbf{X}_A^{[k]}}{\partial X_{C_i}} \frac{\partial \operatorname{Im} [\bar{\mathbf{i}}^{[k]}]}{\partial X_{C_j}} + \frac{\partial \mathbf{X}_A^{[k]}}{\partial X_{C_j}} \frac{\partial \operatorname{Im} [\bar{\mathbf{i}}^{[k]}]}{\partial X_{C_i}} + \mathbf{X}_A^{[k]} \frac{\partial^2 \operatorname{Im} [\bar{\mathbf{i}}^{[k]}]}{\partial X_{C_i} \partial X_{C_j}} \right), \end{aligned} \quad (4.38)$$

where the iteration index h denotes the higher level iteration for evaluating the correct output power, which is explained in detail in the following subsection. The derivatives of the $\mathbf{R}_A^{-1}$ in (4.38) can be easily calculated since they are diagonal matrices.

4.1.4 Complete Design Algorithm with Simulation Example

The link optimisation method introduced in subsection 4.1.3 only works for a predefined primary coil current. However, the objective in this chapter is to also figure out the Tx coil current that

provides the required power to the Rx loads. One way to achieve this would be to start with a rough estimation of the primary coil current and then manually adapt its value, while running the link optimisation scheme on every change, until we reach the desired outcome.

In this subsection, we propose an automated algorithm that gives as outputs both the values of the secondary series tuning capacitances and the required primary coil current to achieve the output power conditions. The high level flow chart of the algorithm is given in Figure 4.7. The inputs to our method are the number of total coupled coils in the IPT system along with the corresponding z-parameters, the operating frequency, and the desired minimum output power and voltage. For the special case of using the half bridge in Figure 4.2 as a HF rectifier, the output voltage needs to be high enough, so that the equivalent input AC resistance is much larger than the Q factor of the corresponding receiver coil in order to achieve high link efficiency, according to (4.1). The outputs of the design method are the individual resonant capacitance values of each receiver and the Tx required coil current to provide the needed total output power. The design of the rectifier circuits is a prerequisite for the link tuning and the primary coil current and reflected resistance derived from this method can then be used in the inverter design algorithm in chapter 2, so that the complete DC/DC IPT system is fully defined.

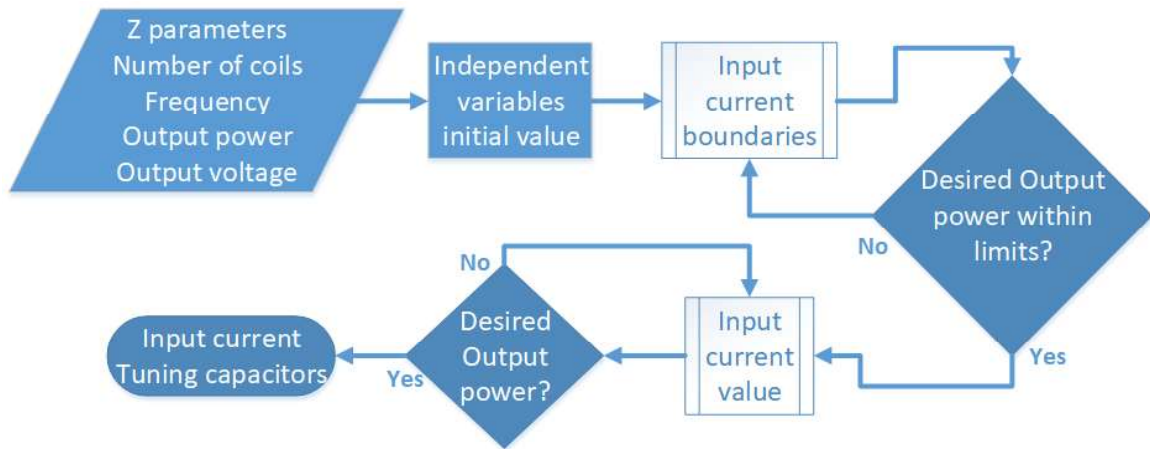


Figure 4.7: Flow process diagram of the main routine that calculates the desired input current and series tuning capacitors for high efficiency operation of a single Tx - multiple Rx's IPT system.

The inputs of the algorithm are used in the "Independent variables initial value" block in Figure 4.7 where the starting points of the series secondary capacitances and the equivalent secondary AC resistors are defined by (4.21) and (4.20), respectively. The initial value for the input current is the equivalent of all the loads at nominal power being individually coupled to the primary, without any cross-coupling. These initial conditions help reduce the total number

of iterations and also ensure convergence to the desired results, especially when the number of receivers is high.

The main function of the flow chart in Figure 4.7 is to calculate the optimal value of the primary current, through the subroutine "Input current value", whose details are shown in Figure 4.8. This subroutine uses a bisection method, with initial boundaries defined in the "Input current boundaries" subroutine. The iterative process terminates either if the output power of each receiver is close enough to the required value, depending on the acceptable tolerance, or if the split of the bisection method is too small.

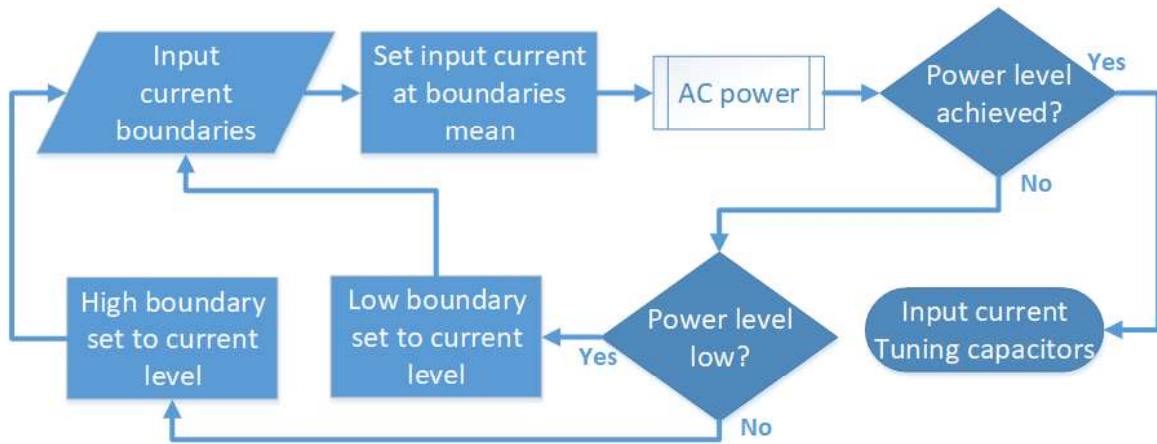


Figure 4.8: Flow process of the “Input current value” iterative method in Figure 4.7. It is a bisection method that uses the input current boundaries calculated in Figure 4.9.

The details of the process flow of "Input current boundaries" subroutine in Figure 4.7 are given in Figure 4.9. This part of the algorithm compares the initial point of the primary current value and multiplies its value by two and by half until the desired power level lies between the two extremes. The subroutine block "AC power" is explained in Figure 4.6, and is executed every time the algorithm adjusts the value of the input primary current.

Numerical Example

Here, we present a numerical example of applying the proposed link design method with the corresponding simulation data for verification. An equivalent version of this example with reduced power output is implemented as a DC/DC converter, the experimental testing of which is presented in our work in [70]. The IPT link consists of one Tx coil and four co-planar Rx coils in the physical configuration shown in Figure 4.10. The distance between the Tx and Rx coils

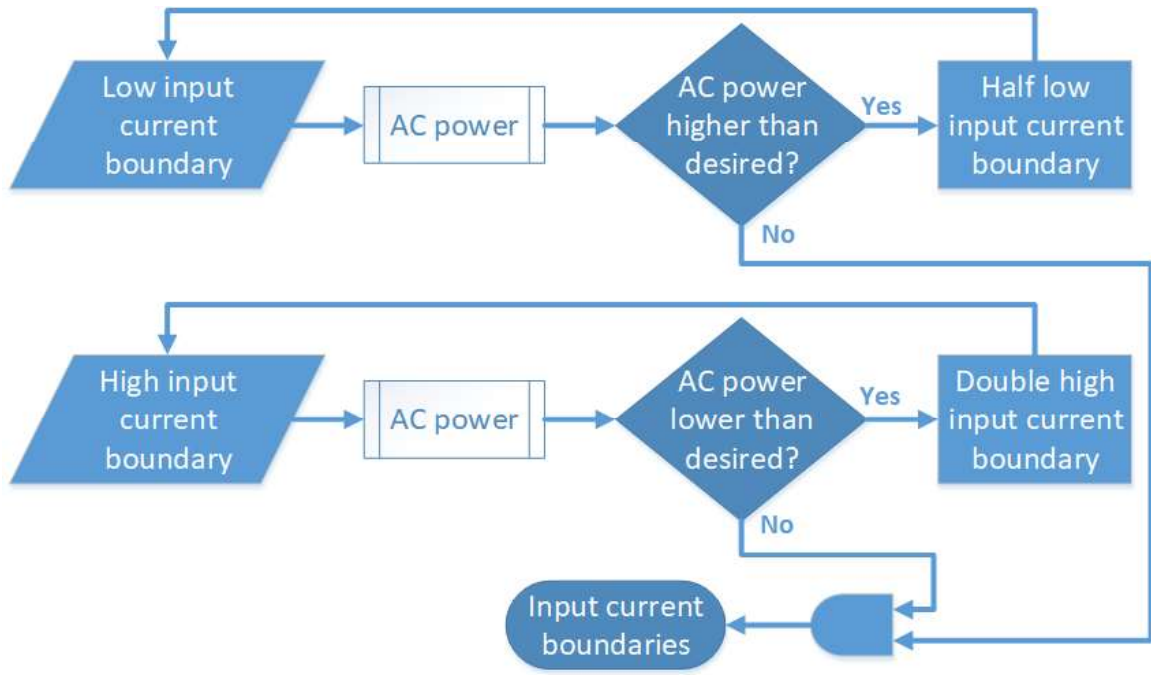


Figure 4.9: Flow process of the “Input current boundaries” subroutine shown in Figure 4.7. This procedure adjusts the upper and lower boundaries of the input current so that the bisection method that follows converges to the desired result.

is 25 mm and each shielding sheet is 35 mm away from the corresponding coil. The z-parameter matrix derived from the finite element field simulation in CST is

$$\mathbf{Z} = \begin{bmatrix} 0.349 & -0.006 & -0.003 & -0.005 & -0.009 \\ -0.006 & 0.632 & -0.018 & -0.0002 & 0.0001 \\ -0.003 & -0.018 & 0.635 & -0.017 & -0.0002 \\ -0.005 & -0.0002 & -0.017 & 0.637 & -0.018 \\ -0.01 & 0.0001 & -0.0002 & -0.018 & 0.631 \end{bmatrix} + \begin{bmatrix} 114.698 & -5.353 & -5.313 & -6.085 & -5.793 \\ -5.353 & +133.327 & -12.011 & -0.743 & -0.055 \\ -5.313 & -12.011 & +138.34 & -11.664 & -0.734 \\ -6.085 & -0.743 & -11.664 & +138.3 & -11.972 \\ -5.793 & -0.055 & -0.734 & -11.972 & +133.671 \end{bmatrix} i,$$

where the sign denotes the relative orientation of the turns of the corresponding coils.

The operating frequency is 13.56 MHz for high link efficiency and the goal DC output voltage of each receiver is 20 V for 20 W of power. Lower voltage with the half bridge topology would

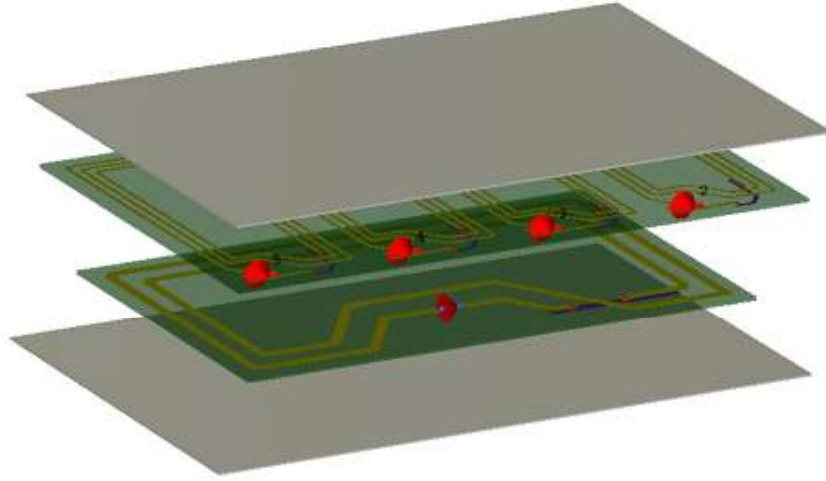


Figure 4.10: Simulation illustration of the IPT link in CST Studio Suite.

reduce the efficiency of the link, because of the voltage drop on the diodes. The diodes of the half bridge (RB088LAM-60TFTR from ROHM Semiconductor) have a forward voltage drop of 0.7 V. Finally, for we set $\gamma = 0.5$ in (4.18) to avoid divergence during the numerical calculations.

The inputs and outputs of the link design algorithm are given in Table 4.1, where it is clear that the objective of the algorithm, i.e. zero reflected reactance to the primary, has been accomplished. Then, we use the reflected resistance and primary output current values to design a single ended Class EF_2 inverter, suitable for the IPT link. The inverter is designed using the method proposed in chapter 2, with the same properties as the Class EF_2 example in that chapter, adapted for the power level required from the receivers in this application. The passive component values of the resulted inverter design are shown in Table 4.2, whereas the device and gate driver remained the same as in chapter 2.

The voltage and current waveforms of the semiconductor devices in the full DC/DC IPT system example are shown in Figure 4.11. Both the transistor and the diodes are operating withing their limits, however the switching performance of the diodes is quite poor at this frequency, because of their high parasitic capacitance. This issue is solved on the practical application in [70] by swapping the RB081LAM-20 Si diodes with WBG equivalent ones. The drain voltage shape of the transistor in the inverter, which is a strong indicator of the reflected impedance of the primary coil driver [148], is equivalent to the measured drain voltages in [70], which shows that the loading characteristics of the experimental set up agree with the simulation. Also, the ZVS and ZVDS conditions are met both in simulation and experiment, which further proves that the ideal expected primary load is present.

Table 4.1: Inputs and outputs of the tuning algorithm for the IPT link shown in Figure 4.10.

	Quantity	Value	Unit
Inputs	f_S	13.56	MHz
	$\mathbf{Z}$	(4.1.4)	—
	P_{dc}	20	W
	V_{dc}	20	V
	V_d	0.7	V
Parameters	γ	0.5	—
	λ	1	—
Outputs	C_{s_2}	97.4	pF
	C_{s_3}	104.8	pF
	C_{s_2}	101.1	pF
	C_{s_2}	97.5	pF
	I_1	2.93	A
	R_R	25.7	Ω
	X_R	−4.3	$\mu\Omega$

Table 4.2: Component values of the inverter design used for the IPT link shown in Figure 4.10.

Quantity	Value	Unit
V_{in}	188.5	V
L_{rfc}	72	μH
f	13.56	MHz
D	25.7	%
C_p	13.4	pF
L_ϕ	1.607	μH
C_ϕ	21.4	pF
C_s	330.3	pF

The input current and the output voltage of the rectifiers in our example are shown in Figure 4.12. The secondary currents are all in phase and with a 90° difference with the primary coil, which is the condition for zero reflected reactance. This is also confirmed through the corresponding measurements in [70]. The output DC voltages of the loads are all around 20 V, as expected from Table 4.2. The small voltage deviation from the desired value in this simulation example were corrected on the experimental rig by connecting a voltage regulator at the output of every rectifier.

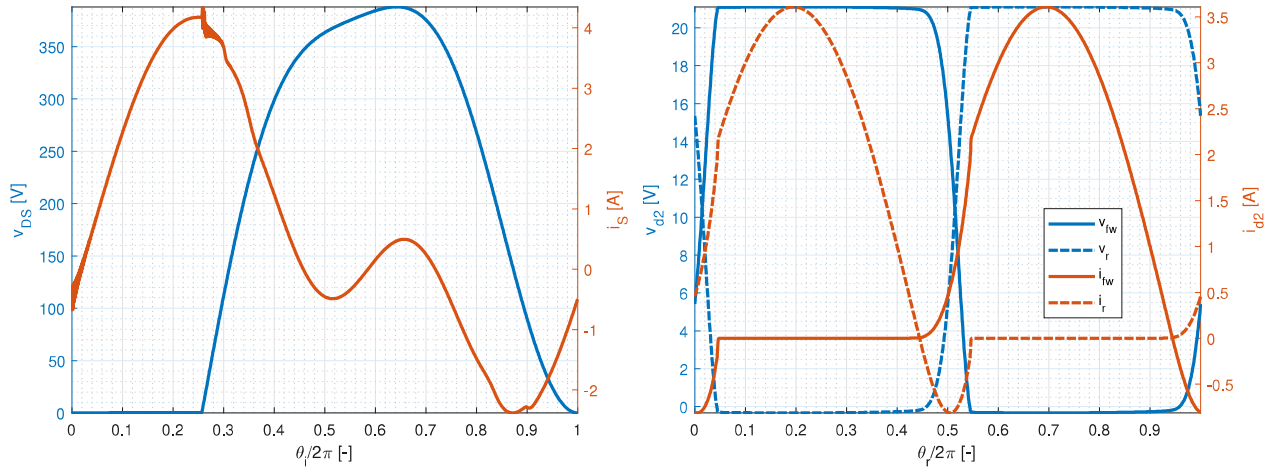


Figure 4.11: Voltage (blue) and current (orange) waveforms of the transistor in the Class EF_2 inverter (left) and the diodes in the half bridge rectifier (right) of the multiple receiver IPT system example. Only the diode waveforms of receiver #2, according to the notation in (4.1.4), are shown here, since the rest of the receivers have similar characteristics due to the link tuning. The time axes in the two subfigures are not synchronised with regards to phase difference for clearer presentation.

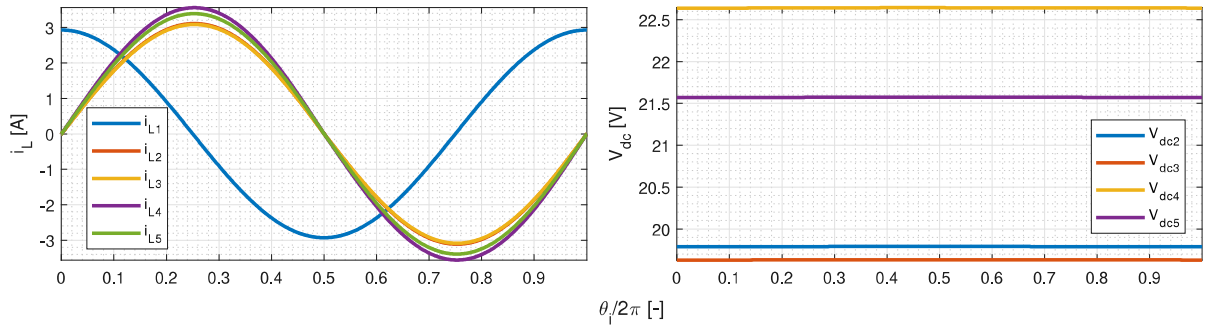


Figure 4.12: Secondary coil currents (left) and output voltages of the rectifiers (right) of the multi-receiver IPT system example.

4.2 Link Estimation

4.2.1 Background

As explained in section 1.4, the optimal operation of any resonant inverter and Class E type inverters in particular is by definition highly sensitive to reactive load changes and thus accurate and reliable estimations of primary and secondary coil impedances as well as coupling factors are crucial. IPT link measurements especially at MHz frequencies are not trivial and contain inherit errors even with specialised equipment [72]. The presence of magnetic shielding on the link, which is a fairly typical practice in IPT link designs [149, 150, 151, 152, 153], complicates

these impedance measurements even further and as a result optimal tuning of the inverter is harder to achieve. Moreover, a conductive shielding plane in close vicinity to the coils can couple capacitively with the IPT link, which further deviates the behaviour of the link from the simple case of two coupled coils.

Here, we propose an indirect method of estimating the impedances of the IPT link by using the coil current measurements of the HF converters of the WPT system. The accuracy of our measurements relies on the assumption that the two converters have been fully characterised and can be modelled precisely. The ability to match the HF converter models with the experimental circuits is successfully and consistently demonstrated in chapter 2 and chapter 3. This method can be useful when the initial traditional link measurement methods fail to produce optimally tuned converters and retuning is required.

4.2.2 Estimation Method

The initial design of the HF converters relies on conventional link measurement techniques. For example, the coil impedances can be measured using an impedance analyser or a VNA [72], and the coupling factor can be estimated by incorporating a secondary resonant AC load, an open-short measurement [20] or using the two step procedure of measuring the voltage ratios with frequency sweep [19]. If, however, the behaviour of the resulting converters is unexpected and does not match the simulation, then the link characterisation needs to be re-evaluated.

The first step involves running the primary coil driver completely unloaded and capturing the corresponding waveforms. Since we are confident in the inverter characterisation, the only degree of freedom and source of error is the primary coil inductance, given that the Q factor is reasonably high and thus irrelevant to the measurements. In the case of the Class E type inverters, the primary coil current is highly dependent on the primary coil inductance, for a given input voltage.

Once the data has been collected, we continue by trying to match the inverter model to the corresponding waveform measurements. Specifically, the output current increases as the primary coil inductance decreases and vice versa. For more robust results, we can gather waveform data for various values of input voltage and duty cycles and base the primary coil inductance estimation upon the average of the matching of this set of measurements. If the various predicted

inductance values do not show large deviations, we can be quite confident on the resulting impedance value.

The next step involves measurements of the full DC/DC IPT system. Our objective now is to determine the effective coupling factor and secondary coil impedance. As was the case with the inverter, our technique is based on the assumption that the rectifier is well characterised and simulated accurately. At this stage, the main waveform measurement of interest is the secondary coil current. Again, multiple measurements can be taken with various DC loads and supply voltages, for more data points for the subsequent simulation.

Once the measurement data has been gathered, we simulate the inverter and the rectifier independently. For the rectifier, we set the secondary coil current and the DC load to the values of their respective measurement. Using the first harmonic values of the input voltage and current of the rectifier, we approximate its input impedance. For the inverter, we try to match the reflected impedance of the simulation to measured input current and output voltage. The reflected reactance mainly affects the amplitude of the output current and the reflected resistance sets the input current level of the inverter.

After all of the above computations, we have multiple pairs of primary reflected impedances along with their corresponding secondary AC loads. It should be noted that the series resonant secondary capacitor of the experimental setup needs to be added accordingly to the final values of the secondary AC loads. These two impedances on the two sides of the IPT link are connected through (1.20), which is a complex equation. Equating the real and imaginary parts of (1.20) produces a system of two equations, which can be solved to provide the values of the secondary coil inductance and coupling factor. This procedure can be done for all the measurements of the various DC loads and taking the mean value of the results at the end.

The exact definition of the system of equations to be solved is

$$R_{eq}^{ij} \left(E_i(L_{s1}) \right) = \frac{\omega^4 k_{ij}^2 E_i(L_{s1}) L_{s2}^{ij} C_{s2}^{ij2} (R_{s2} + R_{ac}^{ij})}{\omega^2 C_{s2}^{ij2} (R_{s2} + R_{ac}^{ij})^2 + (1 - \omega^2 L_{s2}^{ij} C_{s2}^{ij})^2}, \quad (4.39)$$

$$X_{eq}^{ij} \left(E_i(L_{s1}) \right) = \frac{\omega^3 k_{ij}^2 E_i(L_{s1}) L_{s2}^{ij} C_{s2}^{ij} (1 - \omega^2 L_{s2}^{ij} C_{s2}^{ij})}{\omega^2 C_{s2}^{ij2} (R_{s2} + R_{ac}^{ij})^2 + (1 - \omega^2 L_{s2}^{ij} C_{s2}^{ij})^2}, \quad (4.40)$$

where i is the index of the input voltage and j is the index of the DC load. R_{ac} is the real part

of the rectifier impedance and C_{s_2} is the combination of the rectifier impedance and the tuning capacitor. The above system is solved separately for every combination of input voltage and load measurement taken, and the final value of the coupling factor and the secondary coil are derived by the mean of all the solutions. Since the system is non-linear, it is solved numerically and the initial values of coupling and secondary coil used for the first tuning of the converters are used as starting points.

4.2.3 Experimental Example

Description of the IPT System

Here we present an experimental example of the link estimation technique mentioned in the previous section, where the impedance analyser measurements failed to lead to accurate converter designs. The system runs at 3.39 MHz with coils with physically large dimensions and a combination of aluminium and ferrite shielding. Photos of the primary and secondary coils are shown in Figure 4.13 with their details given in Table 4.3.

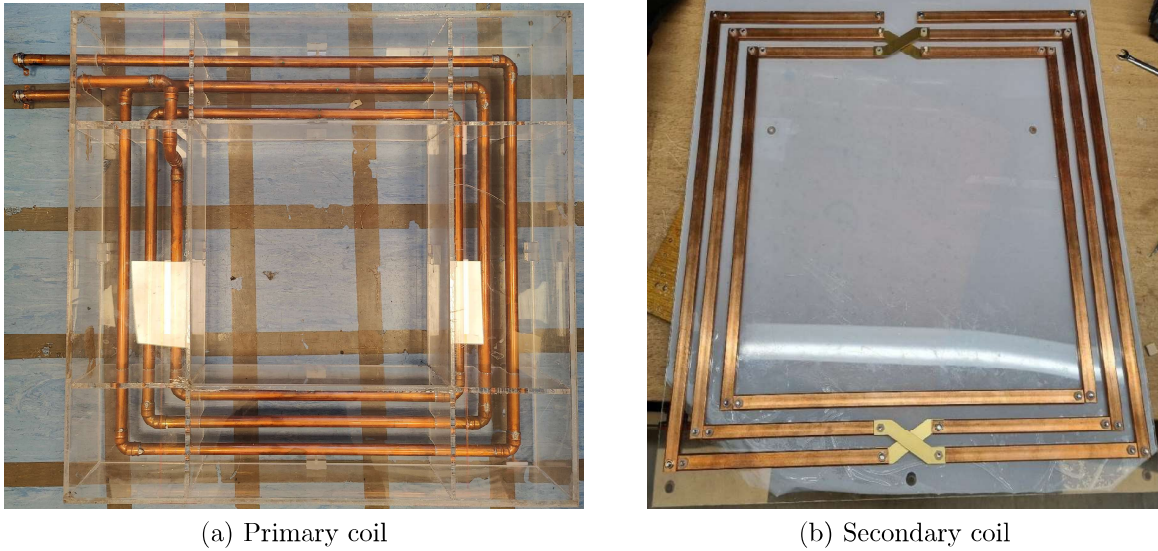


Figure 4.13: Photos of the primary and secondary coil used in the IPT system example.

This IPT system is designed to charge cars with the primary attached to the bottom frame. The emulated electromagnetic environment in the lab is shown in Figure 4.14, where the aluminum sheet on the table represents the bottom of the vehicle. The distance between the two coils is around 15 cm and the distance of the Tx from the shielding is 2 cm. The ferrite plane consists

Table 4.3: Physical characteristics and dimensions of the coils in Figure 4.13.

Parameter	L_{s1}	L_{s1}	Unit
Coil length	74	44	cm
Coil width	74	44	cm
Number of turns	3	3	—
Tube type	Round	Rectangular	—
Tube width	22	12.7	mm

of 6 layers of a 4x4 grid of sheets from WE Electronics (part no: 364003), and lays between the aluminum sheet and the Rx coil.

The inverter is a Class EF₂ parallel push-pull design and the rectifier is a Class DE topology. The inverter configuration was based on chapter 3 and its design was defined using the algorithm in chapter 2. The ϕ inductors are a combination of air-core and cored inductors with the 67 material from Fair-Rite. The PCB layout is the same as the example in chapter 3. The rectifier circuit is the same as in chapter 3, resonating with the receiver coil in Figure 4.13b.

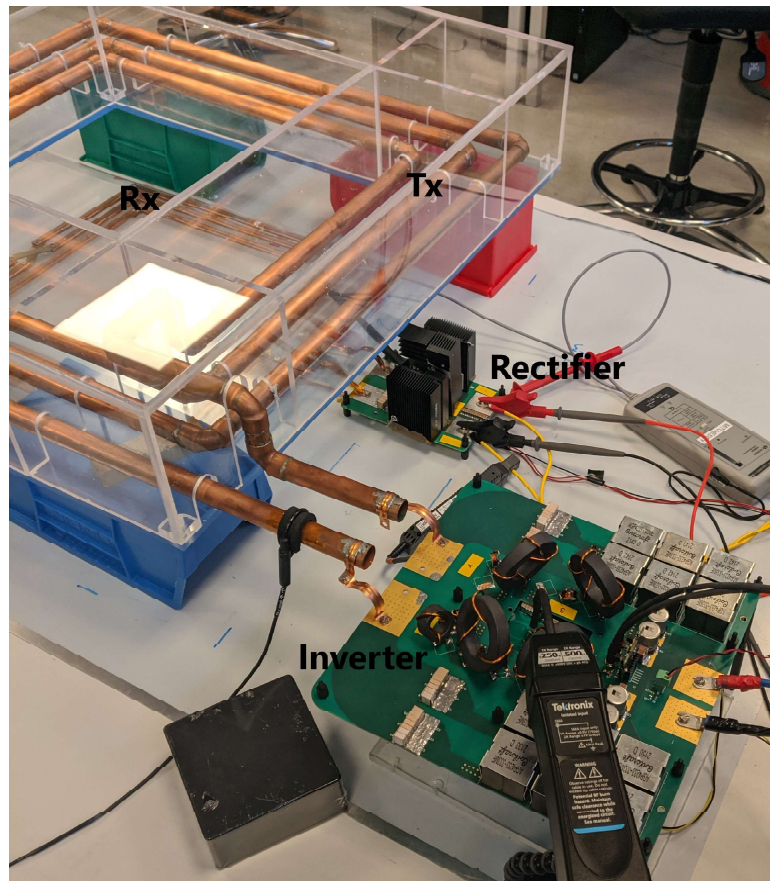
Ferrite Shielding

The benefits of the ferrite shielding over bare aluminum are demonstrated in Figure 4.15. The measurements of the chart in Figure 4.15 were taken with the Keysight E4990A Impedance Analyzer from the system shown in Figure 4.16 at 6.78 MHz, with the shielding on the primary side. The primary coil is the one used as Tx in chapter 3 and the secondary coil is the one used in chapter 2. The coupling estimation method using a resonant secondary AC load is explained in subsection 2.4.4 and the open-short method uses the expression

$$k = \sqrt{1 - \frac{L_{sc}}{L_{oc}}}, \quad (4.41)$$

where L_{sc} is the measured primary inductance with the Rx shorted and L_{oc} is the measured primary inductance with the Rx open. The inductance value in Figure 4.15 is the open measurement.

The coupling factor values from the two measurement methods in Figure 4.15 showcase a slight but consistent difference. In general, the tuned receiver method tends to be more accurate for lower coupling factors, which is the case in Figure 4.15. In addition, the open-short method



(a) IPT system



(b) Tx coil with ferrite

Figure 4.14: Photos of the complete IPT system with shielding and detail of the ferrite shielding of the Tx coil.

relies on very small measurement differences which can be affected by the sensitivity of the equipment. Hence for the case in Figure 4.15, the resonant secondary method produces more reliable coupling factor estimations.

The presence of shielding reduces both the coupling factor and the effective inductance of the coil in close proximity. Also, the conductive sheet introduces parasitic capacitance to the IPT link, which further complicates its characterisation. The ferrite manages to reduce the negative

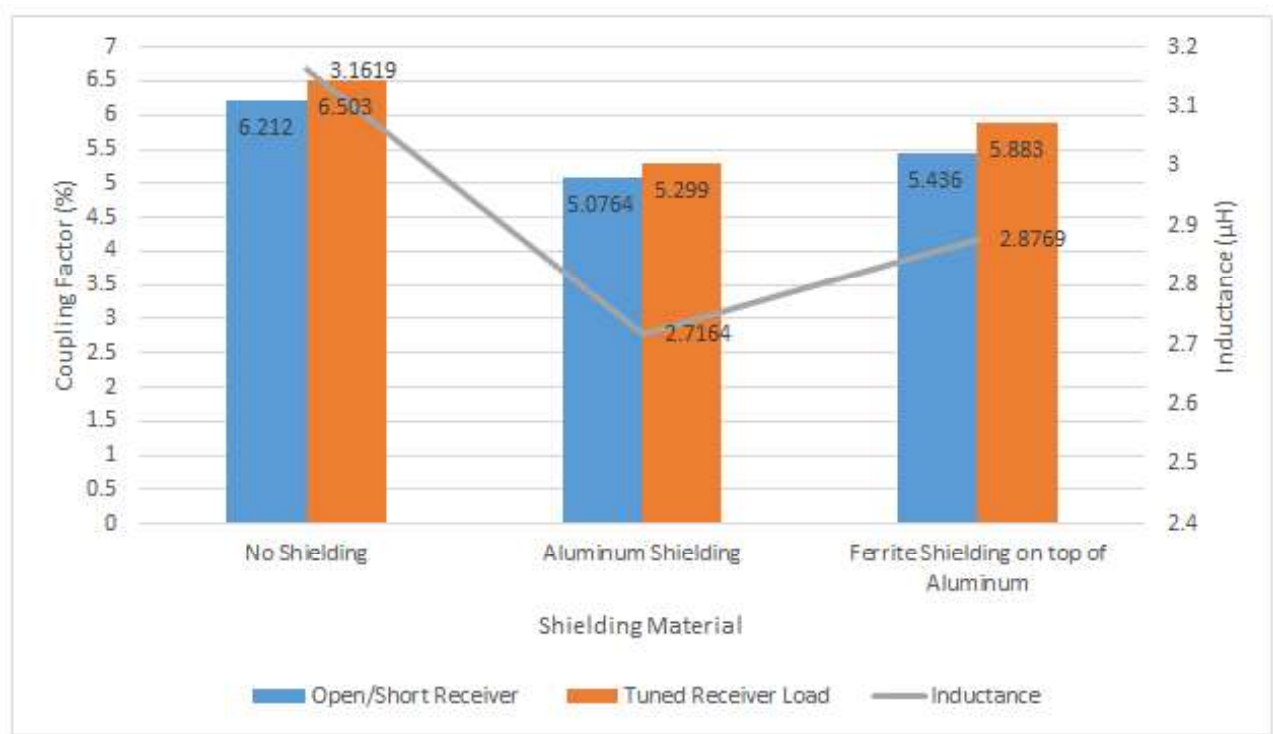


Figure 4.15: Coupling factor and inductance variation with the presence of various types of magnetic shielding.

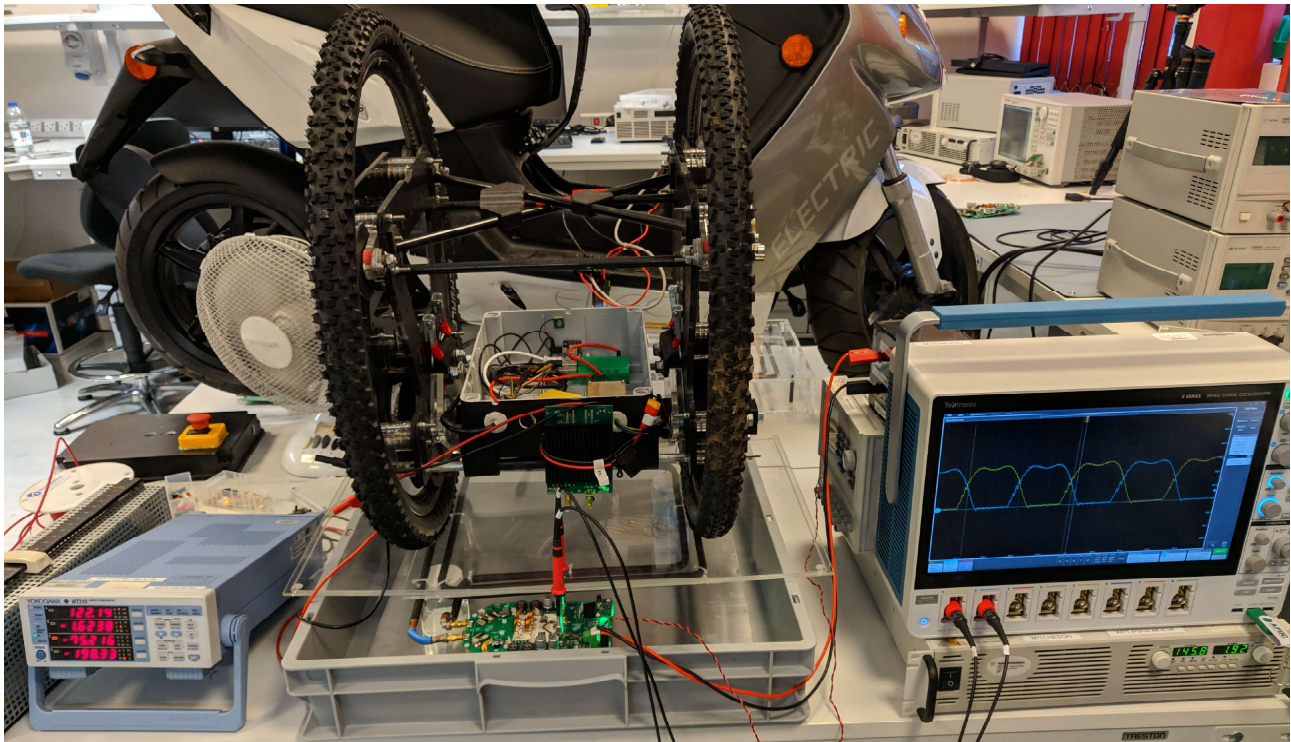


Figure 4.16: Photo of the IPT system used for the measurement of the effect of shielding in Figure 4.15. The primary coil is located on the bottom inside the grey container and the secondary is between the wheels of the autonomous vehicle, which is placed on top of the container.

effect of the shielding to the link efficiency, as shown in Figure 4.15, but does not eliminate it completely.

Link Simulation and Impedance Measurements

The first step of determining the link properties is by performing a finite element (FEM) electromagnetic (EM) simulation at CT Studio Suite. The simulation setup, including the two coupled coils and the shielding, is shown in Figure 4.17. The simulation resulted in $9.12\mu\text{H}$ primary inductance, $5.47\mu\text{H}$ secondary inductance, and 13 % coupling factor.

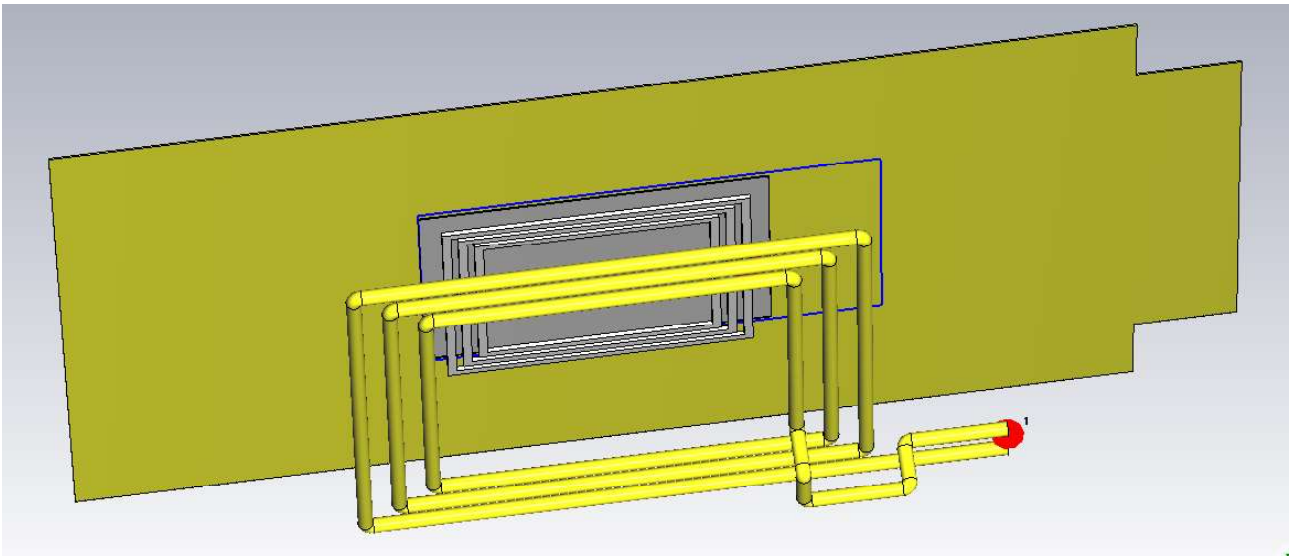


Figure 4.17: Simulation setup with transmitter coil, receiver coil, ferrite sheet shielding and aluminium sheet of electric vehicle (EV) mimic.

Next, we perform measurements using the impedance analyser. Both low frequency (100's of kHz) and high frequency (low MHz around resonance) measurements were performed and the results are given in Figure 4.18 and Figure 4.19, respectively. The low frequency analytic continuation of the fitted inductor model in Figure 4.19 agrees with the corresponding measurements in Figure 4.18, which is a sign of consistency in the measurements. Also, the inductor models match the measured impedances in Figure 4.19.

By comparing the simulation results with the impedance analyser measurements we observe a significant difference in both inductance values and Q factors. The measured effective inductances for both the primary ($10.088\mu\text{H}$) and the secondary coil ($7.347\mu\text{H}$) are over 10 % larger than the simulated ones, which in terms of inverter design is significant. In addition, the

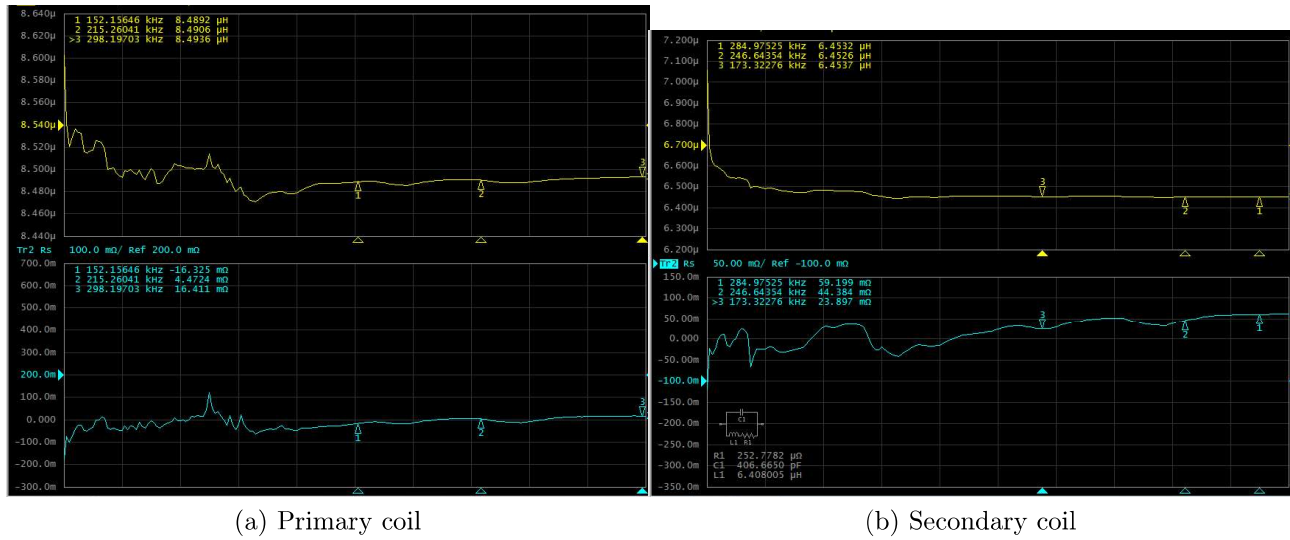


Figure 4.18: Low frequency impedance measurements of the IPT link in Figure 4.14a.

resonant frequency is measured over 1 MHz lower than the simulated prediction and is lower than the 3rd harmonic. As shown in chapter 3, the Class DE rectifier input current contains mainly distortion from the 3rd harmonic, which could possibly further detune the inverter. The most important discrepancy, however, with simulation is the Q factor, since the impedance measurements for the series coil parasitic resistance gave $4.062\ \Omega$ for the primary and $3.022\ \Omega$.

Circuit Measurements and Link Estimation

For the initial HF converter designs we used the measured inductance values of the two coils and the simulated coupling factor and Q factors. Measuring the coupling factor in our shielded setup was not reliable and the measured Q factors were too low to be realistic. The behaviour of the resulted circuits did not match the simulation and the transistors of the inverter were hard switching. The tuning of the Class DE rectifier is independent of the Rx coil. When simulating the rectifier with the measured secondary coil current value, the waveforms and outputs match, which confirms that the rectifier circuit is true to its intended design.

The above mentioned observations are strong indicators that the link characterisation on which the converter designs were based contains errors. To solve that, we apply the link estimation method described in the previous subsection, starting by running the inverter unloaded. The measured waveforms of the unloaded inverter are shown in Figure 4.20, where the voltages are measured with the Tektronix optical probes and the current is measured with a Rogowski probe from Keysight.

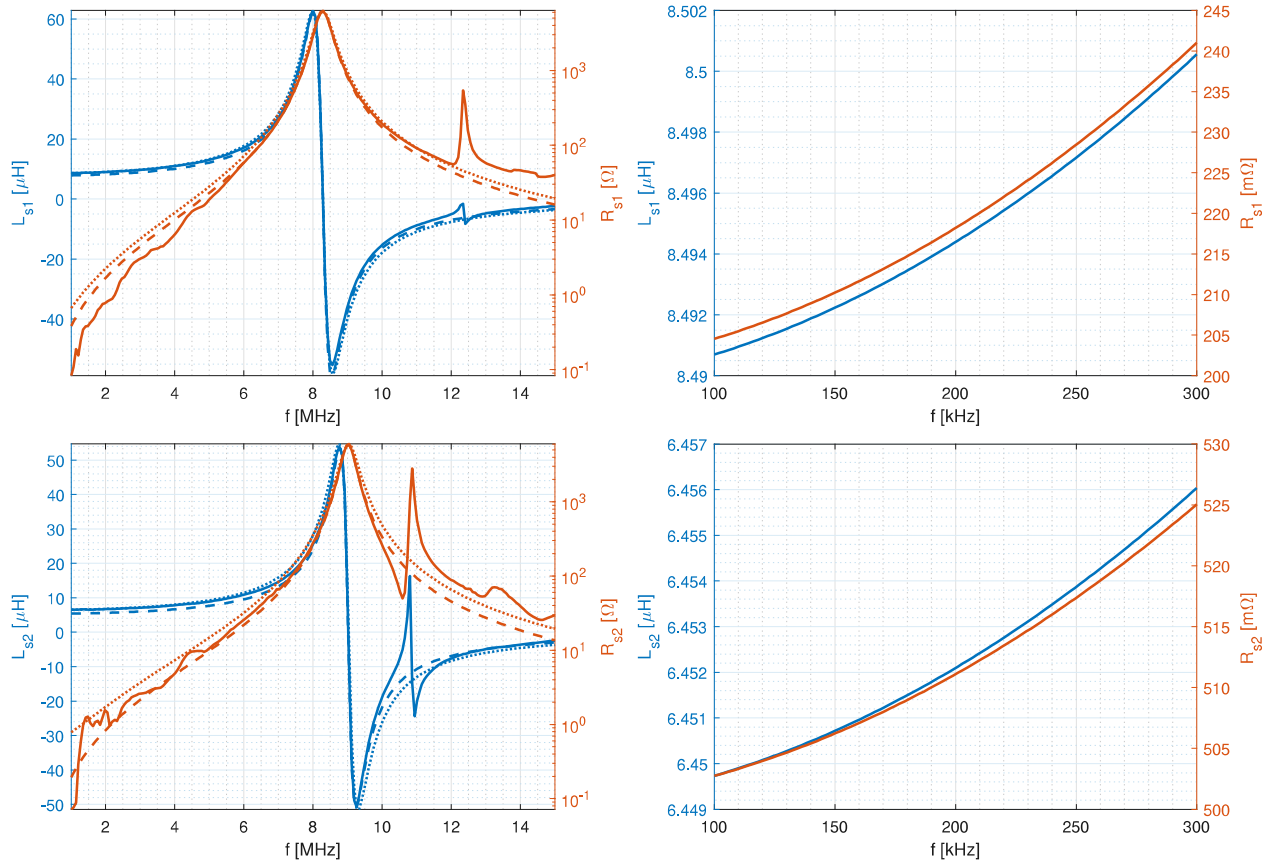


Figure 4.19: High frequency impedance measurements of the IPT link in Figure 4.14a (solid line in the two left curves). The source of secondary resonance higher frequency resonance is the coupling of the opposing side of the IPT system since the measurement took place with the complete system in place, and thus can be ignored. The dashed line is the fitted inductor model of the measurement device. The dotted line is derived by combining the low frequency inductance measurements in Figure 4.18 with the resonance frequency point. The curves on the right are the analytic continuation at low frequencies of the fitted model on the left.

From the power consumption (9 W) of the experiment in Figure 4.20 we can confidently conclude that the Q factor measurements of the impedance analyser in Figure 4.19 are wrong and the series resistance of the primary coil is closer to the simulated value, which is an order of magnitude lower than the measured value. The mean value of the primary coil inductance, after matching the measurements with simulation for several input voltage levels, is $10.123 \mu\text{H}$ with a standard deviation of 55.1 nH , which agrees the impedance analyser measurements. This was expected, since the primary coil is too far away from the shielding for its impedance to be altered meaningfully.

The next step involves measurements with the complete IPT system connected. We perform measurements with three DC load values at a constant input voltage. The DC measurements

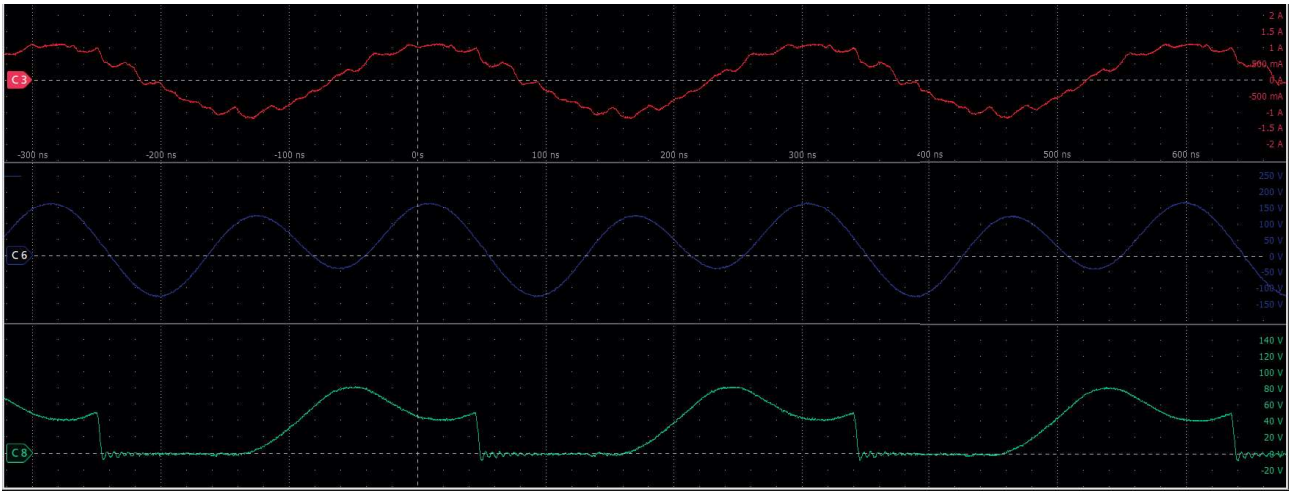


Figure 4.20: Unloaded detuned inverter waveforms at 30 V input voltage. The primary coil current is in red, the drain voltage is in cyan, and the ϕ branch capacitor voltage is in blue. The noise on the output current is an artifact of the Rogowski current probe.

are given in Table 4.4, where again the secondary Q factor agrees with the simulated value rather than the impedance measurements based on the power consumption of the system. The corresponding waveforms of the of the DC measurements in Table 4.4 are shown in Figure 4.21.

Table 4.4: IPT system measurements for link characterisation at 62 V input voltage.

Parameter	Value			Unit
R_L	80	114	132	Ω
I_{in}	0.53	0.66	0.69	A
V_{out}	37.6	50.7	55.6	V
P_{out}	17.6	22.5	23.4	V

Following the procedure described in the previous section for the measurements of the complete system results in mean secondary coil inductance and coupling factor of 7.98 μH and 11.5 %, respectively. The deviation on these estimations is 241 nH and 1.1 %, respectively. The percentage difference of effective secondary inductance and coupling factor of our estimation method compared to measurements and simulation is 9 % and -11.5 %. The simulated, measured and estimated link characterisation figures are summed up in Table 4.5 These differences are quite significant when it comes to tuning the resonant converters, especially for the case of the coil reactance, and they are the reason why the operation of initial design turned out so detuned.

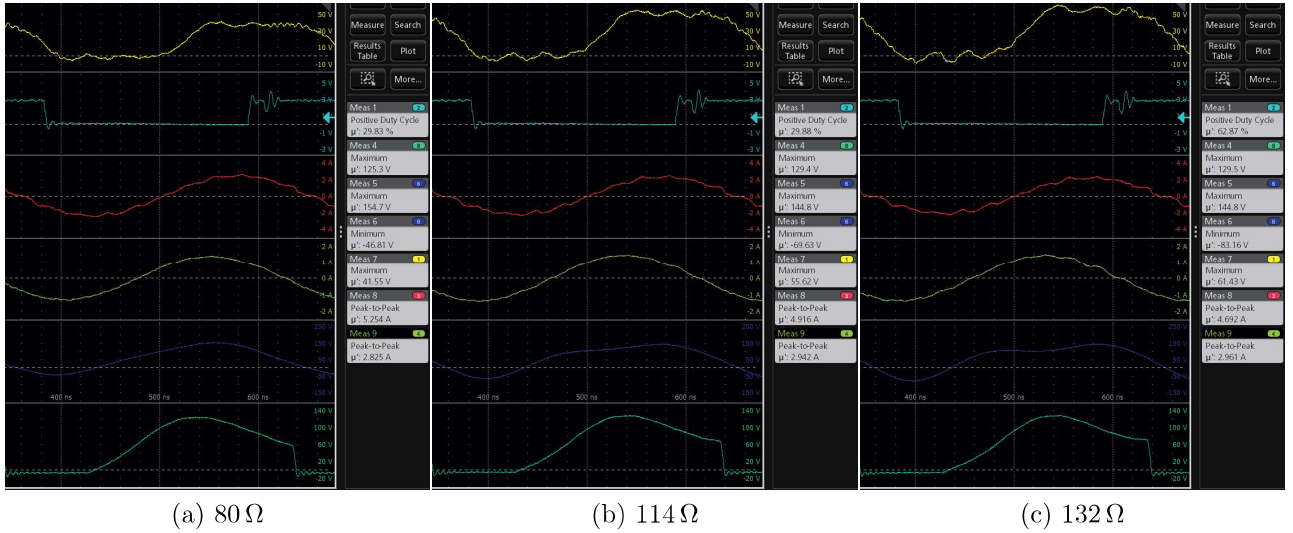


Figure 4.21: Waveforms of the various DC/DC measurements from Table 4.4. The voltage across one of the diodes on the rectifier is in yellow, the input signal to the gate driver is in light blue, the primary coil current is in red, the secondary coil current is in green, the voltage across one of the ϕ capacitors is in blue, and the drain voltage across one of the transistors is in cyan.

Table 4.5: Link characterisation results from EM simulation, impedance analyser measurements and the proposed method.

	CST	E4990A	Estimation	Unit
L_{s1}	9.12	10.08	10.12	μH
L_{s2}	5.47	7.45	7.98	μH
k	13	12.6	11.5	%

4.3 Summary

The first section of this chapter describes an algorithm for calculating the required values of the secondary resonant capacitors in a one to many resonant IPT link. The exact mathematical formulation for the case of the current driven half bridge rectifier was derived and a simulation example that satisfies the maximum power throughput condition while simultaneously eliminating reflected reactance was shown to verify the results of the algorithm. An experimental application of our algorithm is published in [70].

Once the number of receivers exceeds the simple case of one, combined with the input reactance of the rectifiers and the cross-coupling effects between individual receivers, tuning the link for zero reflected reactance to the primary becomes a complex task that cannot be solved with just trial and error. The definition of our solving algorithm is flexible and can accommodate

for various operating conditions. Future work will include different inverter topologies in the algorithm, as well as other operating conditions, such as ensuring specific power level on each receiver.

The second part of the section illustrates a method of implicit link measurements using the HF converter waveforms. An example where traditional impedance analyser measurements and FEM EM simulation failed was presented. Our method managed to correct the initial measurements by 10%, which is very important for successful converter designs. Following the proposed methodology, a test rig can be built, with resilience to hard switching, for the characterisation of complex IPT link with shielding and magnetic field shaping materials in close proximity to the coils.

Chapter 5

Active Class E-type Inverter Control

5.1 Background

Unlike the Class D primary drivers, the Class E type inverters are low bandwidth, operating at a specific frequency, and maintain their optimal operating conditions and soft-switching only for a specific load [19]. Even the current load-independent Class EF [1] and Class E [154] inverters, cannot maintain stable secondary outputs with changes in coupling, and are still negatively affected by reflected reactance. In addition, changing the frequency for example in a Class E-type inverter for changes in load, as is the case in the bridge inverters, would detune the circuit and negatively affect performance. A frequency modulation scheme for maintaining output voltage on a Class E voltage load-independent inverter is presented in [155]. However, this type of load independence is not ideal for WPT, since it cannot accommodate the unloaded primary coil operation.

Also, changes in duty cycle in these resonant circuits do not translate in control of output characteristics as it happens with traditional PWM converters, as explained in chapter 2. The duty cycle is primarily affecting the ZVS condition [156] and a control scheme of it can be used to ensure high efficiency operation.

Another way to adjust the behaviour of the inverter in real-time is by using variable energy storing components. Mechanically variable inductors and capacitors or component arrays [157] are not suitable HF applications because of their inherently low speed of change and losses

introduced by the relays and switches required. Electrically controlled capacitors such as varactors [158] or inductors such as saturable reactors [159, 160, 161, 162, 163] have typically lower Q factors, SRFs and power handling capabilities and thus reduce efficiency.

Here, we investigate the feasibility of an active control scheme for Class E-type inverters using various combinations of its electrical signal, i.e. the input voltage, the duty cycle and the switching frequency. As explained in section 1.3, the inverter typically has a prior power conversion stage to produce the required supply voltage, so its input voltage can be controlled by the duty cycle of the power supply. We perform a variety of simulations and experiments to prove the proposed concept of active control.

5.2 Operation Range of the Passive Inverter

In this section we perform an analysis of the operation of the open-loop Class EF inverter over various loading conditions. We run a comprehensive simulation using the method in section 2.7, where the reflected load is modelled as an AC voltage source at the switching frequency in series with the primary coil, as shown in Figure 5.1. Based on the relevant literature, one of the most suitable design candidates for HF IPT systems with the best performance on varying load is the circuit presented in [1], hence the study that follows is based on data from the load-independent Class EF operation.

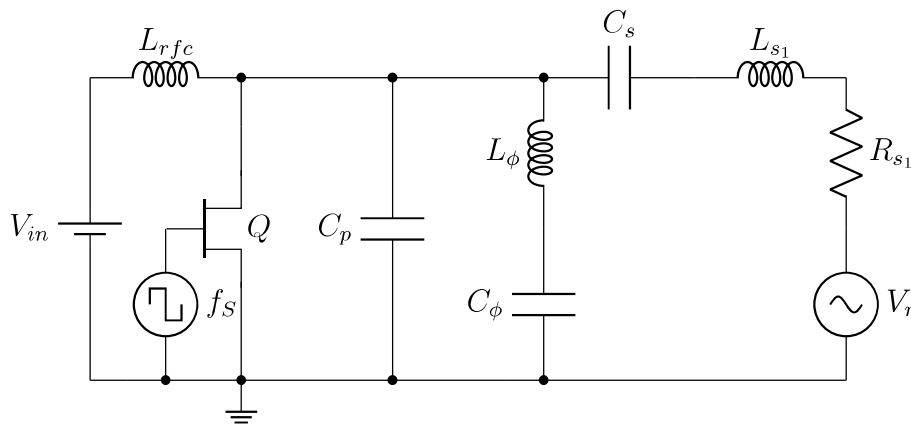


Figure 5.1: Class EF inverter circuit diagram with the reflected load modelled as an AC voltage source V_r at the switching frequency f_s in series with the primary coil L_{s1} .

5.2.1 Analysis of the Load Independent Class EF Inverter

The component values used for the experimental verification of the load independent inverter design in [1], as stated in the paper, lead to over 120 V of hard switching in the drain voltage and 1 A variation in output current in simulation. These findings can be confirmed from the simulated waveforms in Figure 5.2. Such high level of hard switching would not be operational in a real circuit and would result in permanent damage of the GaN device. For this reason, an optimal tuning of the load independent Class EF circuit is required for fair investigation of its operational range under varying load.

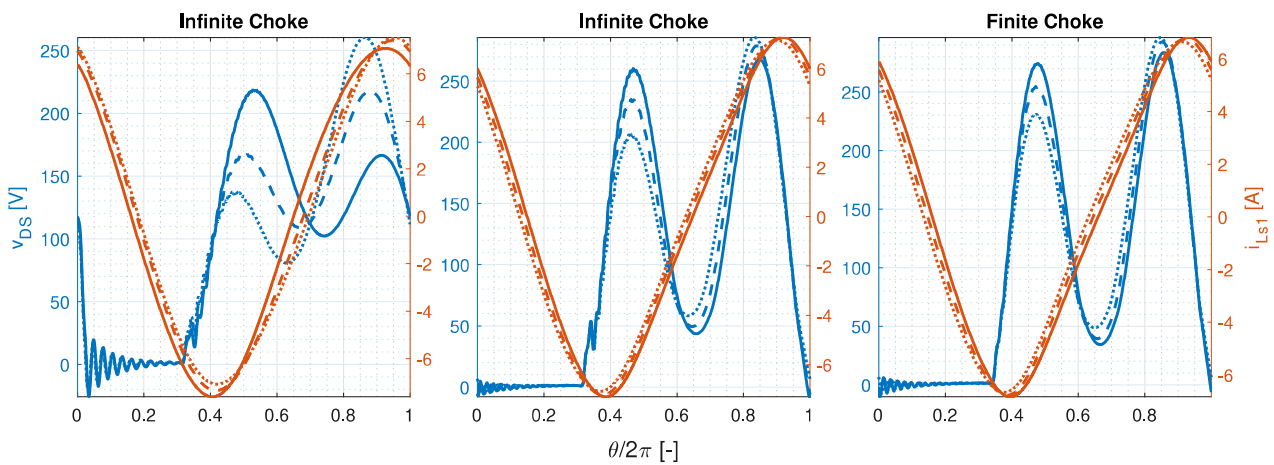


Figure 5.2: Drain voltage (blue) and Tx coil current (orange) waveforms of various 150 W 13.56 MHz load independent designs. The left figure is from [1], the center figure results from the design inputs from [1] but tuned with the algorithm in chapter 2, and the right figure shows a finite choke load-independent design using the method proposed in subsection 2.5.5. The solid line is for the unloaded case, the dashed line is for the partly loaded case and the dotted line is for the ideal load. The drain waveforms of the finite choke are smoother because a gate resistor is used, whereas the simulations of the two infinite choke cases have no damping resistors in the gate.

We use the load-independent design inputs, namely the resonant frequency of the ϕ -branch and the slope of the drain voltage at turn-on, to come up with an optimal Class EF inverter design using the algorithm proposed in chapter 2. The resulted waveforms of the inverter are shown in Figure 5.2 and compared with the traditional FO design outcomes. Unlike the simulation from [1], our version achieves ZVS and manages to maintain it across the entire range of the reflected resistance. In addition, our proposed alternative version has a much lower deviation in output current phase and amplitude. The adjustment of component values from [1] from our design algorithm is -52% for C_p , 25% for L_ϕ , and -20% for C_ϕ .

We also designed a current load-independent inverter with a finite choke, using the method in section 2.5. Applying the load-independent conditions to a FO analysis would be mathematically too complex and practically unusable, as explained in chapter 2. With our inverter design approach however, this process is automated algorithmically, and the resulting waveforms are shown on the right of Figure 5.2. The input choke inductance value is chosen to be 1 μH , 80 times less than the infinite choke version, which could be beneficial for volume constrained applications. The values of all the components of the corresponding circuits from Figure 5.2 are given in Table 5.1.

Table 5.1: Component values of the infinite and finite load-independent designs in Figure 5.2 using the algorithm in chapter 2.

Parameter	Infinite	Finite	Unit
V_{in}	98.41	100	V
L_{rfc}	80	1	μH
f_S	13.56	13.56	MHz
D	30	32.3	%
V_{dd}	6	5	V
R_g	0	2	Ω
Q	GS66504B	GS66504B	—
C_p	166.56	182.4	pF
L_ϕ	228.825	230	nH
C_ϕ	218.48	217.6	pF
C_s	131.84	126	pF
L_{s1}	1.18	1.24	μH
R_{sL}	6	6	Ω

5.2.2 Operation State Mapping

For the next stage of our analysis, we use the optimally tuned finite choke load-independent Class EF inverter from the previous subsection and simulate it across a large reflected complex load range. The complex load is modelled as shown in Figure 5.1 with amplitude from 0 to 1.2 of the equivalent effect of the ideal resistive load and phase from 0 to 2π . The ideal load of 6 Ω corresponds to amplitude of 38.6 V with phase of 2.35 rad.

Since such analysis involves the computation of many data points, we simulated the device using the method in section 2.6. This means that the effects of the non-linear capacitances of the device are included but the stray inductances are omitted. This decreases the time required

for the computations significantly, but also reduces the accuracy, since resonant ringing effects are not captured. For this reason, the performance results from the study conducted in this section are generally better than what would be observed in the real world.

The map of the state of operation of the inverter based on the reflected load is presented in Figure 5.3. The circuit is defined to operate as an inverter when the Tx produces power and as a rectifier when the Tx consumes power. The circuit enters the overvoltage operation when the peak of the drain voltage exceeds 650 V and overcurrent operation when the absolute peak current on the device exceeds 15 A. However, normal operation does not necessarily mean safe operation, as the device could be hard switching or reverse conducting beyond its power handling capabilities. As expected, the load-independent Class EF operates as an inverter without exceeding the device rating at any reflected voltage amplitude as long as the phase does not deviate much from the ideal. Non-ideal phase loads can be accommodated as long as their amplitude is very low.

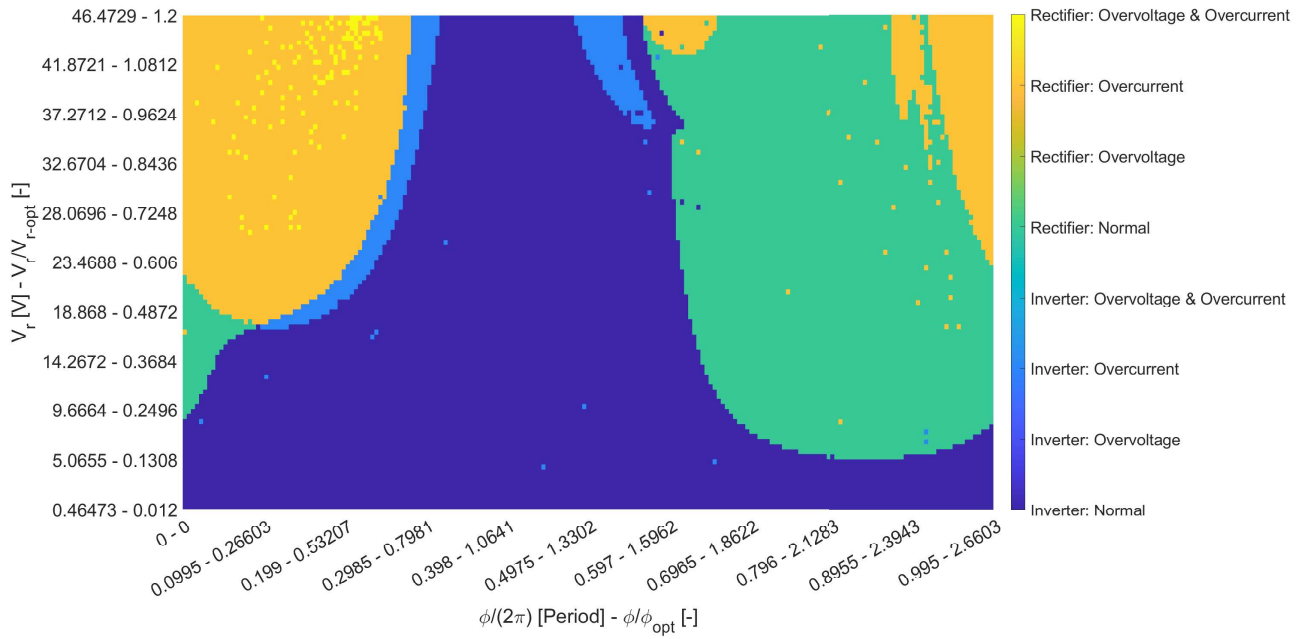


Figure 5.3: State of operation map for the infinite choke load-independent inverter based on the reflected load. The left value on the horizontal and vertical axes are the absolute values and the right ones are the relative ones to the ideal load. The overvoltage and overcurrent states are based on the limits of the transistor from the datasheet.

Waveform examples of two instances from Figure 5.3 are presented in Figure 5.4. The examples are selected at the same load amplitude, with specific load phases so that one is in inverting mode and the other is in rectifying mode. The operation mode can be also confirmed from

the sign of the input current as well as the shape of the drain voltage, according to the load estimation technique proposed in [148].

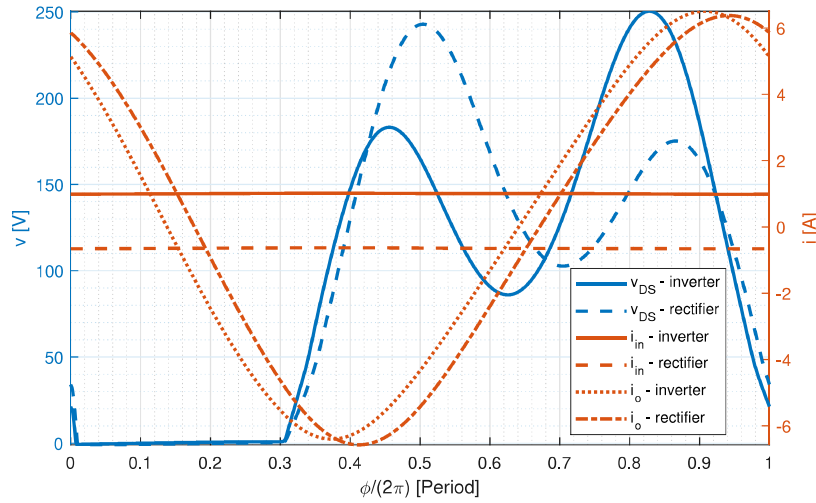


Figure 5.4: Drain voltage (blue) and input and output currents (orange) of the Class EF operation during two instances in Figure 5.3. The inverter operation is at 114% and the rectifier is at 193% of the optimal phase load. Both examples run at 80% of the optimal load amplitude.

An important metric indicating efficient operation and even the possibility of failure is the drain voltage at turn-on, and such information is not shown in Figure 5.3. Ideally, the goal is to maintain ZVS (and even ZVDS if applicable) conditions in a load range as broad as possible. The switching voltage condition map for the inverter example in this section is given in Figure 5.5, where the data points with any amount of noticeable brightness indicate unacceptable operation. When taking into account the information from Figure 5.5, the safe operation range of the Figure 5.3 is even further restricted.

Finally, we calculate the input power at all these load combinations and the results are presented in Figure 5.6. The designed power is only produced in the highly bright area around the ideal load value. At every other loading condition, the inverter fails to satisfy the required power condition of 150 W. It must be noted that the presence of a DC/DC regulator at the output of the rectifier on the Rx side would enlarge the loading range with the required power. However, the regulator itself has limitations on the range of power conversion, adds complexity, increases cost, and reduces the overall efficiency of the WPT system. In addition, the reflected reactance of the rectifier, especially from the non-resonant ones [25], is heavily dependent on the output resistance, so the operation of a regulator at the output of the rectifier may potentially detune the inverter. The information from Figure 5.6 reduces even further the useful operation range

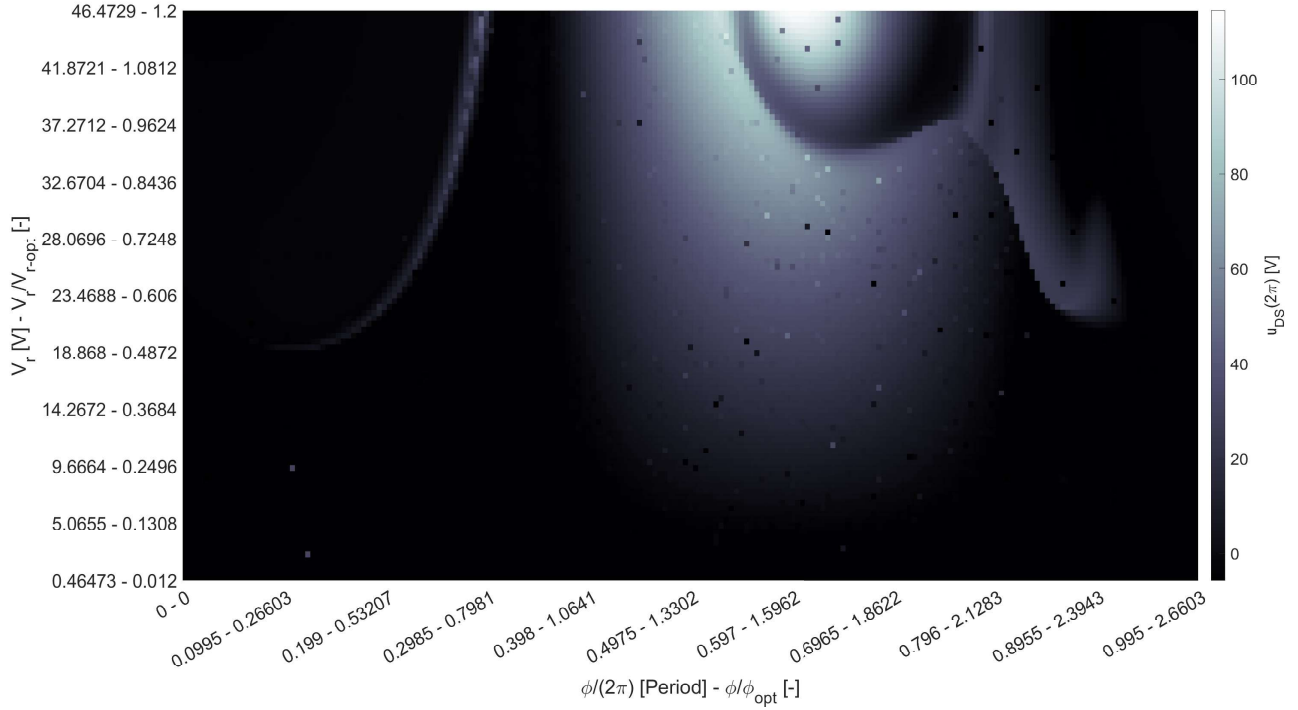


Figure 5.5: Map of the drain voltage at turn-on of the load-independent Class EF inverter based on the amplitude and phase of the load.

of the inverter in Figure 5.3. This observation further proves the need of an active control scheme to ensure high efficiency and power delivery at broad loading conditions.

5.2.3 Reflected Load Identification Techniques

When operating at MHz frequencies, the real time measurement of the reflected load, and especially the primary coil current phase, based on output waveforms is impractical and prone to errors [164, 165]. For this reason, implicit load characterisation methods based on other internal waveforms of the HF primary driver are used. The two main approaches of using the information from these measurements are split into time domain [148, 166] and frequency domain estimations [112], measuring the drain and ϕ capacitor voltages, respectively. Even though the methods proposed in [148] and [112] do manage to produce an accurate estimator of the reflected load, the characterisation model is trained using machine learning from a large amount of experimental data points, and no explanation of the underlying physical principle is provided.

As explained in section 2.4, the DC component of the drain voltage is always the supply voltage,

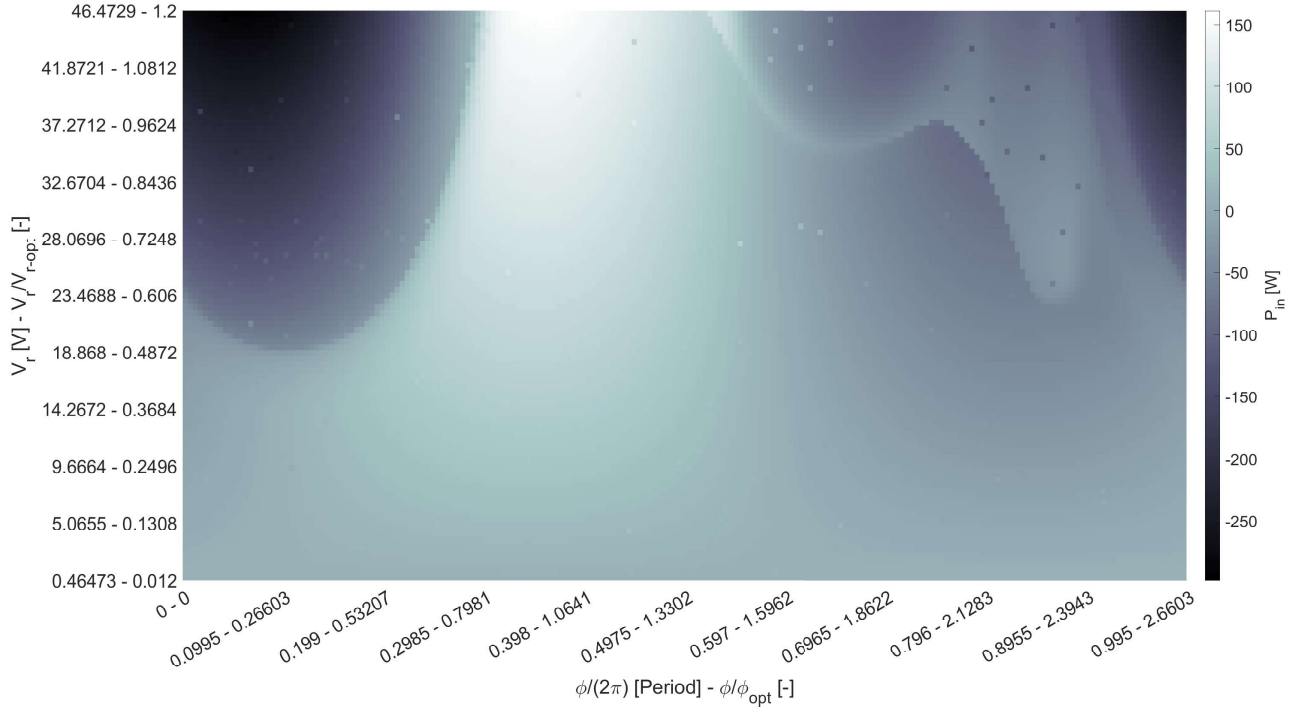


Figure 5.6: Map of the input power of the load-independent Class EF inverter based on the amplitude and phase of the load.

since there is practically almost no real power consumed by the input choke inductor (apart from its series parasitic resistance). This is also the case for the ϕ capacitor because it is operating as a DC block at the ϕ -branch. From (2.27) we see that the main two harmonic contents of the drain voltage are at the switching frequency and the ϕ -branch resonance. From (2.32), the main components of the voltage across the ϕ -branch capacitor are at the switching frequency, the ϕ -branch resonance and τ_2 , which is higher than τ_ϕ , as shown in Figure 6.3.

For the case of the load independent design, the main harmonic contents of the waveforms of interest, according to the above analysis, are the three lowest ones. The amplitude and phase of the three main harmonics in the drain and ϕ capacitor voltages are shown in Figure 5.7 and Figure 5.8, respectively. These graphs correspond to the operation of the load-independent design from Figure 5.1, with the supply voltage turned down to 63 V for better quantitative matching with the results shown in [148] and [112]. The reflected load is transformed to a complex impedance with the real part ranging to negative values to represent the rectifier operation and the imaginary part transformed to a range of negative to positive inductance.

Since all the information of Figure 5.7 is included in time domain and used for the reflected impedance estimation method, theoretically the approach of [148] should be capable of produc-

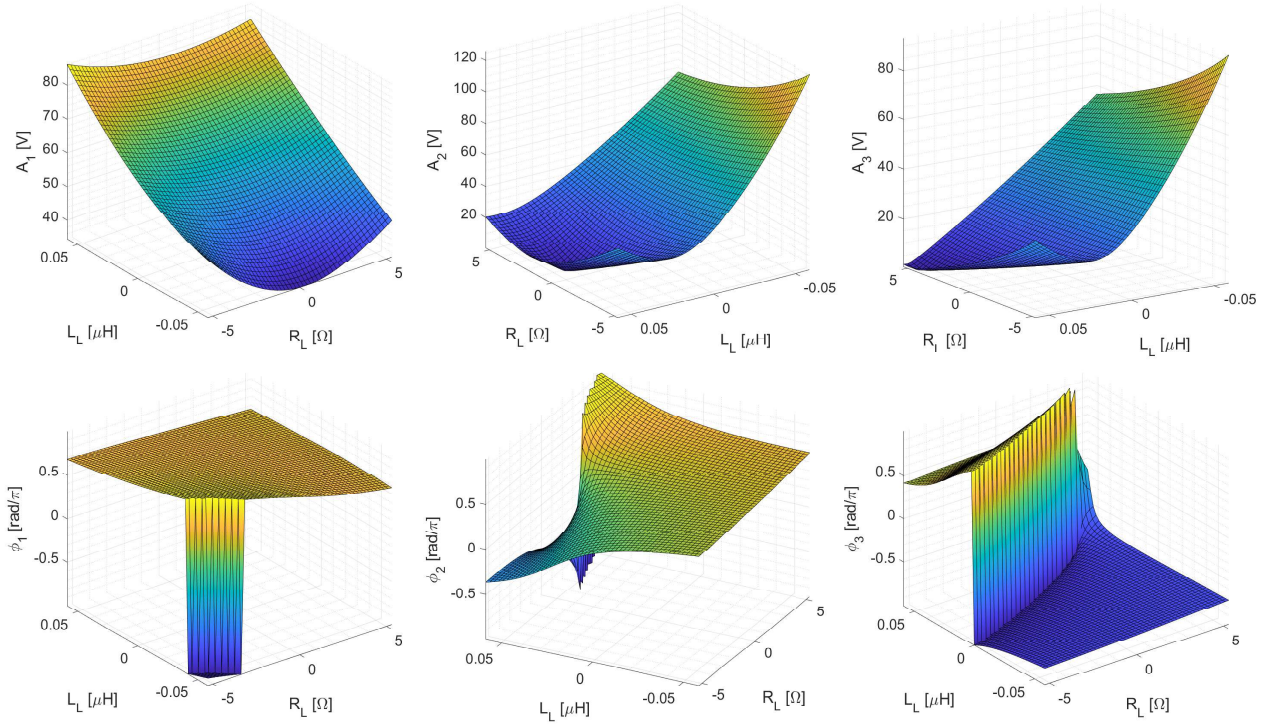


Figure 5.7: First three harmonic amplitudes (top) and phases (bottom) of the drain voltage of the load-independent inverter example across a range of reflected impedance. The phase discontinuity results from the range being defined from $-\pi$ to π .

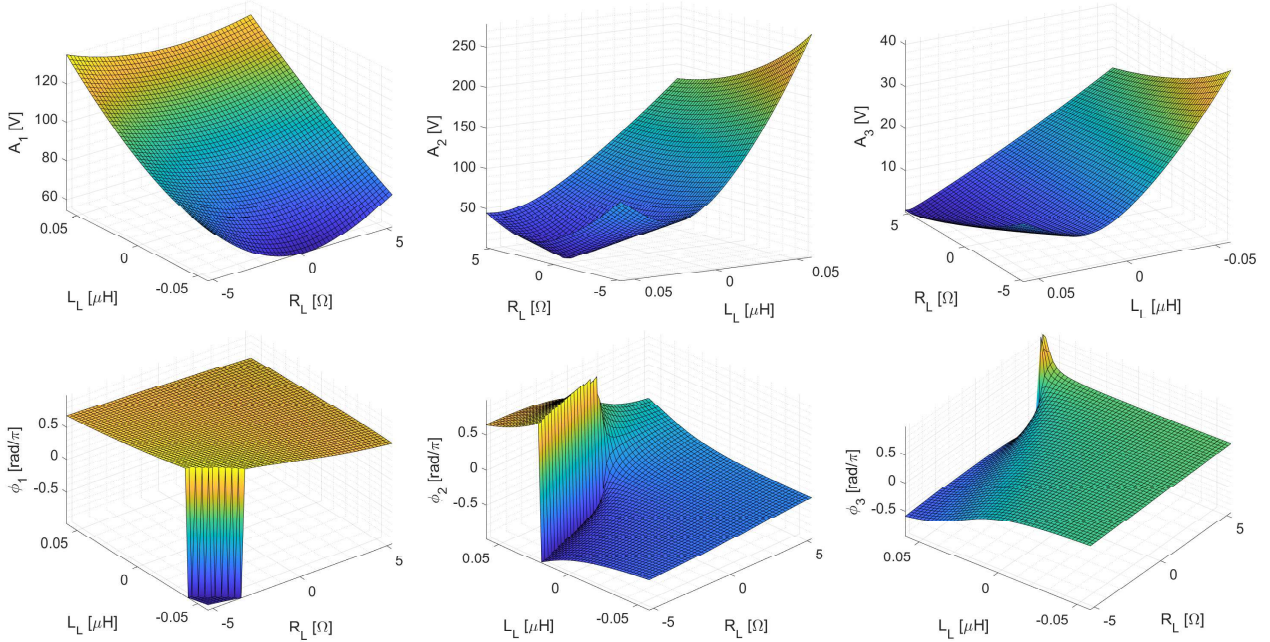


Figure 5.8: First three harmonic amplitudes (top) and phases (bottom) of the ϕ -branch capacitor voltage of the load-independent inverter example across a range of reflected impedance. The phase discontinuity results from the range being defined from $-\pi$ to π .

ing reliable and accurate outcomes. Figure 5.7 proves that there can be a formulation of a high order function with one-to-one relation between the drain voltage and the load.

On the other hand, the study in [112] states that the amplitude of the second harmonic has a linear relationship with the phase of the reflected load and is independent of the real load. This observation cannot be confirmed from Figure 5.8, since the amplitude surface plot of none of the harmonics is monotonic over the reflected reactance range and the value of the resistance does affect its behaviour, too. In addition, [112] shows that the input current is only dependent on the real value of the reflected load. Based on the analysis in [26] as well as (2.54), the above statement does not agree with theory, since the input resistance of the infinite Class E type inverter is a function of its DC to AC gain, which heavily depends on the residual reactance of the output branch. The dependence of the input current (i.e. input power) on reflected reactance is also clear in Figure 5.6. So the estimator in [112] can be reliable only when the IPT system is subject to low values of reflected reactance.

Both the drain voltage and the ϕ -branch capacitor voltage are very convenient to measure since a simple capacitor divider can be connected in series with the main capacitor to scale down the amplitude. By comparing the harmonics amplitudes of v_{DS} and v_{C_ϕ} in Figure 5.7 and Figure 5.8, the ϕ -branch capacitor voltage expresses the same behaviour over a greater range, so it would provide more accurate measurements and be more sensitive to changes.

Another interesting observation about the behaviour of the ϕ -branch capacitor voltage is showcased in Figure 5.9. These waveforms are from the Class EF₂ example developed in chapter 2, and there are four distinct time points during the period where v_{C_ϕ} does not change with changes in reflected resistance, as long as there is no reflected reactance present. The value of v_{C_ϕ} across the entire range of the reflected impedance is shown in Figure 5.10, where the above described behaviour is confirmed.

We have already proved in chapter 2 that simulations can be extremely accurate for predicting experimental waveforms in the Class E type inverter. A carefully developed simulation model can be the core of a look-up table or a fitting curve used to predict the reflected impedance based on implicit waveform measurements on the board. The simulation data can combine specific time domain properties, such as the one shown in Figure 5.9, along with frequency domain observations, to provide the best possible estimator and eliminate errors. The adjustment of the parameters can be either with a fixed increment until the operating conditions are satisfied,

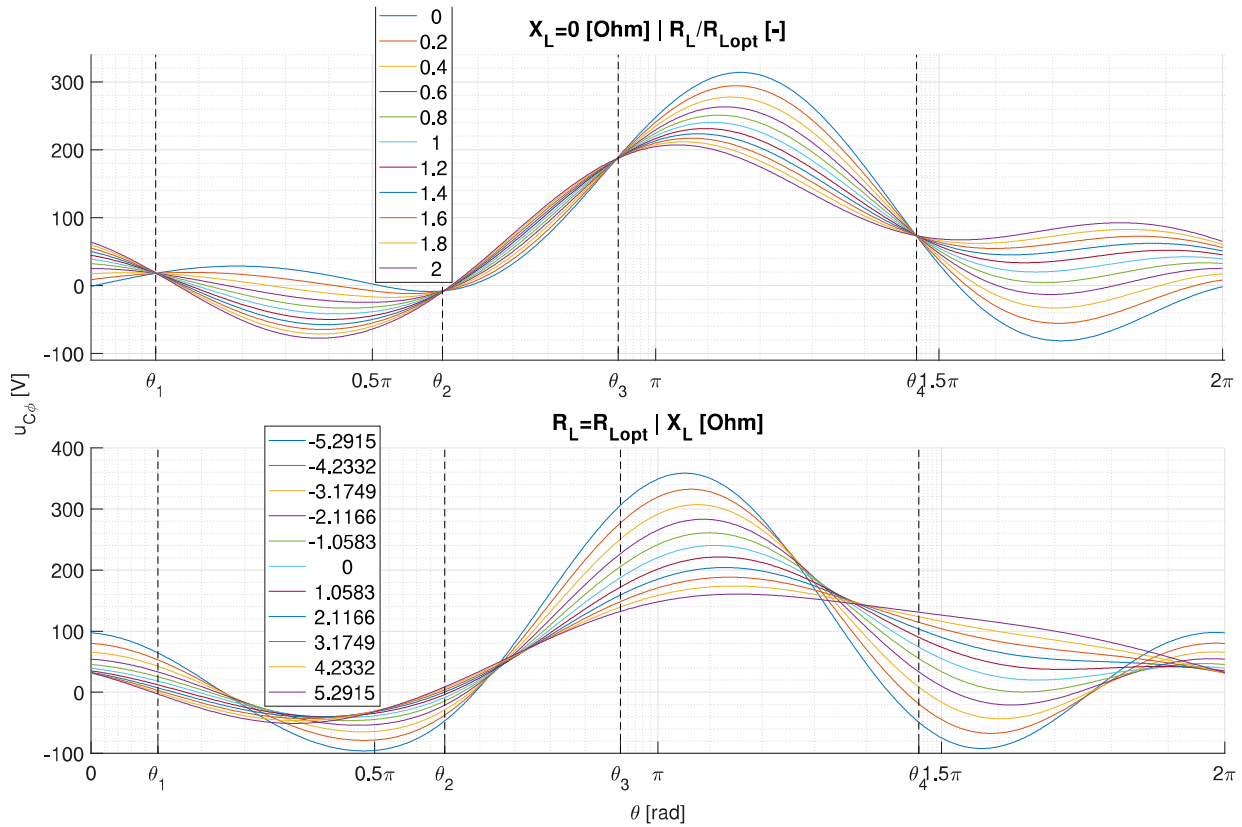


Figure 5.9: Voltage across the ϕ -branch of the Class EF₂ inverter example in chapter 2. The top waveforms are at various reflected resistance values with zero reflected reactance, and the bottom ones are at various reflected reactance values with the ideal load resistance.

or a variable step dependent on the distance from optimal operation.

5.3 Control Scheme Concept

In the previous section, the limitations of the open-loop operation of the Class EF inverter have been demonstrated, and various possible ways of on-board measurements for load identification have been proposed. In this section we present examples from both simulations and experiments that prove the concept of the control scheme on Class E type resonant converters for output power regulation while maintaining high efficiency at various reflected impedance values.

The control variables in our examples are the duty cycle, the input voltage, and the switching frequency. The duty cycle has minimal effect on the output characteristics, especially for the case of the Class EF topology. Changing the duty cycle mainly affects the ZVS and ZVDS conditions, which translates to high drain efficiency. Primarily, hard switching must be avoided, but reverse conduction is also less efficient than normal on-state operation.

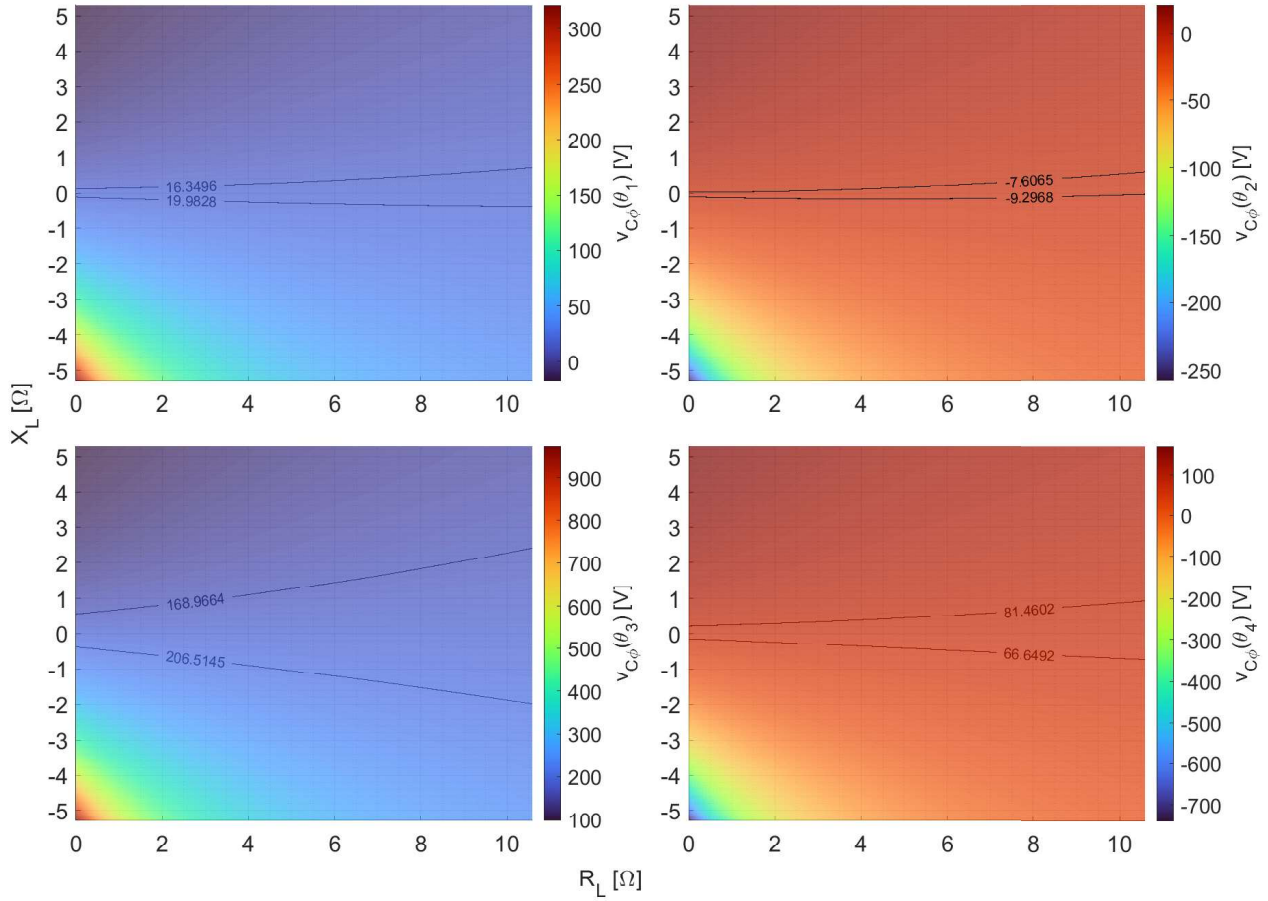


Figure 5.10: Voltage level at the critical time points in Figure 5.9 across the whole reflected impedance range. The area between the designated lines corresponds to 10 % positive and negative deviation from the exact value of the critical time point.

The supply voltage controls the output current, for a given load profile. However, depending on the ratio of output capacitance of the transistor (combined with the reverse external diode if present) to the remaining external shunt capacitance, the supply voltage can have a substantial effect on the soft-switching conditions. This effect becomes more prevalent as the switching frequency rises. Supply voltage lower than the nominal value leads to hard switching and supply voltage higher than nominal results in reverse conduction, when the load is ideal.

Altering the switching frequency effectively changes the residual reactance of the output branch. Secondly, it also affects the shunt and ϕ -branch (if applicable) impedance, which in turn modifies the soft-switching characteristics. Since the operation of the Class E type circuits is very sensitive to reactance changes in the output branch, frequency modulation can be used to control the output power of the inverter while remaining within the ISM band limits, which can be beneficial for HF IPT systems to remain within EMI regulations.

For all the above reasons, a control scheme involving the electrical signals present in a Class E type inverter has the potential to maintain power across a broad range of coupling while at the same time maintaining ZVS and close to ZVDS conditions, and maximising efficiency. A load-independent design is not necessary when such control scheme is applied, and a Class EF₂ design with soft current switching can be used instead, providing higher efficiency with lower EMI.

5.3.1 Simulation Examples

In the demonstration examples that follow the adjustment of each cycle of the control variables is carried out hierarchically, with the frequency being the first to be altered, the input voltage following and the duty cycle last. This choice of operation was based on the sensitivity of the inverter to each signal and its overall corresponding effect. The control cycles continue in this manner until all operating conditions are met (mainly output power and soft switching).

Input Voltage - Duty Cycle Control

In this example we use the Class EF₂ inverter design used in chapter 2. The resistive reflected load varies from critically low coupling (33 % of optimal load) to fully loaded and the reactive part ranged from zero to 10 % of the primary coil reactance in the form of capacitive loading. In this specific case we only adjust the input voltage and the duty cycle of the transistor, as there are applications where the switching frequency is fixed. We modulate the input power and while maintaining ZVS.

The drain voltage waveform as well as the input power level at various reflected impedance values across the range for the Class EF₂, before and after the adjustment, are shown in Figure 5.11 and Figure 5.12, respectively. The change in the duty cycle after the adjustment can be seen from the shift of the turn-off point in Figure 5.11. The change of the input voltage is directly connected to the peak of the drain voltage, as its DC component is set by the supply.

Reverse conduction in our study can reach up to almost 20 % of the period, as shown in Figure 5.11, which would be detrimental to the the drain efficiency as the transistor operates with a higher ON resistance for a quite substantial amount of time. In addition, there are some

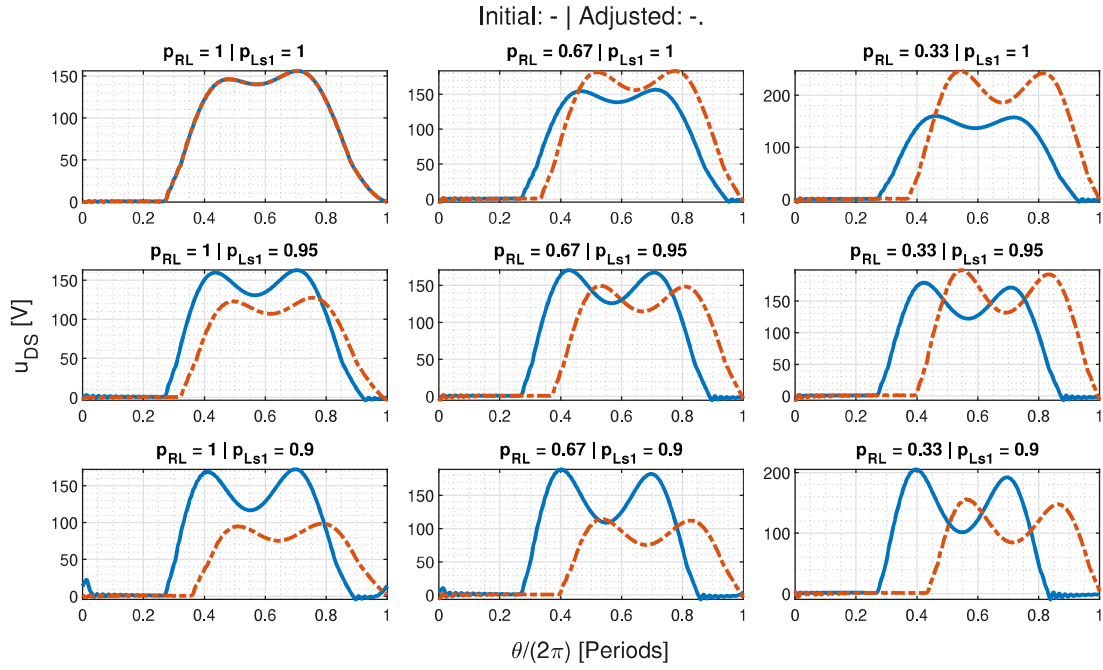


Figure 5.11: Drain voltage waveforms of the Class EF₂ inverter before and after the input voltage and duty cycle adjustment across a range of reflected impedance values. The p parameters represent the fraction of the corresponding reflected load compared to the nominal value.

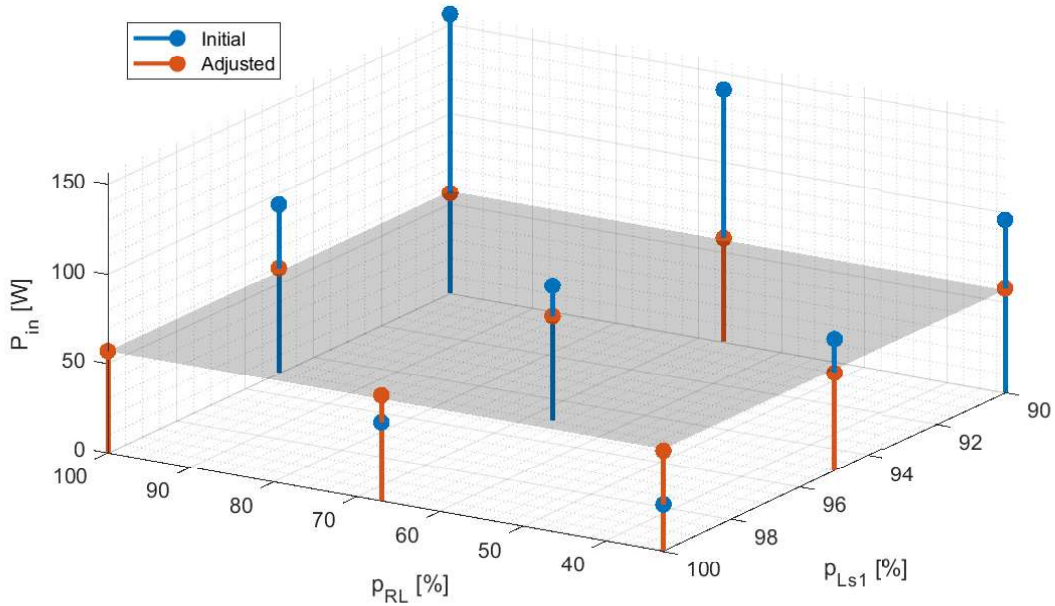


Figure 5.12: Input power of the Class EF₂ inverter before and after the input voltage and duty cycle adjustment across a range of reflected impedance values. The grey plane represent the nominal power level operation.

cases of hard switching. The input power in Figure 5.12 can swing from half to over three times the expected value, if left unregulated. In all of the instances in Figure 5.11 and Figure 5.12, the adaptation of the input voltage and duty cycle control leads to ZVS and operation at nominal

power.

Isolated Power Supply

Here we demonstrate the operation of the full control scheme (V_{in} , D , f_S) in an isolated power supply. The galvanic isolation is provided by two coupled air core coils in close proximity, as for example in the case of a PCB core-less transformer [138, 10]. The primary side is driven with an Class EF inverter and the rectifier at the secondary is a full-bridge current driven Class D. The rectified mains, after the input EMI filtering, is stepped down by a buck converter, which can also operate as a PFC stage [167], in a system block configuration as shown in Figure 1.4. The output DC voltage of the charger is regulated from the primary side, and as a result no final voltage regulation power stage is required.

The circuit diagram of a full-bridge current driven rectifier along with the secondary coil and load is shown in Figure 5.13. It is designed to deliver 100 V at 180 W at nominal operation, according to the equations in [25], and the value of the series resonant capacitance was tuned to absorb the parasitic reactance caused by the C3D06060A Schottky diodes from Wolfspeed. The Class D topology was chosen for this application because of its simplicity and high power density, since no inductors are involved in the design. The high operating frequency (13.56 MHz) also helps keeping the size of the charger small.

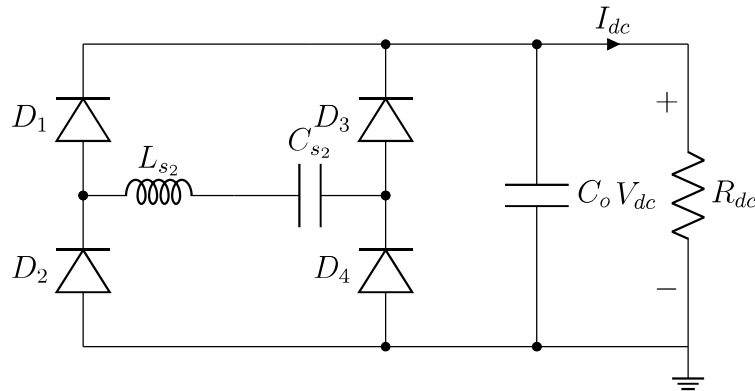


Figure 5.13: Full-bridge Class D current driver rectifier at the Rx side of an IPT system.

The next step is to design the IPT link along with the inverter. A primary coil of 1 μH was chosen to keep the loaded quality factor of the output branch of the inverter reasonably high. The secondary coil was chosen at a quarter of the primary inductance, to reduce the reflected load while also minimise the size on the PCB. The primary driver is a Class EF₂

single ended inverter, to achieve the highest possible input voltage at the minimal power level. This reduces the range required for the buck converter before the inverter, which simplifies the overall operation and feedback control of the DC/DC converter. The component values of the HF IPT part of the power supply unit example are given in Table 5.2 and the switching voltages and link current waveforms are shown in Figure 5.14. The current on the IPT link are no longer sinusoidal due to the high loaded primary Q factor. This however is not an issue in this particular application, since the whole charger is going to be shielded. Also, it must be mentioned that such non-sinusoidal output current inverter designs are possible because of the tuning method proposed in chapter 2.

Table 5.2: Component values of the HF IPT part of the charger example.

Parameter	Value	Unit
V_{in}	234	V
f_S	13.56	MHz
D	24.8	%
L_{rfc}	72	μH
C_p	39.4	pF
L_ϕ	910	nH
C_ϕ	38	pF
C_{s1}	380	pF
V_{dd}	5	V
G	LMG1020	—
Q	GS66504B	—
R_g^{low}	1	Ω
R_g^{high}	0	Ω
L_{s1}	1	μH
L_{s2}	250	nH
k	70	%
C_{s2}	496	pF
D_r	C3D06060A	—
R_L	62	Ω

The results of the mixed signal simulation in Cadence of the charger across a range of output loads is shown in Figure 5.15. The buck converter can run at a much lower frequency compared to the IPT inverter. This property, combined with the 50Hz input mains signal and DC output severely slows down the simulation speed. For this reason, the values of the stabilising capacitors wherever necessary have been reduced, hence the relatively large ripple of the DC signals in Figure 5.15. The load varies from nominal (maximum power) to practically open and the system manages to keep the output voltage stable, while maintaining soft switching.

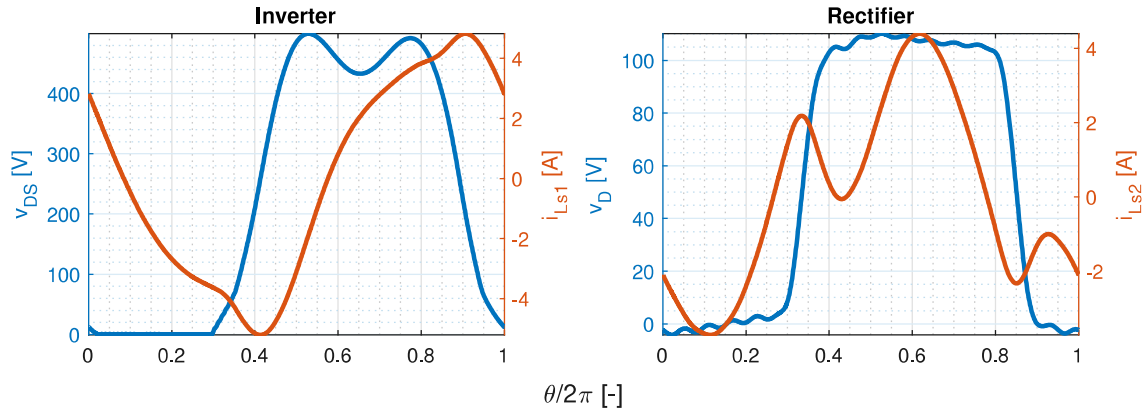


Figure 5.14: Waveforms at nominal load of the drain voltage, primary coil current, secondary coil current and voltage cross a diode of the rectifier in the power supply simulation.

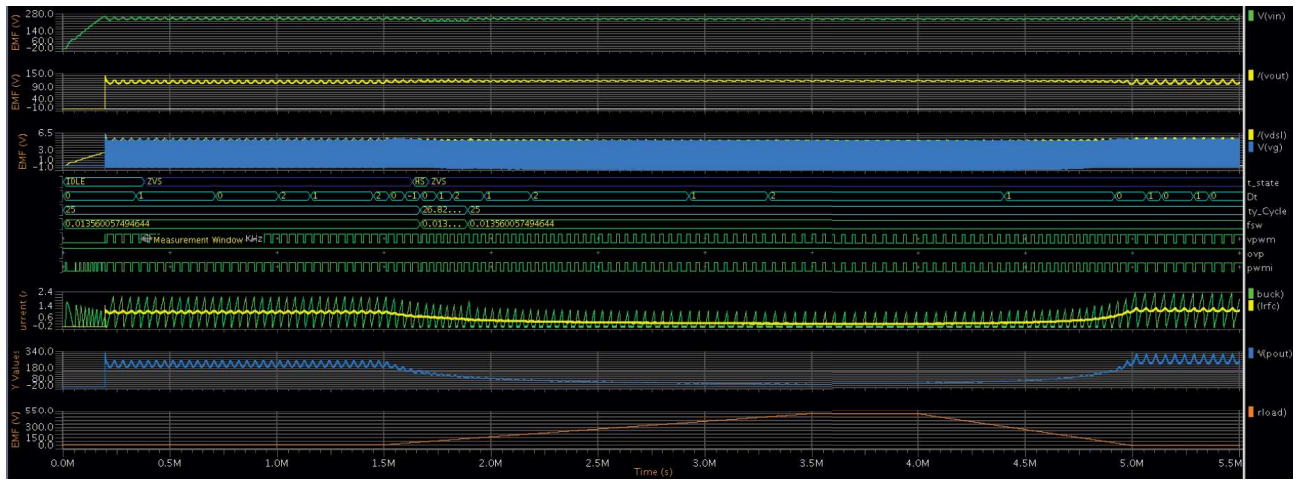


Figure 5.15: Mixed signal simulation of the isolated air-core power supply. The top waveform is the input voltage to the inverter, the yellow waveform underneath is the output voltage of the rectifier, the blue and yellow waveforms at the third row from the top are the gate and drain voltages respectively. The top state signal is the switching condition, the next underneath is the relaxation stage of the switching, then is the inverter duty cycle, and last is the inverter switching frequency. The PWM signals are driving the buck transistor and underneath are the buck inductor current in green and choke current on the inverter in yellow. The blue signal second to last at the bottom is the output power, and at the bottom is the resistance of the load.

The points where the algorithm changes the inverter frequency and duty cycle as well as the buck converter duty cycle can be spotted by the changes in the corresponding signals. In this simulation example the output voltage is fed back to the buck converter in the form of a PWM signal that regulates its duty cycle. The feedback from the output to input can be performed through a high speed optocoupler, like the TLP2767 from Toshiba, to retain complete galvanic isolation. A note for the feedback loop is that in reality the load changes are much slower compared to any switching frequency on the charger, which absorbs the effects of propagation

delays in the feedback circuitry.

The switching condition of the inverter is determined by comparing its duty cycle with the drain voltage. Since there is an inherent time delay between the gate signal and the drain waveform, due to the propagation delay of the gate driver and the switching delays of the transistor at this frequency, we transform the information of the duty cycles into DC voltage levels, before carrying out the comparison. The circuit diagram of the above analog comparison method is shown in Figure 5.16. The comparator on the top left acts as a buffer for the gate signal and the bottom one extracts the actual turn-on time of the transistor, including potential reverse conduction. Hard switching is also detected because of the non trivial transition time in this HF operation. The PWM outputs of the two comparators are filtered and passed to a subtractor, to get the switching information in DC. The values of the potential dividers are calibrated to match the required voltage reference at optimal operation. The duty cycle and frequency are then produced by the AD9833 programmable waveform generator.

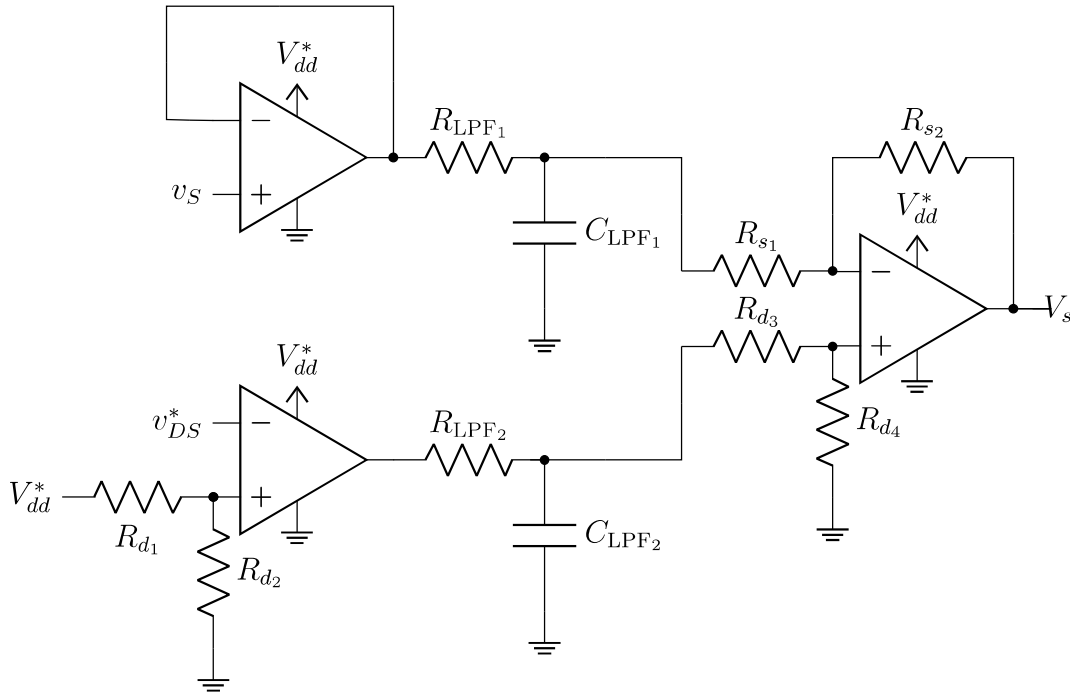


Figure 5.16: Analog measurement technique of the switching condition of a Class E type inverter. The supply voltage V_{dd}^* comes from the output of a linear regulator to minimise noise. The instance of the drain voltage v_{DS}^* is measured across a capacitor divider in series with C_p , and v_S is the input signal to the gate driver. The output DC reference containing the information of the switching condition is the signal V_s . The comparators on the left are the LTC6752 and the subtractor on the right is based on the AD8067.

5.3.2 Experimental Verification

In this subsection we present experimental verification of the concept of two versions of power and efficiency control in an IPT DC/DC system for coupling factor variation. The first example modulates the input voltage and the second the switching frequency to maintain constant output power. The soft switching conditions in both instances are maintained through duty cycle adjustments. The two examples incorporate different inverter and rectifier topologies to demonstrate the robustness of the proposed control approach.

Input Voltage - Duty Cycle Control

In this setup we use the Class EF_2 inverter design discussed in chapter 2 as the primary coil driver and a hybrid push-pull Class E rectifier, shown in Figure 5.17, according to the design guidelines in [21]. The nominal input voltage of the inverter is adjusted to 100 V in order to accommodate the equivalent load reflected by the rectifier, and the output power is set to 40 W to a 13.46Ω DC load at nominal coupling .

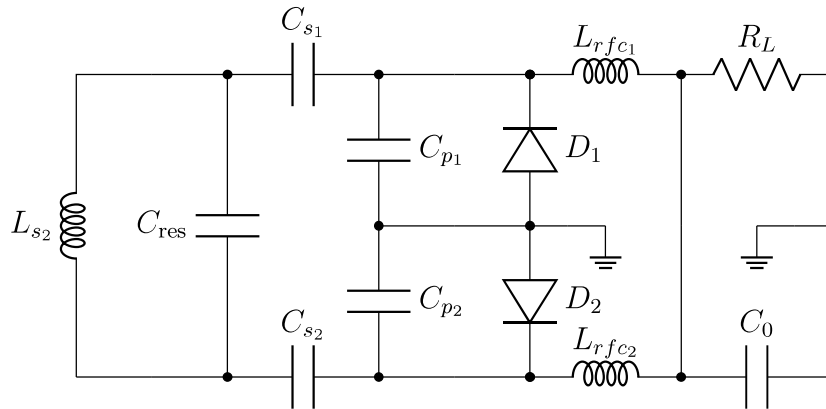


Figure 5.17: Circuit diagram of a hybrid Class E rectifier. The diode model used is the C3D10065 from Cree.

A photo of the DC/DC IPT experimental bench setup is shown in Figure 5.18 and the corresponding waveforms at nominal operation are displayed in Figure 5.19. There is substantial instability in the operation of the rectifier, based on the behaviour of the voltage across the diode, which is primarily caused because of mismatch between the two custom cored output inductors, since the hybrid Class E design uses finite chokes. However, this effect does not propagate neither to the operation of the inverter, nor to the output load. The inverter is operating at both ZVS and ZVDS and the output voltage on the load is stable.

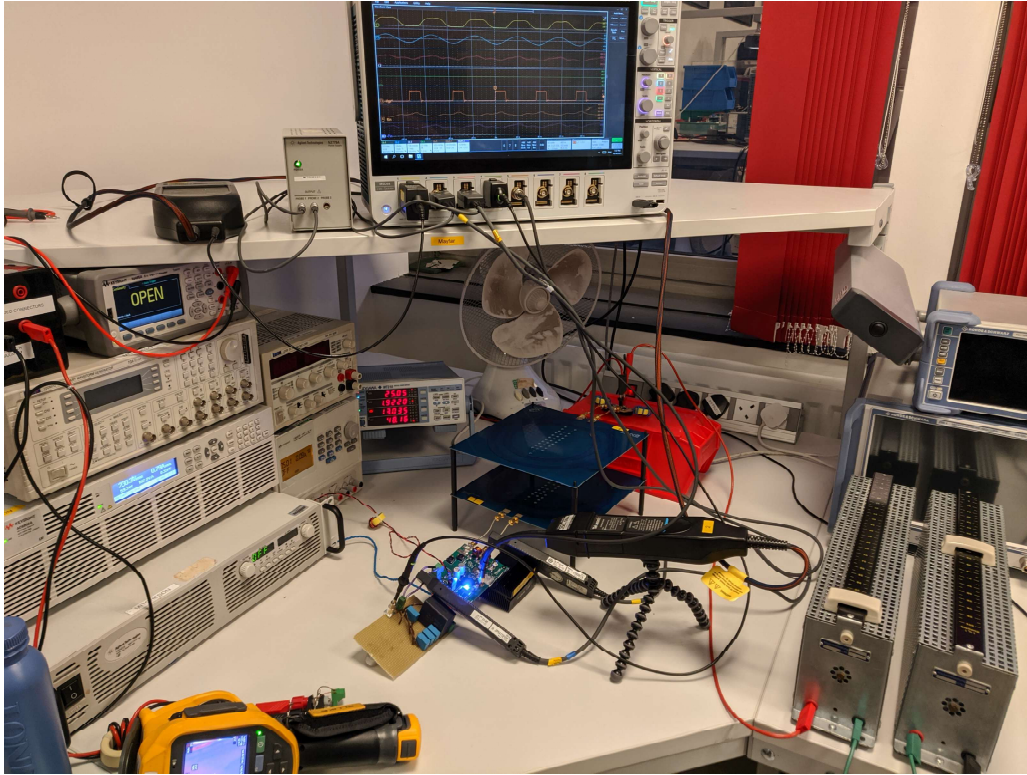


Figure 5.18: Experimental setup of the IPT DC/DC system for demonstration of the inverter input voltage and duty cycle control. The two dark blue PCB's are the coupled coils, the board at the front is the inverter running from mains (left) through a capacitor divider and a rectifier (strip-board at front), the board at the back is the rectifier, and the load consists of the rheostats at the right.

At nominal conditions, the two coils have a gap of 8.4 cm and no misalignment, and the most extreme separation at our example is at 10.1 cm separation and 3.5 cm misalignment. The two instances of coil placements are shown in Figure 5.20. If the inverter is left to operate passively, the case of extreme misalignment causes a 45.6% drop in output power for the same DC load and the overall efficiency drops by 9% due to primarily decrease in link efficiency but also suboptimal drain switching conditions.

The measurements before and after the input voltage and duty cycle adjustment with the link and low coupling are shown in Figure 5.21. Without any adjustment on the inverter, the output voltage, and in turn the output power, on the load is below the required value and the transistor is reverse conducting, reducing overall efficiency. After the adjustment of the input voltage and duty cycle the output power as well as ZVS are restored.

The control variables (V_{in} , D) as well as the regulated quantities (P_{out} , η) at nominal operation and the extreme low case of coupling, are shown in Figure 5.22, both for the passive and active

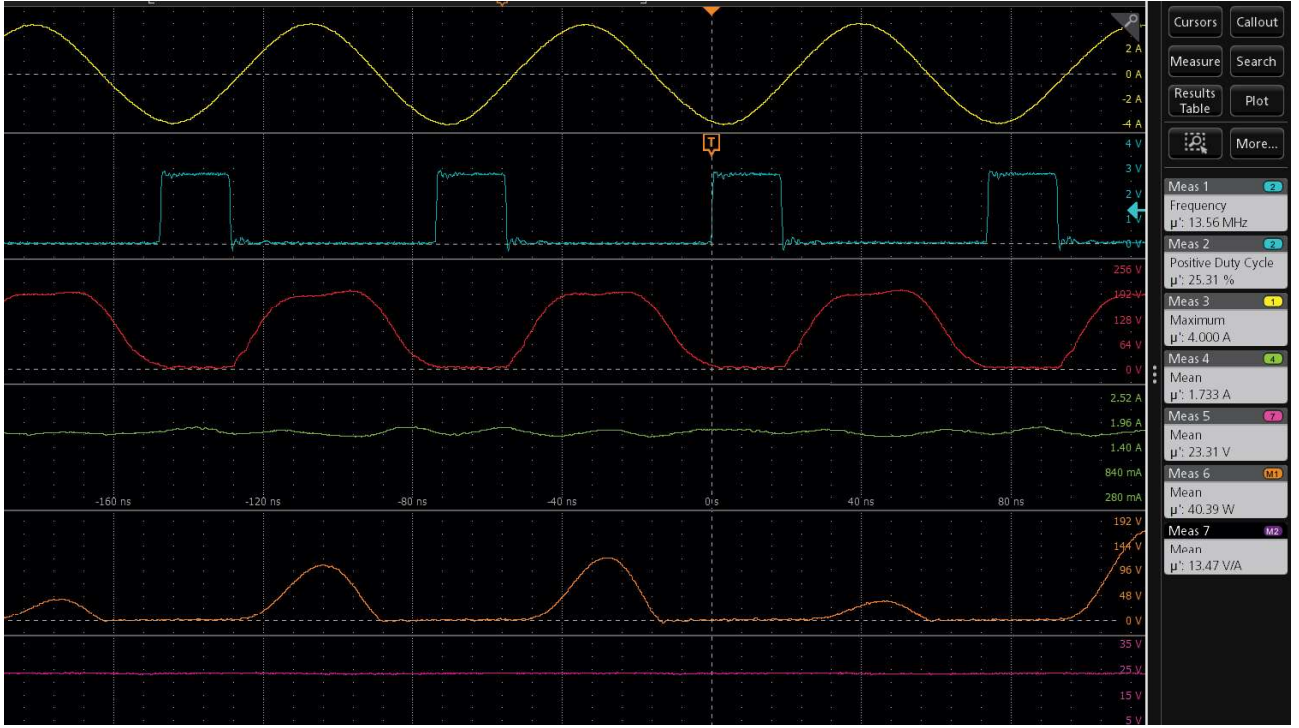
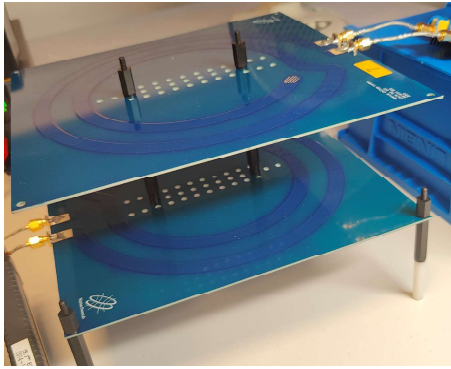
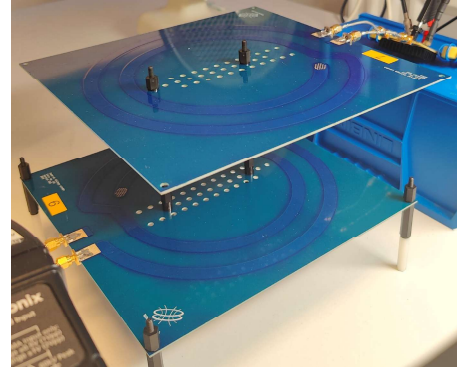


Figure 5.19: Measured waveforms at nominal operation of the setup in Figure 5.18. From top to bottom, in yellow is the primary coil current, in cyan is the switching signal, in red is the drain waveform, in green is the output current, in orange is the voltage across one of the diodes of the rectifier, and in purple is the output voltage. The two measurements of the "Math" functions are the output power ("Meas 6") and load resistance ("Meas 7").



(a) Nominal coupling



(b) Low coupling

Figure 5.20: Photos of the IPT link in Figure 5.18 at maximum coupling (left) and maximum misalignment (right). The low coupling configuration has 20.2 % larger gap distance compared to nominal value, and 33.3 % misalignment relative to the coil outer radius.

inverter operation. The seemingly low overall DC/DC efficiency increase (1 %) of the system after adjustment is because the majority of the losses are attributed to the link, as shown in Figure 2.26. Consequently, all of the efficiency increase is mainly directed to the inverter, and specifically the transistor. This 1 % system efficiency increase is translated to quite substantial gain in drain efficiency, which in turn results in meaningfully lower temperature on the device.

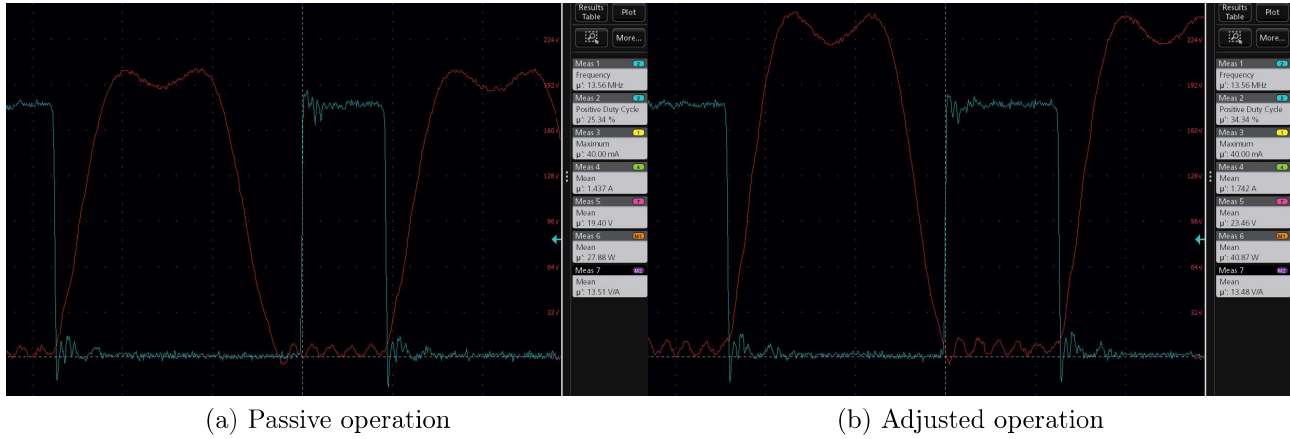


Figure 5.21: Gate signal (cyan) and drain voltage (red) of the inverter in Figure 5.18 at low coupling during open-loop, unadjusted operation (left), and readjusted operation (right). The measurement on the right of the screenshots are inline with the description in Figure 5.19.

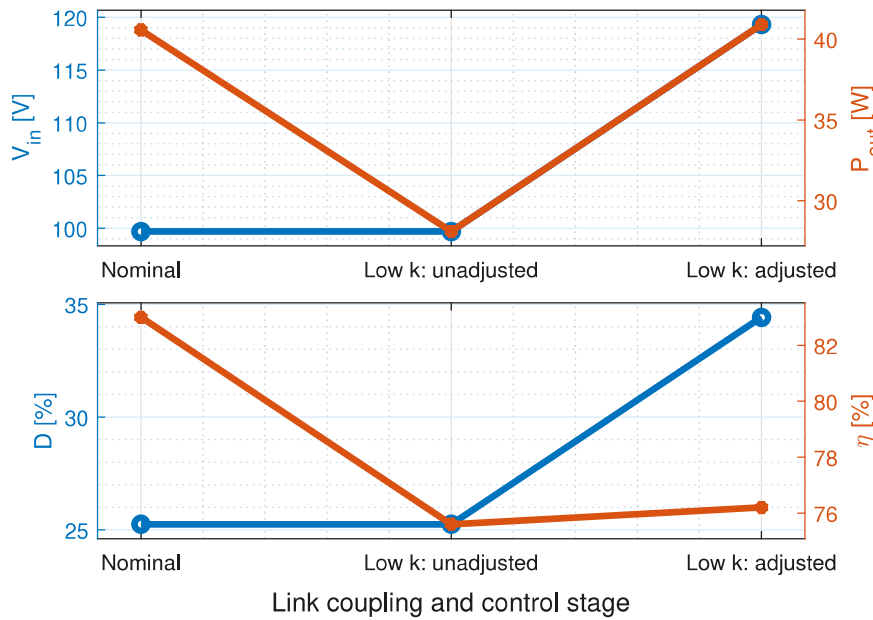


Figure 5.22: Progression of the control variables and regulated quantities of the IPT system in Figure 5.18 at nominal operation, low coupling without regulation, and low coupling with active control.

Switching Frequency - Duty Cycle Control

In this subsection we demonstrate an experimental example of a DC/DC IPT system with output voltage and efficiency regulation by controlling the duty cycle and switching frequency of the primary side. The primary driver is a push-pull Class E running at 6.78 MHz and the secondary is a series tuned Class D full-wave voltage doubler based on the Cockcroft-Walton voltage multiplier [20, 168, 169]. The circuit diagrams of the primary and secondary are shown

in Figure 5.23.

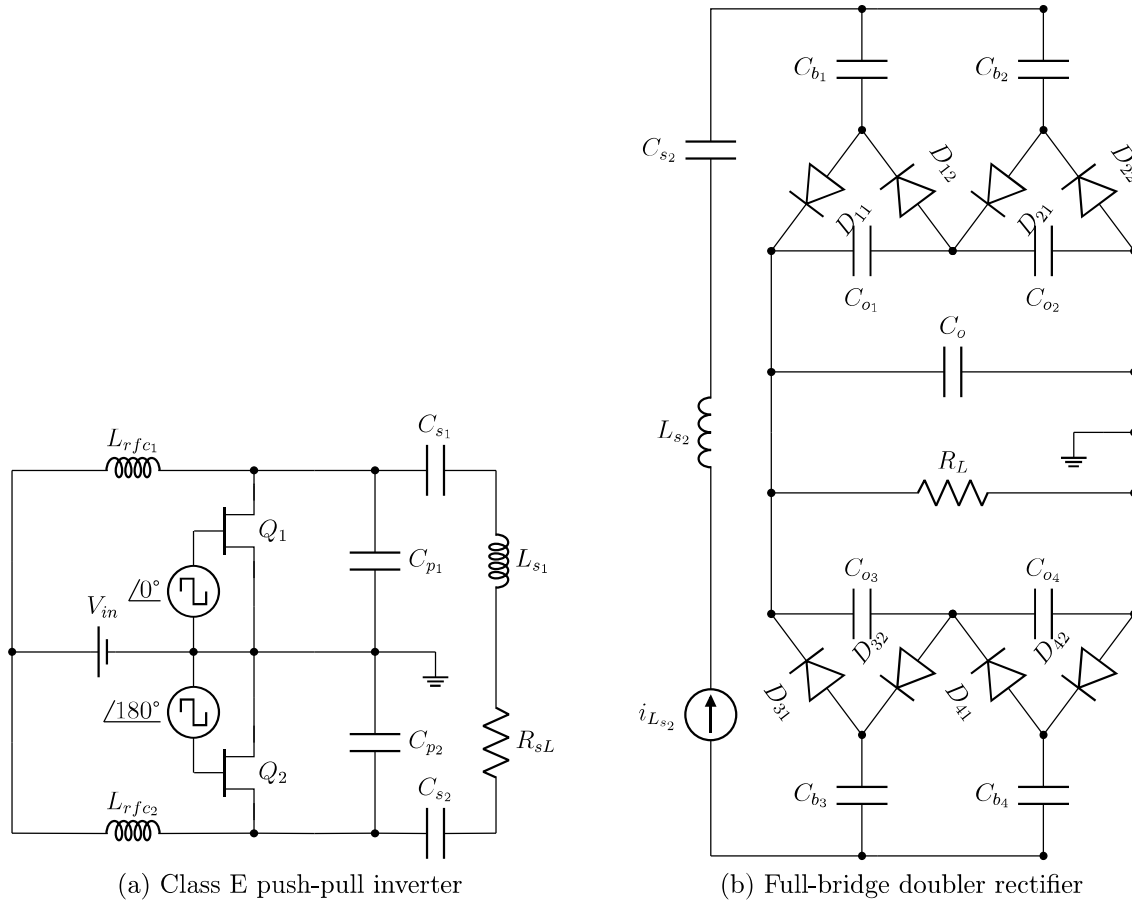


Figure 5.23: Circuit diagrams of the inverter and rectifier topologies used for the experimental test of the switching frequency and duty cycle control.

Photos of the experimental setup are shown in Figure 5.24. The gate and drain waveforms of the inverter at nominal load are shown at the oscilloscope on Figure 5.24a, where both ZVS and ZVDS conditions are met. The supply voltage is kept constant at 50 V, the duty cycle is 29%, and the nominal output voltage is 70 V at 80% DC/DC efficiency. The two gate signals of the inverter are produced through the Siglent SDG6022X waveform generator, as shown in Figure 5.24b.

After the tuning of the system, lateral misalignment was introduced to the link until the voltage drop on the fixed load became the equivalent of around 20% of power loss, where the efficiency dropped to 74.8% with the transistors at reverse conduction. Manually, decreasing the switching frequency to 6.61 MHz with a duty cycle of 38%, without changes in the supply voltage, restored ZVS conditions to the Tx driver and the output voltage to nominal value, while increasing the overall efficiency to 76.9%.

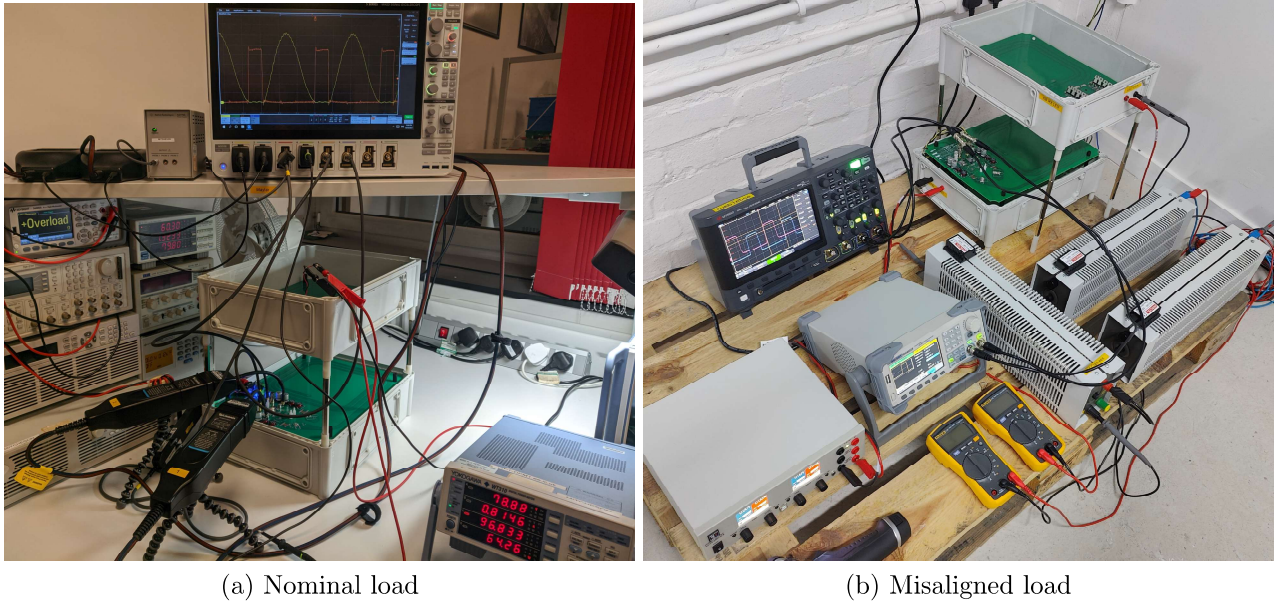


Figure 5.24: Photos of the experimental setup of the frequency and duty cycle control at nominal operation (left) and with link misalignment and power adjustment (right).

5.4 Summary

In this chapter we investigated the limitations of the Class E type inverters for IPT applications under various reflected impedance combinations. Specifically, a load-independent Class EF inverter was designed and the robustness of the soft switching conditions and output power were examined, the results of which strongly supported the benefits of an active primary control scheme. Various possible methods of load identification from the primary side with implicit measurements were proposed, both in time and frequency domain.

Then, four examples of control scheme applications were presented, two in simulation and two based on experiment. Output power regulation while maintaining soft switching was the goal, with the only degrees of freedom being the electrical signals on the inverter. It was successfully demonstrated that the operation of the inverter can be drastically improved with the presence of active adjustment compared to open-loop operation, with the main focus on the behaviour at the extremes of load and coupling values.

Chapter 6

Class Φ Gate Driver

6.1 Background

The optimal operation of all the inverter topologies discussed in section 1.4 relies on the prerequisite that the required gate signal profile is provided to the power transistors [28]. However, as switching frequency and output power increases, driving these power devices successfully becomes a nontrivial task, i.e. charging and discharging the input capacitance of a power transistor in short time intervals while maintaining high switching and conduction efficiency [170].

As with the inverters in section 1.4, the most typical used gate driver circuits are Class D type [171] and Class E type [172]. The Class D types are the most popular because of their simplicity [173] but come with the drawbacks of hard-switching and high-side driving, as explained in subsection 1.4.2, whereas Class E type have the drawback of complex tuning and low tolerances. In this chapter we propose a generalised design method for Class Φ resonant gate drivers. The Class Φ circuit, although more complicated than the Class E, offers more optimal gate voltage shaping properties and more degrees of freedom for tuning [174]. The Class E type gate drivers offer the advantage of only using a single low side transistor, reduced switching losses and soft waveform transitions.

The design method presented here is inspired by the work in [175] for Class Φ resonant gate drivers. A brief description of the design process for a Class Φ gate driver is also mentioned in

[10], without however providing any meaningful practical insights. There are several limitations in the analysis of [175], starting by the FO approximation used to the mathematical formulation of the circuit behaviour. As we have established in chapter 2, FO analysis generally results in poor accuracy in Class Φ converters. Our approach uses SS representation combined with full analytic expressions. Also, we provide solutions for any duty cycle, whereas [175] is limited to 50% only. Finally, the overall design algorithmic steps in [175] are not well defined and a bit abstract, which we also improve with our version.

6.2 Circuit Analysis

The circuit diagram of a Class Φ gate driver is shown in Figure 6.1. The difference between the Class Φ inverter in chapter 2 and the equivalent gate driver topology in this chapter is that the series resonant output branch of the inverter is missing in the gate driver circuit and the shunt capacitance of the gate driver corresponds to the capacitive load. The shunt capacitor simulates the equivalent input capacitance of the power device Q . The frequency of the input signal of the gate driver is the same as the switching frequency of the power device and the duty cycle of S is the reciprocal of that of Q .

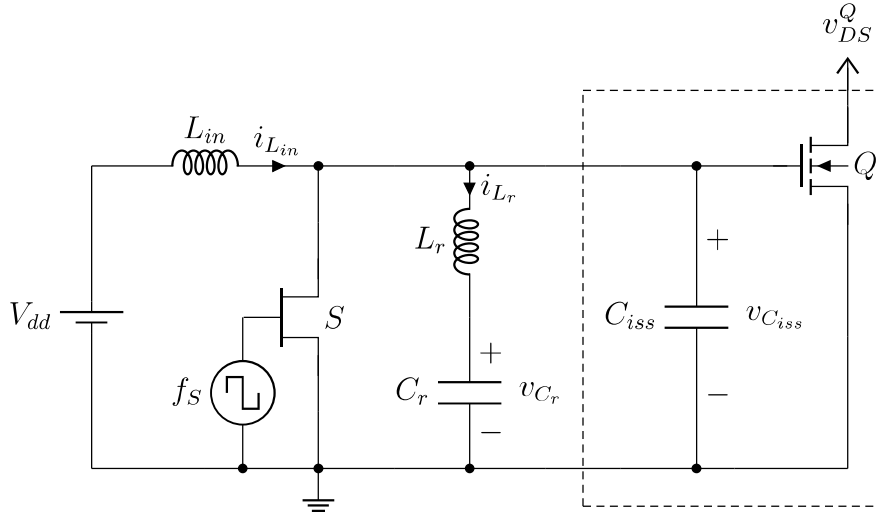


Figure 6.1: Circuit diagram of a Class Φ gate driver supplied by V_{dd} , driving the gate of the power device Q . The overall input capacitance of Q is modelled as C_{iss} , which represents the capacitive load of the gate driver.

The circuit analysis of Figure 6.1 is carried out by assuming that S is an ideal switch, i.e. $i_S = 0$ during $\theta_{\text{OFF}}^+ \leq \theta \leq \theta_{\text{ON}}^-$ and $v_{C_{iss}} = 0$ when $\theta_{\text{ON}+} \leq \theta \leq \theta_{\text{OFF}}^-$. This condition also means

that the discharge of C_{iss} is instantaneous, so zero current flows through the shunt capacitor during turn-on. We must clarify that in this chapter whenever switching timing or transistor signals are mentioned, they are referring to the switching device of the gate driver S and not the power transistor Q , unless explicitly stated otherwise. Consequently, to this convention, $\theta_{OFF}^+ = 0$, $\theta_{OFF}^- = 2\pi$, and $\theta_{ON} = 2\pi D_Q$, where D_Q is the duty cycle of Q . In addition the input capacitance of the power device Q is regarded ideal and constant, independent of the drain voltage. However, we solve the full state space equations for the analysis of the circuit, without any first order approximations applied.

6.2.1 State Equations during Turn-on

Applying KVL to the input branch during turn-on results in the differential equation

$$\omega L_{in} \frac{di_{Lin}^{ON}(\theta)}{d\theta} = V_{dd}, \quad (6.1)$$

whose normalised solution is

$$\frac{i_{Lin}^{ON}(\theta)}{\lambda} = \theta + A_1, \quad (6.2)$$

where A_1 is boundary dependent constant and

$$\lambda = \frac{V_{dd}}{\omega L_{in}}. \quad (6.3)$$

Combining KVL and KCL in the ϕ -branch during turn-on produces the ϕ -branch inductor current state equation

$$-\omega^2 L_r C_r \frac{d^2 i_{L_r}^{ON}(\theta)}{d\theta^2} = i_{L_r}^{ON}(\theta), \quad (6.4)$$

whose normalised solution is given by the relation

$$\frac{i_{L_r}^{ON}(\theta)}{\lambda} = A_2 \cos(\tau_r \theta) + A_3 \sin(\tau_r \theta), \quad (6.5)$$

where $A_{2,3}$ are boundary parameters and

$$\tau_r = \frac{1}{\omega \sqrt{L_r C_r}}. \quad (6.6)$$

Applying (6.5) to

$$v_{C_r}^{\text{ON}}(\theta) = -\omega L_r \frac{di_{L_r}^{\text{ON}}(\theta)}{d\theta}, \quad (6.7)$$

gives

$$\frac{v_{C_r}^{\text{ON}}(\theta)}{V_{dd}} = -k^2 \left(\frac{n}{\tau_r} \right)^2 \frac{d}{d\theta} \frac{i_{L_r}^{\text{ON}}(\theta)}{\lambda}, \quad (6.8)$$

where

$$k = \frac{C_{iss}}{C_r}, \quad (6.9)$$

$$n = \frac{1}{\omega \sqrt{L_{in} C_{iss}}}, \quad (6.10)$$

$$\frac{d}{d\theta} \frac{i_{L_r}^{\text{ON}}(\theta)}{\lambda} = \tau_r [A_3 \cos(\tau_r \theta) - A_2 \sin(\tau_r \theta)]. \quad (6.11)$$

6.2.2 State Equations during Turn-off

Solving the circuit in Figure 6.1 using KVL and KCL so that the Φ -branch inductor current is the only independent state variable during turn-off produces the following 4th differential equation:

$$\begin{aligned} V_{dd} = & \omega^3 L_{in} C_{iss} L_r \frac{d^3 i_{L_r}^{\text{OFF}}(\theta)}{d\theta^3} + \omega \left(L_{in} + L_r + \frac{L_{in} C_{iss}}{C_r} \right) \frac{di_{L_r}^{\text{OFF}}(\theta)}{d\theta} \\ & + \frac{1}{\omega C_r} \int_{\theta_{\text{OFF}}}^{\theta} i_{L_r}^{\text{OFF}}(\theta) d\theta + v_{C_r}(\theta_{\text{OFF}}). \end{aligned} \quad (6.12)$$

The Laplace transformation of i_{L_r} from (6.12) is a rational function whose denominator is a fourth degree polynomial

$$D(s) = as^4 + (b + ac)s^2 + c, \quad (6.13)$$

where

$$a = L_{in} C_{iss}, \quad (6.14)$$

$$b = \frac{L_{in}}{L_r} + 1, \quad (6.15)$$

$$c = \frac{1}{L_r C_r}. \quad (6.16)$$

The discriminant of (6.13) with respect to s^2 is

$$\Delta_{s^2} = (b + d)^2 - 4d, \quad (6.17)$$

where

$$d = ac. \quad (6.18)$$

By definition, $b > 1$ from (6.15) and $d > 0$ from (6.18), since the inductances and capacitances are always positive. As a result, (6.17) is always positive, with its minimum limit at $b = 1$, as shown in Figure 6.2. Consequently, (6.13) has four purely imaginary roots and thus the analytic expression of the inverse Laplace transform of (6.12) turns out to be

$$\frac{i_{L_r}^{\text{OFF}}(\theta)}{\lambda} = \sum_{i=1}^2 \left[\left(A_4 + \frac{A_5}{\tau_i^2} \right) \cos(\tau_i \theta) + \frac{1}{\tau_i} \left(\frac{A_6}{\tau_i} + A_7 \right) \sin(\tau_i \theta) \right], \quad (6.19)$$

where $A_{4,5,6,7}$ are again boundary dependent parameters and

$$\tau_1 = \sqrt{\frac{1}{2} \left[\tau_r^2 \left(\frac{1}{k} + 1 \right) + n^2 \right]} - \sqrt{\frac{1}{4} \left[\tau_r^2 \left(\frac{1}{k} + 1 \right) + n^2 \right]^2 - (n\tau_r)^2}, \quad (6.20)$$

$$\tau_2 = \frac{n\tau_r}{\tau_1}. \quad (6.21)$$

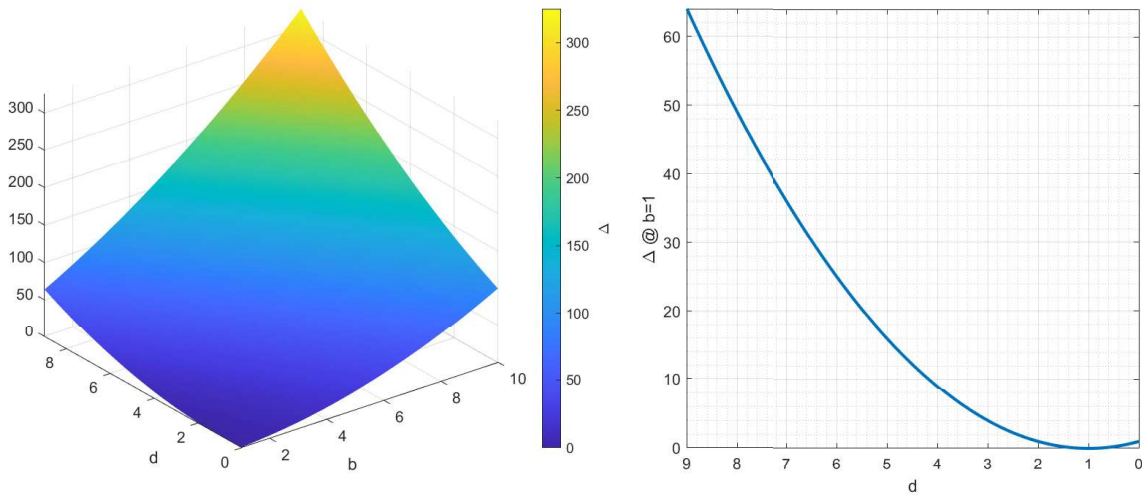


Figure 6.2: Surface plot of (6.17) (left) and line curve of (6.17) at $b = 1$ (right).

The rest of the normalised state variables equations can be directly derived from (6.19) and are

given below:

$$\frac{i_{L_{in}}^{\text{OFF}}(\theta)}{\lambda} = (1+k) \frac{i_{L_r}^{\text{OFF}}(\theta)}{\lambda} + \frac{k}{\tau_r^2} \frac{d^2 i_{L_r}^{\text{OFF}}(\theta)}{d\theta^2} \frac{1}{\lambda}, \quad (6.22)$$

$$\frac{v_{C_r}^{\text{OFF}}(\theta)}{V_{dd}} = 1 - \left[1 + k \left(1 + \frac{n^2}{\tau_r^2} \right) \right] \frac{d i_{L_R}^{\text{OFF}}(\theta)}{d\theta} \frac{1}{\lambda} - \frac{k}{\tau_r^2} \frac{d^3 i_{L_R}^{\text{OFF}}(\theta)}{d\theta^3} \frac{1}{\lambda}, \quad (6.23)$$

$$\frac{v_{C_{iss}}^{\text{OFF}}(\theta)}{V_{dd}} = 1 - (1+k) \frac{d i_{L_R}^{\text{OFF}}(\theta)}{d\theta} \frac{1}{\lambda} - \frac{k}{\tau_r^2} \frac{d^3 i_{L_R}^{\text{OFF}}(\theta)}{d\theta^3} \frac{1}{\lambda}, \quad (6.24)$$

where

$$\frac{d i_{L_R}^{\text{OFF}}(\theta)}{d\theta} \frac{1}{\lambda} = \sum_{i=1}^2 \left[\left(\frac{A_6}{\tau_i^2} + A_7 \right) \cos(\tau_i \theta) - \left(\tau_i A_4 + \frac{A_5}{\tau_i} \right) \sin(\tau_i \theta) \right], \quad (6.25)$$

$$\frac{d^2 i_{L_R}^{\text{OFF}}(\theta)}{d\theta^2} \frac{1}{\lambda} = - \sum_{i=1}^2 \left[\left(\tau_i^2 A_4 + A_5 \right) \cos(\tau_i \theta) + \left(\frac{A_6}{\tau_i} + \tau_i A_7 \right) \sin(\tau_i \theta) \right], \quad (6.26)$$

$$\frac{d^3 i_{L_R}^{\text{OFF}}(\theta)}{d\theta^3} \frac{1}{\lambda} = \sum_{i=1}^2 \left[\tau_i \left(\tau_i^2 A_4 + A_5 \right) \sin(\tau_i \theta) - \left(A_6 + \tau_i^2 A_7 \right) \cos(\tau_i \theta) \right]. \quad (6.27)$$

6.2.3 Boundary Conditions

After deriving the exact analytic expressions of the state variables of the resonant gate driver in Figure 6.1 in subsection 6.2.1 and subsection 6.2.2 during the two states of the transistor, we need to set the boundary continuation conditions for calculating the parameters $A_{1,2,\dots,7}$. These conditions rise from the fact that there cannot be abrupt changes and discontinuities in inductor currents and capacitor voltages during the transitions of the transistor conduction state. The only exception to this rule is the voltage across the input capacitance of the power device Q which acts as a shunt capacitor to the S of the gate driver. Since the transistor is modelled as an ideal short during turn-on, it can theoretically support infinite discharge current which corresponds in discontinuity in the voltage of C_{iss} , unless ZVS conditions are applied.

Setting the boundary continuation conditions of the state signals at turn-off and turn-on produces the following linear system of equation:

$$\mathbf{a} = \mathbf{B}^{-1} \mathbf{c}, \quad (6.28)$$

where

$$\mathbf{a} = \begin{bmatrix} A_1 & A_2 & A_3 & A_4 & A_5 & A_6 & A_7 \end{bmatrix}^T, \quad (6.29)$$

$$\mathbf{B} = \begin{bmatrix}
-1 & 0 & 0 \\
0 & 0 & 0 \\
0 & \cos(\tau_r \theta_{\text{OFF}}^-) & \sin(\tau_r \theta_{\text{OFF}}^-) \\
0 & \frac{kn^2}{\tau_r} \sin(\tau_r \theta_{\text{OFF}}^-) & -\frac{kn^2}{\tau_r} \cos(\tau_r \theta_{\text{OFF}}^-) \\
-1 & 0 & 0 \\
0 & \cos(\tau_r \theta_{\text{ON}}) & \sin(\tau_r \theta_{\text{ON}}) \\
0 & \frac{kn^2}{\tau_r} \sin(\tau_r \theta_{\text{ON}}) & -\frac{kn^2}{\tau_r} \cos(\tau_r \theta_{\text{ON}}) \\
2 + 2k - \frac{k}{\tau_r^2} \sum_{i=1}^2 \tau_i^2 & (1+k) \sum_{i=1}^2 \frac{1}{\tau_i^2} - \frac{2k}{\tau_r^2} & 0 \\
0 & 0 & -\sum_{i=1}^2 \frac{1}{\tau_i^2} \\
-2 & 0 & 0 \\
\sum_{i=1}^2 \left(1 + k - \frac{k\tau_i^2}{\tau_r^2}\right) \cos(\tau_i \theta_{\text{ON}}) & \sum_{i=1}^2 \left(\frac{1+k}{\tau_i^2} - \frac{k}{\tau_r^2}\right) \cos(\tau_i \theta_{\text{ON}}) & -\sum_{i=1}^2 \frac{1}{\tau_i^2} \cos(\tau_i \theta_{\text{ON}}) \\
-\sum_{i=1}^2 \cos(\tau_i \theta_{\text{ON}}) & -\sum_{i=1}^2 \frac{1}{\tau_i^2} \cos(\tau_i \theta_{\text{ON}}) & 0 \\
\frac{k}{\tau_r^2} \sum_{i=1}^2 \tau_i \left(\tau_i^2 - \tau_r^2 - \frac{\tau_r^2}{k} - n^2\right) \sin(\tau_i \theta_{\text{ON}}) & \frac{k}{\tau_r^2} \sum_{i=1}^2 \left(\tau_i - \frac{\frac{\tau_r^2}{k} + \tau_r^2 + n^2}{\tau_i}\right) \sin(\tau_i \theta_{\text{ON}}) & 0 \\
0 & 0 & 0 \\
(1+k) \sum_{i=1}^2 \frac{1}{\tau_i^2} - \frac{2k}{\tau_r^2} & 2 + 2k - \frac{k}{\tau_r^2} \sum_{i=1}^2 \tau_i^2 & 0 \\
0 & 0 & 0 \\
\left(1 + k + \frac{kn^2}{\tau_r^2}\right) \sum_{i=1}^2 \frac{1}{\tau_i^2} - \frac{2k}{\tau_r^2} & 2 \left(1 + k + \frac{kn^2}{\tau_r^2}\right) - \frac{k}{\tau_r^2} \sum_{i=1}^2 \tau_i^2 & 0 \\
\sum_{i=1}^2 \left(\frac{1+k}{\tau_i^3} - \frac{k}{\tau_r^2 \tau_i}\right) \sin(\tau_i \theta_{\text{ON}}) & \sum_{i=1}^2 \left(\frac{1+k}{\tau_i} - \frac{k\tau_i}{\tau_r^2}\right) \sin(\tau_i \theta_{\text{ON}}) & -\sum_{i=1}^2 \frac{1}{\tau_i} \sin(\tau_i \theta_{\text{ON}}) \\
-\sum_{i=1}^2 \frac{1}{\tau_i^3} \sin(\tau_i \theta_{\text{ON}}) & -\sum_{i=1}^2 \frac{1}{\tau_i} \sin(\tau_i \theta_{\text{ON}}) & 0 \\
\frac{k}{\tau_r^2} \sum_{i=1}^2 \left(\frac{\frac{\tau_r^2}{k} + \tau_r^2 + n^2}{\tau_i^2} - 1\right) \cos(\tau_i \theta_{\text{ON}}) & \frac{k}{\tau_r^2} \sum_{i=1}^2 \left(\frac{\tau_r^2}{k} + \tau_r^2 + n^2 - \tau_i^2\right) \cos(\tau_i \theta_{\text{ON}}) & 0
\end{bmatrix}, \quad (6.30)$$

$$\mathbf{c} = \begin{bmatrix} \theta_{\text{OFF}}^- & 1 & 0 & 1 & \theta_{\text{ON}} & 0 & 1 \end{bmatrix}^T. \quad (6.31)$$

6.3 Gate Driver Design

In order to create a design process we first need to map all the parameters of the state equations in section 6.2 to the inputs and constraint conditions of our method. Then, the component values of Figure 6.1 can be directly computed by the state equation parameters. This procedure is not straight forward, and the robustness of the design method relies heavily on the mathematical formulation of this inverse problem.

The main design parameters used as inputs to our tuning algorithm of the Class Φ gate driver are dictated by the requirements of the power stage circuit, namely the switching frequency (f_S), the duty cycle of Q (D_Q), and the effective equivalent input capacitance of Q (C_{iss}). The duty cycle of the gate driver is related to the duty cycle of the power transistor through the relation

$$D_S = 1 - D_Q. \quad (6.32)$$

Furthermore, we decide to use the supply voltage V_{dd} as a design input of choice, since it may be convenient to set it to a value that already exists on the PCB and thus minimise the number of different power supplies needed.

The switching frequency sets the value of ω and the duty cycle sets the turn-on angle. The supply voltage sets the power level, and turns all the normalised state equations to their absolute versions. From this point, the remaining unknowns of the circuit are the values of four passive energy storing components. Since the input capacitance of the power device is provided as an input parameter, we have to define three more constraint conditions in order to calculate the remaining components.

Given that the gate driver is a voltage driven Class E type inverter with shunt capacitance, an unavoidable and straight-forward design condition is ZVS, otherwise high efficiency operation will not be achieved. This condition is mathematically defined from (6.24) as follows:

$$\frac{V_{DS}^{\text{OFF}}}{V_{dd}} = (1 + k) \frac{d}{d\theta} \frac{i_{LR}^{\text{OFF}}(\theta)}{\lambda} \Big|_{\theta=\theta_{\text{ON}}} - \frac{k}{\tau_r^2} \frac{d^3}{d\theta^3} \frac{i_{LR}^{\text{OFF}}(\theta)}{\lambda} \Big|_{\theta=\theta_{\text{ON}}}, \quad (6.33)$$

where V_{DS}^{OFF} is the required value of the drain voltage at turn-on. For ZVS, V_{DS}^{OFF} should be set to zero, but our method allows for circuit designs at any value of $v_{C_{iss}}(\theta_{\text{ON}})$.

From (6.24) we can notice that the harmonic content of the gate voltage of the power transistor has two components, i.e. τ_1 and τ_2 , normalised to the switching frequency. From this observation, we decide to form the remaining two design conditions based on the frequency domain of the gate signal. As explained in [176], the gate signal best approximating a square wave for the circuit in Figure 6.1 is a Class Φ_2 gate driver that includes the first and third harmonic at zero phase, along with a DC component.

In Figure 6.3 we plot the normalised surface of τ_1 and τ_2 with respect to b and d , where we can observe that $\tau_2 > \tau_1$ for any combination of (b, d) . The same conclusion can be made by analysing (6.20) and then applying the conclusions to (6.21). Hence, in order to obtain a square gate voltage signal we need to set (6.20) to represent the first harmonic and (6.21) the third. However, our method still works for any combination of (τ_1, τ_2) .

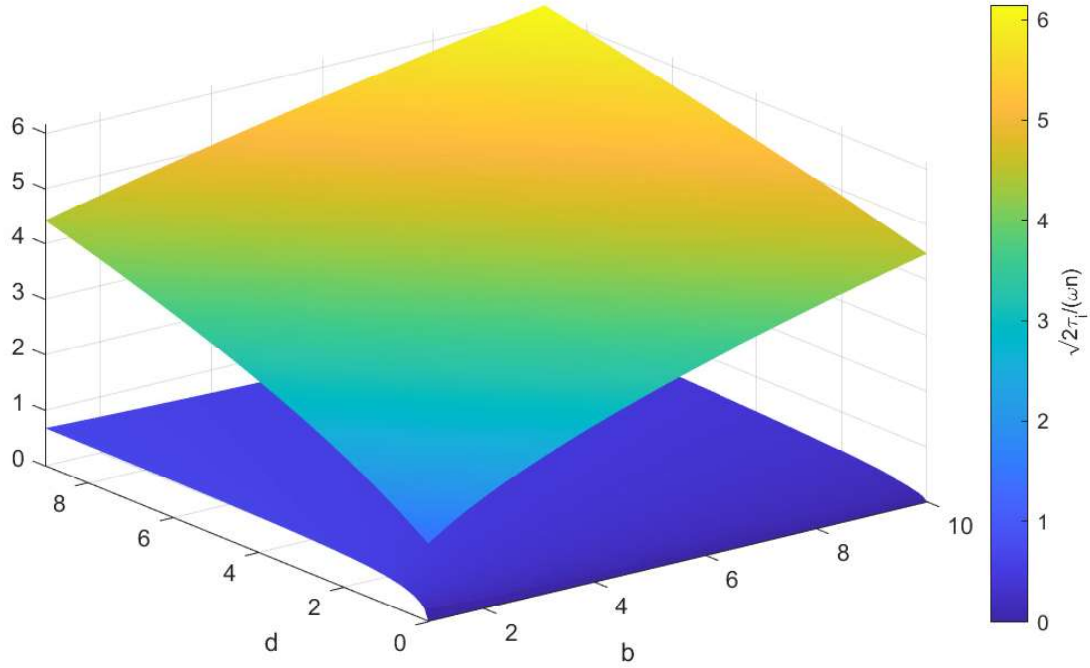


Figure 6.3: Surface plots of normalised (6.20) (bottom) and (6.21) (top) with respect to (6.15) and (6.18).

Since (6.13) is a quadratic equation with respect to s^2 and (6.13) is positive, there is a special relation for the sum and the product of its roots. The product relation is given by (6.21), and the sum is the following:

$$\tau_1^2 + \tau_2^2 = n^2 + \tau_r^2 \left(1 + \frac{1}{k}\right). \quad (6.34)$$

These two equations form the final two condition needed for solving the inverse problem of

designing a Class Φ gate driver.

As mentioned previously, the best approximation of a square voltage gate signal using a Class Φ gate driver is achieved with the ϕ -branch resonating at the second harmonic and ideally the remaining first and third harmonic contents of the output being in phase. However, in practice, this requirement may be too strict to produce a real circuit solution, and therefore we introduce relaxation parameters to the definitions of the harmonic content of the gate voltage. Mathematically, for a Class Φ_2 gate driver this condition is set by

$$\tau_1 = \frac{r_1}{2D_Q}, \quad (6.35)$$

$$\tau_2 = 3r_2\tau_1, \quad (6.36)$$

where $r_{1,2}$ are the relaxation parameters set as inputs to the design method.

6.4 Numerical Example

6.4.1 Power Stage

To demonstrate the Class Φ gate driver design method that we propose in this chapter, we use it to drive the gate of the C3M0032120J1 SiC MOSFET from Wolfspeed, which is a 1.2 kV, 68 A device with quite high input capacitance. The power transistor is part of a single ended 6 kW, 1 MHz Class EF inverter, which was designed using the algorithm proposed in chapter 2. The operating frequency is limited by the switching capabilities of the power transistor, which combined with the high gate charge of the power device would generally favour a Class D gate driver. An experimental demonstration of higher frequency operation using Class Φ_2 gate driver is demonstrated in [176].

The full circuit diagram of the single ended Class EF₂ inverter is shown in Figure 6.4 and the corresponding component values are given in Table 6.1. The design conditions of the power stage were such that the maximum power throughput is achieved, however we do not provide all the details of the inverter since it is merely used as a test bench to evaluate the performance of the gate driver. As explained, Q is a SiC transistor and needs to be connected to an anti-parallel diode, for safe reverse conducting operation. The diode of choice, based on the current

stresses is the 1.2 kV, 26 A C4D20120A SiC Schottky diode from Wolfspeed. The duty cycle is also defined by the power circuit design, which in our case is 30 % and G_Q is the gate driver of Q .

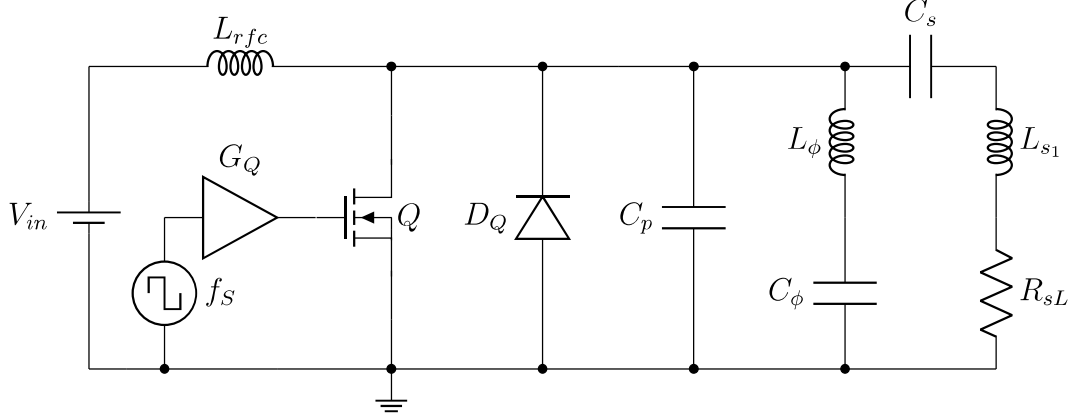


Figure 6.4: Circuit diagram of the Class EF inverter power stage used as the test bench for evaluating the performance of the gate drivers.

Table 6.1: Component values of the test bench in Figure 6.4.

Parameter	Value	Unit
V_{in}	468	V
f_S	1	MHz
D	30	%
L_{rfc}	100	μH
C_p	5.08	nF
L_ϕ	5.075	μH
C_ϕ	1.248	nF
C_s	8.074	nF
L_{s1}	5	μH
R_{sL}	7.5	Ω
Q	C3M0032120J1	—
D_Q	C4D20120A	—

The drain voltage and current waveforms of Q from both the Class Φ_2 and half bridge gate drivers are presented in Figure 6.5, simulated in LTspice. The Fourier contents of the waveforms in the top of Figure 6.5 are presented in Figure 6.6. The details of these two figures are further discussed in subsection 6.4.4.

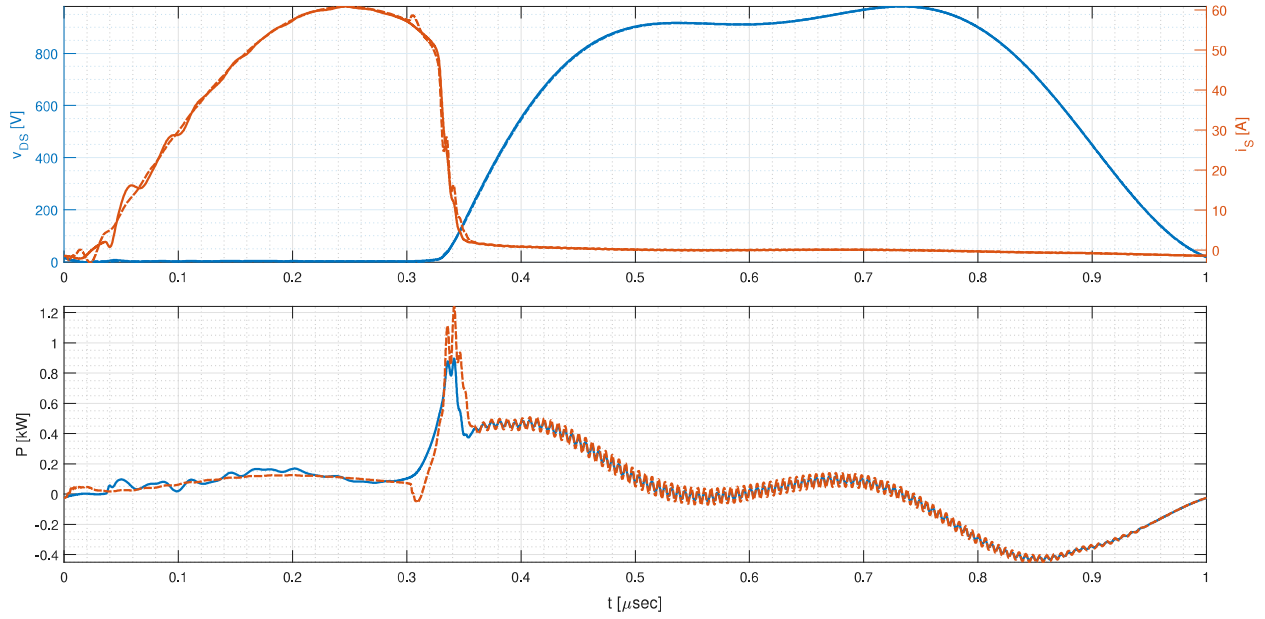


Figure 6.5: The top graph shows the waveforms of the drain voltage (blue) and drain current (orange) of the power device Q in Figure 6.4 for the Class Φ_2 (solid line) and Class D (dashed line) gate drivers. At the bottom, the total instantaneous power of the power transistor is displayed, in blue for the Class Φ_2 and orange for the and Class D gate driver.

6.4.2 Class Φ Gate Driver

As mentioned in subsection 6.3, the switching frequency and the duty cycle of the gate driver are predefined by the power stage requirements. We choose to use GaN transistors as the switching elements of the gate driver examples in this chapter, because of their high switching speeds and low conduction losses. The gate driver chip for the transistors of the gate driver circuits is the LMG1020, whose supply voltage limit is 5 V. We want a single supply source for the entirety of the Class Φ gate driver, hence $V_{dd} = 5$ V.

Although the datasheet of Q does provide a value for C_{iss} , it is only valid for the corresponding value of drain voltage stated. In order to compute a better approximation for the effective total load capacitance of Figure 6.1, without relying on complicated non-linear simulations, we need to accommodate for the Miller effect of both the C_{iss} of Q as well as the C_{oss} of S . According to [175], the effective overall shunt capacitance that should be used for designing the Class Φ gate driver is

$$C_{iss} = C_{iss}^Q + \frac{V_{DS}^Q}{V_{GS}^Q} C_{rss}^Q + C_{oss}^S \left(\frac{V_{DS}^S}{2} \right), \quad (6.37)$$

where the superscripts refer to the corresponding transistor and the values of the voltages are the maximum values of the corresponding waveforms. The first two terms of (6.37) simulate

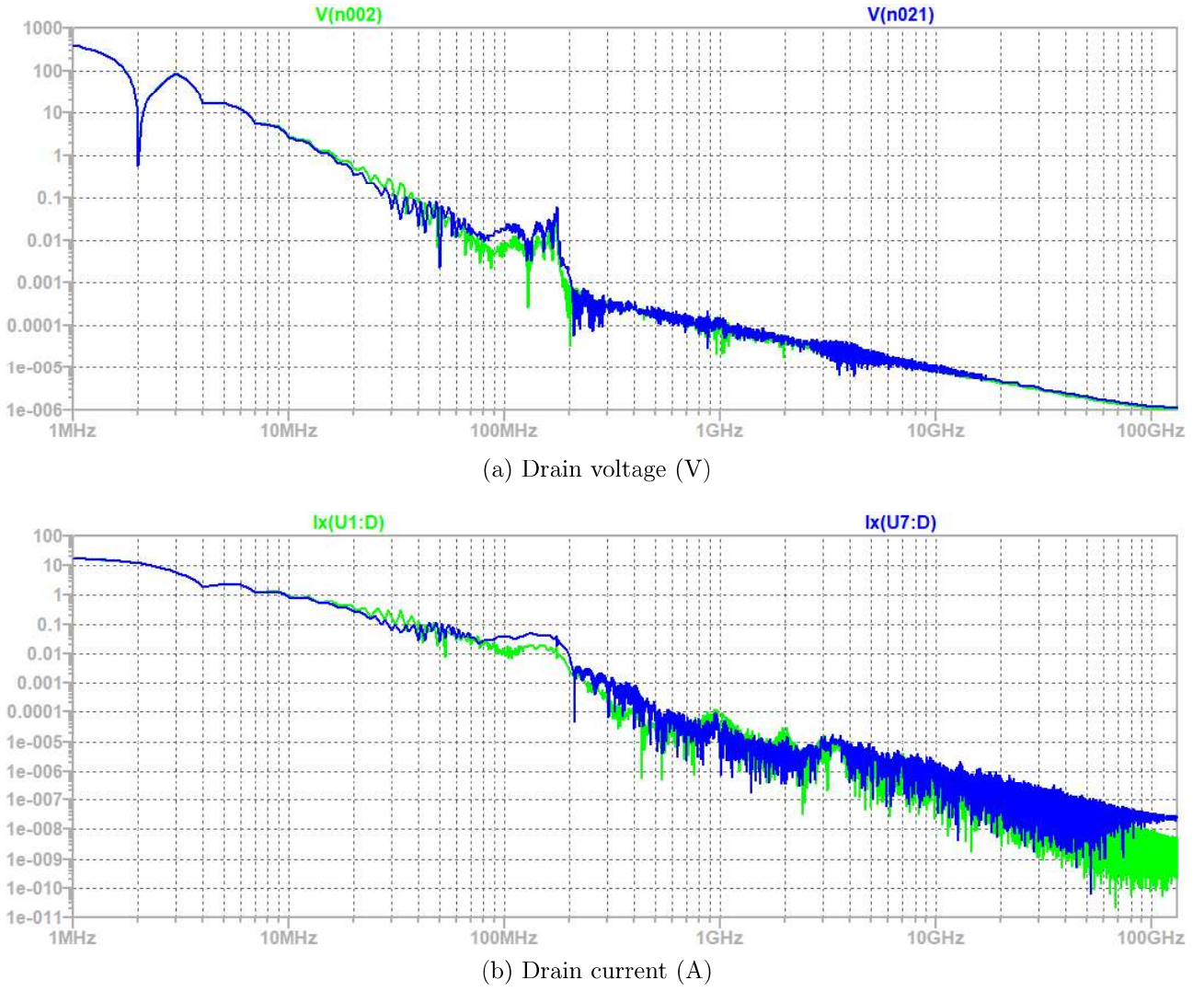
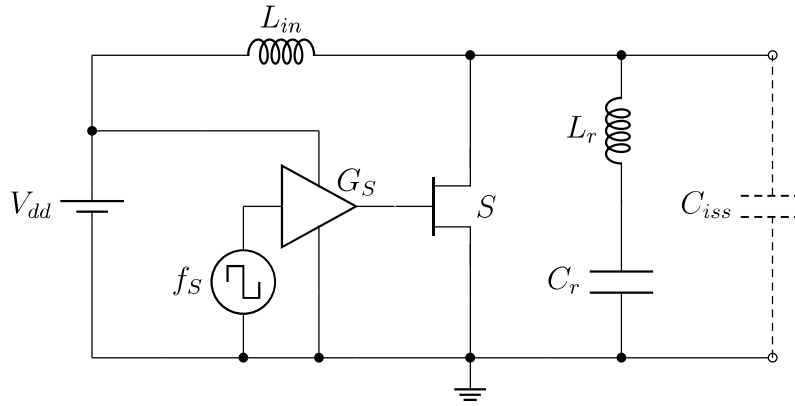


Figure 6.6: Fourier transform in [V] of the drain voltage (top) and drain current (bottom) of the waveforms in Figure 6.5. The Class Φ_2 gate driver is represented in green and the Class D in blue colour.

the Miller effects of the power transistor and the third term approximates the effective value of the output capacitance of S with the capacitance of C_{oss} at half the maximum of its drain voltage.

The solution of the system of design equations (6.21), (6.33), and (6.34) is calculated using the trust-region-dogleg algorithm described in [64, 65]. In order to achieve optimal conversion of the solving algorithm, we slightly increase the value of r_2 in (6.36) from that of the optimal Class Φ_2 operation. The full circuit diagram of the Class Φ_2 example is shown in Figure 6.7 and the corresponding component values are listed in Table 6.2.

The progression of value of the cost function of the design algorithm along the 14 iterations required for convergence is shown in Figure 6.8. The waveforms of the resulting circuit driving

Figure 6.7: Circuit diagram of the Class Φ_2 example.

a constant gate capacitance with an ideal switch S are shown in Figure 6.9. From the shape of $v_{C_{iss}}$ we can confirm that the ZVS condition, the optimum harmonic content, and the desired peak value have been achieved. The peak values of i_S lead to the choice of the GS66502B transistor in Table 6.2. Another important observation from the shape of the waveform of i_{L_r} in Figure 6.9 is that it deviates significantly from a pure 2nd harmonic, which showcases the limitations of the FO analysis used in [175, 176].

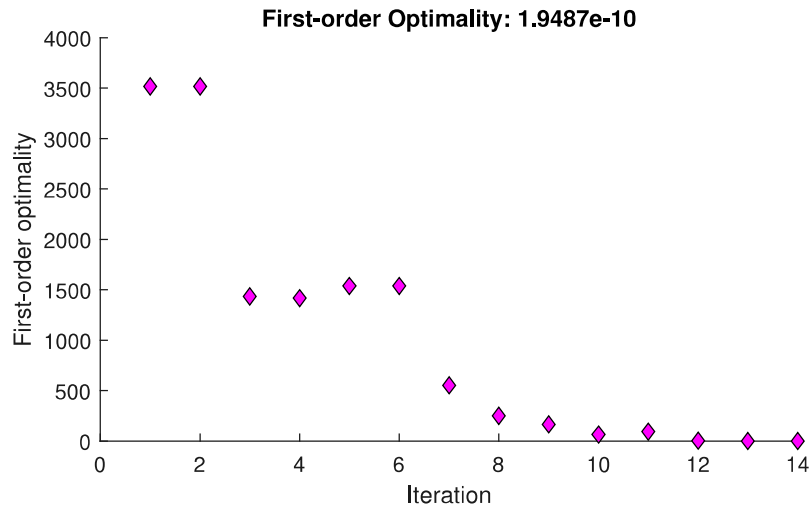


Figure 6.8: Convergence progression of the optimisation cost function with respect to algorithm iterations.

As mentioned in section 6.2, none of the non-linear parasitic effects of S and Q are included in the design calculations, making the waveforms in Figure 6.9 not exactly indicative of the real circuit operation. For this reason, we also run an LTspice simulation of the circuits in Figure 6.4 and Figure 6.7 combined, using the component values of Table 6.1 and Table 6.2 along with the full models of all the semiconductor devices and chips. The resulting gate waveforms of Q and drain waveforms of S are given in Figure 6.10.

Table 6.2: Inputs, outputs and component selection of the Class Φ_2 gate driver example in Figure 6.7.

	Quantity	Value	Unit
Inputs from power stage	f_S	1	MHz
	D_Q	30	%
	C_{iss}^Q	3.424	nF
	C_{rss}^Q	11	pF
	V_{DS}^Q	1	kV
	V_{GS}^Q	20	V
Inputs for gate driver	V_{dd}	5	V
	r_1	1	—
	r_2	1.3	—
	V_{DS}^{OFF}	0	V
	$C_{oss}^S (V_{DS}^S/2)$	110	pF
Design outputs	L_{in}	262	nH
	L_r	378	nH
	C_r	13.5	nF
	pL_{in}	−8	%
Component selection	S	GS66502B	—
	G_S	LMG1020	—

Several observations can be made by comparing the ideal waveforms of Figure 6.9 with the corresponding ones from the LTspice simulation in Figure 6.10. First of all, as noted in Table 6.2, a manual reduction of 8% to the value of L_{in} was performed to acquire the behaviour in Figure 6.10. In practice, by adjusting the value of L_{in} , we control the phase of the two harmonics in $v_{C_{iss}}$, and the goal is to achieve even peaks by minimising the phase difference of the harmonic content in the gate voltage.

Another point worth noting is that ZVS was not achieved in Figure 6.10. However, the hard switching occurs at very low voltage which results in very little discharge current in the device, which has minimum negative effect in the overall efficiency. The main source of losses on S occur from the ripple of the drain voltage during turn-on, which is an artifact of the relatively high R_{DS}^{ON} of GS66502B.

6.4.3 Half Bridge Gate Driver

In order to evaluate quantitatively the performance and the general characteristics of the Class Φ_2 gate driver example we design a typical half bridge gate driver for the same power

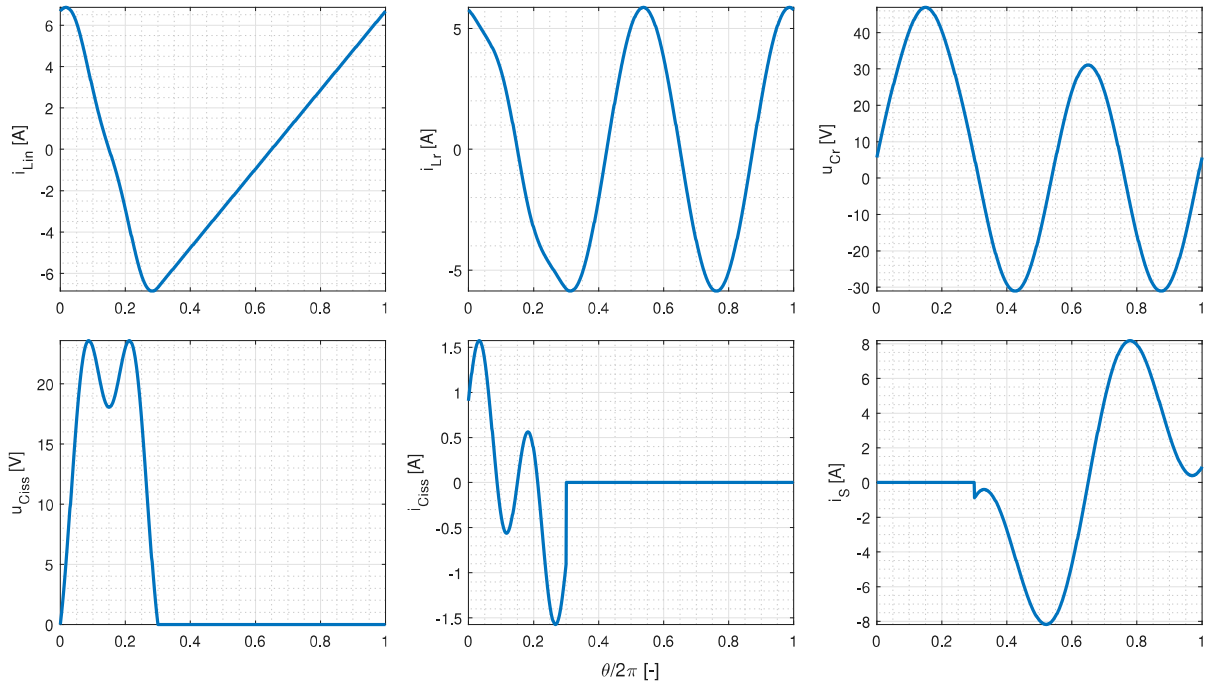


Figure 6.9: Waveforms of the Class Φ_2 example in Table 6.2 using an ideal transistor and load capacitance.

application for comparison. The circuit diagram of the Class D gate driver example is given in Figure 6.11 and the corresponding drain waveforms of the power device driven with this configuration are shown in Figure 6.5.

Based on the current stresses of the two switches in Figure 6.11, the transistor of choice is the GS66504B from GaN Systems. The gate driver for these is again the LMG1020 from TI. Since the GS66504B is an n-channel HEMT and the LMG1020 is a low side driver, we connected the high side in bootstrap configuration. The bootstrap diode is the B520C from Diodes Incorporated, $C_b = 10$ nF, and $R_b = 1 \Omega$. The supply of the LMG1020 is 5 V and the supply of the half bridge is 20 V for consistency with the Class Φ_2 design. A 10 ns dead-time on both transistors was applied to avoid shoot-through and gate resistors $R_{g1,2} = 1 \Omega$ were used for smooth switching. Finally a gate resistor of 2Ω to the output of the half bridge was connected to minimise the overshoot of the gate voltage of the power device.

The various key waveforms from Ltspice simulation of the Class D gate driver in Figure 6.11 are given in Figure 6.12, where it can be confirmed that a 20 V 30 % duty cycle gate voltage to the power device was achieved. In addition, the current stresses on the devices of the half bridge are within their limits, under the condition that the PCB layout will not introduce significant trace inductances.

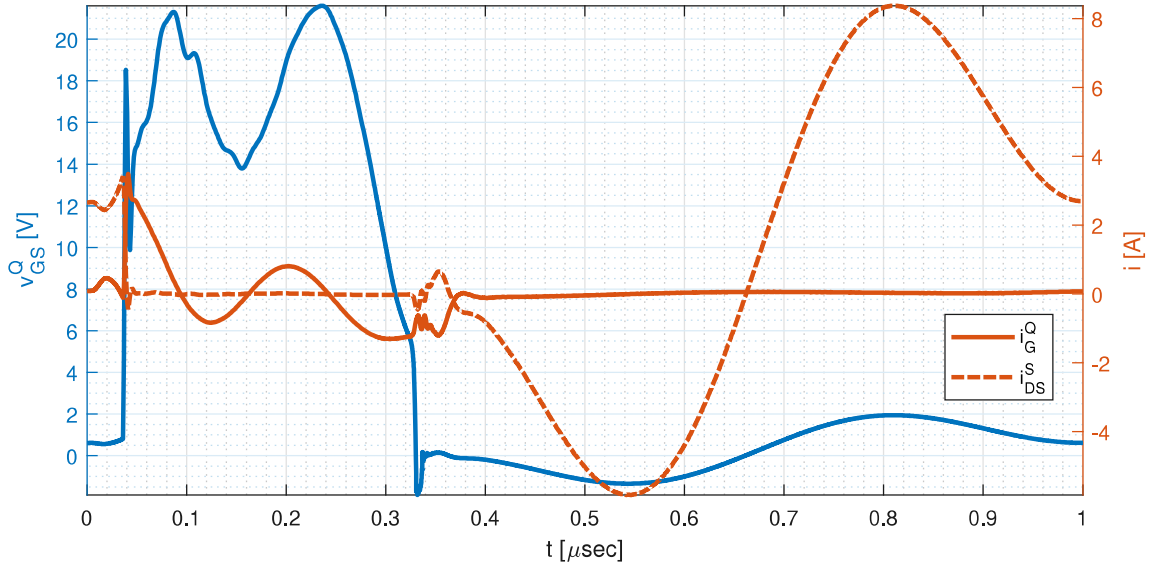


Figure 6.10: Waveforms of the gate voltage and gate current of power device, as well as drain voltage and drain current of the Class Φ_2 transistor. The drain voltage of the Class Φ_2 gate driver transistor is the gate voltage of the power stage.

6.4.4 Performance Comparison of the Two Gate Drivers

In this part of the chapter we present a thorough comparison of various performance metrics of the Class Φ_2 and half-bridge gate driver examples described above. The goal of this analysis is to evaluate the potential benefits and drawbacks of the proposed Class Φ design method as an alternative to a typical gate driving solution, such as the Class D circuit. A summary of both the qualitative and quantitative concepts compared in this subsection is presented in Table 6.3, with the details of the evaluation of each metric and further analysis of the results provided in the following text.

Power Device Performance

The most important quality of a gate driver is the efficiency of the power device and specifically the switching and conduction efficiency. From Figure 6.5 there is no visible difference in the shape of the drain voltage of the C3M0032120J1 transistor between the two drivers. However, that is not the case for the drain current, where the the Class Φ_2 gate driver introduces more ripple at turn-on and the Class D circuit causes high frequency oscillation at turn-off. Overall, the mean power the power device consumed, i.e. the integral over one period of the bottom graph in Figure 6.5, is the same for both gate drivers, which shows that there is no significant

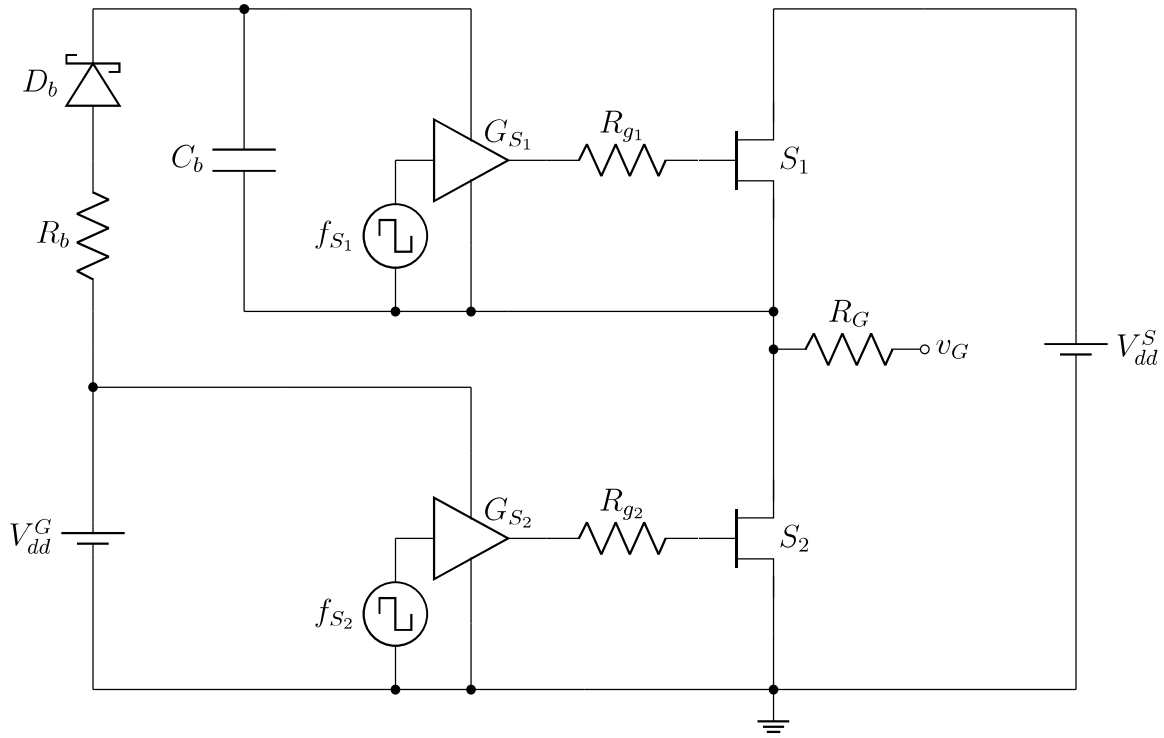


Figure 6.11: Circuit diagram of the half-bridge gate driver example.

performance difference for the power stage between the two circuits. This result can seem a bit counter-intuitive at first glance, since the gate voltage of the Class D gate driver (Figure 6.12) approximates the shape of an ideal voltage source much closer than its Class Φ_2 counterpart (Figure 6.10).

The power on the C3M0032120J1 is calculated around 44 W, where any difference between the two examples being so little that it is indistinguishable from discretisation error during simulation and numerical integration. It should be mentioned at this point that according to the datasheet of C3M0032120J1, 44 W of power dissipation is well within the device's capabilities until 125 °C.

Even though the mean power dissipated on the C3M0032120J1 transistor is practically the same for the two gate drivers, the behaviour of the instantaneous power is very different between the two instances. According to the bottom of Figure 6.5, the peak power of the Class Φ_2 is 28 % lower than that of the half-bridge gate driver. In addition, the half-bridge produces a very high frequency ripple during turn-off, which combined with PCB layout parasitics can increase losses and introduce additional electromagnetic interference (EMI) issues to the power circuit, especially for non soft-switching topologies. This high frequency component difference between the two topologies is also prevalent in Figure 6.6 at frequencies between 70 MHz and 200 MHz.

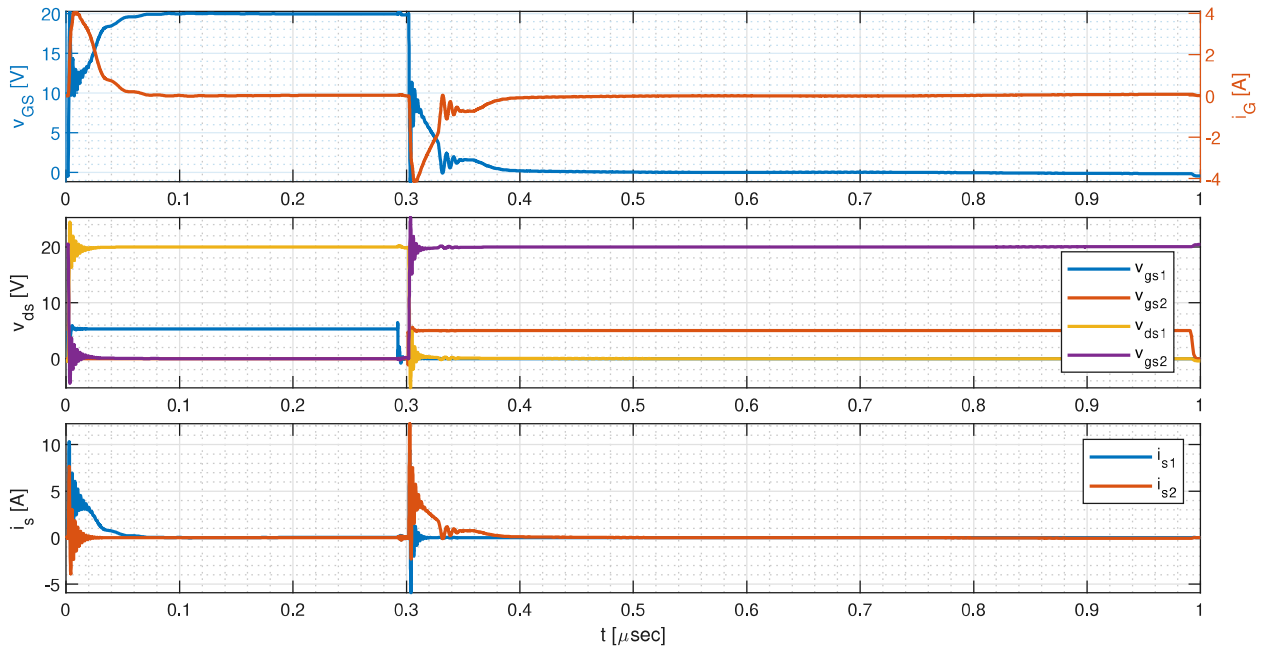


Figure 6.12: Waveforms of the power device gate input voltage and current (top), and gate and drain voltages (middle) and drain currents (bottom) of the half-bridge gate driver.

However, there is no difference in the overall THD with reference to the switching frequency between the drain waveforms of the two gate drivers (Table 6.3).

Gate Driver Performance

By design, the Class D gate driver will always have a substantial benefit over the Class Φ when it comes to the gate voltage waveform shape, as can be observed from Figure 6.10 and Figure 6.12. In our examples, however, this drawback did not translate in increase in power dissipated in the power device for the Class Φ gate driver compared to the Class D, as shown in Table 6.3. The Class Φ example has an overshoot on the gate voltage of over 1 volt, which cannot be suppressed with external gate resistors, as is the case with the half bridge. This overshoot in our example is within the limits of the C3M0032120J1 power transistor.

The Class Φ topology also inherently suffers from the requirement of a complex design procedure, since it is a resonant analog circuit. This issue is only present during the development of the design process. Once the design algorithm is defined and transferred to computer code, the component values for a given application are calculated automatically. On the other hand, the Class D topology requires a lot of manual re-tuning and iterative trial and error until the circuit is optimised (e.g. gate resistances, dead time, etc.), whereas the manual intervention

Table 6.3: Comparison of various performance metrics between the Class Φ_2 and half bridge gate driver examples.

	Quantity	Unit	Class Φ_2	Half bridge	δ [%]
Power Transistor	P_{mean}	W	43.9	43.6	0.69
	P_{max}	kW	0.896	1.24	-28
	$\text{THD}_{v_{DS}}$	%	23	22.92	0.35
	THD_{i_S}	%	82.3	82.07	0.28
	$f_{\text{drain parasitics}}$	MHz	20 to 40	70 to 200	-80
Gate Driver	v_{GS} overshoot	%	1.45	8	451
	Number of S	#	1	2	-50
	Number of passives	#	3	6	-50
	Number of supplies	#	1	2	-50
	$\text{THD}_{i_{in}}$	%	34.6	426	-91.9
	i_{in}^{max}	A	6.86	10.31	-33.5
	i_S^{max}	A	8.37	12.24	-31.6
	P_S^{max}	W	26.3	207	-87.3
	P_S^{mean}	W	1.92*	0.265**	624
	P_G^{total}	W	2.511*	1.431	75
Practical Considerations	Design process	-	Complex	Simple	-
	Manual tuning	-	Minimal	Substantial	-
	PCB layout	-	Simple	Complex	-
	Switching signal	-	Simple	Complex	-
	Decoupling / Input Filter	-	Simple	Complex	-
	Active D control	-	No	Yes	-
	EMI	-	Low	High	-
	High-side switching	-	No	Yes	-
	Transistor current rating	-	Low	High	-
	Main transistor losses	-	Conduction	Switching	-

* Assuming the GS66504B is used.

** Losses on both transistors combined.

needed for our proposed Class Φ design method is minimal.

Another important difference between the two gate driver designs is the switching signal complexity. The Class Φ has a single clock, whereas the Class D requires two complementary clocks, one of which drives a high side device, with the addition of a carefully chosen dead-time to avoid shoot-through. The additional high side transistor of the half-bridge topology also further complicates the gate drive circuitry needed. Also, the half-bridge most probably will require two different levels of supply voltage, one for the transistors and one for the gate driver, which is something that can be avoided through design choices in the Class Φ topology. Both of these issues typically introduce additional complexity to the PCB layout and increase the

component count of the half-bridge. On the other hand, the duty cycle for the Class Φ is fixed because it is based on the resonance of the circuit, whereas in the case of the Class D topology, the duty cycle is controlled by the input clock.

One aspect worth mentioning is the supply decoupling and input filtering required in a practical implementation of the two gate driver examples. This aspect can be qualitatively evaluated by the current waveform of the input inductor in Figure 6.9 for the Class Φ_2 and the drain current of the top transistor in Figure 6.12 of the Class D gate driver. Both the harmonic content Figure 6.13 and the the maximum amplitude of the input current of the half-bridge are significantly larger than those of the Class Φ_2 , which in turn corresponds to the requirement of a more complex supply decoupling solution in the Class D compared to the Class Φ gate driver. The exact numerical values of these differences are shown in Table 6.3. In general, the hard switching Class D topology by default is prone to causing more EMI issues to the overall circuitry compared to the soft-switching resonant Class Φ .

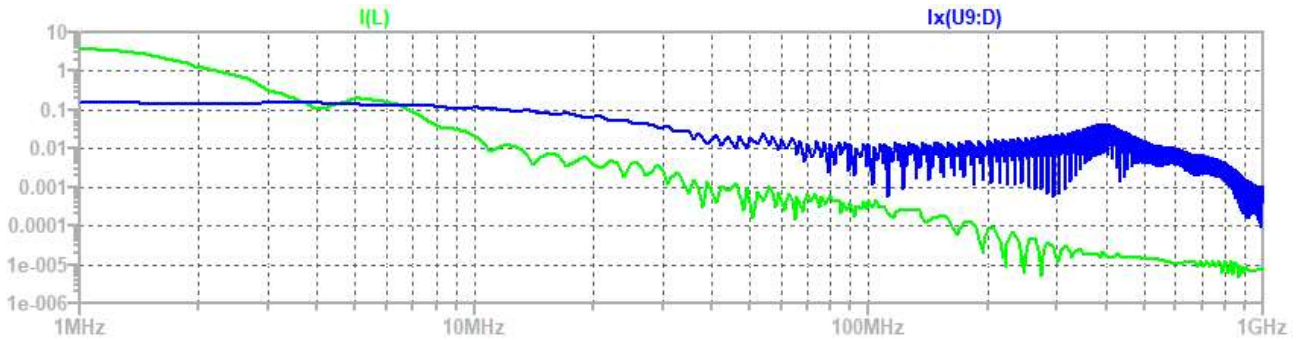


Figure 6.13: Fourier analysis of the input current in [A] of the Class Φ_2 (green) and the Class D (blue) gate driver.

The transistor used for the Class Φ_2 design (GS66502B) has half the current rating of the ones used in the Class D (GS66504B), and the reason is the peak value of the drain current waveforms in Figure 6.10 and Figure 6.12. The exact numerical values of these points are again given in Table 6.3. The instantaneous power over a period at the transistors in the two gate drivers is shown in Figure 6.14, where we can deduct that the main source of losses on the Class D originates from the switching whereas at the Class Φ is because of conduction. Since switching losses typically scale up with frequency and conduction losses are mostly dependent on power level, this is another strong indicator that Class Φ gate drivers are more suitable for high frequency applications, whereas Class D would be more efficient for lower frequency, high power operation. Hence, for a fair comparison, we adjust the transistor losses of the Class Φ

to the R_{DS}^{ON} of the GS66504B, since its ON resistance is half of that of the GS66502B. However, the overall losses on both transistors in the Class D topology are still by far lower compared to the Class Φ_2 , as shown in Table 6.3, even though the peak instantaneous power is higher for the Class D according to Figure 6.14.

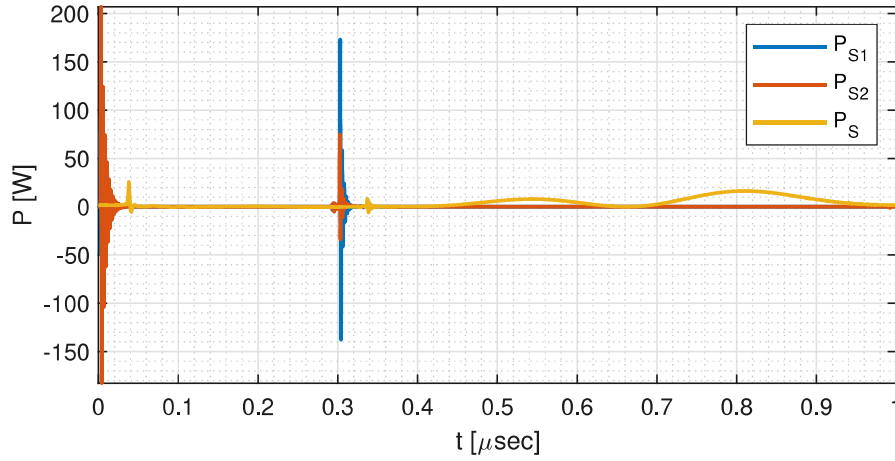


Figure 6.14: Instantaneous power over time on the transistors of the Class D gate driver (top transistor is in blue and bottom transistor is in orange) and the transistor of the Class Φ_2 gate driver (yellow).

Finally, we calculate and compare the total power consumption of the two gate driver examples where we also provide a breakdown of the losses of individual components. The power losses of the Class D gate driver are directly derived from the LTspice simulation data. For the Class Φ_2 example we approximate the current of L_{in} with a first order harmonic and the current of L_r with a second order harmonic, the amplitudes of which are the peak values of the corresponding waveforms in Figure 6.9. We assume the Q factors of both inductors in the Class Φ_2 to be 200, which is reasonable for these frequencies [27]. The formula for the power approximation of those inductors is

$$P_L = \frac{\pi I_L^2 f_L L}{Q_L}, \quad (6.38)$$

where I_L is the peak current, f_L is the harmonic, and Q_L is the quality factor of the inductor L .

The results for the total power losses are presented in Table 6.3 and in Figure 6.15 in a more detailed breakdown. The high gate charge requirement of the C3M0032120J1 transistor combined with the relatively low switching frequency favour the Class D over the Class Φ topology when it comes to gate driver efficiency. However, driving a similar power transistor in a resonant converter at this frequency range with an off-the-shelf gate driver chip consumed over 20 W,

according to [120].

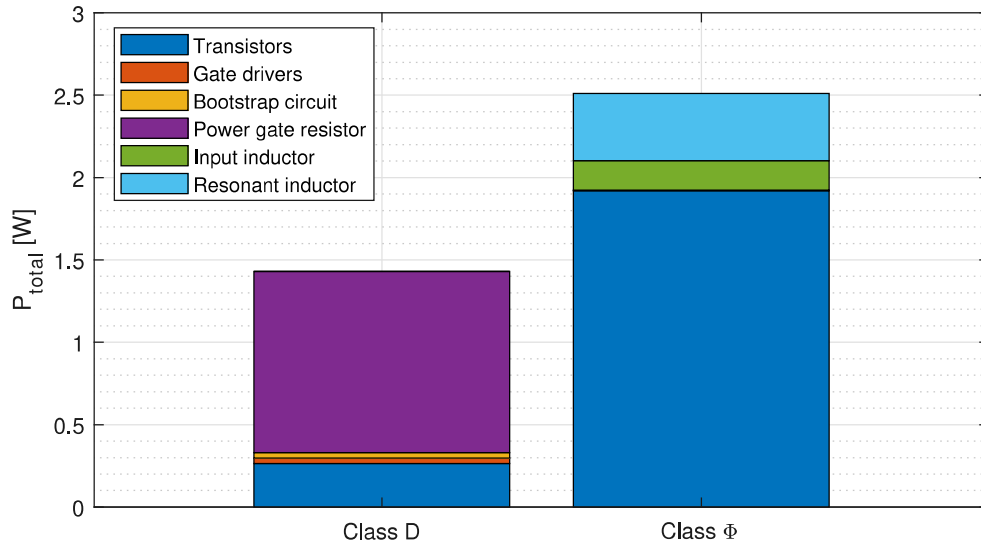


Figure 6.15: Breakdown of the total losses distribution in the two gate driver examples in Table 6.3.

6.5 Summary

In this chapter we first present a comprehensive SS mathematical analysis of a Class Φ gate driver, and derive analytic expressions for the circuit waveforms. Based on this formulation, we propose a complete and well defined design method for calculating the component values of the resonant gate driver. We apply our gate design method to drive a 6 kW, 1 MHz single ended Class E inverter with a GaN based Class Φ_2 gate driver. As a benchmark comparison, we also design a traditional half-bridge gate driver for the same application.

Our thorough comparative investigation of the performance of the two gate driver examples leads to the key results summed up in Table 6.3. The Class D gate driver outperformed its resonant counterpart in efficiency, since the switching frequency was not high enough for the switching losses to become a limiting factor, and gate voltage shaping capabilities, which is by design a strong point for half-bridge topologies. However, the difference in gate driver efficiency has trivial effect on the overall efficiency of the power stage and the efficiency of the power transistor showed no difference.

On the other hand, the Class Φ_2 gate driver has inherently better EMI, because of the soft

switching, which leads to simpler layout, easier circuit debugging during testing, and reduced filtering requirements. Also, has fewer discrete components and only low side switching, which further simplifies the circuit layout. In our example, through the design freedom that our algorithm provides, we manage to only use a single voltage supply for the entire gate drive circuit. In addition, the Class Φ gate driver requires lower device power rating, compared to the Class D, which further increases the potential for high frequency operation.

However, there is still room for improvement in our design method. The analysis of this chapter provides an SS level of accuracy. But, as shown in chapter 2, the full non-linear device model needs to be taken into account to completely eliminate the need for manual retuning, especially as the operating frequency increases. Once the non-linear design method is defined and optimised, an experimental test rig can be set up for the evaluation of the performance and practical limitations of the resonant gate driver.

Chapter 7

Conclusion

7.1 Overview and Main Findings

The main contribution of this thesis is the design method for Class EF and Class Φ inverters, presented in chapter 2. This design method also serves as the basis for the content of the rest of the chapters. The proposed design algorithm is made of four distinct parts, that are standalone. The first part is based on FO analysis, which already has been thoroughly investigated in the literature, where we incorporate incremental improvements and investigate the sources of error. The other three parts of the design algorithm are novel and each one contributes in further improvement with regards to accuracy. Two Class EF inverter examples at 13.56 MHz 50 W are developed, where the experimental setup approaches the theoretical efficiency of 97 %, whilst maintaining all of the other design requirements. The algorithm changes the values of the components over 5 %–50 % and improves the simulated waveform accuracy by 2–12 times compared with the design method based on first-order approximations.

In chapter 3 several methods for scaling up the output power of GaN based HF-IPT systems are discussed. A parallel configuration for resonant inverters is proposed based on both single ended and push-pull individual topologies. Next, the benefits and drawbacks of having a differential shunt capacitor in push-pull Class E inverters are investigated on real transistor models and load variation conditions. In addition, a split capacitor semi-resonance connection for push-pull inverters is introduced, to further reduce the component current stresses in high power applications. Also, the practical design of a novel common infinite choke push pull Class DE

inverter is presented and compared to the traditional Class E and Class DE counterparts. Two experimental setups at 3.39 MHz 3 kW were developed and tested: a push-pull Class EF₂ DC/AC, and a parallel push-pull Class E inverter with a full bridge Class DE rectifier DC/DC IPT system. The DC/DC system exhibits maximum efficiency of 95 % at full load.

A one-to-many resonant IPT link design method is introduced in chapter 4. The algorithm is based on a half-bridge Class D current driven rectifier and the objective conditions are maximisation of power throughput with zero reflected reactance to the primary, while maintaining as balanced outputs as possible. The algorithm is verified through simulation results in this work and is applied to the experimental setup in [70]. Also, in the same chapter, an indirect link characterisation method is introduced, for use when the measurement equipment fails to produce accurate results. The method is based on accurate characterisation of HF converters, which has been established in chapter 2. The application of the method is successfully shown in a parallel push pull Class EF₂ inverter and a Class DE current driven rectifier on electrically large coils in the presence of magnetic shielding.

In chapter 5 the limitations of the open-loop operation of Class E type inverters are studied and the possibility of adjusting to both resistive and reactive load variations is investigated. Several implicit on-board indicators that translate to load changes are identified, and power modulation by controlling the input voltage, frequency and duty cycle while maximising efficiency is proposed. Various examples, both simulated and experimental are shown that prove the concept of active real time inverter adjustment to load and magnetic environment variations.

A Class Φ resonant gate driver design method is proposed in chapter 6. Our design method has state space accuracy with analytic equations, and a fully defined algorithm and detailed breakdown of the methodology are provided. A Class Φ_2 gate driver is developed and compared to a half-bridge gate driver, on a high power SiC based Class EF₂ inverter. The Class Φ_2 gate driver has slightly higher power consumption than the half bridge, but exhibits significant superiority in EMI, and is easier to implement by only requiring a single low side transistor and a single universal power supply for the entirety of the driver circuitry.

7.2 Publications

Journal Publication as Lead Author

I. Nikiforidis, J. M. Arteaga, C. H. Kwan, N. Pucci, D. C. Yates and P. D. Mitcheson, "Generalized Multistage Modeling and Tuning Algorithm for Class EF and Class Φ Inverters to Eliminate Iterative Retuning," in *IEEE Transactions on Power Electronics*, vol. 37, no. 10, pp. 12877-12900, Oct. 2022, doi: 10.1109/TPEL.2022.3176391. This work is listed as reference [113].

Conference Publication as Lead Author

I. Nikiforidis, J. M. Arteaga, C. H. Kwan, D. C. Yates and P. D. Mitcheson, "Design and Modelling of Class EF Inverters for Wireless Power Transfer Applications," *2019 19th International Conference on Micro and Nanotechnology for Power Generation and Energy Conversion Applications (PowerMEMS)*, 2019, pp. 1-4, doi: 10.1109/PowerMEMS49317.2019.61547406204. This work is listed as reference [61].

I. Nikiforidis, C. H. Kwan, D. C. Yates, K. Bampouras, J. Gawith, N. Pucci and P. D. Mitcheson, "A 3 kW 3.39 MHz DC/DC Inductive Power Transfer System with Power Combining Converters," *2023 IEEE Wireless Power Technologies Conference and Expo (WPTCE)*, 2023. This work has been accepted for publication.

Conference Publication as Co-author

J. M. Arteaga et al., "Design of a One-to-Four Isolated DC-DC Converter Using a 13.56 MHz Resonant Air-Core Transformer," *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2021, pp. 2580-2585, doi: 10.1109/APEC42165.2021.9487409. This work is listed as reference [70].

7.3 Future Work

Now that the complete design method for Class EF/ Φ inverters has been defined in detail in chapter 2, the next step would be to conduct a thorough parametric comparative analysis for the effect of various values of the input parameters. The results of such study could be used to structure optimal design guidelines based on specific demands of individual applications. Furthermore, this design methodology can be adjusted and applied to other kinds of Class E type inverters and rectifiers.

The current stage of the design process for the common infinite choke push-pull Class DE topology introduced in section 3.4 is very primitive and relies on manual adjustment starting from a traditional Class DE inverter. The design method should be refined and automated, in-line with the procedures used in chapter 2, so that the behaviour of the resulting converter is controlled according to the input parameters. In addition, the experimental testing of the parallel push-pull inverter topology should be conducted to the limits of the components using better PCB layouts. Also, the possibility of parallel and series transistors for current and voltage splitting can be tried and refined for high frequency operation.

The one-to-many link design can be generalised to many-to-many and the operating conditions, as well as the rectifier topologies can be further enriched from the case presented in this work. In addition, the dynamic behaviour of such a complex link can be studied for more robust link designs.

In this work, the active inverter adjustment experiments applied manual re-tuning, since the objective was to prove the concept of the control algorithm. Future work can introduce automated on board control and more testing under different conditions.

The design method of the Class Φ gate driver proposed has state space accuracy. An important improvement to the current design algorithm would be the incorporation of non-linearities, as shown in chapter 2. Also, our current work lacks experimental verification. Furthermore, the introduction of more resonant branches can be investigated, in order to achieve more control over the shape the gate voltage.

Bibliography

- [1] S. Aldhafer, D. C. Yates, and P. D. Mitcheson, “Load-independent Class E/EF inverters and rectifiers for MHz-switching applications,” *IEEE Transactions on Power Electronics*, vol. 33, no. 10, pp. 8270–8287, 2018.
- [2] S. R. Khan, S. K. Pavuluri, G. Cummins, and M. P. Desmulliez, “Wireless power transfer techniques for implantable medical devices: A review,” *Sensors*, vol. 20, no. 12, p. 3487, 2020.
- [3] N. Pucci, C. H. Kwan, D. C. Yates, and P. D. Mitcheson, “Multi-megahertz ipt systems for biomedical devices applications,” in *2019 19th International Conference on Micro and Nanotechnology for Power Generation and Energy Conversion Applications (PowerMEMS)*, 2019, pp. 1–7.
- [4] J. Sanchez, J. M. Arteaga, N. Pucci, P. Mitcheson, E. Yeatman, D. Young, C. Zesiger, and S. Roundy, “Misalignment parameterization of a 13.56 mhz inductive power transfer system for in-situ soil sensing,” in *2022 21st International Conference on Micro and Nanotechnology for Power Generation and Energy Conversion Applications (PowerMEMS)*, 2022, pp. 278–281.
- [5] G. A. Covic and J. T. Boys, “Inductive power transfer,” *Proceedings of the IEEE*, vol. 101, no. 6, pp. 1276–1289, 2013.
- [6] G. E. Maryniak, “Status of international experimentation in wireless power transmission,” *Solar energy*, vol. 56, no. 1, pp. 87–91, 1996.
- [7] M. El Rayes, G. Nagib, and W. Abdelaal, “A review on wireless power transfer,” *International Journal of Engineering Trends and Technology (IJETT)*, vol. 40, p. 272, 10 2016.

- [8] N. Tesla, *The true wireless*. Simon and Schuster, 2015.
- [9] J. Garnica, R. A. Chinga, and J. Lin, “Wireless power transmission: From far field to near field,” *Proceedings of the IEEE*, vol. 101, no. 6, pp. 1321–1331, 2013.
- [10] M. Meneghini and E. Zanoni, *Gallium Nitride-enabled High Frequency and High Efficiency Power Conversion*. Springer, 2018.
- [11] J. Van Mulders, D. Delabie, C. Lecluyse, C. Buyle, G. Callebaut, L. Van der Perre, and L. De Strycker, “Wireless power transfer: Systems, circuits, standards, and use cases,” *Sensors*, vol. 22, no. 15, p. 5573, 2022.
- [12] A. Kurs, A. Karalis, R. Moffatt, J. D. Joannopoulos, P. Fisher, and M. Soljačić, “Wireless power transfer via strongly coupled magnetic resonances,” *Science*, vol. 317, no. 5834, pp. 83–86, 2007. [Online]. Available: <https://www.science.org/doi/abs/10.1126/science.1143254>
- [13] S. Y. R. Hui, W. Zhong, and C. K. Lee, “A critical review of recent progress in mid-range wireless power transfer,” *IEEE Transactions on Power Electronics*, vol. 29, no. 9, pp. 4500–4511, 2013.
- [14] A. Foote and O. C. Onar, “A review of high-power wireless power transfer,” in *2017 IEEE Transportation Electrification Conference and Expo (ITEC)*. IEEE, 2017, pp. 234–240.
- [15] G. A. Covic and J. T. Boys, “Modern trends in inductive power transfer for transportation applications,” *IEEE Journal of Emerging and Selected topics in power electronics*, vol. 1, no. 1, pp. 28–41, 2013.
- [16] A. M. Jawad, R. Nordin, S. K. Gharghan, H. M. Jawad, and M. Ismail, “Opportunities and challenges for near-field wireless power transfer: A review,” *Energies*, vol. 10, no. 7, p. 1022, 2017.
- [17] C. Jiang, K. T. Chau, C. Liu, and C. H. T. Lee, “An overview of resonant circuits for wireless power transfer,” *Energies*, vol. 10, no. 7, 2017. [Online]. Available: <https://www.mdpi.com/1996-1073/10/7/894>
- [18] D. J. Griffiths, *Introduction to electrodynamics*. American Association of Physics Teachers, 2005.

- [19] K. Van Schuylenbergh and R. Puers, *Inductive powering: basic theory and application to biomedical systems*. Springer Science & Business Media, 2009.
- [20] J. M. Arteaga Saenz, “Design of high frequency inductive power transfer systems for integration into applications,” Ph.D. dissertation, Imperial College London, 2019.
- [21] G. Kkelis, D. C. Yates, and P. D. Mitcheson, “Class-E half-wave zero dv/dt rectifiers for inductive power transfer,” *IEEE Transactions on Power Electronics*, vol. 32, no. 11, pp. 8322–8337, 2017.
- [22] H. Koizumi, T. Suetsugu, M. Fujii, K. Shinoda, S. Mori, and K. Ikeda, “Class DE high-efficiency tuned power amplifier,” *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 43, no. 1, pp. 51–60, 1996.
- [23] J. Choi, J. Xu, R. Makhoul, and J. M. R. Davila, “Implementing an impedance compression network to compensate for misalignments in a wireless power transfer system,” *IEEE Transactions on Power Electronics*, vol. 34, no. 5, pp. 4173–4184, 2019.
- [24] W. Zhang, S.-C. Wong, C. K. Tse, and Q. Chen, “Load-independent duality of current and voltage outputs of a series- or parallel-compensated inductive power transfer converter with optimized efficiency,” *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 3, no. 1, pp. 137–146, 2015.
- [25] G. Kkelis, “Rectifier design for optimisation of multi-MHz inductive power transfer systems,” Ph.D. dissertation, Imperial College London, 2017.
- [26] F. H. Raab, “Effects of circuit variations on the Class E tuned power amplifier,” *IEEE Journal of Solid-State Circuits*, vol. 13, no. 2, pp. 239–247, 1978.
- [27] M. K. Kazimierczuk, *High-frequency magnetic components*. John Wiley & Sons, 2013.
- [28] —, *RF power amplifiers*. John Wiley & Sons, 2014.
- [29] R. J. Gutmann, “Application of RF circuit design principles to distributed power converters,” *IEEE Transactions on Industrial Electronics and Control Instrumentation*, vol. IECI-27, no. 3, pp. 156–164, 1980.

- [30] F. Raab, "Class-E, Class-C, and Class-F power amplifiers based upon a finite number of harmonics," *IEEE Transactions on Microwave Theory and Techniques*, vol. 49, no. 8, pp. 1462–1468, 2001.
- [31] X. Huang, Y. Kong, Z. Ouyang, W. Chen, and S. Lin, "Analysis and comparison of push–pull Class-E inverters with magnetic integration for megahertz wireless power transfer," *IEEE Transactions on Power Electronics*, vol. 35, no. 1, pp. 565–577, 2020.
- [32] F. Raab, "Idealized operation of the Class E tuned power amplifier," *IEEE Transactions on Circuits and Systems*, vol. 24, no. 12, pp. 725–735, 1977.
- [33] A. Grebennikov and M. J. Franco, *Switchmode RF and microwave power amplifiers*. Academic Press, 2021.
- [34] R. Zulinski and K. Grady, "Load-independent Class E power inverters. I. Theoretical development," *IEEE Transactions on Circuits and Systems*, vol. 37, no. 8, pp. 1010–1018, 1990.
- [35] S. Aldhafer, D. C. Yates, and P. D. Mitcheson, "Modeling and analysis of Class EF and Class E/F inverters with series-tuned resonant networks," *IEEE Transactions on Power Electronics*, vol. 31, no. 5, pp. 3415–3430, 2016.
- [36] M. K. Kazimierczuk and D. Czarkowski, *Resonant power converters*. John Wiley & Sons, 2012.
- [37] M. N. Undeland, W. P. Robbins, and N. Mohan, "Power electronics," in *Converters, Applications, and Design*. John Wiley & Sons, 1995.
- [38] M. Etemadrezai, "22 - Wireless power transfer," in *Power Electronics Handbook (Fourth Edition)*, 4th ed., M. H. Rashid, Ed. Butterworth-Heinemann, 2018, pp. 711–722. [Online]. Available: <https://www.sciencedirect.com/science/article/pii/B9780128114070000246>
- [39] G. Zulauf and J. M. Rivas-Davila, "Single-turn air-core coils for high-frequency inductive wireless power transfer," *IEEE Transactions on Power Electronics*, vol. 35, no. 3, pp. 2917–2932, 2020.

- [40] Z. Kaczmarczyk, “High-efficiency Class E, EF_2 , and E/ F_3 inverters,” *IEEE Transactions on Industrial Electronics*, vol. 53, no. 5, pp. 1584–1593, Oct. 2006.
- [41] S. Kee, I. Aoki, A. Hajimiri, and D. Rutledge, “The class-E/F family of ZVS switching amplifiers,” *IEEE Transactions on Microwave Theory and Techniques*, vol. 51, no. 6, pp. 1677–1690, 2003.
- [42] A. Mediano and N. O. Sokal, “A Class-E RF power amplifier with a flat-top transistor-voltage waveform,” *IEEE Transactions on Power Electronics*, vol. 28, no. 11, pp. 5215–5221, 2013.
- [43] L. Zhang, “Load-independent Class-E power conversion,” Ph.D. dissertation, Virginia Tech, 2020.
- [44] W. Luo, Y. Ogi, F. Ebihara, X. Wei, and H. Sekiya, “Design of load-independent Class-E inverter with MOSFET gate-to-drain and drain-to-source parasitic capacitances,” *Non-linear Theory and Its Applications, IEICE*, vol. 11, no. 2, pp. 267–277, 2020.
- [45] L. Roslaniec, A. S. Jurkov, A. A. Bastami, and D. J. Perreault, “Design of single-switch inverters for variable resistance/load modulation operation,” *IEEE Transactions on Power Electronics*, vol. 30, no. 6, pp. 3200–3214, 2015.
- [46] N. O. Sokal, “Class-E RF power amplifiers,” *Qex*, vol. 204, no. 1, pp. 9–20, 2001.
- [47] J. S. Rodríguez Páez and A. Fajardo, “Class-E PA design methodology by re-tuning,” in *2014 IEEE 5th Colombian Workshop on Circuits and Systems (CWCAS)*, 2014, pp. 1–4.
- [48] J. S. Glaser and J. M. Rivas, “A 500 W push-pull DC-DC power converter with a 30 MHz switching frequency,” in *2010 Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2010, pp. 654–661.
- [49] N. O. Sokal and A. Mediano, “Redefining the optimum RF Class-E switch-voltage waveform, to correct a long-used incorrect waveform,” in *2013 IEEE MTT-S International Microwave Symposium Digest (MTT)*, 2013, pp. 1–3.
- [50] M. Kazimierzczuk and K. Puczek, “Exact analysis of Class E tuned power amplifier at any Q and switch duty cycle,” *IEEE Transactions on Circuits and Systems*, vol. 34, no. 2, pp. 149–159, 1987.

- [51] C. Avratoglou and N. Voulgaris, “A new method for the analysis and design of the Class E power amplifier taking into account the Q_L factor,” *IEEE Transactions on Circuits and Systems*, vol. 34, no. 6, pp. 687–691, 1987.
- [52] L. Zhang and K. Ngo, “A constant-current ZVS Class-E inverter with finite input inductance,” *IEEE Transactions on Industrial Electronics*, vol. 68, no. 8, pp. 7693–7696, 2021.
- [53] —, “Design methodology of a ZVS Class-E inverter with fixed gain,” in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2019, pp. 2752–2758.
- [54] Z. Tong, L. Gu, and J. Rivas-Davila, “Wideband PPT Class Φ_2 inverter using phase-switched impedance modulation and reactance compensation,” *IEEE Transactions on Industrial Electronics*, pp. 1–1, 2021.
- [55] J. M. Rivas, Y. Han, O. Leitermann, A. D. Sagneri, and D. J. Perreault, “A high-frequency resonant inverter topology with low-voltage stress,” *IEEE Transactions on Power Electronics*, vol. 23, no. 4, pp. 1759–1771, 2008.
- [56] S. Aldhafer, G. Kkelis, D. C. Yates, and P. D. Mitcheson, “Class EF_2 inverters for wireless power transfer applications,” in *2015 IEEE Wireless Power Transfer Conference (WPTC)*, 2015, pp. 1–4.
- [57] W. Zhu, Y. Komiyama, K. Nguyen, and H. Sekiya, “Heuristic algorithm-based design method for Class-E switching circuits,” in *2021 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2021, pp. 5692–5697.
- [58] J. Ma, Asiya, X. Wei, K. Nguyen, and H. Sekiya, “Analysis and design of generalized Class-E/ F_2 and Class-E/ F_3 inverters,” *IEEE Access*, vol. 8, pp. 61 277–61 288, 2020.
- [59] M. Chudobiak, “The use of parasitic nonlinear capacitors in Class E amplifiers,” *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 41, no. 12, pp. 941–944, 1994.
- [60] J. Choi, D. Tsukiyama, Y. Tsuruda, and J. M. R. Davila, “High-frequency, high-power resonant inverter with eGaN FET for wireless power transfer,” *IEEE Transactions on Power Electronics*, vol. 33, no. 3, pp. 1890–1896, 2018.

- [61] I. Nikiforidis, J. M. Arteaga, C. H. Kwan, D. C. Yates, and P. D. Mitcheson, “Design and modelling of Class EF inverters for wireless power transfer applications,” in *2019 19th International Conference on Micro and Nanotechnology for Power Generation and Energy Conversion Applications (PowerMEMS)*, 2019, pp. 1–4.
- [62] A. Grebennikov, “Load network design techniques for Class E RF and microwave amplifiers,” *High Frequency Electronics*, vol. 3, no. 7, pp. 18–32, 2004.
- [63] A. Grebennikov and H. Jaeger, “Class E with parallel circuit - a new challenge for high-efficiency RF and microwave power amplifiers,” in *2002 IEEE MTT-S International Microwave Symposium Digest (Cat. No.02CH37278)*, vol. 3, 2002, pp. 1627–1630 vol.3.
- [64] M. J. Powell, “A fortran subroutine for solving systems of non-linear algebraic equations,” Argonne National Laboratory, Harwell, Berkshire, Tech. Rep. AERE-R.5947, Nov. 1968.
- [65] J. J. Moré and B. S. Garbow, “User guide for MINPACK-1,” Argonne National Laboratory, Argonne, IL, Tech. Rep. ANL-80-74, Aug. 1980.
- [66] R. Brent, *Algorithms for minimization without derivatives*. Prentice-Hall, 1973.
- [67] G. E. Forsythe, M. A. Malcolm, and C. B. Moler, *Computer Methods for Mathematical Computations*. Prentice Hall Professional Technical Reference, 1977.
- [68] S. Y. R. Hui, W. Zhong, and C. K. Lee, “A critical review of recent progress in mid-range wireless power transfer,” *IEEE Transactions on Power Electronics*, vol. 29, no. 9, pp. 4500–4511, 2014.
- [69] *Power resistor thick film technology*, Vishay Intertechnology, Inc., 2019. [Online]. Available: <https://www.vishay.com/docs/50051/lto100.pdf>
- [70] J. M. Arteaga, C. H. Kwan, I. Nikiforidis, N. Pucci, L. Lan, D. C. Yates, and P. D. Mitcheson, “Design of a one-to-four isolated DC-DC converter using a 13.56 MHz resonant air-core transformer,” in *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2021, pp. 2580–2585.
- [71] E. Shamonina, L. Solymar, and V. Kalinin, “On wireless power transfer between coils in the presence of radiation,” *Journal of Physics D: Applied Physics*, vol. 54, no. 40, p. 405502, jul 2021. [Online]. Available: <https://doi.org/10.1088/1361-6463/ac0c4f>

- [72] J. Lawson, D. C. Yates, and P. D. Mitcheson, "High Q coil measurement for inductive power transfer," *IEEE Transactions on Microwave Theory and Techniques*, vol. 67, no. 5, pp. 1962–1973, 2019.
- [73] *Multilayer ceramic chip capacitors*, TDK, 2021. [Online]. Available: https://product.tdk.com/en/system/files?file=dam/doc/product/capacitor/ceramic/mlcc/catalog/mlcc_automotive_highvoltage_en.pdf
- [74] *Keysight N2780/1/2/3B current probes*, Keysight Technologies, Inc., Colorado Springs, CO, 2013. [Online]. Available: <http://literature.cdn.keysight.com/litweb/pdf/N2780-97005.pdf>
- [75] F. Terman, *Radio Engineers' Handbook*. New York and London: McGraw-Hill Book Company, 1943.
- [76] M. Pinuela, D. C. Yates, S. Lucyszyn, and P. D. Mitcheson, "Maximizing DC-to-load efficiency for inductive power transfer," *IEEE Transactions on Power Electronics*, vol. 28, no. 5, pp. 2437–2447, 2013.
- [77] "Radio regulations," ITU, Geneva, Switzerland, Tech. Rep., 2020.
- [78] N. Sokal and F. Raab, "Harmonic output of class-E RF power amplifiers and load coupling network design," *IEEE Journal of Solid-State Circuits*, vol. 12, no. 1, pp. 86–88, 1977.
- [79] P. C.-K. Luk, S. Aldhaher, W. Fei, and J. F. Whidborne, "State-space modeling of a Class E² converter for inductive links," *IEEE Transactions on Power Electronics*, vol. 30, no. 6, pp. 3242–3251, 2015.
- [80] H. Mahdi, A. M. Ammar, Y. Nour, and M. A. E. Andersen, "A Class-E-based resonant AC-DC converter with inherent PFC capability," *IEEE Access*, vol. 9, pp. 46 664–46 673, 2021.
- [81] F. Zhang, *The Schur complement and its applications*. Springer Science & Business Media, 2006, vol. 4.
- [82] P. Händel, "Evaluation of a standardized sine wave fit algorithm," *Proceedings of NOR-SIG2000 Nordic Signal Processing Symposium*, May 2000.

- [83] F. Hildebrand, *Introduction to numerical analysis: Second edition*, ser. Dover Books on Mathematics. Dover Publications, 2013. [Online]. Available: <https://books.google.co.uk/books?id=ic2jAQAAQBAJ>
- [84] J. Cheer and S. Daley, “A method of adaptation between steepest-descent and newton’s algorithm for multichannel active control of tonal noise and vibration,” in *International Institute of Acoustics and Vibration*, 2014.
- [85] J. Fike, S. Jongsma, J. Alonso, and E. Van Der Weide, “Optimization with gradient and hessian information calculated using hyper-dual numbers,” in *29th AIAA Applied Aerodynamics Conference*, 2011, p. 3807.
- [86] H. Tsai and K. Chan, “A note on parameter differentiation of matrix exponentials, with applications to continuous-time modelling,” *Bernoulli*, vol. 9, no. 5, pp. 895 – 919, 2003. [Online]. Available: <https://doi.org/10.3150/bj/1066418883>
- [87] G. Golub, C. Van Loan, P. Van Loan, and C. Van Loan, *Matrix computations*, ser. Johns Hopkins studies in the mathematical sciences. Johns Hopkins University Press, 1996. [Online]. Available: <https://books.google.co.uk/books?id=mlOa7wPX6OYC>
- [88] *WE-PD performance SMT shielded power inductor*, Würth Elektronik eiSos GmbH & Co. KG, Waldenburg, Germany, 1999.
- [89] *GS66504B bottom-side cooled 650 V e-mode GaN transistor preliminary datasheet*, GaN Systems Inc., 2020.
- [90] *High frequency, high current power inductors*, Coilcraft Inc., 2013.
- [91] R. W. Erickson and D. Maksimovic, *Fundamentals of power electronics*. Springer Science & Business Media, 2007.
- [92] A. T. Tiruneh, “A two-point Newton method suitable for non-convergent cases and with super-quadratic convergence,” *arXiv:1210.5766*, 2012.
- [93] M. Arioli, I. Duff, and D. Ruiz, “Stopping criteria for iterative solvers,” *SIAM Journal on Matrix Analysis and Applications*, vol. 13, no. 1, pp. 138–144, 1992.

- [94] L. Fan, A. Knott, and I. Jørgensen, “Nonlinear parasitic capacitance modelling of high voltage power MOSFETs in partial SOI process,” *Elektronika ir Elektrotechnika*, vol. 22, no. 3, pp. 37–43, 2016.
- [95] J. Zhuang, G. Zulauf, J. Roig-Guitart, J. Plummer, and J. Rivas, “Small- and large-signal dynamic output capacitance and energy loss in GaN-on-Si power HEMTs,” *IEEE Transactions on Electron Devices*, vol. 68, no. 4, pp. 1819–1826, 2021.
- [96] *LMG1020 5-V, 7-A, 5-A low-side GaN and MOSFET driver for 1-ns pulse width applications*, Texas Instruments, 2018.
- [97] S. O. Kasap, *Principles of electronic materials and devices*. McGraw-Hill New York, 2006, vol. 2.
- [98] A. S. Sedra and K. C. Smith, *Microelectronic circuits*, 5th ed. Oxford University Press, 2004.
- [99] J. Pujol, “The solution of nonlinear inverse problems and the Levenberg-Marquardt method,” *Geophysics*, vol. 72, no. 4, pp. W1–W16, 2007.
- [100] A. Botchkarev, “Performance metrics (error measures) in machine learning regression, forecasting and prognostics: Properties and typology,” *arXiv preprint arXiv:1809.03006*, 2018.
- [101] J. Zhuang, G. Zulauf, J. Roig, J. D. Plummer, and J. Rivas-Davila, “An investigation into the causes of Coss losses in GaN-on-Si HEMTs,” in *2019 20th Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2019, pp. 1–7.
- [102] H. P. Langtangen, “Solving nonlinear ODE and PDE problems,” *Center for Biomedical Computing, Simula Research Laboratory and Department of Informatics, University of Oslo*, 2016.
- [103] E. Kvaalen, “A faster Broyden method,” *BIT Numerical Mathematics*, vol. 31, no. 2, pp. 369–372, 1991.
- [104] G. Brocard, *The LTSpice IV simulator: Manual, methods and applications*. Würth Elektronik, 2013. [Online]. Available: <https://books.google.co.uk/books?id=AuGSngEACAAJ>

- [105] N. O. Sokal, “Class-e high-efficiency rf/microwave power amplifiers: Principles of operation, design procedures, and experimental verification,” *Analog Circuit Design: Scalable Analog Circuit Design, High Speed D/A converters, RF Power Amplifiers*, pp. 269–301, 2002.
- [106] T. R. Chandrupatla, “A new hybrid quadratic/bisection algorithm for finding the zero of a nonlinear function without using derivatives,” *Advances in Engineering Software*, vol. 28, no. 3, pp. 145–149, 1997. [Online]. Available: <https://www.sciencedirect.com/science/article/pii/S0965997896000518>
- [107] D. Causton, “A computer program for fitting the Richards function,” *Biometrics*, pp. 401–409, 1969.
- [108] D. Fekedulegn, M. P. Mac Siúrtáin, and J. J. Colbert, “Parameter estimation of nonlinear models in forestry,” *Silva Fennica*, vol. 33, no. 4, pp. 327–336, 1999.
- [109] L. Collatz, *The numerical treatment of differential equations*. Springer Science & Business Media, 2012, vol. 60.
- [110] A. Eiger, K. Sikorski, and F. Stenger, “A bisection method for systems of nonlinear equations,” *ACM Transactions on Mathematical Software (TOMS)*, vol. 10, no. 4, pp. 367–377, 1984.
- [111] *Isolated measurement systems TIVM1, TIVM1L, TIVH08, TIVH08L, TIVH05, TIVH05L, TIVH02, TIVH02L datasheet*, Tektronix Inc., 2018. [Online]. Available: <https://download.tek.com/datasheet/TIVH-Series-IsoVu-Measurement-Systems-Datasheet-51W612172.pdf>
- [112] N. Pucci, J. M. Arteaga, C. Kwan, D. C. Yates, and P. D. Mitcheson, “Induced voltage estimation from Class EF switching harmonics in HF-IPT systems,” *IEEE Transactions on Power Electronics*, 2021.
- [113] I. Nikiforidis, J. M. Arteaga, C. H. Kwan, N. Pucci, D. C. Yates, and P. D. Mitcheson, “Generalized multistage modeling and tuning algorithm for Class EF and Class Φ inverters to eliminate iterative retuning,” *IEEE Transactions on Power Electronics*, vol. 37, no. 10, pp. 12 877–12 900, 2022.

- [114] LiYong, MaiRuikun, LuLiwen, and HeZhengyou, “A novel IPT system based on dual coupled primary tracks for high power applications,” *Journal of Power Electronics*, vol. 16, no. 1, pp. 111–120, 01 2016.
- [115] J. H. Kim, B.-S. Lee, J.-H. Lee, S.-H. Lee, C.-B. Park, S.-M. Jung, S.-G. Lee, K.-P. Yi, and J. Baek, “Development of 1-MW inductive power transfer system for a high-speed train,” *IEEE Transactions on Industrial Electronics*, vol. 62, no. 10, pp. 6242–6250, 2015.
- [116] C. P. Basso, *Switch-mode power supplies*. McGraw-Hill Education, 2014.
- [117] A. Lidow, *GaN power devices and applications*. Efficient Power Conversion Corporation, 2021. [Online]. Available: <https://books.google.co.uk/books?id=PfmNzgEACAAJ>
- [118] *TP90H050WS 900V GaN FET in TO-247 (source tab) preliminary datasheet*, Transphorm, Inc., 2019.
- [119] *C2M0045170D silicon carbide power MOSFET C2MTM MOSFET technology N-channel enhancement mode*, Wolfspeed, Inc., 2022.
- [120] D. C. Yates, S. Aldhaher, and P. D. Mitcheson, “Design of 3 MHz DC/AC inverter with resonant gate drive for a 3.3 kW EV WPT system,” in *2016 IEEE 2nd Annual Southern Power Electronics Conference (SPEC)*, 2016, pp. 1–4.
- [121] J. Choi, D. Tsukiyama, and J. Rivas, “Comparison of SiC and eGaN devices in a 6.78 MHz 2.2 kW resonant inverter for wireless power transfer,” in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2016, pp. 1–6.
- [122] —, “Evaluation of a 900 V SiC MOSFET in a 13.56 MHz 2 kW resonant inverter for wireless power transfer,” in *2016 IEEE 17th Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2016, pp. 1–6.
- [123] *C3M0075120J silicon carbide power MOSFET*, Wolfspeed, Inc., 2019.
- [124] C. H. Kwan, J. M. Arteaga, S. Aldhaher, D. C. Yates, and P. D. Mitcheson, “A 600W 6.78MHz wireless charger for an electric scooter,” in *2020 IEEE PELS Workshop on Emerging Technologies: Wireless Power Transfer (WoW)*, 2020, pp. 278–282.

- [125] L. Gu, G. Zulauf, Z. Zhang, S. Chakraborty, and J. Rivas-Davila, "Push-pull class Φ_2 RF power amplifier," *IEEE Transactions on Power Electronics*, vol. 35, no. 10, pp. 10 515–10 531, 2020.
- [126] H. Chireix, "High power outphasing modulation," *Proceedings of the Institute of Radio Engineers*, vol. 23, no. 11, pp. 1370–1392, 1935.
- [127] F.-S. Tsai, J. Sabate, and F. Lee, "Constant-frequency, zero-voltage-switched, clamped-mode parallel-resonant converter," in *Conference Proceedings., Eleventh International Telecommunications Energy Conference*, 1989, pp. 16.4/1–16.4/7 vol.2.
- [128] D. Czarkowski and M. Kazimierczuk, "Single-capacitor phase-controlled series resonant converter," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, vol. 40, no. 6, pp. 383–391, 1993.
- [129] M. Kazmierczuk, D. Czarkowski, and N. Thirunarayan, "A new phase-controlled parallel resonant converter," *IEEE Transactions on Industrial Electronics*, vol. 40, no. 6, pp. 542–552, 1993.
- [130] K. Shinoda, T. Suetsugu, M. Matsuo, and S. Mori, "Analysis of phase-controlled resonant DC-AC inverters with Class E amplifier and frequency multipliers," *IEEE Transactions on Industrial Electronics*, vol. 45, no. 3, pp. 412–420, 1998.
- [131] D. Kawamoto, H. Sekiya, H. Koizumi, I. Sasase, and S. Mori, "Design of phase-controlled Class E inverter with asymmetric circuit configuration," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 51, no. 10, pp. 523–528, 2004.
- [132] Z. Kaczmarczyk and W. Jurczak, "A push-pull Class-E inverter with improved efficiency," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 4, pp. 1871–1874, 2008.
- [133] H. Hu, Y. Li, and Z. Wang, "An improved push-pull Class-E RF tuned power amplifier with low maximum transistor current," in *ASICON 2001. 2001 4th International Conference on ASIC Proceedings (Cat. No. 01TH8549)*. IEEE, 2001, pp. 322–325.
- [134] A. Marinescu and I. Dumbravă, "Using VNA for IPT coupling factor measurement," in *2016 IEEE International Power Electronics and Motion Control Conference (PEMC)*, 2016, pp. 1026–1030.

- [135] D. C. Hamill, "Class DE inverters and rectifiers for DC-DC conversion," in *PESC Record. 27th Annual IEEE Power Electronics Specialists Conference*, vol. 1. IEEE, 1996, pp. 854–860.
- [136] C. Ekkaravarodome and K. Jirasereeamornkul, "Analysis and implementation of a half bridge Class-DE rectifier for front-end ZVS push-pull resonant converters," *Journal of Power Electronics*, vol. 13, no. 4, pp. 626–635, 2013.
- [137] M. Madsen, A. Knott, and M. A. Andersen, "Low power very high frequency switch-mode power supply with 50 V input and 5 V output," *IEEE Transactions on Power Electronics*, vol. 29, no. 12, pp. 6569–6580, 2014.
- [138] W. Liang, J. Glaser, and J. Rivas, "13.56 MHz high density DC-DC converter with PCB inductors," *IEEE Transactions on Power Electronics*, vol. 30, no. 8, pp. 4291–4301, 2014.
- [139] Q.-T. Duong and M. Okada, "Analysis of reactance compensation for eliminating cross-coupling in multiple-receiver inductive power transfer," in *2017 11th European Conference on Antennas and Propagation (EUCAP)*, 2017, pp. 492–495.
- [140] M. J. Mohammed and T. K. Hassan, "Design and simulation of a multi-receiver wireless power transfer system based on transmitter control method," *Journal of Engineering and Sustainable Development*, vol. 26, no. 6, pp. 39–51, 2022.
- [141] G. Ke, Q. Chen, W. Gao, S.-C. Wong, C. K. Tse, and Z. Zhang, "Research on IPT resonant converters with high misalignment tolerance using multicoil receiver set," *IEEE Transactions on Power Electronics*, vol. 35, no. 4, pp. 3697–3712, 2020.
- [142] Z. Dongye, Y. Wang, H. Zhang, and F. Lu, "A load-independent domino IPT system with π -type compensation network," in *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2021, pp. 432–436.
- [143] Q.-T. Vo, Q.-T. Duong, and M. Okada, "Cross-talk mitigation using band-stop filters for multiple-frequency one-to-multiple inductive power transfer," in *2021 15th European Conference on Antennas and Propagation (EuCAP)*, 2021, pp. 1–5.
- [144] Q.-T. Duong and M. Okada, "Maximum efficiency formulation for multiple-input multiple-output inductive power transfer systems," *IEEE Transactions on Microwave Theory and Techniques*, vol. 66, no. 7, pp. 3463–3477, 2018.

- [145] W. Smith and S. Erdman, "A note on the inversion of complex matrices," *IEEE Transactions on Automatic Control*, vol. 19, no. 1, pp. 64–64, 1974.
- [146] B. Polyak and A. Tremba, "Solving underdetermined nonlinear equations by Newton-like method," *arXiv preprint arXiv:1703.07810*, 2017.
- [147] S. Wright, J. Nocedal *et al.*, "Numerical optimization," *Springer Science*, vol. 35, no. 67-68, p. 7, 1999.
- [148] J. M. Arteaga, N. Pucci, L. Lan, and P. D. Mitcheson, "Load characterization in high-frequency IPT systems using Class EF switching waveforms," *IEEE Transactions on Power Electronics*, vol. 36, no. 10, pp. 11 036–11 044, 2021.
- [149] M. Lu and K. D. T. Ngo, "Comparison of passive shields for coils in inductive power transfer," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2017, pp. 1419–1424.
- [150] T. Campi, S. Cruciani, and M. Feliziani, "Magnetic shielding of wireless power transfer systems," in *2014 International Symposium on Electromagnetic Compatibility, Tokyo*, 2014, pp. 422–425.
- [151] J. Kim, J. Kim, S. Kong, H. Kim, I.-S. Suh, N. P. Suh, D.-H. Cho, J. Kim, and S. Ahn, "Coil design and shielding methods for a magnetic resonant wireless power transfer system," *Proceedings of the IEEE*, vol. 101, no. 6, pp. 1332–1342, 2013.
- [152] S. Cruciani, T. Campi, F. Maradei, and M. Feliziani, "Active shielding design for wireless power transfer systems," *IEEE Transactions on Electromagnetic Compatibility*, vol. 61, no. 6, pp. 1953–1960, 2019.
- [153] M. Kavitha, P. B. Bobba, and D. Prasad, "Effect of coil geometry and shielding on wireless power transfer system," in *2016 IEEE 7th Power India International Conference (PIICON)*, 2016, pp. 1–6.
- [154] T. Sensui and H. Koizumi, "Load-independent Class E zero-voltage-switching parallel resonant inverter," *IEEE Transactions on Power Electronics*, vol. 36, no. 11, pp. 12 805–12 818, 2021.

- [155] Y. Komiyama, S. Matsushashi, W. Zhu, T. Mishima, Y. Ito, T. Uematsu, K. Nguyen, and H. Sekiya, "Frequency-modulation controlled load-independent Class-E inverter," *IEEE Access*, vol. 9, pp. 144 600–144 613, 2021.
- [156] Y.-F. Li, "Auto-tuning controller design of Class E inverter with resonant components varying," in *2012 IEEE International Symposium on Industrial Electronics*, 2012, pp. 217–221.
- [157] F. Issi and O. Kaplan, "Design and application of wireless power transfer using Class-E inverter based on adaptive impedance-matching network," *ISA Transactions*, vol. 126, pp. 415–427, 2022. [Online]. Available: <https://www.sciencedirect.com/science/article/pii/S0019057821004183>
- [158] A. Reatti, F. Corti, L. Pugi, M. K. Kazimierczuk, G. Migliazza, and E. Lorenzani, "Control strategies for Class-E resonant inverter with wide load variation," in *2018 IEEE International Conference on Environment and Electrical Engineering and 2018 IEEE Industrial and Commercial Power Systems Europe (EEEIC / I&CPS Europe)*, 2018, pp. 1–6.
- [159] S. Aldhaher, P. C.-K. Luk, and J. F. Whidborne, "Electronic tuning of misaligned coils in wireless power transfer systems," *IEEE Transactions on Power Electronics*, vol. 29, no. 11, pp. 5975–5982, 2014.
- [160] —, "Tuning Class E inverters applied in inductive links using saturable reactors," *IEEE Transactions on Power Electronics*, vol. 29, no. 6, pp. 2969–2978, 2014.
- [161] S. Aldhaher, P. C.-K. Luk, A. Bati, and J. F. Whidborne, "Wireless power transfer using Class E inverter with saturable DC-feed inductor," *IEEE Transactions on Industry Applications*, vol. 50, no. 4, pp. 2710–2718, 2014.
- [162] D. Medini and S. Ben-Yaakov, "A current-controlled variable-inductor for high frequency resonant power circuits," in *Proceedings of 1994 IEEE Applied Power Electronics Conference and Exposition - ASPEC'94*, 1994, pp. 219–225 vol.1.
- [163] Y. Wei, Q. Luo, and A. Mantooth, "Comprehensive analysis and design of LLC resonant converter with magnetic control," *CPSS Transactions on Power Electronics and Applications*, vol. 4, no. 4, pp. 265–275, 2019.

- [164] D. J. Thrimawithana and U. K. Madawala, "A primary side controller for inductive power transfer systems," in *2010 IEEE International Conference on Industrial Technology*, 2010, pp. 661–666.
- [165] S. Lee, J. Lee, E. Noh, T. Gil, and S.-H. Lee, "Load estimation of a series-series tuned wireless power transfer system," in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2019, pp. 4216–4222.
- [166] L. Lan, J. M. Arteaga, D. C. Yates, and P. D. Mitcheson, "A reflected impedance estimation technique for inductive power transfer," in *2019 IEEE PELS Workshop on Emerging Technologies: Wireless Power Transfer (WoW)*, 2019, pp. 45–48.
- [167] B. Keogh, "Power factor correction using the buck topology-efficiency benefits and practical design considerations," in *Texas Instruments Power Supply Design Seminar*, vol. 4, 2010, pp. 1–37.
- [168] C. G. Maennel, "Improvement in the modelling of a half-wave Cockroft-Walton voltage multiplier," *Review of Scientific Instruments*, vol. 84, no. 6, p. 064701, 2013.
- [169] I. C. Kobougias and E. C. Tatakis, "Optimal design of a half wave Cockroft-Walton voltage multiplier with different capacitances per stage," in *2008 13th International Power Electronics and Motion Control Conference*. IEEE, 2008, pp. 1274–1279.
- [170] K. Nagaoka, K. Chikamatsu, A. Yamaguchi, K. Nakahara, and T. Hikiyara, "High-speed gate drive circuit for SiC MOSFET by GaN HEMT," *IEICE Electronics Express*, pp. 12–20 150 285, 2015.
- [171] M. P. Theodoridis and S. V. Mollov, "Robust MOSFET driver for RF, Class-D inverters," *IEEE Transactions on industrial electronics*, vol. 55, no. 2, pp. 731–740, 2008.
- [172] M. K. Kazimierczuk, "Class E tuned power amplifier with nonsinusoidal output voltage," *IEEE journal of solid-state circuits*, vol. 21, no. 4, pp. 575–581, 1986.
- [173] L. Balogh, "Fundamentals of MOSFET and IGBT gate driver circuits," *Texas Instruments–Application report, SLUA618-March*, 2017.
- [174] A. Juhas and L. A. Novak, "Comments on "Class-E, Class-C, and Class-F power amplifier based upon a finite number of harmonics"," *IEEE Transactions on Microwave Theory and Techniques*, vol. 57, no. 6, pp. 1623–1625, 2009.

- [175] H. Jedi, “Resonant gate-drive circuits for high-frequency power converters,” Ph.D. dissertation, Wright State University, 2018.
- [176] H. Jedi, T. Salvatierra, A. Ayachit, and M. K. Kazimierczuk, “High-frequency single-switch ZVS gate driver based on a Class Φ_2 resonant inverter,” *IEEE Transactions on Industrial Electronics*, vol. 67, no. 6, pp. 4527–4535, 2020.