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Microsystem integration and packaging for chip-scale implantable devices.

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Declaration of originality

I herewith certify that all material in this dissertation which is not my own work has been properly acknowledged.

Katarzyna Szostak-Lipowicz

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Abstract

As a consequence of the progress in miniaturisation technology and material science in the late 20th century, there has been a remarkable development in the form factors and technologies applied to biomedical microsystems, such as implantable neural interfaces. Over time implants dimensions have significantly shrunk while simultaneously their complexity-such as the ability to connect to more electrodes, increased.
Notwithstanding these efforts, the promise of fully implantable brain-machine interfacing systems capable of wireless performance over large cortical areas is yet to be accomplished. Challenges in system integration, implant fabrication and packaging are recognised as the key aspects requiring further advancements on the road towards the future of clinical neural interfaces. Particularly for systems composed of multiple distributed implants, where the relation between their number and size is inversely proportional, it is of utmost significance to reduce the packaging size to the minimum while effectively protecting both the device from deterioration and the host tissue from inflammation. In addition to environmental protection, an implant's package must provide reliable interconnections between the interfacing electrodes and electronic modules responsible for data conditioning and processing. As a consequence, the design of autonomous miniaturised neural interfaces faces a set of challenges that need to be addressed to assure a stable long-term performance. These include implant's compatibility with the biological environment, the safety of its Complementary Metal Oxide Semiconductor (CMOS) electronics and wireless communication, as well as a selection of a fabrication process adaptable to mass manufacturing. The underlying aim of this research is thus to investigate the feasibility of CMOS-compatible packaging and integration scheme for distributed mm-scale neural implants, design of a biocompatible hermetic sealing method applicable for chronic applications, and demonstration of a non-toxic approach to achieve repeatable gold-tin alloys for implementation in sensors packaging. The original contributions of this work are summarised as three aspects.

Contribution 1 The development of the structural design, along with the fabrication method and the *proof of concept* realisation of two versions of mm-sized autonomous neural implant based on microwire electrodes. The design considers the need for the device's compatibility with the biological environment, CMOS electronics and RF communication. Initial mechanical structures are fabricated and described in detail, along with the presentation of a method for a microwire integration.

Contribution 2 The development of a repeatable, CMOS-compatible method of hermetic packaging for use in implantable devices. The proposed technique employs silicon to silicon eutectic bonding through gold-tin layers resulting in the average bonding strength of 28 MPa with a bonding yield of 73%. Identification of the preferred geometry aspects from the mechanical stability and reliability perspectives was made by the series of shear force tests, scanning electron microscopy and scanning acoustic microscopy inspections, and immersion tests.

Contribution 3 A method for repeatable, low-hazard, low-volume sequential electrochemical deposition of gold-tin alloys of controllable composition on silicon substrates is developed and optimised to achieve the minimum possible roughness with the best repeatability of deposited layers thickness. This was done by analysing the influence of several electroplating parameters on the grain morphology and deposit thickness deviations across substrates. The proposed technique is based on a commercially available chemistry and does not require strict bath maintenance.

This work proposes the structural design and packaging methods utilisable in the realisation of millimetre-sized, microwire-based implantable neural interfaces, with an emphasis on the importance of package structural integrity, biocompatibility and manufacturability. I envisage that with further improvements, the proposed approach could be employed in the large scale fabrication of distributed implantable neural interfacing devices.

To my family

"Our doubts are traitors,
and make us lose the good we oft might win,
by fearing to attempt."

William Shakespeare, Measure for Measure.

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List of Abbreviations

ALD	Atomic Layer Deposition
BCI	Brain-Computer Interface
BEOL	Back End Of Line
BGA	Ball Grid Array
BMI	Brain-Machine Interface
CE	Counter Electrode
CMOS	Complementary Metal Oxide Semiconductor
CNS	Central Nervous System
DBS	Deep Brain Stimulation
DI	Deionised (regarding water)
DLW	Direct Laser Writing
DSP	Double Side Polished
DRIE	Deep Reactive-Ion Etching
ECoG	Electrocorticography
ECD	Electrochemical Deposition
EDX	Energy-dispersive X-ray spectroscopy
EEG	Electroencephalography
ENGINI	Empowering Next Generation Implantable Neural Interfaces
FBR	Foreign Body Response
FDA	U.S. Food and Drug Administration
HF	Hydrofluoric Acid
IC	Integrated Circuit
IMC	Intermetallic Compound
IMD	Implantable Medical Device
IPA	Isopropyl Alcohol
LFP	Local Field Potential
LTCC	Low Temperature Co-fired Ceramics
MEA	Micro Electrode Array
MEMS	Microelectromechanical Systems
MHRA	Medicines and Healthcare products Regulatory Agency
MMEA	Michigan Multi-Electrode Array Systems
MSA	Methanesulfonic Acid
MWA	Microwire Array

NI	Neural Interfaces
PBS	Phosphate Buffered Saline
PCB	Printed Circuit Board
PDMS	Polydimethylsiloxane
PECVD	Plasma Enhanced Chemical Vapour Deposition
PNS	Peripheral Nervous System
PVD	Physical Vapour Deposition
RF	Radio Frequency
RPM	Revolutions Per Minute
RoHS	Restriction of Hazardous Substances
SAM	Scanning Acoustic Microscopy
SEM	Scanning Electron Microscopy
SoC	System on Chip
TSV	Through Silicon Via
UEA	Utah Electrode Array
WE	Working Electrode

1. Introduction

The ability to connect, read into and understand the brain, the most complicated organ of the human body, has long fueled the ambition of humankind- the idea to control surroundings with one's thoughts has been the staple of many science fiction films and novels. This nature-engineered system works in a closed feedback loop with the entire body in real-time and is capable of processing in a massively parallel and distributed way. However, despite many years spent on the research attempting to explain the brain nature, it is yet to be fully understood. Currently available brain recording technologies lack enough spatiotemporal resolution and focus mainly on the electric part of the neuronal activity.

Owing to the partially electrical character of a nervous system, the engineering knowledge about electric signals can be utilised to design neural interfaces - miniaturised devices that can connect directly to the brain. Within the interdisciplinary field of Brain-Machine Interfaces, various miniaturised devices are developed to observe and influence brain activity in great detail, thus opening a potential to improve the understanding of neuronal processes, treat various neurological conditions or even expand the sensory capabilities of healthy individuals. These devices, also labelled as electroceuticals, are believed to enable more effective treatment for many neurological conditions than standard pharmacology-based solutions, which because of a blood-brain barrier, often fail to deliver long-lasting results.

A major challenge is to scale down the BMI technology to enable clinically successful, detailed neuronal recording capability using minimally invasive, miniaturised wireless devices that would work effectively over an extended time. The signals of the interest are very local, faint and easily hindered by scarring processes, while devices aimed to record from them remain much larger and suffer reliability issues. As a result of reactions occurring at the probe-tissue interface, implants' stability, and even surgical methods, neural interfacing devices suffer from a progressive worsening of selectivity and sensitivity to neuronal signals, as expressed in a decrease in the signal to noise ratio and electrodes' impedance. Because of a relatively large size of currently available devices, the implantation site is often constrained to specific areas, thus providing only limited information about the neuronal activity. Through the extensive research and innovation, new paradigms can be formed that in the future may constitute new ways of accessing neuronal activity, helping to decode mysteries of the brain.

1.1. Motivation

Throughout history, humans have always sought to improve their well-being and prolong their life. Over the last century, whenever a generation was tormented with a specific disease, either a cure, treatment or a deep understanding of its origins was soon established. Thanks to the myriad of accomplished scientific marvels, today, we can benefit from access to highly specific pharmaceuticals, vaccines, transplantology, implantology or gene therapy. As a result of that, the human population rapidly ages, with a median age increasing by eight and a half years since 1970 [1]. Today, one of the health threats presented to our generation is neurological diseases.

It is estimated that as populations are getting older, health problems of neurological nature are to become highly common, thus causing substantial strain and an economic impact on health care and social services [2]. In India, compared to thirty years ago, the burden of neurological disorders has doubled [3]. Whereas in the United Kingdom, neurological disorders affect over twelve million people in total, twenty per cent of which being progressive conditions causing cognitive, motor and sensory dysfunctions and a decrease in the overall quality of patients' lives [4]. This is because disorders affecting the nervous system are one of the most difficult to treat effectively with pharmaceuticals, as the blood-brain barrier limits entry to the most chemical compounds, and surgical interventions are highly limited. A large part of that patient population could be treated with the use of implantable neural recording and stimulation devices, which have been found beneficial in treating and relieving symptoms of many neurological conditions, including epilepsy, Parkinson's disease, dystonia, tremor, tinnitus, stroke, pain and others. What is more, due to the small number of neural data acquisition methods offering a high resolution of recording in spatial and temporal domains, the essential information on how and where the brain processes information or about the workings and origins of many neurological diseases is still not complete. Enabling a better understanding of brain functions and related neuronal activity would require a considerable increase in the number of concurrently observed neurons in the real time without signal deterioration. The limits of the current state-of-the-art neurotechnologies allow for the recording and manipulation of neural activity at the interface volumes down to few tens of neurons, with the minimum spatial resolution of several microns and sub-millisecond temporal resolution. However, for an average representative implantable neural device, the values of the abovementioned spatiotemporal limitations are still at least an order of magnitude larger.

In these circumstances, today, understanding the human brain is widely considered science's final frontier. Willingness to aid people suffering from a vast number of neurological conditions triggered the expansion of the Brain-Machine Interfaces (BMI) field. It is currently enjoying much interest in the scientific community, with research ranging from motor

control fundamentals to new device technologies. In North America alone, the neuroprosthetics market share is estimated to reach over ten billion dollars by 2023 [5]. Over the last couple of years, the potential of BMIs has also been noticed by the industry, with high profile figureheads and big tech leading new commercial ventures. Examples that have received significant investment and a public interest include Elon Musk (Neuralink), Mark Zuckerberg (Facebook/CTRL-labs), Bryan Johnson (Kernel) and GSK/Google (Galvani Bioelectronics). These endeavours are now inspiring new translational efforts to develop technology to communicate directly with the nervous system for a therapeutic benefit. Success stories of neuromodulating devices that are now routinely bypassing effects of neural disorders for which there was no treatment available a few decades ago, such as DBS probes in Parkinson's disease with over 200k devices in use today, or cochlear implants in deafness with over 500k devices now in use, give hope to the future of BMIs. However, the majority of research efforts still battle to cross the gap from valuable investigation tools to established medical devices. This circumstance is particularly evident for systems belonging to the domain of intracortical neural interfaces [6, 7]. To become widely available in clinical applications, brain-computer interfaces require to be evidenced by the data proving their safety and efficacy. To make it happen, further progress in the devices scalability and chronic stability, as well as reliability of recordings over clinically relevant time frames, is required. [8].

Some of the obstacles still standing in the way to achieve reliable BMIs are implants packaging, reliability and integration with electronics. Despite achievements in the miniaturisation technology leading to size reduction of electronic components, minimum-size system packaging still requires significant developments. Often overlooked, it has become one of the bottlenecks slowing down the pace of BMIs progress.

1.2. Research objectives

The main aim of this research is to explore comprehensive manufacturing and packaging schemes for a novel type of neural interface. By leveraging advancements in material science, electronics and signal processing, the packaging approach will be capable of overcoming the shortcomings of the majority of up-to-date microprobe technologies. In particular, it aims at establishing a method for reliable, hermetic and small footprint sealing of CMOS devices in implantable applications. The method should use bio- and RF-compatible materials to enable wireless communication and improve electronics integration in future distributed neural implants. The realisation of such objectives would aid the development of smaller, more intelligent, wireless brain interfacing implants. That way, the necessity for wired connections could be eliminated and the need for multiple surgical interventions minimised, thus improving the chances for both patients recovery and devices' chronic performance. To achieve this, the following research objectives have been identified:

- **Development of CMOS-compatible methods for the chip-scale hermetic sealing.**
  To investigate a method for wafer- or chip-scale hermetic micropackaging for CMOS devices in implantable neural interfacing applications. This includes materials and techniques compatible with the living biological environment and integrated circuit technologies under minimum footprint constraints. Investigation on optimum features and parameters for process reliability and repeatability must be simultaneously conducted.

- **Investigation of implantable sensor module architectures**
  To explore approaches for creating implantable smart sensor modules that will be capable of seamless integration with external units, such as microelectrode arrays, and will support the wireless exchange of power and data. An assessment of limits of geometric constraints and materials applicability must be conducted. This can be done by modifying existing chip-stacking methods and should be verified in terms of verifying mechanical performance and large-scale fabrication availability.

- **Assessment of biocompatible solder deposition methods**
  Investigate repeatable, controllable, eutectic alloy deposition methods that might allow a small-scale, low-maintenance production using low-hazard materials. This includes ensuring grown layers' biocompatibility by evaluating the deposition processes toxicity footprint.

1.3. Thesis Outline

This thesis is structured as follows:

- **Chapter 1**, *"Introduction"*, provides the foreword to the research on neural interfaces, motivation for the undertaken research and summarises the thesis' main objectives.
- **Chapter 2**, *"Fundamentals of implantable devices and neural interfaces: challenges and current solutions"*, introduces the field of implantable medical devices with a specific focus on neural interfaces, followed by the basis of nervous system function and the fundamentals of a neural signals recording. Principal intracortical device types are described, along with challenges associated with the IMDs development, emphasising difficulties of the CMOS integration and protection in implantable conditions.
- **Chapter 3**, *"Design of a microwire-based mm-scale cortical recording implant"*, commences with the review of structural design considerations for implantable neural devices; next, it reviews packaging requirements and constraints imposed by the ENGINI project. It then presents two versions of microfabrication and assembly strategies for the microwire-based neural implant. A comparative review of two iterations is provided, along with an assessment of microwires integration via solder spheres reflow.
- **Chapter 4**, *"Au:Sn bonding for applications in implantable neural devices micropackaging"*, first discusses wafer-level joining methods applicable in the packaging of miniaturised sensors and reviews them considering CMOS compatibility and implantable devices sealing suitability. The design of the gold-tin-based micro packaging approach is then proposed and discussed, along with an analysis of the most critical seal design parameters identified. An assessment of packages hermeticity and mechanical reliability is then described and discussed.
- **Chapter 5**, *"Sequential electrochemical deposition for Au:Sn eutectic formation"*, discusses and evaluates gold-tin alloy sequential electroplating process using low hazard materials for the packaging of biomedical devices. A summary of common Au:Sn alloy deposition techniques is described, along with the basics of electrochemical deposition procedure. An examination of the most layer morphology-influential deposition process parameters is presented, together with an assessment of deposits cytotoxicity.
- **Chapter 6**, *"Conclusions"*, concludes the research undertaken in this thesis, highlighting original contributions. The directions for further work are outlined, and final thoughts about the future directions of neurotechnology are provided, with a particular focus on devices' packaging and fabrication.

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2. Fundamentals of implantable devices and neural interfaces: challenges and current solutions

2.1. Implantable medical devices

Integration of a human body with foreign objects for either ornamental or restorative purposes is not new and has been present for thousands of years - the earliest eye and foot prostheses can be dated back as far as 3000 BCE, while the first dental implants using organic materials such as shells and bamboo pegs date back to 2000 BCE [3, 4]. With the steady progress in technology and material science, both prosthetic devices and implants became more advanced and sophisticated [5]. Whereas prostheses primary purpose is a passive replacement of missing body parts, implants can also provide supportive, regenerative, drug delivery or monitoring purposes. As opposed to prostheses which are often removable, implantable devices after being fully or partially placed in the body are aimed to remain there for more extended periods.

An implant design is a non-trivial task, given the unique environment of the human body. Implanted devices face conditions of continuous movement, moisture and warmth, all amongst a multitude of chemical and electrical reactions. Nevertheless, since the first commercial pacemakers were introduced in the 1960s, the implants market boomed and has become one of the pillars of modern-day healthcare treatments [6]. The great success of implantable cardiac devices, such as pacemakers and cardioverters-defibrillators paved the way for implants applications in other body areas, including the nervous system. Rapid progress in electronics technology and material sciences caused an explosion in devices being offered and improved every year, much to the needs of a growing number of people in need of them. It is estimated that nowadays, even 10% of the population lives with some form of an implantable medical device, active such as cardiac pacemakers or passive such as hip and knee prostheses, the number which is assumed to grow bigger as the population ages [7].

A portion of the material presented in this chapter has been published in [1, 2]

A particular subsection of implantable medical devices is active implants, which require separate energy sources for operation, such as pacemakers or cochlear implants. Active implantable devices must undergo the most rigorous regulatory controls to become available for therapeutic applications. From the regulatory perspective, medical devices can be broadly divided into different groups, called classes, based on the risk they impose on the patient. The process of the product approval for low- and medium-risk (*Classes I and II,*) medical devices is generally faster, more accessible and does not always require the involvement of a notified body (such as MHRA or FDA). *Class I* medical devices are of the most straightforward design and the least dangerous, such as bandages, stethoscopes or medical gloves. Their market clearance requirements are also the simplest and often include only general conformity controls declared by the manufacturer. For *Class II* medical devices, such as blood pressure kits or infusion pumps, general controls are no longer adequate as they are more complicated and can pose a moderate risk of illness and injury. Market approval of *Class II* devices is more demanding and requires notified body assessment and/or CE marking in Europe, and FDA clearance in the USA. As compared to *Class I* devices, here, the amount of data that needs to be provided to prove devices' safety is larger, and the time it takes to be cleared on the market is significantly longer. Implants are considered *Class III* medical devices and, as such, are considered to have the highest, possibly lethal risk for patients. Because of that, they must undergo rigorous safety and efficacy assessments and risk minimising strategies involving systematic reviews, clinical trials and lifetime monitoring - malfunction of *Class III* medical device is unacceptable. Because of that, the approval process of *Class III* medical devices is very costly and takes several times longer than for lower-class medical devices, often reaching years-timeframes.

After a period of early adaptations, nowadays, essentially all of used active implants contain some electronic circuitry or microelectromechanical devices to sense or stimulate surrounding tissues. Despite the progress of technology, most implants still evoke some level of hostile, foreign body response, limiting their performance. Therefore, advancements in the device's packaging, power supply, and wireless communication must be made to catch up with the miniaturisation progress and improve seamless body integration.

Figure 2.1 shows a limited overview of current implantable medical devices implantation sites in humans. The one implantation area which has gained much interest in recent years, while being one of the most challenging to integrate with implantable medical devices, is the nervous system and brain.

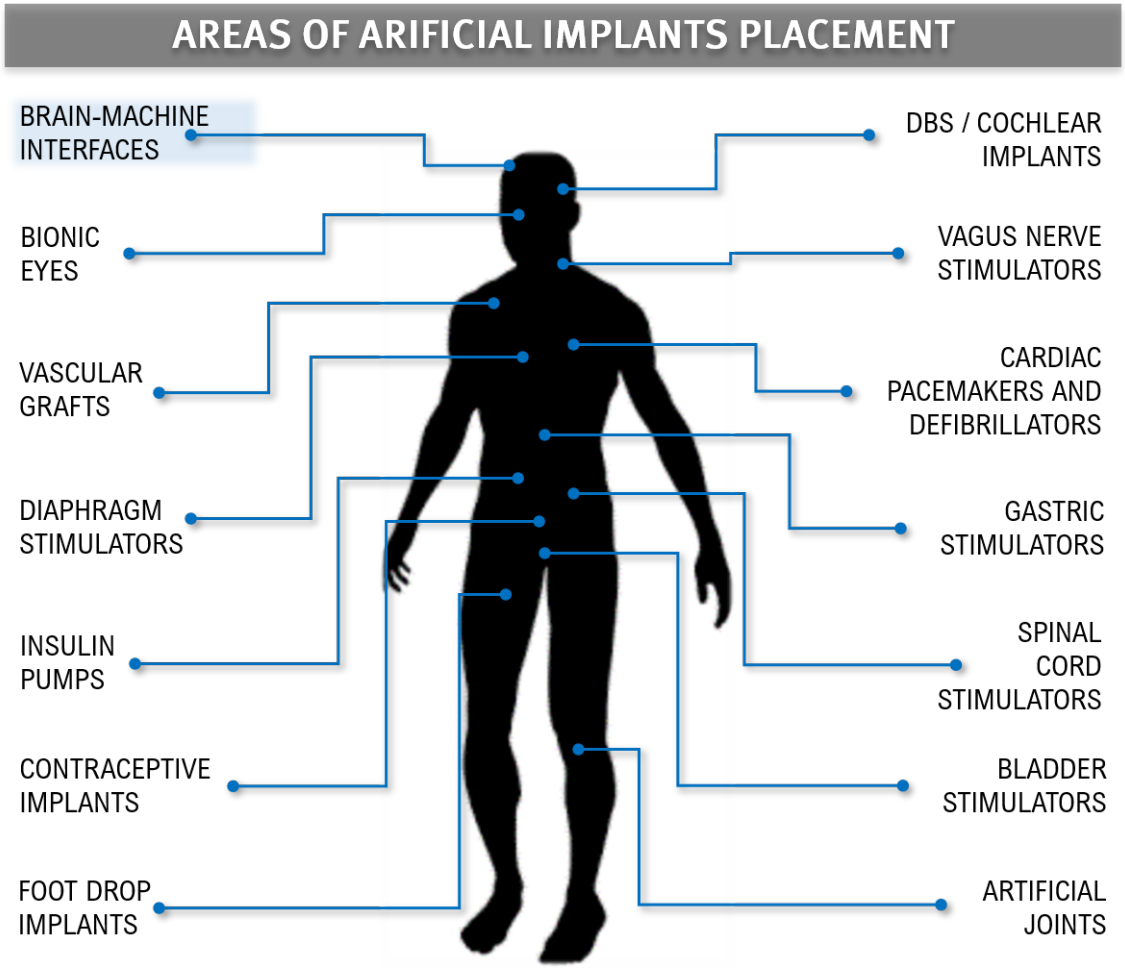


Figure 2.1.: Overview of currently employed or researched human body implantable medical devices and their approximated implantation sites.

2.2. Nervous system and the basics of brain-computer interfacing

2.2.1. Nervous system

The nervous system is structurally and functionally the most complex system of the human body. It is an intricate structure consisting of nerves and highly specialised cells called neurons that transmit signals between different body parts. Essentially, the nervous system controls all body functions, operating as electrical wiring - conducting stimuli from the sensory receptors to the brain and spinal cord and impulses back to other body parts. The nervous system is made up of several subsystems that work together with the rest of the body. Structurally, we can distinguish the central nervous system (CNS) and peripheral nervous system (PNS) (Figure 2.2).

The central nervous system consists of the brain and spinal cord. It is the organism's control centre that receives, analyses and processes information from both internal and external environment, sends responses back to the organs executing the commands, and is responsible for mental activities such as association, memory or learning. CNS is built by specifically arranged neuronal clusters - the majority of neuronal cell bodies make up grey matter, whereas white matter is composed of myelinated axons found in the deeper brain tissues. Being the control centre for the body's vital functions, the central nervous system must be exceptionally well protected against injuries and external factors. The protection is provided threefold: by bone cover consisting of a skull and spinal canal, cerebrospinal fluid, and three connective tissue membranes called meninges- dura mater, arachnoid and

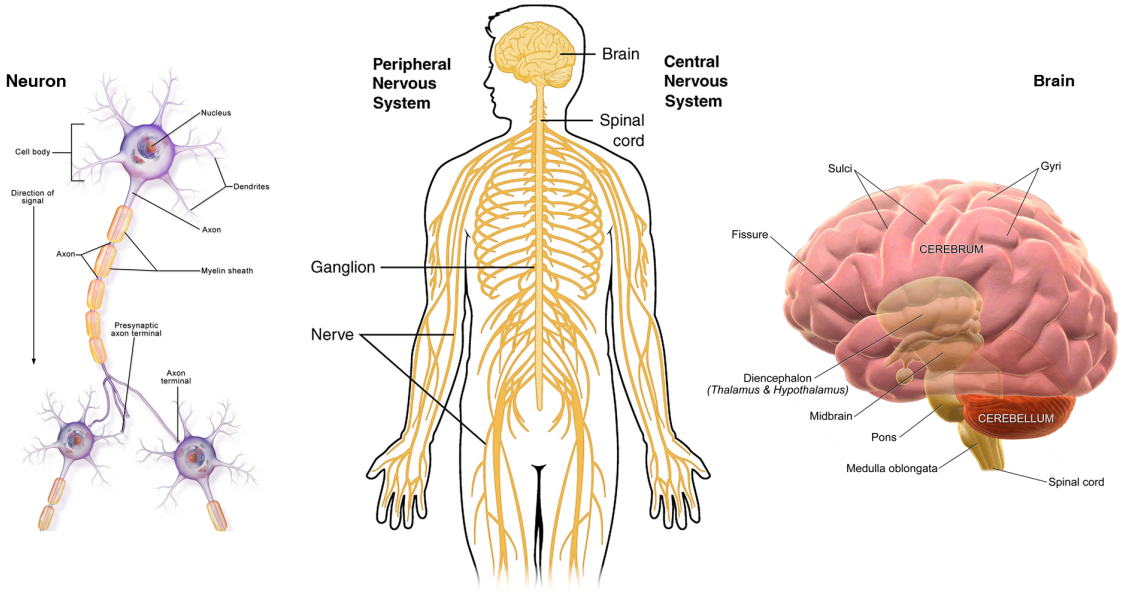


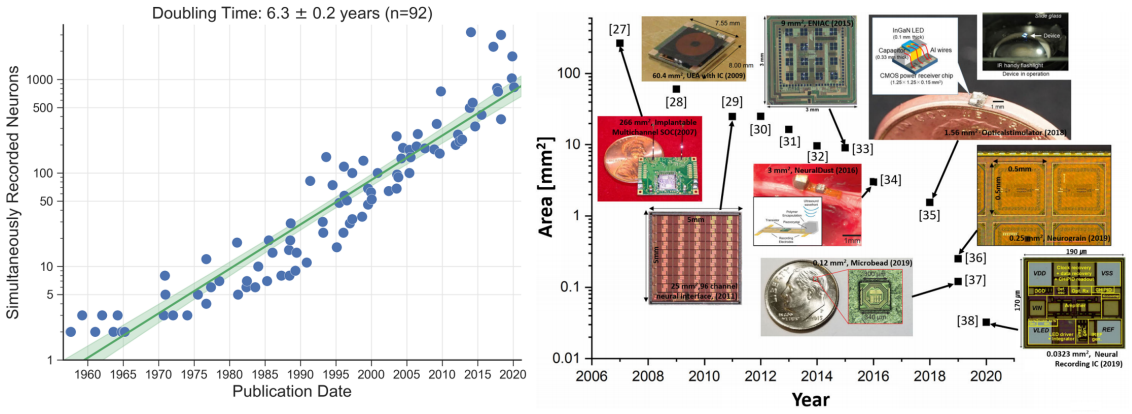
Figure 2.2.: Overview of the human nervous system with the anatomy of a multipolar neuron (left), brain (right) and representation of central and peripheral nervous systems (centre).

pia mater. The peripheral nervous system consists of spinal and cranial nerves with their roots and branches, neuromuscular junctions and peripheral nerves. The purpose of PNS is to provide information exchange between the central nervous system and the rest of the body's organs and tissues. PNS can be further divided into the autonomic nervous system (ANS), providing nerve connections to major organs, including heart, lungs, stomach and majority of the digestive system through the vagus nerve, and somatic nervous system (SNS) of voluntary character, which primarily consists of motor nerves.

The basic computational unit of the nervous system is the neuron. Neurons signal to one another using chemical neurotransmitters that lead to the modulation of ion channels. This activity can be observed and modulated externally electrically, e.g. by using electrodes to translate ionic currents in tissue to electronic currents in external devices. Tree-like neuron's shape is an expression of their adaptation to signal reception and transmission. Neurons contain several short, highly branched protrusions, called dendrites, which carry the information between nearby neurons to the cell body. The most extended, slender projection of the cell body - axon-transmits the action potential impulse to other neurons, muscles or glands.
Neurons connect to each other by synapses, areas where presynaptic axon terminals connect to postsynaptic neuron's dendrites. The transfer of information takes place in the synaptic cleft, an area between surrounding neuron's projections, where an impulse is being passed in the process of electrochemical neurotransmission. When the electrical impulse reaches the axon's terminal, chemicals called mediators and neurotransmitters are secreted into the synaptic gap. They bind to the receptors at the receiving cells membranes, which causes a rise in membrane potential and thus travel of rapid electrical impulse through the axon towards the neighbouring synapses.

2.2.2. Fundamentals of neural recording

Neural interfaces, as the name suggests, interact with neuronal tissue in close proximity through the detection or application of electric potentials to restore compromised motor or sensory functions, and hence are often referred to as neural electrodes, neural probes, or neuroprosthetics [8].
Foundation for the BMI field as we know it today dates back to the middle-18^{th} century and the works of Italian physicist Luigi Galvani who was the first to discover the link between electricity and biological tissues, and Czech anatomist Purkinje, who discovered neuron body in 1837. Their pioneering work sparked an ongoing interest that ultimately, in the early 20^{th} century, led to the discovery of the relation between electrochemical signals and brain activity. It was German psychiatrist Hans Berger, who, in 1924, first discovered and measured brain electrical activity using crude silver wire electrodes, what later led him to develop the electroencephalography method. The foundations for modern electrophysiology were laid with the first animal studies carried out by Eberhard Fetz in the late

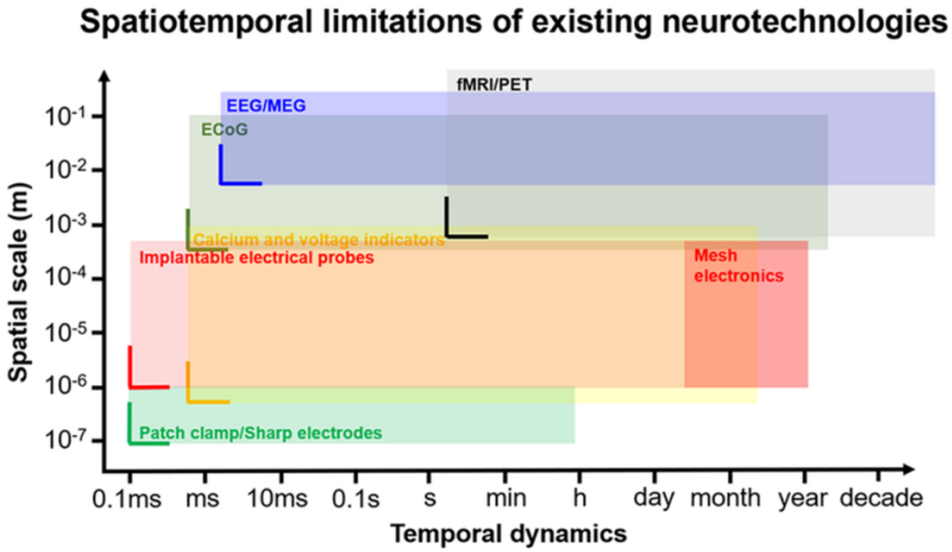


a) b)

Figure 2.3.: Progress in BMI field. a) Exponential growth in the number of recorded neurons over the years [14] b) A time line of recording technologies shows the decrease in size of the devices[15].

1960s, using tungsten wire electrodes [9]. Soon after, in 1973, the term Brain-Computer-Interface (BCI) was coined as a definition for devices that record from the nervous system and use that signal for machine or computer communication [10]. Ever since, the research is focused on a better understanding of neuronal activity and developing new interfacing solutions, which with time became smaller, implantable and more accurate (Figure 2.3). Today, the smallest, single channel, state of the art implants in research use can be as small as several hundred microns and use ultrasonic or optical links as a mode of communication [11, 12, 13]. What is more, advances in microfabrication and ultrafine features processing allow to produce hundreds of small recording

The interfacing quality of neural interfaces highly depends on the distance from the signal source, structure and geometry of the measuring probe, mechanical forces at the tissue-electrode interface, as well as the extent of biological and chemical mechanisms occurring in the vicinity of the implantation site [1].
One way to classify a vast number of brain interfacing technologies presented to date is by the level of their invasiveness and the type of signal they acquire. Over the past seventy years, several different methodologies for neural recording varying in technology, recording resolution, and invasiveness have been proposed, including electroencephalography (EEG), electrocorticography (ECoG) arrays, depth probes, and intracortical microelectrodes (Figure 2.5). Several neural signals sources are useful in brain-machine interfacing, which can be executed using different methods offering various spatiotemporal limitations (Figure 2.4). Electroencephalography is the only truly non-invasive technique using transcranial recording and stimulation employing low-resolution EEG signals. It is considered the least accurate but the easiest to set up and the most cost-effective. The recorded signal is a smoothed, averaged and attenuated version of LFPs originating in large cortical areas be-



Neuroimaging method	Activity measured	Direct/ Indirect Measurement	Temporal resolution	Spatial resolution	Risk	Portability
EEG	Electrical	Direct	~0.05 s	~10 mm	Non-invasive	Portable
MEG	Magnetic	Direct	~0.05 s	~5 mm	Non-invasive	Non-portable
ECoG	Electrical	Direct	~0.003 s	~1 mm	Invasive	Portable
Intracortical neuron recording	Electrical	Direct	~0.003 s	~0.5 mm (LFP) ~0.1 mm (MUA) ~0.05 mm (SUA)	Invasive	Portable
fMRI	Metabolic	Indirect	~1 s	~1 mm	Non-invasive	Non-portable
NIRS	Metabolic	Indirect	~1 s	~5 mm	Non-invasive	Portable

Figure 2.4.: Spatiotemporal characteristics (reproduced from [16]), and the summary of currently existing neurotechnologies (reproduced from[17]). The X and Y-axis of the graph represent spatial and temporal resolutions, whereas the extent of each shaded box shows each technology's spatiotemporal span.

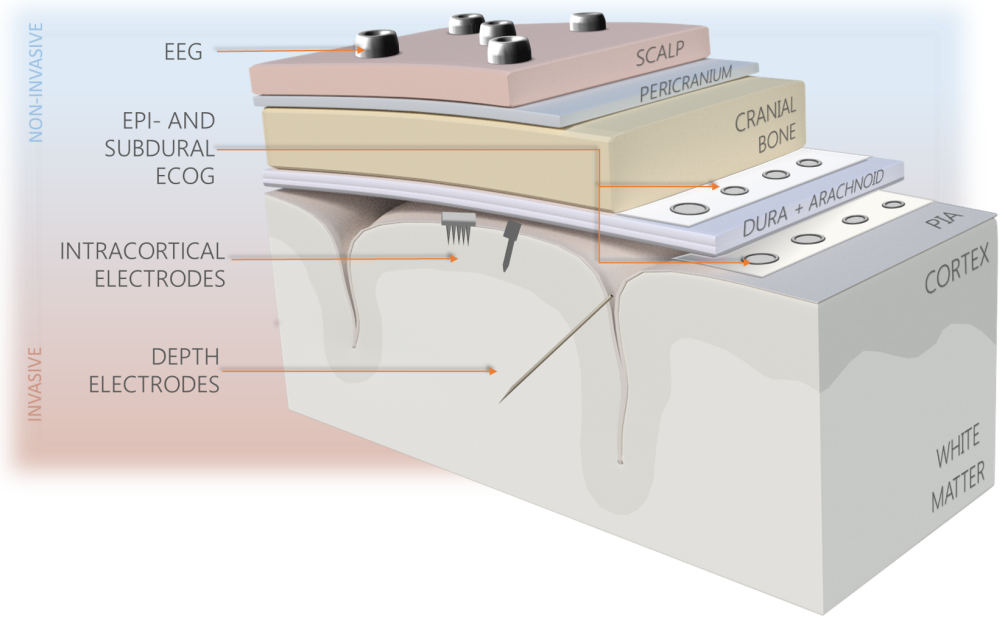


Figure 2.5.: Types of brain interfacing electrodes and their location in the reference to the brain. Less invasive systems (blue background) provide recordings of lower resolution in comparison to intracortically-implanted electrodes.[1].

low electrodes and provides little information about individual neuronal behaviour. The frequency bandwidth of the EEG signal is between 0-100 Hz. Electroencephalography setups typically involve head caps equipped with many small metal electrodes, some of which (wet electrodes) require special conductive gels to improve the quality of signals acquired from the scalp's surface.

More invasive BMI approaches which require placement surgery are epi- and subdural electrocorticography arrays. ECoG is a middle ground recording technique from the perspective of invasiveness; whereas it does require craniotomy to collect signals directly from the brain surface, it does not involve tissue penetration. ECoG arrays are soft and flexible to conform to the brain folds, with a regular grid of Pt-Ir or stainless steel electrodes. The bandwidth of ECoG signals ranges from 0 to 500 Hz. ECoG recording offers better spatial resolution than EEG; however, its use is limited to acute intra- and extraoperative diagnostic applications. Lastly, penetrating intracortical BMI electrodes provide better recording quality than less invasive technologies, as they can record different signal types and offer the best spatial and temporal resolutions. They pick up the neuronal signals from few millimetres deep into the cortical grey matter. When an invasive, conductive microelectrode is implanted within the cortex, neuronal activity can be picked up in the form of higher frequency single or multi-unit activity coming from one or few local individual cells; or as a low-frequency averaged sum of signals from within the volume of the tissue, so-called local field potentials (LFP). Spikes can be recorded from neuronal clusters (multi-unit activity) with signals bandwidths in the 300-25000 Hz range, whereas local field potentials

are low-frequency components of the signal and are in 0.1-300 Hz frequency range. Single unit activity recordings can be obtained by an analysis of recorded multi-unit activity data, for example by using spike-sorting algorithms [18]. The significant disadvantage of intracortical probes' use is their limited longevity resulting from a high degree of invasiveness and tendency of progressive worsening of recorded signal quality. To date, none of the probes developed is capable of completely overcoming the long-standing effects of foreign body reaction, despite a variety of materials, shapes, and sizes used [19, 20]. It is believed that reactions occurring at the probe-tissue interface, implant characteristics, and the quality of the initial implantation procedure influence the performance consistency; however, their mutual relations are not comprehensively explained.

In addition to the complex electrical characteristics of the brain and the nature of an electrochemical interactions between the implanted material and the neuronal tissue, the quality of obtained recordings highly depends on the electrode's electric performance. Aside from the signal-to-noise ratio value, the most prevalently used electrode characterisation parameter is the recording site impedance value at 1 kHz, which to some extent is believed to reflect the recording efficiency. It is estimated that the resistance in the range of at least 40-150 kΩ is necessary to enable sensitivity in detecting a single-unit action potential, while electrode's impedances greater than 5 MΩ overpower neural signals recordings [21, 22]. The one approach to address this issue is to retain micrometric recording sites but increase their effective geometrical surface area by roughening, or functionalisation with nanostructured materials [23]. However, it should be noted that impedance changes are closely related to various non-electrode related factors potentially introducing error, such as blood flow, local pressure, movements, and tissue resistivity. Hence, impedance characterisation should be treated more as an indirect monitoring instrument. Instead, signal to noise ratio parameter provides a good indication of the implant's electrical performance *in vivo*.

Focusing on single and multi-unit recordings requires minimal recording sites of large signal to noise ratio and low impedance, that need to be located close to the source neurons. In practice, a suchlike arrangement is difficult to sustain over extended periods because of changes in the local cellular architecture, non-continuous neuronal activity, body fluids, and the electrode, which undergoes some limited biofouling and degradation with time. At the same time, LFP signals are generally easier to record (i.e. LFP signals are often observable in the absence of single-unit activity) and have been shown to contain useful information while not being as affected by structural changes in the local cellular environment [24]. Recording of local field potentials is not constrained by size or neuron accessibility requirements, as signals are generally more spread within the tissue and can be recorded as far as a few hundred microns up to centimetres away from their source and through the glial encapsulation [25].

2.3. Overview of Intracortical Brain Interfacing Technologies

Overall, intracortical neural interfacing systems consist of three main functional elements groups: implanted probe body containing recording sites (direct cortical interface), electronic circuitry providing data processing and power management and communication interface connecting the other two. Tissue interfacing units, commonly referred to as microelectrodes, are in direct physical and electrical contact with neural tissue and can be of various profiles, typically in the form of single or multi-stem arrays of long, conductive, high aspect ratio structures protruding from the implant's body. Usually, electrodes resemble slim, pointed, millimetres-long stems on which recording electrodes are located-either one at the distal end or multiple along the entire length of the device. The materials of which probes are made highly influences devices performance and structural integrity [26].

The type of the neural electrodes can be divided into three broader categories based on the primary material used for their fabrication: two-dimensional multisite electrode arrays and three-dimensional multi-electrode arrays fabricated on planar rigid substrates (further referred to as *micromachined probes*); primarily planar multisite probes based on soft polymer layers and microwire-based electrode arrays.
A brief comparison between the leading three technologies based on their characteristics, recording capability and fabrication methods can be found in Table 2.1. Fabrication and packaging of any neural interfacing electrode is a time-consuming process requiring several processing steps, presented in a great brief in Figure 2.6, with the distinction between probes based on different electrode types.

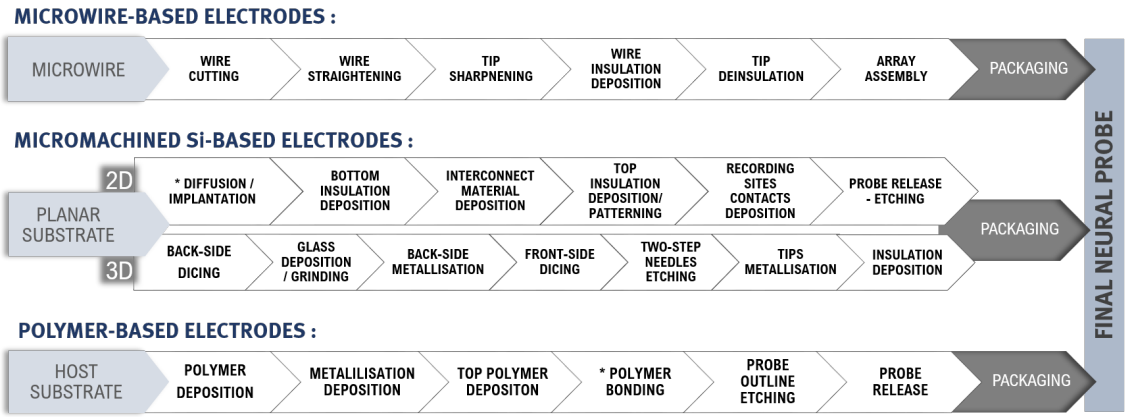


Figure 2.6.: General, exemplary fabrication procedures employed in the formation of three main neural implants' types: microwire electrode-based, micromachined silicon electrode-based, and micromachined polymer electrode-based probes.

Implantable neural interfaces come in a variety of shapes, sizes and materials. For the purpose of the given assessment, the discussion will not cover epicortical or deep-brain electrodes. Instead, it will focus on miniature, intracortical implants, which represent technologies competitive to the scope of the ENGINI project, the main application of which is targeting the motor cortex for BMI.

Table 2.1.: Summary of three main neural interfacing microelectrodes technologies.

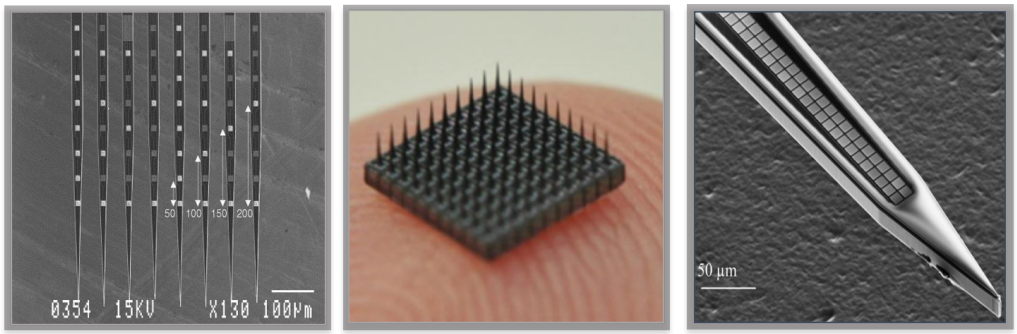
		WIRE – BASED PROBES	MICROMACHINED SUBSTRATE- BASED PROBES		POLYMER-BASED PROBES
			3D-multielectrode arrays (Utah Electrode Array)	2D- multisite arrays (Michigan Electrode Array)	
MATERIALS	Substrate	Plastic or ceramic connectors , Alumina, PCB	Silicon, Stainless steel, Platinum	Silicon, Silicon-on-insulator, Semiconductors, Glasses, Alumina	Host: silicon/glass wafer, Structural: Polyimide, BCB, SU-8, PTFE, PDMS, Parylene, LCP
	Conductors	Thin wires of 10 - 200 µm diameter W, Pt, Pt-Ir, Au, Stainless steel, Eligiloy, Nichrome, Conductive polymers	Au, Pt, Pt-Ir	Au, Pt, Pt-Ir, Ir, metal silicides, polysilicon, conductive polymers,	Cr/Au, conductive polymers
	Isolation	PTFE, Parylene-C, Polyimide, PMMA, Epoxy, Glass, S-isonel	Glass, Silicon oxide, Parylene-C, Polyimide, Silicones	Silicon oxynitride, Silicon nitride, Silicon oxide, Glass, Polyimide, Silicones, Parylene-C,	Same as the substrate
FEATURES		Discrete-wired arrays Layered-arrays Wire bundles Single wires	Three-dimensional needle electrodes One recording site per needle	Planar multisite electrodes Multi-shank, multisite designs	Planar flexible probes 3D thermoformed probes Multisite designs
FABRICATION METHODS		Handmade assembly Electrolytic etching Ultrasonic bonding	CMOS/MEMS micromachining Dicing Wire electrical discharge Flip-chip bonding	CMOS/MEMS micromachining	CMOS/MEMS micromachining Laser structuring Moulding Thermoforming Flip chip, thermal bonding
RECOR-DINGS		Acute and chronic up to 78 weeks in humans, rodents, primates	Acute and chronic up to 52 weeks in humans, rodents, primates	Acute and short up to 18 weeks in rodents, primates	Acute and short up to 8 weeks in rodents, primates
CHARCTERISTICS		Long-lasting Well- established Small dimensions Accessibility to deep neuronal structures Simple and non-expensive Reproducibility and implantation accuracy problems	Approved for human trials High selectivity in recording/stimulation Stiff Large tissue damage upon implantation Integration difficulties	Freedom of design Great dimensional control Microfluidics integration possibility On-chip electronic circuitry integration Planar electrode sites Easily fractured	Flexible and conformal to the tissue Microfluidic integration possibility Compatible with CMOS/MEMS fabrication methods High-temperature sensitive Integration difficulties Implantation problems Non – hermetic

2.3.1. Micromachined probes

Micromachined microelectrodes are the biggest and the most diverse group of penetrating neural probes. This type of electrode technology offers great freedom in design and high precision over dimensions and selectivity, allowing an increase in the number of contacts per probe and large-scale parallel fabrication of multiple probes. Manufacturing is typically carried out in highly controlled cleanroom environments, which is desirable for the quality of medical devices. Microfabrication of neural electrodes based on micromachining techniques requires the use of different materials for substrate, electrical contacts and passivation layers, unlike in wire technology, where the same wire serves as both the substrate and electrical contact material. Substrate materials include mostly silicon and silicon-on-insulator wafers; however, glasses and ceramics are also found.

A variety of two and three-dimensional architecture designs using several bulk materials and thin-film coatings have been introduced and examined for periods as long as 81 and 300 weeks in non-human primates [27, 28]. The major advantage of micromachined BMIs is the ability of multiple recording sites over a small area, providing important insight about neural activity spatial representation, enhancing the identification of the exact origin of recorded signals. Typically, most silicon-based neural microelectrodes designs are either examples or modifications of two-dimensional multisite Michigan electrode arrays (MMEAs) or three-dimensional multi-needle Utah electrode arrays (UEAs).

The first proposed silicon-based intracortical probe was the planar Michigan electrode array based on tapered, 15–50 μm-thick, 30–50 μm-wide silicon stem with multiple metal recording sites along (Figure 2.7 a) [32]. Electrode's geometry is determined entirely by photolithography, providing unique design and customisation possibilities. As a result of



a) b) c)

Figure 2.7.: Examples of neural microelectrodes fabricated with micromachining methods on silicon substrate: a) Michigan electrode –style 64-channel planar probe [29], b) 10x10 Utah electrode array [30], c) 1000-channel close-packed silicon microelectrode [31].

their planarity and fabrication process compatibility, probes can be integrated with IC circuits, microfluidic, and micromechanical structures. The length of the probe's system depends on the application and varies between a few millimetres up to a few centimetres, with a typical length being about five millimetres. MMEAs are used primarily in rodent studies for acute LFPs, single and multi-unit recordings from various cortex areas. It is hypothesised that the 2D-geometry of MMEAs-based recording electrodes makes them more likely to be affected by distance-increasing body fluids and glial encapsulation, thus being the reason for chronic recordings failure. Because of the high aspect ratio and material rigidity, Michigan planar electrode arrays are also more prone to material fractures.

The second most popular micromachined neural interface representative is the Utah electrode array, thus far the only intracortical device cleared for human trials (Figure 2.7 b). UEAs are bulk-micromachined, three-dimensional arrays of millimetres–long needles having tip-recording sites coated with platinum or iridium oxide. UEAs are characterised by significant size and only limited design flexibility- only certain geometry aspects can be predefined, for example, electrode spacing. UEAs implantation surgery is complicated because of notable tissue dimpling. As a result, high-speed implantation procedures based on pneumatic inserters are employed. A high density of recording sites within Utah electrode arrays allows for observing the activity of large neuronal populations with the excellent resolution provided by tip-location of electrodes. Utah electrode arrays are implanted in relatively larger brain volume subjects, such as feline, non-human primates, or humans. They are applied in rehabilitative applications to record and stimulate neurons to perform given tasks, such as control over prosthetic limbs [33, 34]. Similar to other microelectrode technologies, the quality of signals recorded with Utah electrode arrays degrades with time. Recording losses causes are found in the vascular damage, FBR, interconnection failures, size, and rigidity of probes. However, in comparison to planar MMEAs, Utah electrode arrays perform better in chronic applications, what it is believed to be caused by the recording electrodes location at the tips of the needles as opposed to the sides of the shanks.

2.3.2. Polymer-based probes

The majority of polymer-based neural electrodes are shaped similarly to the solutions fabricated in the silicon, such as thin shanks having multiple metal recording sites along the probe's length (Figure 2.8). However, because of the possibility for the employment of polymer-characteristic material modification techniques, such as moulding and thermoforming, and unique mechanical properties, polymer-based electrodes can be shaped into the more advanced geometries, such as cylinders, meshes, or the sinusoid [35, 36, 37].

Critical factors limiting neural recording quality of silicon-based and wire microelectrode arrays are their size and the mechanical mismatch with the brain [38]. Utilising polymers as a devices' base material is likely to help overcome the disadvantages of rigid materials and create conformal contact with soft, irregular nervous tissue. Having lower Young's modulus and being stretchable, polymers do not provoke significant strain on the tissue, limiting the secondary inflammation. While largely identified as rather biocompatible, polymers are characterised by water uptake that often causes material delamination, mechanical, and adhesion problems in vivo and can change the probe's electrical performance over time [39]. Polymers structural degradation causes faster deterioration of underlying metallisations and diffusion of various molecules to and from the implant, impacting body response to the device. Because of that, nowadays, the majority of research on flexible electrode arrays is limited to acute and short-term neural recordings. Thus far, most of the research involving polymer-based intracortical electrodes in animal studies focused on tissue reactions and implant insertion behaviour. However, acute and short-term recordings in rats' and non-human primate cortex, reaching up to several weeks in the latter case, were performed [40, 41]. The technology of polymer-based neural recording probes is currently under constant development, with new designs being presented regularly.

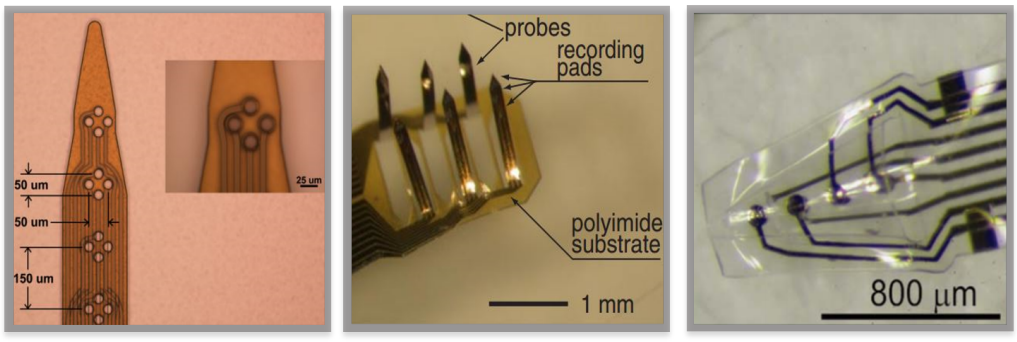
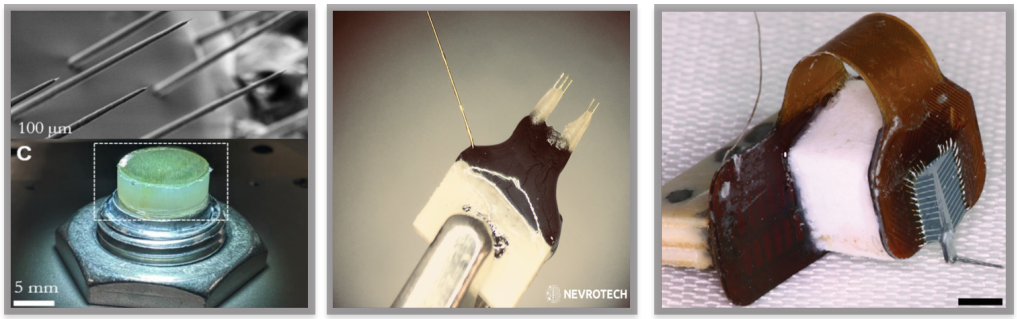


Figure 2.8.: Polymer-based neural microelectrodes: a) Flexible polyimide-based planar multisite shank electrode [42], b) Polyimide-based three dimensional multichannel electrode [40], c) Three-dimensional thermoformed Parylene-C-based cone polymer sheath electrode [43].

2.3.3. Microwire-based probes

Notwithstanding numerous advancements in the field of multi-channel micromachined silicon probes, there has not been much evidence to suggest that those perform better than traditional microwire arrays (MWA), representing the historically the first neural probe technology in use for more than sixty years [47].
Arrays are based on the bundles of 10–200 μm diameter conductive material microwires (Pt, Au, Ir, W, carbon fibre) with an uninsulated tip used to observe the biopotential from neurons in the vicinity. There have been various designs introduced using wire electrodes of different shapes and sizes. These include single wires, co-spun bundles, and organised multiple-lead arrays held together by PCBs or connectors with dental cement, methyl methacrylate, or polyethylene glycol. Despite the maturity of MWA solutions, there have not been many advancements in the overall design and structure of complete implants [48]. What is more, precise controlling of their spacing and location is challenging, especially for higher density electrode arrays.

To this day, a large part of neuroscience society chooses to use microwire electrodes because of the high quality of observed signals. MWAs longevity and chronic recording performance are unparalleled, showing implants operating for years [49]. MWAs are conventionally used in studies of neural activity in the brains of rodents, non-human primates, mammals, and humans, especially in applications requiring stable long-term performance or interfacing deeper brain structures [50]. In comparison to Si-based electrodes, microwire arrays chronic stability stems from generally smaller and more circular cross-sections causing less damage during insertion. MWAs record from the tip of each wire and, as such, observe the activity of tissue not affected by FBR, compared to planar electrodes, which are adjacent to tissue experiencing significant mechanical stresses.



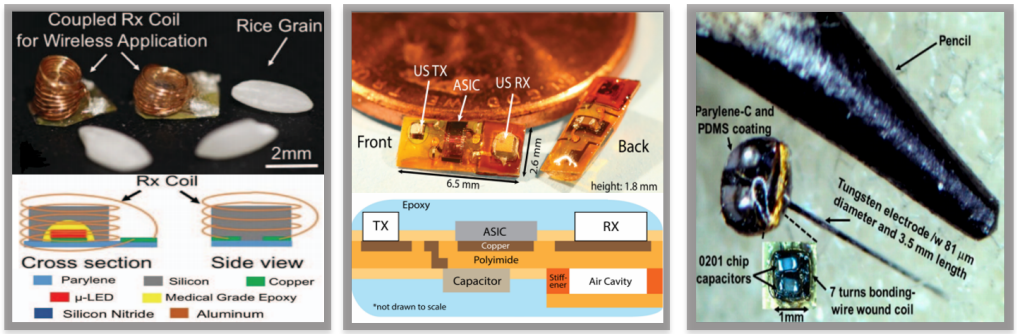
a) b) c)

Figure 2.9.: Microwire-based neural microelectrodes: a) Argo System - Pt-Ir microwire array bonded to a CMOS voltage amplifier array [44], b) Nevrotech Stainless Steel/Pt-Ir microwire array [45], c) A high-density carbon fiber neural recording array [46].

2.3.4. Distributed neural probes

One of the current trends in the development of BMI systems is the shift from centralised, single tethered units to much simpler but highly miniaturised networks of implants (Figure 2.10). With an aim to make systems of floating neural interfaces viable, the footprint of each individual implant should be kept to a minimum. The size should preferably be much smaller than the currently achievable few square millimetres so that several units can be placed next to each other and cover larger cortical areas. In addition to facilitating systems scalability, it has been proven that smaller implants cause a reduced inflammatory response in the surrounding tissue, thus are safer when considering implantation of a large number of devices [51, 52, 53, 54].

Despite the size of an individual floating device being considerably smaller compared to centralised, multi-channel implants like Utah arrays, due to the scale, the total tissue displacement and system invasiveness may be more significant as multiple devices rather than one are being involved. This is because, in distributed approach, the total number of implanted devices is much larger; thus, the overall tissue displacement must be seen cumulatively - as the sum of the volume of tissue being affected by each individual implanted probe. Materials employed in designing and fabricating distributed BMIs depend mainly on the packaging scheme of choice. Solders, ceramics, and polymers such as liquid crystal polymer (LCP), polyimides, Parylene-C and Polydimethylsiloxane (PDMS) are found in SoC-based systems. On a chip level, they include silicon oxide, silicon nitride, silicon carbide, hafnium oxide, aluminium oxide and their combinations.



a) b) c)

Figure 2.10.: Overview of the architectures of autonomous distributed neural interfaces: a) Optical neural interface implant employing polymer substrate and epoxy protection of micro LED module interface [55], b) Multi-component neural interfacing implant assembled on polyimide substrate with Epoxy coating [56], c) Tungsten microwire-based implant with Parylene-C/PDMS polymer package [57].

2.4. BMI development challenges

2.4.1. Foreign Body Reaction

The challenge of a neuronal implant to stay active and work reliably for a long time arises the moment it is introduced to a biological environment, when a cascade of body events forming a so-called foreign body reaction (FBR) takes place.
FBR is a body's natural self-defence mechanism causing the probe to deteriorate, and tissue around the implant to form scarred sheath reaching as far as 150 microns from the surface of implant[58]. The rejection mechanism progresses within months from initial insertion and involves activating various cells, which densify and thicken to form a tight capsule, inevitably changing local neuronal architecture (Figure 2.11). As a result, the quality of recordings from microelectrodes degrades over time, which can be observed as an increase in electrode impedance.

Because of the high complexity of the FBR mechanism and the number of ways it affects recording from neural implants, the exact explanation of its foundations and influencing factors is debated. Currently dominating belief is that the extent of FBR is related to the degree of inflammation and cellular reorganisation resulting from the damage to the local vasculature [60]. Indeed, it has been shown that recording capability decreased much faster in implants around which the degree of blood-brain barrier damage was more significant [61]. Moreover, neurodegeneration is also observed at the areas of iatrogenic stab wounds, suggesting that the change in cellular architecture is being correlated with the extent of initial bleeding after surgery trauma and amplified by the presence of implanted foreign

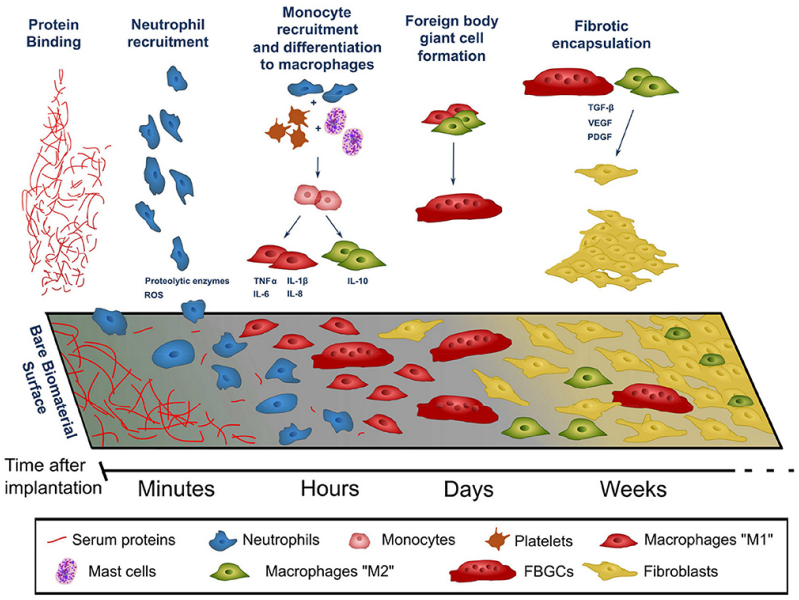


Figure 2.11.: Timeline of cellular activity accompanying foreign body response after material implantation. Reproduced from [59].

body [60]. Some research supports the astrocyte hypertrophy forming glial capsule as a valid explanation for recording loss. It is believed that it can isolate electrodes physically and electrically from healthy nervous tissue at a scale large enough to block signal recording and push active neurons away from the device's surface. Other hypotheses imply that recording losses are caused by material corrosion following contact with the corrosive biological environment, prolonged reduction in neuronal counts, or due to demyelination and degradation of cellular functionality.

2.4.2. Wireless telemetry and power delivery

Packaging of neural implants nowadays is mainly achieved by housing electronics and power supply in head-mounted stages, and connecting with probes body by transcranial flexible leads [62]. Using cables requires forming prevailing transcranial and percutaneous connections, which may become an entry point for infections. Aside from that, cables induce compressive force around an implantation site, leading to flattening and reorganising adjacent neuronal architecture. A solution to that problem could be using wireless telemetry, which in implantable applications faces issues of signal attenuation and scattering, weak coupling, and non-uniform power coverage, among others [63].
Because of restricted postoperative accessibility to implants, a rechargeable powering scheme is preferred over single-use batteries, especially when multiple devices are to be implanted. The challenge in achieving wireless power delivery in implantable neural interfaces are the efficiency of remote charging and the need for energy storage of small physical dimensions, but sufficient internal storage capacity and low internal impedance [5]. From the embedded electronics perspective, the power delivery difficulties raise a challenge to devise electronic systems capable of high-efficiency signal processing under a limited, low power budget.

To date, fully-integrated neural interfacing systems remain instead confined to the acute scientific applications, and only several systems offer fully wireless mode of powering and telecommunications via RF, optical or ultrasonic links [64, 65, 66]. The reason for that is the characteristics of the environment. Any wireless communication performed through thick, attenuating media such as dura, skin and bone is compromised. Additionally, when using wireless links, it must be ensured that the total communication does not heat adjacent tissue by more than 2°C, as that can lead to cellular necrosis.

2.4.3. Packaging and CMOS integration

Nowadays, CMOS electronic chips are commonly integrated within devices used in a myriad of applications, including sensors, MEMS, or lab-on-chip. Some of these devices successfully operate in demanding environments of elevated temperature or ionising radiation. Nevertheless, where implantable biomedical devices are considered, harsh environmental

conditions of a living body and strict safety requirements prove electronics integration particularly challenging.

The formation of intelligent, autonomous, and miniaturised implants necessitates integration with some form of smart modalities usually achieved by including on-device electronics. To date, the majority of cortical neural interfacing systems relied on positioning power supply and data processing units on the outside of the body and utilising flexible cables to provide connections to an implant [1]. That way, tissue interfacing microelectrodes could be manufactured using various methods regardless of their CMOS compatibility. With the decentralised distributed neural interfacing systems of tens of IMDs coming into the light, such an approach is no longer feasible. In order to avoid an accumulation of wired connections, it is desirable to embed the electronic chips inside the implant package. That way, data processing can be performed locally, minimising the possibility of transmission losses and the presence of cable-induced infections. However, placement of the electronics inside an implant, especially when miniaturisation of devices is assumed, imposes additional requirements for the packaging strategy, as CMOS chips involved must be protected from the effects of the body environment. At the same time, the implantation environment should likewise be shielded from unnecessary material exposure.
To create a standalone implantable neural recording system, sensing units consisting of microfabricated arrays of probes need to be connected with computational, communication, and power supplying blocks and encapsulated within a hermetic package. Despite a high level of miniaturisation achieved for penetrating probes, integrated neural interfacing systems remain large because of the limitations in the choice of available assembly, interconnection and packaging methodologies.
Ultimately, the choice of packaging approach should account for materials permeability characteristics and application requirements [67]. Figure 2.12 illustrates the relation between material thickness and time needed for the moisture to penetrate through a given layer. A brief analysis of this relationship shows that packaging materials of choice should be dense inorganic materials, such as thick glasses, ceramics, pure crystals, or metals, for applications requiring long-term hermeticity. Such materials can keep the environment humidity-free for years thanks to their compact atomic structure, which is limiting the occurrence of moisture trapping.

Protection of electronic circuitry from moisture in implantable applications can be achieved using one or a combination of two basic packaging strategies: direct deposition of the protective material coating on the chip or provision of additional outer enclosure made of polymer, glass, or metal. Figure 2.13 depicts various combinations of microimplants packaging concepts based on the two main packaging strategies concerning their hermeticity on the system- and component-level, where hermeticity is understood as an airtight, gas and moisture-impermeable barrier. Hermeticity in those concepts can be achieved either

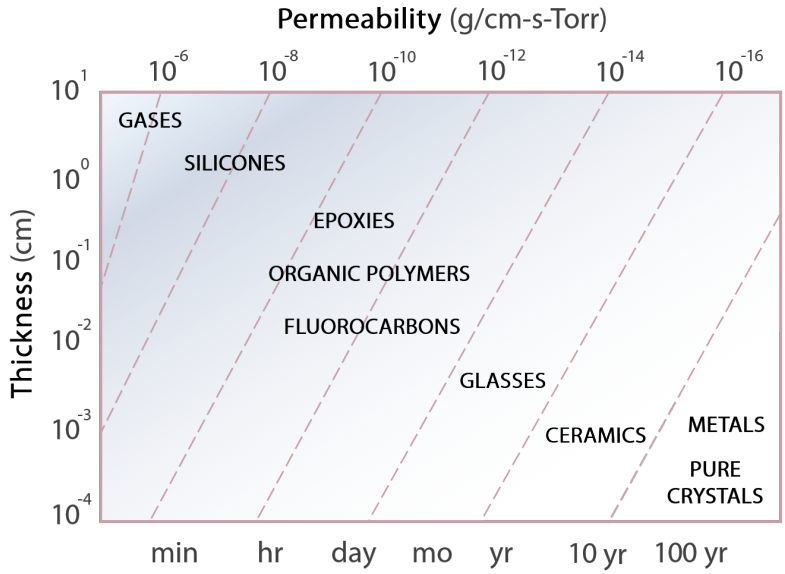


Figure 2.12.: Material hermeticity performance over time in relation to its thickness. The primary x-axis shows time for package interior to reach 50% of exterior humidity [68].

on a system level by protecting multiple components under one hermetic housing or ensuring each system's sub-component is protected individually. Hermetic housing on the system level is typically executed using various metals and ceramics, whereas system-level non-hermetic packaging uses conformal polymer coatings.

The first packaging strategy relies on coating implants with layers of protective materials, usually polymers such as Parylene-C, PDMS, and epoxies, and is typically achieved by depositing material at the end of fabrication and assembly run. Whereas an implant's polymer jacket cases have been shown to provide an acceptable level of hermeticity, given the polymer's porous nature, such coating requires a relatively thick layer to serve its purpose over time. Polymers' affinity to moisture degradation is causing them to swell and delaminate. This characteristic makes using polymers as outer packages for miniaturised interfaces complicated and does not secure devices' integrity in the longer term. What is more, being organic materials, polymers are more prone to degradation due to biological and chemical processes such as enzymatic mechanisms, hydrolysis, or biofouling. [39, 70, 57, 55, 63].

On the other hand, approaches of using thin, ALD-deposited high-K ceramic materials such as Hafnium Dioxide and multilayers of Silicon Dioxide with Hafnium Dioxide as a protective coating on neural implants have recently emerged [71, 72]. They hold the promise of thin, stable coatings; however, they would not solve the issue of mechanical stability of chips stressed by the tissue nor integration difficulty of more advanced microelectrode designs on the system-level, as ALD process effectiveness is highly dependent on the substrate's surface.

Instead of protecting circuitry utilising additional layer deposition, another packaging strategy is to provide a custom enclosure made of two components. Two components are base and lid, made of inorganic materials such as silicon, ceramics, or quartz connected either on a molecular level or by an intermediate layer of other material. Depending on the intermediate layer material, this approach can be considered fully hermetic, allowing for life-long protection of devices within. The main challenge of this method is selecting correct joining techniques providing reliable joint as in the two-component approach, the seal in between is the weakest and possibly the least hermetic point of the system. The seal itself can be achieved employing brazing, anodic bonding, or soldering [73, 74]. All-metal brazed packages are popular packaging solutions in implants designed for other regions, such as cardiac pacemakers. Despite that, they are impossible to use in applications where wireless communication or MRI compatibility is necessary, as they could reflect the transmission signal or pose a health risk to the host. The hurdle in the capsule-like packaging

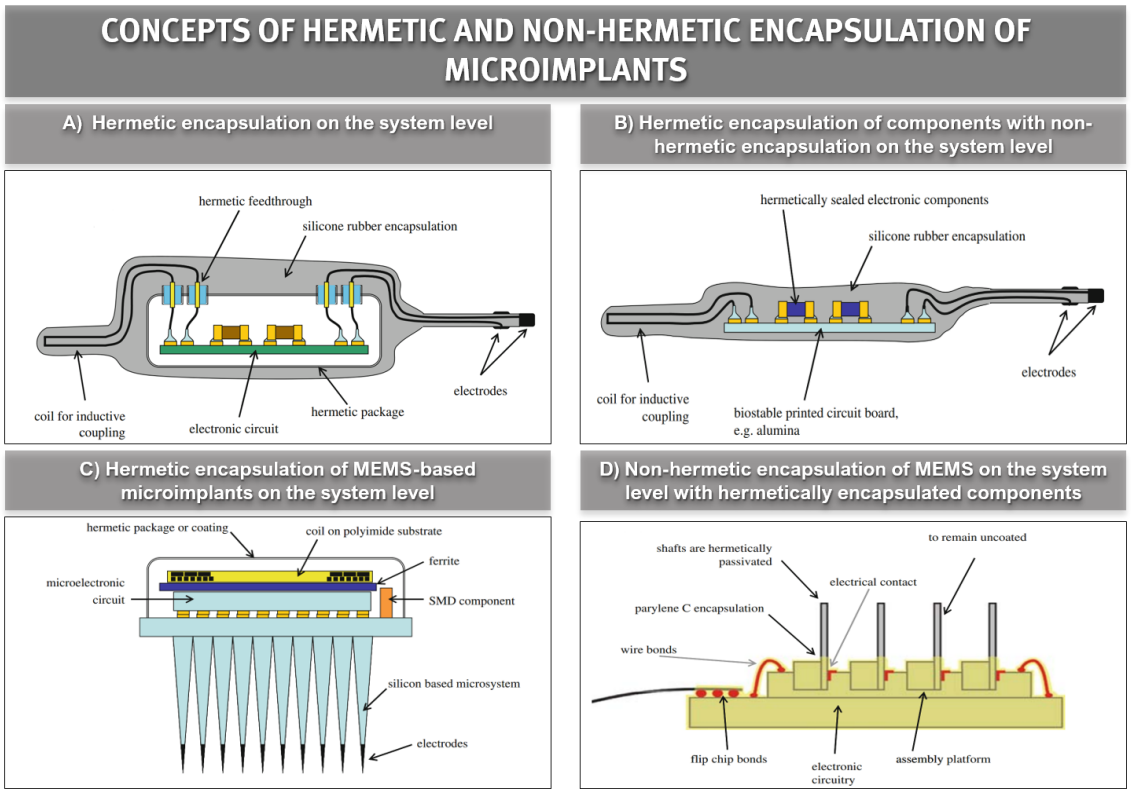


Figure 2.13.: Simplified concepts of hermetic and non-hermetic encapsulation of microimplants. A) Hermetic encapsulation on the system level; all electronic components are placed inside a hermetic package, and feedthroughs connect electrodes and coil for inductive coupling. B) Hermetic encapsulation of components with non-hermetic encapsulation on the system level; C) Hermetic encapsulation of MEMS on the system level; D) Non-hermetic encapsulation of Si-based MEMS on the system level with hermetically encapsulated components. Reproduced with changes from [69].

approach is the integration with microelectrodes, which requires forming interconnects either tunnelled underneath the seal or vertically through the package using vias, thus complicating the fabrication run.
To ensure the performance of electronics enclosed within an implant is up to specifications, chosen assembly and packaging methods should avert the involvement of high temperatures and reactive materials. This prevents the possibility of dopant re-distribution, creating oxide defects, and material migration into the circuit's junctions. Any process involving thermal treatment in temperatures higher than 350-400° C can lead to circuitry degeneration, thus when implants are to integrate ICs, techniques of sealing and packaging which are well-established in MEMS and sensor industries such as anodic bonding, glass frit, or thermocompression bonding become largely incompatible [75].

CMOS toxicity

Fabrication of CMOS devices typically involves utilising several materials and chemicals hazardous to humans, the traces of which may remain present in the final device. When not properly secured, these remnants could leach and affect local tissue. The possible toxic effect on the host is more significant the larger the number of devices in the system, as the cumulative effect of cytotoxicity of CMOS dies present inside each implant becomes more impactful [76]. In addition, any outer materials in contact with on-implant circuitry should be free of metal or mobile ions, which could otherwise migrate to the IC's junctions [77].
Once implanted, the effect of the environment on the devices' integrity must be considered. Bodily fluids are usually of ionic content, widely containing reactive mobile elements, such as chloride, calcium, potassium and sodium. Unprotected exposure of CMOS die to such environment can lead to device's premature failure caused by a shortage or corrosion. Similarly important is electrochemical compatibility of an environment with various materials used in devices, including materials used in integrated electronic circuitry. When a neural interface is used for stimulation as well as for recording, exceeded stimulation water window and insufficient packaging can lead to uncontrolled electrochemical reactions at the interface and pH variations which can cause neuronal degeneration or corrosion to exposed metallisation [78, 79]. The electrochemical stability of aluminium, which is the most popular top-level metallisation material in CMOS, changes with pH. Its behaviour can vary from corroding at low and high pH to purely passive in neutral pH [78]. Nonetheless, neutral pH conditions would occur solely if the device with an aluminium layer would be immersed in pure DI water. In reality, the surrounding medium is CSF, present with ions, including chlorides, which, when adsorbed, can locally generate harmful HCl molecules [76]. Other than that, aluminium has been found to have a toxic effect on the human body, with a clear adverse impact on the nervous system.
When fabricated, CMOS devices are coated with dielectric layers of silicon oxide and silicon nitride, which on their own provide a limited level of protection against environmental

effects. The robustness of such insulation depends on the thickness and quality of deposited films which may differ depending on the equipment and processes used [80, 81]. Some studies indicate that when exposed to the biological environment, unprotected CMOS insulation alone may start dissolving. However, thus far, the research on this phenomenon is inconclusive.[80].

2.5. ENGINI Project

Described work is a part of the ENGINI (Empowering Next Generation Neural Interfaces) project, which aims to develop an entirely new generation of standalone mm-sized intracortical neural implants. Compared to currently dominant centralised multisite BMIs, which either offer very detailed information from small brain volume or averaged signal from large brain areas, ENGINI differs in a simplified, distributed approach. ENGINI interface is going to be composed of tens of individually addressable mm-sized, non-tethered implants distributed in various cortical regions, each containing a handful of microwire electrodes (Figure 2.14). The choice of microwire interfacing electrodes is reasoned by their superior long term implantation performance and material robustness.
By developing a wireless mode of power exchange and data communication combined with an IC-housing hermetic package, it is envisaged that ENGINI probes could provide real-time access to detailed neuronal processes over large cortical regions. To make it possible, ENGINI, instead of focusing on single-neuron spiking activity, is going to focus on the recording of LFPs, which have been shown to contain useful information over a prolonged time. Research within the ENGINI project is concentrated on the following areas:

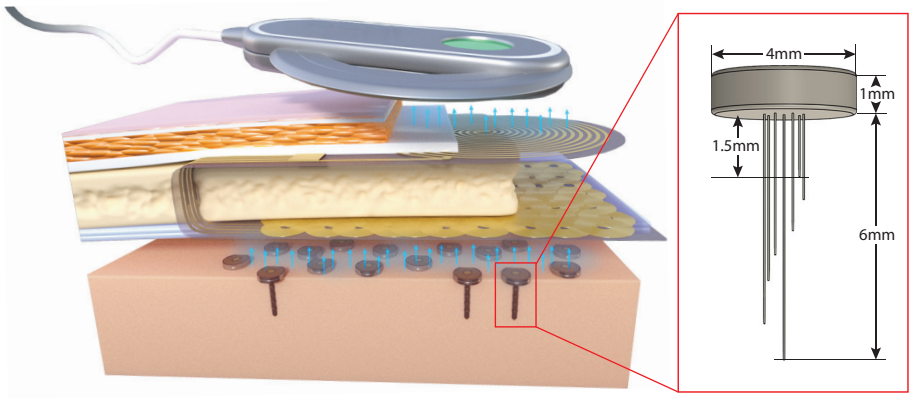


Figure 2.14.: ENGINI system concept. The architecture of the probe body housing embedded electronics and multiple recording microwires. The three-tier RF wireless system provides power and data communication.

- **Hermetic CMOS micropackage and scalable technology for fabrication and implantation of implant's body architecture.** This includes employment of bio-, RF-, and CMOS-compatible methods and materials for creating interconnections, assembly, packaging, microwire integration and, where possible, using approaches allowing for future automation and large scale production.
- **Fully wireless powering, communication and data transfer** to avoid the need for transcranial wired connections. The problem of signal attenuation resulting from the tissue absorption and psychical distances between transceivers will be achieved by implementing three-tier RF inductive link architecture. Application of low-power

electronics equipped with autonomous power regulation will enable hundreds of devices to use the same transmitter and accommodate varying electromagnetic field strength levels.

- **Neural recording target**. This focuses on recording LFP signals using a deep-learning decoder strategy. Focusing on LFPs at different depths along cortical column allows benefiting from the long-term stability of LFP signal recordings, even in the presence of foreign body reaction effects.
- **Data minimisation and decoding**. To observe large scale neuronal activity through multiple distributed electrodes, instead of typically applied linear decoders, non-linear decoding based on deep-learning techniques will be employed, optimised and realised on a low-power platform for real-time application.
- **Design of custom electronics** including signal acquisition and reference circuits under low power, high versatility and minimum footprint constraints. Implants power regulation will be performed entirely autonomously, allowing multiple devices distributed over large cortical areas to use one transmitter and accommodate varying electromagnetic field strength levels.

2.6. Summary

This chapter provides an introduction to implantable medical devices with a specific focus on devices interfacing with the nervous system. An overview of basic types of intracortical neural electrodes is given, along with the presentation of the basic anatomy of the nervous system, fundamentals of neural recording and process of foreign body response.

Since implanted cardiac pacemakers appeared in the 1960s, they saved life and health of countless people. Nowadays, different implantable devices are available for the majority of human body areas and come in various shapes, sizes and purposes. Active IMD systems dedicated to interface with the nervous system, apart from cochlear and DBS implants, are still in the early stages of progress. That is mainly because of the difficulties in obtaining stable, high-resolution neuronal recordings from specific neuronal groups of interest without introducing invasive electrodes. That creates a need for a compromise between BMI systems invasiveness, long-term performance and high-detail recording capabilities. Design and implantation of IMDs is a task charged with multiple challenges, including system integration, implant packaging and wireless telemetry. Nowadays, most state of the art BMI devices are limited to academic use, and as such, help gain more knowledge about mysteries of the brain processes. However, with the evergoing technology progress, hopefully, they will soon become therapeutic treatments.

New paradigms in intracortical neural devices promise to overcome challenges given by the complex brain environment. One of them is the approach of implanting multiple devices spread over large cortical areas. It is believed that by shifting the focus of implantable brain devices from single, highly complicated units to networks of more straightforward, wireless devices, the overall system's stability and autonomy can be improved.

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3. Design of a microwire-based mm-scale cortical recording implant

Designing the form, size, and general packaging architecture of the sensor integrated within the biological environment requires acknowledging its desired function and the host habitat. It is essential to ensure the hermeticity by selecting an appropriate sealing method, as described in the Chapter 4, though it is equally crucial to guarantee the sensor's shape, configuration and dimensions to enable and ease the performance in a final application.

A vast amount of research has been dedicated to the implantation of active devices into the brain and finding a correlation between implants' shape and their performance. Owing to the complexity of co-influential factors affecting the interpretation of the implantation results, the decision on the architectural design aspects of implants becomes critical. Implant's package is not only responsible for housing electronics, interconnections, power and communication modules but also for ensuring integration of the device with the biological environment. Designing implantable devices is charged with a variety of constraints that must be adhered to for the reasons of safety and efficacy in chronic applications. Given the specificity of the brain environment, one must account for such issues as biocompatibility, tissue electrical impedance, brain's viscoelasticity, and density mismatch between implant materials and neural tissue. The most pressing issue in the design and packaging of implantable neural probes is the realisation of interconnects. While miniaturisation progresses in almost every field, from CMOS devices to packaging, the bottleneck remains in how connections between implant modules are made. This is true, especially when interconnects join two vastly different materials, such as metal wires and electronic chips.

This chapter provides a background on the materials and strategies employed in the design of implantable cortical devices. Design considerations are reviewed in the context of the microwire-based ENGINI probe. Two generations of designs for the probe architecture are proposed and described, along with microwire-CMOS interconnection concepts.

A portion of the material presented in this chapter has been published in [1, 2]. Part of this work has been a collaborative research with Mr Matthew Cavuto, together with whom the packaging concept for the ENGINI V2 was established, and who designed the layout of the PCB mock-up and ceramic LTCC probe microwire modules. Additionally, Dr Federico Mazza explored the ENGINI V2 3D-printing approach.

3.1. Neural Implants Design Considerations

Regardless of the technology, BMIs follow the same constraints given to implantable devices, such as high functionality, reliability and stability. As the miniaturisation progresses and the overall number of devices to be implanted increases, the aspect of a system's safety becomes even more crucial. However, when implanted for long periods in harsh conditions of a living organism, even the most robust of materials are going to experience degrading effects on their integrity [3]. Therefore, for long-term implanted devices, it is essential to ensure the maximum degree of material safety and resilience, as even as early as a week after the implantation, the effects of materials compatibility can be observed [4]. Each device needs to be long-term hermetically packaged, which requires encapsulation methods to keep the implant's size small while ensuring safe use without affecting data and power transfer. In addition, both the packaging and fabrication methods should be easily applied to hundreds of devices at a low cost, preferably in a parallel manner. From the fabrication perspective, it is crucial to ensure each implant has the same characteristics to avoid any performance variability between devices.

Figure 3.1 outlines the fundamental types of failures which may occur to the implanted device once placed in the tissue, which any device's design should account for. Primary issues are related to the body response to the implanted device, such as bleeding, gliosis or neuronal degeneration. Other failure types are directly related to the design of an implant itself, including damage to the insulation materials, corrosion, loss of hermeticity or broken interconnections.

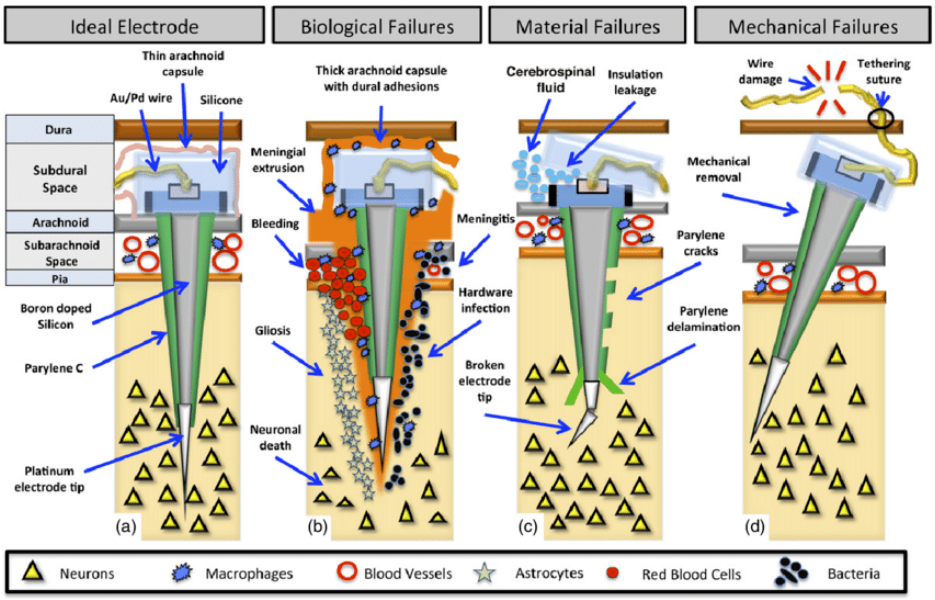


Figure 3.1.: Major failure modes of implantable neural electrodes (a) Failure-free scenario with ideal implantation of about 1-1.5 mm into the cortex. (b) Biological failures (c) Material failures (d) Mechanical failures [5].

Table 3.1.: Comparison between the most popular materials used in implantable devices in relation to their characteristics important for the packaging.

Properties:	**Metal:**	**Ceramic:**	**Polymer:**
Biocompatibility	Good for some	Good for some	Good for the most
Hermeticity	Good	Medium	Mostly poor
Outgassing	Low	Low	Mostly high
Mechanical flexibility	Poor	Poor	Good
Reliability	Good	Good	Mostly poor
Optical transparency	Poor	Mostly poor	Good
RF transparency	Poor	Good	Good
Processing Ease	Medium	Difficult for the most	Easy
Cost	High	High	Low
Relative Weight	Heavy	Medium	Light

The choice of materials used for the implanted devices, particularly in the outer layers, strongly influences the type and magnitude of an interaction between an implant and a surrounding tissue. For this reason, implant's building materials should satisfy the necessary biocompatibility requirements as to their toxicity, biostability, allergenicity, and biofouling [6, 7, 8]. Typical materials employed in designing and fabricating neural interfaces largely depend on the packaging scheme of choice. Materials most commonly used include silicon oxide, silicon nitride, silicon carbide, hafnium oxide, aluminium oxide and their various combinations on a chip level; alongside solders, ceramics, and polymers such as liquid crystal polymer (LCP), polyimides, Parylene-C and Polydimethylsiloxane (PDMS), in SoC-based systems. Table 3.1 outlines essential characteristics of different materials in the context of their practicality in the building and packaging of implantable devices.

It might not be possible to entirely exclude the use of non-biocompatible materials from the entirety of an implant (for example, those used in CMOS fabrication). However, it is strictly necessary to ensure that the outermost layer of encapsulation is fully protective and biocompatible. Embedded electronics generate heat, which, aside from affecting the local biological environment, can influence the integrity of interfaces made with materials of different thermal characteristics [9]. As a result, thermal conductivity properties should also be considered when selecting implant's structural materials and designing their final shapes. It is an additional advantage when the materials employed allow for safe magnetic resonance imaging (MRI) inspections; however, they must enable and support the transmission of data and power signals or allow for embedding wired interconnections.

Irrespective of the materials selected, the implant and its package ought to tolerate obligatory procedures of medical device sterilisation, which require a combination of radiation, chemical, or thermal treatments[10].

3.1.1. Mechanical Considerations

In addition to implanted device's shape and characteristics, the implant's reliability heavily depends on the structural design of the probe. The specificity of a shape and the characteristics of electrodes largely influence how the implant's interconnections may be achieved, so in turn, what type of packaging can be used.

From the mechanical design point of view, implants should exhibit properties that would allow for easy implantation, integration with the neurons without straining the tissue around, and avoid the possibility of breakage. Mechanical characteristics of nervous tissue are largely different to those of materials used in neural interfaces (Figure 3.2). Brain tissue's low elastic modulus (5-100 kPa) and its viscoelastic properties make any implantation of stiff probes problematic- instead of sliding through it, most implants will rather buckle and compress tissue significantly before and during penetration. This is an undesired effect that could potentially add to an already long list of potential complications after the brain surgery. Tissue dimpling can be reduced with stiff probes of sharp tips and slender geometry, but for a price of a continuous local irritation resulting from the significant mechanical mismatch, which may reach up to the eight orders of magnitude [12]. Pressure applied by stiff probes and a lack of mechanical conformity may lead to the formation of interfacial gaps, which, when filled with body fluids, effectively shunt recording electrodes between adjacent sites. The opposite approach assumes using materials that would be soft and flexible, like polymers, to fit low elastic modulus of the neural

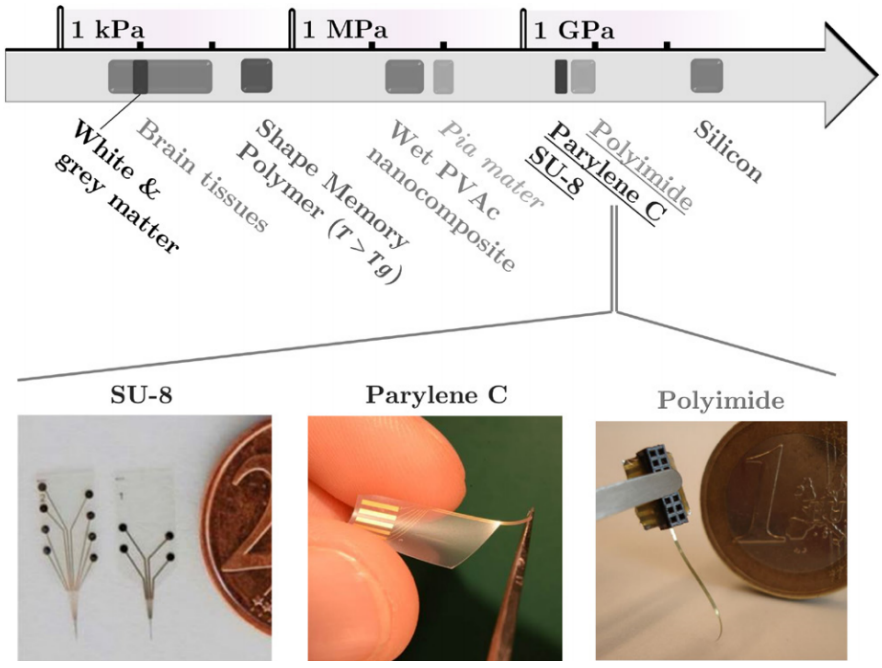


Figure 3.2.: Differences between mechanical properties of the brain tissue and materials typically employed in neural interfaces, with a special focus on soft materials representation (inserts below). Reproduced from [11]

tissue and minimise a relative micromotion, however for the price of insertion problems and resulting in difficulties during implantation surgery [13].

In the microscopic view, it has been shown that implants with induced surface nanoroughness tend to integrate better with the host tissue by promoting neuronal ingrowth and cellular attachment. This is most likely because of a similarity to the morphology of the extracellular matrix environment. Macroscopically, both in the chronic and acute implantation, small, cylindrical or lattice-like shapes evoked an overall smaller body response than large, planar geometries, as proven by histological, transcriptomic and electrophysiological studies [14]. Nonetheless, as far as the size debate goes, there still seem to be a doubt, as earlier studies indicated that implants size reduction is beneficiary only initially and generally does not influence the formation of the glial encapsulation [15]. It has been shown that minimising FBR mechanisms can be achieved with the micrometre-scale implants and by conforming to the soft, moving neural tissue. Whereas fabricating such systems is possible, for example, by using polymeric or micrometre-scale sized materials and components, their implantation becomes exceptionally complex [16]. Generally, the electrode's type should be tailored to the target implantation subject, as the brain architecture differs greatly between humans and other species. Likewise, the electrical activity of targeted brain regions of interest imposes electrodes impedance requirements.

As a rule, miniature, cylindrical probes have been found to evoke less intense body responses - both acutely and chronically, as compared to larger, planar structures [17, 18]. Ensuring minimised dimensions is especially important in the vertical direction, as it correlates the most with the typical axis of the brain displacement. Due to the daily movement, respiration, and vasculature pulsation, the brain displacement ranges from several microns up to a few millimetres [19]. Because of that, BMIs are commonly designed with the part protruding from the cortex being possibly the flattest and with a minimum number of edges that could damage surrounding tissue. However, when considering recording effectiveness over time, microwire electrodes' performance is unparalleled despite their larger size compared to, for example, polymer probes. Interfacing electrodes ought to withstand axial implantation forces without buckling and compressing underneath tissue. This is more easily achieved for stiff, smooth electrodes of pointed tips and a small footprint. The length of the probe and distribution of electrodes is related to the architecture of the neuronal structures of interest. However, it is always beneficial to provide many recording sites along the probe to record the depth profile of a neuronal activity without displacing large tissue volumes.

3.1.2. Interconnections

Nowadays, the trend is to miniaturise implants while equipping them with more and more channels, thus increasing the interconnection pitch density and giving rise to the problem of connectivity method selection [20, 21]. In fact, alongside the need for a way to package implants hermetically, the problem of feedthroughs becomes often overlooked but a significant obstacle on the way to achieve a new level of neural interfaces' miniaturisation, and technological advancement. As a whole, the interconnectivity problem is observable also in larger-scale devices, such as DBS probes, where implanted leads often cause devices failures. The type of tissue-interfacing electrodes used in implants and the level of electronics integration on the devices directly influence how all implant's sub-components can be connected to each other. The connectivity problem is somewhat easier to tackle for fully photolithographically-defined micromachined probes, where it can be solved on the system level by chip stacking, extra electric paths tunnelled under dielectrics and TSV technology (Figure 2.13 c). Where that cannot be achieved, flexible cables soldered or thermocompression-bonded to the microelectrode array platforms and distally-ended with various connectors for connecting to external electronics are employed.
The realisation of the interconnectivity is particularly challenging for microwire-based microelectrode implants. Microwires are typically secured to the head of an implantable probe through wire bonding or relatively bulky external connectors [27] (Figure 3.4). Such connectors are usually passive, meaning no active electronics is hosted within, and the element is used only to wire electrodes to electronic circuits that are placed further away

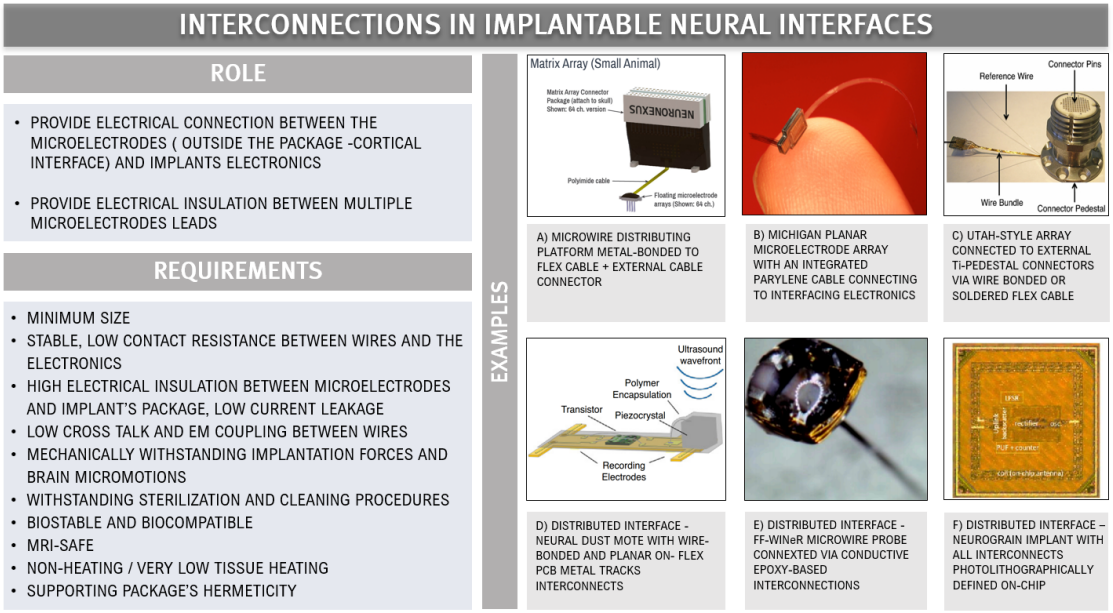


Figure 3.3.: Overview of interconnection approaches in various neural interfaces [22, 23, 5, 24, 25, 26]

from the implantation site. The use of connectors is labour-consuming and does not lend itself to the miniaturisation of devices or their scalability. Moreover, current microwire encapsulation methods often rely on polymer-based solutions that do not provide long-term hermeticity because of their permeability characteristics (Figure 2.12). To date, aside from connectors, the primary method of securing electrodes and preventing damage for single-microwire smart miniaturised implants systems is by soldering and fixing wires in place using epoxies and silicones [28]. A new approach for microwire-based implants has been proposed by Paradromics company, where thousands of microwires are bundled together into one shank and then pressed against a CMOS pixel array to form connections [29] (Figure 3.4 c). Securing the bundle is again made with epoxies. Whereas such an approach enables parallel connectivity for the multitude of microwires simultaneously, the size of the resulting bundle is quite large and thus affecting local neuronal tissue.

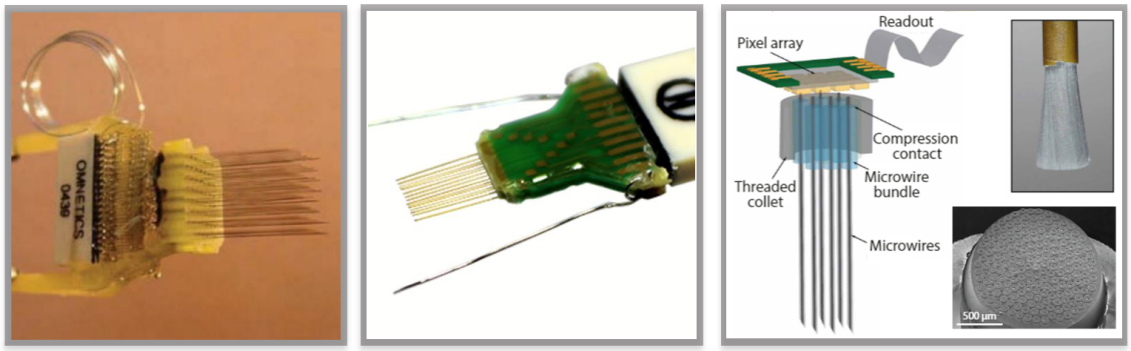


Figure 3.4.: Examples of the interconnectivity in microwire-based electrode neural interfaces: a) 64 channel, floating, discrete 8×8 microwire electrode array assembled into a connector [30]; b) Tucker Davis' 32-channel layered polyimide-insulated tungsten wire array assembled onto the custom PCB; c) Paradromics microwire array [29].

3.2. Design of the ENGINI implant's architecture

ENGINI system packaging requirements and constraints

As stated earlier, the ENGINI probe is being designed with several specific requirements in mind. Unlike most other systems available in the field, each implant will employ several microwires as a neural recording medium, which are to be integrated with the electronic chip and wireless coil, all in a single package.

Instead of focusing on both recording and stimulation, to simplify material choice, ENGINI implants are primarily designed with the aim of LFP recording only, as properties' prerequisites for recording and stimulation sites are, to some extent, more relaxed. The size of the implant's head should be small enough to allow for multiple implant nodes to be located close to each other, forming the array of probes. On the whole, an entire implanted sensor is to stay within a millimetre scale, with the aspect ratio of probe head diameter to its total thickness not less than two. The top head module should be circular to avoid sharp corners and facilitate conformal coating of the barrier material. The total height of the floating pin's head should not be much larger than 2 mm, owing to the limited dura's stretchability and confined subdural space, which depending on the cortical region, varies between 0.5-7 mm. To assess probes' hermeticity, they will be equipped with a small cavity located at the CMOS-capping wafer interface, allowing for the accumulation of air samples that can be then tested for a moisture ingress with the appropriate CMOS-based humidity sensors. A critical issue to address is the way the interconnections between electronic and microwires-housing parts are formed. Since direct mounting is exceptionally challenging because of the fragility of CMOS substrate, interposer technology can be employed instead. Interposer is an additional substrate introduced to the implant stack that can provide further mechanical support, electrical contacts redistribution layer, or both. All fabrication and integration methodologies are selected with biocompatibility, CMOS compatibility and RF-communication support in mind. Additionally, process design accommodating the future possibility of a large-scale production is taken into the consideration.



Figure 3.5.: Concept image of the targeted ENGINI's implant shape.

3.2.1. First generation ENGINI probe

Respecting the abovementioned design considerations and constraints resulting from the ENGINI project, the initial embodiment of the project's probe was fabricated as a proof of concept.

The first-generation ENGINI implant body (V1) was designed to evaluate the possibility of microwire mechanical fixation combining dual-interposer technology. The probe body comprises three main modules: dual interposer- a stack made of passive glass and active silicon die, CMOS chip, and four microwires. In this embodiment, wire electrodes are kept in place thanks to the interposer pair consisting of pre-patterned glass and silicon substrates (Figure 3.6). The bottom glass substrate serves as a mechanical support and ensures sufficient structural stability for high aspect ratio metal leads. It houses a central through via from which symmetrically spread grooves depart. These grooves are deep enough to house every individual wire within. Bonded on top of the glass is a silicon interposer layer that acts as an electrical connections redistribution layer to the active electronics (CMOS substrate), which can be die-bonded face down on the top of the probe. Wire electrodes are threaded through etched vias, and the connection to the top planar interconnections is secured by filling them with metal in the process of *in situ* electroplating. The overall size of the probe head measures 4×4 mm. In this version, the number of wires was limited to four.
Although the proposed design aims at fully integrating the active electronics within the floating probe, processing techniques used in various manufacturing steps do not need to be CMOS-compatible. This is possible thanks to the chip containing the integrated circuitry being bonded to the probe at the very last step. This characteristic allows

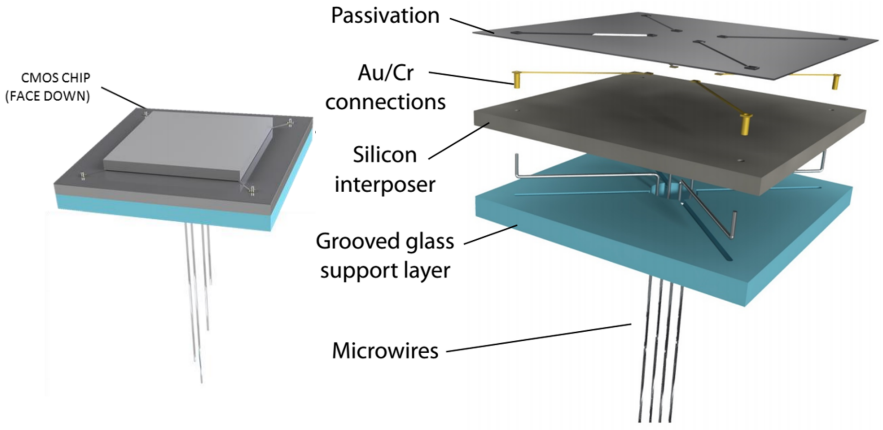


Figure 3.6.: Schematic of the V1 ENGINI probe assembly showing different components. The active IC is to be flip-chip bonded on the top of the probe, making contact with four centre pads of metal interconnections.

high temperature and high electrostatic field processes without the risk of damaging the electronic circuitry. Moreover, the cavity formed between the integrated circuit and the silicon interposer could be hermetically enclosed (for example, utilising a eutectic seal), thus extending the chronic performance of the device. A further level of encapsulation can be achieved by passivating and encapsulating with a polymer coating layer, such as biocompatible Parylene-C or PDMS. The overall design of the probe is also suited for a large number of recording channels. However, the maximum channel quantity is limited by the size of the chip allowing for the accommodation of new channels.

Probe microfabrication

The glass part of the interposer is to support microwires mechanically. It was made of a four inch-diameter, 500μm thick Pyrex 7740 glass wafer, which was patterned to form grooves and vias using mechanical micromachining. Using any chemical etching methods on the glass to retain original dimensions is hindered because of the isotropic nature of the process. Grooves were created by running a dicing saw up to a depth of 200μm across the rotated wafer, after which the substrate was turned by 90°, and the process was repeated. The wafer was then diced to 4×4 mm dies, and the 0.4 mm wide central through-hole was formed at the crossing point of the grooves. The hole was created by mechanical means using the diamond drill or by repeated laser engraving. Achieving higher yields is more likely with the former method; however, laser engraving is more expensive and time-consuming. After dicing, samples were released from the dicing tape, washed in DI water ultrasonic bath, followed by cleaning in the Piranha solution (3:1 mixture of sulfuric acid and 30% hydrogen peroxide) and the oxygen plasma.

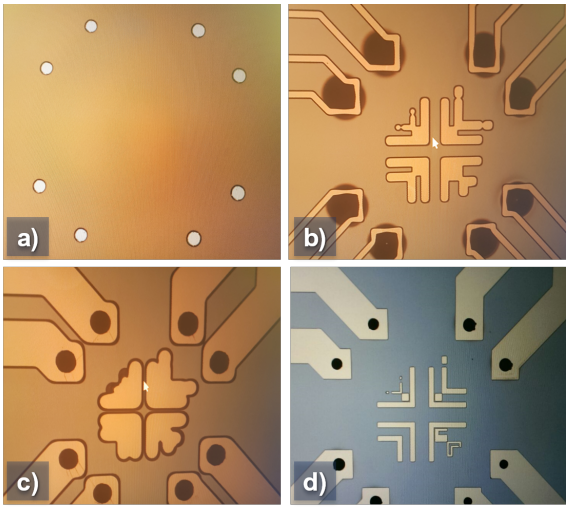


Figure 3.7.: Over-TSV DLW/ metallisation process optimisation: a)TSV mask b-c)Process optimisation d)Final result

The silicon interposer layer was fabricated using a 3-inch diameter, 380μm thick DSP silicon wafer. All photolithography steps were performed with a direct laser lithography setup directly on the wafers. This allows for a faster prototyping time compared to standard mask processes. First, substrates were coated with 150 nm thick PECVD silicon oxide and patterned with four circular openings of different diameter sizes per chip (125, 150 and 175μm diameters). As a mask layer for the through-wafer etching, a thick SPR-220 photoresist was used. Next, the oxide layer was removed in buffered HF, and the wafer was etched through using a custom-designed Deep

Reactive Ion Etching (DRIE) process. The process for the TSV forming was optimised to minimise the angle via taper. Once through-vias were formed, the photoresist mask was removed, and the underlying oxide etched away. The substrate was then cleaned and either thermally oxidised to 180 nm or only the top surface was coated with a 300 nm PECVD oxide. Afterwards, the top interconnection layer connecting through vias with the middle area of the chip where CMOS is to be mounted face down was patterned in the lift-off process. For that purpose, 30 nm chromium and 90 nm gold layers were sputtered. To ensure proper coverage of vias with the metal, a custom laser writing process on AZ MIR 701 photoresist was designed and optimised (pictured in Figure 3.7), as seen on the eight-wire interposer substrate surface). To provide the top passivation and ensure no electrical shorts were formed between neighbouring lines, a 150 nm thick PECVD layer

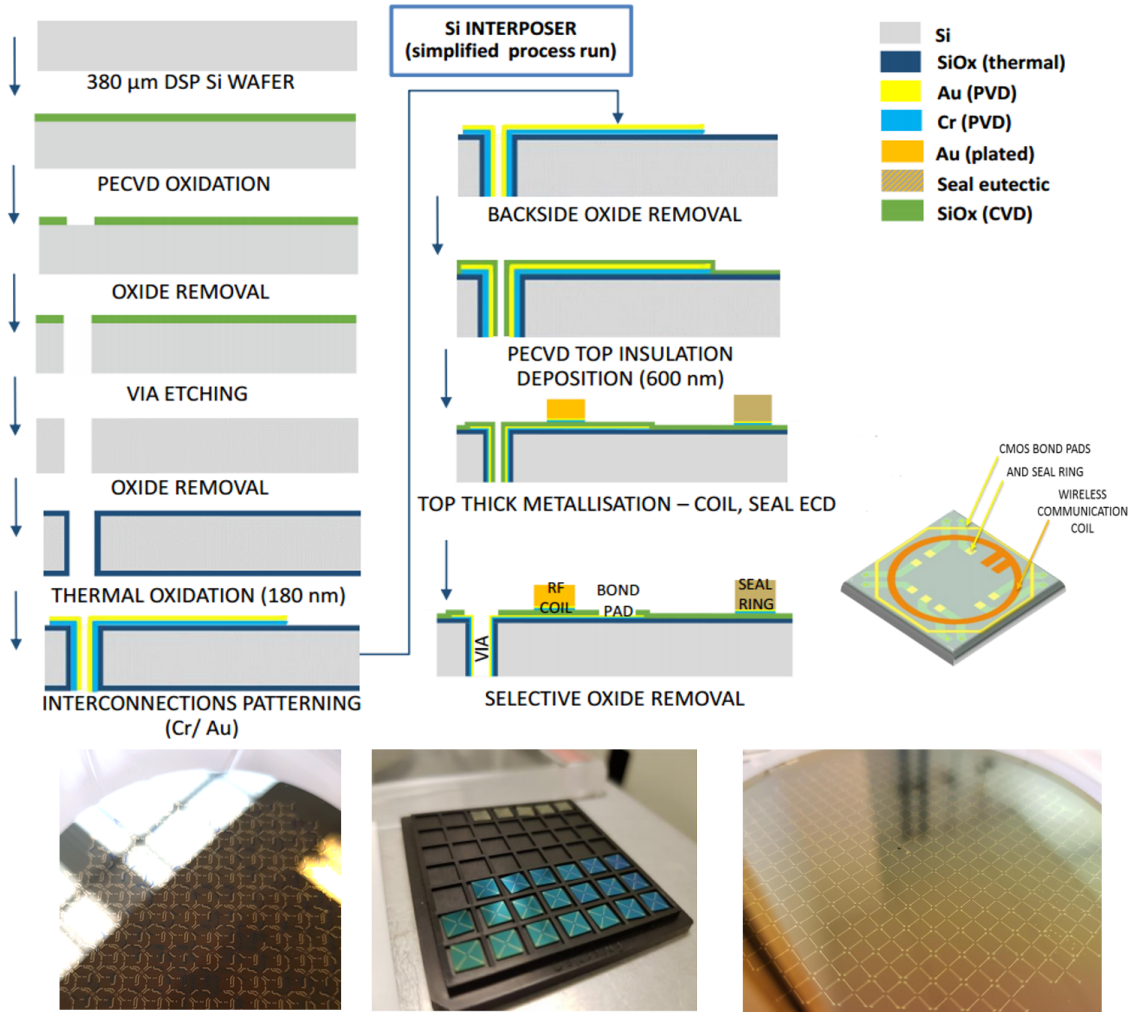
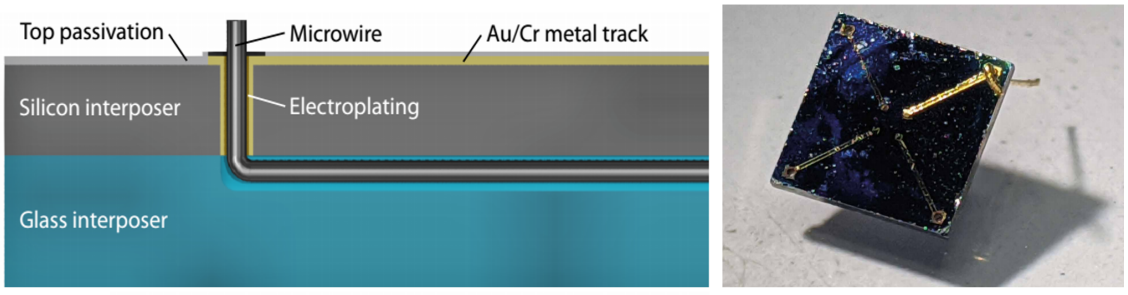


Figure 3.8.: Simplified microfabrication process flow for the silicon interposer, interposer layout and the real-life pictures of its realisation. Bottom row from left to right: images of the TSV wafer with metal interconnections for the eight-wire probe, PECVD-insulated chips after dicing, the TSV wafer with metal interconnections for the four-wire probe.

of silicon oxide was deposited. In order to secure the electrical access to vias and open bonding pads for the IC connection, wafers were patterned to locally remove the oxide in a buffered oxide etch. Finally, wafers were diced, and the resulting samples were cleaned in the Piranha solution and the oxygen plasma. Two versions of the silicon interposer differing by the number of supported microwires were fabricated, one for the four-wired probe and one for the eight-wired version. Microwires used in the V1 prototype of the ENGINI probe were made of 75 μm thick tungsten. For that purpose, a pre-straightened microwire was acquired from a commercial vendor (Goodfellow Cambridge Ltd., UK), cleaned in the IPA solvent bath, cut to the correct length using wire cutters and then manually bent to their final shape before insertion. The use of tungsten was motivated by the high stiffness of this material, which aided in the proof-of-concept assembly. As a final probe microwire material, thanks to its biological inertness, chemical stability and small diffusion current density, Niobium was identified as it could provide superior noise performance in the LFP frequency band [1]. A simplified process schedule for the V1 ENGINI probe along with interposer images can be seen in Figure 3.8.

Probe assembly

The probe was manually assembled by threading the microwires through openings in the silicon interposer. To assemble the probe, a special jig to hold it in place was designed. The glass interposer was then placed machined surface up, and pre-bent wires were accommodated in the grooves. Next, the silicon interposer part was placed on the top to accommodate microwires inside previously etched vias. In the event of the adhesive leaking or the need for better mechanical stability, in place of an adhesive bonding, glass-Si electrostatic bonding can be employed instead. The glass-silicon pair was then joined together in the process of adhesive bonding with cyanoacrylate glue to form a uniform structure. Once the mechanical stability was secured between the substrates, wire endings protruding from silicon vias were cut down close to the substrate layer using wire cutters.



a) b)

Figure 3.9.: a) Schematic cross-section view of the electroplated connection between the microwire and silicon interposer in prototype generation ENGINI's probe b) Image of the probe head's surface after in-via wire electroplating.

To provide electrical connectivity between middle bonding pads and electrode leads, microwire ends were electroplated within vias with gold in the ECF60-plating solution until the deposited layer filled the inside of a via as depicted in Figure 3.9. According to the application's specific needs, the recording side of the microwires could finally be cut at different heights.

Design findings

Despite several design considerations that have been taken into account during the V1 manufacturing process, the assembly according to the presented scheme resulted in non-repeatable results and a significant process variation (Figure 3.10). Forming wire interconnections in the process of electroplating was found particularly challenging. For the electroplating to be successful, the correct selection of a through-via size for a given microwire diameter is of the utmost importance. Too-large dimension mismatches often resulted in a poor electrical connection and mechanical non-stability, compromising the device's performance. Too small of a diameter difference led to threading problems, as TSVs are etched with narrowing profiles so that the outlet opening is always slightly larger than the inlet.
During electroplating, the cathode contact was made by attaching a connector clip to the protruding end of the in-via microwire. Holding that contact itself was difficult given the size of microwires, but also, passing the current through has led to the gold over-plating above the insulation layer. In some cases, the combination of plating current, high mobility of solution's ions and its reactivity led to complete lifting off the passivation layer. This situation prevents the further possibility of the CMOS and wireless coil mounting as they would short all electrode connections. The occurrence of the overplating, as depicted in Figure 3.9 b, could be prevented by depositing a layer of masking material over the

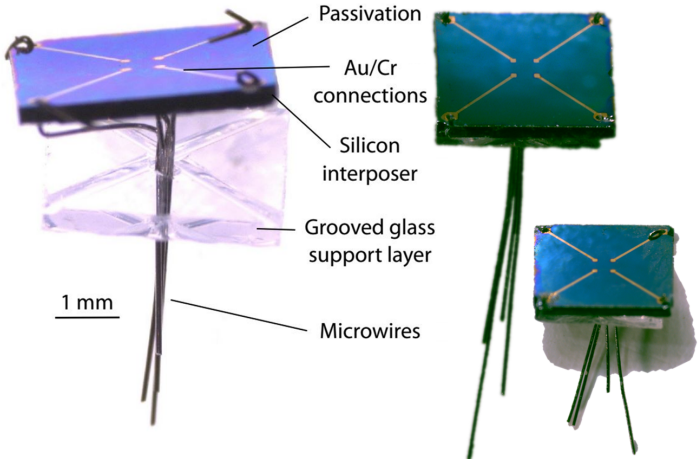


Figure 3.10.: Assembled ENGINI V1 implant module prototype, excluding the IC chip and the communication coil.

interposer sample during plating. In this instance, it was not applied due to the existence of a passivation layer which was believed would prevent plating over the sample's surface.

The most significant obstacle that led to the redesign of the concept of the ENGINI probe is related to the assembly yield. Manual assembly of the V1 probe required accurate threading of micrometre-sized parts and the exact alignment, which is time-consuming and could be problematic to adapt to large-scale production. During chip stacking, microwires, owing to the high stiffness of tungsten, acted like a spring necessitating considerate pressure to enable joining glass and silicon. What is more, with this design, all assembly must be done at the die level, thus being difficult to scale up and ensure good repeatability.

3.2.2. Two-module approach

Based on the design shortcomings identified for the V1 ENGINI probe, a second approach to the device's redesign was made. Initially utilised design has subsequently been refined further to reduce the level of complexity in the assembly process by alleviating the need for two interposers. Instead, two separate modules are used: the microwire module and the microelectronics module. As previously, the probe is constructed using standard microsystems materials and microfabrication technologies, thus limiting the total number

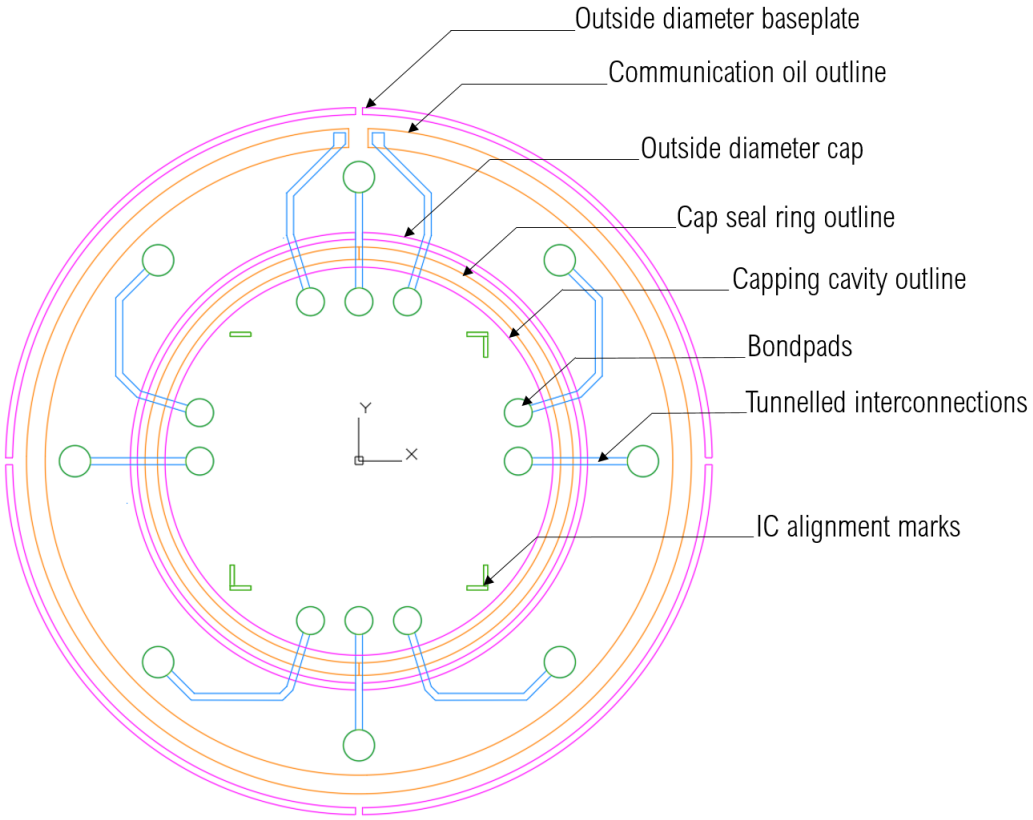


Figure 3.11.: ENGINI V2 microelectronics module mask design.

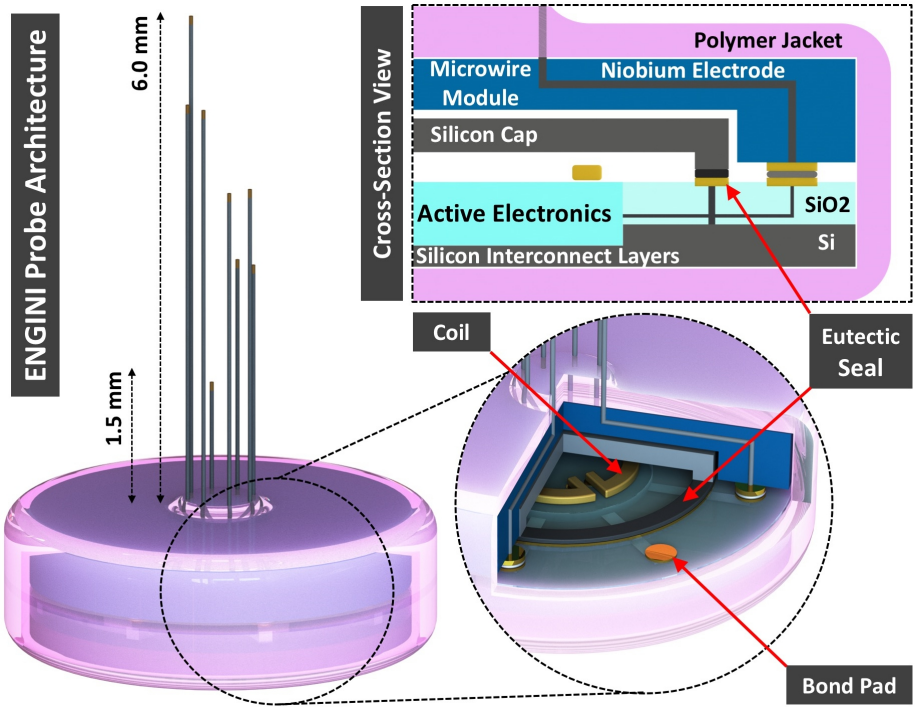
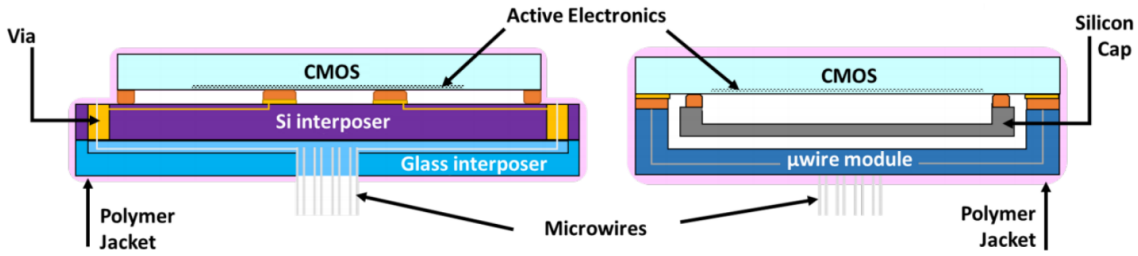


Figure 3.12.: ENGINI probe construction and the packaging concept, combining two sub-systems: hermetically-packaged microelectronics module; polymer-encapsulated microwire array. Illustration not to scale.

of manually performed steps. This allows for the miniaturisation of system components, parallel manufacturing and easier integration with the electronics. To possibly limit the total number of steps requiring high precision manual handling, it was decided that the microwire interposer should be outsourced.

The microelectronics module is essentially a micropackage that houses the active CMOS electronics. It comprises two mm-sized, rounded silicon substrates joined together by a continuous seal of the gold-tin eutectic. The joint is located around the edge between substrates, and as a consequence of being less than 100 μm in width, it does not significantly impact the size of a whole probe. CMOS protection is ensured in one step by capping the surface with Au:Sn-eutectic alloy bonded silicon lid, like described in Chapter 4. The lid would be manufactured with an inside cavity to accommodate gold-based wireless communication coil placement. Connections to the CMOS are located outside the seal ring, as they are tunnelled from the active electronics area to the perimeter of the chip via deeper BEOL layers. The connection of these pads to the microwire module can be then achieved through a solder bump deposition followed by flip-chip bonding. Schematic visualisation of the probe design is depicted in Figure 3.12, while the details of redesigned masks, for which the new microfabrication approach was designed, is depicted in Figure 3.11.

Microwires mechanical stability is achieved by fabricating the array as a separate assem-



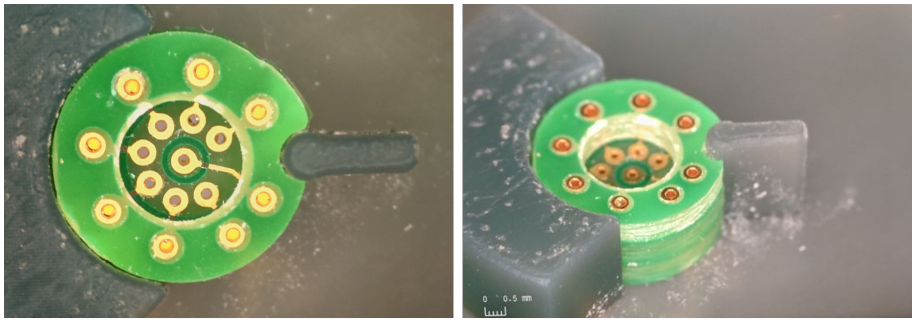
	First generation	Second generation
Approach	Three substrates/chips stacking: Capping wafer, CMOS, Si interposer, glass interposer	Two modules assembly: microwire module (independently developed) and head module (CMOS+ Capping wafer)
Methods	CMOS post processing, electroplating, Si interposer formation , glass interposer formation, TSV etching, chip stacking, eutectic/solder bonding, anodic or adhesive bonding, manual microwire handling, microwire electroplating	CMOS post processing, electroplating, capping wafer formation, membrane etching, chip stacking, eutectic/solder bonding
Materials	Silicon, AuSn, Au, glass	Silicon, AuSn, ceramic microwire module
Interconnections	Silicon interposer - based	CMOS-based
Reconfigurability	Not possible	Possible with different recording (microwire) modules

Figure 3.13.: Summary comparison between two proposed architectures of ENGINI probes.

bly. Thanks to that, there is no need for the manual embedding of microwires which has been proven very challenging earlier. The benefit of the glass-silicon interposer system was that its Si-part enabled planar connections to the microwires. In the second generation of ENGINI probe assembly, that can be achieved by employing the fabrication technology allowing for buried metal interconnections. One of the technologies enabling that is the LTCC co-firing, which in short relies on co-firing multilayers of metal-patterned thin ceramic films under pressure. As a result, uniform ceramic shapes with embedded metal tracks and vias (if needed) can be fabricated.

Since the microwire module is designed as a one-piece, a multitude of versions can be developed in parallel, only to be assembled at the end of the probe's production, thus allowing for a certain degree of reconfigurability. In contrast with one central opening accommodating all the microwires in the form of a bundle, as seen in V1, in the central part of the mould of the V2 probe's microwire module, there are several straight vias where microwires are to be placed. Vias contain pre-metallised walls which connect through the buried metallisation to the edge of the module, where surface pads are located. The solder reflow process can provide fixation and establish an electrical connection between microwires and vias. The architecture of the microwire module is based on a similar approach as in the V1 probe. The characteristics comparison between two generations of proposed ENGINI probe architectures and simplified cross-sections are presented in Figure 3.13.

The final step in the fabrication of the V2 ENGINI probe is the assembly of the two modules. Using bond pads on corresponding planar surfaces as bonding faces, two parts can be joined together by solder or thermocompression bonding. The assembled device can be then coated with a layer of barrier polymer, such as silicone or Parylene-C, to provide an



a) b)

Figure 3.14.: PCB mock-up wire module before assembly. A) Top view B) Side view

additional level of protection and promote tissue integration.

Microwire module early verification

Learning from the challenges faced during the fabrication of module components in the V1 probe, it was decided to verify assembly procedures before designing a custom CMOS chip and committing to outsourcing microwire module production. Chip hermetic sealing capability has been proven with tests described in Chapter 4 and designing the CMOS chip to fit the proposed architecture is within NGNI's group expertise. Two areas of concern left are establishing mechanical and electrical connections between microwires and ceramic modules and connecting two final assemblies. The latter can only be achieved once LTCC prototypes are fabricated; however, testing module to microwire connectivity could be proven by testing the microwire module mock-up realised in the PCB technology.

For this purpose, the PCB-equivalent of a microwire module was designed and fabricated*. The size of the module needed to be slightly enlarged, and some layout's elements adjusted because of the PCB technology limitations. To facilitate microwires placement, a custom assembly jig was 3D printed*. Next, pre-straightened microwires were cut to different lengths, which would allow for easier handling. To enable connectivity between the microwire and the module, remelting various sizes of lead-free BGA-balls dropped to the vias was tested. To do that, each PCB module was first degreased, wiped clean and mounted in the previously prepared jig. The ends of microwires, which are to be surrounded by the remelted solder, were cleaned and dipped in the drop of a flux. Next, using precise tweezers, microwires were manually placed inside the vias. Using the assembly jig significantly eased the entire procedure, which can be readily automated in the future. Next, solder balls were transferred with the use of a syringe needle and carefully dropped to the inside of each via. Next, the entire module was heated up with a heat gun until BGA balls melted and the contact was established.

* The work of Mr Matthew Cavuto

Subsequently, the electric connection was inspected with a standard laboratory multimeter. However, only two out of eight microwires have exhibited connectivity to the PCB base. Encountered problems were likely due to problems with solder balls remelting as a result of very little flux used. What is more, because of the temperature-stability of the PCB module, delivered heat was likely insufficient to melt the solder, especially given that it was placed inside the vias. From the mechanical stability perspective, microwires were held in place well, and manual pulling tests using tweezers failed to displace them. However, it is envisaged that microwires would be additionally secured with a biocompatible fast-setting adhesive such as cyanoacrylate after establishing an electrical connection.
To inspect the state of BGA-balls dissolution, SEM inspection was carried out, which has indeed confirmed the remelting problems (Figure 3.15). Under closer examination, it has become apparent that the incomplete solder dissolution took place as several BGA-balls remained with spherical shape despite repetitive heating up above the melting temperature. It is likely caused by a layer of native oxide coating each sphere, thus preventing it from melting and collapsing. The connection was established only when a larger amount of flux was used, then some of the deposited solder volume melted. Based on these results, it was established that better-suited electric connections would be tin-rich gold-tin eutectic preforms in a cylindrical shape or the process of tin electroplating directly onto wire tips.

Design findings

Compared to the first version of an implant architecture, the proposed second iteration reduces the probe complexity by manufacturing the package as two independent modules. Thanks to that, each of the parts can be manufactured at a large scale in environments best suited for each of the module's requirements- head module on the wafer-level employing MEMS techniques and the microwire module by LTCC co-firing and lamination processes.

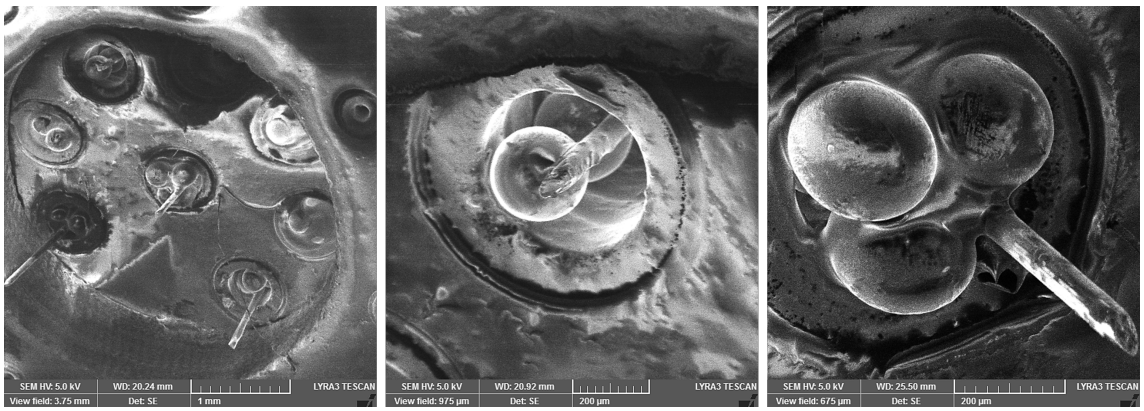


Figure 3.15.: SEM pictures of PCB-wire module with microwires fitted with BGA-solder balls.

Each module is responsible for providing crucial qualities to the device- CMOS protection and wires interconnections. Such an approach also increases the probe's versatility as different wire modules can be produced in parallel and fit the one base module at the end of the processing schedule. What is more, the overall production yield can be enhanced, as an individual fault of one probe's parts does not constitute the entire device failure. Each module's connectivity ports and the electronics reliability can be tested prior to the final assembly, further minimising an error risk.

Nevertheless, the suggested design needs to undergo further optimisation, especially within the aspect of an assembly process. Different solders and in-via solder delivery techniques must be tested to allow for the microwires' safe and easy placement inside the module. Similarly, techniques of modules stacking must be carefully reviewed and the manual assembly automated. Assuredly, the entire probe must also undergo biocompatibility and accelerated ageing tests, including sterilisation procedures.

3.3. Conclusions

In this chapter, approaches to the design of the BMI probe architecture were presented. After a general introduction about materials, electrodes and interconnections in neural interfaces, design considerations were introduced, specifically in relation to the ENGINI project packaging requirements. The selection of materials, processes and geometry was justified concerning the final application of the device.
Because of the microwire integration necessity, a modular approach to the probe package was presented. As a result, two different versions were considered, of which one was manufactured and the second designed and early-verified so far. Design changes covered the way microwires connect to the electronic unit, the number of materials and substrates used and technologies employed. Drawing from experiments on the effectiveness of the eutectic sealing in hermetic packaging for implantable applications, CMOS chips are protected by reflown Au:Sn metallic frame in both designs; additionally, the V2 improved design is reinforced by the microwire module cover.
As a result of these early prototyping stages, the following considerations were made:

- From a perspective of minimising the failure risk, it is beneficial to split the fabrication of implants into parallel processes focused on the development of modules that are different in technology or purpose. That way, it is possible to "fail early" and introduce necessary design changes only on the fragment of an entire design before a costly and time-consuming manufacturing process commences. The modularity of the design additionally offers eased reconfiguration possibilities in regards to the number, length and diameter of wires placed.

- Proposed assembly techniques can enable building up functional neural probes, however only in small numbers. The first generation of a probe was fully manually assembled, thus suffered repeatability and assembly accuracy problems. The issue was alleviated in the microwire module of the probe's second generation, thanks to the 3D-printed assembly jig, which allowed control over microwires protrusion and eliminated some of the handling problems. Whereas this is acceptable for small-scale, academic or proof-of-concept adaptations, the automation process must occur if larger scales of hundreds of probes are considered. Especially microwires preparation-such as cutting, bending and handling would greatly benefit from specially dedicated devices and processes so that no manual handling is involved.

- Establishing electrical connections between microwires and the PCB, or in the future ceramic-based microwire module by remelting in-via-dropped solder spheres is possible. However, it suffers from difficulties with placement accuracy and solder reflow uniformity. It would be beneficial in the future to test out a similar approach but using cylindrically shaped solder preforms, preferably made of tin-rich Au:Sn

solder as it has been shown biocompatible (Chapter 5.4). These could be placed directly onto microwires. Alternatively, the approach of the microwire electroplating or biocompatible solder paste deposition could be reviewed.

- With the current state of the art, in order to establish robust interconnections between microwires and the on-chip CMOS electronics in implantable applications, the only viable solutions are external connectors and some form of interposer technology. Any other direct way of coupling microwires to bond pads, such as wire, thermocompression or thermosonic bonding, is deemed inadequate because of the poor mechanical stability of the joint. Without reinforcement, given the size, especially the length of the microwires, leads could easily be broken away from the interface. Hence, microwires must be supported by placing them in either a connector or an interposer. Assuredly, given their form factors, external connectors are too large for future miniaturised implantable devices. Here, the interposer is understood as any form of the redistribution of microwires inside other material directly attached to the electronic chip, such as ceramic plates, glass, plastic holders, and alike.

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4. Au:Sn bonding for applications in implantable neural devices micropackaging

Notwithstanding rapid progress in the field of construction and manufacturing of chronic implantable neural devices described in the Chapter 2, the issue of providing devices with compact and reliable packaging remains one of the main challenges left to overcome. Novel implantable devices ever-expanding capabilities more often include fully wireless communication and on-node data processing, thus imposing more rigorous requirements for device packaging [3].

To ensure the IMD's electronic core long-term performance stability, it is essential for the implants' package to remain hermetic. Moisture ingress gives rise to the corrosion and dissolution of materials, degradation of on-chip circuitry, and mechanical stresses, leading to compromised stability. Until now, the majority of implants were packaged by encasing entire systems in metal or glass cases or by using thick outer coatings, mainly made of medical-grade silicones [4, 5, 6]. Typically, these solutions either do not provide an appropriate level of hermeticity or are too large and not fit for wireless systems with integrated electronics. At the same time, it is not certain whether standard IC insulation layers alone are sufficient in providing enough protection against the inherently wet and often corrosive character of the tissue environment over a long time [7, 8, 9]. Drawing from the MEMS-based micropackaging technology perspective (Figure 4.1), different approaches to implant packaging could be employed. Gold-tin-based eutectic bonding presents the potential for achieving low-footprint seals with low permeability to moisture at process temperatures below 350°C.

This chapter presents a brief review of wafer-level bonding methods used for sensors packaging, focusing on methods applicable for safe and reliable integration of CMOS devices in implantable applications. The design of the gold-tin-based micro packaging approach is then proposed and discussed, along with an analysis of the most critical seal design parameters found, hermeticity and reliability assessment.

A portion of the material presented in this chapter has been published in [1, 2]

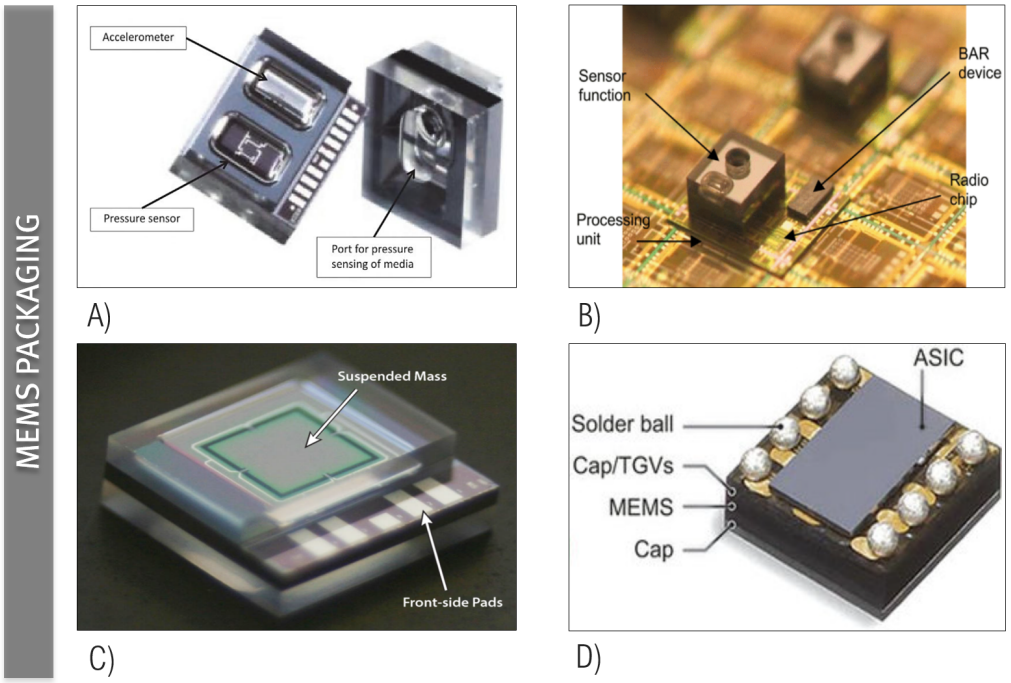


Figure 4.1.: MEMS-based packages examples. A) Sensonor AS triple-stack multisensor [10], B) E-Cube tire pressure monitoring system [11], C) Vibration sensor [12] D) 3-axis accelerometer [13].

4.1. Wafer-level bonding techniques

By employing techniques developed for the MEMS industry, CMOS chips can be protected immediately after fabrication using wafer or die-level bonding (Table 4.1). At the wafer level, CMOS can be secured before die singulation, thus increasing the packaging process throughput and decreasing the resulting price of the single unit. At a die level, throughput is smaller, but process control can be done more accurately.
Bonding is a set of various technological procedures that enable the creation of a permanent junction between solid materials of flat and smooth surfaces. Bonding plays a crucial role in today's microtechnology, enabling packaging, assembly, and connection of various substrates using methods leveraging different physical phenomenons. In general, bonding is based on joining two flat substrates or interfaces together, with or without an intermediate layer of sealant, and applying a combination of temperature, force, and pressure to form a cohesive, mechanically stable bond. Bonding extends standard technological capabilities to form complicated microstructures, as it allows the joining of multi-layered micromechanical structures into one. It is used in MEMS, photonics, and heterogeneous integration applications to enable die stacking and provide environmental compatibility.

Depending on the characteristics of a process, wafer bonding methods can be divided into two main groups: direct bonding and intermediate layer bonding. The first one typically

results in the formation of a chemical bond at the interface via the application of high electrostatic fields, temperatures or pressure, and is greatly influenced by the surface properties of the samples to be joined, such as smoothness, flatness, and water affinity.
The second bonding type, intermediate bonding, is more tolerant to the lower surface finish quality because it uses layers of another material sandwiched between bonding surfaces as a joining medium. Adhesives, polymers, glasses, or metals are typical materials used as an intermediate layer.
ENGINI project envisages the development of a fully wireless, millimetre-scale free-floating intracortical BMI capable of in-situ data analysis. As mentioned in the section 2.4.3 of this chapter, this must involve the presence of CMOS chips directly at the implantation site. Integrating electronics and RF components onto ENGINI probes imposes several limitations on the choice of materials and fabrication processes. Typically, the main requirement given to neural electrodes aside from their performance is the biocompatibility.

Table 4.1.: Most popular large-scale bonding methods and their applications.

	Direct Bonding		**Intermediate Layer Bonding**				
	Anodic	**Direct**	**Adhesive**	**Eutectic**	**Glass Frit**	**Thermo-compression**	**Ultrasonic/ Thermosonic**
CMOS compatibility	No	No	Yes	Yes	No	Yes	Yes
Temperature range	250-500 °C	250-500 °C	<400 °C	200-400 °C	400-1100 °C	350-600 °C	200-300 °C
Bonding pressure	None	Very Low	Low to medium	Low to medium	Low to medium	High	Low to medium
High vacuum sealing	Yes	Yes	No	Yes	No	Yes	Yes
Surface quality requirements	Medium	High	Low	Low	Low	Medium	Medium to high
Sensitivity to particles	Medium	Very high	Low to medium	Medium	Low	Medium	Medium
Applications	MEMS, sensor packaging	SOI wafers, photonics	MEMS, sensor packaging, 3D ICs	Hermetic packaging, flip chip bonding	Sensor packaging	3D ICs	MEMS, 3D ICs
Advantages	Low CTE mismatch, high bond strength	Hermetic, high bond strength	Versatile, particles insensitive	Hermetic, self-aligning	Nonconductive, mature process	Hermetic	Rapid, low process temperature
Disadvantages	High electrostatic field required	Substrate requirements, high temperatures	Not hermetic, limited temperature stability	Eutectic composition control, solder flow	Large bond frame, complex	High forces, difficult on the wafer level	Complex process setup, difficult on the wafer level

Regarding the ENGINI probe, total RF and CMOS compatibility and size in the range of a few square millimetres are required. That necessitates using materials, architectures, and methods that guarantee the implant's life-long inertness and stability while ensuring support for electronics and wireless transmission in a single package. All fabrication steps must not include high-temperature processing while designing with the minimal use of metals near the communication coils to avoid unnecessary electromagnetic interference. In the aspect of the requirements mentioned earlier, the majority of low-permeable materials cannot be included. Conformal metal housing would make RF-wireless communication impossible; glass-silicon bonding requires CMOS-incompatible high electrostatic field, whereas global glass coating and ceramic encapsulation involve the application of temperatures exceeding the maximum allowable CMOS temperatures.

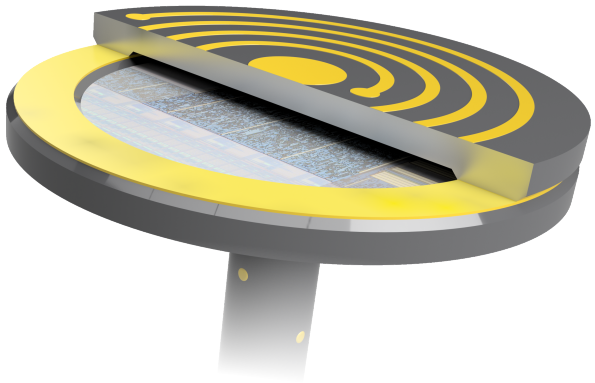


Figure 4.2.: Concept of the ENGINI probe head architecture. CMOS electronics is protected by a metallic seal ring and silicon cap.

From a wide range of bonding techniques available in electronics and MEMS packaging, only a few do not require high-temperature processing or contain toxic materials while providing a good seal hermeticity, making them applicable for implantable devices containing embedded ICs [14, 15]. Amongst these, eutectic bonding can be performed using relatively relaxed environmental parameters, while the availability of several different eutectic compositions enables the choice of the one that would suit the application needs the best. The prospect of hermetically enclosing implant electronics at a wafer-scale using narrow metal seal rings with the addition of in-silicon feedthroughs is highly desirable. A clear advantage of frame-based metal sealing is the tolerance to substrate unevenness and very low permeability to moisture, superior to even those of silicon or glass [16]. Both the thickness and width of the joint can be in the micrometre range, thus contributing to the overall size minimisation. It is the method of a great fit for the hermetic CMOS sealing thanks to the wide range of solders, comparatively low processing temperatures (Table 4.2), and good tolerance to surface non-uniformities.

Following experiments with solder deposition described in the Chapter 5, Au:Sn eutectic solder bonding was selected as a joining technique of preference in the ENGINI probes fabrication run. The decision was made on the ground of Au:Sn promising biocompatibility [17], stability in harsh environments, and CMOS-compatible temperature range, as op-

posed to alloys containing silver, copper, and aluminium. The outline of a seal is going to be placed around CMOS circuits and sandwiched from above by an additional substrate, thus creating a lid consisting of a monocrystalline cap and metallic walls, which should be sufficient to provide the appropriate level of hermeticity (Figure 4.2). An additional preventive measure, an outer jacket made of less permeable materials, such as Parylene-C, can be deposited.

4.1.1. Eutectic Bonding

Eutectic bonding belongs to the family of intermediate layer joining methods as it uses layers of specific alloys as a sealant holding two parts together. The unique advantage of eutectic bonding (or soldering) is typically a lower temperature of alloy melting as compared to the melting temperatures of individual constituents that make up the mixture. That allows using materials that otherwise could be too temperature-demanding, such as gold or copper, and enables one to prevent thermal damage to the substrates to be joined. Solder alloys in microelectronics are typically chosen so that their melting temperature does not exceed 350° C, to comply with CMOS compatibility requirements. Because of that, often near-eutectic material compositions are preferred in order to minimise alloy's melting temperature.
Eutectic alloys are mixtures of high melting metals (usually gold, copper, or aluminium) with the addition of low-melting metals (such as tin or indium, or germanium). Thanks to their low viscosity, they can spread easily over the bonding area without needing an external pressure application. Thanks to the unique characteristics of eutectic alloys, low-void, conductive joints can be formed for a variety of applications, from components soldering, die-attach, and bumping to hermetic sealing. To aid the flow of the solder and minimise the possibility of voids formation, eutectic bonding is typically assisted by the application

Table 4.2.: Most popular, Pb-free eutectic alloy compositions, their melting temperatures and critical characteristics.

Alloy:	**Eutectic Composition [wt%]**	**Eutectic Temperature [° C]**	**Characteristics**
Au:Sn	80/20	280	- Steep liquidus lines
Au:Si	82/18	363	- Long process times - Under-solder-metallisation challenges
Au:Ge	71/28	423	- High eutectic temperature - Native oxide removal difficulties
Au:In	0.6/99.4	156	- SLID bonding - Complex phase diagram - Premature mixing difficulties
Al:Ge	49/51	419	- High eutectic temperature
Al:Si	87.5/12.5	580	- Very high eutectic temperature
Sn:Ag	96.5/3.5	221	- Native oxide removal difficulties - Silver cytotoxicity
Sn:Cu	95/5	231	- Copper cytotoxicity

of moderate force. Frequently, the procedure is performed either in a vacuum or in an inert atmosphere to prevent materials from oxidising prematurely.

Eutectic bonding is a physical process relying on the direct transformation between solid and liquid states without passing a two-phase equilibrium. Eutectic reaction is invariant- to occur, alloy constituents are required to be present at the specific composition and temperature. Typically, without the application of external heat, solid states of alloy constituents are insoluble and do not mix. It is only above a particular temperature, known as eutectic temperature or eutectic point, and at a specific ratio of alloy's components when the phase transformation from solid to liquid can occur. It is also at the eutectic point when the phases will solidify directly from the melt when cooling down.
At a eutectic point, components making up the alloy are in thermal and chemical equilibrium, with two solids and liquid coexisting simultaneously. Upon cooling down, the solid eutectic macrostructure will be formed, with the morphology dependent mainly on the component's nucleation characteristics and the dynamics of the cooling process.

Of the eight most popular Pb-free eutectic alloys commonly used in the industry (Table 4.2), three (Au:Ge, Al:Ge, Al:Si) require process temperatures above 400° C, which precludes their use in CMOS-containing devices. Of the rest, the other two (Sn:Ag and Sn:Cu) contain cytotoxic elements, which makes them incompatible with implantable bioelectronics applications. All three remaining alloys are based on gold, and the choice between them is up to their process characteristics. The best from the thermal budget requirements is the gold-indium bonding. However, the very high indium content of the alloy creates problems with premature oxidation, and low activation energy causes a premature intermixing of bond materials to occur. The final choice for applications in CMOS-containing implantable medical devices is then between the gold-tin and the gold-silicon eutectic compositions. Between them, gold-tin requires excellent control over the alloy's composition, while the gold-silicon eutectic involves higher process temperatures and needs high planarity and parallelism of bonded surfaces.

4.1.2. Gold-Tin alloy

Gold-tin solder has been widely used in the semiconductor and MEMS industries, mainly for die attachment but also for hermetic sealing, predominantly in RF and inertial applications (Table 4.3). Thanks to the high percentage of gold, the unique characteristic of Au:Sn solder is the availability of fluxless processing. Gold content also makes the surface oxidation minimal. However, depending on the deposition method, the amount of gold needed can lead to a price increase. Because tin oxidises, the alloy is usually reflown in either vacuum or forming gas atmosphere. However, with suitable reflow parameters, bonding without oxide reduction is also possible. The minor difference between the thermal expansion coefficients of Si and Au:Sn makes it suitable for high-temperature devices. Au:Sn does not suffer from outgassing on its own; therefore, it can be adapted for vacuum applications.

Gold-tin joints are brittle and do not undergo plastic deformation due to the significant presence of intermetallic phases AuSn and Au_5Sn. Therefore, care must be taken to avoid too much build-in stress that arises at the interface. It is essential to control the deposition of eutectic composition correctly, as at precisely 80/20 Au:Sn by weight (71/29 by molar content), the low eutectic temperature of the alloy is paired with desirable mechanical properties of Au_5Sn intermetallic phase. The alloy allows for a hermetic sealing both in ambient as well as in elevated service temperatures, thanks to the high alloy strength. In fact, despite being made of two relatively soft metals, Au:Sn material strength is akin to those of high-temperature brazing materials, while at reduced processing temperatures [23]. Of all hard solders, Au:Sn is characterised by the lowest melting

Table 4.3.: Selected applications of Au:Sn solder rings for hermetic sealing.

Application:	**Details:**	**Year**
Smart inertial MEMS sensor systems	- Chip-to-wafer integration - Au:Sn frame: 18 μm height, electroplated - Bonding: 300° C, 6 kN force	2008 [18]
RF MEMS switch	- Wafer-level integration - Au:Sn frame: 5 μm height, electroplated - Bonding: 310° C	2010 [19]
Piezoelectric silicon resonators	- Wafer- and array-level integration - Au:Sn frame: 4 μm height, electroplated	2011 [20]
MEMS microresonators and microbolometers	- Chip-level integration - Au:Sn frame: 20 μm, electroplated - Bonding: 340° C	2013 [21]
MEMS timing devices	- Wafer-level integration - Au:Sn frame: 19 μm, electroplated - Bonding: 300° C	2013 [22]

point of 280° C. Strict control of Au:Sn concentration is paramount. When alloy becomes Sn-rich by even a mere few per cent, eutectic temperature raises dramatically, causing an inability to form a joint. Another major drawback of using the Au:Sn system is directly associated with tin, which produces a native oxide layer and therefore reduces its molar percentage in the composition. Both an advantage and disadvantage is larger alloy's melting temperature after initial reflow, which is caused by an increase in the total alloy's gold content because of an adhesion layers consumption. This property is useful for the packaging of devices for high-temperature applications. However, in the die-attach, the increase of liquidus point complicates the possibility of a future rework. Gold-tin alloy is also characterised by a good wettability and steep liquidus line, which accounts for overall beneficial reflow properties. The range of Au:Sn applications is all the wider thanks to the alloy's high thermal and electrical conductivity. Characterised by high corrosion and oxidation resistance, gold-tin alloy holds a promise of the material capable of a hermetic sealing for devices operating in challenging environments. Table 4.4 summarises principal physical properties of $Au_{80}\,Sn_{20}$ alloy material.

Au:Sn thermodynamic properties

Outstanding qualities of the gold-tin alloy are a result of thermodynamic characteristics, which can be described with the use of the alloy's phase diagram (Figure 4.3). Of many binary solder systems, Au:Sn presents itself as one of the more complicated from the thermodynamic perspective. The research on Au:Sn has been ongoing for over a century, and yet some of more Au-rich areas are still under observation today [24, 25].
The look on the phase diagram reveals that the Au:Sn system consists of two eutectic points, six intermetallic compounds, and three peritectic points. To a certain degree, the complexity of the Au:Sn system, and the fact it contains as many as four stable intermetallic compounds, is a result of the substantial difference in thermodynamic properties of alloy's constituents. The difference in the electronegativity between tin and gold is 0.5, larger for Au (2.3) than for Sn (1.8). Of all IMCs phases, three (AuSn, $AuSn_2$, $AuSn_4$)

Table 4.4.: Summary of physical properties of $Au_{80}\,Sn_{20}$ alloy at room temperature.

Property	**Value**
Melting point	280 ° C
Density	14.7 g/cm^3
Coefficient of thermal expansion	16×10^{-6}/° C
Thermal conductivity	57 W$\times$ m$^{-1}\times$ K^{-1}
Tensile strength	275 MPa
Young's modulus	68 GPa
Shear modulus	25 GPa
Electrical resistivity	$16.4\times10^{-8}\,\Omega\times$ m
Elongation	2%

can be observed in the microstructure at room temperature.

Au:Sn first eutectic point is at 217° C and 93.7% Sn (wt%), further referred to as tin-rich eutectic. It consists of two intermetallic phases: very brittle and hard $AuSn_2$ ε-phase and more ductile $AuSn_4$ η-phase. The interface between these two phases is brittle and known to be a place of origin for cracks [26]. This Au:Sn eutectic aggressively scavenges gold from the underlying metallisation, often causing instability of the system [27]. Therefore tin-rich Au:Sn solder joints are less popular than their gold-rich counterparts. What is more, very high tin content can lead up to the whisker formation, which in the long term affects the seal geometry [28].
Second eutectic point of the Au:Sn system is located in the gold-rich region at approximately 280° C and 20% Sn (wt%), and it is of the primary interest in the packaging applications as a soldering material (Table 4.4). This eutectic composition consists of two main intermetallic compounds, which at room temperature form a uniform mixture made of a relatively brittle, hexagonal AuSn δ-phase and trigonal Au_5Sn ζ'-phase. The popularity of this solder is thanks to the location of the gold-rich eutectic at the phase transition point placed between two steep liquidus lines.

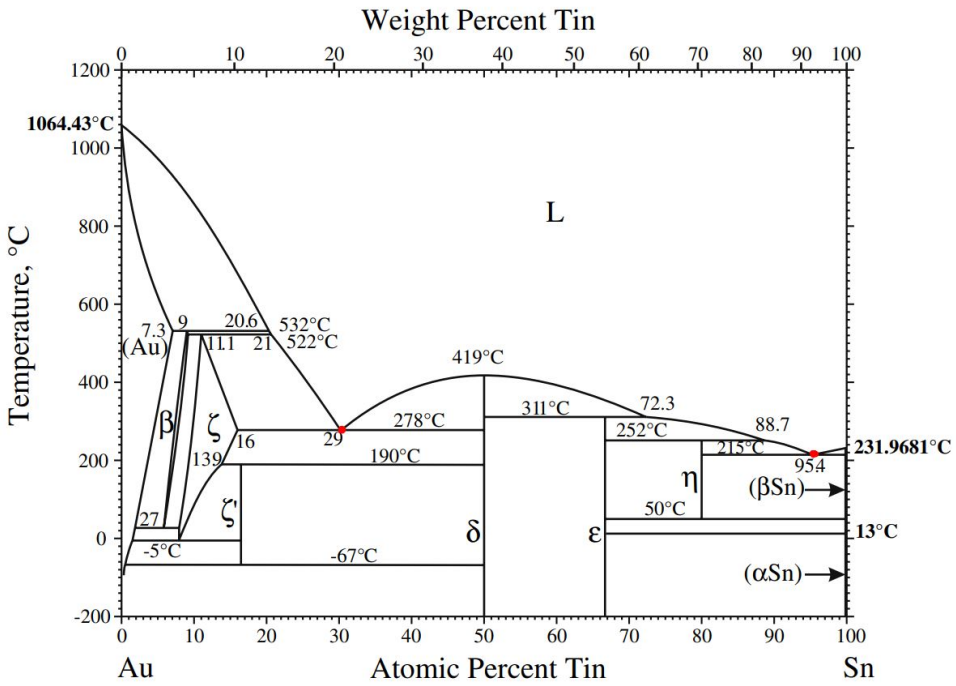


Figure 4.3.: Au:Sn phase diagram. Eutectic points are marked with red dots. Reproduced from [29]

4.2. Investigation of the effectiveness of thin-frame Au:Sn eutectic bonding in providing the hermetic seal and mechanical stability

Notwithstanding the Au:Sn bonding being formerly demonstrated for the MEMS packaging applications, particularly in RF and inertial systems, further investigation of bond characteristics and reliability is necessary to utilise the method more widely and effectively. Only limited research is available on the influence of global process parameters on bond characteristics, despite a mature character of the eutectic bonding in packaging. This is to a certain extent because the differences in processed samples greatly influence process outcomes. The research on solder geometries and bonding process parameters for hermetic sealing is limited and usually applies to samples of either significantly larger bond-frames (in ceramic packages with solder preforms) or of a much smaller ratio of bond-frame to enclosed space areas. As the size of solder joints decreases, new challenges arise that must be addressed to achieve a reliable package.
When bond frames are minimised, the behaviour of the joint can no longer be approximated from the properties of the solder as tested in bulk. It is because it is affected more by the characteristics of the interface, and the type of materials joined together. Firstly, the ratio between the bond area and total solder volume increases, especially for larger samples. Compared to thicker and larger solder frames, this causes the diffusion of a surface metallisation into the alloy to affect the solder's composition to a greater degree. The issue of diffusion is crucial for the gold-based metallisation, as the element is known to diffuse rapidly into the majority of solder alloys [30, 31]. In addition to the metal diffusion, because of the different volume ratio to the surface area, solder joints exhibit different solidification behaviour than bulk alloys. Partially, this is because of different heat exchange patterns of bulk and constrained solder alloys. Secondly, thinner and smaller joints are more dependent on solder's microstructural features, such as the grain size, which influence its mechanical behaviour.

Three main determinants of joint reliability can be distinguished- intrinsic characteristics of used solder, the geometry of a seal, and properties of the process of joint formation. The fourth factor, the character of a target application environment, is more crucial in applications where thermal cycling is expected. Here, the operational temperature is assumed to be at a constant 36.6 °C. In this study, the effectiveness of the tin-rich sequentially deposited Au:Sn alloy eutectic bonding of Si-based chips is evaluated in order to determine parameters critical for achieving reliable, hermetic seals. The influence of bond pressure, seal geometry, and reflow characteristics are assessed and presented. All experiments were carried out in an academic cleanroom laboratory setting, in the Centre for Bio-Inspired Technology and London Centre for Nanotechnology cleanrooms. Technical details of specific fabrication steps employed throughout the manufacturing run, such

Table 4.5.: An overview of bonding process parameters tested in the study.

Solder Ring Width [μm]	Solder Ring Height [μm]	Solder Ring Geometry	Bonding Force [N]	Reflow Profile
30	10	• Circle	0	• (FR) Fast direct ramp-up, long hold time
60	15	• Square	10	• (PFR)Fast direct ramp-up and long holdtime on pre-reflownsamples
90	20	• ChamferedSquare	20	• (SR) Ramp-up with intermediate pre-reflowstep at 200 °C,short hold time
150	30		30	
			40	

as the RCA-cleaning, solvent and piranha cleaning, photoresist processing and stripping, are not provided as they are considered standard processing protocols.

4.2.1. Design of test structures

For the purpose of assessing eutectic bonding effectiveness, a wafer-level photolithography mask set was designed (Figure 4.4). All designs accommodated 1 cm of pattern-free exclusion zone ring around the wafer edge. Different geometry characteristics were included, the overview of which is presented in Table 4.5.

Layer 1

Consists of alignment marks, and its design allows for the use with any future processes requiring the alignment of up to eight separate layers. As oriented to the wafer flat, the entire mask design is located on the outer east and west areas of the wafer and occupies a few square millimetres on each side. It contains a series of arrows pointing to the direction of alignment marks, a column of numbers indicating the currently processed layer, several geometrical shapes for the alignment, and a set of rectangular openings allowing for process inspections.

Layer 2

Consists of a set of rectangular openings located either at corners of the chip, above a chamfer, or inside the ring that are referred to as spillage stoppers. These structures are to be plated only with a gold layer, thus not melting under the high-temperature application. They are designed to possibly prevent or limit the extent of a spill-out of the molten solder.

Layer 3

This layer is used to pattern solder seal rings and includes twenty-seven different frame designs which differ in size, width, and shape.
Included are three chip sizes: 2×2 mm, 3×3 mm, and 4×4 mm; three seal geometries: rectangular, chamfered, and circular; and four frame widths: 30 μm, 60 μm, 90 μm, and 150 μm; with the circle being only available with a 90 μm width. The choice of the chip

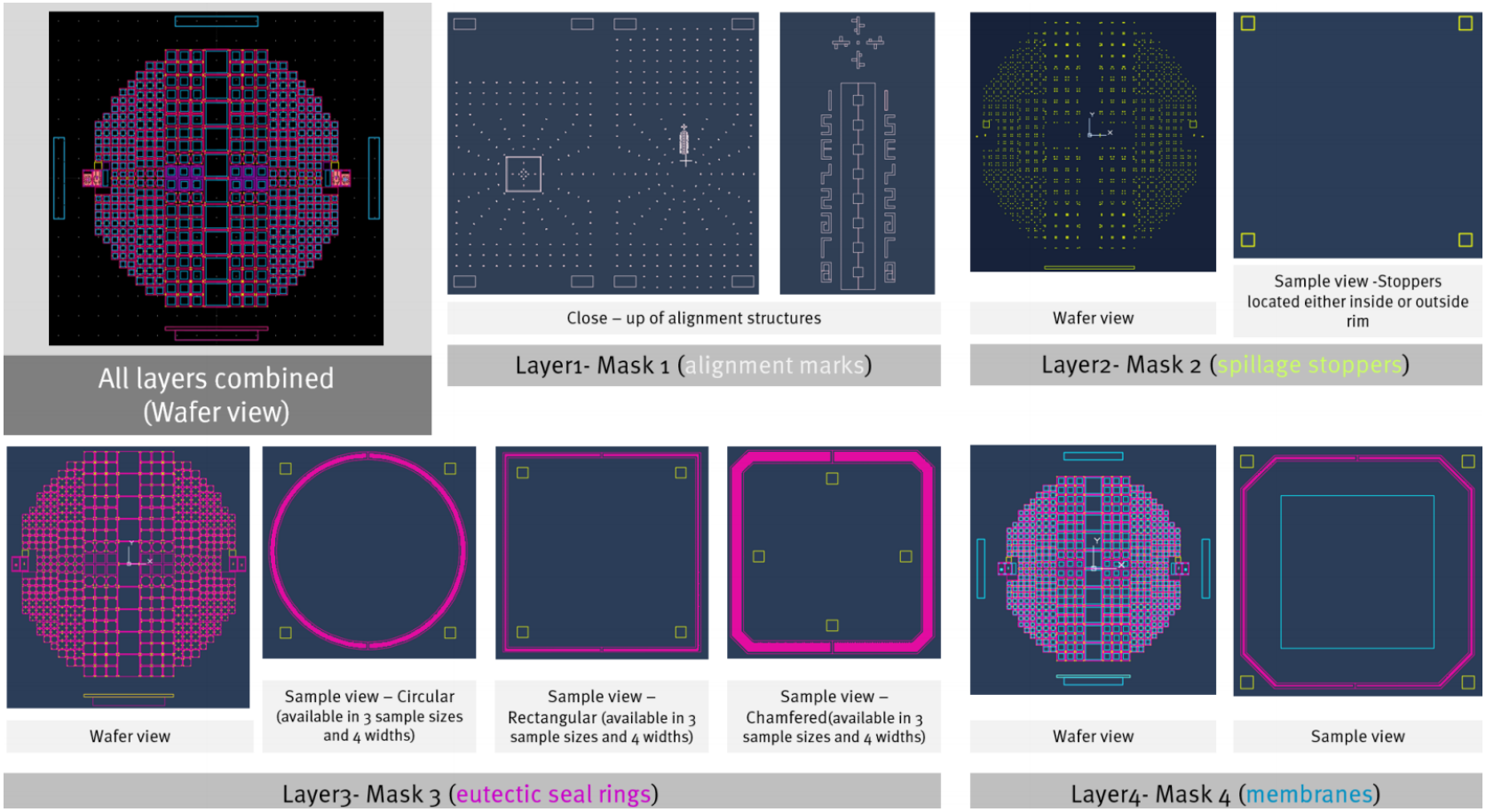


Figure 4.4.: Wafer-level photolitography masks set design for the plating effectiveness tests.

sizes was motivated by the design constraints of ENGINI probe heads, which are limited to a maximum area of 4x4 mm. Because of the bonding equipment limits, 2x2 mm samples were not considered in the assessment.
To determine an optimum frame design from the perspectives of hermeticity, mechanical stability, and ease of processing, frame geometries were selected to cover a wide range of designs. Despite occupying the smallest area on a substrate, thin bond frames could be the most prone to misalignment, effects of premature oxidation, and problems with voids compromising seal hermeticity. Compared to a few micron-wide frames, all tested widths are in the range of tens of micrometres, thus providing a margin large enough to minimise the abovementioned effects. Different shapes of bond frames were tested to investigate whether the geometry of solder lines of the same width and thickness influences its mechanical stability. With the progressing miniaturisation of devices, less real estate is available for critical sub-components such as communication coils, or power and data management ICs, hence the importance of geometry assessment.

Layer 4

This mask consists of a set of rectangles the size of 50% of the inside-seal area, placed within a seal frame, which are used to pattern openings for the formation of cavities. Such openings are formed in the dry-etch step and can be utilised twofold: for bonding processes conducted in the vacuum, the bottom of deep-etched cavities can be considered a membrane, the deflection of which is an indicator of the seal hermeticity; for any bonding process, an etched cavity can also be used as an additional space to fit high aspect ratio components within, like ICs or inductors. The depth of the cavity was designed to create a silicon roof robust enough to account for the safe handling of samples before bonding and minimise dicing-induced losses. In this research, to evaluate the bond hermeticity, cavity structures provide space for the placement of cut copper film pieces, the oxidation level of which is the indicator of moisture ingress.
All mask layers were custom-designed so that cap wafers sealing rings would match those on the base wafers. Eutectic stacks heights were electroplated to the heights of either 5 μm, 10 μm or 15 μm, which corresponds to Au(3 μm): Sn(2 μm), Au(6 μm): Sn(4 μm) and Au(9 μm): Sn(6 μm) tin-rich compositions, respectively. The choice of the height of plated solder layers was motivated by a couple of factors. Firstly, plated thickness control over the wafer area is more difficult in alloys of thinner heights. Considering the desire for thin layers, the thinner the deposit, the more accurate thickness control it requires. On the ground of the constant character of parameters such as material's grain size or plating non-uniformity, one can notice that to achieve better composition control it is more convenient to aim for the deposits of thicknesses in a several micrometres range. Secondly, chosen height range corresponds to those formerly reported in the literature of the subject.

4.2.2. Fabrication of base and lid wafers

All processes were carried on prime, DSP, 525 μm thick 4-inch (100) silicon wafers of a total thickness variation smaller than 2.3 μm to ensure substrate properties did not hinder bonding experiments. Even though molten eutectic tolerates surface topography quite well, too much of the variation in the surface planarity across the wafer could lead to an uneven pressure application in the bonding phase and the possibility of plating rate variations during ECD. Schematic, simplified overview of fabrication steps is presented in Figure 4.5.

Before any structural processing commenced, substrates underwent cleaning in 80° C Piranha solution, followed by a brief dip in HF to remove any present surface contamination. Next, lid wafers were oxidised to approximately 320 nm of dry thermal silicon oxide, while base wafers were coated with approximately 960 nm PECVD oxide (Mesc Multiplex 13241, STS, UK). The base wafer's oxide is different from the lid wafer's so that it better reflects the type and thicknesses of oxide in BEOL layers in the 0.35 μm technology node, in which ENGINI's project electronics is realised. ENGINI's specific type of 0.35 μm technology has a thick top PECVD oxide layer available, which aids in a device's protection. After surface oxidation, both lid and base wafers underwent positive-tone photolithography with Mask 1 in the AZ 701MiR photoresist (MicroChemicals GmbH, Germany) to pattern alignment marks near substrates' edges, followed by a silicon dioxide removal in buffered HF etch. Subsequently, alignment marks were etched down by 2-3 μm depth in a Bosch process (Multiplex Pro DRIE, SPTS, UK). Then, the photoresist was stripped, and the wafers were solvent-cleaned, followed by exposure to oxygen plasma.
Next, adhesion layers of either Cr or Ti were sputtered (PVD75, K.Lesker, USA) to the thickness of 20 nm directly followed by sputter deposition of 100 nm layer of Au, which would work as a seed layer for future electrodeposition steps.

These layers are used as an under-solder barrier and adhesion metallisation (USM). A thin film of one of those metals is necessary to improve the adhesion of gold to the Si/SiO_2 bilayer, create a barrier for the formation of intermetallic compounds, and prevent the diffusion between eutectic solder and substrate material. Later, selected substrates were photolithographically patterned with 5 μm AZ 15nXT (115 CPS) photoresist (MicroChemicals GmbH, Germany) to form an array of square-shaped openings, which are later electroplated with gold to the height of 5 μm. This is to create gold standoffs near the solder lines, which would work as possible spillage stoppers, preventing solder collapse during bonding. Then, the photoresist was stripped in heated MICROPOSIT Remover 1165, and substrates were cleaned in acetone and isopropanol baths, followed by DI water rinse and nitrogen blow dry.
Until this point, substrates intended for both the base and lid of the package were processed parallelly. In the next step, lid wafers were photolithographically patterned with the shapes of seal rings in AZ1518 HS photoresist followed by a differential etching away

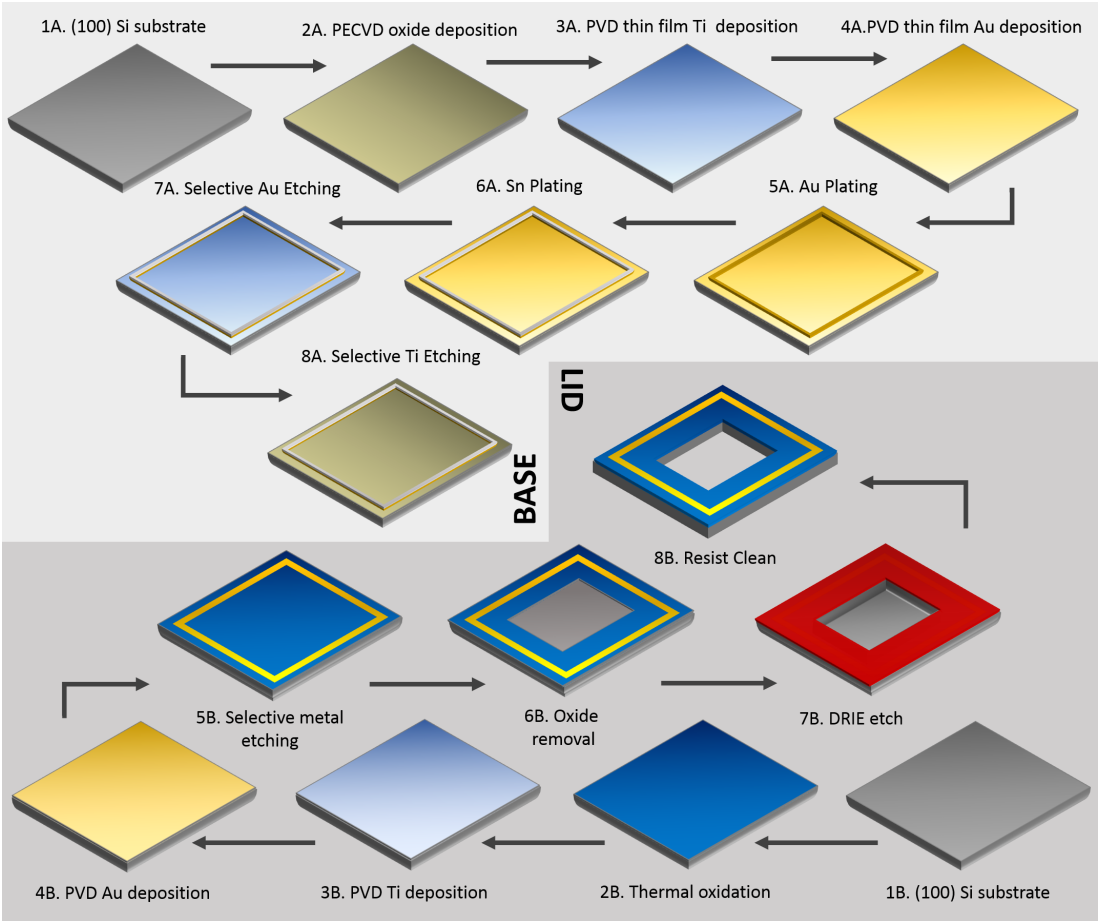


Figure 4.5.: An overview of base (above) and lid (below) wafers fabrication process flow.

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of previously sputtered Ti/Au layers and removal of the photoresist in acetone. This patterning step was performed in a positive tone so that only seal rings' outlines would be left on the oxidised surface after the metal-etching procedure. Special attention was given to avoid over-etching the metallic bi-layer, as it could otherwise compromise lid-to-base structures' complementarity. In the next step, lid wafers were again patterned using SPR-220 photoresist (Rohm and Haas, USA) to create central square openings used to form central cavities.

Following the removal of silicon dioxide in buffered hydrofluoric acid, cavities were etched down in the Bosch process to the depth of 200μm (Multiplex Pro DRIE, SPTS, UK). Then, substrates were stripped of photoresist, solvent- cleaned, and diced into 4 mm^2 and 9 mm^2 dies (DAD3230 dicing saw, DISCO Corporation, Japan). After final cleaning to remove any dicing-induced contamination, singulated samples were ready for the bonding process.

After electroplating of spillage-stoppers, base wafers were cleaned and sectioned into four separate fragments containing the designs of the same size geometries. This was to avoid electroplating with starkly different local current densities across the wafer, thus allowing

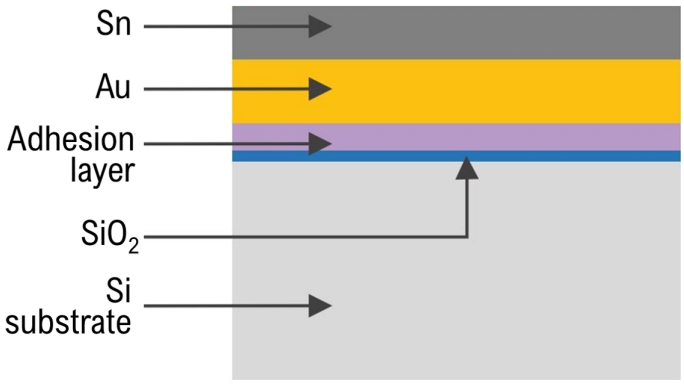


Figure 4.6.: Cross section of the structure of deposited layers as seen at the seal ring.

for better control of the deposition process. Each of the base wafers' sections underwent photolithography with layer 3 to pattern outlines of seal rings. For that, a thicker version of the previously used photoresist AZ 15nXT (450 CPS) with the thickness of 120% of desired plated deposit thickness was used (MicroChemicals GmbH, Germany). After that, substrates were sequentially electroplated with gold and tin layers using parameters described in the Chapter 5. After that, the photoresist was stripped, and wafers solvent-cleaned. Next, samples underwent selective etching of adhesion and seed layers in dedicated gold, and chromium or titanium etchants (KI, $HClO_4$:$(NH_4)_2[Ce(NO_3)_6]$, HF; respectively) thus leaving only layers of deposited solder on the silicon dioxide base. Base wafer sections were then diced to isolate dies of sizes corresponding to those diced from lid wafers. Finally, all samples were labelled according to their original location on the wafer, and the exact solder height of each solder ring was measured by a contact stylus profilometry. Prior to the bonding, one set of samples was annealed in a vacuum oven at 200° C for four hours. Before they were finally reflown, the remaining samples were stored for various times, reaching up to 6 weeks. Sketch of the final cross-section of the fabricated structure is presented in Figure 4.6, while Figure 4.7 represents photographs of wafers fabricated accordingly to the abovementioned process flow, along with close-ups of base and lip chips after dicing, ready for the bonding step.

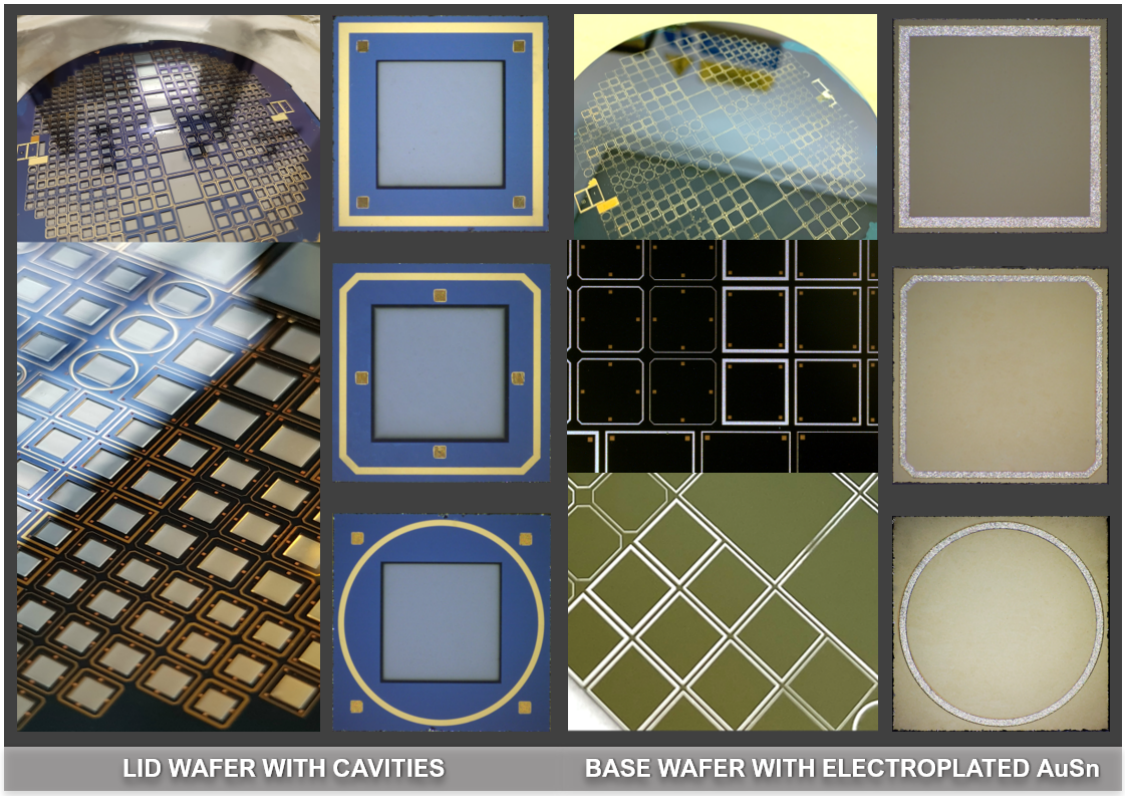


Figure 4.7.: Photographs of fabricated lid and base wafers,inserts on the right present close-ups of representative solder frames ready for bonding step.

4.2.3. Bonding process

To test the effectiveness of sequential electrodeposition in forming eutectic composition and to evaluate bond characteristics, corresponding lid and base dies were bonded to each other using a chip bonder (Fineplacer Lambda, Finetech, Germany). A schematic of the procedure is presented in Figure 4.8. In total, 110 sample pairs were processed. All samples were bonded at least three weeks after the last electroplating step to account for the ageing, typically observed with unavoidable processing delays.

Shortly before bonding, sample pairs were briefly cleaned in acetone and isopropanol and carefully dried with a nitrogen gun to remove any possible dicing-induced contamination. Lid and base dies were aligned at a maximum separation using Fineplacer's optical system, brought together to direct contact, and subjected to the force of value ranging from 0 N to 40 N per solder ring. Immediately preceding alignment, all samples were photographed to note any surface or solder irregularities that could later affect joining process outcomes. Bonding was performed by applying two different temperature profiles, depending on the tested batch (Figure 4.8). Batches FR and PFR containing samples pre-reflown in the vacuum oven were bonded by applying 320° C on the sides of both base and lid dies, with the ramp rate of 20 K/s and held at the maximum temperature for 10 min, after which heating was turned off, and samples were allowed to return to room temperature without any external cooling. Samples from batch SR were reflown by applying 200° C to both base and lid dies, with the ramp rate of 20 °C/s for 60 s followed by a further stage ramp-up to 320° C bonding temperature where they were held for 5 min. After that, samples were first actively cooled to 200° C and then allowed to further cool down to ambient

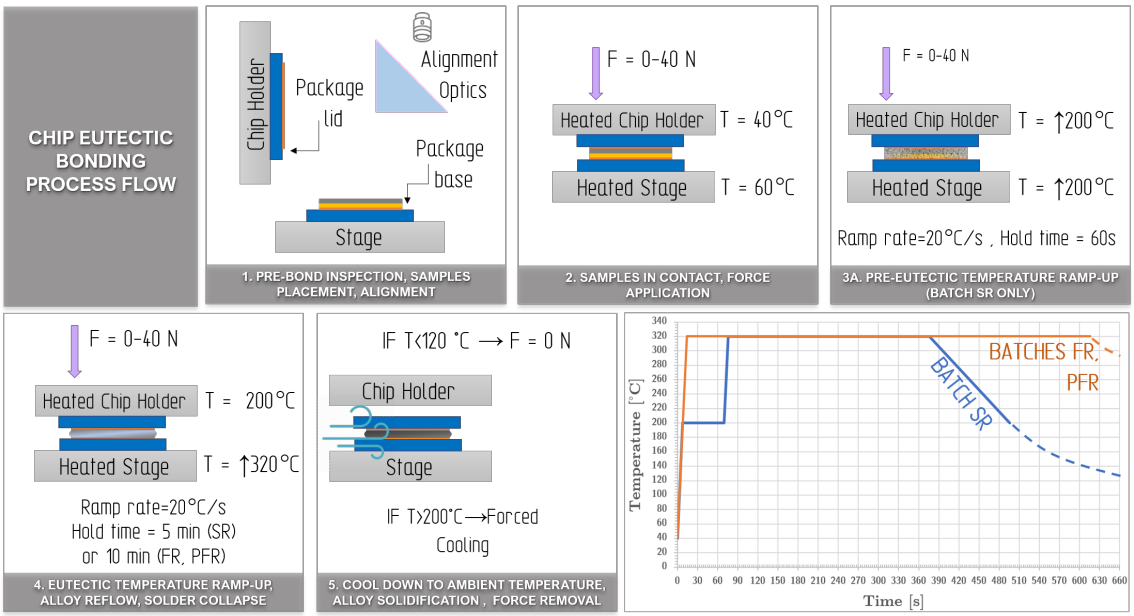


Figure 4.8.: Schematic of bonding process steps (1-5) alongside temperature profiles used.

without any external aids. When bonded pairs achieved a temperature lower than 120° C, the force was removed. Once samples completely cooled down to room temperature, they were transferred from the bonder for characterisation. Throughout an entire bonding process, samples were observed for the eutectic temperature, premature melting, spillages, and bond collapse via the side camera (Figure 4.9). As a result, characteristics of phase transformations could be observed *in situ* for the majority of samples processed. Two dominant reflow patterns were distinguished, differing in the appearance of an alloy when at near-eutectic and eutectic temperatures.

A first reflow pattern (reflow A, Figure 4.9) was observed in 47% of samples observed with the side-camera. In these samples, the glittery phase of alloy appearance could be observed only shortly before the complete solder reflow, during which the alloy exhibited a smooth-silvery look. The phase transition occurred instantaneously and was accompanied by an observable change in the solder height, and in some cases, by a slight shift of lid chip position in relation to the base chip. It was only for samples in this group where solder spill-outs reaching outside the perimeter of silicon chips were observed. Typically, those solder-overhangs appeared first before the solder's remaining volume turned into the liquid phase. Such a sequence of events would suggest that these spilt-out spheres are composed of excess tin.
The second pattern (reflow B, Figure 4.9), observed in approximately 9% of samples, showed no signs of temperature influence on the look of an alloy, until around 200° C, after which solder started showing signs of tin melting, and the whole layer exhibited a glittery appearance. After the temperature was increased up to 320° C alloy remained at the glittery phase and slowly turned more yellow as alloy constituents mixed better.

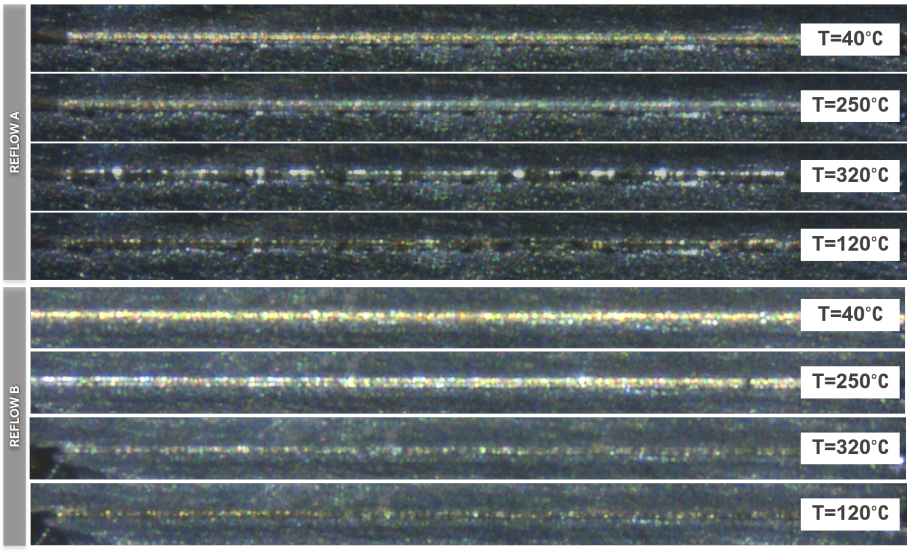


Figure 4.9.: Side-camera close-up view of bond interfaces exhibiting two visually distinct solder reflow characteristics.

No significant bond collapse was observed, and the pattern was more prevalent in samples that underwent bonding with the pre-reflow heating step. Reflow patterns of the remaining 44% of samples were not assessed because access to the chips' interface was obstructed, effectively disabling the possibility of solder melting observations with the side-camera.

4.2.4. Bond characterisation

An implantable device package's objective is to protect the device against an external, humid environment of the living body over a long time. Thus, the effectiveness of the bonding approach was characterised with a focus on the shear strength, reflown alloy make-up, hermeticity, cell response to the sealing material, and an overall yield of the bonding process.

Shear strength testing

The strength and integrity of single seal Au:Sn frames were measured through shear tests. Shear strength testing is one of the most common methods for the evaluation of material's limitations. The material's shear strength can be generally considered as its resistance to the dislocation motion upon load. It is a destructive measurement commonly performed by applying a pulling force to the sample to undergo a sliding failure along an axis parallel to the force. Shear tests were carried out using a Sauter FH500 force gauge with 0.1 N measurement accuracy (Figure 4.10). The unit was fitted with custom-designed 3D-printed fixtures to which sample holders (single lap joint-type) could be affixed and aligned in XY directions. All custom parts were 3D-printed using specific, high tensile strength, high rigidity, resistant resin to ensure setup durability and no influence on the measurement results. Additionally, all parts were printed as fully-filled and large enough to ensure maximum rigidity and no material elongation during measurement. Before samples were characterised, the durability of 3D-printed chip holders was measured. As a

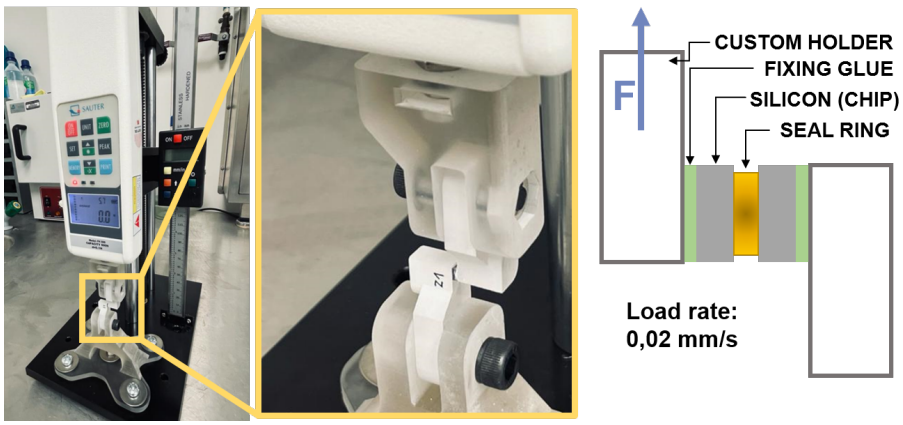


Figure 4.10.: Shear test setup.

result, sample holders' shear strength value exceeded the measurement range of the gauge.

Once it was confirmed that 3D-printed holders would not negatively impact measurement outcomes, the backside surface of measured samples was carefully fixed to holders using fast-setting cyanoacrylate-based adhesive. Adhesive of thick, gel-like consistency was used to ensure no bleeding into the interface between lid and base dies takes place. Additionally, a dedicated surface primer and adhesive activator spray were selected to aid the fast setting of the glue, which was used only in minimal amounts on the entire backside of the samples. The surface onto which the adhesive is placed is more than ten times larger than the area of the bond frame, preventing failure at the glued interface during shear measurement. Once the glue had set, samples were transferred to the force gauge, and holders were secured in place with screws. The load was applied with the approximate rate of 0.02 mm/s until samples debonded at the interface and the maximum measured force was registered. The shear strength was then calculated by dividing the recorded force by the total bonded area. Samples were subsequently inspected with an optical microscope and scanning electron microscope to examine the extent of possible spillages and evaluate the fracture mechanism of broken bonds. All recorded shear strength values were later evaluated accordingly to the MIL-STD-883G-2019.5 military standard. The regulation specifies microelectronic systems screening and test optimisation requirements and includes specifics on shear strength values for microelectronic dies suitable for use within military and aerospace electronic systems. In agreement with the standard, acceptable shear strength value should fulfil the following rule:

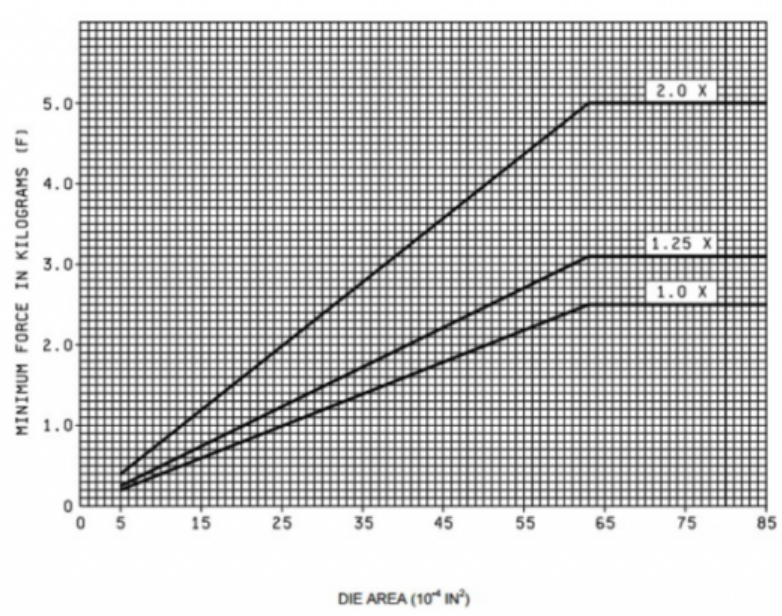


Figure 4.11.: MIL STD 883 die shear strength criteria (minimum force verses die attach area) [32].

"A force sufficient to shear the die from its mounting or equal to twice the minimum specified shear strength (Figure 4.11), whichever occurs first, shall be applied to the die." [32].

Bonding Yield

Considering the sample size of over a hundred samples of different geometries, the majority of tested chips exhibited favourable mechanical characteristics of produced joints. On the global level across various parameters examined, an overall yield of the bonding process was 73%. However, within the well-bonded group, 12% of samples exhibited shear strength values below the minimum as described by MIL-STD-883G military standard for die-attach, thus reducing the total yield of bonding process across all examined parameters to approximately 64%. Whereas the bonding success of yield value in this range may not necessarily be considered good from the industrial point of view, it should be noted that this is a cumulative value including results across all sample sizes and process conditions, all done using a small-scale laboratory setup. Having that in mind, the translation of the process to the high-scale manufacturing facilities with a clearly defined set of the most favourable process conditions for bonding and electroplating is expected to improve the success rate further. Figure 4.12 outlines measured shear force values of the group of 78 samples of the entire processed population, divided into five groups, depending on their frame geometry and MIL-STD-883G-standard requirements for the minimum acceptable shear force. Significant variation between results obtained for the same frame width groups, as visible in Figure 4.12 is an effect of different process conditions used for each of the included samples.

The remaining 24% of samples have exhibited seals of mechanical characteristics too poor to conduct shear strength measurement. Those samples debonded upon normal handling circumstances, such as during storage box transfer or fixing the sample holders to the force gauge. When analysing representatives of the failed group, some distinctive samples' subgroups can be distinguished. Bonding pressure-wise, it was found that the largest group of failed samples (38 %) comprised of specimens that were bonded under no force (0 N), or low-force (10 N per ring) conditions. This finding might be considered an early indicator that applying pressure upon bonding aids in solder attachment to the package lid. As a consequence, using solder frames terminated with tin, as opposed to alloys finished with a thin layer of gold, one must recognise the need to break through the naturally-formed stannous oxide. Upon exposure to air, especially at low humidity, tin is known to form thin layers of native oxide, which is very hard and brittle [33]. The oxide's melting temperature is much higher; it can prevent melted alloy from easily attaching to the gold metallisation on the package's lid. For that reason, native oxides are often reduced *in situ* shortly before the bonding process, either chemically or mechanically [34]. The high occurrence of samples failing shear test despite proper reflow type observations in the no-pressure-applied group appears to indicate the presence of oxide thick enough to require scrubbing motion or high bonding pressure for the purpose of SnO reduction.

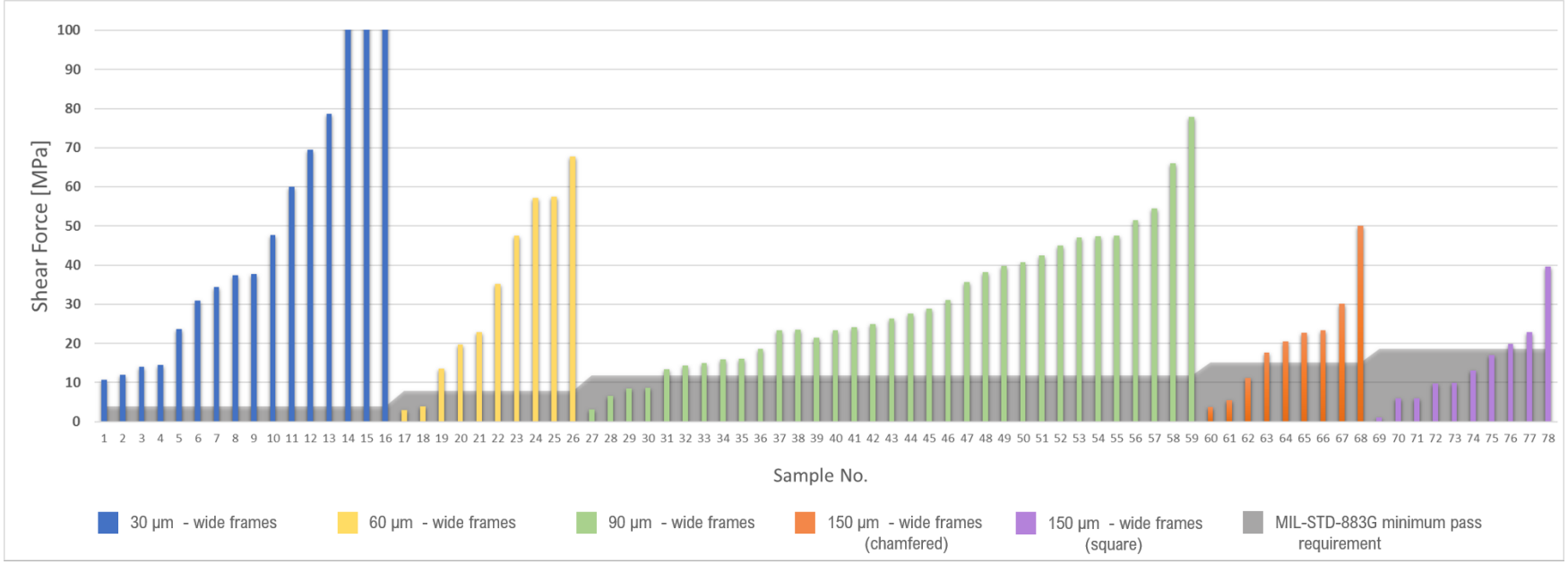


Figure 4.12.: Measured shear force values for samples of different frames widths with the notion of the minimum required shear force as described in military standard MIL-STD-883G for semiconductor components.

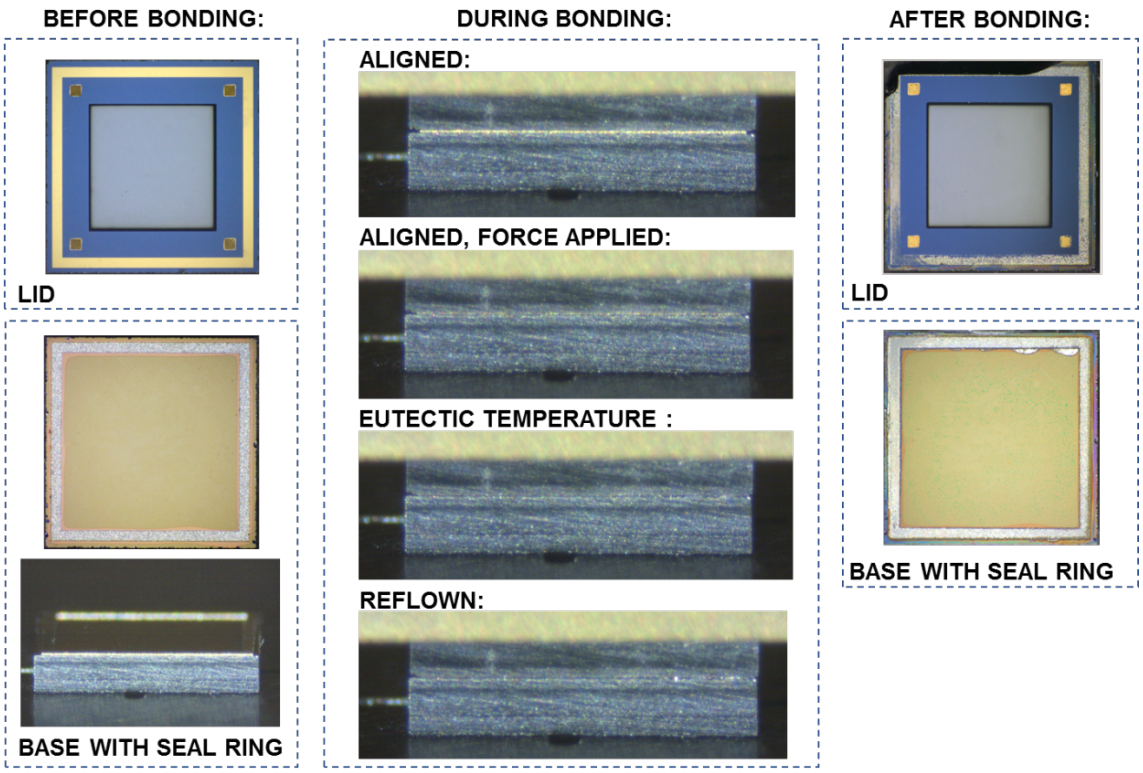


Figure 4.13.: Microscope photographs of lid and base chips' surface as seen before the bonding process (left), after reflow, and following shear tests (right). The side profile of the chip stack as seen during the bonding procedure (centre). Solder collapse and change in the colour appearance of solder are observed.

From the perspective of the size of bonding lines, it was found that of all four widths, bonds tended to fail the most for the thinnest of tested geometries, which was 30 μm-wide. This finding supports claims that in thinner and narrower solder lines, diffusion from adhesion metallisation impacts the volume of the solder more and can lead to the formation of intermetallic compounds with underlying metal tracks, shifting the composition of an alloy. Furthermore, narrower solder lines are more affected by outcomes of chips misalignment.

Impact of the under layer metallisation material

The choice of suitable adhesion and barrier metal layers for eutectic applications is one of the more intensively researched topics in the literature on solder alloys [35, 36]. Multilayers combining several elements are often employed to provide the solder with ultimate conductivity, adhesion, and barrier conditions. The interest in researching those multilayers stems mainly from the fact that AuSn-eutectic is broadly used in high power electronic devices, which generate much heat. Such applications' high service temperatures influence the microstructure of used solder and can turn the Au:Sn layer brittle, breakable and prone to peeling off the device's surface. Therefore, intermediate metal layers are crucial to establish a good anchorage to the substrate and, if applicable, to release stresses due to the CTE mismatch. Many materials regularly used as barrier/adhesion underlayers cannot be used in implantable applications because of their cytotoxicity, the examples being copper or nickel films. However, as the service temperature of implantables is constant and relatively low, it was decided to test the applicability of simple bilayers of Cr/Au:Sn and Ti/Au:Sn.

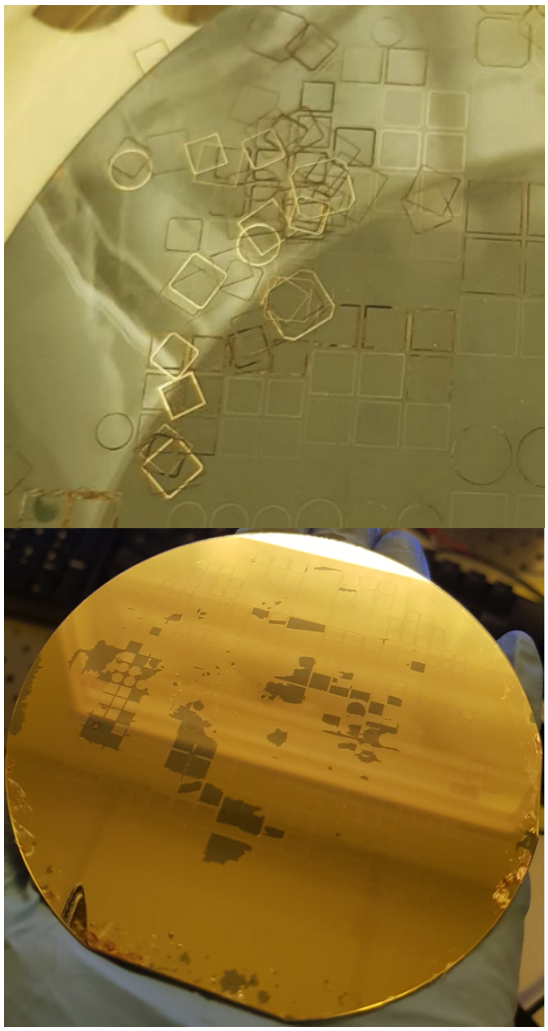


Figure 4.14.: Delamination of deposited Au:Sn solder frames and observed seed layer delamination issues, resulting from poor chromium adhesion.

One small batch of samples (batch SL2) processed in the parallel fabrication run was made with chromium adhesion/barrier metal and plated with a thinner, 7μm-Au:Sn stack (4.2μm Au, 2.8μm Sn). In total, ten sample pairs with these characteristics were processed. Of all, five samples did not survive until the shear tests, and two others debonded upon the low force application. The remaining three exhibited shear forces within the average measured range. It could be attributed to the little thickness of the tested alloy and the choice

of chromium as an underlying metal. Preceding the fabrication run described in detail in this chapter, wafer-level bonding experiments on Cr-metallised substrates were conducted.

Notwithstanding seemingly frequent occurrence of Cr/Au/Sn metallisation in the literature of the subject [37, 38, 39, 40], in this study, it was determined that such a trilayer should be avoided in applications aimed for packaging. Compared to titanium, chromium is more prone to undergo interdiffusion with overlaying gold films, thus disturbing the composition balance of solder alloy above [41]. While this phenomenon could be beneficial from the perspective of mechanical properties, it influences the bonding yield- primarily when thin solder lines are used. The growth of chromium-related metallic compounds at the solder interface can be considered inorganic contamination, as it creates unwanted intermediate layers that are not easily wetted by the molten Au:Sn alloy. Since the formation of intermetallic compounds is known to progress when heated, using Cr should be avoided, especially in applications where devices bonded with Au:Sn would need to operate at elevated temperatures.
Both metals have a similar affinity to oxidation and readily grow native oxide films upon exposure to air. For that reason, care must be taken to ensure an oxygen-free environment during PVD depositions. During processing silicon wafers for Au:Sn packaging applications (section 4.2.2 after Au/Sn electroplating, seed and adhesion metal layers must be removed by a differential etching (steps: 7a, 8a, and 5b; Figure 4.5). It has been found that this particular step is challenging for chromium-based underlayers because of the process compatibility point of view. Industry-standard chromium etchants are strong oxidisers, leading to premature degradation of the deposited tin layers. This could be avoided by either terminating solder stack with thin gold layers or extra photolithography steps to cover plated alloys and limit etchant access. Moreover, it was observed that chromium base metallisation was more prone to delamination problems, leading to the complete detachment of solder lines from the substrates. Chromium was also found cytotoxic and, as such, should be avoided in implantable applications [42]. Issues as mentioned above were not encountered with the use of titanium as underlayer metallisation.

To sum up, the SL2 batch yielded the lowest shear strength values as the chromium layer was proven insufficient to provide an adequate level of adhesion for the grown eutectic (Figure 4.16). For that reason, results from group SL2 are not included in the remaining statistics of the experiment. Once the adhesion/barrier layer was switched to the sputtered titanium film, non-reflown solder adhesion problems faded.

Impact of bond frames geometry

No correlation between the shape of seal lines and the resulting measured bond strength could be unequivocally found. Figure 4.15 represents the comparison between average shear strength measured for different sets of chips bonded under the same temperature and force (40N per ring) conditions. Results are divided accordingly to the width and shape of the frames. Analysis of the results brings the possibility of an assumption that, aside from the widest frames, in each case, chamfered frames exhibit an average shear strength values higher than squared seals. While this could be right on the base that rounded or chamfered structures are likely to relieve interfacial stresses better than the structures with squared corners, one must also account for the influence of the bond area. Given two bond frames of equivalent main geometry features, such as line width and the chip size, the total bond area of the chamfered design will be smaller than in the squared frame. In this experiment, the bond force applied was not adjusted per total area of each bond to achieve equal bond pressure, but arbitrarily by applying either 0, 10, 20, 30, or 40 N. This was caused by the nature of operation of the bonder employed in the tests, which allows only for manual management of bonding force, with an accuracy of around 2N. Therefore, results presented in Figure 4.15 could both mean that chamfered shapes are performing better mechanically as well as more bonding pressure during the process leads to better shear strength values. What is more, the results could not be directly compared because of the unevenness and small size of each group's population, which in some

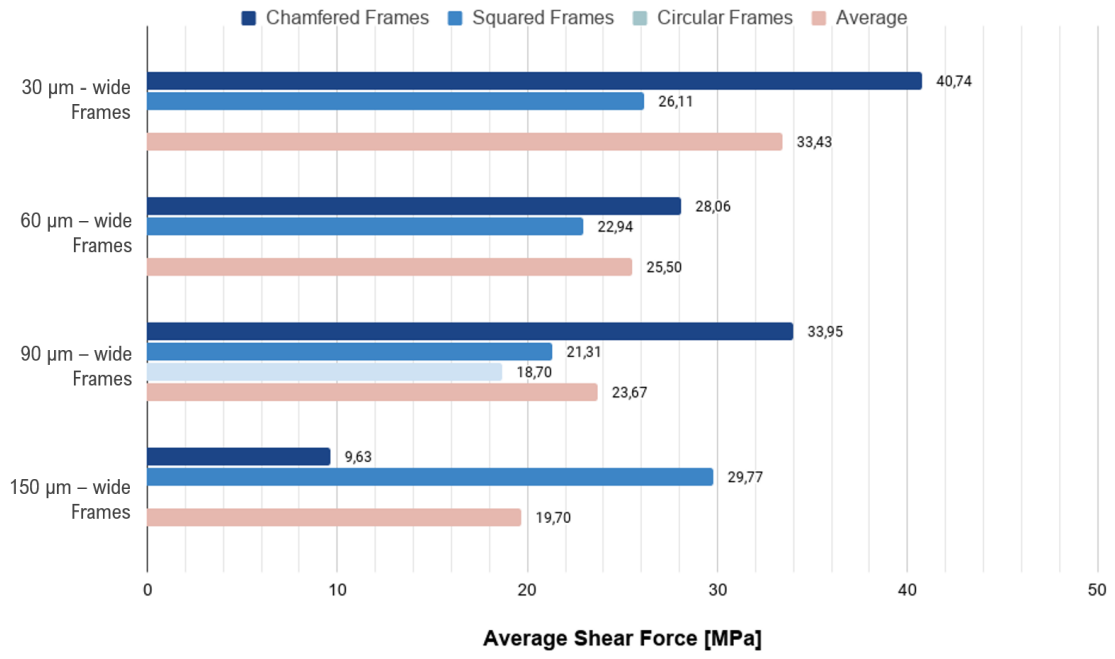


Figure 4.15.: Comparison of average shear strength values between bond frames of different shapes.

cases varied significantly (group: 30μm chamfered- 4 samples, 30μm squared- 4 samples, 60μm chamfered- 3 samples, 60μm squared- 4 samples, 90μm chamfered- 6 samples, 90μm squared- 8 samples, 90μm circle- 4 samples, 150μm chamfered- 6 samples, 150μm squared- 4 samples).
When comparing all samples processed globally and looking at the shear strength values for different bond geometries, all shapes (circle, square, chamfered square) exhibited similar ranges of measured shear strength values. To conclude, when mechanical properties are of primary importance, it cannot be determined with confidence that solder rings' shape is a high relevance parameter. Therefore, the choice of shape should be based on the requirements of the final application and the constraints it has.

An average measured shear strength for samples of the same solder line width was calculated. Each width's averaged value was calculated irrespectively of applied bonding conditions (pink bars, Figure 4.15). Based on that, variations in a seal behaviour were observed for bond frames of different widths, as 150 μm lines exhibited lower shear strength values than thinner 90 and 60 μm wide lines of the same height (Figure 4.15). Several reasons could explain this, all of which are related to differences in the ratio of solder's volume to the bond area. Wider frames have a larger Au: Sn interface surface area, thus more availability for premature gold diffusion and the formation of high-temperature intermetallic compounds. At the same time, because of the larger surface area, wider frames achieve eutectic point and solidify faster. Moreover, as mentioned earlier, thinner frames can better concentrate applied bonding force so that penetration of molten solder through any surface contaminants and irregularities is more successful.
The resulting bonding strength may be more influenced by a solder height and bonding conditions than the seal's geometry. When comparing the difference between an average shear strength between the lines of different widths, it can be noticed that the strength value scales up with the size. Changing the line width by 10μm results in the change of resulting shear strength by roughly 0.6 MPa. It could mean that noticed difference results only from smaller bond areas and is a result of the constant strength of the alloy, which, when recalculated to pressure, gives larger values for smaller samples. This relation is only not valid for the thinnest of tested widths, as the difference in shear strength between lines of 30μm and 60μm is 4.5 times larger. Irrespective of the reasons, the results show that Au:Sn bonding method or hermetic sealing is especially suited for samples of smaller geometries and sizes.

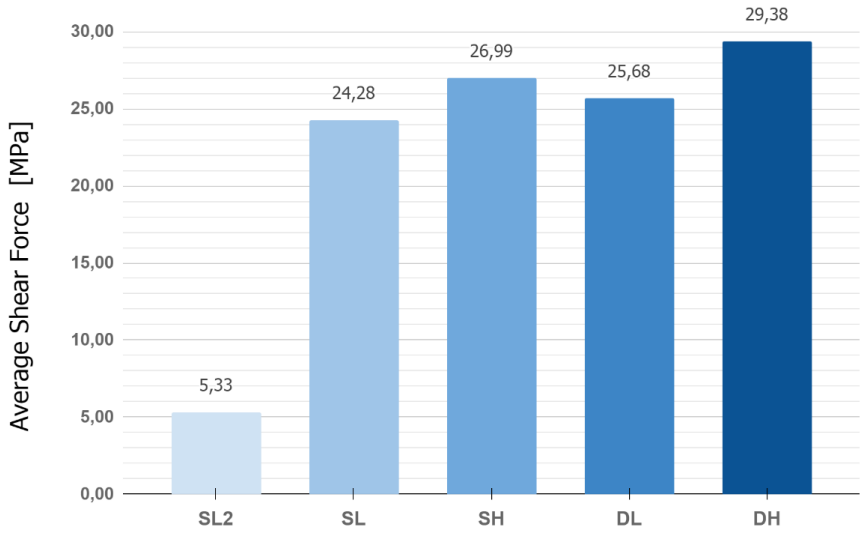


Figure 4.16.: Average shear force for samples of different as-plated solder heights. SL-2 7μm-10 μm total solder on-base die only with Cr adhesion layer, SL-10 μm total solder on-base die only; SH-15 μm total solder on-base die only; DL-20 μm total solder on base and lid dies; DL-30 μm total solder on base and lid dies.

A structural parameter that exhibited more influence on the shear strength values was the stack height. Deposited layers were higher than 10μm to ensure the proper ratio of gold to tin was maintained. Two distinct metallic layers of different grain sizes were achieved when sequentially electroplating gold and tin from two different solutions. In comparison, gold layers are deposited to form smooth layers of small grains and compact microstructure, while deposition of tin from methane sulphonic acid produced films of a comparably more developed morphology. Micro roughness of tin, resulting from its grain size, leads to difficulties in precisely measuring the deposited layer, thus controlling the correct eutectic ratio, especially for thin solder layers. When chosen eutectic height is tall enough, the grain size measurement error becomes insignificant, allowing for a successful Au:Sn proportion deposition. Any premature Au:Sn intermixing and resultant consumption of metals favouring the formation of intermetallic compounds different to Au_5Sn is minimised with thicker layers deposited. All samples of as-deposited Au:Sn heights of 10 μm and 15 μm achieved eutectic composition, as observed by the presence of a single uniform metal phase in post-reflow SEM images and *in-situ* observed reflow temperature.

Four different eutectic height groups were evaluated: SL with 10μm of as-plated eutectic height on the base die; SH with 15μm of as-plated eutectic height on the base die; DL with 10μm of as-plated eutectic height on both base and lid dies (total of 20μm) and DL with 15μm of as-plated eutectic height on both base and lip dies (total of 30μm).

Additionally, the SL2 group consisting of dies with 7μm -high Au:Sn eutectic on the base die with Cr adhesion layer was tested (Figure 4.16). As mentioned earlier in the Section 4.2.4 about an impact of the metallic underlayer, the latter group yielded the lowest shear strength values as the chromium layer was proven insufficient to provide an adequate level of adhesion for the grown eutectic. What is more, selective etching of chromium thin film from die surface during the last step of processing led to the premature rapid oxidation of the electroplated tin surface, thus hindering further bonding steps.
For the remaining samples with titanium deposited as an adhesion layer, the average shear force measured was more significant for higher thicknesses of the deposited solder. For the groups of dies with solder stack present only on one die, the variation in an average shear strength between solder heights of 10 and 15μm was only 2.71 MPa. Doubling the amount of solder by depositing a eutectic stack on both base and lid wafers led to an average shear strength increase of 1.4 MPa for samples with double-10μm stacks and 2.39 MPa for samples with double-15μm stacks. It must be noted that when a double solder height is considered, a considerably more extensive excess solder spill-out was observed for samples of all geometries. Furthermore, all double-height-bonded samples exhibited different shear fracture modes, mainly breaking at the bond interface. Considering the increased cost and complexity of double-stacked samples against only a minor increase in the shear strength, it was concluded that stacks deposited on only one of the package dies were sufficient to provide a reliable seal.

Impact of bonding pressure and reflow profiles

An analysis of the relation between achieved shear strength and pressure applied onto the seal frames during the bonding process has not shown a clear correlation between the two factors. Figure 4.17 represents a scatter of the results of measured shear strength of the seal versus bonding pressure conditions, and as such, a considerable variation of results can be observed. It must be noted that data points in Figure 4.17 depict a cumulative representation of a large number of samples, including samples of various sizes, geometries and reflow profiles, which impedes the possibility of a direct correlation observation. To some extent, a vague trend where achievable shear strength is on average higher with an increase of the bonding pressure can be observed. Improved mixing of solder phases in part causes this during reflow under pressure. Applying pressure aids in removing voids and improving wetting of solder to the substrate; however, it causes a bond line widening and increases the possibility of solder squeeze out and spillages. Very high bonding pressures were also found to cause minor shifts in dies alignment when the surface of the bonder was not perfectly levelled. On the other hand, minimal or no bonding pressure was a parameter used in 40% of all samples from the group of the weakest bonds that failed upon regular handling. Application of pressure helps to break rigid native tin oxide and minimise the influence of surface contaminants, which in the absence of flux largely influence wetting and spreading of molten Au:Sn solder. Furthermore, bonding pressure helps to keep both substrates planar and homogenises any occurring height variations. Nonetheless, applying low to moderate pressures along with the suitable adjustments of other bond parameters, such as eutectic height, makes it feasible to attain shear strengths in the range above 20 MPa, which are applicable for intended implantable purposes.

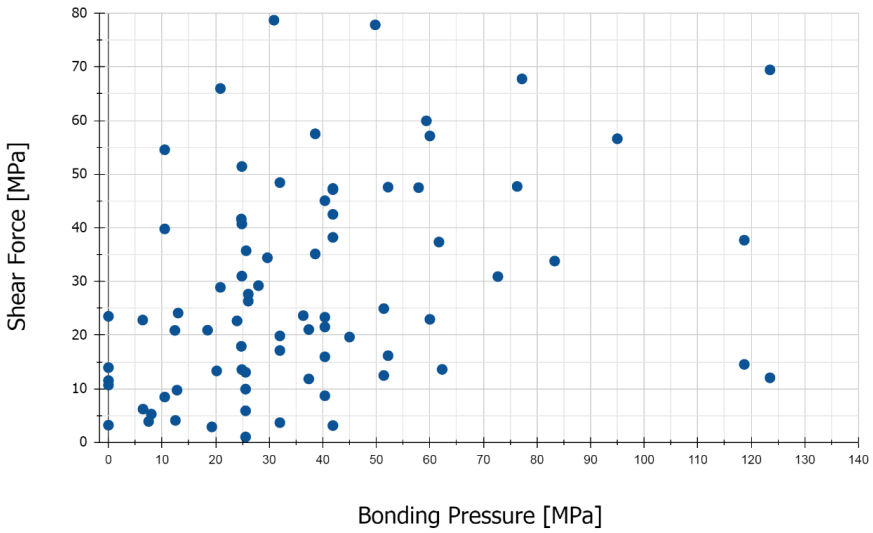


Figure 4.17.: Measured shear force in the relation to pressure applied to the sample during the bonding procedure.

Clear differentiation between the total yield of well-bonded samples can be observed for dies reflown with different temperature profiles (Figure 4.18). Samples that were heat-treated in a vacuum oven before a final reflow successfully bonded in only 36% cases, while using the same temperature profile on samples without any prior annealing led to an increase in yield to 78% of well-sealed samples. Pre-annealing before a final bonding is known as the double-reflow process, which is supposed to aid in the volatilisation of organic contaminants from the alloy surface. Pre-reflow annealing is also employed to increase the bondability of as-deposited layers over time by minimising the diffusion rate of Au into Sn, and the formation of unwanted intermetallics [43]. However, in this research, annealing negatively impacted bonding process yield, likely due to an increased Ti adhesion layer consumption. Application of the intermediate annealing step at 200° C directly before the reflow above eutectic temperature also negatively impacted process yield. At the same time, samples that were bonded following temperature profile with a rapid ramp-up to bonding temperature and gentle cool down were the most successful, with the total yield of samples passing minimum shear strength requirements reaching nearly 80%. Thus preferably from the process yield perspective, reflow at a temperature above the eutectic should occur as soon as possible, with as fast as possible ramp up and without any prolonged exposure to temperatures above the melting temperature of tin.

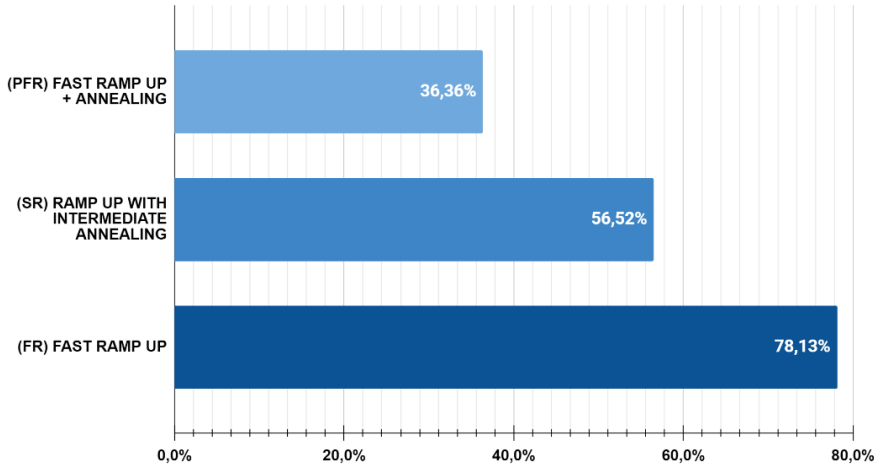


Figure 4.18.: The yield of successfully bonded samples reflown with different temperature profiles, with or without pre-bonding annealing step.

Shear fracture mode analysis

Following shear strength measurements, all fractured samples were examined to identify the mode of failure occurring at the bond interface. Initial fracture type assessment was performed grossly with an optical microscope; then, the representative examples of recorded failure modes were analysed via SEM inspection. In general, the mechanical behaviour of metallic Au:Sn seals is devoided of plastic deformation and linear elastic up to the point of an abrupt material rupture. For that reason, no shear failure modes of plastic character could be observed.

SSeveral failure mechanisms can occur between samples bonded together with intermediate metallic layers. The first type, cohesive sealant fracture, occurs as a crack within the sealing material resulting in the remains of the sealant retained on both formerly joined surfaces. The occurrence of cohesive failure indicates that the system's weakest point is the alloy itself, and the forces between molecules are determinants of the strength. Another type of cohesive failure is the fracture within one of the adherents, in this case, within the silicon chip. This type of failure indicates that the maximum strength of the joint is larger than the structural integrity of the silicon. From the perspective of bond strength, this type of failure is the preferred one to be observed as it confirms that the maximum joint strength for the system is achieved. Both of these fracture modes were observed in tested samples. Cohesive adherent failure, represented as fragmentary remains of the corresponding sample from the pair attached to the soldered frame, was the second most observed across all tested samples and shows the bond strength surpassing fracture strengths of silicon/silicon oxide die. (Figure 4.19).

The least observed fracture mode was the one occurring within the bulk of the bond frame itself. None of all debonded samples exhibited a typical cohesive sealant failure, where the Au:Sn alloy would remain on both lid and base surfaces after shearing. However, a transient cohesive failure where the bond was sheared vertically across was noted (Figure 4.20). Such fault was usually caused by either the local solder imperfections such as

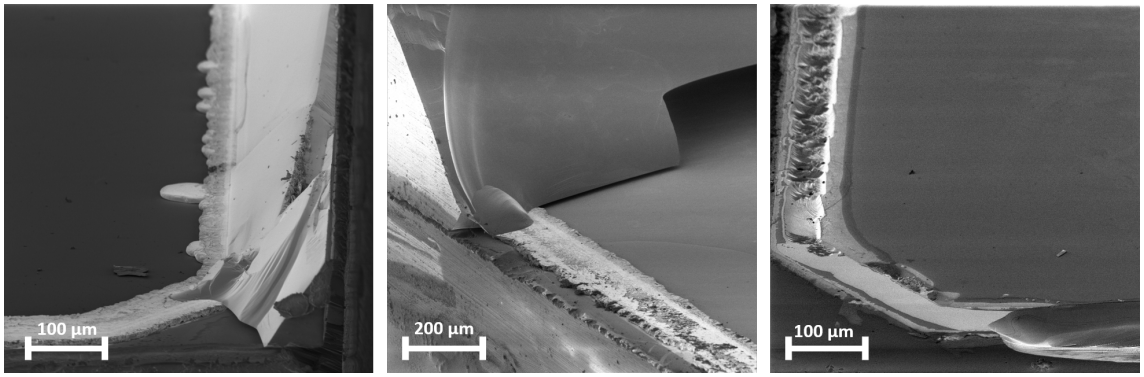


Figure 4.19.: Examples of the cohesive shear fracture of adherent Si chips following shear testing.

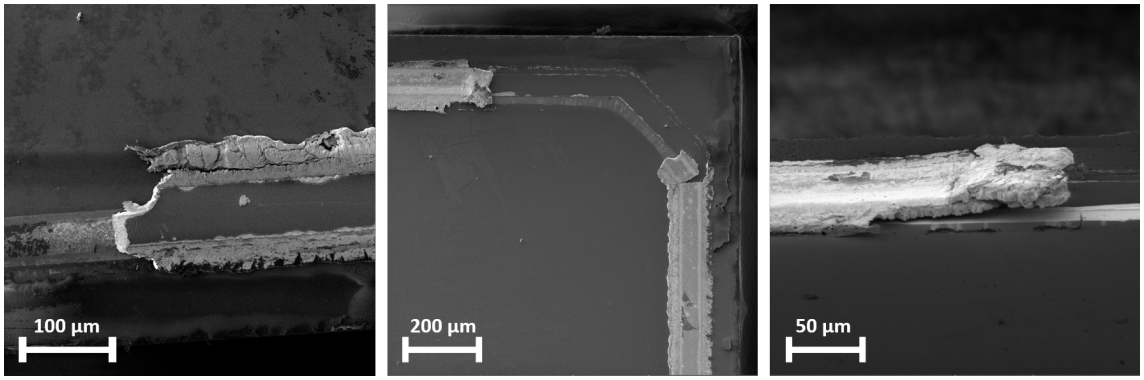


Figure 4.20.: Examples of Au:Sn solder transient shear fracture following shear testing.

voids, bonding force non-uniformity, or by the deviation from the 80:20 composition of the solder and, therefore, phases non-uniformity. Because of these local imperfections, the stability of the solder is locally impaired, therefore, easier to break.
The second type of failure modes that can be observed when shearing samples are adhesive, or in other words, interfacial fractures. Interfacial failure is typically demonstrated as film delaminations, either between solder and adhesion layers or between the entire metallic stack and the substrate. The occurrence of adhesive failures is highly dependent on the quality of the surface, including its cleanliness, interdiffusion between solder stack components and the alloy's wetting behaviour. When interfacial failure occurs, the entire solder stack remains at only one side of a soldered stack, either on the lid or the base chip. For multiple samples analysed, the transfer of Ti:Au thin film bi-layer from a silicon surface onto the bond frame was observed. This indicates the failure occurring at the solidified solder and adhesion layer interface, pointing out the bond's good mechanical stability and quality. The exact location for that type of failure could occur both at the interface between Au:Sn and Ti, as well as Ti and SiO_2. The highest occurrence rate of this fracture mode may indicate the need for improvements of an adhesion layer to limit the dissolution of Ti into the solder.

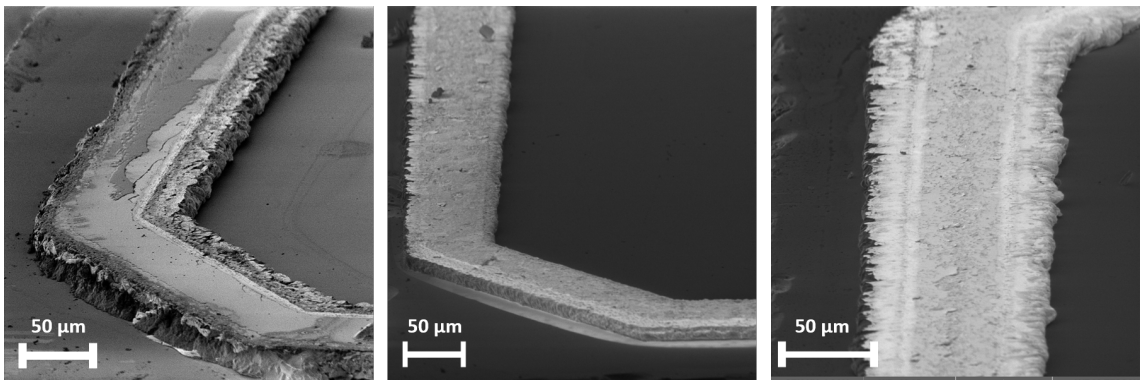


Figure 4.21.: Examples of Au:Sn solder interfacial shear fracture following shear testing.

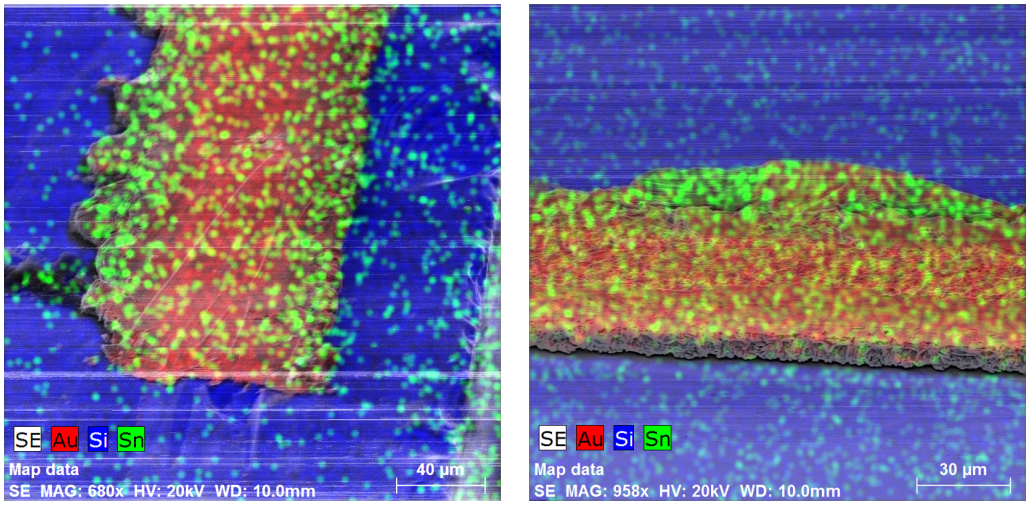


Figure 4.22.: Energy Dispersive X-ray spectroscopy map of elemental distribution in sheared samples exhibiting interfacial failure mode.

A selection of sheared samples was additionally investigated with the Energy Dispersive X-ray spectroscopy (EDX) to assess Sn distribution in the joints. All EDX-analysed samples belonged to the most numerous fracture-mode group, having an interfacial failure. EDX is a common chemical analytical method used to identify and quantify elements within a small sample volume. It is a method typically used along with SEM scanning and does not cause any damage to tested samples. However, EDX allows only for the analysis of the surface elemental composition of the samples.

EDX investigation of the samples examined in this chapter revealed that the majority of spill outs observed after bonding are composed of mostly tin. Figure 4.23 represents an elemental composition analysis showing the area of the bond frame having an alloy with the composition of roughly 3:1 Au to Sn ratio, which is not far off from the ideal eutectic composition of 71% Au to 29% Sn (80:20 Au to Sn by weight), however when analysing the spill out area the ratio changes and tin dominates by 2:1 to gold. This could imply an excess of this element was present in as-deposited samples, which was then squeezed out during the bonding phase. Excess tin would also explain the presence of glittery look of solder at below-eutectic temperatures as observed during reflow (Figure 4.9). The middle part of debonded samples was observed to be clearly richer in gold, which may indicate that the thin seed layer from the lid chip was transferred onto the bond frame, proving adhesive failure at the Au-Ti interface (Figure 4.22).

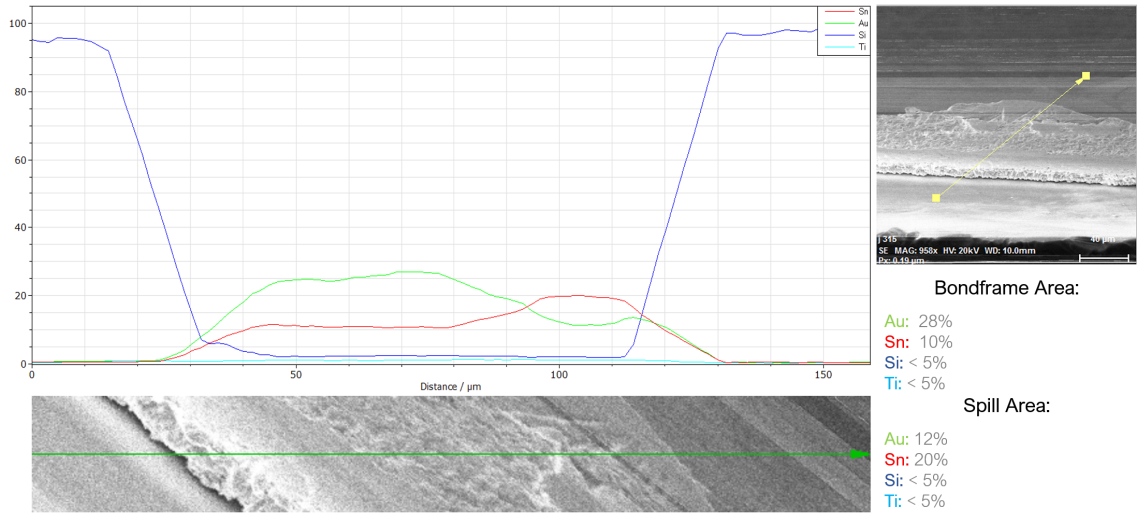


Figure 4.23.: Energy Dispersive X-ray spectroscopy analysis of elemental composition percentage in sheared samples exhibiting interfacial failure mode.

4.2.5. Bond hermeticity assessment

The provision of a tightly sealed, mechanically robust package has proven to be crucial in various applications where the inclusion of CMOS dies is required, as moisture has been known to be a significant factor in the process of IC's degeneration. Particularly in the case of devices intended for chronic service in implantable applications, the packaging method must remain hermetic. Whereas several hermeticity testing methods have been known, examining packages of internal volumes as small as chips tested in this experiment is complicated [44].

The helium fine leak rate test is the gold standard of hermeticity testing techniques. This method relies on exposing the tested sample to the pressurised helium gas to fill any internal cavities via infiltration through the package's cracks and micro packaging defects. Then, the package is transferred to a mass spectrometer to detect any possible fine leak of helium from the inside of the contained sample. Notwithstanding the common use of the method as verification of hermetic capabilities across different industries, its results are questionable unless the package's internal volume is larger than tens of cubic millimetres [8]. Otherwise, the size of the leak may not be detected. It is because of the equipment detection limits and the possibility of most helium escaping from the package during the transfer phase. For that reason, the use of different hermeticity testing methods had to be used.

The first method for an assessment of the hermeticity of sealed samples used was scanning acoustic microscopy. It is a non-destructive method of imaging using high-frequency ultrasonic waves to image the inside of a sample immersed in water. Despite SAM being an imaging method, it can also be applied to identify any significant leaks in the packages without damaging the samples in any way [45].

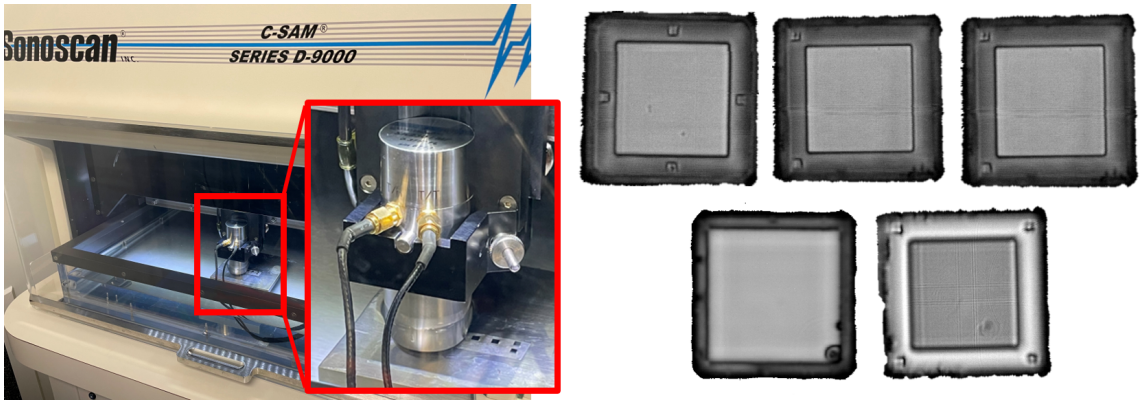


Figure 4.24.: Scanning Acoustic Microscope setup during imaging of bonded samples (left). SAM images of measured samples (right).

In brief, the SAM mode of work relies on the piezoelectric transducer of a typical frequency of 10-400 MHz sending acoustic waves through water, which works as a liquid coupling medium, into the measured sample located at a short distance. Emitted wave is then reflected on any sample's inhomogeneities, and its amplitude is captured back and digitally transformed and reproduced in the form of an image. The amount of the wave signal reflected depends on the acoustic impedance of the measured medium; hence if a sample contains both solid materials and air or water, a clear difference in the image intensity will be noticeable. Because of that, SAM imaging is a suitable method of detection for interfacial delaminations, voids and cracks, which would otherwise be difficult to observe. A representative group of 10 samples was scanned using 100 Mhz transducer generating longitudinal waves (C-SAM D-9000, Sonoscan, USA). Figure 4.24 represents the selection of obtained results that had an acceptable level of the recorded noise. Because of the small geometries of tested samples' structures of interest and the lack of availability of different transducers, the bond interface could not be well observed, and images contained much noise. Nonetheless, no major voids nor cracks were observed, and the high contrast value between a silicon and cavity area indicates no water is present inside; thus, the structure is airtight despite the water immersion. Because of the low resolution of images, another test for hermeticity was conducted based on copper oxidation changes.

Hermeticity was more qualitatively assessed by evaluating the change in the surface oxidation of copper foils as exposed to a wet environment. Copper is known for growing oxide layers, which change the appearance over time, depending on the temperature and the duration of exposure (Figure 4.25) [46]. Thus when Cu is sealed, any change in its appearance may coarsely indicate the tightness of the bond. Initial tests relied on the immersion of bonded samples in deionised water. As the copper source, fragments of copper sheet wiped with IPA were cut to the size that would be able to be accommodated in previously etched lid cavities. The thickness of a copper sheet was selected to be thin-

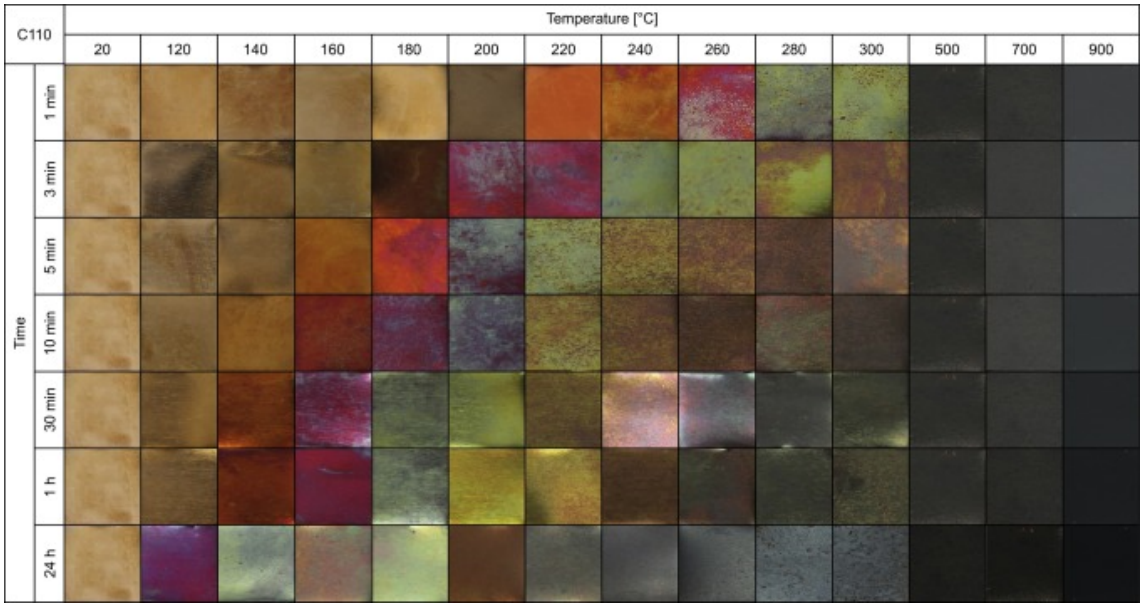


Figure 4.25.: An appearance of copper sheet surfaces as a result of atmospheric oxidation after various exposure times to different temperatures. Reproduced from [46]

ner than the maximum cavity depth not to affect the bonding performance. Fragments were manually placed inside cavities using tweezers and then gently pressed down. Directly after bonding, a bonded sample set of six samples (two of each of 30μm, 90μm and 160μm-wide solder frames) was placed in deionised water for twelve weeks along with the exposed copper control sample. The liquid was kept at room temperature and changed weekly. Then, samples were debonded, and enclosed copper pieces were evaluated for the change in appearance.

For both the control sample as well as several test samples, the copper film colour change was observed as it turned darker, less saturated and more pinkish-brown than previously noted orange shade (Figure 4.26). It was noted that wider frame widths were found more robust in maintaining the hermeticity of packages. Leakages were observed in thinner frames, likely as a result of a higher probability of misalignment between lid and base dies. In 30μm frames, the appearance of voids has more of a detrimental impact because of the smaller volume of the solder available for package protection. All copper pieces enclosed by 30μm wide Au:Sn seal frames showed signs of exposure to water as observed by the copper colour changes. Both samples of 150μm and 90μm-wide frames kept enclosed copper pieces intact after twelve weeks in water.

NNotwithstanding promising results of hermeticity tests employing the immersion in deionised water, another test was conducted to further assess seals' performance in a more corrosive environment on a larger number of twelve samples, including all four frame widths. In order to perform a hermeticity evaluation that will be more reliable, second

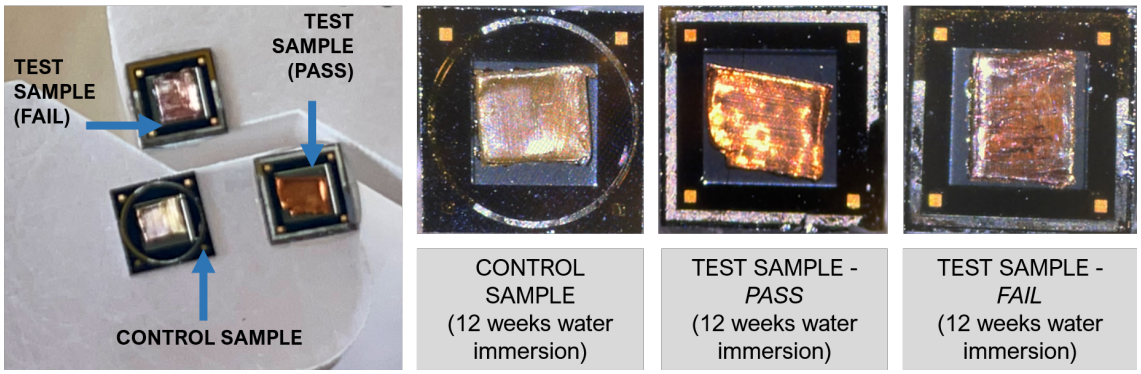


Figure 4.26.: Comparison of an oxidation level of copper films immersed for twelve weeks in the water: control sample, fail:test sample with leaky Au:Sn frame; pass: test sample with hermetic Au:Sn frame.

testing using phosphate-buffered saline, which is more comparable to implantation environment, was used as the immersion liquid. Moreover, this time accelerated testing approach was employed by keeping the solution's temperature elevated at 55° C.

Accelerated testing enables determining prolonged effects of the service environment on the tested sample and thus finding out possible packaging failures in a shorter time. This is typically done by applying additional stress factors, such as heat, pressure, humidity or vibration, which speed up the rate of the ageing process. Widely accepted accelerated testing methods for medical devices are outlined in the ASTM F1980 - Standard Guide for Accelerated Ageing of Sterile Medical Device Packages [47]. According to the guide, storing samples at 55° C for seven weeks equals ageing for approximately one year-storage at room temperature conditions or half-year at 36.6° C. These values are calculated based on the Arrhenius equation, which outlines that increase in temperature by 10° C doubles the rate of chemical reactions. Constant-temperature accelerated ageing techniques are employed more often for polymers than metals, as these are aged through cycled temperature testing. However, in the case of implantable applications, temperature elevation and 100% humidity conditions, and corrosive character of immersion fluid are appropriate conditions for an assessment of Au: Sn-based joints performance.

As in the case of former water immersion tests, copper film pieces were manually placed within lids' cavities before bonding, joined together and then transferred into a glass graduated cylinder filled with phosphate-buffered saline solution. The cylinder was capped with a thick paraffin-based lid to ensure no liquid evaporation takes place, which could otherwise lead to change in the PBS solution's concentration level, and kept in an oven at 55° C. The same liquid volume has been used throughout the test period. In order to avoid deoxygenation, each time the control sample was inspected, the liquid was shaken to introduce some oxygen from the air. Along with eleven tests samples, a control silicon lid die with copper film exposed was immersed and regularly inspected for changes in appearance. Figure 4.27 shows the difference in the look of copper film placed inside

one of the sheared lid sample's cavities after immersion in heated PBS at different time points. All photographs were taken using the same microscope and lighting settings. It can be noted, the first change in the look of the film can be observed directly after going through the reflow temperature cycle as copper turns somewhat darker, less saturated shade. During immersion in the PBS solution, the copper film turns gradually darker and pinkier/browner, while a greenish deposit due to reactions occurring between PBS and Cu surface forms. Moreover, differences in the appearance of the reflown solder can be seen as well, as right-hand-side fragments of remaining Au:Sn turn a darker shade. Based on the observations of the control sample, it has been established that just like in earlier water immersion tests, the sign of copper film exposure to moisture would be first visible as a change of the copper film colour shift to a darker pinkish brown.

Of twelve samples immersed in the heated PBS, a total of nine have not shown indications of a moisture ingress inside bonded cavities, as examined by the inspection of enclosed copper samples (Figure 4.28, Figure 4.29). No precise determination on the influence of a frame width or solder height on the hermeticity could be distinctly established. Nonetheless, the experiment proved the ability of the joints to withstand prolonged exposure to moisture and a corrosive environment with no detrimental impact on the quality. Although this way of hermeticity testing does not provide quantitative data on the seal's hermeticity, it does give a rough qualitative estimation of the ability of solder joints to remain watertight for more extended periods.

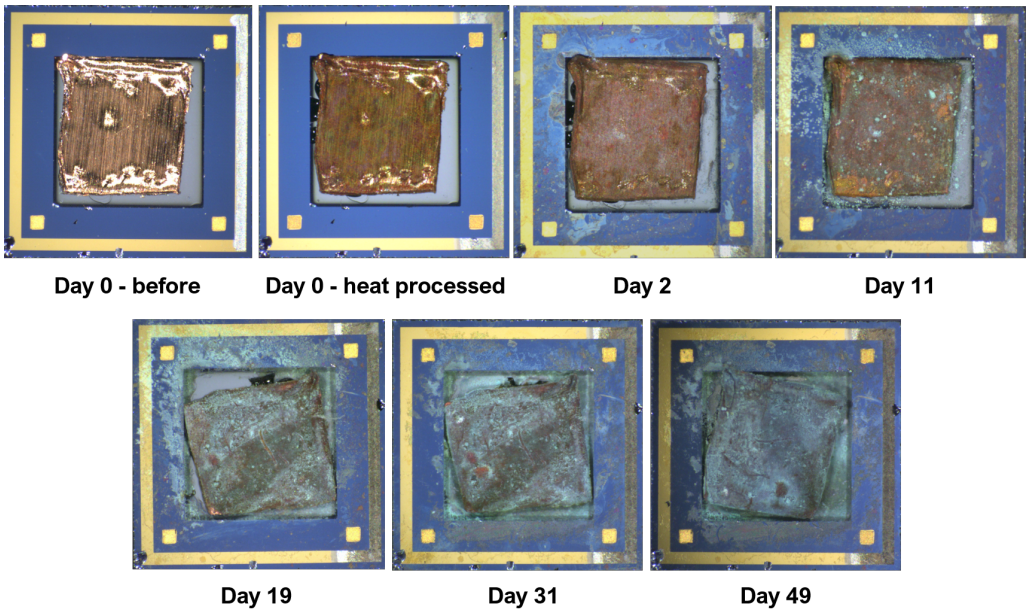


Figure 4.27.: Comparison of a visual appearance of copper film control sample immersed for a seven weeks in the phosphate-buffered saline solution kept at 55° C.

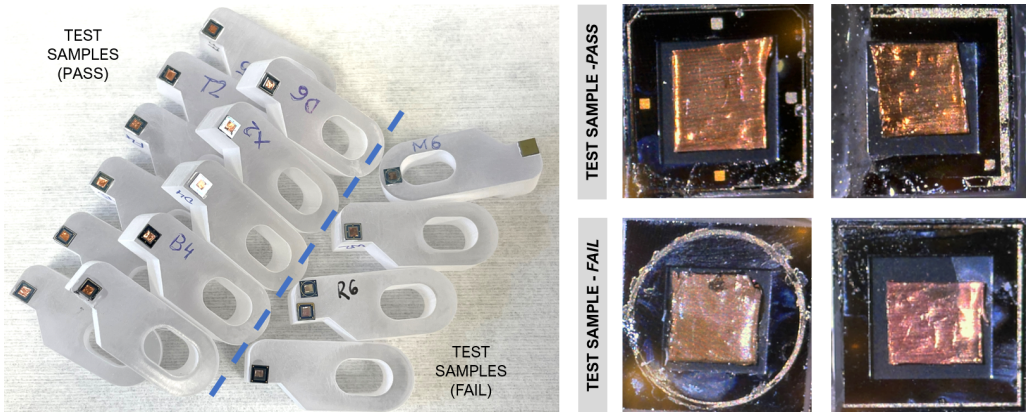


Figure 4.28.: Comparison of a visual appearance of enclosed copper films, following immersion for twelve weeks in the water or seven weeks in heated phosphate-buffered saline solution.

In the future, it is envisaged for the ICs enclosed within the eutectic seal to be provided with on-chip humidity sensors, the readout of which will continuously inform about the state of a cavity's interior. Although none of the seal geometries has exhibited a clear advantage on the bond hermeticity, some conclusions on which design is the safest from the perspective of process yield could be drawn. Because of problems with the layer's grain size influencing composition control and higher risks of misalignment and voids impact in thinner widths, optimum seal geometries found to work the best for die sizes examined were those of middle range of widths (60 μm and 90 μm).

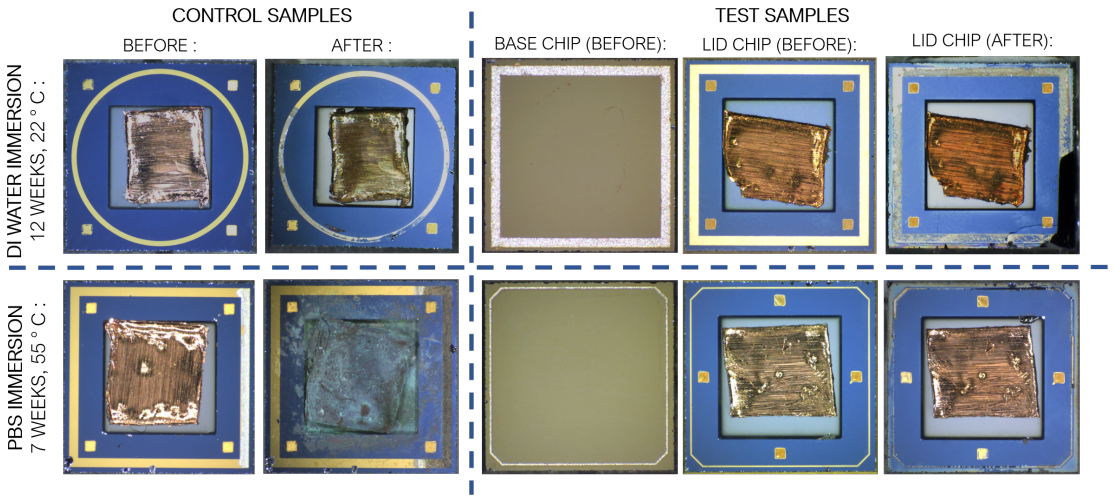


Figure 4.29.: Comparison between copper film oxidation levels as immersed for twelve weeks in deionised water at room temperature (upper row) and immersed for seven weeks in phosphate-buffered saline solution at 55° C (lower row). The left side of the figure represents a view of control samples (exposed to moisture), while the right side shows samples sealed by Au:Sn frame.

4.3. Conclusions

In this chapter, the method for creating solid and hermetic seals using Au: Sn alloy-based bonding is developed and presented. Eutectic frames are fabricated using standard microfabrication methods, and thanks to the maximum process temperature of 320° C can be applied to temperature-sensitive devices, such as CMOS microelectronics dies in implantable applications. On the basis of the presented design and fabrication processes as well as experimental results, the following conclusions are drawn:

- Bonding tests with varying parameters of applied temperature, reflow profile, and frame geometry, along with immersion tests, have shown the possibility of the Au: Sn-based bonding method to create an enclosed, mechanically robust hermetic environment. The presented method appears suitable packaging approach to protect integrated circuitry in implantable applications or any other application where a device must be protected from an external operating environment. The possibility to hermetically seal IC-electronics within an implant, simply and robustly, as with using Au:Sn eutectic, can pave the way to expand the horizon of implantable devices into the new areas.

- Across all geometries and process parameters tested, the average measured bonding strength was over 28 MPa with a bonding success yield of 73%. The dominant shear fracture observed was at the interface of the adhesion layer, pointing to the need for improvement under solder metallisation. Nonetheless, even with only Ti/Au stack underneath, samples have exhibited excellent mechanical properties. It would be of future interest to investigate different under-layer metallisation stacks to further improve the mechanical stability of seals and avoid layers delamination.

- Analysis of an average bond shear force between samples having either single- or double-sided solder rings has shown no need for a solder presence on both base and lid dies. This means that for applications where CMOS dies are used as a base, there would be no need for on-chip electroplating, as solder frames on separately processed lid chips would be sufficient to provide a high-quality seal.

- Immersion tests conducted for the duration of three months, or an equivalent of six months in the corrosive medium, have shown no signs of the moisture penetration in the majority of samples sealed with frames of 90 μm and 150 μm width, whereas some of the thinner 30 μm-wide frames have exhibited leakage.

- Once combined with the right approach to challenges of power and data transmission out of implants [48], the correct packaging methodology, such as the one presented in this chapter, could enable future devices to be potentially safer, less invasive, and easier to implant [49, 50].

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5. Sequential electrochemical deposition for Au:Sn eutectic formation

On account of RoHS directive limitations, as well as because of high power devices packaging needs, in recent years, there has been much interest focused on finding environmentally friendly Pb-free solders (Table 4.2) [3]. Aside from a non-toxicity, a long list of requirements is given to soldering alloys, including good wetting and spreading behaviour, moderate processing temperatures, and favourable mechanical properties [4]. In the case of implantable or biocompatible applications, the use of cytotoxic materials should be prevented or limited. Therefore if alloys contain copper, silver or chromium, they shall be avoided [5]. That leaves a limited choice of available eutectic alloys. Of many lead-free alternatives, binary alloys based on mixtures of tin with second metal (often noble) are promising due to their simple composition and considerably low processing temperatures, especially for packaging applications. Of them, thanks to its unique properties, gold-tin eutectic is one of the most popular and widely used in semiconductor and optoelectronic packaging.

Despite a maturity of the technique and a broad literature on the subject of Au:Sn use in the packaging and its respective deposition approaches, there is a lack of broad availability of methods and technical notes published that would provide a working, repeatable recipe for $Au_{80}\,Sn_{20}$ alloy composition deposition, especially when to be performed at an other than industrial scale [6, 7, 8]. What is more, the majority of currently used gold-tin plating solutions is either based on cyanides and other toxic chemicals or requires strict bath maintenance because of their short lifetime. A less toxic approach should be taken to avoid the remains of the solution's toxic components affecting the biological milieu.

In this chapter, an assessment of the sequential Au:Sn electroplating method using commercially available, moderate-hazard materials for the packaging of biomedical devices is carried out. The fundamentals of the electrochemical deposition process are explained, along with an overview of Au:Sn alloy deposition techniques. An investigation on the deposition process parameters influencing layers morphology the most is presented, together with the stack cytotoxicity assessment.

A portion of the material presented in this chapter has been published in [1, 2]. Part of this work on the biocompatibility testing has been a collaborative research with Dr Meysam Keshavarz.

5.1. Gold-Tin alloy deposition techniques

Steep slopes of liquidus lines surrounding the gold-rich eutectic point of Au:Sn alloy, as seen on its phase diagram, mean that the elementary composition of the alloy must be carefully controlled (Figure 4.3). Minor imbalance of the tin to gold ratio can result in a sudden rise in the melting temperature. Because of that, the choice of an alloy's deposition method, which allows for precision in deposit control, is critical in providing good quality solder seals. There are several possible methods for depositing gold-tin alloy: ready-made preforms, solder pastes, PVD methods of sputtering and evaporation and electrochemical deposition.

The most popular way of delivering Au:Sn alloy to a substrate is commercially available solder preforms. Those can be acquired in a multitude of shapes and thicknesses, are reflowed at a below-eutectic temperature and are of $Au_{80}\,Sn_{20}$ composition (Figure 5.1). The main drawback of the preform use is a lack of availability to acquire preforms of small (tens of microns) dimensions. This is mainly due to the limit of handling capabilities that ensure preforms structural integrity during placement. Another reason for size limitations is how the preforms are made- often by a mechanical singulation from large alloy sheets. Alignment precision and solder oxidation are known problems when using this type of Au:Sn solder source. In terms of linewidth and thickness, preforms are usually within the range of hundreds and tens of micrometres, respectively [9]. As a result, they cannot be used with ENGINI implants, as they would take up too much space of an already heavily occupied chip's real estate.

Alternative to ready-made preforms is the use of solder pastes; however, they oxidise and contaminate the joint with organic binders present within the material [9]. Moreover, the limits of available geometries obtainable with pastes are directly related to the limitations of the screen printing equipment. To aid in achieving the eutectic composition, deposited solder is often slightly biased towards the tin-rich side. Thanks to that, after the consumption of an underlying gold metalisation, the resultant alloy is still eutectic. Such an approach is impossible to obtain when using preforms and pastes because of their ready-made nature.

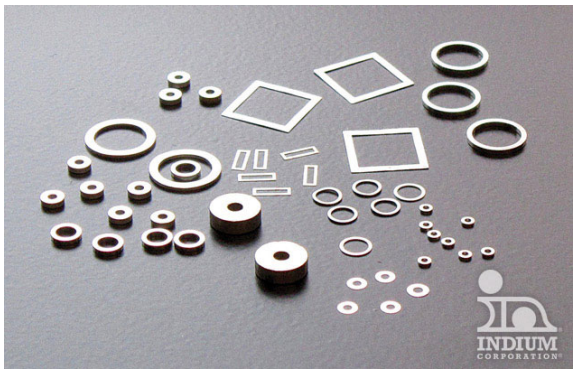


Figure 5.1.: Examples of Au:Sn solder preforms. Reproduced from [10].

Second to preforms is the possibility of PVD-based deposition of Au:Sn alloy. Both sputtering and evaporation methods can be used for that purpose, and similar to any other method, PVD guarantees the best thickness control and uniformity. Since all PVD deposition occurs under high vacuum conditions, there is no risk of an *in-situ* tin oxidising, and deposited metals are of high purity. Nonetheless, both sputtering and evaporation methods cannot deposit layers thicker than a couple of microns, or even a few hundreds of nanometres for high-stress layers, without the danger of peeling and cracking off a surface. Since it has been shown that the gold-tin interdiffusion is observable already after deposition at room temperature, to avoid premature depletion of the tin content from composition, somewhat thicker layers are preferred. Moreover, PVD deposition rates are comparatively low, so the overall cost of production is higher.

Last but foremost, electrochemical deposition provides a flexible, cost-alternative method of a gold-tin alloy deposition. When combined with lithography methods, it allows for the creation of various shapes more cost-effectively in high volume production lines. ECD is compatible with standard microfabrication processes. However, the process is very sensitive. Typically, industrially available Au:Sn alloy plating baths suffer from a variety of problems, including short lifetime, bath instability, plating rates or toxic ingredients [11]. A more detailed description of the electroplating process is provided in the next section.

5.2. Electrochemical deposition of metals

Electroplating, otherwise known as electrochemical deposition, is a deposition technique based on an electrochemical reaction resulting in the growth of metallic deposits on a conductive surface immersed in an electrolyte under the influence of externally applied potential. Passing the current between electrodes immersed in an electrolyte containing complex metal salt ions of the material to be plated results in the hydrolysis and reduction to the pure metallic state.
To explain in more detail, one needs to observe the Helmholtz double region in the vicinity of a cathode's surface, where co-ordinated metal positive ions from the solution are attracted, and distortion of ligands distribution around the metal occurs. As a result of introducing an electric field at the cathode, complex charged anions become polarised, and ligand ions are released. In consequence, the complex breaks up, its component ligand molecules are freed, and the positive metal ion is deposited as a metal atom on the cathode (Figure 5.2b). The process is well established and has been widely applied in semiconductor, decorative and finishing industries. By manipulating different process parameters, deposits of various morphology can be produced, which is widely used, for example, in nanotechnology. Electroplating is based on the redox (reduction-oxidation) reactions occurring in the electrochemical cell at the electrode-electrolyte interface. The standard electrolytic cell consists of (Figure 5.2a):

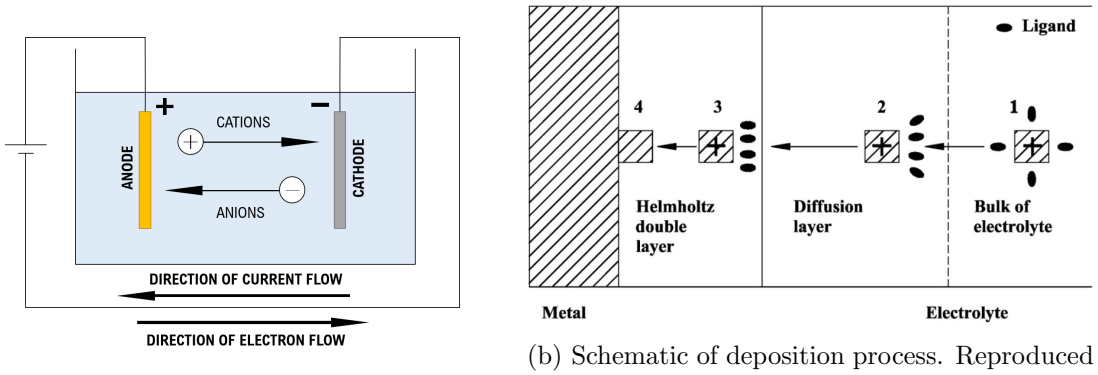
- **Electrolyte**- liquid in which electrodes are immersed. Usually contains salts of metals to be plated and some complexing agents assisting in the plating process. Once dissolved, salts produce positively charged metal ions (M^{n+}). Plating solutions can be of aqueous, alkaline or acidic character, depending on the material to be plated.

- **Working electrode** - (cathode) electrode connected to the negative terminal of the power supply, the place where processes of metal deposition, hydrogen evolution and reduction occur. Made of material/sample to be plated, which must be conductive. Cathode reaction can be presented as follows:
$$M^{n+}(aq) + ne^{-} \longleftrightarrow M(s)$$

- **Counter electrode** - (anode) electrode connected to the positive terminal of the power supply, the place where processes of metal dissolution, oxygen evolution and oxidation occur. Generally made of a high-purity source of the material to be plated, which gets dissolved during the process. In certain systems with the right electrolyte containing dissolved salts of plating material, CE can be realised as an inert electrode made of neutral materials, such as platinised titanium or glassy carbon. Anode reaction can be presented as follows:
$$M(s) \longleftrightarrow M^{n+}(aq) + ne^{-}$$

- **Reference Electrode*** - an electrode having a stable, well-defined and reproducible electrode potential that does not change over time or with the temperature. It allows for the accurate measurement and control of a working electrode's potential without passing any current through it. Necessary in maintaining and controlling a precise potential in the system by serving as a reference.

The built-in potential between the solution and metal to be plated (electrode potential), dependent on the reaction kinetics and sample's surface conditions, must be overcome for the deposition to occur. To influence the potential, plating characteristics such as solution concentration, agitation, applied current density, the distance between the electrodes, or bath temperature can be varied.



(a) Plating cell.

(b) Schematic of deposition process. Reproduced from [12].

Figure 5.2.: Schematic diagrams of electrochemical deposition characteristics.

5.2.1. Au:Sn alloy co-electroplating versus sequential electroplating.

The research on the advanced electroplating process carries on because of the increasing demand for the Au:Sn solder. As mentioned earlier, Au:Sn can be deposited both from a single solution already as an alloy, as well as sequentially from two different chemistries. Each of these solutions presents significant advantages but is not devoid of drawbacks. Alloy co-deposition seems better, owing to the lack of the need for two separate plating setups and thickness control of each deposit; however, all available Au:Sn alloy baths suffer from short shelf life. This is partly caused by the change in electrolyte's tin content caused by oxidation of stannous ions to stannic ions under the influence of the oxygen released at the anode or from the atmosphere. Another issue is the maintenance of Au and Sn potentials at comparable levels so that co-depositing of an alloy of a specific ratio can occur. Moreover, co-electroplating of Au:Sn alloy in a low-hazard manner is complicated because of difficulties in the development of a stable plating electrolyte while avoiding the use of dangerous complexing agents such as cyanides or ethylenediamine [13]. Therefore, alloy-electroplating chemistry requires careful maintenance and highly accurate process control, increasing overall process expenditure.

As opposed to the co-deposition of alloys, sequential electroplating involves using different chemical solutions to deposit each component of the eutectic alloy. When Au:Sn is plated sequentially from two separate baths, the problems of tin oxidation, baths cross-contamination or process incompatibility may occur. As a consequence of the abovementioned problems with alloy co-deposition, sequential electroplating of gold and tin was applied in this study.

5.2.2. Fundamentals of gold electroplating

Gold electrochemical disposition process has been known for ages and founds its applications in a wide range of industries, but predominantly in jewellery, electronics and decorative plating. Gold can be deposited from chemical solutions in various colours, brightness, resistance, hardness or surface finish.

Gold is one of the most stable noble metals, and it can be reduced only by certain chemicals, such as cyanides, thiocyanate, thiourea or halides, to form stable aqueous complexes which can be dissolved in mild oxidising solutions. Several gold electroplating solutions were developed over the years, characterised by a different bath pH, chemical compounds or resulting layer properties, only a fraction of which can be used for a selective plating with the use of photomasks, mainly due to their pH compatibility [12]. For appearance applications, gold plating baths are prepared with additives providing the plated layer of high hardness and bright, shiny finish; for applications in the electronics industry, gold contacts resistance, purity of the material, and corrosion resistance are more important.

TTraditionally the most stable and widespread gold plating baths are cyanide-based. Despite their well-known behaviour, expectable results and the choice of pH values they can operate at, they are highly toxic to use. Moreover, free cyanide ions generated during the process are incompatible with photoresist films causing them to lift. As alternative non-cyanide baths are available, however, they can operate only at near-neutral or alkaline pH and deposit only a soft gold [12].
Keeping in mind ENGINI biocompatibility requirements and willingness to design a process devoted to any steps involving highly hazardous materials, the remains of which could be left at a device surface, sulphite-based ECF60 (Metalor, UK) gold bath of moderately alkaline pH, without additives or grain refiners was selected. The composition of ECF60 is 0.05 M Au (10 gm/litre) with 0.24 M Na_2SO_3 with a pH between 9.5 and 10.0. Sulphite baths are known to produce layers of ductile, soft pure gold with a good throwing power; however, attention must be kept to keep pH within the 9-10 range to avoid problems with the photoresist dissolution. Sulphite-based electroplating baths are considerably less toxic to their cyanide-equivalents; however, as they produce only a matte gold, the roughness of the deposit is a little larger, which can cause issues with the thickness control. Gold

in the sulphite bath is present mainly in $[Au(SO_3)_2]^{-3}$ form, which decomposes to gold in the following reactions:

$$Au(SO_3)_2{}^{3-} \longleftrightarrow Au^+ + 2\,SO_2{}^{3-}$$

A precipitate of metallic gold is formed by the following disproportionation reaction:

$$2\,Au^+ \longrightarrow 2\,Au^0 + Au^{3+}$$

5.2.3. Fundamentals of tin electroplating

Tin plating, also known as tinning, thanks to its good solderability and corrosion resistance, is one of the basic techniques used in today's industry for a variety of applications, such as food packaging, iron corrosion protection, engine bearings and electronics fabrication. Tin ECD baths are generally one of two types that differ in the type of deposit that can be achieved- either bright or matte tin.
Deposited bright tin is shiny resulting from the addition of brighteners to the solution that cause finer metallic grains to be deposited. Such layer is of smooth structure and a bright appearance, but the metal itself is not pure and suffers from high built-in internal stresses because of organic additives. The second type is a matte tin bath that deposits layers of high purity and lower internal stresses from solutions without additives. Moreover, matte tin does not suffer from a whisker formation, a common occurrence in bright deposits. Common issues with tin plating systems apart from a whisker formation is deposited thickness non-uniformity. Tin baths can be both alkaline and acidic, with the majority being the second type. Of acidic baths, three systems are the most prevalent- sulphuric acid-based, phenolsulphonic acid-based and methanesulfonic acid-based. Of the three, the MSA-based bath is comparatively the most stable and the least toxic.
In this work, a commercially available bath, Semiplate-Sn100 based on methanesulfonic acid is employed. In this electrolyte the tin is present in a Tin(II)-methane sulphonate $(CH_3SO_3)_2Sn$ form, which dissociates into Sn^{2+} stannous ions. Similarly to the selection of gold-plating bath, electrolyte choice was made based on the basis of the solution's toxicity and compatibility with photoresists. In aqueous acidic solutions (such as MSA-based bath), stannous ions can also oxidise into Sn^{4+} stannic ions:

$$2\,Sn^{2+} + 4\,H^{+4e} \longrightarrow 2\,Sn^{4+} + 2\,H_2O$$

As the result of an electric field at the cathode (wafer to be plated), both stannic and stannous cations combine with electrons, returning to the zero valence state and forming metallic tin coating, as per reactions below (based on stannous ion example):

$$Sn^{2+} + 2\,e^- \longrightarrow Sn$$
$$2\,H^+ + 2\,e^- \longrightarrow H_2$$

5.3. Assessment of Gold-Tin sequential electroplating for the formation of stable eutectic composition

Regardless of the broad applicability of the electrochemical deposition method across many industries, the process is difficult to control, owing to the multitude of parameters required to regulate during plating. Aside from the previously mentioned need for constant bath maintenance, parameters such as the sample size, cathode to anode distance, bath volume, agitation, and temperature influence deposit characteristics. Especially when considered on a small scale, where no multi-litre plating lines are used, and deposited layers are of micrometre-geometries, electroplating reproducibility is troublesome. For that reason, industrial electroplating of small batches containing a few wafers is expensive, despite the overall low cost of the process. At the same time, prototyping of medical devices is usually performed on a low number of test devices; therefore, reliable methods of low-batch processing are needed. What is more, it is important to ensure traces of possibly toxic materials to which samples are exposed during processing are not left on the surface or within devices. Otherwise, once implanted, the devices can unnecessarily evoke a much larger foreign body response.

With an aim to produce gold-rich Au:Sn layers for packaging of ENGINI neural implants, an investigation of the effectiveness of the sequential electroplating process was carried out. The study was based on the use of sulphite and methanesulfonic acid-based baths that were examined towards the electrolytes compatibility with each other and standard photoresists; deposits roughness, coplanarity and cell toxicity. The assessment of effects of different tin electrodeposition parameters such as current density, agitation and pulsed plating on the ability to form Au:Sn eutectic composition capable of being reflown was undertaken. All depositions were performed using small-scale setups and electrolytes' volumes smaller than $0.5\,\mathrm{dm}^3$. Each electroplating step was optimised to achieve the minimum possible roughness with the best repeatability so that the eutectic composition of Au to Sn can be achieved. Since this work is aligned towards applications that require the device's biocompatibility, it was ensured to limit materials that could potentially be harmful or hazardous to the biological environment. That is why electrolytes were chosen based on their toxicity.

5.3.1. Deposition setup

For all described electroplating experiments, a small-scale, tabletop custom electrochemical deposition setup was assembled. The Versastat-3-400 electrochemical workstation capable of working in both potentiostatic and galvanostatic modes with 6 pA minimum current resolution was used as a power source. That way, as compared to standard laboratory power sources, a better current control could be in place.

Gold deposition requires heating of electrolyte; therefore, a hotplate with an immersion thermometer providing closed-loop temperature control of 0.2° C resolution and magnetic stirring was employed. Initially, in the experiments, the beaker with the solution was placed directly onto the hotplate. Later, to minimise the solution's temperature variations and hotplate temperature overshoot, the setup was adjusted using a heated water bath. To achieve that, the beaker with an electrolyte was placed into a larger container pre-filled with water and Teflon pellets minimising the evaporation.

To ensure better control over the plating current and voltage, depositions were conducted in a three-electrode system consisting of a reference electrode, counter electrode and working electrode (see section 5.2). As opposed to two-electrode systems, the existence of a reference electrode allows for accurate control and the measurement of working electrode potential without the need to apply any potential through it, hence without posing any risk to the sample being plated. Here, three different reference electrodes were employed:

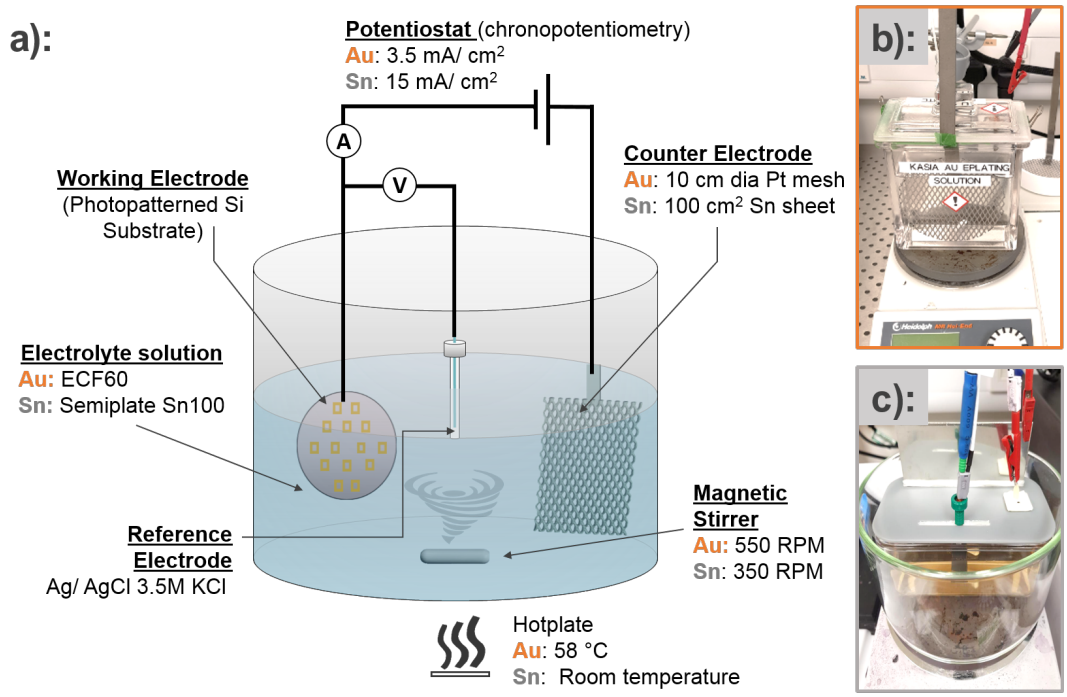


Figure 5.3.: A) Overview of setup used for electrochemical deposition of Au and Sn layers; B) Picture of Au-electroplating setup realisation; C) Picture of Sn-electroplating setup realisation.

either glass tube Ag:AgCl (3.5M KCl) electrodes, double-junction Ag:AgCl (3.5M KCl) electrodes or in-house prepared, agarose-covered Ag:AgCl (3.5M KCl).
Samples to be electroplated were connected as a working electrode. As a solution container, either a standard 2l glass beaker, vertical glass tank or polypropylene box was used. Initially, a vertical glass tank was used in gold plating, later changed to a tall borosilicate-glass glass beaker. In tin depositions, a plastic tank was employed. During all plating experiments, the distance between the substrate and a counter electrode was fixed at 4 cm, owing to the geometry of the containers and the use of custom-designed 3D-printed container lids. To provide an electrical connection between the potentiostat and electrodes, crocodile connectors were applied. In a situation of a sudden loss of connectivity between electrodes and the sample, due to excess moisture or mechanical fault, a layer of adhesive copper tape was applied on the surface of the clip. Before each deposition, the quality of electric contacts was inspected with a digital multimetre. To limit the loss of the gold electroplating solution due to evaporation when heated, containers were always additionally covered with a stretched layer of the paraffin film.
The exact plating current to be applied was calculated for each sample based on the amount of exposed area and current density requirements of each electrolyte. Total exposed area calculations were based on the mask designs described in Section 4.2.1 (Figure 4.4).

Gold electroplating was carried out against a 10 cm diameter round platinised titanium mesh counter electrode in a chronopotentiometry mode. The solution was heated up to 58 °C and maintained at this temperature throughout the process with an average variation of 1 °C. To avoid poor quality layer deposition resulting from worsening electrode contacts, the plating curve (V(t)) was monitored to spot sudden voltage changes as an indicator. Since the solution was being shared across different users, attention was given to monitoring the quality of the bath by inspecting its pH value and filtering through a 0.2 μm syringe filter to remove any contamination or the formed precipitate if it was to be found.
In all experiments described here, tin electroplating was performed against 50 cm^2 high-purity tin sheet counter electrode. As a container, a plastic vertical tank was used. The solution was kept at room temperature of 20-21° C. The solution was filtered every few depositions and regularly exchanged into a fresh one as the older bath turned cloudy. All electrodes used in the experiments were cleaned before each deposition session to prevent any contamination to the plating baths. In order to limit the formation of an ion-depleted solution layer in the cathode vicinity over time, both gold and tin ECD were performed in the intermittent mode with varied plating intervals (15 s plating time followed by 30 s or 45 s of off time). Additionally, the gold electroplating solution was continuously stirred by an immersed magnetic pellet with a speed of 550 RPM. As per the manufacturer's advice, the tin plating solution was not stirred.

5.3.2. Samples preparation

Samples used in electroplating were prepared accordingly to the protocol described in the previous chapter (Section 4.2.2). In general, electroplating was carried out on metallised silicon wafers, or silicon samples, where the underlayer metallisation was formed of thin titanium and platinum layers. Selectivity of a plating area was achieved via the use of photolithographically-defined masks made in the photoresist.

For the prolonged gold-plating sessions and once electroplating parameters were established, Novolak resin-based AZ 15nxt (450cps) photoresist was used as a masking layer. The selection for a negative photoresist was motivated by its high stability upon prolonged exposure to harsh chemical conditions and a favourable undercut profile.

Parametric investigations were performed on the test samples fabricated with a moderately different protocol. There, the geometry of a mask design consisted of the set of ten long, 100 μm-wide rectangles placed at a short distance from each other to help spot any disturbances in the plating behaviour early (Figure 5.4). The design was laser-written directly on the sample rather than irradiated through Cr-mask. Such an approach considerably shortens time as no sample alignment is needed, and multiple small-sized samples can be processed faster. DLW requires the use of positive-tone photoresists; therefore, a thick AZ4562 photoresist was applied instead. The change in the photoresist used in tests considerably shortens processing time compared to its negative equivalent, while its stability is still satisfactory for the short-timed plating experiment.

The characteristics of deposited layers were measured with contact profilometry and visually inspected by optical and scanning electron microscopes. Contact profilometry was done with Dektak X Veeco profilometer with 2 μm stylus tip fitted.

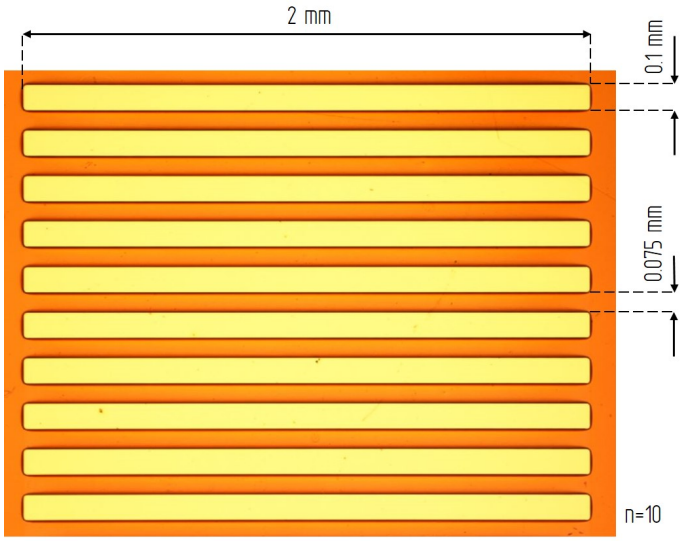


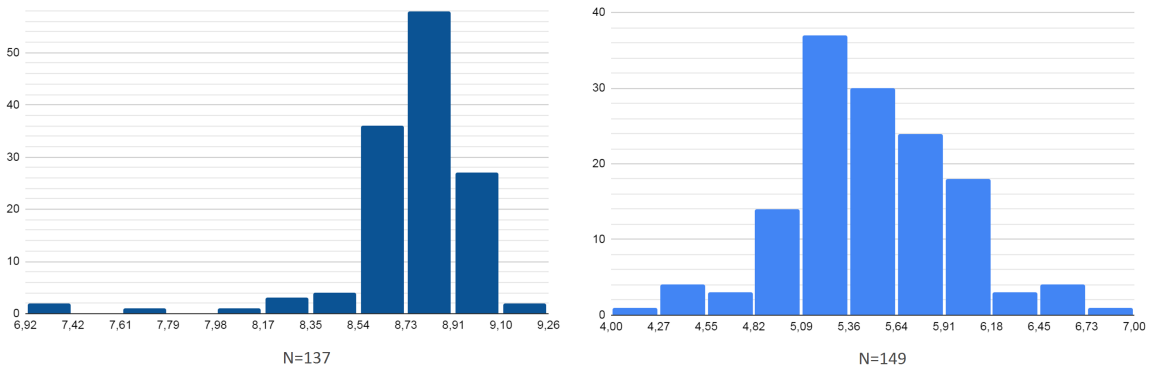
Figure 5.4.: Microphotograph of the test structure designed to spot electroplating irregularities during parametric tests of Sn-plating.

5.3.3. Wafer-level experiments

Pilot testing of the gold-tin deposition was carried out on the wafer-scale in large, 1 l-volume glass beakers. Wafers were patterned only once with a thick, negative-tone AZ 15nXT 450 cps photoresist, which was removed only when the final thickness of a deposit was achieved. Based on the extensive literature of the sulphite-based gold plating, plating current value was 3.5 mA/cm^2 where the in-built stress of an on-silicon gold deposited film is the lowest [14], directly followed by tinning with 20 mA/cm^2 current at a room temperature, as per manufacturer's recommendations.

As a result of differences in the current density between very narrow and broader lines, one of the first observations recorded was the varying plating rate of both gold and tin baths for the features of different widths. Between feature widths of 30 μm and 150 μm the rate of resulting deposition was different by 50 nm/min for gold deposition and by 87 μm/min for tin deposition. To electroplate the entire wafer with the exact concentration of Au to Sn and the required height of features, it must be ensured that all features will be of comparable dimensions (that includes alignment marks). Otherwise, high stand-offs of small geometry features will hinder proper contact when bonding. This is especially noticeable around very fine lines of alignment marks that result in tall deposits; hence, care must be taken to place those as far as possible from the area of importance, preferably close to the wafer exclusion zone. What is more, with width variations, only a fraction of the design present on the wafer would achieve the correct, eutectic composition.

When considering plated features of the same size across one wafer, thickness non-uniformities can be found too. The maximum thickness deviation as measured for the spillage stoppers layer varied between 2- 11% with an average of 3% for the gold plating and 9% when considering features of the same size in the tin plating. Figure 5.5 represents the spread of an achieved deposit thickness across the same wafer when plating to the target height of 9 μm of gold (a) and 6 μm of tin (b). The average obtained gold thickness was slightly



a) Thickness of electroplated gold deposit [µm]

b) Thickness of electroplated tin deposit [µm]

Figure 5.5.: Histograms of the deposited gold/tin layer thickness as measured on structures of a comparable geometry across one wafer.

less than the target. However, the spread of the thickness variation was relatively moderate, reaching 3% of average thickness and a standard deviation of 0.33. The spread of measured tin deposits is much more significant for tin deposits, with thickness variations reaching 9% of an average thickness and a standard deviation of 0.5. Whereas the average thickness deviation of 3% of an entire thickness of the deposit is acceptable, differences of more than one-tenth of the expected final tin deposit cause alignment parallelism to be challenging, especially when the total deposit thickness is to be in the range of several microns.

Differences in an averaged final gold thickness as plated under the same conditions over the same time but on different wafers can differ by up to a few hundreds of nanometres, making up a large percentage of the total target thickness. These likely differ in height due to a non-uniform solution mixing and minor changes in a total exposed area of features to be plated. These variations further prove the need for a continuous inspection of as-grown deposits. The only source of solution mixing is an immersed magnetic pellet. Hence, the solution exchange is the fastest in the areas directly neighbouring it, namely near the wafer edges. The solution depleted of metal-carrying ions is being replaced the fastest, thanks to a fluid velocity drop that grows with the distance from the mixing source. Of notion is also an influence of the shape of the vessel in which plating takes place. The bath volume should be preferably big enough to ensure a uniform circumnavigation of the fluid around the plated sample. However, in laboratory and low-volume ECD setups, it is not always the case. Here, all depositions are performed in containers giving only a couple of millimetres of the clearance between sample edges and vessel walls. Hence the fluid flow could be disturbed. Considering all depositions are performed in the intermittent mode, the overall deposition times become prolonged to several hours at the time. Such

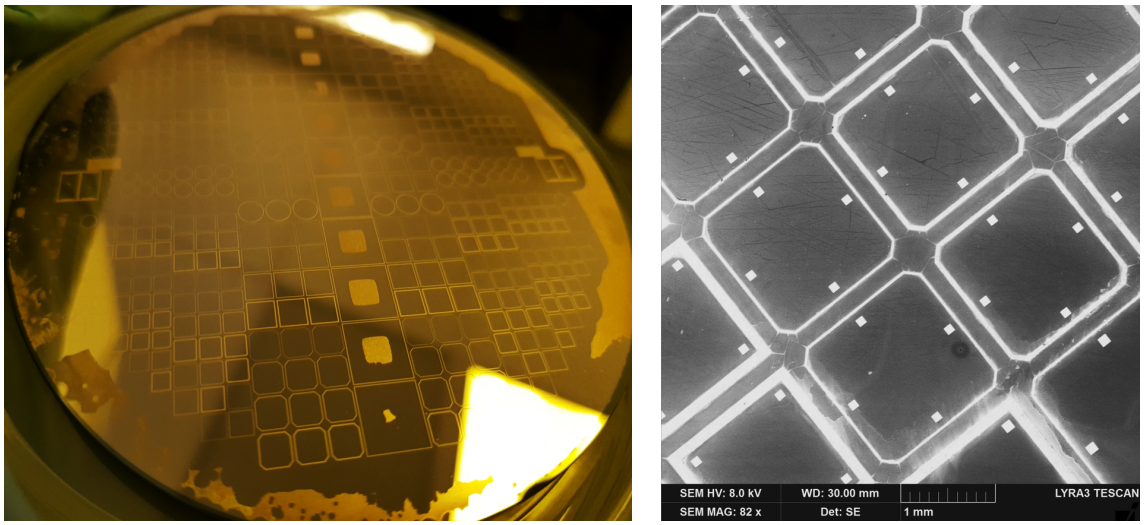


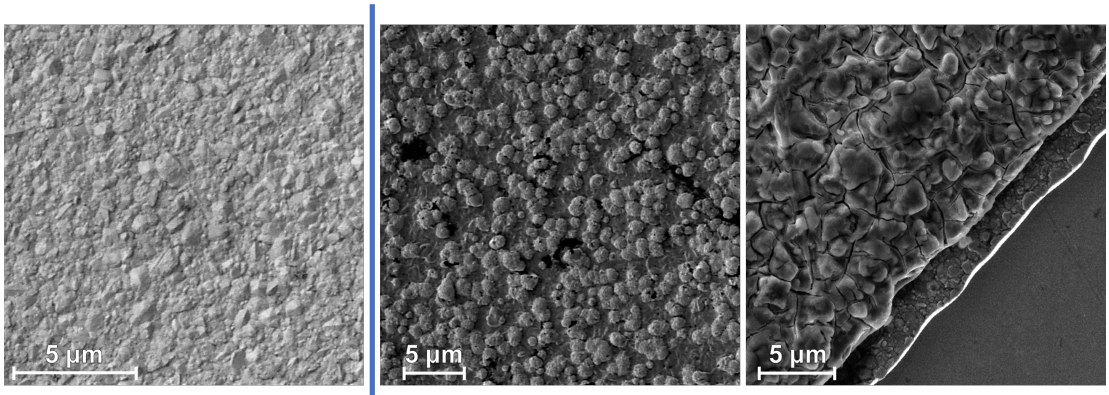
Figure 5.6.: Effects of poor photoresist stability in an electroplating bath: excess metallic deposition around wafer edge and close to feature corners both in global (left) and local (right) aspect.

a long exposure of substrates to the heated (for gold bath) and stirred solution caused some notable damage to the photoresist layer. Although photoresist used (AZ 15nXT 115-450 cps) is a negative tone novolak resin-based polymer that exhibits good stability against chemical exposure, cracks around feature edges were noticed. This could be caused by repeated removal of substrates from the solution for already-deposited thickness control, where several times, wafers were moved from the warm solution and immediately rinsed in cold DI water. The cracking problem can be alleviated to a certain point by limiting the number of inspections; nonetheless, when substrates are transferred from the gold to tin bath of a different pH, cracking and underplating become evident. Once an underplate occurs, it is difficult to remove an excess material without affecting the stack, as all etchants attacking underplate result in removal of the main material, too, unless it is covered by photoresist layer, which requires additional photolithography in a positive tone.

Underplating was significantly reduced by a two-step patterning approach relying on the complete resist removal after the gold electrodeposition and repeated photolithography for the tin plating purpose only. Thanks to that, the plated gold deposit could be appropriately measured with a profilometer against the wafer surface as a reference (rather than against uneven photoresist surface) before the tin is plated to ensure a proper ratio of metals is deposited. Figure 5.6 shows the problem of the photoresist stability and resulting underplating both in a global (wafer) view (left) as well as in a microscopic view (SEM image, right). An additional gold deposit can be seen around the wafer perimeter and in the central space of larger-size frames where the photoresist is lifted. In the SEM image, non-uniformities and excess material deposits at the places where the resist layer cracked around the features' corners can be noticed. A further issue to address in prolonged sequential electroplating is protecting the substrate's backside and rough edges. Despite an inferior adhesion, both gold and tin are extra deposited as thin layers on the uncoated areas of the substrate which have not been PVD-pre coated with adhesion layers before the procedure. From the functional perspective, this does not cause concern as a thin deposit is easily removed ultrasonically in water. However, it influences control of the plating process by increasing the overall plating area to consider when calculating



Figure 5.7.: Deterioration progression of Ag:AgCl reference electrodes as a result of electrolyte precipitation, expressed by a change of colour.



a) Gold b) Tin

Figure 5.8.: SEM photographs of the morphology of deposited layers. Left: gold layer, right: tin layer.

the proper current density. Gold electroplating bath's throwing power is large enough to provide uniform coatings over entire silicon wafers with a steady deposition rate, in contrast to the tin ECD solution where severe frothing, even in the absence of additional mixing measures, can be observed. Because of bubbling, tin layers locally exhibit spherical over-deposits of a poor anchorage to the substrate. The size of the tin over-deposits and resulting non-planarity of the layer could hinder the bonding phase; hence they need to be removed through ultrasonication in water. Moreover, these deposits are releasable to the plating bath, causing micro masking problems and requiring frequent solution filtration. Because of the solution's precipitates, the ceramic diaphragm of the reference electrode becomes clogged as plating time increases (Figure 5.7). As an initial solution for that problem, cheaper, in-lab custom-made reference electrodes were used instead. These were made of polypropylene tubes filled with 3.5 M KCl-based agarose gel, within which chlorinated silver wire was placed. Such electrodes were of single-use only and suffered from leaking of the gel into the electroplating solution. As a final solution, a commercial, double-junction Ag:AgCl reference electrode was used, where the ceramic diaphragm was cleaned and sanded down after every electroplating session.

From the morphology perspective, gold and tin formed ECD significantly differ from each other (Figure 5.8). Gold deposits form irregular, dense layers of material that uniformly coat the sample's surface despite some moderate roughness observable. Such morphology characteristics are in agreement with the type of the bath used- as sulphite-based electrolytes produce matt, soft tin of slightly increased roughness characteristics. On the other hand, tin creates either non-continuous layers of large grains or cracked layers of a high roughness. Irregularly developed morphology makes it challenging to ensure the thickness accuracy of deposited material with thin eutectic stacks. Large spherical grains form islands on the exposed surface and accumulate in clusters. The average grain size

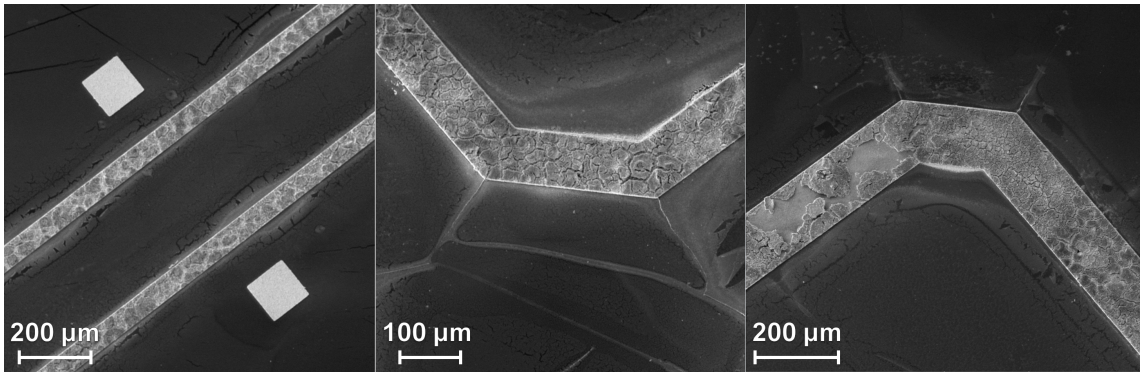


Figure 5.9.: SEM images of 5μm-thick thermally-cycled wafer level-plated Au:Sn stack. Cracks on the top tin layer and the absence of a phase mixing between elements can be observed.

is approximately 2-3 μm; therefore, when a tin deposit of twice the thickness is to be deposited, it is challenging to estimate the actual layer thickness as deviations caused by the grain size obscure it.

The initial wafer-level study has demonstrated some of the critical challenges in using the sequential approach to electroplating for the deposition of Au:Sn eutectic stacks in the form of thin frames. Gold-tin eutectic formed by two-stage sequential plating is challenging to control unless thicker-electroplated or deposited directly as an alloy. Whereas in small-setup conditions, the gold deposition over the wafer size exhibits a thickness uniformity on the satisfactory level, cluster-like tin deposits and localised plating rate variations complicate achieving the correct eutectic ratio of materials. Diverse characteristics of electrolytes lead to layer non-uniformities and problems in subsequent bonding steps, especially if the stacks of lower heights are needed. Figure 5.9 represents the SEM image of the reflown surface of the Au:Sn stack, which had been wafer-level plated to the total stack height of 5μm (Au: 3μm, Sn: 2μm). Electrochemical deposition of stoichiometrically proper Au:Sn eutectic stack of that height was shown unsuccessful. An apparent absence of phase uniformity can be noticed, with the tin layer cracking on the unchanged gold surface, possibly as a result of a mismatch between built-in stress of each layer.

Different pH characteristics of plating baths cause problems in choosing the suitable masking material too. Positive photoresists do not withstand prolonged exposure to the alkaline character of gold plating solution, whereas negative resists, such as dedicated AZ15nxt, show a significant impairment upon exposure to chemicals of varying temperature and acidity. The issue can be somewhat alleviated by repeated patterning before each plating; however, it is likely to compromise the seal geometry accuracy and prolong an overall fabrication time. To further investigate tin deposition characteristics, chip-level tin plating tests were designed to establish the effectiveness and compatibility of two plating chemistries to form small-size eutectic-composition frames on silicon.

5.3.4. Chip-level tin plating

To assess the possibility of the tin plating solution to produce smooth, controllable layers, experiments aimed at finding the right set of deposition properties that would fit the properties of the deposited gold layer were conducted. The overall setup size was reduced. The plating vessel was exchanged to the 0.3 l polypropylene tank, sample sizes reduced from a wafer-size to chip-level, and magnetic stirring pellet introduced. Additionally, a pulsed plating approach rather than an intermittent plating was evaluated. All in order to potentially reduce the level of solution frothing resulting from a rapid hydrogen evolution during the plating, smoothen the deposit morphology and reduce built-in stresses to prevent the tin from cracking off the surface of underlying gold. By reducing the size of plated samples, it was believed the morphology of the deposits would differ too, as fewer hydrogen bubbles will be released at once within the volume of a solution. What is more, by adding agitation, removing any over deposits and surface bubbles could be faster, thus potentially improving the tin layer morphology.
To shorten the processing times, diced and DLW-patterned samples were used, prepared accordingly to the protocol described in the section 5.3.2 (Figure 5.4). All depositions were performed at room temperature. Effects of stirring rate, current density and pulsed rather than continuous current electroplating on the morphology and uniformity of obtained layers were investigated.

Agitation influence

As a first measure, the influence of agitation on deposition characteristics was analysed. The use of agitation in the ECD process can aid in transporting a fresh solution in the vicinity of a plated surface. As the plating process progresses, metal-carrying ions in close proximity to the cathode get depleted. Thus the introduction of stirring helps to counteract that process. However, care must be taken to avoid generating turbulent flow around the electrode as it may lead to the deposition non-uniformities.
Five samples were prepared, the deposition current density was arbitrarily selected at 15 mA/cm^2, which was within the range suggested by the manufacturer (15-25 mA/cm^2). Each sample was deposited in the chronopotentiometry mode for 60 s without breaks. After plating, each sample was cleaned in solvent to remove the photoresist layer and then measured with a contact profilometry both along the plated rectangle lines as well as across them. The averaged thickness value of each pass was noted for every rectangle present in the design. Figure 5.10 represents the relation between an applied agitation and the resulting deposit thickness, including standard deviation for each measurement. Compared to the lack of stirring scenario, the introduction of an agitation moderately increases the thickness of a grown deposit. This is in line with what can be expected once the rate of solution mixing is increased. Outlier measurement was recorded for the sample plated with the 300 RPM agitation. While this value is unexpected, it is likely a result of

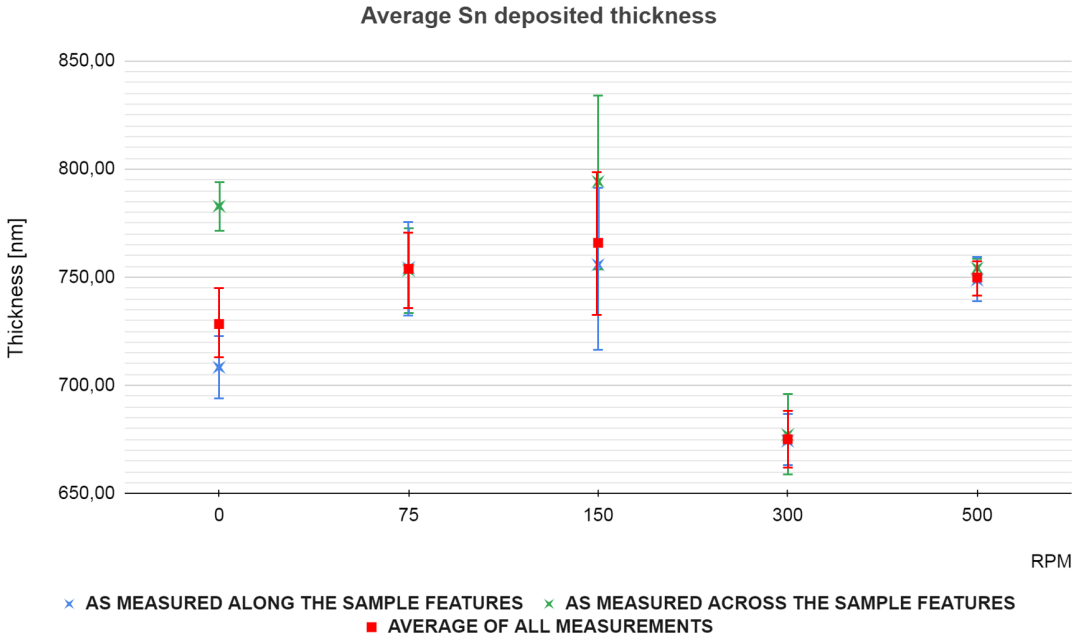


Figure 5.10.: Average layer thickness variation including standard deviation of deposited tin layers in relation to different rates of electrolyte agitation.

underestimating the exact plating area and thus the application of different current than aimed. When looking at the standard deviation of recorded thickness values, it can be noted that, aside from the sample plated with 150 RPM, averaged deposit uniformity increases with an increase of the stirring rate. Analysing differences between thicknesses and variation of recordings between measurements done along and across sample's surfaces, it can be noticed that the most significant difference is observed for the sample plated without any agitation. An increase in the stirrer's revolutions' rate leads to a decrease in the standard deviation of the layer's thickness. Whereas that could mean the application of higher agitation rates is beneficial, one should analyse the morphology of the layers first, as values recorded for all stirring rates are in the comparable range.

Figure 5.11 presents SEM images of surfaces of the abovementioned samples. Visual inspection of the layers reveals minimal differences between the morphology characteristics of samples plated under different agitation conditions. One exemption is the sample plated with no agitation present, which appears to have a more rugged appearance of tin grains, showing the beneficial effect of stirring. Whereas layers plated with agitation rates of 150 RPM and 300 RPM appear somewhat smoother, no significant indicators of the superiority of given agitation rate can be indisputably found. Of the samples plated with stirring, the one deposited with 500 RPM exhibits somewhat more developed morphology, likely as an effect of a near-turbulent electrolyte flow at that agitation rate in the vessel of

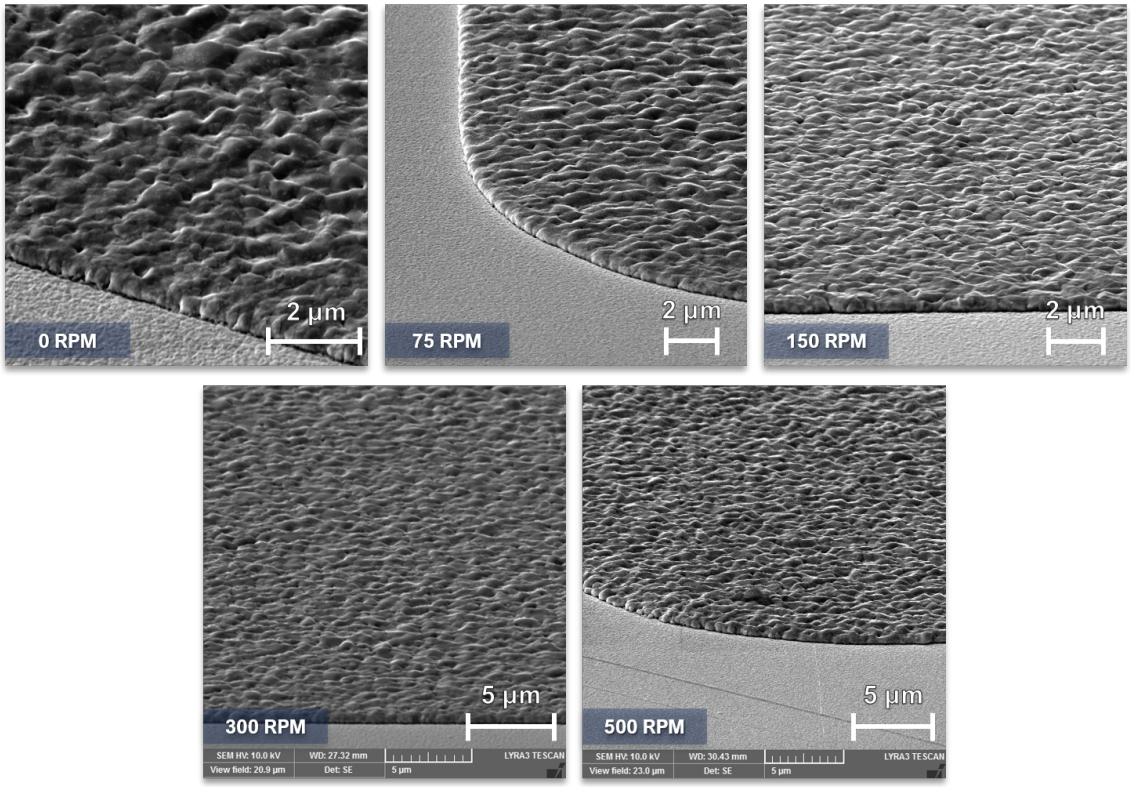


Figure 5.11.: Morphology of tin deposits in relation to the rate of agitation applied during electroplating.

the size used. What can also be observed is a significant change in the layers' morphology compared to the wafer-level plated structures presented above. Likely, it results from a significantly reduced plating current in relation to the electrolyte volume, and therefore significantly reduced hydrogen generation.

At this point in the analysis, it was concluded that all but 0 RPM agitation rates, could be employed, whereas 150 RPM and 300 RPM seemed the most promising thanks to their low deviation of thickness measurements. As can be observed from the averaged measures (red squares on Figure Figure 5.11), the highest uniformity of the thickness across the samples' design can be noted for samples plated with an agitation of 500 RPM shortly followed by 300 RPM and 75 RPM. Summarising visual inspection results with SEM and analysis of measured thicknesses results, it was further decided to proceed with the agitation of 300 RPM. Whereas the agitation with the speed of 500 RPM yielded satisfactory uniformity results, a more developed morphology of obtained layers and near turbulent behaviour of a liquid inside the plating vessel at that stirring rate could lead to inconsistency across multiple plated samples. Compared to the non-agitated solution scenario, the agitation of 300 RPM provides better layer morphology while still securing good uniformity results.

Current density influence

The second parameter analysed searching for optimum parameters allowing for the sequential gold-tin electrodeposition was the plating current density (I_d). It is the single most important and influential parameter to control during the ECD process. In general, the electroplating mechanism on a plated surface can be brought down to two essential phases- material nucleation and growth mechanisms, including the deposition rate, both controlled by the current density. The nucleation rate is directly proportional to the increase of current density, contrary to the growth processes. For that reason, smaller grain sizes can be obtained at higher deposition current densities [15]. However, a higher current leads to the local increase of pH in the proximity to the cathode, leading to the conflict between a material deposition and hydrogen release [16]. The generation of hydrogen bubbles is recognised as a contributor to the increase of internal stresses in the grown layer and the deposition irregularities such as voids and local over-deposits; therefore, its impact should be minimised wherever possible [17].

To evaluate the effect of current density, six different samples were plated in a chronopotentiometry mode, continuously for 60 s, with an agitation set for 300 RPM. Current density was varied within the range of 5-35 $\mathrm{mA/cm^2}$. Like before, when finished, samples were cleaned and inspected with SEM and contact profilometry.
To account for the morphology influence, this time, an average roughness value (R_a) was also computed for each measurement. Being a measure of surface fluctuations, average surface roughness is calculated as an arithmetic average of absolute values of thickness deviations from a mean line as measured along given measurement length L, where y is the profile height (thickness) function:

$$R_a = \frac{1}{L} \int_{x=0}^{x=L} |y| \, dx$$

In other words, the average roughness value is an average of a group of single measurements of sample's peaks and valleys.

As mentioned earlier, I_d directly influences the growth rate of the deposit. The maximum current which can be passed through the electrolyte is limited and depends on the concentration of the metal ions available in the bath. Based on the manufacturer's information, optimum current for the MSA-based tin plating bath 20 $\mathrm{mA/cm^2}$, however, the acceptable range is in between 10-30 $\mathrm{mA/cm^2}$; therefore, a selection of the values within the range as well as low and high-range outlier values were tested. Once plated, each sample was measured at forty different places, both along and across rectangle structures, and the mean deposited thickness value was calculated by averaging all measurements taken. Figure 5.12 represents the graph of a relation between the average deposit thickness of the tin layer after one minute of electroplating at different applied current densities. As

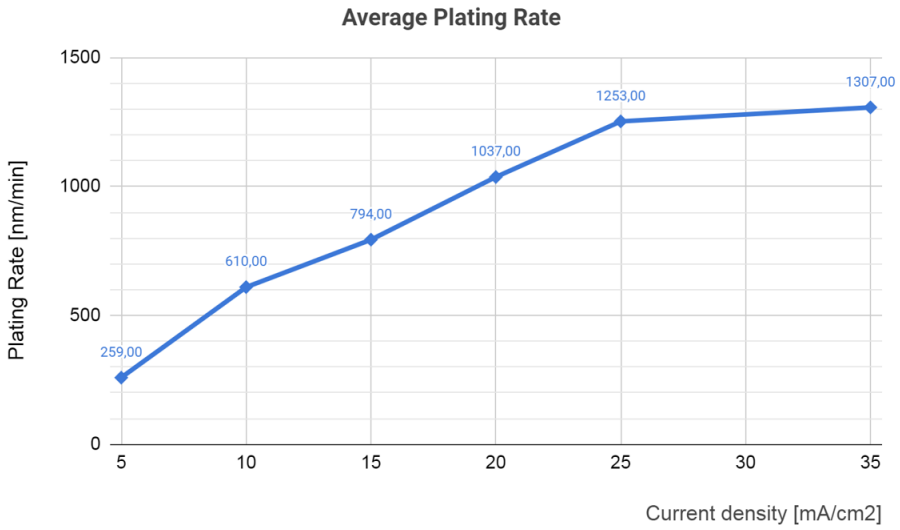


Figure 5.12.: Average plating rate of tin from the MSA-based chemistry at different current densities.

expected, the correlation is directly proportional, albeit not linear. If not for the more significant extent of hydrogen evolution, even thicker layers of tin deposits could likely be achieved at higher current densities. For utility purposes, it is better to maintain the rate of the plating process on the lower end of the range, as it allows for more accurate control over the growth process. At current densities too high, rapid hydrogen evolution at the cathode occurs, accompanied by the growth of a fragile, rough, dendritic deposit. To assess deposition uniformity at different current densities, average computed roughness was plotted against the applied I_d, along with deposited thickness standard deviation, both to give an insight into the process variability (Figure 5.13).

With a larger current applied, more fluctuation in both the thickness uniformity, as well as more surface roughness, can be noted. Dispersion of the tin layer thickness locally plateaus between 10-25 $\mathrm{mA/cm^2}$, which is in agreement with the manufacturer's range of recommended current densities. There was no deposition performed and analysed for the plating current density of 30 $\mathrm{mA/cm^2}$, which is also found within the manufacturer's recommended range. Therefore, it should be noted that the plateau region is possibly extending towards that current value. The least average roughness and thickness variation was noted for the lowest current densities of 5 $\mathrm{mA/cm^2}$ and 10 $\mathrm{mA/cm^2}$ which resulted in the plating rates of 259 nm/min and 610 nm/min, respectively. Some correlation between the thickness standard deviation and the surface roughness can be observed, as both plots follow a similar pattern which stabilises in 15-25 $\mathrm{mA/cm^2}$ range. That is likely caused by the fact that the deposited layer's thickness depends on the growing layer's grain size.

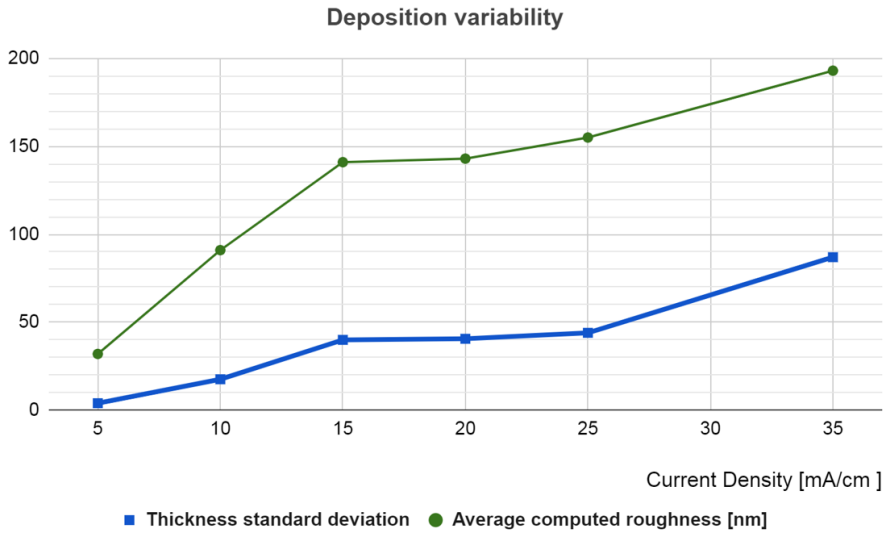


Figure 5.13.: Tin electrodeposition variability from the MSA-based chemistry at different current densities.

Since numeric values do not represent the complete information about the state of the deposited surface, visual morphology evaluation was performed via SEM analysis (Figure 5.14). In spite of the tin layer deposited at the smallest tested current density ($5\,mA/cm^2$) having the lowest deposition variability according to profilometry experiments (Figure 5.13) when inspected visually with SEM, it is clear the deposited layer is plated in a more cluster-like manner, with loose gaps in between the grains, affecting the plating density. Within each cluster, boundaries between grains are relatively smooth and uniform. The edge effect can be observed where near structure boundary the density of intermediate gaps is more significant. The average grain size is estimated to be around 600-800 nm.

Increasing current density by $5\,mA/cm^2$ leads to the significant change in a surface texture exhibited by the denser structure, no longer interspersed by gaps. Grain boundaries are more pronounced, with an average size within the range of 1-1.4 μm. Further smoothened are grains observed in layers electroplated with a current density of $15\,mA/cm^2$, where the average grain size marginally shrunk to an average of 1-1.2 μm. Within this range, layers are bright and moderately uniform. Further increase of the applied current density leads to the development of an incrementally more rugged morphology of rough, dendritic grains and scattered peaks of local over-deposited clusters.

At higher currents, the grain growth is comparably lower than the rate of the nucleation, thus as mentioned earlier, deposits obtained with these parameters should exhibit a fine-grained morphology. However, the change in deposit morphology can be observed because the degree of hydrogen evolution increases alongside the plating rate. Because of the vast stream of Sn^{2+} ions reaching the cathode, and thus a heavy diffusion of tin ions that get

replenished from the bath, the gradient at the cathode-electrolyte interface is formed, and plating occurs randomly at the cathode surface wherever any nucleation sites are found. Because of that, unsteady growth occurs, resulting in rugged, dendritic layers of irregular orientation. Based on all experiments performed on the influence of current density, it was estimated that the lower-end of the manufacturer's acceptable range of I_d as plated on the small sized-samples would be further used in the electroplating for the deposition of eutectic Au:Sn layers.

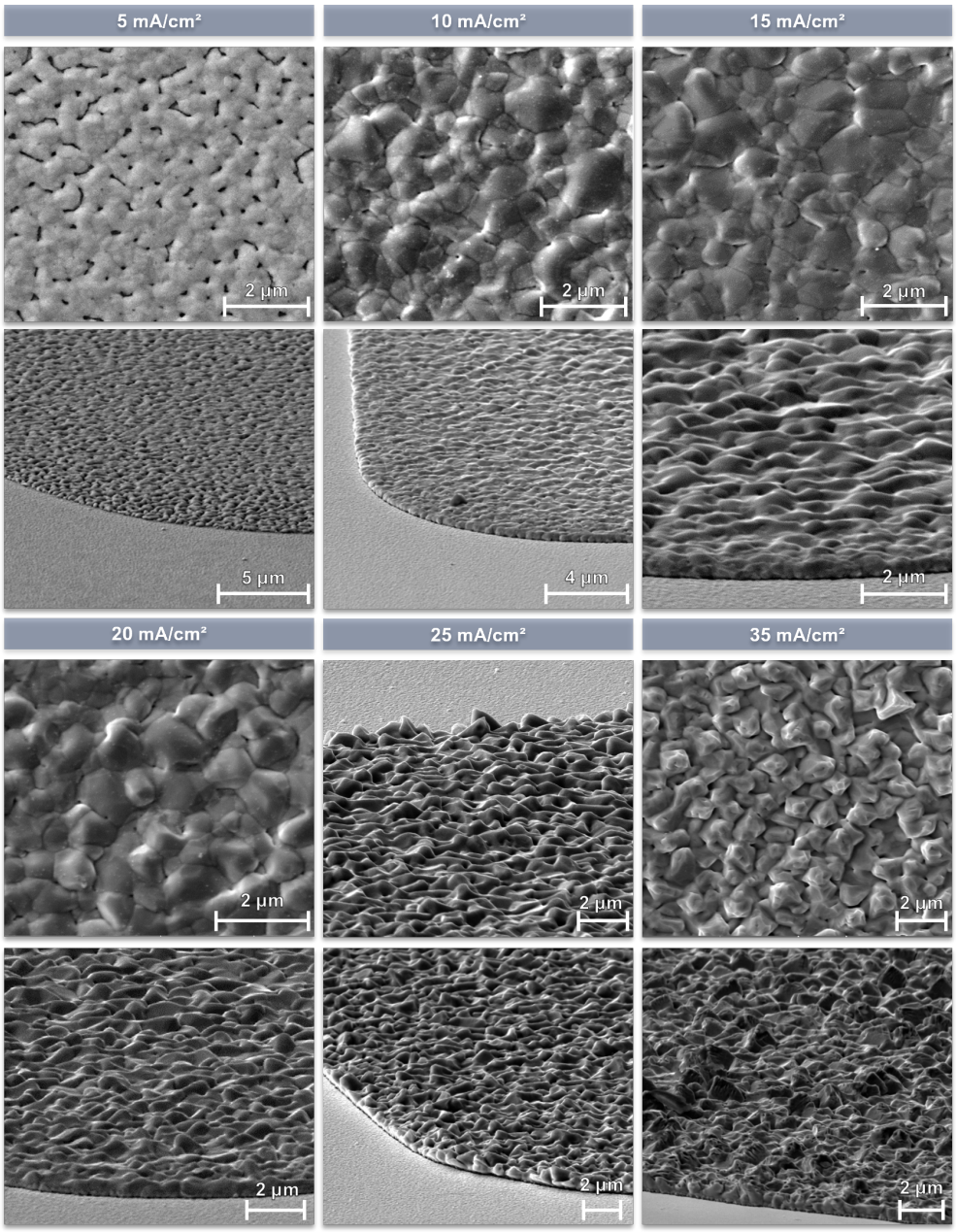


Figure 5.14.: Morphology of tin layers deposited for 60 s at different plating current densities.

Pulsed electroplating

To review whether the morphology of produced tin deposits plated from the MSA-based electrolyte can be further improved without using any bath additives, the pulse (AC) electroplating approach was examined. AC electroplating of tin has been studied for the deposition of the material from stannous sulfate and stannous chloride electrolyte baths; therefore, a short study on its effectiveness from the MSA-based bath was conducted here [18, 19, 20]. The foremost objective of the AC plating is an improvement of layer characteristics by changing how the crystallisation process occurs at the cathode interface. With modulation of the pulses lengths when the plating current is applied, the nucleation rate can be influenced, which in turn directly affects deposited morphology, such as grain size and orientation [13]. Periodical inversion of the signal polarity can also decrease thickness variations, as it allows for a better replenishment of material's ions in the cathode vicinity.

Unlike the standard DC electroplating, which can be performed by controlling the current within the electrolyte bath over time, pulsed ECD also includes the modulation of the length of on and off times during which the deposition takes place. Generally, every pulse can be characterised by an on-time (T_{on}) during which the electroplating current or potential is applied, and an off-time (T_{off}) when no current is applied. Frequency is the reciprocal of the sum of that time. The relation between the on and off pulses is known as the duty cycle:

$$Duty\,Cycle\,(\%) = \frac{T_{on}}{T_{on} + T_{off}}$$

When the duty cycle is 100%, no pulses are applied, and electroplating works in the DC mode with constant current (or potential) being applied over time. Current density in the AC electroplating is equivalent to I_d in DC electroplating, and it is expressed in the form of the average current density I_{avg}:

$$I_{avg} = Duty\,Cycle \times I_{peak}$$

Where the I_{peak} is the peak current density applied. By modulating an average current density, pulse duration, and frequency, the properties of the deposition process can be changed. At a higher pulse duration at low frequencies, the double region is more effectively charged and discharged, resulting in bigger grain sizes as compared to the fine grains obtainable at higher frequencies. It was reported that the size of deposited grains decreases with an increase of a duty cycle up to the value of 44%. Above that, larger grain size is observable, as in the DC plating [21]. During the T_{on} time, a hydrogen evolution occurs. At lower duty cycles during T_{off} there is more time available for the dissolution of hydrogen molecules in the electrolyte so that less gas ends up being absorbed in the deposit, resulting in more dense and uniform deposits. Lower duty cycles below 20% are

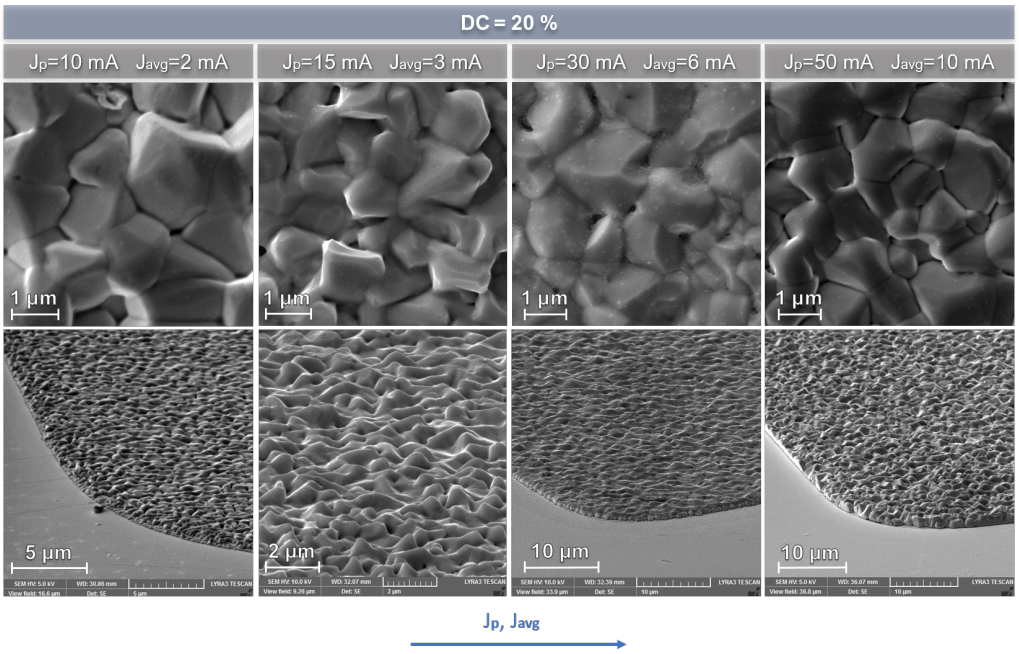


Figure 5.15.: AC tin electrodeposition: morphology of layers deposited with different peak and average current densities at 20% duty cycle. All current values are shown per square centimetre area.

therefore preferred to avoid an increase in the deposit porosity [22].
As mentioned, the average plating current in pulse electroplating is a similar parameter to applied current density in DC electroplating. The same value of I_{avg} can be obtained for different peak current densities and variations of on and off times. Using higher I_{peak} values enables crystallisation of deposits with smaller grains while modulating the time prevents depletion of tin ions and aids uniform growth process.
Nine different samples were deposited with tin layers in the pulsed plating process of varied duty cycle, peak current density and average current density, to evaluate if any morphology changes take place. Tested parameters varied between 5% to 20% for duty cycle, 10 mA/cm^2 to 100 mA/cm^2 for peak current density and 0.5 mA/cm^2 to 10 mA/cm^2 for average current density. All depositions were performed at room temperature, with an agitation set at 300 RPM, pulse frequency of 90 Hz and total T_{on} time of 60 s. The value of applied frequency was selected based on the literature of pulsed-tin plating from other chemistries [23].

Figure 5.15 represents SEM images of the tin deposits morphology as electroplated in a pulsed mode, keeping 20% duty cycle at 90 Hz, while varying the maximum peak current density. As can be seen from the images, the surface of layers is somewhat comparable for all four tested samples. The average grain size decreased moderately with each current incrementation, being: 1.8 μm for I_{peak}=10 mA/cm^2; 1.3 μm for I_{peak}=15 mA/cm^2; 1.3 μm for I_{peak}=30 mA/cm^2; and 1.1 μm for I_{peak}=50 mA/cm^2. The thickness of the de-

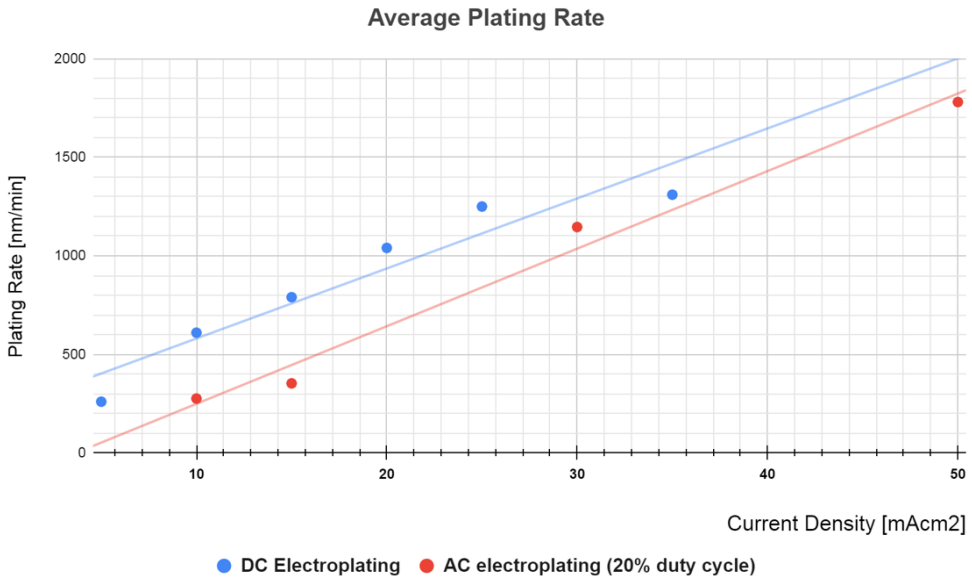


Figure 5.16.: Comparison between an average rate of the tin deposition at different current densities and peak current densities in the AC and DC plating.

posit increased along with current values nearly linearly; however, obtained thicknesses were less than those obtained during DC plating (Figure 5.16). That is by large because during off times, processes of adsorption and desorption take place. The nucleation of new grains occurs at the beginning of each *on* pulse, followed by the growth of the grains, so by multiplying the number of pulses, more of the new nucleation sites appear, and the average grain size is smaller as compared to DC electroplating.

Secondly, while keeping the maximum peak current density at a constant, 10 mA/cm^2 level, duty cycle and therefore average current density was varied. The value of the peak current density was chosen to fit one of the values previously tested during the DC electrodeposition so that the comparison between them is possible. Average current densities were very close to each other, ranging from 0.5-2.0 mA/cm^2. Thickness-wise, with an increase in the duty cycle and average current density, the average plating rate have risen only slightly. However, with changes in the duty cycle, differences in the morphology of deposited layers were observed. At the lowest duty cycle of 5%, the deposited layer is of non-uniform coverage with gaps visible in between grains, which connect to each other, forming somewhat network-like morphology. Increasing duty cycle by 5% and 10% leads to the densification of deposit and an increase in the granularity of the layer. Surfaces obtained when electroplating at these values highly correspond to those plated in the DC mode at 10-15 mA/cm^2 range (Figure 5.14). At 20% duty cycle applied, grain sizes underwent significant enlargement, likely because of an increased T_{on} time, triggering more gas evolution.

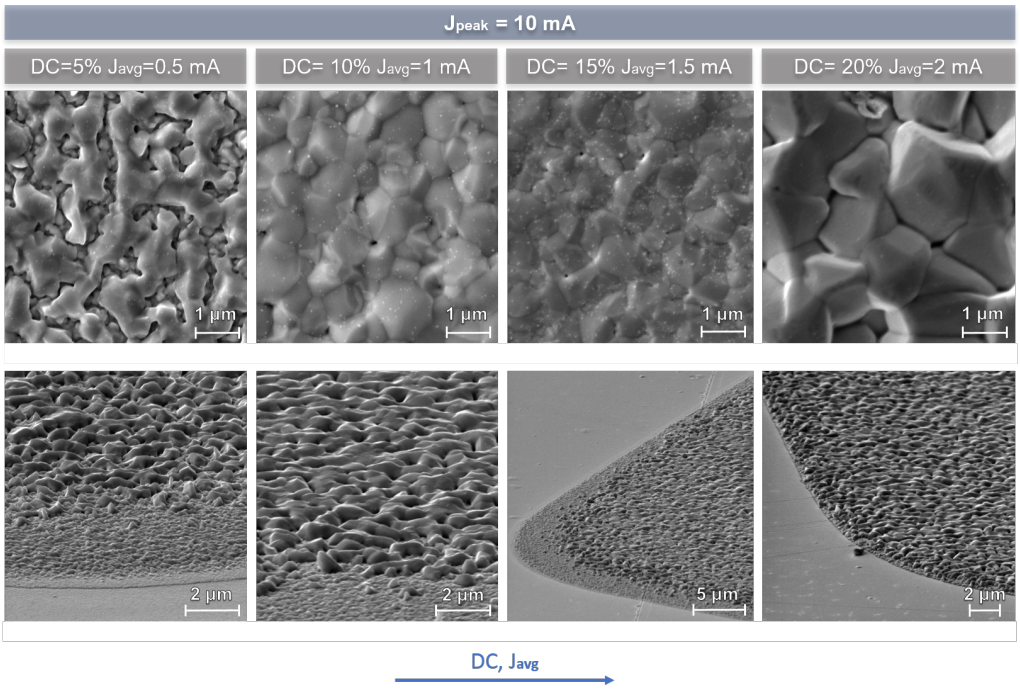


Figure 5.17.: AC tin electrodeposition: morphology of layers deposited with different pulse duty cycles and average current densities at 10 mA peak current density. All current values are shown per square centimetre area.

Finally, the effect of varying duty cycles at a constant average current density was investigated. To keep an average current density at the comparable level, I_{peak} was varied between 50-100 mA/cm^2. Duty cycle changed from 10% to 20%. In this test, all observed samples exhibited surfaces of high roughness and well developed, rugged morphology (Figure 5.18). When analysing high magnification images of the deposited films' side view, a multitude of minuscule voids can be observed. These voids result from a very high rate of hydrogen evolution experienced at such large peak current densities. Because of the large current applied, deposited layers are very thick, reaching as much as 4.7 μm after a one minute of the total T_{on} time. This makes the process too rapid and flawed to be considered beneficial in a controllable deposition for achieving exact Au:Sn composition.

To summarise, AC electroplating is a good technique allowing for modification of deposited layers morphology without the need of introducing significant plating current density changes. It solves the problem of depletion of the diffusion layer in the cathode vicinity by allowing the plating electrolyte to rebalance during the off pulse when no current is applied. That way, the hydrogen dissolution is minimised, and certain control over the grain size of produced layers is introduced. However, the whole process takes much longer because of its pulsed nature. Depending on the duty cycle applied- by as much as ten times. It was found that the parameter the adjustment of which gives the most impact on layers morphology was pulse duty cycle. However, it should be noted that this study

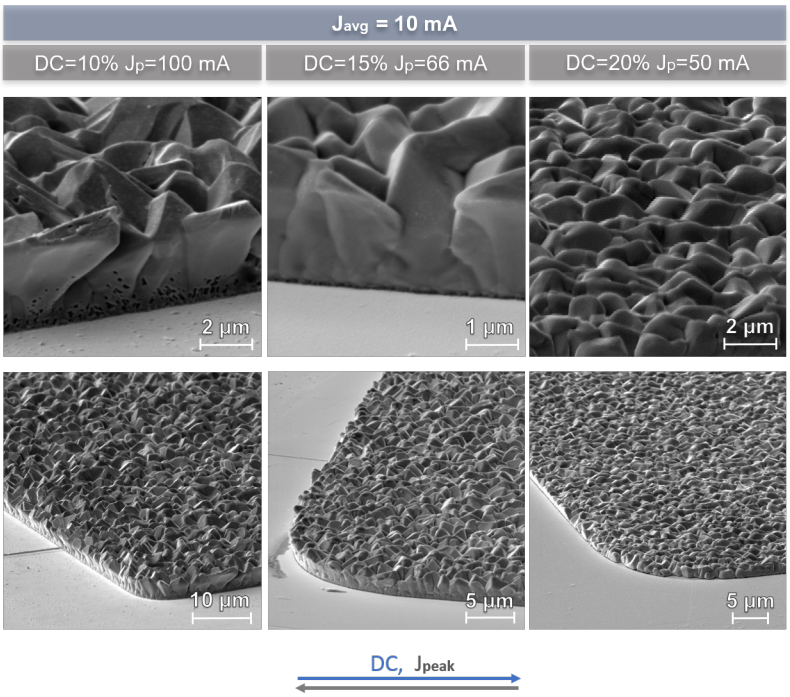


Figure 5.18.: AC tin electrodeposition: morphology of layers deposited with different pulse duty cycles and peak current densities at 10 mA average current density. All current values are shown per square centimetre area.

was limited to only a few tested parameters. In order to establish correct AC plating parameters correctly, more samples and more variations of frequencies should be tested. For the range of parameters tested and the electrolyte used in this study (methanesulfonic acid-based), results obtained by the DC plating are considered analogous to those achieved with the AC plating.

5.3.5. Au:Sn deposition by variable area electroplating

Drawing from the conclusions made after wafer- and chip-level electroplating tests, a final, mixed approach for the deposition of Au:Sn at the eutectic composition was tested.
Since good results were obtained for the gold electroplating on the wafer level, the same approach and parameters described in section 5.3.3 were applied. Whenever thicker gold layers were required, mask patterning was done twice to avoid issues with underplating and photoresist lifting. With the purpose of avoiding tin plating non-uniformities as experienced at the wafer level, tin electroplating was performed on variable areas. Scaling up sample size requires scaling up the entire setup size to avoid problems with electrolyte frothing and layers degeneration resulting from the gas building into deposited layers. Therefore, as a means to limit the total current required to reach a given current density, only selected areas of the entire wafer were patterned at the time. In the event of excessive gas evolution, plating areas were selected so that bubbles would not overshadow structures

placed above. They were typically thin, 1-2 cm strips of samples along the length of the four-inch wafer substrate.

Reflecting on the positive results of pulsed plating, but in the interest of limiting a total processing time, an intermediate approach of intermittent electroplating was applied. This was done by repeated electroplating in the chronopotentiometry mode continuously for seven seconds, after which no-current breaks lasting fourteen seconds were applied to help in an ionic replenishment of the electrolyte. Based on chip-level tests, process parameters of 150 RPM agitation rate and 15 mA/cm^2 of plating current density were applied. As a result of introduced changes, the thickness variation of the tin-plated deposits was significantly reduced. Figure 5.19 represents the histogram of thickness variations of tin deposits across a selected, plated area of the sample wafer when electroplated to the target thickness of 6 μm. In comparison to the results obtained previously during initial wafer-level tin plating tests (Figure 5.5), the deposition uniformity has significantly improved across a similar testing area. Average obtained thickness (6.06 μm) was almost as targeted, with the standard deviation of a mere 0.2. The dispersion of thicknesses achieved after small-scale setup process adaptations increases the yield of samples having composition utilisable for eutectic bonding. Analysing the final ratio of gold to tin while taking into account both gold and tin process variabilities, the average total obtained height was 14.8 μm for the

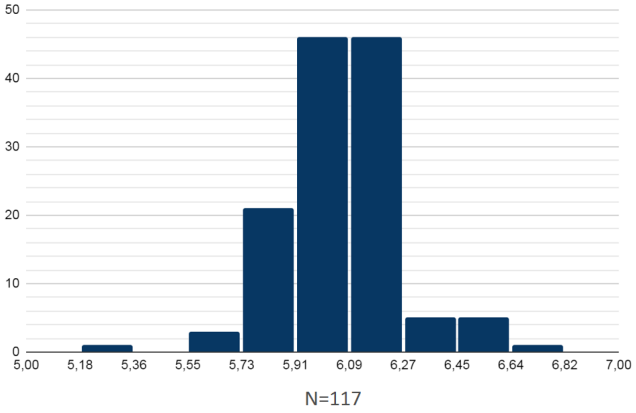
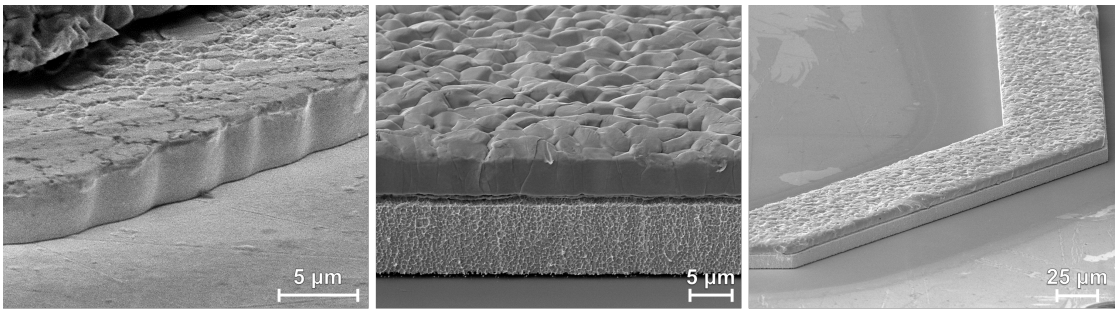


Figure 5.19.: Histogram of the deposited tin layer thickness after process adaptations.



a) Gold surface close-up b) Au (bottom), Sn (top) c) Au (bottom), Sn (top)

Figure 5.20.: Surface of gold and tin layers after process adjustments.

target height of 15 μm, while an average ratio of Au to Sn was 1.44 compared to the target of 1.50. Such a result would provide the right concentration of materials for the stack to achieve a melting point at 280° C.

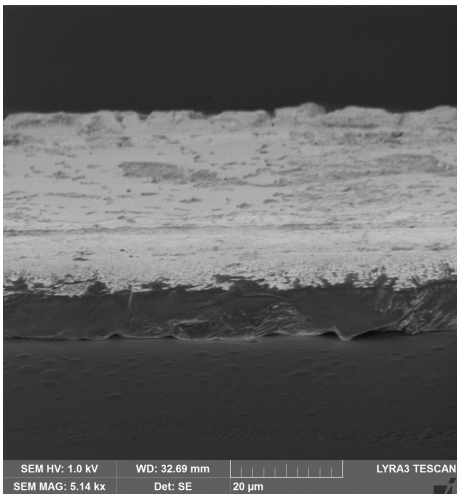


Figure 5.21.: $Au_{80}Sn_{20}$ alloy formed upon a reflow of electroplated layers at 280 ° C.

Figure 5.20 presents the morphology of gold and tin layers deposited using an approach of intermittent and variable area plating at a small scale setup. After process adjustments, it was achievable to obtain layers of surfaces smooth enough to enable the control of their thickness during the deposition, thus allowing forming the correct relation of gold to tin ratio equivalent to that needed to obtain the eutectic composition. Formed layers were of dense, compact structure and matching mechanical stresses, as no cracking nor peeling was observed. Upon reflow, a uniform alloy can be formed (Figure 5.21), thus proving that the $Au_{80}Sn_{20}$ eutectic ratio can be formed using an approach of small-scale sequential electroplating as demonstrated in this chapter.

5.4. Biocompatibility of sequentially electroplated Au:Sn layers

Both gold and tin are materials considered to have a low-toxic effect on the human body [24, 25]. Gold being a highly inert, noble metal, is widely used in various medical devices, both in a solid form and an electroplated coating. The high biocompatibility of gold has led to the use of the material in endovascular stents, dental implants, pacemakers and many others. What is more, also in micro-and nanoparticle forms, gold seems to be highly biocompatible [26, 25]. Where it comes to tin, this soft, matte metal has found its everyday use in metallurgy, the food packaging industry and in electronics, where it is used as a component in solder mixes. In medical applications, tin has been historically used in dental fillings. Whereas there have been only a few studies on the toxicology of an inorganic tin, it is generally considered a non-toxic element [24]. However, whereas a non-toxic tin behaviour is accepted for the metallic tin and some inorganic Sn-compounds, the same cannot be said for tin's stannous ions and toxic organic compounds.
Despite both gold and tin having low toxicity, their alloyed effect on the human body can differ. In the literature, only scarce information on employing Au:Sn alloy's toxicology and its uses in the medical field can be found, where it is mentioned only in the context of dental restorative materials [27, 28]. Furthermore, used electroplating chemistry could accumulate on the samples' surface and interact with the human body. To establish a preliminary validation of the biocompatibility critical for any implantable applications, the cytotoxicity of plating chemistry, as well as the alloy itself, were assessed by *in vivo* culturing of human fibroblast cells on reflown samples' surface. Evaluation of implanted material's influence on a body by utilising cell culture benefits from extremely high sensitivity of fibroblast cells to toxic agents.

Nine previously reflown, or reflown and debonded, random samples were used as substrates for the human fibroblast cell viability and cytotoxic assessment. Samples used were sectioned off wafers before dicing; therefore, they were larger, each containing several seal rings. That way, the comparison of seeded cells viability on regions with and without solder present could be performed with a higher level of certainty. Biocompatibility was assessed via an analysis of cell morphology as inspected by scanning electron microscopy. Initially, samples were sterilised by exposing them to the UV light for 20 min followed by washing with PBS three times before adding to the cell culture medium. Next, cultured human fibroblast cells were employed in cell experiments to ascertain the cytotoxicity and cellular response to the fabricated layers. The cell line used in this experiment -fibroblast cell BJ (ATCC® CRL-2522™), was purchased from ATCC and cultured in Dulbecco's modified Eagle's medium (DMEM) containing 10% heat-activated fetal bovine serum with 1% penicillin-streptomycin antibiotics (Pen-strep). Subsequently, the cells were seeded and cultured on reflown Au:Sn substrates and placed in Petri dishes with a seeding density of

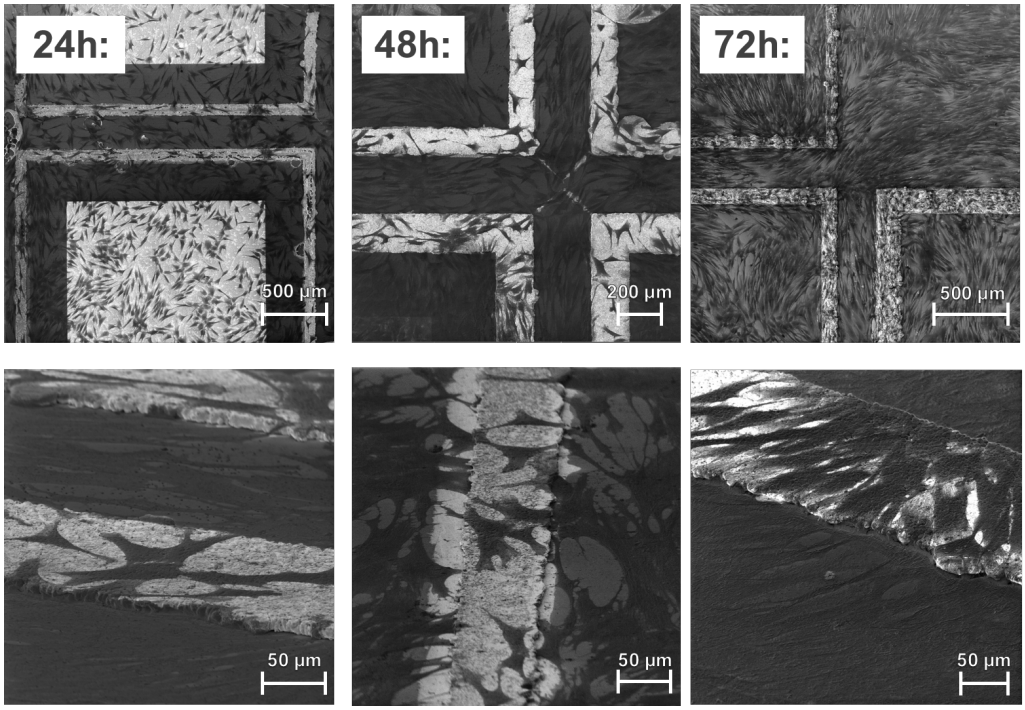


Figure 5.22.: SEM images of the reflown chip surface containing Au:Sn solder lines used for the fibroblast cell culturing after 24, 28, and 72 hours of incubation.

750,000 cells/ cm^2. The cells were incubated in the medium for 24, 48, and 72 hours at 37° C and 5% CO_2 while they were examined every 12 h.

Cell adhesion and morphology were observed by SEM on the surface of reflown Au:Sn eutectic after culturing for 1, 2, and 3 days. Representative surfaces after incubation in the cell culture medium are shown in (Figure 5.22). No cytotoxicity effect on the fibroblasts structure could be observed between time points of 1, 2 and 3 days, with cells consistently exhibiting normal, spindle-like morphology. Cell density exponentially increased over the course of an incubation time. After three days, a continued proliferation of the fibroblast has created a tissue-like structure on the surface of samples that suggest the biocompatibility and non-cytotoxicity of the substrates (Figure 5.23, right) [29, 30]. An untreated area of the samples was considered as a control. Increasing numbers of fibroblasts attached to the surface and in contact with each other were observed. The clear preference of a cellular attachment on the silicon oxide compared to the reflown Au:Sn was noted, with a sparser cellular layer covering solder lines. Nonetheless, fibroblasts present on the solder frames remained of a healthy morphology, with only a few single individual cells exhibiting round shape. After culturing for more than three days, the density of fibroblasts coverage was high enough to cover the majority of sample surfaces, proving no cytotoxic effect of sequentially electroplated Au:Sn solder. Figures 5.22 and 5.23 represent SEM images of samples surfaces after the cell culturing study. In Figure 5.23 (left), cells can be found climbing over Au:Sn solder walls in pursuit of forming connections which

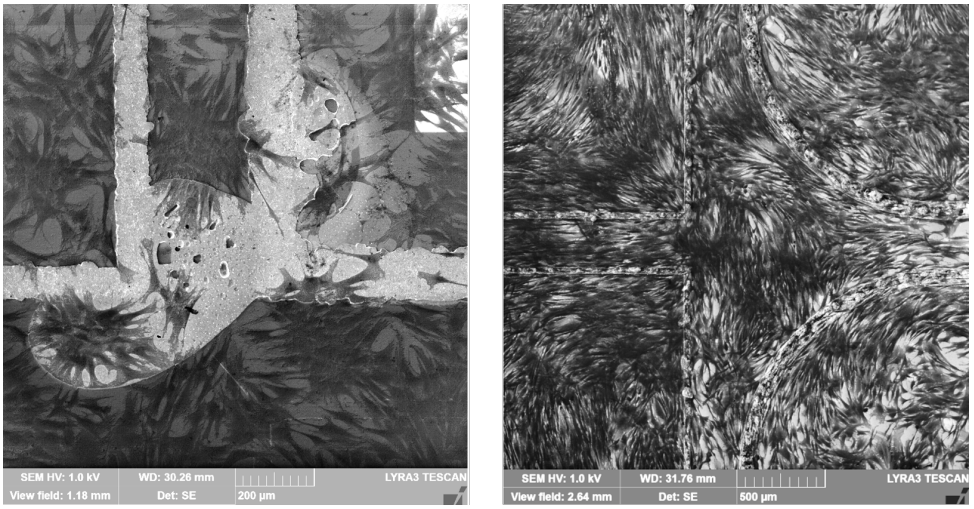


Figure 5.23.: SEM images depicting fibroblast attachment to the surface of reflown Au:Sn alloy. Dark areas represent cell structures (left) eventually forming tissue-like arrangement (right).

each other, while still displaying a spread-like morphology, indicating good health of the cell.

5.5. Conclusions

This chapter describes the study on the performance and capabilities of sequential electroplating for the deposition of the $Au_{80}\,Sn_{20}$ alloy composition. Key challenges in obtaining satisfactory layers characteristics while conducting the process in a low-hazard, low-volume manner were identified. The choices of parameters variations have been justified regarding the application of the deposited layers in implantable devices, thus keeping maximum possible biocompatibility. For that reason, the least hazardous commercially available electrolytes were employed. Keeping in mind the level of complication in ECD systems, where the process is influenced by a multitude of interdependent parameters, the focus of the study was aimed at achieving the layers of low roughness, good mechanical properties and thickness uniformity. The setup and deposition process was designed to allow for low-cost, low-volume prototyping in the laboratory rather than the industrial setting. Based on the experimental results obtained, the following conclusions are drawn:

- The use of electroplating over other methods of an alloy deposition allows for a parallel formation of multiple solder frames with a great geometry control while the choice of plating sequentially significantly reduces problems of plating solution stability and shelf life. The wide availability of a considerably low toxicity gold and tin electroplating chemistry makes the process both cost and time effective.

- Thin eutectic stacks are more challenging to obtain using sequential electroplating when precise control over the deposited composition is required. This is because the accuracy of the control over deposited thickness highly depends on the minimum achievable grain size, whereas gold and tin formed during sequential deposition from solutions without any grain-refining additives differ significantly from each other from the morphology perspective.

- Pulse electroplating on the MSA-based tin-plating electrolyte is a promising technique allowing for the regulation of deposited grain size without the need for radical current density changes. Alternations of duty cycles, along with an applied current density, are the most surface-influential parameters. However, in order to utilise the technique, better tests of MSA-based chemistry performance in a lower frequency range should be performed. That way, the effect of bath replenishment during the off pulse can be utilised better.

- Maximising the effective electroplating yield in a small-scale setup is possible by varying plated area so that the differences between plating chemistries can be accommodated, resulting in layers of compact morphology. Otherwise, a different dynamics of the tin electrolyte compared to a gold bath leads to an excessive hydrogen evolution that affects the layer uniformity. An intermittent plating approach can also reduce the effect of gas evolution on grown layers.

- Sulphite-based soft gold and methanesulfonic acid-based tin electroplating solutions without plating-moderating additives are an appropriate combination of ECD chemistries for forming Au:Sn-eutectic layers in implantable applications. Cell-culturing using highly sensitive, human fibroblast cell line over deposited and reflown samples have shown no toxic effect of the alloys deposited from the abovementioned electrolytes on the biological environment.

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6. Conclusions

Implantable technologies available in clinical applications have not changed much over the last several years. The majority of solutions rely on bulky titanium cans and wired connections. Whereas such approaches may seem enough for implantation in abdominal areas where there is enough space to utilise for large devices, placement in more confined, demanding environments such as the cranial space precludes their usability. Moreover, implants with all-metal packages do not allow for wireless links, which minimise devices invasiveness.
Nevertheless, tremendous efforts are put to employ microsystems technologies in the packaging of minimally invasive implants within the neuroscience community. MEMS techniques, widely based on substrate bonding, are well proven in the packaging of sensors aimed to operate in demanding applications. Now, this approach is being expanded in the implantable biomedical systems space so that future implants can be smaller, safer and with more capabilities enabling their faster translation into clinical space.

This research is dedicated to the aspects of implantable devices micropackaging, the improvement of which is one of the main bottlenecks in a current neurotechnology preventing it from a faster clinical adaptation. The main aim is to investigate CMOS, bio-, and RF-compatible methods for packaging and assembling the next generation of mm-sized, autonomous ENGINI neural probes.

6.1. Summary and original contributions

Below, a shortened summary of each of the thesis' chapters is provided, highlighting key achievements and original contributions. The related publications regarding each chapter can be found in the Appendix A.

Chapter 2

This chapter provides a literature review and background on the most commonly used neural interfaces, with a specific focus on intracortical devices. The benefits and challenges associated with each technology are highlighted. The background information about the nervous system and brain function is provided, next to the fundamentals of a neural activity recording. The chapter identifies obstacles on the way to the miniaturisation of neural

interfaces and introduces distributed BMIs as a way of current solutions' improvement. Finally, ENGINI's project approach to neural interfacing device development is presented.

Chapter 3

In this chapter, the challenges related to the micropackaging of neural implants from the perspective of materials selection, electrode integration and mechanical reliability are reviewed. The methodology for the implant's structural design in a view of the ENGINI project is presented. The original contributions in this chapter can be summarised as follows:

- The first generation of ENGINI's microwire-based, CMOS-integrated, the neural probe body design is made and the *proof of concept* version fabricated and pre-assembled. The body of the V1 device relies on the use of micromachined glass joined with a Si-based interposer serving as a redistribution layer, employing TSVs and surface metallisation. Microwire integration relies on in-via electroplating to establish electrical connections between substrates. This probe design was assembled fully manually, and as such, suffered repeatability, scalability, manufacturability, and assembly accuracy problems.
- The second generation of the probe body's is designed and reviewed in the light of challenges encountered during the assembly of the first generation of the probe. The architecture was redesigned by dividing the fabrication efforts into two separate entities: LTCC-based microwire and head modules. The purpose of the two-module approach is to increase the yield and minimise failed assembly risks. The concept of the microwire integration through an in-via solder spheres remelting is proposed and reviewed through assembly tests with the PCB-based microwire module mock-up.

Chapter 4

This chapter demonstrates the method for creating solid and hermetic seals using the Au:Sn alloy. The background information on wafer-scale joining techniques is presented, and the thermodynamic properties of gold-tin alloy are explained. Eutectic frames are fabricated employing standard microfabrication methods, and thanks to relatively low process temperatures, the approach can be applied to temperature-sensitive devices, such as CMOS microelectronics dies. Original contributions can be summarised as follows:

- Bonding method for chips of an mm-sized geometry is presented and evaluated by tests using varying parameters of applied temperature, reflow profile and frame geometries, proving the possibility of this method to create an enclosed, mechanically robust hermetic environment. Across all geometries and process parameters tested, the average measured bonding strength was over 28 MPa with a bonding success

yield of 73%. The proposed bonding technique is a suitable solution for the protection of sensitive elements in implantable applications or any other application where a device must be protected from an external operating environment.

- Process optimisation is carried out, pointing out the most effective parameters leading to the high percentage of strong, successful joints. It was identified that alloy deposited on the package lid only is enough to provide a hermetic environment for periods extending half a year, as proven in accelerated immersion tests in the corrosive medium.

Chapter 5

In this chapter, a method of the sequential electroplating of Au:Sn alloy is proposed and assessed with regards to its effectiveness towards achieving layers at the eutectic composition. Electrochemical deposition's physical and chemical fundamentals are introduced, and a review of alternative gold-tin alloy deposition techniques is provided. Below, the original contributions are summarised:

- A method for a low-hazard, low-volume electroplating of gold-tin alloys of a controllable composition is developed and optimised to achieve the minimum possible roughness with the best repeatability of deposited layers thickness. The use of electroplating over other deposition techniques enables the growth of multiple solder frames in parallel while maintaining great geometry control over the deposit. The sequential approach significantly reduces issues with electrolyte stability and short shelf life. The proposed method employs readily available plating solutions and does not require high maintenance of the process.

- An evaluation of gold-tin eutectic alloy cytotoxicity is carried out for the first time. Cell-culturing evaluation reveals that the layer grown from sulphite-based soft gold and methanesulfonic acid-based tin electroplating solutions without plating-moderating additives do not show toxic effects on human fibroblast cells, thus making the method suitable for use in the applications requiring interfacing with the biological environment.

6.2. Future work

Notwithstanding contributions made and the work done within this thesis, the initiated research would benefit from further developments, the directions of which are briefly summarised below.

Design and integration of microwire-based neural implants

It would be beneficial for the purpose of further improvements of the ENGINI implant prototype to explore various fixation modes of microwires to the CMOS chip and the microwire module and their impact on design reliability and hermeticity. This could include such approaches as bundling microwires and direct compression bonding onto the redistribution surfaces, different solder technologies or fixing microwires directly in the module during the co-firing process.

Micromodules' integration and reliability assessment. Different assembly approaches of a microwire-to-base module integration could be carried out. Characterisation of the hermeticity and connectivity with custom IC dies designed for the ENGINI project's purpose should be evaluated. *In vivo* characterisation of implants impact on the tissue should be then performed.

Study of the impact of different electrode leads on the ENGINI integration scheme and the LFP-recording capability. It would be beneficial to establish an integration with various microelectrode types to extend the ENGINI reconfigurability opportunities, such as thermally drawn glass fibres with metallic core. Such electrodes could be beneficial from the perspective of a minimised risk of insulation degradation and good biocompatibility characteristics.

Hermetic packaging based on sealing of eutectic frames

Wafer-level validation of the implant's packaging. For that, a significant scaling up of both electroplating and bonding setups would be required. Approaches of wafer-to-wafer and chip-to-wafer assembly techniques could be explored, followed by a statistical analysis of the reliability and packaging yield.

Exploration of different under-solder-metallisation stacks, including ALD-grown layers for the purpose of increase of the hermeticity level and minimising solder adhesive fractures.

Quantitative analysis of the hermeticity of achieved seals. This could be explored by adapting He-leak testing for extremely small cavity volumes using gas-sensitive elements, such as microresonators or Pirani gauge. Otherwise, hermeticity monitoring can be per-

formed wirelessly by integrating a humidity sensor inside a sealed cavity.

In-package wireless humidity sensor integration. This could expand the reliability of sensors by enabling wireless control of in-cavity humidity monitoring and early prevention of package failure. Wireless links could be achieved utilising either RF methods, building upon telemetry already employed within the ENGINI approach, or exploring optical communication methods.

6.3. Concluding remarks

In the final section of this work, I would like to share personal reflections on the neurotechnology that I have come to after working in this field for a few years.

For years, we have been witnesses to the pop culture's dream notions of thoughts reading, telepathy or controlling devices with only one's mind. Especially recently, after worldwide's attention has been drawn on Elon Musk's BCI company, Neuralink, the understanding of the public eye is that connecting one's brain to the internet is as close to happening as the new season of the public's favourite show. Without a doubt, having access to a fully implantable, autonomous neural interface capable of chronic performance, without harming the host tissue, would revolutionise our understanding of brain function. Nevertheless, despite multiple worldwide efforts, the BMI field is still years from making such circumstances a widely available reality. Considerations about BMIs future possibilities are captivating but often overshadow more practical issues needing attention now, such as long-term safety or reliability. The majority of currently reviewed devices are still in the early stages of conceptualisations and improvements, and as such, the problem of how to make things work long-term remains. Nonetheless, that does not mean the field does not observe progress; on the contrary, there seems to be an increasing extent of interest in neurotechnology.

The human body is an extremely demanding environment; therefore, the ultimate success of brain-machine interfacing is dependent on the combined efforts of specialists across multiple disciplines. Undoubtedly, input from professionals representing electronic and electrical engineering, neuroscience, medicine, biology, chemistry, material science, data science, computer science or production engineering is required, and their contributions should not be underestimated.

The primary root causes and stimuli exacerbating the extent of foreign body reaction in the brain must be wholly recognised so implants might be designed with a minimum negative impact on the tissue. Instead of relying on adaptations of current techniques, new materials and fabrication methods explicitly tailored for implantable applications could allow for further miniaturisation and simplify an electronics integration. Attention should be paid to cooperatively engineer novel materials and packages, manufacturing techniques, as well as integration and implantation methodologies, which could overcome prolonged stability limitations of existent neural probes. Existing materials do not have the proper set of mechanical, biological, nor electrical properties to match nervous tissue, thus creating the need for some that could offer such. Minimised implants' sizes will require establishing new means and devices enabling their safe implantation, too.

Thanks to the increasing interest in neurotechnology and brain-machine-interfacing, new promising implants design and fabrication approaches have been emerging, which could accelerate potential future breakthroughs in the field. With the use of new functional polymers, implants have been taking shapes of flexible meshes, lattices, scaffolds and stretchable nanoneedles, often enriched by incorporating anti-inflammatory agents or conductive nanoparticles. The field's preferences appear to head towards widespread use of these soft materials, combined with wireless telemetry for communication, and a multimodal integration combining standard recording approaches with opto- and chemogenetic schemes. Moreover, with rapid prototyping and additive manufacturing technologies being widely available and offering more and more accuracy, the design cycle is faster than before.

Questions of the most beneficial structural design and how to provide a fully autonomous power delivery and high bandwidth communication *in vivo* remain unanswered. One of the often-overlooked design areas is implant's packaging, where most solutions rely on adapting materials and packaging schemes from MEMS devices and CMOS stacking technologies. Limits of current microfabrication and integration methods lead to problems with further scaling down of implants devices, as interconnects are typically much larger than the core of the device themselves. Because of that, centralised, multi-electrode implants have become the dominant type of intracortical interfaces thus far. Studies on the potential influence of manufacturing methods on the final material and implant biocompatibility could simplify our design approaches. It is not fully acknowledged if numerous chemicals to which devices are exposed during fabrication do not leave toxic remains or alter materials biostability. On the same note, a thorough assessment of the degradation mechanisms of various hybrid, composite and compound materials widely used in IMDs should be performed.

From the biology perspective, testing passive electrodes in small animal models may not be translatable to the behaviour of active devices implanted in a much larger human brain. Finally, the variety of surgical methods used causes a clear comparison between devices' performance blurred. This is particularly true for short-term *in vivo* studies as the majority of general anaesthetics are found to decrease neuronal firing rates as far as a few days after the implantation, depending on an animal. Furthermore, it is most likely that most of the abovementioned issues and mechanisms are co-dependent on each other. That makes the BMI development a field that not only benefits from a multi-faceted interdisciplinary approach, but in fact, it requires it.

ENGINI project is one of the examples of distributed approaches to neural interfacing hardware, which in recent times has emerged within the neurotechnology community. As an alternative to single, highly advanced implants containing hundreds of recording channels, the focus is shifted to developing hundreds of smaller, simple devices of merely a

few recording points building a scattered BMI network. Whereas the devices are comparatively more straightforward, distributed BMIs must follow the same constraints of implantable devices such as high functionality, reliability and stability, with a necessary addition of wireless telemetry. Designing such a device is a game of compromises between engineers working on it. Combining multiple functionalities, various materials, and several novel methodologies in the design of one device, which is aimed to work in one of the most demanding of environments, can lead to a general over-complication. Often, the device's parameters most suitable in one aspect preclude the possibility of other functionality to take place. It is of the greatest challenge to decide on the validity of each design aspect and further redesign the device accordingly to the order of importance. In this process, the issues of long-term reliability testing, safety, and packaging are often left to the very end, with a hope that standard methodologies will work out for the otherwise very specific, custom designs.

Before smart, distributed BMIs are widely available, much research is still required to ensure a sufficient level of implant's safety and high performance. Foremost, thorough studies of a chronic neuronal tissue response should be conducted on cellular and extra-cellular levels to recognise the impact of a tissue reaction on electrode performances. Being considered devices of the highest risk to the prospective patients, implantable neural devices will also require a thorough control from the efficacy, safety and quality perspectives before they can obtain validation from regulatory bodies. As the regulatory procedures can take years to finalise, the need for necessary experiments and documentation, under quality-management systems, should not be trivialised but instead taken into account early on in the design process. There should be close cooperation between engineers and neuroscientists to identify design aspects that, when adjusted, would boost devices' performance in specific brain regions. Only then neural interfaces will be seen as the long-missing element in the repertoire of neuroscience hardware.

A. Publications

The following parts of this thesis include work previously published as research papers.

Chapter 2 includes content from:

- K. M. Szostak, P. Feng, F. Mazza, and T. G. Constandinou. "Distributed neural interfaces: challlenges and trends in scaling implantable technology", in: N.V.Thakor *Handbook of Neuroengineering*, Springer Singapore, p. 1-37, 2021.

- K. M. Szostak, L. Grand, and T. G. Constandinou, "Neural interfaces for intracortical recording: Requirements, fabrication methods, and characteristics," *Frontiers in Neuroscience*, vol. 11, p. 665, 2017.

Chapter 3 includes content from:

- K. M. Szostak, F. Mazza, M. Maslik, L. B. Leene, P. Feng, and T. G. Constandinou. "Microwire-CMOS integration of mm-scale neural probes for chronic local field potential recording". *2017 IEEE Biomedical Circuits and Systems Conference (BioCAS)*

- N. Ahmadi, M. L. Cavuto, P. Feng, L. B. Leene, M. Maslik, F. Mazza, O. Savolainen, K. M. Szostak, and others. "Towards a distributed, chronically-implantable neural interface". *2019 9th International IEEE/EMBS Conference on Neural Engineering (NER)*, p. 719-724, 2019.

Chapters 4 and 5 include content from:

- K. M. Szostak, M. Keshavarz, and T. G. Constandinou, "Hermetic chip-scale packaging using Au:Sn eutectic bonding for implantable devices," *Journal of Micromechanics and Microengineering*, vol. 31, p. 1-13, 2021.

- K. M. Szostak and T. G. Constandinou, "Hermetic packaging for implantable microsystems: Effectiveness of sequentially electroplated Au:Sn alloy," *2018 40th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC)*, pp. 3849–3853, IEEE, 2018.