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Thermoelectric Effects in Silicon Nanowires

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November 2013

A thesis submitted to Imperial College London for the degree of

Doctor of Philosophy

Declaration

I state that the research undertaken with this thesis is the original work of the author except where explicitly stated and referenced.

Emiljana Krali

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To my parents Domenico and Zhaneta, my brother Cosimo and my grandmother Matilda. Your support and encouragement have always been my very main strength.

Abstract

The increasing demand for fossil fuels, and the need to reduce greenhouse gases, requires 'clean' energy sources and more efficient utilisation of energy. Thermoelectric (TE) materials provide a means towards achieving these objectives, as they convert a temperature difference ΔT directly into an electric potential difference ΔV. For practical applications, a TE material is chosen only if the dimensionless figure-of-merit $ZT = S^2\sigma T/\kappa \sim 1$. Where $S = \Delta V/\Delta T$, σ and κ are the Seebeck coefficient, electrical and thermal conductivity, respectively, at temperature T. Conventional bulk TE materials, such as Bi_2Te_3, require a compromise between S, σ and κ. In nano-structured materials, these parameters may be varied quasi-independently, suggesting a new approach to obtain high values of ZT.

In this thesis, silicon nanowire (SiNW) arrays were fabricated using a metal-assisted chemical etching process, creating SiNWs from 30 to 400 nm in diameter, a maximum length of 350 μm and aspect ratio up to 3000. A novel transient measurement method was used to characterise the temperature dependence of S in two different n-type doped SiNW arrays, $\sim 10^{15}$ cm^{-3} and $\sim 10^{18}$ cm^{-3}. In the lightly doped 35 μm long SiNWs, $S = 1850$ μV/K at 300 K, an increase by a factor of 2.5 compared to its parent bulk Si (S_{Bulk}). Furthermore, the phonon drag component, a manifestation of electron-phonon scattering in the sample, is heavily suppressed due to surface scattering. In the moderately doped 30 μm long SiNW array, $S = 1480$ μV/K $= 2.5S_{Bulk}$ at 300 K. An increase in S was also observed in the n- and p-SiNWs measurements in ambient conditions. A transient method was used to characterise the temperature dependence of κ in the range 300 – 30 K. At 300 K, $\kappa = 23$ W/mK $= 0.19\kappa_{Bulk}$. Finally, the I-V characteristics of the SiNW arrays were measured and only a limited change was observed from bulk Si. Assuming σ is unchanged, in the 30 μm long SiNWs, $0.0255 \leq ZT_{NW} \leq 0.34$. This corresponds to an increase in ZT from 32 to 55 times than the bulk Si value.

Publications

Journal

1. Krali, Emiljana and Durrani, Zahid A. K., 'Seebeck coefficient in silicon nanowire arrays', Appl. Phys. Lett 102 (2013), pp. 143102-1 – 143102-2.

2. C. Li, E. Krali, K. Fobelets, B. Cheng, and Q. Wang, 'Conductance modulation of Si nanowire arrays', Appl. Phys. Lett. 101(22) (2012) 222101-1 – 222101-2

3. Rasool, K., Rafiq, M.A., Li, C. B., Krali, E., Durrani, Z. A. K. and Hasan, M. M., 'Enhanced electrical and dielectric properties of polymer covered silicon nanowire arrays', Appl. Phys. Lett 101 (2012), pp. 023114-1 – 023114-4.

Conference

1. Emiljana Krali, Chuanbo Li, Kristel Fobelets, Z. A. K. Durrani 'Seebeck coefficient in silicon nanowire arrays' 38th International Conference on Micro and Nano Engineering, London, United Kingdom 16-19 September 2013.

2. Emiljana Krali, Chuanbo Li, Kristel Fobelets, Z. A. K. Durrani 'Seebeck coefficient in silicon nanowire arrays' Japan Society for the Promotion of science, Japan, 4 February 2013.

3. Emiljana Krali, Chuanbo Li, Kristel Fobelets, Z. A. K. Durrani 'Seebeck coefficient in silicon nanowire arrays' 38th International Conference on Micro and Nano Engineering, Toulouse, France 16-20 September 2012.

4. Emiljana Krali, Chuanbo Li, Kristel Fobelets, Zahid A. K. Durrani 'Seebeck Coefficients in Silicon Nanowire Arrays' 9th European Conference on Thermoelectrics, Thessaloniki, Greece 28-30 September 2011.

Acknowledgments

I would like to express my deepest gratitude to my supervisor Dr. Zahid Durrani for his help and support throughout these years, and in writing this thesis.

My sincere thanks also go to Dr. Kristel Fobelets for her great support and inspiration during my PhD, and for all the squash games played together.

Thanks to Prof. Mino Green for his enthusiasm and advice. During my time spent in the lab, Dr. Chuanbo Li, Valerie Stevens, Dr. Munir Ahmad, Tom Tate and Amine Halimi have been of great help, and offered answers to my questions.

Thanks to Phil for having prepared all of my measurement apparatuses, and assistance whenever they would break down. He has set himself apart by introducing me to squash, that I enjoy very much! Thanks to Aifric for all the inspiring coffee breaks and theatre time spent together. Thanks to my colleagues Alexey, Bob, Chen, Ed, Hadri, Hisham, Kai, Kaushal, Manuel, Mario, Pit, Taz, Timmy, Tzern, Werner and Will for the patience demonstrated with my very loud experiments and for the great time spent together.

Thanks to Lara and Brian for their proof reading. A special thank you goes to my partner Diego for his encouragement, great guidance and believing in me in these years. You have been a great example to me.

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1 Literature Survey

1.1 Introduction

The limited availability and increasing global demand for fossil fuels, as well as the urgency to find alternative energy sources without negative environmental impact, have recently led to great interest in thermoelectric (TE) materials.

TE materials convert a temperature difference directly into an electric potential difference and viceversa. Hence, TE devices can be used for scavenging of waste heat in mechanical and electrical systems, providing an additional means to enhance overall system efficiency. Furthermore, they are of interest in cooling applications, since they do not emit greenhouse gases, have no moving parts, noise or vibration.

Typically, a TE device or generator (TEG) is composed of several pairs of alternating p- and n-type semiconductors blocks (generator legs or thermocouples), which are connected thermally in parallel and electrically in series [1, 2, 3]. The number of p-n pairs can range between 7 and 254, depending on the required dimensions [4]. Figure 1.1 shows a schematic diagram of a TE device that can work in two different configurations. If heat is applied at the top through a heat reservoir, while maintaining the bottom part or heat sink cold, this will cause charge carriers, holes (h^+) in the p-type material and electrons (e^-) in the n-type, to flow from top to bottom. An electrical current is generated as a consequence of the flow of charge carriers. However, if current is applied through the external electrical connections in the TE device, then the device will work as a cooler.

TE devices are employed in a large number of fields, e.g. in military, aerospace, instrumentation, biology, medicine, industrial and commercial applications [5, 6, 7, 8, 9]. The wide variety of applications can be divided into four main categories, each of them is described briefly in the following paragraphs.

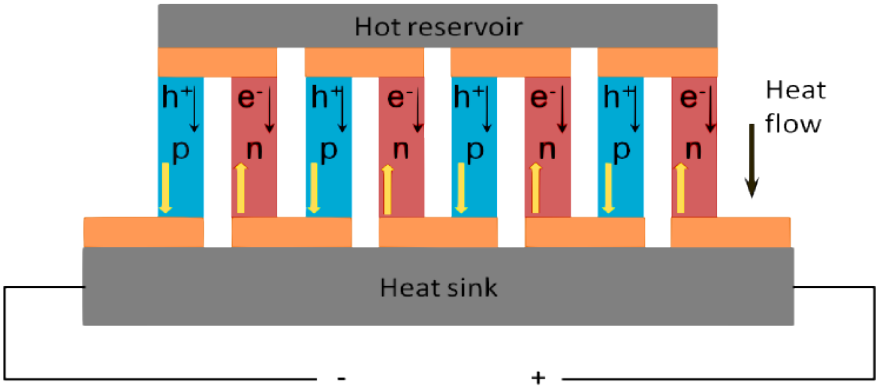


Figure 1.1: Thermoelectric device composed of alternating p- and n-type semiconductor legs, that are connected thermally in parallel and electrically in series. The black arrows represent the direction of the movement of charge carriers. The yellow arrows indicate the direction of current. Electrons are indicated by the symbol e^-, and holes by h^+ [1].

1.2 Thermoelectric applications

1.2.1 Radioisotope Thermoelectric Generators

A radioactive thermoelectric generator (RTG) exploits the nuclear decay of a radioactive isotope, generally plutonium 238, as its heat reservoir. The heat released in the nuclear decay is converted into electrical energy through TE converters, that are attached to the heat reservoir. This process has been successfully exploited by NASA in deep space and long life missions to supply power to different spacecrafts [10]. Some examples of missions where RTGs have been adopted are: the Apollo Lunar mission, the Viking Mars landers, Voyager, Ulysses, Galileo, Cassini, etc. A full list of the missions and description of the various technologies operated in each of them is given by Bennett [11].

The materials used in TE devices by NASA are alloys of lead telluride (PbTe), silicon germanium (SiGe), and a composite of tellurides of antimony, germanium, and silver (TAGS). Lead telluride alloys were the first to be used by NASA in missions such as SNAP-3A, SNAP-9A, SNAP-19, Transit-RTG, etc. Here, SNAP refers to "systems for nuclear auxiliary power". The later RTGs used SiGe generators because of higher operating temperatures than PbTe. Here, SiGe can operate at temperatures between 1275 K and 575 K, while PbTe has a range of 823 – 483 K. In addition, TEGs based on SiGe work without utilising a cover gas for vacuum operation, while this is necessary for PbTe-based generators. Here, a cover gas of argon and helium is used to avoid or minimise sublimation

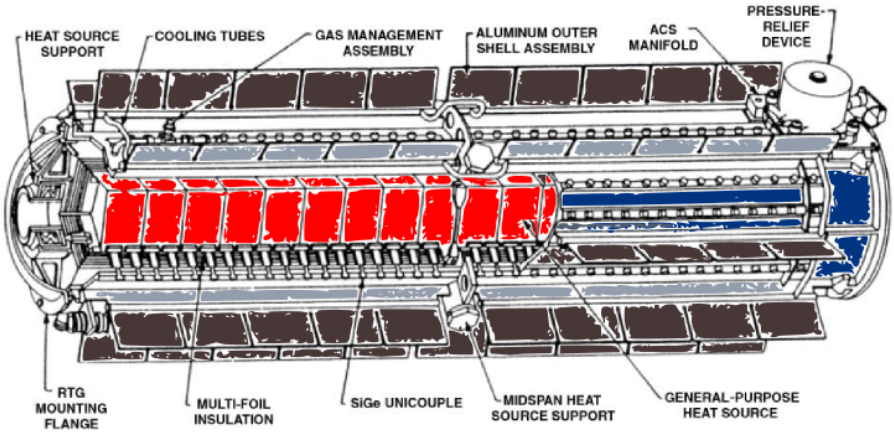


Figure 1.2: Configuration of a GPHS-RTG with silicon germanium thermoelectric elements. This RTG was included in the Galileo and Ulysses spacecrafts, launched on 1989 and 1990, to investigate Jupiter. Figure adopted from Ref. [10].

of the TE materials. Other problems of PbTe are related to the high temperature instability of p-PbTe and to the susceptibility to poisoning during processing and operation. TAGS composites were then used as an alternative to p-type PbTe [12]. Figure 1.2 shows a general purpose heat source radioisotope thermoelectric generator (GPHS-RTG) based on SiGe that is currently employed in space applications. This type of device was used on Galileo and Cassini spacecrafts to explore Jupiter and Saturn. The average RTG mass shown in Fig. 1.2 is 55.9 kg, with a length of 114 cm, fin span of 42.2 cm, and a capability of producing power of 300 Watt electrical (We).

1.2.2 Waste heat recovery for low and high power generation

Applications for automotive industry

Fuel energy is the source of automobile mobility. However, not all of the energy used in the combustion of the gasoline is consumed for the mobility of the automobile. There are different parasitic losses where energy is wasted as heat to the environment. Figure 1.3 illustrates the energy path in a gasoline-fueled vehicle. Once the combustion of gasoline occurs, 40% of it is released to the exhaust gas system, 30% is lost in the coolant, and 5% accounts of friction and air drag. The remaining 25% of the overall energy is used toward mobility.

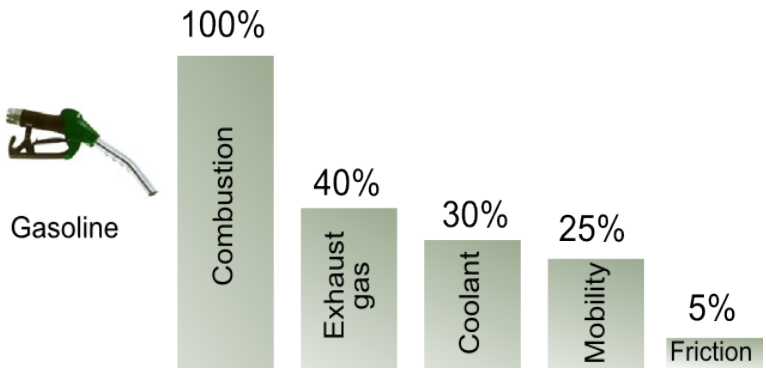


Figure 1.3: Losses in the combustion of a gasoline-fueled vehicle. Adapted from Ref. [10].

The automotive industry is exploring the integration of TE devices in the exhaust system of automobiles to convert part of this waste heat into electrical power, partially eliminating the mechanical load of the electric generator on the engine, improving vehicles fuel efficiency [13]. Up to now, conversion of car waste heat has been included in luxury cars, such as BMW, Porsche and Nissan. Figure 1.4 illustrates a simplified diagram of a TEG integrated in the exhaust gas of an automobile. Here, the TEG is coupled in between the hot side of the exhaust gas and the cold side of the coolant or air. The produced electrical energy is used to power the air conditioner within the vehicle.

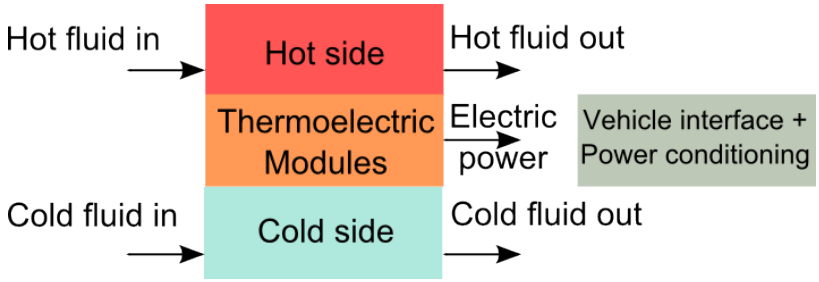


Figure 1.4: Schematic diagram of a TEG coupled to the exhaust gas of a gasoline-fueled vehicle [13]. The hot fluid represents the heat released to the exhaust system.

Applications in power plants

Power plants use steam turbine generators to produce energy. They have a conversion efficiency of 33%, the rest is released as waste heat. Therefore, utilisation of TE modules in a power plant would allow a higher conversion efficiency. In Japan, TE modules have been employed to build a 500 kW thermoelectric system for waste heat recovery in a pressurised

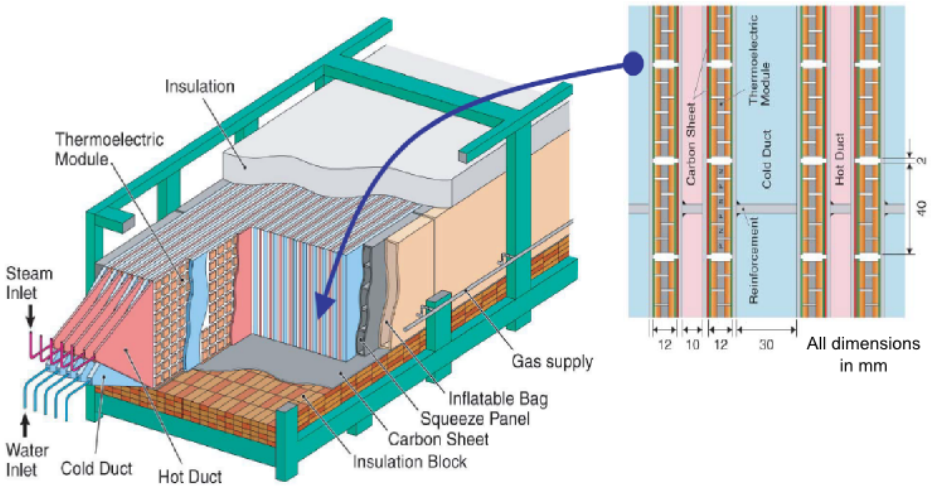


Figure 1.5: Thermoelectric system employed in a PWR power plant in Japan. Figure taken from Ref. [14].

water reactor (PWR) power plant [14]. Here, the TE modules are coupled in between the hot ducts, with operating temperature of approximately 220 °C, and the cold ducts, where water flows at a temperature of 20 °C. Figure 1.5 illustrates the TEG system used in the 500 kW power plant system. The TE modules are brazed at the cold side, while a carbon sheet is used in between the hot ducts and the TE modules to allow thermal expansion.

1.2.3 Cooling applications

As mentioned in the beginning of this chapter, TE devices can operate as a heater as well as a cooler. This cooling process is based on the Peltier effect (to be explained later) and has been used in different applications such as air conditioning, lasers, infrared detectors, etc.

In the 1980s, Stockholm reported the installation of a thermoelectric air conditioning in a train carriage of the French railways [15]. Here, a temperature controller would monitor the functioning of the thermoelectric units. When the temperature in the carriage would fall below 22 °C, the thermoelectric units would work as a heater, with air coming partly from the outside of the carriage and partly from the inside. The air would go cross-wise through the unit while being heated. If the temperature would rise above 22 °C, then the air would be cooled in a similar way.

Nowadays, TE coolers are used in applications where reliability and scalability are very important. Some of these applications are laser and infrared detectors.

In laser modules, Peltier coolers guarantee a stable operating temperature. This ensures that the optical output power of the laser does not change even when there is fluctuation in the outside temperature. Furthermore, an accurate control of the temperature is fundamental for lasers where emission wavelength is critical [16, 17].

In a similar way to lasers, solid state infrared (IR) detectors, in near- and mid-IR wavelengths, use TE modules to guarantee stable performance of the detectors [18].

1.2.4 Solar thermoelectrics

The Sun irradiates the Earth's atmosphere with an immense amount of energy, on average 174 petawatt (PW). Approximately 120 PW reaches the Earth, with 30% of this energy being lost because of scattering and optical absorption through the atmosphere [8, 19]. The solar energy is partially exploited by technologies such as photovoltaics (PV) or solar cells and concentrated solar powers (CSP).

A PV cell is composed of *p*- and *n*- type semiconductor materials that form a junction. When light strikes the cell, photon absorption leads to the formation of an electron-hole pair that is separated at the junction, and then collected through metal contacts. This results in the generation of charge carriers. Generally, the conversion efficiency in case of pure crystalline silicon cells is 25%, while cheaper alternative such as amorphous silicon and dye sensitized cells are within 10% efficiency [20].

A CSP system is based on a series of mirror or lenses (collectors) used to concentrate a large area of sunlight onto a small area. These collectors transform solar radiation into the internal energy or heat of a transport medium (air, water or oil). Heat engines are then used to produce electrical power. This type of technology works only with direct sunlight and in countries where there is lot of sunshine. On average, CSPs have an efficiency of 20%, but efficiencies up to 30% can be achieved in the best systems [8].

In a PV cell, the portion of light that is used for conversion energy is in the ultraviolet and visible portion. This accounts of 58% of the energy, with the remaining 42% of the infrared portion being wasted as heat. This heat causes deterioration of the efficiency and the longevity of a solar panel. The wavelength dependence of the solar spectrum is shown in Fig. 1.6(a). A solution for the waste heat is possible by considering a hybrid between PV and CSP cells. Here, a concentrated solar beam is split in two parts, one consisting of the visible portion and the other one of the higher-energy part. The first part is used for

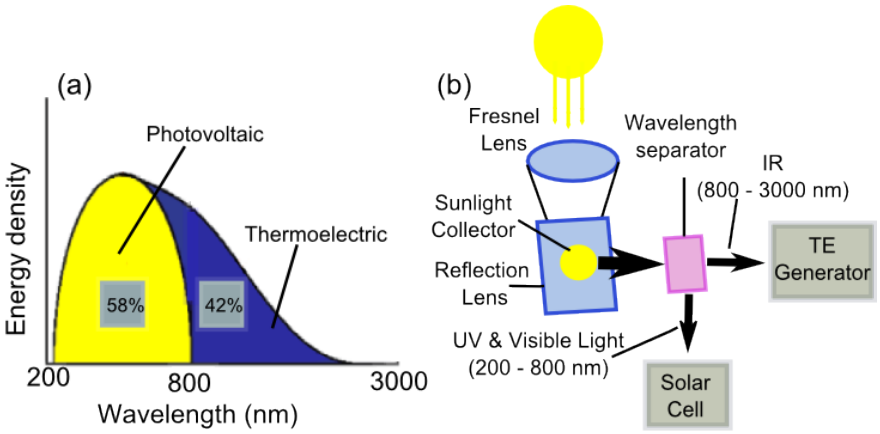


Figure 1.6: (a) Solar energy density as a function of wavelength. Photovoltaics works in the ultra-violet to visible wavelengths, while thermoelectrics works in the infrared spectrum. (b) A schematic diagram illustrating the process of the separation of the light through a mirror or lens [21].

the photovoltaic conversion, while the infrared portion is used for TE devices, to convert heat into electricity [8, 22, 23, 24]. Fig. 1.6(b) shows schematically the process of the light separation into visible and infrared. Coupling of the IR to a TE device results in the production of electrical current as a consequence of a temperature difference. This hybrid device has been already used in China to provide electrical energy to the remote parts of Mongolia [23].

1.3 State of the art in thermoelectricity

Thermoelectric effects were first observed and studied almost two centuries ago. An understanding from a macroscopic point of view dates from the decades 1820 – 1850. At the time, these effects were studied only in metals. After a century, in the early 1950s, A. Ioffe proposed semiconductors instead of metals as a promising thermoelectric material [25]. Intensive research followed in the decades 1950 and 1960, where the main purpose was the establishment of good TE materials for cooling applications. At this time, Goldsmid and Douglas discovered Bi_2Te_3, the best TE material up to now [26]. Although a lot of progress was then made and various applications launched, the high cost of the raw materials and a low efficiency, $<5\%$, limited its use only to niche applications. The decades that followed the 1960s had only consisted in a limited research in this field. However, in the 1990s, Hicks and Dresselhaus carried out theoretical work that predicted a significant increase in

the efficiency of the TE materials when nanoscale dimension was approached [27, 28]. This has lead to intense experimental work in order to demonstrate proof-of-principle nanoscale TE devices.

1.4 Thermoelectric figure-of-merit

A TE material is selected primarily on the dimensionless figure-of-merit ZT given by:

$$ZT = \frac{S^2 \sigma T}{\kappa} = \frac{S^2 T}{\rho \kappa} \tag{1.1}$$

where S is the Seebeck coefficient (measured in VK^{-1}), σ the electrical conductivity ($\Omega^{-1}\mathrm{m}^{-1}$ or Sm^{-1}), T the absolute temperature (K), κ the total thermal conductivity ($\mathrm{Wm}^{-1}\mathrm{K}$), and ρ the electrical resistivity (Ωm). Furthermore, κ can be expressed as $\kappa = \kappa_e + \kappa_L$, with κ_e and κ_L representing electron and lattice contributions, respectively [29]. The contribution of ZT to the overall efficiency η in a TE device is given by [30, 31]:

$$\eta = \eta_C \frac{\sqrt{1+ZT}-1}{\sqrt{1+ZT}+T_C/T_H} \tag{1.2}$$

where η_C is the thermodynamic efficiency of a reversible Carnot cycle operating between temperatures T_H, the temperature of the hot side, and T_C the temperature of the cold side. $T = (T_H + T_C)/2$ is the average temperature. In the case of power generation, η_C is given by $\eta_C = (T_H - T_C)/T_H$ and in the case of cooling applications $\eta_C = T_C/(T_H - T_C)$.

Optimisation of the efficiency requires maximisation of the ZT factor, since η_C is only dependent on the operating temperatures of the cycle. Maximisation of ZT, see Eq. 1.1, implies large S and σ, accompanied by a low thermal conductivity. This determines the ideal characteristics of a good TE material. Fig. 1.7(a)-(b) show S, σ, $S^2\sigma$, also known as the power factor, and κ as a function of the logarithm of the carrier concentration n in insulators, semiconductors and metals [32, 33]. Electrical and thermal conductivity have a broadly similar trend, *i.e.* they increase as the charge carrier concentration increases, whereas S behaves in a completely opposite way, increasing with decreasing carrier concentration. Typical values of S, σ and κ for insulators, metals and semiconductors are reported in Tab. 1.1.

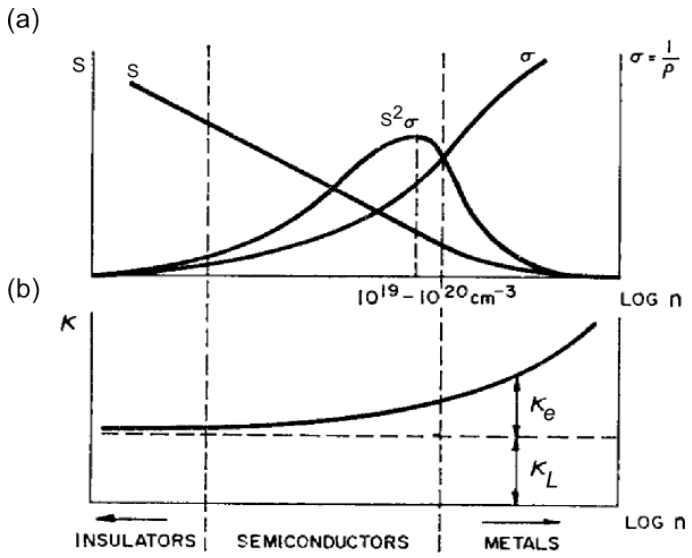


Figure 1.7: (a) S, σ, the power factor $S^2\sigma$ and (b) κ vs. the logarithmic concentration of charge carriers. (b) κ in insulators, semiconductors and metals. Contributions κ_e and κ_L are also shown. Figure taken from Ref. [32].

In addition, Tab. 1.1 shows the calculated ZT and the part of κ, that is predominant in the material. From Tab. 1.1, it is possible to see that insulators are the material with the largest S and the lowest κ, but they manifest a very small carrier concentration. This gives a ZT of almost zero (10^{-14}). Metals show the highest number of charge carriers available for transport, but also a high κ, and a very small S, making them also unsuitable as thermoelectric candidates.

	Insulators	Semiconductors	Metals
S	1000 μV/K	200 μV/K	5 μV/K
σ	10^{-10} Sm^{-1}	10^{5} Sm^{-1}	10^{8} Sm^{-1}
$\kappa = \kappa_e + \kappa_L$	$\kappa_e \ll \kappa_L = \kappa$	$\kappa_e < \kappa_L$	$\kappa_L \ll \kappa_e = \kappa$
κ	0.1 – 1 Wm^{-1}K^{-1}	1 – 100 Wm^{-1}K^{-1}	10 – 1000 Wm^{-1}K^{-1}
ZT	10^{-14}	0.1 – 1	10^{-3}

Table 1.1: Typical S, σ, κ and ZT values for insulators, semiconductors and metals. It is also indicated which of the thermal conductivity contributions is dominant in the materials [34].

On the other hand, semiconductors manifest a large Seebeck coefficient, of the order of several hundreds of μV/K, and their charge carrier concentration can be modified by the doping level. It is then possible to choose a doping level where σ is high, but S is not significantly reduced, leading to a high value of $S^2\sigma$. Fig. 1.7(a), shows the maximum of the power factor $S^2\sigma$ corresponding to a high doping level of 10^{19} – 10^{20} cm^{-3}. This leads to a tunable ZT, with values ranging from 0.1 to a maximum of 1. This implies that semiconductors are the most promising materials for TE applications.

1.5 Bulk semiconductor alloys

Up to now, TE applications are based on three semiconductor compound families: (1) the V-VI compounds based mainly on Bi_2Te_3, which are used for applications around the room temperature range; (2) the IV-VI compounds based on PbTe, used in an intermediate temperature range and (3) IV-IV compounds based on SiGe alloys, used for applications at very high temperature, e.g. RTGs [35]. Table 1.2 shows typical ZT values of the best semiconductor alloys families at 300 K. Silicon and germanium values are reported as a comparison. Bi_2Te_3 is the material with the highest $ZT = 0.66$ for p-type and 0.78 for n-type elements. If a composition of Bi_2Se_3 is added, this can lead to a maximum $ZT = 0.9$ for n-type. The temperature dependence of ZT for the above families is shown in Fig. 1.8. Bi_2Te_3 has a peak value of ZT of $\sim$0.9 at 400 K, while SiGe has a similar ZT value at 1200 K.

Material	*ZT*	*Reference*
Si	0.01	[36]
Positive elements:		
ZnSb	0.3	[37]
PbTe	$<$0.36	[37]
PbSe	$<$0.36	[37]
Sb_2Te_3	0.36	[37]
Bi_2Te_3	0.54	[37]
Ge (thin film)	$1{\cdot}10^{-3}$	[38]
Bi_2Te_3	0.66	[39]
Bi_2Te_3 - 25% Bi_2Se_3	0.81	[39]
Bi_2Te_3 - 10% Bi_2Se_3	0.84	[39]
Negative elements:		
PbTe	0.45	[37]
Bi_2Te_3	0.69	[37]
Ge (thin film)	$2{\cdot}10^{-4}$	[38]
Bi_2Te_3	0.78	[39]
Bi_2Te_3 - 25% Bi_2Se_3	0.81	[39]
Bi_2Te_3 - 50% Bi_2Se_3	0.84	[39]
Bi_2Te_3 - 74% Bi_2Se_3	0.9	[39]

Table 1.2: ZT of main semiconductor compound families at 300 K. Silicon and germanium are included as a comparison [40]. References are given in the last column.

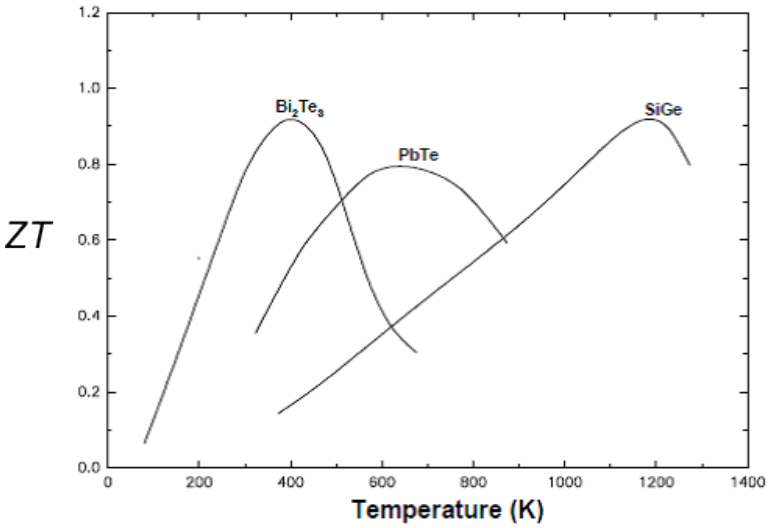


Figure 1.8: ZT of the three n-type TE families dominating since 1990. Figure taken from Ref. [41].

Bismuth telluride

Bi_2Te_3 is the best compound semiconductor for thermoelectric applications. It is a narrow band gap semiconductor, with a band gap of 0.13 eV at 293 K, and has a six valley band structure. The dimensions of the unit cells are $a = 4.4$ Å and $c = 30.5$ Å. The layers along the c-axis form the sequence

– $Te^{[1]}$ – Bi – $Te^{[2]}$ – Bi – $Te^{[1]}$–

and this sequence is repeated up to the crystal boundary. Here, 1 and 2 refer to the single and double bond. Bi and Te layers share a strong ionic-covalent bond, while there are no electrons that connect the adjacent Te layers. A van der Waals force is responsible for the weak binding between adjacent Te layers [42, 43]. This accounts for the ease of cleavage along the plane perpendicular to the c-axis, and for the anisotropic electronic and thermal transport properties. Undoped Bi_2Te_3 is p-type, with $S = 230$ μV/K. If an acceptor impurity is added, such as Pb, S falls and the electrical conductivity rises. On the other hand, if a donor impurity is added, such as iodine, S rises to a maximum of 260 μV/K to then fall to zero and changes sign, reaching a minimum value of -270 μV/K [42]. It is interesting to note that κ is very low, with $\kappa = 1.5$ $Wm^{-1}K^{-1}$ along the plane perpendicular to the c-axis and a value of 0.7 $Wm^{-1}K^{-1}$ along the c-axis direction.

Lead telluride

PbTe is also a narrow band gap material, 0.30 eV at 300 K. It has a melting point of 923 °C, while in Bi_2Te_3 this is 585 °C. Its crystal structure is a cubic sodium chloride type, and the thermoelectric properties are independent of crystal orientation. Suitable doping can lead to a maximum $S = 300$ μV/K [44]. The materials used as dopants are alkali metals, working as acceptors, and halogens acting as donors. It is possible to obtain alloys by substituting sulfur or selenium for tellurium or tin for lead. The ZT value of PbTe is ∼0.3 at room temperature, see Tab. 1.2. However, at temperatures above 600 K, it increases to a maximum of 0.8, as shown in Fig. 1.8.

Silicon germanium

Neither Si nor Ge are good TE materials, as it can be seen from Tab 1.2. Although, they have high electrical conductivity, they also manifest a high thermal conductivity, 113 and 63 $Wm^{-1}K^{-1}$ at 300 K for silicon and germanium, respectively [44]. This leads to a

low ZT. SiGe have a melting point temperature that lies in between that of Si, 1693 K, and Ge, 1231 K. In a similar way, the band gap varies in between that of Si, 1.15 eV, and Ge, 0.65 eV [44]. A good composition for TE applications is given by $Si_{0.7}Ge_{0.3}$, with $\kappa = 10$ $Wm^{-1}K^{-1}$ and a ZT that varies in between 0.3 at 500 K to $\sim$1 at 1200 K, see Fig. 1.8.

1.6 Routes to higher ZT

1.6.1 Two new directions

Although, the bulk alloy families described above have a good ZT, in order to extend the use of TE materials to commercial applications a higher ZT is required. A TE device with a $ZT = 1$ operates at 10% of η_C, while a conventional refrigerator operates at 30% of η_C. Therefore, to be competitive for commercial applications a ZT at least greater than 2 is required [3, 45].

Another problem lies in Bi_2Te_3, the best TE material for room temperature applications. Tellurium, similar to platinum, is one of the rarest element, with an abundance of 1 μg/Kg and it is very expensive [46, 47]. Therefore, an extended utilisation of TE devices should rely on a material that is abundant and cheap and also has a high ZT. For these reasons, research up to now has focused on different approaches that can lead to the discovery of new materials or methods that contribute to a substantive increase in ZT. The wide variety of materials that are being investigated can be grouped into the following two categories:

- New families of advanced bulk thermoelectric materials [48, 49, 50, 51];
- Low-dimensional material systems [52, 53, 54].

1.6.2 Developments in bulk thermoelectric materials

The bulk material approach focuses mainly on identifying new materials that have good electronic properties and a very low thermal conductivity, e.g. semiconductors that possess glass-like thermal conductivity. This concept was introduced by Slack (see chapter 34 of Ref. [40]), who proposed that phonon-glass electron-crystal (PGEC) materials were desirable candidates as TE materials. PGEC materials have a short phonon mean free path, so that less heat is conducted, and have a long electron mean free path, leading to a high σ.

The materials that classify in this category are skutterudites, clathrates, chalcogenides and other complex inorganic structures.

Skutterudites

$CoAs_3$ was first discovered in Skutterud, Norway, from where it derives its name. Skutterudites are composed of binary semiconducting compounds with the structure given by MX_3, where M = Co, Rh, or Ir and X = P, As or Sb [44]. They have a cubic crystal structure with eight M atoms occupying the corners of the cubic cell and twenty four atoms situated such as to create a void within the cubic cell. This system has an open structure lattice, with two voids in each unit cell, that are large enough to accommodate different elements. The voids can be filled by group III, group IV, lanthanide, actinide and alkaline-earth ions, leading to a filled skutterudite. The new element is now given by the formula $\square_2M_8X_{24}$, with $\square$ representing the void.

Introduction of a guest atom into the void acts as a scattering center, where the void-fillers can vibrate or 'rattle', and thus provide effective phonon scattering centers which lead to a drastic reduction of the thermal conductivity. The voids can be full or partially filled. The partial filling has given good results in n-type materials. Nolas et *al.* [55] have studied the introduction of different percentage of La in $CoSb_3$. They measure κ as a function of partial filling and observe a great reduction when the concentration of La in the skutterudite is 25 – 30%. In partial filling, the random distribution of La atoms into the voids is more effective in scattering phonons. In the full filling, atoms are distributed with order, this leads to a less effective scattering of phonons. In addition, partial fillers act as an electron donor leading to an increased carrier concentration. Nolas et al. [56] have measured $Yb_xCo_4Sb_{12}$ with x = 0.066 and 0.19. $Yb_{0.19}Co_4Sb_{12}$ gives a better ZT, with a value of 0.3 at room temperature and $ZT \sim 1$ at $T = 600$ K. Fig. 1.9 reports the temperature dependence of ZT for $Yb_{0.066}Co_4Sb_{12}$ and $Yb_{0.19}Co_4Sb_{12}$ [56].

Although these ZT values are not yet sufficient, research in the skutterudite families has lead to a better understanding of thermal transport phenomena and new-phonon scattering mechanism that has pushed research in finding new materials with similar structure to skutterudites. Another material of great interest is represented by the clathrates family, described in more detail below.

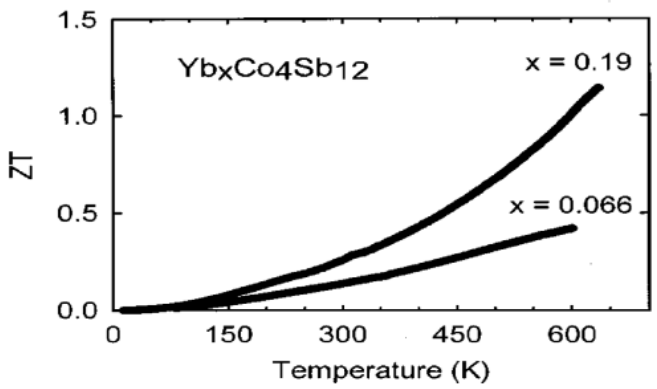


Figure 1.9: ZT versus temperature of $Yb_xCo_4Sb_{12}$, where x = 0.066 and 0.19. Figure taken from Ref. [56].

Clathrates

Similarly to skutterudites, clathrate compounds have a periodic crystal structure with tetrahedrally bonded atoms that form a cage or void where it is possible to accommodate a heavy atom that acts as a rattler [51, 57, 58, 59]. There are different forms of clathrate, the most common are type-I and type-II. Fig. 1.10(a) shows type-I structure, as a cubic cell that contains forty-six group-IV atoms in the unit, *i.e.* Si, Ge, or Sn. The cubic cell is formed of two type of cavities, two smaller pentagonal dodecahedra on each corner of the cubic cell, with twenty molecules of water arranged to form twelve pentagons and two hexagons. There are eight atomic cages (M), this gives in total 8M-46(IV) [44, 60].

The structure of type-II clathrates is shown in Fig. 1.10(b), the unit cell is composed of 136 atoms arranged in sixteen pentagonal dodecahedra and eight hexakaidecahedra. The cage walls, given by the twelve pentagons and four hexagons, are formed of twenty-eight water molecules. In total, a unit cell is composed of twenty four cavities and the general formula is 24M-136(IV). Due to these structure, clathrates exhibit thermal conductivity values that are close to or smaller than that of amorphous materials. Among these materials, Ge clathrates are the one that show good potential for TE applications. They exhibit a glass-like thermal conductivity and high carrier concentration. $Ba_8Ga_{16}Ge_{30}$ is amongst the material with the highest ZT, with a value of 1.35 at 900 K and an extrapolated ZT = 1.63 at 1100 K [61]. Fig. 1.11 shows the ZT of $Ba_8Ga_{16}Ge_{30}$ as a function of temperature. Here, values beyond 900 K, represented by dashed lines, were extrapolated. These materials are very promising for Te applications at high temperatures.

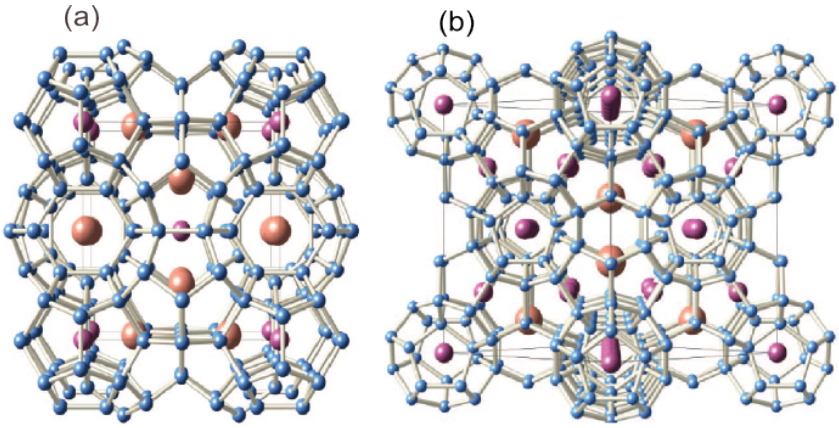


Figure 1.10: Crystal structure of (a) type I clathrate and (b) type II clathrate. The framework atoms are represented in blue, the guest atoms inside the tetrakaidecahedra are in orange and the guest atoms inside the pentagonal dodecahedra are purple. The figure was taken from Ref. [60].

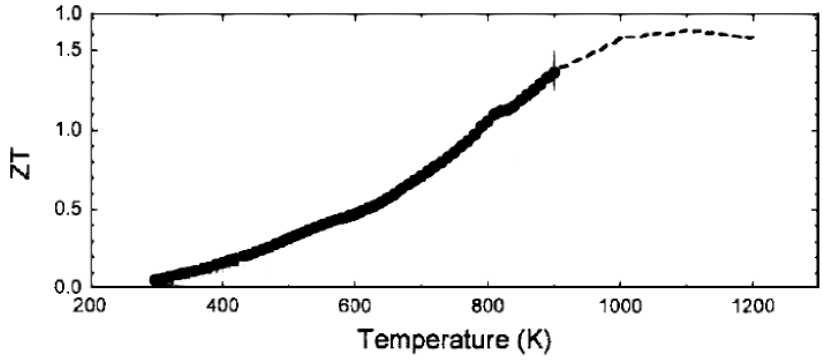


Figure 1.11: ZT as a function of temperature for a crystal clathrate of $Ba_8Ga_{16}Ge_{30}$, values beyond 900 K were extrapolated [61].

More complex Bi and Te based materials

$CsBi_4Te_6$ $CsBi_4Te_6$ has an anisotropic structure and possesses a lamellar structure with sheets of Bi_4Te_6 alternated with layers of Cs^+ ions. When properly doped with SbI_3 or Sb, its ZT can reach a value up to 0.8 at 225 K [60]. The peak of ZT can be shifted to even lower temperatures by controlling the doping level. This would allow utilisation for low temperature applications.

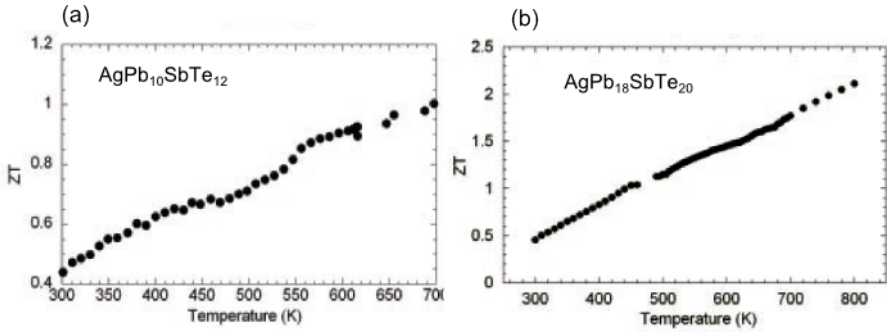


Figure 1.12: ZT as a function of temperature for (a) $AgPb_{10}SbTe_{12}$, and (b) $AgPb_{18}SbTe_{20}$. Figure was taken from Ref. [63].

Tl_9BiTe_6 and Tl_2SnTe_5 These are thallium based compounds, where Tl_9BiTe_6 has a $\kappa_L \sim 0.39$ $Wm^{-1}K^{-1}$ at 300 K, and a $ZT \sim 1.2$ at 500 K [60]. While, Tl_2SnTe_5 similar to the previous ternary compound manifest a low $\kappa \sim 0.5$ $Wm^{-1}K^{-1}$ and an optimised $ZT \sim 1$ at 500 K [62].

Ag_9TlTe_5 This compound manifests a low κ, similar to the other thallium-based compounds, and a ZT ~1.23 at 700 K.

These results are interesting from a scientific point of view, but there is an impracticability of TE thallium-based devices due to its toxicity.

$AgPb_mSbTe_{m+2}$ This belongs to the chalcogenide family and it is defined as LAST-m, where LAST stands for 'lead antimony silver tellurium'. Values of ZT range from 1.2 for LAST-10 and 1.7 for LAST-18 at 700 K [63]. Figure 1.12(a)-(b) show the ZT of LAST-10 and LAST-18. The change of the parameter m can lead to different type of compositions.

1.6.3 Nanostructured materials

The main advantage in low-dimensional materials lies in their size, which can be made smaller than the mean free path of phonons, but larger than that of electrons and holes. This brings a reduced κ, without compromising the other ZT parameters [33, 64, 65].

In the 1990s, Hicks and Dresselhaus calculated the theoretical ZT of Bi_2Te_3 quantum-well superlattices and quantum wires [27, 28]. As the dimensionality of the material is reduced, going from 3D to 2D and further down to 1D, there is an increase in the ZT factor due to the change in the density of states. The reduced dimensionality additionally

causes a reduced thermal conductivity due to increased phonon scattering as these may be scattered off the interfaces. In Ref. [28] a calculated ZT_{1D}= 6 is found when a 10-Å-wide wire is considered, against a ZT_{2D} = 2.5 for superlattices with 10 Å width.

Utilisation of low-dimensional materials has lead to a significant improvement of thermoelectric properties, as well as an increase in the ZT. These materials may be classified as nanotubes, nanowires, nanorods, nanoparticles, quantum well, superlattices and ultra-thin films. They will be now considered in more detail.

Carbon Nanotubes

A carbon nanotube (CNT) is composed of a graphene sheet wrapped into a seamless cylinder. High aspect ratio of ∼1000 are possible, where aspect ratio = length / diameter. There are two type of nanotubes, single-walled nanotubes (SWNT) and multi-walled nanotubes (MWNT), with the latter composed of concentric SWNT. Carbon nanotubes are rich in charge carriers with $\sigma = 10^6$ S/m, S of 80 μV/K for single MWNTs at 300 K [66] and 40 μV for SNWTs [67]. However, they exhibit extremely high κ, 3000 $\mathrm{Wm^{-1}K^{-1}}$ for MWNT and up to 10^4 $\mathrm{Wm^{-1}K^{-1}}$ for SWNT. This gives very low ZT of 6.4×10^{-4} for MWNTs and 4.8×10^{-4} for SWNTs.

CNT exhibit interesting properties that change depending on environmental gas conditions. S, in both SWNT and MWNT, is highly sensitive to oxygen exposure, with the sign of S changing in a reversible way from positive to negative as the sample is cycled between oxygen and vacuum [68]. The change of the sign of S indicates that the carbon nanotubes switch from p-type when exposed to oxygen, to n-type in vacuum conditions. However, if CNTs are doped, they manifest a permanent n- or p-type behaviour. Experiments on boron doped SWNT [69] and nitrogen MWNT [70] indicated permanent n- or p-type carriers, with boron acting as hole donor and nitrogen as an electron donor.

Although CNTs are very interesting and rich in charge carriers, their thermal conductivity needs to be reduced in order to achieve reasonable ZT values. In order to decrease κ, a similar approach to the filled skutterudites has been considered. Introduction of C_{60} molecules within the core of SWNTs would act as rattlers leading to a reduced κ. Figure 1.13(a) shows a schematic diagram of a CNT before and after the introduction of C_{60} in its core. Fig. 1.13(b) reports theoretical calculations of κ for empty CNT and C_{60} filled nanotubes as a function of temperature. Results indicate a reduction of ∼40% around 300

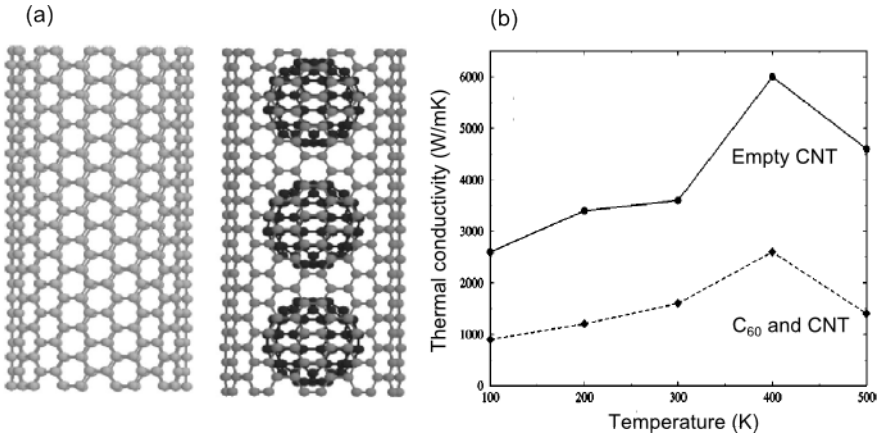


Figure 1.13: (a) Diagram of an empty CNT and integration of C_{60} within the CNT. (b) Theoretical calculation of κ in empty CNT and filled CNT. Figure taken from Ref. [71].

K. This indicates that introduction of rattlers within CNTs may be the route to a reduced κ. However, further progress is necessary to obtain more appropriate values of ZT.

Superlattices

Superlattices based mainly on materials with good thermoelectric properties have been investigated as a means to further increase ZT. These materials are Bi_2Te_3/Sb_3Te_3, PbTe/PbSe, Si/Ge and Bi/Sb superlattices. The anisotropic properties of superlattices allow the possibility to improve ZT in two directions, parallel (in-plane) and perpendicular (cross-plane) to the film. The potential of in-plane direction is given by the possibility of utilising the sharp features present in the density of states and a reduction of κ_L due to scattering at the interfaces. The cross-plane advantage relies on utilising interfaces as a reflector for phonons and allowing transmission of electrons.

Venkatasubramanian *et al.* have reported a $ZT \approx 2.4$ p-type Bi_2Te_3/Sb_2Te_3 thin film superlattices and a $ZT \approx 1.4$ for n-type $Bi_2Te_3/Bi_2Te_{2.83}Sb_{0.17}$ superlattices at 300 K [72]. The superlattices were grown by metallorganic chemical vapour deposition on GaAs substrates [73]. The thickness of both p- and n-type superlattices were 10 Å/50 Å. ZT in the cross-plane direction was measured with the Harman technique [74]. In this method, current passes through the sample, allowing all the parameters of $ZT = S^2\sigma T/\kappa$ to be measured at the same time and at the same place. $ZT = 1.4$ in the n-type superlattices, lower than the p-type material, was associated to the higher κ_L and also a lack of improvement in electronic mobilities compared to the bulk parent $Bi_2Te_{3-x}Sb_x$ alloys.

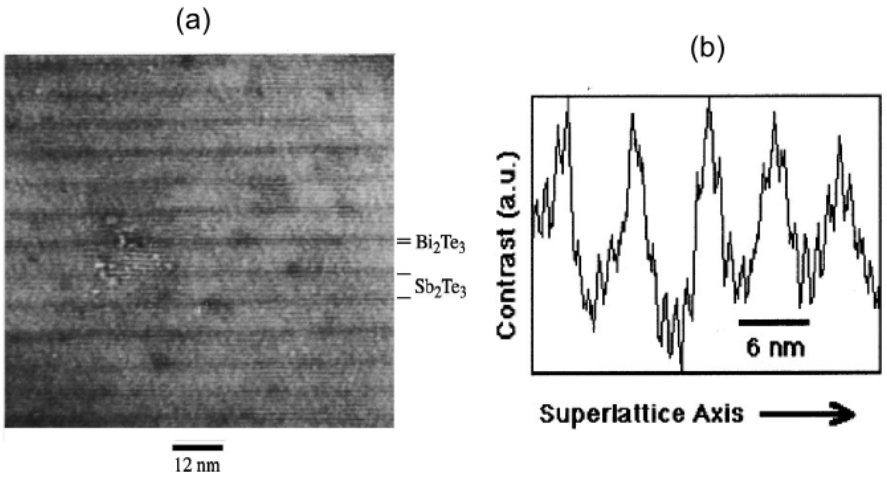


Figure 1.14: (a) TEM of Bi_2 Te_3 /Sb_2 Te_3 superlattice with a thickness of 10 Å/50 Å. (b) Intensity oscillation across the superlattice. Figures taken from Ref. [73].

In contrast, an enhanced carrier mobility was observed in p-type materials. This work suggests the possibility of achieving higher ZT in superlattices, since they act as phonon-blocking/electron-transmitting structures. Figure 1.14(a) shows a transmission electron micrograph of the Bi_2Te_3/Sb_2Te_3 superlattice, while Fig. 1.14(b) illustrates the intensity oscillation measured across the superlattice with thickness 10 Å/50 Å. Harman *et al.* [75] used molecular beam epitaxy to grow PbSeTe-based quantum dot superlattices. These manifested a better cooling efficiency when compared to their corresponding bulk material. The bulk PbTe-based alloys have a maximum $ZT \approx 0.4$ at 300 K, while the measured ZT of n-type PbSeTe/PbTe quantum dot superlattices is in the range of 1.3 to 1.6 at 300 K. This improvement was associated with the high density presence of quantum nanodots, composed of 100% PbSe. These nanodots were then embedded in a three-dimensional slab matrix of PbTe. Measurements of ZT on quaternary quantum dot superlattices based on PbTe/PbSnSeTe have given a value of 2 at 300 K [75].

Other superlattice systems have been investigated such as Si-Ge [76, 77], Bi-Sb [78], and skutterudite-based superlattices [79]. In Si/Ge superlattices and quantum dot superlattices the only measured parameter κ shows a significant reduction in the cross-plane.

Layered Co oxides

Hybrid crystal structures of oxide-based materials have also been investigated for TE applications. A p-type layered structure of Na_xCoO_2 composed of alternated CoO_2 and Na

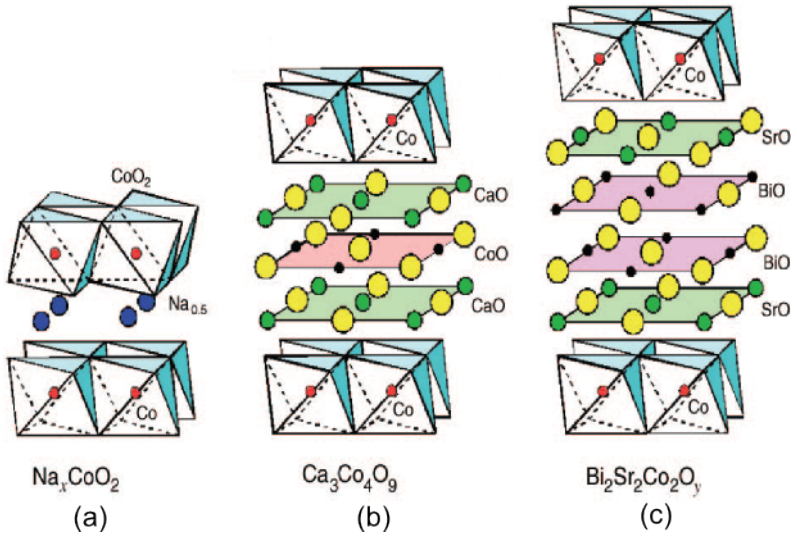


Figure 1.15: Illustration of the crystal structure of: (a) Na_xCoO_2, (b) $Ca_3Co_4O_9$, (c) $Bi_2Sr_2Co_2O_y$. Figure taken from Ref. [82].

layers, was studied as a function of x, with x the composition of Na. The crystal structures that can be obtained depend on the composition of x and are labeled as follows: α ($0.9 \leq$ x ≤ 1), α' (x $= 0.75$), β ($0.55 \leq$ x ≤ 0.6), and γ ($0.55 \leq$ x ≤ 0.74) phases [80, 81]. Good TE properties were observed for the γ phase. Other oxide layered structures with good Te properties are: $Ca_3Co_4O_9$ and $Bi_2Sr_2Co_2O_y$ [82]. Figure 1.15 shows a schematic illustration of the crystal structures of these oxide materials. Fig. 1.15(a)-(c) show the structures of Na_xCoO_2, $Ca_3Co_4O_9$ and $Bi_2Sr_2Co_2O_y$ [82], respectively. The measured thermoelectric parameters in the in-plane direction of these three structures are shown in Fig. 1.16. Fig. 1.16(a) shows the resistivity, with Na_xCoO_2 being the most conductive compound. S and κ are shown in Fig. 1.16 (b)-(c). The ZT values in these structures are: $ZT_{Na_xCoO_2} \approx 0.6$, $ZT_{Ca_3Co_4O_9} \approx 0.0256$ and $ZT_{Bi_2Sr_2Co_2O_y} \approx 0.025$. In this case, the high ZT of Na_xCoO_2 is due to its very low resistivity. The potential advantage of layered devices relies on the fact that is possible for electrical and thermal current to flow in different directions. This allows optimisation of the structure by choosing the appropriate thermal insulating layered block and conductive layered material.

1.6.4 Silicon Nanostructures

Most of the low-dimensional materials described above are very difficult to scale, such as Bi and Te, and are also difficult to integrate with existing semiconductor technology. More recently, attention has focused on Si based materials, due to their ease of integration with

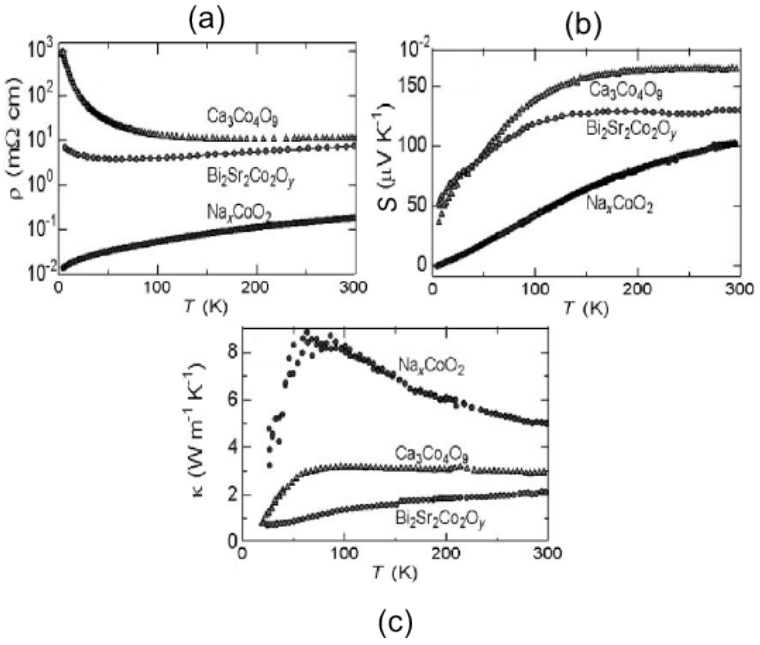


Figure 1.16: (a) In-plane resistivity vs. temperature, (b) Seebeck coefficient and (c) thermal conductivity as a function of temperature for the three Co oxide layered structures. Figure taken from Ref. [82].

existing semiconductor fabrication processes. Si is also one of the most abundant and low cost materials present [83]. If a good ZT were to be achieved, then fabrication of Si TE based devices would not be expensive.

Heavily doped bulk silicon, 10^{19} cm^{-3}, has a very poor ZT value which approaches 0.01 at 300 K [84] due to a high thermal conductivity $\kappa = 150$ Wm^{-1}K^{-1} at room temperature [85]. However, with reduced dimensions, an increase in ZT is expected as a result of the reduction of κ. Two research groups have reported a $ZT \approx 1$ in p-type SiNWs [86, 87].

Single silicon nanowire

Hochbaum *et al.* [86] have measured a $ZT \approx 0.6$ at room temperature for a single p-type silicon nanowire (NW). Here, p-type SiNWs were synthesised by an aqueous electroless etching method and by a vapor-liquid-solid (VLS)-grown gold-catalysed method. The electroless etched NWs were rougher than the VLS grown NWs, with the former having an average surface roughness of the order of several nm (1 – 5 nm). A single NW was suspended in between two membranes, one acting as a heater and the other one as a heat sink. Fig. 1.17(a) shows the single NW anchored to the two membranes by platinum (Pt) bonding.

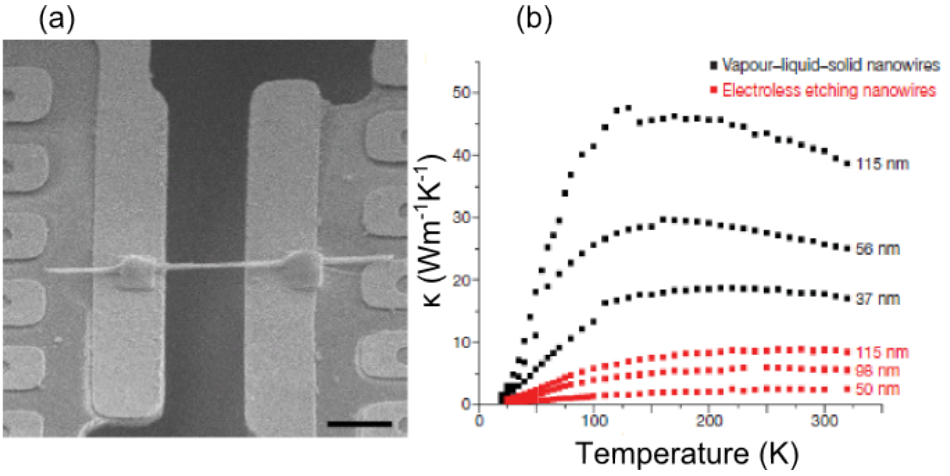


Figure 1.17: (a) SEM image of a single electroless etched NW bonded to two Platinum bridges that act as heater. (b) Thermal conductivity of SiNWs as a function of temperature and NW diameter, for NWs obtained by electroless etching and by VLS method. The scale bar is 2 μm. Figure taken from [86].

The thermal conductivity κ of the NWs, fabricated using two different methods, was measured as a function of the diameter. Fig. 1.17(b) shows the measured temperature dependence of κ for VLS and electroless etched NWs. In both cases, κ exhibits a diameter dependence, however the electroless etched NWs show a five to eight time lower κ than VLS NWs. This suggests that NW surface roughness acts as a source of scattering for phonons. Furthermore, κ is also studied as a function of the doping level. Fig. 1.18 reports κ as a function of temperature for electroless etched NWs with resistivity from 10 Ωcm to 10^{-2} Ωcm, corresponding to doping levels $\sim 10^{14}$ – 10^{18} cm^{-3}. κ of the 52 nm diameter is strongly reduced $\sim$1 W/mK, this is close to the amorphous limit for silicon. As mentioned above, Hochbaum *et al.* [86] argue that the reason for this significant decrease is due to an increased surface scattering. S and ρ are then measured on a heavily doped 48 nm diameter NW, to maximize σ. These values and κ of the 52 nm diameter NW were used to calculate ZT. Figure 1.18(b) shows S^2/ρ, on the left coordinate, and ZT, on the right coordinate, as a function of temperature. $ZT_{300K} \sim 0.6$, as a consequence of the highest S^2/ρ.

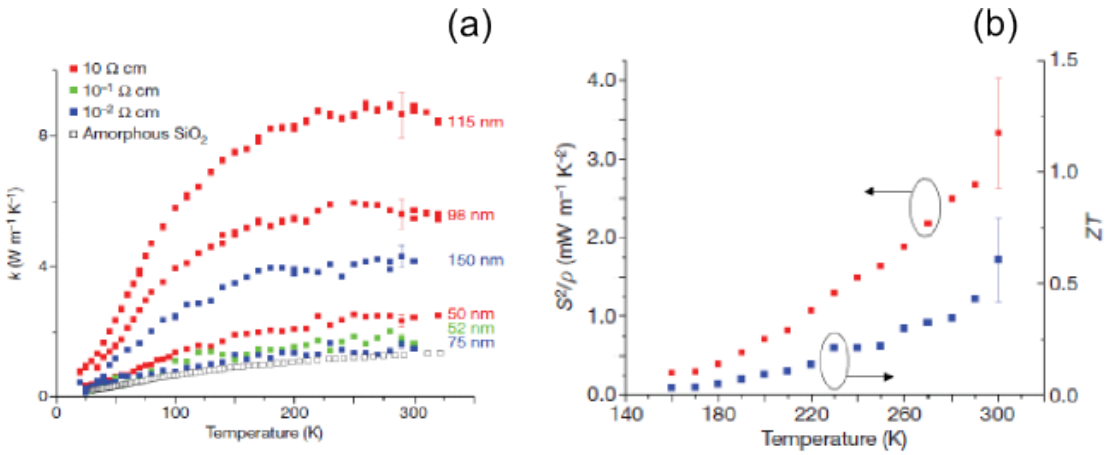


Figure 1.18: (a) Thermal conductivity for NWs with different diameter and different doping level as a function of temperature. (b) Power factor $S^2\sigma$ (left coordinate) and ZT (right coordinate) of single nanowire. Figure taken from Ref. [86].

Si nanowires in parallel

Boukai *et al.* [87] measured the thermal characteristics of ∼100 p-SiNWs in parallel. They reported a ZT∼1 at 200 K, and their measured $\kappa = 0.99$ Wm^{-1}K^{-1} is below the theoretical limit for silicon. NWs were fabricated by the superlattice nanowire pattern transfer (SNAP) method. The atomic control over the layer thickness of the superlattice allows manipulation in the spacing and width of the nanowires. NW arrays of several micrometers length were prepared with a lateral width × thickness dimension of 10 nm × 20 nm and 20 nm × 20 nm. Figure 1.19(a) shows a scanning electron micrograph (SEM) image of the suspended platform used to measure the thermal characteristics of the SiNWs. These are indicated in the figure in the green color.

A four-point probe of the electrical conductivity measurement indicated that σ varied in between 10% to 90%. A set of data for 10 and 20 nm wide NWs were collected to establish κ. A $\kappa = 0.76$ Wm^{-1}K^{-1}, below the amorphous limit, was found for the 10 nm wide NW. Figure 1.19(b) shows S^2 versus temperature for 20 nm wide NWs of doping levels of 3×10^{19} cm^{-3} to 2×10^{20} cm^{-3}. The NWs with a doping level of 7×10^{19} cm^{-3} give the highest S^2 value. The data presented in Fig. 1.19(b) are normalised to an individual NW. Finally, ZTs of 20 and 10 nm wide NWs corresponding to two different doping levels were measured. These ZT values are shown in Fig. 1.20. The 20 nm wide NW with doping level

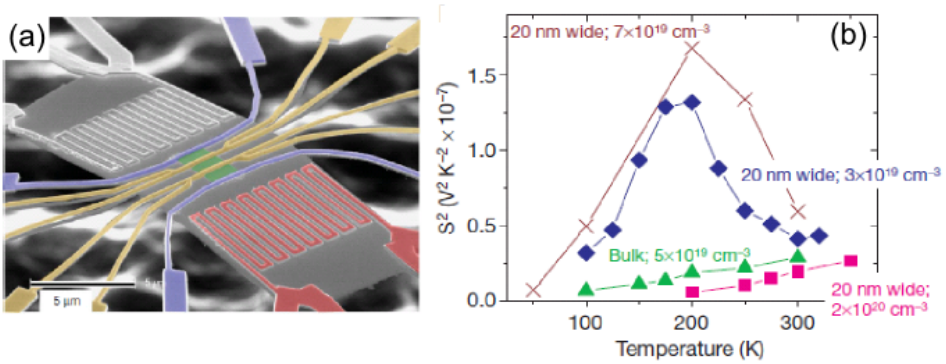


Figure 1.19: (a) SEM image of the device used by Boukai *et al.* [87] to characterize the thermoelectric quantities of SiNW arrays. (b) S^2 as a function of temperature for different doping levels. The plot also reports as a reference the data of bulk Si. Figure taken from [87].

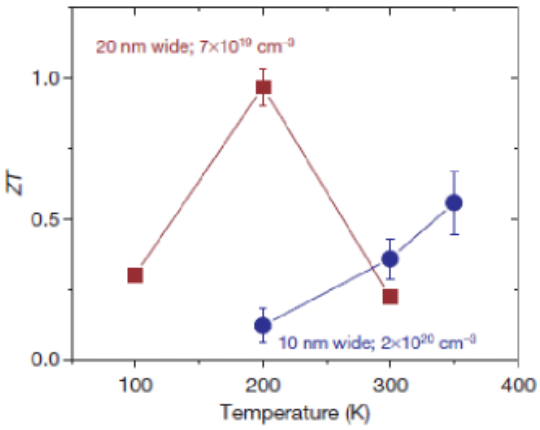


Figure 1.20: ZT versus temperature for 10 nm and 20 nm wide NW of doping level 2×10^{20} cm^{-3} and 7×10^{19} cm^{-3}, respectively. Figure taken from Ref. [87].

7×10^{19} cm^{-3} manifests a $ZT \approx 1$ at 200 K. This is due to the peak of S that is centered at 200 K. Boukai *et al.* argue that the increase in S is due to a high number of phonons contributing to the electron transport, phonon drag, as a consequence of a crossover from a three-dimensional to a one-dimensional behaviour.

'Holey' silicon

Tang *et al.* [88] have studied a different form of nanostructure, 'holey' silicon. High density nanoscopic holes of p-Si with dimension of 350, 140 and 55 nm were created in thin 100 nm single crystalline silicon membranes either by nanosphere lithography or block co-polymer lithography. Holey silicon nanoribbons were characterised by a micro-electromechanical system device, shown in Fig. 1.21(a). SEM images of the nanoribbons of 350 nm and

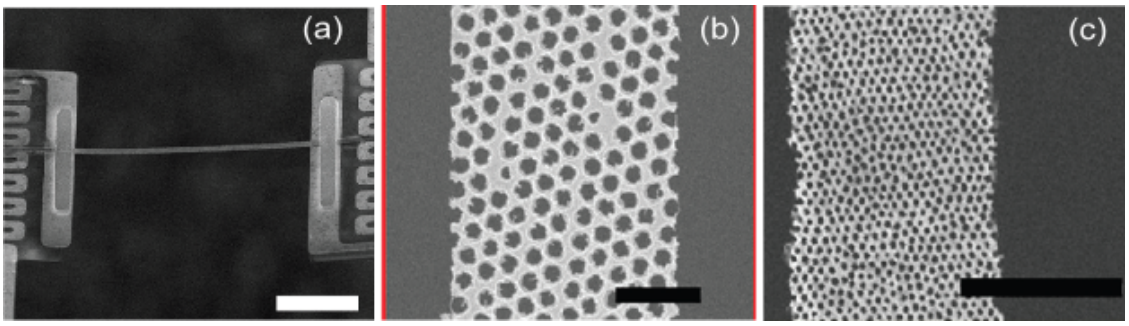


Figure 1.21: (a) SEM image of a holey silicon ribbon suspended between the two SiN_x membranes used to thermoelectrically characterise the ribbons. (b) SEM image of a 350 nm pitch and (c) of a 55 nm pitch. The scale bars are (a)-(b) 10 μm, and (c) 1 μm, respectively. Figure were taken from Ref. [88].

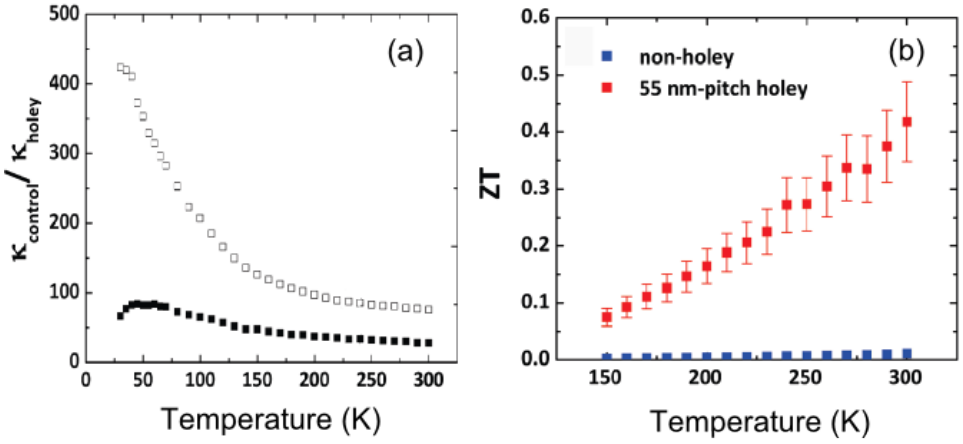


Figure 1.22: (a) Comparison of κ of bulk silicon (white squares), doping 1.7×10^{19} cm^{-3} and κ of 55 nm nanoribbon (black squares). (b) ZT of 55 nm pitch ribbons as a function of temperature. Figures taken from Ref. [88].

55 nm are shown in Fig. 1.21(b) and (c). The porosity of the ribbons was 35%. Figure 1.22(a) shows a comparison between κ of heavy doped bulk silicon and nanoribbons of 55 nm of 5×10^{19} cm^{-3}. A minimum $\kappa = 1.73$ Wm^{-1}K^{-1} at 300 K was measured for the 55 nm holey ribbons. Figure 1.22(b) shows the temperature dependence of ZT for the 55 nm ribbons, a maximum value of $\sim$0.4 was achieved at 300 K. This corresponds to a 40 times increase in the ZT compared to their parent bulk Si, this is consistent with the results measured in the previous works [86, 87].

In summary, bulk Si is a poor thermoelectric material, but by reducing the thermal conductivity without much affecting the Seebeck coefficient and electrical resistivity, $ZT \sim 1$ is possible in Si. These observations demonstrate the potential for Si TE devices, raising

the possibility of increased functionality in Si and direct integration of TE and electronic devices for energy scavenging.

1.6.5 Figure of merit of advanced bulk and nanocomposite materials

Tab. 1.3 reports the ZT values for the advanced bulk thermoelectric and low dimensional materials. The materials are grouped by their corresponding family, *i.e.* skutterudites, clathrates, superlattices, Si nanostructures, etc. For some materials, the room temperature ZT as well as their maximum ZT values are shown; for others, only the maximum ZT is reported with the correspondent temperature given. From Tab. 1.3, among the advanced bulk thermoelectrics, $AgPb_{18}SbTe_{20}$, belonging to LAST, has the higher $ZT{\sim}1.8$ at 700 K. From the data shown in Tab. 1.3, advanced bulk thermoelectric materials are very good for high temperature applications, due to their high ZT for temperatures above 500 K, except for $CsBi_4Te_6$ that has a $ZT{\sim}0.8$ at 225 K. In nanostructured materials, the highest $ZT{\sim}2.4$ is reported for p- Bi_2Te_3/Sb_2Te_3 superlattices. In Si nanostructures, $0.4 \leq ZT \leq 0.6$ was reported at room temperature for SiNW [86] and Si nanoribbons [88]. The highest $ZT{\sim}$ 1 was measured at 200 K for p-Si nanowires in parallel by Ref. [87]. Fig. 1.23 shows the ZT values as a function of temperature of the advanced bulk and nanocomposite materials reported in Tab. 1.3. The ZT of MWNT, SWNT and the oxide $Ca_3Co_4O_9$ have not been reported as their values are very close to zero. Whereas, the value of n-PbTe/PbSnSeTe, ranging between 1.3 to 1.5, has been approximated in the graph by the average value 1.5. The maximum ZT is given for the p- Bi_2Te_3/Sb_2Te_3 superlattice at 300 K and $AgPb_{18}SbTe_{20}$ at 700 K. Superlattices are the material with the highest ZT in the room temperature range. Whereas, in the room temperature range, nanostructures manifest ZT values below than 1, but their ZTs are higher than the advanced bulk materials. Hence, they may represent good candidates for room temperature applications.

Material	*ZT*	*Reference*
Skutterudites		
$Yb_{0.066}Co_4Sb_{12}$	0.15 (300 K); 0.5 (600 K)	[56]
$Yb_{0.19}Co_4Sb_{12}$	0.3 (300 K); 1 (600 K)	[56]
Clathrates:		
$Ba_8Ga_{16}Ge_{30}$	1.35 (900 K)	[61]
$CsBi_4Te_6$	0.8 (225 K)	[60]
Thallium based:		
Tl_9BiTe_6	0.39 (300 K); 1.2 (500 K)	[60]
Tl_2SnTe_6	1 (500 K)	[62]
Ag_9TlTe_6	1.23 (700 K)	[60]
Chalcogenide		
$AgPb_{10}SbTe_{12}$	1.2 $Ca_3Co_4O_9$(700 K)	[63]
$AgPb_{18}SbTe_{20}$	1.8 (700 K)	[63]
Carbon nanotubes:		
MWNT	$6.4{\cdot}10^{-4}$ (300 K)	[66]
SWNT	$4.8{\cdot}10^{-4}$ (300 K)	[67]
Superlattices $AgPb_{18}SbTe_{20}$		
p- Bi_2Te_3/ Sb_2Te_3	2.4 (300 K)	[72]
n- PbSeTe/PbTe	1.4 (300 K)	[72]
n- PbTe/PbSnSeTe	1.3 – 1.6 (300 K)	
Layered Co oxides:		
Na_xCoO_2	0.6 (300 K)	[82]
$Ca_3Co_4O_9$	0.0256 (300 K)	[82]
Si Nanostructures:		
Single *p*- SiNW	0.6 (300 K)	[86]
p- SiNWs in parallel	1 (200 K)	[87]
p- 55 nm ribbons	0.4 (300 K)	[88]

Table 1.3: ZT values in advanced bulk thermoelectric materials and in low dimensional materials at a given temperature. References are given in the last column.

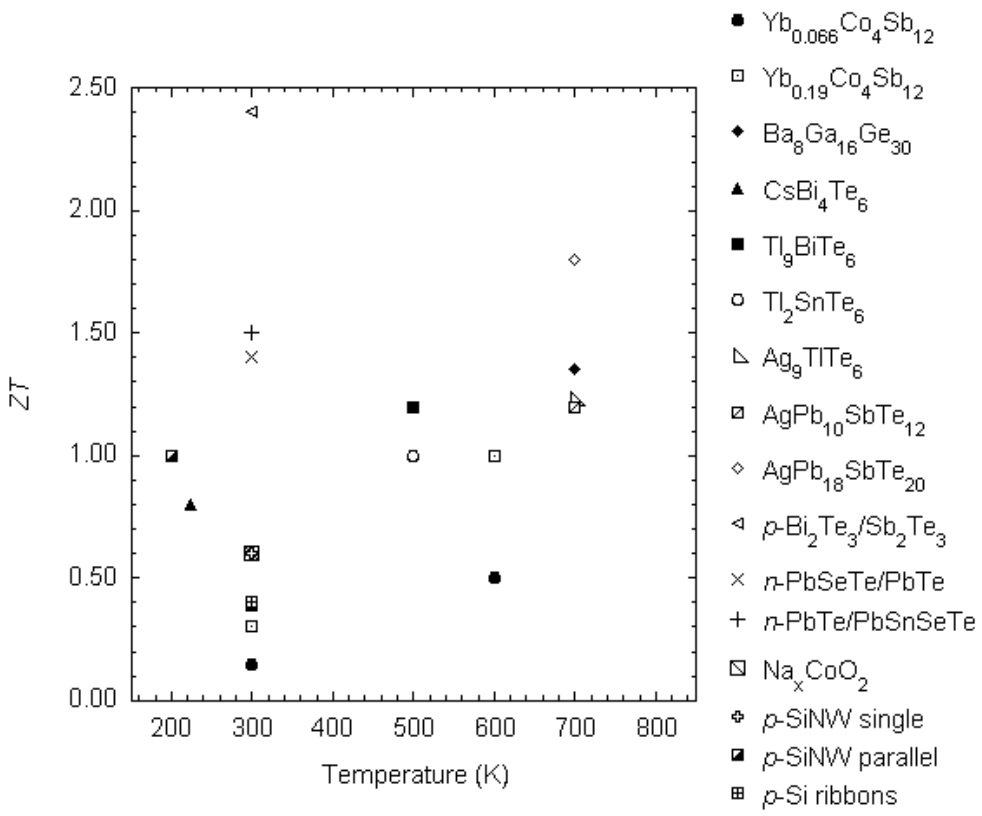


Figure 1.23: ZT values as a function of temperature for TE materials reported in Tab. 1.3. ZT of $Ca_3Co_4O_9$ and CNT were not reported due to its values close to zero.

1.7 Summary of this project

The intent of this project is to investigate the enhancement of TE performances in SiNW arrays. Here, the temperature dependence of S, the primary TE parameter, σ and κ are measured in samples consisting of $\sim 10^7$ – 10^8 vertically-aligned SiNWs, fabricated using metal-assisted chemical etching, and compare this to bulk Si samples. Realisation and testing of a measurement device for ambient condition measurements and a transient technique to measure temperature and voltage across the sample is developed, allowing measurement in moderate vacuum of thermoelectric parameters even in very thin samples. Both lightly- and moderately-doped SiNW samples were measured, in order to characterise the effect of doping on the electron/phonon interaction and transport within the nanostructured material. In the lightly-doped sample, the Seebeck coefficient of SiNW arrays S_{NW} was found $\sim 3S_{bulk}$ and $ZT_{NW} \approx 100ZT_{bulk}$ at room temperature. In the moderately doped Si, $S = 2.5S_{Bulk}$, where $S = S_{Bulk} + S_{NW}$ and a $ZT = 55ZT_{Bulk}$ at 280 K. This demonstrates a large improvement in the TE properties of SiNWs compared to bulk Si and raises the possibility of practical thermoelectric devices in Si.

1.7.1 Outline of the thesis

This thesis is divided into seven chapters. The topics covered on each of them are as follows:

Chapter 2:

The principles of the thermoelectric theory and the thermal transport coefficients are discussed in detail for the lightly and heavily doped cases. Thermoelectric characterisation, *i.e.* Seebeck coefficient, electrical conductivity and thermal conductivity, of thin samples is introduced for room temperature measurements and in vacuum.

Chapter 3:

A brief introduction for the fabrication of the nanostructures is given. The MACE process is discussed in detail as this is the method utilised for fabrication of n- and p-type lightly doped and n-type moderately doped SiNW arrays. Ag metal deposition and etching of NWs in two different steps is discussed. Also, the morphology of NWs as a function of

metal deposition, H_2O_2 concentration and doping level are considered.

Chapter 4:

Here, the measurement apparatus is introduced and tested for room temperature characterisation of the Seebeck coefficient. n- and p-type bulk Si and SiNWs with and without metal contacts are measured. Seebeck coefficient of n- and p-type SiNW array samples with different lengths are measured and analysed as a function of the Fermi level.

Chapter 5:

In this chapter, the characterisation of SiNW arrays in a closed-cycle cryostat with moderate vacuum conditions is introduced. Temperature measurements are performed in the range from 300 – 30 K. A transient technique to measure temperature and voltage across the sample is developed, allowing thermoelectric measurements in very thin samples. The effect of doping on the electron/phonon interaction and transport within the nanostructured material is studied by measuring samples with two different doping levels, *i.e.* lightly and moderately doped samples.

Chapter 6:

Two terminal I-V measurements of bulk Si and SiNWs with two different doping levels are presented in this chapter. I-V curves as a function of temperature are characterised in the range 300 – 40 K. The conductance of the samples and activation energies are extracted and the temperature dependence of the I-V characteristics are measured in n- and p-type polymer filled NWs. In the second part of this chapter, a transient heat measurement technique is presented and the thermoelectric conductivity of the SiNWs is measured using this technique. In conclusion, ZT calculation for the moderately doped samples are given.

Chapter 7:

Here, conclusions and recommendation for future work are presented.

2 Thermoelectricity: Theory

2.1 History

Thermoelectric generation is characterised by three phenomena: the Seebeck, Peltier, and Thomson effects. In 1821, Thomas J. Seebeck discovered the first and the most fundamental of these effects. He observed that an open circuit potential difference ΔV was produced as a result of a temperature gradient, at the junction between two dissimilar conductors at different temperatures, see Fig. 2.1 (a). This phenomenon was named the Seebeck effect [37, 89].

Later, in 1834, Jean C. A. Peltier published some results that provided the discovery of a second thermoelectric effect. When electrical current was passed through a junction of two dissimilar conductors, there was absorption or generation of heat Q depending on the direction of the current, see Fig. 2.1 (b). In 1838, Lenz demonstrated that if current was passed through a bismuth-antimony junction, water could be frozen. Otherwise, if the direction of the current was reversed, the ice could be melted [37].

In 1855, William Thomson showed that by using the principles of thermodynamics, a relationship would be demonstrated between the Seebeck and Peltier effects [42]. The derivation of this relationship led to the discovery of a third thermoelectric effect, now called the Thomson effect. When current flows in the direction of a temperature gradient ΔT, heating or cooling ΔQ is produced, as sketched in Fig. 2.1 (b). In between 1909–1911 the German scientist E. Altenkirch developed the theory of thermoelectric generators and refrigerators. He showed that for both applications, materials with high Seebeck coefficient, and high electrical conductivities were required in order to decrease the Joule heating, and a low thermal conductivity was necessary to minimise heat transfer losses. At this time, thermoelectricity and the thermoelectric effects were well known; despite this fact, good thermoelectric materials were not yet identified. Advances in the field were made when

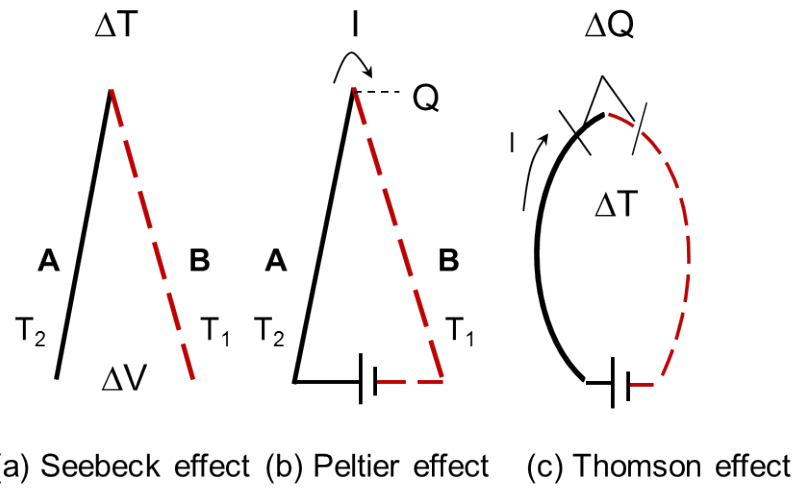


Figure 2.1: The thermoelectric effects, A (black solid line), B (red dashed line) represent two different type of conductors and Q is the heat produced or absorbed. T_2 and T_1 correspond to two different temperatures of the junction. Adapted from Ref. [37].

metallic thermocouples were substituted by semiconductor thermocouples.

In the 1920s, Abram Ioffe introduced semiconductors as promising thermoelectric materials. Although metals show a high value of the ratio of electrical to thermal conductivity (σ/κ), the majority of them have a Seebeck coefficient S which does not exceed a few μV/K, as mentioned in section 1.4. In semiconductors S can reach values of up to one or more mV/K [25, 90], but the ratio of the electrical to the thermal conductivity is smaller than in metals. However, this ratio can be easily manipulated by addition or removal of dopants. This implies that semiconductors are superior to metals in thermoelectric applications.

In 1954, Goldsmid and Douglas [26] discovered the potential of bismuth telluride Bi_2Te_3 for thermoelectricity. Until now, Bi_2Te_3 remains the most widely used thermoelectric material and the material with the highest efficiency, $ZT \approx 1$ [91].

2.2 Thermoelectric effects

A thermoelectric material converts a temperature difference directly into a potential difference, known as the *Seebeck effect*. Conversely, when a voltage is applied to it, it creates a temperature difference, namely the *Peltier effect*. A coefficient is associated to each of the thermoelectric effects. Hence, the *Seebeck*, *Peltier* and *Thomson* coefficients are explained

in terms of S, Π and τ coefficients, respectively.

Let us consider a basic thermoelectric circuit as shown in Fig. 2.2, which is composed of two dissimilar conductors A and B, with junctions at points W and X [44]. If a temperature difference $\Delta T = T_1 - T_2$ is applied between W and X, a voltage difference $\Delta V = V_1 - V_2$ will appear between the two conductors ('B'). Under open circuit conditions, the ratio of ΔV to ΔT is proportional to an intrinsic property of the material defined as the *Seebeck coefficient* S_{AB} and also referred to as the thermoelectric power. This can be written as [44, 92]

$$S_{AB} = \lim_{\Delta T \to 0} \frac{\Delta V}{\Delta T} = \frac{dV}{dT} \tag{2.1}$$

with the sign of S_{AB} governed by the materials (A) and (B) and the relative temperatures of the junctions. The sign convention considers S_{AB} positive, if the electromotive force tends to drive an electric current through conductor (A) from the hot to the cold junction. The magnitude of S_{AB} depends on the absolute temperature of the junctions.

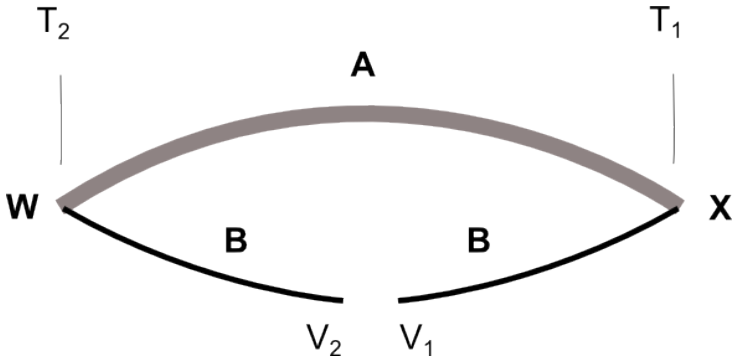


Figure 2.2: Thermoelectric circuit formed of two different conductors A and B, when a temperature difference is applied at its junctions. Figure adapted from ref. [44] .

If current is passed through the circuit in Fig. 2.2, then absorption of heat from the surrounding or release of heat to the surrounding occurs. The ratio of the electric current I to the rate of heating or cooling Q_P developed in this process at each junction is proportional to the *Peltier coefficient* Π_{AB} [44]

$$\Pi_{AB} = \frac{Q_P}{I} \tag{2.2}$$

Here, the sign convention considers I as positive, if current flows from (A) to (B), see

Fig. 2.2, and $Q_P > 0$ implies heat absorption by the system. As for S_{AB}, the sign of Π_{AB} depends on the materials (A) and (B) and the temperature of the junctions. Conventionally, Π_{AB} is defined as positive, if the junction at which the current enters (A) is heated and the junction at which it leaves (B) is cooled [93]. The potential difference that builds up due to Peltier heating or cooling opposes the potential difference that builds up in the Seebeck effect. This implies that the two coefficients are closely related to each other. Thomson (Lord Kelvin) considered a thermoelectric system as a reversible system and he applied the first and second laws of thermodynamics to the thermoelectric circuit, obtaining a relationship between S_{AB} and Π_{AB} as follows [93, 94]

$$\Pi_{AB} = S_{AB}T \tag{2.3}$$

Eq. 2.3 is known as the Kelvin relation. Thomson concluded that if *Peltier* heating is produced when current passes through a TE circuit, then the *Peltier* voltage produced in the process will equal the *Seebeck* voltage, and both coefficients should be linearly proportional to the temperature difference. Furthermore, Thomson realised that there is reversible heat generation or absorption whenever an electric current passes through a single homogeneous conductor, where a temperature gradient dT is maintained. The *Thomson* heat Q_T generated or absorbed is proportional to the current (I) and is given by

$$Q_T = \tau I dT \tag{2.4}$$

Hence, the *Thomson coefficient* τ is defined as the rate of heating per unit length of a conductor as a result of a unit current passing along the conductor, when a unit temperature gradient is present. τ is given by [89]

$$\tau_{AB} = T\frac{dS_{AB}}{dT} \tag{2.5}$$

The sign convention of the *Peltier* coefficient applies also to the *Thomson* coefficient. τ is positive if heat is absorbed, $Q_T > 0$, and current flows from the cold to the hot side. These three TE effects described are reversible. In a reversible effect the sign changes both with direction of the electric current and/or with temperature gradient [94]. When

a magnetic field is present other thermoelectric effects occur, *i.e. Hall*, *Ettingshausen* and *Nernst* effects.

In an isotropic material, when a current density i_x, along the x-axis and a magnetic field B_z are present, then an electric field E_y along the y-axis will appear [44]. E_y is proportional to both the magnetic field and the current density. This is known as the *Hall effect* and the *Hall coefficient* R_H is given by [44]

$$|R_H| = \frac{E_y}{i_x B_z} \tag{2.6}$$

If there is a temperature gradient dT/dx and a magnetic field B_z, then a transverse electric field E_y will appear. This is the *Nerst effect*, corresponding to the transverse equivalent of the Seebeck effect and it should be measured in the absence of current flow. The *Nerst coefficient* N is given by [44]

$$|N| = \frac{E_y}{B_z}\left(\frac{dT}{dx}\right)^{-1} \tag{2.7}$$

When there is a current flow and a transverse temperature gradient, the *Ettingshausen effect* will appear. This is the transverse equivalent of the Peltier effect. The *Ettingshausen coefficient* P is defined as [44]

$$|P| = \frac{1}{i_x B_z}\frac{dT}{dy} \tag{2.8}$$

Similarly to S and Π that obey the Kelvin relationship (Eq. 2.3), N and P obey the *Bridgman* relationship [44]:

$$P\kappa = NT \tag{2.9}$$

where κ is the thermal conductivity. There is a final effect due to the magnetic field presence. This is known as the *Righi-Leduc* effect and is the appearance of a transverse temperature gradient due to an imposed longitudinal gradient. The Righi-Leduc coefficient RL is expressed as follows:

$$RL = \frac{1}{B_x}\frac{dT}{dy}\left(\frac{dT}{dx}\right)^{-1} \tag{2.10}$$

where RL should be measured in open circuit conditions. A more detailed description of these effects can be found in Ref. [44].

2.3 Thermoelectric effects in semiconductors

2.3.1 Semiconductors

Let us consider how the thermoelectric effects originate in a semiconductor. We begin with a basic introduction to electrical conduction in a semiconductor. Semiconductors are solid materials that are characterised by a finite forbidden energy gap. Here, electrons lie in two bands, the valence and the conduction band, separated by an energy gap E_g. At temperature $T = 0$, the valence band is completely filled with electrons. In contrast, the conduction band is completely empty of electrons. If a sufficient amount of energy is provided, *i.e.* via thermal excitation, than an electron will jump from the valence to the conduction band. This leaves behind a vacancy that is called hole. The electron in the conduction band, and the hole in the valence band, can move freely through the semiconductor, such that an applied voltage results. Both electrons and holes are called charge carriers. Pure semiconductors are referred to as 'intrinsic' and carriers become available for conduction only after thermal excitation of electrons. However, as 'intrinsic' semiconductors are poor conductors, impurities are added to increase the number of carriers available for electrical conduction. This process is called doping and the semiconductors are now referred to as 'extrinsic'. The impurities supply or trap charge carriers that are close to the conduction or valence band, respectively, hence creating electrons or holes. Impurities that increase the number of electrons are called donors (e.g. phosphorus in silicon) and the resulting doped semiconductor is known as n-type. If the number of holes is increased than the impurities are called acceptors (e.g. boron in silicon) and the semiconductor becomes p-type.

A further concept to consider is the Fermi energy E_F or Fermi level. At the temperature of absolute zero, all the states up to E_F are occupied by electrons and the energy states above E_F are empty. In contrast, if we consider a finite temperature T, these states are partially filled within a temperature range of $\sim 2k_BT$ of E_F. The probability to find an electron in any given energy state is related to the energy difference between the state and E_F. Figure 2.3(a)-(b) show the junction between a metal and n-, and p-type semiconductors, in equilibrium. Here, the energy of the bottom of the conduction band is indicated by E_C and the top of the valence band by E_V.

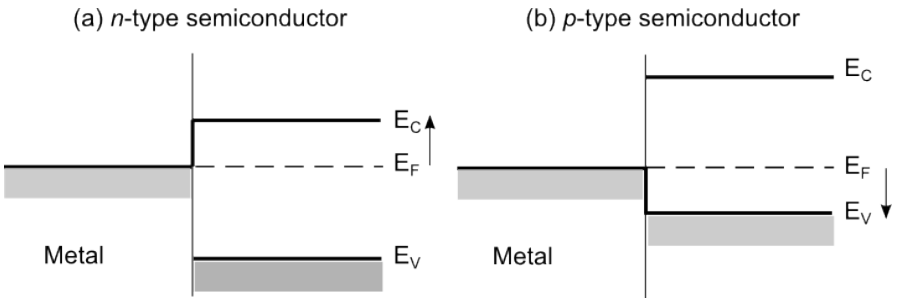


Figure 2.3: Junction between a metal and a semiconductor. Energy level diagram of (a) n-type and (b) p-type semiconductors. E_C corresponds to the energy at the bottom of the conduction band, and E_V at the top of the valence band. E_F is the Fermi level and the arrow indicates the direction at which the energy possessed by the carriers is measured [37].

In the case of an n-type semiconductor, we have 'flat band' conditions, *i.e.* the work function in the metal and semiconductor are equal and charge is not trapped at the metal/semiconductor interface. Hence, in order to excite an electron into the conduction band, an amount of energy equal to $E_C - E_F$ is necessary. A similar concept applies to holes, with the required energy being equal to $E_F - E_V$.

2.3.2 Thermoelectric couple

Let us now consider a thermoelectric couple composed of two dissimilar types of semiconductors with an intermediate metal contact. Figure 2.4 shows a single semiconductor thermoelectric couple. Here, the thermo-element is formed by two branches or legs, consisting of n- and p-type semiconductors, joined by a metallic bridge. The top part, joined by the metal, is called the *junction end*. Instead, the other part is called the *reference end* and forms a heat sink. The two legs (n- and p-type) are connected thermally in parallel and electrically in series [1, 44]. When a current I is applied to the thermocouple, with direction from n- to p-type, the device will act as a refrigerator (cooling mode), as shown in Fig. 2.4(a). Current flows from n-type to p-type material, and both carriers, electrons and holes move away from the cold junction, at a temperature T_C, toward the hot junction, at temperature T_H. Heat is absorbed from the environment and released to the heat sink. Cooling is possible since heat is transferred from the cold to the hot junction by electron transport. The heat carried is proportional to the Peltier coefficient Π and $Q = \Pi I$.

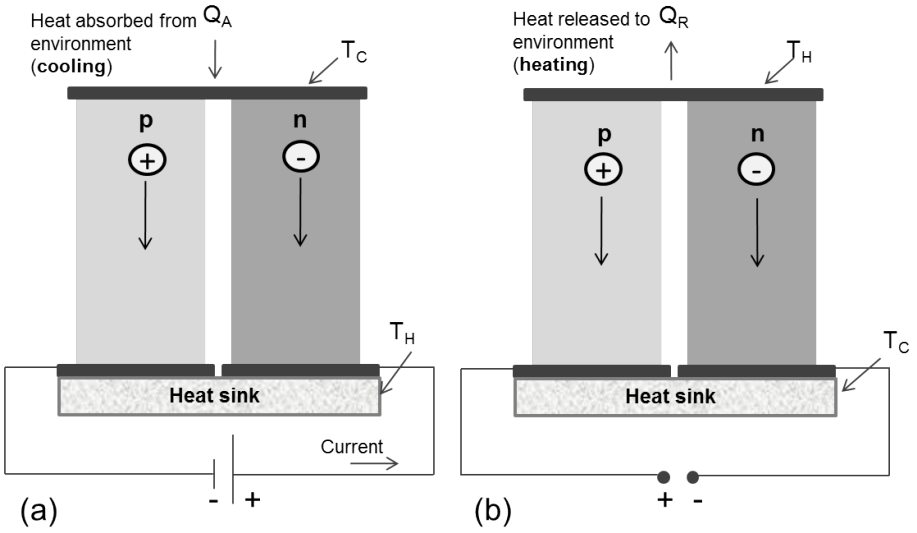


Figure 2.4: A single thermoelectric couple formed of a p- and n-type semiconductors in (a) refrigeration mode and (b) power generation. The sign of charge carrier in each leg is indicated by p (positive) and n (negative). The arrows indicate the direction of movement of charge carriers and (+) and (-), holes and electrons, respectively.

When a temperature gradient is applied to the thermocouple, a voltage drop ΔV is measured at the reference end of the thermo-element. This voltage is proportional to the Seebeck coefficient S, $\Delta V = S\Delta T$. This configuration is shown in Fig. 2.4(b), and in this case, heat is released to the environment.

2.3.3 Electronic contribution

Now, let us consider a semiconductor maintained at a temperature T and an electric field E drives through it an electric current density j_q [95]. Initially, the interaction of electrons with the crystal lattice is ignored. The charge flux of electrons can be expressed as

$$j_q = n(-e)(-\mu_e)E = ne\mu_e E \tag{2.11}$$

where n is the electron density, e the electron charge, and μ_e the electron mobility. In reference to the Fermi level E_F, the average energy carried by an electron is

$$(E_C - E_F) + \frac{3}{2}k_B T \tag{2.12}$$

with k_B the Boltzmann constant. The energy flux associated to this charge flux is then

$$j_U = n(E_C - E_F + \frac{3}{2}k_B)(-\mu_e)E \tag{2.13}$$

It is possible to define the Peltier coefficient Π by the relation $j_U = \Pi j_q$. This corresponds to the energy carried per unit charge and in the case of electrons becomes

$$\Pi_e = -(E_C - E_F + \frac{3}{2}k_B T)/e \tag{2.14}$$

Π_e is negative since the energy flux is opposite to the charge flux [95]. A similar consideration is valid for holes, where the charge flux can be written as

$$j_q = pe\mu_h E \tag{2.15}$$

where p is the hole density and μ_h the hole mobility. The energy flux is given by

$$j_U = p(E_F - E_V + \frac{3}{2}k_B T)\mu_h E \tag{2.16}$$

As a consequence, the Peltier coefficient for holes is positive and is expressed as

$$\Pi_h = (E_F - E_V + \frac{3}{2}k_B T)/e \tag{2.17}$$

From the Kelvin relation, given by Eq. 2.3, the Seebeck coefficient of electrons can be expressed as

$$S_e = \frac{\Pi_e}{T} = -\frac{k_B}{e}\left(\frac{E_C - E_F}{k_B T} + \frac{3}{2}\right) = -\frac{k_B}{e}(ln\frac{N_C}{n} + \frac{3}{2}) \tag{2.18}$$

with N_C the effective density of states in the conduction band. The right hand side of Eq. 2.18 has been obtained by substituting $E_C - E_F$ by the relation [96]

$$E_C - E_F = k_B T \cdot ln(N_C/n) \tag{2.19}$$

Here, the electron density n may be expressed as

$$n = N_C exp(-\frac{E_C - E_F}{k_B T}) \tag{2.20}$$

In a similar way, the Seebeck coefficient for holes S_h is given by

$$S_h = \frac{k_B}{e}(\frac{3}{2} + ln\frac{N_V}{p}) \tag{2.21}$$

where N_V is the effective density of states in the valence band. $E_F - E_V$ is given by [96]

$$E_F - E_V = k_B T \cdot ln(N_V/p) \tag{2.22}$$

and the hole density p may be written as

$$p = N_V exp(-\frac{E_F - E_V}{k_B T}) \tag{2.23}$$

2.3.4 Phonon contribution and the phonon drag

Here, the interaction of charge carriers with the crystal lattice is considered. In a real semiconductor, the charge carriers are continually moving and interacting with the lattice. When a temperature gradient is present, energy will flow in the atomic lattice as a form of thermal lattice waves (phonons), with net energy flow from the hot to the cold side. Phonons interact with the conduction of carriers, electrons for n-type and holes for p-type semiconductors, such that phonons can scatter or drag carriers along, from the hotter to the colder end. This carrier-phonon interaction or dragging is known as the *phonon drag* effect [89], initially observed by Frederikse, Geballe and Hull [97, 98] in Seebeck measurements of germanium. In these experiments, the *Seebeck coefficient* was much higher than predicted by theory. Herring [99] then introduced the concept of phonon drag, giving a justification for the measured values of S in germanium.

In a semiconductor with carrier density N and in the presence of an electric field E, charge carriers will gain momentum dP at the rate of $\mp NeE$ per unit volume. Here, the negative sign applies to electrons, and the positive sign to holes. This momentum may be transferred to impurities or other defects, subsequently momentum is then lost to random thermal vibration. Alternatively, momentum may be transferred to phonons, and they loose it in non-momentum-conserving collisions [42]. Hence, the momentum Δp per unit volume lost by carriers with phonons is given by

$$\Delta p = \frac{dP}{dt}\tau_p = \mp \beta N e \tau_p E \tag{2.24}$$

where τ_p is the relaxation time of phonons, and β characterises charge carriers-phonon interaction. In the *phonon drag* process, scattering of carriers occurs with low frequency phonons. The heat flux for the phonon system is given by

$$w = v^2 \Delta p \tag{2.25}$$

where v is the sound velocity, that can be approximated by an average value [42]. The *phonon drag* component of the *Peltier coefficient* Π_p can be found by the relation of heat flux to the current density and Π_p can be written as [42]

$$\Pi_p = \frac{w}{j_q} = \mp \frac{\beta v^2 \tau_p}{\mu_{e/h}} = \mp \frac{\beta v l_p}{\mu_{e/h}} \tag{2.26}$$

where $\tau_p = l_p/v$ and l_p is the mean free path of phonons participating in the *phonon drag*. By using the Kelvin relation, Eq. 2.3, the *phonon drag* component of the *Seebeck coefficient* S_p is defined as [42, 44]

$$S_p = \frac{\Pi_p}{T} = \mp \frac{\beta v l_p}{\mu_{e/h} T} \tag{2.27}$$

In a lattice, there is also an anharmonic coupling of phonons that gives rise to the interaction of phonons with each other. This anharmonic coupling becomes stronger as the temperature increases and the phonon-phonon collisions become more frequent than the phonon-electron interactions. At high temperatures, the phonon-phonon interaction or Umklapp scattering is predominant, with $\beta \approx 0$ at room temperature. As the temperature is lowered in a semiconductor, the Umklapp scattering becomes increasingly difficult, with $\beta > 0$. However, $\beta \leq 1$ and $\beta \approx 1$ at very low temperatures, where the phonon-phonon interaction is almost void. Theoretically, S_p has a dependence on the temperature as $T^{-9/2}$, since the carrier mobility varies as $T^{-3/2}$ and τ_p varies as T^{-5}. There is no dependence of Eq. 2.27 on the carrier concentration, but $|S_p|$ decreases as the carrier concentration increases. This is a consequence of the scattering of phonons with the impurities added to the doped semiconductor. Confirmation on this aspect was observed experimentally in silicon Seebeck measurements by Weber and Gmelin [84]. In Ref. [84], S_p of lightly- and heavily-doped silicon were measured and the results demonstrated that S_p is negligible in heavily-doped samples.

The *phonon drag* effect was also observed in metals, but the values of S_p do not exceed 10 μV/K. In contrast, in semiconductors S_p can reach values of several mV/K [89].

2.3.5 Total Seebeck coefficient

In section 2.3.3 and 2.3.4 it was introduced an expression of the *Seebeck coefficient* for charge carriers S_d and the expression of the *phonon drag Seebeck coefficient* S_p. Both S_d and S_p have the same sign and they add up toward the overall or total Seebeck coefficient S given by

$$S = S_d + S_p \tag{2.28}$$

where S_d is the component of S for diffusion of carriers, holes or electrons. Hence, when the phonon interaction with charge carriers is taken into consideration, Eq. 2.18 and Eq. 2.21 must account of this phonon alteration. Charge carriers have an average kinetic energy $\varepsilon_{av} \sim \frac{3}{2}k_BT$, but the average energy must be weighted to take into account the energy dependence of the relaxation time $\tau_{e/h}$ for the charge carrier scattering. The latter becomes

$$\tau_{e/h} = \tau_0 \varepsilon^r \tag{2.29}$$

where ε is the energy, and τ_0 and r are constants. The *Peltier* and *Seebeck* coefficients are depended on the impurity concentration. Hence, it is important to distinguish between the case of non-degenerate semiconductors and degenerate semiconductors. Taking scattering into account, and weighting the average kinetic energy, we can rewrite the *Seebeck coefficient* of electrons, given by Eq. 2.18, for a non-degenerate semiconductors as [44]

$$S_{d,e} = -\frac{k_B}{e}\left(\frac{E_C - E_F}{k_BT} + \left(r + \frac{5}{2}\right)\right) \tag{2.30}$$

Here, the factor $(r + 5/2)$ accounts for the reduced kinetic energy that is transported by current. The scattering factor r *is* taken to be -1/2, if electrons are scattered by phonons. When ionized-impurity scattering dominates over phonon scattering, r is taken to be 3/2 [37]. Similarly for holes, we can rewrite Eq. 2.21 as [44]

$$S_{d,h} = \frac{k_B}{e}\left(\frac{E_F - E_V}{k_BT} + \left(r + \frac{5}{2}\right)\right) \tag{2.31}$$

In the degenerate case, heavily doped semiconductors, S_d for electron and holes is given by [42]

$$S_{d,e} = \frac{\pi^2 k_B^2}{3e} T \left(\frac{r + 3/2}{E_C - E_F} \right) \tag{2.32}$$

$$S_{d,h} = -\frac{\pi^2 k_B^2}{3e} T \left(\frac{r + 3/2}{E_F - E_V} \right) \tag{2.33}$$

The letter e or h will be omitted in this thesis and we will refer to $S_{d,e}$ as 'S_d of electrons' and to $S_{d,h}$ as 'S_d of holes'.

2.4 Electronic conduction

2.4.1 Doped semiconductors

The electrical conductivity of a doped semiconductor can expressed as [96]

$$\sigma = Ne\mu_{e/h} \tag{2.34}$$

where N is the number of charge carriers per unit volume and is given by Eq. 2.20 for electrons and by Eq. 2.23 for holes. The effective density of states in the conduction band N_C of Eq. 2.20 is given by [96]

$$N_C = 2 \left(\frac{2\pi m_e^* k_B T}{h^2} \right)^{3/2} M_C \tag{2.35}$$

where h is the Planck's constant, M_C is the number of equivalent minima in the conduction band, and m_e^* the effective density-of-states mass for electrons [96]

$$m_e^* = (m_1^* m_2^* m_3^*)^{1/3} \tag{2.36}$$

m_1^*, m_2^*, m_3^* are the effective masses along the principal axes of energy surfaces. In the case of silicon, $m_e^* = (m_l^* m_t^{*2})^{1/3}$, where m_l^* is the longitudinal effective mass and m_t^* is the transverse effective mass for electrons [96]. The effective density of states in the valence band N_V of Eq. 2.23 is given by [96]

$$N_V = 2\left(\frac{2\pi m_h^* k_B T}{h^2}\right)^{3/2} \tag{2.37}$$

where m_h^* is the density-of-state effective mass of the valence band:

$$m_h^* = (m_{lh}^{*3/2} + m_{hh}^{*3/2})^{2/3} \tag{2.38}$$

with the subscripts *lh* and *hh* corresponding to light and heavy hole masses.

Moreover, carriers also contribute to the conduction of heat. This is added to the heat that is carried by *phonons* and the total κ is given by

$$\kappa = \kappa_e + \kappa_L \tag{2.39}$$

κ_e is related to σ by the Wiedemann-Franz law [29, 37]

$$\kappa_e = L\sigma T \tag{2.40}$$

where L is known as the Lorenz factor. In a similar case to S, we must distinguish between the non-degenerate and degenerate case. In the non-degenerate approximation, the Lorenz factor is given by

$$L = \left(\frac{k_B}{e}\right)^2 \left(\frac{5}{2} + r\right) \tag{2.41}$$

the weighting factor is the same as that used for electrons in section 2.3.5. In the degenerate case, the expression for L is given by [42]

$$L = \frac{\pi^2}{3}\left(\frac{k_B}{e}\right)^2 \tag{2.42}$$

Here, the Lorentz number is a constant, this is the case of all metals. The Wiedemann-Franz law, Eq. 2.40, is often written as $\kappa_e/\sigma = LT$, *i.e.* the ratio of thermal to electrical conductivity at the same temperature for all metals is the same, with $L = 2.4 \times 10^{-4}$ $\mathrm{J^2K^{-2}C^{-2}}$ [1].

2.4.2 Intrinsic conduction

Let us now consider the situation when more than one carrier contributes to the transport processes. This is the case of intrinsic or mixed conduction, when both electrons in the

conduction band and holes in the valence band contribute, or when there are comparable type of carriers of the same type, *i.e.* light and heavy holes. Here, the contribution to the electric current density j_q is expressed as [42]

$$j_{q1} = \sigma_1 \left(E - S_1 \frac{\partial T}{\partial x} \right), \qquad j_{q2} = \sigma_2 \left(E - S_2 \frac{\partial T}{\partial x} \right) \tag{2.43}$$

where σ_1 and σ_2 correspond to the conductivity of carrier type *1* and carrier type *2*, with x the direction of flow of charge carriers. When zero temperature gradient is present, then the total current density j_q is expressed as

$$j_q = j_{q1} + j_{q2} = (\sigma_1 + \sigma_2)E \tag{2.44}$$

with the electrical conductivity $\sigma = \sigma_1 + \sigma_2$. When j_{q1} and j_{q2} are equal and opposite, then [42]

$$(\sigma_1 + \sigma_2)E = (S_1\sigma_1 + S_2\sigma_2)\frac{\partial T}{\partial x} \tag{2.45}$$

Hence, S is given by [37]

$$S = \frac{S_1\sigma_1 + S_2\sigma_2}{\sigma} \tag{2.46}$$

S_1 and S_2 can be calculated using Eq. 2.18 and Eq. 2.21, depending on the type of the carrier. σ of a mixed semiconductor is defined as follows [37]

$$\sigma = e(n\mu_e + p\mu_h) \tag{2.47}$$

Let us now examine the heat flux densities associated with the two carrier types,

$$w_1 = S_1 T j_{q1} - \kappa_{e,1}\frac{\partial T}{\partial x}, \qquad w_2 = S_2 T j_{q2} - \kappa_{e,2}\frac{\partial T}{\partial x} \tag{2.48}$$

In the absence of an electric current, i_1 and i_2 must be equal and opposite, then [42]

$$j_{q1} = -j_{q2} = \frac{\sigma_1\sigma_2}{\sigma_1 + \sigma_2}(S_2 - S_1)\frac{\partial T}{\partial x} \tag{2.49}$$

Substituting Eq. 2.49 into Eq. 2.48 and calculating the total heat flux [42]

$$w = w_1 + w_2 = -\left[\kappa_{e,1} + \kappa_{e,2} + \frac{\sigma_1\sigma_2}{\sigma_1 + \sigma_2}(S_2 - S_1)^2 T\right]\frac{\partial T}{\partial x} \tag{2.50}$$

with

$$\kappa_e = \kappa_{e,1} + \kappa_{e,2} + \frac{\sigma_1\sigma_2}{\sigma_1+\sigma_2}(S_2 - S_1)^2 T \tag{2.51}$$

Hence, κ_e is greater than the contributions of $\kappa_{e,1}+\kappa_{e,2}$ for an intrinsic semiconductor. The difference $S_2 - S_1$ is maximum when the carriers are both electrons and holes, respectively. The additional contribution in Eq. 2.51 is known as the bipolar thermo-diffusion effect.

2.4.3 Diffusion Seebeck coefficient in lightly doped silicon

Let us now consider an n-type silicon and investigate the dependence of the Seebeck coefficient of electrons S_d as a function of temperature and scattering factor r. S_d is expressed as

$$S_d = -\frac{k_B}{e}\left(\frac{E_C - E_F}{k_B T} + \left(r + \frac{5}{2}\right)\right) \tag{2.52}$$

The Fermi energy E_F can then be calculated by using the neutrality condition, as the number of ionized donors has to be equal to the electron concentration n. Here, n is expressed as $n = N_C exp(-(E_C - E_F)/k_B T)$. Hence, it follows [96]

$$n_d\left(1 - \left(\frac{1}{2}exp\left(\frac{E_D - E_F}{k_B T}\right) + 1\right)^{-1}\right) = N_C exp\frac{E_F - E_C}{k_B T} \tag{2.53}$$

Here, n_d is the ionised donor concentration, $E_D = 0.045$ eV the donor (phosphorous) energy and N_C is given by Eq. 2.35. $E_F - E_C$ is calculated using Eq. 2.53, and then substituted in Eq. 2.52. It is then possible to plot S_d as a function of temperature. Equations were solved using Matlab. Figure 2.5 shows S_d for low to moderate doping levels, assuming that electrons were scattered by phonons, *i.e.* r = -0.5, as for the case of low-doped materials. S_d decreases as the doping level increases, this is due to an increase in the scattering of electrons with the impurities. It is also important to note that for very low doped samples, *i.e.* 10^{12} cm^{-3}, S_d reaches a minimum at very low temperature, followed by a sharp increase as T further decreases. As n_d increases the minimum of S_d shifts slightly toward higher temperature to then disappear for $n_d = 10^{16}$ cm^{-3}. Figure 2.6 shows the dependence of S_d on the parameter r. Fig. 2.6(a) shows S_d for $n_d = 10^{14}$ cm^{-3} and Fig. 2.6(b) S_d for $n_d = 10^{16}$ cm^{-3}. Here, the factor r changes from -1/2 to 3/2. Although in lightly doped samples, r should be equal to -1/2, this might not be the case when imperfections are present in the crystal. S_d in Fig. 2.6(a)-(b) increases as r increases. This reflects the

physical situation that more electrons contribute to S_d for more positive values of r, due to less scattering of electrons with phonons.

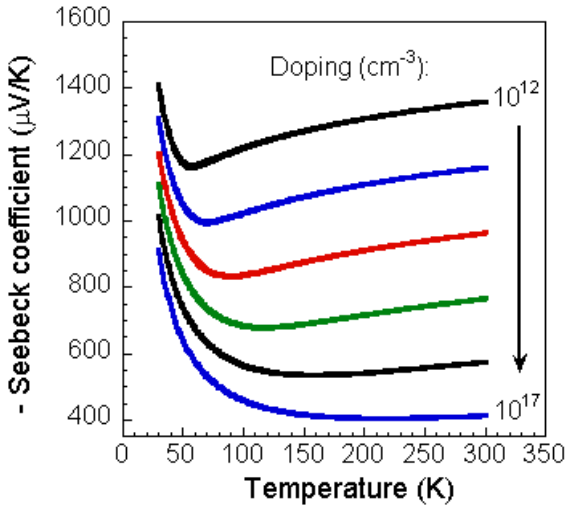


Figure 2.5: Temperature dependence of S_e for low to moderate doping levels, 10^{12} - 10^{17} cm^{-3}, and a scattering parameter r = - 1/2.

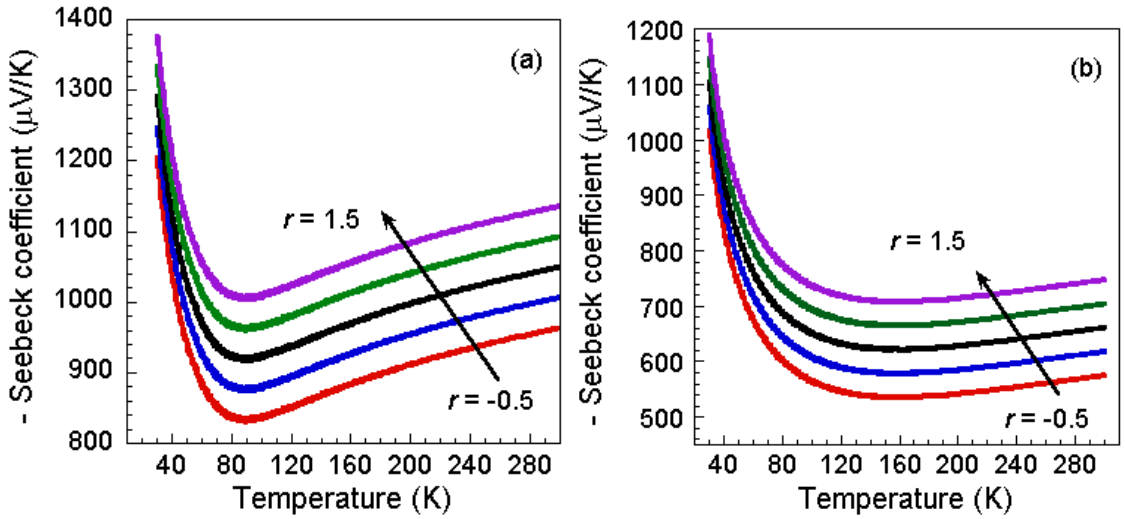


Figure 2.6: S_d vs. T for different values of the scattering parameter r. Doping level of (a) 10^{14} cm^{-3} and (b) 10^{16} cm^{-3}. r varies in the range (-0.5, 1.5), with 0.5 steps.

2.5 Thermal conductivity

Thermal conductivity $\kappa = \kappa_e + \kappa_L$ is the sum of electronic κ_e and lattice κ_L contributions. κ_L arises from the conduction of heat by the lattice vibration of the crystal. In metals,

κ_e is the sole contribution to the thermal conductivity, while in insulators κ_L is the main contributor and is also significant in semiconductors. The expression for κ_L is the following [37]

$$\kappa_L = \frac{1}{3} C_v v l \tag{2.54}$$

where l is the mean free path of phonons, or the average distance that they travel before being scattered. C_v is the specific heat per unit volume, and v the velocity of sound. In a perfect crystal, vibrations are completely harmonic and l must be infinite. In a real crystal, phonons are scattered by various mechanisms and the vibrations are anharmonic with l being finite [29, 37]. At high temperatures, the predominant scattering mechanism is phonon-phonon interaction. In a crystal, the most important processes involve the exchange of energy between three normal modes. Annihilation of one phonon leads to the formation of two others, or two phonons disappear to create a third. These processes can be distinguished in:

- *Normal* or N-processes, where momentum is conserved. These processes do not contribute to the thermal conduction, but they must be taken into account since they contribute to the change in the phonon distribution between the various modes.
- *Umpklapp* or U-processes, momentum is not conserved. These contribute to κ_L.

The mean free path of phonons l is determined by the anharmonicity of the vibrations and their intensity. Here, the intensity of the vibrations is proportional to the temperature, l and κ_L are then inversely proportional to the temperature. Fig. 2.7 shows the behaviour of $C_v/\mathbb{N}k_B$ as a function of T/θ_D, as predicted by the Debye's theory. $\mathbb{N}$ is the number of phonon modes, θ_D is the Debye's temperature and is different for each material. At the absolute temperature of 0 K, C_v is zero. At temperatures T smaller than θ_D, C_v follows a T^3 law. As the temperature approaches θ_D, C_v approaches a limiting value of $3\mathbb{N}k_B$ [42]. Experimental values of C_v closely follow the behaviour of the curve shown in Fig. 2.7.

The theoretical temperature dependence of κ_L of a finite crystal with no imperfections is shown in Fig. 2.8. At high temperatures κ_L follows a $1/T$ law. As the temperature is lowered below θ_D, κ_L rises to a maximum value. Beyond this value, κ_L is then limited by the temperature dependence of the specific heat, *i.e.* T^3 law. In the low temperature range, boundary scattering is predominant and l mainly depends on the size of the sample. As T approaches 0 K, C_v becomes zero and so does κ_L [29].

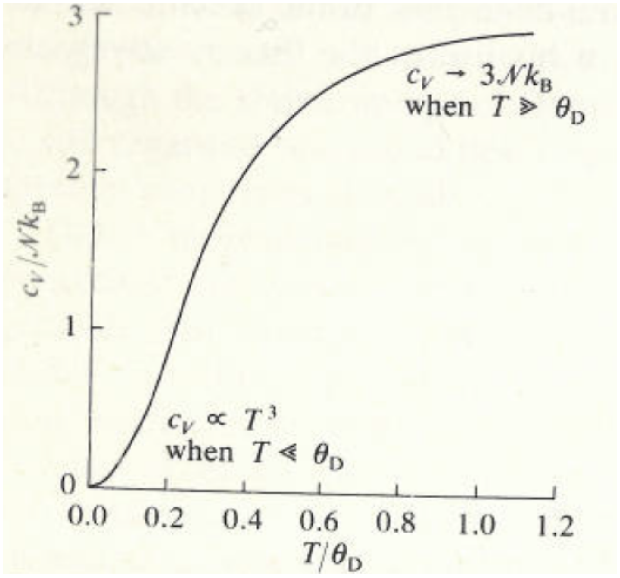


Figure 2.7: Temperature dependence of the specific heat according to Debye's theory [42].

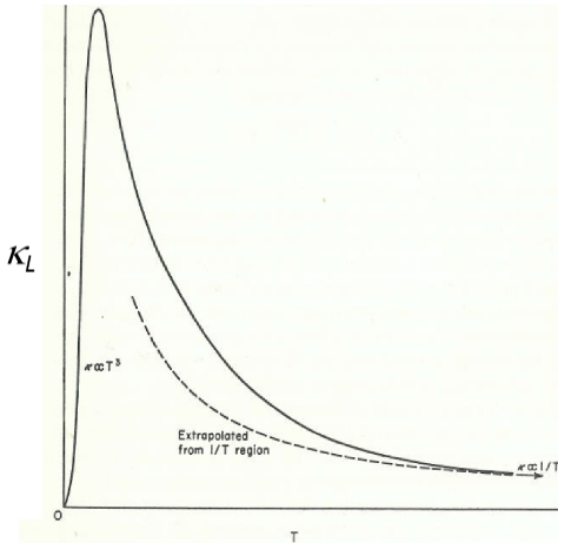


Figure 2.8: Temperature dependence of the lattice thermal conductivity for a finite perfect crystal. Figure taken from Ref. [29].

2.6 Transport coefficients using Boltzmann transport equation

The description given in this section follows the derivation given in Ref. [44]. Here, the Boltzmann equation of carriers is considered as the main contributor. In a real crystal, the transport of electrons is limited by scattering mechanisms that alter their transport. This leads to the definition of mean free path or *relaxation time* τ_e between collisions. When the system of electrons is disturbed from the equilibrium condition f_0 to f, the system then relaxes following the equation

$$\left(\frac{\mathrm{df}(E)}{\mathrm{dt}}\right)_{scatter} = -\frac{\mathrm{f}(E) - \mathrm{f}_0(E)}{\tau_e} \tag{2.55}$$

This is only valid when $|\mathrm{f}\text{-}\mathrm{f}_0| \ll \mathrm{f}_0$, where f_0 is the Fermi distribution function and indicates that the probability of a particular state being filled is given by

$$\mathrm{f}_0(E) = \left[\exp\left(\frac{E-\varphi}{\kappa_B T}\right) + 1\right]^{-1} \tag{2.56}$$

where T is the temperature and φ is the Fermi energy offset measured from the appropriate band edge and in the appropriate direction, *i.e.* $\varphi = E_F - E_C$ for electrons, or $\varphi = E_V - E_F$ for holes. The value of φ is given by

$$\int_0^\infty \mathrm{f}_0(E)\mathrm{g}(E)\mathrm{d}E = n \tag{2.57}$$

with n the total number of free electrons per unit volume. Here, $\mathrm{g}(E)$ represents the density of states, *i.e.* the number of electron states permitted per unit volume in the energy interval (E, E + $\mathrm{d}E$) and is given by

$$\mathrm{g}(E)\mathrm{d}E = \frac{4\pi(2m)^{3/2}E^{1/2}\mathrm{d}E}{h^3} \tag{2.58}$$

with m the mass of free electrons and h Planck's constant.

In addition, the relaxation time of electrons can be expressed as

$$\tau_e = \tau_0 E^r \tag{2.59}$$

where τ_0 and r are constants. Scattering of charge carriers with phonons is assumed to do not lead to any change in the distribution of carriers. Taking into account the dependence of the Fermi distribution function on the electric field and the temperature gradient, Eq. 2.55 can be written as:

$$\frac{\mathrm{f}(E) - \mathrm{f}_0(E)}{\tau_e} = u\frac{\partial \mathrm{f}_0(E)}{\partial E}\left(\frac{\partial \varphi}{\partial x} + \frac{E-\varphi}{T}\frac{\partial T}{\partial x}\right) \tag{2.60}$$

where u is the electron velocity along the x-axis. In the presence of a perturbance, the carriers, with charge $\mp e$, move in the x direction with velocity u. The minus sign corresponds to electrons and the plus sign to holes. The electric current density j associated to the movement of charge carriers can be written as

$$j = \mp \int_0^\infty eu\mathrm{f}(E)\mathrm{g}(E)\mathrm{d}E \tag{2.61}$$

where $\mathrm{f}(E)\mathrm{g}(E)\mathrm{d}E$ is the number of charge carriers per unit volume in the energy range (E, E + $\mathrm{d}E$) and $\mathrm{g}(E)$ is given by Eq. 2.58. In a similar way, we can express the rate of heat flow w per unit cross-section area as

$$w = \int_0^\infty u(E-\varphi)\mathrm{f}(E)\mathrm{g}(E)\mathrm{d}E \tag{2.62}$$

with $(E - \varphi)$ total energy transported by a carrier. In Eq. 2.61 and Eq. 2.62, f can be replaced by (f - f_0), given by Eq. 2.60, since there is no heat or charge flow when f = f_0. Furthermore, considering an isotropic electron gas, in the thermoelectric case, thermal velocity of carriers is much greater than drift velocity and u can be expressed as

$$u^2 = \frac{2E}{3m^*} \tag{2.63}$$

with m^* the effective mass

$$\frac{1}{m^*} = \frac{1}{\hbar}\frac{\mathrm{d}^2E}{\mathrm{d}k^2} \tag{2.64}$$

Here, k is the wave vector. Substituting u^2 into Eq. 2.61 and Eq. 2.62 and considering that $\partial T/\partial x = 0$, it is possible to calculate electrical conductivity σ [44]

$$\sigma = \frac{j}{\varepsilon} = -\frac{2e^2}{3m^*}\int_0^\infty \mathrm{g}(E)\tau_e \frac{\partial \mathrm{f}_0}{\partial E}\mathrm{d}E \tag{2.65}$$

where the electric field $\varepsilon = \pm(\partial\varphi/\partial x)e^{-1}$. Considering Eq. 2.61, where f has been replaced by f-f_0 (given by Eq. 2.60), then the Seebeck coefficient S can be calculated by $(\partial\varphi/\partial x)(e(\partial T/\partial x))^{-1}$, as in this case the electric current is zero. Hence, S can be expressed as

$$S = \pm\frac{1}{eT}\left[\varphi - \frac{\int_0^\infty \mathrm{g}(E)\tau_e E^2 \frac{\partial \mathrm{f}_0}{\partial E}\mathrm{d}E}{\int_0^\infty \mathrm{g}(E)\tau_e E \frac{\partial \mathrm{f}_0}{\partial E}\mathrm{d}E}\right] \tag{2.66}$$

In a similar way, the electron thermal conductivity κ_e is given by $-w(\partial T/\partial x)^{-1}$ and

$$\kappa_e = \pm\frac{2}{3m^*T}\left[\frac{\left(\int_0^\infty \mathrm{g}(E)\tau_e E^2 \frac{\partial \mathrm{f}_0}{\partial E}\mathrm{d}E\right)^2}{\int_0^\infty \mathrm{g}(E)\tau_e E \frac{\partial \mathrm{f}_0}{\partial E}\mathrm{d}E} - \int_0^\infty \mathrm{g}(E)\tau_e E^3 \frac{\partial \mathrm{f}_0}{\partial E}\mathrm{d}E\right] \tag{2.67}$$

The Peltier coefficient is then found by using the Kelvin relationship, Eq. 2.3, or as the ratio w/i. For simplicity, the integral in Eq. 2.66 and Eq. 2.67 can be written in a more general form

$$K_s = -\frac{2T}{3m^*}\int_0^\infty \mathrm{g}(E)\tau_e E^{s+1}\frac{\partial \mathrm{f}_0}{\partial E}\mathrm{d}E \tag{2.68}$$

We substitute g, τ_e in terms of m^*, r and τ_0 by using Eq. 2.58 and Eq. 2.59. We also define $\zeta = E/k_BT$ as the reduced energy and substitute it into Eq. 2.68. Now, integration Eq. 2.68 by parts gives

$$K_s = \frac{8\pi}{3}\left(\frac{2}{h^2}\right)^{3/2}(m^*)^{1/2}T\tau_0\left(s + r + \frac{3}{2}\right)(k_BT)^{s+r+3/2}\,\mathrm{F}_{s+r+1/2}(\zeta) \tag{2.69}$$

where $\mathrm{F}_n(\zeta)$ is expressed as

$$\mathrm{F}_n(\zeta) = \int_0^\infty \zeta^n \mathrm{f}_0(\zeta)\mathrm{d}\zeta \tag{2.70}$$

with n = s + r + 1/2. Numerical solutions of F_n are known as Fermi-Dirac integrals [44]. Hence, electrical conductivity can now be expressed in a more simplified form:

$$\sigma = \frac{e^2}{T}K_0, \tag{2.71}$$

It is then possible to rewrite S as

$$S = \pm\frac{1}{eT}\left(E_F - \frac{K_1}{K_2}\right) \tag{2.72}$$

Likewise, the electron thermal conductivity κ_e is given by

$$\kappa_e = \frac{1}{T^2}\left(K_2 - \frac{K_1^2}{K_0}\right) \tag{2.73}$$

These equations can be further simplified, when φ is much greater or much less than zero, by using the approximation of the Fermi distribution function.

Non-degenerate approximation

When $\varphi/k_BT \ll 0$, *i.e.* the Fermi level lies within the forbidden gap and away from the band edge. This is the non-degenerate case and the Fermi-Dirac integrals are expressed as

$$\mathrm{F}_n(\eta) = \exp(\eta)\int_0^\infty \zeta^n \exp(-\zeta)\mathrm{d}\zeta = \exp(\eta)\Gamma(n+1) \tag{2.74}$$

where $\eta = \varphi/k_BT$ and Γ satisfies the property $\Gamma(n+1) = n\Gamma(n)$ and $\Gamma(1/2) = \pi^{1/2}$. It is possible to express the transport integral K_s in terms of Γ

$$K_s = \frac{8\pi}{3}\left(\frac{2}{h^2}\right)^{3/2}(m^*)^{1/2}T\tau_0\,(k_BT)^{s+r+3/2}\,\Gamma\left(s+r+\frac{5}{2}\right)\exp(\eta) \tag{2.75}$$

It follows that the electrical conductivity of a non-degenerate semiconductor is given by

$$\sigma = \frac{8\pi e^2}{3}\left(\frac{2}{h^2}\right)^{3/2}(m^*)^{1/2}T\tau_0\,(k_BT)^{r+3/2}\,\Gamma\left(r+\frac{5}{2}\right)\exp(\eta) = ne\mu \tag{2.76}$$

with n the concentration and is expressed as

$$n = \int_0^\infty \mathrm{f}(E)\mathrm{g}(E)\mathrm{d}E = 2\left(\frac{2\pi m^* k_BT}{h^2}\right)^{3/2}\exp(\eta) \tag{2.77}$$

with μ mobility and is given by

$$\mu = \frac{4}{3\pi^{1/2}}\Gamma\left(r+\frac{5}{2}\right)\frac{e\tau_0(k_BT)^r}{m^*} \tag{2.78}$$

From Eq. 2.72 and Eq. 2.75, the Seebeck coefficient of a non-degenerate semiconductor is given by

$$S = \pm\frac{k_B}{e}\left(\eta - \left(r + \frac{5}{2}\right)\right) \tag{2.79}$$

where -η may be considered as the reduced potential energy and $(r + 5/2)$ as the reduced kinetic energy transported by current. The electron thermal conductivity κ_e is conventionally expressed through the Lorenz number $L = \kappa_e/\sigma T$. Using Eq. 2.71 and Eq. 2.73, L can then be written as

$$L = \frac{1}{e^2T^2}\left(\frac{K_2}{K_0} - \frac{K_1^2}{K_0^2}\right) \tag{2.80}$$

and in the non-degenerate case:

$$L = \left(\frac{k_B}{e}\right)^2\left(r + \frac{5}{2}\right) \tag{2.81}$$

Degenerate approximation

In the degenerate case $\varphi/k_BT \gg 0$ and the Fermi-Dirac integrals are given by [44]

$$\mathrm{F}_n(\eta) = \frac{\eta^{n+1}}{n+1} + n\eta^{n-1}\frac{\pi^2}{6} + n(n-1)(n-2)\eta^{n-3}\frac{7\pi^4}{360} + ... \tag{2.82}$$

Taking into account the first term of Eq. 2.82, it is possible to calculate the electrical conductivity of a degenerate semiconductor [44]

$$\sigma = \frac{8\pi e^2}{3}\left(\frac{2}{h^2}\right)^{3/2}(m^*)^{1/2}\tau_0 E_F^{r+3/2}\Gamma\left(r + \frac{5}{2}\right)\exp(\eta) = ne\mu \tag{2.83}$$

Whereas, the Seebeck coefficient of a degenerate conductor is obtained by considering the first two terms of Eq. 2.82

$$S = \mp\frac{\pi^2}{3}\frac{k_B}{e}\frac{\left(r + \frac{3}{2}\right)}{\eta} \tag{2.84}$$

The first two terms of Eq. 2.82 must be considered for the Lorenz number in the degenerate case

$$L = \frac{\pi^2}{3}\left(\frac{k_B}{e}\right)^2 \tag{2.85}$$

2.7 Characterization of ZT in semiconductors

In order to calculate the figure of merit $ZT = S^2\sigma T/\kappa$, reliable and accurate measurements of their electrical and thermoelectric properties have to be performed. Ideally, one should estimate simultaneously all the parameters (κ, σ and S). These measurements are important in order to optimise the TE performances of the material. The techniques used to measure the TE parameters are described below.

2.7.1 Seebeck coefficient measurement

In principle, S is the simplest quantity to determine, but errors associated in the correct determination of the temperature gradient can lead to a wrong value or sign of S. Fig. 2.9 shows a schematic diagram of the experimental apparatus. The sample is sandwiched between a bottom (cold) Cu heat sink (temperature T_1) and a top Cu 'hot' reservoir (temperature T_2), allowing measurement of the temperature difference $\Delta T = T_2 - T_1$. The open circuit voltage and the temperature differences can be measured either by soldering the ends of the Cu blocks to the sample, or by applying pressure in order to press the heat sink and the hot reservoir against the bare faces of the sample [42].

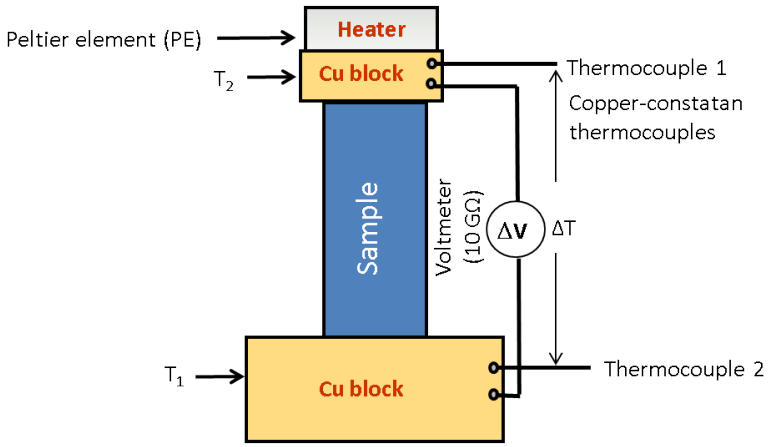


Figure 2.9: Apparatus for measurement of S, σ and κ. A heater is attached to a small copper plate, which is welded to the top of the sample. The bottom copper block acts as a heat sink.

Despite the interface resistance, in the latter configuration given smooth Cu/Si interfaces, the majority of the temperature drops within the thermoelectric material. Here, the temperature gradient is higher near the interfaces and the regions near the end of

the sample contribute more to the Seebeck coefficient. The pressure contact configuration should not be used if the ends of the sample have been metalised. In this case, a significant portion of the temperature difference can occur outside the thermoelectric material, hence within the metal [42]. This would lead to an incorrect measurement of S. Furthermore, the measured S includes both the sample contribution and the electrical lead contribution. However, the lead contribution is usually of the order of few μV/K, hence it can be neglected.

2.7.2 Thermal conductivity measurements

High accuracy in the measurement of thermal conductivity is very difficult. Radiation loss or gain between the surroundings and the sample, convection in a gas environment, and conduction through the lead wires and the gaseous medium can lead to substantial errors. Generally, the '*steady state technique*' is the preferred method to measure κ [30, 84][1]. However, this method is very slow and cumbersome due to the time required to reach equilibrium. Hence, a dynamic or transient technique is often preferred. In our case, we will use the dynamic method, first used and explained by Ioffe [29, 42]. The apparatus is illustrated in Fig. 2.10, in this case no electrical contacts are used, since no voltage signal is needed, and a mica sheet is utilised for the purpose of electrical insulation. In order to minimise heat losses, experiments are measured in a moderate vacuum ($10^{-4} - 10^{-5}$ torr), using a cryostat.

At the start of the experiment, the whole apparatus is at ambient temperature, 300 K. Then the temperature of the lower Cu block is reduced and the temperature difference of the two Cu blocks is monitored as a function of time. The upper block loses heat at the rate of

$$Q = -\frac{C_2 dT_2}{dt} \tag{2.86}$$

where C_2 is the thermal capacity of the upper Cu block and t represents time. In the ideal case, the rate of heat loss Q must be equal to [42]

$$Q = \kappa \left(T_2 - T_1\right) \frac{A}{L} \tag{2.87}$$

[1] Chapter 23 of Ref. [30]

with L the length of the specimen. It follows that

$$\kappa = -\frac{C_2 + \frac{1}{3}C}{T_2 - T_1}\frac{dT_2}{dt}\frac{L}{A} \tag{2.88}$$

where $\frac{1}{3}C$ accounts the part of the heat entering the lower block that is originated within the specimen and C is the heat capacity of the sample.

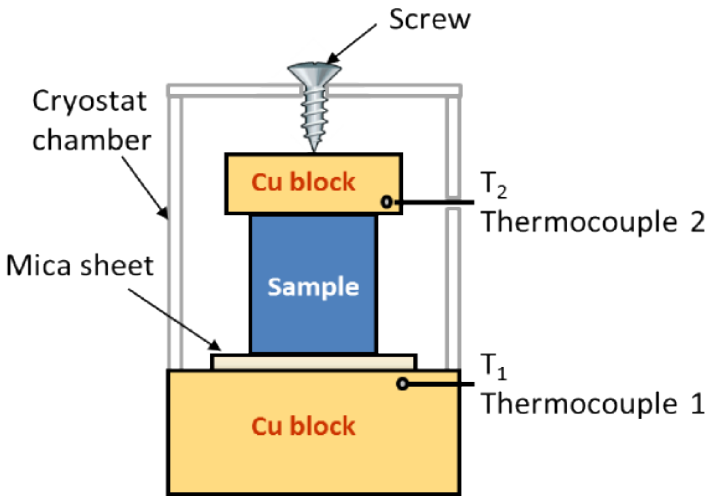


Figure 2.10: Apparatus used to measure κ with the dynamic technique.

2.7.3 Electrical conductivity

Electrical conductivity measurements can in principle be straightforward. However, contact resistance, oxide layers and deterioration of contacts may become limiting factors. In a TE material, a ΔT is generated as a consequence of current I passing through the material. This leads to the presence of a thermal voltage, $V_{TE} = S\Delta T$, that is added to the sample voltage $V_S = IR$. The total voltage V_T measured across the sample is now $V_T = IR + S\Delta T$. To avoid V_{TE} generation, a fast measurement, of the order of few seconds ($\sim$ 2–3 s), must be performed. It is also important to determine accurately the sample dimension, as the resistivity is given by [100]

$$\rho = \frac{1}{\sigma} = \frac{AR}{L_0} \tag{2.89}$$

where A is the cross section of the sample, R is resistance and L_0 the sample distance between the measuring leads. Good electrical contacts are necessary to avoid large contact resistances that may lead to Joule heating. Furthermore, to prevent errors in measurement

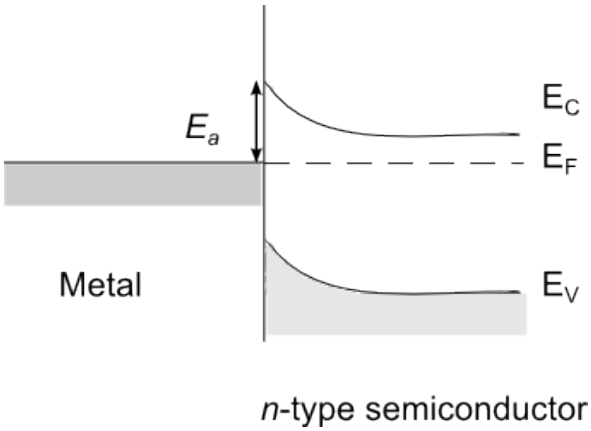


Figure 2.11: Band diagram when a Schottky contact is present between the metal-semiconductor junction in equilibrium conditions. E_a is the barrier height or activation energy.

due to oxide layers, leading to errors in measurements of A and L_0, samples can be etched in HF to determine A and L_0 accurately. In order to determine the conductivity, a four point probe method should be utilised. Here, two of the terminals are used to inject current into the sample, with the other two terminals functioning as voltage probes. This method eliminates the contact resistance on the voltage measurement. However, this method can be utilised when $L - L_0 \geq 2w$, where L is the total length of the sample, L_0 the distance between the voltage terminals and w the thickness of the sample. In our case, as we measure samples with dimensions $\approx 0.85 \times 0.85$ cm^{-2} and $L_0 \approx 0.4$ cm, the difference $L - L_0 \geq 2w$ is not satisfied. Hence, we use the two terminal apparatus shown in Fig. 2.9 to determine the conductance G of the samples with ohmic contacts. G is given by [96]

$$G = \frac{dI}{dV} \tag{2.90}$$

It is then possible to calculate the activation energy for the conduction mechanism. Here, the activation energy may correspond to the barrier height E_a formed by upward band bending when there is a Schottky contact at the metal-semiconductor interface, see Fig. 2.11. The barrier height can then be calculated by using the equation below [96]

$$G = G_0 exp(-\frac{eE_a}{k_B T}) \tag{2.91}$$

where G_0 is a constant. Using the logarithm of Eq. 2.91, it follows

$$ln(G) = ln(G_0) - \frac{eE_a}{k_B T} \tag{2.92}$$

Using Arrhenius plots, where ln G is plotted vs. $1/T$, the slope of the plots can be used to extract the barriers height, and obtain information on the contacts of the samples. If E_a is negligible then contacts at the metal-semiconductor interfaces may be considered as Ohmic.

2.8 Harman technique

The Harman technique or *Z-meter* [74, 101] is a direct method for determining the figure of merit ZT. If we consider a sample with $\Delta T = 0$ and current $I = 0$, then the sample voltage $V_S = 0$. When a current I is applied, the voltage increases by a quantity $V_{IR} = IR_S$, where R_S is the sample resistance. Considering that we are dealing with a TE material, a ΔT will arise due to the Peltier effect, $Q_P = SIT$, and also a voltage V_{TE} will add up to the existing V_{IR}. At steady state or adiabatic conditions, the heat associated with the Peltier effect will be equal to the heat of the thermal conduction [30]:

$$SIT = \frac{\kappa A \Delta T}{L} \tag{2.93}$$

Let us consider ZT, we divide and multiply it by a quantity $A\Delta T/\mathrm{L}$

$$ZT = \frac{S^2 T}{\rho\kappa} = \frac{S^2 T}{\rho\kappa A\frac{\Delta T}{L}} A\frac{\Delta T}{L} = \frac{S^2 T}{\rho SIT} A\frac{\Delta T}{L} = \frac{S\Delta T}{\rho\frac{L}{A}I} = \frac{S\Delta T}{RI} \tag{2.94}$$

where $R = \rho L/A$ is the electrical resistance. In steady state conditions, the overall voltage is $V_A = V_{TE} + V_{IR}$ and equation 2.94 can be related to V_A by the following equation

$$ZT \quad = \frac{S\Delta T}{RI} \quad = \frac{V_{TE}}{V_{IR}} = \frac{V_A - V_{IR}}{V_{IR}} = \frac{V_A}{V_{IR}} - 1 \tag{2.95}$$

where $V_{TE} = S\Delta T$ is the thermoelectric voltage. We can express equation 2.93 as

$$I = \kappa\frac{A}{STL}\Delta T \tag{2.96}$$

Then at a constant temperature, $I = \kappa C_0 \Delta T$, where C_0 is a constant at a given T. The thermal conductivity is then given by the slope of I vs. ΔT . The value calculated from

this technique should be compared to the ZT calculated by measurement of each of the individual parameters of Eq. 1.1. A relationship can be derived between ZT, the adiabatic voltage $V_A = V_{IR} + V_{TE}$ and the sample voltage V_{IR}

$$ZT = \frac{V_A}{V_{IR}} - 1 = \frac{S^2 \sigma T}{\kappa} \tag{2.97}$$

This relationship is a good approximation of ZT, but assumes an ideal situation, and generally samples with $ZT > 0.1$ should be considered.

3 Fabrication of silicon nanowires

In recent years, nanostructures have become increasingly important because of their novel physical properties arising as a consequence of their low-dimensionality. Silicon, the basis of large-scale integrated circuits, has further attracted attention in its nanostructure form for applications such as optoelectronics and thermoelectricity. The approaches developed to fabricate nanostructures can be divided into top-down and bottom-up. In top-down approaches, bulk material is gradually etched to lower dimensions and desired shape. Bottom-up approaches exploit chemical and mechanical properties of molecules or nanoparticles to self organize or self assemble nanostructures.

3.1 Introduction

The most common methods among the top-down approach include electron beam lithography and optical lithography [102]. In the electron beam lithography, a nanowire (NW) pattern with a diameter down to 10 nm can now be defined using a focused electron beam. Optical lithography utilises a mask to define the desired NW pattern, a resist is then applied to the mask substrate and light is used to develop the resist.

In the bottom-up approach, the most common methods are vapour-liquid-solid (VLS) growth and, more recently, metal assisted chemical etching (MACE) [103]. In the VLS method, a liquid-phase metal nanoparticle catalyst is used to form the NW. Silicon precipitation occurs in the nanoparticle, followed subsequently by NW growth [104]. The diameter of the nanostructures is a function of the diameter of the alloy droplet at its tip.

In recent years, there has been interest in the MACE process for the following reasons:

- Simple and low-cost process. It allows control over different parameters, such as diameter, length, orientation, doping type, doping level, and cross-sectional shape.
- Enables control over the orientation of the nanostructure relative to the substrate.

The development of different etching methods have permitted control over the etching direction, enabling etching of vertically aligned Si nanowires along (100) direction and non (100) direction.

- The crystalline quality is high and the nanowires do not contain crystallographic defects.
- No strong limitation on the length of the nanowires.

A disadvantage is given by the rough surface of the nanowires. However, this may represent an advantage when applied to thermoelectricity, due to increased surface scattering of phonons leading to a reduced κ [86, 105].

3.2 Fabrication process

3.2.1 Metal deposition and etching mechanism: a review

The fabrication of our SiNWs uses MACE, based on a two step process. In the first step, metal is deposited by electroless deposition or galvanic exchange. Then, NW etching or formation is achieved in a solution of HF and H_2O_2. Noble metal ions are reduced at the Si surface through a cathodic process and oxidation of Si atoms at the Si surface occurs, *i.e.* an anodic reaction. Typically, the metals used consist of Ag in a solution form ($AgNO_3$), Au and Pt. As the electrochemical potential of noble metals compared to Si is more positive, a galvanic displacement reaction occurs in Si by injection of holes into the valence band, see Fig. 3.1(a). Metal ions are further reduced on the Si surface by electrons provided by the Si-Si bonds [106].

The cathodic and anodic reaction taking place on the surface of the Si can be highlighted in the following equations [106]:

$$Ag^+ + e^- \rightarrow Ag^0(0) \qquad (1)$$

$$Si(s) + 2H_2O \rightarrow SiO_2 + 4H^+ + 4e^-_{VB} \qquad (2)$$

$$SiO_2(s) + 6H \rightarrow H_2SiF_6 + 2H_2O \qquad (3)$$

where Eq. (1) corresponds to the cathode reaction and Eq. (2) and (3) to the anode reaction. When Ag is used as a metal, Ag^+ ions in the proximity of the silicon surface

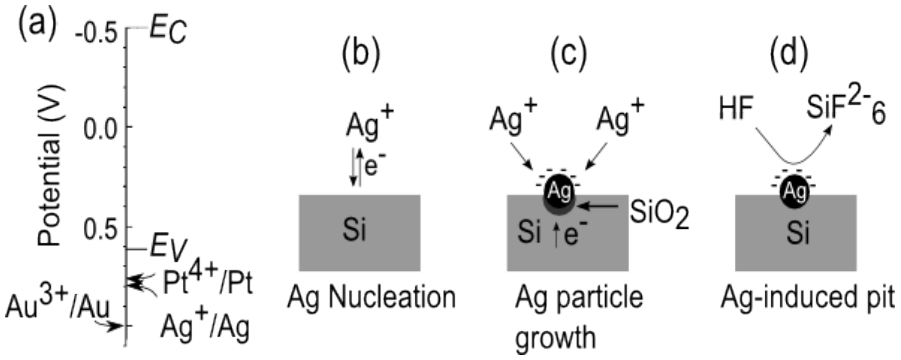


Figure 3.1: (a) Qualitative diagram of the comparison of electrochemical electron energy levels of Si band edges and three redox systems, $AuCl_4^-/Au$, $PtCl_6^{2-}/Pt$, Ag_4^+/Ag in HF solution. E_C and E_V are the conduction and valence band of Si, respectively. (b)-(d) Process of electroless silver deposition on a Si substrate immersed in $HF/AgNO_3$ solution [106].

capture electrons from the valence band of silicon, see Fig. 3.1(b). Holes are generated in the Si valence band and the Ag^+ is reduced into Ag nuclei. Deposition and growth of Ag nuclei facilitates the formation of SiO_2 underneath the silver nanoparticles, see Fig. 3.1(c). SiO_2 is then etched away by HF, with the nanoparticles sinking into the silicon and forming SiNWs, as shown in Fig. 3.1(d) [103, 107].

It is possible to etch NWs in a solution of HF and $AgNO_3$, as used in Ref. [108]. In this case, the Ag in excess will form a dendrite structure that is removed using HNO_3 solution.

3.2.2 Morphology of nanowires

The etching morphology of the silicon surface is greatly influenced by the thickness of the Ag-particle film. If the electroless deposition time is rapid (10s), this would lead to a very thin layer of Ag, composed of small particles. In this case, only disordered Si nanostructures would form on the surface. Refs. [106, 109] studied morphology of NWs as a function of Ag thickness. The formation of nanowires easily occurs on the Si surface when there is high density of Ag particles. Fig. 3.2(a1), (b1) and (c1) show SEM images of Ag film on Si substrate for three different thicknesses of Ag [109]. In Fig. 3.2(a1), the Ag is only 5 nm thick, this corresponds to a very fast deposition time. The etching on the Si substrate is random and not homogeneous, with gaps and a sponge-like form, see Fig. 3.2(a2)-(a3). As the thickness of the Ag is increased to 20 nm thick, see Fig. 3.2(b1), the etching leads to vertically-aligned, interconnected NWs, see Fig. 3.2(b2)-(b3). If the Ag thickness is increased to 50 nm, Fig. 3.2(c1), the etched NWs do not have a uniform

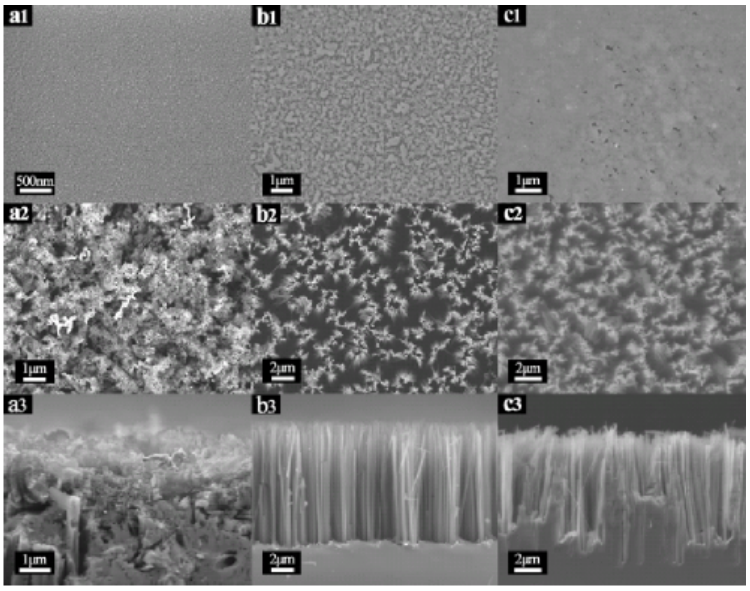


Figure 3.2: SEM images of SiNW samples with three different thicknesses: (a1) 5 nm thick Ag on Si substrate, (b1) 20 nm thick Ag and (c1) 50 nm thick Ag. (a2)-(a3), (b2)-(b3), (c2)-(c3) are planar and cross-sectional SEM images of (a1), (b1) and (c1), respectively [109].

length, Fig. 3.2(c3), due to the non-uniform Ag nanoclusters that prevent some parts from being etched from the etching solution, Fig. 3.2(c2). Hence, the metal deposition is an important step in the formation of NW as it influences the shapes, the distances and the packing factor.

The temperature of etching may also influence the NWs morphology. Peng *et al.* [108] etched SiNWs at different temperature. Fig. 3.3(a)-(c) show samples etched in a solution of 0.02 mol L^{-1} Ag^{+} at temperatures of 15 °C (Fig. 3.3(a)), 50 °C (Fig. 3.3(b)) and 120 °C (Fig. 3.3(c)). The SEM images indicate that the etching temperature could lead to disorder on the surface of the micro-structures, with porous structures obtained with etching temperature of 120 °C. When the Si substrate is immersed in a solution of $HF/AgNO_3$ for a period of time $\geq$30 min, then the formation of dendrite structures is observed on top of the Si surface, see Fig. 3.3(d).

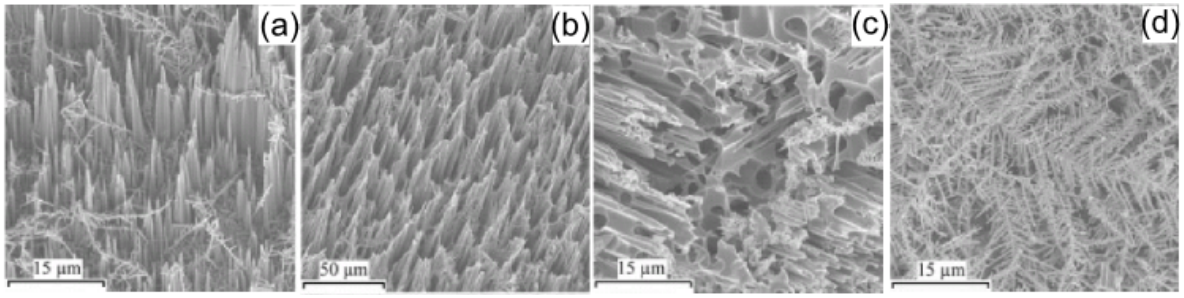


Figure 3.3: SEM images of NW arrays at different etching temperatures: (a) 15 °C, (b) 50 °C and (c) 120 °C. (d) dendrite structure formed when Si is etched in a solution of HF/$AgNO_3$ [108].

Cheng *et al.* reported a linear relationship between the etching time and the length of the NWs [110]. This experiment was repeated for different etching temperatures, leading to longer NWs when the temperature was higher. Fig. 3.4 shows the length of SiNWs as a function of the etching time in the temperature range 0 – 60 °C, with the relationship between SiNW length and etching time being linear. As the etching temperature is increased, the rate of etching increases [110].

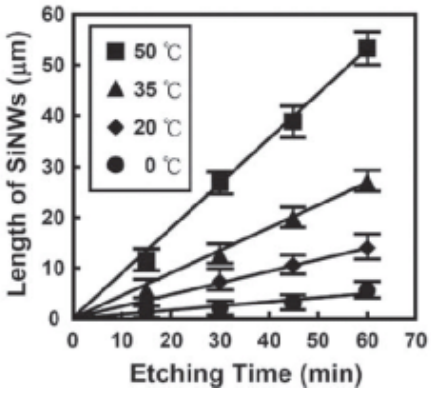


Figure 3.4: Time dependence of the length of SiNWs for different etching temperatures [110].

3.2.3 Etching mechanism in hydrogen peroxide solution

After Ag nanoparticles were deposited on the Si surface, etching of NWs is carried out in a solution of HF and hydrogen peroxide H_2O_2. In a similar way to the metal nanoparticle deposition, etching in a solution of HF and H_2O_2 is characterised both by cathode and

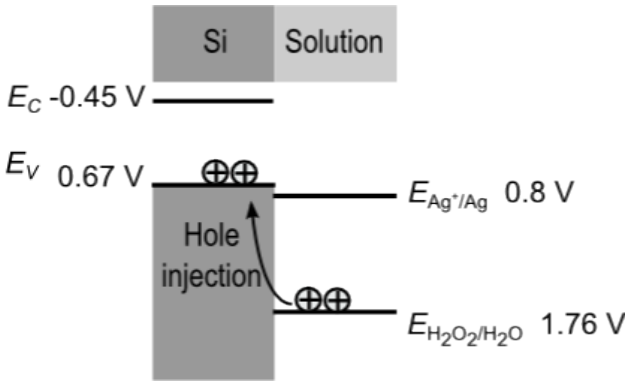


Figure 3.5: Schematic diagram of the relationship between bands in Si and H_2O_2. The case of Ag^+/Ag is also shown [103].

anode reactions. The electrochemical potential of H_2O_2 is more positive than Si (Fig. 3.5), as a consequence etching of Si will occur both in n- and p-type. The etching rate in HF/H_2O_2 is homogeneous and ~10 nm/hour, if metal nanoparticles are not deposited on a Si substrate [103]. Therefore, metal deposition is necessary step for NWs to form in HF/H_2O_2 , as the Si in contact with the noble metal has an etching rate much faster than Si without metal coverage. The cathodic reaction of H_2O_2 or O_2 occurs on the Ag metal surface, with a reaction given by [111]:

$$H_2O_2 + 2H^+ + 2e^- \rightarrow 2H_2O \qquad (1)$$

The holes are injected into the Si substrate in contact with the metal. The area under the metal is dissolved by HF (anode reaction). While different models have been proposed for the dissolution of Si, this depends also on the noble metal used. These can be grouped into three types: (1) direct dissolution of Si in a tetravalent state, (2) direct dissolution of Si in a divalent state, and (3) Si oxide formation then followed by oxide dissolution. Here, we give the anode reaction relative to (3) in the presence of Ag noble metal [111]:

$$Si + 2H_2O \rightarrow SiO_2 + 4H^+ + 4e^- \qquad (2)$$

$$SiO_2 + 6HF \rightarrow [SiF_6]^{2-} + 2H_2O + 2H^+ \qquad (3)$$

The H_2O_2 concentration is an influencing factor in the etching mechanism. Its concen-

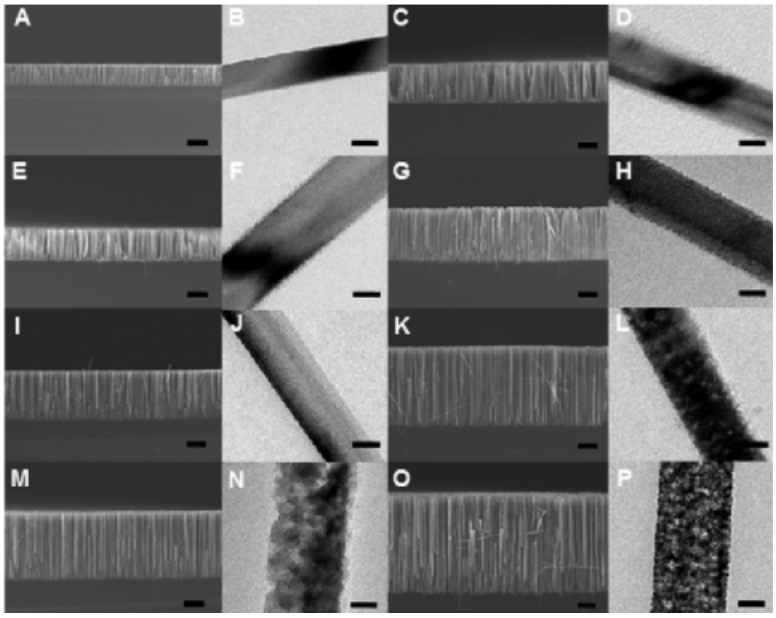


Figure 3.6: SEM and TEM images: (A, B) in a solution of 0.1 M H_2O_2 for 30 min and (C, D) for 60 min. (E, F) 30 min in 0.15 M H_2O_2 and (G, H) for 60 min. (I, J) 0.2 M H_2O_2 for 30 min and (K, L) for 60 min. (M, N) 0.3 M H_2O_2 for 30 min and (O, P) for 60 min. SEM and TEM scale bar are 10 μm and 60 nm, respectively [111].

tration affects not only the etching rate but also the morphology of the NWs. Qu *et al.* [111] studied the morphology of the NWs as a function of H_2O_2 concentration. Results of the study are shown in Fig. 3.6(A-P), with scanning electron microscope (SEM) and transmission electron microscope (TEM) images of n-type Si for different H_2O_2 concentrations [111]. Fig. 3.6(A, E, I, M) show SEM images of NW arrays immersed for 30 min in a (0.1 M, 0.15 M, 0.2 M, 0.3 M) H_2O_2 solution, respectively. Fig. 3.6(B, F, J, N) show the TEM images of Fig. 3.6(A, E, I, M), respectively. Similarly, Fig. 3.6(C, G, K, O) and (D, H, L, P) show SEM and TEM for n-Si NW arrays immersed for 60 min in 0.1 M, 0.15 M, 0.2 M, 0.3 M H_2O_2 solution, respectively. As the H_2O_2 concentration increases, the surface roughness of the NW increases, with porosity present in the shell that surrounds the solid core of the NW for the 0.3 M H_2O_2 case, see Fig. 3.6(P). Furthermore, the longer the etching time, the rougher the NWs.

Charter *et al.* have studied the morphology of NWs as a function of the parameter $\rho = [HF/(HF+H_2O_2)]$. Their result can be summarised as follows [112, 103]:

- 100 % $>\rho >$ 70 %, high HF concentration: the H_2O_2 concentration determined the rate of etching. Holes were formed underneath the Ag/Si interface, as the HF

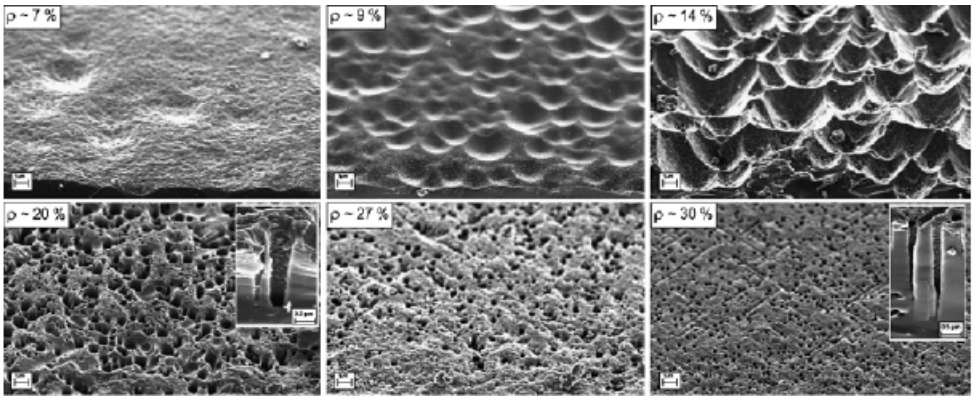


Figure 3.7: SEM images of p-Si (100) substrates etched in a solution of different ρ values [112].

percentage was sufficient to dissolve Si or SiO_x and the Ag particles lead to straight cylindrical pores with diameter similar to that of the Ag particle.

- 70 % $>\rho >$ 20 %: the rate of etching was determined by the HF concentration. The consumption of holes at the Ag/Si interface was smaller than the holes generation. Therefore, the excess holes would diffuse to the side wall leading to microporous Si on the sides of the pore. Here, the nanostructures had a cone-shaped pore.

- 20 % $>\rho >$ 9 %: crater-like structures of several diameters were formed.

- $\rho <$ 9 %, high H_2O_2: diffusion of holes involved all the Si surface, with etching occurring everywhere independent of the Ag particles position, leading to a macroscopically polished surface.

SEM images for the case of 30 % $>\rho >$5 % are shown in Fig. 3.7 for a p-type Si (100).

3.3 Silicon nanowire arrays

3.3.1 Preparation

Large area of vertically aligned SiNW arrays were fabricated from lightly- and moderately-doped n-type (phosphorus doped) and lightly doped p-type (boron doped) silicon (100) wafers. The arrays were fabricated using the MACE process [113, 108, 107, 106, 111, 114].

In our case, Ag nanoparticles acting as a catalyst were deposited first, followed by NW etching at room temperature. Here, the Si sample was first cleaned in acetone and IPA, the reverse side of the wafer was protected by poly(methyl methacrylate) (PMMA). Then

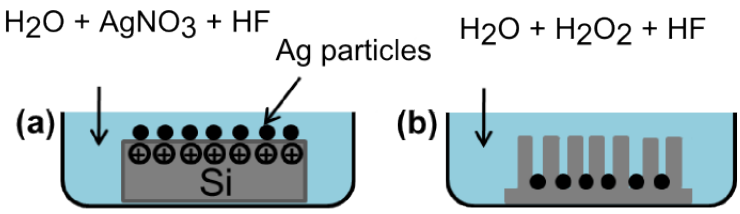


Figure 3.8: (a) Electroless deposition of Ag nanoparticles and formation of holes (represented by +) into the Ag/Si surface. (b) Silver nanoparticles sink into Si and subsequently Si is etched by HF, leading to NW formation.

the sample was immersed in a solution of $HF/AgNO_3/H_2O$ at room temperature for 15 minutes (volume ratio 1:1:8, with 60mM $AgNO_3$). This deposited Ag nanoparticles on the Si surface via an electroless deposition (galvanic exchange) mechanism, see Fig 3.8(a). The nanoparticles then acted as catalysts for subsequent etching of the NWs in $HF/H_2O_2/H_2O$ solution (volume ratio 1:2:1, with 0.6M H_2O_2). The process involved etching of the Si in contact with the Ag nanoparticles, with NWs of irregular cross-section formed in the remaining, un-etched regions. As the etching process proceeded, the nanoparticles sank into the Si, see Fig. 3.8(b). The length of the NWs has a linear dependence on the etch time with average etch rate ~30 μm/hr, for the lightly doped wafer. In contrast, in moderately doped sample, we did not find a linear dependence. The rate was slower than the lightly-doped material, ranging between 8 – 25 μm/hr. Finally, the deposited Ag was removed using 5M HNO_3. A filling factor of ~30% was found for both the lightly doped and moderately doped NW arrays. The filling factor (measured by Valerie Stevens) was extracted by measuring the change in sample weight after oxidation. Samples were oxidised at 1050 °C for several hours, completely oxidising the NWs. The change in sample weight allowed extraction of the weight of NWs. Using the NW weight, length, and density of Si, it is then possible to obtain the total cross-section area through the NWs and hence, the filling factor.

3.3.2 Characterisation of lightly doped nanowires

The main part of Fig. 3.9 shows an SEM image of the cross-section through a 60 μm long SiNW array. The SiNWs were synthesized from a lightly-doped n-type silicon (100) wafer, resistivity ρ ~1 – 5 Ωcm, phosphorous doping from 5×10^{14}– 3×10^{15} /cm^3. The NW arrays, fabricated by the MACE process, were etched for 1 hour and 30 minutes.

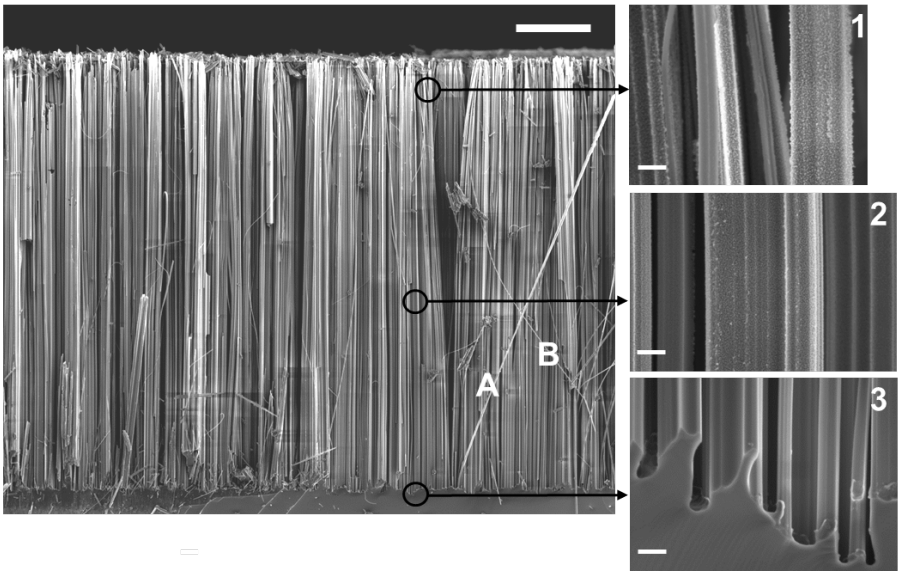


Figure 3.9: Main image: Cross-sectional scanning electron micrograph through a 60 μm long SiNW array. SiNWs marked 'A' and 'B' are ∼100 nm and ∼50 nm wide. The scale bar is 10 mm. Insets 1 – 3 show high-resolution micrographs of the corresponding circled regions. The scale bar is 200 nm.

The process creates SiNWs from 30 to 400 nm in diameter, with large aspect ratio up to 1:3000. The NWs are vertically-aligned, with parallel sidewalls over the full etch depth. The etch depth is regular across the entire width of the wafer, as can be seen from the cleaved edge of the main part of Fig. 3.9. The insets 1 – 3 show higher resolution images of three areas (circled), at ∼5, ∼30, and ∼60 μm depth. Inset 3 shows the base of the array, where NWs join the un-etched substrate, cleaved at an angle to the NW cross-section. The NW morphology is complex, with irregular cross-section. This consists of a columnar core ∼100 – 400 nm in width with vertically-aligned attached ribs ∼30 – 100 nm in width. At least some of the ribs are poorly attached or may be pinched-off, e.g. the NWs marked 'A' (diameter ∼100 nm) and 'B' (diameter ∼50 nm) may have broken off from a wider section. In each of our 0.5 × 0.5 cm^2 samples, using an array filling factor of ∼30% and an average NW diameter of ∼250 nm, there are ∼10^7 NWs.

Insets 1-3 allow comparison of the NW surface roughness with array depth. This reduces from ∼10 – 20 nm near the top (inset 1), to ∼5 nm at ∼30 μm depth (inset 2), to a negligible value at the bottom (inset 3). This suggests that the longer a section of NW surface remains immersed in the etchant, the greater the surface roughness due to increased surface etching.

High resolution SEM images of the top part of the NW array are shown in Fig. 3.10(a)-

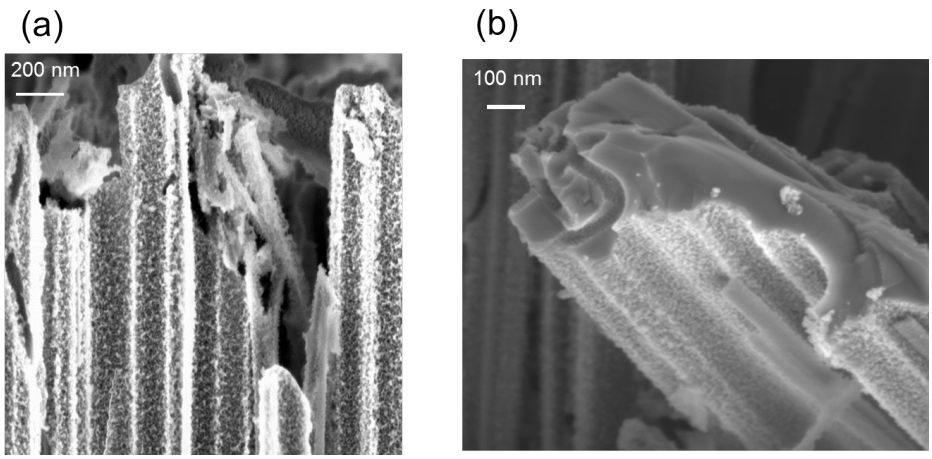


Figure 3.10: (a) Details of the roughness present at the top of the NW array. (b) Broken-off section from the top of the array.

(b). Fig. 3.10(a) shows a particular of the roughness present at the surface of the NWs at the top of the array. Fig. 3.10(b) shows a broken-off section of the top of the array. It can be seen that the shell of the NW is rough only at the surface, with the NW surface roughness ∼20 nm. The NW core appears unaffected and undamaged.

Figure 3.11 shows further scanning electron microscope (SEM) images of the SiNW arrays used for the Seebeck measurements, discussed in chapter 5.3. Figure 3.11(a) shows the surface morphology of a typical SiNW array. Figure 3.11(b)-(d) show cross-sectional images of arrays with 35 μm, 80 μm and 350 μm long NWs respectively. Figure 3.12(a) shows a transmission electron microscope (TEM) image of a 35 μm long SiNW array. The sample was etched for an hour, and used for the Seebeck coefficient measurement, reported in chapter 5.3. After measurements, the NW array was immersed in IPA and suspended NWs were deposited into a carbon TEM grid. The figure shows two NWs with diameter of ∼180 nm and ∼400 nm. The black solid lines in the two SiNWs indicate that the NWs maintain the single crystalline properties. The diameter of both NWs shows some irregularity across its length (3.2 μm). Fig. 3.12(b) illustrates a high resolution TEM image of a NW with a diameter of ∼200 nm. Surface roughness can be observed along the NW. The inset of Fig. 3.12(b) shows a selected area electron diffraction (SAED) pattern of our NWs along [100]. The diffraction pattern indicates that the SiNWs conserve the single crystal behaviour of their parent bulk Si. Fig. 3.12(c) is a particular at the edge of the NW, the circle indicates that the lateral surface roughness is ∼20 nm thick.

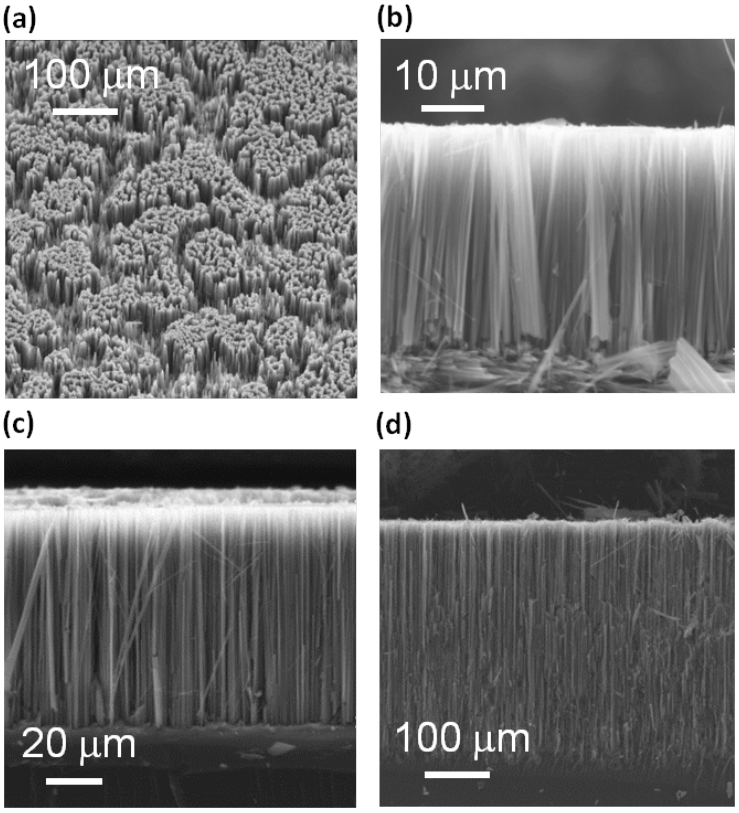


Figure 3.11: SEM images of SiNW arrays (a) Surface morphology of NW array. (b)-(d) Cross-section images through samples with 35 μm, 80 μm and 350 μm long NWs respectively.

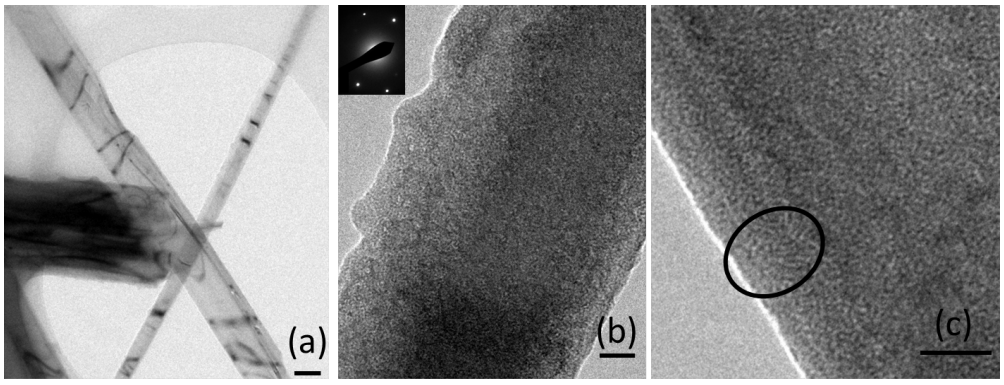


Figure 3.12: TEM images of : (a) two lightly doped SiNWs with diameter of ∼180 and ∼400 nm. (b) Particular of the roughness across the surface of a NW with ∼200 nm in diameter and (c) Detail of the NW edge. The scale bar is 0.2 μm for (a) and 20 nm for (b) and (c), respectively.

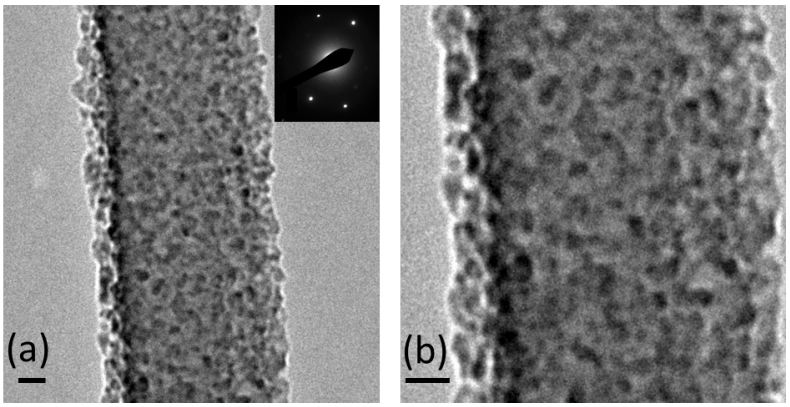


Figure 3.13: (a) TEM image of 130 nm diameter NW and (b) section of the NW surface. The scale bar is 20 nm in both cases.

Fig. 3.13(a) illustrates a high resolution TEM image of a NW with a diameter of ∼130 nm. The NWs were etched for four hours and the length of the original SiNWs was 130 μm. The surface of the NWs is rougher than the one hour etched sample, indicating that the longer the etching time, the greater is the roughness of the NWs. The inset shows a SAED pattern of the NW along [100], indicating that the NW is single crystalline. Fig. 3.13(b) shows a section of the surface of NW at the edge. The edge is very irregular and the whole surface is rough, with features of lateral dimension of ∼ 5 –15 nm and depth ∼20 nm thick.

3.3.3 Characterisation of moderately doped nanowires

We now consider the fabrication of SiNWs synthesized from a moderately doped n-type silicon (100) wafer, resistivity ρ ∼0.01 – 0.03 Ωcm, phosphorous doping from 6×10^{17}–1×10^{18} /cm^3. The NW arrays were etched for 3 hours. The main part of Fig. 3.14 shows an SEM image of the cross-section through a 50 μm long SiNW array. Most of the NWs are vertically-aligned, with parallel sidewalls over the full etch depth. In contrast, in other parts of the array, some NWs are slightly bent and grouped into bundles. The etch depth is irregular across the entire width of the wafer, as it can be seen from the cleaved edge of the main part of Fig. 3.14. Furthermore, the length of the wires is irregular across the array. The NW marked 'A' may have broken off from a wider section and has a diameter of ∼150 nm. The insets 1-3 show higher resolution images of three areas (circled) at ∼5, ∼15 and ∼45 μm depth. Considering a sample with similar area to the lightly doped, 0.5 × 0.5 cm^2, and an array filling factor of ∼30% and an average NW diameter of ∼250 nm,

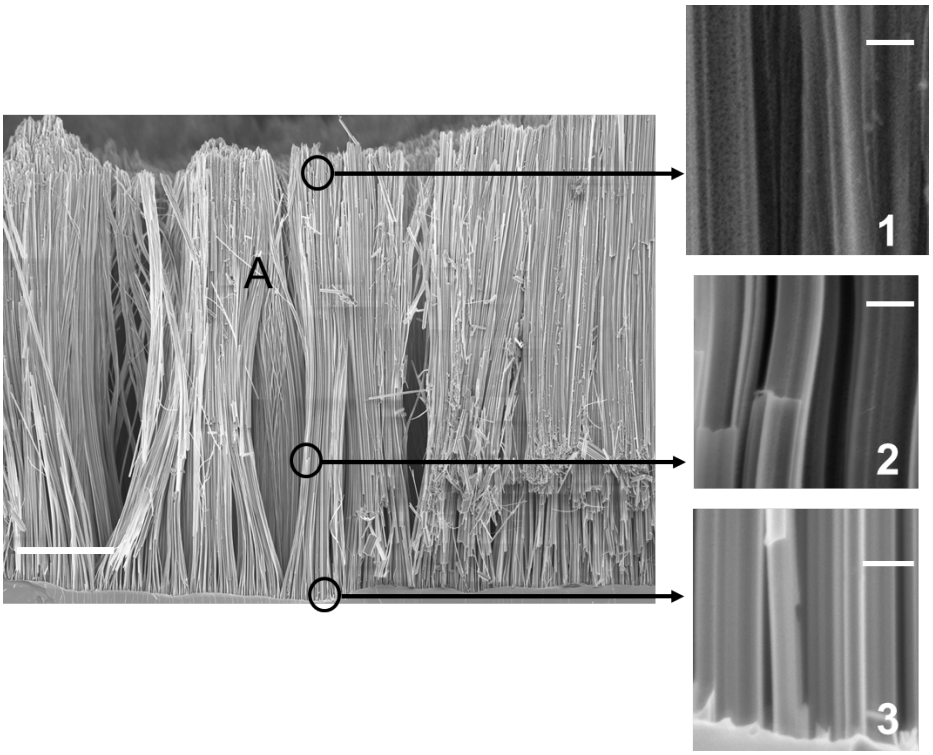


Figure 3.14: Main image: Cross-sectional scanning electron micrograph through a 50 μm long SiNW array. The SiNW marked 'A' has a diameter of $\sim$150 nm. The scale bar is 10 μm. Insets 1 – 3 show high-resolution micrographs of the corresponding circled regions. The scale bar is 200 nm.

there are $\sim 10^7$ NWs. Insets 1-3 allow comparison of the NW surface roughness with array depth. The roughness slowly increases as the top of the array is approached. However, the moderately doped NWs are less rough than the lightly doped wires. Qu *et al.* [111] and Hochbaum et *al.* [114] have found that as the doping level increases, the roughness of the NWs increases, leading to porous nanowires in case of heavily doped, see Fig. 3.6. This was not the case for the NWs prepared in a similar manner to the others by Zhang *et al.* [115]. The roughness of the NW is influenced by different factors, such as the etching time, the concentration of hydrogen peroxide, H_2O_2, and the etching temperature. The cross section of the NWs is similar to that in lightly doped NWs. Fig. 3.15(a) shows a top view SEM image of moderately doped wires. Fig. 3.15(b)-(c) show an SEM image of the 40 and 30 μm long NW arrays that were used for the measurement of S and κ. The 30 μm long NW arrays were etched for 4 hours, whereas the 40 μm long NW arrays were etched for only an hour. Here, the 30 μm and 40 μm long SiNWs samples have a same doping level and they were etched at the same time using the same etching conditions. However, a non

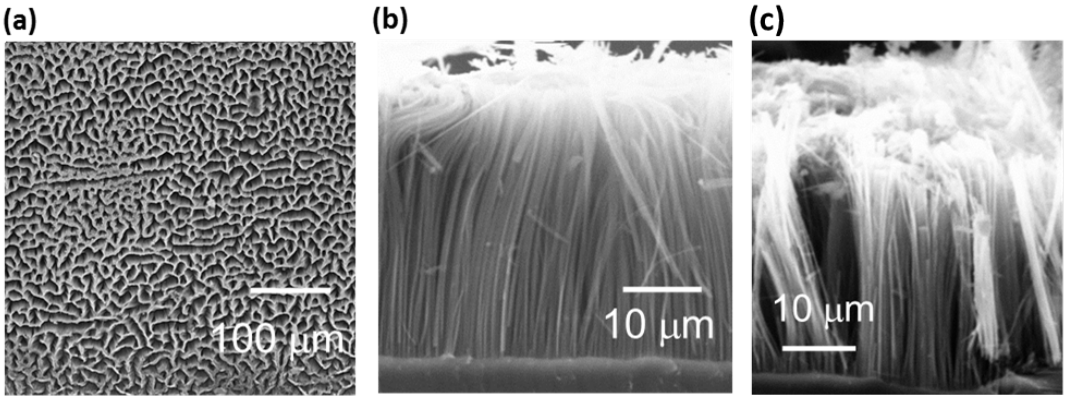


Figure 3.15: SEM images of SiNW arrays (a) Surface morphology of NW array. (b)-(c) Cross-section images through samples with ∼40 μm, 30 μm long NWs respectively.

linear relationship was found between the etching time and length. Furthermore, longer etching hours did not lead to SiNW arrays of greater length.

3.4 Nanowires before and after measurement

During experiments, SiNW arrays were sandwiched in between two Cu blocks for electrical and thermal characterisation. To study changes in the arrays before and after pressure is applied at both ends, SEM images have been taken of SiNW array before and after measurements. Fig. 3.16(a) shows an SEM image of ∼90 μm long vertically aligned SiNW arrays before measurement. Fig. 3.16(b) shows the SiNW arrays after measurement. Here, the NWs are still vertically aligned, but the tips of the wires are broken off. $\sim$ 10 μm of the top part of the array have broken-off and the tips of wires form a connection with all the wires, as shown in Fig. 3.16(c). The network formed by the NWs might be useful as they connect most of the NWs, reducing empty spaces, facilitating thermal conduction and reducing interface temperature drops. However, the NWs are very robust and they maintain their vertical morphology even when high pressure is applied to the ends.

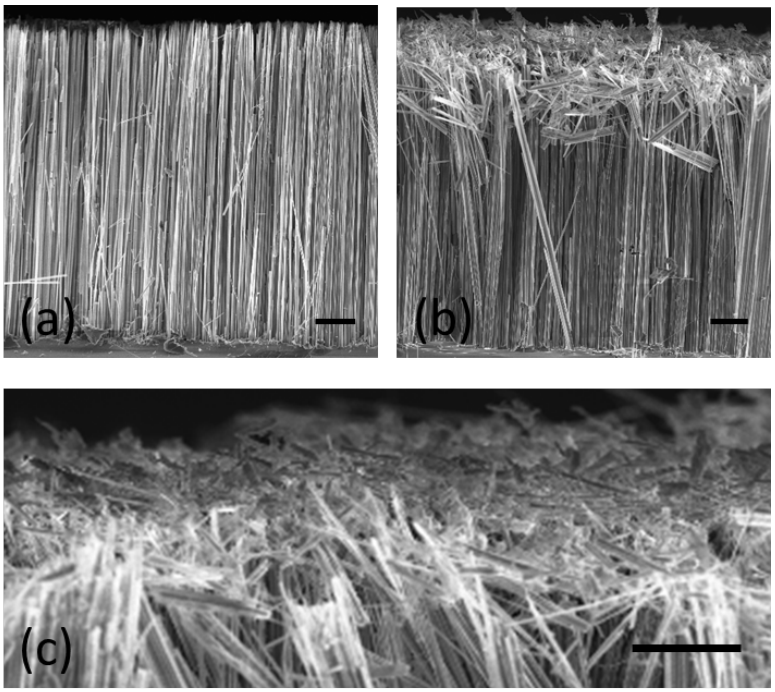


Figure 3.16: SEM image of SiNW arrays ~90 μm long, before (a) and after (b) measurement in between two Cu blocks. (c) Particular of the top of the array after measurement. Here the top of the wires are all broken off and connected with each other. Scale bars are 10 μm.

4 Thermoelectric measurements at room temperature

A measurement apparatus was fabricated to characterise S, at equilibrium and in open circuit conditions, in thin area samples of SiNW arrays. n- and p-type SiNW arrays of different lengths were measured at ambient conditions. An inversion of carrier type from p- to n-type behaviour was observed in the 90 μm long p-SiNW array, which may be related to positive fixed charge trapped at the NW surface. Our measured data indicate a strong influence of the surface on the NW Fermi level. Considering the dependence of S as a function of the NW length, we find an optimum length of $\sim 30 - 40$ μm in both n- and p-type SiNWs.

4.1 Design and construction of measurement apparatus

Figure 4.1 shows the measurement apparatus that has been fabricated in order to characterise the thermoelectric properties of Si nanowire arrays. The apparatus is composed of two different copper blocks, the large block having dimensions of 5 cm $\times$ 3.7 cm $\times$ 0.7 cm, and the small block with dimensions 1.5 cm $\times$ 1.5 cm $\times$ 0.4 cm. A small hole, 1 mm in diameter, was drilled on each copper block, near the surface. Copper-constantan thermocouples were secured in the holes with epoxy. A Keithley 2000 multimeter, with high input impedance (10 GΩ), was used to measure the voltage. A cylindrical delrin weight mounted on a clamp was used to apply uniform pressure to the setup.

The accuracy of the measurement setup and any error that may be associated was verified by analysing a device with known properties. The Seebeck coefficient of a Peltier element (PE) with dimensions 0.15 cm $\times$ 0.15 cm $\times$ 0.15 cm, supplied by Laird Technologies was measured [116]. In order to enhance the thermal conductance an interfiller was used on the interfaces of the PE, to fill any void gaps. The PE was then measured in two different

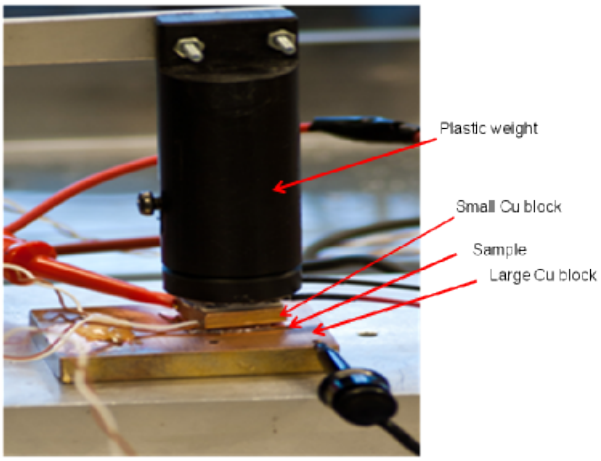


Figure 4.1: Apparatus used for the Seebeck coefficient measurements.

configurations. In the first case, current was applied to the PE, sandwiched in between the two copper blocks. Current was changed in the range of 0.8 to 1.7 A, and at a given current I, voltage V and temperature ΔT across the PE were recorded. This single PE configuration is illustrated in Fig. 4.2(a). In the second case, two PEs were used. Here, one of the PE acted as the heater on top of the small Cu block and the second PE, sandwiched in between the two Cu blocks, acted as the test sample to be characterised, see Fig. 4.2(b). By varying the current of the heater, it was possible to apply a ΔT across the second PE and then measure the voltage V versus ΔT, using a high impedance voltmeter. In this configuration, the current flow through the tested PE is zero. This experiment is fundamentally different from the first case, where a current flows through the PE.

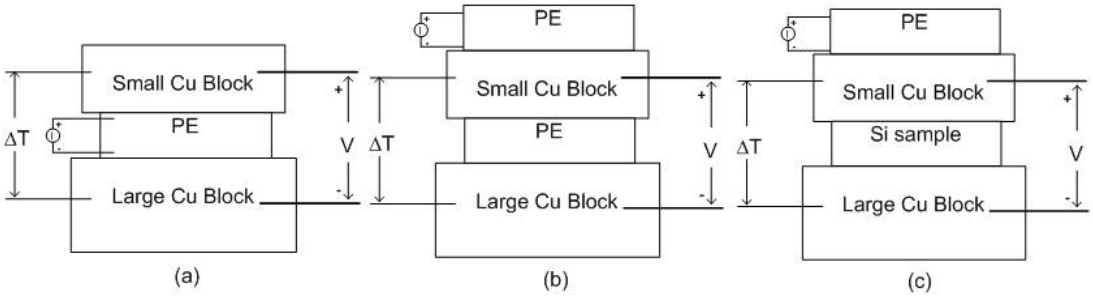


Figure 4.2: Schematic diagram of the apparatus used in (a) single PE configuration; (b) double PE configuration; (c) Si sample measurement configuration. The dimensions of the large Cu block are 5 cm × 3.7 cm × 0.7 cm, the small Cu block 1.5 cm × 1.5 cm × 0.4 cm, and the PE 0.15 cm × 0.15 cm× 0.015 cm.

The Seebeck coefficient was measured for both cases by using the following equation [117]

$$V = 2N\left(\frac{I\rho}{G} + S(T_H - T_C)\right) \tag{4.1}$$

where V is the voltage applied to the PE, N is the number of thermocouples in the PE (31 in our case), ρ the electrical resistivity (Ωcm), G the ratio of area over length (cm), I the current (A), S the Seebeck coefficient (Volt/Kelvin), T_H the hot side temperature (Kelvin) and T_C the cold side temperature (Kelvin). S is determined by the slope $2NS$ of Eq. 4.1 for a given current. Fig. 4.2(c) illustrates a diagram of the apparatus when used to measure Si and SiNW array samples in ambient condition, at room temperature.

4.2 Testing

4.2.1 Single Peltier element configuration

Figure 4.3 shows the measured data (circles) of V vs. ΔT at a given current I, for a single PE, and the lines correspond to the calculated (V, ΔT, I), where I is varied in a range of 0.8 A to 1.7 A. Additionally, the measured data points (V, ΔT, I) are also tabulated (Table 4.1). The theoretical curves shown in Fig. 4.3 are calculated by using Eq. 4.1 at various voltages and at constant current I as follows

$$V = A_1 I + A_2 \Delta T \tag{4.2}$$

$$A_1 = 2N\rho/G \tag{4.3}$$

$$A_2 = 2NS \tag{4.4}$$

The y-intercept A_1 and the slope A_2 were obtained by substituting data points corresponding to a given set (V, ΔT, I) into Eq. 4.1. Two equations, corresponding to two data points were solved simultaneously to get A_1 and A_2. We then have V as a function of ΔT for current values given by $0.8 \leq I \leq 1.7$. In our case, Eq. 4.2 becomes $V = 0.759{\cdot}I + 0.01875\Delta T$. The experimental values in Tab. 4.1 fit well to the respective constant current lines, that are plotted in Fig. 4.3. We find that in the single PE configuration, the Seebeck coefficient is approximately 300 μV/K.

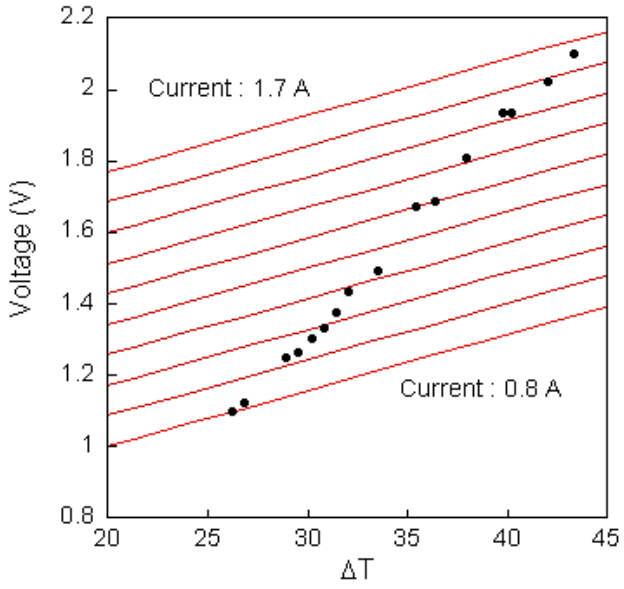


Figure 4.3: Measured values are represented by circles. The lines represent the calculated voltages for different currents in the range of 0.8 – 1.7 A.

Table 4.1: Measured data points for the single PE configuration.

Voltage (V)	Current (A)	ΔT
1.099	0.791	26.2
1.124	0.819	26.8
1.266	0.94	29.5
1.302	0.975	30.2
1.333	0.998	30.8
1.376	1.033	31.4
1.435	1.082	32
1.491	1.134	33.5
1.673	1.295	35.4
1.688	1.295	36.4
1.809	1.383	37.9
1.933	1.516	39.8
1.936	1.516	40.2
2.02	1.604	42
2.1	1.698	43.3

4.2.2 Two Peltier elements configuration

Fig. 4.4 shows the plot of the measured data for the two-Peltier configuration. In the plot the measured V as a function of applied ΔT is shown. Furthermore, V varies linearly with ΔT, this suggest that the relationship of $S = V/\Delta T$ is valid. Hence, from the slope of the curve, it is possible to extract the Seebeck coefficient, which in this case is $\sim$223 μV/K. There is a discrepancy in the values obtained with the two different configurations. This may be related to variation in the temperature drop at the interfaces, or due to heat carried away by current flow in the first configuration.

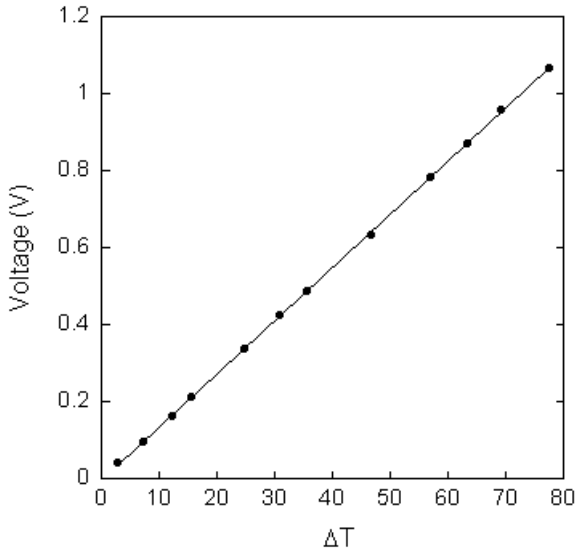


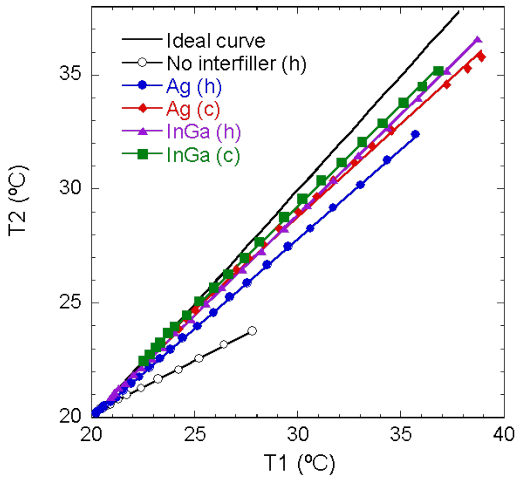
Figure 4.4: Measured voltage V versus ΔT. The circles represent the measured values and the line is a linear fit to the data.

4.2.3 Copper on copper

To identify any temperature drop within the measurement apparatus (sketched in Fig. 4.1), an experiment where copper lies on copper, without any sample, has been performed. The configuration of this experiment is similar to Fig. 4.2(b), but in this case there was no PE sandwiched in between the two Cu blocks. The top Cu block was heated up in a temperature range 20 – 40 °C and the temperatures of both copper blocks were recorded. Experiments were performed without interfiller, with silver and indium gallium interfillers. The interfiller was used to improve thermal and electric contacts and hence reduce the contact resistance between the two interfaces.

Contact resistance is a consequence of the surface roughness. When two solids with plane surfaces are pressed against each other, the actual contact between the two solids is limited to a number of points since the surfaces are not perfectly smooth and there may be micro roughness. The thermal resistance is a function of roughness of surface, type of material, interface pressure and type of fluid filling the voids [118, 119].

Measurements were carried out by cooling down the small Cu block in a temperature range from 40 – 20 °C. The results are shown in Fig. 4.5, with the table reporting the linear fit to the data. The solid line corresponds to the ideal case $T_2 = T_1$, where no temperature is lost at the interface. The other curves correspond to the cases of no interfiller, Ag and InGa interfillers. When there is no interfiller at the interface, the linear fit is $T_2 = 10.9 + 0.46T_1$. When $T_1 = 22$ °C, $T_2 = 21.02$ °C, this is equivalent to a ∼5% temperature drop. However, at higher temperatures, *i.e.* $T_1 = 30$ °C, $T_2 = 24.7$ °C, this corresponds to ∼18% temperature lost at the interface. When an interfiller is used, temperature losses at the interface are greatly reduced. In the case of Ag interfiller, during heating, at $T_1 = 35$ °C, $T_2 = 31.9$ °C. This corresponds to ∼9% temperature drop, that is reduced to ∼6% when cooling the sample, giving T_2 =33 °C, for a starting T_1 =35 °C. In the case of InGa interfiller, the temperature losses at the interface are even lower, demonstrating that InGa makes a better thermoelectric contact. In the InGa case, at $T_1 = 35$ °C, $T_2 = 33.8$ °C, giving a temperature drop of ∼3.4% for the case when the Cu block is allowed to cool from a high temperature. These experiments outline that when no interfiller is used, ∼20% of the temperature difference across the Cu blocks occurs at the interface. Hence, interfiller was used to improve thermal contact between sample and Cu blocks.



	T_2
No interfiller (h)	$10.92+0.46T_1$
Ag interfiller (h)	$4.28+0.79T_1$
Ag interfiller (c)	$4.34+0.82T_1$
InGa interfiller (h)	$2.52+0.88T_1$
InGa interfiller (c)	$2.65+0.89T_1$

Figure 4.5: Temperature of the large copper block T_2 versus temperature of the small copper block T_1 for different conditions. The solid line corresponds to the ideal case $T_2 = T_1$. Circles represent the experimental points and the lines represent the linear fit. The table, on the right, reports the linear fit to the data where (h) is for heating, and (c) for cooling.

4.3 Bulk silicon and silicon nanowires with Ohmic contacts

Seebeck measurements were initially performed on reference samples of n- and p-type bulk silicon of thickness ~375 μm. 50 nm chromium (Cr) followed by 140 nm gold (Au) was deposited by sputter coating to form Ohmic contacts. The samples were then annealed using a Rapid Thermal Annealing (RTA) at 450 °C for 1 min. The resistivity of the n-type phosphorus doped sample was 1 – 5 Ωcm, corresponding to a doping level of 1×10^{15} – 5×10^{15} cm^{-3}. The p-type boron doped sample resistivity was 1 – 10 Ωcm, with a doping level of 1.5×10^{15} cm^{-3} – 1.5×10^{16} cm^{-3}. Fig. 4.6(a)-(b) show measurements of voltage as a function of ΔT for the n- and p-type silicon samples, with and without interfiller. The measured S for the n-type bulk Si in Fig. 4.6(a) are ~10 μV/K and ~40 μV/K, without and with Ag interfiller, respectively. While, the measured S for the p-type Si sample, shown in Fig. 4.6(b), are ~5, ~21, and ~43 μV/K, without, with Ag and InGa interfillers, respectively. The observed increase of up to an order of magnitude of S in the cases where an interfiller is used can be associated with a better thermal and electrical contact. Additionally, when no interfiller is used, as explained in section 4.2.3, there is a

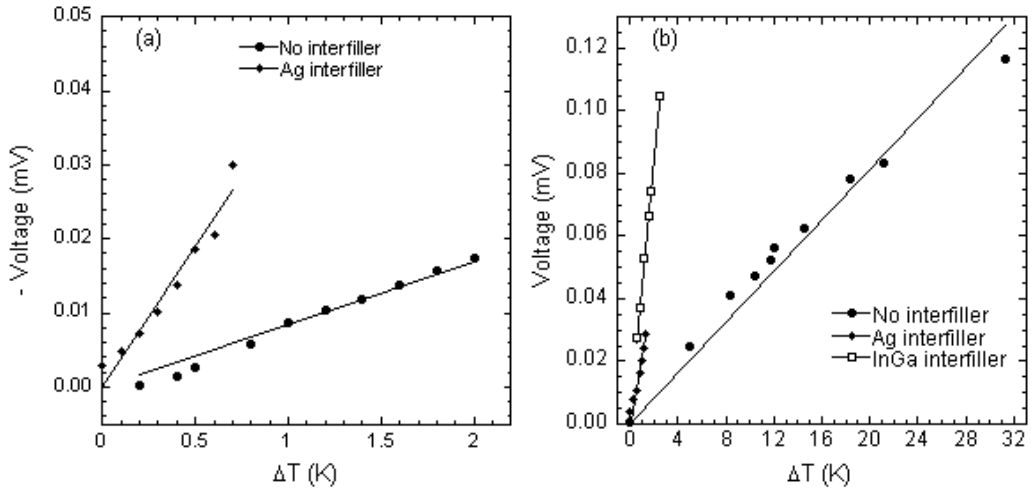


Figure 4.6: Voltage vs. ΔT: (a) n-Si bulk, and (b) p-Si bulk, without and with Ag and InGa interfillers.

temperature drop at the Cu interfaces (up to ~20%).

Figure 4.7 shows voltage as a function of ΔT for p-SiNW array samples of length 30 and 60 μm, with 50 nm Cr/140 nm Au Ohmic contact. Bulk silicon is also shown for comparison. In this measurements no interfiller was used. The measured S are: ~2.2 μV/K, 3 μV/K and 10 μV/K for bulk Si, 30μm and 60 μm SiNW arrays, respectively.

Samples with Ohmic contacts were measured as this would allow measurement on the same sample of S, σ and κ. However, as mentioned in section 2.7.1, when the ends of a thermoelectric material are metalised, the temperature difference can occur within the metal and not in the thermoelectric material. In fact, the measured values of S in the case of samples with Ohmic contact for n- and p-type bulk Si are well below the theoretical value. It is possible to calculate the theoretical S for Si samples with our doping level by using Eqs. 2.30 and 2.31. Here, $E_C - E_F$ and $E_F - E_V$ have been substituting by using Eqs. 2.19 and 2.22 with $N_C = 2.9\times10^{19}$ cm^{-3} and $N_V = 2.65\times10^{19}$ cm^{-3}. As an estimate, the S values obtained were in the range of ~900 – 1000 μV/K for n-type, and in between ~775 – 970 μV/K for the p-type Si. These values are similar to the measured value for an n-type Si samples doped at 2.8×10^{16} cm^{-3} by Ref. [84]. In conclusion, in samples with Ohmic contacts most of the temperature drop can occur at the metal interface. Therefore, in the next section, bulk Si and SiNW samples were measured without metal deposited on its ends.

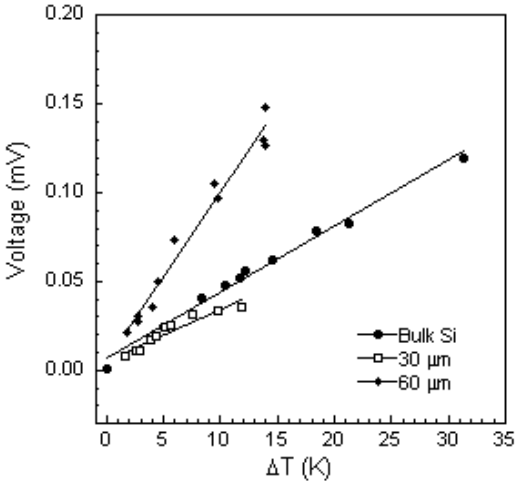


Figure 4.7: Voltage vs. ΔT for bulk p-Si and p-SiNW array samples of length ∼30 and 60 μm.

4.4 Bulk silicon and silicon nanowires without metalisation

4.4.1 Bulk silicon

Figure 4.8(a)-(b) show voltage as a function of ΔT for both n- and p-type samples. The resistivity of bulk Si is the same as the one specified in section 4.3. Fig. 4.8(a) shows bulk n-Si without and with InGa interfiller. Fig. 4.8(b) shows bulk p-Si without and with Ag interfiller. In the case of n-Si, the measured S values are ∼ -360 and ∼ -540 μV/K without and with Ag interfiller, respectively. For the p-Si, the corresponding values of S are ∼225 and 380 μV/K, without and with interfiller, respectively. Here, S is two order of magnitudes higher than the case of samples with Ohmic contacts presented in section 4.3.

It is important to note that the measured experimental points with interfiller gaps show fluctuation in comparison to the case without any interfiller. Also, Ag interfiller is preferred to InGa, as the latter although it guarantees a better thermal contact, diffuses within the Cu blocks. This causes difficulty in removal of InGa from the Cu blocks after each experiment. Furthermore, it was observed during experiments, that there is a contact potential issue due to charge trapped at the contacts.

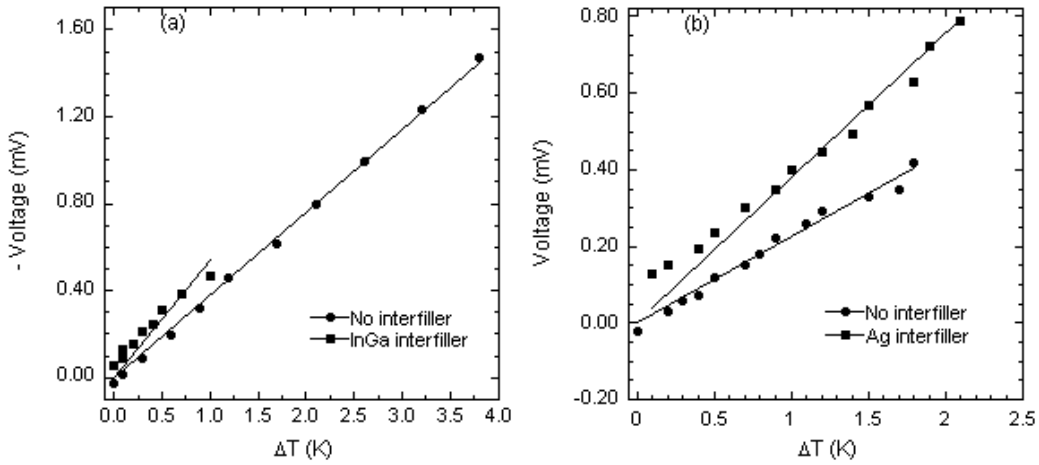


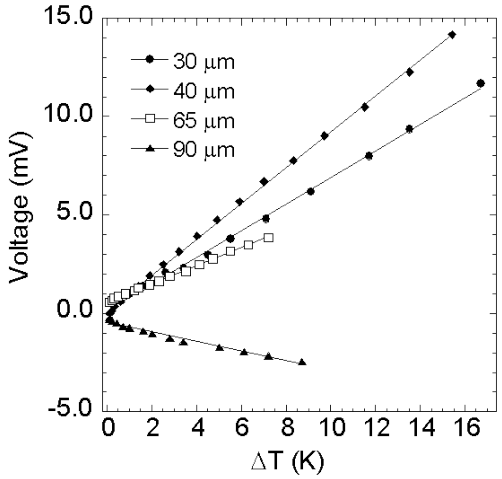
Figure 4.8: Voltage vs. ΔT measurement of bulk silicon. (a): n-type silicon without and with InGa interfiller. (b): p-type silicon without and with Ag interfiller.

This behaviour is associated with the open circuit nature of the measurement and with the absence of ohmic contact. To minimise offsets in the ΔV vs. ΔT graphs, discharging of the charge on the contacts was carried out before each experiment. In Ref. [120], it was found that a contact potential issue may influence the sign of the Seebeck coefficient when S is determined at only two temperature points. In our case, the ΔV vs. ΔT curves are linear, and the slope to these ΔV vs. ΔT curves are used to find S. The slope of the curve should not change even if a contact potential is present [120].

4.4.2 p-type silicon nanowire arrays

Figure 4.9 shows voltage ΔV vs. ΔT for vertically aligned p-SiNW arrays of lengths ∼30, 40, 65, and 90 μm. The sample area is ∼1.5 cm × 1.5 cm, and using an array filling factor of ∼30% with average NW diameter of ∼250 nm, there are $\sim 10^9$ SiNWs in parallel. In the table of Fig. 4.9 are reported the measured S values, the calculated $E_F - E_V$ and the calculated carrier density p. These have been calculated by solving Eq. 2.31 for $E_F - E_V$, with S_h known, and p by using Eq. 2.23. S increases as the length of the wires increases. In the 90 μm SiNW array, an inversion of carrier type from p- to n-type behaviour is observed. The calculated doping level for bulk Si, reported in the table of Fig. 4.9, is slightly higher, but still in good agreement with the doping level predicted from the wafer supplier. The doping level for the SiNWs changes from a minimum of $\sim 2.9 \times 10^{15}$ cm^{-3}, in the case of 40 μm long SiNWs, to a maximum of $\sim 5.7 \times 10^{17}$ cm^{-3}, for the 65 μm SiNWs.

In the case of the 90 μm SiNW array, the predicted carrier density is $\sim 7.2 \times 10^{18}$ cm^{-3}, which corresponds to a heavily doped n-Si sample.



Sample	*S (μV/K)*	*E_F - E_V (eV)*	*p (cm^{-3})*
Bulk Si	640	0.15	7.1 10^{16}
Si NWA 30 μm	680	0.17	4.5 10^{16}
Si NWA 40 μm	915	0.23	2.9 10^{15}
Si NWA 65 μm	460	0.1	5.7 10^{17}
Si NWA 90 μm	-250	0.04	7.2 10^{18}

Figure 4.9: Voltage vs. ΔT of p-type Si NW arrays of length 30, 40, 65 and 90 μm. Seebeck coefficient of bulk Si and SiNW arrays samples is reported in the table on the right hand side. In the table are also shown the calculated $E_F - E_V$ and the carrier density p.

The data illustrate a strong influence of the NW surface on the NW Fermi level. Furthermore, the 90 μm long SiNW sample manifests carrier inversion, which may be related to positive fixed charge trapped at the NW surface. These trapped charges can lower the conduction band energy edge E_C and the valence band energy edge E_V in the NW, relative to the Fermi energy E_F and invert the NW from p- to n-type. This inversion has been observed in Zaremba-Tymieniecki *et al.* [121], Boukai *et al.* [122] and Jie *et al.*[123]. In Zaremba-Tymieniecki *et al.* [121], a p-type SiNW transistor operated as an n-channel FET. In Boukai *et al.* [122], a positive S was measured for an individual n-type bismuth nanowire of 55 nm length. Similar behaviour was observed in Jie *et al.* [123], where the electrical characteristics of n-type SiNWs show p-type behaviour. Here, Jie *et al.* [123] argues that the transport properties of the SiNWs are strongly influenced by the surrounding ambient and surface conditions of the SiNWs. Jie *et al.* [123] suggest that in normal ambient conditions, there is absorption of gas molecules such as oxygen and humidity that trap electrons on the surface of SiNWs, causing surface band bending. As

a consequence, the excess holes from surface absorption may compensate the electrons in the NWs, converting the NWs to p-type.

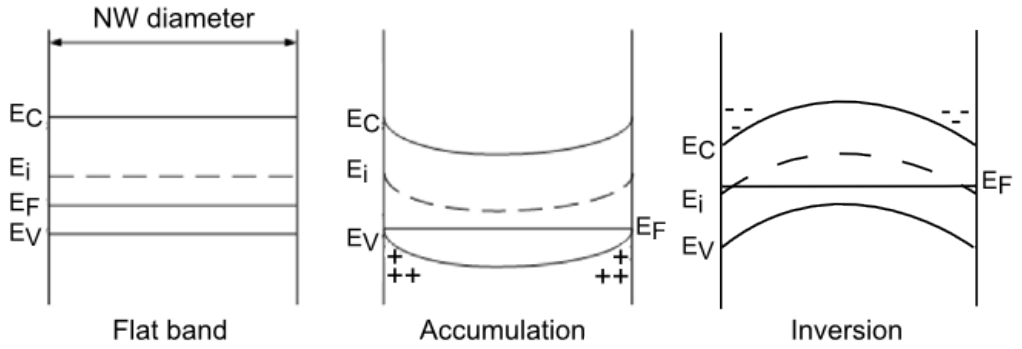
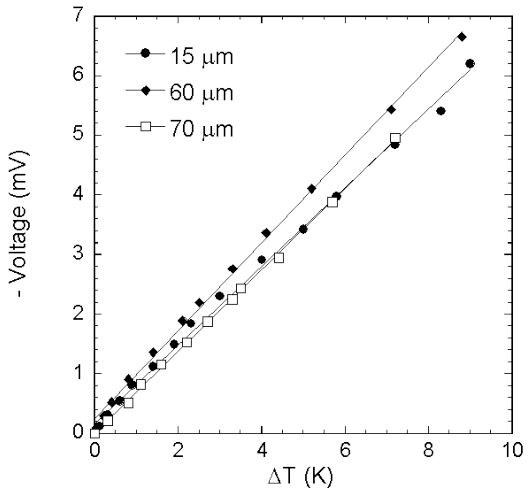


Figure 4.10: Energy band diagram of a p-type NW in the ideal case of flat bands, accumulation of holes and inversion of charge carriers. E_i is the intrinsic Fermi energy. Electrons are represented by the "minus" sign, and holes by the "plus" sign.

Fig. 4.10 illustrates the energy band diagram of a p-type NW in the ideal case of flat bands, accumulation and inversion. Flat bands would occur when there is no charge trapped at the surface of the NW. When the Si atoms at the surface of the NW react with atoms in the atmosphere, O_2 and H_2O_2, that donate holes into the NW (trap electrons), there is an accumulation of holes near the surface that causes the bands to bend upwards. This corresponds to accumulation. In the case of Si atoms at the surface of the NW reacting with atoms that act as electron donors, the number of electrons at the surface is larger than that of holes, creating downward bending. In this case, there is an inversion of charge carriers near the surface. A similar situation applies to n-type NWs. Furthermore, the presence of the surface state charge, or defects at the surface, can cause the Fermi level to be pinned at the Si surface at a position of approximately one third of the band gap [96]. An inversion of charge carriers from n- to p- type and viceversa has also been observed in CNT when exposed to oxygen (section 1.6.3).

4.4.3 *n*-type silicon nanowire arrays



Sample	S(μV/K)	E_C-E_F(eV)	n(cm^{-3})
Bulk Si	-425	0.09	$9.4\,10^{17}$
Si NWA 15 μm	-660	0.16	$5.5\,10^{16}$
Si NWA 60 μm	-740	0.16	$6.2\,10^{16}$
Si NWA 70 μm	-680	0.17	$4.9\,10^{16}$

Figure 4.11: Voltage vs. ΔT of n-SiNW array samples of length ∼15, 60, 70 μm. The measured S, the calculated $E_C - E_F$ and the calculated carrier density n are reported on the table on the right hand side.

Graphs of voltage as a function of ΔT, for n-SiNW arrays of length 15, 60, 70 μm, are shown in Fig. 4.11. The measured S, the calculated $E_C - E_F$ and the carrier density n are tabulated in the table of Fig. 4.11. Eq. 2.30 and 2.20 have been used to calculate $E_C - E_F$ and n, in a similar way as discussed in section 4.4.2. From data in the table of Fig. 4.11, it is possible to see that S is greater for the 60 μm long SiNW array than the 15 and 70 μm long SiNW arrays. The etching conditions of n-type Si were the same as for the p-type. However, it was not possible to obtain n-Si NW arrays with length beyond 70 μm. This may be related to difference in the ambient temperature conditions or the difference in the doping level. $E_C - E_F$, given in the table in Fig. 4.11, increases as the length of the wires increases, leading to a lower doping level. The calculated doping level n for bulk Si is more than an order of magnitude higher than the wafer supplier. In n-type NWs, the doping level shows smaller changes than in p-type NWs, with a minimum of $\sim 4.9\times10^{16}$ cm^{-3} for the 70 μm long SiNWs, and a maximum of $\sim 6.2\times10^{16}$ cm^{-3} for the 60 μm long SiNWs. As for the p-type SiNW arrays, this denotes influence of the NW surface on the Fermi level. As described earlier, modulation of the doping level can occur in the NWs as a consequence of interaction of surface atoms with the atmosphere.

Fig. 4.12 shows S for n- and p-type SiNW arrays as a function of length of the array. As

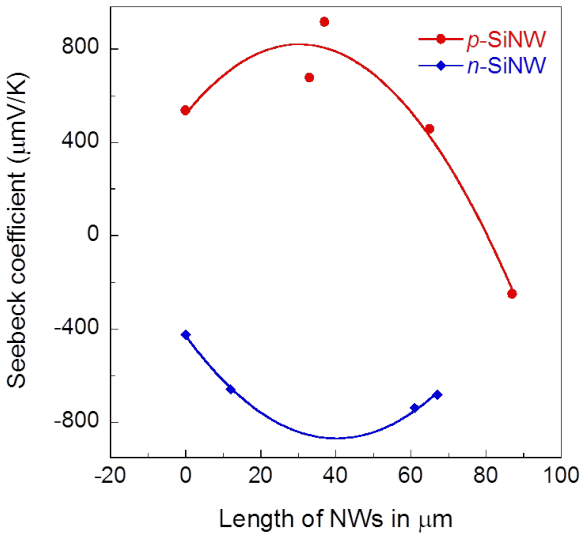


Figure 4.12: Seebeck coefficient NW length dependence for n- and p-type SiNW arrays. The solid lines are a guide to the eye.

for case of the p- and n-type, the absolute value of S slowly increases to a maximum and then decreases. The maximum magnitude for S occurs at approximately a similar length for both p- and n-type SiNWs, $\sim 30 - 40$ μm. As the length of the NWs goes beyond the 40 μm, S starts to slowly decrease in magnitude. Fig. 4.12 indicates that there is an optimum length of the NWs, corresponding to $\sim$30 to 40 μm for both n- and p-type SiNWs. Furthermore, in the case of p-type SiNWs, an inversion of the charge carriers is observed, leading to a negative S. The value of the optimum length may depend on the phonon mean free path, or it may be associated with the strong influence of the surface of the NW on the NW Fermi level.

5 Transient thermoelectric measurements

This chapter discusses the characterisation of SiNW arrays performed in a closed-cycle cryostat with moderate vacuum conditions, where a temperature range from 300 – 30 K can be reached. The measurements allows further investigation of the influence of the surrounding atmosphere and measurement of the temperature dependence of the NW arrays. Here, the temperature dependence of S in samples consisting of $\sim 10^{15}$ cm^{-3} and $\sim 10^{17}$ – 10^{18} cm^{-3} doped vertically-aligned SiNWs is measured. A transient technique to measure temperature and voltage across very thin samples is developed, allowing measurement of thermoelectric parameters. Both lightly- and moderately-doped SiNW array samples were measured, in order to characterise the effect of doping on the electron/phonon interaction and transport within the nanostructured material. We find $S_{NW} \sim 3S_{bulk}$ at room temperature, and $ZT_{NW} \sim 100ZT_{bulk}$. This demonstrates a large improvement in the TE properties of SiNWs compared to bulk Si.

5.1 Transient method

5.1.1 Measurement apparatus and its characterisation

Figure 5.1(a)-(b) show a schematic diagram and an image of the experimental apparatus used for transient measurements, respectively. The sample was sandwiched in between a bottom (cold) Cu 'heat' sink (temperature T_1) and a top Cu 'hot' reservoir (temperature T_2), allowing measurement of the temperature difference $\Delta T = T_2 - T_1$. We use a top Cu block with dimensions of 0.6 × 0.6 × 0.3 cm^3. An Oxford Instruments Si diode temperature sensor (substrate area 1.84 × 3 mm^2) is attached to the top Cu block with GE low-temperature varnish (C5-101) for good thermal contact. The Si diode operates in a temperature range of 475 – 1.4 K and is placed as close as possible to the sample to minimise temperature drops within the Cu. Here, the separation between the centers

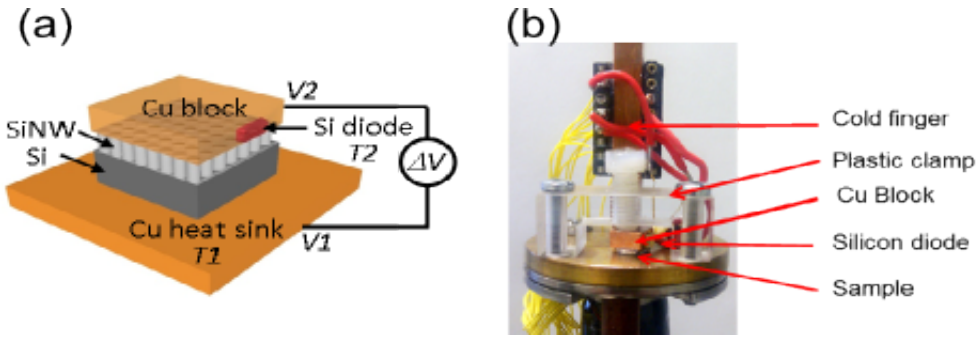


Figure 5.1: Measurement apparatus employed in the transient method. (a) schematic diagram and (b) image of the apparatus.

of the Si diode and the sample top surface is ∼0.2 cm. The bottom Cu block is formed by the cold finger of a Janis closed cycle refrigerator. Measurements were performed at a moderate vacuum (10^{-4} – 10^{-5} torr). Al foil (thickness 120 μm) at both Cu–sample interfaces is used to form a good thermal contact under pressure. Pressure is applied to the top Cu block using a polycarbonate screw and clamp, as can be seen from Fig. 5.1(b). The open circuit voltage difference ΔV between the top and bottom Cu blocks is measured using the high-resistance (1 GΩ) voltmeter in an Agilent 4155B semiconductor parameter analyser. This is also used to simultaneously measure the voltage output of the Si diode temperature sensor, which is then subsequently converted to temperature values.

As a starting point, the silicon diode is characterised with temperature. Fig. 5.2 shows the voltage temperature behaviour of the Si diode attached to the small Cu block. The experiment was performed without and with interfiller to verify any change in the thermal contact, where the interfiller was used to improve thermal and electric contacts and hence reduce the contact resistance between the two interfaces. In both cases, the data points behave in a similar way. A polynomial fit is used to interpolate the data. The best fit for the temperature of the Si diode is given by the equation $T_{Diode} = 616 - 803V_{Diode} + 548V_{Diode}^2 - 272V_{Diode}^3$.

Ideally, in S measurements, the temperature sensors should be mounted as close as possible to the either ends of the sample, to minimise a temperature offset. In typical measurements of S, the sample is comparatively long, such that the separation between the temperature sensor and the sample is small compared to the length of the sample [100]. However, in this work is not possible as thin samples are used, 500 μm and 975 μm in thickness.

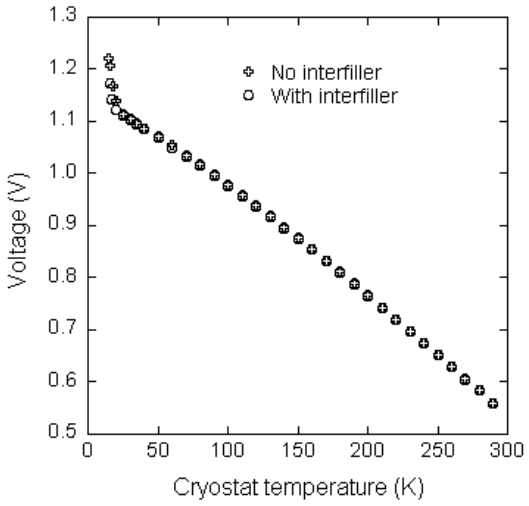


Figure 5.2: Voltage temperature dependence of Si diode without and with interfiller, to enhance thermal properties.

S is measured using a transient temperature and voltage technique, allowing characterisation of thin, large area samples. In contrast, in equilibrium measurements, a larger separation between the hot and cold ends of the sample is preferable to allow ΔT to be maintained at low heating power inputs to the Cu reservoir [30, 100]. In previous work single or small numbers of SiNWs were used, such that the thermal resistance was large and ΔT could be established at equilibrium [86, 87]. As we characterise $\sim 10^7$ to 10^8 NWs in parallel, the thermal resistance is reduced, making equilibrium measurements difficult. The transient measurement method is as follows. First the bottom Cu block temperature T_1 is reduced by 20 K. As a time lag exists for heat to flow and the temperature to equalise between the top Cu block at temperature T_2 and T_1, lower Cu block, this creates a small ΔT up to $\sim$2 K across the sample. ΔT and ΔV are then simultaneously measured as a function of time, from the point where T_1 is maintained at a constant base value by the cryostat temperature controller. Measurements are performed for base values of T_1 from 300 – 30 K.

The temperature drop within the top Cu block is characterised by measuring ΔT for three different temperature sensor–sample separations (0.34, 0.57 and 0.87 cm between sensor and sample top surface centers). A schematic diagram for the three configurations is illustrated in Fig. 5.3(a)-(c). Fig. 5.4 shows the temperature drop for the three different sensor-sample separation. The temperature at the sample top surface is $0.3\Delta T$ for the

0.2 cm sensor-sample separation in our measurements. As a consequence, the raw measured data will be corrected by this factor.

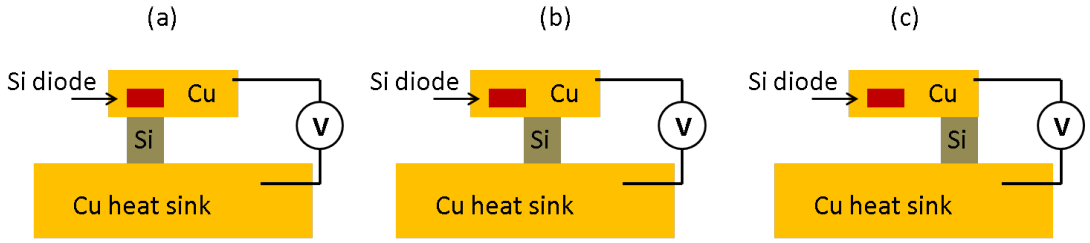


Figure 5.3: Schematic illustration for different temperature sensor–sample separation. (a) 0.34 cm, (b) 0.57 cm and (c) 0.87 cm separation.

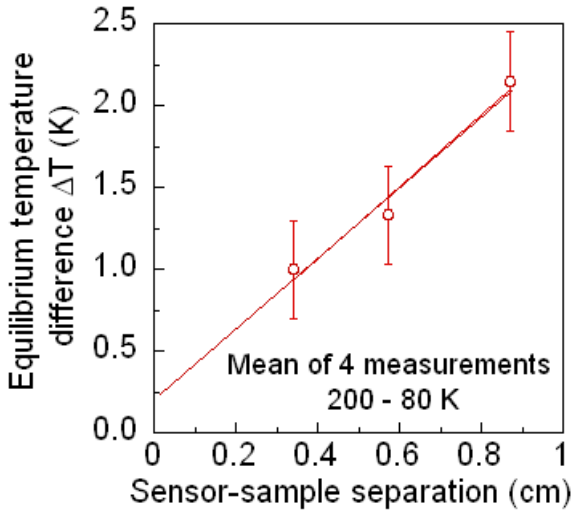


Figure 5.4: Equilibrium temperature dependence as a function of Si diode-sample separation.

Similarly, two thicknesses of bulk Si (375 μm and 975 μm) were characterised at different temperature points to estimate any Cu-Si interface temperature drops. Figure 5.5 shows the measured data as a function of Si length in the temperature range 260 – 140 K. The combined (top and bottom) interface temperature drop is small, $\sim 0.9\Delta T$. The inset in Fig. 5.5 shows the exponential of ΔT as a function of time for bulk Si at 160 K. The final

temperature, *i.e.* 160 K, corresponds to the temperature of the cold finger of the cryostat. Here, the temperature of the sample is measured as a function of time after the point when the cold finger reaches 160 K. Therefore, ΔT across the sample is given by the difference between the temperature of the top Cu block and the cold finger.

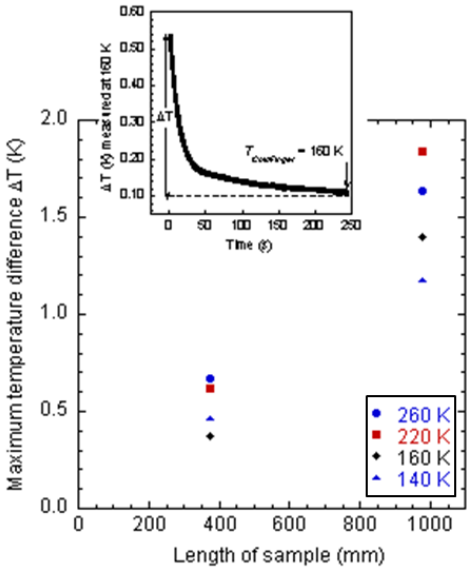


Figure 5.5: Temperature difference ΔT as a function of bulk Si samples length in a temperature range 260 to 140 K. Inset shows how ΔT is measured compared to the temperature set up at the cold finger of the cryostat.

5.1.2 Closed cycle refrigerator

The temperature characterisation of parent bulk Si and SiNW arrays of different length is obtained by using a Janis closed cycle refrigerator (CCR) or cryostat operating in the temperature range 325 K to <10 K, see Fig. 5.6. Here, the source of cooling is given by a closed loop of helium gas that is compressed and expanded based on the Gifford-McMahon (G-M) thermodynamic cycle [124]. The cryostat is composed of a cold finger, on which the sample is mounted. Removal of heat from the cold finger occurs during each expansion phase. This is provided with a heater and a thermometer used to precisely monitor the temperature of the sample. The temperature of the cryostat is monitored through a Lakeshore 331 Temperature controller. Once the chosen temperature is set, then Proportional (P), Integral (I) and Derivative (D) parameters can be entered in the temperature controller. The system is provided with auto-tuning of the PID values. However, in our



Figure 5.6: Janis closed cycle refrigerator utilised for temperature characterisation of SiNW arrays. Figure taken from Ref. given in footnote 1.

Table 5.1: PID values used for the temperature controller in the temperature range 300 – 20 K.

Temperature (K)	*P*	*I*	*D*	*Heater Range*
20 – 30	8	100	0	High
30 – 40	20	60	0	High
40 – 60	80	40	0	High
60 – 300	500	20	0	High

experiments, these were set manually. Generally, when operating at low temperatures, P should be low and I should high. D can remain zero throughout the entire operating range. At high temperatures, large proportional and small integral values can increase the stability and response time. Different combination of PID values were tried, but better control and stability was found with the values reported in Tab. 5.1, see footnote [1]. The last column indicates the heater range of the built-in heater provided with the cryostat. A 30% output of the high heater range was utilised during the experiments.

5.2 Measurement method and experiments on bulk silicon

Measurements were first performed on lightly-doped ($\sim 10^{15}$ cm^{-3}) n-type bulk Si and the data used as a reference for other samples. These measurements allow us to verify on

[1] http://www.triumf.info/wiki/bnmr/index.php/%CE%92-NMR/NQR_Manual#PID_Temperature_Control_for_the_.CE.B2NMR_cryostat. Visited on 1st of April 2013.

transient measurement method, in comparison with more conventional equilibrium measurements. Fig. 5.7(a) shows the exponential decays of ΔV and ΔT vs. time for bulk Si at 160 K. ΔV and ΔT decay exponentially, with similar time constants ~16 s or greater.

Figure 5.7(b) shows the measured exponential decay of ΔV vs. time for bulk Si, for final values of T_1 from 260 – 60 K. Figure 5.7(c) shows the corresponding measured ΔT vs. time curves. A constant offset of 0.3 mV and 0.3 K were added to the curves for clarity. These data can then be used to plot ΔV vs. ΔT, as shown in Fig. 5.7(d). $S = \Delta V/\Delta T$ is then calculated from the slope of the ΔV-ΔT plots. The curves are linear, corresponding to a constant S as expected for the small ΔT range, and the extracted values of S change with the base value of temperature. As the temperature is lowered, the time constants of the ΔV and ΔT exponentials become decreases, see Figure 5.7(b) and Figure 5.7(c), indicating an increase in the Seebeck coefficient. This is clearly visible in the ΔV-ΔT, plotted in Fig. 5.7(d). Here, the slope of ΔV-ΔT increases as the temperature decreases.

Figure 5.8(a) shows measured S_{Bulk} vs. temperature. Here are also reported the calculated S_d and the extracted S_p. S_d has been calculated by using equation

$$S_d = -\frac{k_B}{e}\left(\frac{E_C - E_F}{k_B T} + \left(r + \frac{5}{2}\right)\right) \tag{5.1}$$

Considering a doping concentration of 10^{15} cm^{-3}, E_F has been calculated by solving equation

$$n_d\left(1 - \left(\frac{1}{2}exp\left(\frac{E_D - E_F}{k_B T}\right) + 1\right)^{-1}\right) = N_C exp\frac{E_F - E_C}{k_B T} \tag{5.2}$$

S_p is given by $S_p = \frac{\beta v l_p}{\mu_e T} = S_{Bulk} - S_d$. At room temperature and above, phonon-phonon interaction (Umklapp scattering) is predominant, and β is ~ 0. This implies that S_p may be neglected at room temperature and $S_{bulk} \approx S_d$.

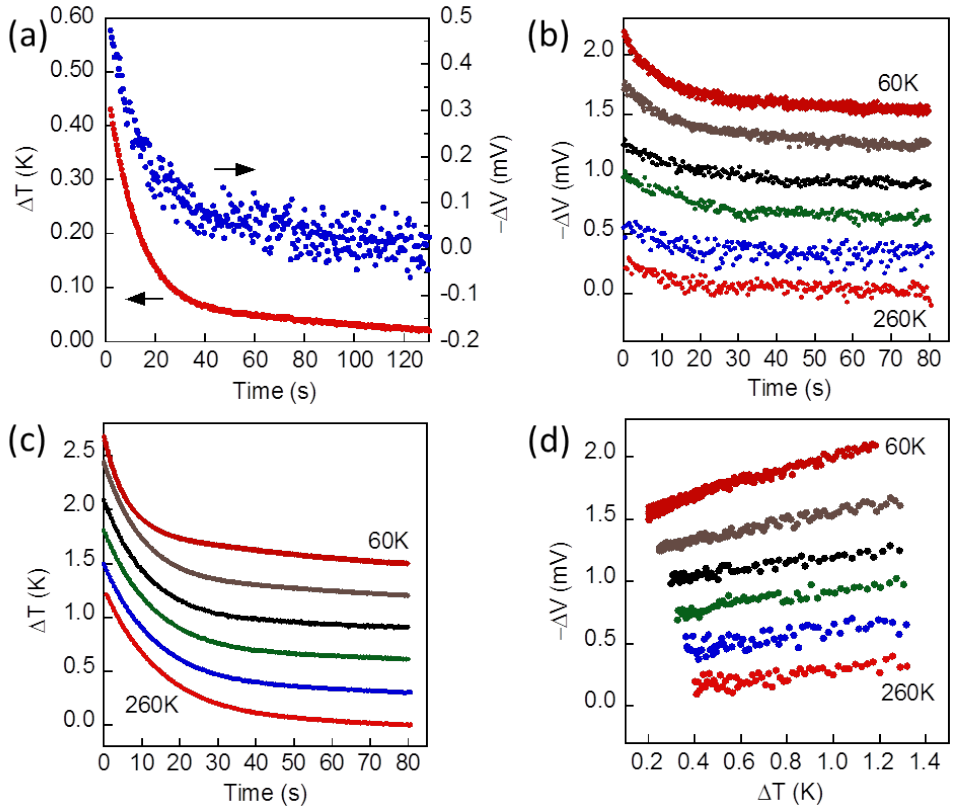


Figure 5.7: (a) ΔV and ΔT vs. time for bulk Si at 160 K. (b) ΔV vs. time for 260 – 60 K heat sink temperature, in 40 K steps. (c) ΔT vs. time for 260 – 60 K, in 40 K steps. (d) ΔV-ΔT plots for the data of (b) and (c). Curves in (b)-(d) and (c) are offset by 0.3 mV and 0.3 K per temperature step for clarity, respectively.

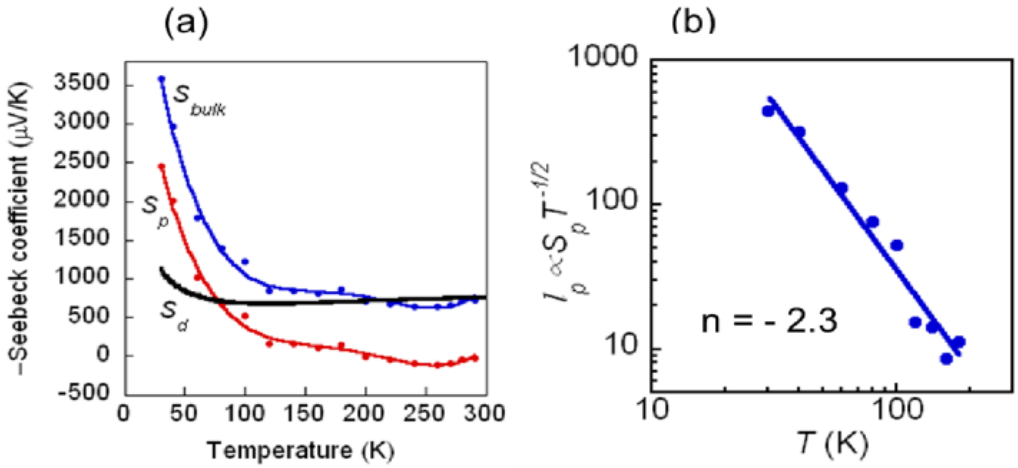


Figure 5.8: (a) S_{bulk} (measured), S_d (calculated) and S_p (extracted) vs. T in bulk Si. (b) $l_p \propto S_p T^{-1/2}$ vs. T [105].

As the temperature is lowered, Umklapp scattering becomes increasingly difficult, leading to $\beta > 0$. At low temperatures phonon-phonon interaction is almost void and $\beta \approx 1$ [37]. At 290 K $S_{bulk} \approx S_d \approx 730$ μV/K, S_{Bulk} is however slightly smaller than S_d from 220 K $<$ T $<$ 300 K, as we may have overestimated S_d if r < 0.5, or underestimated S_{Bulk} due to unaccounted interface temperature drops. S_p increases below ~250 K and below ~80 K, $S_p > S_d$ (e.g. at 30 K, $S_p = 0.7S_{Bulk}$). As expected, S_{Bulk} increases as a consequence of strong enhancement of phonon drag. This behaviour was also measured in a Si sample with doping level of $2.8{\times}10^{16}$ cm^{-3} in Ref. [84]. Furthermore, as $\mu_e \propto T^{-3/2}$ in lightly-doped Si and v, velocity of sound (see also Eq. 2.27) may be assumed to be constant, we have $l_p \propto S_p T^{-1/2}$, providing a means to obtain the temperature dependence of the phonon mean free path l_p from S_p. Fig. 5.8(b) shows the temperature dependence of l_p found by plotting $S_p T^{-1/2} \propto l_p$ vs. T on a log-log scale. A power-law dependence is found, with $l_p \propto T^n$ where $n = 2.3$. This is associated with the reduction in Umklapp scattering of phonons with reducing T and is similar to published data, where $n \sim 2.1$ [84].

5.3 Lightly doped nanowire arrays

Lightly-doped (10^{15} cm^{-3}) n-type Si is investigated as a means to reduce impurity scattering of electrons and phonons. At low doping levels, phonon drag is the dominant contribution to S at moderate to low temperatures (~200 – 30 K) [84]. Low doping levels disentangle impurity scattering from surface scattering and leave the NW dimensions as the main source of scattering, unlike heavily-doped SiNWs used in previous work [86, 87].

Below ~150 K, it was not possible to measure the SiNWs due to increasing sample resistance and because of the low doping level. This may be associated with a carrier freeze out that occurs in low doped materials. Fig. 5.9 shows the temperature change of electron density or carrier concentration for a Si sample with donor concentration of 10^{15} cm^{-3}, similar to the donor concentration of n-Si samples used in our experiments. In the temperature range of ~300 – 150 K, the electron density is constant (saturation regime). As the temperature is lowered beyond ~150 K, there is a rapid decline in the electron density. Furthermore, the voltage measurements across the Si sample present some background noise as a consequence of low doping and small voltage signal, *i.e.* ~0.5 mV.

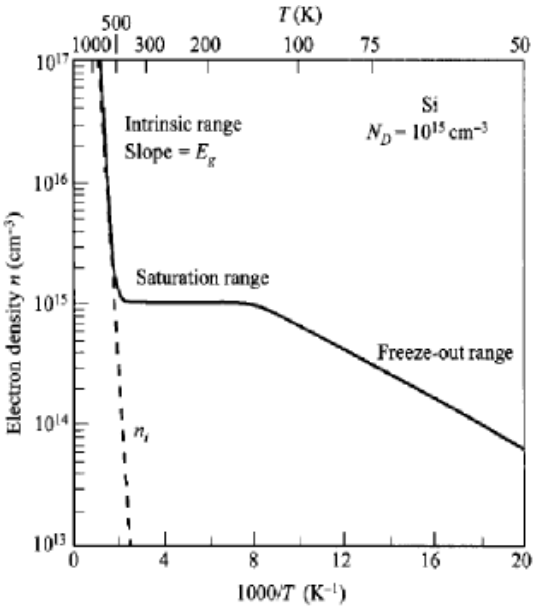


Figure 5.9: Temperature dependence of the carrier (electron) concentration for a Si sample with donor concentration of 10^{15} cm^{-3}. Figure taken from Ref. [96].

In addition, the time constants of the exponential decays for ΔV and ΔT are similar and very long ($\sim$10 s or greater). The electron distribution can then adjust as the temperature changes, and quasi-static conditions exist in the sample. This allows the use of equilibrium equations to quantify S. The equilibrium measurements on the SiNWs at room temperature give similar values of S to our transient measurements, see section 4.4.2 and 4.4.3. Finally, we consider the suitability of the top Cu block as a heat reservoir. The heat capacity of Cu $\sim$24 J/mol.K [125] and of Si is $\sim$20 J/mol.K [95]. The mass of the Cu block is 1 g and of the Si sample is 0.1 g. It then follows that the heat stored in the top Cu block is $\sim$9 times greater than in the Si sample. Fig. 5.10 shows ΔT as a function of time for bulk and SiNW samples at 160 K. The time constants for bulk (τ_B) and the SiNWs (τ_{SiNW}) are very different, with $\tau_B = 16.8$ s and $\tau_{SiNW} = 44.12$ s.

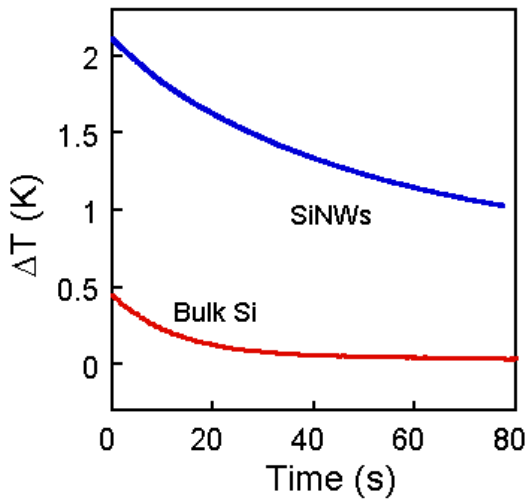


Figure 5.10: ΔT exponentials of bulk and SiNW arrays at 160 K.

(A) Measurements on 35 μm long SiNWs

Figure 5.11(a)-(b) show ΔV and ΔT exponentials as a function of time for the 35 μm long SiNW array in the temperature range of 290 – 150 K, with 20 K steps. A constant offset of 0.3 mV and 0.3 K were added to the curves for clarity purpose. Compared to bulk Si, the ΔV and ΔT curves in the 35 μm SiNW array do not show a significant change as the temperature decreases. In Fig. 5.11(a), the time constant of the ΔV exponentials increase as the temperature decreases. In a similar way, the time constants of the ΔT exponentials, within the temperature range 290 – 150 K, see Fig. 5.11(a), increases as T decreases.

The ΔV-ΔT data for this sample are shown in Fig. 5.12. As in the previous case, a 0.3 mV offset has been added to the curves for clarity. The change in the slope of ΔV-ΔT curves is different than bulk, with a slight decrease in the slope of the curves as the temperature is lowered, indicating a decrease in S with decreasing temperature. This is opposite to the bulk Si behaviour.

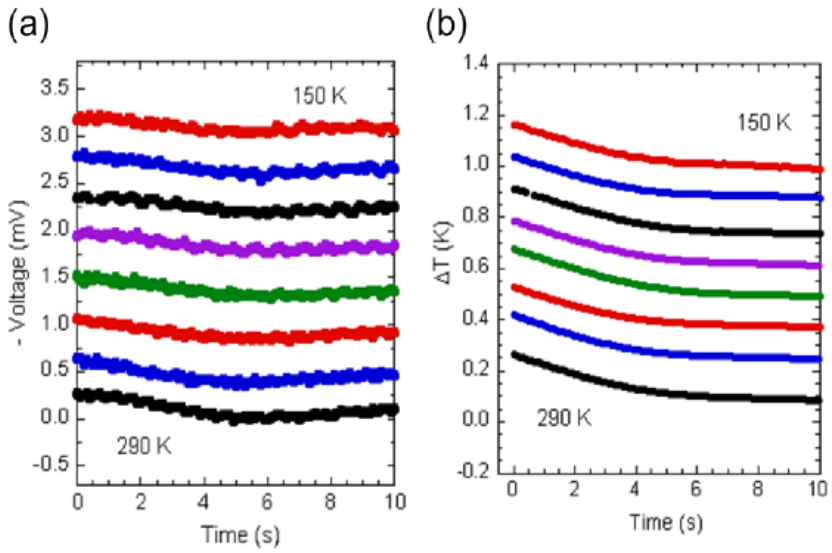


Figure 5.11: Characteristics of the 35 μm long SiNW arrays in a temperature range 290 – 150 K. (a) ΔV as a function of time, with 20 K temperature steps. (b) Temperature ΔT vs. time, with 20 K steps. The curves in (a) are offset by 0.3 mV, and curves in (b) are offset by 0.3 K for clarity.

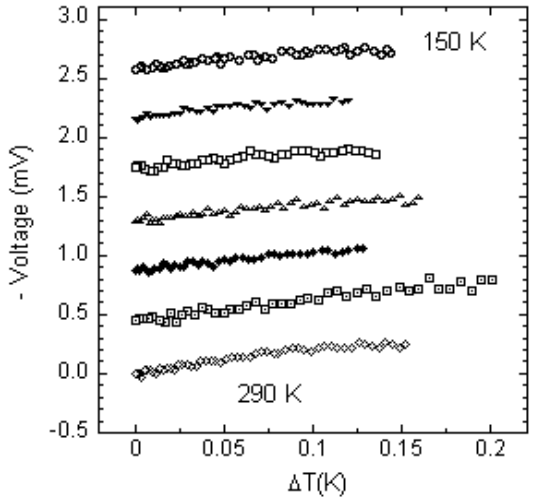


Figure 5.12: Voltage ΔV vs. ΔT for the 35 μm long SiNW arrays in the temperature range 290 – 150 K, with 20 K steps. Curves are offset of 0.3 mV for clarity.

(B) Measurements on 80 μm long SiNWs

Figure 5.13(a)-(d) show similar plots to those of the 35 μm long SiNW arrays. In Fig. 5.13(a)-(b), the time dependence of ΔV and ΔT exponentials are shown for the 80 μm long SiNW array in the temperature range of 290 – 150 K, with a 20 K measurement step.

Constant offsets of 0.3 mV to the ΔV curves and 0.3 K to the ΔT curves were added for clarity purpose, respectively. A maximum ΔV of ~0.3 mV, see Fig. 5.13(a), and a maximum ΔT of ~ 0.8 K, see Fig. 5.13(b) are measured across the 80 μm SiNW array at 290 K. In the case of ΔV, see Fig. 5.13(a), the time constants of the ΔV measured across the array increases as the temperature decreases. Similarly, the maximum ΔT measured across the SiNWs occurs at room temperature, *i.e.* 290 K.

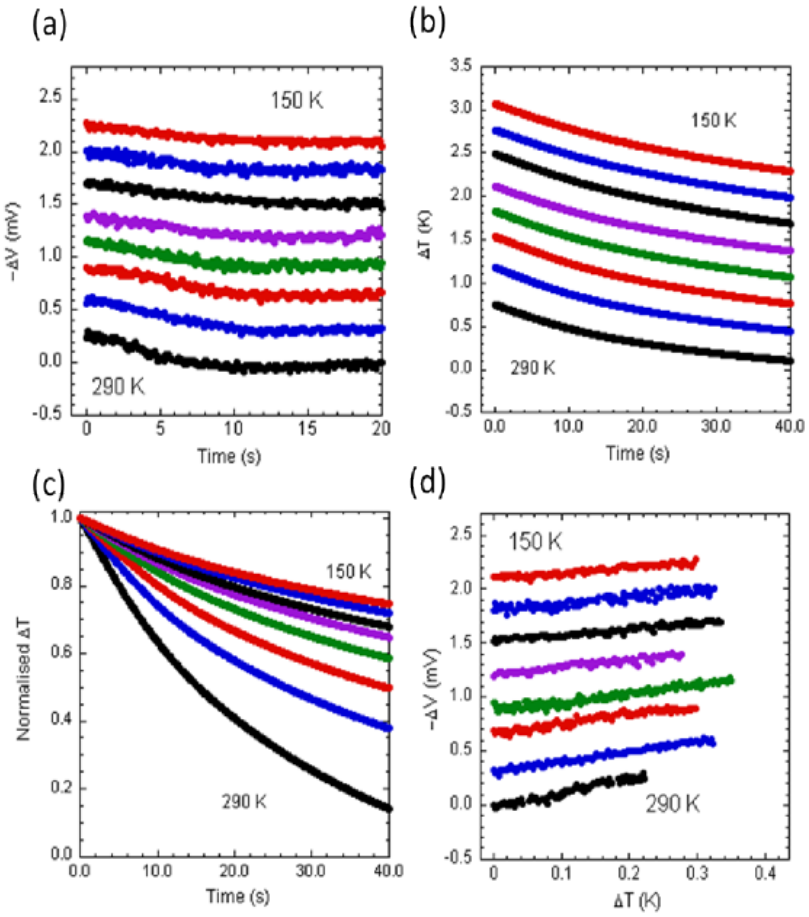


Figure 5.13: Characteristics of the 80 μm long SiNW arrays in a temperature range 290 – 150 K, with 20 K steps. (a) ΔV as a function of time. (b) ΔT and (c) Normalised ΔT vs. time, with respect to the first temperature point. (d) ΔV-ΔT plots. Curves in (a) and (d) are offset of 0.3 mV, while curves in (b) and (c) are offset of 0.3 K.

This is clearly visible by considering the normalised ΔT time dependence, shown in Fig. 5.13(c). Here, it is possible to see that the time constants of the ΔT exponentials across the SiNW arrays changes with T, with the time constant of the ΔT exponentials increasing as

the temperature decreases. Figure 5.13(d) shows the $\Delta V - \Delta T$ curves in the temperature range 290 – 150 K . In a similar way to the 35 μm SiNW array, the slope of the $\Delta V - \Delta T$ curves decreases as the temperature decreases, indicating a decreasing S.

(C) Measurements on 350 μm long SiNWs

Figure 5.14(a)-(d) show the temperature characteristics of the 350 μm long SiNW arrays. In Fig. 5.14(a)-(b), the time dependence of ΔV and ΔT exponentials are shown in the temperature range of 290 – 150 K , with a 20 K measurement step. Constant offsets of 0.3 mV and 0.3 K were added to the ΔV and ΔT curves for clarity purpose, respectively.

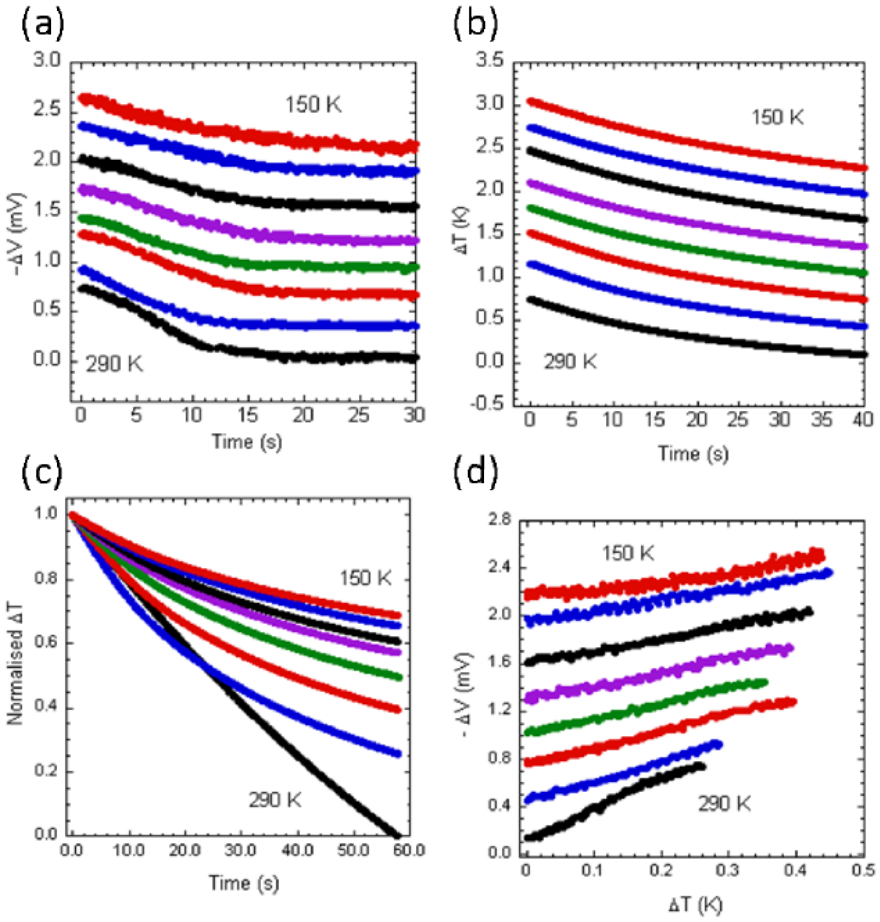


Figure 5.14: Characteristics of the 350 μm long SiNW arrays in a temperature range 290 – 150 K, with 20 K steps. (a) measured ΔV as a function of time. (b) ΔT as a function of time. (c) Normalised ΔT vs. time, with respect to the first temperature point. (d) ΔV–ΔT plots. Curves in (a) and (d) are offset for clarity of 0.3 mV, while curves in (b) and (c) are offset of 0.3 K.

Here, a maximum ΔV of ~0.6 mV, see Fig.5.14(a), and a maximum ΔT of ~0.7 K, see Fig. 5.14(b), are measured across the 350 μm SiNW array at 290 K. As the temperature decreases, the time constants of the ΔV exponentials across the vertically-aligned SiNWs increase. The time constants of the ΔT exponentials increase with decreasing temperature. This can be clearly seen in the normalised ΔT time dependence shown in Fig. 5.14(c), with the ΔT across the SiNW arrays changing in a similar way to the 80 μm SiNW arrays. Figure 5.14(d) shows the ΔV-ΔT curves in the temperature range 290 – 150 K, with 20 K steps. As in the previous cases, *i.e.* 35 μm and 80 μm SiNW array, the slope of the ΔV-ΔT curves reduces as the temperature decreases, indicating a decreasing S. All of the three NW samples manifest a behaviour that is opposite to their parent bulk Si, with a decreasing S as T decreases for the NWs.

5.3.1 Effect of the Si substrate in SiNW array measurements in lightly doped:

In the above measurement, the samples analysed are composed of the SiNW array with length L_{NW}, and the bulk Si substrate with length L_B. Both the SiNWs and the Si substrate contribute to the measured S in the system 'NWs + Bulk'. It is therefore necessary to extract the contribution of SiNW arrays S_{NW} from S, as follows.

First, S is expressed in terms of the voltage and temperature across the SiNW arrays and the bulk Si substrate, (ΔV_{NW}, ΔT_{NW}) and (ΔV_B, ΔT_B), respectively. Hence

$$S = \frac{\Delta V}{\Delta T} = \frac{\Delta V_{NW} + \Delta V_B}{\Delta T_{NW} + \Delta T_B} \tag{5.3}$$

Here, ΔV and ΔT are voltage and temperature across the sample. Furthermore, ΔV_{NW} and ΔV_B can be expressed as

$$\begin{aligned} \Delta V_{NW} &= S_{NW} \Delta T_{NW} \\ \Delta V_B &= S_B \Delta T_B \end{aligned} \tag{5.4}$$

Here, S_B is the Seebeck coefficient in the Si substrate. We now define the ratio

$$\frac{\Delta T_{NW}}{\Delta T} = \frac{\Delta T_{NW}}{\Delta T_{NW} + \Delta T_B} = \frac{1}{1 + \frac{\Delta T_B}{\Delta T_{NW}}} \tag{5.5}$$

However, ΔT_B and ΔT_{NW} are given by:

$$\begin{aligned} \Delta T_B &\propto \frac{1}{\kappa_B}\frac{L_B}{A_B} \\ \Delta T_{NW} &\propto \frac{1}{\kappa_{NW}}\frac{L_{NW}}{F \times A_B} \end{aligned} \tag{5.6}$$

(κ_B, L_B) and (κ_{NW}, L_{NW}) are the thermal conductivity and length in the bulk Si and SiNWs respectively, A_B is the bulk Si surface area, and F is the filling factor of the SiNW array. In our case, $F = 30\%$, while for κ_{NW} and κ_B, data from literature were used [84, 86], where SiNWs were fabricated by a MACE process. Here, κ_{NW} is used only to estimate ΔT across the SiNW and the bulk substrate. By substituting Eq. 5.6 into Eq. 5.7, we obtain:

$$\frac{\Delta T_{NW}}{\Delta T} = \frac{1}{1 + 0.3\frac{\kappa_{NW} L_B}{\kappa_B L_{NW}}} \tag{5.7}$$

It is also possible to calculate the ratio S_{NW}/S, given by:

$$\frac{S_{NW}}{S} = \frac{\Delta V_{NW}/\Delta V}{\Delta T_{NW}/\Delta T} \tag{5.8}$$

Furthermore,

$$\frac{\Delta V_{NW}}{\Delta V} = \frac{\Delta V_{NW}}{\Delta V_{NW} + \Delta V_B} = \frac{1}{1 + \frac{S_B \Delta T_B}{S_{NW} \Delta T_{NW}}} \tag{5.9}$$

Substituting Eq. 5.9 into 5.8 and solving for S_{NW}, we have:

$$S_{NW} = S\left(1 - \frac{S_B}{S}\right)\frac{\Delta T}{\Delta T_{NW}} + S_B \tag{5.10}$$

Here, $\Delta T/\Delta T_{NW}$ can be found from Eq. 5.7, S is the measured value of the SiNW/Si substrate sample, and S_B is measured directly on a bulk Si only sample.

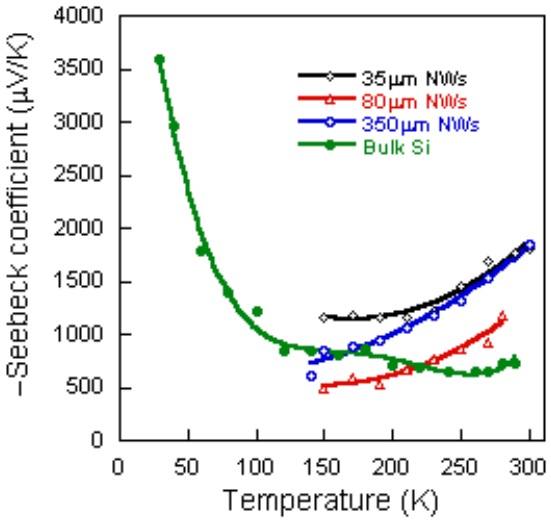


Figure 5.15: Measured S vs. T for SiNW array samples of ~35 μm, ~80 μm and ~350 μm. Bulk Si is also shown as a comparison.

5.3.2 Seebeck coefficient of nanowire arrays

Figure 5.15 shows the temperature dependence of the as measured S, obtained from the slope of the ΔV-ΔT curves, for the ~35, ~80 and ~350 μm vertically aligned SiNW arrays. Bulk Si is also shown as a reference. Here, the SiNW arrays include the contribution of bulk Si, *i.e.* SiNW + bulk Si. As predicted by theory [42] and experiments [84], S in bulk Si increases due to the contribution, at low temperatures, of the phonon drag. However, this is not the case of the SiNW arrays. All of the three arrays show a similar trend, with S decreasing as T decreases. Figure 5.16(a) shows S vs. temperature for the three SiNW arrays when bulk contribution has been removed [105].

At room temperature, $S_{NW} > S_{bulk}$ by up to ~3 times. However, S_{bulk} increases and S_{NW} decreases with decreasing T and at lower T, $S_{NW} < S_{bulk}$ (e.g. at 220 K for the 80 μm sample).

The increase in S_{bulk} is caused by strong enhancement of phonon drag [84]. The decrease in S_{NW} then implies suppression of the phonon drag. Typically $S_{bulk} = S_p + S_d$, where S_p is the phonon drag and S_d the electron diffusion component. In the phonon drag, momentum transfer from phonons to electrons via electron-phonon scattering increases the number of electrons reaching the cold side and therefore S. S_p is large in lightly-doped in comparison with heavily-doped materials as in the later case, impurity scattering of phonons suppresses S_p [84]. In lightly-doped bulk semiconductors, S_d is given by Eq. 2.30

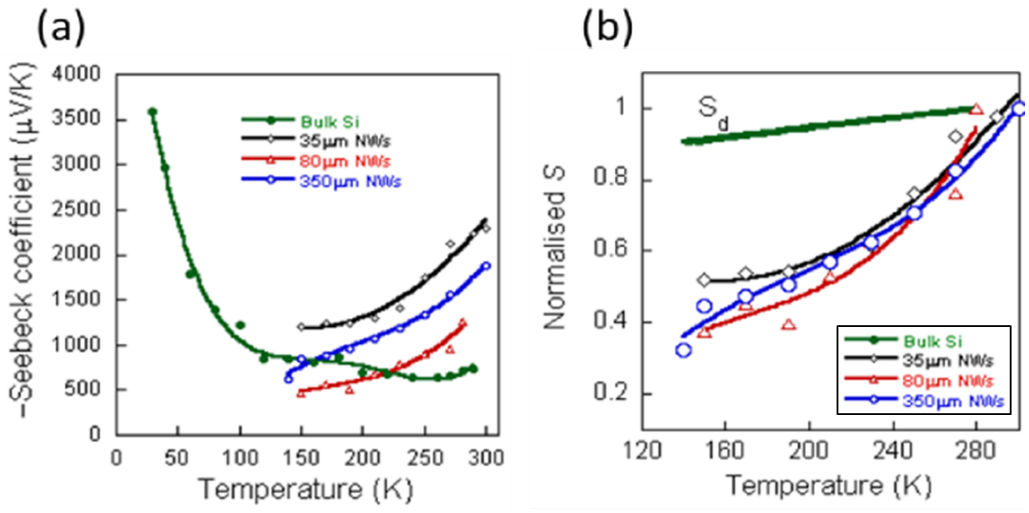


Figure 5.16: (a) S_{NW} as a function of temperature for SiNW samples of length ∼35, ∼80, ∼350 μm. Contribution of bulk has been removed. (b) S_{NW} normalised with the room-temperature values, for three samples, vs. T. S_d is shown for comparison [105].

[37, 44]. Finally, Fig. 5.16(b) shows S_{NW}, normalised to room-temperature values, as a function of temperature. All samples show a similar behaviour, demonstrating a 'universal' temperature dependence with the NW length.

In the lightly-doped NWs, impurity scattering of phonons is negligible and cannot suppress phonon drag. This leaves surface scattering due to restricted NW dimensions and surface roughness as the likely suppression mechanism. As $l_p \sim 1$ mm in lightly-doped bulk Si at 300 K, Ref. [84], and increases at lower temperatures (Fig. 5.8(b)), l_p is always greater than the NW diameter. Strong surface scattering of phonons in the NWs then limits $l_p \sim$ NW diameter and suppresses S_p. This is the same underlying mechanism for reduced κ in SiNWs, implying interdependence between S_{NW} and κ_{NW} [86, 126]. We also observe maximum $S_{NW} \sim 3S_{bulk}$ at room temperature (Fig. 5.16). This may be attributed to either a change in the scattering factor r (Eq. 2.27) due to the change in scattering mechanism from phonon to surface scattering, or an increase in $E_C - E_F$ due to surface effects. Finally, we estimate ZT in the NWs at 300 K [105]. Using the maximum $S_{NW} = 2300$ μV/K, $\kappa_{NW} = 8$ W/mK [86], and assuming σ in the NWs is unchanged from bulk, $ZT_{NW} = 0.005 \approx 100 ZT_{bulk}$. This suggests a very large improvement in the TE properties of lightly-doped SiNWs compared to bulk Si. Later, in Chap. 6, ZT is calculated using κ values measured in this thesis.

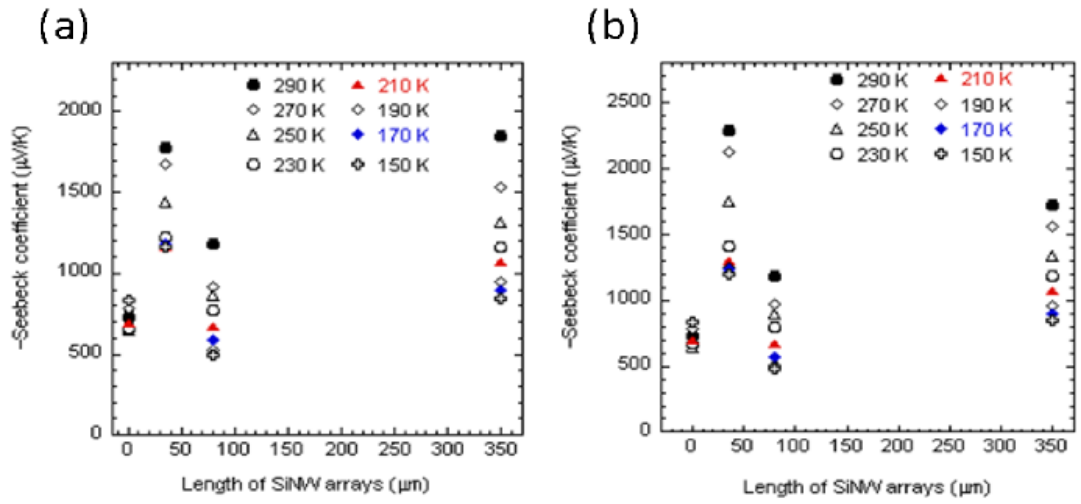


Figure 5.17: S as a function of SiNW arrays length in a temperature range 290 – 150 K, with 20 K steps. (a) with bulk contribution and (b) bulk contribution removed. The case of $L_{NW} = 0$ corresponds to the bulk Si data.

Figure 5.17(a)-(b) show the dependence of S versus the NW array lengths for 35 μm, 80 μm and 350 μm for the temperature points of 290 – 150 K, with 20 K steps, before and after removal of the bulk Si contribution. The bulk Si data have been considered for the case of zero NW length. In Fig. 5.17(a), the higher value of $S \approx$ 1900 μV/K is at 290 K for 350 μm long SiNWs. However, after bulk contribution is removed, the highest measured S is obtained for the 35 μm SiNW arrays. Hence, an increase in S is observed for the 30 μm long NW arrays. The S values decrease for the 80 μm long SiNW arrays, and increase again for the 350 μm long NW arrays. If the NW contribution is isolated to the bulk contribution, see Fig. 5.17(b), the 350 μm long NW arrays manifest a smaller S compared to the 35 μm long SiNW arrays. In this case, the maximum value of S is obtained for the 35 μm long SiNWs. This suggest that, in order to achieve a higher S an optimum length is required. This corresponds to 35 μm long SiNWs, when bulk contribution is not taken into consideration. The result is similar to that obtained in section 4.4.3, where the optimum length of the array, in both n- and p-SiNWs, ranges in between 30 – 40 μm. However, in the measurements of section 4.4.3 bulk contribution was not removed.

5.3.3 Fermi level and doping concentration

It is possible to calculate $E_C - E_F$ and doping level n for the 'NW + Bulk' samples, to observe how it changes with the length of the NWs. $S = S_d$ as S_p is suppressed, and S_d is

T = 280 K	35 μm	80 μm	350 μm
S (μV/K)	1804	1180	1853
S_{NW} (μV/K)	2293	1268	1886
$E_C - E_F$ (eV)	0.44	0.27	0.46
$(E_C - E_F)_{NW}$ (eV)	0.58	0.29	0.47
n (cm^{-3})	0.3×10^{12}	4×10^{14}	0.16×10^{12}
n_{NW} (cm^{-3})	0.1×10^{11}	1.4×10^{14}	0.11×10^{12}

T = 150 K	35 μm	80 μm	350 μm
S (μV/K)	1158	492	846
S_{NW} (μV/K)	1194	476	611
$E_C - E_F$ (eV)	0.14	0.04	0.095
$(E_C - E_F)_{NW}$ (eV)	0.15	0.039	0.059
n (cm^{-3})	5×10^{14}	1.17×10^{18}	1.9×10^{16}
n_{NW} (cm^{-3})	3×10^{14}	1.4×10^{18}	2.9×10^{17}

Table 5.2: $E_C - E_F$ and n have been calculated in the 'NWs + Bulk' and in SiNWs only at 280 K and 150 K.

the electronic contribution given by equation

$$S_d = -\frac{k_B}{e}\left(\frac{E_C - E_F}{k_B T} + \left(r + \frac{5}{2}\right)\right) \tag{5.11}$$

Using Eq. 5.11, we can calculate $E_C - E_F$. Tab. 5.2 shows the calculated $E_C - E_F$ in the system composed of 'NW + Bulk' and NW arrays only of ~ 35, ~ 80 and ~ 350 μm long, for two temperature points 280 K and 150 K. Given $E_C - E_F$, the doping level has been calculated by using equation

$$n = N_C exp(-\frac{E_C - E_F}{k_B T}) \tag{5.12}$$

In the case of the ~ 35 μm long SiNWs, after bulk contribution is removed, $E_C - E_F \approx 0.58$ eV. Hence, an intrinsic semiconductor is obtained or there may be a change in the scattering factor r. The data in Tab. 5.2 show that the NWs have a strong influence on the Fermi level and $E_C - E_F$ values are affected by the length of the NWs. .

5.4 Moderately doped nanowire arrays

We now discuss the characteristics of SiNWs with moderate doping. The NWs were n-type, phosphorous doped, with resistivity 0.01 – 0.03 Ωcm, corresponding to a doping level

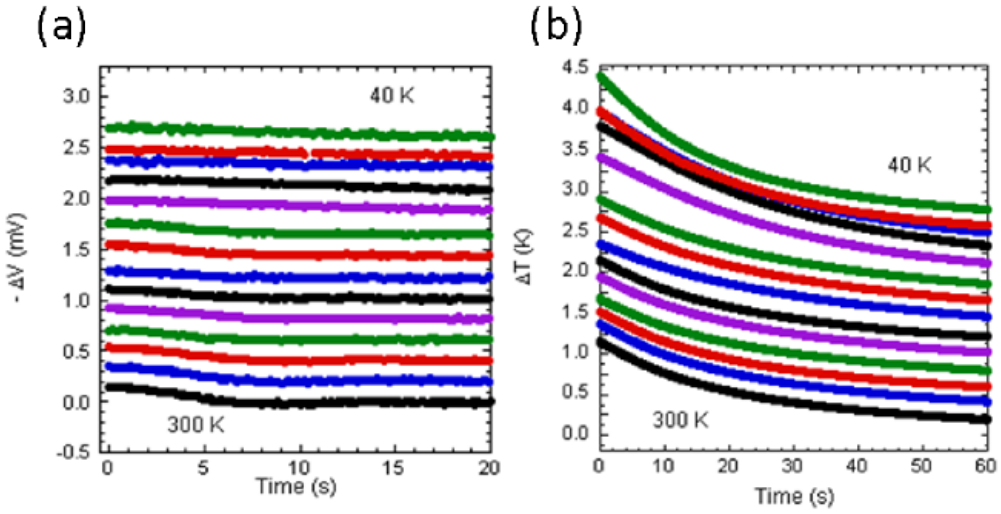


Figure 5.18: Temperature dependence of (a) ΔV and (b) ΔT as a function of time for bulk Si in the temperature range 300 – 40 K, with 20 K steps. Offsets of 0.2 mV and 0.2 K have been added to the curves for clarity, respectively.

10^{17} – 10^{18} cm^{-3}. The higher doping level corresponds to the onset of a heavily doped regime. In this regime, in contrast to the lightly doped samples, impurity scattering of phonons and electrons occurs, suppressing phonon drag even in bulk Si. However, there is a $\sim 10^2$ – 10^3 times increase in σ, leading to a potential large increase in $ZT = S^2\sigma T/\kappa$.

In a manner similar to section 5.2 and 5.3, S is measured in large arrays of SiNWs, with $\sim 10^8$ NWs in parallel. The analysed samples consist of SiNWs from $\sim$30 – 400 nm in diameter, with lengths $\sim$30 – 40 μm, and an average area of $\sim$0.25 cm^2. As discussed in section 5.2, a transient temperature and voltage measurement technique is used, allowing direct measurement of S in relatively thin (1 mm thickness) but large area samples. The measurement technique is identical to that discussed in section 5.2, with a transient measurement of both ΔT and ΔV vs. time, allowing extraction of the corresponding ΔV vs. ΔT curves and hence of S.

(A) Bulk Si measurements

Figure 5.18(a)-(b) show measurements of (ΔV, ΔT) as a function of time in bulk Si, respectively, for the temperature range 300 – 40 K, with 20 K steps. Offset by 0.2 mV and 0.2 K have been added to ΔV, and ΔT, respectively. The time constant of the ΔV exponentials decreases as the temperature decreases. In the case of ΔT curves, shown in Fig. 5.18(b), the maximum ΔT measured across bulk is $\sim$1 K at 300 K. The ΔV-ΔT plots

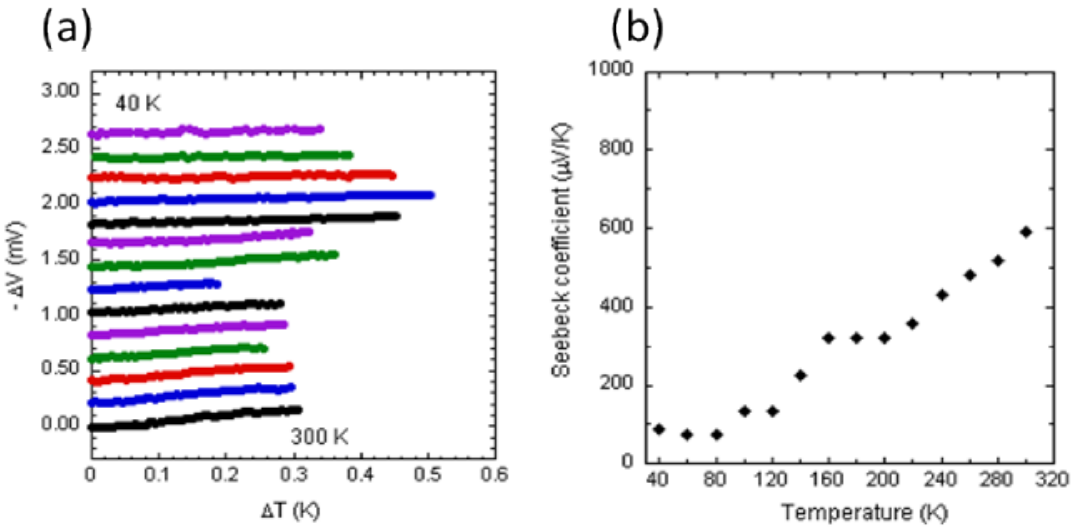


Figure 5.19: (a) ΔV-ΔT curves for bulk Si in the temperature range 300 – 40 K, every 20 K step. The curves are offset of 0.2 mV for clarity. (b) S_{Bulk} temperature dependence in 300 – 40 K.

of bulk Si are shown in Fig. 5.19(a). As expected, the change in the time constants for the exponentials increases slowly with temperature. This indicates a decreasing S, with decreasing temperature. Fig. 5.19(b) shows S_{Bulk} vs. temperature. In contrast to the lightly doped Si bulk sample (Fig. 5.11), we do not observe an increase in S associated with phonon drag as T reduces, as ionized-impurity scattering of phonons suppresses the phonon drag. Results for bulk Si are similar to those in Ref. [84], where $S_p = 0$, as it is suppressed.

(B) 30 μm SiNW array measurements

Figure 5.20(a)-(b) show the time dependence of ΔV and ΔT in a temperature range of 300 – 80 K, respectively. As in the previous cases, curves are offset 0.3 mV for ΔV and 0.3 K for ΔT. As the sample doping level of the SiNW arrays is much higher than the lightly doped NW samples discussed in section 5.3, ΔV can be measured even for temperatures well below the ~150 K, possible in the lightly doped NWs. The voltage signal across the sample can be measured up to 80 K. The maximum ΔV measured across the 30 μm SiNW arrays is ~2 mV at 300 K, see Fig. 5.20(a). The ΔV exponentials reach equilibrium after ~50 s, such that the ΔV across the SiNWs is almost zero. The time constants of the ΔV exponentials increase slowly with decreasing temperature. The time constant of the ΔT exponentials behaves in a similar way to the ΔV exponentials, see Fig.

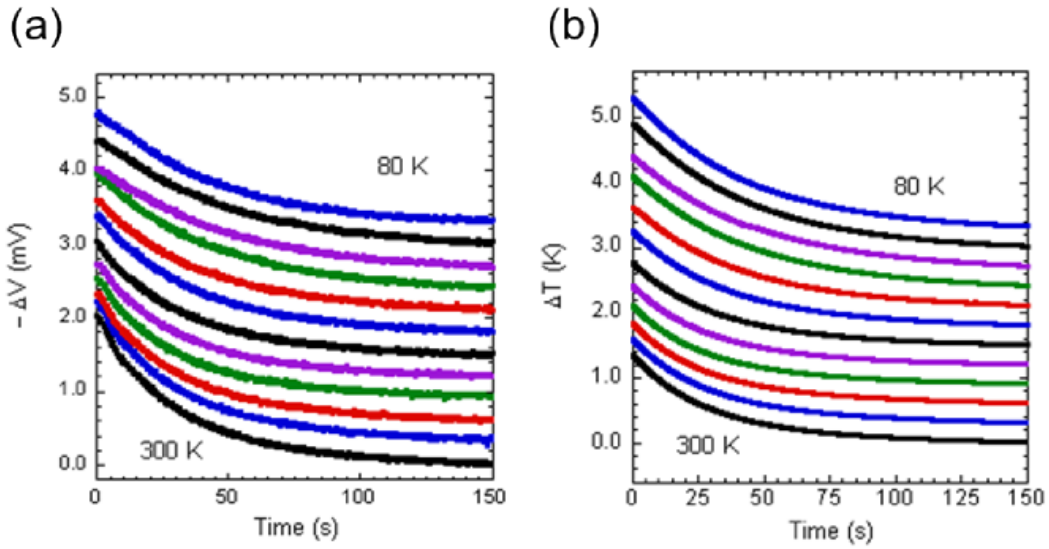


Figure 5.20: Characteristics of the 30 μm long SiNW arrays in a temperature range 300 – 80 K, with 20 K steps. (a) measured ΔV as a function of time. (b) Temperature difference ΔT measured as a function of time.

5.20. The maximum ΔT measured across the sample is ~1.1 K, at 300 K.

Figure 5.21 shows the ΔV-ΔT curves for the data shown in Fig. 5.20(a)-(b), with 0.3 mV offset added to the curves for clarity. The slope of the ΔV-ΔT curves slowly decreases as the temperature is lowered. This indicates that S decreases with decreasing temperature. It is important to note that the ΔV-ΔT curves are linear. This allows clear measurement of $S = \Delta V/\Delta T$ in the samples.

(C) 40 μm SiNW array measurements

Figure 5.22(a)-(b) show the time dependence of ΔV and ΔT exponentials in the temperature range 300 – 40 K, with 20 K steps. The maximum ΔV across the SiNW sample is < 0.5 mV at 300 K, see Fig. 5.22(a). The time constant of the ΔV exponentials increases slowly with time as the temperature decreases. In comparison to the 30 μm long SiNW arrays, ΔV exponentials have a time constant much smaller, *i.e.* after ~10 s ΔV approaches zero. ΔT vs. time, see Fig. 5.22(b), behaves in a similar way to the ΔV curves.

The ΔV-ΔT curves of the 40 μm SiNW sample are shown in Fig. 5.23. A maximum ΔT of ~0.5 K is obtained at 80 K and 100 K. The slope of the curves decreases as the temperature decreases, indicating a decreasing S as the temperature decreases. The ΔT measured across the 40 μm SiNW sample is ~3 times smaller than the 30 μm long SiNW.

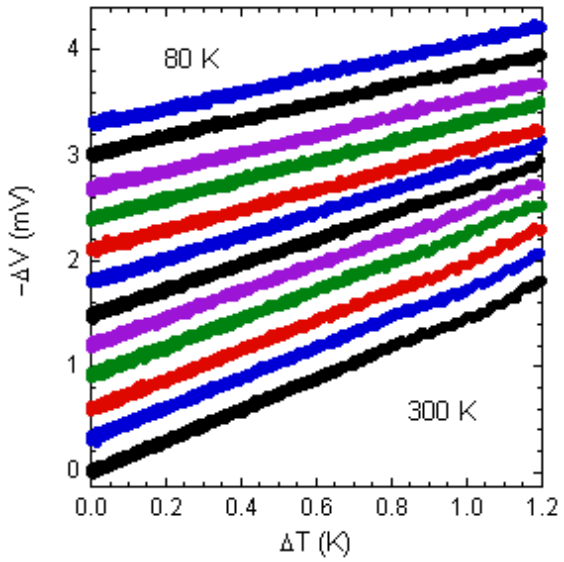


Figure 5.21: ΔV-ΔT for 30 μm SiNW arrays in the temperature range 300 – 80 K. Curves are offset of 0.3 mV, for clarity.

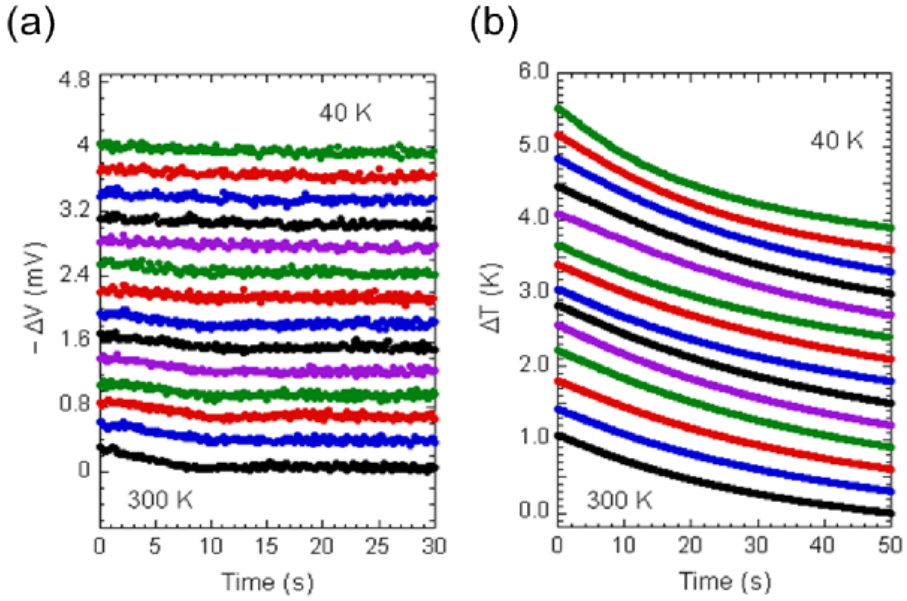


Figure 5.22: Characteristics of the 40 μm long SiNW arrays in a temperature range 300 – 40 K, with 20 K steps. (a) ΔV exponentials as a function of time. (b) ΔT exponentials as a function of time. Curves in (a) are offset of 0.3 mV and in (b) of 0.3 K.

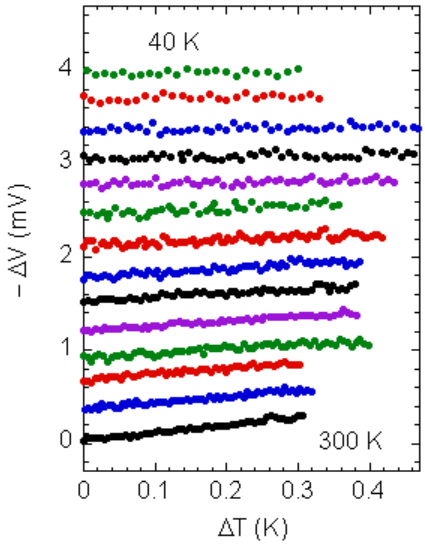


Figure 5.23: ΔV–ΔT for 40 μm SiNW arrays in the temperature range 300 – 40 K. Curves are offset for clarity of 0.3 mV .

Similar is the case for ΔV. It was not possible to obtain SiNW arrays longer than 40 μm for the moderately doped wires due to non-linearity of the NW length with time, see Chap. 3.3.3. Figure 5.24(a)-(b) show S measured in a temperature range 300 – 40 K for parent bulk Si, ∼30 μm and ∼40 μm SiNW arrays. In Fig. 5.24(a) bulk contribution to the SiNW samples has not been removed.

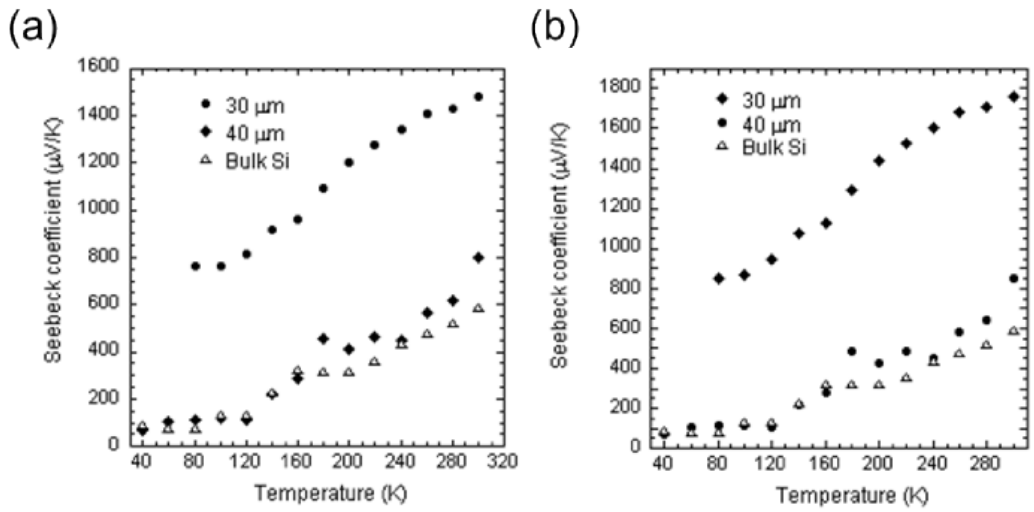


Figure 5.24: Temperature dependence of S in SiNW arrays for the 30 μm and 40 μm long SiNWs, doped n-type 10^{17} – 10^{18} /cm^3. (a) bulk contribution is included, (b) bulk contribution has been removed. The temperature range is 300 – 80 K for the 30 μm long SiNWs and 300 – 40 K for 40 μm long SiNWs.

Fig. 5.24(b) shows the Seebeck coefficient of SiNWs S_{NW} after removal of bulk contribution. Here, S_{NW} has been obtained by using Eq. 5.10, with a filling factor of 30%, where the filling factor is given by the ratio of bulk cross section area to SiNW cross section area. $\Delta T/\Delta T_{NW}$ is then given by Eq. 5.7, where κ_{NW} and κ_{Bulk} values were taken from literature data [84, 86]. In Fig. 5.24(a)-(b) SiNW samples follow a similar trend to bulk, but in the case of the ~30 μm SiNW array there is a remarkable increase in S. S of the 30 μm SiNW sample is ~1480 μV/K at 300 K, whereas $S_{Bulk} \simeq 590$ μV/K. This corresponds to an increase by a factor of 2.5. Removal of the bulk contribution leads to $S_{NW} \simeq 1760$ μV/K, implying an increase by a factor of ~3 over S_{Bulk} and that $S_{NW} \simeq 1.2S$. In the case of the 40 μm SiNW array, before removal of the bulk contribution, S is slightly higher than S_{Bulk} at 300 K, $S \simeq 800$ μV/K, with an increase of only ~1.35. When bulk is removed, $S_{NW} \approx 850$ μV/K, this corresponds to an increase by a factor of ~1.44 over S_{Bulk}. Both SiNW arrays manifest a higher Seebeck coefficient than bulk Si. After removal of bulk contribution, S_{NW} increase with respect to S of 'NW + Bulk' are even higher to the case of bulk contribution. In the 30 μm SiNW array most of the component of S, *i.e.* 84%, is due to the presence of NWs. In a similar way, in the 40 μm SiNW array 70% of the contribution to S is due to the NWs. This indicates that the NW

arrays are the most contributing part in the 'NW + Bulk' structure. After removal of bulk, S_{NW} is higher than S, where $S = S_{NW} + S_{Bulk}$.

Fig. 5.25(a)-(b) show S and S_{NW}, respectively, as a function of the NW length in the temperature range 300 – 40 K. In the case of NW length equal to zero, S_{Bulk} values have been considered. Before removal of bulk contribution, see Fig. 5.25(a), the difference between S measured at 300 K and at 80 K, is ∼700 μV/K, similar for the two NW lengths. This difference increases when the bulk contribution is removed. The difference between (S_{NW}, 300 K) and (S_{NW}, 80 K), see Fig. 5.25(b), is ∼1000 μV/K for the 30 μm SiNW array and ∼800 μV/K for the 40 μm SiNW array. The plots shown in Fig. 5.25(a)-(b) indicate that there is a maximum S around 30 μm long SiNWs and this peak is further emphasised after removal of bulk contribution. This is a similar result to that observed in Chap. 4.4.3 and 5.3.2.

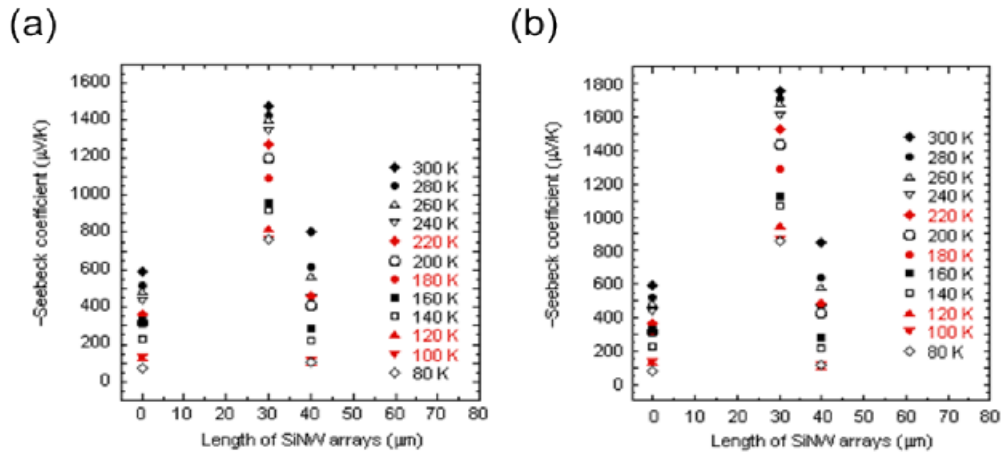


Figure 5.25: S as a function of SiNW arrays length in a temperature range 300 – 80 K. (a) S before removal of bulk contribution and (b) after removal of bulk. $L_{NW} = 0$ corresponds to the bulk Si data.

5.4.1 Fermi level and doping concentration

The resistivity of the n-Si sample is 0.01 – 0.03 Ωcm, corresponding to a doping level of 10^{18} – 10^{17} cm^{-3}. Here, the higher doping level represents the onset of a heavily-doped regime. In this case, S_d is then given by

$$S_d = \frac{\pi^2 k_B^2}{3e} T \left(\frac{r + 3/2}{E_C - E_F} \right) \tag{5.13}$$

Table 5.3: $E_C - E_F$ and n have been calculated in the 'NWs + Bulk' and in SiNWs only at 300 K.

T = 300 K	30 μm	40 μm
S (μV/K)	1480	800
S_{NW} (μV/K)	1760	850
$E_C - E_F$ (eV)	0.38	0.18
$(E_C - E_F)_{NW}$ (eV)	0.46	0.19
n (cm^{-3})	1.2×10^{13}	3.3×10^{16}
n_{NW} (cm^{-3})	0.5×10^{12}	1.84×10^{16}

However, as the doping of our sample is moderate, away from the conduction band, S_d is extracted using Eq. 5.11 of the lightly doped Si. S_d is calculated using a doping level of 10^{17} cm^{-3} and a scattering factor $r = 3/2$, valid for the case of phonon scattered by dopants. At 300 K, the calculated S_d is equal to 610 μV/K and agrees well with the measured S_{Bulk} ≈590 μV/K, this represents only 3% discrepancy between the measured value and the theoretical value. At temperatures below room temperature, the discrepancy between S_d and S_{Bulk} increases. This may be related to impurities present in our Si sample. Using Eq. 5.11, where S_d has been taken to be equal to the measured S, $E_C - E_F$ and n have been calculated in 'bulk + NW' system and 'NW array only' for $\sim$ 30 and 40 μm long, at 300 K. These data are tabulated in Tab. 5.3. Before removal of the bulk contribution, $E_C - E_F$ = 0.38 eV and 0.18 eV, for the $\sim$ 30 and 40 μm long SiNW arrays, respectively. These values correspond to a doping level of 1.2×10^{13} cm^{-3} and 3.3×10^{16} cm^{-3}. Hence, in the case of the 30 μm long SiNW arrays, the sample has lost many electrons, with the sample having changed from moderate-doped to lightly-doped. Instead, in the 40 μm long SiNW arrays, the number of electrons lost is only an order of magnitude. This explains the difference in S between the 30 and 40 μm long SiNW arrays. After removal of bulk contribution, $E_C - E_F$ slightly increases with values of 0.46 eV and 0.19 eV, for the $\sim$ 30 and 40 μm long SiNW arrays, respectively. In this case, the doping level in the SiNWs, n_{NW}, is 0.5×10^{12} cm^{-3} and 1.84×10^{16} cm^{-3}. The doping level within the NWs is even lower than 'bulk + NW' system, indicating that electrons may be lost at the NW surface. As for the lightly-doped SiNW arrays, results for the moderately-doped Si indicate a strong influence of the NWs on the NW Fermi level. Furthermore, $E_C - E_F$ and hence n are affected by the length of the NW. In the case of the $\sim$ 35 μm long SiNWs, after bulk contribution is removed, $E_C - E_F \approx 0.58$ eV. Hence, an intrinsic semiconductor is

obtained or there may be a change in the scattering factor r. The data in Tab. 5.3 show that the NWs have a strong influence on the Fermi level and $E_C - E_F$ values are affected by the length of the NWs.

6 Electrical and thermal conductivity measurements

In the first part of this chapter, we present two terminal I-V measurements of SiNWs, fabricated by the MACE process, for two different doping levels, 5×10^{15} – 5×10^{14} cm^{-3} and 10^{18} – 10^{17} cm^{-3}. The I-V curves are characterised in the temperature range 300 – 40 K. The conductance of the samples is extracted, as it is not possible to measure electrical conductivity accurately in a two terminal measurement.

The temperature dependence of the I-V characteristics is measured for n- and p-type polymer filled NWs. Polymer filled SiNW measurements were analysed to study any changes in the electrical characteristics of the NWs, when the NW surface is passivated. An Agilent 4155 parameter analyzer with a probe station was used to measure the room temperature I-V, and a closed-cycle refrigerator, described in section 5.1.2, was used to obtain measurements in the temperature range 300 – 40 K.

In the second part of this chapter, a transient heat measurement technique is presented and the thermoelectric conductivity of the 30 μm long SiNWs is measured using this technique.

6.1 Electrical measurements

6.1.1 Lightly doped n-silicon bulk and nanowire arrays

I-V measurements on n-type bulk Si, used as a reference sample, were measured, followed by I-V measurements of SiNW arrays. The n-type samples were doped using phosphorous, with resistivity 1 – 10 Ωcm, corresponding to a doping level from 5×10^{15} – 5×10^{14} cm^{-3}. Spin-on dopant (SOD) diffusion is used to dope top and bottom of the Si sample surfaces of a thin layer to $\sim10^{18}$ cm^{-3} (phosphorous doping) in order to improve metal contact deposition. The SOD was spin-coated on the wafer and then prebaked at 200 °C for ten

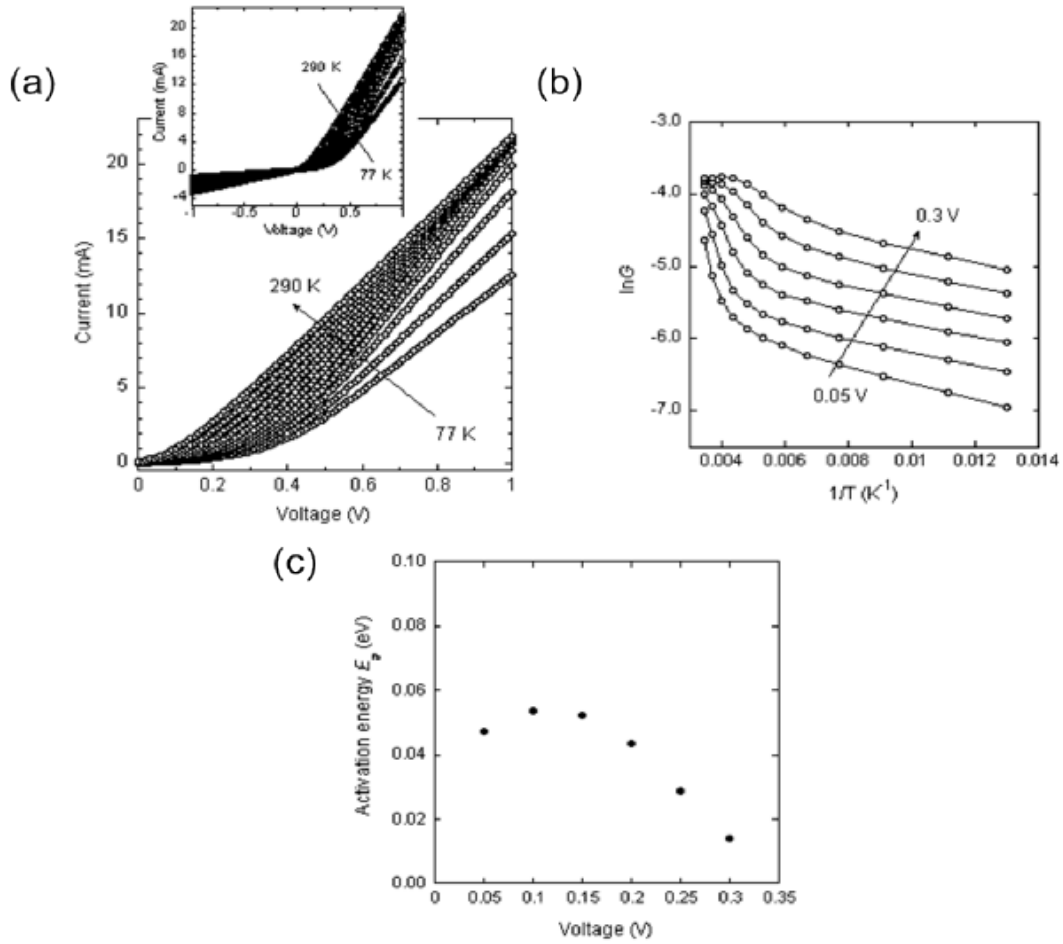


Figure 6.1: (a) I-V temperature dependence of bulk Si in the temperature range 290 – 77 K, at 20 K steps. (b) Arrhenius plots of bulk Si conductance G vs. inverse temperature. (c) Activation energies E_a of bulk Si in the voltage range. Voltage range is 0.05 – 0.3 V at 0.05 V steps.

minutes. The wafer was then annealed in a quartz tube furnace for five to ten minutes at 800 – 900 °C in an argon (Ar) or nitrogen gas (N_2) atmosphere. After a layer of SOD was deposited on both sides of the sample, Al contacts of 300 – 500 nm were evaporated at 40° angle to the normal of the axis to the metal source, to avoid short-circuiting the NWs. The SOD and contact metals were prepared by Dr. Chuanbo Li.

Figure 6.1(a) shows the I-V characteristics of bulk Si in the temperature range 290 – 77 K, with 20 K steps, and in the voltage range 0 – 1 V. The inset shows the I-V curves for voltage range (-1 V, 1 V). The sample exhibits non-Ohmic contacts for negative voltages, indicating a Schottky barrier at one of the bulk semiconductor-metal interface. This may be related to the low doping level. The I-V curves in the voltage range 0 – 1 V show a small non-linearity, and the resistance (including contact) is ∼45 Ω at 290 K. In the

(0 – 1 V) range, the I-V curves show a small rate of change with temperature and a difference in current of only 10 mA between 290 K and 77 K. Above 0.5 V, a resistance of ∼83 Ω is seen at 77 K. We obtain Arrhenius plots for conductance ln$G$ as a function of the inverse of temperature, shown in Fig. 6.1(b) for voltages 0.05 – 0.3 V, at 0.05 V steps. It is possible to extract the activation energy E_a by considering the straight lines sections in the graph. Fig. 6.1(c) shows E_a as a function of voltage. A decrease in E_a is observed as the voltage increases beyond 0.1 V. The activation energies are very small, $\sim$ 0.014 eV for 0.3 V and a maximum of $\sim$ 0.053 eV for 0.1 V. This values is close to the ionisation energy of dopants.

Fig. 6.2(a) shows the I-V characteristics of n-SiNWs in the temperature range 290 – 77 K. The I-V characteristics are Ohmic throughout the measured temperature range, with a total resistance (including contact) of ∼250 Ω at 290 K, ∼370 Ω at 270 K and ∼550 Ω at 250 K. The resistance then rapidly increases as T is decreased below 230 K. In comparison to bulk Si, the changes with temperature in the I-V characteristics of the SiNWs are greater than bulk. The resistance of SiNW is ∼5.5 times greater than bulk at 290 K and current is within $\sim 0.4\times10^{-7}$ A at 77 K. The negligible currents measured at low temperature, *i.e.* below 170 K are related to a carrier freeze out, similar to the case of the Seebeck coefficient measurement, described in Chap. 5.3, for the lightly doped NWs. Fig. 6.2(b) shows ln$G$ vs. $1/T$ in the voltage range of 0.05 – 0.3 V, with 0.05 V steps. Extracted activation energies E_a are shown in Fig. 6.2(c). The activation energy, *i.e.* potential barrier height along the conduction path, is almost constant and its maximum value is 0.138 eV at 0.05 V. E_a is very small but still ∼10 times higher than bulk Si. This difference may be related to the ionisation energy of dopants. If the latter is close to the NW surface, then this may alter the activation energy leading to an increased ionisation energy of dopants. The differences in the I-V characteristics between bulk and SiNWs indicate that there may be surface traps at the NW surface, causing some of the electrons to be trapped at the NW surface. This might lead to an increase in the activation energy, associated with a greater 'barrier' height in the NWs. This barrier lies along the conduction path and may be associated either with the Schottky barrier height at the contacts [121] or with a more depleted region within the NWs. Another possibility may be that among the NWs in parallel, only those with the best conductivity dominate.

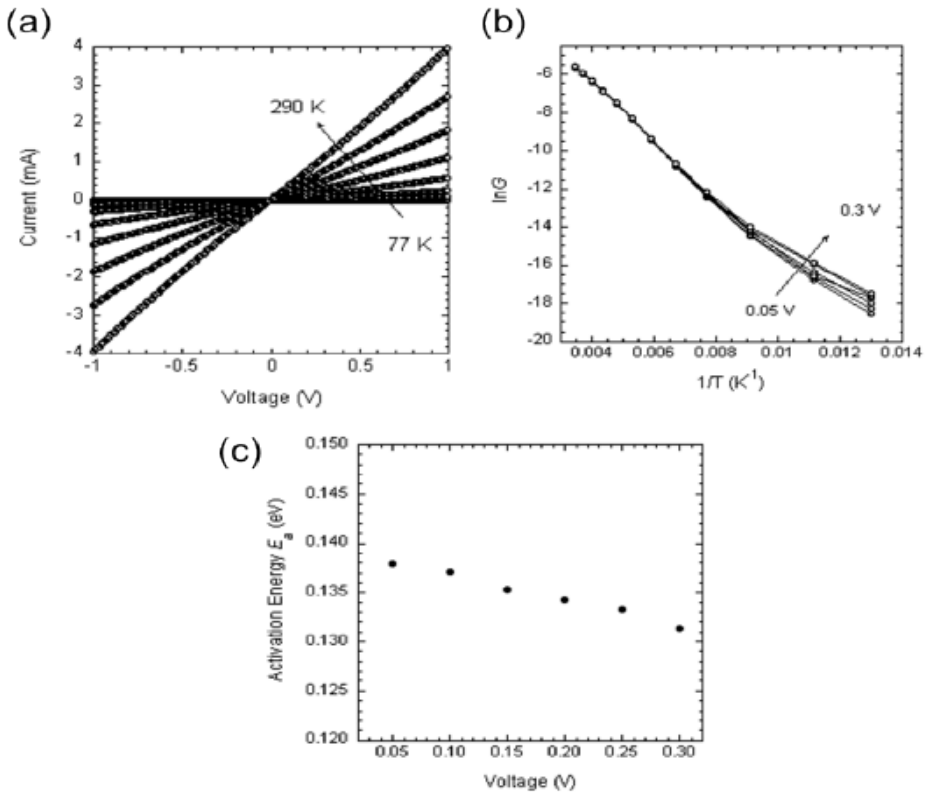


Figure 6.2: (a) I-V temperature dependence of SiNW arrays. (b) Arrhenius plots of NW array conductance G vs. inverse temperature in the range of 0.05 – 0.3 V, at 0.05 V steps. (c) Activation energies E_a of SiNWs in the voltage range 0.05 – 0.3 V, at 0.05 V steps. The temperature range is 290 – 77 K at 20 K steps.

6.1.2 Moderately doped n-Si bulk and nanowire arrays

In a similar way to section 6.1.1, the temperature dependence of the I-V characteristics was measured for bulk Si and SiNW arrays in moderately doped samples. The Si samples were phosphorous doped with resistivity 0.01 – 0.03 Ωcm, corresponding to a doping level from 10^{17} – 10^{18} cm^{-3}. Al contacts ∼500 nm thick were evaporated at 40° angle, to avoid short circuiting the NWs. Figure 6.3(a) shows the bulk Si I-V dependence in the temperature range 300 – 40 K. The I-V characteristics are Ohmic at 300 K, with a total resistance (including contact) of ∼1 Ω respectively. The bulk Si characteristics remain Ohmic throughout the temperature range, as expected for the higher doping level. The inset of Fig. 6.3(a) shows the I-V characteristic of Cu vs. cryostat finger, measured

after removal of bulk and SiNWs. Arrhenius plots of the conductance G, calculated in the voltage range 0 – 0.09 V, with 0.01 V steps, are shown in Fig. 6.3(b). A minimal change is observed in the conductance throughout the temperature range 300 – 40 K, indicating that there is no thermally activated barrier height and that the contacts are Ohmic throughout the temperature range.

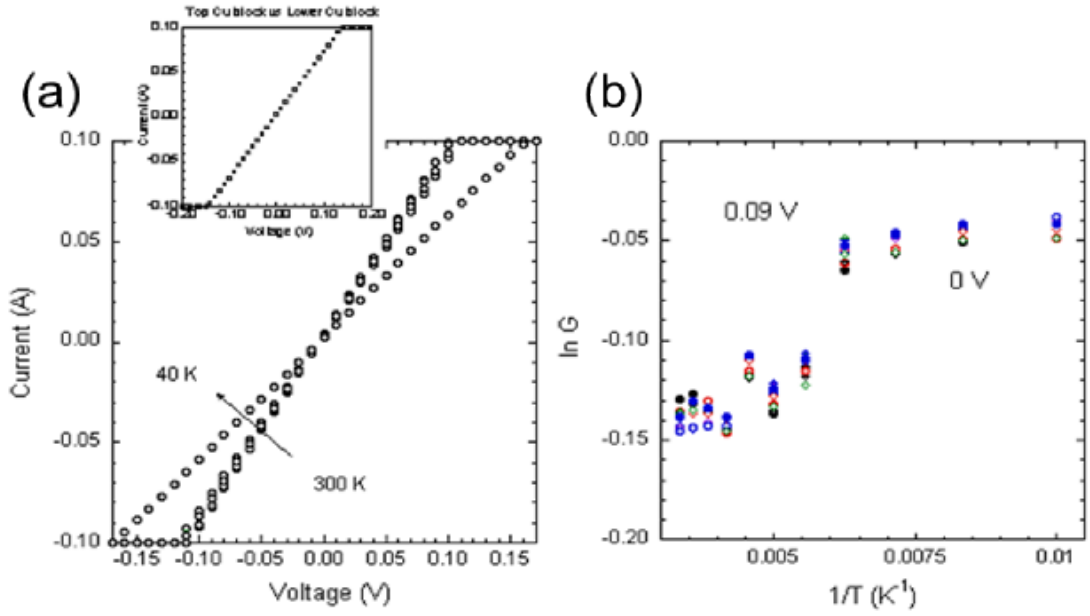


Figure 6.3: Temperature dependence of electrical characteristics of bulk Si. (a) I-V temperature dependence of bulk Si. Inset shows the I-V characteristics of Cu block on the cryostat finger. (b) Arrhenius plots of conductance G vs. inverse temperature in the range of 0 V – 0.09 V, at steps of 0.01 V. The temperature range is 300 – 40 K.

Figure 6.4(a) shows the I-V characteristics of the SiNWs as a function of temperature, in the temperature range from 300 – 40 K. As for the bulk Si, the I-V characteristics in the SiNW array sample are Ohmic, and at 300 K the total resistance (including contact) is 3 Ω. The I-V curves remain Ohmic throughout the temperature range, except at low temperatures. There is a small non-linearity in the SiNW characteristics at temperatures $<$80 K, implying the presence of a small potential barrier in the device. This is likely to exist at the SiNW/Al top contact. The increase in the total resistance in the NW sample compared to bulk can be attributed to the reduction in contact area by the packing factor of ∼30% of the NW array. Fig. 6.4(c) shows ln$G$ as a function of inverse of temperature. We

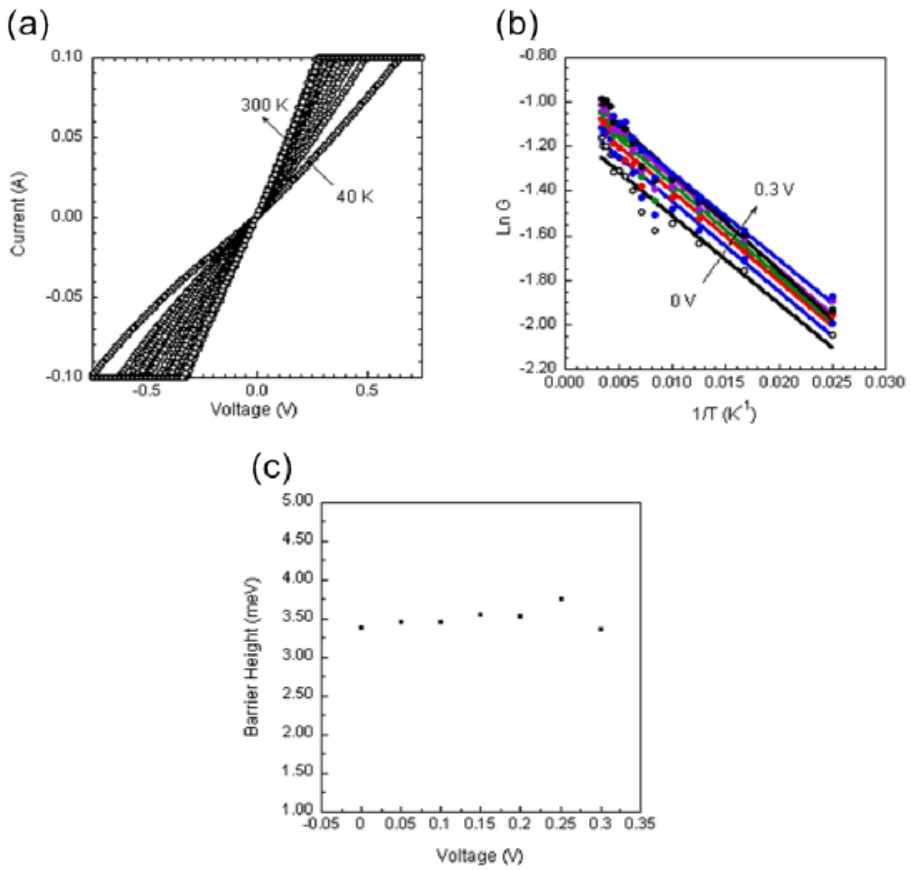


Figure 6.4: (a) I-V temperature dependence of SiNW arrays in the temperature range 300 – 40 K. (b) Arrhenius plots of NW array conductance G vs. inverse temperature in the range of 0 – 0.3 V, at 0.05 V steps. (c) Activation energies E_a of SiNWs in the voltage range 0 – 0.3 V, at 0.05 V steps.

find that $\ln G$ vs. $1/T$ is linear, implying a thermally activated temperature dependence. The slope of the lines corresponds to an activation energy, i.e. potential barrier height, of $\sim$3.5 meV. This is a very small value, implying that even in the SiNW samples, the I-V characteristics are Ohmic except at temperatures of $\sim$ 40 K and below. Finally, as the conductance of the sample excluding the contact resistance is theoretically $< 0.01\ \Omega$, this cannot be extracted in a two terminal measurement. The electrical characteristics for the moderately doped sample illustrate minimal change in the conductance from a bulk Si sample to a SiNW sample, implying that the NW conductivity is unaffected.

In lightly doped samples, a strong reduction is observed in the conductance of SiNWs vs. bulk Si, in comparison to the moderately doped samples. This may be related to a relatively stronger influence of traps at the NW surface, determining the number of electrons available for conduction.

To overcome surface traps, passivation of the NW surface is considered by filling them with polymer. The polymer filling may act as an electron donor or hole acceptor and may lead to better electrical characteristics. This is described in the following section.

6.1.3 Polymer filled silicon nanowires

Polymer filling of NWs is a possible means to enhance their electrical characteristics, as this may passivate traps at the NWs surface. The DC electrical characteristics of hybrid polymer/p- and n-type SiNW devices were measured and compared with SiNW samples without polymer. For both cases, the nanowires were etched at the same time. Hybrid polyacrylic acid (PAA) was chosen as it can be diluted in water and is simple to apply. The vertical SiNW arrays were filled with PAA by repeated spin coating. After PAA, with 450k molecular weight, was highly diluted in deionised (DI) water (∼1.65 wt% PAA with DI water), it was spun on the SiNW arrays at 500 rpm for 60 seconds. To allow the PAA to dry, the samples were heated at 50 $^\circ$C in air for 15 minutes. The spinning and heating processes were repeated two further times under similar conditions. Here, ∼3.3 wt% PAA in DI water was spun at 500 rpm for 60 seconds, again followed by drying at 50 $^\circ$C. This process was repeated twice. Finally, PAA ∼6.6 wt% with DI water was spun at 1000 rpm for 60 seconds, followed by drying at 50 $^\circ$C in air for 30 minutes. This process was repeated two times. These steps yielded the incorporation of PAA down to the bottom of the nanowires. These experiments were performed by K. Rasool and Dr. C. Li and are explained in detail in Ref. [127]. The metal contacts formed by 300 – 500 nm Al layers for n-type, and 50 nm chromium (Cr) followed by 300 nm Gold (Au) layers for the p-type. The current-voltage (I-V) characteristics were measured by the author. Annealing of the contacts was not performed to avoid degradation of the PAA. The area of all samples was 0.85 cm×0.85 cm.

(A) Measurements on PAA filled n-SiNWs

Here, I-V measurements are presented for the n-SiNW arrays with PAA and n-SiNW arrays only. The samples resistivity was 1 – 10 Ωcm and the doping level 5×10^{15} – 5×10^{14} cm^{-3}. Figure 6.5(a)-(b) show the I-V characteristics of the PAA filled SiNW sample and the SiNW sample without PAA in the temperature range 290 – 77 K. Nonlinear I-V characteristics are measured for the polymer filled SiNW sample, indicating a Schot-

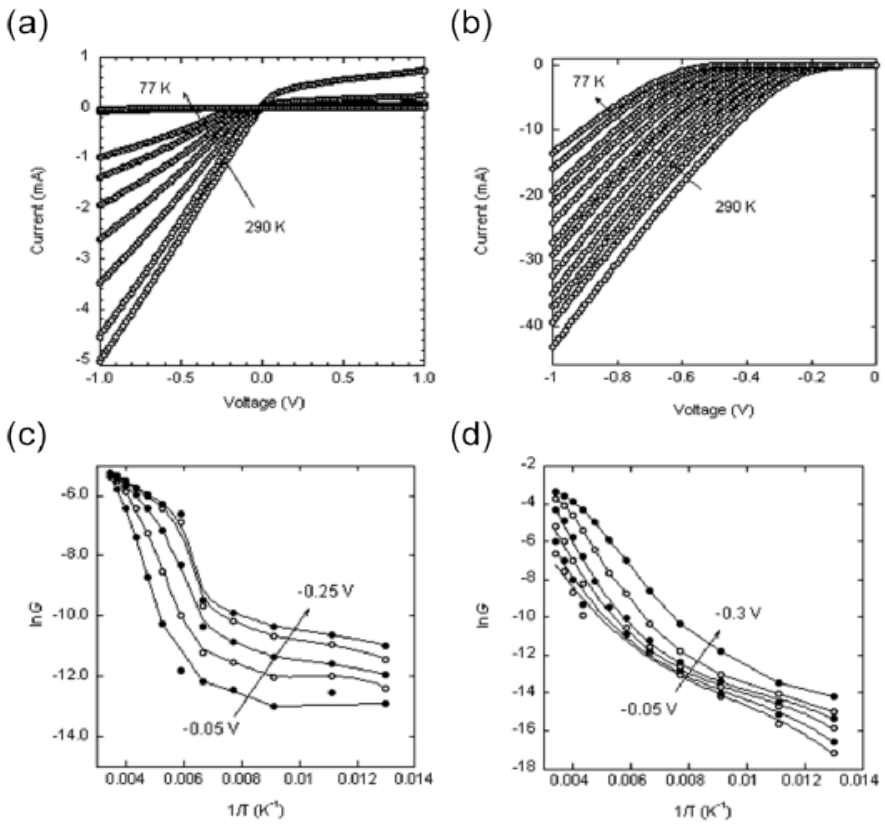


Figure 6.5: (a) Temperature dependent I-V for SiNWs/PAA hybrid device. (b) Temperature dependent I-V for SiNWs only (c) Ln of conductance (G) vs. reciprocal of temperature ($1/T$) for SiNW/PAA hybrid device. (d) Ln of conductance (G) vs. reciprocal of temperature ($1/T$) for SiNW device.

tky barrier at the junction between SiNWs/metal contact. The PAA filled SiNW samples manifest a smaller current as compared to the SiNW devices. At (1 V, 290 K), the currents for the PAA filled SiNW and SiNW samples are 5 mA and 43 mA, respectively. This is equivalent to ~8.6 times lower current for PAA + SiNWs than SiNWs only. As the temperature decreases, the current of the polymer filled SiNWs approaches zero. At temperatures below 170 K, a drastic decrease in the current of the PAA filled SiNW is observed.

Figs. 6.5(c)-(d) show Arrhenius curves for PAA filled SiNWs and NWs without PAA, respectively. Activation energies (E_a) were extracted and these are listed in Table 6.1. In SiNWs without PAA, an increase in the activation energy is observed, whereas a decrease is observed in the PAA filled SiNWs. The reduction in activation energy may be due to the work function difference between the PAA and the SiNWs. In this case (n-type), inclusion of PAA does not lead to an improvement and instead a decrease in current is measured in comparison to the SiNW samples. These suggest that PAA may introduce electron traps.

	Activation energies E_a (eV)				
Voltage (V)	0.05	0.1	0.15	0.2	0.25
n-SiNWs	0.116	0.129	0.148	0.168	0.171
PAA/n-SiNWs	0.163	0.144	0.125	0.106	0.100

Table 6.1: Activation energies E_a of n-SiNWs and PAA/n-SiNWs at different voltages.

Hence, electron recombine at the Si/PAA surface, reducing the overall number of electrons available for conduction.

(B) Measurements on PAA filled p-SiNWs

Vertically aligned p-SiNW arrays and p-SiNW arrays with PAA, resistivity 1 – 5 Ωcm and doping level of 5×10^{15} – 1 $\times10^{15}$ cm^{-3} were also analysed. Figure 6.6(a)-(b) show the I-V characteristics of the PAA filled SiNW sample and the SiNW sample without PAA, in the temperature range 290 – 77 K. Nonlinear I-V characteristics are measured in both cases. Larger current is measured for the PAA filled SiNW samples as compared to the SiNW devices, particularly at low temperature. At (290 K, 0.3 V), the currents for the PAA filled SiNW sample and the SiNW sample are 100 mA and 80 mA, respectively. This corresponds to an improvement of only ∼1.25. As the temperature decreases, the current of the polymer filled SiNWs is greater than the bare SiNWs. At (77 K, 0.3 V), the currents are 19.8 mA and 7.26 nA for the PAA filled SiNW and SiNW samples, respectively, an improvement by a factor of $\sim 10^6$. In general, at temperatures below 190 K, a drastic increase in current of the PAA filled SiNW is observed.

Figs. 6.6(c)-(d) show Arrhenius curves for PAA filled SiNWs and NWs without PAA, respectively. Activation energies (E_a) are listed in Table 6.2. PAA filled SiNWs show a reduction in E_a in comparison with SiNWs without PAA. The reduction in activation energy may be related to the work function difference between the PAA and the SiNWs. Here, decomposition of the acidic part of carboxylic acid groups in the PAA chain produces an interfacial dipole layer. Negative functional groups can form on the SiNWs which act as acceptor like states, causing upward band bending and increasing the majority carrier (hole) concentration in our p-SiNWs [127]. This leads to an improvement in the conductivity of our PAA wrapped SiNWs. HF treatment and solvent rinsing of the SiNWs can result in a dominantly hydrogen terminated, hydrophobic surface [128]. In a humid air environment, oxidation can create a hydrophilic surface and Si-OH bonds. In addition,

removal of Ag by HNO_3 can cause the NWs to become hydrophilic. Finally, a water soluble polymer like PAA can initiate the formation of Si-OH groups on the SiNW surface. These processes may introduce energy states on the surface of the SiNWs, which can then act as acceptor like states [129]. Enhanced conductivity has been observed in p-type SiNWs treated with tetraethyl ammonium bromide due to the generation of acceptor like states due to negatively charged Br–. The resistance, measured in DC electrical measurements, decreases in SiNWs covered with PAA in comparison with SiNWs without PAA. This may be a consequence of formation of acceptor-like states at the SiNW/PAA interface [127].

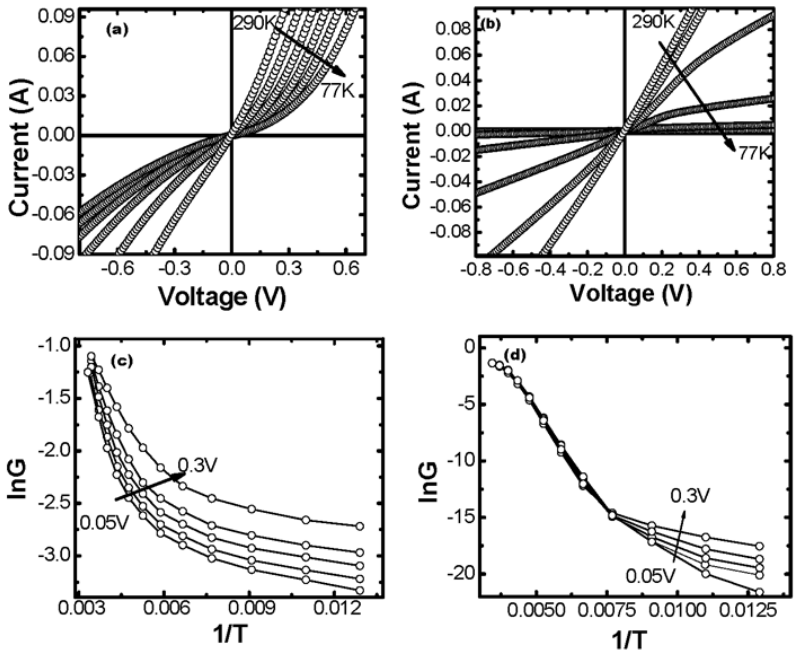


Figure 6.6: (a) Temperature dependent I-V for SiNWs/PAA hybrid device. (b) Temperature dependent I-V for SiNWs only (c) Ln of conductance (G) vs. reciprocal of temperature ($1/T$) for SiNW/PAA hybrid device. (d) Ln of conductance (G) vs. reciprocal of temperature ($1/T$) for SiNW device. Figure adapted from Ref. [127].

	Activation energies E_a (eV)				
Voltage (V)	0.05	0.1	0.15	0.2	0.3
SiNWs	0.299	0.301	0.307	0.312	0.306
PAA/SiNWs	0.082	0.079	0.077	0.066	0.046

Table 6.2: Activation energies E_a of SiNWs and PAA/SiNWs at different voltages.

6.2 Thermal conductivity measurements

6.2.1 Heat conduction in transient conditions

Let us now consider a body of mass m, volume V, surface area A, density ρ_m and specific heat c at a uniform temperature T_i . If the body is surrounded in a medium at temperature T_∞ and time $t = 0$, there will be heat transfer between the body and the environment. For simplicity, we assume $T_\infty > T_i$, but the analysis is valid for $T_\infty < T_i$, and temperature changes with time within the body are described by $T = T(t)$. After a time interval $\mathrm{d}t$, there will be an increase of temperature $\mathrm{d}T$ within the body of mass m. The heat transfer taking place at time $\mathrm{d}t$ between the body mass and the surrounding can be written as [130, 131, 132]:

$$hA(T_\infty - T)\mathrm{d}t = mc\mathrm{d}T \tag{6.1}$$

where h is the heat transfer coefficient. The left hand side of this equation corresponds to heat transferred into the body within time $\mathrm{d}t$ and the right hand side is the increase in the energy of the body during time $\mathrm{d}t$. Substituting $m = \rho_m V$ and $\mathrm{d}T = \mathrm{d}(T\text{- }T_\infty)$, with T_∞ = constant, Eq. 6.1 can be expressed as:

$$\frac{\mathrm{d}(T - T_\infty)}{T - T_\infty} = -\frac{hA}{\rho_m V c}\mathrm{d}t \tag{6.2}$$

Integrating from $t = 0$, *i.e.* $T = T_i$, to any time t, where $T = T(\mathrm{t})$, we have [130, 132]

$$\int_0^t \frac{\mathrm{d}(T - T_\infty)}{T - T_\infty} = -\frac{hA}{\rho_m V c}\int_0^t \mathrm{d}t \tag{6.3}$$

$$\ln\frac{T(t) - T_\infty}{T_i - T_\infty} = -\frac{hA}{\rho_m V c}t \tag{6.4}$$

Eq. 6.4 can be further simplified and rearranged as [130, 132]:

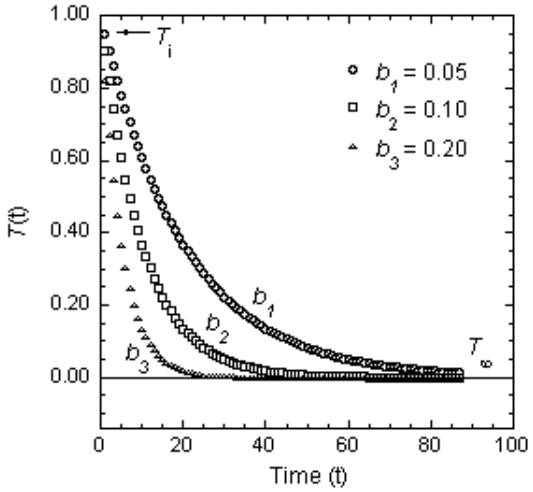


Figure 6.7: Temperature changes within a lumped system. The system approaches T_∞, *i.e.* the environment temperature as time gets larger.

$$\frac{T(t) - T_\infty}{T_i - T_\infty} = \mathrm{e}^{-bt} \tag{6.5}$$

where

$$b = \frac{hA}{\rho_m V c} \tag{6.6}$$

with b positive and has the dimension of (time^{-1}). The time constant corresponds to the inverse of b, *i.e.* has the time unit, and is denoted with τ. Systems that obey the above description are called lumped systems. Figure 6.7 shows the temperature within a lumped system by plotting Eq. 6.5 for three different values of b, *i.e.* 0.05, 0.1 and 0.2. The smaller the value of b, the longer is the corresponding exponential decay and the greater is the time constant (inverse of b). In this case, it takes longer for the system to approach the environment temperature T_∞. We use this approach to measure the time constant of exponential decay of ΔT.

6.2.2 Moderately doped silicon nanowires

The thermal conductivity of the SiNW arrays κ_{NW} is measured using a transient measurement of temperature ΔT vs. time t. The measurement apparatus used is shown in Fig. 2.10 and was discussed in Chap. 2.7.2. A thin ($<$ 1 mm) mica sheet was inserted between the sample and the lower Cu block to prevent charge transfer and loss of electrons from the sample to the lower Cu block [37]. In principle, a transient method allows direct

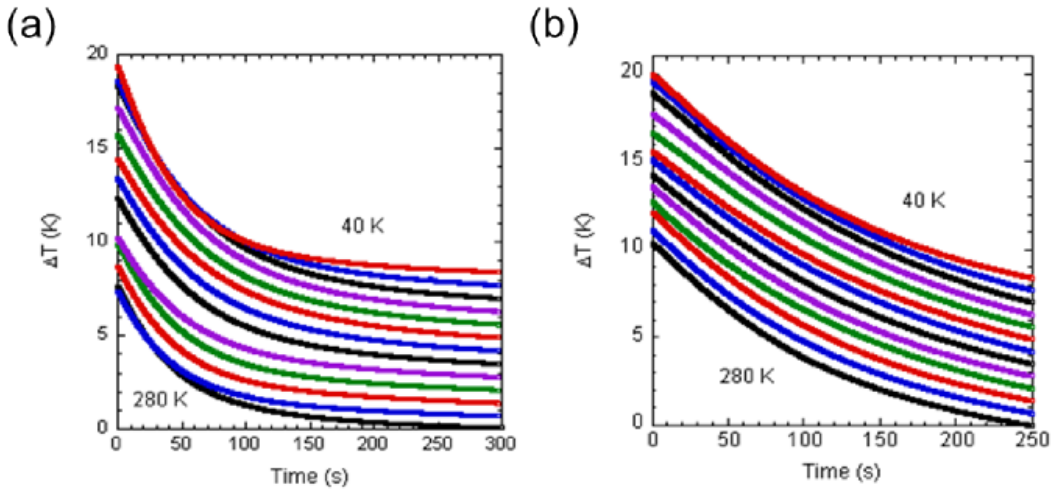


Figure 6.8: Temperature dependence of the exponential decays of ΔT as a function of time for (a) bulk Si and (b) 30 μm long SiNW arrays. Temperature range is 280 – 40 K, with 20 K steps.

measurement of κ_{NW}. However, this would require an estimate of the heat loss from the top Cu block, e.g. through the leads connecting to the block and the temperature sensor. In order to measure κ_{NW}, we use moderately doped SiNWs samples with the highest S values, *i.e.* the 30 μm long SiNW array used for S measurement in Fig. 5.21. We then measure the time constants τ of the exponential decays in ΔT vs. time t, inverse of Eq. 6.6, in both bulk Si and the SiNW array sample. Results of ΔT vs. time t without a mica sheet were not satisfactory.

Figure 6.8(a)-(b) show the time dependence of the exponential decays in the temperature range 280 – 40 K. In the case of bulk Si, the time constant of the exponentials ranges between ∼45 to ∼76 s. The time constant of the SiNWs exponentials are greater, with values ranging from 128 to 208 s. Hence, ΔT within the NWs is maintained for a longer period of time.

Figure 6.9 shows the time constant dependence of bulk Si and 30 μm long SiNW array versus temperature. Both samples show a peak at moderate to low temperatures, ∼120 K, with the peak being more pronounced in the NW array. The time constants τ_{NW} (NW sample) and τ_{Bulk} (bulk Si sample) are directly proportional to the sample thermal resistances and hence inversely proportional to the thermal conductivities κ_{NW} and κ_{Bulk}.

Using the known values of κ_{Bulk} measured in Ref. [84], and multiplying these by the ratio $\tau_{Bulk}/\tau_{NW} \propto \kappa_{NW}/\kappa_{Bulk}$ gives us κ_{NW}.

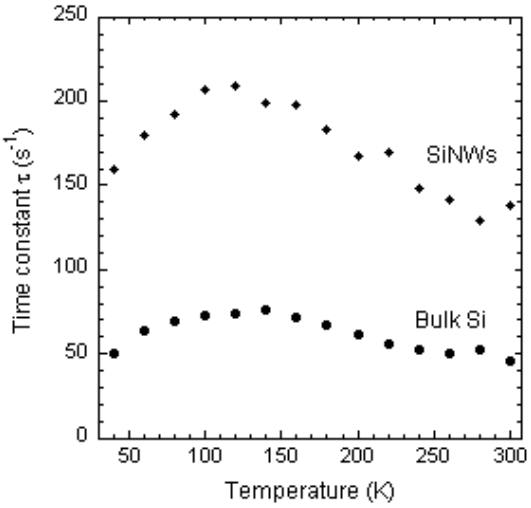


Figure 6.9: Temperature dependence of bulk Si and SiNW array time constants τ of the exponential decays of ΔT vs. time.

Figure 6.10(a) shows κ_{Bulk} and κ_{NW} vs. T in the temperature range 300 – 40 K. Here, κ_{Bulk} is the data for heavily doped bulk Si from Ref. [84]. We find that κ_{NW} remains approximately constant from 300 – 80 K, at a value of ~30 W/mK, implying that the phonon mean free path l_p remains approximately constant, as this is restricted by the NW widths.

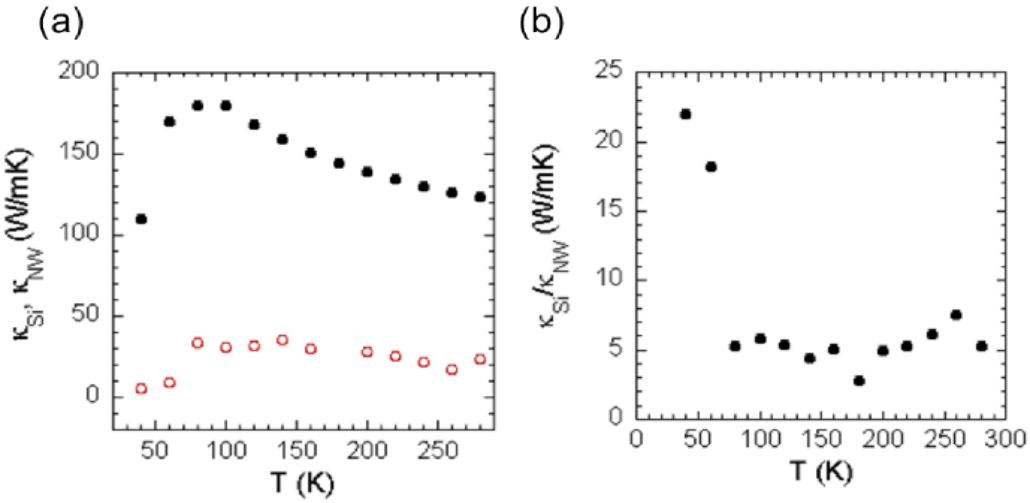


Figure 6.10: κ of SiNW arrays (κ_{NW}, empty circles) compared to bulk Si (κ_{Bulk}, filled circles). (a) κ_{NW} and κ_{Bulk} as a function of temperature. The data for κ_{Bulk} is from [84] and κ_{NW} is extracted by comparing transient measurements of ΔT in the NWs to bulk samples. (b) Ratio of κ_{Bulk} to κ_{NW}.

The reduction in κ_{NW} below 80 K is associated with the fall in specific heat C_p at lower temperatures. This behaviour may be contrasted with the behaviour of κ_{Bulk} where the reduction in Umklapp scattering from 300 – 80 K leads to an increase in l_p and hence κ_{Bulk}. Figure 6.10(b) shows the ratio $\kappa_{Bulk}/\kappa_{NW}$ vs. T, directly obtained from our measurements. From 300 – 100 K, $\kappa_{Bulk}/\kappa_{NW} \sim 5$, and increases even further below 80 K. This demonstrates the strong reduction in κ_{NW} due to phonon scattering in the NWs.

6.3 ZT in moderately-doped silicon nanowire arrays:

We now estimate ZT in the 30 μm long SiNW array. Table 6.3 shows ZT data at temperatures 300 K, 280 K, 200 K and 100 K for the 30 μm long SiNW array. ZT was initially calculated with the raw data, Tab. 6.3(A). Here, the temperature drop within the top Cu block was not included, see Chap. 5.1.1. In Tab. 6.3(B), the temperature drop within the top Cu block was considered in the measurement of S. In this table, κ_{Bulk} are the values taken from Ref. [84], S are the measured data for 'bulk + NW' and κ_{NW} corresponds to our measured data shown in Fig. 6.10(a). As for the case of σ, some of the electrons may be lost at the surface, since the NW surface affects the Fermi energy. However, we assume that in the NWs, $\sigma = 10^4\ \Omega^{-1}\mathrm{m}^{-1}$ – $0.33\times10^4\ \Omega^{-1}\mathrm{m}^{-1}$ (corresponding to the range of doping level), is unchanged from the bulk value. This assumption is supported by both our SiNW array I-V characteristics (section 6.1.2) and by the high field-effect mobility observed in SiNW FETs [121]. This represents the best case scenario. In the table are also given minimum and maximum ZT values. ZT_{min} corresponds to $\sigma_{min}= 0.33 \times 10^4\ \Omega^{-1}\mathrm{m}^{-1}$ and ZT_{max} is calculated with $\sigma_{max} = 10^4\ \Omega^{-1}\mathrm{m}^{-1}$. ZT_{Bulk} has been calculated first with the raw data, see Tab. 6.3(A) and then including the temperature drop of the top Cu block, Tab. 6.3(B).

In the case of raw data, the 30 μm long SiNW array has $ZT \sim 0.0255$ at 300 K, an increase by a factor of 100 compared to bulk. The maximum of $ZT \sim 0.03$ is obtained at 280 K, this is related to the lower κ_{NW} observed at 280 K. As the temperature decreases, a maximum increase by a factor of ~ 250 is observed at 140 K.

After removal of the temperature drop in the top Cu block from the S values, $ZT = 0.09$ – 0.28 at 300 K, this is an improvement by a factor of ~32 compared to bulk Si. In particular, at 280 K $ZT = 0.34 = 55ZT_{Bulk}$, this is our best ZT and lies within the range necessary

(A)

T	κ_{Bulk} (W/mK)	κ_{NW} (W/mK)	S (μV/K)	ZT_{min}	ZT_{max}	ZT_{Bulk}
300 K	120	23	444	0.0084	0.0255	$0.00032-9.7\times10^{-5}$
280 K	123	17	430	0.01	0.031	$1.8\times10^{-4}-5.4\times10^{-4}$
200 K	140	28	360	0.003	0.01	$1.02\times10^{-5}-3.1\times10^{-5}$
100 K	117	31	230	0.0005	0.0016	$6.6\times10^{-6}-\ 2\times10^{-5}$

(B)

T	κ_{Bulk} (W/mK)	κ_{NW} (W/mK)	S (μV/K)	ZT_{min}	ZT_{max}	ZT_{Bulk}
300 K	120	23	1480	0.0936	0.28	$0.0029-0.0087$
280 K	123	17	1433	0.11	0.34	$0.002-0.006$
200 K	140	28	1200	0.03	0.1	$9.2\times10^{-5}\ -0.00028$
100 K	117	31	766	0.0057	0.017	$5.9\times10^{-5}\ -0.00018$

Table 6.3: ZT calculated for the 30 μm long SiNWs, before and after inclusion of top Cu drop, at 300 K, 280 K, 200 K and 100 K. ZT_{min} and ZT_{max} were obtained using σ_{min} and σ_{max} respectively.

for practical application of TE effects in a material. In a similar way to the raw data, the ZT improvement over bulk is maintained even at low temperatures. An increase by a factor of 100 is observed at 140 K.

Fig. 6.11(a)-(b) show the calculated ZT_{min} and ZT_{max} of the 30 μm long SiNW arrays. In Fig. 6.11(a)-(b), ZT has been calculated using raw data, and by taking into account the temperature drop in the top Cu block, respectively.

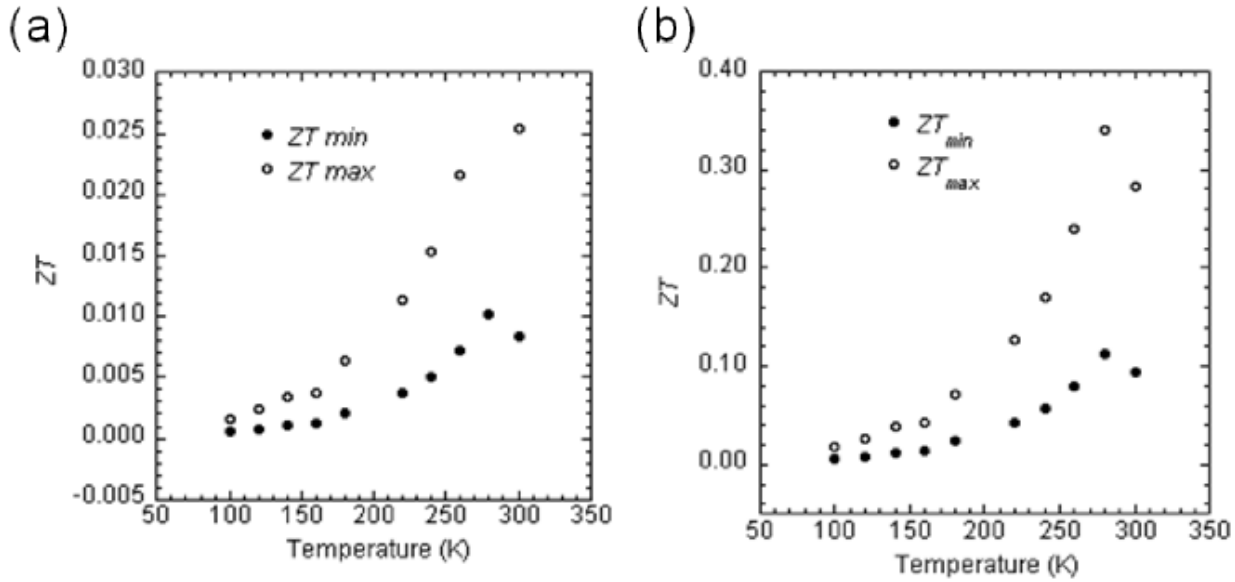


Figure 6.11: ZT calculated for the 30 μm long SiNW arrays, using our measured κ_{NW}. (a) The measured S ('bulk + NW') does not include the temperature drop of the top Cu block copper drop of our measurement apparatus. (b) Cu drop has been considered in our measured S. ZT_{min} has been calculated by using $\sigma = 0.33\times10^4\ \Omega^{-1}\mathrm{m}^{-1}$. ZT_{max} corresponds to the maximum value of $\sigma = 10^4\ \Omega^{-1}\mathrm{m}^{-1}$.

7 Conclusions

This thesis has investigated thermoelectric effects in SiNW arrays. Thermoelectric (TE) materials represent good candidates for waste heat scavenging in mechanical and electrical systems, allowing an overall enhancement in system efficiency. There exists different applications that utilises TE modules, mainly based on Bi_2Te_3 material. Bi_2Te_3 has one of the highest $ZT = S^2\sigma T/\kappa \approx 1$, where S is the Seebeck coefficient, σ the electrical conductivity, T absolute temperature, and κ thermal conductivity. However, tellurium (Te) is a very rare element and hence very expensive. In contrast, Si is one of the most abundant, low cost materials available, but in bulk form is a very poor TE material. While in bulk materials, S, σ, and κ are interrelated, in nanostructures these may be varied quasi-independently. Here, S can be increased by quantum confinement of electrons without excessively affecting σ and furthermore, κ may be reduced independently of the other parameters by either increased surface scattering of phonons or modification of the density-of-states. These effects depend primarily on the length scale, hence there is greater freedom in material choice, and TE devices in materials even with nominally poor ZT become feasible.

In this thesis, we measure the thermoelectric characteristics of n- and p-type silicon nanowire (SiNW) arrays at room temperature conditions, and n-type SiNW arrays with two different doping levels, in vacuum, in the temperature range 300 – 30 K. Our NW arrays were fabricated using a metal-assisted-chemical-etching (MACE) process. This process fabricates large areas of vertically aligned SiNWs ($\sim 10^{18}$ NW) with diameter of 30 – 400 nm and high aspect ratios, up to 3000. In the MACE process, the sample was immersed in a solution of $HF/AgNO_3/H_2O$ at room temperature. This deposited Ag nanoparticles on the Si surface via an electroless deposition (galvanic exchange) mechanism. The nanoparticles then acted as a catalysts for subsequent etching of the NWs in $HF/H_2O_2/H_2O$ solution. The process involved etching of the Si in contact with the Ag nanoparticles, forming NWs of irregular cross-section. Lightly n- and p-type Si, and moderately doped n-type Si, were

used to prepare SiNW arrays of different length and different doping type. A filling factor of ∼30% was found in both types of doped NW arrays.

To characterise the SiNWs in ambient condition, a measurement apparatus was developed and characterised. This was used to measure S, the fundamental thermoelectric parameter, at equilibrium in n- and p-type SiNWs and in a bulk Si, reference sample. SiNW arrays of different lengths were measured. In p-SiNWs, the arrays were ∼30, 40, 65 and 90 μm long. In the n-SiNWs, the arrays were ∼15, 60, 70 μm long. In the p-SiNW arrays, S is higher than bulk, except for the 90 μm SiNW array which manifests an inversion of carrier type from p- to n-type behaviour. This may be related to positive fixed charge trapped at the NW surface. These trapped charges can lower the conduction band energy edge E_C and the valence band energy edge E_V in the NW, relative to the Fermi energy E_F, and invert the NW from p- to n-type. In Ref. [121], [122] and [123] inversion of carrier type also was observed. In Ref. [121], a p-doped SiNW transistor behaved as an n-channel FET. In Ref. [122], a positive S was measured for a single n-type bismuth nanowire of 55 nm length. The electrical characteristics of n-type SiNWs, measured in Ref. [123], behaved as p-type. In Ref. [123], the changes were associated with the surrounding ambient and surface conditions strongly affecting the transport properties of the SiNWs. Peng *et al.* [123] suggest that in normal ambient conditions, there is absorption of gas molecules such as oxygen and humidity that trap electrons on the surface of SiNWs, causing surface band bending. As a consequence, excess holes from surface adsorption may compensate electrons in the NWs, converting the NWs to p-type. Our measured data indicated a strong influence of the surface on the NW Fermi level.

To investigate the influence of the surrounding atmosphere and the temperature dependence of the NW arrays, characterisation of n-type SiNW arrays was performed in a closed-cycle cryostat with moderate vacuum conditions and in a temperature range from 300 – 30 K. The temperature dependence of S for lightly (5×10^{14} – 5×10^{15} cm^{-3}) and moderately doped Si (∼10^{7} – 10^{8} cm^{-3}) was measured. Two different doping levels were analysed in order to study the effect of doping on the electron/phonon interaction and transport within the nanostructured material. A novel transient measurement method to characterise temperature and voltage across the sample was developed, allowing measurement of thermoelectric parameters even in very thin and large area samples. The measurement is based on the transient heat flow from a copper hot reservoir to a heat

sink. We measure the time dependence of voltage ΔV and temperature ΔT, and hence ΔV vs. ΔT characteristics, and the Seebeck coefficient.

Lightly-doped (10^{15} cm^{-3}) n-type Si is investigated as a means to reduce impurity scattering of electrons and phonons. At low doping levels, phonon drag is the dominant contribution to S at moderate to low temperatures (∼200 – 30 K) [84]. Low doping levels disentangle impurity scattering from surface scattering and leave the NW dimensions as the main source of scattering. S of bulk Si, and SiNW arrays ∼35, 80 and 350 μm long, was measured in the temperature range 300 – 30 K. The Seebeck coefficient in bulk Si increases as the temperature reduces, as a consequence of 'phonon drag', manifestation of electron-phonon scattering in the sample. In contrast, in all the SiNW arrays, S reduces as the temperature reduces. We attribute the reduction in S in the SiNW arrays to a restriction of phonon transport in the nanowire. We find $S_{NW} \sim 3S_{bulk}$ at room temperature, and $ZT_{NW} \sim 100ZT_{bulk}$. This result demonstrates a large increase in the fundamental TE behaviour of SiNWs in comparison with bulk Si.

We now discuss the characteristics of the moderately doped SiNW arrays. S in bulk Si and SiNW arrays of ∼30 and 40 μm long was measured, and S was found to decrease with temperature. However, in the case of the 30 μm long SiNW arrays, an increase in the magnitude of S by a factor of ∼2.5 with respect to bulk Si was observed.

Finally, two terminal I-V measurements of SiNWs, for the two doping levels (5×10^{15} – 5×10^{14} cm^{-3} and 10^{18} – 10^{17} cm^{-3}), and I-V curves characterised in the temperature range ∼300 – 40 K. The electrical characteristics for the moderately doped sample illustrated minimal change in the conductance from bulk Si sample to a SiNW sample, implying that the NW conductivity was not strongly affected. In contrast, in lightly doped samples, a strong reduction was observed in the conductance of SiNWs vs. bulk Si. This may be related to a relatively stronger influence of traps at the NW surface, determining the number of electrons available for conduction. To overcome surface traps, passivation of the NW surface as a means to overcome surface traps was performed by using polymer filled. This may act as an electron donor or hole acceptor and lead to better electrical characteristics. The temperature dependence of the I-V characteristics in n- and p-type polymer filled NWs was measured. However, an improvement was observed only in the electrical characteristics of p-type PAA filled SiNWs. At room temperature, an increase in current of the polymer filled SiNWs by a factor of ∼1.25, with respect to bare Si, was

measured, but as the temperature decreased, an improvement by a factor of $\sim 10^6$ was found. In general, at temperatures below 190 K, a drastic increase in current of the PAA filled SiNW was observed.

Thermal conductivity of the 30 μm long SiNW arrays was measured with a transient measurement of ΔT vs. time t. Here, the time constants τ of the exponential decays in ΔT vs. time t, in both bulk Si and the SiNW array samples were measured. Using the known values of κ_{Bulk} from Ref. [84], and multiplying these by the ratio τ_{Bulk}/τ_{NW} $= \kappa_{NW}/\kappa_{Bulk}$ allowed an estimate of κ_{NW}. We find that κ_{NW} remains approximately constant from 300 – 80 K, at a value of $\sim$30 W/mK, implying that the phonon mean free path l_p remains approximately constant, as this is restricted by the NW widths.

Finally, we estimate ZT for the moderately doped 30 μm long SiNW sample. In the NWs, we assume σ ranging from 10^4 Ω^{-1}m^{-1} to 0.33×10^4 Ω^{-1}m^{-1}, unchanged from the bulk value. This assumption is supported by both our SiNW array I-V characteristics (section 6.1.2) and by the high field-effect mobility observed in SiNW FETs [121]. We first calculated ZT for our raw data and find a maximum $ZT \sim 0.0255$ at 300 K. This is an increase by a factor of $\sim$100 compared to bulk. With decreasing T, the enhancement in ZT over bulk increases, reaching an average increase by a factor of $\sim$ 210 versus bulk. Below 140 K, an increase over bulk by a factor of > 250 is observed. These data are then corrected for the temperature drop at the top Cu block in our measured S values. In this case $ZT = 0.09 – 0.28$ at 300 K, an improvement by a factor of $\sim$40 over bulk. At 280 K, $ZT = 0.34 = 55ZT_{Bulk}$, this is the best possible ZT, within the range necessary for practical application of TE effects in a material.

In previous work, only thermoelectric characteristics of p-Si nanostructures were characterised. In Hochbaum *et al.* [86], SiNWs were fabricated by aqueous electroless etching. Here, κ in single SiNWs of different diameter and different doping level, $10 – 10^2$ Ωcm, was measured as a function of temperature in the range 300 – 20 K. In a 52 nm diameter heavily doped SiNW (10^{-1} Ωcm), $\kappa = 1.6$ W/mK. S and σ were characterised in a heavily-doped 48 nm diameter SiNW. Finally, ZT ≈ 0.6 was calculated at 300 K. Hochbaum *et al.* [86] argues that the reason for this significant decrease is due to increased surface scattering of phonons.

In Boukai *et al.* [87], a few hundred heavily doped p-SiNWs were characterised. Here, SiNWs were fabricated using the superlattice nanowire pattern (SNAP) method. NW

Ref.	S (μV/K)	σ (Ω^{-1}m^{-1})	κ (W/mK)	ZT	T (K)
Hochbaum *et al.* [86]	250	6×10^4	1.6	0.6	300
Boukai *et al.* [87]	386	1×10^5	3	1	200
Tang *et al.* [88]	260	3.1×10^4	1.73	0.4	300
This work	1480	1×10^4	23	0.34	280

Table 7.1: Thermoelectric parameters (S, σ, κ) and ZT for silicon nanostructures. In the case of Boukai *et al.* [87], data were taken from the supplementary material.

arrays of several micrometer length were prepared with a lateral width × thickness dimensions of 10 nm × 20 nm and 20 nm × 20 nm. $\kappa = 0.76$ Wm^{-1}K^{-1}, surprisingly below the amorphous Si limit, was found for the 10 nm wide NW. In the NWs with a doping level of 7×10^{19} cm^{-3}, the highest S^2 value was observed. Finally, ZTs in 20 nm and 10 nm wide NWs, corresponding to two different doping levels, were measured. $ZT \approx 1$ was measured at 200 K for the 20 nm wide NW with doping level 7×10^{19} cm^{-3}, and $\kappa = 3$ Wm^{-1}K^{-1}(data presented in supplementary information of [87]). Boukai *et al.* argue that the increase in S is due to the phonon drag contributing to the electron transport as a consequence of a crossover from a three-dimensional to a one-dimensional behaviour.

Tang *et al.* [88] fabricated a different type of nanostructure, namely 'holey' silicon. Here, high density nanoscopic holes of p-Si with dimension of 350, 140 and 55 nm were created in thin 100 nm single crystalline silicon membranes, 5×10^{19} cm^{-3} doped, either by nanosphere lithography or block co-polymer lithography. A minimum $\kappa = 1.73$ Wm^{-1}K^{-1} at 300 K was measured for the 55 nm holey ribbons. A maximum ZT of ∼0.4 was measured at 300 K. This corresponds to a 40 times increase in ZT compared to their counterpart bulk Si, consistent with the results measured in Refs [86, 87].

Our work on the temperature dependence of the Si nanostructures were carried on n-type SiNWs of two different doping, light and moderate doping. A $ZT = 0.28$ measured at 300 K is in accordance with results obtained by others [86, 87, 88]. Tab. 7.1 shows a summary of best ZT results in silicon nanstructures performed by Hochbaum *et al.*, Boukai *et al.*, Tang *et al.* and the work of this thesis. In the table are also reported the thermoelectric parameters (S, σ, κ) and the temperature of the best ZT.

The maximum measured S in the Si nanostructures is 1480 μV/K, measured in this thesis for the 30 μm long SiNW arrays, followed by 386 μV/K measured in 20 nm wide NWs, fabricated by Boukai *et al.* [87]. The maximum $\sigma = 1\times10^5$ Ω^{-1}m^{-1} is given by the 20 nm wide NWs, in Boukai *et al.*. κ measured in Hochbaum, Boukai, and Tang *et*

al., are similar in value, with the lowest $\kappa = 1.6$ W/mK obtained in Hochbaum *et al.*. κ measured in this thesis is ∼14 times higher than that measured in Hochbaum *et al.* [86], but the doping of our SiNW is lower than that present in other work (10^{18} cm^{-3}). Finally, the maximum $ZT \approx 1$ at 200 K, was calculated in Boukai *et al.* [87], this may be a consequence of the very high value of σ. Our calculated $ZT \approx 0.34$ at 280 K is very good and comparable to that calculated in Hochbaum *et al.* [86] and Tang *et al.* [88]. The increase in our ZT is associated to the increase in S and the decrease in κ.

Future work

It is possible to envisage various experiments on SiNWs, to extend the thermoelectric measurements presented in this thesis. The temperature dependence of the Seebeck coefficient for p-SiNWs of different length and different doping, and heavily-doped n-SiNWs (∼10^{19} – 10^{20} cm^{-3}), can be performed in the future. Temperature characterisation of p-type SiNWs would allow a comparison with results obtained for the n-SiNWs. Measurements of p-SiNW arrays are important, in order to integrate n- and p-type SiNW samples into n- and p- generators for a full and practical TE device. Heavily-doped Si may lead to a further increase in the room temperature ZT. In other works by Hochbaum *et al.* [86], Boukai *et al.* [87] and Tang *et al.* [88], the utilisation of heavily-doped Si has led to a $ZT > 0.4$ at 300 K.

It is also important to find the dependence of ZT across a wider temperature range, including at very high temperatures (600 – 700 K) in order to find the peak and the corresponding temperature for ZT. This is essential to determine the temperature range of the device and where it is most efficient.

Other nanostructures, such as nano-crystalline SiNWs [133] and SiGe NWs [134, 135], can also be considered and further investigated to fully characterise their thermoelectric performance and to measure their ZT. The additional nanostructure in these materials, e.g. associated with nano-crystalline Si grains or with SiGe/Si superlattices may allow further manipulation and phonon scattering, leading to an even lower κ and hence a greater ZT. In the work of Neophytos *et al.* [133], a simultaneous increase in S and σ was found for p-type heavily-doped nano-crystalline Si with grain sizes of ∼30 nm and grain boundaries of ∼2 nm. Here, the nano-crystalline Si material was fabricated by depositing thin layers of nano-crystalline Si films (200 nm in thickness) onto an oxidised Si substrate by chemical

vapour deposition. The material doping density was $\sim 5.6 \times 10^{19}$ cm^{-3}, and S and σ were five times greater than bulk Si. This improvement was attributed to an increase in carrier filtering due to the energy barriers at the grain boundaries. Another factor influencing the improvement in S and σ was related to the non-uniformity of lattice thermal conductivity between the grains and grain boundaries [133]. Xu *et al.* [134, 135] have measured the Seebeck coefficient and power output of TE devices based on SiGe NW arrays of different length and different Ge concentration at ambient conditions. In Xu *et al.* [135], S and the power output of n-Si–p-$Si_{1-x}Ge_x$ NW arrays were measured for concentration x changing between 0 to 0.4, at room temperature. Here, SiNW and SiGe NW arrays were fabricated with the MACE process, creating $\sim 10^7$ vertically-aligned NWs [135]. The measurements indicated that utilisation of SiGe NW arrays with length less than 30 μm led to an increase by a factor of 10 in the output power of the p-n TE device.

Polymer filled NWs can also be investigated further to study their effect on σ. While the effect of polymer filling on SiNW array conductance has been presented within this thesis, the effect on S and κ has not been investigated due to time issues. Temperature measurements of S and κ on polymer filled SiNWs and a measurement of ZT remains to be performed. Hence, ZT will also be characterised. In addition, different polymer can be considered for n-SiNWs, as PAA filled n-SiNWs did not lead to an improvement in the electrical conductivity.

In summary, there are a number of approaches possible to further characterise and improve the thermoelectric performance of SiNW based structures. These approaches may be used to further increase ZT in this system to ~ 1 or even greater, with values similar to the best bulk Bi_2Te_3 based materials. This may open the way for practical application of low-cost, efficient TE devices in Si.

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