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In-body Power Transfer and Data Communication for Active Neural Implants

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Declaration of Originality

I hereby certify that the work presented in this thesis is my original own. All material in this thesis which is not my own work has been properly acknowledged. All material that I have adapted for this work has been identified as such and where applicable the original source cited.

October 2021, Dorian Hacı

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Abstract

The advent of *active implantable medical devices* has led to a paradigm shift from previous solutions to medical conditions. The remarkable success of early therapeutic devices, such as the cardiac pacemaker, has encouraged the development of more advanced systems, expanding the reach and ambition of implantable devices - now targeting significantly more complex diseases and treatments. *Neural implants*, which are able to effectively interact with the nervous system, are an important example of this progress. Such medical devices have demonstrated a significant impact on the quality of life of millions of patients worldwide, e.g. with treatments of Parkinson's disease and Epilepsy. Neural implants have evolved in the years, transitioning from open-loop neuromodulators to *closed-loop neuromodulators*. These includes also a monitoring function in addition to stimulation. This method allows to activate the intervention only when required and to receive feedback on the effectiveness of the treatment.

More recently, to target the limitations of the single-module implants new generations of AIMDs are emerging that are based on a *multi-module approach*: the system is now partitioned and distributed across multiple implants, each with specific functions and located at different sites. Distributed systems promise to give clear advantages, paving the way for numerous medical applications requiring high-channel stimulation and sensing to/from many locations in the body. However, they introduce a new set of challenges, both at the development and deployment stages. These are related to additional design considerations specific to the presence of multiple modules within an implanted system.

This thesis investigates power transfer and data communication between multiple implanted devices and the development of interfacing circuits, which will contribute towards the implementation of a modular closed-loop AIMD for treating *refractory focal Epilepsy*. The specific objectives of this investigation have been framed to address the key challenges in the creation of a medical device for clinical trials, thus prioritising adequate performance of the medical functions, while ensuring implant system reliability in a human body. A custom protocol has been developed – the *4WiCS* – and circuits for inter-module connectivity have been designed, implemented, and fabricated in CMOS and PCB technology. These have been tested within an end-to-end platform, informing further design of a novel fully-integrated System-on-Chip – the *CANDO4 SoC* – fabricated as part of the CANDO project neural implant.

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‘Always be respectful to others. You don’t know what they have gone through in their lives.’

Ndue Haci

‘Always demand respect from others. They don’t know what you have gone through in your life.’

Roza Maca Haci

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List of Acronyms

4WiCS	4-Wire Communication System
AC	Alternating Current
AIMD	Active Implantable Medical Device
ADC	Analogue to Digital Converter
ANT	Anterior Nucleus of the Thalamus
AP	Action Potential
ASIC	Application-Specific Integrated Circuit
BER	Bit-Error Rate
BI	Brain Implant
BMI	Brain-Machine Interfaces
BP	Body Potential
BPE	Body Potential Electrode
BRC	Body Reference Circuit
CAN	Controller Area Network
CANDO	Controlling Abnormal Network Dynamics using Optogenetics
CDR	Clock and Data Recovery
CI	Central/Chest Implant
CLA	Current Limit Amplifier
CMOS	Complementary Metal–Oxide–Semiconductor
CMRR	Common-Mode Rejection Ratio
CP	Charge Pump
CRC	Cyclic Redundancy Check
CS	Chip Select
DAC	Digital to Analogue Converter
DC	Direct Current
DBS	Deep Brain Stimulation
DCU	Data Communication Unit
DL	Downlink Communication

DRE	Drug-Resistant Epilepsy
E2E	End-to-End
EA	Error Amplifier
ECoG	Electrocorticography
EEG	Electroencephalography
EMI	Electromagnetic Interference
ESD	Electrostatic Discharge
FDA	Food and Drug Administration
FFT	Fast Fourier Transform
FIFO	First-In-First-Out
FPGA	Field Programmable Gate Array
FSM	Finite State Machine
GUI	Graphical User Interface
HDL	Hardware Description Language
HV	High-Voltage
I2C	Inter-Integrated Circuit
IC	Integrated Circuit
ICD	Implantable Cardiac Defibrillators
IDE	Integrated Development Environment
ILAE	International League Against Epilepsy
IPG	Implantable Pulse Generators
I/O	Input-Output
LDO	Low-Dropout (Regulator)
LED	Light Emitting Diodes
LFP	Local Field Potential
LPF	Low-Pass Filter
LV	Low-Voltage
MCU	Micro-Controller Unit
MCLK	Master Clock
MEA	Microelectrode Arrays
MISO	Master Input Slave Output
MMNI	Multi-Module Neural Implants
MOSI	Master Output Slave Input
MPW	Multi-Project Wafer
MRI	Magnetic Resonance Imaging

MRST	Master Reset
MUX	Multiplexer
NHP	Non-Human Primate
NMOS	N-Channel MOSFET Transistor
NNP	Networked Neuroprosthetic
OTA	Operational Transconductance Amplifier
PCB	Printed Circuit Board
PCE	Power Conversion Efficiency
PC+S	Primary Cell + Sensing
PFD	Phase and Frequency Detector
PLD	Programmable Logic Devices
PLL	Phase-Locked Loop
PM	Power Management
PMOS	P-Channel MOSFET Transistor
POR	Power-on-Reset
PTE	Power Transfer Efficiency
RAM	Random-Access Memory
RC+S	Rechargeable Cell + Sensing
RNS	Responsive Neurostimulation
ROM	Read-Only Memory
RTL	Register Transfer Level
SAR	Successive Approximation (Converter)
SC	Switched Capacitor
SCK	Serial Clock
SDI	Serial Data In
SDO	Serial Data Out
SI	Satellite Implant
SoC	System-on-Chip
SPI	Serial PeripheralInterface
UL	Uplink Communication
UART	Universal Asynchronous Receiver-Transmitter
VCO	Voltage-Controlled Oscillator
VNS	Vagus Nerve Stimulation
WHO	World Health Organisation
WPT	Wireless Power Transfer

Chapter 1

Introduction

1.1 Motivation

Thanks to the remarkable achievements obtained from decades of research in medical and biomedical sciences, our knowledge about the human body and its functioning have drastically changed the outcomes for many diseases. For example, in the years between 2000 and 2015, the percentage change in causes of death in the United States had decreased for many severe diseases, e.g. HIV (-60.6%), stroke (-12.7%), and heart disease (-8.9%) [1]. This has been possible due to a deeper understanding of such disease state, which has allowed for early detection and intervention.

Unfortunately, the mortality rate due to disorders related to the nervous system has not seen a decrease. Mortality due to Alzheimer’s disease for example has more than doubled (+145%) in the same time window and is expected to continue to grow [2]. Not only mortality but also morbidity – the condition itself of being diseased – due to neuropsychiatric disorders and mental illness is at the highest: this is evaluated in terms of disability-adjusted life years (DALYs) by the World Health Organization (WHO) and is measured to be at 28.47% [3]. In other words, this means that more than a quarter of disabilities from all medical causes can be attributed to neurological disorders. This number is even higher when considering low- and middle-income countries.

In addition, chronic conditions such as Parkinson's disease and Epilepsy, carry a significant burden to both the individual and their families/carers, as well as to society as a whole. Also sudden onset conditions due to damage to the nervous system, e.g. traumatic brain injury and spinal cord injury, add up to this financial and social load. It has been estimated from a study in 2011 that the total cost of brain disorders, in a European population of around 500 million back then, was a staggering €266 billion [4]. It is not surprising to learn that for the past decade the cost per capita has been rising further. Many aspects contribute to these dramatic figures. For example, the progressive ageing of the population is making more and more people worldwide contracting age-related neurological disorders, such as different forms of dementia. Not to mention the alarmingly rising number of people suffering from major depression, often triggered by social and relational factors. The most critical factor, when compared to non-neurological conditions, is the limited availability of effective therapeutic interventions. The main reason for this is to be found in the challenge of understanding and interacting with the nervous system and its central unit: the *brain*.

The brain is the most complex and arguably the most interesting organ of the human body. For centuries its characteristics and behaviour have been studied for explaining the causal relationship between our thoughts and our actions/interactions. Nonetheless, the nervous system remains by far the most undiscovered part of our body due to its complexity and cellular density. It may feel discouraging to know that to fully comprehend the function of the brain we need to decode the immense number of interactions between the neurons. At the same time, what is largely understood and characterised is the single intracellular communication link between neurons and how to interface with it, which provides us with the basic element of the electrical language neurons use to communicate with each other: the action potential.

The recent progress in microtechnology has allowed for active devices to effectively connect to the nervous system by exploiting the electrical properties of these nerve cells, both for understanding and explaining its behaviour and for intervening when its normal functioning is impaired [5]. Devices with these capabilities, referred to as Neural Interfaces (NI) or Brain-Machine Interfaces (BMIs), give rise to fascinating possibilities in the treatment of neurological conditions and in prostheses application [6].

The outstanding success of implantable neural interfaces, called also **neural implants** – e.g. deep brain stimulators and spinal cord stimulators – has proven that even with limited knowledge of the functioning of the nervous system, it is possible to have a highly positive impact on the life of people suffering from neurological conditions. For this reason, in the past few years, there has been a surge in the development of novel implantable neurotechnologies. These come both from established players in the medical device industry and from emerging research groups and companies – run by ambitious leaders and entrepreneurs. In fact, we are now entering a tremendously exciting era, in which brain research is no longer confined to just a few neuroscience laboratories. Technology advancements in implantable microsystems are enabling new tools not only for scientific discovery but also translational opportunities and clinical application.

Many challenges arise when dealing with the development of active implants for the human body. These are mostly due to their characteristic of being subcutaneous and in electrical contact with the biological tissue. In order to perform their function in such a harsh environment for electronics and to avoid any risks for the body, these devices require conformity for bio-compatibility and reliability. In addition, an increasing number of applications in the treatment of neurological diseases is requiring neural implants to include more “smart-capabilities”, in terms of efficiency and selectivity of the interventions, and to be able to interface with multiple locations in the human body. This has initiated the generation of implant systems which (1) combine both monitoring/sensing and stimulating functions (closed-loop) and (2) are distributed in different locations – to acquire a better holistic view of the nervous system activity and to apply the medical intervention from multiple angles.

This modular approach brings in new questions associated with how these modules interact with each other and with the surrounding tissue, and how these interactions affect the functionality and performance of the single modules and of the system. Moreover, the design and implementation of such devices must be achieved in the context of a clinical framework, thus considering the patient needs and “user’s requirements”. This translates into ensuring the technology developed delivers effectively the clinical benefits, without compromising patient safety and reliability implant system.

1.2 Research Objectives

The aim of this research has been to investigate power transfer and data communication between multiple implanted devices. To achieve this, an end-to-end interfacing system was designed and implemented. This will contribute towards the development of a modular active implantable medical device for treating refractory focal Epilepsy.

The specific objectives of this investigation have been framed to address the key challenges in developing a closed-loop multi-module device suitable for use in human trials. This translates into the need for prioritising adequate performance of the medical functions – simultaneous monitoring and stimulation of neural activity – while ensuring implant system reliability in a human-body environment. These objectives are:

1. In-body wireline power transfer and data communication

- Explore power transfer techniques, ranging from power delivery/recovery methods to power conversion circuit architecture, in order to design and implement a power management interfacing system that allows for multiple implants to operate from a single energy source located at one of the implanted modules.
- Investigate the development of a full-duplex data communication between modules that is optimised for the specific application and physical communication channel. This custom protocol needs to meet the data throughput requirement in both directions (master-to-slave and slave-to-master), allowing for neural recording (brain monitoring function) to operate while other functions are performed – e.g. stimulation.

2. System integration challenges and considerations

Implement a platform integrating the end-to-end in-body interfacing system in order to:

- verify feasibility and scalability of a modular approach for implantable systems;
- demonstrate the proposed interfacing system maintains the required performance while ensuring the neural recording and stimulation are functional in operational conditions;

- evaluate the system integration challenges that could potentially compromise both the interfacing system and the core medical function performance.

3. Monolithic integration of the in-body interface within a chip-scale implant

While taking into account (1) the clinical and technical requirements set by the CANDO project, (2) the results obtained from the system integration evaluation and the tests, and (3) the technology limitations/constraints:

- Generate a set of specifications for an integrated circuit that can be integrated within a chip-scale medical device for implantation in the brain and that prioritises system reliability and patient safety;
- Implement the next generation of the in-body interfacing circuit based on this specification document. This will be monolithically integrated with the circuitry responsible for performing the medical core functions – recording neural activity, driving optical stimulation.

1.3 The CANDO Project: A Collaborative Endeavour

This research is part of the CANDO Project and in collaboration between several teams from Imperial College London, University College London, Newcastle University, and Newcastle-Upon-Tyne Hospitals NHS Trust. CANDO has been funded under the Innovative Engineering for Health programme by the Wellcome Trust and EPSRC, receiving £10m support over 7-years. During the doctorate programme, the Ph.D. thesis author has been a member of the CANDO team for 5 years. This way he was exposed to a multi-disciplinary environment, to a "design with the user in mind" approach, and to regulatory procedures and documentation.

The following members of the CANDO project group have contributed to this doctorate research. They are listed with their current roles – at the time of writing this document – and with their responsibilities when involved within the CANDO project.

- *Mr Dorian Hacı* (Ph.D. thesis author), Imperial College London, Research Assistant.
Responsible for the design, implementation, and test of the in-body interfacing system.
- *Dr Tim Constandinou*, Imperial College London, Professor.
Supervisor, line manager, and Co-Principal Investigator within the CANDO project.
- *Dr Yan Liu*, Shanghai Jiao Tong University, Associate Professor.
Co-Supervisor and lead microelectronics designer within the CANDO project.
- *Dr Sara Goreishizadeh*, University College London, Lecturer.
Co-Supervisor and lead designer of the first version of the 4WiCS ASIC.
- *Mr Andrea Mifsud*, Imperial College London, Research Associate.
Electronic designer of the 4WiCS chest implant interface – hardware and software.
- *Dr Nick Donaldson*, University College London, Professor.
Co-Principal Investigator within the CANDO project.
- *Dr Patrick Degenaar*, Newcastle University, Professor.
Co-Principal Investigator and Engineering Lead within the CANDO project.
- *Dr Andrew Jackson*, Newcastle University, Professor.
Lead Principal Investigator within the CANDO project.

1.4 Outline of the Report

The rest of this thesis is divided into six chapters: the first two introduce background and literature review; the middle three present the work done to answer to the research questions, derived from the above-presented research objectives; the last chapter concludes the report.

- Chapter 2 provides essential background on active implantable medical devices, focusing on implants connecting to and interacting with the nervous system. An overview of neuromodulation is given, highlighting the differences between the open-loop and closed-loop approaches.

The next generation of neural implants, based on a modular approach, are then discussed with considerations on their challenges and opportunities.

- Chapter 3 introduces the CANDO project, describing in detail the project goal and approach. The clinical application targeted by CANDO – drug-resistant epilepsy – is introduced; existing solutions based on neural implants are discussed. The method developed by CANDO – based on an optogenetic, closed-loop, multi-module neural implant – is outlined with a description of the novelties proposed, both from a scientific and engineering perspective. The medical device is eventually presented, defining its requirements, specifications, and functions.
- Chapter 4 presents the design, implementation, and test of the 4WiCS inter-module interfacing system created for the CANDO multi-module medical device. Its functional characteristics are first introduced. The three main components of such an interfacing system are then detailed. These are the 4WiCS brain implant interface (integrated circuit), the 4WiCS chest unit interface (printed circuit board), and the interfacing channel (implantable cable).
- Chapter 5 describes the development of an end-to-end platform, which integrates the modules of the CANDO implant system – including the 4WiCS interface – in order to implement system integration testing and verify the 4WiCS end-to-end functionality. This platform is characterised first for power transfer and data communication. Key design considerations are then made in terms of power management/efficiency, recording performance, system reliability, and safety.
- Chapter 6 presents the design and implementation of the latest generation of the CANDO4 microelectronics for the brain implant modules – the optrode system-on-chip. This includes two sub-systems: the CANDO4 CORE and the CANDO4 4WiCS. These are described at a circuit level and simulations are presented for the 4WiCS power management and data communication circuits, both at a block level and system level.
- Chapter 7 concludes the dissertation, highlighting the author’s original contribution. Plan and suggestions of future work and improvements are discussed, followed by personal final thoughts from the Ph.D. thesis author.

Chapter 2

Active Implantable Medical Devices

The need for safer and more effective medical treatments, supported by recent advances in microsystem technologies, has paved the way for the development of a wide range of **Active Implantable Medical Devices (AIMDs)**. As defined by the European Directive 90/385/EEC on Active Implantable Medical Devices, an AIMD is *"any active medical device which is intended to be totally or partially introduced, surgically or medically, into the human body or by medical intervention into a natural orifice, and which is intended to remain after the procedure"* [7]. Because AIMD belong to one of the highest risk categories of devices, they are subject to rigorous regulatory controls both during production and clinical applications [8]. Over the past few decades AIMDs have shown remarkable success both as: (1) *therapeutic devices* in treating debilitating conditions; and (2) as *prosthetic devices* in restoring functions by bypassing dysfunctional organs/pathways [9].

This recent history of successes was pioneered by the most famous implant: the *cardiac pacemaker*, a device that uses periodic electrical pulses to stimulate the heart and control its functioning [10]. It has been employed as a prosthetic implant for disorders where the heart is not stimulated on its own at a proper rate. An examples is heart block condition, which presents an obstruction in the electrical conduction system of the heart causing the natural pacemaker to fail [11]. The first implantable cardiac pacemaker prototype dates back to 1958. It consisted of a metallic can unit containing a battery, a coil recharging antenna, and the electronic cir-



Figure 2.1: Evolution of implantable cardiac pacemakers since the first AIMD for heart conditions.

cuit; the latter comprising two transistors and a small number of other components. Despite its simplicity, such a device managed to keep alive a patient that required resuscitation many times a day and whose situation was considered hopeless [12].

Since then, the market of implantable cardiac pacemakers has significantly increased, motivating the development of more modern and effective implants. For several decades, this established market has set the trends for the whole AIMD industry, driving toward miniaturised and multi-electrode devices. Recent developments of the technological capabilities in biosignal sensing have expanded the reach of medical implants for cardiac conditions. These now include not only Implantable Pulse Generators (IPG), but also chronic monitoring devices for real-time diagnostics of heart conditions. Such devices have brought immense benefit to patients, e.g. for atrial fibrillation – the most commonly diagnosed arrhythmia [13]. Despite their invasive nature, monitoring implants have in many cases replaced conventional wearable devices, such as holter monitors – based on wearable electrocardiogram (ECG). This is also due to the longevity of these implantable technologies and the significantly decreased risk for the patient since the first implantable cardiac pacemaker.

Thanks to advances in biocompatible materials, energy storage technology, and microelectronics, other devices more complex than cardiac AIMDs have been developed. **Neural implants** are an example of recent sophisticated AIMDs. They are defined as implantable devices with the ability to interact directly with the nervous system and are the subject of this manuscript.

2.1 Active Neural Implants

Neural AIMDs¹ have demonstrated a significant impact to the quality of life of millions of patients, by effectively connecting to the nervous system. This is achieved by intervening and altering the neural activity, exploiting the electrical properties of the interactions between the nerve cells.

2.1.1 Open-Loop Neuromodulators

Typically called *neurostimulators* or *neuromodulators*, such AIMDs are capable of stimulating the nervous system – both at a central and peripheral level – to either treat a disease/disorder or to restore a lost function.

Two examples are *cochlear implants* to aid profoundly deaf people and *Deep Brain Stimulators (DBS)* to mitigate movement disorders, such as Parkinson’s disease [14]: The former has allowed more than 600,000 deaf patients worldwide to regain some level of functional hearing, while the DBS neurostimulator has provided enormous clinical benefit for over 200,000 people with Parkinson’s disease and essential tremor (ET) by relieving and in certain cases completely suppressing the tremor [15]. Recent studies and trials have shown that DBS can be an effective treatment for certain mental health/psychiatric conditions, including obsessive-compulsive disorders, addictions, and depression [16]. Other implantable medical devices worth mentioning are *spinal cord stimulators*, with commercially available examples from Boston Scientific and Nevro, which have played a key role in the treatment of chronic pain [17]. In addition to these clinical applications, implantable devices have proven effective in treating Epilepsy. Epilepsy is one of the most severe neurological disorders. It affects 1% of the world population and the symptom that characterises this neurological state is called *epileptic seizure* – an abnormal oscillation of the nervous system.

¹In the following sections, the term *neural implants/AIMDs* is used to refer to implantable medical devices that are used to directly connect to – and interact with – the nervous system. Nevertheless, the concepts, opportunities, and challenges presented hereby are applicable to the wider AIMD field, comprising also medical devices that don’t necessarily interact directly with the nervous system, such as implantable cardiac defibrillators. This is valid also for the *open-loop*, *closed-loop*, and *multi-module approaches* discussed in this chapter.

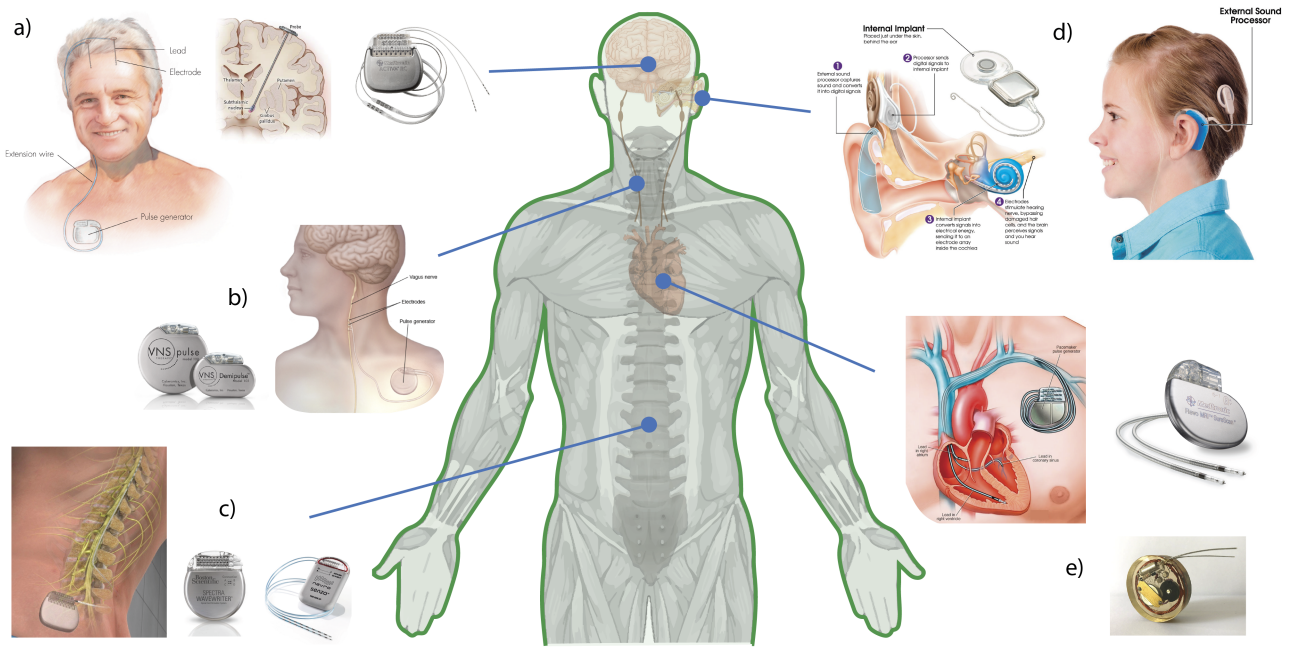


Figure 2.2: Examples of successful AIMDs: (a) deep brain stimulator; (b) vagus nerve stimulator; (c) spinal cord stimulator; (d) cochlear implant; (e) heart pacemaker

Neuromodulation regulates neural activity by electrically stimulating the nervous system with neural implants. It can be direct, by interfacing with the area of the brain where the seizure has started, or indirect, by using a specific peripheral nerve as a window to the central nervous system. An example of the latter is the *Vagus Nerve Stimulation (VNS)* technique invented by Cyberonics (now Livanova) [18]. This well-established treatment controls the neural activity in the brain by indirectly stimulating it with electrical pulses applied to the left vagus nerve. [19]. An implantable lead extends from the device (located in the chest area) to reach the nerve and an electrode is typically wrapped around it (in the neck area). New promising techniques, based instead on direct stimulation of the brain tissue, have revealed positive results. For example, deep brain stimulation for bilateral stimulation of the Anterior Nucleus of the Thalamus (*DBS-ANT*) by Medtronic has achieved a significant reduction in mean seizure frequency [20] [21]. In this case, the two implanted electrodes are inserted deep into the brain regions with rigid leads to reach the ANT in both hemispheres.

The AIMD presented so far are known as *open-loop neuromodulators*: they provide periodic stimulation signals without monitoring the biosignal activity and without closing the loop with feedback signals recorded from the brain. Despite their great success in the treatment of neu-

rological disorders, open-loop therapies lack adaptive and personalisation capabilities. In fact, most of them rely on input from clinicians to optimise and adapt the intervention to the patient's need and treatment response. The requirement for responsive and on-demand techniques in modern therapies has stimulated a recent surge in the supply of *closed-loop neuromodulators*, which offer a monitoring function in addition to stimulation.

2.1.2 Closed-Loop Neuromodulators

This relatively new category of implantable devices uses front-end neural recording, signal conditioning, and processing to obtain a real-time indication of the neural activity. This allows both to stimulate only when needed and to receive feedback on the effectiveness of the treatment [22] [23]. Closed-loop neuromodulation has been shown in many cases to be clinically more effective than open-loop neuromodulation. Effective closed-loop neuromodulation relies on: the definition of the relevant neural biomarker; the identification of the optimal location for biomarker monitoring and stimulation; the implementation of the biomarker sensing methodology and instrumentation; the differentiation and filtering of the biomarker responses from background noise/interference through signal processing; the application of decision and dose tuning algorithms to determine when and how much to stimulate [24]. Examples of neurosignals used as biomarkers for closed-loop neuromodulation are electrocorticography (ECoG) signals, local field potentials (LFP), and action potentials (APs) [25]. ECoG signals are obtained with partially-invasive cortical electrodes placed on the surface of the brain. LFPs and APs are measured with electrodes implanted into the neural tissue, they have a higher spatial resolution, and can monitor the activity of a small population of neurons and even single-unit activity.

Recent developments in microelectronics, energy storage, and implant system technologies have led to improvements in power efficiency and device integration density. Although this has led to a significant reduction of the implant volume and energy requirements, most closed-loop AIMDs retain a centralised configuration, similar to their open-loop predecessors. The control unit is typically implanted in the upper chest; it is based on a metallic or ceramic can enclosing the battery and the active electronics. This is responsible for running the closed-

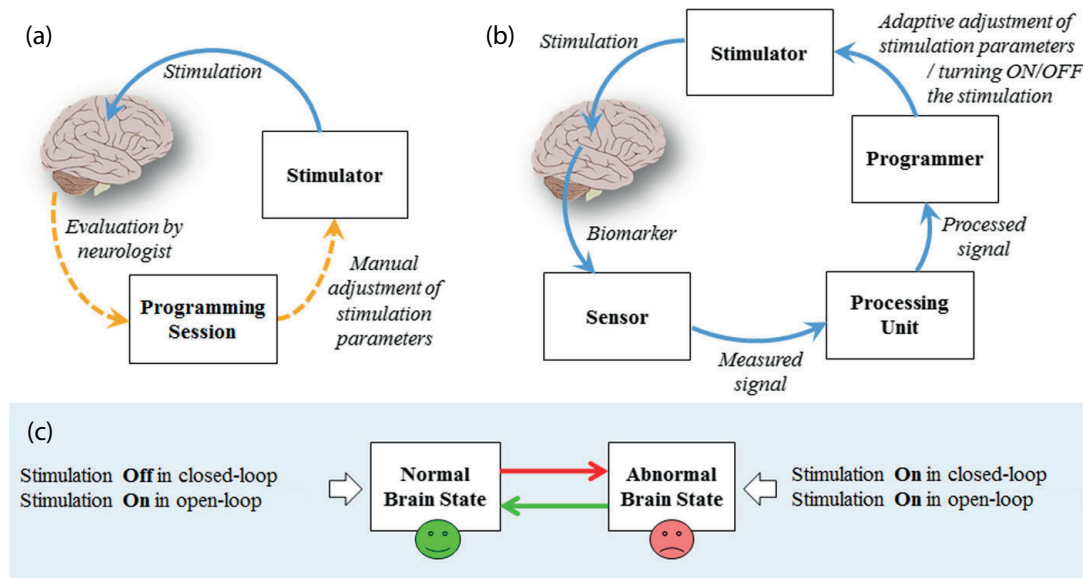


Figure 2.3: Comparison between open-loop and closed-loop neuromodulation concepts: in open-loop (a) the stimulation parameters are manually adjusted by the clinician every few weeks/months; in closed-loop (b) programming of the stimulation parameters is performed automatically based on the measured biomarker. Closed-loop neuromodulation allows for stimulation to be on only when the brain is in an abnormal state (c). Figure adapted from [26].

loop algorithm, besides converting/processing the neurosignals and activating the stimulation drivers. Implantable leads are used to reach the area of interest in the body – brain, spine, and peripheral nerves – and multiple contact electrodes are responsible for delivering the electrical pulse to the target tissue, as well as sensing the biosignal activity.

Examples of FDA-approved and CE-marked – thus now clinically-available – neuromodulation devices with both sensing and stimulation capabilities include the DBS Activa Primary Cell + Sensing (PC+S) and Activa Rechargeable Cell + Sensing (RC+S) systems from Medtronic, and the Responsive NeuroStimulation (RNS) system for refractory partial epilepsy developed by NeuroPace [26] [27]. Implants from the Medtronic Activa ”+S” family are placed in the chest or abdomen and are connected to extensions and leads implanted in the brain [28]. Like their open-loop counterpart, they deliver a controlled electrical pulse to precisely targeted areas of the brain. In addition, they have sensing capabilities, allowing for the recording of brain signals. These are measured with electrodes placed on the same lead as the stimulation ones, hence able to record activity close-by the stimulation sites. Differently from Medtronic, the approach pursued by NeuroPace is based on an implant located in the patient’s head, under the scalp, caved-in and attached to the skull, with an implant size sensibly smaller compared to

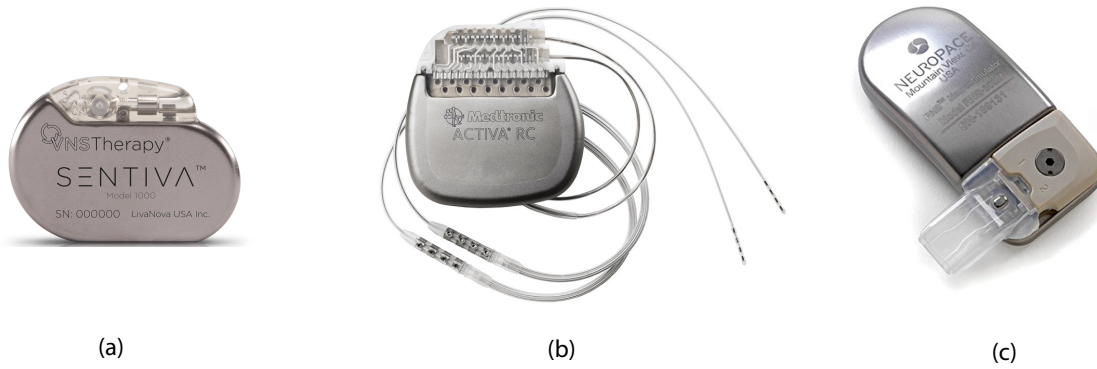


Figure 2.4: Commercial examples of active neural implants: (a) Sentiva VNS device from LivaNova; (b) Activa RC DBS device from Medtronic; (c) RNS device from NeuroPace.

other technologies - occupying a volume of 11 cc [29]. Two leads connected to the titanium case penetrate the skull through a gate connector. The extremities of the leads at the brain tissue end present different electrodes: one lead carries stimulation signals delivered through a depth penetrating electrode, while the other retrieves neurosignals through a strip of surface cortical electrodes – ECoG. The RNS system provided by NeuroPace is the first system that proposes a *true closed-loop responsive therapy* for the treatment of refractive Epilepsy, i.e. the electrical stimulation parameters are modulated in real-time in response to the measured biosignals [30].

Closed-loop applications are now requiring more recording and stimulation sites at multiple locations. This is to have a wider interfacing area for a high information throughput (recording) and a multi-directional intervention means (stimulation). However, the demand for many interfacing channels poses significant challenges for connectivity. For example, the implementation of an increasing number of implantable leads, thus of conductors in each lead, and of electrical connections/feedthroughs into the device hermetic package. Another challenge arises when trying to observe microvolt-level biopotential signals through multiple lengthy leads, as these are more prone to pick up noise and interference, presenting significant artifacts at the front-end recording[31]. Additionally, surgical and safety considerations place further requirements on how certain functions are performed in delicate locations. For example, a chest-mounted AIMD can occupy more volume (i.e. larger battery) and dissipate more power/heat (i.e. more capacity for on-board processing) than one mounted in the head.

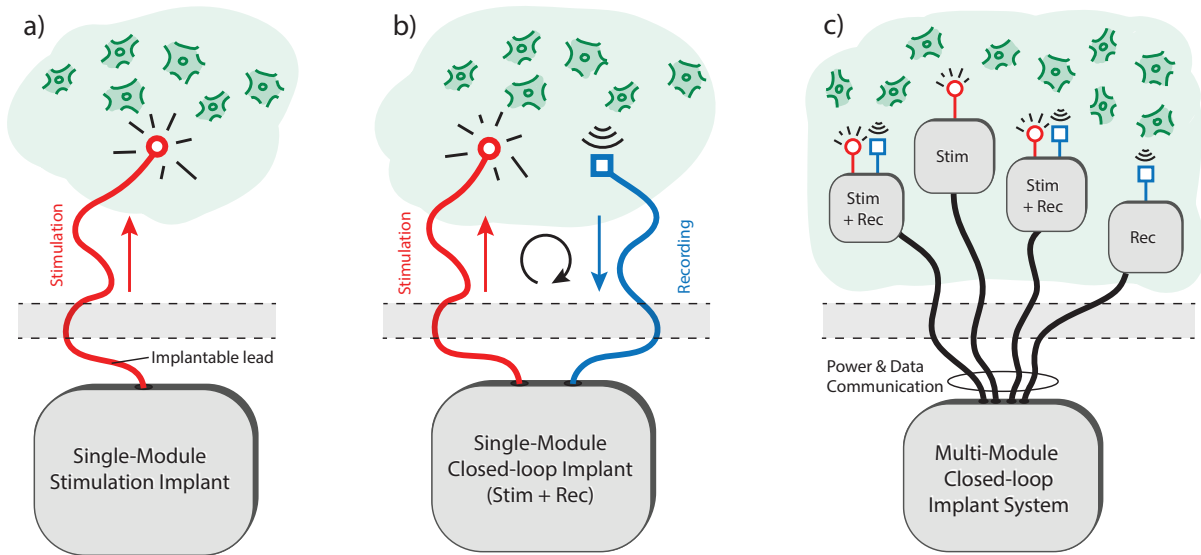


Figure 2.5: Comparison between different AIMD generations: (a) single-module open-loop stimulation-only implant, (b) single-module closed-loop stimulation and recording implant, and (3) multi-module closed-loop implant system.

2.2 Next Generation Neural Implants

To address this, a new generation of implantable medical devices is now emerging. Instead of the centralised approach that uses a single active implantable device, the system is now being partitioned and distributed across multiple neural implants, each with specific functions and located at different sites, e.g. [32] [33].

Such approach is following the trends set by advancements in the fields of *bioelectronic medicine* and *brain-machine interfaces*. The former aims at developing miniaturised implants to create new diagnostics and treatment options for patients suffering from neurological conditions [34], focusing mostly on interfacing modalities with the peripheral nervous system [35]. The goal of BMIs is instead to provide novel tools for directly connecting to the brain and decoding its activity, allowing for neural control of computers and machines, e.g., robotic arms, wheelchairs, computer cursors, virtual keyboards, etc [36].

We noticed such trend in current implantable systems and we first formally defined it as *multi-module approach* and described it in [32] and [37]. The typical configuration of these implant systems comprises of one *central module*, or central implant, and multiple smaller *satellite modules*, or satellite implants, located in close proximity of the target interface sites, as shown

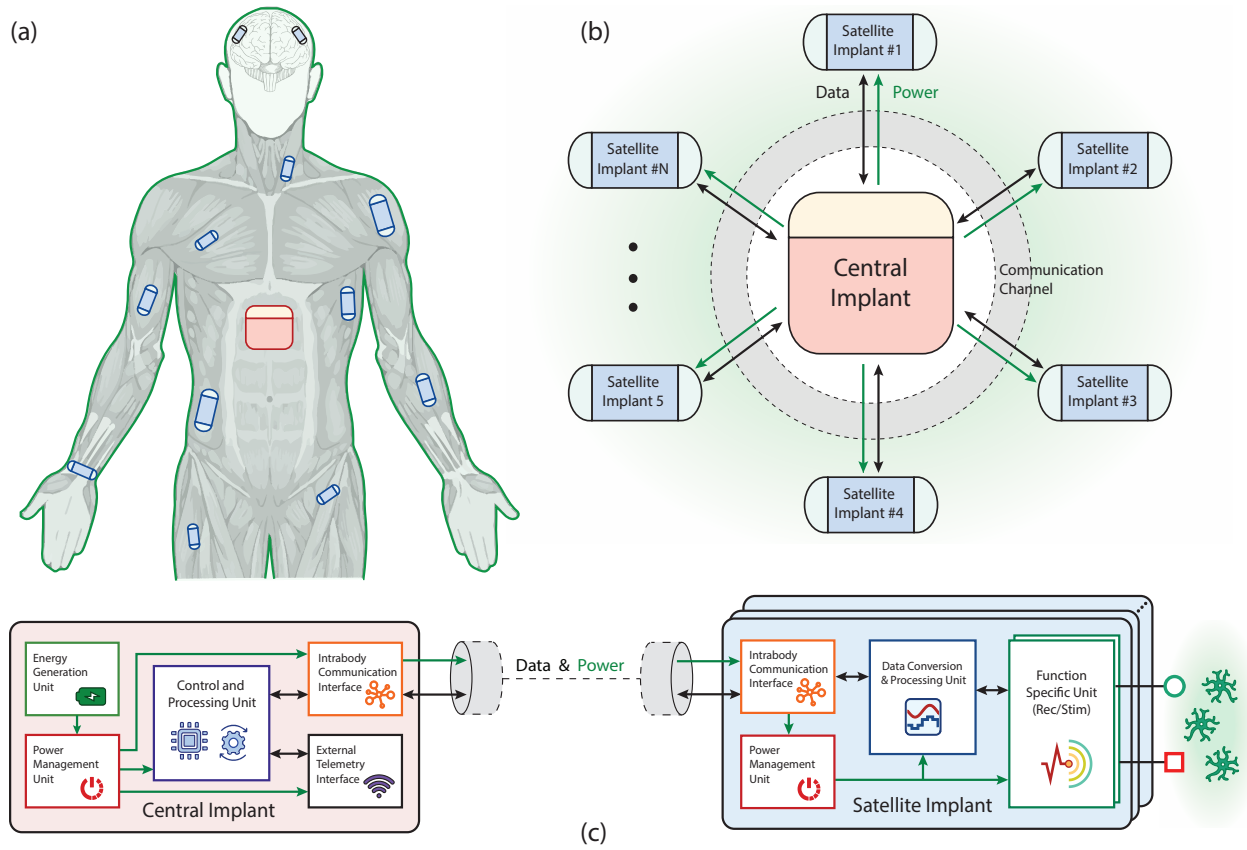


Figure 2.6: Concept of the multi-module implantable system: (a) conceptual body model with of a distributed implant system; (b) inter-module connectivity and; (c) block diagram of the internal structure of both central and satellite implants and their interfacing.

in Figure 2.6. Typically, the former includes the *energy source* (battery), *power management circuitry*, a *control and processing unit*, and *communication interfaces* to transmit and receive data to communicate with the satellite module through a communication channel. Generally, the satellite modules don't include an energy source, thus also power needs to be provided, e.g. from the central module. At the receiving end of this network, the satellite modules must also contain an *inter-module communication interface*, to interact with the network and to receive power. This will supply: (1) the *front-end function-specific units*, which can be both recording and stimulation; (2) the *power management circuitry*; (3) the *data conversion circuitry* - analogue-to-digital and digital-to-analogue; and (4) the *digital processing unit*.

Depending on the physical characteristic of the communication channel (wireless or wired), two categories of multi-module neural implants (MMNIs) have been identified: 1) *fully-wireless neural implants*; 2) *wireline neural implants*.

2.2.1 Fully-Wireless Multi-Module Neural Implants

To this group belong implant systems that include an external central module coupled wirelessly with multiple satellite implanted modules. Depending on the application, these can be located inside the skull in contact with the brain or placed subcutaneously in the proximity of the spinal cord and peripheral nerves. As this category comprises also neuromodulators besides BMIs, the satellite modules boast both recording (sensor) and stimulation (actuator) functions. They are used to form a network of distributed nodes, with the central module as hub and generator of the Wireless Power Transfer (WPT) carrier and the data communication link. In fact, such nodes do not include an implanted battery, but rather embody dedicated coils and electronics to receive the energy through the transcutaneous link. Depending on the geometric dimensions and location of the satellite modules, the wireless power carrier is optimised to achieve the highest Power Transfer Efficiency (PTE), without compromising safety and functional reliability.

In the latest years, there has been tremendous interest and significant effort among the research

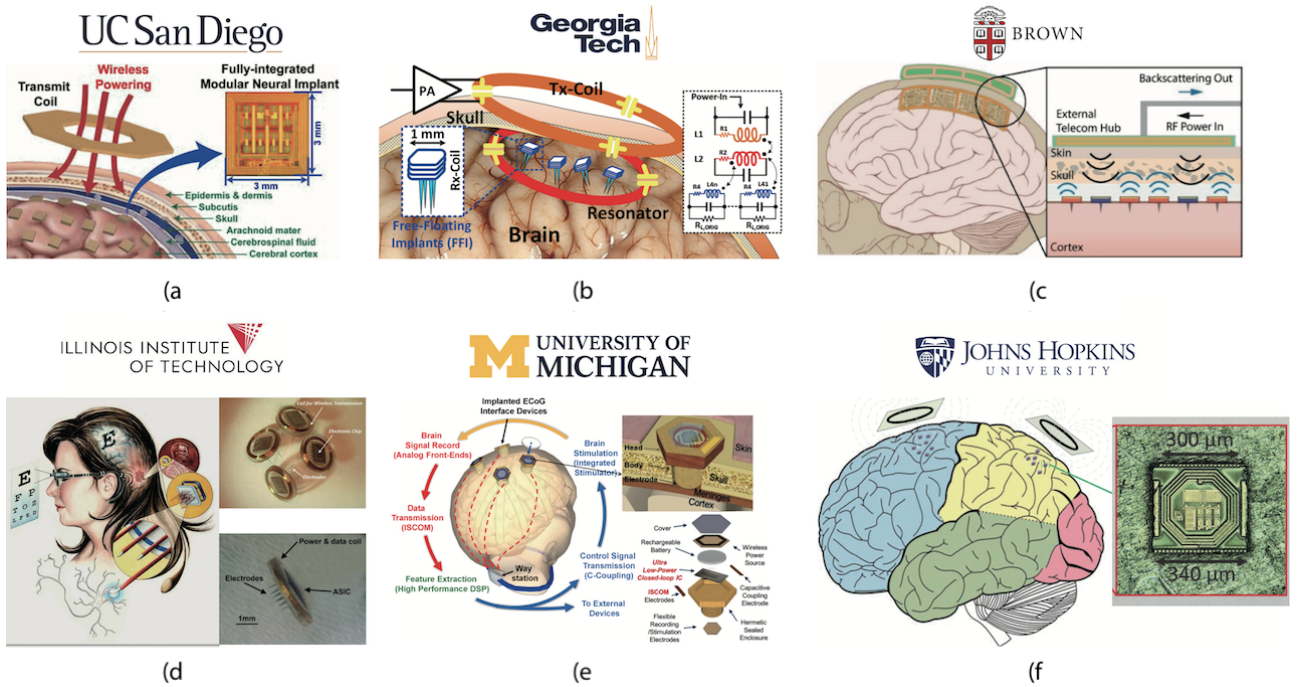


Figure 2.7: Examples of wireless distributed implants based on electromagnetic power transfer: (a) Encapsulated neural interfacing acquisition chip (ENIAC) [38]; (b) Distributed free-floating wireless implantable neural recording (FF-WINeR) system [39] [40]; (c) Human neurograin network with a 4-quadrant resonator [41]; (d) Wireless floating microelectrode array (WFMA) for intracortical visual prosthesis (ICVP) [42] [43]; (e) Distributed wireless ECoG recording systems [44]; (f) Scattered microbead implantable wireless neural stimulator [45].

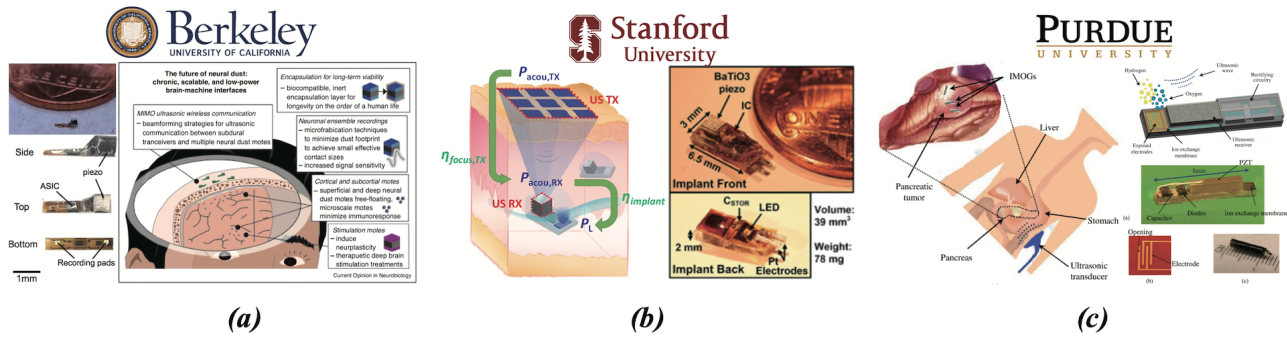


Figure 2.8: Examples of ultrasonic power transfer systems for distributed implants: (a) neural dust [46]; (b) ultrasound powered mm-sized implant [47]; (c) implantable micro-oxygen generator [48].

community in investigating different methods of implementing transcutaneous wireless networks and architectures. Examples of electromagnetic power transfer systems for distributed implants are shown in Figure 2.7.

The encapsulated neural interfacing acquisition chip (ENIAC) system from the University of California San Diego has proposed an advanced 2-coil link for powering the implanted modules [38]. Such link, however, suffers from low power transfer efficiency due to the weak coupling coefficient – maximum PTE achieved is 3.4%, even with advanced boosting techniques in use. To overcome low PTE and position miss-alignment typical of 2-coil links, various architectures based on 3-coil power links have been demonstrated. Examples are the human neurograin networks from Brown University [41] and the wireless floating microelectrode array (WFMA) for intracortical visual prostheses from the Illinois Institute of Technology [42]. The latter aims also at combining power and data telemetry on the same coil/antenna. The ENGINE probes developed within our Next Generation Neural Interfaces lab are a novel example of wirelessly powered implants based on a 2-tier power transfer [49]. Results have shown a maximum achieved PTE of 13.29% [50].

Other attempts at delivering power wirelessly to miniaturised neural implants have led to the creation of techniques based on ultrasonic waves. These are absorbed by the tissue considerably less than electromagnetic waves and have a shorter wavelength, allowing for ultra-small implants placed at different depths in the biological tissue. Although they can reach deeper penetration, power delivery based on ultrasound lacks high PTE in the short-range, thus is considered mostly for applications in the peripheral nervous system rather than in the shielded brain and spine.

2.2.2 Wireline Multi-Module Neural Implants

Despite the surge in the research and development of wireless networks of multi-module implants, they are yet to prove useful in clinical settings, mainly due to challenges related to the surgical procedures for implantation and the safety and reliability of the power delivery links [51] [52] [53]. For this reason, most of the clinically viable MMNIs require a wired connection between the individual modules [54] [55].

Inter-module wired networks comprise a central implant (CI) and multiple satellite implants (SI), with a multi-conductor implantable lead serving as a bidirectional communication channel and a power delivery medium (from CI to SI). Compared to inter-module wireless networks, this allows for: (1) a more stable communication link between the hub, CI, and the nodes, SIs; (2) a higher PTE of the power delivery, given the power loss in a highly conductive material is negligible for low currents; (3) significantly lower heat dissipation in the body, as the biological tissue itself is not part of the medium through which power is transferred. In addition, wireline implants give the possibility to transmit power signals both in direct current form (DC) and in alternating current form (AC). These advantages come at the expense of important considerations and trade-offs to be made, following the addition of an implanted lead to connect the modules. A direct consequence is an increase in the total implant system area and in the number of feedthroughs at the module end. These are the electrical connectors used to join the wires in the cable and the electronic circuits in the modules. Accordingly, key design considerations on the encapsulation are necessary to ensure system reliability and patient safety.

In medical settings, the transition from clinically-applicable and established medical devices to new generations has always been a slow process, given the barriers of regulation and demonstration of clear advantage compared to the current standard-of-care. Moreover, the development of implantable systems/hardware has historically happened in commercial sectors, where confidentiality and intellectual property often prevent the sharing of knowledge. This has led to limited literature in the field, hence very few publications on wireline multi-module medical implants are available.

The Networked Neuroprosthetic (NNP) System developed at Case Western Reserve University in Cleveland, Ohio, is a good example of a medically viable wireline implantable system [33]. The wired multipoint topology is based on one central 'power module' and daisy-chained function-specific 'remote modules' equipped with interfacing electrodes for sensing (sensor modules) and stimulation (actuator modules). These are distributed throughout the body, as shown in Figure 2.9, and aim at targeting individuals with nervous system disorders and dysfunctions, such as spinal cord injury and stroke [56] [59]. The central module, which is implanted in the chest or abdomen, delivers power to the remote modules (unidirectional) through a multi-wire lead, used also as a physical channel for data communication between modules of the system. Although the system can operate untethered from any external control, it includes communication interfaces between the central module and an external device for programming and data analysis [60]. The NNP neuroprosthesis system is designed such that it can be both modular and customised. This is to address the specific needs of paralysed patients and aiming at restoring lost functions [61]. The capabilities of the NNP system show the vast range of applications addressable by neural implants based on multi-module wireline systems and the reach they have in creating effective medical solutions.

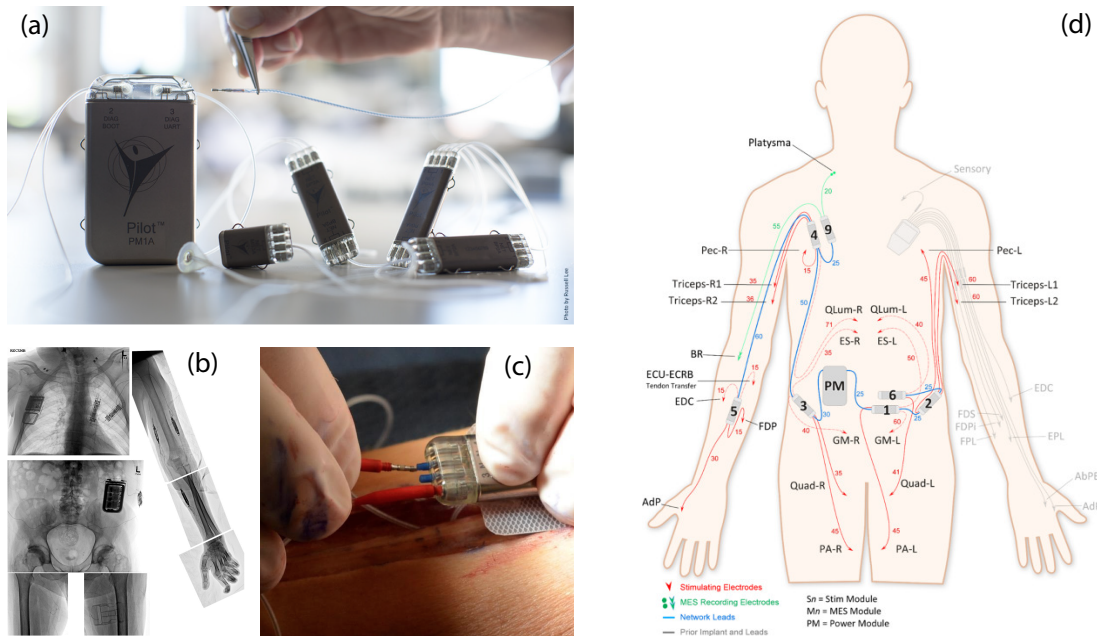


Figure 2.9: Networked Neuroprosthetic (NNP) system: (a) picture of the NNP components – the power module connects through the network cable to multiple remote modules [56]; (b) x-ray of the implanted NNP system for grasp, reach, and postural stability; (c) intraoperative picture showing color-coded connection of an electrode [57]; (d) illustration of the multi-module implant system [58].

2.3 Challenges and Opportunities

Distributed systems promise to give clear advantages when compared to single-module AIMDs, paving the way for numerous medical applications requiring multi-channel stimulation and sensing to/from many locations in the body. However, they introduce a new set of challenges, both at the development and deployment stages. These are related to additional design considerations specific to the presence of multiple modules within an implanted system. With challenges, come also opportunities. In fact, recent advancements in microsystem and integrated circuit technology give the opportunity to implement miniaturised function-specific implants, thus extending the ability to reach hostile environments such as the brain and other previously inaccessible areas of the body.

In the following, the focus is on challenges and opportunities related to *wireline neural implants*. These can be categorised into 3 groups: (1) power supply of the implanted modules; (2) communication between the modules; and (3) reliability of the implant system and, thus, patient safety.

2.3.1 Power Supply

Differently from single-module implants, which enclose the energy storage unit and the function-specific electronics in the same module, multi-module systems require energy to be transferred from the central implant, housing the battery, to multiple satellite implants, housing sensing and/or stimulation circuits. In this case, the CI acts as a *power generation unit* and the SIs as *power consumption units*. The wires in the implantable lead form the physical channel through which the power is transmitted. This can be in form of a DC signal (electrical charge flows in one direction - CI to SI) or of an AC signal (changes direction periodically). In order to avoid a DC voltage bias across the conductors in the lead, power transmission schemes based on AC-coupling are preferred and typically used in wired implant systems [62]. This allows to maintain the charge balance over time, thus reducing the risk for undesired direct current paths from being formed, if damage to the insulation occurs.

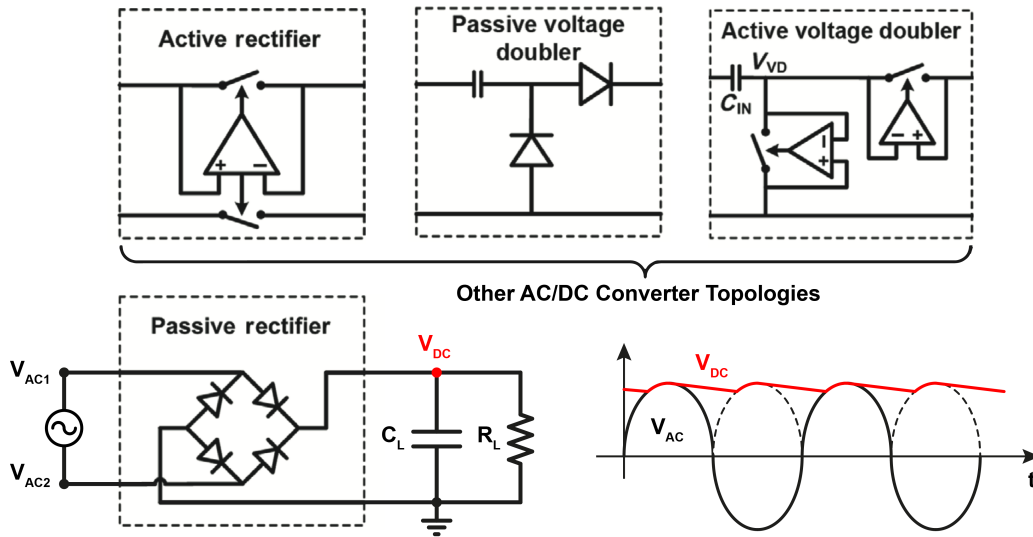


Figure 2.10: AC/DC converter topologies – passive and active rectifiers, passive and active voltage doublers – and input/output signals. Figure adapted from [63].

This requires both DC-to-AC power domain conversion to be implemented at the CI end, and an AC-to-DC conversion at the SI end. The former can be achieved by either transmitting a sinusoidal power delivery carrier through a sine-wave synthesiser or, in case the carrier is a square-wave, by employing switched-based drivers to activate the 'high' and 'low' states of the signal. At the satellite modules, AC/DC conversion needs to generate a suitable DC supply voltage for the front-end circuitry [63] [64]. When considering implementations based on integrated circuits, various AC/DC converter topologies can be used for this application, e.g., *passive rectifiers*, *active rectifiers*, *voltage multipliers*, and *hybrid configurations*.

Passive rectifiers present a simple configuration using 4 diodes [65]. Taking advantage of the CMOS technology configuration, diode-connected MOSFET transistors can be implemented; the N-well can be connected to any positive potential within the circuit, making PN junction diodes available in the standard CMOS process. Although easily accessible, passive rectifiers suffer from large voltage dropout and low PTE due to the power loss across the diodes [64]. To address this, compensation circuits can be implemented. For example, the dynamic biasing scheme ensures the body of the diode-tied MOSFET is always connected to the highest potential node in the circuit, minimizing the threshold voltage of the transistor and thus reducing the forward voltage drop across the passive diode. Another solution to the high voltage drop across passive diodes is to use Schottky diodes. These have been widely employed in conven-

tional discrete-element rectifiers and in many low-voltage high-power applications [66]. The low dropout voltage comes at the cost of high leakage current and low reverse breakdown voltage. Also, they are not available in a standard CMOS process without extra fabrication steps.

Active rectifiers, on the other hand, have higher Power Conversion Efficiency (PCE) and show to be the most promising solution [66], although their design complexity is significantly increased. They are usually based on comparators controlling the gate terminal of a pass transistor acting as a diode. The typical forward voltage drop of a passive diode or a diode-tied MOSFET is about 0.7 V, but that of an active diode can be reduced by more than 1 order of magnitude, to tens of millivolt, depending on the power transistor sizing and other specifications. *Voltage multiplier* circuits can be both passive and active, as the rectifiers. Differently from traditional rectifiers, voltage multipliers can generate a DC voltage with higher amplitude than the peak AC input. If the output voltage amplitude is double that of the input, they are called voltage doublers. Usually, this is achieved at the cost of degraded PCE, limiting the load drivability, and of additional on-chip passive storage components.

In some applications, where input amplitude can drop below the required output DC voltage, a combination of voltage doubler and a traditional rectifier can provide a reconfigurable solution. This operates as a rectifier when input peak amplitude is higher than the target DC output and as a voltage doubler otherwise. Such flexibility of switching between the two configurations depending on the application translates into an increased complexity and silicon area [67]. Besides the power form conversion given by the AC/DC, another important stage of the power transfer path is the regulation of the DC supply, which is provided by DC/DC converters. Such regulation stage is crucial for satellite implants, as these require a stable supply voltage reference to power-up stimulation drivers and noise-sensitive recording circuits.

The most common DC/DC converter is the *linear voltage regulator*. Its function is to ensure the output voltage V_{out} of the converter is stable, despite input voltage V_{in} variations. Its primary components are a variable resistive element and a feedback element. The latter controls the value of the variable resistor in order for the voltage drop to follow the input voltage variations, permitting the output voltage to maintain a steady value. The main limitation

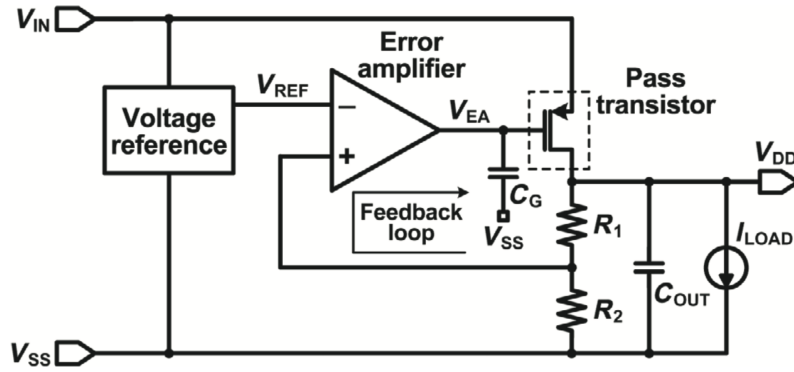


Figure 2.11: Conventional architecture of a low-dropout linear regulator. From [63].

for linear regulators is that the voltage drop on the resistive element causes energy loss (as heat dissipation) proportional to the drop. In modern integrated circuit technologies, these components are implemented with transistors. A *pass transistor* acts as the resistive element, while an operational amplifier drives it to regulate the output voltage, as shown in Figure 2.11.

Low-Dropout regulators (LDOs) are examples of linear regulators and the most employed ones in low-power implantable devices, due to their simple and compact structure and their low voltage drop across the pass transistor [68]. Moreover, they are able to provide a regulated supply voltage with minimal ripple to noise-sensitive blocks, e.g., front-end recording amplifiers.

Other methods for converting a DC voltage to another DC voltage are based on *switch-mode DC/DC converters*. These are much more efficient than linear regulators, as they can operate with lower losses – without excessive heat dissipation – and can be both step-down (output voltage lower than the input voltage, called buck converters) and step-up (output voltage higher than the input voltage, called boost converters) [69]. However, they have usually more complex circuitry with large inductive components and introduce switching noise, inherent in their characteristics. For this reason, LDOs are generally preferred in low-noise and miniaturised implantable systems.

In summary, depending on the different requirements on power efficiency, voltage levels, and performance, suitable power management and transfer techniques need to be identified, ranging from power delivery/recovery methods to power conversion circuit architecture, and circuits developed accordingly.

2.3.2 Inter-Module Communication

The presence of physical wires connecting multiple modules in an implant system gives many advantages in data connectivity/communication, such as the possibility for high-speed communications, enhanced information security, better link reliability, low or negligible attenuation even for long-distance between the modules, etc. In network theory, there are various possible arrangements of the elements within a communication network, called topologies. The most common and typically used in wired networks are the *star topology*, the *bus topology*, and the *ring topology*, as shown in Figure 2.13. Communication networks between implantable devices are usually based on a hybrid approach, combining a star topology (a central hub with multiple satellite nodes) with a bus topology (each node of the network is connected to a single cable, the ‘bus’). In this case, the central hub acts as the master of the bus, while the satellite nodes act as the slaves, receiving commands sent from the master and responding to them through the same bus.

Although standards for wireless communication for wearable and implantable devices exist, e.g. the recent IEEE 802.15.6 standard for Wireless Body Area Network (WBAN), to the best of the writer’s knowledge, standards specifically for wireline communications within the body have not been developed yet [70]. This is presumably because there are many standard protocols based on wired communications employed in other fields and they could be adapted for implant system networks depending on the medical application, the location and distance between each module, and the number of wires needed.

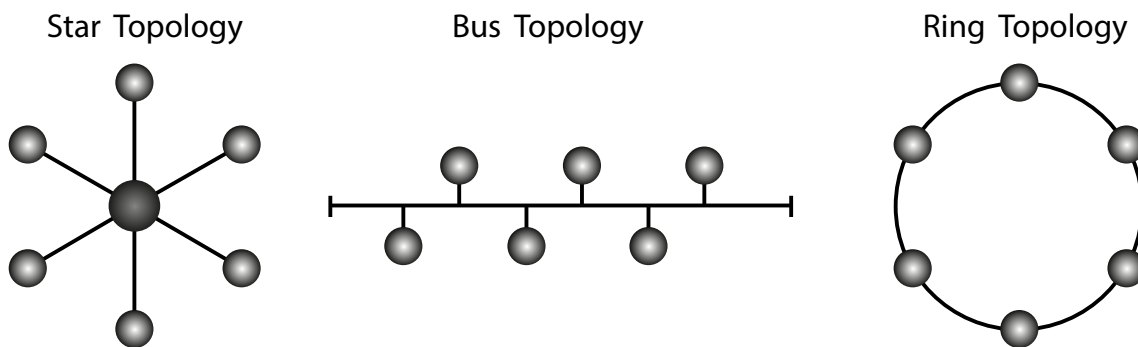


Figure 2.12: Conceptual diagram of the three most common network communication topologies: star, bus, ring.

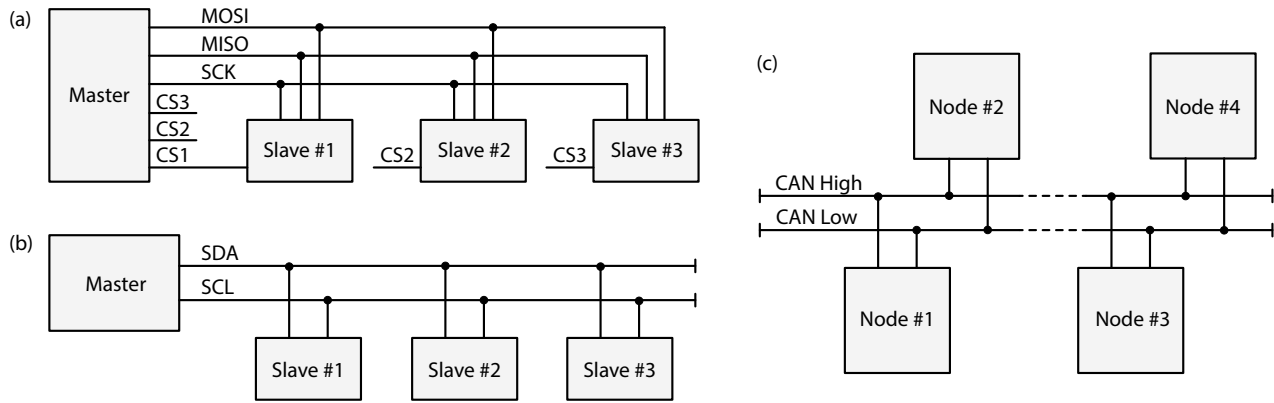


Figure 2.13: Examples of standard protocols allowing communication between multiple nodes of a network: (a) *serial peripheral interface, inter-integrated circuit, controller area network*.

Examples of standard protocols are *Serial Peripheral Interface (SPI)*, *Inter-Integrated Circuit (I2C)*, *Controller Area Network (CAN)*. In order to use a communication protocol, interfacing circuitry needs to be implemented both at the *central* and at the *satellite ends*. Such circuits can either be already integrated into an embedded system – if the implants include microcontrollers or microprocessors managing the communication interface – or implemented with standard Programmable Logic Devices (PLD), e.g. Field Programmable Gate Arrays (FPGAs), with additionally passive components when required.

Although embedded systems and PLDs with standard protocols present flexibility and rather low design complexity, they are not the preferred solution when considering inter-module connectivity in networked implant systems, due to their size and power consumption, critical parameters for subcutaneous devices. What is chosen in such systems is having both a customised protocol – optimised for the given function and adapted to the employed communication channel – and an Application-Specific Integrated Circuit (ASIC) [68]. This allows for a smaller interface size at both ends, lower power consumption per unit area, and circuit optimisation for the signal amplitudes and frequencies in use [71].

However, custom protocols usually present further challenges with regard to synchronisation and data recovery. Since satellite implants don't usually include a crystal oscillator due to space/size limitations, appropriate *clock recovery* and *data recovery circuits* must be implemented at the SI end. These will both generate the local clock signal employed by the digital circuits (digital controller and data conversion) and retrieve the information encoded in the

signal sent by the central implant. *Phase-Locked Loops (PLL)* are typically employed to recover an input signal and generate a local signal with a stable frequency at multiples of the input signal frequency [72]. These have been widely used in many fields, e.g. in telecommunications for demodulation of frequency modulated (FM) signals and in microprocessors for digital synchronisation and clock multipliers [73].

In order to implement a closed-loop implant system that senses, monitors, and stimulates neural activity, a bidirectional communication scheme is required [74]. This is due to the requirement for both data commands to be sent from CI to SI and neural recorded data sent from SI to CI. As discussed earlier, in a multi-module configuration the central implant (*master*) needs to provide also the power to the satellite implants (*slaves*). This has led to the creation of architectures allowing for a superposition of the forward data link (CI-to-SI) with the power carrier [54]. This limits the selection of the modulation schemes, given that by superimposing the always-on power carrier there is a need for constant power flow in the forward link.

Such requirement determines *phase* or *frequency shift keying modulation* as preferred modulations schemes, rather than amplitude modulation – with the drawback of increased complexity and power consumption due to the on-chip clock and carrier synchronisation [75].

2.3.3 System Reliability and Safety

By definition, implantable neural systems are placed inside the human body, hence surrounded by biological tissue. This is rich in water and salt, which can cause material corrosion and degradation, leading to device failure. Since the devices are active, thus host electronic circuits, it is crucial to ensure there is a barrier between such electronic components and the body environment [76]. Moreover, besides these potential reactions at the interface between the implants' outer materials and the body, also electrical and mechanical interactions can cause risk both for the AIMDs and the body itself. For these reasons, careful considerations must be made on the reliability of the devices implanted in the body and the safety of the patient.

The leads connecting the different modules and its endings (connectors) in wireline implant

systems are among the most vulnerable elements. They must be robust to mechanical stress and other external agents that can expose the wires to direct contact with the tissue, thus creating a path for electrical signals into the body. Details of the implantable cables characteristics and their connections with the modules are scarce in the limited literature on multi-module implants. However, more information can be found with regards to implantable leads used in classical single-module AIMDs to stimulate and record [77]. Such cables have in fact similar requirements to the ones connecting multiple implant modules, e.g. lead biocompatibility, wires isolation, low conductor resistivity, etc. On the other hand, they have a different core function, as in MMNIs the implantable leads are utilised for transferring power and digital data signal. Therefore, additional requirements are resistance to electromagnetic interference (EMI), low capacitive and inductive coupling between different wires and between wires and body.

Standard connectors for the Implantable Pulse Generators (IPG) industry exist, e.g. for cardiac pacemakers and Implantable Cardiac Defibrillators (ICDs). Established standards are IS-1, IS-4 (i.e. low energy) and DF-1, DF-4 (i.e. high energy) [78]. These can be employed for connecting to larger central implants – e.g. >20 cc – located in the chest or the abdomen, nonetheless, they are not preferred for interfacing with miniaturised satellite implants located in the brain or in other space-limiting locations. Miniaturised, non-standard custom connectors are generally developed for physical connection for the conductors at the SI end, creating an interface optimised and embodied into the implant itself. More recently, an important step for practical implementation of MMNIs has been the development of detachable systems and extension leads. These have allowed standard implantable extension cables stretching along the body while giving the possibility for ‘front-end’ custom cables – directly connected to the satellite modules – to have low-profile shape/dimensions and high-performance materials, and to be encapsulated within the implant module itself. Such an approach gives clear advantages for the surgical procedure and for module replacements to be performed locally, without removing the complete system.

Another important aspect is the front-end current exchange between the devices and the body. Both during the recording function and the stimulation function, there is an electrical current exchange between the sensing/stimulating electrodes and the biological tissue. Although this

is unavoidable by design, systems to monitor such current – and make sure it remains within the expected safety limits – should be put in place. For MMNIs, every module has a ‘reference’ electrical potential, *ground*. All signals within each device are established in reference to their local ground. How each ground signal is generated and how they are referenced to each other will have an effect on the electrical fields present in the implant system, hence on its reliability. It is, therefore, crucial to design an interfacing system that maintains the charge balance overtime to avoid DC charging 1) among conductors within the cables and 2) among power and ground voltage levels on different modules. This is to preclude undesired current paths from being formed if damage to the insulation occurs. Packaging and encapsulation failure may lead to electrochemical damage of the biological tissue, with life-threatening consequences [79].

Finally, the digital communication channel used to transfer signals between the modules and the front-end sensing/recording circuits are sensitive to interference to external electromagnetic fields and to different sources of artifact and noise. Excessive interference may both affect the quality of the recording signals and cause signal integrity issues and data corruption, thus compromising performance and functionality.

2.4 Multi-Module Neural Implants for Epilepsy

As introduced in the previous section, *Epilepsy* is a neurological condition affecting more than 50 million people worldwide and 1 over 100 people in the UK alone. The epileptic seizure, or fit, is an abnormal oscillation of the nervous system which significantly alters normal daily activities such as movements, sensations, awareness, and behavior, causing a devastating effect on patients’ quality of life [80]. Fortunately, most cases respond to drugs, but when antiepileptic medications are not helpful – in 30-40% of cases – it may be necessary to surgically remove the small ‘focus’ of the brain where the excessive activity is localised. This possibility, however, is not suitable for all the patients and can damage cognitive functions.

Treatment modalities based on neuromodulation techniques have shown to be alternative solutions. The VNS therapy previously presented was approved in 1997 by the United States

Food and Drug Administration (FDA) for reducing seizure frequency in patients suffering from refractory epilepsy. Over 80,000 patients have received treatment with VNS with good efficacy [81]. However, only half of the implanted patients have achieved a $\geq 50\%$ reduction in seizures after 2 years of treatment and complete seizure freedom is rare [82]. DBS-for-ANT from Medtronic and RNS from NeuroPace have proven to be more effective than indirect methods in many cases, as the electrodes' close proximity to the brain allows for more targeted stimulation. Moreover, the closed-loop capabilities of the responsive neurostimulation therapy boost an adaptive method that can detect and predict seizure development. Current medical devices based on single-module implant systems have many limitations, as previously mentioned, e.g. bulky implant units, noise-sensitive recording, and outdated stimulation techniques. These have incentivised the creation of novel MMNIs for the treatment of refractory epilepsy.

An example of such new systems and of an ambitious academic effort is the CANDO project. *CANDO (Controlling Abnormal Network Dynamics using Optogenetics)* is a world class multi-site cross-disciplinary project to develop an active implantable medical device for optogenetic neural control [83] [84]. This ongoing Innovative Engineering for Health Award arises from a collaboration of engineers, neuroscientists, and clinicians from Imperial College London, University College London, and Newcastle University. The goal is to create a first-in-man trial of the device in patients with focal epilepsy who present resistance to pharmaceutical drugs and are not suitable for neurosurgery.

The proposed treatment aims to use a multi-probe cortical implant to modulate abnormal activity in the brain cortex, so preventing seizure development. This is achieved by continuously monitoring brain waves via implanted electrodes and altering them by providing precisely timed stimulation through light sources. As shown in Figure 2.14, besides the miniaturised brain implant with multiple satellite modules (*optroelectrodes* or *optrodes*), the system includes a chest implant, responsible for high-level control and for housing the power source. The CANDO project and its clinical application – refractory focal epilepsy – will be thoroughly discussed in the next chapter.

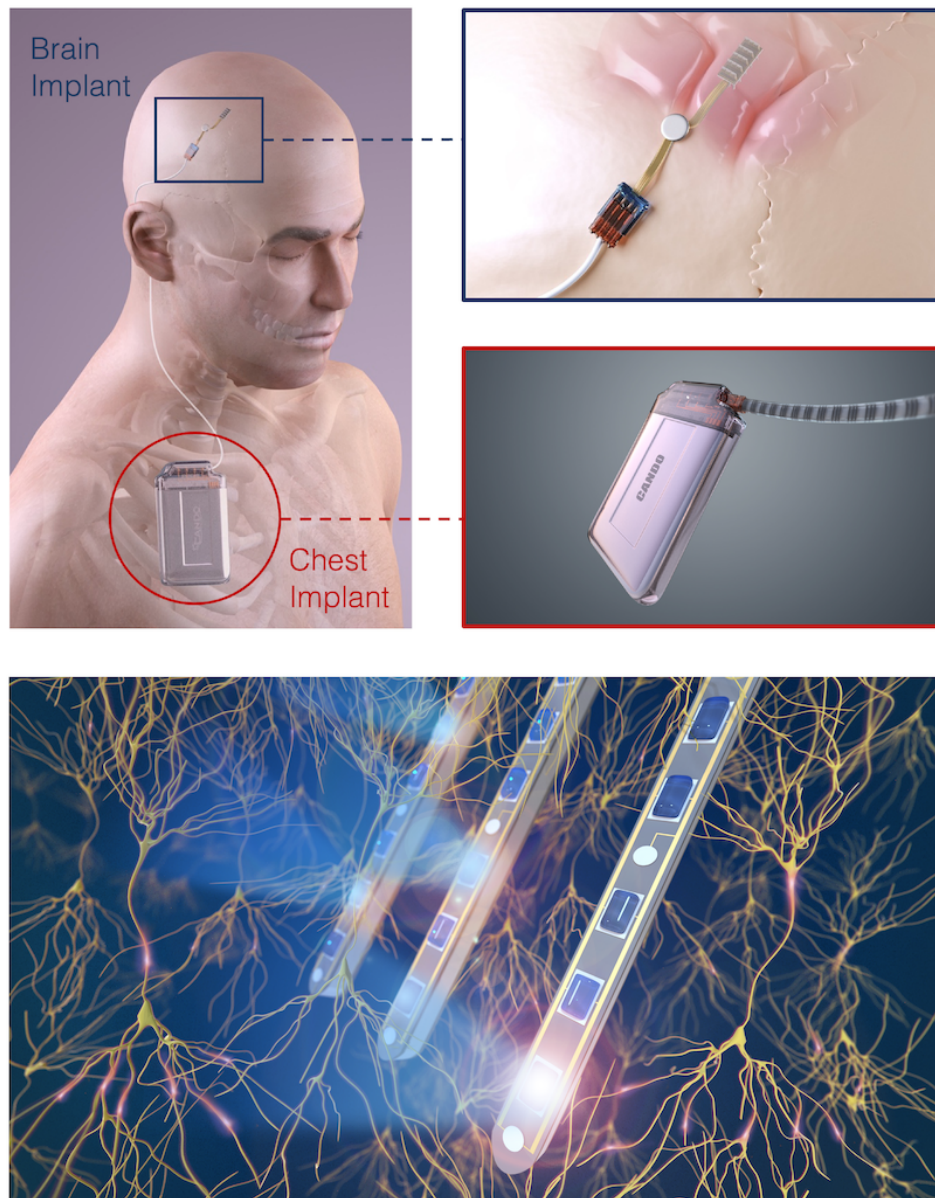


Figure 2.14: (Top) illustration of the CANDO implant system concept: (1) a brain implant placed under the skull, in contact with the cortex; (2) a chest implant placed subcutaneously in the chest/abdomen area and connecting to the brain implant through a cable. (Bottom) Conceptual representation of the optogenetic stimulation provided with implantable LEDs attached to the modules at the brain implant.

Chapter 3

CANDO: Controlling Abnormal Network Dynamics using Optogenetics

Our research group from the Centre for Bio-inspired Technology of the Imperial College London is part of the CANDO team and the research objectives we are responsible for in the project involve the design, implementation, test, and documentation of the microelectronics development. This includes (1) the front-end *recording* system, (2) the on-chip *control* hardware, (3) the wired subcutaneous *data and power communication* system.

The work presented within this Ph.D. thesis was developed as part of the CANDO project. This Chapter is dedicated entirely to the description of the project, starting with an introduction to epilepsy – the targeted neurological condition – continuing with the CANDO approach to creating a solution for treating such condition, and concluding with the research questions and challenges associated with developing a medically applicable implant system based on 3 core features: (1) a revolutionary technique – *optogenetics*; (2) a novel adaptive method – *closed-loop algorithm*; and (3) an innovative implantable system – *multi-module neural implants*.

The Chapter then concludes with an outline of the requirements of the proposed medical device, its functions, and capabilities.



Figure 3.1: Illustrative concept of Epilepsy. 1 in 100 people worldwide suffer from Epilepsy [80].

3.1 The Goal: Treating Focal Epilepsy

The word **Epilepsy** is derived from the Greek word *epilambanein* and means “to be seized”. This was used to connote both the disease and the single attack [85]. The illness has been long viewed as evidence of the connection between human and spiritual realms. Reference to epilepsy can be found throughout the ages, in different parts of the world, and in different cultures. Epilepsy was medically defined in 2005 as “*a disorder of the brain characterised by an enduring predisposition to generate epileptic seizures*” and the **seizure** as “*a transient occurrence of signs and/or symptoms due to abnormal excessive or synchronous neuronal activity in the brain*” [86]. In operational/practical terms, the definition of epilepsy has been applied as having two unprovoked seizures >24 h apart. It was eventually changed to a more detailed one by the International League Against Epilepsy (ILAE) for purposes of clinical diagnosis and in accordance with how epileptologists think about epilepsy [87]. The new definition includes also special circumstances that don’t require more than one unprovoked seizure [80]. A task force was put in charge for this and it proposed epilepsy to be considered as a disease of the brain defined

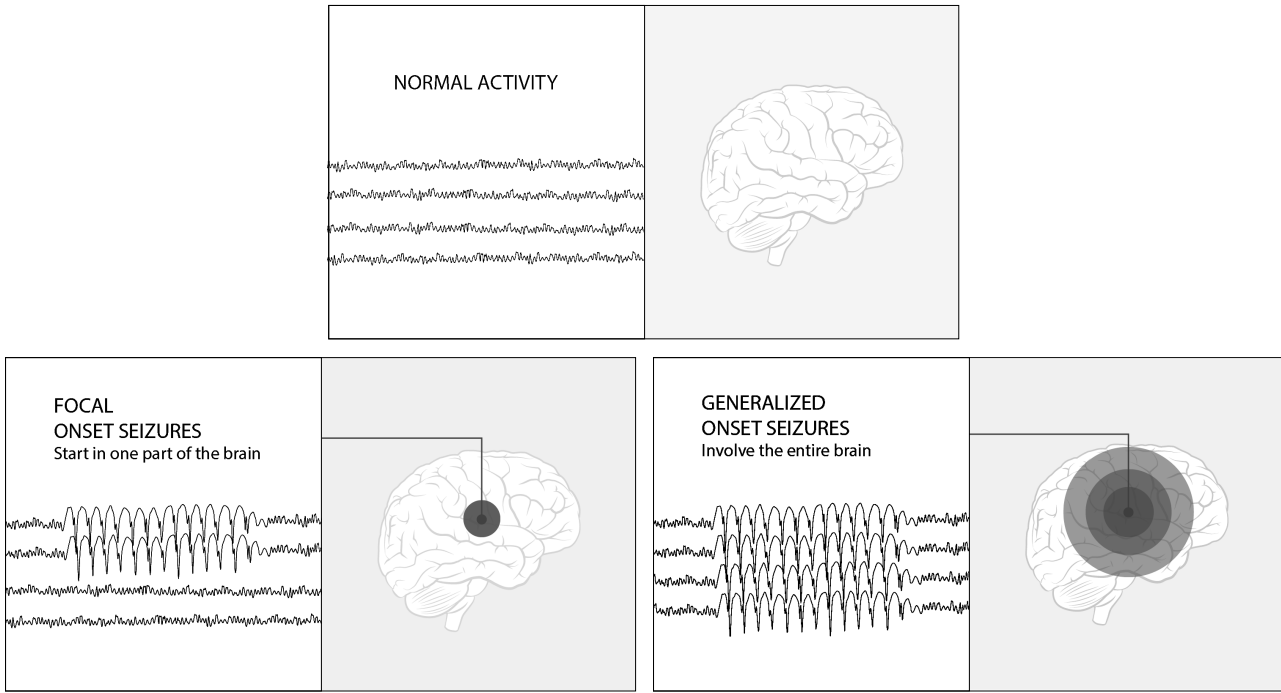


Figure 3.2: Illustration comparing the brain activity of the two main types of epilepsy – focal and generalised – and the brain normal activity. Adapted from [90]

by any of the following conditions: (1) at least two unprovoked (or reflex) seizures occurring >24h apart; (2) one unprovoked (or reflex) seizure and a probability of further seizures similar to the general recurrence risk (at least 60 %) after two unprovoked seizures, occurring over the next 10 years; (3) diagnosis of an epilepsy syndrome. In 2015, ILEA created also a revised classification for different types of epilepsy. This classification is not based on fundamental mechanisms of the disease and anatomy as done before, but rather on the origin of the seizures in the brain [88]. The three main categories are *focal onset*, *generalised onset*, and *unknown onset*, with subgroups related to motor and non-motor symptoms at the onset and to retained or impaired awareness for focal epilepsy [89]. Figure 3.2, Figure 3.3, and Figure 3.4 give more details on these categories.

3.1.1 The Burden of Epilepsy

Although updated definitions and classifications have helped to better understand Epilepsy, this disease is still one of the most misunderstood. Myths regarding Epilepsy have historically created widely spread misconceptions and stigma, with people still today incorrectly believing

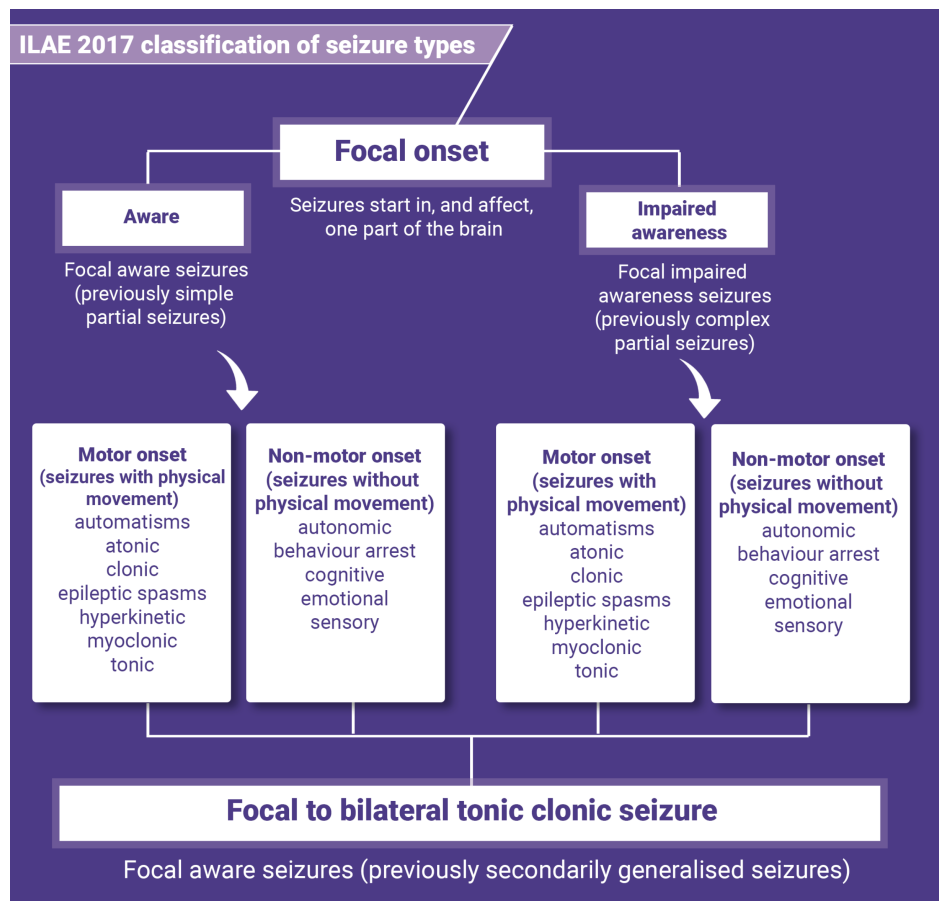


Figure 3.3: Block diagram and description of the updated seizure classification/type by ILAE in 2017 – **focal onset epilepsy** [91]. Figure from [92].

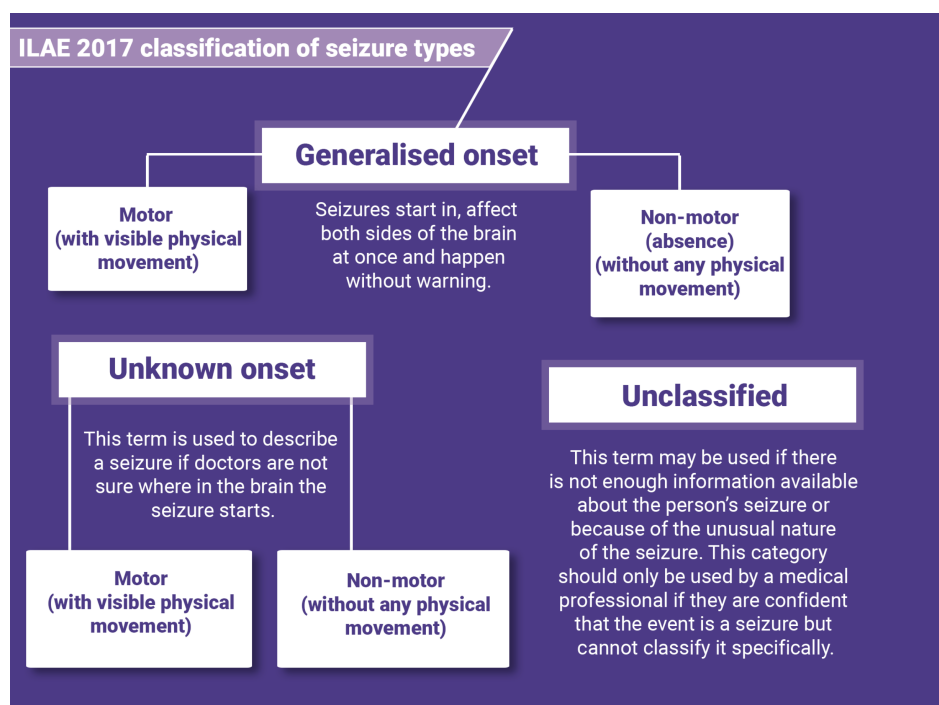


Figure 3.4: Block diagram and description of the updated seizure classification/type by ILAE in 2017 – **generalised onset epilepsy** [91]. Figure from [92].

it is a contagious disease or that epileptic patients are possessed by spirits. This has created fear and discrimination towards people suffering from epilepsy and their families for many centuries, even though it is a very common disorder, especially in low- and middle-income countries – 80% of people with epilepsy live in these countries [93]. Epilepsy is not just a single condition, but a group of conditions that have in common brain seizure development, as described earlier. Although the underlying medical mechanisms that lead to Epilepsy are often identified and understood, in half of the cases the cause of the disease is still unknown. These can be genetic syndromes and conditions, brain tumors, infections of the brain tissue from parasites, injuries to the head, lack of oxygenation of the brain caused by stroke, by prenatal or perinatal causes [94]. As these are not related only to a specific population age, Epilepsy can affect every person, at any time of their life. Moreover, despite having in common the epileptic seizure as an underlying symptom, patients experience different manifestations of the seizure, depending on its localisation and development. In summary, epilepsy designates a vast range of heterogeneous disorders of the nervous system that differ with respect to etiology and symptomatology.

Thanks to anti-seizure medications, epilepsy disorders can be controlled, more than 2/3 of patients can be potentially treated and become seizure-free, with affordable treatments. This, however, doesn't translate to the global number of epileptic patients who use medications and are seizure-free, as 70% of people suffering from this condition don't actually have access to treatment, even though these can be produced at a low cost. Such a significant difference is because of unavailability of antiepileptic medicines and of training for healthcare providers in resource-poor settings, thus widening the so-called *Epilepsy treatment gap* [95]. Important steps forward reducing this gap are being made, especially aiming at raising awareness and providing better information on epilepsy and on its impact on patients and society. The World Health Organization, together with the International League Against Epilepsy (ILAE) and the International Bureau for Epilepsy (IBE), has led the Global Campaign Against Epilepsy to bring the disease "Out of the Shadows" [96] [95].

Beside social and humanitarian efforts, the scientific and research communities continue to give their contribution to better understanding epilepsy, both from neurological and neuroscience

perspectives. Recent research has shown that epileptic seizure is related to abnormal network dynamics within the brain, thus defining epilepsy as a network disease, and not only a symptom of the local excessive activity [89]. The process of developing epilepsy, thus of converting a non-epileptic brain into one that can generate seizures, is called *epileptogenesis*. This is often described as the result of an *imbalance between excitatory and inhibitory neural activity within the cortical networks*, causing excessive oscillation. The imbalance generating such oscillations is in most of the cases due to a high activity level of the excitatory neurons compared to the inhibitory neurons, although there are circumstances where the abnormal inhibition can be epileptogenic [97]. These abnormally low or high levels of oscillatory synchrony are able to disrupt not only the neuronal activity within the local area in the cortex they generated from but also the activity of other neurons in the network, altering the wider network dynamics [98].

3.1.2 Drug-Resistant Epilepsy

Although drugs have shown to be helpful and effective in most cases, for 1 in 3 epileptic patients seizures neither reduce their length nor their occurrence when using medicines. Drug-resistant epilepsy (DRE), also known as intractable epilepsy or refractory epilepsy, is defined as the failure of at least two anti-seizure drugs [99]. In these cases, patients have frequent and disabling seizures, limiting their ability to work and participate in activities [100]. Other non-pharmacologic options can be used to break the abnormal synchronization of epileptogenic neurons, bringing the network dynamic back to a normal state. As already discussed in the previous chapter, there are effective neurostimulation techniques that have been granted FDA approval for the clinical treatment of refractory epilepsy, e.g. established open-loop methods like vagus nerve stimulation and deep brain stimulation and adaptive methods such as the responsive neurostimulation. They have helped over 100,000 patients in the world living with epilepsy, being in many cases a life-changing solution.

To explain in simple terms how these intervene to suppress the epileptic seizure by breaking the network dynamics, the following analogy can be used: if we think of the *brain* as an *ocean*, we can consider the electrical brain activity as the waves of the ocean's water. When the neural

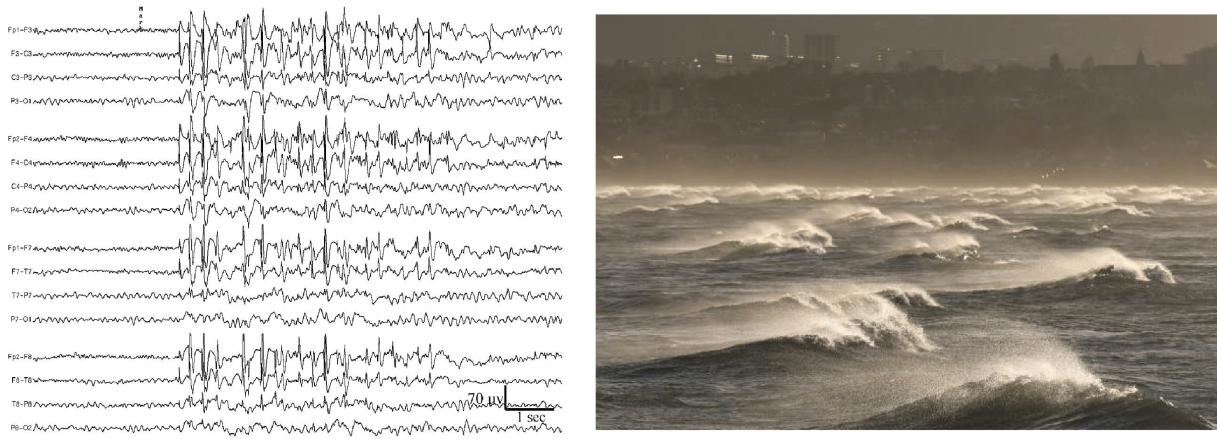


Figure 3.5: Conceptual analogy between electrical waves in the brain and water waves in the ocean. Excessive activity can provoke oscillations, thus waves.

activity is in a normal state, brain signals depend on inputs coming from the nerves delivering sensory information, and on outputs sent to the organs and muscles. Similarly, the ocean waves have a movement that depends on factors such as winds, atmospheric pressure, temperature, water currents/streams, incoming rivers, etc. An epileptic fit in the brain can be compared to a storm in the ocean. Waves go into an abnormal state, synchronizing with each other, thus increasing their amplitude and frequency. This could lead to excessive synchronization into solitary waves, such as tsunamis. The effects of epileptic seizures on people's lives are like the impact of the waves on the ocean coasts and on the organisms living in the water. The more frequent and taller waves are, the worse their impact is.

Open-loop therapy

When considering VNS therapy for drug-resistant epilepsy, periodic electrical stimulation is applied to the left vagus nerve, the longest nerve of the autonomic nervous system. It communicates both sensory and motor signals between the brain and organs of the human body. These signals are responsible for the parasympathetic control of the heart, lungs, and digestive system. Intermittent electrical stimulation of the vagus nerve was one of the first and most famous techniques to reduce seizure development in refractory epileptic patients. Using the analogy with the ocean – stimulating the vagus nerve to stop seizures corresponds to significantly altering the mass flow of one of the main rivers delivering water to the ocean, in order to stop

the abnormal waves caused by a storm. Such a method could in theory work as – if correctly modified at a regular pace – the water flowing through the river’s mouth can create obstructing waves. These could interfere with the abnormal wave progression created by the storm on the surface, thus breaking the excessive oscillations. However, there are many unknowns that play a key role: how much should the flow be changed? How often? Is it better to increase or decrease the flow? Where is the storm located relative to the mouth of the river? Moreover, important alterations of the river flow can translate into a negative impact on the river bed and to the ‘river-ocean’ water exchange ecosystem. Analogous challenges have to be faced and considerations to be made for VNS in epilepsy treatment. Since the vagus nerve activity is fundamental for many functions of the nervous system, an incorrect stimulation could cause side effects and undesired symptoms. Finally, the biological mechanisms causing the positive effects of VNS are still not fully understood, as it is an indirect neuromodulation method, i.e. the electrodes are not in contact with the brain tissue [101].

ANT-DBS is a technique that modulates activity by acting on network nodes located deep into the brain regions, rather than altering widespread brain networks acting on a peripheral nerve. Deep brain stimulation is a direct and more targeted method to control network dynamics, as the stimulating electrodes are placed in the anterior nucleus of the thalamus, where network nodes connected directly to the cortical areas can be found. Many studies have indicated that the anterior thalamic region is critical in maintaining and propagating epileptic seizures [102], thus a precise pulsed stimulation of these deep brain regions can break the network synchronization and bring the activity to a normal state [103]. As for the water analogy, it would be like placing water pumps deep into the water where ocean currents flow. The activity of surface waves, therefore, could be modified by altering periodically the flow of deep currents in order to limit and interfere with the creation of abnormal waves caused by a storm.

Although DBS targets directly the brain instead of the vagus nerve, it presents similar challenges and limitations to VNS [104]: they both intervene by stimulating network pathways to reach and disrupt the source of the seizure rather than directly intervening on the cortex. These pathways, if excessively disrupted with electrical stimulation, have primary functions that can induce side effects to affect sleep, mood, alertness, metabolism, etc. In addition, they are both

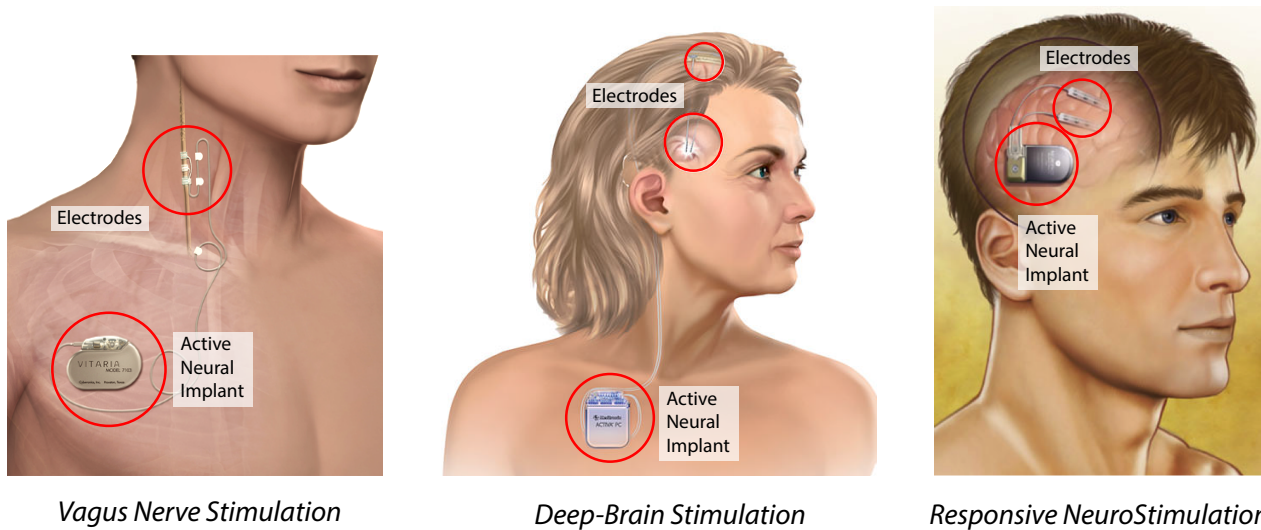


Figure 3.6: Implant concept comparison for the three main neurostimulation therapies for drug-resistant epilepsy: vns, dbs, rns.

open-loop solutions which don't monitor the activity of cortical areas where seizures generate, hence lacking seizure detection and prediction capabilities.

Closed-loop therapy

This limitation has been addressed by the RNS therapy, which includes a system that records neural activity to detect specific patterns of epileptogenic oscillations and triggers focal stimulation to interrupt the seizure [105]. The major differences of RNS with VNS and thalamic DBS treatments are: (1) RNS provides a closed-loop therapy that monitors abnormal electrographic activity and decides when to activate electrical stimulation; (2) both recording electrodes and stimulation electrodes can be placed on the surface of the cortex and/or deep in the internal structures; (3) it targets focal epilepsy with up to two foci localised in one brain hemisphere [106]. The ability to sense brain signals directly from the focus of the seizure allows both for real-time detection and intervention which limits the duration of the seizures and for a more accurate diagnosis in order to predict future seizures and reduce their frequency in the long term [107]. It is clear that by knowing precisely where a storm in the ocean forms and by detecting when it is about to start – analogous to where and when a focal seizure in the cortex generates – it would be much more effective to intervene: ways could be used to disrupt the formation of the waves and avoid their propagation and limit their damage.

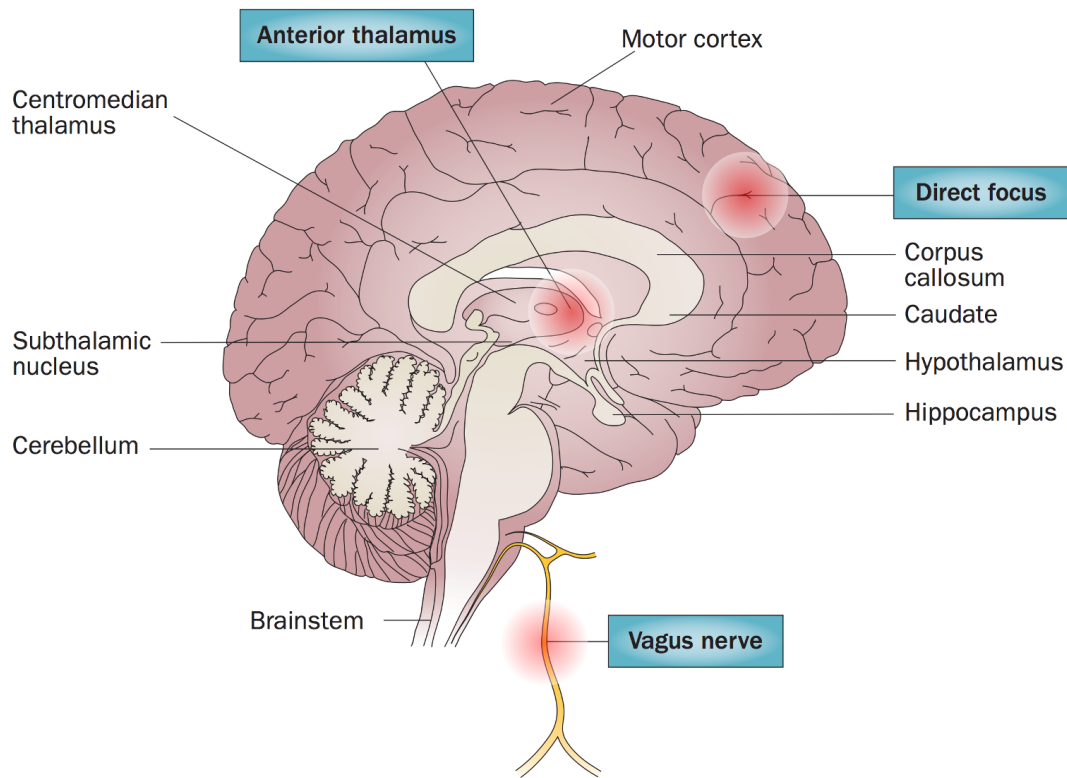


Figure 3.7: Illustration of the brain internal structures, with emphasis on the regions where VNS, ANT-DBS, and RNS intervene with their solution: vagus nerve, anterior nucleus of the thalamus, direct cortical focus.

The water analogies used so far are meant to help visualise the brain activity during an epileptic fit and the effect of the various solutions. It is important to highlight this is a very simplified view, as the complex structure of the brain and its activity are yet to be fully understood. Therefore, the reasons why some therapeutic mechanisms work instead of others are often not well known. For example, recent studies on RNS have surprised the epilepsy research community by showing – on a patient cohort of 11 people – that seizure reduction was not associated with the direct effects of real-time responsive stimulation events, but rather with indirect long-term effects. In these cases, the therapeutic outcomes of closed-loop stimulation seem to emerge from modulation of the seizure network over time rather than from the acute detection and interruption of individual seizure events [108].

Nonetheless, the advantages provided by the responsive neurostimulation therapy have encouraged the medical devices industry to add recording capabilities to their established neuromodulation therapies, paving the way for closed-loop techniques for treating DRE [109].

In the meantime, academic efforts in experimental and translational neuroscience, together with advances in implantable microelectronics, have given rise to ambitious research projects. They are developing neural microsystems for closed-loop control of normal and pathological network dynamics in the brain, such as epilepsy. Such systems started being developed first as research tools for in-vitro and in-vivo experiments in animal, e.g. mice and rats, to evaluate evoked behavioural response following electrical stimulation [110]. Examples of closed-loop methods for epilepsy suppression have presented systems that aim at detecting seizure occurrence with different closed-loop algorithms [111], including both analytical [22] and machine-learning-based classifiers [112]. These are often based on EEG and ECoG recording from rodents and not further pursued in larger animal models or humans [113] [23].

Precise activation and silencing of single neurons of specific types are required to study how large populations of neurons interact with each other in complex networks [114]. Although electrical stimulation remains the most reliable stimulation means for in-human medical use, it is neither directional nor selective for small families or specific types of neurons. Since the sensing function is based on the recording of electrical activity, significant interference from stimulating to the recording electrodes is intrinsically present in closed-loop systems. *Stimulation artifacts* from electrical current delivered to the tissue are always present [115]. This is one of the critical limitations of closed-loop systems and has led to the advent of new methods based on different neuromodulation means.

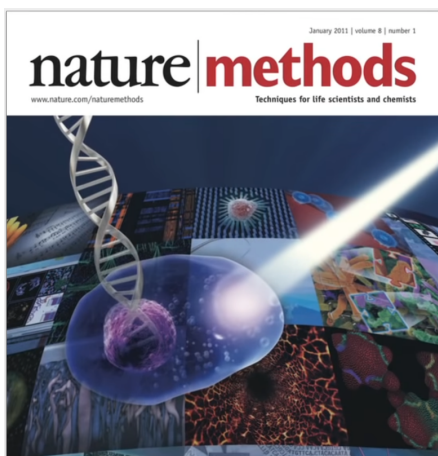
The clinical target of the CANDO project is to develop a novel therapy for drug-resistant focal epilepsy. The goal is to develop a closed-loop neurostimulation system based on the electrical recording of cortical activity and optical stimulation of the epileptogenic tissue. The approach relies on the revolutionary technique called Optogenetics.

3.2 The Approach: Closing the Loop with Optogenetics

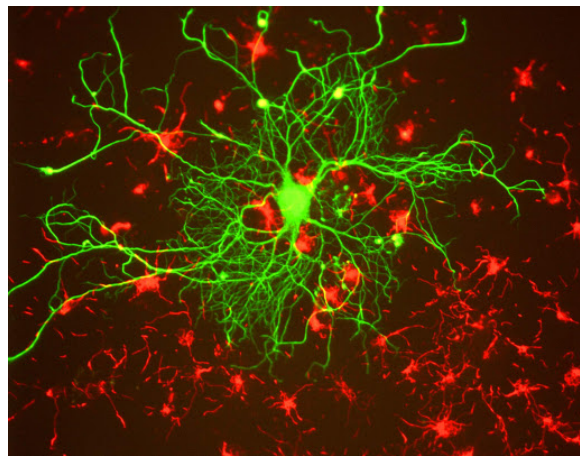
The breakthrough of **Optogenetics**, which has enlightened new landscapes for the study of biology both in health and disease, has provided a new means to actively communicate with the nervous system: **light**.

Optogenetics received the ‘Method of the Year 2010’ award by the journal Nature Methods. This technique gives the possibility to control the electrical behaviour of individual nerve cells with optical stimulation. It exploits genetically encoded light-sensitive proteins, which can be naturally occurring or chemically modified, to target specific populations of neurons and turn them into light-sensitive cells by altering their genetic structure. The gene that encodes the protein is carried by a safe virus that infects the neural tissue and delivers the gene itself. Only a chosen subset of the neurons has the right characteristics to decode and express the protein. Different light wavelengths can activate different proteins, responsible for excitation or inhibition of the cells (Fig.3.10). When optical stimulation is provided to the infected cells, the illuminated neurons can be turned on or off depending on the colour of the light [83].

In recent years, optogenetics has become a fast-expanding field thanks to several technological developments, both in biology – such as gene therapy and gene expression – and in engineering, such as light-delivery technologies and techniques to readout the biological effects introduced



(a)



(b)

Figure 3.8: Optogenetics in two pictures: (a) cover of the journal Nature Methods with optogenetics as “Method of the Year 2010”; (b) picture of a genetically modified neuron for optogenetic activation.

by optogenetics [116]. Early studies have shown the potential of this method for retinitis pigmentosa – a neurodegenerative eye disease where the loss of photoreceptors can lead to complete blindness – to restore vision by addressing limitations of current neural interfaces (based on electrical stimuli) with direct illumination of genetically modified retinal ganglion cells in the eye [117]. Despite promising results from successful animal trials performed by many research groups and prestigious institutes, optogenetics has been for many years considered mainly as a groundbreaking tool for neuroscience research, rather than a paradigm shift for medical devices. Nevertheless, key milestones have been achieved in the past decade to prepare such technology for in-human use. A pivotal one was accomplished in 2016 in the field of sight restoration from a medical company, RetroSense Therapeutics, developing gene therapy applications for optogenetics: the first human patient was successfully injected in the eye with a virus encoding a light-sensitive protein: Channelrhodopsin-2 [118]. Soon after, GenSight Biologics – a European company based in Paris, France – enrolled one subject in a first-in-man clinical trial combining gene therapy and optogenetics for the treatment of Retinitis Pigmentosa. This has led to the first successful clinical application of optogenetics in human, which was published in *Nature Medicine* in May 2021 [119]. A blind patient suffering from retinitis pigmentosa was injected in the eye with an adeno-addiciated viral vector encoding an opsin (light-sensitive) protein: ChrimsonR. A wearable pair of goggles captures images from the visual world pixel by pixel using an event-based camera, transforms the events into monochromatic images, and projects them in real-time as local 595-nm light pulses onto the retina. By using these goggles, the patient was able to perceive and locate various objects, demonstrating the effectiveness of the therapy. This is an important leap forward for the field, as it's the first reported case of partial functional recovery in a neurodegenerative disease after (and thanks to) optogenetic therapy.

As it is located within the eye, thus not covered by skin or bone, the retina is the only part of the nervous system that is exposed to direct light. This makes it more accessible for optogenetic treatment, since wearable devices can be used to generate the light to activate the genetically-modified cells and apply it directly to the eye. Nonetheless, optogenetics has the potential to be employed in other parts of the nervous system, e.g. the brain. Invasive neurotechnologies

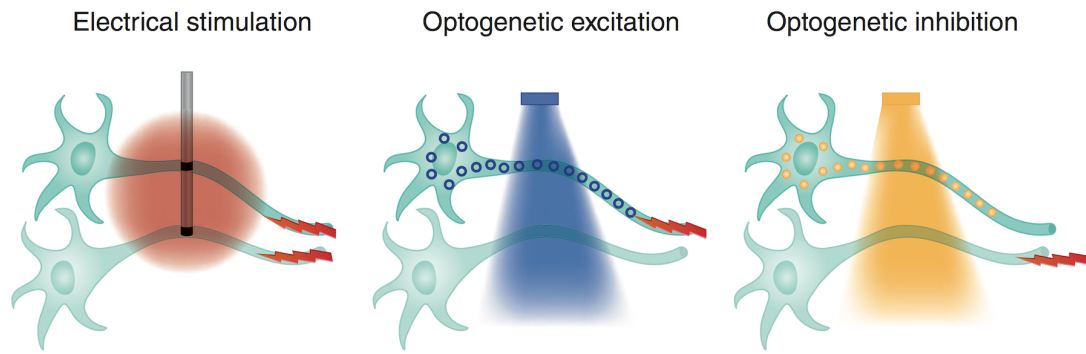


Figure 3.9: Comparison between electrical stimulation and optogenetic excitation and inhibition. Targeted excitation (blue light-activated channelrhodopsin) or inhibition (yellow light-activated halorhodopsin), conferring cellular specificity while maintaining high temporal precision [83].

for the brain have demonstrated capabilities to effectively interact with nervous system activity through electrical recording and stimulation. The advent of optogenetics has pushed the limits of electrical stimulation, as individual cells or circuits can be targeted with exact timing. Besides cell specificity, optogenetics allows also for spatial selectivity because light can be focused with much more accuracy compared to electromagnetic fields. Since light does not interfere with concurrent electrical recordings, this technique enables real-time, continuous closed-loop control of neural activity, without having to deal with direct coupling between electrical stimulation and recording – stimulation artifacts. For these reasons, there has been rapid rise in the number of publications on optogenetics, which has become a widespread research subject not only in neuroscience but also in neurotechnology and engineering. Indeed, in the past decade, implantable neural probes including light sources have been developed by various research groups [114] [120]. Optogenetic neural implants aim to become an effective solution for various medical applications, by combining (1) a powerful toolkit based on genetic and optical methods with (2) modern, high-channel count neural microsystems. Retinal prostheses for the blind are the first clinical success, other therapies requiring closed-loop treatments for the brain, e.g. for drug-resistant epilepsy, can also benefit from this technology. To the best of the author’s knowledge, there are no ongoing clinical trials with optogenetics for the brain. Yet, several research projects are developing implantable systems proposing applications in human. CANDO is among them – its goal is to create a first-in-human clinical trial of a medical device treating patients with focal epilepsy who present resistance to pharmaceutical drugs and are not suitable for neurosurgery.

3.2.1 An Innovative Academic Endeavour

The CAND0 project multidisciplinary team is divided in three *Work Packages*, which in turn are divided into smaller teams. These are working to meet the technical challenges of developing an optogenetic implantable system and to enable such medical device to detect abnormal network dynamics and prevent this activity from progressing to a seizure. The novelty of the approach used in CAND0 relies on the combination of three core techniques: (1) optogenetics for light activation of neurons in the brain cortex; (2) closed-loop control of network dynamics associated with focal epilepsy; (3) distributed implant system based on multi-module active neural implants.

Making neurons in the human brain sensitive to light

The only cells of the human body where opsins naturally occur are in the retina. Therefore, to use opsins to treat epilepsy in the brain, we need a way to introduce them safely in the specific neurons that are targeted, as these don't respond to light spontaneously. We now know that gene therapy has the ability to deliver such proteins and allow neurons in the cortex to be turned on and off with optical stimulation.

– *But how is optogenetics achieved for cells in the human brain?*

First of all, an appropriate type of opsin needs to be identified and chosen depending on the function that is required. Widely employed opsins for optogenetics belong to the family of Rhodopsins. Examples are channelrhodopsins, which act as ion channels that open in response to light, permitting the flow of ions across the neuron membrane along their electrochemical gradient. In other words, it allows the cell to be *turned on* with light. Differently, bacteriorhodopsins and halorhodopsins act as ion pumps, where absorption of a photon provides the energy to move a number of ions across the cell membrane against their electrochemical gradient, therefore, neurons can be *turned off* with light.

The first application of these opsins to neuroscience came in 2004 when researchers incorporated channelrhodopsins into mammalian neurons [121]. This was shortly followed up by a

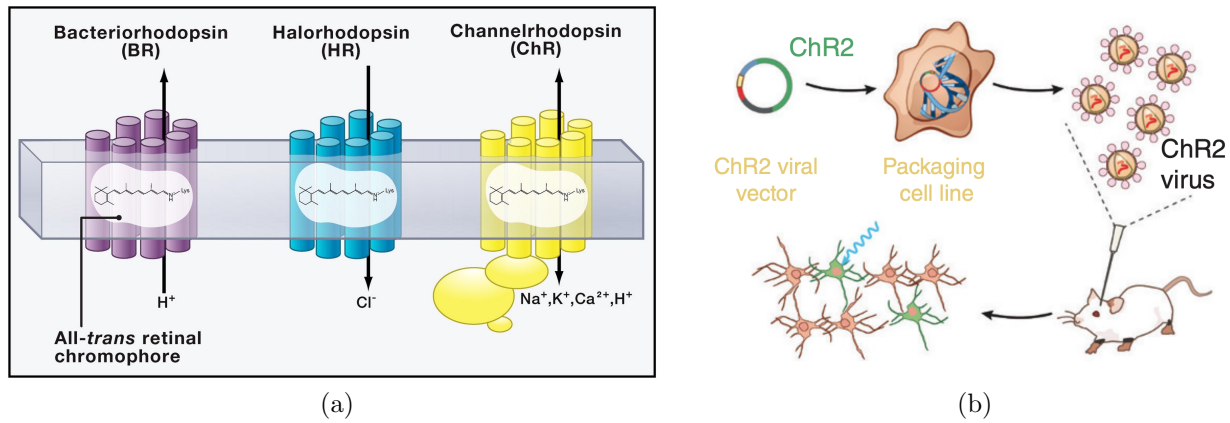


Figure 3.10: (a) Examples of the main Rhodopsins used in optogenetic therapies: bacteriorhodopsin; halorhodopsin; channelrhodopsin [122]. (b) Optogenetic viral vector and injection into animal models [83].

demonstration of the use of halorhodopsin [122]. This opsin pumps one chloride ion into the cell for each photon it absorbs. The result is a hyperpolarising current that acts to inhibit the neuron and prevent spiking activity. This is important for epilepsy as it is characterised by the over-activity of various neural circuits. The ability to inhibit neurons optically, along with the ability to target this inhibition to specific cell types, has therefore led to a range of investigations into the control of epilepsy [123].

The second step in the optogenetic therapy development is to get the target cells to manufacture and express these opsins in their cell membrane. As early as 1966, scientists identified that viruses possessed properties that could be useful in delivering genes into cells [124]. A virus is a small infectious agent that requires another living cell to replicate. Viruses enter cells and instruct the cell's own machinery to make new copies of itself, causing the infection to spread. By contrast, the modified viral vector in gene therapy makes copies of useful proteins like opsins. It does this by introducing a new piece of genetic code into the cell, which contains the instructions for making the opsin. Importantly, this code does not contain instructions for making more virus copies, and therefore the viral vector is not infectious and cannot spread. Together with the desired gene, the virus includes also a promoter. This is a small piece of genetic code that lets the host cell know there is a gene that can be translated into a protein and starts this process. Different types of cells will translate genes following specific promoters. As a result, even if different types of cells are infected, by selecting the right promoter sequence

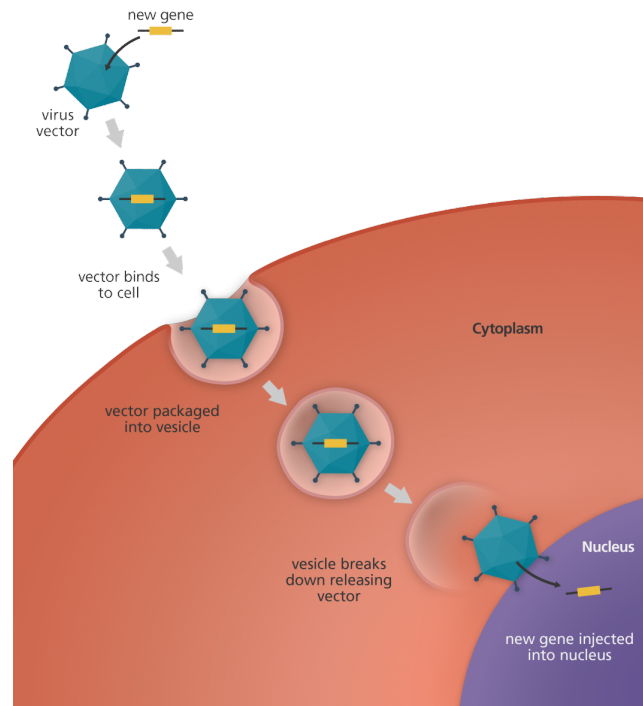


Figure 3.11: Visual representation of steps of a viral vector delivery. Credit: Genome Research Limited

only a specific cell type will ultimately manufacture and express the inserted gene. This makes optogenetics a highly selective technique for targeting specific cell types.

As discussed earlier, optogenetic gene therapies are already being trialed in humans, delivered to the eye as a potential treatment for blindness. However, before any optogenetic therapy is tested in the human brain, it is essential to prove that the viral vector and opsin proteins are not harmful. The *CANDO optogenetics team* focuses on identifying both the most suitable opsin for the clinical application selected and the viral vector to deliver the opsin. This involves the design of a safe and effective gene therapy and experiments in-vitro (human cortex slices) and in-vivo (in animal models) to validate the proposed therapy.

Developing a closed-loop algorithm to suppress seizures development

Since optogenetics allows for stimulation of neurons – activation or inhibition – without preventing simultaneous electrical recording, the light stimuli can be continuously modulated in response to real-time brain signal activity, creating a closed-loop interaction with local net-

works. This means that, besides the presence of a system able to monitor electrical signals and generate and drive pulses of light, also a closed-loop algorithm is needed. To provide an effective treatment for focal epilepsy, such an algorithm should be able to identify an abnormal oscillation in the area of interest, thus detect the start of a seizure, and activate the stimulation with specific timing and intensity to break the oscillatory behaviour and bring the network back to a normal state.

– *But how is the algorithm defined and how are the simulation parameters chosen?*

Optogenetic closed-loop systems have been attempted in the past for control of epileptic activity, using concurrent recording and optical stimulations in animal models. However, these rely upon real-time recording and detection of the seizure, followed by an “on-off” open-loop optical stimulation to stop the pathological activity [125] [126]. Although in control theory these are defined also as closed-loop systems, since the control signal (optical stimulation) depends on the measured output signal (brain activity), what is hereby intended as a *closed-loop* is the ability to change in time the amplitude of the control signal depending on the feedback from the output signal. In other words, modify the intensity of the light stimuli – thus the activation or inhibition of the neurons – depending on the amplitude of the electrical activity measured from the neuron population.

In neuroscience, it is generally acknowledged that “*all nervous processes of any complexity are dependent upon the interaction of excitatory and inhibitory cells*” [127]. A localised neural population is therefore considered as composed of an excitatory subpopulation and an inhibitory subpopulation. *Excitatory neurons* are cells that release neurotransmitters that have excitatory effects on the connected neurons, e.g. glutamate. This means the latter will have increased likelihood to fire an action potential in response. In contrast, *inhibitory neurons* release neurotransmitters that have inhibitory effects/ e.g. GABA, as they decrease the likelihood that the connected neurons will fire an action potential. In published reports on optogenetic control, epileptic activity has been usually controlled either by ‘turning off’ excitatory neurons, which are genetically modified to express inhibitory opsins (e.g. halorhodopsin) [128] [129], or by “turning on” inhibitory neurons, which are genetically modified to express excitatory opsins

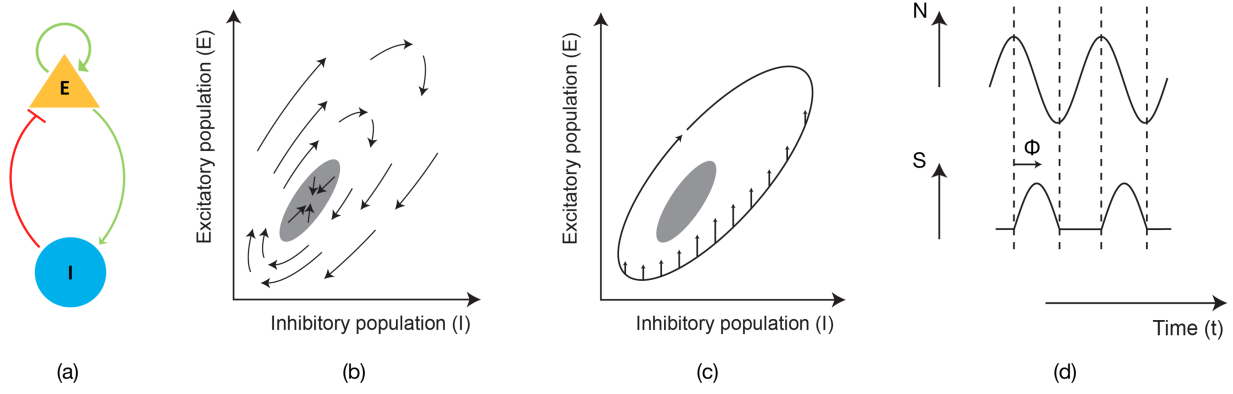


Figure 3.12: Simplified Wilson-Cowan model for excitatory $E(t)$ and inhibitory $I(t)$ neurons and graphical representation of the closed-loop algorithm. Courtesy of Professor Andrew Jackson.

(e.g. channelrhodopsin) [125]. It is reasonable to assume that, to suppress excessive network activity from epileptogenic neuron populations, it is sufficient to stop the activity of excitatory neurons or increase the activity of inhibitory ones. The approach taken by the CANDO team, on the contrary, is to explore the possibility of controlling epileptic activity by stimulating excitatory neurons that express excitatory opsins – increasing the neuron activity instead of decreasing it.

Although this may sound counter-intuitive, the hypothesis is based on the Wilson-Cowan neural mass model that has previously been applied to epileptic activity [130] [131]. The model comprises two interconnected neural subpopulations – excitatory $E(t)$ and inhibitory $I(t)$ – whose activity is represented in two-dimensional phase space, as shown in Figure 3.12.a. The instantaneous state evolves through time according to nonlinear dynamics, which divide the phase space into two regimes (Figure 3.12.b). Derived from control theory approaches, the core assumption is that by altering the timing of stimulation relative to the ongoing neural activity, differential effects could be influenced on the local networks, thus adding a new temporal dimension to the control of neural dynamics [132]. Considering the “ $E(t), I(t)$ ” model, this would translate to increased activity of the $E(t)$ neurons that will increase also the activity of the $I(t)$ neurons, which in turn will inhibit $E(t)$, ultimately pushing the state space trajectory towards a stable regime, as illustrated in Figure 3.12.c. The proposed closed-loop algorithm is implemented as follows:

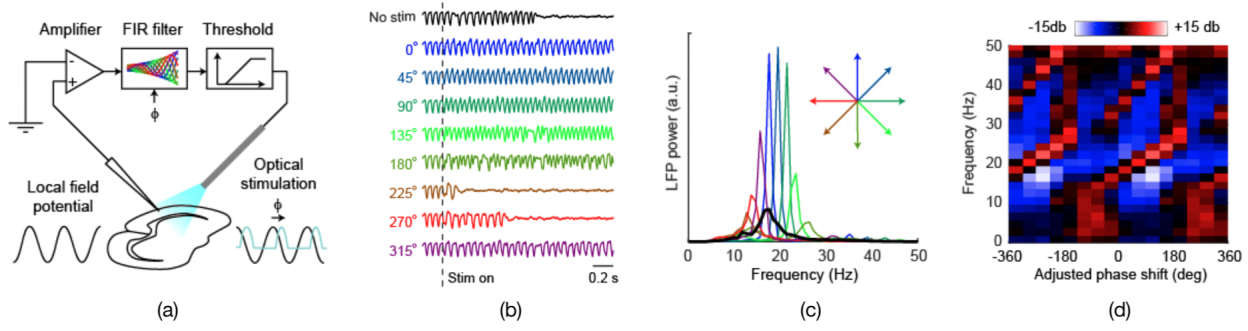


Figure 3.13: Closed-loop algorithm representation: (a) schematic of the experimental setup, with LFPs recorded from a mouse brain slice, filtered and used to control optical stimulation in real-time; (b) simulated seizure bursts with 8 different phase-shifts; modulation of LFP power relative to no stimulation: (c) LFP power vs frequency graph with 8 different phase shifts; (d) red-blue heat-map for visualization of stimulation effect on LFP power. Figure adapted from [132]).

1. The electrical activity of the neurons is monitored in real-time – biopotential recording
$$N(t) = f[E(t), I(t)];$$
2. The recorded signal is amplified and filtered – band-pass finite impulse response (FIR)
$$F(t) = g(N(t)) = g(f[E(t), I(t)]);$$
3. The output of the filter is phase shifted – a delay is applied to filtered signal;
$$P(t) = F(t) + \Phi = g(f[E(t), I(t)]) + \Phi;$$
4. The shifted signal is half-wave rectified – only positive values of the signal are maintained
$$S(t) = R(P(t)) = R(g(f[E(t), I(t)]) + \Phi);$$
5. The abnormal oscillation is detected (when present) – threshold based detection on the power spectra of the rectified LFPs;
6. The optical stimulation is activated and its intensity is regulated based on the $S(t)$ signal (Figure 3.13.d).

Given the various steps and signal transformations of this closed-loop algorithm, it is evident that many parameters and variables play a key role in delivering a suitable stimulation signal, e.g. the filter frequency parameters, the phase shift Φ (time delay), the conversion from $S(t)$ to light intensity, etc. The *CANDO closed-loop algorithm team* is focused on testing this novel method in silico simulations, in-vitro experiments both in animal and in human brain slices, and in-vivo experiments in animal models (rodents and non-human primates), to demonstrate the effectiveness of seizure suppression before employing such algorithm in clinical trials. It is

expected that only a subset of phase shifts would ultimately reduce the abnormal oscillations, while other phase shifts would increase both the amplitude and duration of the instability. The Φ parameter, therefore, is of crucial importance and at the core of the CANDO research.

Implementing a multi-module implantable medical device

The gene therapy for optogenetic stimulation of neurons and the closed-loop algorithm for controlling abnormal network dynamics are the core techniques at the base of the CANDO approach. Still, to take such scientific innovation out of academic laboratories and into clinical practice, a medical device needs to be engineered. Electronic and optical components must be integrated into an implantable system intended for first-in-human clinical trials. This is required to (1) record continuously the brain activity, (2) convert it to be analysed in real-time by a processing unit implementing the closed-loop algorithm, and (3) drive light sources to stimulate the brain tissue when an epileptic seizure is detected.

– *But how is such a complex system made fully implantable and able to interact with the brain?*

In the previous chapter, we have introduced the distributed approach of multi-module neural implants and the opportunities they bring. These devices have allowed to effectively partition the system into physically separated modules, with the different functions located at different sites. The CANDO medical device relies on such approach, by proposing a modular implant system with a *central implant* located in the chest area and a *brain implant* located on the surfaces of the cortex. These communicate with each other through a multi-wire implantable lead. The CI module includes the battery, the power generation circuit, a processing/control unit implementing the closed-loop algorithm, and the communication interface. The implant at the brain side consists of an array of multiple modules, called *optoelectrodes*, or *optrodes*, all with the same functional capabilities. Each optrode comprises active electronics responsible for front-end recording and conversion of biopotential activity and generation of drive signals for the light sources. As the CI architecture is derived from established single-module IPGs architectures, the core research and development challenges gather around the optoelectrodes design and integration within the implant system. These include the physical construction of the

implantable modules, the circuit design of the active microelectronics, and their interaction with the other modules and the surrounding biological tissue. Moreover, the whole implant system has to be designed such that it meets the regulatory requirements for approval to be clinically used in epilepsy patients. Fortunately, in the past decade, several front-end *optoelectronic systems* have already been proposed in academic settings, showing promising results in animal experiments. These have employed diverse methods, both for recording and for stimulation, and have set the ground for developing the optoelectrode. To the best of the author's knowledge, this is the first attempt of its kind: a closed-loop optoelectronic medical device for the treatment of focal epilepsy.

Some of the earliest optoelectronic systems have used deposited electrode materials for recording and single-light guiding fibres for optical stimulation [133]. Others have integrated optic fibres within the established microelectrode arrays (MEAs), e.g. Utah recording electrodes [134], or developed directly arrays of penetrating optic fibres [135]. The key restriction with such approaches is that the number of emitted light channels is limited to a few optical sites, either located on the surfaces of the cortex or penetrating to reach deeper layers of the cortex, with resulting optical emission being transverse through the cortical layer structures. Zorzos et al. [136] improved on these designs by developing a probe with multiple light guiding structures. By doing so, emission was improved to a 45° angle, however, this created a new set of challenges related to optical multiplexing and connectivity.

Light guiding allows to generate the light externally and transport it to the location of interest, i.e. neural tissue. This gives many advantages to on-site light sources, as the electronic components are not in direct contact with the neural tissue. However, it creates also limitations, such as implantability and light transfer efficiency. McAlinden et al. have successfully fabricated an optical probe directly on an LED Gallium Nitride substrate [137]. In parallel, Doroudchi et al. [138] and Cao et al. [139] have demonstrated silicon probes with bonded on mini ($100\mu\text{m}$ to $500\mu\text{m}$ width/length dimensions) or micro-scale (sub $100\mu\text{m}$ dimensions) Light Emitting Diodes (LEDs). A key advantage with this approach is that the light emission is longitudinal with the cortical layering, giving the possibility to use multiple LEDs located at different depths, each of them illuminating only the cells of the same layer.

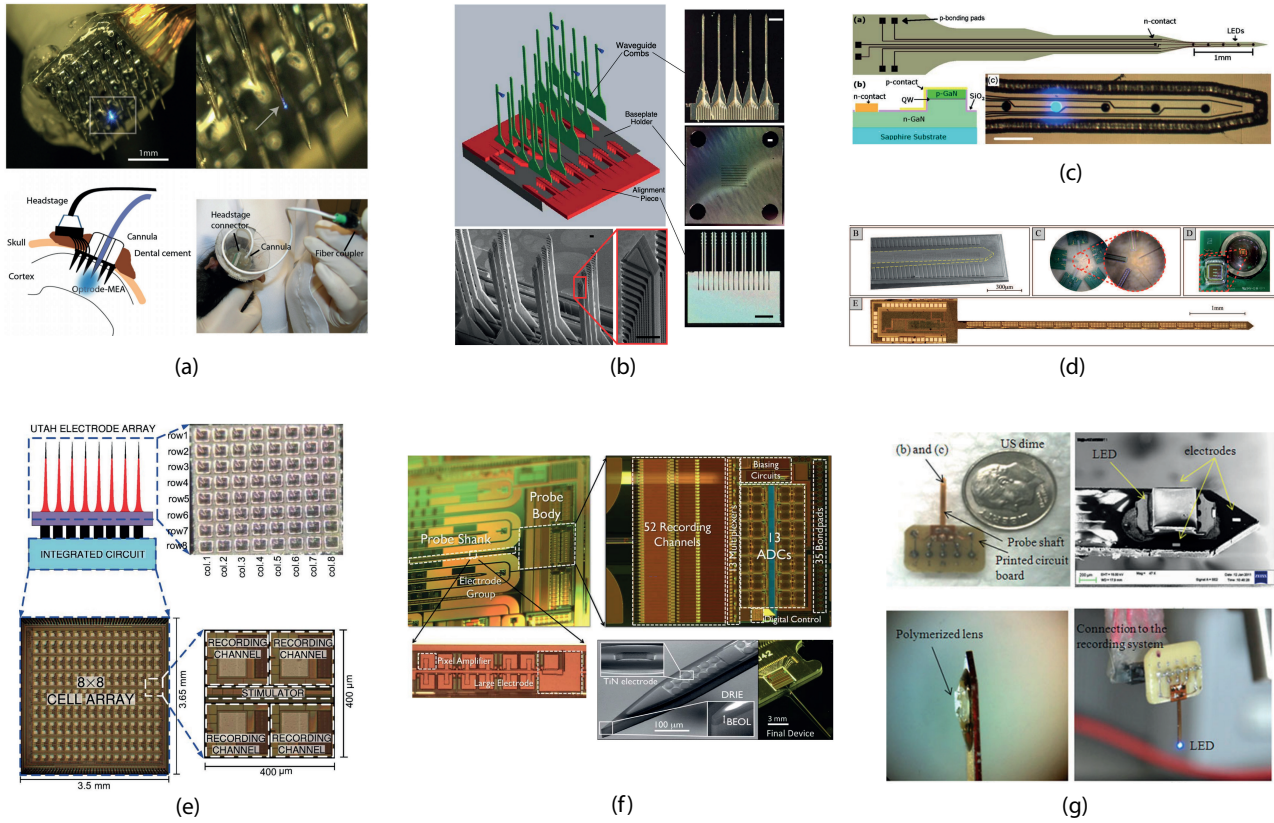


Figure 3.14: Examples of implantable probes for high-channel neural recording and/or optical stimulation: (a) hybrid device (optrode-MEA) incorporating a tapered coaxial optical electrode and a 100 element microelectrode array [134]; (b) implantable 3D waveguide array capable of independent light delivery to sets of neural targets in brain tissue [136]; (c) GaN-based LED probe for optogenetic applications [137]; (d) fully-multiplexed CMOS neural probe for in-vivo acute recordings [140]; (e) 320-Channel active neural probe for closed-loop electrical recording and stimulation [141]; (f) a fully-CMOS neural probe containing 455 active electrodes in the probe shank [142]; (g) integrated neural probe for simultaneous recording of neural activity and optical stimulation with μ LEDs [139].

This provides more accurate stimulation and a higher degree of control compared to light guiding methods. These solutions, however, have required to be driven via external electronics, which means the larger the number of stimulation and recording sites, the more connective wires are needed. This is highly undesirable for devices aiming for clinical translation. A more viable and scalable approach is to implement and integrate clever multiplexing of signals onto the probe itself. A number of highly integrated electronic probes with large numbers of electrical stimulation and recording sites have been previously described. For example, Shulyzki et al. [141] have demonstrated a chip, which can be combined with existing 8×8 Utah-style probes and up to 256 external recording pads. In addition, both Lopez et al. [142] and Angotzi et al. [140] have demonstrated probes fabricated from a CMOS base which incorporate respectively 455,

and 512 recording electrodes. An example of a system capable of both driving high radiance μ LEDs and performing electronic recording is the work presented by Chen et al. [143] In this case, the stimulator circuitry is designed primarily for laser control, and the electronic recording is designed for single-unit (action potential) recordings.

The *CANDO implant system team* aims to develop implantable probes that have capabilities to efficiently perform multi-channel neural recordings and drive multiple high-radiant light sources at different cortical depths. The proposed architecture is meant for long-term chronic use inside the human body, thus making the overall system efficiency a core priority, both for the recording and stimulating functions. LFPs are chosen for recording, as they have proven to be the most stable extracellular measurement for long term chronic studies [144] [145], while high-efficiency mini-LEDs are considered the most suitable option for light generation. Finally, microelectronic circuits for amplification and recording are based on the team's previous efforts in the design of analogue front-end for low-noise low-power neural recording [146] [147], and in CMOS-driven high-radiance neural stimulators for retinal prosthetics [148] [149].

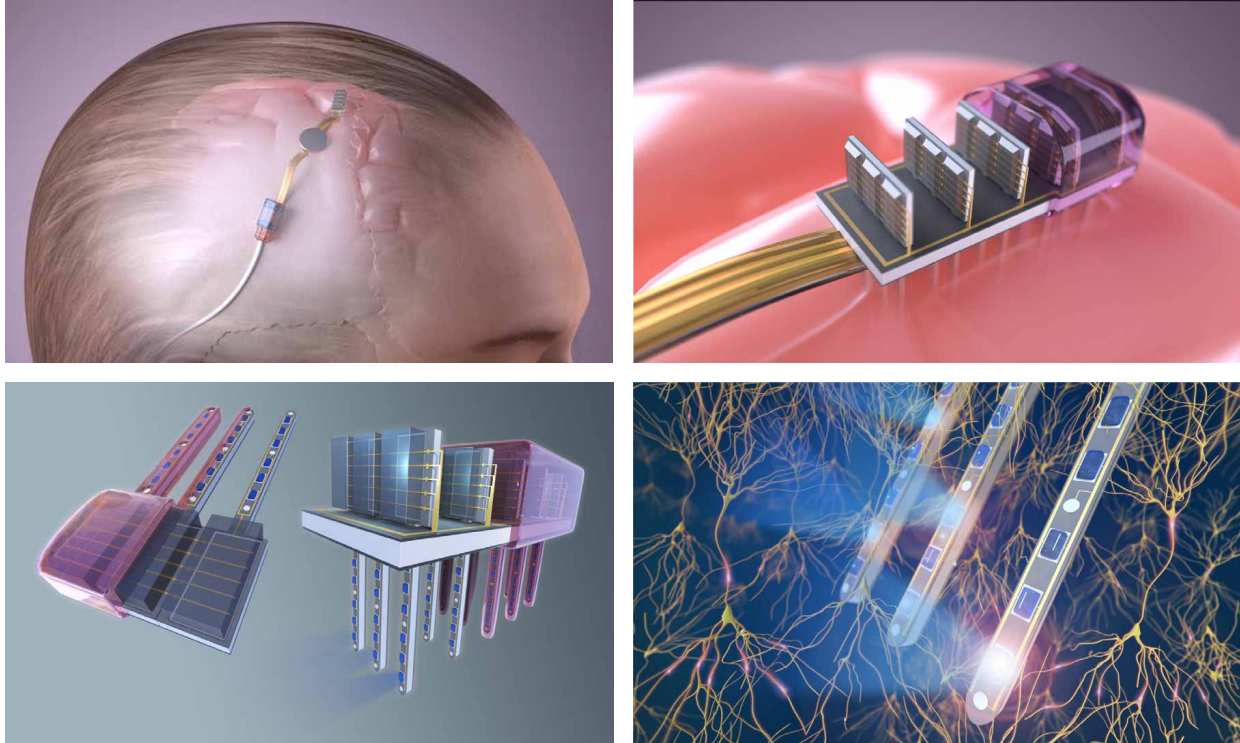


Figure 3.15: Illustrative concept of CANDO implant system, including the multi-optrode array delivering optogenetic control. This is achieved with penetrating probes comprising recording electrodes and blue-light mini-LEDs along the shaft.

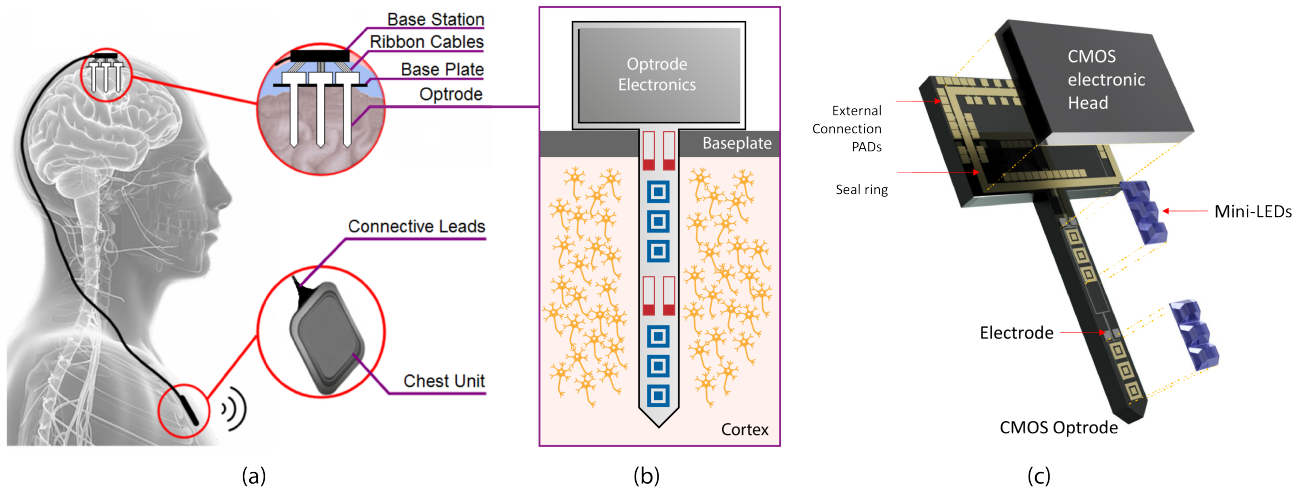


Figure 3.16: (a) the CAND0 modular implant concept: one chest implant, multiple probes within the brain implant; (b) illustration of the optrode implanted into the cortex; (c) 3D model of the optrode with the CMOS-based integrated circuit on the ‘head’ and the LEDs and the electrodes on the ‘shaft’.

3.3 The Implant System: Multi-Module Medical Device

The CAND0 implant system concept and optrode design are shown in Figure 3.16. The chest implant is a metallic case that houses a battery and electronic components. It connects to a connective lead, which is implanted under the skin and reaches the head passing along the neck, under the scalp, and eventually attaching to a base station/hub on the skull. This is a bridge that acts as an extension of the lead, by interfacing with the brain implant through custom ribbon cables. The latter are flexible, isolated wires that penetrate the skull to connect to the multi-optrode array within the brain implant. Each optrode presents a *head*, comprising the active electronic circuits, and a *shaft*, comprising recording sites (metallic electrodes) and stimulation sites (blue light mini-LEDs). The shaft is inserted longitudinally into the brain tissue to reach all the cortical layers, so that it can record from and illuminate neurons at different depths of the cortex. The optrodes are grouped together and secured mechanically onto a support baseplate, which ensures the original implant position and the distance between each optrode are maintained.

Particular effort is put by the CAND0 team on the development of the optrodes and brain implant – the core engineering challenge – both in terms of microelectronics design of the active electronics, implemented in CMOS technology, and of microfabrication and packaging of the

physical device. The development of other components, i.e. chest implant and implantable lead, is intended to be outsourced. At the time of writing, several iterations of the CANDO system have already been developed and integrated into various systems [150] [151] [152] [84]. These have been employed for bench-top tests and experiments in rodents to validate both the core functions of the devices and the end-to-end closed-loop control [153] [154]. In addition, experiments in Non-Human Primates (NHP) are currently ongoing. They are necessary to further validate the device in large animal models and to demonstrate pre-clinical data on safety and efficacy for the medical device to be approved for a first-in-human clinical trial.

Regulatory Approval

To obtain such approval, the technology/product development needs to follow the definition of the *user requirements* for delivering a medical device in accordance with the proposed clinical solution and with the stakeholders needs: patients, surgeons, clinicians, scientists, and manufacturers. Moreover, regulatory documentation is developed alongside the technology to ensure the clinical device meets the more extensive *technical requirements* defined by relevant directive guidelines and standards. Such requirements allow therefore to set the *design specifications* and the *technical specifications* for the development of the implantable system within the framework of the regulatory documentation. Through various stages of testing, the finalised device for use in clinical trial needs to verify the specification and ultimately validate the requirement.

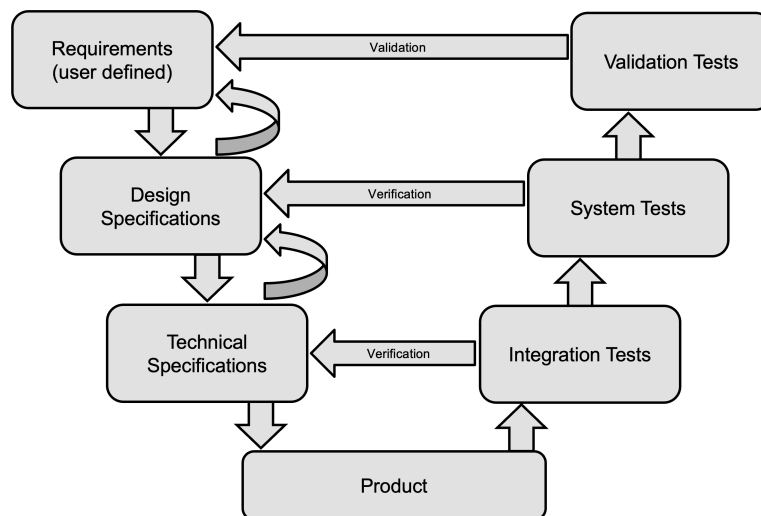


Figure 3.17: Development process for a medical device to ensure regulatory approval.

3.3.1 User Requirements and Technical Specifications

The CANDO medical device is targeted at patients with DRE. These patients typically have frequent seizures, and unless treated will continue to have seizures for the remainder of their life. Clinical solutions with implantable technologies require surgery and long-term implantation of a medical device that continuously interacts with the biological tissue. The key user requirements are summarised in the following:

1. *Efficacy*: the implant system must achieve sufficient control of abnormal network activity to abolish or significantly reduce seizure frequency and intensity.
2. *Tolerability*: the implant must have a life span of many years, and must produce minimal or no side effects.
3. *Safety*: the implant must produce no or minimal mechanical, thermal or chemical damage to the surrounding tissues over its lifetime. It must be sufficiently robust to withstand incidental trauma or the effects of a generalised tonic-clonic seizure. It must be immune to external sources of radiomagnetic interference, and must provide sufficient warning of failure to allow alternative treatments to be instigated.
4. *Compatibility*: patients with epilepsy are as likely as any other to develop unrelated pathologies. The implant must therefore not interfere with the diagnosis or treatment of these unrelated pathologies; specifically if possible it should be Magnetic Resonant Imaging (MRI) compatible to allow high-resolution structural brain imaging.
5. *Sterility and surgery*: The device must be able to be sterilised and be convenient to use in a surgical setting.

Each item of this list of requirements expands into an extensive list of technical requirements, which in turn yield sets of technical and design specifications. These are formalizations of the technical requirements into a set of verifiable capabilities and constraints that the design should incorporate. As there are many ways of realising these requirements, the design specifications have been subject to change throughout the project development. Compliance of such specifications are fulfilled through compliance with standards, e.g. ISO 13485 Medical Devices.

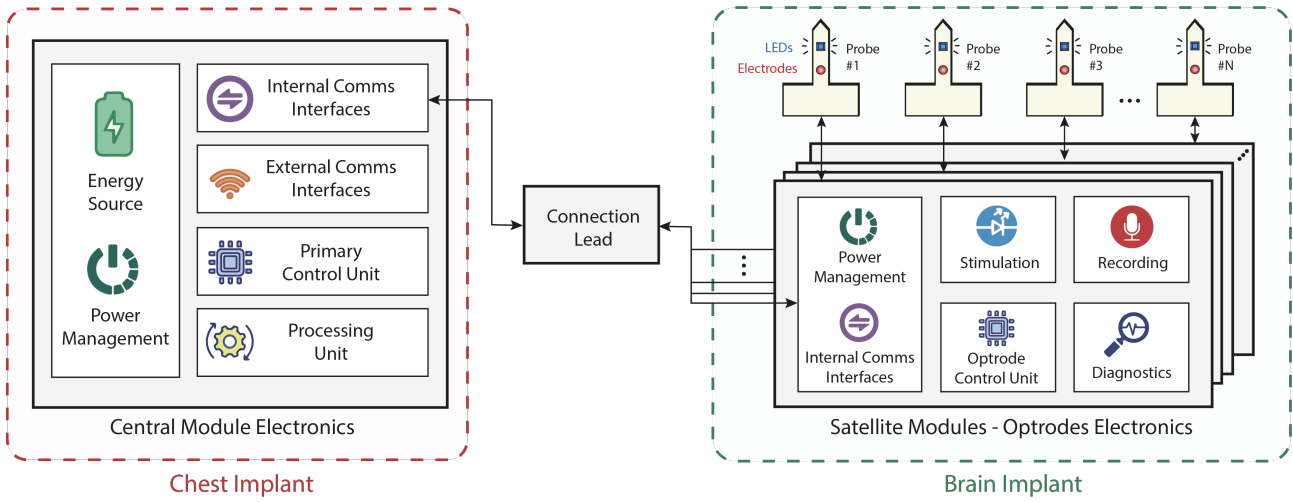


Figure 3.18: Block diagram of the CANDO implantable system with conceptual representation of the main functions and circuitry.

It is clear to note the complexity of designing, developing, and implementing a medical device for in-human use, as this has to meet requirements from various stakeholders and to comply with strict standards. As it would take a full thesis on its own to discuss about the requirements and the decisions that led to defining the design specifications of the implantable device, in the following we are focusing on the high level specifications of the key features and novelties of the implantable medical device: (1) *core functions*, i.e. recording and stimulation; (2) and *connectivity functions*, i.e. power management and data communication.

The connectivity functions will be only introduced in this Chapter and will be described in detail in the next Chapters, as it is the research focus of this doctorate thesis. A block diagram of the CANDO implantable system architecture is presented in Figure 3.18, illustrating the different core functions, connectivity functions, and additional support functions.

3.3.2 Core Functions: Recording and Stimulation

Observing Neural Activity - Recording

Neural activity can be observed extracellularly at single unit level using penetrating implantable electrodes and electronics to amplify and sample this with sufficient bandwidth (typically 10-20 kHz). Although such technology has been the workhorse for most experimental neurosci-

entists over recent decades, observing this activity chronically has proven challenging. This is because of a number of reasons stemming from the fact that any silicon probe is essentially a ‘foreign body’, with different mechanical/material properties to the surrounding tissue, and the insertion will cause short term damage (rupturing blood vessels, cutting through tissue), and longer term effects (foreign body response, gliosis/scar tissue growth, cell death). Furthermore, there could also be secondary effects due to the integrity of the probe itself (electrode damage, corrosion, mechanical failure during insertion, etc). These challenges are described in some detail in recent reviews by Chen et al [155] and Szostak et al [156].

There has recently been significant interest in utilizing local field potentials as the early evidence suggests these may be more resilient to the neural recordings ‘fading’ over time [157] [158]. LFPs are primarily in the 1-100 Hz range, but high frequency oscillations can extend to hundreds of Hz [159] [144]. It has been shown however that even the lower frequency LFPs have useful information content [145] [160].

The CANDO recording function presented herein thus utilises low frequency LFPs for two reasons: firstly to exploit this ‘improved’ chronic stability (compared to single-unit recordings); and second to allow for increased scalability – as these recordings require a lower data bandwidth, more channels are possible for a given power budget. As discussed, the ultimate goal is to develop devices capable of controlling the dynamics of neural populations, such as abnormal oscillations. Such population dynamics is readily observed in LFP biopotential, hence recording LFPs it’s shown once more to be the most suitable method for identifying epileptic seizures, hence used in CANDO.

Every optrode includes multiple recording sites and channels. Each channel will continuously observe LFP signals from a specific site in the shaft – one recording electrode and one reference electrode. LFP signals can have amplitudes up to 5–10 mV, with a power spectrum predominantly below 100–200 Hz, down to sub-Hz. A recording channel consists of different front-end stages that amplify and filter the measured biopotential, so to amplify the signal of interest and reduce the noise and interference. The analogue signals are then converted into digital data (with an ADC) to be sent to the chest implant for processing and analysis.

Modulating Neural Activity - Stimulation

Optical stimulation can be physically conducted using high efficiency LEDs. Gallium Nitride μ LEDs implemented onto passive optrodes have been described previously by McAlinden et al [137] and have demonstrated efficiencies of around 5%. Similar efficiencies were recorded in past efforts of the CANDO teams with such devices [148] [149] [161]. Mini LEDs can provide higher efficiencies as they can be driven at lower current densities for the same amount of luminance. The light sources most suitable for the optrode design are CREE (DA2432), which provides up to 30% efficiency in the driving range required for optogenetic stimulation. Implementation of similar devices onto passive optrodes has previously been described by Doroudchi et al [138] and Cao et al [139].

Optogenetically encoded cells will integrate light over a period of milliseconds to tens of milliseconds which then modifies their baseline activity [162] [163]. Thus, light can be either driven as a modulated intensity signal over time, or as a fixed intensity with pulse width modulation, i.e. it is the integral photon flux, which will drive the biological response. In the former case, for the light to be emitted by the LEDs, thus for the LEDs to turn on, a large enough voltage must be provided and maintained during the stimulation time. In addition, a current control driver is needed to modulate the light intensity in time. In the second case, the driver sets a fixed value of the current and provides light intensity control by switches the LED on and off with a variable duty-cycle. When stimulation is needed, the chest implant informs the optrodes to turn the LEDs on. The light intensity value is set by a DAC that generates the analogue signal to drive the LEDs with the defined current (or duty-cycle ratio).

It is important to note that, while the LED radiance (power emitted in watts) increases linearly with driving current, the LED efficiency (the amount of light produced for each watt of electricity consumed) does not behave in the same way. In fact, it reaches a peak and then drops as the current increases. LED drive currents in the region of 0–1 mA are considered sufficient to stimulate enough neural tissue to provide effective optogenetic stimulation, while maintaining adequate efficiency levels.

3.3.3 Connectivity Functions: Power and Data Communication

For the optrodes to operate correctly, thus to perform their core functions, it is crucial at any time to ensure adequate power levels and operation instructions are provided. As the CANDO system is fully-implantable, the energy source needs to be provided either from outside, through wireless charging, or from inside, with an implantable battery. To meet the user requirements, e.g. tolerability and safety, the implant system includes a rechargeable battery in the central module, responsible for generating the energy for all the electronic components in the system. Given the multi-module characteristics of the implant, such energy needs to be distributed to each module and adapted to the required voltage and current levels.

The power management circuits, located both at the central implant and within each satellite module at the brain implant, guarantee such levels are achieved by transferring power from CI to BI and converting it from DC domain to AC domain at CI end and from AC to DC at the BI end. In fact, an alternating signal is employed as power carrier, exploiting the physical wires within the implantable cable that connects the different modules. Such cable is also used to allow bidirectional communication between the latter. This ensures commands generated at the central module are encoded and delivered to the optrodes, which interpret them and perform the core functions in response to the decoded information. In turn, the optrodes send back to the CI digital data representing the analogue signal recorded from the cortex. To implement this end-to-end communication system, a custom protocol is developed for the CANDO inter-module communication: the *4-wire Communication System (4WiCS)*. This is chosen rather than standard protocols as it can be optimised for the chosen communication channel and for the required data rates in the two directions. Furthermore, it allows to superimpose the power carrier to the data communication signal.

This 4WiCS protocol – together with the circuitry designed to effectively implement it – is the focus of the next Chapter 4. Its operation within an emulated end-to-end implantable system is presented in Chapter 5, followed by a discussion on key design considerations to achieve an efficient, reliable, and safe system. Finally, an improved 2nd version of the circuits is demonstrated as part of a fully-integrated microsystem for use in clinical trials.

Chapter 4

In-body Wireline Interface for Power and Data Transfer

This Chapter¹ introduces and describes the inter-module interfacing system implemented within the CANDO multi-module implant. This allows the CI module to effectively communicate with the BI modules and provides a power management and transfer scheme that supplies all modules with power generated from a single energy source located at the CI end. A new data protocol, tailored to the specific application and information exchange rate, is also created as part of the interfacing system. First, such system is introduced and its high-level features outlined in the context of the CANDO implant system. Then the main sub-systems/blocks constituting the interfacing are presented and described, expanding on the circuit implementation and performance characterisation through measured results. These are implemented both with off-the-shelf components assembled on printed circuit boards – i.e. for the chest implant interface – and a custom chip designed and fabricated in CMOS technology – i.e. for the brain implant interface. Moreover, a medical-grade implantable cable is used as interfacing channel between CI and BI, which is electrically characterised and described.

¹The designs, implementations, tests, and results presented in the following are obtained from the research pursued within the CANDO project. They derive from collaboration with colleagues, peers, and students from the Centre for Bio-inspired Technology of Imperial College London, promptly cited in the relative sections. The content described hereby has already been published in two conference papers and one journal paper. Portions of the content written in this document have been adapted from such publications. They are: [164] [165] [32]. The author of this thesis is a co-author in all three publication.

4.1 4-Wire Communication System (4WiCS) Interface

This work proposes an in-body wireline interfacing system based on a new custom protocol for power and data transmission between multiple implants. This system is called **4-Wire Communication System – 4WiCS**. It provides wireline neural implants with communication capabilities. It is developed to meet the specifications and constraints of the CANDO implantable medical device, thus optimised for the latter. As described in the previous Chapter 3, this includes a chest implant, or central module, and a brain implant comprising multiple satellite modules. The chest implant houses power management circuits, control and processing units. These are responsible for generating the signals to power and control also the modules at the brain implant. The latter contains an array of active probes (optrodes) for observing neural activity (electrical recording), and neuromodulation (optical stimulation using optogenetics). These functions are enabled with the probe core circuits. Figure 4.2 illustrates the 4WiCS interfacing concept and the implant system block diagram.

The physical communication layer is implemented with a 4-wire subcutaneous lead, connecting to both implants through two interfaces, the *4WiCS chest implant interface* and the *4WiCS brain implant interfaces*, as shown in Figure 4.2. These realise the following functions: (1) providing power from the chest implant to the brain implant; (2) communicating configuration data and stimulation control commands via the *downlink* (chest-to-brain); (3) receiving recording and diagnostic data via the *uplink* (brain-to-chest). As the system requires simultaneous data recording and stimulation, a full-duplex communication link is used between CI and BI.

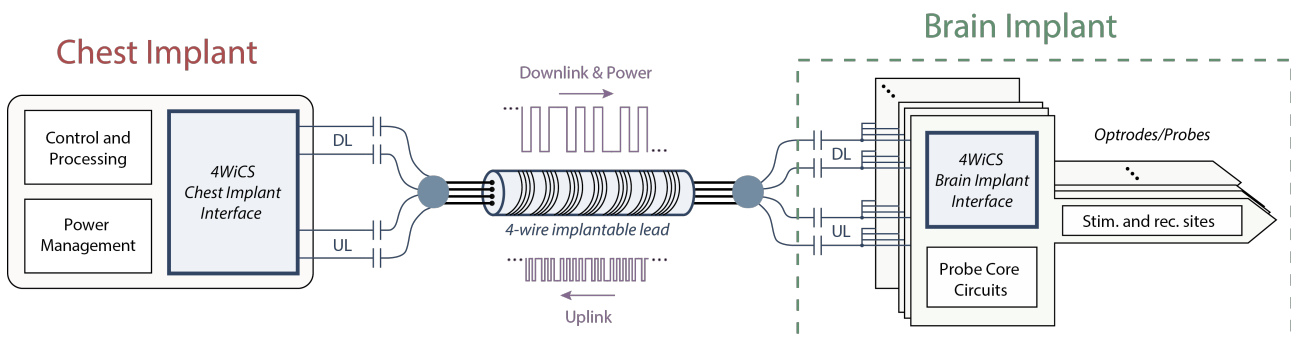


Figure 4.1: 4WiCS interfacing concept, with highlighted in blue the three blocks constituting the system.

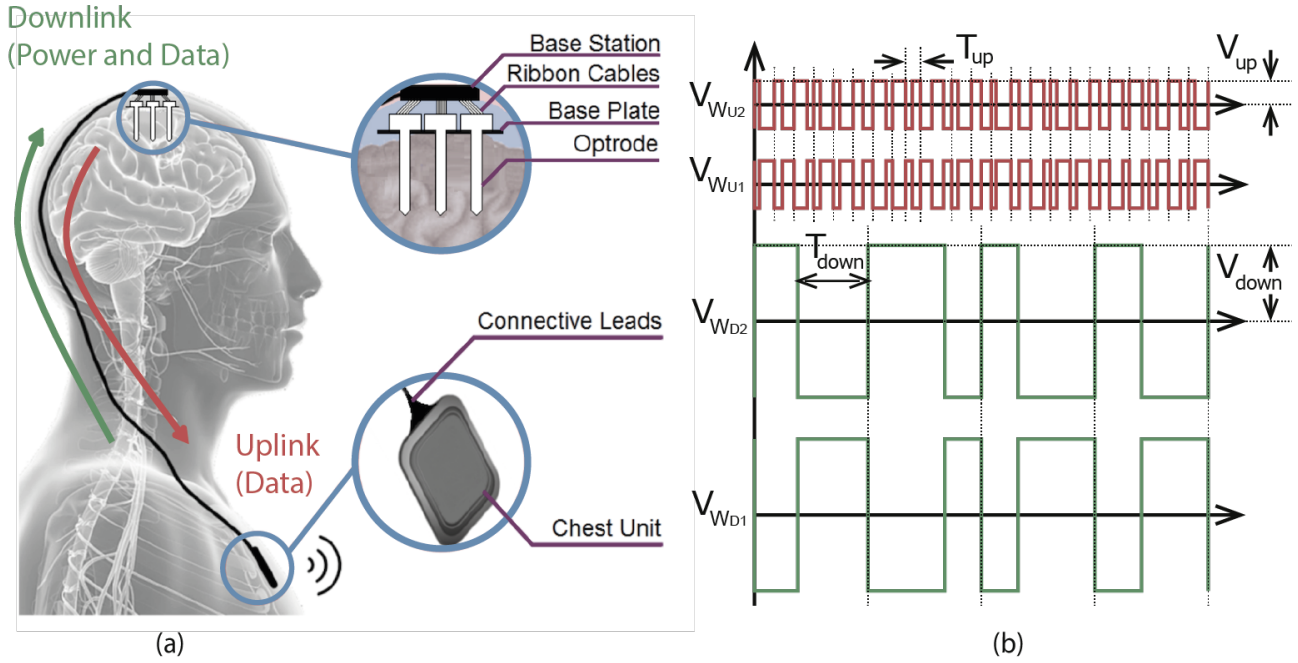


Figure 4.2: (a) Model of CANDO implant system and 4WiCS interfacing concept; (b) Ideal voltage waveforms on the 4-wire implantable lead.

The communication protocol is based on a hybrid *star-bus multipoint network*: the CI is the central hub and acts as the master of the communication link, sending command data packets through the bus. The optrodes at the BI end are the satellite nodes that act as the slaves, responding back to the CI through the same data bus.

To reduce the risk of corrosion to lead-insulation due to static electric fields or the possibility of any current leakage, all connections outside the chest and brain implants have DC-blocking capacitors in series with the wires. Moreover, a fully-differential data transmission scheme is adopted for immunity to common-mode noise and lead interference. This is preferred to single-end for data communication through implantable cables, as currently available leads (approved for human use) impose limitations on the system due to their relatively low bandwidth, large transmission delay, high wire-to-wire capacitance, and non-uniform characteristics (e.g. each conductor present different parasitics) [166], [68]. These also tend to lack shielding of the different wires to improve mechanical properties (e.g. flexibility).

To implement a star-bus network architecture, all 4 wires are shared and connected in parallel to all optrode devices (Figure 4.2). This solution is chosen also to keep the number of wires of the cable to a minimum. For this same reason, the power transmission and downlink are

Table 4.1: 4WiCS Interfacing - Design Specification Parameters

Implant Module	Parameter	Value
Power Transfer	Transmission means	2 wires (with downlink)
	Transmission form	AC square wave
	Transmission direction	chest-to-brain
	Maximum peak current at BI	20 mA
	Average current at BI	4 mA
Downlink Communication	Physical layer	2 wires (with power)
	Coupling	AC coupled
	Data packet width	26 bits
	Modulation scheme	Phase encoding
	Bit-rate	100 kbps
Uplink Communication	Physical layer	2 wires
	Coupling	AC coupled
	Data packet width	26 bits
	Modulation scheme	Phase encoding
	Maximum Bit-rate	1.6 Mbps

combined and superimposed on a single pair of wires. This will, in addition, allow to save energy, resulting in an increase of the chest implant battery-life. A second pair of wires is therefore dedicated exclusively to the uplink data communication, ensuring a reliable data recovery on the chest implant. Superposition of downlink+power and uplink in the same 2 wires is excluded. Although this is possible and would contribute to reducing the number of wires further, it would require complex hardware and signal processing at the CI end to recover the uplink data.

A square-wave signal is used (instead of sinusoidal) for power transmission through the downlink path. This is done to: (1) avoid the need for large off-chip smoothing capacitors for the AC/DC conversion at the 4WiCS BI interface; (2) simplify the downlink generation at the 4WiCS CI interface; and (3) maximise the power efficiency at the different signal conversion stages. This comes at a cost of higher power loss in physical layer, as the high-frequency components of the square wave induce a larger dielectric loss in the cable. Furthermore, both the downlink and uplink communications use baseband digital modulation due to relatively small bandwidth of the lead wires.

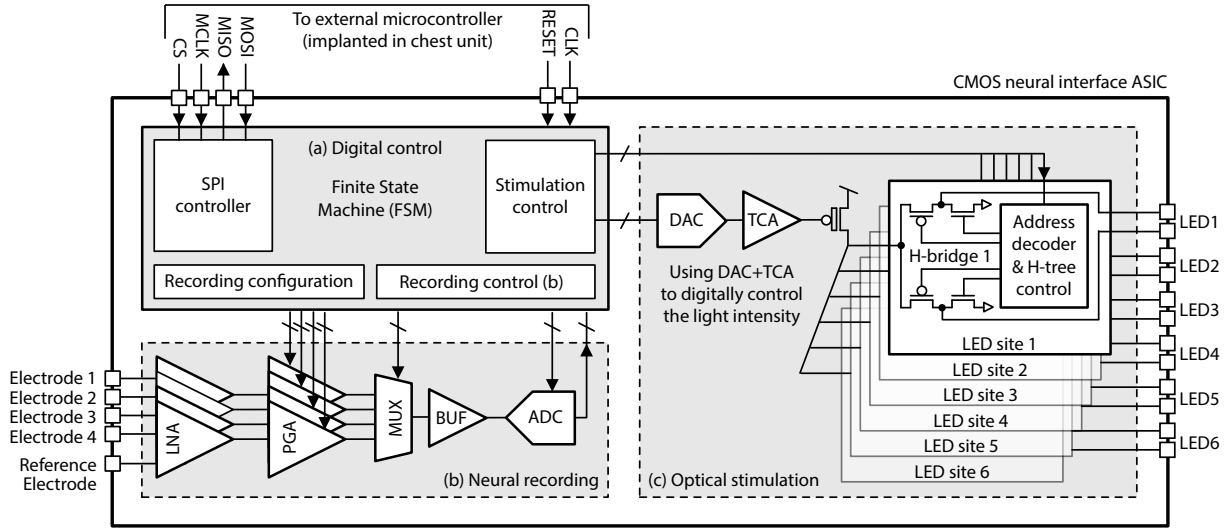


Figure 4.3: System architecture of the CANDO1 microelectronic implementation.[84]

Table.4.1 lists the design parameters for the 4WiCS implant system interface. These derive both from the technical requirements set by the CANDO clinical application, e.g. maximum heating/temperature increase allowed for each optrode, and from the technical specifications of the probe core circuits, e.g. number of LEDs per optrode and their electrical characteristics. Moreover, at the time of the design of the 4WiCS interfaces, two iterations of the optrode microelectronics had been implemented by the CANDO team, hence also two iterations of the core circuits. The first version, *CANDO1* chip, was implemented in 0.35 μm CMOS technology and is thoroughly described within the "*On-Probe Neural Interface ASIC for Combined Electrical Recording and Optogenetic Stimulation*" paper published in the 3rd 2018 issue of the TBioCAS Journal [84].

Table 4.2: Design parameters comparison between CANDO1 and CANDO3 ASICs

Core Function	Parameter	CANDO1	CANDO3
Optical Stimulation	# of LEDs per optrode	6	8
	LED voltage supply	5 V	5 V
	LED drive maximum current	1.1 mA	5.3 mA
Neural Recording	# of rec channels per optrode	4	2
	Recording voltage supply	3.3V	3.3V
	Recording bandwidth per channel	0.1-1000Hz	0.1-1000Hz
Power and Data Comms	Power supply	Off-chip	On-Chip
	Primary data comms protocol	SPI	SPI + 4WiCS
	Data packet size	8-bit	26-bit

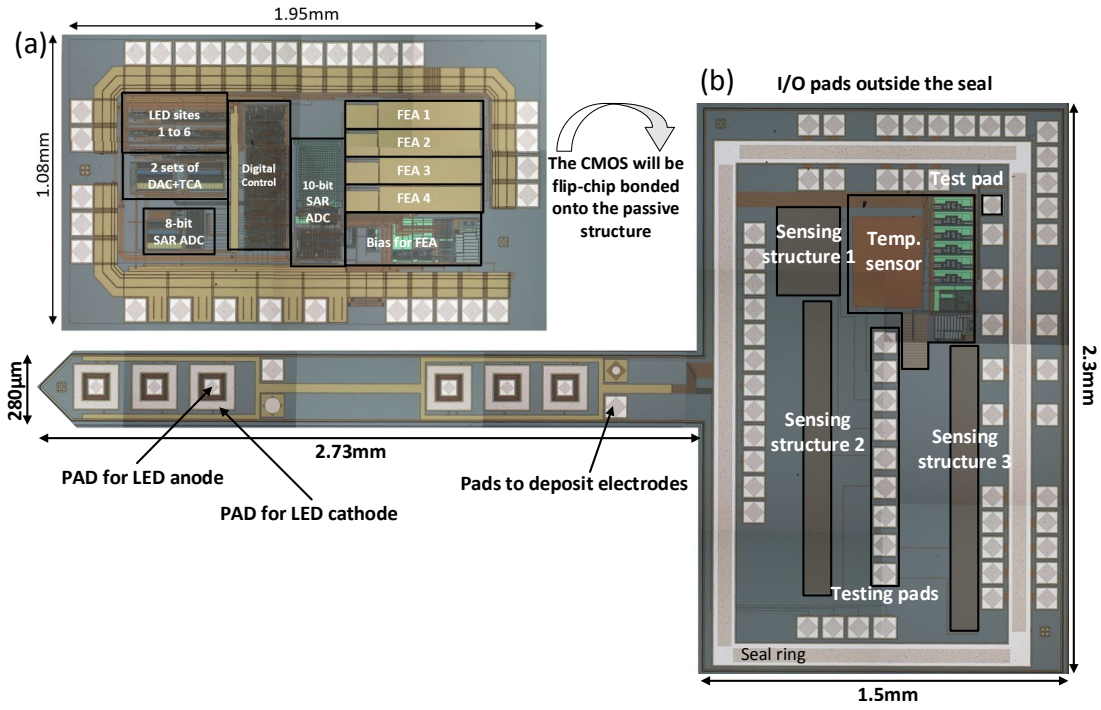


Figure 4.4: CANDO1 fabricated device microphotograph showing: (a) the optrode microelectronics implemented in $0.35\ \mu\text{m}$ CMOS technology; (b) CMOS-based probe with pads for LED and electrodes. [84]

The 4WiCS interface presented in this Chapter is designed to be compatible with the core circuitry implemented within the *CANDO3* microelectronics version². Although there are no publications describing the circuits within this specific version, its high-level architecture is unchanged from *CANDO1*. The main features of *CANDO3* and the differences with *CANDO1* are summarised in the Table 4.2.

In the following, the three main blocks of the 4WiCS interfacing system are presented and described in detail. These are:

- the 4WiCS brain implant interface – interfacing unit within each satellite module;
- the 4WiCS implantable lead – physical wired communication channel;
- the 4WiCS chest implant interface – interfacing unit within the central module.

²additional interfacing circuitry is necessary for correct operation.

4.2 Satellite Module - ASIC Interface Design and Test

The work described in this section has been accomplished in collaboration with Dr Sara Ghoreishizadeh, Dr Yan Liu, and Dr Tim Constandinou. Both a conference paper and a journal paper have been published, respectively in the LASCAS 2017 Proceedings [164] and in the TCAS-I Journal 2017 Special Issue [165]. Dr Sara Ghoreishizadeh led the chip design and publication drafting. The author of this thesis has contributed in part to the architecture design of the CMOS ASIC, and also by leading the testing and characterisation of all the circuits and the communication channel.

In the brain implant, a passive baseplate hosts multiple identical satellite modules and a few discrete components connecting to the 4-wire lead. Each optrode has 3 electrical recording sites (2 channel inputs, 1 reference input) to provide spatial resolution for recording of local field potentials, and a number of optical stimulation sites/LEDs for optogenetic neuromodulation. In order to function properly and with the required performance, such core circuits have the following requirements:

- DC power supply across LEDs for optical stimulation (@5 V DC)³;
- Stable DC power supply for powering up core circuitry (@3.3 V DC);
- Upscaled clock for the digital circuitry (@1.6MHz);
- Demodulation/decoding circuitry (downlink);
- Modulation/encoding circuitry (uplink).

4.2.1 Circuit Design and Implementation

To provide the optrodes with the required power supply and interfacing features, the **4WiCS brain implant interface** has been designed and implemented in 0.35 μ m CMOS technology. This ASIC has been designed as a separate integrated circuit with the intent to be monolithically

³The 5 V requirement is due to the high ‘turn on’ voltage needed as forward bias for the LEDs (>4 V) and to allow for a voltage drop on the connectors due to the contact resistance.

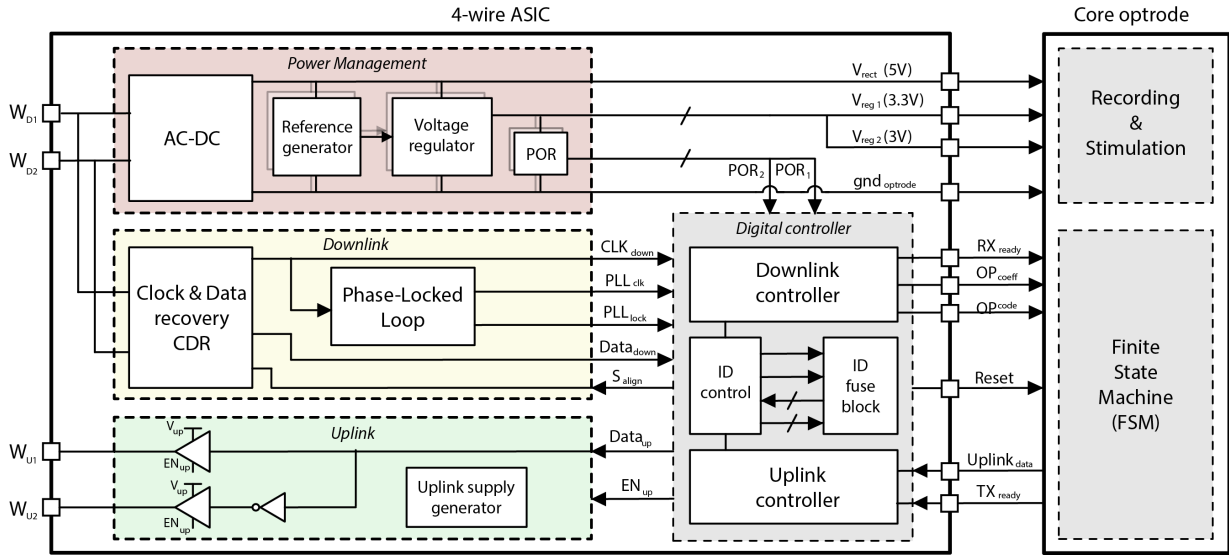


Figure 4.5: Top-level system architecture of the 4WiCS brain implant interface ASIC. Highlighted are the power management, the downlink, and the uplink circuitry.

integrated within each of the optrodes in the future. It is divided into three main blocks: (1) Power Management (PM); (2) Downlink Communication (DL); and (3) Uplink Communication (UL), providing the three main interfacing functions. The top-level architecture of the 4WiCS ASIC is shown in Figure 4.5.

Power Management

The PM subsystem is connected to the first two wires of the 4-wire lead from which it receives the input power signals (AC domain) to convert. At the output, it provides the core optrode circuitry with the converted power output signals (DC domain). The PM block diagram is illustrated in Figure 4.5, while the specific circuits are shown in the schematics in Figure 4.6.

- Since a fully-differential power and data transmission scheme is employed, an AC/DC converter is required at the PM. Therefore, a passive *full-wave voltage rectifier* is designed to generate the 5V DC-supply starting from the squarewave AC signal on the two wires W_{D1} and W_{D2} (Figure 4.5). It is based on a topology consisting of a diode-connecting p-channel MOSFET transistor (PMOS) pair and a cross-coupled n-channel MOSFET transistor (NMOS) pair [64] [167]. Moreover, a dynamic body biasing technique is used to bias the PMOS bulks at the highest potential [168].

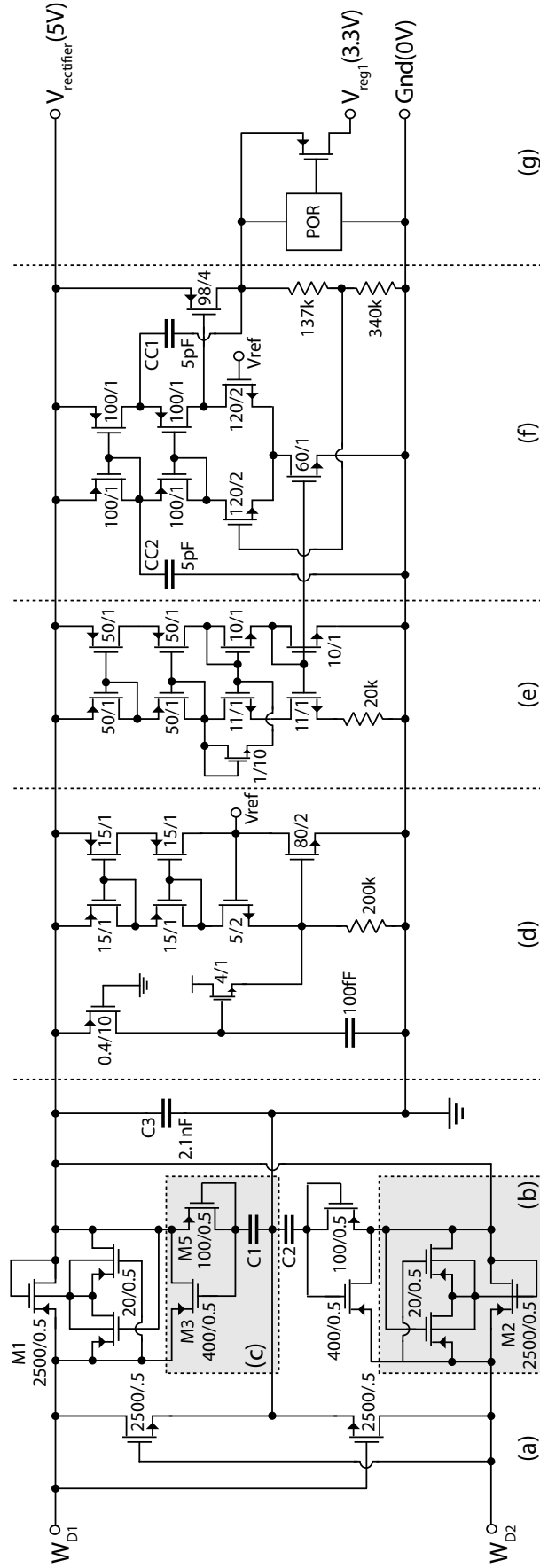


Figure 4.6: Circuit schematic of the power management subsystem on the 4WiCS ASIC showing: (a) full-wave voltage rectifier with (b) bulk biasing, and (c) charge storage techniques; (d) reference voltage generator with start-up circuit; (e) bias voltage generator for power gating during start-up; (g) connections to the POR circuit for power gating during start-up.

- The voltage at the output of the rectifier is thus used by a *linear voltage regulator* as input signal in order to generate as output a 3.3V regulated supply for powering up the optrode core circuits. The regulator, REG_1 , is based on a telescopic amplifier driving a pass-transistor that provides the negative feedback (using Miller compensation to eliminate the forward zero). A circuit for biasing the core regulator is also implemented on-chip by means of a beta multiplier. Furthermore, a *reference voltage generator* ensures the reference output is maintained constant over a wide range of supply voltages [169]. A second regulator with the same topology, REG_2 , is implemented in order to provide two separate regulated supplies for different circuits. This is to limit the interference to noise-sensitive elements.
- A *power-on-reset* (POR) circuit is employed to guarantee the regulator output is disconnected from the load during start-up and in the event of large voltage drops.

Downlink Communication

The DL subsystem shares the same wires, W_{D1} and W_{D2} , with the PM. The input signals are retrieved and decoded and then sent to the core circuits as data and clock signals.

- The differential signal on W_{D1} and W_{D2} is encoded in Manchester coding (phase encoding). This line code is chosen because it prevents long sequences of highs-only (or low-only) data bits from being transmitted, as both 'zeroes' and 'ones' are encoded with a transition – from high-to-low ('0' bit) or low-to-high ('1' bit). A decoder and clock/data separator is needed to obtain two distinct signals – data and clock. To achieve this, a *Clock and Data Recovery (CDR)* circuit is used to first convert the differential signal to a single-ended signal and then recover the downlink data and clock signals (clk1@100kHz). Non-hysteretic comparators and an inverter shift the signal level, while an edge detector is employed to achieve clock and data separation. Finally, a thyristor-based delay circuit generates a delay time in order to ensure a correct clock recovery [170]. The data signal and the clock signal are therefore separated in $data_{down}$ and clk_{down} signals, as shown in Figure 4.7(a).
- The clock is additionally processed in order to generate a second clock signal, the uplink clock (clk2@1.6 MHz), needed to drive the optrode core circuits and the UL circuitry. This

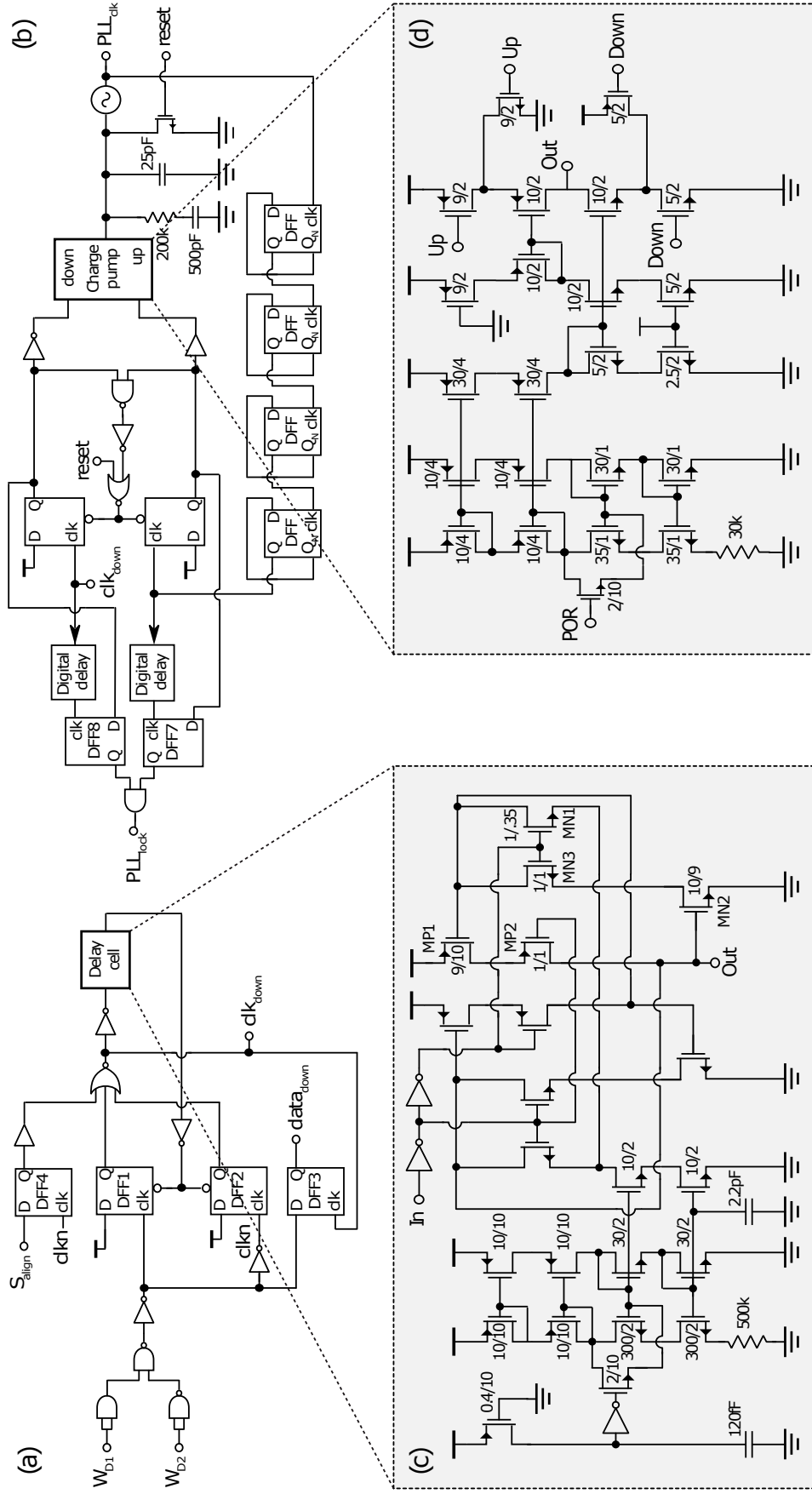


Figure 4.7: Downlink Communication subsystem schematics showing: (a) clock and data recovery; (b) phase-locked loop; (c) delay cell used in CDR; (d) charge pump circuit used in the PLL.

is accomplished by means of a second-order *Phase Locked Loop* (PLL), a device that can generate a higher frequency signal at the output, starting from a lower frequency signal at the input. It is based on 4 main sub-circuits: *Phase and Frequency Detector (PFD)*, *Charge Pump (CP)*, *Loop Low-Pass Filter (LPF)* [171], and *Voltage-Controlled Oscillator (VCO)*. Besides the new clock signal, a lock signal is generated as well in this subsystem, which activates when the clock frequency at the PLL output is in the required range.

Uplink Communication

The UL subsystem is physically connected to the second pair of wires (W_{U1} and W_{U2}) and transmits differential signals through them. The uplink data signal and the uplink clock signal are received coming from the core optrode and encoded with a simple *XOR gate* (phase encoding). The encoded signal is then inverted and the two versions of the signal, the inverted and the non-inverted ones, are sent to two tristate buffers. When the buffers are enabled by an enable signal from the core optrode, the two signals are transmitted to W_{U1} and W_{U2} .

Integrated Circuit Fabrication

The 1st generation (gen1) of the 4WiCS application specific integrated circuit has been implemented in AMS 0.35 μ m 2P4M CMOS technology (H35B4S3) occupying a silicon footprint of 1.5 mm^2 . Thick oxide transistors have been used for all circuits that interact with W_{D1} and W_{D2} . The power management and full-duplex communication circuits have been configured and fabricated in two different form factors: (1) as a complete system embedded within the optrode to be used in the end-application, with only access points being connections to the 4-wire lead; and (2) as a standalone test circuit, with the CDR, PLL and power management unit accessible for testing purposes. Inverting voltage buffers were used on the digital outputs $data_{down}$, clk_{down} , PLL_{lock} , and PLL_{clk} . The buffers are powered through the same supply voltages powering the CDR and PLL. The I/O ring was connected to the rectifier output. The microphotograph and layout with annotated floorplan are shown in Figure 4.8, while Table.4.3 lists the simulated circuit specifications.

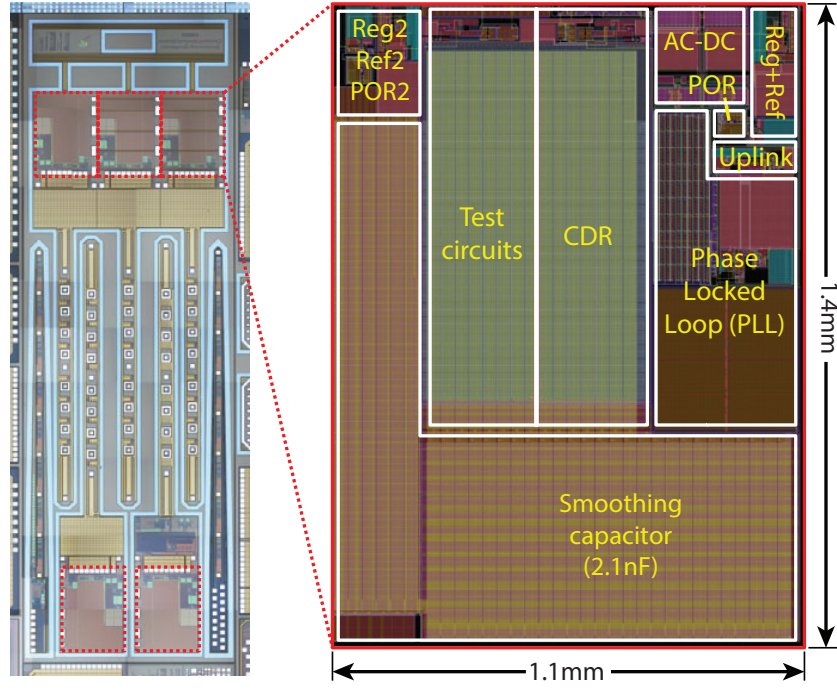


Figure 4.8: Fabricated 4WiCS gen1 ASIC implemented in $0.35\mu\text{m}$ CMOS technology. Shown are: (a) microphotograph of optrode system (5 optrodes shown); (b) layout and annotated floorplan of the 4WiCS brain implant interface.

Table 4.3: Simulated Technical Specifications

Circuit	Parameter	Value	Unit
Rectifier	V_{out}	≈ 5	V
	$I_{out,max}$	2.5	mA
	$V_{drop,rect}$	1.15	V
Reference generator	I_{DD}	8	μA
	V_{ref}	2.09	V
	PSRR@0.2 MHz	65	dB
Voltage regulator	PSRR@1 kHz	76	dB
	PSRR@0.2 MHz	46	dB
	I_{DD}	21	μA
	line regulations	0.2	mV/V
PLL	Lock-in range	33-200	kHz
	$I_{DD,avg}$	10.5	μA
	start-up time	$70 \times T_{clk,in}$	
	rms jitter	70	ps
CDR	$I_{DD,avg}$	1.2	μA
	T_d	7.5 ± 2	μs
Uplink	$I_{DD,avg}$	21.5	μA
Total	$I_{DD,avg}$	91.2	μA
	area	1.5	mm^2

4.2.2 Testing and Measured Results

The 4WiCS ASIC has been tested under various conditions using the measurement setup shown in Figure 4.9. To emulate the signals coming from the chest implant (central module), a 2-channel function generator was used, providing both power and downlink signals. The Cooper cable was employed as communication channel: this is an implantable lead approved under both the FDA and EU regulations (described in Section 4.3). The cable was connected between the function generator and the 4WiCS chip through two $1.5\mu\text{F}$ DC-blocking capacitors per wire, placed at either end of the wires. Although in theory, one capacitor per wire is enough to decouple the chest and brain implants, in this work two DC-blocking capacitors per wire were used for safety reasons. This is to ensure that, in case of breakage on the lead and/or the DC-coupling capacitors on the CI side, the brain implant is still decoupled from the rest of the system and any DC current is prohibited.

The wires W_{D1} and W_{D2} were used for downlink, and W_{U1} and W_{U2} for uplink. A capacitive equalization network was added such that the coupling from downlink path to uplink path, thus the interference deriving from that, is minimised. More details of such interference are given in the next section. All voltages were measured differentially, either between two wires within the lead or with respect to the local ground at the output of the rectifier. The rise/fall time of the squarewaves on the function generator were set to 50 ns and the amplitude was tuned to compensate for the voltage drop on the cable and on the rectifier, such that the voltage rectifier outputs an average unregulated voltage of 5 V.

Downlink Communication and Power Management

The downlink and power management circuits were tested under two different conditions and results are shown in Figure 4.10:

- (1) a single IC was driven by a V_{down} (squarewave at 100 kHz frequency); The recovered $Data_{down}$ signal remains at zero while clk_{down} successfully recovers the 100 kHz clock. This is because a squarewave of 100 kHz corresponds to a data sequence of all zeros (Manchester

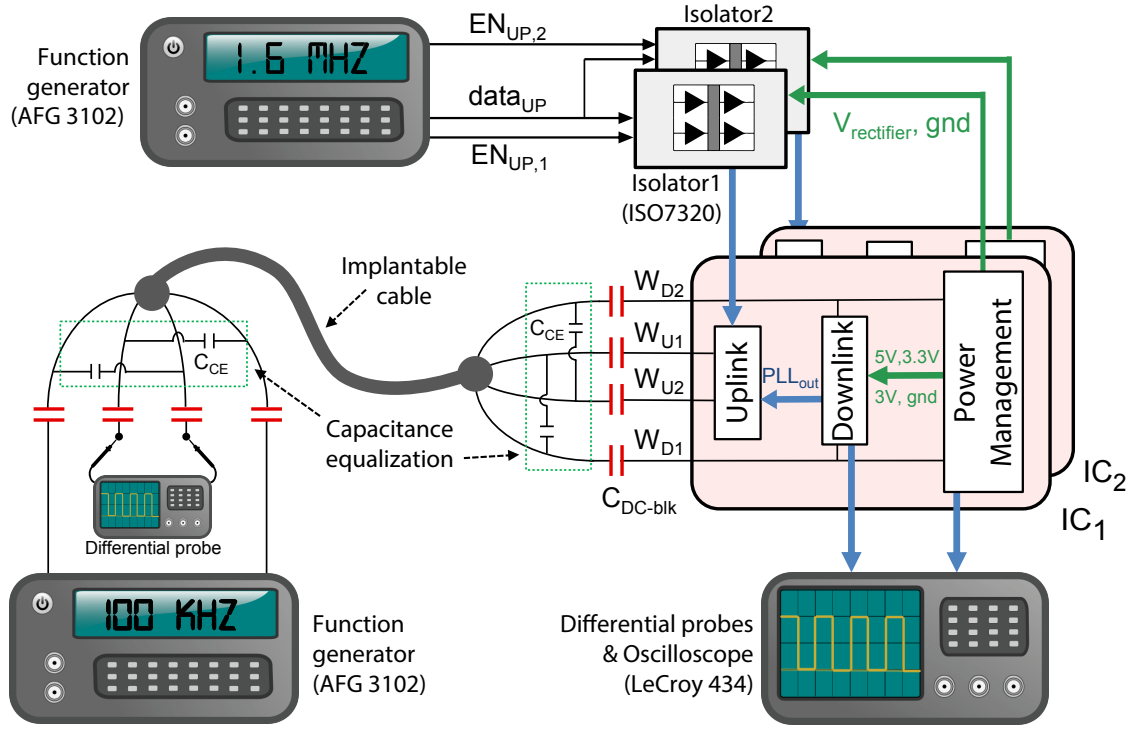


Figure 4.9: Experimental setup used for device testing and measurements.

code). The PLL, driven by clk_{down} , locks to the correct frequency of 1.6 MHz (i.e. the signal PLL_{lock} remains high).

- (2) The frequency of V_{down} is changed to 50 kHz; This represents a downlink data with alternating bit pattern in Manchester encoded data (01010101...), and is correctly recovered by the CDR while at the same time the PLL remains in the locked condition. In both measurements the ripple on the rectified 5 V is 200 mVpp.

A load of 120 k Ω (27 μ A) and 100 pF was added to V_{reg1} (connected to CDR) to model the load and parasitics of the core circuits within the optrode. A load of 50 k Ω (60 μ A) and 220 pF was added to V_{reg2} (connected to PLL) for the same reason. Therefore, the total current taken from the chest implant is 178 μ A per optrode including the standby current consumption of the 4WiCS IC itself.

The transient voltage spikes on V_{reg1} are up to 1.3 V_{pp} with a duration of almost 100 ns and happen during each voltage transient on clk_{down} . The V_{reg2} has spikes with up to 600 mVpp at 1.6 MHz frequency due to switching activities within PLL. The spikes decays within almost 100 ns.

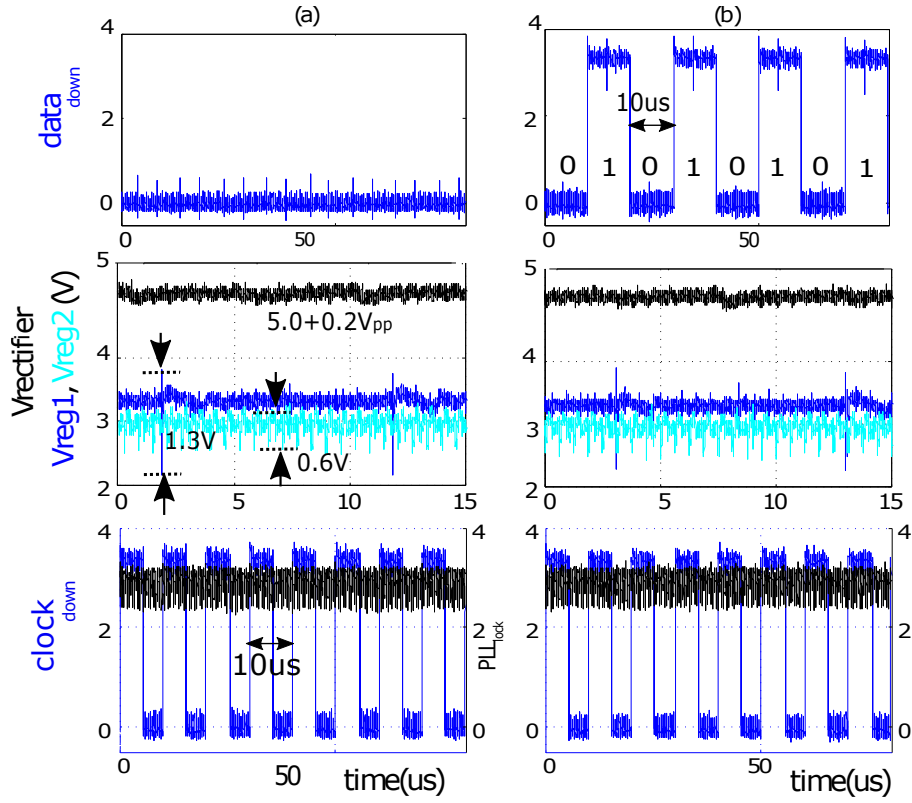


Figure 4.10: Measured waveforms at the power management and downlink blocks of the 4WiCS ASIC when (a) V_{down} at 100 kHz was sent through W_{D1} and W_{D2} to the 4-wire interface; (b) the frequency of V_{down} was changed to 50 kHz representing alternating data pattern.

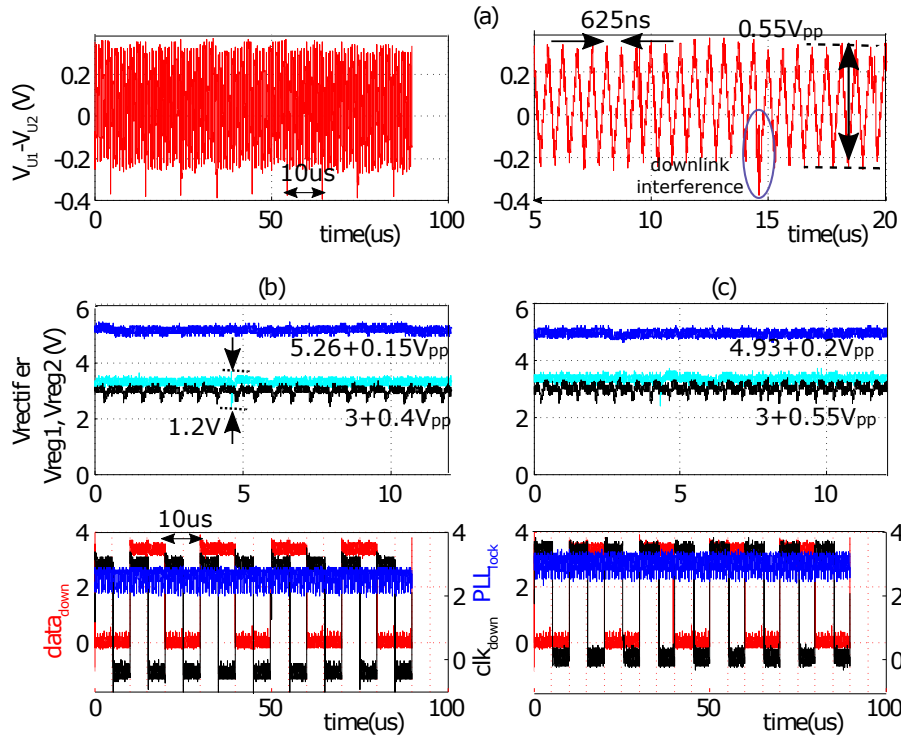


Figure 4.11: Measured waveforms when uplink and downlink are simultaneously active. (a) The received uplink, $V_{U1}-V_{U2}$ at 1.6 MHz, while IC_1 drives the uplink; On the right, the magnified version of the same waveform is shown. (b) The voltages at different nodes on IC_2 . (c) Same voltages on IC_1 .

Uplink Communication

The uplink communication was tested using two 4WiCS ASICs (IC_1 and IC_2) connected in parallel to the 4-wire lead, emulating simultaneous communication with two satellite modules. To study the effect of using different uplink clock frequencies, two experiments were run:

- In the first experiment the internal uplink clock frequency of 1.6 MHz was employed, thus the PLL_{out} was used to drive the signal $Data_{up}$. The measured waveforms of downlink, power management, and uplink are shown in Figure 4.11. Here the frequency of V_{down} was set to 50 kHz and the PLL_{clk} was used to drive the uplink on IC_1 , while the uplink on IC_2 was disabled. In order to ensure no errors were present on the downlink communication while testing the uplink communication, a Bit Error Rate (BER) measurement was performed. Results show the downlink data and clock are correctly recovered in both devices. The BER was measured during a 15-hour test (i.e. 2×10^8 data samples) on both IC_1 and IC_2 , and no bit error was found.
- In the second experiment, a function generator was used to provide a different clock. A digital isolator (ISO7320C) per optrode was used to drive the uplink enable and data signals (UL_{EN} and UL_{data}) from a function generator while keeping the supply and ground domain of the function generator and the 4WiCS ASIC decoupled. The isolators were powered through the voltage rectifier; V_{down} amplitude was increased to accommodate for the extra load and ensure 5 V at rectifier output. The differential uplink waveform received at the chest implant end of the lead was measured at different $Data_{up}$ frequencies, 500 kHz and 1 MHz. Measurements were taken with an active differential probe and displayed on an oscilloscope. Results are shown in Figs.4.12-(a) and (b). Although the amplitude of the received waveform does not settle to V_{up} (i.e. 3 V), it has a peak-to-peak amplitude of 0.85 V at 500 kHz and 0.55 V at 1 MHz, and can be easily detected at the chest implant.

In both experiments, the voltage V_{ref} on the uplink circuit was tied to V_{reg2} . The effect of uplink activity on the rectifier output is shown in Figure 4.12-(c); The average value of the rectified voltage on IC_1 drops by 225 mV and 112 mV during uplink activity on IC_1 and IC_2 ,

respectively. The latter is due to the increased voltage drop on D1 and D2 wires due to their resistance. At the same time, the CDR recovers the data and clock correctly from downlink (Figure 4.12-(d)). The PLL however oscillates between lock and unlock conditions which could be attributed to the effect of large voltage spikes on the rectifier output. These are due to the transient activities of the isolator IC during the transitions of the $EN_{UP,1}$ and $EN_{UP,2}$.

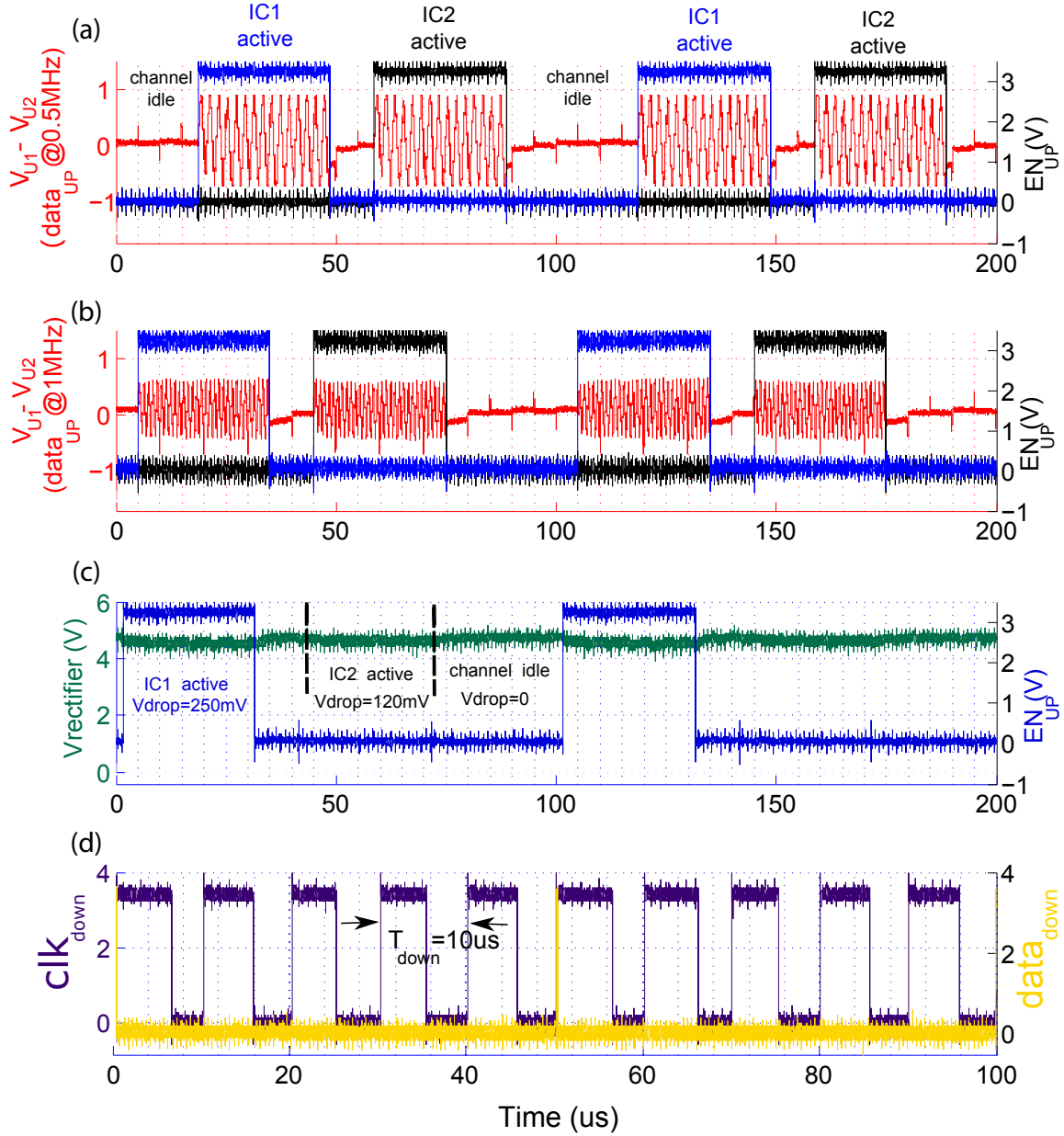


Figure 4.12: Measured waveforms of the 4WiCS power management, downlink, and uplink circuits when two ICs are connected in parallel to the Cooper cable. (a) Received $V_{U1} - V_{U2}$ when $Data_{up}$ is at 500 kHz; Two non-overlapping EN_{up} signals enable the uplink on two ICs; (b) same signals when $Data_{up}$ is at 1 MHz; (c) the rectifier output and uplink enable $EN_{up,1}$ of IC₁ during uplink activity; (d) the recovered clk_{down} and $data_{down}$ during uplink activity.

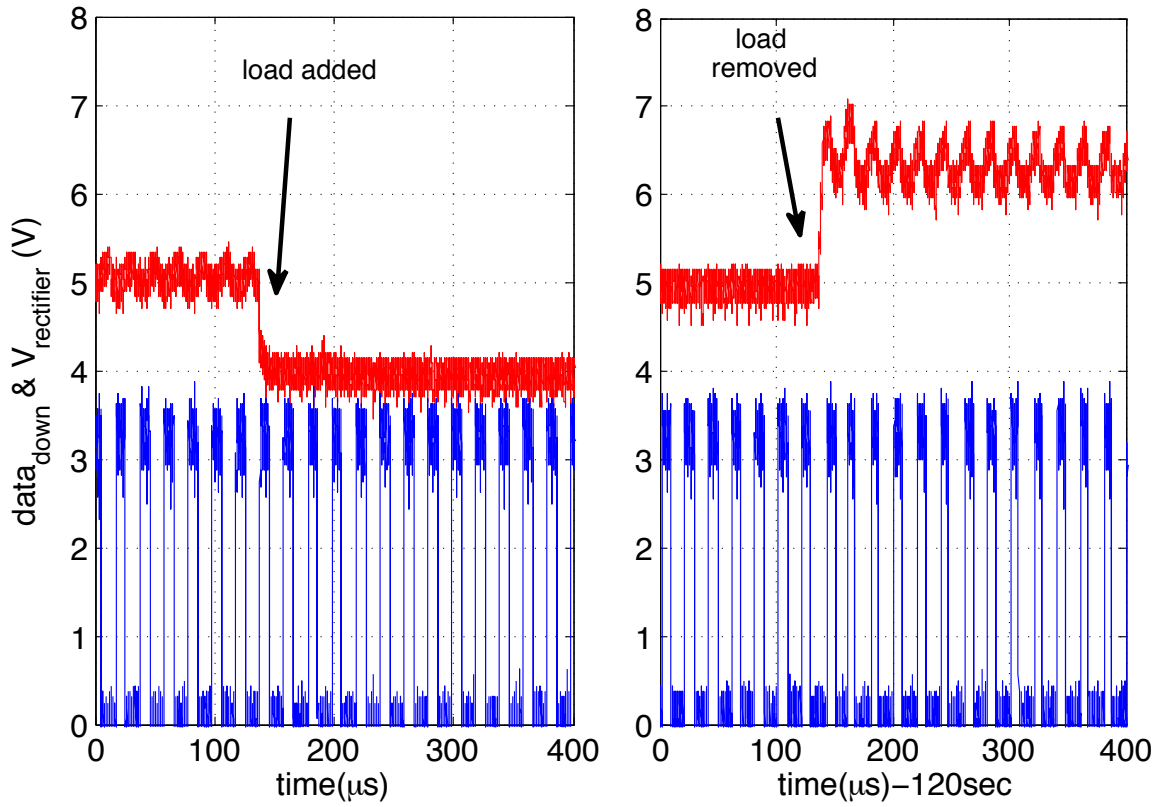


Figure 4.13: The emulated effect of LED stimulation on the recovered data and the rectifier voltage: Left: A load of $2.7\text{ k}\Omega$ ($\sim 1.8\text{ mA}$) added to the rectifier output; right: The load is removed after 120 s; the ripples on the rectifier decay within $80\text{ }\mu\text{s}$. During the two load changes, V_{down} was increased to increase the rectifier output voltage to 5 V.

Stimulation Effect - Load Fluctuation

One of the core functions of the optrode circuits is to drive the LED stimulation. These are turned on or off depending on whether the stimulation is required or not. From a power management perspective, the LEDs and stimulation drivers form a variable load that toggles from an off (no current through LED) to an on state (adjustable current through the LED).

To evaluate the effect of LED stimulation on the 4WiCS power management circuits, an abrupt change in the load of the rectifier was emulated. In particular, it is important that the downlink/power signals are not significantly impacted by the fast current change and that downlink commands ($\text{Data}_{\text{down}}$) are correctly recovered while in stimulation mode. To verify this, a resistive load of $R_{\text{Stim}} = 2.7\text{ k}\Omega$ ($\sim 1.8\text{ mA}$) was switched on and (after almost $120\text{ }\mu\text{s}$) off at the rectifier output. Figure 4.13 shows the variation of the rectifier output during the load switching. When the load is inserted or removed the output voltage of the rectifier changes by almost

1 V. Part of this is due to the voltage drop on the Cooper cable ($R_s \times 1.8 \text{ mA} = 0.57 \text{ V}$) and the rest (0.43 V) is due to the voltage drop on the rectifier. The latter is due to the use of the diode-connected thick-oxide PMOS devices in the rectifier which have relatively high threshold voltage and small transconductance (i.e. high resistance). In between the two transitions, the V_{down} at the chest side of the lead was increased manually to maintain 5 V at rectifier output. The manual tuning is to emulate the automatic and dynamic adjusting of V_{down} . The recovered $Data_{down}$ is not affected by the load switching, indicating the correct operation of downlink during the stimulation phase. This test has confirmed the need for an adaptive power transfer technique, such that the voltage drop on the cable due to increased load current is compensated in real-time from the CI end. This will be discussed in Section 4.4.

4.3 Communication Channel - Lead Characterisation

The choice of the communication channel is informed by the need for a fully implanted wireline system, which requires a subcutaneous lead with suitable mechanical and electrical characteristics. In fact, when implanted, the cable is subject to external agents on its path from the chest to the brain, hence to risk of corrosion and breakage. For this reason, an implantable, medically-approved lead is chosen to serve as a communication link: the **Cooper Cable** [166].

As shown in Figure 5.4(a), the 4 wires are arranged in a parallel coil-based structure: each conductor, made of a platinum-iridium Pt-Ir alloy, is a helix that rotates around a central tube made of silicon rubber and polyimide varnish and is covered by a coating of the same insulator material. The conductor's pitch is maintained constant along the whole length of the cable. This particular design is chosen both for mechanical and electrical reasons. Mechanically, the helix configuration provides the lead with resistance to crushing (vertical stress) and allows for high level of stretching, twisting, and bending (horizontal stress) without damaging the cable and without altering the distance between the conductive coils. From an electrical perspective, the parallel configuration of multiple wires gives the possibility to overcome the lack of electrical shielding (typically not employed in implantable leads) by transferring signals differentially.

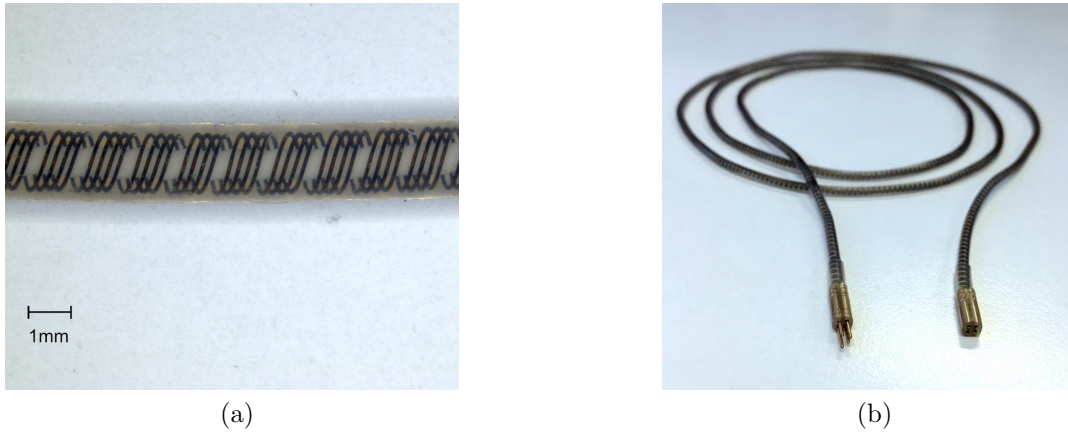


Figure 4.14: Pictures of the Cooper cable showing the helix configuration of the 4 wires.

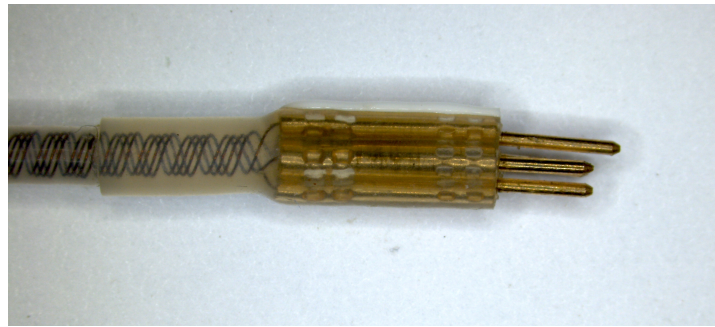


Figure 4.15: Termination of the Cooper cable – the Creggs connector.

Therefore, this allows to remove the effect of the common-mode noise and limiting the interference. Nonetheless, the main drawback of a coil structure is the increased electrical resistance per unit length, which in turn causes an increase in the power dissipation on the wires.

4.3.1 Cooper Cable Electrical Model

Electrical characterization of the lead was performed on a 77 cm long 4-wire Cooper cable supplied by Finetech Medical Ltd. The single-wire impedance measurements were performed with Keysight E4980A/AL Precision LCR Meter in a frequency range including frequencies employed in downlink (100 kHz) and uplink (up to 1.6 MHz). Since the transmitted signals are square waves, the frequency range is larger than the one considered for the characterization of the cable, as it includes the higher frequency harmonics. It is however assumed that the power density of the higher harmonic components of the square wave signals is negligible for such characterization, therefore a simplification is made by evaluating the first harmonic only.

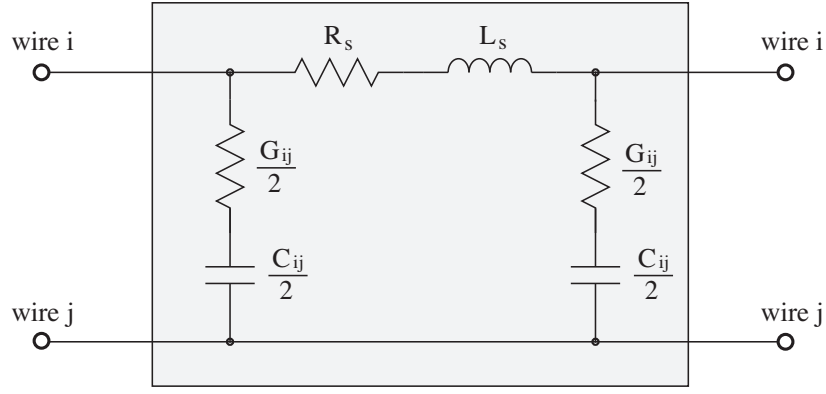


Figure 4.16: Lumped Π model of the Cooper cable used in the lead characterisation.

A 2-port network characterization of the lead is performed in air between each pair of wires within the 4-wire lead. All 6 different pair combinations were measured. During each measurement the conductors not in use were kept open on both ends, i.e. left floating.

A lumped element Π model is defined (Figure 4.16) to represent the line parameters. A lumped model is chosen over a distributed model because the required length of the implanted cable, l_{cable} is significantly smaller than the wavelength of the signal. The line parameters (valid for a 77 cm Cooper cable) are therefore derived from the discrete element model by measuring 3 impedances: (1) the *equivalent impedance* Z_i for each single wire; (2) the *short-circuit impedance* Z_{sc} ; and (3) the *open-circuit impedance* Z_{oc} for each combination of two wires (6 different two-port network combinations). Z_{sc} is measured on one end of a single two-port network when at the other end the two wires are shorted with each other (the other two wires are left open and floating), whereas Z_{oc} is obtained by measuring one end and leaving the two wires at the other end open (the remaining two wires are left open and floating). The series resistance R_s and inductance L_s are derived from the real and imaginary parts of Z_i (Eqns. 4.1). The dielectric capacitance C_{ij} and the dielectric conductance G_{ij} between each pair of wires are extracted from the measured Z_{sc} and Z_{oc} using Eqns. 4.2 and 4.3.

$$Z_i = \frac{R}{2} + j\pi fL \quad (4.1)$$

$$Z_{sc} = \left(\frac{G}{2} - \frac{j}{\pi fC} \right) \parallel (R + j2\pi fL) \quad (4.2)$$

$$Z_{oc} = \left(\frac{G}{2} - \frac{j}{\pi f C} \right) \parallel \left(R + j2\pi f L + \frac{G}{2} - \frac{j}{\pi f C} \right) \quad (4.3)$$

The model parameters are summarised in Table 4.4. For each parameter, both the average value and its variation among the wires within the same category (i.e. adjacent, non-adjacent) are given. For example, the R_s and L_s of each wire are within 1 % of the average resistance and inductance of all wires and remain so by increasing the frequency to f_{up} . The 2-port related parameters instead depend on the choice of the two wires: the adjacent wires have almost 25 % higher C_{ij} compared to the non-adjacent ones. The extracted parameters are almost frequency-independent except for G_{ij} . The frequency-dependency of G_{ij} and C_{ij} may be attributed to the approximation made in the lumped model compared to a distributed model.

Capacitance Equalization Network

The lead parameters that affect the efficiency of the power and data transmission are: (1) the series resistance, R_s , that causes the thermal energy loss and the $R_s I$ drop; (2) the parallel capacitance, C_{ij} , which causes dynamic power loss between each pair of wires. To minimise the dynamic power loss on the lead, a non-adjacent pair of wires was chosen for power/downlink transmission – i.e. W1 and W4, as C_{14} is slightly smaller than C_{13} and C_{24} . However, any asymmetry between the C_{ij} from the uplink wire, U1 (or U2), to the two downlink wires, D1 and D2, induces an undesired squarewave voltage at the frequency of f_{down} on U1 (and U2). The peak-to-peak of the induced voltage (measured differentially between U1 and U2) is as high as 4 V depending on which pair of wires are chosen for uplink/downlink. For example,

Table 4.4: Measured lumped Π model parameters of 77 cm Cooper cable in air

Parameter	Unit	100 kHz	1.6 MHz
R_s	Ω	313 ± 3	310 ± 3
L_s	μH	3.59 ± 0.05	3.59 ± 0.05
C_{ij} , adjacent*	pF	118 ± 2.4	122 ± 2.5
G_{ij} , adjacent	mS	19.2 ± 0.5	29.3 ± 1.2
C_{ij} , non-adjacent	pF	89 ± 1.3	92 ± 1.5
G_{ij} , non-adjacent	mS	22.5 ± 0.7	27.3 ± 0.4

*Adjacent wires: W1-W2, W2-W3, W3-W4.

when W1 and W4 are used for downlink, the differential peak-to-peak voltage induced on W2 and W3 (i.e. uplink wires) is 2.1 V.

To mitigate this, a capacitive equalization network is added such that the total capacitance from U1 (or U2) to D1 becomes equal to the total capacitance between U1 (or U2) to D2. The optimum equalization (i.e. maximum reduction of the induced voltage on U1 and U2) was achieved in the experiments when two similar sub-networks were placed at either end of the lead instead of one network on one end (Figure 4.9). This could be attributed to the use of the relatively long lead where the measured induced voltage on the head side of U1 and U2 is in fact the collective effect of interference that happened along the whole length of the wire. Therefore, it can be fully equalised using a distributed (in this case, two) equalization network rather than a single lumped network. Each sub-network includes two capacitors, C_{CE} . Adding an external capacitor between a single pair of wires affects the total capacitance between all other pairs as well. The minimum C_{CE} to equalise the capacitance between the uplink and downlink wires was found from impedance measurements to be 27 pF. By adding the equalization network, the average of the total capacitance between one of the uplink wires (U1 or U2) and one of the downlink wires (D1 or D2) increases to 147 pF, while their variation from the average value remains at ± 2 pF. The parallel capacitance measured between the two downlink wires, D1 and D2, increases to 121 pF.

Electrical properties limitations

Because of the rather high resistance value R_s ($313 \pm 3 \Omega$), the voltage drop across the cable would be more than 6 V when a peak current of 20 mA is required at the brain implant end – worst-case scenario. In this case, the power transfer efficiency will be less than 50% with more than half of the power being dissipated as heat, creating possible temperature raising issues in the body, besides drastic reduction of battery life at CI end. For this reason, a second version of the Cooper cable was created in collaboration with Finetech Medical Ltd: differently from the first version, each conductor on the new lead is based on a metallic core made of silver (28% of its cross-sectional area), with a Pt-Ir (90-10) sheath around it which helps to maintain its

mechanical properties. The electrical properties, on the other hand, are significantly improved, by decreasing the resistance of the conductors from $55\ \Omega/m$ to $11\ \Omega/m$, thus helping to reduce the voltage drop across the cable by 80%. As this cable was not available and fully characterised at the time the tests and experiments described in this report were performed, the first version of the Cooper cable has been employed for them.

4.4 Central Module - PCB Interface Design and Test

The work shown in this section has been accomplished in collaboration with Mr Andrea Mifsud during his MSc project at EEE Department of Imperial College London. Mr Mifsud's project was co-supervised by Mr Dorian Hacı (Ph.D. thesis author), Dr Sara Ghoreishizadeh, Dr Yan Liu, and Dr Timothy Constandinou. A conference paper was published in BioCAS 2017 Proceedings [32]. The contribution of the author of this thesis has been in establishing the high-level system architecture and in supervising the MSc student, who was the lead designer of the hardware and software components.

The role of the central module at the CI end is to (1) power the optrodes at the brain implant (satellite modules), (2) retrieve and process the data received from neurosignal recording, and (3) control the optrodes with commands sent to them through the communication channel. The chest implant is also responsible for communication with devices outside the body, which function as external systems and data monitoring and battery charging units, as well as for implementing medical and electrical closed-loop control algorithms to perform the optogenetic treatment. The work presented in the following is focused specifically on the interfacing between the chest implant and the brain implant. The implementation of the *4WiCS chest implant interface* is described, discussing moreover techniques to add adaptive functionalities and improve performance of the power transfer and data communication.

In order to be able to bidirectionally communicate with the brain implant through the 4WiCS protocol, the chest implant needs to include a 4WiCS CI interface that complies to the specifications listed in Table.4.1, both for downlink and for uplink. Moreover, given (1) the power

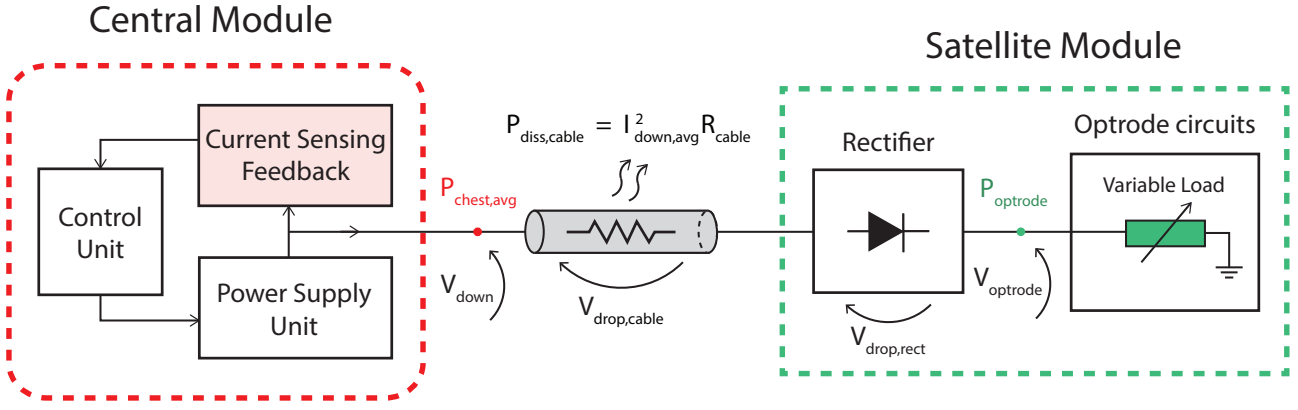


Figure 4.17: Adaptive closed-loop power delivery method.

requirements set by the optrode core circuitry, (2) the performance of the 4WiCS brain implant interface (the 4WiCS ASIC), and (3) the electrical characteristics of the Cooper cable, the 4WiCS CI interface has to ensure enough power is provided at the BI end, as well as correct voltage levels are maintained in every condition. By knowing the voltage drop on the AC/DC converter in the 4WiCS ASIC and by evaluating the IR voltage drop on the communication channel, the driving voltage to be generated at CI end is calculated:

$$V_{down} = V_{optrode} + V_{drop,rect} + R_{cable}I_{down,avg} \quad (4.4)$$

where $V_{optrode}$ is the output of the rectifier that needs to have an average of 5 V for LED stimulation; $V_{drop,rect}$ is the voltage drop across the rectifier; R_{cable} is the resistance of the downlink wires W_{D1} and W_{D2} of the Cooper cable; while $I_{down,avg}$ is the average of the absolute current flowing through W_{D1} and W_{D2} . Since the voltage on each differential wire has a square waveform, the average transmitted power from the chest, neglecting the rise/fall time of the squarewave, is:

$$P_{chest,avg} = V_{down}I_{down,avg} \quad (4.5)$$

Such power depends on the average current $I_{down,avg}$. This is however not fixed because the current required at the brain implant is variable due to the optical stimulation function. The latter is active only when stimulation is required, thus demanding a dynamic stimulation current that makes in fact the brain implant core circuitry a variable load.

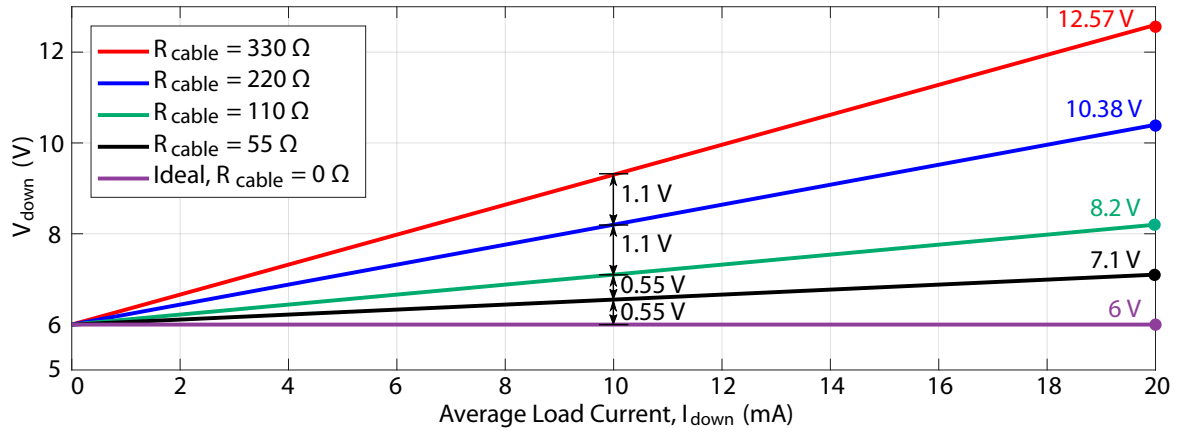


Figure 4.18: V_{down} vs. I_{down} for different values of R_{cable} .

To provide the brain implant circuitry with the correct constant voltages at any time, a new method is proposed herein that adaptively regulates the power within the chest implant through closed-loop feedback, as shown in Figure 4.17. By continuously sensing the current flowing through the implantable cable, the IR drop across the cable can be calculated in real-time and compensated for. Accordingly, the V_{down} voltage can be dynamically adjusted, based on the instantaneous load, $I_{down,avg}$, to ensure that a constant voltage level is received at any time by the satellite module. As a result, the power loss in the delivery process is exclusively due to the IR drop across the wired link. This method can easily be extended to multiple optrodes, provided that such satellite modules have similar load characteristics to each other. In this case, the current measured by the feedback path corresponds to the sum of the load currents of all the optrodes, with the voltage received being common to all modules.

4.4.1 Circuit Design and Implementation

A *4WiCS chest implant interface* prototype (gen1) has been designed to achieve both full-duplex communication and CI-to-BI power transfer, with capabilities to interface with the Cooper cable. It receives commands and data packets through an asynchronous serial connection, UART, from a PC-based graphical user interface (GUI) and updates the downlink and uplink modules as necessary by means of a digital controller.

The hardware system is based on Printed Circuit Board (PCB) technology and is physically

divided into 2 subsystems: a digital control unit based on a field-programmable gate array development board, and a custom-made PCB including all the interfacing circuits. Such interfacing circuits are grouped into four main blocks: (1) power management; (2) downlink drivers; (3) feedback; and (4) uplink receivers. The top-level architecture of the circuit implementation is illustrated in Figure 4.19.

Power Management

The instantaneous voltage V_{down} , required to maintain a constant 5 V supply for the satellite modules in the brain implant, is dependant on the current flowing through the communication link. From Equation 4.4, by knowing the voltage drop on the rectifier at the BI end ($V_{drop,rect} \approx 1$ V), such voltage can be derived by measuring the current I_{down} :

$$V_{down} = 5\text{ V} + 1\text{ V} + I_{down}R_{cable} = 6\text{ V} + I_{down}R_{cable} \quad (4.6)$$

Considering different values for R_{cable} , Equation 4.6 yields the characteristics illustrated in Figure 4.18. These show that the choice of cable is critical since this directly affects power losses in the communication link and thus the efficiency of the end-to-end system. For an R_{cable} of $220\ \Omega$, an off-the-shelf DC/DC converter was chosen (LTC3130) so as to be able to supply a voltage (at the CI side) of between 6 V and 10.5 V from a 5 V supply. The output voltage of this boost converter is set by a potential divider connected to the output pin (V_{down}), feedback pin, and ground. In our system, this is provided through digital potentiometers that are controlled by the FPGA. Three $200\text{ k}\Omega$, 32-tap, digital potentiometers are here connected in series, ensuring a high resistance to minimise power consumption.

Downlink Drivers

This was implemented by using four SPST (2 NO, 2 NC) switches, S1 to S4 (available in one package as the MAX4679), connected as one SPDT switch per pair (1 NO, 1 NC) with inverted input connections (V_{down} and GND). Alternating between V_{down} and GND, these switches

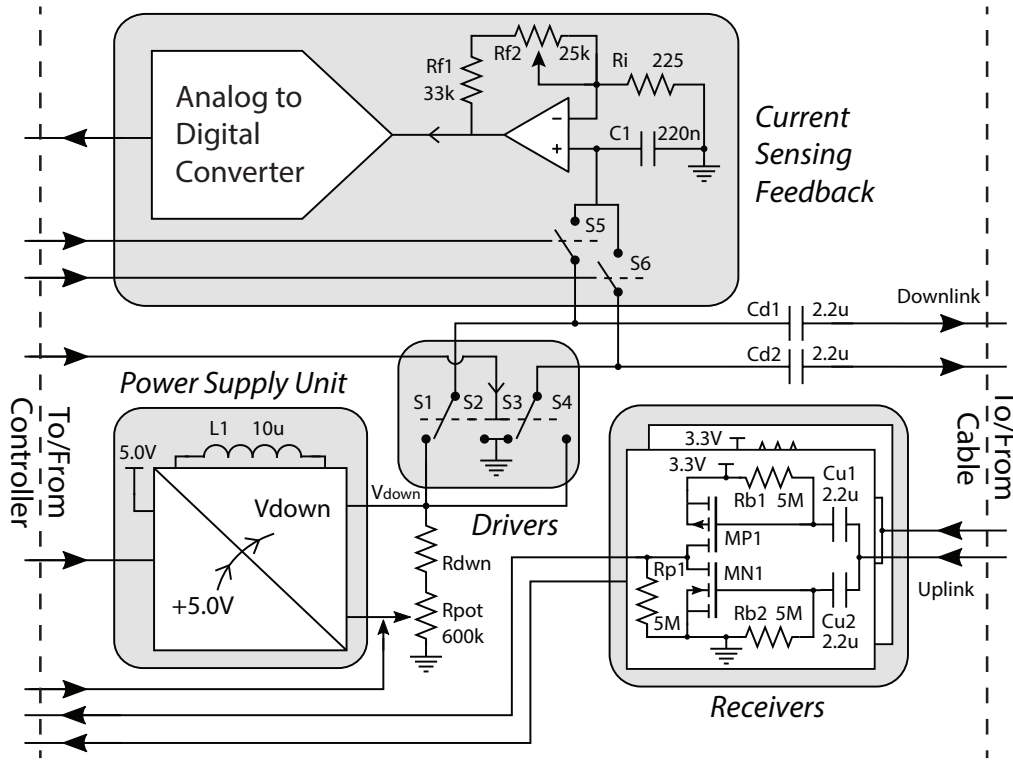


Figure 4.19: Top-level circuit schematics for the power management and data communication interface within the chest implant – 4WiCS chest implant interface.

deliver concurrent power and Manchester encoded data (at 100 kbps) through the cable. To reduce the power losses at the chest implant it is important to have switches with a very low on-resistance. Also, break-before-make circuitry is essential, to ensure that the normally closed switch is disconnected before connecting the normally open switch (and vice-versa). This is required to avoid an instantaneous short circuit at the transitions (i.e. V_{down} and GND).

Current Sensing Feedback

To be able to adjust V_{down} depending on the load current, a current sense circuit is required. This is usually achieved by measuring a voltage drop across a current sense resistor placed in series with the load, resulting in additional loss of power. In this case, however, the voltage drop across the on-resistance of the switches was measured instead. To avoid dealing with high voltages, low-side current sensing was implemented. This required two SPST switches (S5 and S6) in order to multiplex the driver output that is connected to ground. The switch outputs are then sampled by a hold capacitor, and an amplifier to make use of the full-scale input

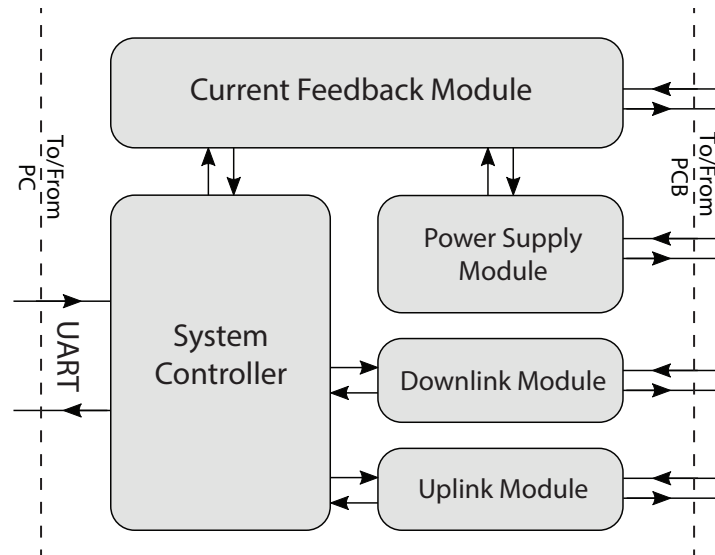


Figure 4.20: Digital control unit implemented on the FPGA.

range of the ADC. The value for the hold capacitor was set so as to reduce the voltage droop from leakage currents, limit the change in voltage from charge injection, and to ensure that the capacitor charges to the set voltages within the available minimum time.

Uplink Receivers

For the uplink receiver, a CMOS inverter is used for each wire to be able to monitor each line separately. The gate of each MOSFET is biased at either 3.3V or ground to make sure that both MN_x and MP_x are off during idle operation – i.e. no activity on uplink. Therefore, for a valid output value during idle operation (as both transistors are off), a pull-down high-value resistor is connected to the output of the inverter. During normal operation, the received uplink signal is superimposed on the DC gate voltage by a capacitor. The inverter then converts this signal to an LVCMOS33 digital signal which is then processed by the FPGA to decode the data received.

Digital Control Unit

This was implemented in VHDL on an IGLOO Nano FPGA board (AGL250V2-VQG100 Starter Kit) consisting of several modules to control and monitor each part of the system based on the

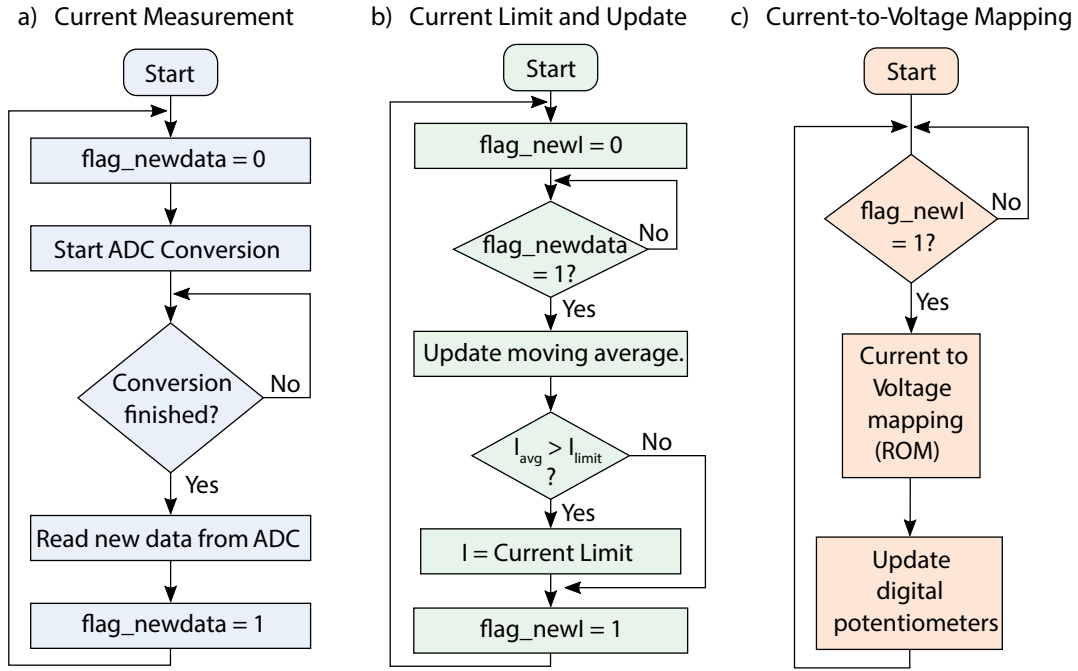


Figure 4.21: Digital control algorithms for evaluation and feedback (implemented as a finite state machine on FPGA).

commands received through UART. During normal operation, voltage regulation is achieved by first requesting a new acquisition from the ADC to sample the current flowing through the cable. Once the new sample is received, an 8-sample moving average is updated, and the result is mapped to a voltage by a ROM which stores this mapping based on specific parameters of the system. This voltage is then converted into a number of taps, for the digital potentiometers to be updated, thus updating V_{down} . For data communication, data is sent to the optrodes at the BI end by controlling the drivers as required, and any new data received from the optrodes are sent through UART. During idle operation, the downlink drivers are switched at a frequency of 100 kHz to keep transmitting power while sending a logic low.

Graphical User Interface

A GUI has been implemented in LabVIEW (Figure 4.22). This can communicate with the system via the available UART port connected to the FPGA. It provides (1) high-level commands for operating the system controlled in the FPGA and (2) monitoring features for displaying the voltage V_{down} and load current I_{down} .

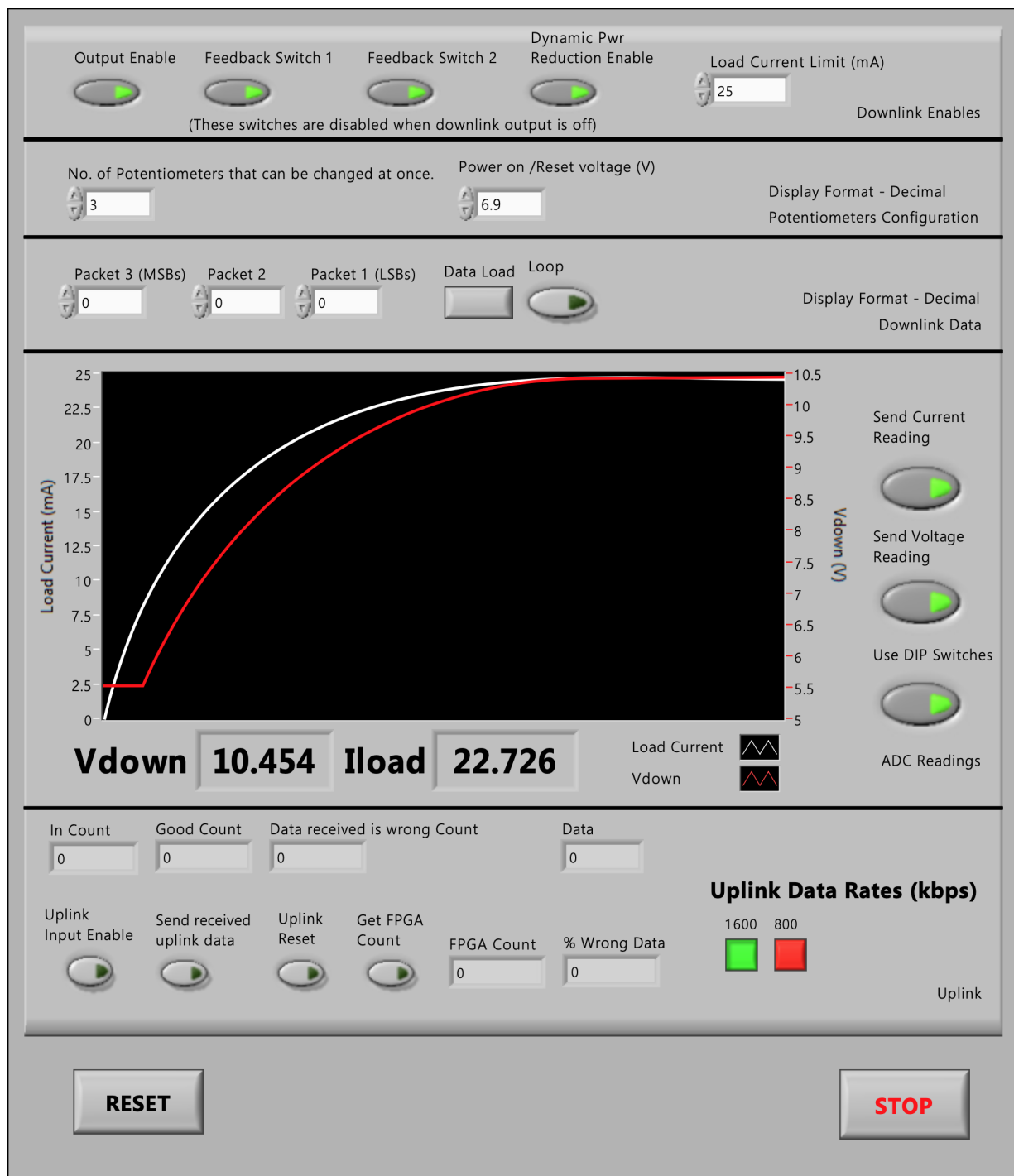


Figure 4.22: The graphical user interfaces developed using the LabVIEW design software.

4.4.2 Testing and Measured Results

The CI power delivery and downlink data communication was tested for various load conditions and V_{down} values using a dummy resistive load, as shown in Figure 4.23. Two tests were carried out, one to determine the efficiency of the PCB-based central module and another for the worst-case step-response of the system. Key system specifications are summarised in Table 4.5.

The measured results for efficiency are shown in Figure 4.24. This demonstrates that the efficiency increases when V_{down} decreases and(/or) when the load current I_{down} increases. The main loss in the system is found to be dynamic power dissipation of the downlink drivers, measured at 8.6 mW for V_{down} of 6 V, and increasing by an order of magnitude at 10.4 V. The stability of the system was tested by applying a step in I_{down} of 22 mA as illustrated in Figure 4.25. Initially, the current settles at approximately 13 mA, increasing linearly as V_{down} increases to compensate for the voltage drop on the cable, until the current measurement saturates at 20 mA. Thus, the measured worst-case settling time of the system is 1.5 ms.

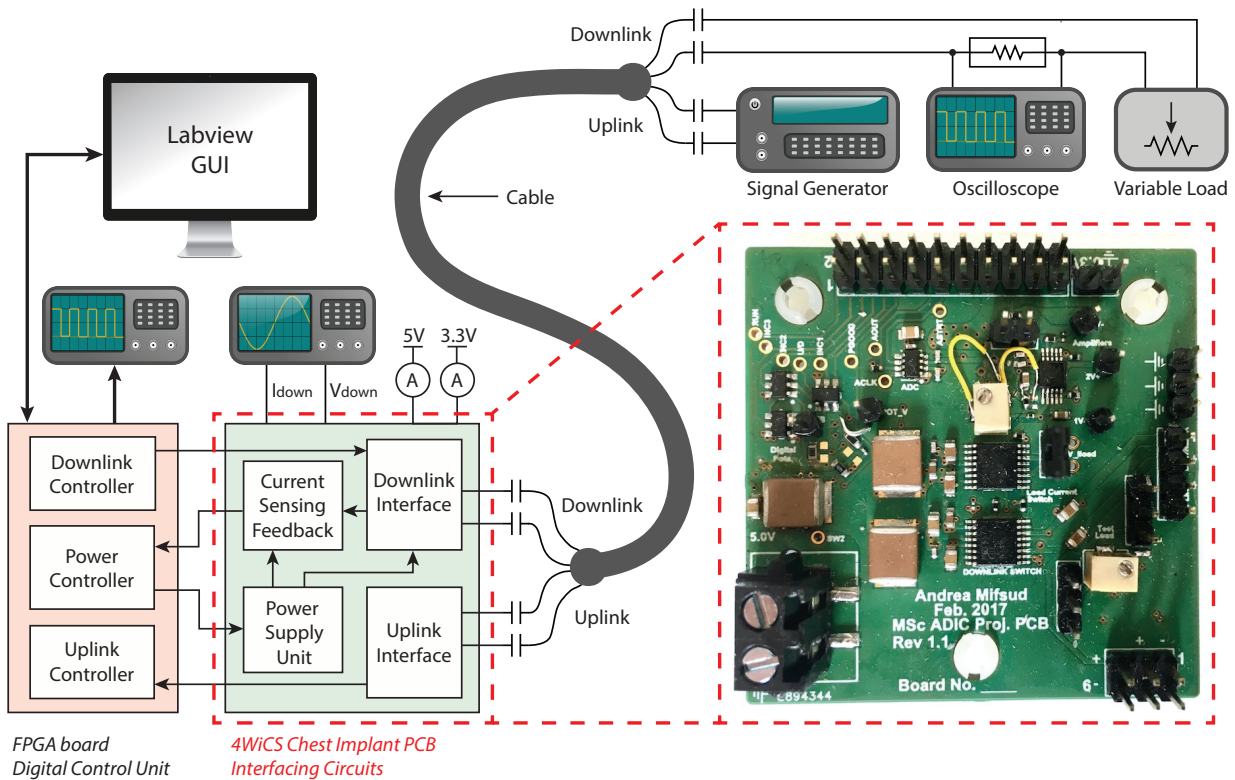


Figure 4.23: Experimental setup and PCB prototype of the 4WiCS chest implant interface.

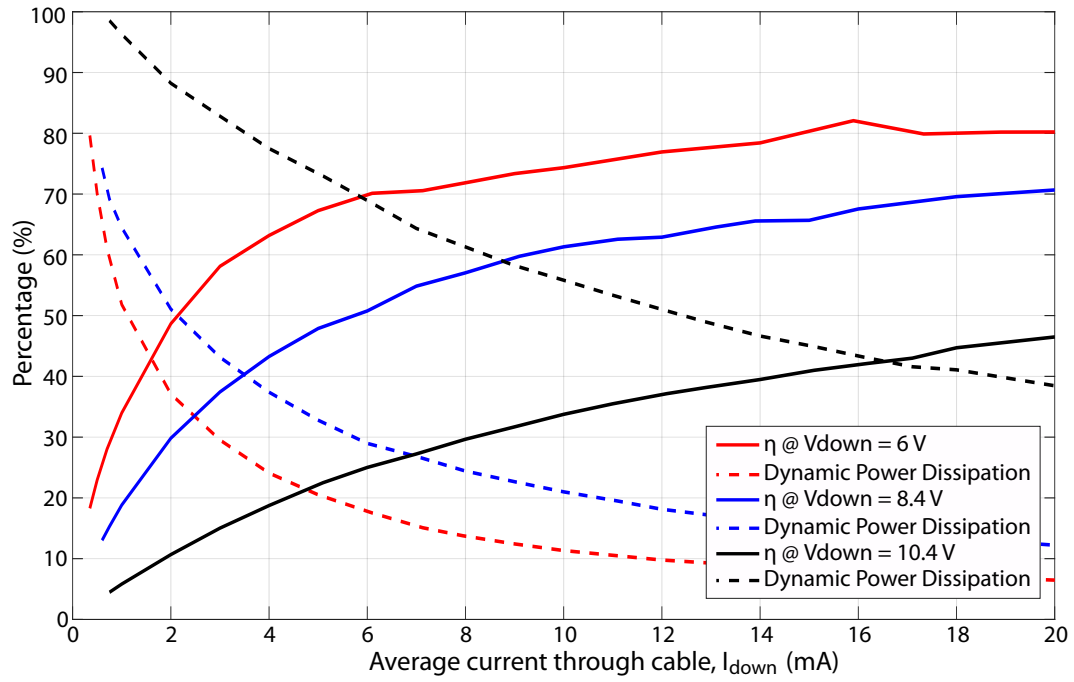


Figure 4.24: System efficiency for different values of V_{down} , and load current.

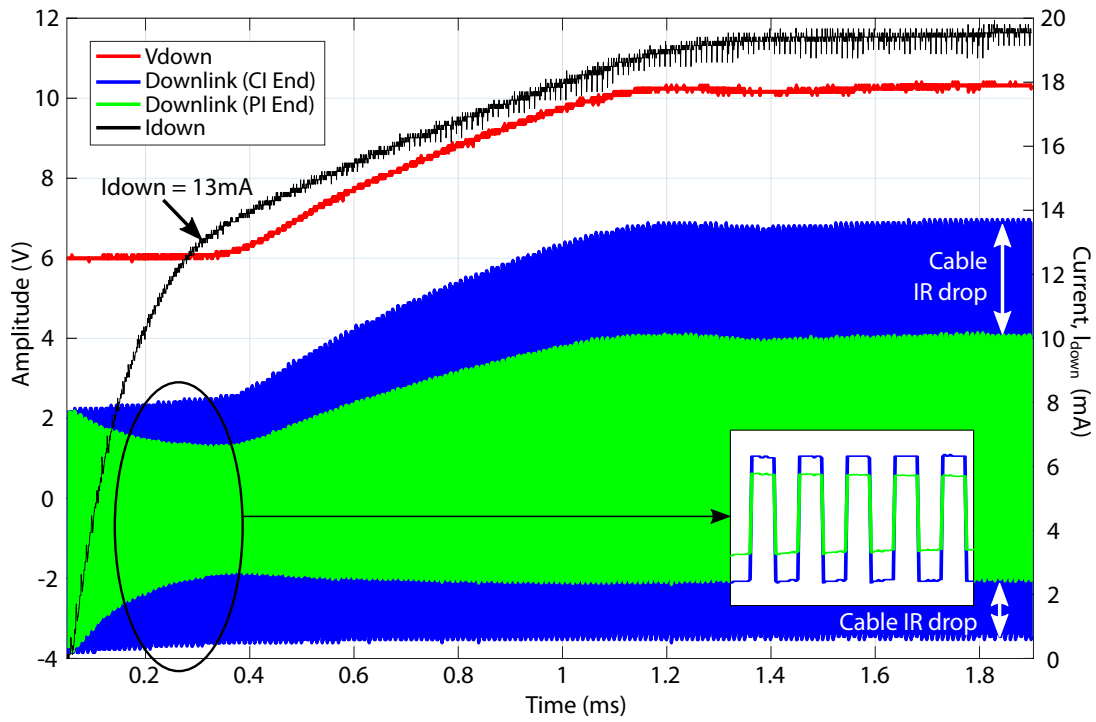


Figure 4.25: System step response. $I_{down} = 22\text{ mA}$ at $V_{down} = 10.4\text{ V}$, $RL = 470\ \Omega$

Table 4.5: Achieved System Specifications

Function	Parameters	Value
Power Management	$V_{in}, I_{down,max}$	5 V, 20 mA
	$V_{down,min}, V_{down,max}$	5.5 V, 10.4 V
Current Sensing Feedback	$F_s, Resolution, t_{s,max}$	100 ksps, 8 bits, 1.5 ms
Downlink Driver	AVDD, DVDD	5.5-10.4 V, 3.3 V
	$t_r, t_f, Datarate$	250 ns, 100 ns, 100 kbps
Uplink Receiver	DVDD, Data-rate _{max}	3.3 V, 1.6 Mbps

4.5 Summary

This chapter has presented the design and implementation of the 4-Wire Communication System – an in-body interfacing allowing for multiple satellite modules within an implantable system to bidirectionally communicate with a central module and to receive power supply from an energy source located at the central module. The 4WiCS interface has been developed to be compatible with the CANDO implant system, which comprises a chest implant, housing a battery and a processing unit, and a brain implant with multiple modules, optrodes, capable of interacting with the biological tissue through recording and stimulation. Two interfaces have been presented which enable the use of the full-duplex 4WiCS protocol and CI-to-BI power delivery – the 4WiCS BI interfaces (within the satellite module) and the 4WiCS CI interface (within the central module). The former was implemented in form of a CMOS-based ASIC, while the latter was implemented with a PCB-based system. The circuits of both interfaces have been tested, characterised, and presented. Also the implantable lead connecting the two implants, the Cooper cable, has been electrically characterised and introduced in this Chapter.

Measurement results demonstrate the capabilities of the PCB-based CI interface to reliably generate and transfer power through the implantable lead, by providing adaptive power delivery as well as full-duplex data communication. The proposed power management system can deliver up to 120 mW power at the BI end, superimposed on a phase-encoded serial bitstream with datarate of 100 kbps (downlink). The maximum efficiency achieved for this implementation is 80 %, with the dynamic power dissipation of the drivers being the dominant source of power

loss across all load current ranges. A worst-case recovery for a 6 V constant supply at the BI end takes 1.5 ms for a step of 22 mA. Uplink communication is achieved at a maximum data rate of 1.6 Mbps.

Testing of the 4WiCS ASIC shows the interface can recover an unregulated 5 V (from rectifier) and a regulated 3.3 V (from regulator) supply thanks to the on-chip power management circuits. The required full-duplex communication capabilities are demonstrated with a 100 kbps bitstream correctly recovered for downlink and a 1.6 Mbps generated for the uplink communication. The power transmission efficiency is dependant on the total average current of the load – optrodes at the brain implant – and achieves a maximum value of 66 %. The power loss is mainly due to the IR dissipation on the implantable lead, the voltage drop on the diode-based passive rectifier, and the inherent power loss of a linear regulator.

The results and characterisation of these three different blocks of the 4WiCS interfacing was achieved by testing the components separately and in ideal conditions. However, to evaluate the correct functionality and performance of such components when they are connected together within a biological environment, i.e. implanted in a human body, an end-to-end emulation platform should be developed. The next Chapter focused on the implementation of such platform and on the challenges arising.

Chapter 5

End-to-End Implant System Integration

This Chapter¹ presents the development of an emulation platform integrating the modules of the CANDO implant system in a single system to implement system integration testing.

In Chapter 4, the two units that constitute the 4WiCS interfacing system (*4WiCS brain implant interface*; *4WiCS chest implant interfaces*) and the communication channel (*Cooper cable*) have been introduced and described in detail. In addition, testing and measurement results of the single units have been presented, which demonstrate the performance and capabilities of the different circuits within the two units and the characteristics of the cable. These tests are achieved with ideal power supplies and signal generators and performed in air, limiting the non-idealities and the noise/interference sources. Needless to say, when integrating multiple modules within an implantable system, new challenges will arise due to interactions between different modules and between the modules and the environment – biological tissue and sources of interference.

¹The designs, implementations, tests, and results presented in this Chapter are obtained from the research pursued within the CANDO project. They derive from collaboration with colleagues, peers, and students from the Centre for Bio-inspired Technology of Imperial College London, promptly cited in the relative sections. The content described hereby has already been published in three conference papers. Portions of the content written in this document have been adapted from such publications. They are: [37] [172] [173]. The author of this thesis is first author of these three publication.

These interactions create non-idealities and parasitics that need to be taken into account, as they may modify the behaviour of the components and their performance. Also, design considerations need to be taken into account for efficient power management, system reliability, and patient safety.

For this reason, an end-to-end emulation platform is developed and tested to verify the 4WiCS interfacing system meets its power generation and transfer requirements and to show the capability of the 4WiCS protocol to target and control multiple satellite modules from a central module, thus demonstrating the scalability of the data communication system. Additional considerations on the key aspects of a multi-module implant system are discussed, which are crucial to informing the future development of a 2nd generation of the 4WiCS interface.

5.1 CANDO Multi-Module System Integration

5.1.1 4WiCS End-to-End Platform: Design and Implementation

The **End-to-End (E2E) 4WiCS demonstration platform** has been developed and assembled at PCB-level including components described in Chapter 4. The proposed demo platform architecture, shown in Figure 5.15, consists of the following blocks: (1) a Graphical User Interface (GUI) operating on a PC; (2) a 4WiCS chest implant interface; (3) an implantable lead; and (4) a brain implant with 4 PCB-based satellite modules. Each satellite module includes:

- a *4WiCS brain implant interface (4WiCS ASIC)* that connects to the implantable lead, recovering power and encoding/decoding data through the 4WiCS protocol;
- a *programmable logic device* to provide a digital interface (4WiCS-to-SPI) between the 4WiCS interface output and the core optrode circuitry;
- *core optrode circuitry (CANDO3 ASIC)* with digital controller (FSM), stimulation, and recording circuitry communicating through SPI with the 4WiCS-to-SPI device; and
- a *passive probe* with LEDs and recording sites connected to the core optrodes circuitry.

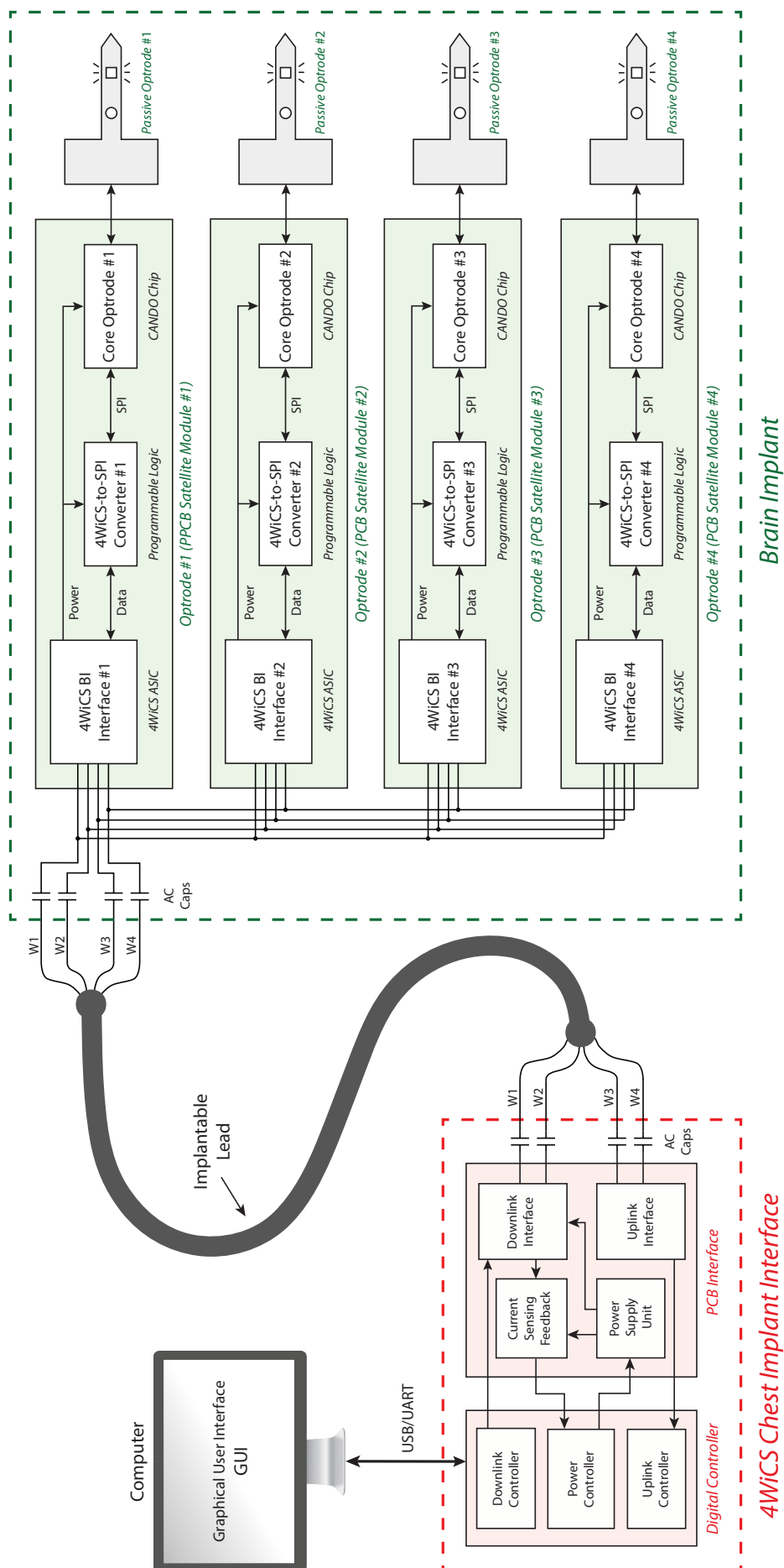


Figure 5.1: Top level architecture of the 4WiCS E2E demonstration platform.

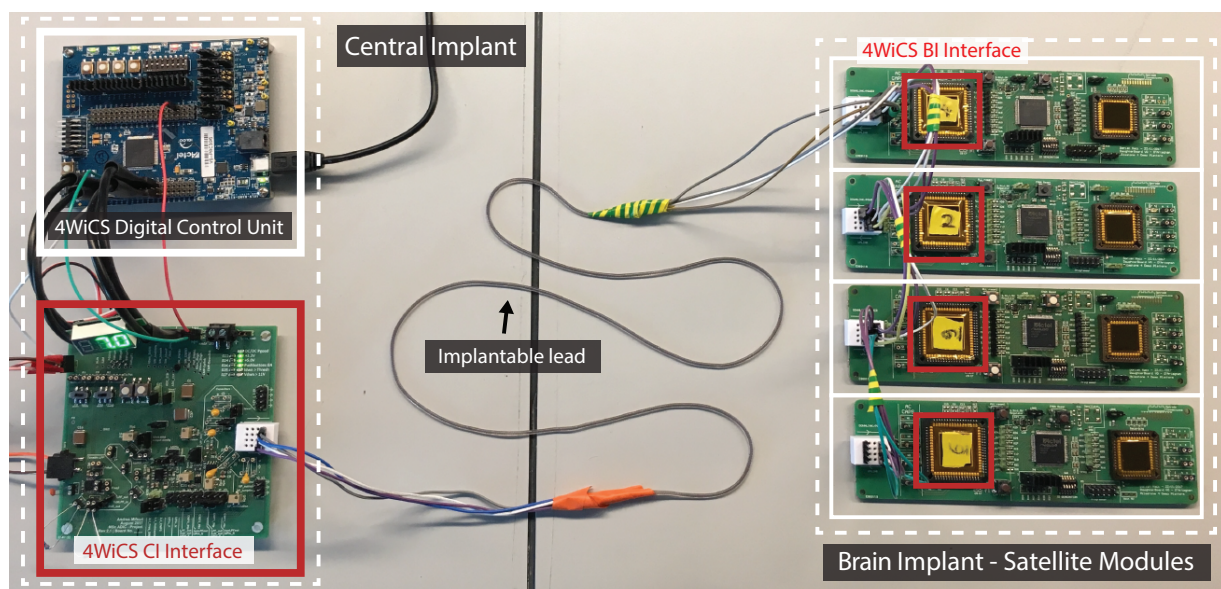


Figure 5.2: PCB-level implementation of the 4WiCS E2E platform.

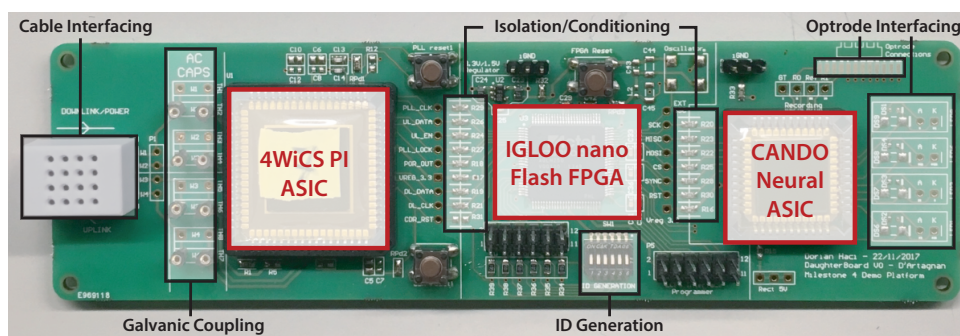


Figure 5.3: Picture of the PCB-based satellite module with highlighted the 3 core circuits: the 4WiCS BI ASIC; an FPGA implementing the 4WiCS-to-SPI bridge; the CANDOS Neural ASIC.

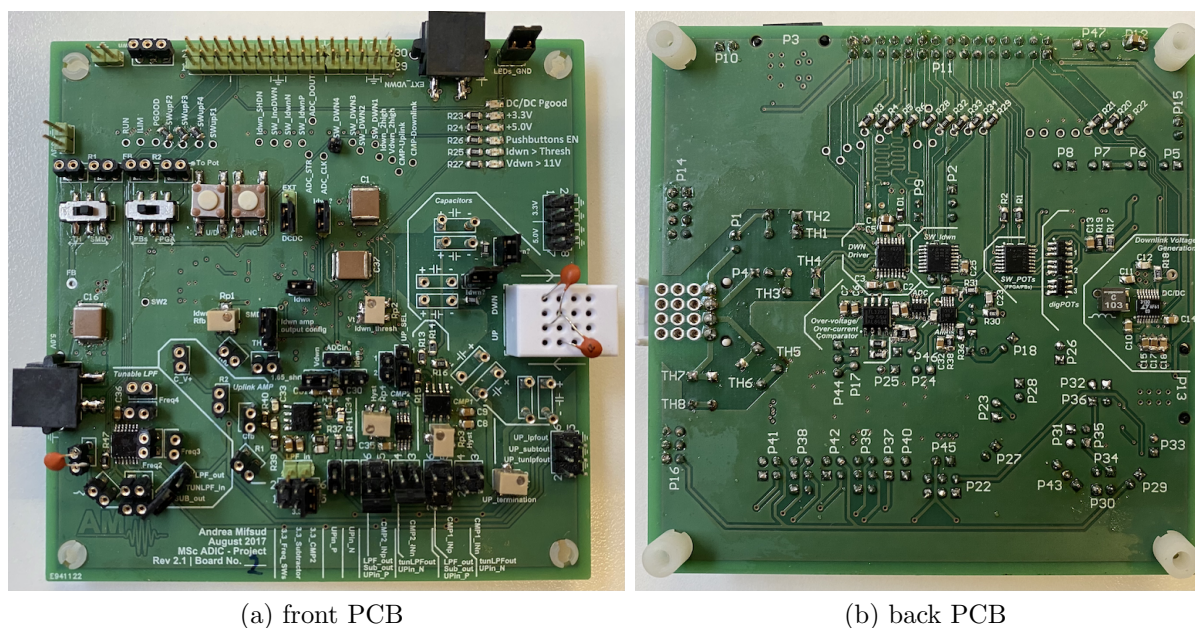


Figure 5.4: PCB-based 4WiCS chest implant interface V2 [174].

A first successful implementation of the E2E demo platform has been achieved. This is shown in Figure 5.2. At the chest implant end, an updated version of the 4WiCS chest implant interface described in Chapter 4, Section 4.4, has been used as central module. This (version V2) features higher power efficiency, improved stability, and a more reliable uplink signal recovery. Moreover, the V2 circuits are implemented with flexibility in mind, to allow for most of the parameters to be tunable for optimization [174].

The Cooper cable, presented in Section 4.3, was used as the physical communication channel, interfacing at both ends with the Craggs connectors [175]. At the brain implant end, 4 identical printed circuit boards have been designed to serve as the optrode circuit integration. Such PCBs have been fabricated, assembled, and tested. The ASIC described in Chapter 4, Section 4.2, was employed in each satellite PCB module. This was packaged on a 68-pin PLCC chip carrier and soldered on the PCB. As core optrode circuitry, the CANDO chip V3 (CANDO3) was used – comprising of recording, stimulation, diagnostics, and digital control circuitry – and included in the PCB.

In order to allow the 4WiCS ASIC and the CANDO3 chip to communicate with each other through the standard SPI protocol, programmable logic circuit is required to convert the 4WiCS protocol to the SPI protocol (downlink) and vice-versa (uplink). For this reason, an IGLOO Nano FPGA integrated circuit has been configured, acting as a bridge to convert the 4WiCS signals to the standard SPI signals. Such FPGA was chosen because of its capability to implement bidirectional parallel threads, despite its minimal number of logic elements. Both the CANDO chip and the FPGA are powered directly by the 4WiCS interface power signals (5V and 3.3V).

The FPGA has been programmed in Verilog code through the Libero SoC integrated development environment (IDE). To allow for each of the 4 optrodes to be addressed uniquely, a 6-bit switch-based ID generation scheme has been implemented on each PCB; before the 4WiCS-to-SPI conversion, the FPGA checks whether the 6-bit address (part of the 32-bit 4WiCS data packet) corresponds to the 6-bit unique ID of the optrode. The SPI transmission starts only if the two IDs match.

5.1.2 System Power-up and Functional Testing

The E2E demo platform includes: (1) **5 custom PCB boards** with over 15 off-the-shelf integrated circuits and over *300 passive components*; (2) **8 custom integrated circuits** – 4 4WiCS ASICs and 4 CANDO3 ASICs; (3) **5 FPGAs** – one at the CI end for the digital controller and 4 at the BI end for the 4WiCS-to-SPI bridges. Due to the complexity of the system and its modularity, before performing a functional test, a detailed setup power-up sequence needs to be observed. An *application/manual document* specifying the setup configuration and the power-up/startup steps has been prepared during the implementation of the E2E demo platform. This is not included in this thesis due to its lengthy content. However, the fundamental points and procedures are summarised in the following and expanded in Appendix B:

Power-up sequence

- 4WiCS CI interface is powered up and voltages are inspected;
- The current through the Cooper cable and voltage levels at SI end are inspected;
- Rectifier and regulator outputs are measured and confirmed within the expected range;
- Correct clock and data recovery is verified and high-frequency clock generation confirmed;
- The downlink communication is enabled and commands are sent from CI to SI;
- Correct start of SPI communication is verified by inspecting SPI MOSI at the target SI;
- Correct response of the SPI slave is verified by inspecting SPI MISO at the target SI;
- Correct end-to-end communication is verified by inspecting the uplink signal at the CI.

Functional testing

The 4WiCS E2E demo platform has been tested for correct functionality following the above power-up sequence. Capabilities of the platform to (1) supply power from the central module to the satellite modules and (2) to simultaneously communicate with 4 satellite modules in parallel were verified. The DC supply voltages at each of the satellite modules were measured

to be within 6% of the expected values (5V and 3.3V). Downlink data and clock recovery was verified at each satellite module, as shown in Figure 5.5.

Moreover, downlink and uplink communication were demonstrated by correctly delivering data packets from CI to BI along the downlink path and by receiving the acknowledgement response from each of the different modules separately along the uplink path. To demonstrate unique addressing of different optrodes, 4 different IDs have been chosen and assigned to the 4 modules. These were accessed one by one with the relative address from the GUI: only the module with

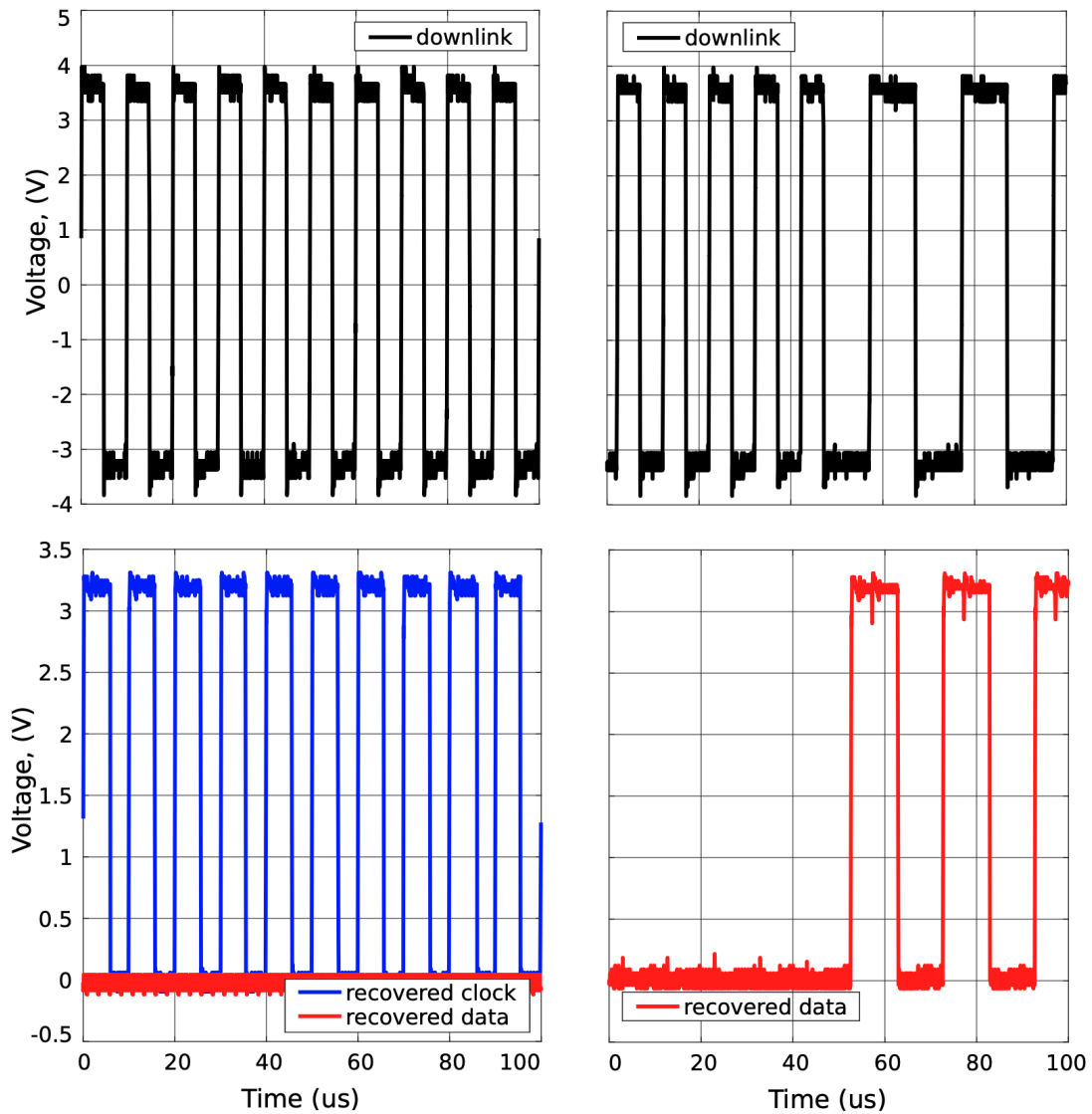


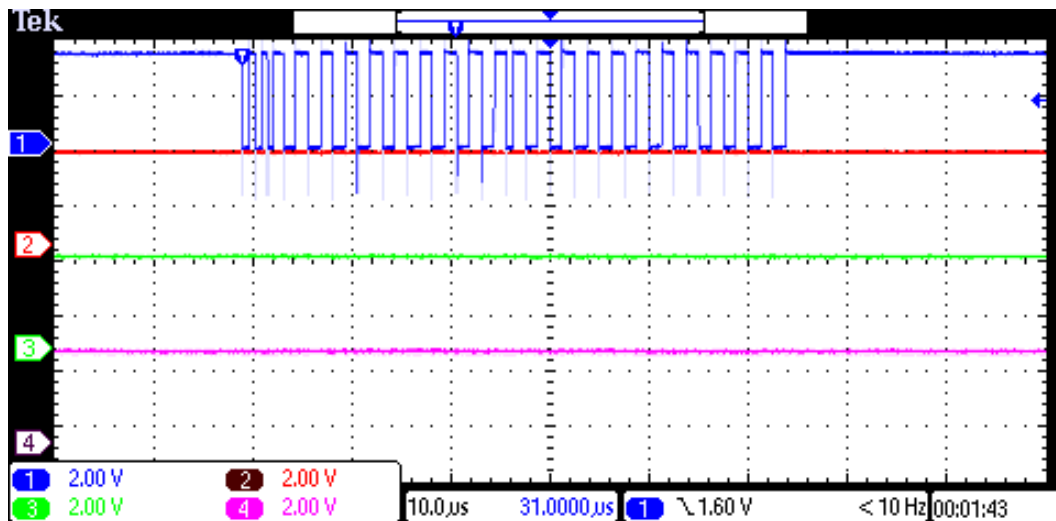
Figure 5.5: Measured downlink clock and data signals recovered by one of the 4WiCS ASICs. (left) no information encoded in the downlink signal results in a 100 kHz clock and a constant logic "low" for the data; (right) information encoded (Manchester code) as alternation of zeroes and ones (010101010...) in the downlink signal results in recovered/decoded data as an alternation of logic 'low' and logic 'high'. Adapted from [32].

matching address has been able to receive the downlink data packet and respond with the acknowledgement data packet, as shown in the oscilloscope signals in Figure 5.6.

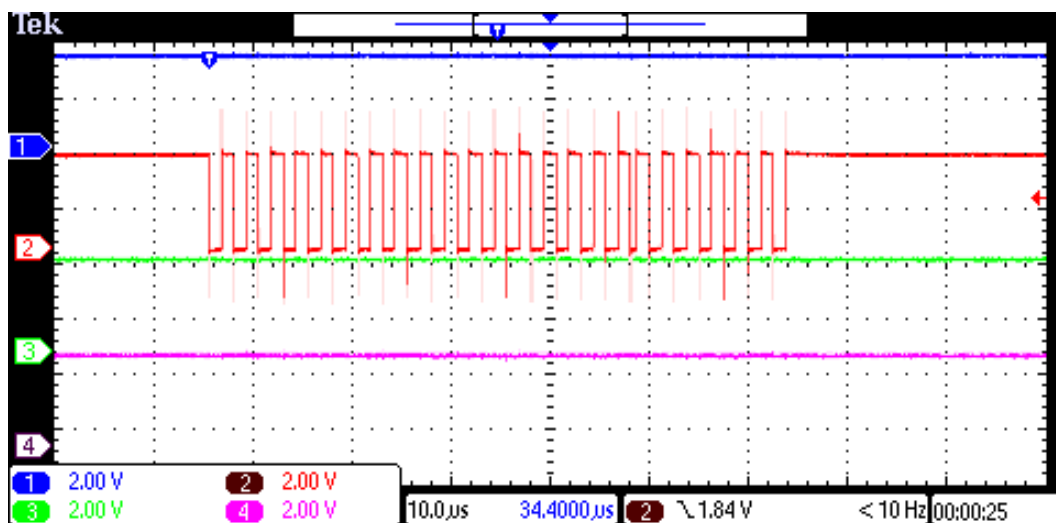
In addition, to verify the information encoded in the data packet is maintained during the various conversion and encoding/decoding stages, *LED-ON* and *LED-OFF* commands were chosen to be used as a demonstration of the end-to-end CANDO system functioning for one of its core applications – optical stimulation. In fact, such commands are responsible for activating the LED drivers when received at the CANDO3 ASIC. For this specific demonstration and for simplification, off-the-shelf LEDs were employed. One LED per satellite module was connected to the 4 different CANDO3 ASICs and driven by the LED #1 diver.

Figure 5.7 illustrates communication signals on the satellite module #3 (Optrode 011) when the LED1-ON command is generated at the CI end. Such signals are: (1) the downlink signal decoded by the clock and data recovery circuits on the 4WiCS ASIC (blue trace); (2) the SPI SCK clock and SPI MOSI generated by the 4WiCS-to-SPI bridge (green and red traces respectively) ; and (3) the SPI MISO response from the CANDO3 ASIC (purple trace). These show that (1) the downlink signal is correctly decoded by the 4WiCS ASIC, (2) the protocol conversion bridge translates correctly the downlink signal to SPI MOSI, and (3) the CANDO3 ASIC correctly interprets the MOSI signal and answers by activating the SPI MISO. Such test was performed on each of the 4 optrodes. Moreover, Figure 5.8 shows the same LED1-ON command being sent to 3 different optrodes in succession by using different ID addresses. Only the targeted module activates the SPI SCK clock, thus also the communication with the CANDO3 ASIC. This test was also performed and recorded on videocamera for visual demonstration of correct functionality – LEDs from different optrodes turning on and off in sequence following the command being sent by the GUI. The video has been uploaded online and can be found at the following link:

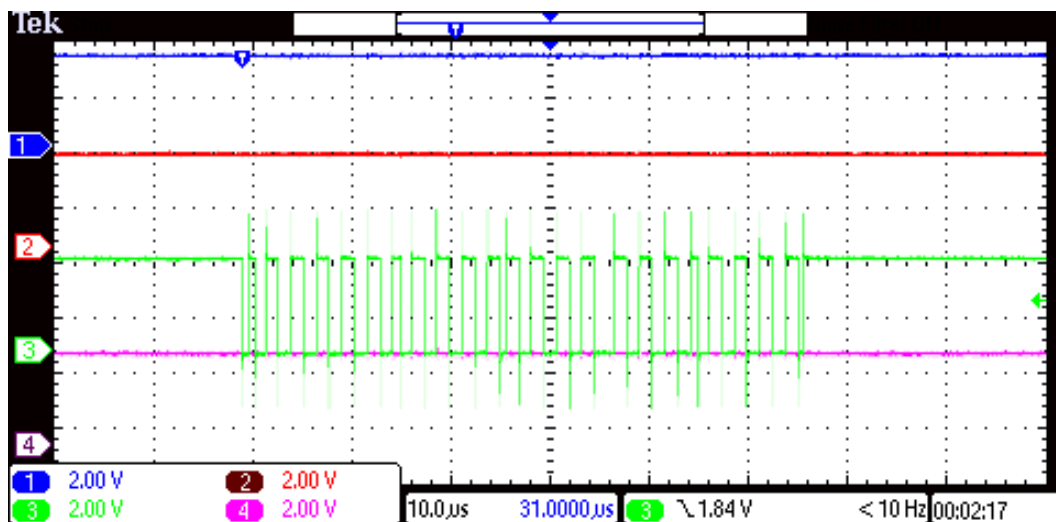
https://www.dropbox.com/s/iutvmuwx4g0ew3f/4WiCS_end-to-end_testing.MOV?dl=0



(a) SPI MISO signal Optrode 001 (blue).



(b) SPI MISO signal Optrode 010 (red).



(c) SPI MISO signal Optrode 011 (green).

Figure 5.6: Oscilloscope views of the acknowledgement packet sent over the SPI MISO signal by the satellite modules/optrodes when univocally addressed by the central module.

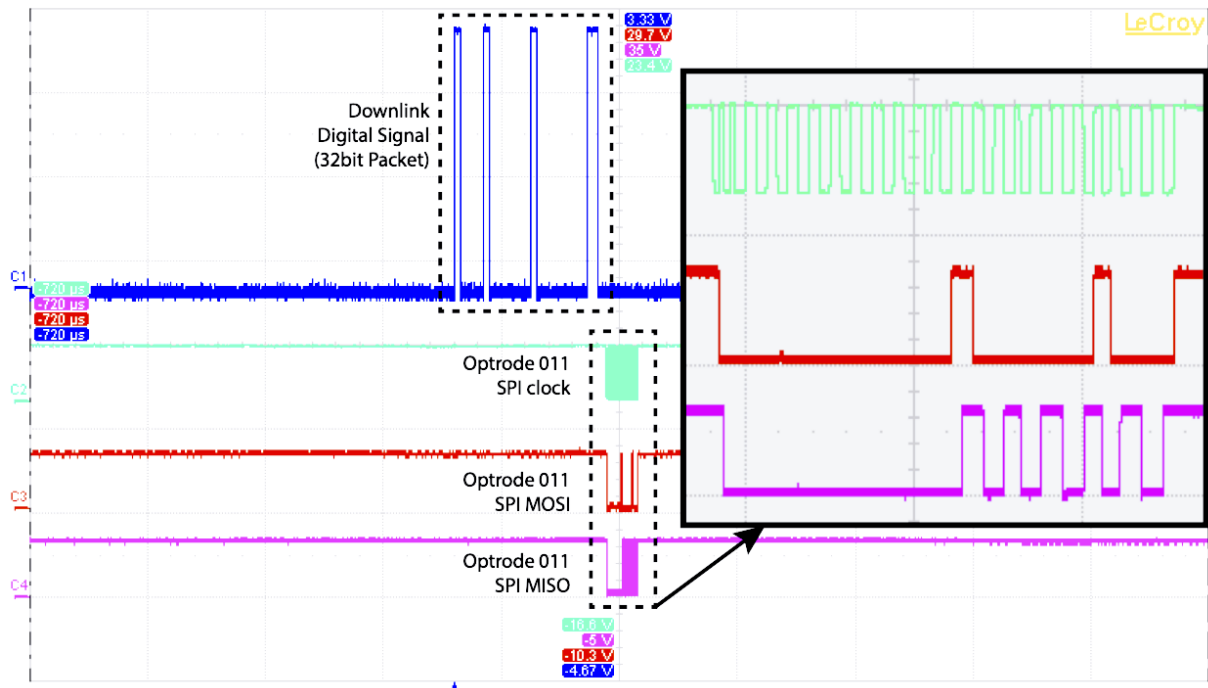


Figure 5.7: Oscilloscope traces of downlink and SPI signals (SCK, MOSI, MISO) with acknowledgement response from a an optrode through SPI link.

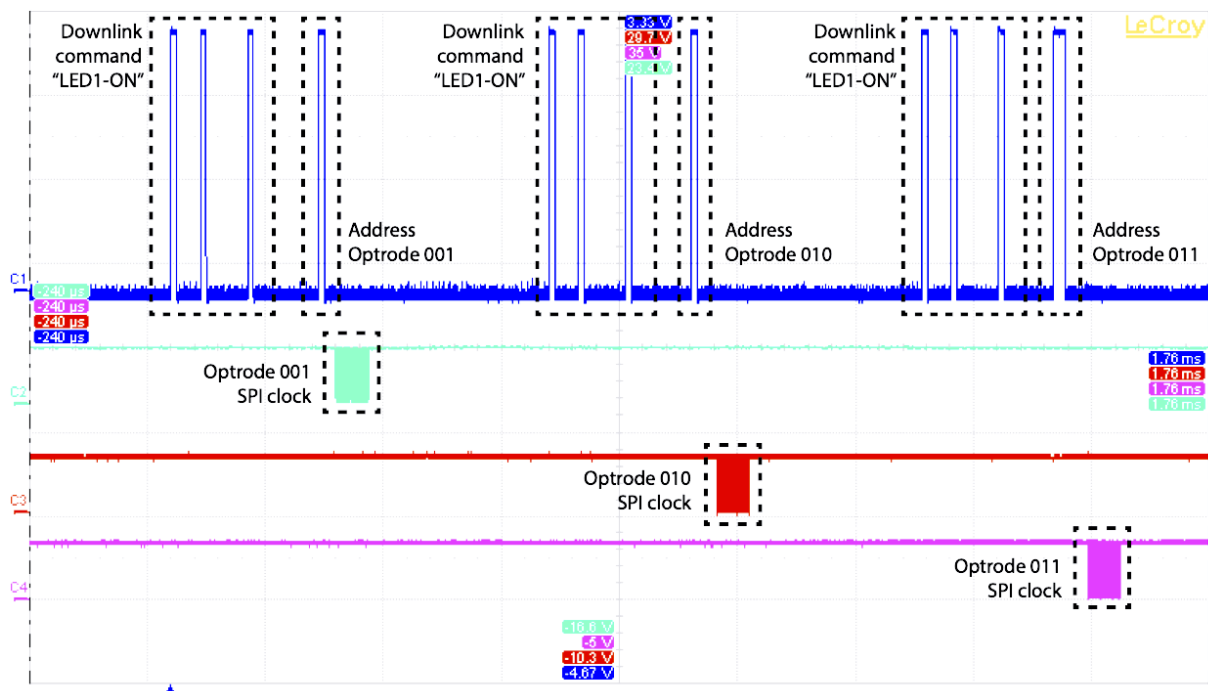


Figure 5.8: Oscilloscope traces of 3 optrodes establishing SPI communication when addressed with respective ID codes.

5.1.3 System Characterisation and Performance Testing

Besides the above-presented tests validating the functionality of the end-to-end 4WiCS interfacing, further tests have been carried out to characterize the system and evaluate the combined performance of the functions of the 4WiCS demo platform. Key parameters were chosen in order to illustrate performance:

- Voltage range and ripple of the unregulated 5V (rectifier output);
- Power Transfer Efficiency (PTE) of the power delivery system;
- Bit Error Rate of the data communication system.

Power delivery characterization and performance

As described in the previous Chapter 4, the power delivered from CI to BI is generated in DC domain by the power supply unit within the 4WiCS CI interface and guided in AC form through the Cooper cable by the downlink drivers. Thanks to the adaptive power delivery method employed at the CI end, the peak to peak AC signal received at the BI by each rectifier is kept constant. This allows for the output of the rectifier V_{rect} to be $\sim 5V$ in every acceptable load condition – within the operational range 0-4 mA current load. This DC voltage has been probed and measured for each of the 4 optrodes separately, whilst having the other 3 modules supplied by the same power signal simultaneously. An off-chip capacitor of 200 pF was added at the output for smoothing the 5V power signal. The $V_{rect-mean}$ mean value was measured to be in the range $5V \pm 300mV$ for all 4 optrodes and the $V_{rect-ripple}$ voltage ripple is less than 200 mV. As shown in Figure 5.9, the largest drop of the V_{rect} happens when there is a transition of the downlink/power squarewave at the input of the rectifier, causing oscillations, thus the ripple. This is however contrasted by the filtering effect of the smoothing capacitance that dampens the glitches caused by the squarewave transitions, ultimately limiting it to a maximum ripple of 200 mV.

In addition to the generation of a reliable supply voltage on each optrode of the brain implant, the 4WiCS interface needs to ensure adequate power efficiency. This is a key parameter in an

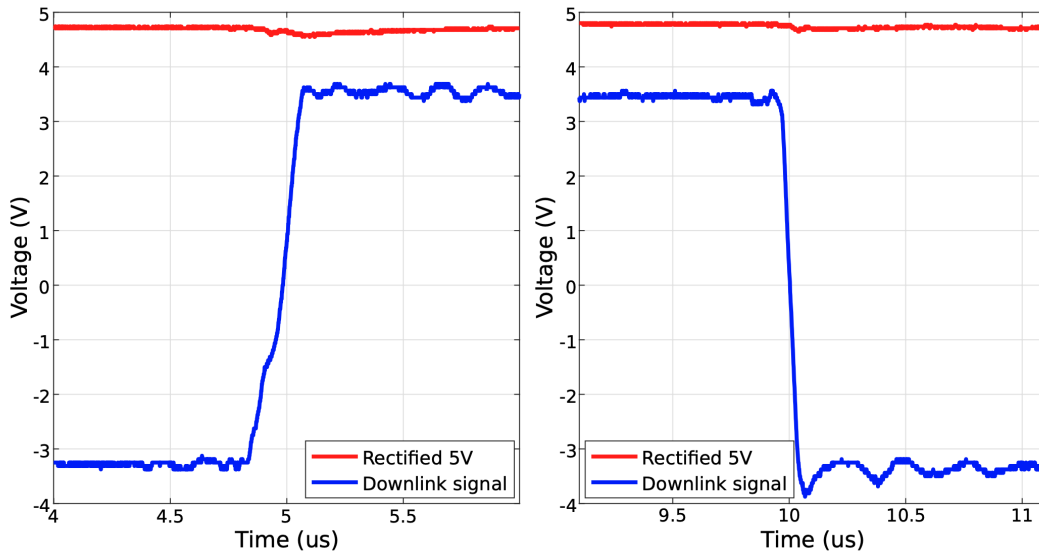


Figure 5.9: Downlink/power waveform and recovered V_{rect} at the rectifier output. [174]

implantable system, which is powered by an energy-limited implantable battery. High efficiency allows for reduced losses, hence increased battery life. In the following, PTE is defined as the ratio between the power provided at the output of the rectifier at the BI end ($P_{out} = V_{rect}I_{load}$) and the power generated by the DC/DC converter at the CI end ($P_{in} = V_{down}I_{down}$). Therefore, the losses that are taken into account are on the DC/AC stage at the CI (downlink drivers), on the Cooper cable, and on the AC/DC stage at the BI (rectifier). The former is negligible compared to the other losses, as the relatively high resistance of the cable wires and the switching of the passive rectifier account for most of the losses in the power delivery path.

The relevant voltages and currents were measured at the CI and at a single satellite module at the BI. P_{in} and P_{out} were calculated for different load conditions (0-4.2 mA). The plot in Figure 5.10 presents the PTE, which achieves a maximum value of 70%.

Data communication characterisation and performance

The evaluation of the data communication system performance relies on the evaluation of correct reception and decoding of the data packets at all receiving ends of the system. Therefore, the most appropriate and typical performance measurement is the BER, which gives an indication of how many bits are decoded/received incorrectly in comparison to how many bits are

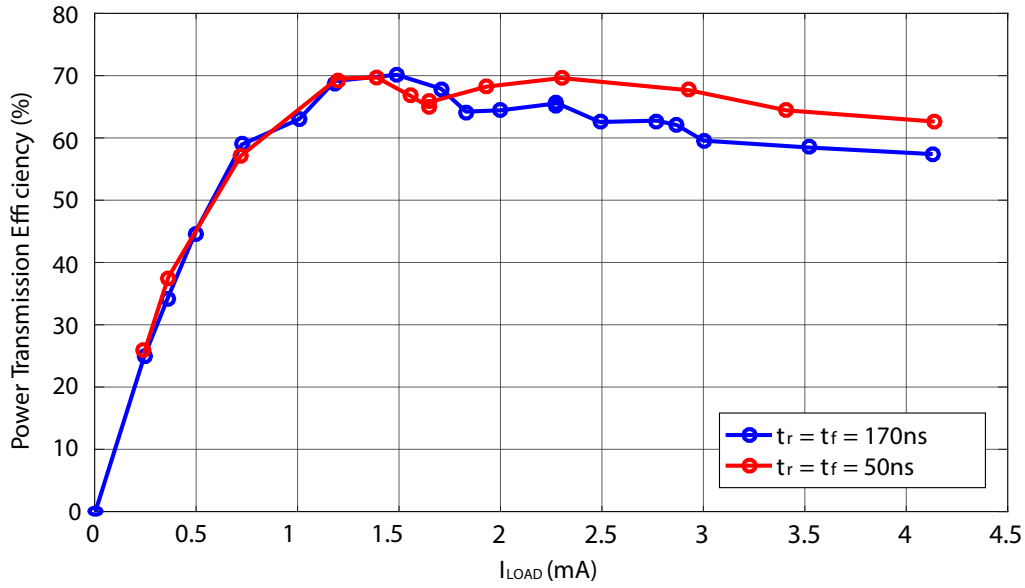


Figure 5.10: Power Transmission Efficiency (PTE) of the power delivery to varying of load current. (Red) rise and fall time of power carrier square wave $t_r = t_f = 50$ ns; (blue) $t_r = t_f = 170$ ns.

sent. BER tests both for the downlink and uplink communication were performed.

For the downlink communication BER evaluation, more than 10^8 data samples were sent in a 10+ hours test without any data packets being received incorrectly. This result is justified by the large peak-to-peak value of the downlink signal ($>5V$) and the low transmission frequency (100 kHz), which makes the communication path robust to effects caused by interference and noise, typical causes of errors. This allows for the decoder within the CDR circuits to reliably recover data packets without errors. Differently, the uplink data path is susceptible to interference/noise, as its peak-to-peak signal is one order of magnitude smaller than the downlink ($\sim 100 mV_{pp}$) and the waveform at the receiver end (CI) is a triangular-shaped wave rather than a squarewave (Figure 5.11). This is due to the low-pass filtering effect of the RC characteristics of the cable wires and to the low drive strength of the tristate buffers within the 4WiCS ASIC. For this reason, the uplink receivers within the 4WiCS CI interface PCB-V2 have been updated and optimised in order to ensure the uplink waveform is correctly retrieved and converted into a decoded digital signal. The CMOS inverters used as receivers in the 4WiCS CI interface PCB-V1 (described in Chapter 4, Section 4.4) have been updated to a more complex receiver based on a subtractor, a tunable low-pass filter, and a comparator with hysteresis. These components are illustrated in Figure 5.13.

Table 5.1: Test results for uplink communication BER

Parameters	Value
Data Rate	1.6 Mbps
Data Packet	2396745 ₁₀
Total # of packets sent	1,385,057
Number of correct packets	1,385,050
Number of wrong packets	7
BER	$5.1 \cdot 10^{-6}$
Operating Conditions	$V_{down} = 6.5 V$ $V_{rect} = 5.2 V$

The uplink BER test was performed with the updated receivers and a 300Ω termination resistor at the chest implant. Table 5.1 presents the results from the uplink BER test. A BER value of $5.1 \cdot 10^{-6}$ was calculated. It is important to highlight that the small number of wrong packets (7 out of 1,385,057) were all identified by the digital controller and ignored before being sent to the GUI, thus no data packet was erroneously displayed on the GUI. This demonstrates the capability of the communication system to recognise errors in time when occurring and act accordingly.

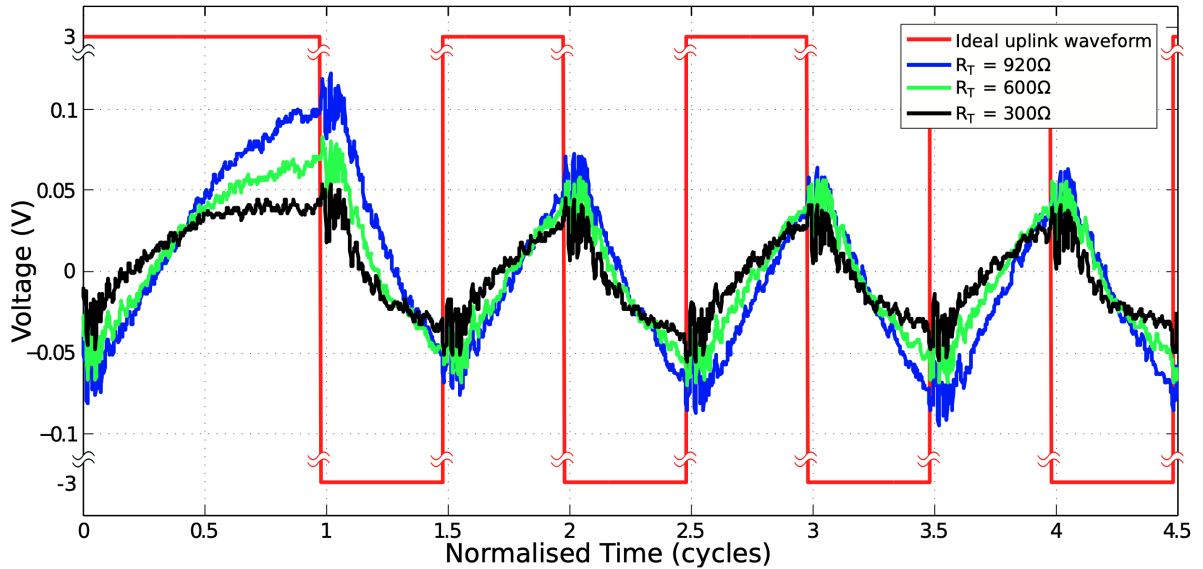


Figure 5.11: Real uplink signal received at the CI end (measured with 3 different termination resistors) compared to the ideal uplink waveform.

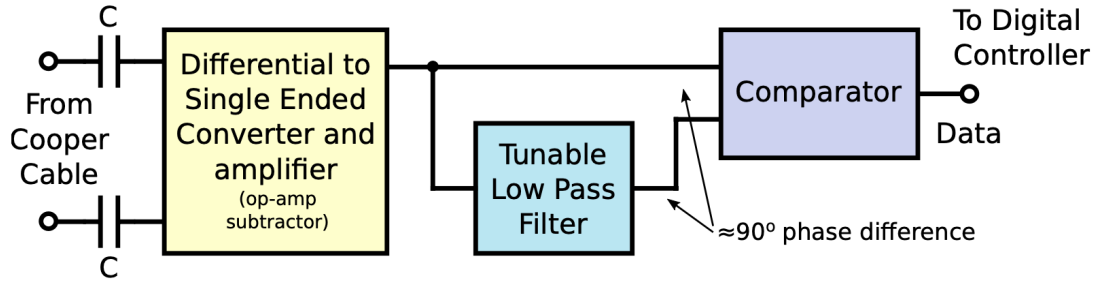


Figure 5.12: Uplink receiver block diagram based on a subtractor, a tunable LPF, and a comparator.

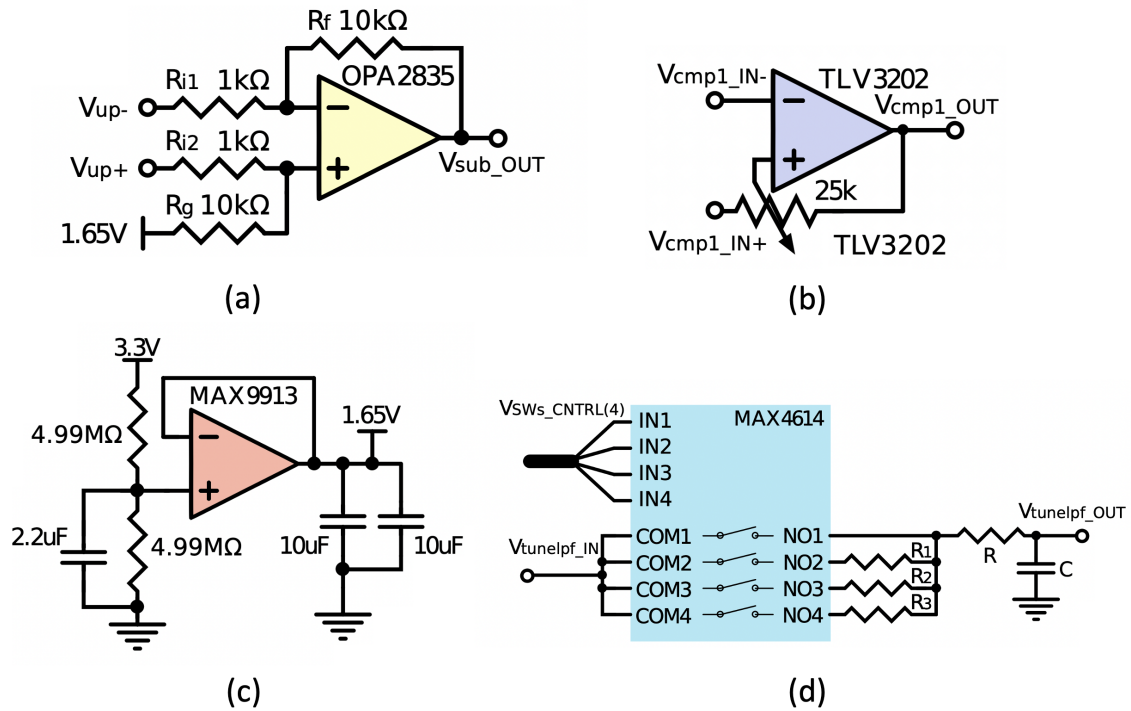


Figure 5.13: Schematics of the uplink receiver and relative off-the-shelf components chosen for integration into the 4WiCS CI interface V2 PCB: (a) op-amp subtractor – OPA2835; (b) hysteretic comparator – TLV3202; (c) reference bias supply – MAX9913; (d) tunable LPF – MAC4614. [174]

5.2 Integration Challenges:

Power Management and System Efficiency

From the power delivery performance tests presented in the previous section, it is clear that the efficiency of the whole implantable system is highly dependant on the efficiency of the power transmission from CI to BI – PTE. The latter is the product of the efficiency of (1) the *power delivery circuits* at the CI end $\eta_{dcac,ci}$ (DC/AC drivers), (2) the *cable* η_{cable} , and (3) the *power recovery circuits* at the BI end $\eta_{acdc,bi}$ (AC/DC converter). Nevertheless, in order to design a more efficient 4WiCS end-to-end interfacing, other elements within the implantable systems should be taken into account. Besides the 4WiCS components responsible for distributing the energy from the chest implant to the brain implant, it is crucial to consider also other key circuits within the system that generate, store, and utilise the energy.

5.2.1 Power Management Strategy

For these reasons, an overall power management strategy should be established, proposing a holistic approach that evaluates power requirements from a system-level perspective and optimises the strategy with respect to the target application. The choice of modality used to generate, store, and distribute the energy within the implantable system depends on three main factors: (1) external requirements relating to the medical application – e.g. user desirability; (2) essential application-specific functions; and (3) implementation constraints. The power management strategy should thus take into account all such key factors that are often conflicting and optimise the overall system power consumption.

1) Medical application and energy supply

Most currently available AIMDs are intended for therapeutic applications. In some cases, they provide a first-line treatment for patients with life-threatening conditions, such as the implantable cardiac defibrillator employed for people at risk for sudden cardiac arrest, or the

artificial cardiac pacemaker regulating the electrical conduction of the heart through timed pulses. Due to their life-critical function, these devices must include a *long-lasting battery* and power management circuitry to ensure the therapy is autonomous and uninterrupted.

However, for AIMDs that are correcting or restoring ‘non-vital’ functions, it is not critical to ensure a continuous power supply (i.e. any interruption would not risk patients’ life). An example is DBS for movement disorders such as Parkinson’s disease. Although this still uses a subcutaneous chest implant with a primary cell, the neuromodulation that is delivered to deep brain structures can be enabled by way of an external programmer. This allows patients and clinicians to activate the treatment when needed. On the other hand, cochlear implants do not contain a battery; but rather receive their energy (and data) via an *inductive transcutaneous link* to an external device. It is this external device (e.g. wearable, behind the ear) housing the battery (and thus user changeable) together with microphone, auditory processor and inductive coil. If this is thus detached from the scalp, the implant is turned off and the function is interrupted.

The application constraints guide the choice of which energy generation modalities are needed and where. This in turn defines the high-level power management architecture that is required. In battery-powered implants, for example, DC/DC supply conversion is required to generate the appropriate voltage levels for the underlying circuitry; whilst in wirelessly powered implants, AC/DC conversion is required (i.e. rectification, smoothing, regulation) to recover a stable, constant DC supply.

CANDO: in the target application, seizures may occur at any moment of the day or night. The closed-loop strategy continually monitors neural activity and, on detection of key biomarkers, provides real-time intervention through neural stimulation. This requires the implant system to always be on, and therefore the power management strategy includes an implanted battery to ensure a continuous, uninterrupted supply to the whole system. This translates into the requirement for power delivery from CI to BI to be active at any time.

2) Functional requirements and implant lifespan

Medical implants can interact with the human body by (1) modulating neural activity using electrical, optical, or ultrasound stimulation, and/or by (2) sensing neural activity typically electrically. As introduced in Chapter 2, most of the early AIMD were electrical stimulation only devices. Examples of neuromodulation devices such as vagus nerve stimulators for epilepsy and spinal cord stimulators for chronic pain also belong to this category, as they provide open-loop therapies. The power consumption of such devices is thus largely dependant on the required stimulation parameters. As earlier discussed, closed-loop neuromodulation devices rely on real-time biopotential sensing in addition to stimulation. On one hand, such platforms allow for energy saving by optimising the stimulation delivery function. Nevertheless, the additional circuitry for sensing, data conversion, signal processing and closed-loop algorithms significantly increases the system complexity and thus also the total system power requirements.

The vast majority of implants designed to deliver open-loop treatments operate autonomously, based on a "prescribed dose". The required energy capacity can thus be predicted by specifying a target primary cell capacity – in some cases with an autonomy of up to 10 years before replacement [176]. Closed-loop devices however, particularly if also used as research platforms, have less well defined power requirements and therefore a (rechargeable) cell is preferable to allow maximum versatility, and battery lifetime. For this reason, the AIMD industry has started also using *rechargeable battery* technology. These allow for a significant increase in implant lifespan, despite having a lower capacity per unit volume.

For example, the Activa PC+S device from Medtronic includes a primary cell with a battery capacity of 6.3 Ah. This means that, for the battery to last for 4 years implanted in the body, the average current should not exceed 0.18 mA. This limits significantly the capability of the medical function, as trade-offs need to be made in order to allow for long-term implantation. Another, more recent member of the Medtronic Activa family, the Activa RC+S, comprises a 500 mAh rechargeable battery. Despite its lower energy density compared to the primary cell counterpart, it can be recharged on a weekly/quarterly basis, allowing for a higher power consumption available each day. In fact, considering a rechargeable interval of 7 days, the

Table 5.2: Examples of commercially-available AIMDs compared to the CANDO system.

Parameter	Medtronic Activa PC	Medtronic Activa RC+S	NeuroPace RNS	CWRU NNP System [61]	CANDO System [84]
Application	DBS Therapy	DBS Therapy	Epilepsy	Neuroprosthetics	Epilepsy
Neuromodulation	Open-loop	Closed-loop	Closed-loop	Closed loop	Closed-loop
Energy source	Primary cell	Rechargeable	Primary cell	Rechargeable	Rechargeable
Battery capacity	6.3 Ah	500 mAh	706 mAh	N/A	600 mAh
Battery lifetime	4-6 years	7-14 days/charge	3-9 years	N/A	24 hr recharge
AIMD Location	Chest	Chest	Head (skull)	Torso and limbs	Chest and brain
Modularity	Single unit	Single unit	Single unit	Multi-module	Multi-module

average current consumption achievable is almost 3 mA – more than one order of magnitude higher than the primary-cell-based implant. Although this addresses the fundamental energy capacity challenge, it brings in: (1) design challenges, e.g. need for reliable wireless charging techniques and additional power management circuits, and (2) patient adoption concerns, e.g. device/tissue interface overheating, recharging time and recharging interval. It is thus crucial to assess the expected power requirements, and energy budget needed early in the design process.

CANDO: as part of the closed-loop CANDO therapy, a real-time intervention is provided. This requires front-end acquisition circuits (neural recording amplifiers, filters, data converter) in addition to a digital signal processor to continuously operate, thus forming a baseline static power consumption. The stimulation function on the other hand is activated in response to a seizure detection, and thus energy requirements depend on the occurrence frequency of the seizures. Despite this somewhat sporadic nature of the neuromodulation, the power requirement of the light sources used to facilitate the optogenetic activation of neurons is not negligible; it is estimated this requires an additional >10 mW average power during stimulation. Considering the maximum energy density of a typical implantable Lithium-ion battery is ~ 1 Wh/cm³ [177], a rechargeable battery is necessary to guarantee an implant lifetime of at least 2 years.

This in turn leads to further trade-offs from the end-user and medical application perspective between battery (i.e. chest implant) volume and recharge interval. The current requirement for the CANDO implant system is to include a battery of 600 mAh, with a daily recharge interval (every 24–36 hours) – as shown in Table 5.2.

3) Implementation constraints and number of modules

Typically, AIMDs have been limited to *single unit devices* and implanted either in the upper chest, abdominal area or head. They connect to the neural interface (i.e. electrode) target or stimulation and/or recording using one or multiple implantable leads. The advent of *multi-module implantable systems*, that propose a distributed approach to the interaction with the body, has introduced the need for powering multiple modules simultaneously. The decision on which energy generation modality is used – whether implanted battery or external wireless powering – in this case will determine also how the power is distributed among the modules.

The most common and reliable method for transferring power within the body is via a wired connection, as previously discussed, i.e. with a central implant housing the battery (power supply unit) and connecting to the satellite implants through implantable leads (power consumption units). Modalities based on fully wireless powering of multiple implants exist, as these provide improved biocompatibility, reliability, and space utilisation [36]. However, they pose a new set of challenges and have limited energy storage capabilities and very low power transfer efficiency. Hybrid solutions here deliver wireless power transfer transcutaneously to a rechargeable battery, which in turn employs a wireline link to distribute the power to active satellite implants. For all different types of AIMDs however, depending on the location and number of modules, specific power interfacing circuits are required to transmit and recover power. Moreover, as the power consumption within the satellite modules has a dynamic component (variable load), the power delivery needs to be adaptive to be able to provide the required voltage levels and currents.

CANDO: the proposed device employs a multi-module neural implant system with a wired-based link between the central module and satellite modules. The central module generates the power that is sent to the satellite modules – power consumption units only. The stimulation function makes these modules considered as variable loads for the central module. The latter has to guarantee a fixed voltage supply for the satellite circuits to function properly while providing variable current in order for the optical stimulation (i.e. LEDs) to be turned on and off. For this reason, the central module requires an adaptive power delivery technique.

5.2.2 Power Consumption and Efficiency Considerations

By considering the system and application requirements and the implementation constraints as previously identified, the overall system power specifications and power management strategy can be devised for the CANDO implant system to optimise energy utilisation and power efficiency. This can be evaluated by considering two parameters: (1) the recharging power transfer efficiency $\eta_{recharge}$ and (2) the total power efficiency of the implant system η_{total} .

(1) Recharging power transfer efficiency - $\eta_{recharge}$

The CANDO system presents three units managing power signals: the external battery charger, the central implant, and the satellite modules at the brain implant. The number of satellite modules (optrodes) is here considered as 4. The charger and the CI are wirelessly coupled through the skin by means of two inductive coils, allowing for transcutaneous recharging of the implanted battery. For this reason, $\eta_{recharge}$ highly depends on the inductive coupling

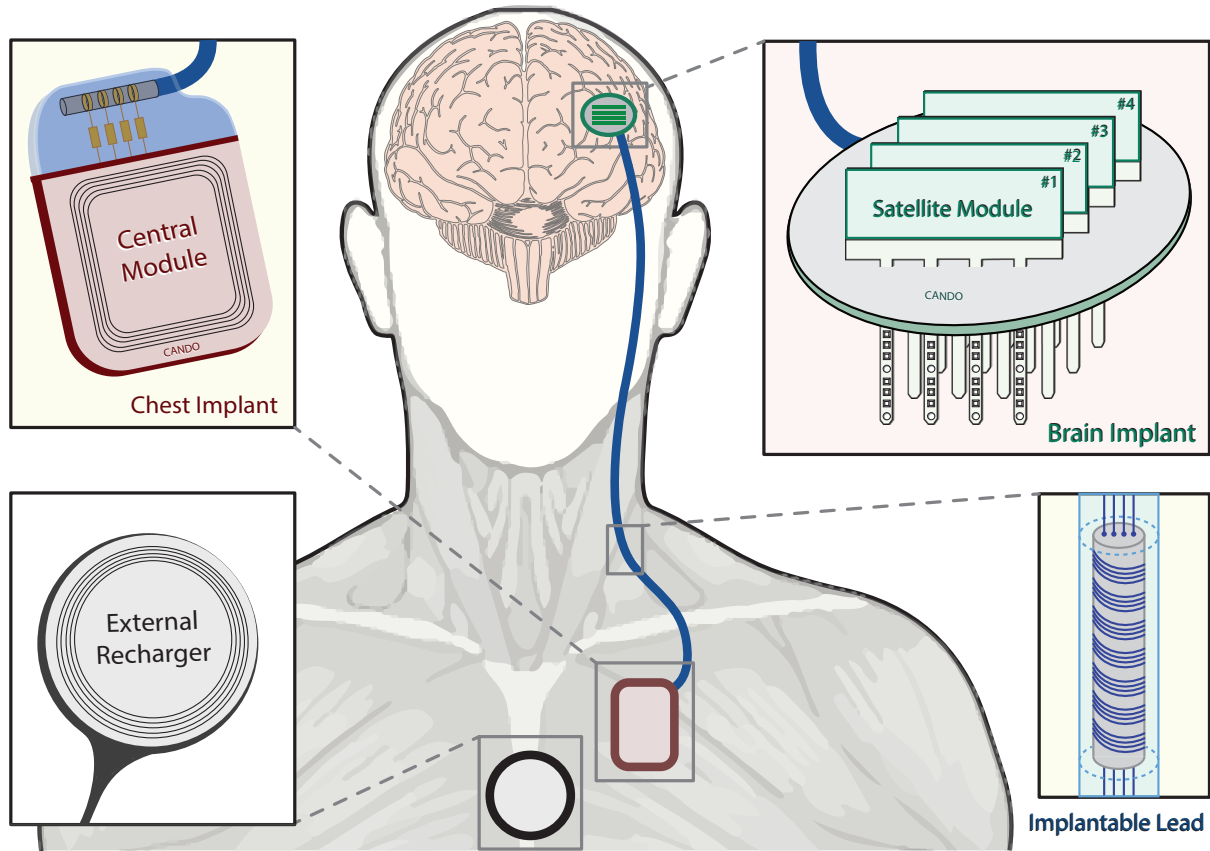


Figure 5.14: Concept of the CANDO implant system with (1) an *external recharger*, (2) one *central module* in the chest, and (3) multiple *satellite modules* at the brain end.

coefficient, which measures how much power from the generated electromagnetic field at the external primary coil is induced in the secondary coil at the CI. Management circuits are employed at both ends to maximise such coefficient and to inform when the inductive link is lossy due to miss-alignment or malfunctioning.

(2) *Total power efficiency of the implant system - η_{total}*

The η_{total} efficiency is defined as the ratio between the total power consumed by the primary functions and the total power generated by the battery. For simplification, such primary functions are here considered to be *data processing/management* (at the CI end) and *recording and stimulation* (at the BI end). Such efficiency parameter describes the ability of the system to convert/distribute the energy and to minimise the losses. Hence it depends on: (a) the *power conversion efficiency* of the power management circuits generating the supply at the chest implant, (b) the end-to-end *power transfer efficiency* from CI output to BI input, and (c) the *power conversion efficiency* of the power recovery and conversion circuits at each satellite on the BI end.

Implant System Efficiency

1. *Processing power efficiency η_{proc}* : the energy generated by the battery is converted and its output voltage regulated by a DC/DC conversion stage. Part of the output power is used to supply directly the processing and data management circuits in the CI, thus the efficiency of the power path from the battery to these circuits is equal to the efficiency of the DC/DC converter $\eta_{dcdc,ci}$:

$$\eta_{proc} = \frac{P_{proc}}{P_{proc,bat}} = \eta_{dcdc,ci} \quad (5.1)$$

2. *Recording and stimulation power efficiency η_{stim}, η_{rec}* : since the stimulation and recording functions are performed at the BI, the power generated at the CI end needs to transfer through various stages of power domain conversion. After the first DC/DC stage ($\eta_{dcdc,ci}$), the power allocated for supplying the BI is conditioned to be delivered through the implantable

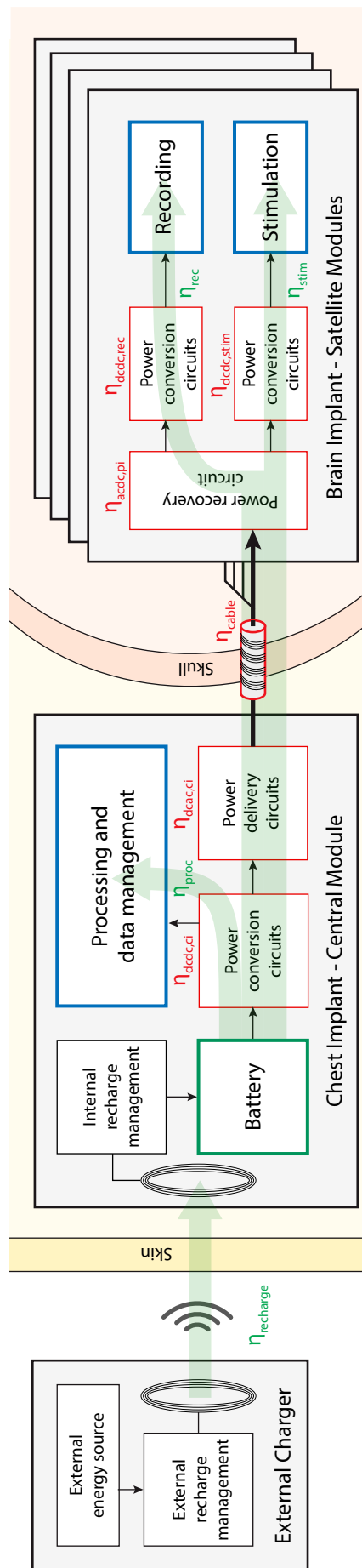


Figure 5.15: Power management architecture for the CANDO system showing the overall organisation and power distribution strategy.

cable in alternating current AC form ($\eta_{dcac,ci}$). The wires in the cable cause power loss through I^2R dissipation; this is taken into account in the cable PTE parameter η_{cable} , which is a function of both characteristics of the wires (fixed) and the current consumption of the satellite modules (variable). When received at the BI end, each of the modules retrieves the DC power signal by way of a rectification stage – AC/DC converter ($\eta_{acdc,bi}$). The path is then split into two directions, one for stimulation and one for recording. As these two functions include circuits supplied at two different voltage levels, they should have separate DC/DC conversion and regulation stages ($\eta_{dcdc,stim}$, $\eta_{dcdc,rec}$). The efficiency of the battery-to-recording (and battery-to-stimulation) power path is calculated as the product of the efficiencies of all power blocks along the path, as shown in the Equations 5.2 and 5.3.

$$\eta_{stim} = \frac{P_{stim}}{P_{stim,bat}} = \eta_{dcdc,ci} \cdot \eta_{dcac,ci} \cdot \eta_{cable} \cdot \eta_{acdc,bi} \cdot \eta_{dcdc,stim} \quad (5.2)$$

$$\eta_{rec} = \frac{P_{rec}}{P_{rec,bat}} = \eta_{dcdc,ci} \cdot \eta_{dcac,ci} \cdot \eta_{cable} \cdot \eta_{acdc,bi} \cdot \eta_{dcdc,rec} \quad (5.3)$$

By knowing the average power consumption of the primary functions P_{proc} , P_{stim} , P_{rec} and the efficiencies of the power conversion/transfer blocks η_{proc} , η_{stim} , η_{rec} , it is possible to determine the total power efficiency of the implant system. This is defined as the ratio between the total power consumed by the primary functions (processing, recording, stimulation) and the total power generated at the battery:

$$\begin{aligned} \eta_{tot} &= \frac{P_{prim,func}}{P_{tot,bat}} = \frac{P_{proc} + 4P_{stim} + 4P_{rec}}{P_{proc,bat} + 4P_{stim,bat} + 4P_{rec,bat}} = \frac{P_{proc} + 4P_{stim} + 4P_{rec}}{\frac{P_{proc}}{\eta_{proc}} + \frac{4P_{stim}}{\eta_{stim}} + \frac{4P_{rec}}{\eta_{rec}}} = \\ &= \frac{(P_{proc} + 4P_{stim} + 4P_{rec}) \cdot \eta_{proc} \cdot \eta_{stim} \cdot \eta_{rec}}{P_{proc} \cdot \eta_{stim} \cdot \eta_{rec} + 4P_{stim} \cdot \eta_{proc} \cdot \eta_{rec} + 4P_{rec} \cdot \eta_{proc} \cdot \eta_{stim}} = \\ &= \frac{(P_{proc} + 4P_{stim} + 4P_{rec}) \cdot \eta_{dcdc,ci} \cdot \eta_{dcac,ci} \cdot \eta_{cable} \cdot \eta_{acdc,bi}}{P_{proc} \cdot \eta_{dcac,ci} \cdot \eta_{cable} \cdot \eta_{acdc,bi} + \frac{4P_{stim}}{\eta_{dcdc,stim}} + \frac{4P_{rec}}{\eta_{dcdc,rec}}} \end{aligned} \quad (5.4)$$

To optimise the system power efficiency, it is crucial therefore to maximise the PCE of the DC/DC power conversion circuits ($\eta_{dcdc,ci}, \eta_{dcdc,rec}, \eta_{dcdc,stim}$) of each module and the PTE of the CI-to-PI delivery path ($\eta_{dccc,ci}, \eta_{cable}, \eta_{acdc,stim}$), therefore to optimise the efficiencies of each power conversion/transmission stage. Nevertheless, from Equation 5.4, it is clear that the total efficiency depends not only on the on single efficiencies of each stage, but also on the power consumption of the primary functions of the implant: $\eta_{tot} = f(P_{proc}, P_{stim}, P_{rec})$.

When considering the 4WiCS end-to-end platform described in the previous section, a typical operation of the three primary function of the CANDO implant system translates into the following power consumption:

- $P_{proc} = 10 \text{ mW}$ (average power of the data processing in the central module)
- $P_{rec} = 2 \text{ mW}$ (average power of the front-end recording in each satellite module)
- $P_{stim} = 5 \text{ mW}$ (average stimulation power in each satellite module when stimulating)
- $P_{prim,tot} = P_{proc} + 4P_{rec} + 4P_{stim} = 38 \text{ mW}$ (total average power of the primary functions)

In normal conditions and typical operation, the efficiencies of the power conversion/delivery stages are evaluated (from measurement or simulations) as follows:

- $\eta_{dcdc,ci} \approx 0.8$ (power efficiency of DC/DC converter at CI end)
- $\eta_{dcac,ci} \approx 0.95$ (power efficiency of downlink drivers at CI end)
- $\eta_{cable} \approx 0.65$ (from Cooper cable characteristics at typical operation)
- $\eta_{acdc,bi} \approx 0.8$ (power efficiency of full-wave rectifier at BI end)
- $\eta_{dcdc,stim} = 1$ (converter not present in current design)
- $\eta_{dcdc,rec} \approx 0.65$ (power efficiency of the voltage regulator)

Therefore, from Equation 5.4, it is possible to derive the total system efficiency:

$$\begin{aligned}
 \eta_{tot} &= \frac{(P_{proc} + 4P_{stim} + 4P_{rec}) \cdot 0.8 \cdot 0.95 \cdot 0.65 \cdot 0.8}{P_{proc} \cdot 0.95 \cdot 0.65 \cdot 0.8 + \frac{4P_{stim}}{1} + \frac{4P_{rec}}{0.65}} = \\
 &= \frac{(10 \text{ mW} + 4 \cdot 5 \text{ mW} + 4 \cdot 2 \text{ mW}) \cdot 0.8 \cdot 0.95 \cdot 0.65 \cdot 0.8}{10 \text{ mW} \cdot 0.95 \cdot 0.65 \cdot 0.8 + \frac{4 \cdot (5 \text{ mW})}{1} + \frac{4 \cdot (2 \text{ mW})}{0.65}} = \frac{15.02}{37.25} = 0.4
 \end{aligned} \tag{5.5}$$

The means that in order to provide 38 mW of power to be used by the primary functions of the implantable device, the battery needs to generate 95 mW, thus losing 60% of the power alongside the power conversion and delivery stages.

The critical stages are the ones with the lowest power efficiency, in this case, the *cable* and the *voltage regulator*. The former gives a loss of ~ 20 mW in typical operating conditions due to its very high resistivity. Although developed to be used as an implantable lead, the Cooper cable was not originally meant for transmitting power signals between multiple implants that use high voltage (>5 V) and high current (>10 mA). For such reason, having low wire resistivity was not a feature of a high priority compared to mechanical flexibility. As mentioned in the previous Chapter 4 (Section 4.3), a second version of the cable was developed specifically for the CANDO project. It presents 5 times lower resistivity for each wire and an optimised form factor, i.e. shorter length. This allows for the power dissipation on the wires to be reduced to less than 4 mW for the typical operation used in the above example, thus increasing the system power efficiency η_{tot} to 0.48 (48%). Similar to the cable, the power loss from the 4 voltage regulators is dissipated as I^2R heat. In this example, it accounts for $\sim 7.5\%$ of the total loss (4.3 mW). This is intrinsic to the architecture of the linear regulator, thus it cannot be improved. However, as the regulator main characteristic is to have a low drop-out voltage, in the CANDO satellite modules it is not used as such, but to have a 5 V unregulated voltage (output of the rectifier) into a 3.3 V regulated voltage. This translates into a voltage drop of 1.7 V that is the cause of the power loss. A better solution would be to use a DC/DC switched converter that offers a lower loss. This is however not suitable for the CANDO implant system due to its large on-chip dimensions (presence of large capacitors, inductors, and switches).

5.3 Integration Challenges:

System Reliability, Performance, and Safety

Despite being subcutaneous, thus virtually isolated from external electrical sources, fully implantable medical devices can be subject to interference coming from outside the body. EMI, for example, is an important source of interference for medical implants, especially with the recent proliferation of technology that emits electromagnetic signals, such as mobile phones, wearables and smart devices [178]. In a multi-module neural implant, this may both affect the signal recording quality and the data communication integrity. Besides external sources, also internal coupling between different signal paths could have a significant impact on the performance.

In the CANDO implantable system, two main sources of interference have been identified to negatively affect the performance of the recording function: (1) the squarewave downlink and uplink signals through the cable and (2) the activation of the stimulation. The first is due to the coupling of the wires within the implantable lead and the biological tissue surrounding it. Although the wires are embedded in silicon rubber, the capacitance between each wire and the tissue/body is not negligible and is expected to be of the order of tens pF. Since the sensing

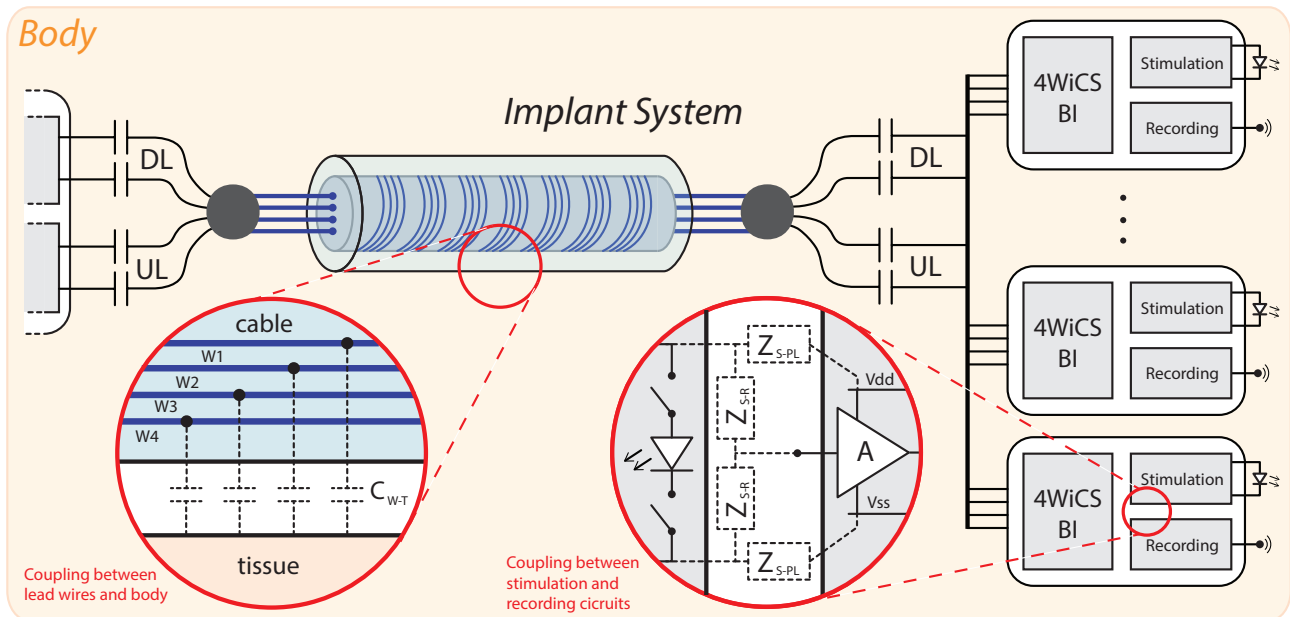


Figure 5.16: Graphical representation of the sources of interference due to internal coupling.

electrodes on the optrodes are in direct contact with the brain tissue, an impedance path is hence created between the wires and the input of the recording. From the neural recording perspective, the effect of such coupling is to be considered as a continuous noise source. The second source of interference comes from the LED stimulation circuits. This artefact appears only when the stimulation is turned on and off and is due to impedance coupling between the switching components in the stimulation circuitry and noise-sensitive circuitry, i.e. input and power rails of the front-end sensing amplifier [179].

Other important considerations need to be made moreover on how the electrical power rails of each implant module are referenced to each other and to the electrical potential of the tissue in contact with the implants. As mentioned in the previous chapter, in order to avoid a DC voltage bias across the conductors in the implantable lead [62], and thus to maintain the charge balance over time, a power transmission scheme based on AC-coupling is used in the 4WiCS interfacing system. Accordingly, AC/DC power domain conversion is implemented at the BI side. This generates a suitable DC supply voltage for the front-end circuitry ($V_{dr} - V_{ss}$), hence the module ground rail ($GndS = V_{ss}$), as shown in Figure 5.17 [63]. However, such power domain conversion creates DC isolation between central and satellite implants and therefore the electric potential of the module ground at the satellite implant ($GndS$) is not referred to the module ground at the central implant ($GndC$).

Unlike bedside hospital equipment, an implant system is placed inside the human body and it is not directly connected to the AC electric power coming from the mains (grid power); instead, it receives the electrical energy from the battery enclosed within the chest implant. Unless the body touches the mains, the generated potential rails are to be considered floating and not referenced to the earth ground. The human body, however, has its own electric potential, body potential (BP). In electrical equilibrium (no current flow within the body), this potential is considered the same over the whole body. The body potential has to be taken into account, as the potential displacement of $GndC$ and $GndS$ from BP may have as well a significant impact on recording quality and system reliability and safety.

The neural recording system in the brain implant connects the sensing electrodes that are

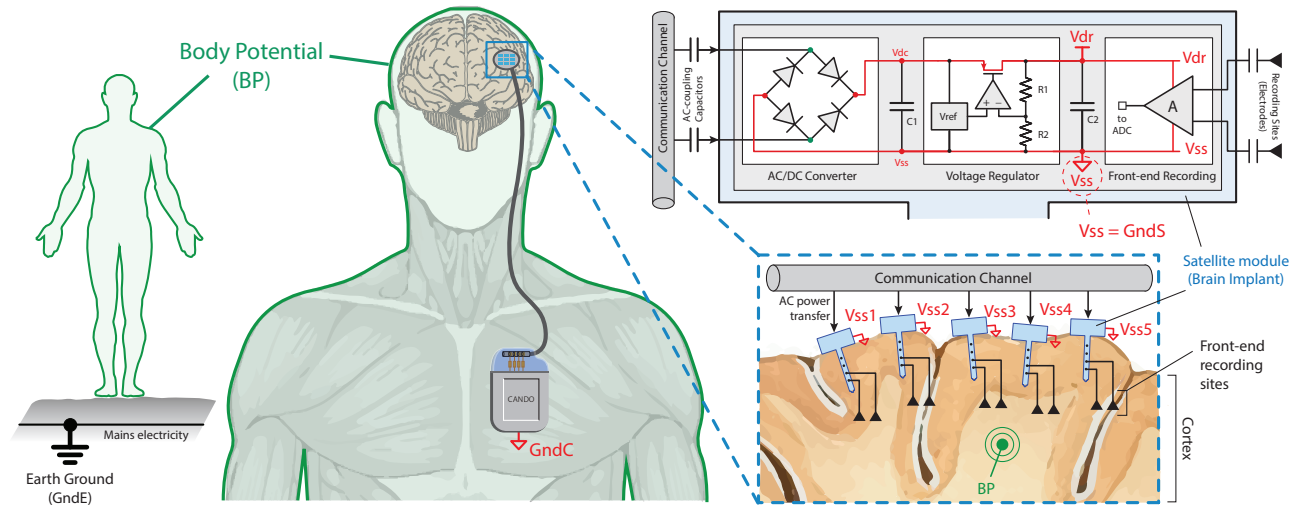


Figure 5.17: Model of the CANDO implant system with satellite modules (optrodes), each comprising power recovery and V_{dr}/V_{ss} DC rail generation, and neurosignal front-end recording circuits in direct contact with the body potential.

in direct contact with the tissue, i.e. with BP, to high impedance amplifier inputs. The observed biopotential therefore consists of this large baseline (BP) in addition to a relatively weak analogue AC signal (desired activity to be recorded). A differential front-end amplifier is used to record these signals; it senses and amplifies the difference in potential between two electrodes while suppressing the common potential (common-mode rejection, CMR). Moreover, to deal with the unknown DC offset between the BP and recording circuit (power rails V_{dr} and $V_{ss}/GndS$), the biopotential amplifier inputs are AC coupled through capacitors. This leaves the BP having a relatively high impedance to the recording circuit power rails that effectively makes the tissue an ‘antenna’ for picking up noise that will affect the recording amplifier as common-mode noise. It is thus essential to maintain a relatively low impedance connection between the recording circuit power rails and the body potential to attenuate the observed common mode noise (at the amplifier inputs).

Furthermore, in terms of safety, a significant difference in electric potential between $GndC$ (or $GndS$) and BP (voltage) may lead to corrosion/failure of encapsulation that would result in current flow into/from the tissue exceeding the safety limits defined by the international directives on active implantable devices. For these reasons, an appropriate ground referencing is required in the CANDO implant system in order to ensure good recording quality of the optrodes, but also device reliability and ultimately patient safety.

5.3.1 Ground Referencing Schemes

Given that the central implant is enclosed within a case serving as DC electrical screen from the body, with no direct contact between internal circuitry and body tissue, there is no need for $GndC$ to be referenced to BP . On the other hand, the satellite implants have a direct path to the tissue through the recording electrodes (Figure 5.17), hence the need for proper referencing of the DC rails to the body potential.

The most common and simple ground referencing configuration is the passive connection of a satellite device power rail (either V_{dr} or V_{ss}) to the body potential. In acute experiments performed for neuroscience research, the satellite module ground $GndS$ is usually shorted directly to the BP through a ground electrode, so as to reference the tissue to the lowest potential of the module. The passive scheme is represented in Figure 5.18.a with a resistive divider. The ‘short’ is obtained from this when considering either $R_1 = 0$, $R_2 = \infty$ ($BP = V_{dr}$), or vice-versa ($BP = V_{ss}$). Depending on the initial value of the body potential, compared to the shorted rail, there will be current flow from/to the tissue in order to equilibrate the potential between the two nodes. In the scenario of multiple satellite implants close to each other, it is usually preferred to connect the BP directly to all the satellite grounds ($GndS1, \dots, GndSN$).

The second ground referencing category is composed of active components forming the body referencing circuits (BRC). This can be further divided into two topologies: (1) driving BRC; and (2) sensing BRC. The driving reference circuit is shown in Figure 5.18.b consisting of a reference voltage generation circuit (e.g. a resistor divider) and an output buffer with a low output impedance to drive the BP . In both passive and drive schemes, there is current flow between implant and tissue. This ensures the voltage between BP and $GndS$ to be fixed, thus reducing the common-mode signal at the input of the recording amplifier, at the expense of current exchange between satellite module and body. Unlike for the passive scheme, the BRC with driver/buffer ensures that the current injected into or out of the tissue is limited and controlled, providing a level of stability to the source (satellite implant) from inherent fluctuations of the potential around BP .

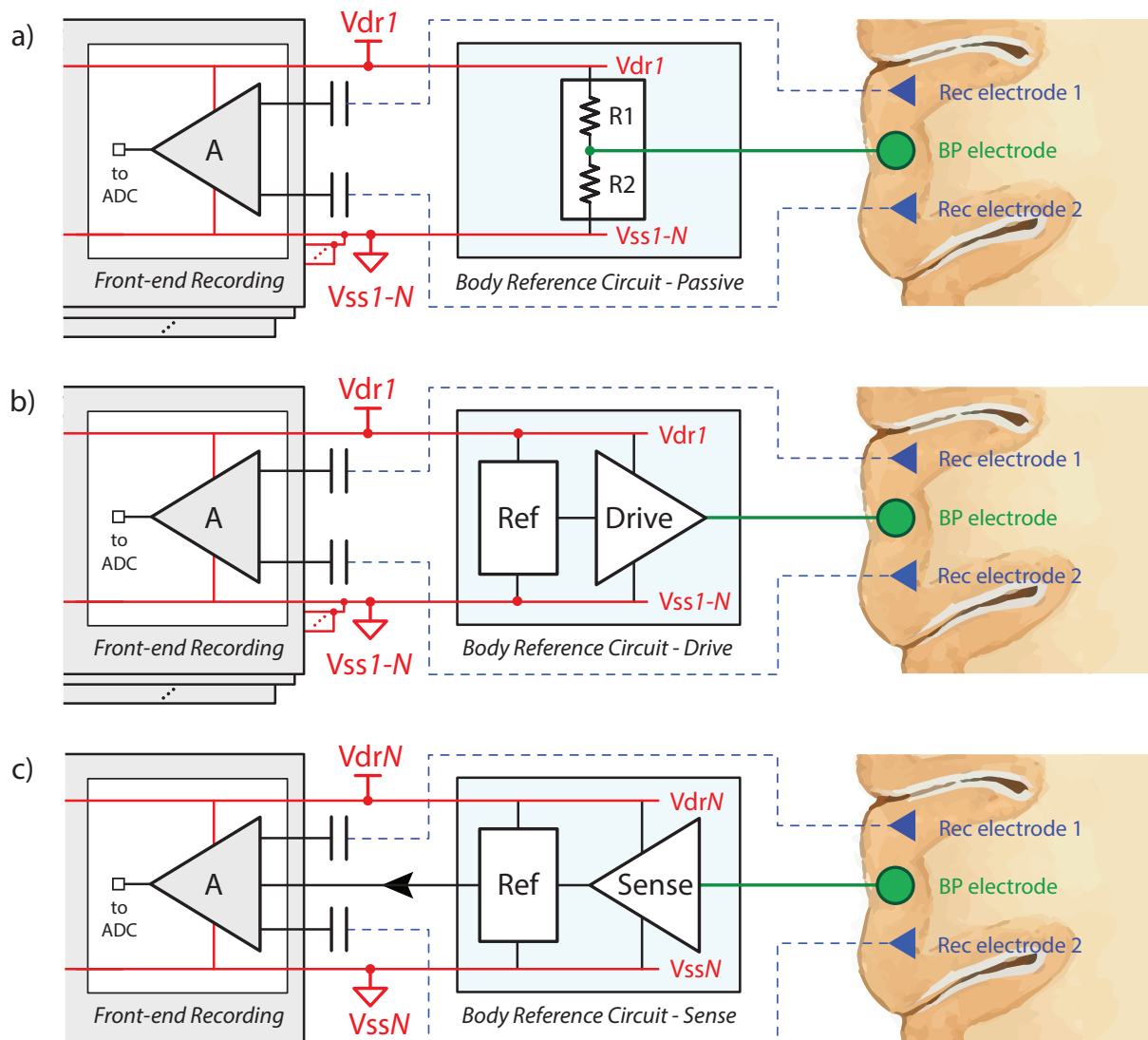


Figure 5.18: Different grounding schemes: (a) passive; (b) drive; (c) sense.

Figure 5.18.c presents a third scheme, based on a sensing BRC: this time, a front-end sensing circuit is used as body reference circuit to measure the BP instant value and references the satellite rails level accordingly. The sensed voltage ($BP - GndS$) can thus be sent to the recording amplifier, which uses it to adjust the input biasing point of the latter. By doing so, the body potential fluctuation itself, seen as common-mode from the recording input electrodes, is employed in fact as part of the common-mode rejection of the amplifier.

Insights to Practical Implementation

So far in the discussion, the interfacing between the BRCs and the body has been considered as ideal, with negligible parasitic elements and considering an ideal body potential electrode (BPE). When implementing the circuits in a specific technology and connecting them to the biological tissue, new challenges arise due to: (1) electrode interface (metal-tissue) non-idealities and; (2) circuit implementation constraints.

The electrical model of the electrode needs to be taken into account when evaluating the impact of the ground referencing in the different schemes, both for recording quality and safety limitations of current injection. A simplified model is presented in Figure 5.19. Capacitive coupling and current leakage from the power rails, represented by R_{leak} and C_{coup} , also affect the implant-tissue interfacing. This depends mainly on encapsulation and circuit technology.

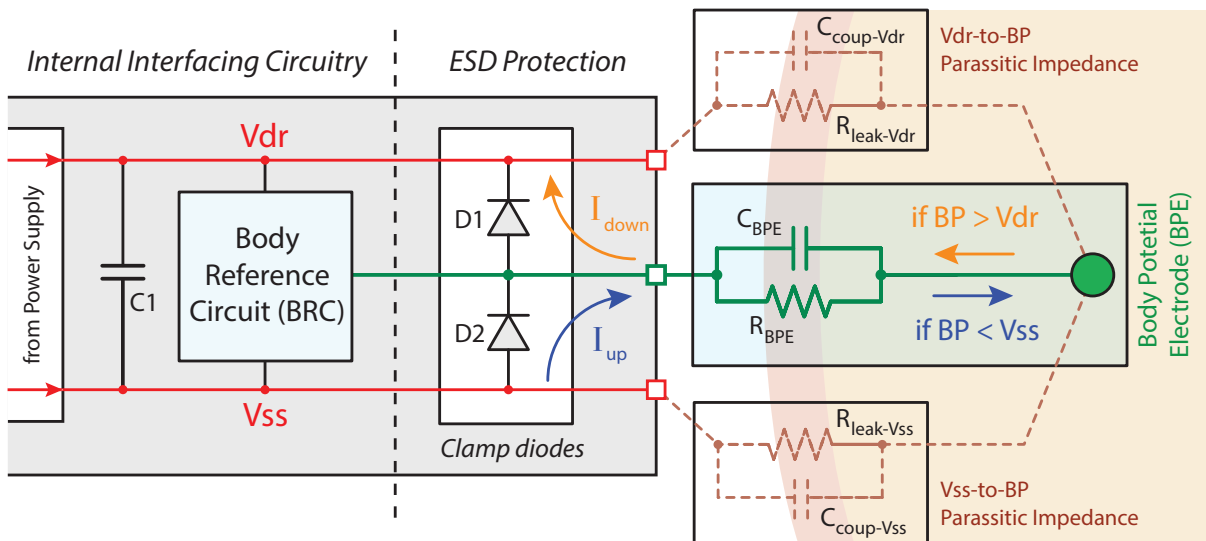


Figure 5.19: Practical implementation interfacing of the body reference circuit with the body potential (ESD, parasitic impedances, and BPE model).

The latter introduces another interfacing aspect: typically, in CMOS technology, integrated circuits require electrostatic discharge (ESD) protection at the interfacing pads, in order to prevent device malfunction or breakdown. This is usually implemented using reverse-biased pn-junction diodes, which ensure the potential at the pad doesn't exceed the upper and lower limits of the power rails ($V_{ss} < V_p < V_{dr}$). These diodes ($D1$ and $D2$ in Figure 5.19) add to the parasitic impedances of the implant-tissue interface, nonetheless, they prove to be advantageous in clamping the body-potential within the implant rail-to-rail range by providing a 'weak' leakage path.

Recording Performance and Safety Considerations

The three ground referencing schemes proposed in the previous section give a different contribution to the neural recording performance depending on the BRC implementation. As shown in Figure 5.20, where a schematics of BP to V_{ss} path is illustrated, the BRC and BPE impedances intervene in the modification of the total impedance path. By maintaining the latter a low impedance path, thus reducing the BRC common-mode gain A_{BRC-CM} , the common-mode fluctuations seen at the recording amplifier inputs are minimised.

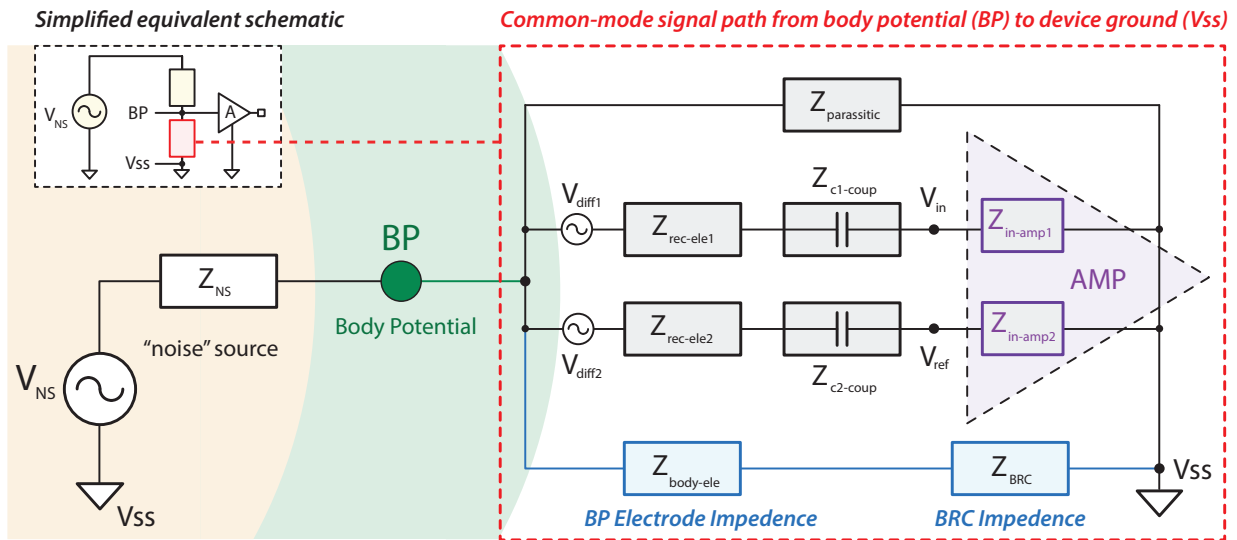


Figure 5.20: Common-mode signal path in an experimental setup. Noise sources (V_{NS}) are observed at the recording amplifier inputs via stray noise coupling impedance (Z_{NS}). The purpose of the body reference circuit is to shunt this common-mode signal to the recording amplifier ground such that it is attenuated at the recording amplifier input. There is essentially a potential divider between Z_{NS} and $(Z_{BODY-ELE} + Z_{BRC})$. It is therefore essential to maintain a low impedance BP drive relative to the recording circuit ground.

However due to the frequency response of the BRC, A_{BRC-CM} may increase with frequency and possibly reach its maximum theoretical value of 0 dB (open circuit), i.e. the common-mode noise adds directly on the recording inputs (V_{in} and V_{ref}) through the recording path. This is represented in the example plot in Figure 5.21 by the effective $CMRR$ at frequency f_2 . On the other hand, a zero impedance BRC (short circuit) would reduce to 0 the V_{NS} potential division on BP, thus cancelling out the common-mode signal. This scenario is theoretically possible, however, due to parasitic and electrode impedances, it remains a practical implementation challenge.

Besides altering the neural recording performance, the chosen grounding scheme and the technology features are key aspects for body safety requirements, since they define the electrical behaviour at the implant-body interface ($BP - GndS$ potential difference and current flow). Except for its intended function, active IMDs are required to be electrically neutral when in contact with the body and the maximum current density at the surface of an electrode is set to $\leq 0.75 \mu A/mm^2$ according to the directive, section 16, in [8]. For this reason, current limiters are necessary when employing driving ground referencing topologies, alongside implant encapsulation and implant-to-implant electrical isolation.

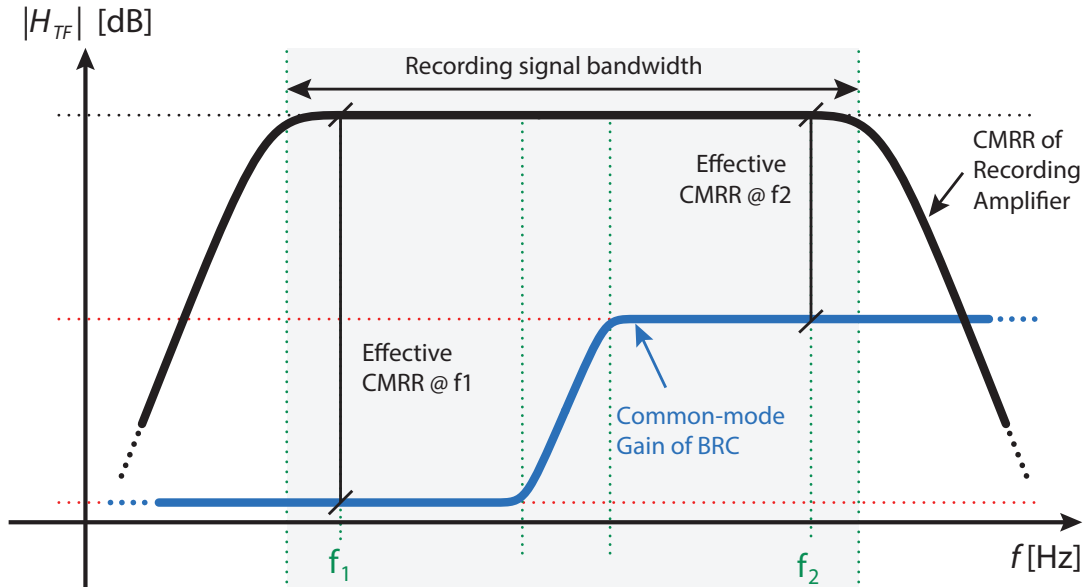


Figure 5.21: Common-mode Rejection Ratio (CMRR) of Recording Amplifier and Common-mode gain of Body Reference Circuit (BRC) with the effective observable CMRR being the difference between these responses. The BRC configuration, i.e. impedance of BP relative to recording amplifier ground, determines the magnitude and frequency dependence of the common-mode signal observed at the amplifier inputs (V_{in} and V_{ref}). This is critical for experimental design.

5.3.2 Measurements and Results

In order to identify the impact of the different sources of interference on the recording performance and how the above-introduced ground referencing scheme can reduce it, a testing setup was assembled as shown in Figure 5.23 for experiments in saline. Initially, the effect of the 4WiCS communication signals is investigated. The end-to-end 4WiCS platform was employed in the setup, with at the brain implant a single satellite module PCB. This powers up the core optrode circuits, thus the front-end recording amplifier.

In addition, an off-the-shelf component was used to generate a mid-rail voltage to implement the BRC for the ‘drive’ grounding scheme presented above. Such voltage rail-splitter, the TLE2426 from Texas Instruments, generates a low-impedance buffered output of 2.5V and is powered from the V_{dd} power rail of 5V. The ‘short’ grounding scheme was implemented as well to compare the effects on the neurosignal recording of the two different configurations. The ‘sense’ scheme was not used in this experiment due to its implementation complexity in a bench-top setup. A 10Ω body potential electrode, designed by the microfabrication team within the CANDO project, was employed to recreate a realistic impedance path for the body potential referencing.

Measurement Setup

Two identical wires connected to the differential inputs of the recording amplifier were therefore immersed into a container filled with 0.9% saline solution (9 gr of NaCl in 1 litre of distilled water) emulating the the human body tissue, as illustrated in Figure 5.23 [180]. The output of the amplifier was measured with a differential probe and displayed on an oscilloscope. The body potential electrode is introduced as well in the solution and initially connected to the V_{ss} rail generated from the 4WiCS power management circuits, thus using the ‘short’ grounding configuration. In order to mimic the neurosignal activity of the brain, the solution was driven by a signal generator, injecting a sinusoidal signal with 500 Hz frequency and a tunable amplitude. This is required to ensure the signal amplitude seen at the input of the differential amplifier is

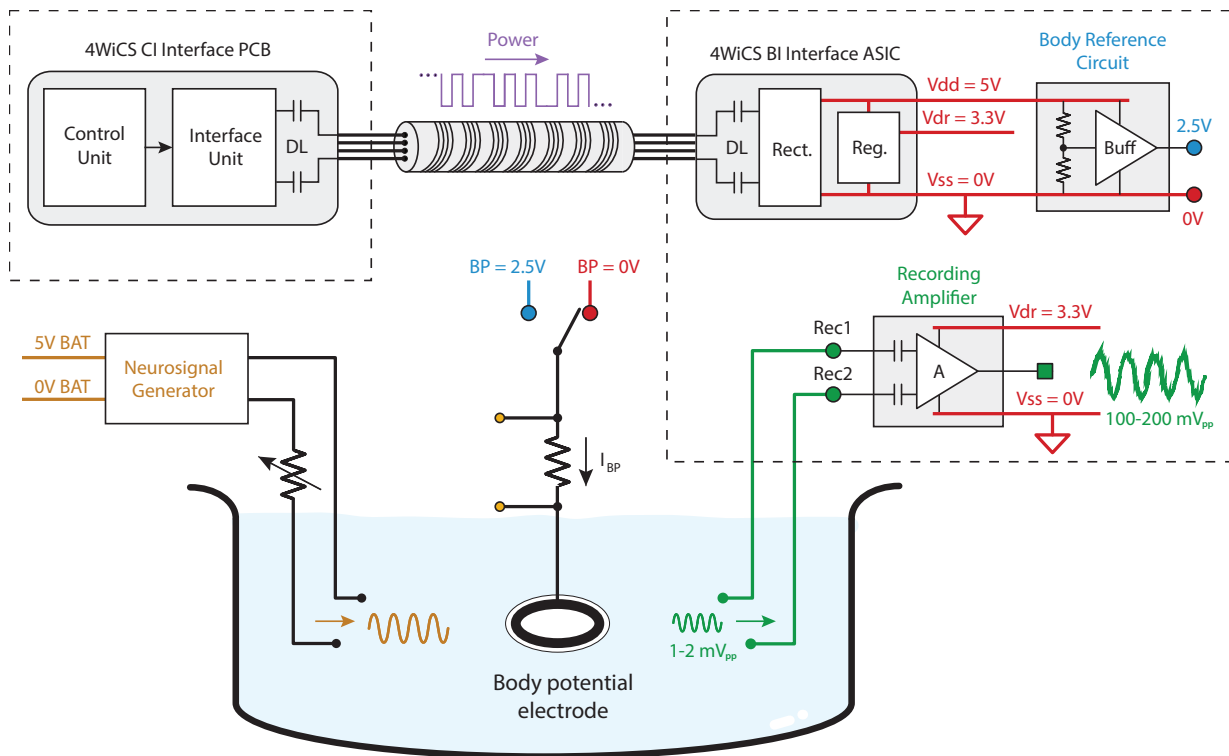


Figure 5.22: Experimental setup for the 4WiCS interference testing. On the top, the end-to-end 4WiCS platform is used to generate the signals to power up the body reference circuit and the recording system. On the bottom, the saline solution together with the neurosignal generator, emulate the brain activity recorded by the front-end differential amplifier.

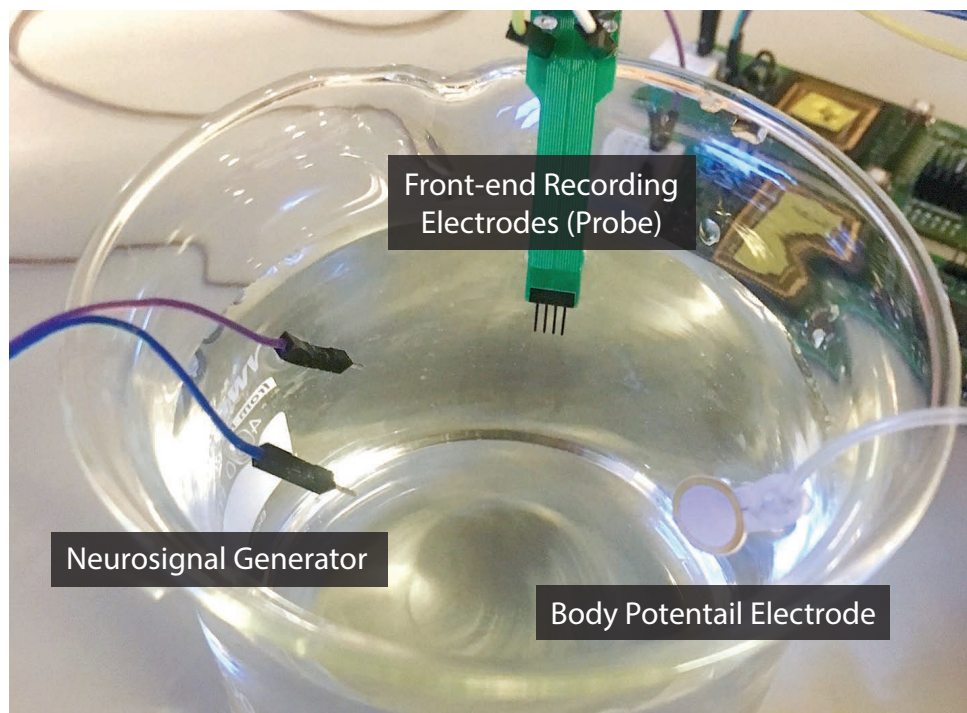


Figure 5.23: Experimental setup picture.

in the range of 1-2 mV – typical value for the amplitudes of the neurosignals of interest. It's crucial moreover that the signal generator is powered up by an external isolated energy source (battery) to avoid ground loops, which would compromise the accuracy of the recorded signals.

Experimental Results

The measurement results are presented in Figure 5.24 and Figure 5.25. In the first case, the implantable cable was maintained far from the saline solution to avoid direct electrical coupling through the solution. The 500 Hz sinusoid representing the neural signal of interest is measured to be 130 mV_{pp} (-13.7 dBm) from frequency domain obtained with the Fast Fourier Transform (FFT). Peaks of the power spectral density at the fundamental frequency of 200 kHz (2 mV_{pp}) and its harmonics can be noticed on the FFT, contributing to a total summation of the noise components of 44 mV_{pp}. Therefore, from the frequency domain analysis of the amplifier output signal is clear that the squarewave signal on the downlink path interferes with the recording, since such signal switches polarity at a frequency of 200 kHz. Furthermore, the squarewave contains a wide range of harmonics that can generate electromagnetic radiation and pulses of current that interfere with the recording system both through EMI radiations (through air-solution path) and electric coupling through power supply circuits. Although the CMRR and PSRR of the recording and power supply systems should reject such interference, this is not negligible and add up as a noise component to the output signal of the neural amplifier.

This is demonstrated also in the second experiment performed by moving the implantable lead of the end-to-end platform this time close to the recording system and partially immersed in the saline solution. By doing so, the coupling through the wires in the cable and the recording system is expected to be strengthened, thus the interference increases. The measurements of the amplifier output, shown in Figure 5.25, confirm the interference is increased by ~33%, with a total peak to peak noise component of 59 mV, without altering the measured amplitude of the sinusoidal neurosignal.

While maintaining the rest of the setup configuration unchanged, further tests were performed by modifying the grounding scheme from 'short' to 'drive'. This was obtained by connecting

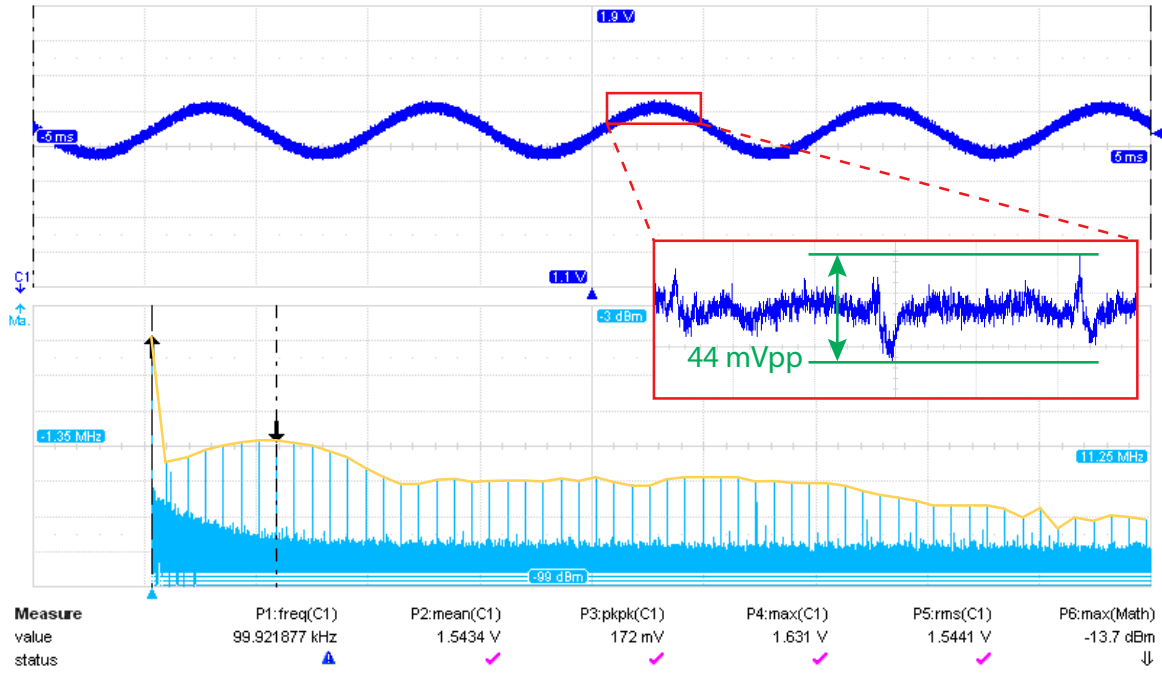


Figure 5.24: Oscilloscope measurement of the recording amplifier output of an ideal sinusoidal neurosignal, shown both in time and frequency domain (FFT). The saline solution is grounded to V_{ss} through a $10\ \Omega$ electrode. The implantable lead is in air, not in contact with the solution.

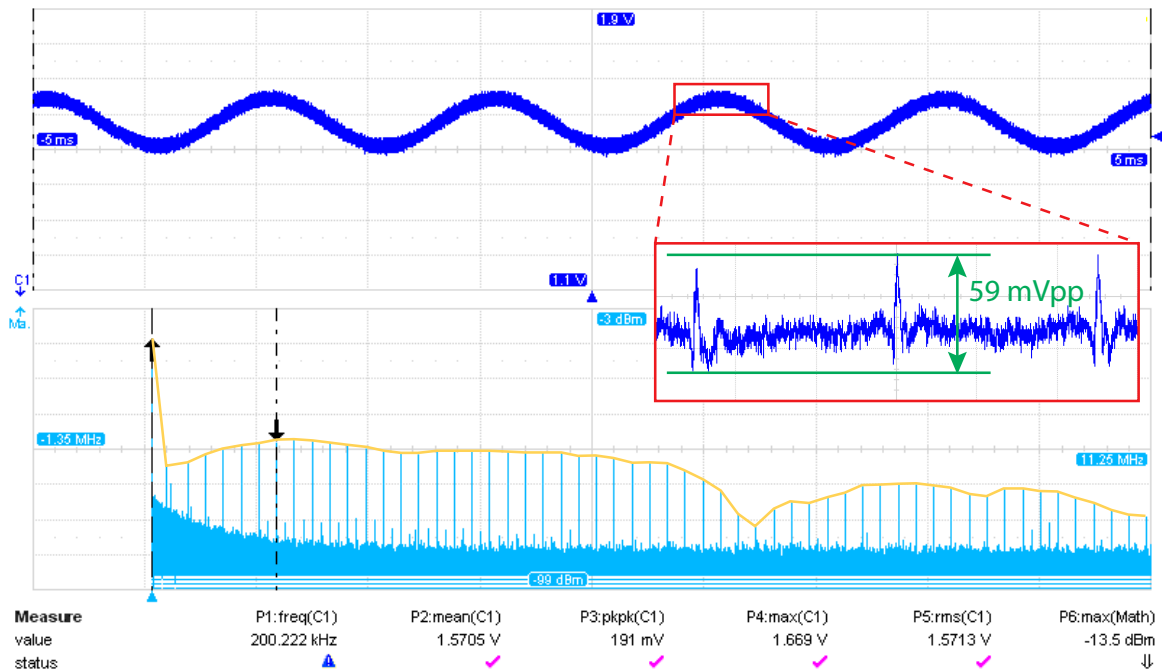


Figure 5.25: Oscilloscope measurement of the recording amplifier output of an ideal sinusoidal neurosignal, shown both in time and frequency domain (FFT). The saline solution is grounded to V_{ss} through a $10\ \Omega$ electrode. The implantable lead is immersed in the solution.

the body potential electrode to the 2.5 V output of the BRC – generated by the rail-splitter. Although the power spectral density differs slightly in the two cases, measurement results don't show significant variability of the two configurations in terms of total noise/interference performance of the recording system. Nevertheless, compared to the scenario of no body potential referencing/grounding, thus with no BPE connected to the saline solution, both the 'short' and the 'drive' schemes shown interference reduction. In fact, the total noise component when no grounding is implemented was measured to be of the order of the sinusoidal neurosignal (110.6 mV_{pp}), making the latter unreadable (Figure 5.26).

The tests performed so far have demonstrated that the CANDO implant system can be subject to forms of electromagnetic interference and internal coupling (1) between different circuits within the same satellite module and (2) between implants and communication signal paths. Such interference adds up as a noise component at the front-end recording but can be reduced with a proper potential referencing between device power rails and tissue. Further experiments with multiple satellite recording modules will give more insights into the impact of such interference/coupling on multi-module implant systems.

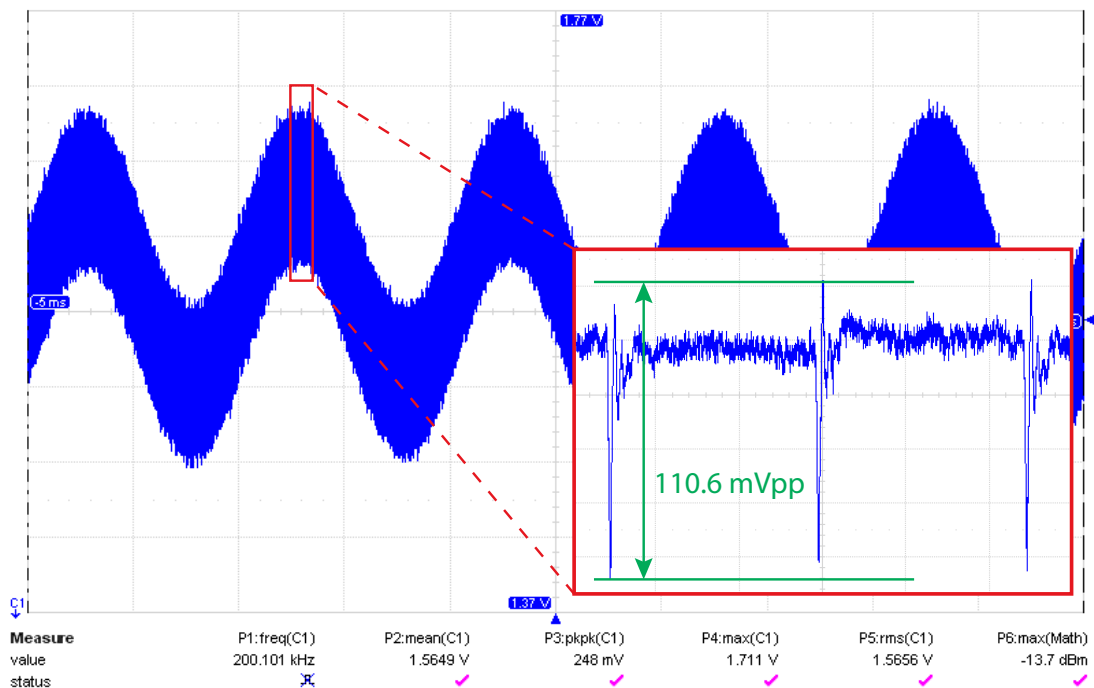


Figure 5.26: Oscilloscope measurement of the recording amplifier output of an ideal sinusoidal neurosignal. The saline solution is not grounded and left floating. The implantable lead is immersed in the solution.

5.4 Summary

This Chapter has discussed the implementation of a demonstration platform to verify the functionality and performance of the 4WiCS end-to-end interface. Such platform aims at creating a realistic setup and environment, in order to emulate 4WiCS operation within an in-body implant system. First, the E2E platform was presented, comprising the components of the 4WiCS interfacing system introduced in Chapter 4. Given its complexity – 15 off-the-shelf integrated circuits, 8 custom integrated circuits, 5 FPGAs and over 300 passive components – the E2E demo platform was tested following a specific startup/power-up sequence to ensure correct functionality of all stages.

Furthermore, both (1) the CI-to-BI power delivery and (1) bidirectional data communication have been verified and characterised. For the former, the voltage range and ripple of the rectifier output has been used as a measure of the ability of the system to provide stable supply, while the PTE is employed for evaluating the capability to efficiently deliver power from power source to power consumption units. With regards to the data communication, the end-to-end system functionality was demonstrated by verifying the commands sent from CI to BI were correctly decoded, interpreted, and acknowledged by the optrodes. A simple “LED-ON/LED-OFF” sequence of commands (per each optrode) was used for this purpose. Moreover, the BER was used as a performance metric for the downlink and uplink communication, showing high reliability of the interfacing link in both directions.

The test performed with the E2E platform raise discussion points about the efficiency of the power delivery path in a multi-module implant system, highlighting the need for establishing an in-depth power management strategy. This should take into consideration the key factors when designing a power management system with multiple transfer and conversion stages – both from a clinical/user and a technical/design perspective. These are (1) the medical application and energy supply, (2) the functional requirements and implant lifespan, and (3) implementation constraints and number of modules. Such factors have been discussed and applied to the strategy used for the power management of the CANDO implant system, to ultimately maximise the system efficiency.

Finally, when creating a medical device, it is particularly important to ensure that the support/connectivity functions (power supply and data communication) don't interfere with, or disrupt, the core functions (recording and stimulation) and don't compromise patients safety. For this reason, design consideration on system reliability and recording performance have led to the definition of the ground referencing schemes. These are required in order to maintain good neurosignal recording quality of the optrodes while limiting excessive current exchange between the the electronic devices and the biological tissue, thus ensuring device reliability and ultimately patient safety. In-saline tests have demonstrated the need for ground referencing in order to reduce the impact of both internal and external sources of noise and interference.

The above-presented considerations, tests, and results have directly informed the design of the 4th generation of the CANDO optrode microelectronics (CANDO4), which includes the 2nd generation of the 4WiCS BI interface. The latter will be described in detail in the next Chapter 6. Additional circuits have been added to the CANDO4 4WiCS IC – e.g. body potential driver – to address the challenges and limitations presented in this Chapter.

Chapter 6

CANDO4 System-on-Chip: Next Generation Implantable Microelectronics

This Chapter¹ describes in detail the design of the **CANDO4 System-on-Chip (SoC)** and its implementation in 180 nm CMOS technology. This integrated circuit is the 4th generation of the CANDO microelectronics and includes updated versions of the CANDO3 ASIC and the 4WiCS ASIC, introduced in the previous Chapters. The CANDO4 SoC is intended to be employed both as a research tool for experiments in animal models and as part of the medical device for first-in-human clinical trials. This system, therefore, addresses the limitations of the previous generations of ICs to allow for the expected application flexibility and to meet the requirements for regulatory approval. As such, the *Microelectronics Specification Documents* have been drafted in parallel with the development of the CANDO4 SoC and included within the CANDO regulatory documentation. The content presented in the following is partially derived from such specification documents.

¹The designs, implementations, tests, and results presented in this Chapter are obtained from the research pursued within the CANDO project. They derive from collaboration with colleagues, peers, and students from the Centre for Bio-inspired Technology of Imperial College London, promptly cited in the relative sections. The system architects and circuits designers of the CANDO4 SoC – and authors of the CANDO4 specification documentation – are Mr Dorian Haci (Ph.D. thesis author), Dr Yan Liu, and Dr Timothy Constandinou.

First, the latest generation of the CANDO implantable system is introduced, with relevant updates on the system specifications. These derive from (1) the technical requirements and specification of the previous versions of the implant system – as discussed in Chapter 3 – and (2) from the design considerations and testing results discussed in Chapter 5. The definition of the high-level system specifications leads to the revision of the technical specifications of the optrode microelectronics – CANDO core functions circuits (CORE) and of the inter-module interfacing circuits (4WiCS). Therefore, a description of the CANDO4 SoC architecture and circuitry is hereby given, detailing the features of its two sub-systems – *CANDO4 CORE* and *CANDO4 4WiCS* – with particular focus on the latter circuits and modifications from the previous 4WiCS generation. Finally, the integration of these two blocks within a system-on-chip is discussed and contextualised as part of the CANDO implantable medical device.

6.1 Towards a First-In-Human Trial

The engineering team of the CANDO project has delivered in the years various prototypes of the implant system. These have been developed considering the ultimate application as a medical device for in-human clinical trials. Nevertheless, as the CANDO project is an academic endeavour and not a product-driven industrial venture, the implementation of the prototypes has been optimised for intermediate tests and experiments that have led to research publications and technical reports, key outcomes for meeting the project milestones. For this reason, besides the 4WiCS E2E platform discussed in the previous chapter, other prototypes/platforms have been implemented. These are not only for functional and performance tests of the electronic system but also for validation of the CANDO approach to treating focal epilepsy. Laboratory tests in emulated environments (e.g. saline solutions) and experiments in-vitro and in-vivo – first in small animal models (i.e. rodents) and then in large animals (i.e. non-human primates) – have been performed with different platforms optimised for the specific application, as introduced in Chapter 3 (Section 3.2). Examples are shown in Figure 6.1, Figure 6.2, and Figure 6.3. Such prototypes employ the 3rd generation of the microelectronics, CANDO3 ASIC, as optrode electronics. This is addressed and controlled by a *processing unit* through SPI serial

communication and powered-up with DC supply by external *power management units*.

In order to develop a medical device that is able to safely and effectively operate in human, the next generation of the CANDO implant system, hence also the CANDO brain implant, needs to comply with the relevant directives and standards and meet the essential requirements to provide therapeutic benefit for the patients. This, together with the results obtained from previous implementations, leads to the creation of the specifications for the physical construction for the 4th generation of the brain implant, as illustrated in Figure 6.4. Similar to the previous generations, the proposed BI architecture is based on a multi-optrode array sitting on a base-plate. This time, however, limitations are given for the optrode arrangement and dimensions (width and height), and for the integration technique of the microelectronics within the brain implants - wire-bonding to the physical optrodes.

6.1.1 Microelectronics Requirements

In parallel with BI construction specifications, also technical requirements are set for the optrode microelectronics, both from a physical and electrical perspective. Accordingly, both functional and performance limitations of previous designs (CANDO3 ASIC and the 4WiCS ASIC) are addressed in the definition of the technical requirements for the 4th generation of the microelectronics: the **CANDO4 system-on-chip**. These are listed in the following, categorised by primary characteristics and functions:

- APPLICATION:
 - **Medical Device:** design to be compliant to the ‘*active implantable medical device*’ directive for use within an implantable system for clinical trials delivering an optogenetic closed-loop treatment to epileptic patients.
 - **Research Tool:** versatile design to allow for (1) separate use as a stand-alone module in tests to validate functionality and performance, (2) exploratory studies in neuroscience experiments, (3) pre-clinical validations of the closed-loop treatment.

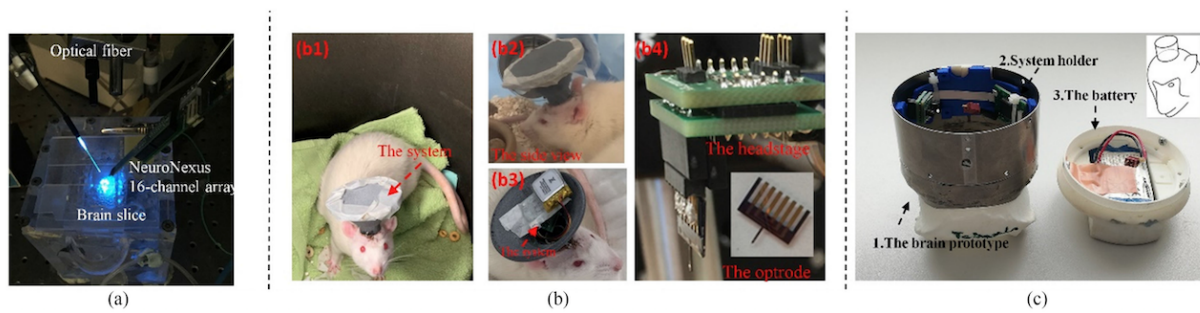


Figure 6.1: Prototypes of the CANDO 'control system' employed for tests in animal models [154].

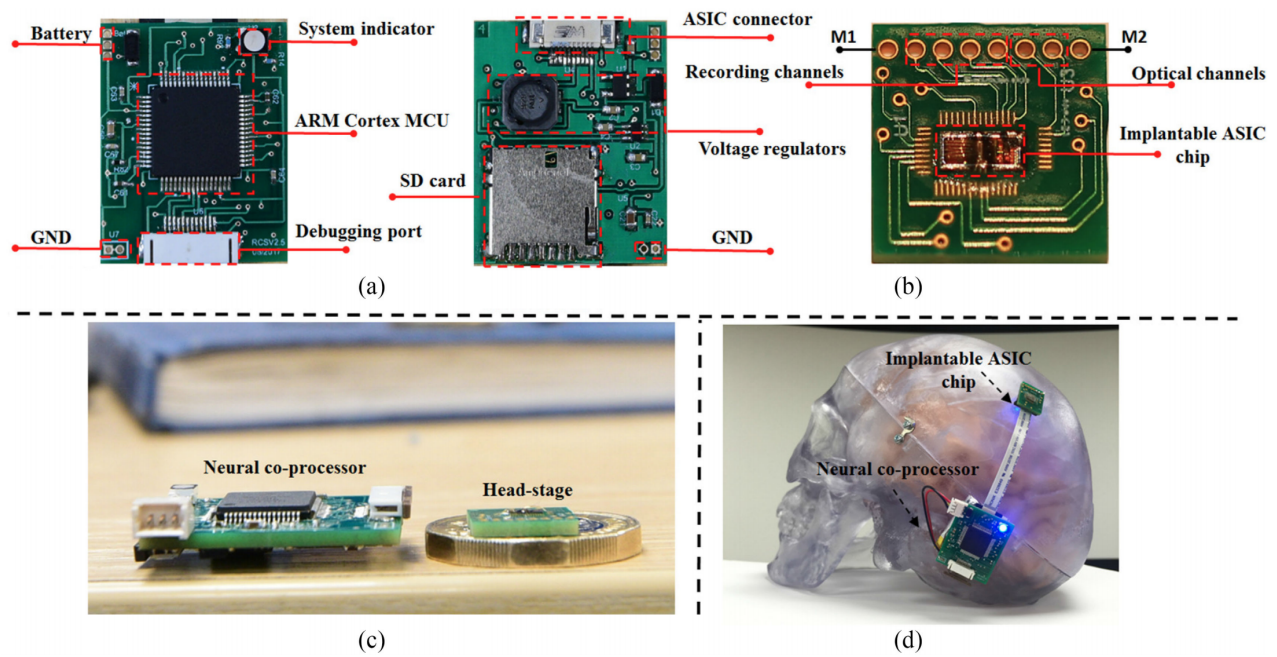


Figure 6.2: Prototypes of the CANDO 'control system' including the CANDO3 ASIC [154].

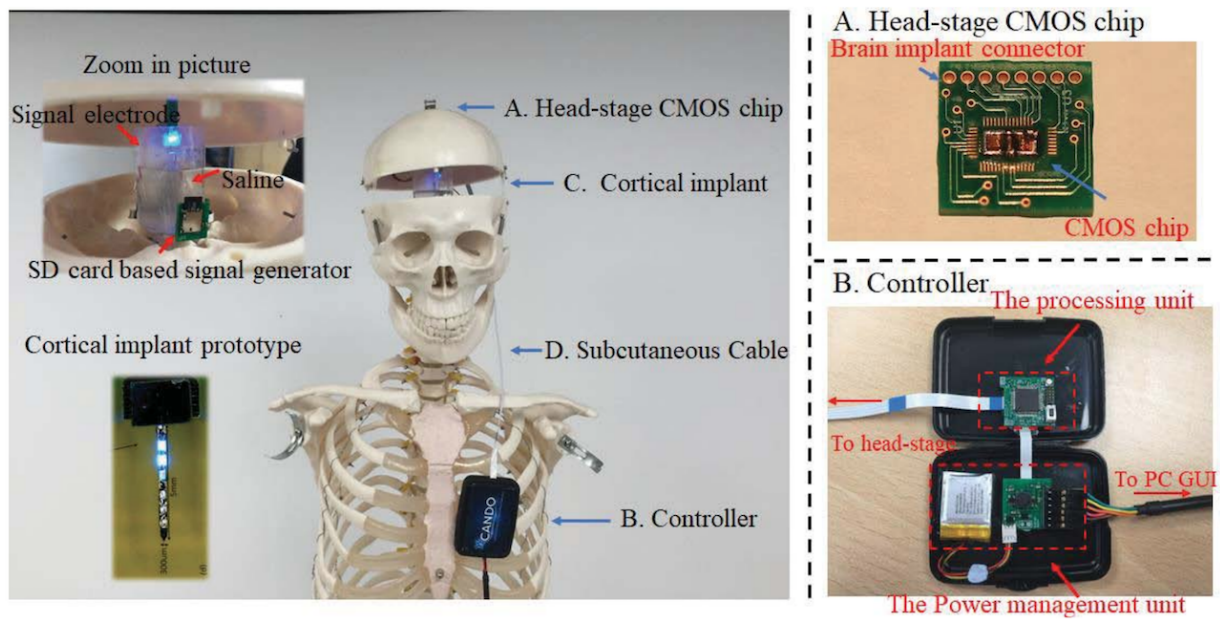


Figure 6.3: Demonstration platform of the CANDO implantable system – including one CANDO3 ASIC controlled through SPI communication DC powered [181].

- **CONFIGURATION:**
 - **Architecture:** to (1) allow for one chip to operate with a *multi-optrode fork* (array of 4 passive optrodes) and (2) enable up to 4 forks (16 optrodes) to connect using the 4WiCS protocol and a parallel 4-wire connection.
 - **Physical Features:** to (1) fit a multi-optrode (fork) head, (2) be compatible with a reliable bonding technique, (2) facilitate integration of external passive elements (e.g. additional capacitors).
 - **Backward Compatibility:** to allow compatibility with previous prototypes and 4WiCS end-to-end platform, with minimal adjustment for system integration.
- **CORE FUNCTIONS:**
 - **Stimulation:** drive up to 16 LEDs (4 LEDs/optrode) using a balanced driving scheme to avoid encapsulation degradation due to static electrical fields.

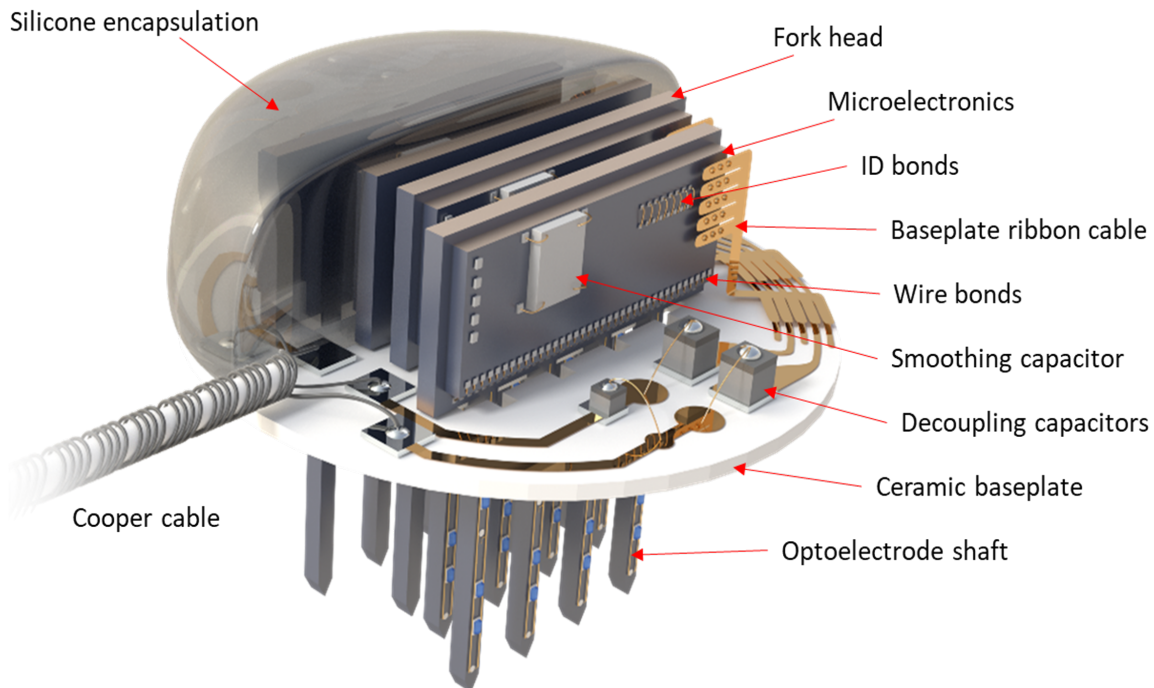


Figure 6.4: Concept illustration of the CANDO4 brain implant construction. The proposed architecture comprises four multi-optrode forks integrated within a ceramic baseplate that provides physical structure and connections. Each fork includes a CANDO4 SoC, bonded to the fork head. Passive components, i.e. decoupling capacitors, equalization capacitors, and ribbon cable, provide an interconnection path to the 4-wire Copper cable. The whole brain implant is encapsulated with a polymer-based package.

- **Recording:** monitor LFPs and APs with up to 8 neural recording channels (2 channels per optrode) by using differential inputs with adequate CMRR.
 - **Body Potential:** safe electrical bias of the body potential for (1) improved recording performance and (2) reduced static electrical fields on stimulation sites.
 - **Diagnostics:** ability to characterise/interrogate all connections of the optrode during operation for real-time functional examination.
 - **Control:** FSM-based on-chip digital controller with instruction set optimised for (1) both individual and group operations, (2) risk mitigation with "fail-safe" mode, and (3) flexible data communication protocol (4WiCS SPI).
- **INTERFACING FUNCTIONS:**
 - **Power Supply:** receive AC power via 2 wires (from 4-wire lead) and supply on-demand DC power to all circuitry of the system-on-chip, prioritizing efficiency.
 - **Data Communication:** provide (1) full-duplex communication with error detection using a 4WiCS bus (shared among all optrodes) and (2) an auxiliary SPI interface.

6.1.2 System-on-Chip Specifications: CANDO4

The CANDO4 SoC is conceived to monolithically integrate all active electronics within a multi-optrode fork in a single ASIC, thus including circuits designed to perform all of the above-mentioned functions:

1. *LED stimulation drivers* – for activation and control of optical illumination;
2. *Front-end analogue recording* – for measuring and monitoring neural activity;
3. *Diagnostics instrumentation* – for functional ‘check-up’ of the optrode connections;
4. *Digital control unit* – for managing command interpretation and data configuration/control;
5. *Power management unit* – for supplying correct voltage/current levels to all the circuits;
6. *Data communication unit* – for external interfacing with SPI and 4WiCS protocols;
7. *Body potential driver* – for biasing the tissue with current-monitored electrical contact.

Table 6.1: Comparison between CANDO3 ASIC and CANDO SoC Specs

Function/Circuit	CANDO3 (per single optrode)	CANDO4 (per 4-optrode fork)
<i>Stimulation</i>	8 LEDs unbalanced biphasic via either V or I mode	4 LEDs per optrode (16 LEDs in total), I-mode fwd-bias, V-mode, balanced rev-bias
<i>Recording</i>	2 bipolar channels per optrode with common ref (3 inputs), LFP only	2 bipolar channels per optrode with common ref (3 inputs, 8-ch tot), LFP & EAP
<i>Diagnostics</i>	DC I-V hardwired to LEDs	Generic DC I-V (to probe any optrode I/Os – e.g. for LEDs, leakage, thermal)
<i>Control</i>	FSM with 28-command interpreter	FSM with 22-command interpreter (including group operations & stim timeout)
<i>Power</i>	3 power inputs (vv5, vdd3, avdd3) 3 ground inputs (vss5, vss3, avss3)	4-WICS (modular sub-system) or 2 power supply inputs (vdd, vss)
<i>Data</i>	SPI + CLK + RST (6 wires)	SPI + CLK + RST (6 wires) or 4-WiCS (modular) + error detection
<i>BP driver</i>	VSS hard-wired	VSS hard-wired or active AGND (monitored)

The primary specifications of the CANDO4 SoC are listed in Table 6.1 and compared with the CANDO3 ASIC specifications. This highlights the key limitations (e.g. interfacing) addressed by CANDO4 and the main changes from the previous microelectronics generation.

Modular configuration

Differently from its predecessor, CANDO4 includes in the same integrated circuit both the core and the interfacing functions. In fact, despite comprising an SPI interface, the CANDO3 required the addition of the 4WiCS ASIC, passive elements, and the 4WiCS-to-SPI bridge to extend the interfacing capabilities to the 4WiCS protocol, thus allowing to connect to the medical-grade communication channel as shown in Chapter 5. Although not necessary for benchtop tests and in-animal experiments, compliance with the 4WiCS interface is required for in-human use, since the SPI interface alone doesn't meet the power management and data communication constraints (e.g. number of wires, multi-module parallel addressing, power domain) and the scalability requirements. In order to meet the above-presented requirements, the CANDO4 microelectronics is proposed with a modular configuration: the SoC electronics is partitioned into separate sub-systems: the CANDO4 CORE and the CANDO4 4WiCS. These are physically co-located (i.e. on the same chip), but not electrically connected directly on-chip.

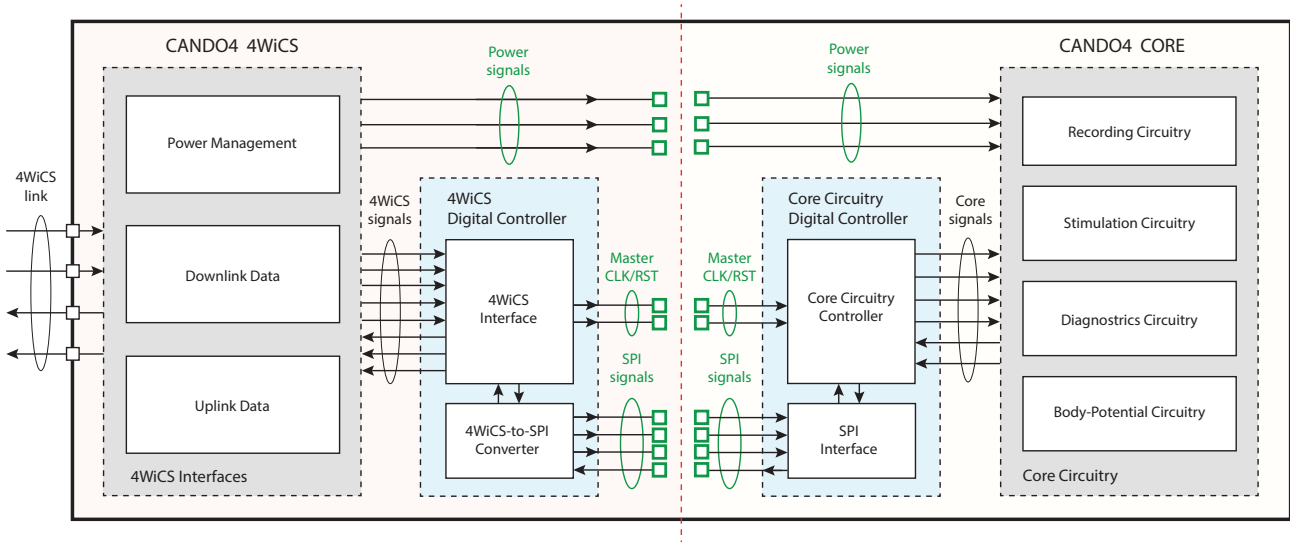


Figure 6.5: Modular approach of the CANDO4 SoC: the system is partitioned into two integrated sub-systems that are not electrically connected. The connection can be achieved by shorting the corresponding physical bondpads (green pins in the figure), allowing for power to be supplied from 4WiCS to CORE and for internal SPI communication to be established.

This configuration is chosen for its flexible design that allows employing the same chip both as part of neuroscience research tools for experimental work and within the CANDO medical device for clinical trials.

- **Use in a research tool:**

The CORE sub-system can be used as a peripheral device connecting with a microcontroller or embedded system via the SPI bus and powered from a DC power supply. They can connect to the CORE system by bypassing the 4WiCS interfaces through available bondpads. This provides backward compatibility with SPI-based experimental prototypes, allowing for the previous CANDO3 chip to be easily upgraded to the CANDO4 SoC.

- **Use in a medical device:**

For the integration of CANDO4 within the CANDO multi-optrode array, the 4WiCS subsystem is needed to meet the clinical requirement. In this configuration, the CORE system and 4WiCS interface can be connected with each other using bondwire links. It would additionally be possible to hardwire these in the future by simply adjusting the metal connections within the CMOS design (e.g. by shorting across the physical bondpads) with no edits to the circuitry.

External communication interface

The modular approach, therefore, allows for the two sub-systems to be electrically independent, despite being monolithically integrated and fabricated as part of the same chip. This makes the CANDORA SoC addressable in two different ways: (1) with SPI protocol (connecting directly to the CORE sub-system); (2) with 4WiCS protocol (connecting to the CORE through the 4WiCS sub-system).

1. *Serial Peripheral Interface (SPI):*

The CORE system communicates using a standard SPI interface consisting of four signals: an active-low chip select (CS); a serial data clock (SCLK); a “Serial Data In” data line (SDI) to receive commands from the master device; and a “Serial Data Out” data line (SDO) to send results from prior commands to the master device. In addition, two other inputs are required for the proper functioning of the CORE sub-system: MCLK (master clock) and MRST (master reset) to drive the internal controller.

The CORE system always functions as the SPI slave device. The SPI interface can be used in conjunction with the 4WiCS interface (that translates the 4WiCS protocol to SPI), or directly to an external SPI master/controller (standalone configuration for interfacing to a single chip).

When multiple slaves are addressed by the same master, two configurations are possible, as shown in Figure 6.6 and Figure 6.7:

- (a) *Multi-slave selectable SPI configuration*: shared (parallel) connection for SCLK, MISO, and MOSI and separate lines for CS (Figure 6.6). Although it has the capability to address multiple devices concurrently, it can communicate only with one at a time, by employing time-division multiplexing - enabled by timely CS activation.
- (b) *Multi-slave active SPI configuration*: shared SCLK bus, but independent CS, MISO, and MOSI lines (Figure 6.7). This type of configuration (effectively using multiple independent SPI buses) can be used to address multiple devices, all communicating concurrently.

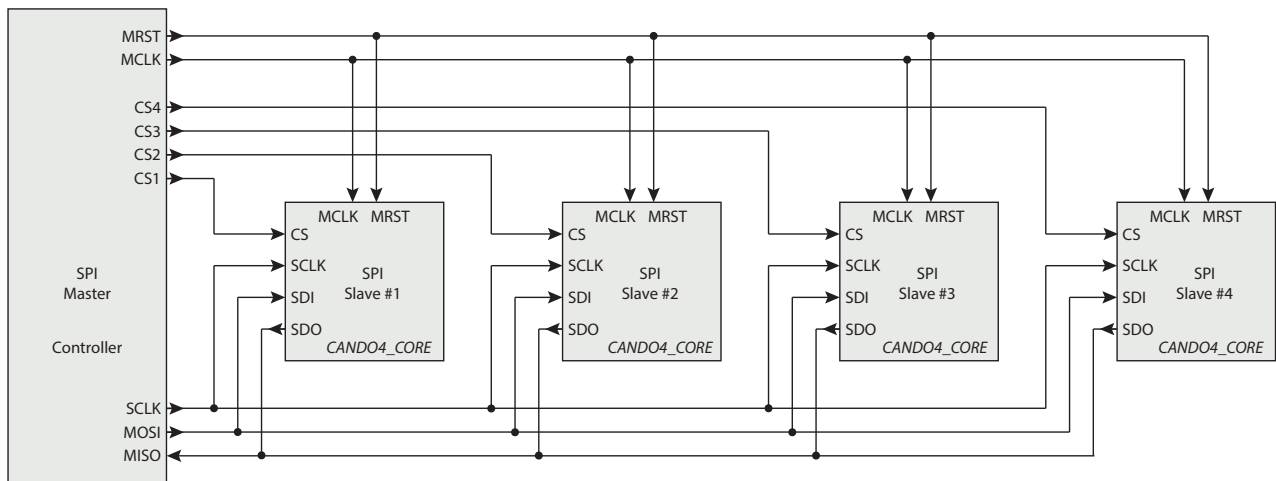


Figure 6.6: Multi-slave SPI configuration using shared (parallel) MISO/MOSI lines. This allows for a single (CANDO4) slave device to be active at a time.

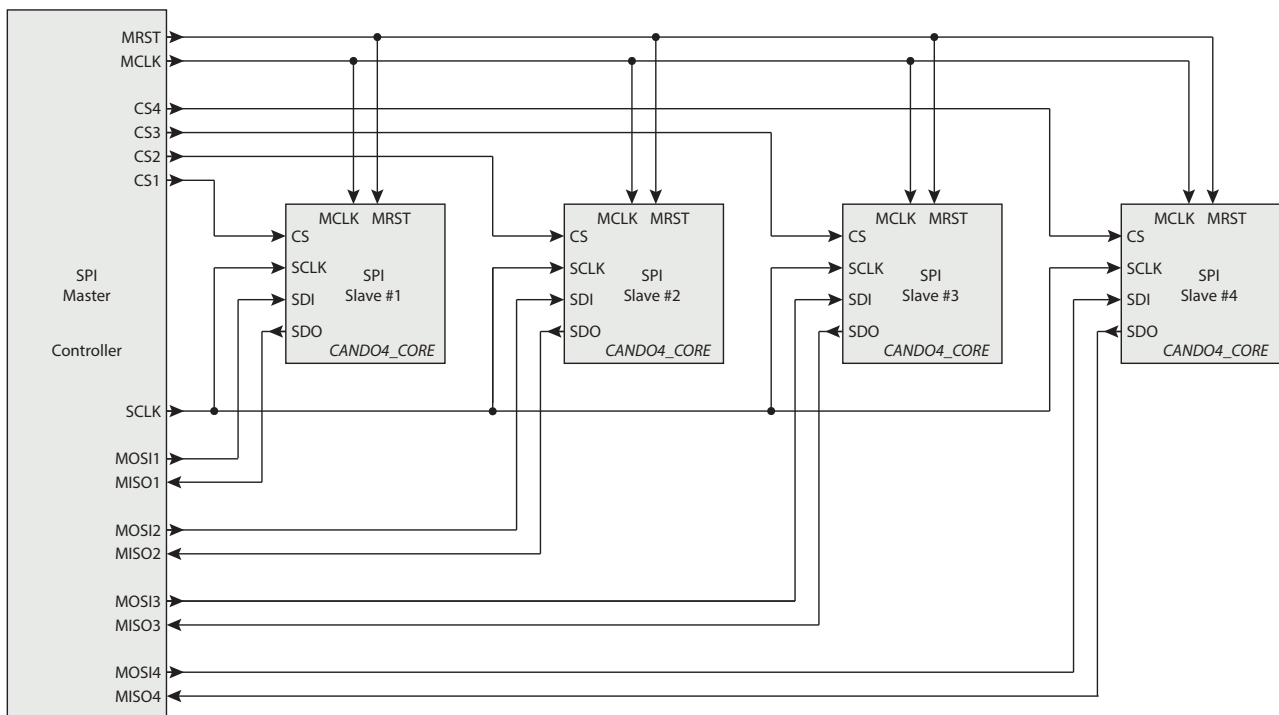


Figure 6.7: Multi-slave SPI configuration using independent lines. This allows for multiple (CANDO4) slave devices to be concurrently active.

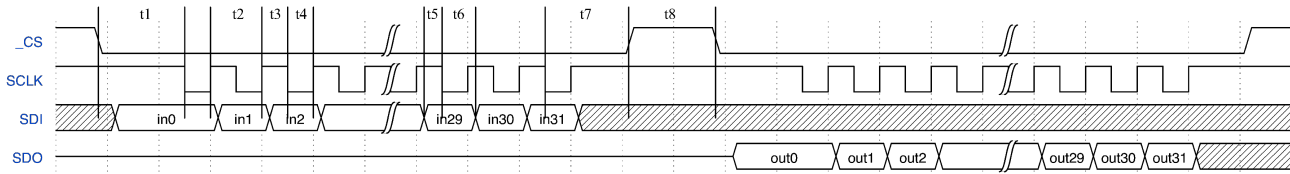


Figure 6.8: Timing diagram for SPI communication.

The low-level implementation of the SPI interface is designed according to the standard protocol, configured using the parameters specified in Table 6.2. This uses the same configuration of SPI protocol as implemented previously for CAND03 (with the exception of data length: 24-bit in CAND03 vs. 32-bit in CAND04). The communication is based on a bidirectional half-duplex link (i.e. 32-bit input word/packet followed by 32-bit output word/packet) with a typical timing diagram shown in Figure 6.8.

2. 4-Wire Communication System (4WiCS):

In addition to the SPI interface, CAND04 includes the 4-Wire Communication System (4WiCS) interface. This will allow multiple devices to be powered from and communicate bidirectionally (i.e. between master and multiple slaves) using a shared 4WiCS bus (4-wire cable). The 4WiCS proprietary protocol and interface have been developed for CAND0 to address a number of critical challenges that relate to its use in an implantable device. Such requirements cannot be met using standard ICT communication protocols (e.g. I2C, SPI, CAN, USB, etc). The 4WiCS protocol and interface features have been largely discussed in Chapter 4 and Chapter 5.

Table 6.2: SPI Configuration Parameters

Parameter	Value
Data Packet Length	32 bit
Data Rate	3200 kbit/s
Shift Direction	LSB first
Clock Polarity	Idle logic high (1)
Clock Phase	Falling-edge sample & trigger

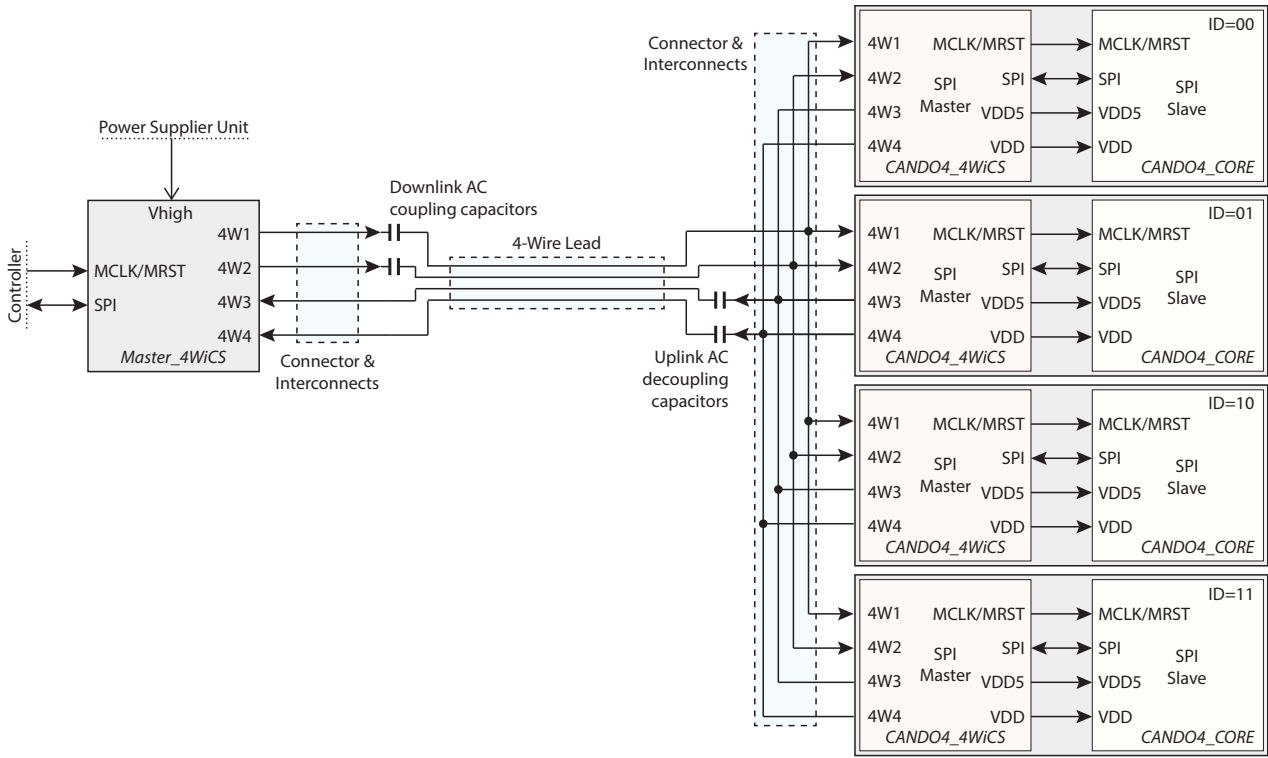


Figure 6.9: Multi-slave 4WiCS configuration using shared lines. This allows for up to 4 (CANDO4) slave devices to be concurrently active.

Key features of the 4WiCS interface are:

- Power can be transmitted together with data – downlink path;
- Multiple devices can be addressable using a shared bus – parallel connection;
- Bi-directional, full-duplex data communication;
- Zero net DC voltage – the four wires are arranged in two pairs using fully-differential AC signaling.

The typical configuration for the 4WiCS shared bus, connecting a single master device onto four (CANDO4) slave devices is shown in Figure 6.9.

The 4WiCS interfacing is established by connecting multiple CANDO4 chips via a wireline channel to the master controller. This channel will consist of an implantable lead (e.g. Cooper cable), connectors, baseplate interconnects, ribbon cables, rivet bond, etc. A simplified circuit model of the wireline channel is shown in Figure 6.10. This is based on the characterizations derived in Chapter 4 (Section 4.3) and on the considerations discussed in Chapter 5 (Section 5.3).

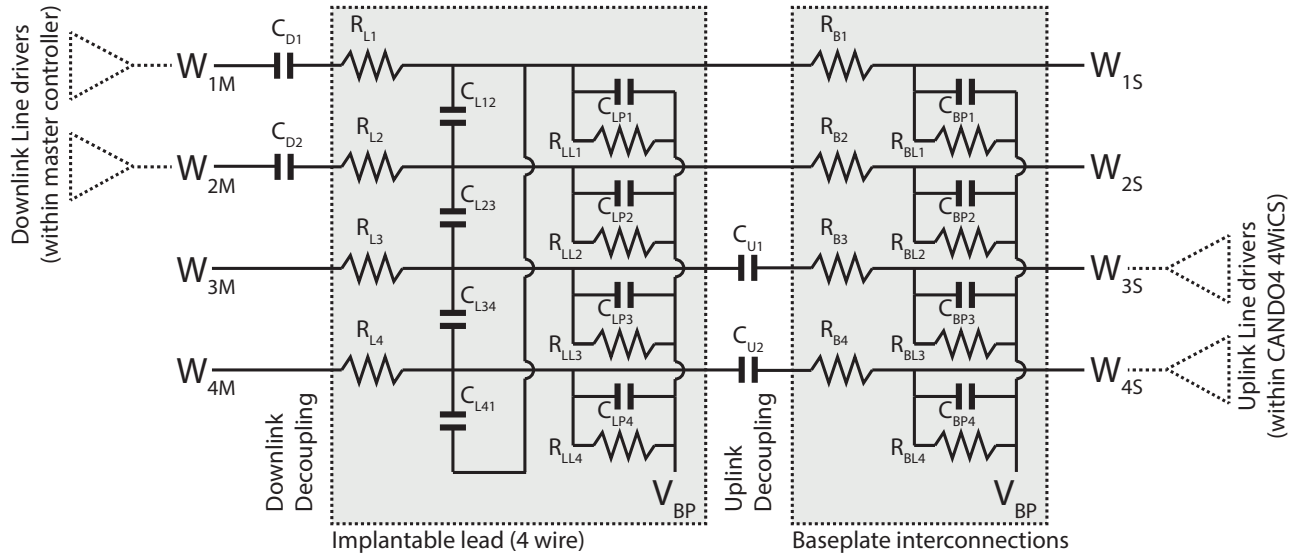


Figure 6.10: Simplified electrical model for the 4WiCS wireline channel. Illustrated are the implantable lead (series resistances R_{L1} , R_{L2} , R_{L3} , R_{L4} , coupling capacitances C_{L12} , C_{L23} , C_{L34} , C_{L41} , parasitic insulation capacitances C_{LP1} , C_{LP2} , C_{LP3} , C_{LP4} , insulation leakage resistances R_{LL1} , R_{LL2} , R_{LL3} , R_{LL4}) and baseplate interconnections (series resistances R_{B1} , R_{B2} , R_{B3} , R_{B4} , parasitic insulation capacitances C_{BP1} , C_{BP2} , C_{BP3} , C_{BP4} , insulation leakage resistances R_{BL1} , R_{BL2} , R_{BL3} , R_{BL4}) models.

Physical organization

The physical arrangement that has been defined is additionally a key feature offering high versatility and minimization of production cost. Specifically, the CAND04 chip is constrained to a rectangular 5 mm x 2.5 mm die, with physical bond pads positioned around the perimeter, allowing for fabrication through standard production service provided by semiconductor foundries. The chip can therefore be implemented as a standalone die and bonded to a traditional chip package for electrical and functional testing.

As shown in Figure 6.11, such die has the capability to be also connected with wirebonds to a substrate representing the passive multi-optrode fork, including recording sites and LEDs. Moreover, this arrangement gives the possibility for the chip to be rapidly integrated into an all-CMOS fork design, by maintaining the active circuits within a 5 mm x 2.5 mm head, and wiring internally to passive shanks (i.e. all designed and manufactured within a CMOS process). With this in mind, the CAND04 SoC is envisaged to prioritise flexibility and to minimise – or eliminate – circuit design difference between active chip of passive probe (Figure 6.11a), or active probe with integrated chip (Figure 6.11b).

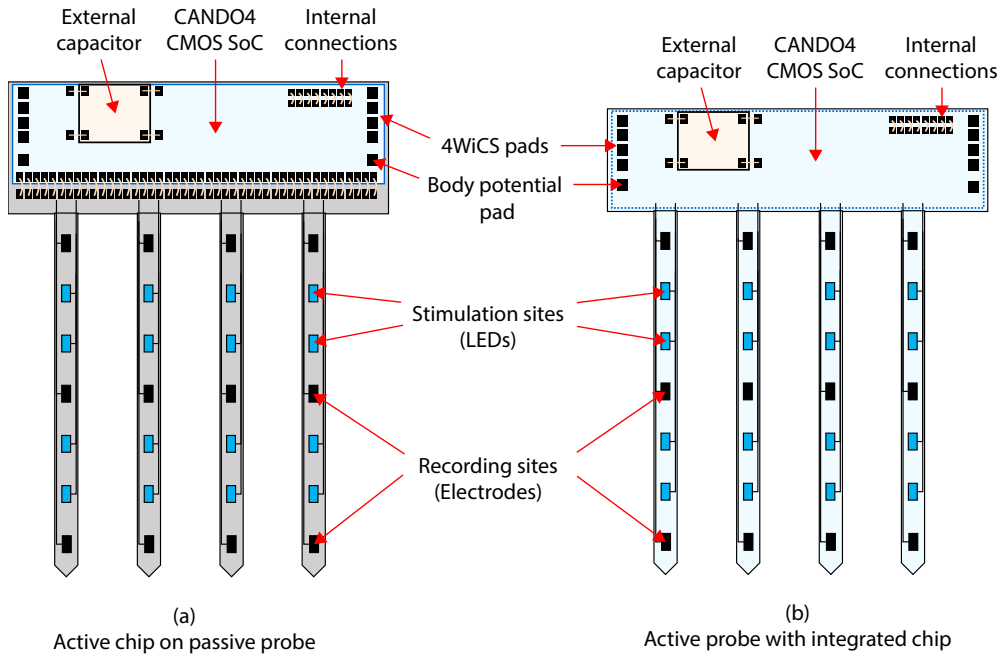


Figure 6.11: Multi-optrode proposed construction. Two possible options: (a) CANDO4 CMOS SoC bonded on the head of a bespoke *passive multi-optrode* fork; (b) CANDO4 CMOS SoC monolithically integrated within *active CMOS multi-optrode* fork.

The CANDO4 SoC floorplan is partitioned according to the following constraints:

- All the connections to the multi-optrode fork are located along the bottom edge;
- A 5-wire ribbon cable connects the chip to the baseplate (4 connections for the 4WiCS, 1 connection for the body potential) and is replicated on both left and right edges for reliability and redundancy.
- The power and SPI connection bondpads for SPI-based external control are positions along the top edge - they are shorted if 4WiCS and CORE are to be connected;
- An off-chip thin capacitor, required specifically for filtering out the oscillation and noise at the output of the rectifier, is connected with wirebonds to the chip – located around the die central point;
- The analogue and digital domains are separated and powered up by different supplies;
- The recording circuits are isolated from noisy circuits (including stimulation, 4WiCS, and digital control circuits);
- The I/O circuits (recording amplifier, stimulation drivers, diagnostic instrumentation, and body potential driver) are strategically positioned as close as possible to the physical bondpads for parasitics limitation.

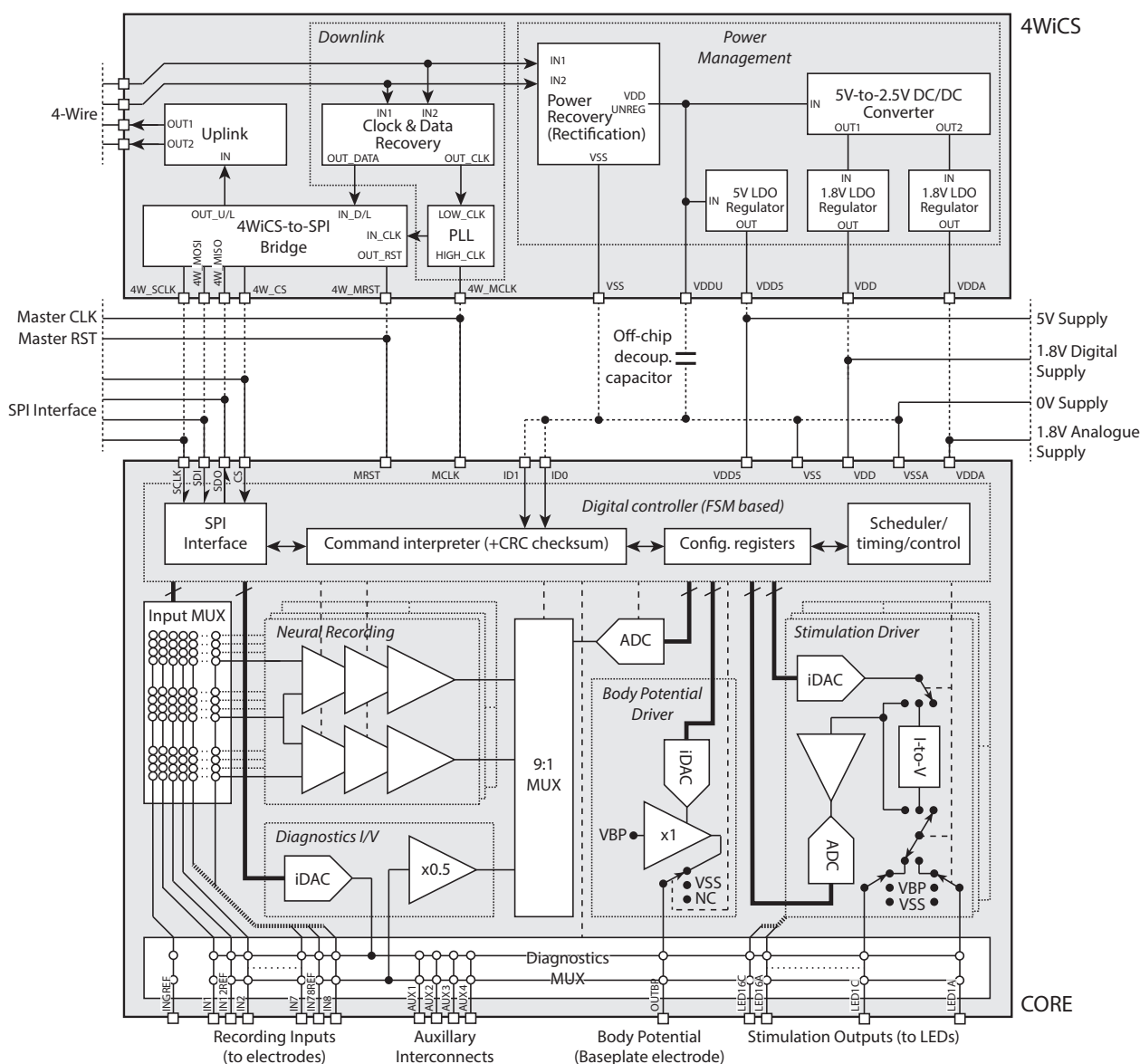


Figure 6.12: CAND04 System-on-Chip architecture.

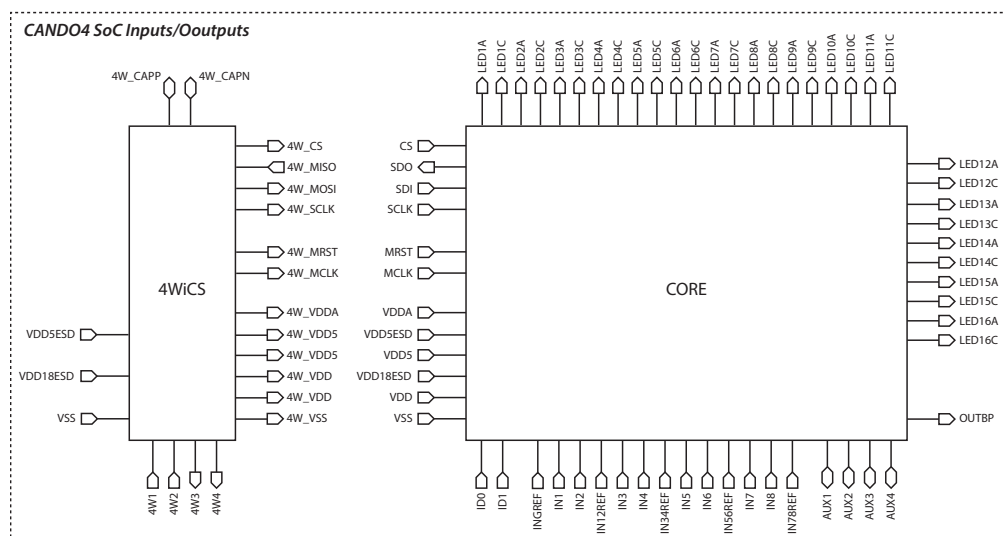


Figure 6.13: CANDO4 SoC symbol showing the I/Os of the whole system.

Circuit implementation

The CAND04 SoC architecture is illustrated in Figure 6.12, and it represents all the active circuitry listed in the previous section. The two sub-systems – CORE and 4WiCS – have been designed separately and combined to form the CAND04 SoC at design finalization. Moreover, Figure 6.13 outlines the I/Os of the system, thus also the physical pins/pads that the IC uses to interact externally, both through the communication interfaces – SPI and 4WiCS – and through the core functions – recording inputs from electrodes, stimulation outputs to LEDs, body potential output to baseplate electrode, and diagnostics interconnects from/to core circuit I/Os.

In the following, each of the circuits that constitute the 2 sub-systems will be introduced and discussed. More focus will be given to the 4WiCS sub-circuits and the adjustments/improvements from the previous generation.

6.2 CAND04 CORE Sub-System - Circuit Design

*The leading architect and chip designer of the CAND04 CORE sub-system is **Dr Yan Liu** and the circuits have been implemented with the support of Mr Dorian Hacı (Ph.D. thesis author) and Dr Timothy Constandinou. The core circuits and their functions are summarised in the following.*

6.2.1 Core Instrumentation Circuits

LED Stimulation Drivers

Each CAND04 integrated circuit includes 16 stimulation drivers to directly modulate a number of LEDs (16 in total, arranged in 4 LEDs per shank x 4 shanks per fork). The stimulation drivers need to provide a programmable (magnitude and duration) current pulse stimulus with the capability of also providing a voltage bias to compensate the net (i.e. average DC) electric field. Experimental data have demonstrated that providing balanced, symmetric stimulation

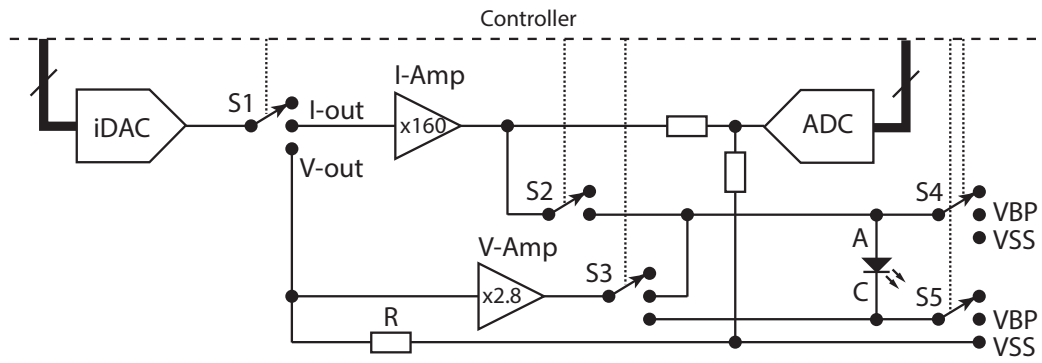


Figure 6.14: Schematic of stimulation driver circuit for providing the three stimulation profiles, showing LED (stimulation) outputs as: A=Anode, C=Cathode.

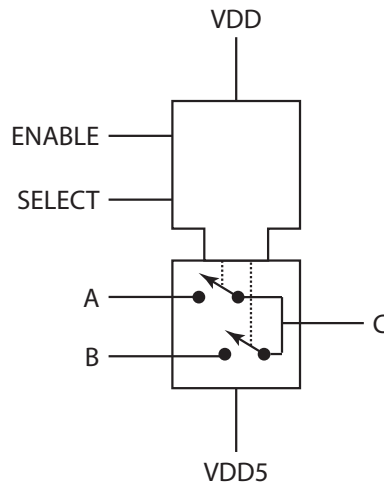


Figure 6.15: Symbol of analogue MUX required for the stimulation circuit.

in terms of voltage bias (thus also electric field) can improve the long-term viability of the encapsulation. Each LED out of total 16 LEDs will have dedicated driving and compensation circuits for its anode and cathode. The top-level schematic of the stimulation driver is shown in Figure 6.14. This contains a current DAC (iDAC), ADC, current amplifier, voltage amplifier, and 5 analogue multiplexers. The iDAC and ADC operate in the 1.8 V domain, whereas the analogue multiplexers, current and voltage amplifiers operate in the 5 V domain.

For the iDAC, a current DAC topology has been selected because: (1) it can be used to generate both the current stimulus, and voltage bias required for the compensation phase; (2) implementation simplicity; and (3) ability to power gate (minimal power consumption when inactive). The iDAC has been designed to have a reduced current range (compared to the required stimulation range), in order to reduce power consumption during the compensation phase (voltage output). A current amplifier is thus needed for two purposes: (1) to amplify/scale

the stimulation current (from iDAC output); and (2) to boost the output impedance of the current source output. The current amplifier is implemented using a cascade of current mirror stages with feedback amplifiers to ensure precision by regulating the output current at the output of each stage. The voltage buffer converts the iDAC current output (1.8 V domain) to a programmable voltage bias (5 V domain) for the balanced compensation phase. This uses a resistive load to convert the iDAC output to a voltage reference. The voltage amplifier then scales this from 1.8 V to 5 V domain and buffers the output (provides a low impedance voltage source). An independent ADC is required for the stimulation subsystem to sample the voltage during the stimulation phase. This will in turn be used to provide a voltage bias to balance the electric field during the compensation phase. For the implementation of switches S1-S5 in the stimulation circuit (Figure 6.14), an analogue multiplexer is required (Figure 6.15).

Neural Recording Instrumentation

The CORE sub-system includes 8 recording circuits (2 differential amplifiers per shank) to directly observe the neural signals via a number of recording electrodes (12 in total, arranged in 3 electrodes per shank x 4 shanks/fork). The recording instrumentation amplifies the observed biopotential signal, conditions this (i.e. filter), and converts to a digital representation for communication and subsequent closed-loop processing. The recording circuits consist of an input multiplexer (MUX), a cascade of 5 amplification stages, and a shared ADC that selects the channel to be sampled through an output MUX. The neural recording instrumentation sub-system is shown in Figure 6.16. The signal range at each stage along the acquisition path is annotated accordingly.

Since there are three electrodes in each shank (IN1 IN2 INREF12), and two recording front-end in each shank, each front-end differential amplifier is configured to have one of its inputs (e.g. INP) directly connected to a corresponding electrode input (e.g. IN1). The other input (e.g. INN) connects to an input multiplexer to select the reference scheme: (1) local reference (MUX = 2'b00); (2) global reference (MUX = 2'b01); (3) single-ended configuration (MUX = 2'b10); (4) auxiliary input reference for test purposes (MUX = 2'b11). Therefore, the input of

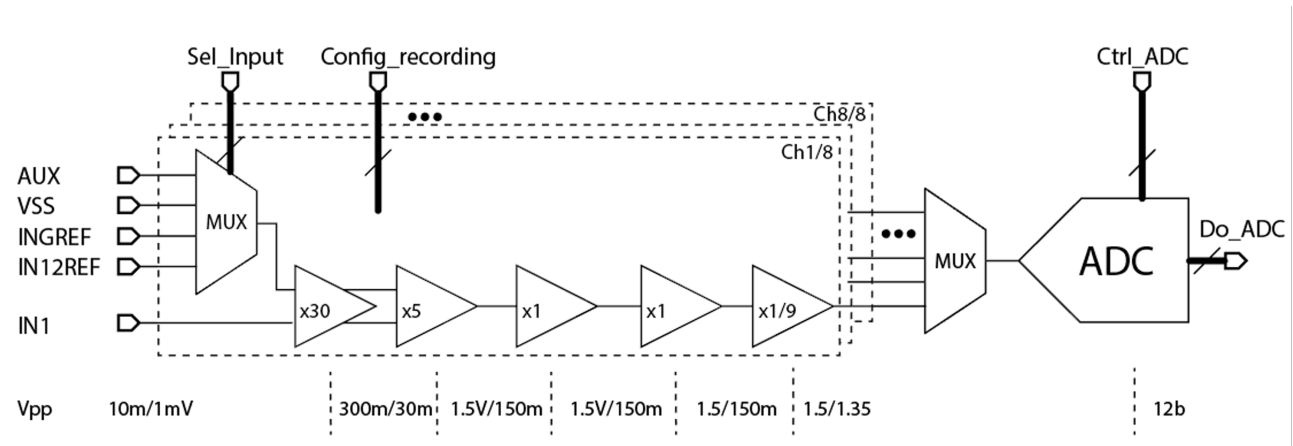


Figure 6.16: Recording sub-system architecture including the 8 differential recording channels, input and output MUXs, and the ADC. Configuration and ADC timing are provided directly from the controller.

INN is connected to a 4:1 multiplexed, whose inputs are local reference (current shank), global reference, VSS, and auxiliary test input. The front-end amplifier, i.e. 1st amplifier stage, is a fixed gain, low noise, fully differential (differential input and output), AC-coupled neural amplifier. This is based on the “Harrison” topology using a large pseudo-resistor to define its high pass corner to reject the DC offset of the electrodes. The 2nd amplifier stage is an AC coupled differential amplifier with a single-ended output. This has a fixed gain and tuneable bandwidth. The 3rd and 4th amplifier stages use the same AC coupled differential amplifier with a single-ended output. This has a fixed gain and tuneable bandwidth. The 5th and final amplifier stage is a tuneable gain, AC coupled differential amplifier with a single-ended output.

The output of each recording channel is routed to a multiplexer before being fed into the ADC. As the ADC is shared between the 8 recording channels, and also the diagnostic circuit, a 9:1 multiplexer is required. Apart from the different number of inputs, this can utilise the same technical specifications as the input multiplexer described previously. The analogue-to-digital converter (ADC) samples the input analogue signal from either the recording channels or diagnostic circuit and converts it to an equivalent digital representation. The ADC is controlled by the top-level digital controller, and its output is latched synchronise to the digital buffer. The topology selected is based on a charge-redistribution successive approximation (SAR) converter with 12-bit resolution and maximum sampling rate of 100 kHz. This topology has been selected due to a good power/area trade-off for low-to-mid-resolution converters. Also, previous

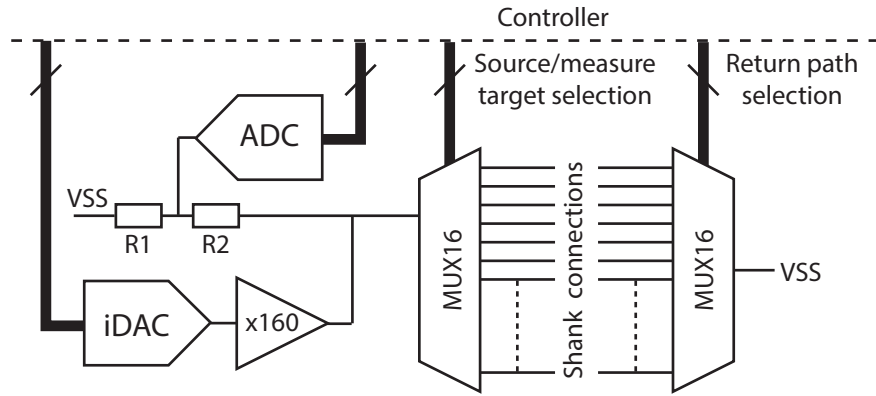


Figure 6.17: Diagnostics sub-system architecture, including circuits for current source generation, voltage measurement, and current path routing. Configuration and diagnostics timing are provided directly from the controller.

iterations of the design have used this topology successfully.

Diagnostics Instrumentation

The diagnostics instrumentation provides source-measure capability (current source, voltage measure) between any 2 of the 49 connections to the multi-shank fork. This uses a current DAC and current amplifier to source the current and scales the observed potential onto the ADC range for digitisation of the voltage quantity. The diagnostics circuits can be used to test, for example, I-V characteristics of the LEDs, to assess the mechanical integrity of the silicon shanks (via auxiliary connections), or to test leakage currents through encapsulation.

The diagnostics sub-system uses two multiplexers to route the current path between any two connections (pins) from CANDO4 (excluding the digital I/Os between 4WiCS and CORE, and the 4-wire I/Os – that are externally powered). In total there are 50 individual connections to the 4 shanks (12 connections per shank – 8 to LEDs, 3 recording, 1 auxiliary), 1 global reference, and 1 body potential electrode connection. The diagnostics instrumentation architecture is shown in Figure 6.17. Although the diagnostics can only probe one port at a time, this block is repeated per shank (i.e. 4 per chip) to allow for efficient floorplan management. The controller configures the 8 multiplexers (i.e. 2 per shank) to select the two ports, one to connect the current source onto, and another to provide a return path, i.e. provide a current sink to VSS. The current source is implemented using a programmable iDAC and current amplifier

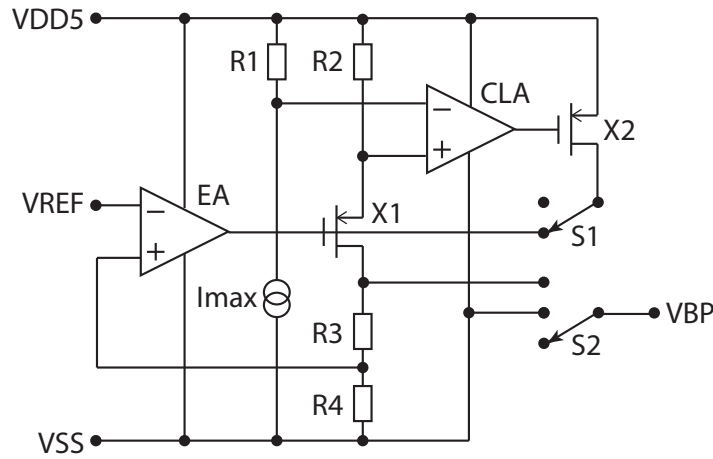


Figure 6.18: Simplified schematic of the body potential driver circuit (EA=Error Amplifier, CLA=Current Limit Amplifier).

– using identical designs to those detailed previously in the stimulation circuits. The voltage at the node the current output connects to the MUX is then measured. First, this voltage is attenuated (from 5 V to 1.8 V domain) and then fed into the recording ADC via the recording input multiplexer.

Body-Potential Driver

The body potential driver circuit biases the body potential electrode. This electrode is patterned as a ring on the underside of the baseplate and is in direct contact with the surface of the brain. This circuit, therefore, has the ability to pass DC current to the body. This ensures a constant bias is maintained between the body and system power supply, as discussed in the previous Chapter 5 (Section 5.3).

It is essential however to guarantee that the maximum DC current that the body potential driver can provide is small. The maximum allowable limit is defined by the relevant regulatory standard, depending on the surface area of the electrode:

BS EN 45502-1:2015, 16.2 (Implants for surgery - Active implantable medical devices):

“Except for its intended function, implantable parts of an Active Implantable Medical Device shall be electrically neutral when in contact with the body. [...] The direct current density at the surface of any conductive surface or electrode shall be $\leq 0,75\mu\text{ A/mm}^2$.”

A simplified schematic for the body potential driver circuit is shown below in Figure 6.18. The Error Amplifier (EA), pass transistor (X1), and resistors R3, R4 form a standard voltage regulator circuit, with target output voltage given by $V_{REF} \cdot (R3+R4)/R4$. The Current Limit Amplifier (CLA), compares the maximum allowable current (I_{maxBP}) that flows through R1, with that flowing through sense resistor R2, and if overcurrent, triggers the bypass transistor (X2) that pulls up the gate of pass transistor (X1) to reduce the output current. Quiescent current can be reduced by scaling resistors R1 and R2 such that $I_{maxBP} = R1/R2 \cdot I_{max}$ (where $I_{max} < I_{maxBP}$ and $R1 > R2$). Switches S1 and S2 are set by the controller depending on the required body potential driver configuration. Opening switch S1 (normally closed for “standard” mode) disables the current limit (for “investigational” mode). Switch S2 can be configured to disable the body potential output (i.e. leave open circuit) or select VSS (for “investigational” mode).

The circuit implementation of the topology shown in Figure 6.18 can be further optimised to reduce power by reorganising the current comparison section. Specifically, the bias voltage (output of EA), can be copied to a drive a reference branch for current comparison, thus replacing the current branch through R1 and I_{max} .

6.2.2 Core Digital Controller

The controller within the CANDO4 core is a digital circuit that handles all SPI communication (either via 4WiCS or direct external controllers, e.g. MCU), interprets and executes commands, provides configuration, and controls/monitor all subsystems. It is designed in a hardware description language (HDL), Verilog, and follows a standard-cell based design methodology: the Verilog code is first verified (simulated), then synthesised (translated) to Register Transfer Level (RTL) (i.e. a digital cell-based circuit description). The RTL is, in turn, converted into a layout via Place Route using the standard cell library provided by the technology vendor. After RTL synthesis and final place and route are complete, timing information is fed back into the original simulation for further validation of the physical implementation.

The overall structure of the digital controller is shown in Figure 6.19. It consists of an SPI

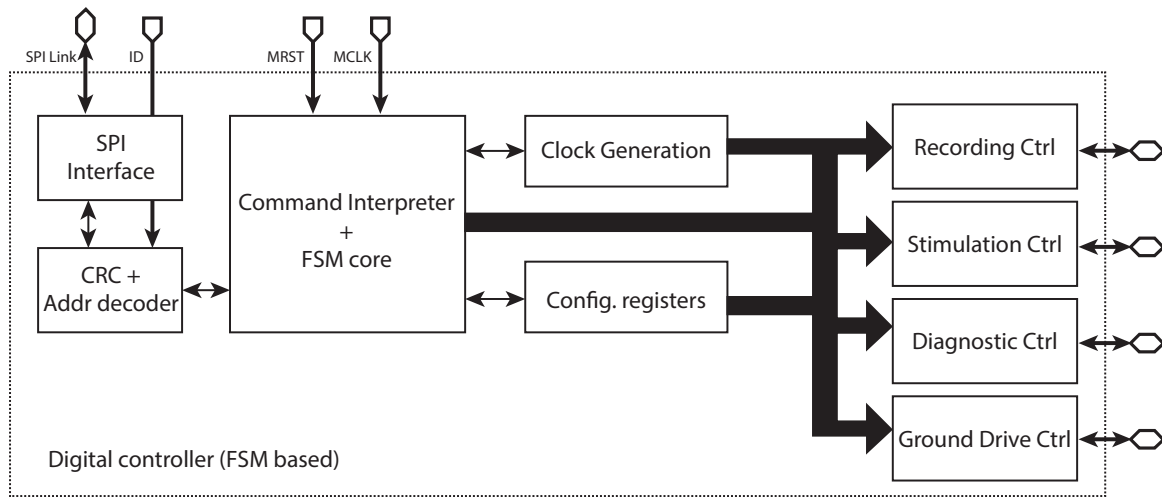


Figure 6.19: System organisation of the digital controller.

controller, CRC and address decoder, core Finite State Machine (FSM) for command interpretation, internal register map, clock generation, and control drive for all the sub-blocks. The controller includes a bank of Random-Access Memory (RAM) including a number of registers, organised in 8-bit blocks (1 register = 1 byte = 8 bits). Each memory location is used to configure and control the behaviour of the sub-systems. These registers can be individually read or written to via the different commands.

SPI Communication Interface: the SPI (low level) protocol has been discussed previously in this chapter. The communication between the FSM and SPI controller requires a handshake to accommodate for having different clock domains between the core and SPI controller, i.e. the core has an independent clock (higher frequency) than the SPI bus. Each SPI data packet has a fixed word size of 32-bits that is sent via either the host (external controller), i.e. down-link or slave (CANDORA devices), i.e. uplink. Both the handshake and data communication are contained within this word format. Each word includes 24-bits data and an 8-bit Cyclic Redundancy Check (CRC) code (32-24). This format is illustrated in Figure 6.20.

Command Interpreter: the command interpreter (within the digital controller) will receive the SPI data packet and read the relevant bits (i.e. bits 11-16) to interpret the different commands. The controller will then respond by changing its operational state to execute the required command, for example, configuring the stimulation scheduler, or interrogating the data converter to read in recording data, and then relaying this to the SPI bus.

Instruction Set: a custom instruction set has been defined for CANDO4. The commands can be divided into five groups: (1) stimulation, (2) recording, (3) BP driver, (4) diagnostics, and (5) other. Within the stimulation (Instruction Set), recording (Instruction Set), and body potential driver (Instruction Set) groups, there are two sub-groups: (a) configuration instructions (*CFG*) to set static parameters; and (b) operation instructions (*OP*) to initiate the required commands.

Recording Controller: the recording controller is responsible for all operations relating to the recording function. Its specific objectives are: (1) to set the configuration bits for individual recording channels, according to memory and the instruction received; (2) to control the ADC behaviour continuously to fetch the recording data or diagnostic data and store the data into the internal buffer; (3) to power down disabled channels (as configured), and skip sampling their outputs (i.e. data conversion).

Stimulation Controller: the stimulation controller (or scheduler) is responsible for all operations relating to the stimulation function. This controls the stimulation circuits according to the received instructions and configuration stored in memory.

Diagnostics Controller: the diagnostics controller (or scheduler) is responsible for all operations relating to the diagnostics function. This initiates the diagnostics operation upon request. During this operation, both recording and stimulation will be disabled automatically. This sets the required MUX and DAC configuration for diagnostics, as described previously in Figure 6.17, and reads out the ADC value providing the diagnostics results.

Body Potential Controller: the body potential controller is responsible for all operations relating to the body-potential driving function. This sets the relevant configuration bits for the circuits, defines the voltage level and current compliance.

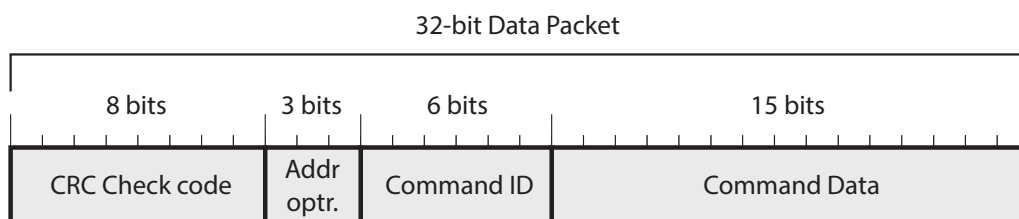


Figure 6.20: Communication data packet (word) format.

6.3 CANDO4 4WiCS Sub-System - Circuit Design

The leading architect and chip designer of the CANDO4 4WiCS sub-system is **Mr Dorian Hacı** (Ph.D. thesis author) and the circuits have been implemented with the support of Dr Yan Liu, Dr Sara Ghoreishizadeh, and Dr Timothy Constandinou. In addition, the active rectifier and linear regulator architectures within the power management unit derive from previous results achieved by two graduate students, respectively Mr Junhao Zhang and Mr Nicolas Scremin.

The 4WiCS interface that is implemented in CANDO4 is based on the high-level architecture of the first generation (4WiCS ASIC) originally developed in parallel with the CANDO3 ASIC and described in Chapter 4. This sub-system of the CANDO4 SoC allows for an external central module (at chest implant) and the CANDO4 satellite modules (at brain implant) to communicate with each other through the 4WiCS proprietary protocol and for a CI-to-BI power carrier to power up multiple satellite modules, thus multiple CANDO4 systems.

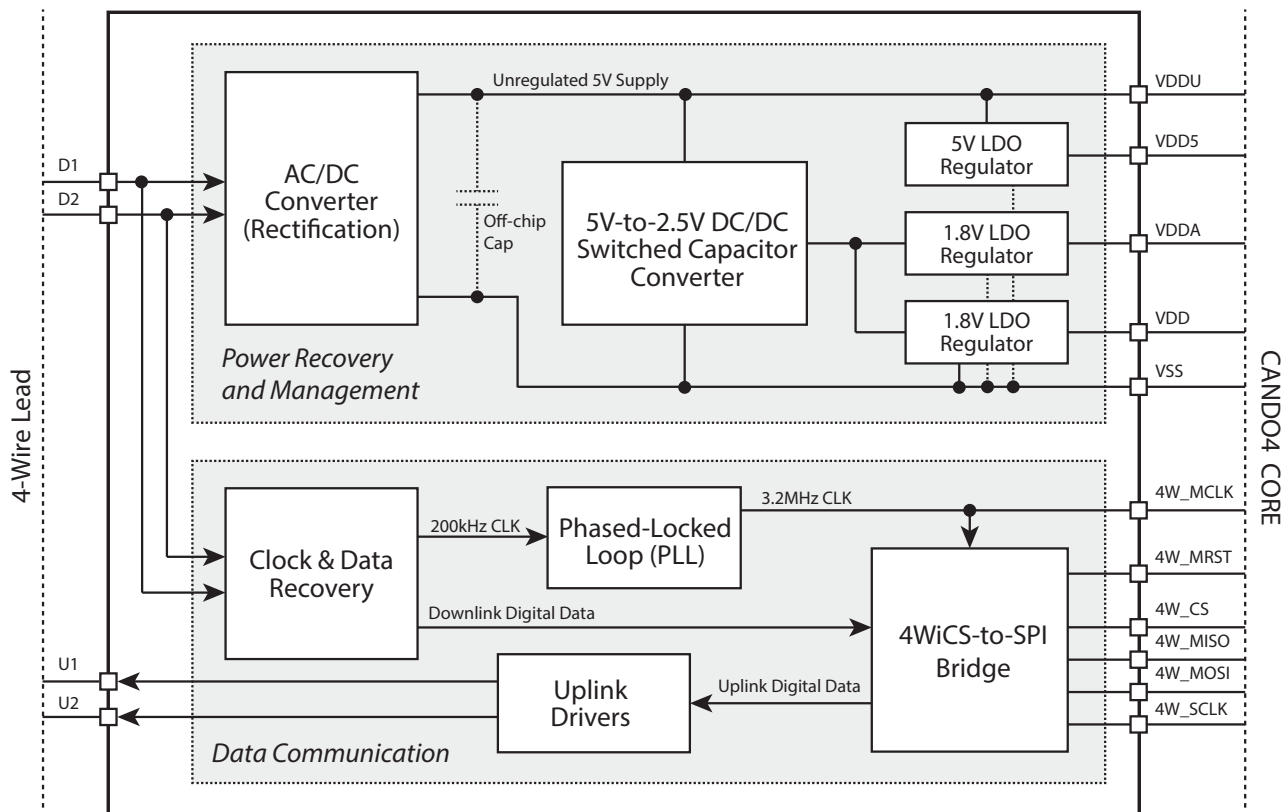


Figure 6.21: Top-level architecture of the CANDO4 4WiCS sub-system.

The CANDO4 4WiCS sub-system physically connects on one end to the 4-wire lead through the downlink and uplink AC differential signals and on the other end to the CORE system through single-ended DC power and digital data signals. Refer to Section 6.1.2 for 4WiCS functional description and key feature. The system architecture of the 4WiCS interface is divided into two sub-blocks, depending on its two main functions: (1) *Power Management Unit (PMU)*; and (2) *Data Communication Unit (DCU)*. An overview of the architecture of the 4WiCS interface is presented in Figure 6.21.

The main blocks in the PMU subsystem are:

- *AC/DC Converter (Full-wave Active Rectifier)*
- *5 V-to-2.5 V DC/DC 2:1 Converter (Switched Capacitor Halver)*
- *One 5 V and four 1.8 V Linear Voltage Regulators (Low-Dropout Regulators)*

The main blocks in the DCU subsystem are:

- *Downlink Receivers*
 - *Clock and Data Recovery Circuit*
 - *Phase-Locked Loop Circuit*
- *Uplink Drivers (Tri-State Buffers)*
- *4 WiCS-to-SPI Bridge (4 WiCS digital controller)*

6.3.1 Power Management Unit

The PMU is responsible for recovering the DC power from the AC differential signal coming from two wires of the 4-wire lead (D1 and D2) and for generating the appropriate DC voltage levels used for powering up the 4WiCS internal circuitry and the CANDO4 CORE circuitry. As the latter requires both 5 V and 1.8 V stable voltage domains, the PMU ensures these are generated and regulated. The waveforms on the downlink wires D1 and D2 are squarewaves transmitting both the downlink signal and the power carrier. The square-wave on the D1 wire, with respect to a reference point (electric potential 0V), is the inverted version of the square-wave on D2 with respect to the same reference point, as shown in Figure 6.23.

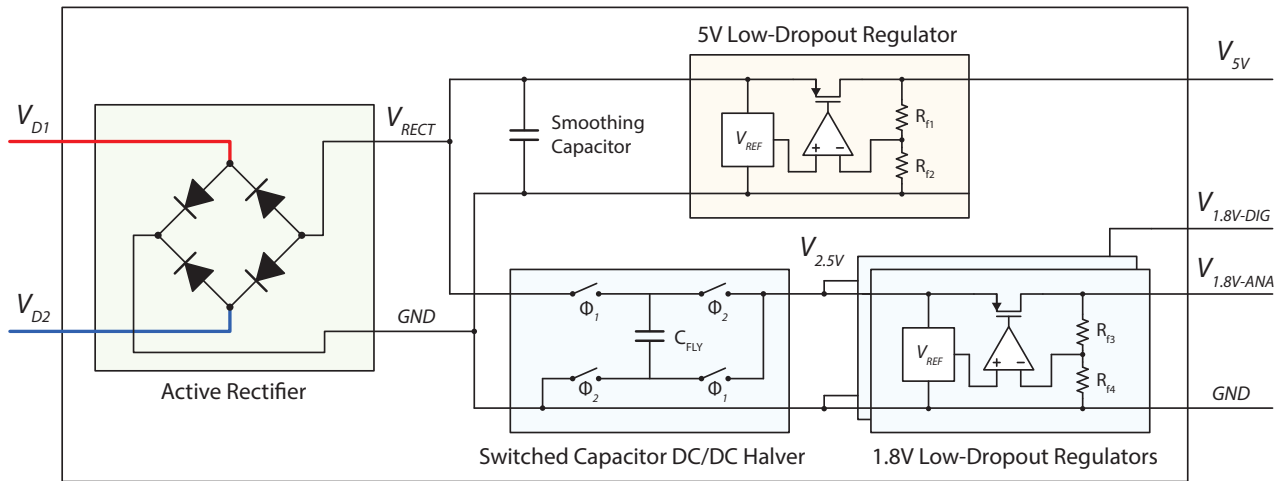


Figure 6.22: Top-level architecture of the Power Management Unit within the CAND04 4WiCS interface.

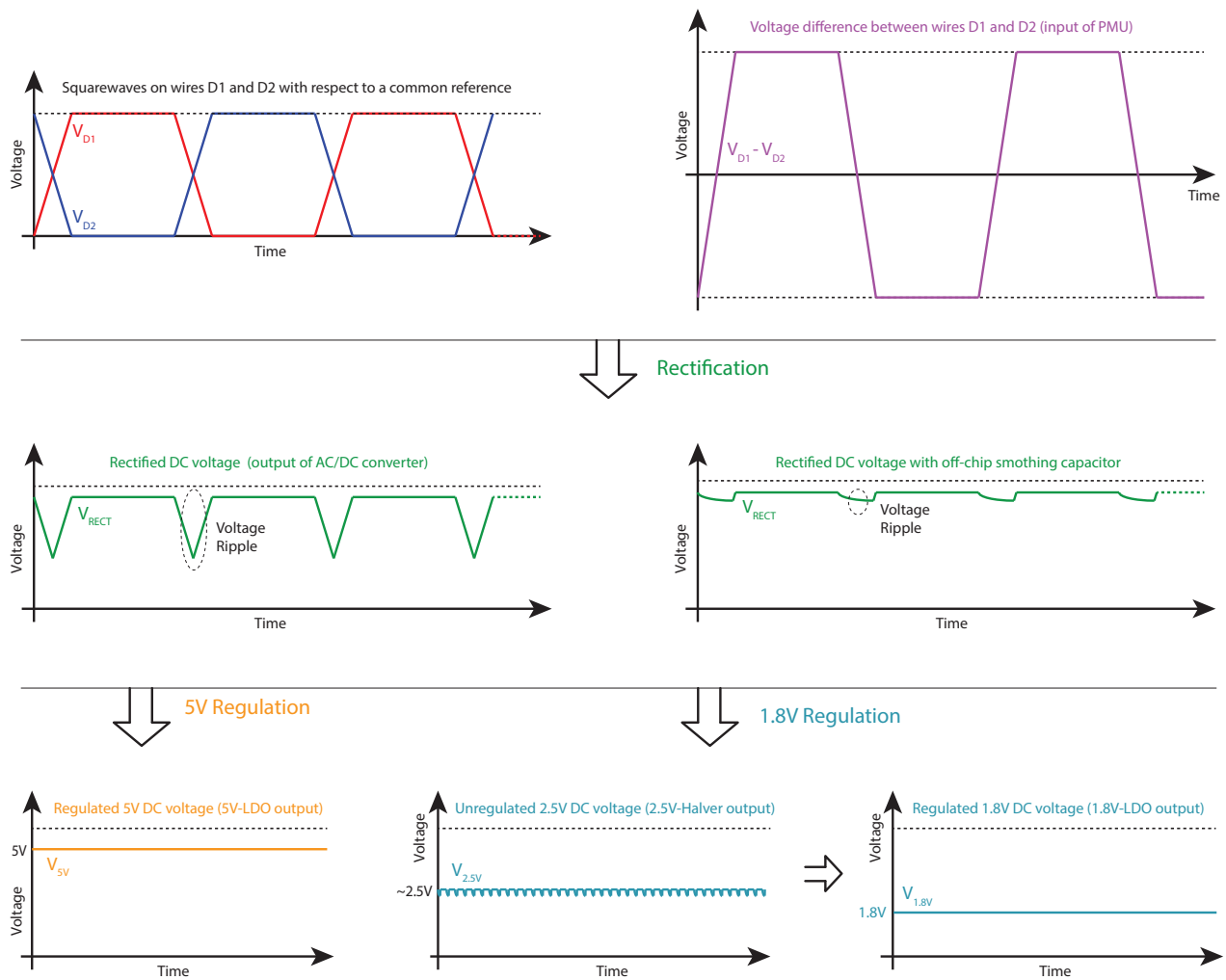


Figure 6.23: Illustration of the power signals at the different PMU stages: rectification, 5 V regulation, DC/DC conversion, and 1.8 V regulation.

The differential signal on the downlink wires (voltage difference between V_{D1} and V_{D2}) is received at the PMU. A first power domain conversion is performed by the AC/DC converter that rectifies the AC signal with a full-wave active rectifier, generating a DC voltage. To reduce the voltage ripple at the output of the rectifier, an off-chip smoothing capacitor is used. This unregulated power signal is furthermore processed by two circuits in parallel to create the regulated 5 V and 1.8 V signal domains. The former is obtained with direct regulation of the smoothed rectifier output through a low-dropout voltage regulator. To achieve the 1.8 V signal instead, the output of the rectifier is first down-converted by a DC/DC halver based on switched capacitors (SC). The SC DC/DC converter down-scales the voltage level (in this case dividing it by two), however, differently from linear voltage regulators, it up-scales the current allowing for a higher PCE compared to an LDO. A regulation stage is further needed to obtain the regulated 1.8 V domain from the ~ 2.5 V output of the SC DC/DC converter. This is achieved with an LDO using the same topology of the 5 V LDO. The power signal path with the conversion stages is shown in Figure 6.23 and Figure 6.22.

AC/DC Conversion - Full-Wave Active Rectifier

Differently from the 4WiCS ASIC gen1, which includes a passive rectifier, a full-wave *active rectifier* is used in the CANDORA 4WiCS to convert the AC differential signal to the DC single-ended power signal. An active topology based on comparators is chosen to reduce the dropout voltage and thus achieve a higher power conversion efficiency, at the cost of a larger area (Figure 6.24a). This is based on the design first presented in [182].

The two comparators shown in Figure 6.24a, work as drivers for the pass transistors MN1 and MN2, which operate in triode region as synchronous switches with low on-resistance. The combination of comparator and NMOS creates an active diode, which functions as the two low-side diodes in the passive full-wave rectifier. The two high-side diodes are instead replaced by two cross-coupled PMOS transistors. In such configuration, the forward voltage drops of a typical passive rectifier are reduced from $2V_D$ to $2V_{DS}$, where V_{DS} is the turn-on voltage, which is equal to the drain-to-source voltage of the power switches [66]. The 4-input comparators (2

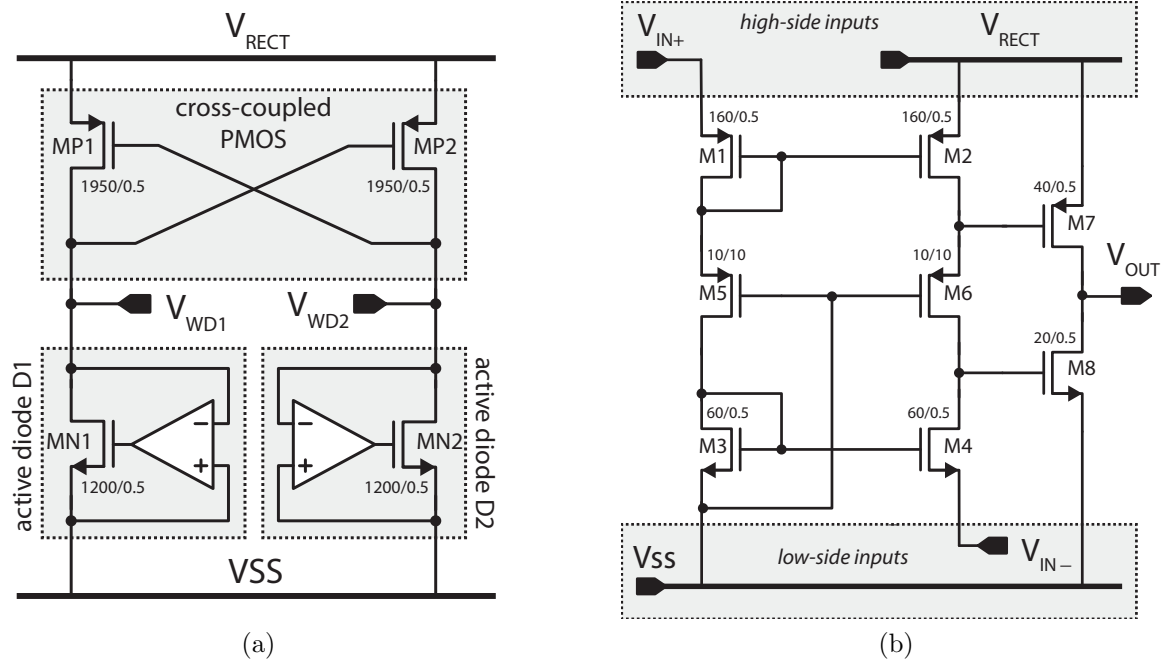


Figure 6.24: Active rectifier architecture: (a) top circuit of the comparator-based rectifier; (b) 4-input comparator circuit. All transistors are HV MOSFETs (12 V).

high-side input and 2 low-side inputs) used to drive the NMOS transistors are designed to be self-powered and biased by the unsteady and distorted squarewave voltages V_{WD1} and V_{WD2} to ensure that the rectifier can start up before V_{RECT} is charged up.

- *Simulated Results:*

The rectifier has been implemented with high voltage transistors and post-payout simulation results show reliable performance and high PCE in various load conditions – 2 mA to 10 mA, with 220 nF capacitor. As shown in Figure 6.25, with a load current of 2 mA, the maximum voltage drop is 125 mV, with a ripple of 68 mV. When a load of 10 mA, is considered, the voltage drop remains low – 240 mV – without impacting the stability – ripple 60 mV. In a typical operation of the rectifier (5 mA load current) The power conversion efficiency maintains an average value of 90%. This drops to 80% when the load current is as the smallest – 2 mA, PCE worst-case scenario. Despite its trade-off in the area occupied – more than double of the 4WiCS gen-1 AC/DC – for this specific application, the performance of the active rectifier is significantly higher than that of the passive rectifier.

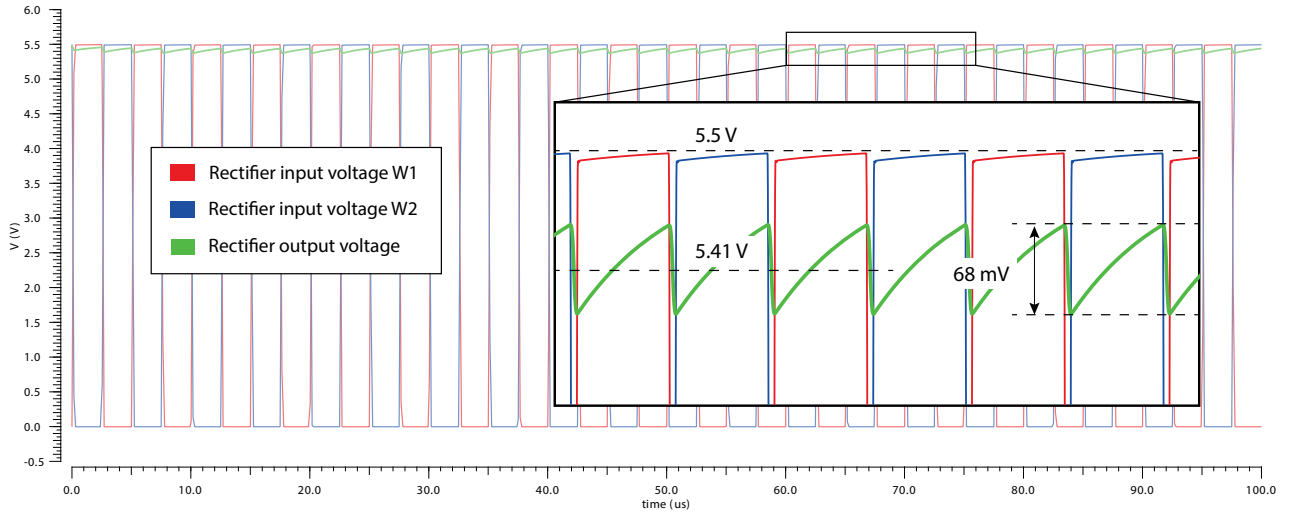


Figure 6.25: Active rectifier post-layout simulation. The input signals are simulated with realistic parameters – i.e. 5.5 V peak-to-peak squarewaves, 100 ns rise/fall time, and emulated model for 4-wire cable. The rectifier output presents typical sawtooth-wave characteristics with a 68 mV peak-to-peak value (output ripple) at 2 mA load current. The average voltage output is 5.41 V, thus dropping 90 mV in average.

DC/DC Conversion - 2:1 Step-Down Switch Capacitor Converter

A DC/DC 2:1 step-down converter is used to halve the voltage at the output of the rectifier, thus generating the unregulated voltage (~ 2.5 V) for the 1.8 V domain. The use of a switching DC/DC is essential in this case as the DC signal rectified by the active rectifier has a voltage >5 V, while the required voltage for the front-end recording and the digital controller is 1.8 V. If a linear regulator was employed instead of a switching DC/DC, the regulation would cost 64% of the total power to be lost in heat dissipation. Switching DC/DCs allow for the voltage to be significantly reduced without the power conversion efficiency degrading. Two different types of DC/DC converters can be used to step down the voltage depending on the choice of passive components utilised for energy storage: inductor-based (buck) and capacitor-based converters.

Given the large area and power cost of the common inductor-based buck when implemented with integrated inductors, a DC/DC converter based on switched capacitors is chosen instead with a total on-chip capacitance of 400 pF. This employs a conversion cell with a flying capacitor C_{fly} and four switches that allow the capacitor to (phase ΦX) charge up to half the input voltage and (phase ΦX) discharge on the output load [183]. If the switching frequency is fast enough for the capacitor to discharge of a small ΔV_{fly} value, the output voltage of the converter will

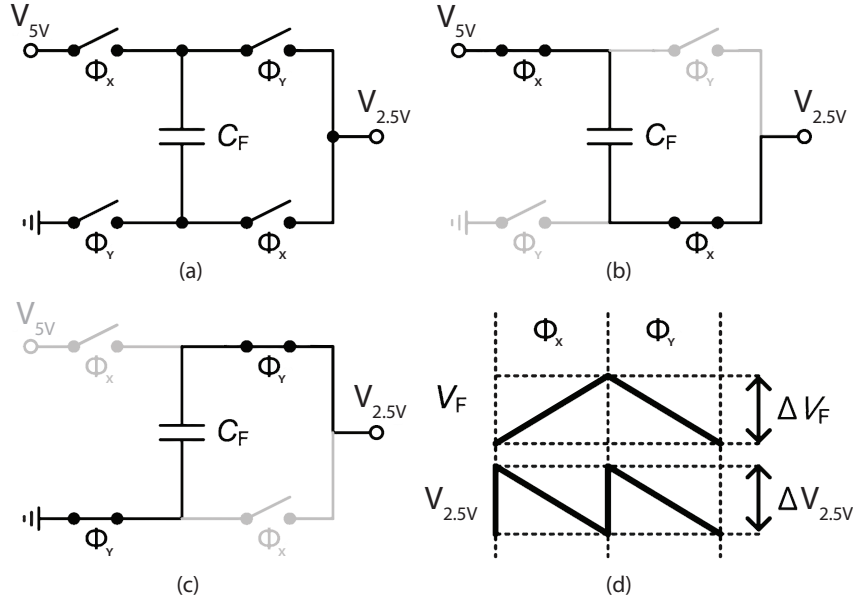


Figure 6.26: (a) Simplified architecture of a switched-capacitor cell; (b) serial connection of C_{fly} between V_{in} and V_{out} at Φ_X ; (c) parallel connection of C_{fly} between V_{out} and GND at Φ_Y and (d) C_{fly} charging/discharging process during Φ_X and Φ_Y with relative output ripple $\Delta V_{2.5V}$. Figure adapted from [184].

be half of the input voltage, with a ripple of $\Delta V_{2.5V}$, as shown in Figure 6.26.

The output voltage ripple depends primarily on the storage capacity of C_{fly} and on Φ_1 and Φ_2 switching frequency f_{SW} . In order to mitigate the ripple $\Delta V_{2.5V}$, while maintaining a fixed C_{fly} and f_{SW} , the multiphase interleaving technique is furthermore used, by partitioning the converter into multiple cells and driving each cell with different clock phases.

A k-phase interleaving permits to reduce by a factor k the voltage ripple by using k switched-cap

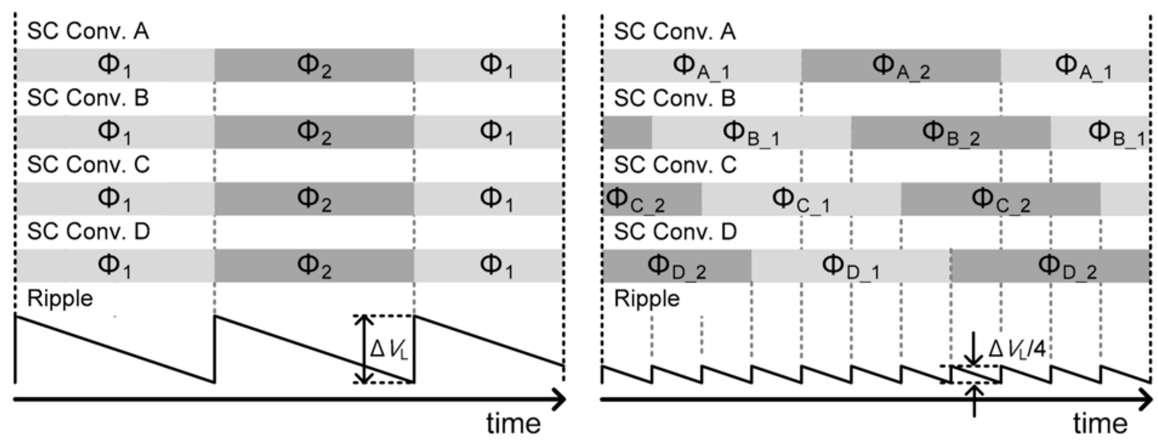


Figure 6.27: K-phase interleaving to reduce ripple voltage whilst maintaining the same total capacitance. Adapted from [184].

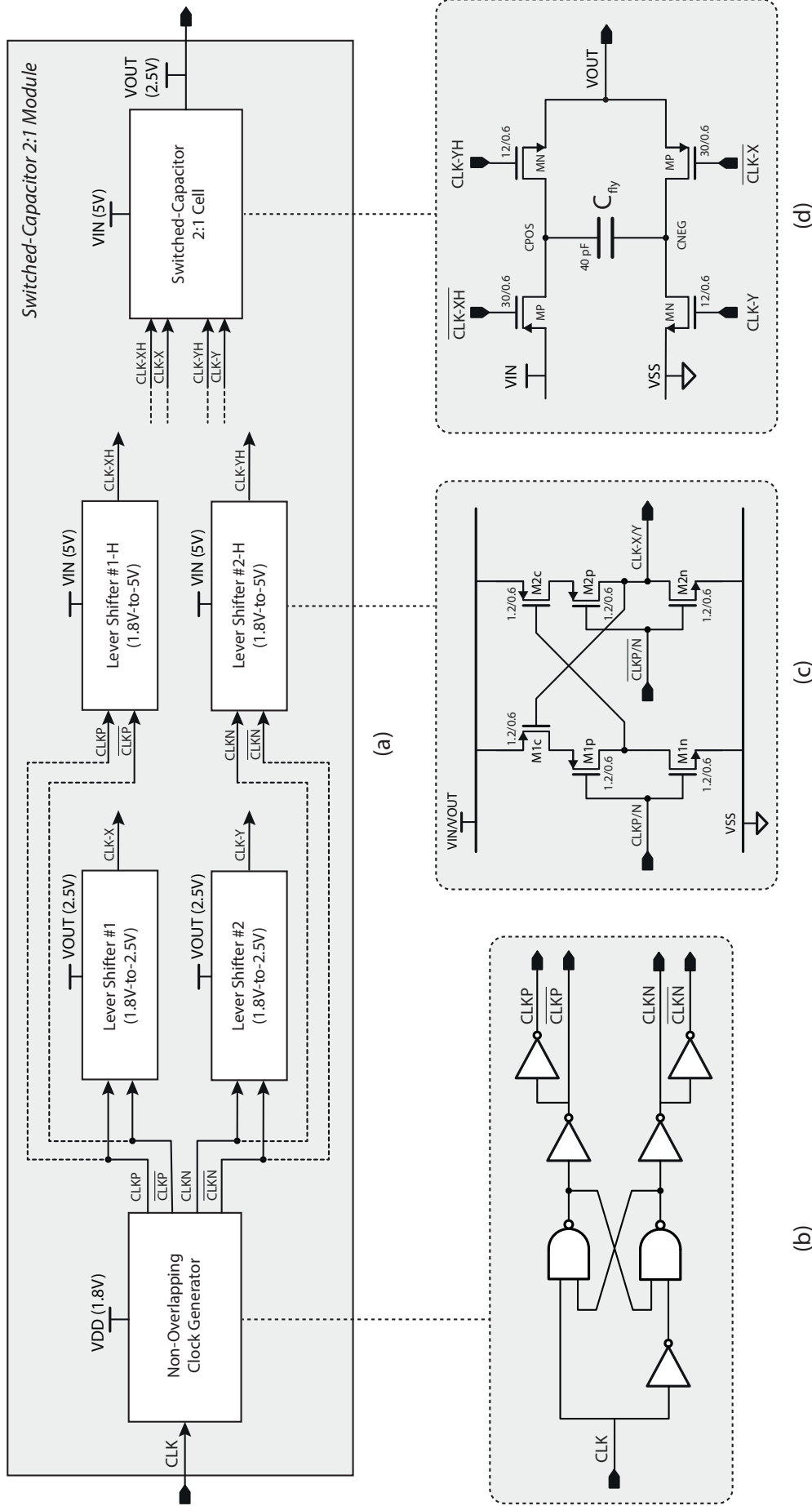


Figure 6.28: Switch-Capacitor DC/DC 2:1 module and cell architecture. (a) Top-level architecture of the switched-capacitor module, comprising: (b) non-overlapping clock generator – all transistors are minimum size; (c) 4 level shifters to increase the voltage level from 1.8 V to 5 V and 2.5 V to drive the switches – all transistors are HV MOSFETs (5 V); (d) switched-capacitor 2:1 cell architecture with 4 switches and the C_{fly} capacitor – all transistors are HV MOSFETs (5 V).

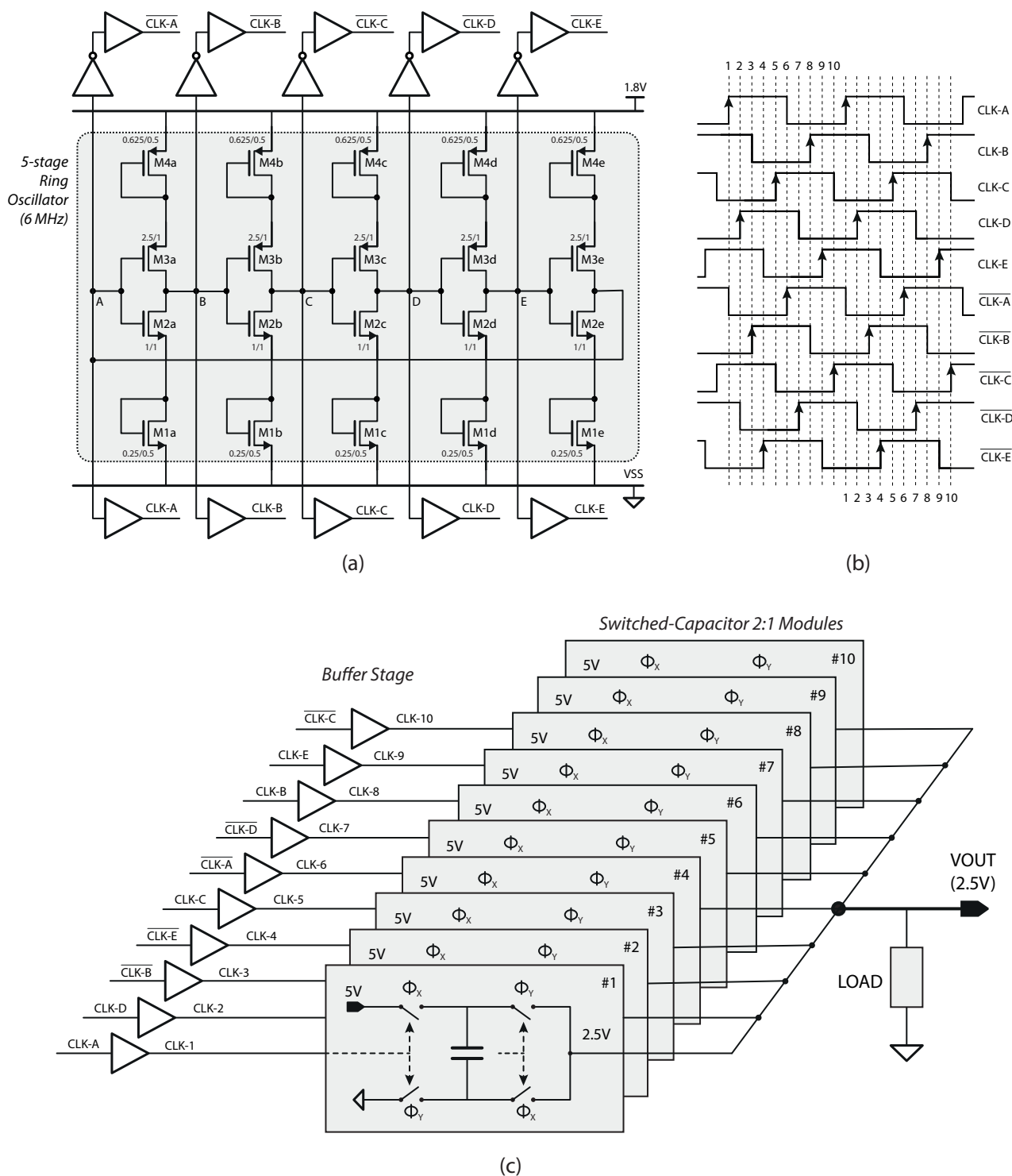


Figure 6.29: Switch-Capacitor DC/DC 2:1 converter architecture: (a) generation of the 10-stage interleaving clocks with a 5-stage ring oscillator; (b) 10 interleaving clocks with different switching time (rising edge); (c) 10 switched-capacitor 2:1 modules driven by the 10 interleaving clocks.

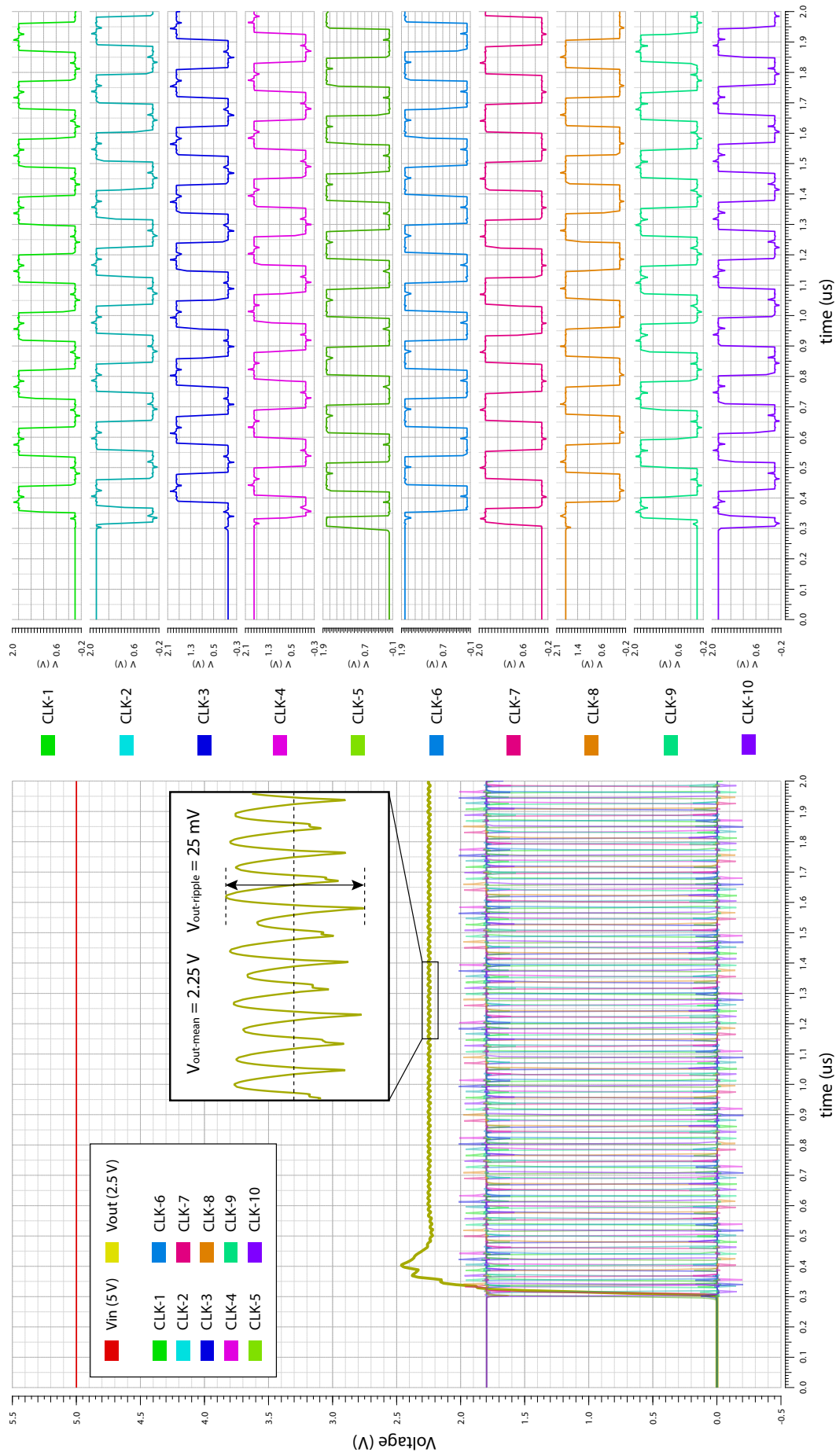


Figure 6.30: Post-layout simulation results of the DC/DC switched capacitor converter. Load conditions: $I_{load} = 2\text{ mA}$, $C_{load} = 100\text{ pF}$, $C_{fly} = 40\text{ pF}$ per cell (400 pF total). The input and output signals are plotted in the left-end graph, together with the 10 interleaving clock signals. These are also plotted separately in the right-end graph, showing the phase difference between each other.

cells, each with (1) a capacitor of value C_{fly}/k and (2) four switches controlled by equidistant phase-shifted versions of $\Phi1$ and $\Phi2$ clocks. Such reduction is shown in Figure 6.27, where the effect of a 4-phase interleaving is illustrated. In the DC/DC converter in the 4WiCS interface, a 10-phase interleaving is employed. This is achieved with a 5-stage current starved ring oscillator generating $\Phi1$ and $\Phi2$ and their phase-shifted version. For this reason, 10 cells are used, each comprising a capacitor of value $C_{fly}/10$ (400 pF/10). The top-level architecture of the stitched-capacitor DC/DC converter is shown in Figure 6.29, whereas the circuit implementation of each switched-capacitor module (comprising the capacitor cell) is illustrated in Figure 6.28.

- *Simulated Results:*

Post-layout simulation results show the DC/DC converter achieves an output average voltage $V_{out-mean}$ of $2.3\text{ V} \pm 0.1\text{ V}$ and a output voltage ripple $V_{out-ripple}$ of $22\text{ mV} \pm 8\text{ mV}$ – with a 5 V input voltage, an output capacitance of 100 pF, and an output load current varying from 0.5 mA to 2.5 mA. The highest PCE reached during simulation is 85%, achieved with a load current of 1 mA. Figure 6.30 shows the input and output signals of the DC/DC converter, together with the 10 switching clock signals generated by the ring oscillator.

It is clear that using a switched-cap DC/DC converter significantly improves the PCE compared to linear regulators. To achieve the 5 V-to-1.8 V conversion – specific requirement for the CAND0 system – the whole voltage drop would be lost in heat dissipation on the pass transistor if only linear regulators were used. By employing a combination of the DC/DC converter (5V-to-2.5V – e.g. 85% PCE) and a linear regulator (2.5V-to-1.8V – e.g. 70% PCE), the total PCE is $\sim 60\%$ instead of $\sim 35\%$. Similarly to the rectifier, the trade-off is in circuit area and design complexity.

Voltage Regulation - Capacitor-less Low-Dropout Linear Regulator

Capacitor-less low-dropout regulators are used for generating both the 5 V and 1.8 V domains. Typical LDO voltage regulators require a relatively large output capacitor in the single microfarad range to create a dominant pole and guarantee adequate stability. The topology employed

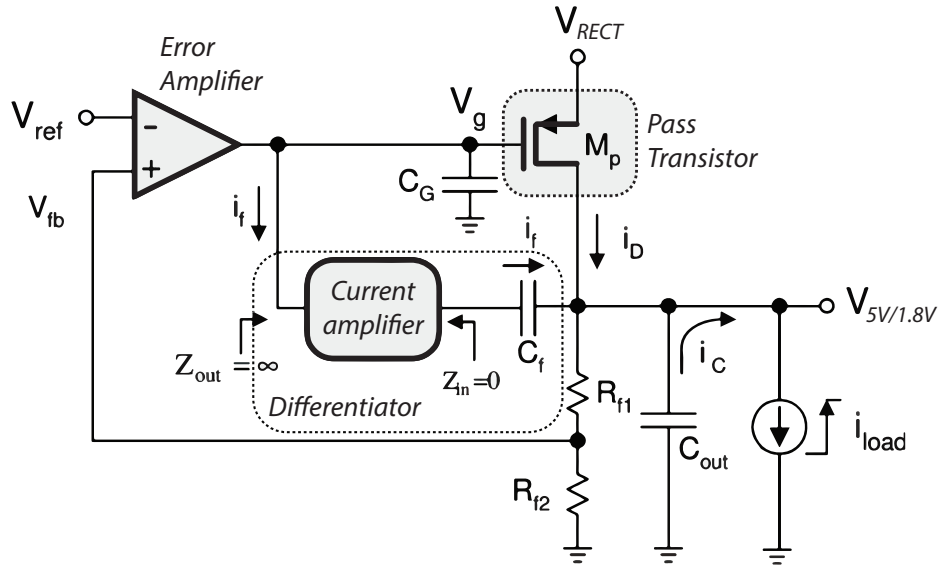


Figure 6.31: LDO linear regulator topology used for implementing a capacitor-less regulator. The presence of the *differentiator* allows to use a small load capacitor (pF range) while (1) maintaining stability in operational conditions, (2) minimising under-/over-shoots during transient, and (3) achieving good line/load regulation. Figure adapted from [185].

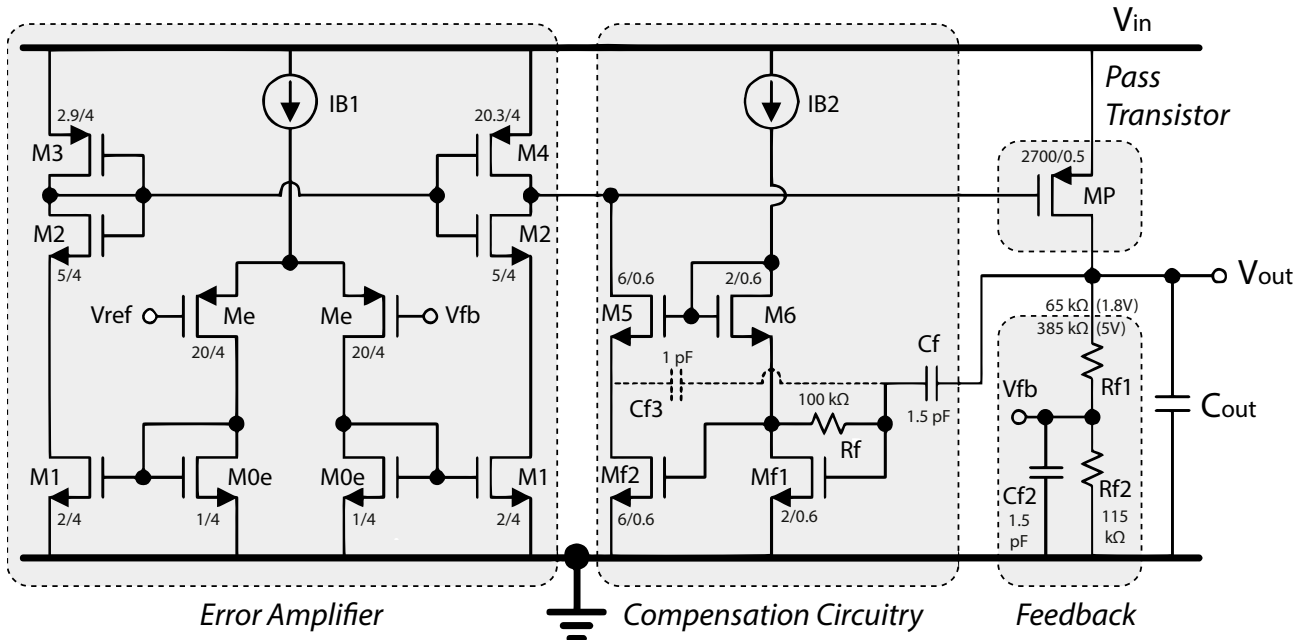


Figure 6.32: Schematics of capacitor-less LDO with differentiator. The output of a 3 current-mirror OTA drives a PMOS pass transistor whose gate is controlled also by a compensation circuit, which influences the position of the two frequency poles introduced by the pass transistor, allowing for improved stability. Figure adapted from [185].

here allows for the large external capacitor to be removed without compromising performance, i.e. AC stability and load transient response [186]. This is achieved by using a compensation scheme based on the differentiator [185]: a current amplifier in series with the feedback capacitor C_f that acts as an auxiliary fast loop in addition to the main voltage loop as shown in Figure 6.32. Therefore, the LDO is composed of:

- An *error amplifier* using operational transconductance amplifier (OTA) architecture. It includes a differential amplifier ($M_E M_E$) and 3 current mirrors ($2 \times M_{oe} M_1$, M_2 - M_3);
- A *pass transistor* M_P designed as a common-source amplifier;
- A *differentiator* (M_{f1} , M_{f2} , M_5 , M_6 , C_f) that amplifies the current to charge the pass transistor's gate quicker when the input voltage varies. It includes two common-source amplifiers M_{f1} , M_{f2} with a current-mirror as an active load M_5 - M_6 .

The 5V-LDO is used to generate the 5V domain to power up the stimulation drivers, the diagnostics instrumentation, and the body potential driver. This receives as input signal directly the voltage output of the rectifier V_{RECT} . Two 1.8V-LDOs are implemented to generate the 1.8V digital domain and the 1.8V analogue domain of the core circuitry. The former is responsible for powering the digital controller and the data communication digital circuitry. The second 1.8V-LDO powers the analogue circuits in the neural recording instrumentation. They both receive as input the signal output of the DC/DC halver. In addition, two further 1.8V-LDOs are included in the 4WiCS sub-system, one to power up the digital circuits driving the DC/DC switches and level shifters, and one for supplying the uplink drivers.

- *Simulated Results:*

Post-layout simulations of the 5V and 1.8V LDOs demonstrate the expected capabilities of the capacitor-less LDO to achieve adequate performance both in terms of transient response and in terms of stability. For simplicity, the simulation results of the 5V LDO are hereby considered and discussed – the 1.8V LDO has similar characteristics and performance. The main characteristics to evaluate the transient response of the system are line regulation and load regulation. Line regulation is defined as the circuit's ability to maintain the specified output voltage with varying input voltage [187]. This is typically

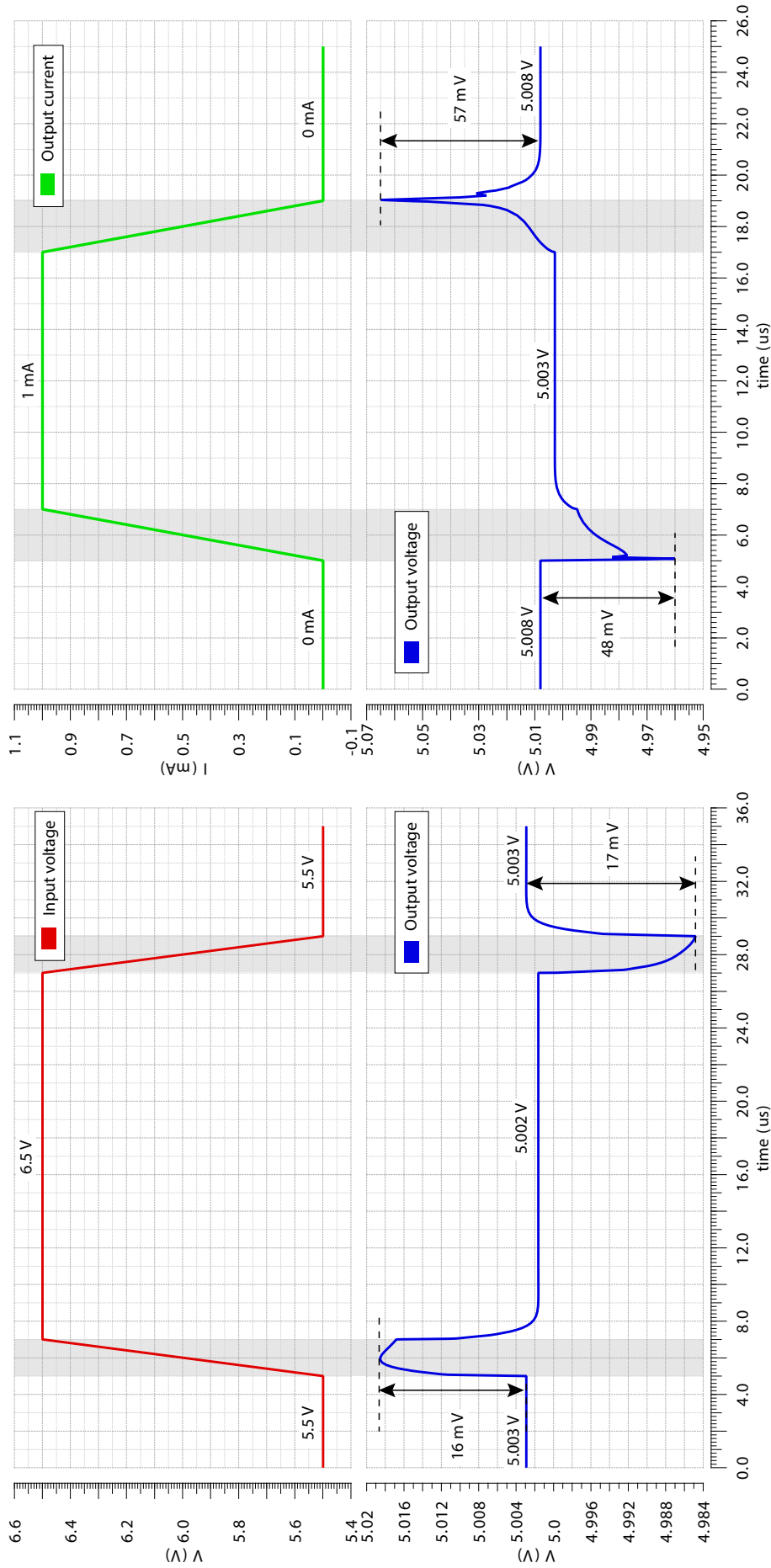


Figure 6.33: Post-layout simulation results of the 5V LDO: (left) line regulation when 1 V step-up and step-down voltage is applied; (right) load regulation when 1 mA current is applied and removed at the load.

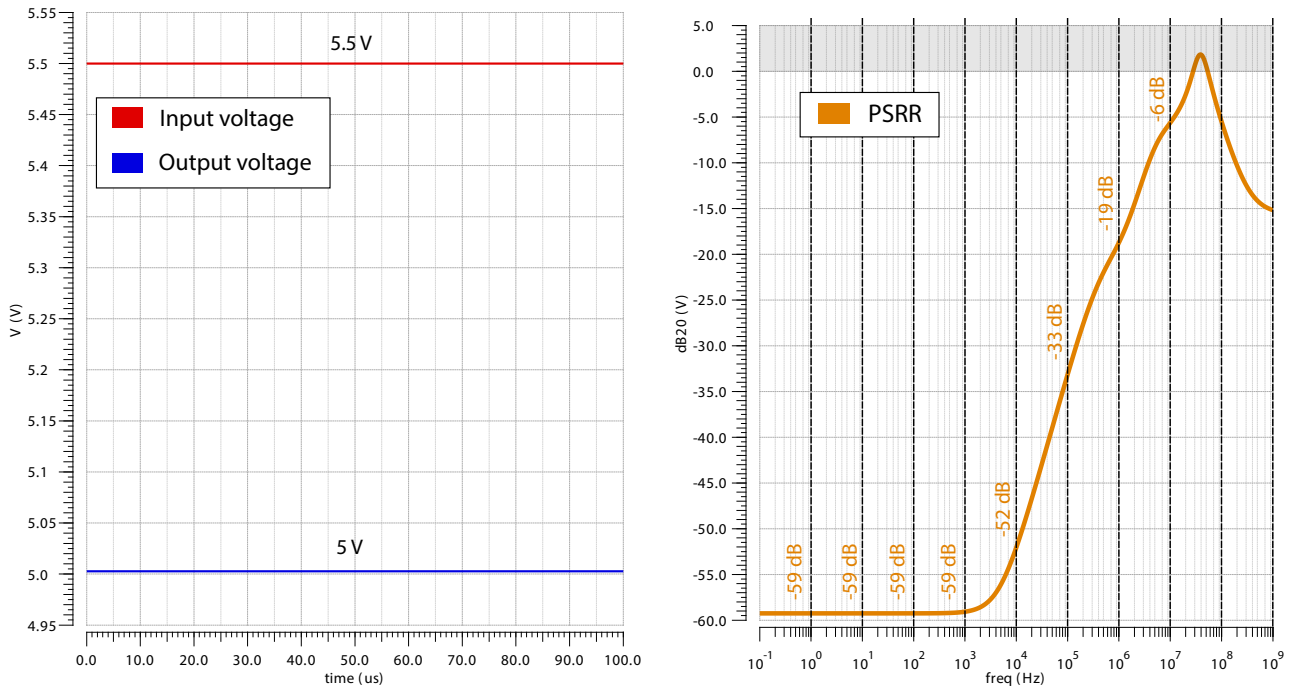


Figure 6.34: Post-layout simulation results of the 5V LDO: (left) input/output signals; (right) PSRR.

evaluated by applying a step-up to the input voltage and measuring the output voltage variation. As shown in Figure 6.33 (left), the output voltage variation is less than 1 mV when a 1 V increase is applied to the input. During the transition at the input, the LDO output signal receives fast spikes of current injections that increase the output voltage for a brief period of time. This is settled within 1 μ s after transition, without exceeding 17 mV at the peak of the spike.

Load regulation is defined as the circuit's ability to maintain the specified output voltage while varying the output load [187]. This is evaluated by increasing the load current from 0 mA to a typical operation load (in this case, 1 mA). As shown in Figure 6.33 (right), the output voltage variation is less than 5 mV and the spikes reach a maximum value of 57 mV, settling to steady-state in $\sim 2 \mu$ s after the transition.

Another important parameter for a linear regulator is the Power Supply Rejection Ratio (PSRR). Also known as ripple rejection, PSRR measures the LDO's ability to prevent the regulated output voltage fluctuating caused by input voltage variations. The same relation for line regulation applies to PSRR except that the whole frequency spectrum is considered. Figure 6.34 (right) shows the simulated 5V LDO PSRR from 0.1 Hz to 10 GHz. The ripple rejection is high at low frequencies (-59 dB up to 1 kHz) and starts to

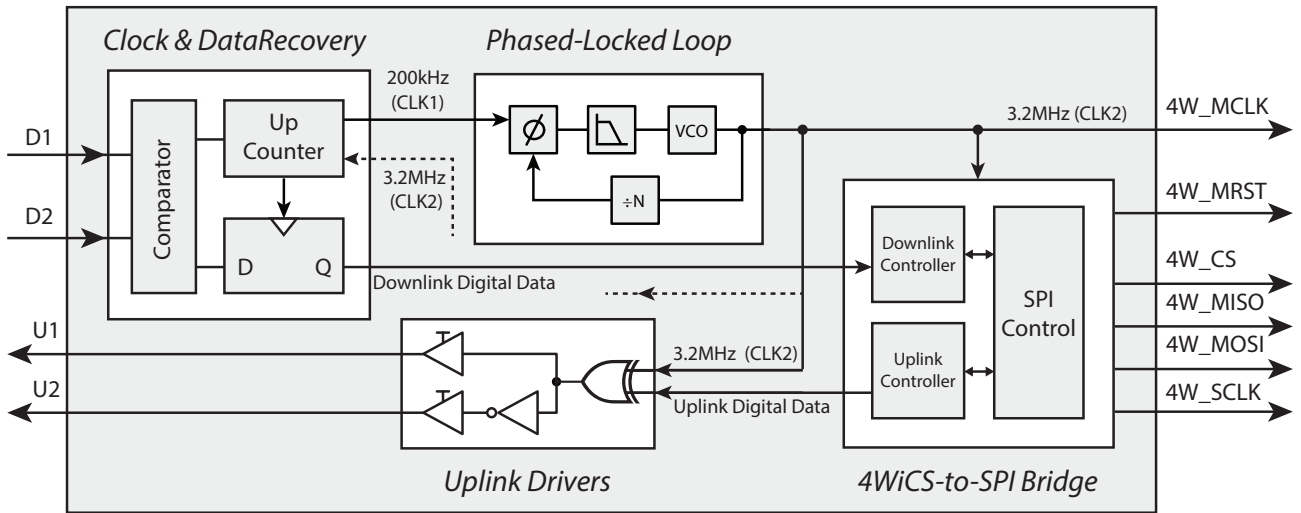


Figure 6.35: Top-level architecture of the Data Communication Unit within the CANDO4 4WiCS interface.

degrade at higher frequencies. It can be noticed the PSRR is -30 dB at 200 kHz (downlink frequency with a high source of interference and ripple generation).

6.3.2 Data Communication Unit

The DCU is responsible for implementing a full-duplex communication between one 4WiCS master and multiple 4WiCS slaves. It operates as a communication interface, which translates the 4WiCS protocol to the SPI protocol used by the CANDO4 CORE. The DCU receives along the downlink path (master-to-slave) the AC downlink signal from the master through two wires of the 4-wire lead (DW1 and DW2) and recovers the encoded digital data and the 200 kHz clock signal. The latter is then used by the PLL to synthesis the master clock, a higher frequency clock (x16) of 3.2 MHz required by the digital circuitry in the CANDO4 CORE. Both the downlink digital data and the clock are fed to a digital circuitry that acts as a 4WiCS-to-SPI bridge, generating the SPI Chip Select, SPI Clock, and SPI MOSI signals to forward communicate with the (CANDO4 CORE) slave.

The slave device communicates back to the master with the SPI MISO signal, which is received by the 4WiCS-to-SPI bridge and translated into the uplink digital data. This in turn is encoded

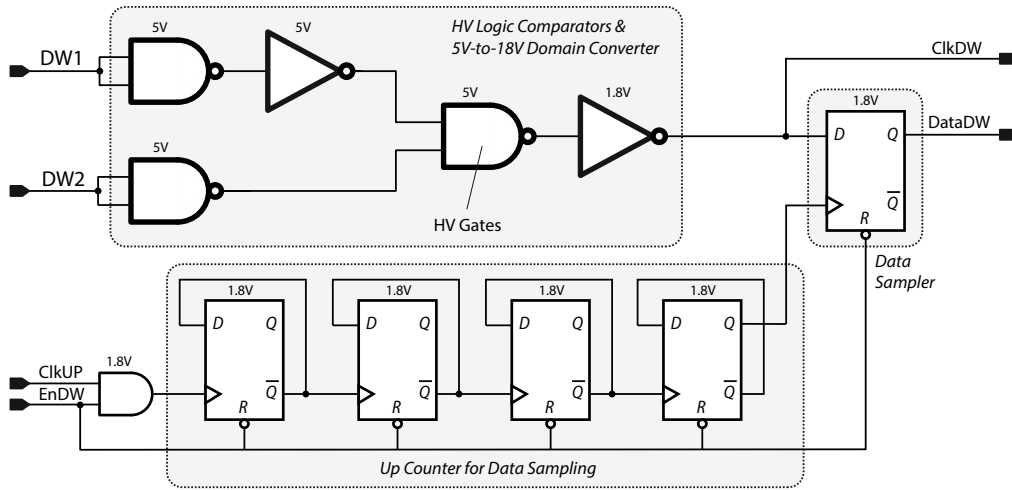


Figure 6.36: Clock and Data Recovery architecture. The high voltage logic comparators recover the clock signal and shift the voltage level from 5V to 1.8V, while the up-counter circuit ensures the clock signal is sampled at half the period to decode and retrieve the data signal.

and conditioned by the uplink drivers in order to be transmitted through the second pair of wires (U1 and U2) along the uplink path (slave-to-master).

Downlink Circuits - Clock & Data Recovery and Phased-Locked Loop

The downlink module ensures the signal along the downlink path is correctly retrieved, decoded, and adjusted to be sent to the 4WiCS-to-SPI bridge.

Clock and Data Recovery:

The clock and data recovery circuit first converts the $V_{DW1-DW2}$ downlink signal from $>5V$ differential to 1.8 V single-ended. This is achieved with a non-hysteretic comparator and a 5 V-to-1.8 V level-down shifter. Such single-ended downlink signal has the same frequency as the low-frequency clock (CLK, 200 kHz) and encodes the data information in the pulse width (33% duty cycle for logic low, 66% duty cycle for logic high). The CLK1 signal can be therefore derived directly from the single-ended downlink signal and sent to PLL, whereas the data signal requires further processing. The data separation is obtained with an up counter using the high-frequency clock from PLL output (3.2 MHz) to trigger the sampling circuit at half the low frequency (200 kHz) time period. This detects therefore the Pulse Width Modulation (PWM) code and ensures data alignment to input differential signal V_{D1-D2} . The data signal

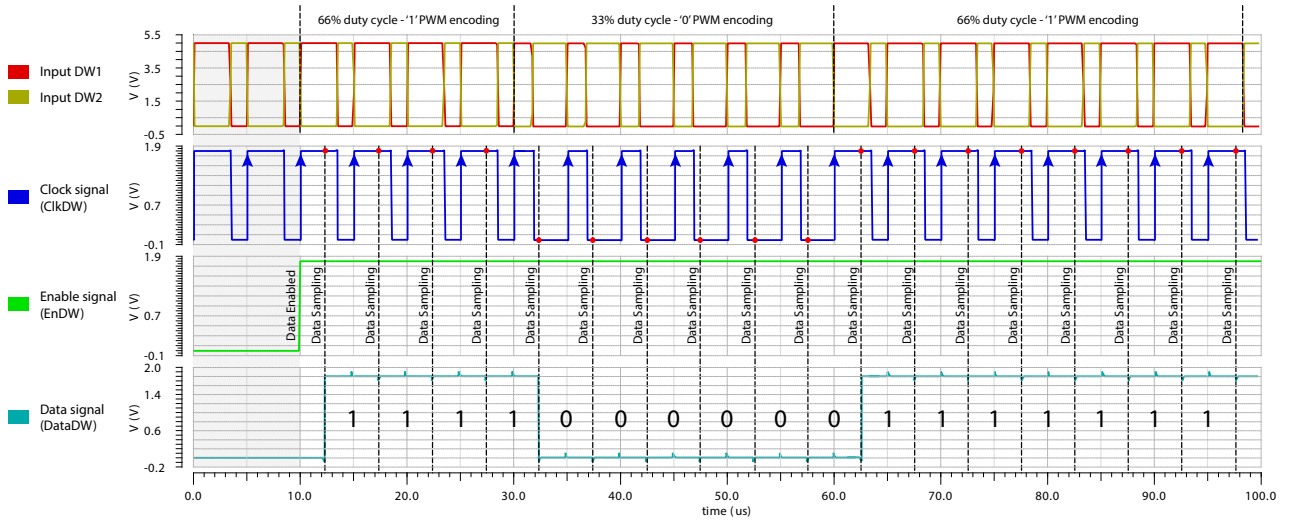


Figure 6.37: Post-layout simulation results of the CRD circuit. Digital data sequence encoded on the downlink signal: “111100000011111111”. The data sampling is enabled at 10μ and clock and data signals are correctly separated and recovered.

is therefore decoded and prepared for further stages.

This method differs significantly from the CDR circuit implemented 4WiCS gen1. The change is done to reduce complexity of the clock and data separation – previously achieved with an edge detector – and to avoid dependence of recovery and clock generation performance on device parasitics – previously based on a thyristor-based delay cell. This new technique, associated with the PWM encoding method, increases the reliability of the downlink communication and clock stability.

- *Simulated Results:*

Post-layout simulation results of CDR circuit demonstrate the 5 V differential input (downlink signal) is correctly down-scaled to a 1.8 V signal (ClkDW), which corresponds to the recovered clock. This is sampled at a precise time (at half period) to recover the data encoded with the PWM technique (66% duty cycle = ‘1’, 33% duty cycle = ‘0’). As shown in Figure 6.37, clock and data are correctly separated and data information is decoded.

Phased-Locked Loop:

A second-order Phase-Locked Loop is implemented to generate a higher frequency clock CLK2

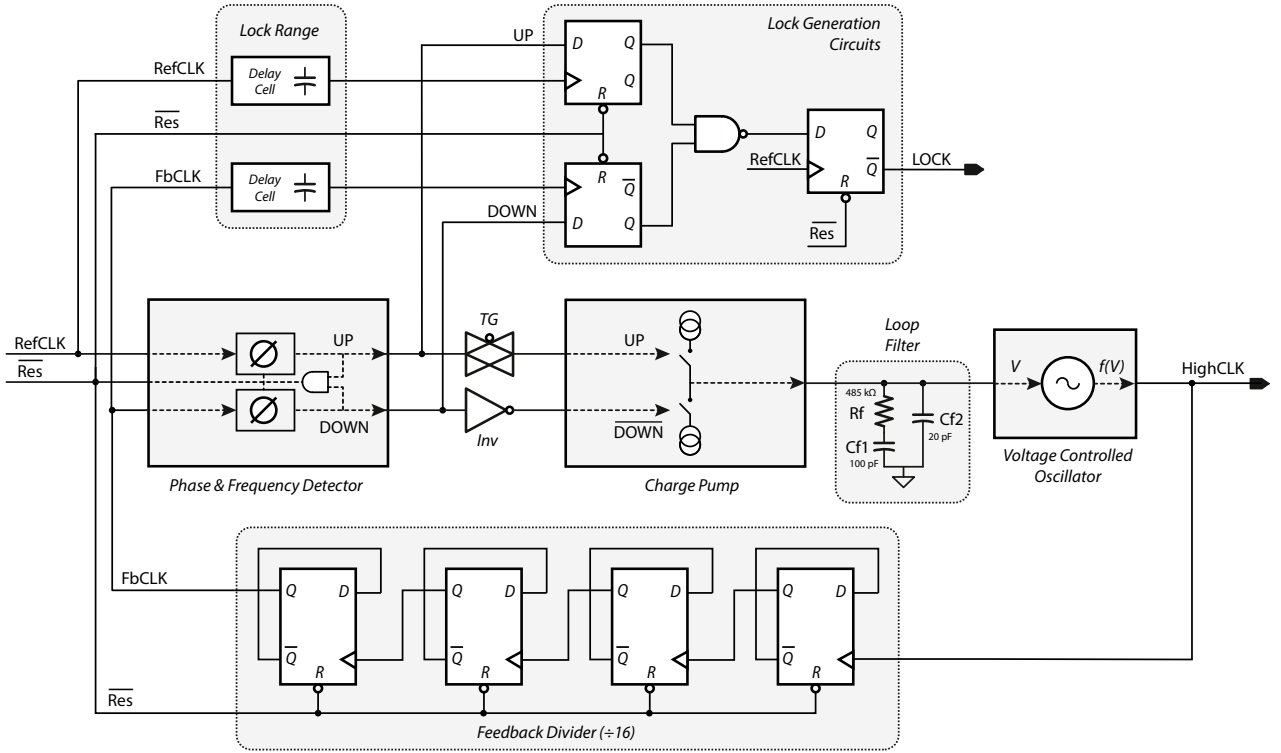


Figure 6.38: Top-level architecture of the Phased-Locked Loop. It is responsible for generating the 3.2 MHz uplink clock signal (HighCLK) starting from the 200 kHz downlink signal (RefCLK). It comprises: a phase and frequency detector, a charge pump, a loop filter, a voltage controlled oscillator, a feedback divider, and a lock generation circuit.

(3.2 MHz) starting from the lower frequency CLK1 (200 kHz) to drive the uplink drivers and CANDO4 CORE [72]. This consists of a *phase and frequency detector (PFD)*, a *charge pump (CP)*, a *low-pass filter*, a *voltage-controlled oscillator (VCO)*, a *feedback divider*, and a *lock signal generator*. Its function is achieved by measuring the phase difference between the input signal (CLK1) and output signal (CLK2) and tuning the output signal frequency until such difference is eliminated (output locked to input). For the past three decades, most PLL designs have employed a combination of a PFD and a CP, therefore these PLLs are often referred to as CP-PLLs. CP-PLLs are preferred over other topologies of phase-locked loops due to the advantages of large system gain, low static phase offset, and low bias current.

The PFD is responsible for comparing the two phases θ_{CLK1} and θ_{CLK2} . It is an error detector that uses two D-type flip flops with a delay element and acts as a controller for the current sourced by a charge pump (depending on the phase measured) through two digital signals – *UP* and *DOWN*. The CP outputs a single-ended signal whose voltage is raised or lowered by charge

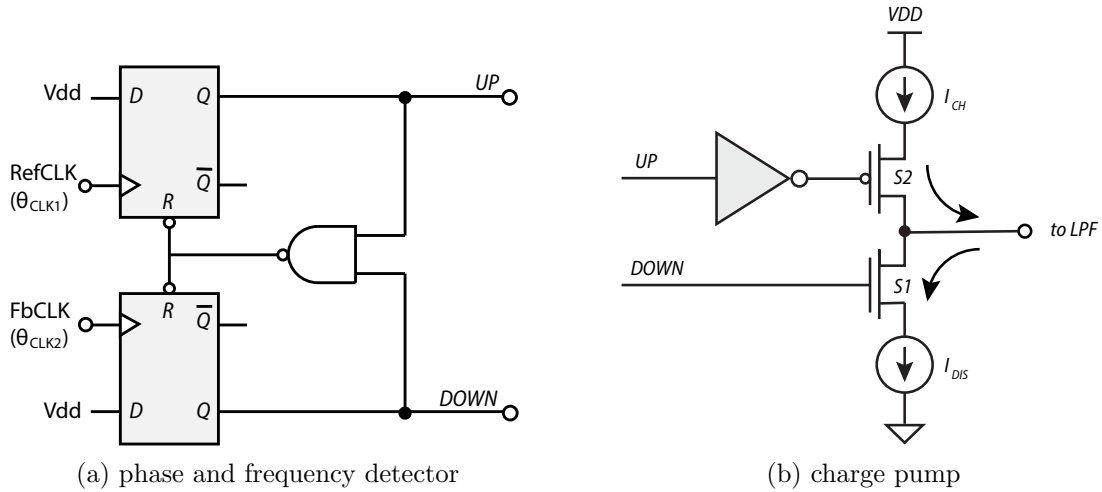


Figure 6.39: Typical architecture for the PFD and CP circuits in a conventional CP-PLL.

exchange with the CP load (low-pass filter). This is achieved with two current sources, I_{CH} and I_{DIS} , which are activated from the UP and $DOWN$ digital signals, as shown in Figure. In a conventional CP, two transistor switches are used to implement this (Figure 6.39b).

The PFD used in the 4WiCS interface is based on the topology called Type IV PFD and consists of two D flip-flops with reset, as it is shown in Figure 6.39a [188]. The implemented circuit optimises the number of gates for each D flip-flop and allows for an additional external reset signal. Various charge pump architectures have been implemented in the years as part of a CP-PLL. The three most common categories are: (1) switch in drain; (2) switch in gate; and (3) switch in source. As the names suggest, the difference between categories is how the switching element connects to the circuit generating the current source (i.e. current mirror) [189]. The charge pump circuit designed as part of the PLL described hereby is based on a source-switched charge pump due to its fast switching speed and low power consumption. The two transistors M_n and M_p are employed to remove most of the charges stored on the parasitic capacitance present at node A and B, thus minimising the ‘charge sharing’ effect [190]. This guarantees a significant reduction of the charge sharing effect during turn-off periods of UP and $DOWN$ signals from the PFD [191]. In addition, to reduce the charge coupling to the gate of the $M1$ and $M2$ transistors (current sources) and to enhance the switching speed, M_{C1} and M_{C2} are added between the gates of $M1$ and $M2$ and the power supply – respectively VSS and VDD [192].

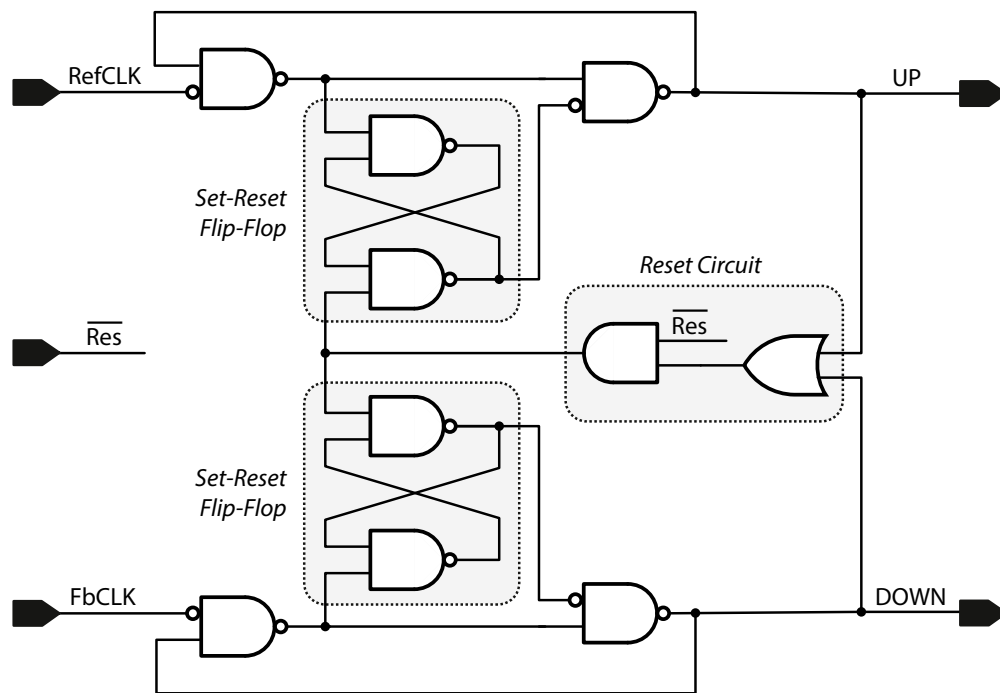


Figure 6.40: Phase & Frequency Detector architecture with external reset.

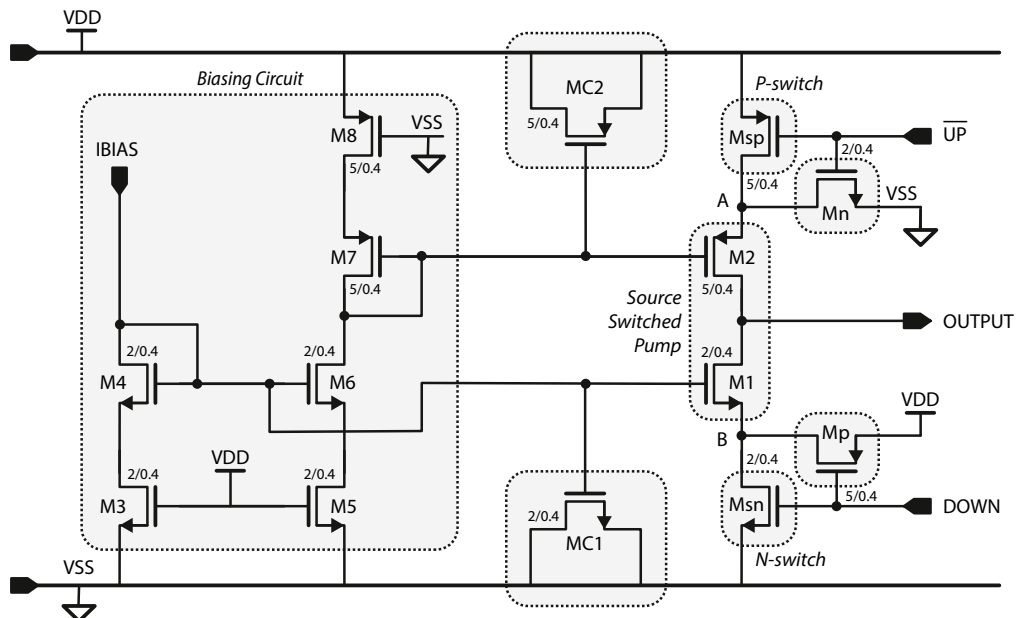


Figure 6.41: Charge Pump architecture based on a source-switched topology.

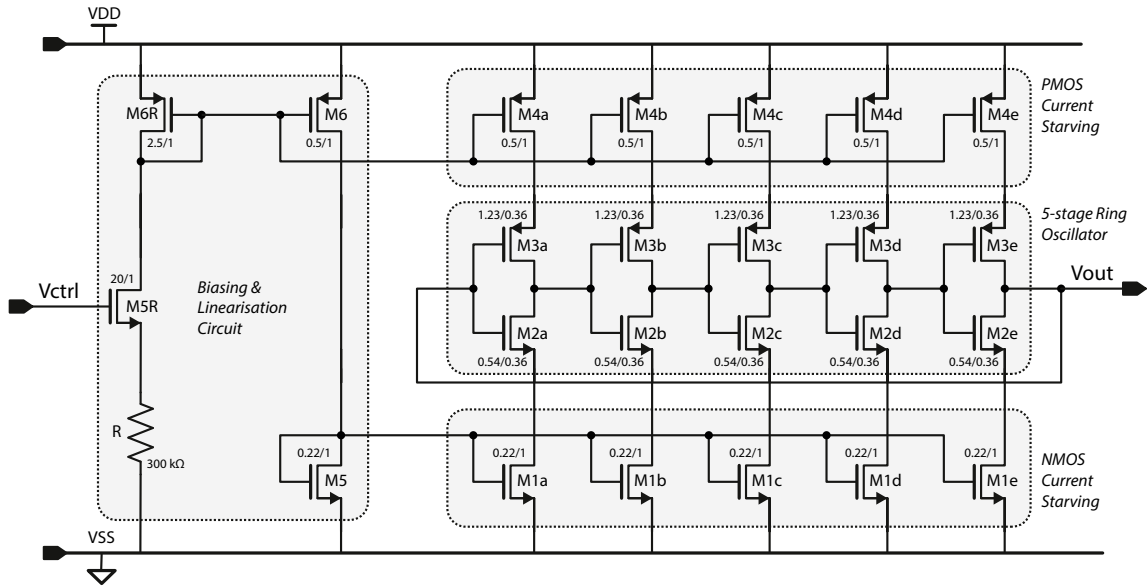


Figure 6.42: Voltage Controlled Oscillator architecture based on a 5-stage ring oscillator.

The loop filter conditions the voltage outputted by the charge pump in order to be used by the VCO. The latter is an oscillator whose output oscillation frequency is controlled by the input voltage. The feedback divider ensures the correct frequency multiplication is obtained on the output signal. When the comparison is in steady-state, and the PLL output frequency and phase are matched to the PLL input frequency, the PLL is in “locked” condition and a lock signal is raised. A 2nd order passive filter is used as loop filter, while a simple current-starved ring oscillator is used as VCO. Given the low jitter and frequency stability requirements for the CLK2 (3.2 MHz), a wide M10 input transistor is employed in combination with 300 kΩ resistor connected at its source. Moreover, the addition M5 and M6 allows for the current flowing in the various inverter stages to be linearised [193].

- *Simulated Results:*

Post-layout simulation results of PLL have been performed both for the PLL as a full system and for the sub-circuits separately. The PLL achieved its ‘locked’ condition in 220 μs from startup. The system is considered locked when the output signal has achieved an average frequency of 3.2 MHz with a standard deviation of < 5 KHz, as shown in Figure 6.43. The histogram in Figure 6.43 (right) shows the distribution of the simulated frequency samples (897) after the PLL is locked, demonstrating the lock circuit functionality and the high performance of the PLL. Figure 6.44 illustrates the simulation of the PFD

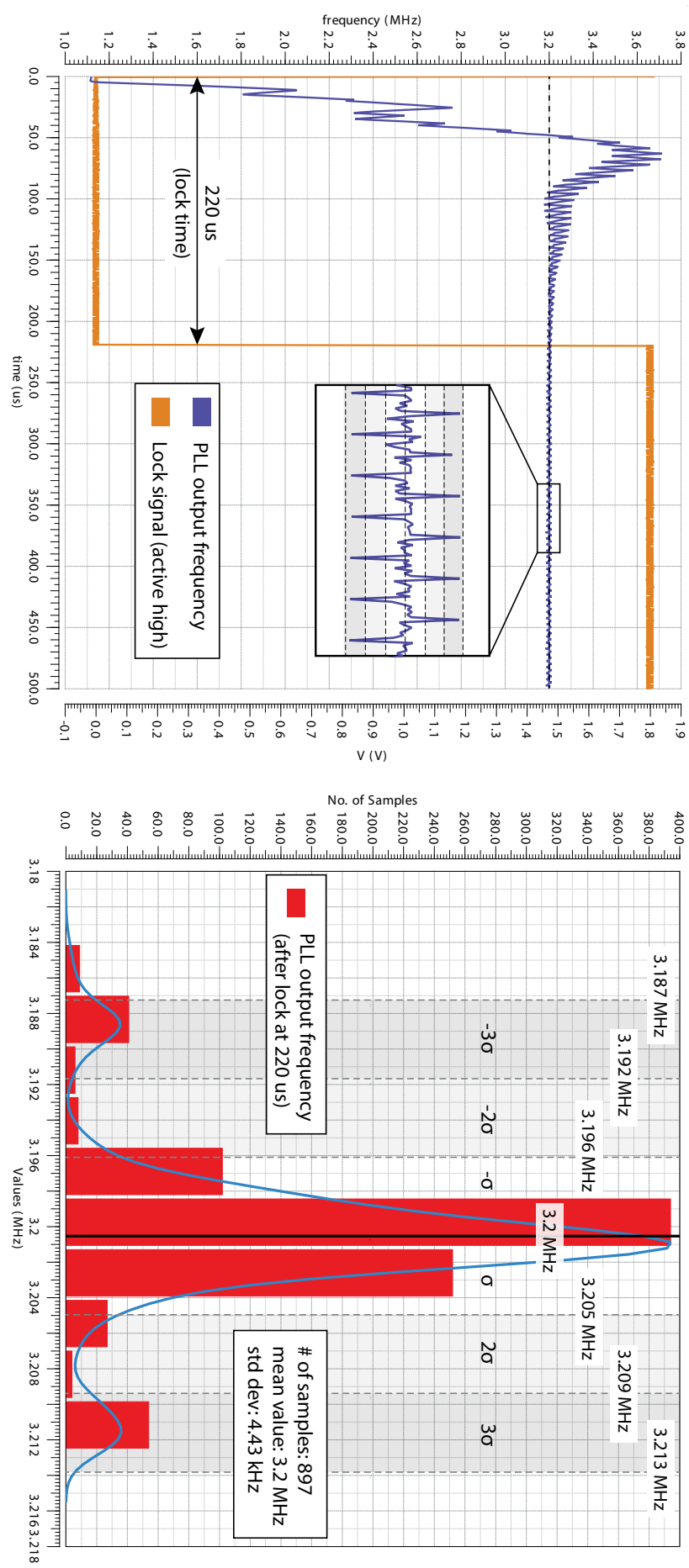


Figure 6.43: Post-layout simulation results of the PLL: (left) PLL output frequency and lock signal activating when the frequency enters the required range. (right) Distribution of the PLL frequency after the locked condition is achieved.

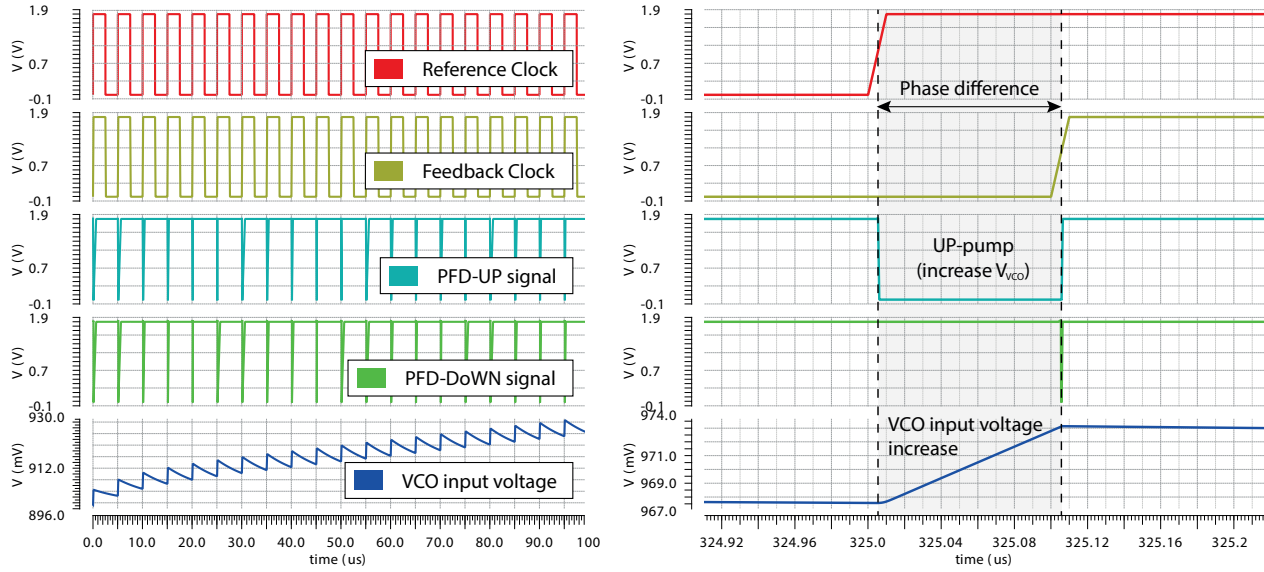


Figure 6.44: Post-layout simulation results of the PFD and CP circuits. The phase difference between the reference and feedback clock activates the charge pump to modify the VCO voltage accordingly.

and CP, highlighting the UP and DOWN signals responsible respectively for the increase and decrease of the VCO input voltage. As shown in Figure 6.44 (right) the phase difference between the reference clock (RefCLK) and feedback clock (FbCLK) activates the charge pump that increases the voltage, which in turn will increase the feedback clock frequency to reduce the phase difference.

The VCO simulated characteristics is presented in Figure 6.45. To achieve an output signal (HighCLK) with a 3.2 MHz frequency, the VCO requires an input voltage V_{VCO} of 1.14 V. This is chosen at design stage to ensure the output frequency is in the linear range of the VCO characteristics. The maximum reachable frequency of the oscillator is 6.3 MHz (with 1.8 V input voltage).

Uplink Circuits

The uplink module ensures the signal along the uplink path is correctly encoded and adjusted to be transmitted through the U1 and U2 wires.

Voltage Shift and Line Driver: The Manchester encoding is implemented by an XOR gate which combines the uplink digital data received by the 4WiCS-to-SPI bridge with 3.2 MHz

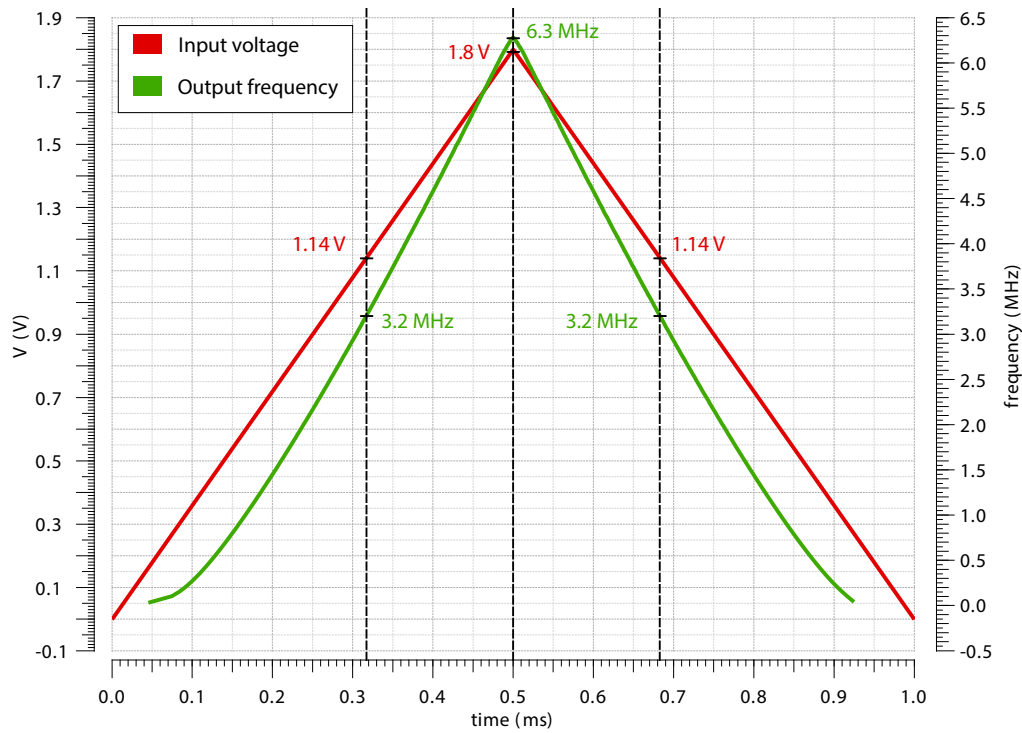


Figure 6.45: Post-layout simulation results of the VCO. The characteristics of the VCO show a highly linear relationship between the input voltage and the output frequency.

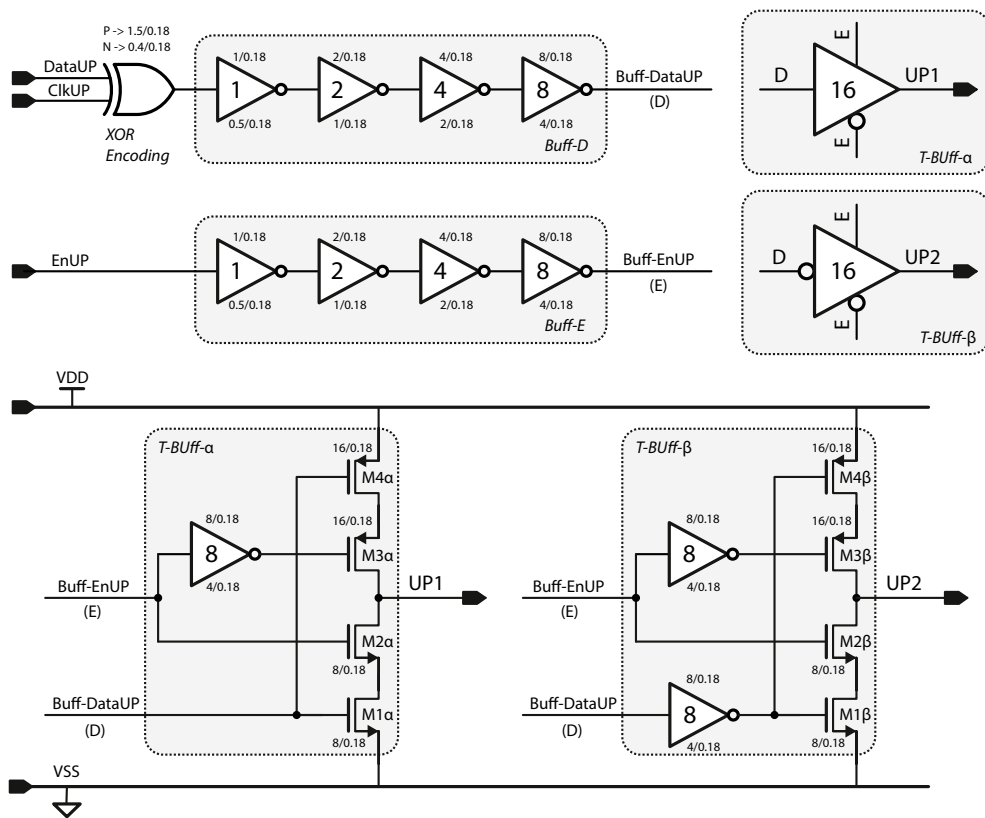


Figure 6.46: Uplink Drivers architecture based on a 5-stage inverter buffer and front-end tristate buffers.

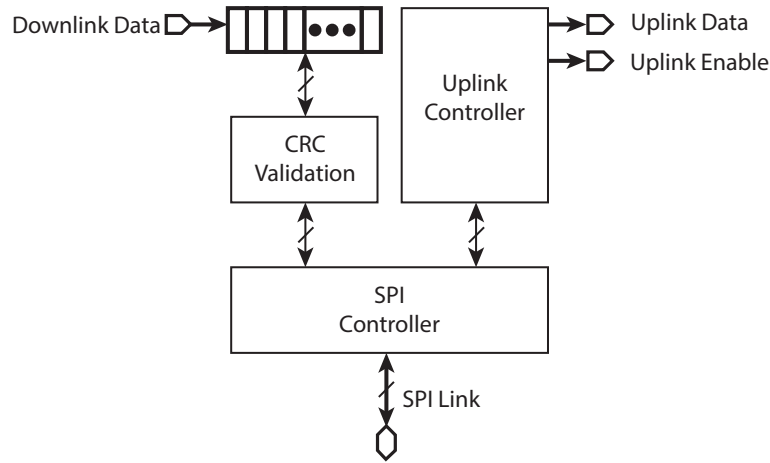


Figure 6.47: High-level structure of the 4WiCS Digital controller for 4WiCS-to-SPI signal conversion.

master clock synthesised by the PLL. The encoded data signal is conditioned by the uplink drivers through a 4-stage inverting buffer followed by a wide tri-state buffer to be transmitted as a differential signal on the two uplink wires U1 and U2 on the implantable lead. The large size of the drivers is required because of the relatively large RC time constant of the uplink wires. As learned from the uplink tests shown in Chapter 5.2.3, the uplink signal received at the chest implant module is significantly degraded due to the filtering response of the Cooper cable. Also, a separate LDO voltage regulator is used exclusively for supplying the uplink drivers.

4WiCS Digital Controller

4WiCS-to-SPI Bridge: The 4WiCS-to-SPI bridge is a digital circuit that operates as a digital controller and bidirectional translator between the 4WiCS protocol and the SPI protocol. It identifies valid data packets and feeds the data packet to the SPI controller.

Input data from the 4WiCS downlink is fed into a 36-bit FIFO (First-in-First-out) buffer. The CRC check is performed on the fly within such 36-bit FIFO. Once a valid data packet is identified in the FIFO, it will be latched and pushed to the SPI controller. Conversely, when a valid SPI is received from the slave, i.e. from the CANDO4 CORE controller, the received data will be streamed out via the uplink controller. The structure is shown in Figure 6.47. The SPI controller is based on the same SPI protocol, as discussed in Section 6.2.2, i.e. LSB first, 32-bit. It acts as a master controller in the SPI link to the CANDO4 core digital controller.

6.4 Simulated System Results

The circuits within the CAND04 4WiCS system have been simulated both separately – as shown in the previous section – and within the 4WiCS system. To achieve so, a testbench schematic has been prepared that includes also models of the chest implant 4WiCS interfaces and Cooper cable to emulate the characteristics of the communication through downlink and uplink signals. Moreover, realistic loads have been added to the 4WiCS outputs to emulate the typical operation of the CORE sub-system and its circuits.

Figure 6.48 shows a summary of the main signals 4WiCS signals simulated in the conditions mentioned above. The transient simulation is initiated with the downlink (and power) signals generated at the CI – 6 V peak-to-peak. This is transmitted through the cable model (causing a voltage drop) and received by the 4WiCS system through the WD1 and WD2 inputs (red and green traces). The transitions of such signals have an average duration of 165 ± 5 ns. Due to the filtering effect given by the Cooper cable, AC-coupling capacitors, and the equalization capacitors, the differential squarewaves received don't reach immediately the peak voltage, but rather increase with the cumulative RC time constant.

The rectifier output (blue trace) follows this trajectory as well, reaching 5 V after $25 \mu\text{s}$. At a steady state, the rectifier output reaches an average of 5.55 V with a ripple of 23 mV. The 5V-LDO output (pink trace) starts regulating at $30 \mu\text{s}$ – when the voltage input (rectifier output) is at 5.12 V. The average regulated voltage output is 4.95 V with a ripple of 25 mV. This is higher than expected and is due to one main reason: the 200 kHz downlink signals are squarewaves, thus they have high-frequency components due to their fast switching transitions. These end up falling in the frequency range where the PSRR of the LDO is very low (or absent), thus causing a significant output ripple.

The switched-capacitor DC/DC converter is activated by the power-on-reset circuit $15 \mu\text{s}$ after simulation startup, when its input (rectifier output) achieves 4.5 V. The DC/DC output ripple (purple trace) – 46 mV at steady state – has two major components due to: the downlink switching transitions and the interleaving switching. The latter has a frequency of 6 MHz

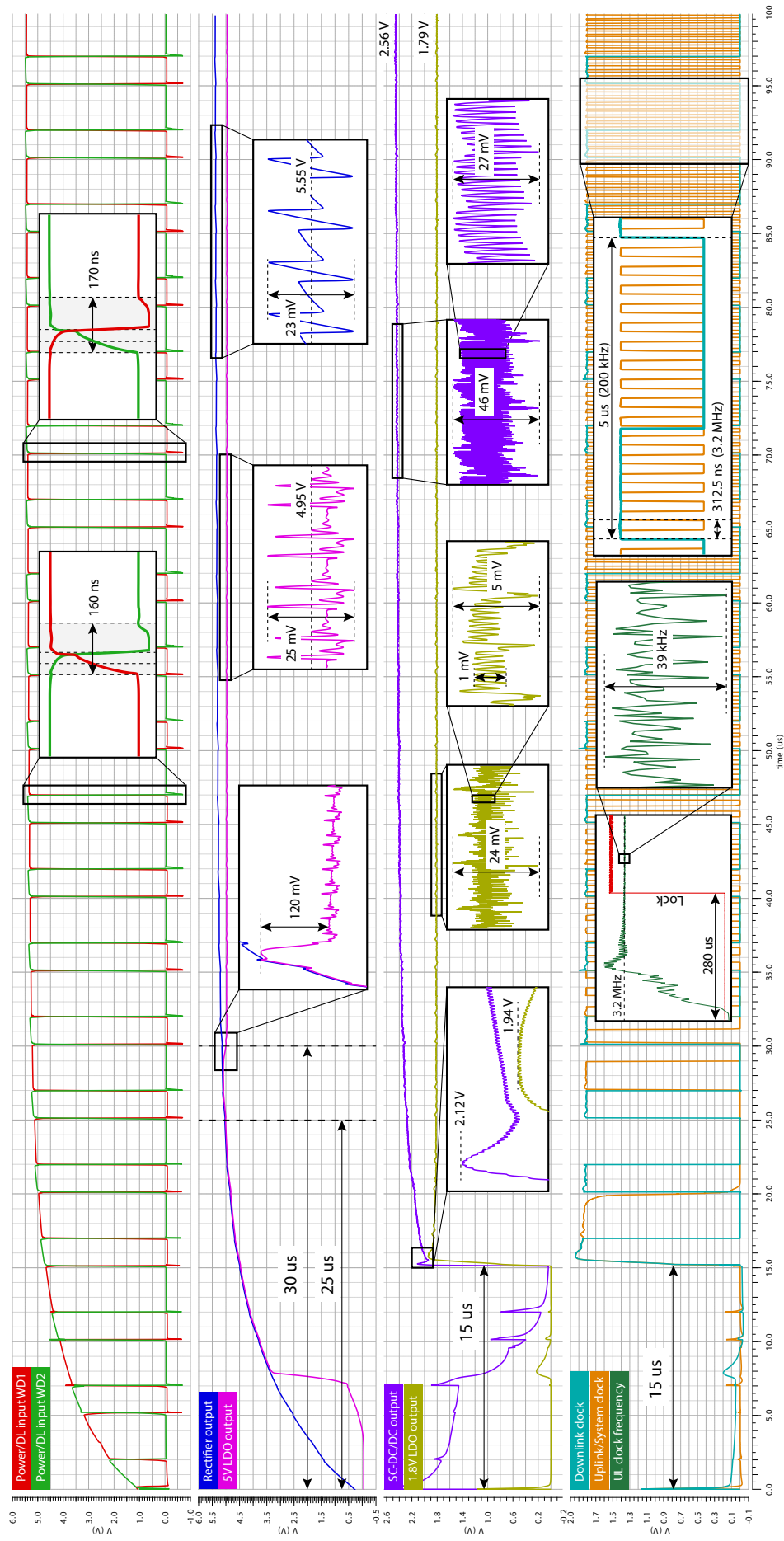


Figure 6.48: Post-layout simulation results of the 4WiCS sub-system with a representation of the main signals. These are (in order from top to bottom): downlink/power signals, rectifier output signal, 5V-LDO output signal, DC/DC converter output signal, 1.8V-LDO output signal, downlink clock signal, uplink clock signal, uplink clock signal frequency.

(generated by the ring oscillator), however, since there are 10 interleaving stages equally shifted in phase, the noise injected from the interleaving switching has a frequency of 60 MHz – causing 27 mV ripple. The 1.8V-LDOs are activated right after the DC/DC output exceeds 1.9 V by a 2nd POR circuit. The average voltage of the 1.8V-LDOs is 1.79 V with an output ripple of 24 mV (yellow trace). This includes noise components caused both by the downlink switching (largest component at 24 mV) and the DC/DC switching – 6 MHz (5 mV) and 60 MHz (1 mV).

When the 1.8V-LDO powering up the digital circuits is activated (at 15 μ s), the data communication unit is turned on. The clock signal is recovered (light-blue trace) and the PLL starts generating the uplink clock (3.2 MHz – orange trace). This achieves the locking condition after 280 μ s, raising the lock signal. Due to system complexity, the data recovery, uplink drivers, and digital controller are not simulated as part of the full system.

6.5 System-on-Chip Implementation and Fabrication

The CANDO4 System-on-Chip has been designed and implemented in CMOS TSMC CV018BCD technology, a high-voltage process that allows for a minimum mosfet channel length of 180 nm and up to 70 V HV devices. Other relevant features of this technology are listed in the following:

- Single/double gate oxide options (1.8 V, 5/6/7/8/12/16/20/24/29/36/45/55/65/70V)
- 1 polysilicon layer, N+/P+ poly gate, unsalicyded resistors
- High resistance polysilicon 1k/sq or 3 k Ω /sq.
- Four LV wells, two HV wells and N+ buried layer
- 59 kinds of HV MOS, 14 kinds of HV BJTs, 28 kinds of HV diodes, 8 kinds of HV resistor, 15 kinds of LV MOSFETs, 14 kinds of switch devices, 10 kinds of slit devices, OTP.
- Tungsten contact and via, CMP, AlCu interconnection, metal fuse
- 4-6 metal layers, top metal options: 8K, 8K+15K, 8K+30K, 8K+40K
- 1fF/ μ m² and 2fF/ μ m² MIM capacitors between below top metal or 2nd top metal

The floorplan, the circuit design layout, and the microphotograph of the fabricated CANDO4 SoC are displayed respectively in Figure 6.49, Figure 6.50, and Figure 6.51.

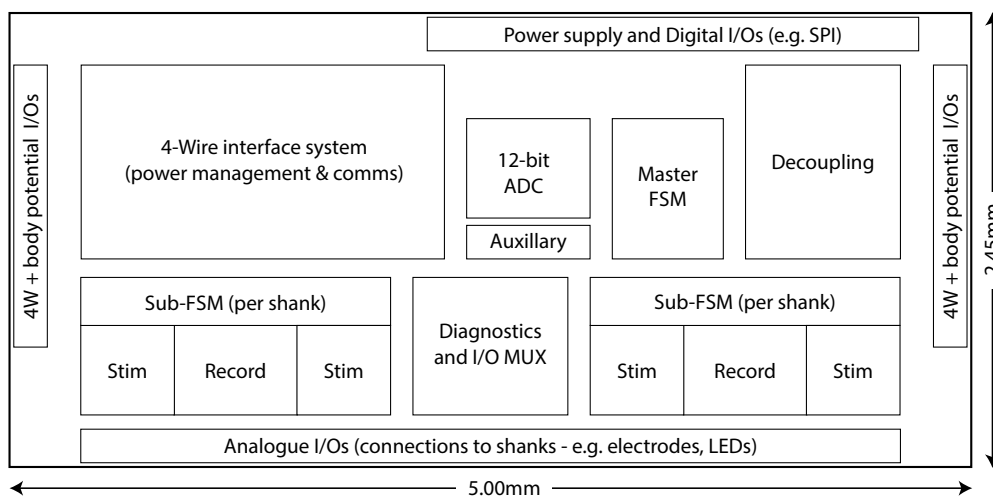


Figure 6.49: CANDO4 System-on-Chip Floorplan.

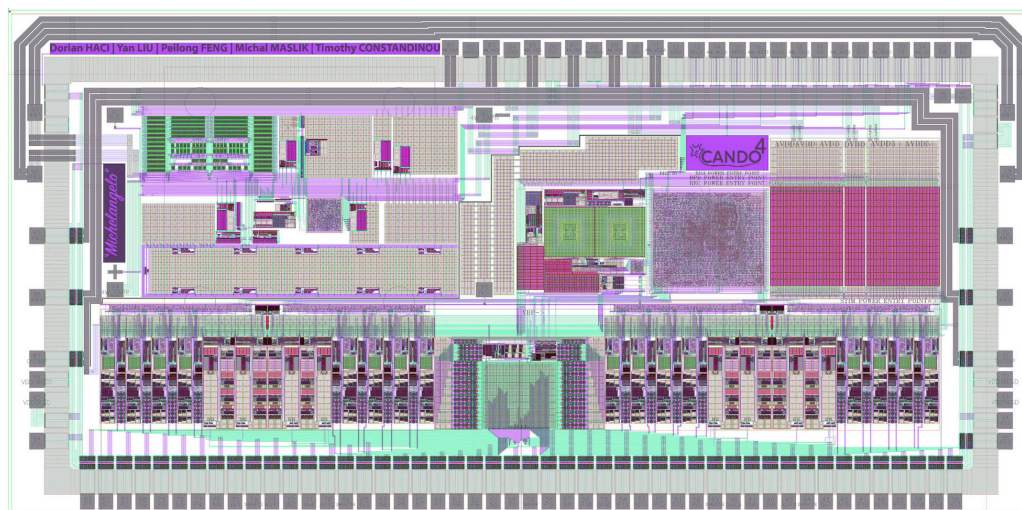


Figure 6.50: CANDO4 System-on-Chip Layout.

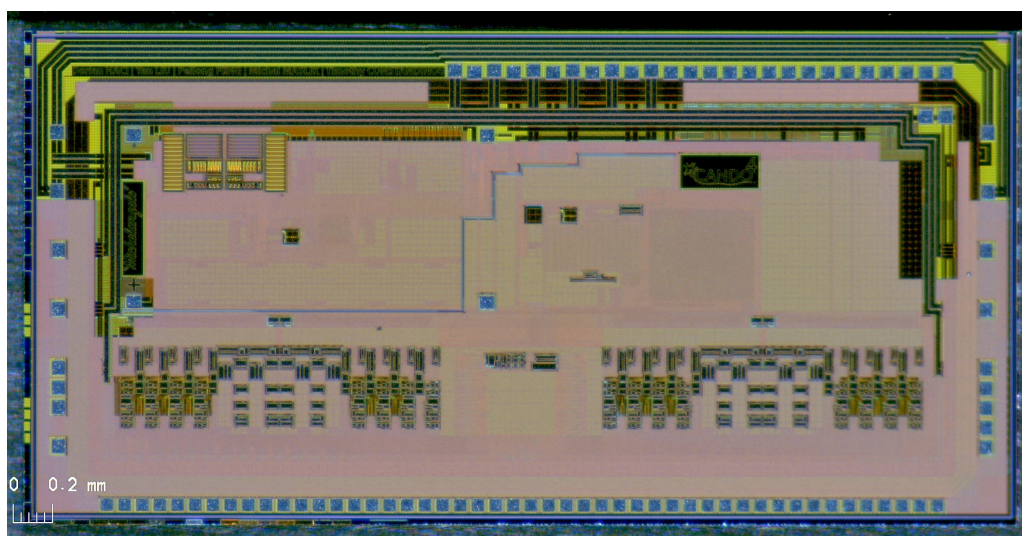


Figure 6.51: CANDO4 System-on-Chip Microphotograph.

6.6 Summary

This Chapter has presented the design and implementation of the CANDO4 SoC – implantable microelectronic system for the CANDO medical device. To contextualise the CANDO4 design specifications within the CANDO implantable system, the technical requirements of the optrode microelectronics for medical use are listed and its functions presented. This has led to the creation of the technical specifications for CANDO4, presented with focus on the differences and improvements from the previous microelectronics generation – CANDO3. One of these is the monolithic integration of the 4WiCS interface within the CANDO4 SoC, allowing the system to employ the 4WiCS protocol to receive power and communicate data through the 4-wire implantable lead.

Since CANDO4 is expected to be used both as part of the medical device for clinical trials and as a research tool for neuroscience, the system is designed with a modular configuration, allowing for it to be used within an implantable system thanks to the 4WiCS interface and to be tested and used in laboratory experiments by connecting to it with external DC supply and SPI communication. This flexibility is achieved by implementing two CANDO4 sub-systems – CORE and 4WiCS – that are integrated on the same chip, but electrically disconnected from each other. In order for them to operate together, thus for the system to be controlled directly from the 4WiCS interface, simple wirebonds are required between specific pads, without the need for any modification to the internal circuitry or addition of external components. The circuit design of both CANDO4 CORE and CANDO4 4WiCS has been described in detail. As the Ph.D. thesis author is the leading architect and chip designer of the 4WiCS circuitry, more emphasis is given to the design, implementation, and simulations of power management and data communication circuits within the 4WiCS sub-system.

Differently from the 1st generation of the 4WiCS interface, CANDO4 4WiCS includes: 5V linear regulation for power supply of the stimulation circuits; duty-cycle (PWM) encoding instead of phase (Manchester) encoding at the downlink, to simplify the clock and data recovery circuit and increasing signal integrity; increased frequency both at downlink (200 kHz) and at uplink (3.2 MHz); switched-capacitor DC/DC converter to improve power efficiency; body potential

driver to provide local grounding and limit current exchange with the body. Although it is difficult to compare the two generations in terms of results – as they have different requirements and specifications – post-layout simulation results of 4WiCS (simulated separately) show significant improvements in terms of power efficiency and system stability/reliability. The design of an active rectifier – instead of a passive one – and the addition of a switched-capacitor DC/DC converter have demonstrated an increased power conversion efficiency. However, such active switching elements have introduced internal noise sources into the system that now require additional filtering/components to achieve low-noise performance – crucial for the recording circuits.

System-level simulations demonstrate both the power and data circuits maintain their characteristics achieved during block-level simulation also when operating as part of the 4WiCS system. Together with the block-level simulations, this proves the 4WiCS interface has the capability to power up the CORE circuits (within the optrode) and communicate both internally with the CORE sub-system and externally with the chest implant. The CANDO4 SoC has been implemented and fabricated in TSMC 180 nm technology. Future measurement results from the testing of the System-on-Chip will be required to validate the simulation results.

Chapter 7

Conclusion

The nervous system and its central module, the brain, have been for decades the spotlight of research from different scientific fields. Biology, neurology, neuroscience, medical science, and more recently also engineering, have tried to unveil the secrets of this beautiful and elusive system. Despite remaining the most mysterious organ of the human body, the knowledge we currently have about the brain is in many cases enough to set the ground for the development of medical interventions that can impact the lives of millions of people. This has been proved by exceptional successes, such as cochlear implants and deep brain stimulators, leading to advancements both in neural technology development for discovery and in novel techniques for medical therapies.

In 2014, the CANDO project set the goal for developing one of the most complex implantable medical systems ever conceived. The solution for controlling abnormal network dynamics in the brain was proposed as a treatment of refractory focal epilepsy. Its innovation stands in the combination of three techniques that were never used together before: the revolutionary optogenetics technique for neuromodulation, a novel closed-loop algorithm for seizure detection/prediction, and a multi-module approach for the fully-implanted medical device.

The engineering team developing the multi-module implantable system had to come up with a solution to allow for the different modules within the system to receive the required power and to interact with each other. The inspiration for the inter-module connectivity came from

the best designer in the world: nature itself. In fact, the nervous system of the human body includes a central module – the brain – and satellite modules – the nerves connected to the organs. The brain connects to the peripheral nerves by using electrical signals flowing through the spinal cord – the physical communication channel.

The CANDO implantable system was thus envisaged to include a central module (located within an enclosed device implanted in the chest) and multiple satellite modules (located at the target sites in the brain where the treatment is performed). The former houses the processing unit that runs the algorithm, sending commands to the satellite modules and acquiring information from them. These are in direct contact with the target and are responsible for the front-end interactions - recording and stimulation. The central-to-satellite connection is established through a physical implantable lead. Therefore, the CANDO system is designed for the nervous system, inspired by the nervous system.

The work presented in this Ph.D. thesis has contributed to the creation and development of the in-body power distribution/transfer and data communication protocol between the multiple modules. This interfacing was developed in conformity with medical device standards, which have guided the definition of the technical requirements and specifications of the medical device for the treatment of drug-resistant epilepsy. For example, the power levels, the signal frequency ranges, the components materials, etc, have all been carefully selected – and periodically reviewed – by the CANDO team to comply with the relevant standards and directives. The first generation of the interfacing circuits has been employed to verify the functional characteristics within the medical implant and to evaluate its limitations in an emulated environment. The obtained results, together with considerations, have informed the development of a 2nd generation of the interfacing circuits, which have been implemented and fabricated.

7.1 Original Contribution

Throughout the duration of this doctorate programme, a number of original contributions have been achieved and can be detailed in relation to the research objectives.

Chapter 4:

- A custom protocol, the 4-Wire Communication System, was proposed and interfacing units were designed for both ends of the system – chest implant and brain implant. A power transfer technique is implemented in combination with the data communication to be employed specifically with a medical-grade implantable lead – the 4-wire cooper cable.
- The BI interface was designed, within the satellite modules, which includes: (1) power management and conversion circuits to recover the AC power carrier and provide the DC supply for the BI circuits; (2) digital circuits to allow full-duplex data communication and clock recovery.
- The CI interface was designed, within the central module, which includes: (1) a digital controller to generate the commands and data packets for communicating information; (2) an adaptive power delivery circuitry to generate the AC power carrier; (3) drivers and receivers to establish a bidirectional data communication.

Chapter 5:

- A demonstration platform was implemented for the emulation of the end-to-end CANDO system. This includes: (1) the above described CI interface and multiple BI interfaces; (2) the implantable lead with interfacing passive elements; (3) additional control circuitry, at the CI end, and the CANDO core circuits (recording and stimulation) at the BI end.
- System integration testing was performed, validating the functional operation of the 4WiCS interfaces and characterising its performance while ensuring the core functions are operational.
- Considerations on power management, interference, and system reliability were identified and discussed. These provide a key resource for addressing limitations and challenges that arise when integrating the 4WiCS interface within an implantable medical device.

Chapter 6:

- A CMOS-based system-on-chip has been designed and implemented as part of the 4th generation of the CANDO brain implant. This is designed such that it meets the requirements for use in clinical trials while having the flexibility to be employed as a research tool for laboratory experiments. It comprises circuits for performing the core functions and for interfacing externally by means of the 4WiCS interface.
- The 4WiCS interface sub-system is implemented as a stand-alone component (electrically isolated), despite being monolithically integrated within the SoC together with the CORE sub-system. Its design targets the limitations of the previous 4WiCS BI interface. The chip has been designed and fabricated in CMOS 180 nm technology.
- Simulation results of the block-level characteristics of the single 4WiCS components show improved efficiency and performance compared to the previous generation of the circuits. System-level simulations of the 4WiCS sub-system demonstrate functionality in typical operational conditions.

7.2 Future Work

The CANDO4 System-on-Chip has been fabricated and the wirebonded/package integrated circuits are now available for testing. In short term, obtaining measurement results from both the block-level circuits and the 4WiCS system is the next obvious step. This will allow verifying that the functional characteristics of the CANDO4 4WiCS sub-system meet the specifications set for the SoC and to validate its performance against the high-level user requirements. Moreover, the CANDO4 SoC is expected to be employed in the near future in non-human primates, thus the whole system characteristics must be tested first within an end-to-end platform – similarly to what is achieved in Chapter 5 – to ensure the system requirements are met before testing in large animal models.

Further improvements could be made to the 4WiCS circuitry. As mentioned in Chapter 6, the addition of switching elements within the power circuits, e.g. switched-capacitor DC/DC con-

verter, may significantly increase efficiency, but they add interference to the front-end recording. As the latter is measuring μV -level analogue signals, it is crucial the noise is minimised, thus switching elements within the same chip are not ideal. However, additional filtering and isolation stages of the switching elements could minimise their impact on the recording performance.

Although the implementation of the chest implant is not the focus of the CANDO project – this is intended to be outsourced to a design and manufacturing medical device company – to be used in clinical trials it will require in any case a 4WiCS CI interface to be included in it. At the moment, such interface is based on PCB technology, as shown in Chapter 4 and Chapter 5, thus too large to be integrated with other components in a typical chest implant. For this reason, further development should be pursued to optimise the 4WiCS CI interface and ideally design the required circuits as part of an ASIC chip instead of a PCB – as it is done for the 4WiCS BI interface. Moreover, as the CANDO4 CORE sub-system was designed to be compatible with the SPI protocol, the 4WiCS interface includes a 4WiCS-to-SPI bridge. This controller could be further extended to make the 4WiCS interface compatible not only with SPI, but also with other standards protocols, e.g. I2C, CAN, UART, etc.

As of today, the CANDO project is still active and the different teams are pursuing the development of the medical device. The final goal for CANDO is to achieve a first-in-man trial, using the implantable system for treating patients suffering from refractory epilepsy. After 5 years' experience within the CANDO project, I'm eager to see the microelectronics system we have developed being used as part of an active implantable medical device, providing benefit to epileptic patients and their families. In addition, I am confident that scientific discoveries will be made by using the CANDO4 SoC as a research tool for neuroscience. This could lead to more and more research groups starting to develop multi-module neural implants that require interfacing between multiple modules. In that scenario, the papers we have published on the 4WiCS interface, in addition to this report, will come helpful to microsystems and electronic designers of such devices. I strongly believe that the development of the 4WiCS interfacing system will be considered a pioneering work, which will inform the creation of future standards for in-body wireline communications.

7.3 Final Thoughts and Lessons Learned

During one of the first dinners of the whole CANDO team, following a full day of meetings, one of the principal investigators of the project told me:

“There are typically two ways to create impact in this field: you either improve a bit the lives of many people, or you improve a lot the lives of a few people. At CANDO, we are aiming to improve a lot the lives of many people.”

This mission has stuck with me throughout the 5 years I spent as one of the researchers of the CANDO project. During a Ph.D. programme, there are many up and down moments. I made sure not to forget about our mission both during ‘up’ moments, e.g. when my first paper was accepted for publication, and during ‘down’ moments, e.g. when smoke was coming out of my end-to-end PCB platform during a crucial experiment.

I have given a lot to the CANDO project in terms of time and effort. I have gained even more from the learning experience I had within the project, especially from the interactions with the CANDO members. A crucial lesson for me has been to appreciate the importance of the multi-disciplinary nature of such a complex project. CANDO has set a very ambitious target since the beginning, assembling a group of engineers, neuroscientists, and clinicians – who sometimes speak different “languages” – to develop an innovative medical device within an academic setting. Back in 2014 when the project was born, this vision may have sounded premature and pretentious. Nonetheless, since then, other academic groups and emerging companies have initiated projects with highly ambitious goals and similar complexity to CANDO.

In the past 5 years, I have worked and interacted with more the 25 people within the CANDO project, attending a total of over 30 full-day meetings – locked in the same room with the CANDO team for 6-7 hours straight. This experience has given me insights into how a large academic project works, teaching me much more than just microelectronics and neuroscience. For this reason, I have listed in the following my advice both for who wants to join and for who wants to lead a project like CANDO.

For all students and junior researchers who are about to start working in an inter-disciplinary, cross-site, ambitious project, my suggestions are:

- Get the most out of each team meeting and take notes;
- Be proactive and make your voice heard – if you strongly agree/disagree with something there is always a valid reason;
- Learn from fields which are not your core expertise, but that are important for the project;
- Enjoy the unnecessarily-long full-day meetings – strangely enough, you will miss them;
- Set your own intermediate goals and action points;
- Make sure you record the results of designs/tests/experiments that have failed and why they did – you don't want to make the same mistakes twice;
- Always keep in mind the big picture – it will help with the 'down' moments;
- Ask for help and advice from senior people – they were in your shoes not long ago;
- If you are part of the project, at any level, you are worth as much as everyone else;
- Be patient, hard-working, and respectful – you will be the one leading in the future.

For the principal investigators interested in starting/leading an inter-disciplinary, cross-site, ambitious project in academia, my suggestions are:

- Set initially flexible milestones, which are updated on a yearly basis;
- Define intermediate deliverables with realistic requirements and specifications;
- Create an environment that encourages communication/interaction between all members of the project;
- Listen to the ideas proposed by junior researcher and student, as it is likely they are the most creative minds in the room;
- Define clear action points on a regular basis and check they are met;
- Identify in advance expected outcomes for each team meeting;
- Share important responsibilities with your senior team members;
- If you want people to work hard, be the one to set the example;
- Be kind, optimistic, and confident – people within the project are inspired by you.

To my initial surprise, this PhD journey has required me to use and refresh most of the knowledge and skill set developed during my undergraduate and postgraduate studies: from FPGA design to digital modulation, from programming to PCB design, from microelectronics to cable characterisation. Many times I had to dust off my precious notes from the university years to revive what I thought were already buried memories. In addition, I was fortunate enough to acquire new technical skills and learn how to write papers and reports. But that's not it.

You may hear most of PhD graduates say that if they were to start their projects again, they would use a different method, would plan their work in a more structured way, and would focus on a few selected tasks and deliverables. The same is valid for me. This is, in my opinion, the most important lesson one can learn from a doctorate experience: how to develop a *critical methodology* and a *research approach*.

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Appendix A

List of publications

This appendix lists the papers that have been published by the author of this thesis. The publications derived directly for the research presented and described in this report are grouped in themes and listed in the following.

First generation of the CANDO brain implant microelectronics: CANDO1 ASIC

- R. Ramezani, Y. Liu, F. Dehkhoda, A. Soltan, **D. Hacı**, H. Zhao, ... & P. Degenaar, "*On-Probe Neural Interface ASIC for Combined Electrical Recording and Optogenetic Stimulation*," in IEEE Transactions on Biomedical Circuits and Systems, vol. 12, no. 3, pp. 576-588, June 2018, doi: 10.1109/TBCAS.2018.2818818.

First generation of the 4WiCS brain implant interface: 4WiCS ASIC

- S. S. Ghoreishizadeh, **D. Hacı**, Y. Liu, N. Donaldson and T. G. Constandinou, "*Four-Wire Interface ASIC for a Multi-Implant Link*," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 64, no. 12, pp. 3056-3067, Dec. 2017, doi: 10.1109/TCSI.2017.2731659.
- S. S. Ghoreishizadeh, **D. Hacı**, Y. Liu and T. G. Constandinou, "*A 4-wire interface SoC for shared multi-implant power transfer and full-duplex communication*," 2017 IEEE 8th Latin American Symposium on Circuits Systems (LASCAS), 2017, pp. 1-4, doi: 10.1109/LASCAS.2017.7948050.

PCB-based chest implant module and end-to-end platform

- **D. Hacı**, A. Mifsud, Y. Liu, S. S. Ghoreishizadeh and T. G. Constandinou, "*In-body wireline interfacing platform for multi-module implantable microsystems*," 2019 IEEE Biomedical Circuits and Systems Conference (BioCAS), 2019, pp. 1-4, doi: 10.1109/BIOCAS.2019.8918756.
- A. Mifsud, **D. Hacı**, S. S. Ghoreishizadeh, Y. Liu and T. G. Constandinou, "*Adaptive power regulation and data delivery for multi-module implants*," 2017 IEEE Biomedical Circuits and Systems Conference (BioCAS), 2017, pp. 1-4, doi: 10.1109/BIOCAS.2017.8325208.

Key design consideration and challenges for multi-module neural implants

- **D. Hacı**, Y. Liu, S. S. Ghoreishizadeh and T. G. Constandinou, "*Key Considerations for Power Management in Active Implantable Medical Devices*," 2020 IEEE 11th Latin American Symposium on Circuits Systems (LASCAS), 2020, pp. 1-4, doi: 10.1109/LASCAS45839.2020.9069004.
- **D. Hacı**, Y. Liu, S. S. Ghoreishizadeh and T. G. Constandinou, "*Design Considerations for Ground Referencing in Multi - Module Neural Implants*," 2018 IEEE Biomedical Circuits and Systems Conference (BioCAS), 2018, pp. 1-4, doi: 10.1109/BIOCAS.2018.8584708.

During the doctorate programme, the author has in addition published the following papers:

- **D. Hacı**, Y. Liu, K. Nikolic, D. Demarchi, T. G. Constandinou and P. Georgiou, "Thermally Controlled Lab-on-PCB for Biomedical Applications," 2018 IEEE Biomedical Circuits and Systems Conference (BioCAS), 2018, pp. 1-4, doi: 10.1109/BIOCAS.2018.8584664.
- **D. Hacı**, Y. Liu and T. G. Constandinou, "*32-Channel ultra-low-noise arbitrary signal generation platform for biopotential emulation*," 2017 IEEE International Symposium on Circuits and Systems (ISCAS), 2017, pp. 1-4, doi: 10.1109/ISCAS.2017.8050427.
- M. Cacho-Soblechero, S. Karolcik, **D. Hacı**, C. Cicatiello, C. Maxoutis and P. Georgiou, "*Live Demonstration: A Portable ISFET Platform for PoC Diagnosis Powered by Solar Energy*," 2019 IEEE Biomedical Circuits and Systems Conference (BioCAS), 2019, pp. 1-1, doi: 10.1109/BIOCAS.2019.8919227.

Appendix B

End-to-End Platform Startup Sequence

- At first, the central module (4WiCS CI interface) is powered up and the voltage levels are inspected before generating the 100 kHz power delivery carrier. On-boards LEDs are turned on when the power-up sequence starts. These display green light when the voltage levels are in the expected ranges and red light when they exceed them or if the system is in an unexpected state.
- After all LED lights are green, the power/downlink carrier is therefore activated from the GUI. Initially, there is no meaningful information encoded in the downlink signal (all zeroes), to ensure first the current through the Cooper cable and the voltage levels at the satellite end are within the correct range. This is achieved and measured via the current sensing feedback, allowing for fixed voltage levels at the brain implant. A 7-segment mini-LCD screen is located on the PCB board at the CI end to display in real-time the power carrier peak voltage. The latter is also displayed on the GUI, together with the value of the current flowing through the cable – measured by the current sensing feedback circuits.
- At the BI end, the power carrier is converted by the rectifier circuit on each 4WiCS ASIC and two DC voltages are generated, 5V (unregulated) and 3.3V regulated. These are measured both to ensure successful CI-to-BI power transfer and to verify the power conversion circuits are functioning.

- Correct clock and data recovery must be verified by ensuring the downlink data signal (after decoding) is always logic "low" (no information encoded – all zeroes). The downlink clock signal at the output of the CDR and the uplink clock signal generated by the PLL must respectively 100 kHz and 1.6 MHz.
- Following the verification of all power supply levels within the system and the downlink signals inspection, the downlink communication is enabled and commands are sent from CI to BI. These commands are generated from a script on the PC running the GUI and sent to the central module through UART. The commands are encoded within a 32-bit data packet, which includes also error-detecting code – cyclic redundancy check (CRC) – a 2-bit packet-start code, and the address of the targeted satellite module.
- Since the topology used for communication is based on a star-bus multipoint network, all nodes (satellite modules) receive the signal sent by the hub (central module). For the targeted module to decode and acknowledge the data packet, a unique ID code is assigned to each module. When the ID is recognised by the FPGA logic at one of the satellite modules, the 4WiCS-to-SPI conversion is activated and the SPI SCK (serial clock) and SPI MOSI (master output slave input) signals are sent to the CANDO3 ASIC. The latter is thus able to receive the data packet, acknowledge the command, and promptly respond via the SPI link.
- The response from the CANDO3 chip and activation of the SPI MISO (master input slave output) signal with the acknowledgment packet demonstrate: (1) correct downlink data decoding and clock recovery (100 kHz) by the CDR circuit on each 4WiCS ASIC; (2) correct 4WiCS-to-SPI conversion by the programmable logic bridge; and (3) correct generation of the uplink clock frequency (1.6 MHz) by the PLL. The response sent through the uplink path is finally received at the CI end and the uplink data packet displayed on the PC GUI.