

Class-E Half-Wave Zero dv/dt Rectifiers for Inductive Power Transfer

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Abstract—This paper analyses and compares candidate zero dv/dt half-wave Class-E rectifier topologies for integration into multi-MHz inductive power transfer (IPT) systems. Furthermore, a hybrid Class-E topology comprising advantageous properties from all existing Class-E half-wave zero dv/dt rectifiers is analysed for the first time. From the analysis, it is shown that the hybrid Class-E rectifier provides an extra degree of design freedom which enables optimal IPT operation over a wider range of operating conditions. Furthermore, it is shown that by designing both the hybrid and the current driven rectifiers to operate below resonance provides a low deviation input reactance and inherent output voltage regulation with duty cycle allowing efficient IPT operation over wider dc load range than would otherwise be achieved. A set of case studies demonstrated the following performances: 1) For a constant dc load resistance, a receiving end efficiency of 95 % was achieved when utilising the hybrid rectifier, with a tolerance in required input resistance of 2.4 % over the tested output power range (50 to 200 W). 2) For a variable dc load in the range of 100 % to 10 %, the hybrid and current driven rectifiers presented an input reactance deviation less than 2 % of the impedance of the magnetising inductance of the inductive link respectively and receiving end efficiencies greater than 90 %. 3) For a constant current in the receiving coil, both the hybrid and the current driven rectifier achieve inherent output voltage regulation in the order of 3 % and 8 % of the nominal value respectively, for a variable dc load range from 100 % to 10 %.

I. INTRODUCTION

WEAKLY coupled inductive links, Fig. 1, tend to operate in the low MHz region in order to increase their link efficiency (η_{link}), [1]–[3]. The optimal link efficiency ($\eta_{link,opt}$) of a particular inductive link geometry occurs when the receiving coil (L_{rx}) is tuned at the frequency of the generated magnetic field and the ratio of the ac load resistance (R_{ac}) to the reactance of the tuning capacitor (C_{rx}) satisfies a specific value (α_{opt}) [1]. The α_{opt} value depends upon the coupling factor (k) between the transmitting coil (L_{tx}) and L_{rx} , the unloaded quality factors of the two coils and the tuning method of L_{rx} , parallel (Fig. 1a) or series (Fig. 1b) [1]. When a rectifier is added to an inductive link, its input resistance will be the ac load and must therefore be evaluated according to maximum link efficiency requirements. Furthermore, the rectifier topology should be efficient at the frequency of operation, be compatible with the output type of the tuned receiving coil, voltage output for parallel tuned

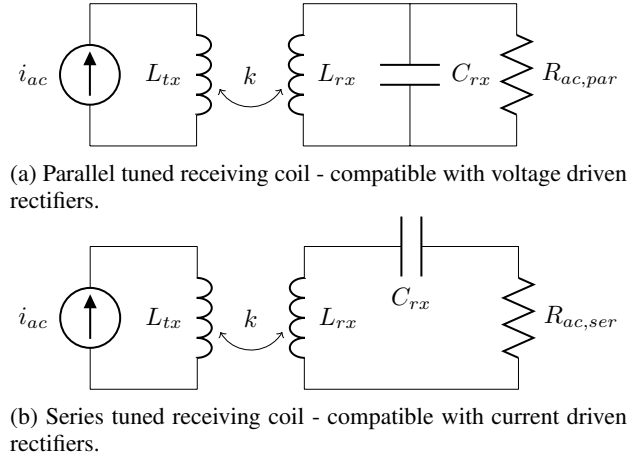


Fig. 1: Inductive link circuit configurations.

receiving coil (Fig. 1a) or current output for series tuned coil (Fig. 1b), and its input reactance should be absorbed by C_{rx} such that the tuning of L_{rx} will be unaffected.

Class-E rectifiers, [4], [5], are very popular in multi-MHz resonant converters [6]–[13] due to their efficient soft switching capability and low electromagnetic footprint. Due to their success in resonant converters, the utilisation of Class-E rectifiers is gaining popularity in weakly coupled multi-MHz IPT systems [14]–[16]. This section provides a general description of the operation of Class-E rectifiers. It then examines and presents the various developments of the topologies presented in literature. Fig. 2 summarises the circuit configurations of the reviewed Class-E rectifiers. Fig. 3 classifies the reported Class-E designs according to their operating frequency and maximum output power and Table I provides further details about the operation, performance and targeted application of the topologies of Fig. 3.

Class-E zero dv/dt rectifiers use a capacitor (C), or a capacitive network of total capacitance C in the case of the hybrid topology (Fig. 2a), to achieve zero rate of change of the voltage across the diode when it is reverse biased. An inductor (L) is used for the circulation of the dc load current when the diode is forward biased. A filter capacitor (C_f) is used to stabilise the output voltage. The operation of Class-E zero dv/dt rectifiers can be classified in three modes based on a variable A_r , defined as the ratio of the resonance frequency of the LC network (ω_r) to the operating frequency (ω). The first mode is at the point where ω_r equals to ω , A_r is equal to unity, and the rectifier is therefore operating at

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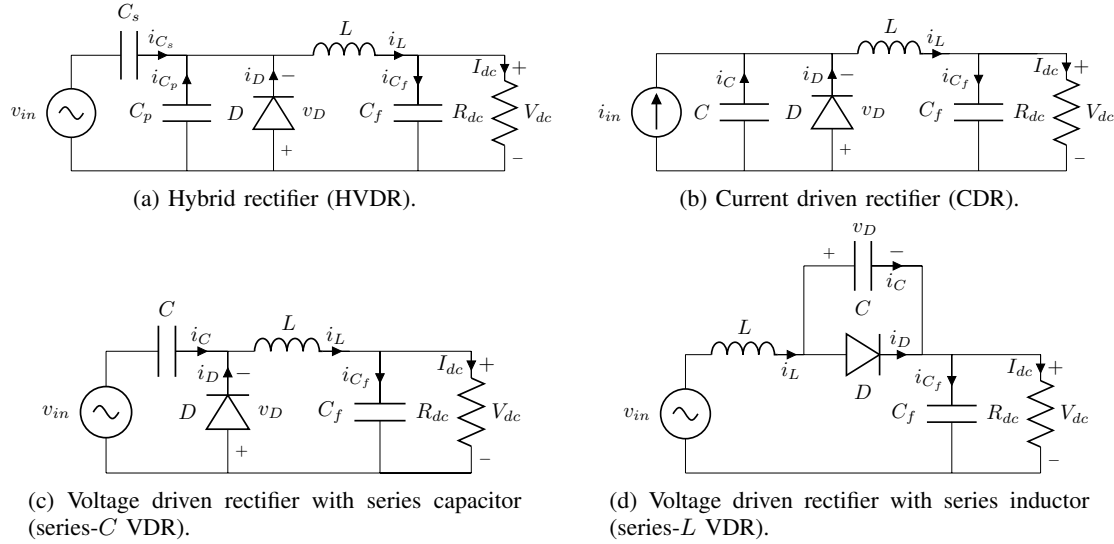


Fig. 2: Hybrid and Conventional Class-E half-wave zero dv/dt rectifiers.

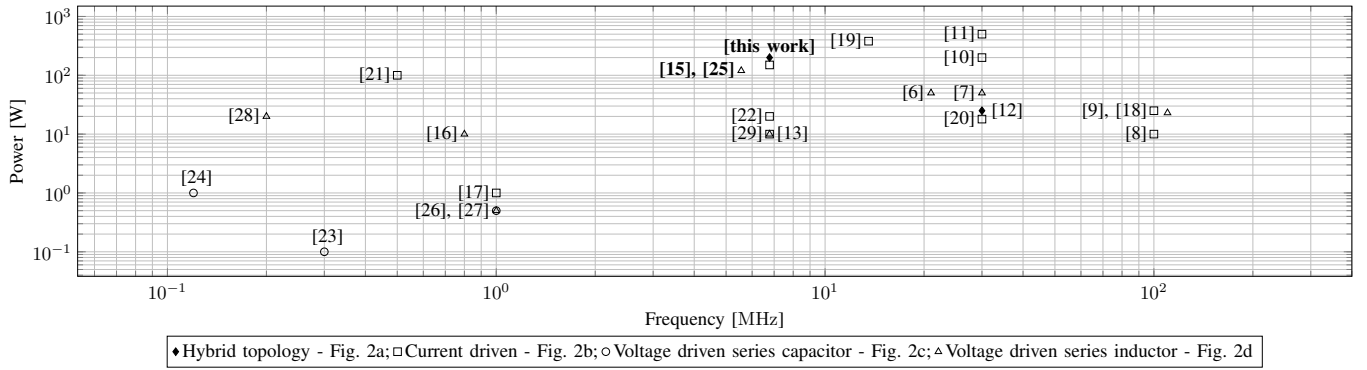


Fig. 3: Power vs frequency map for reported half-wave Class-E rectifiers.

TABLE I: Further characteristics of reported Class-E rectifiers in literature.

Rectifier	Ref.	Full Load	Diode Technology	Application	η [%]	Comments on Developed Rectifiers
Fig. 2a	[this work]	77 V; 2.6 A	SiC Schottky	IPT ¹	95**	Most efficient design from the case studies. Rectifier developed to provide optimal loading to the IPT of [2].
Fig. 2a	[12]	28 V; 0.89 A	Schottky	RPC ²	82.5*	Rectifier developed in a SEPIC converter as the dual circuit of Fig. 2d.
Fig. 2b	[8]	12 V; 0.83 A	Si Schottky	RPC	75*	Designed to present a resistive input impedance by using a finite impedance inductor.
Fig. 2b	[9]	12 V; 2 A	Si Schottky	RPC	75*	Two circuits with resistive input impedances, as in [8], added in a resistance compression configuration.
Fig. 2b	[11]	65 V; 7.69 A	SiC Schottky	RPC	81.6*	Resistive input impedance design in a push-pull configuration.
Fig. 2b	[10]	33 V; 6 A	SiC Schottky	RPC	82.5*	Same design as in [8] but L was replaced with an auto-transformer.
Fig. 2b	[13]	5 V; 2 A	Silicon Schottky	RPC	N/A	Analysis assuming a finite impedance inductor (L) and development to present a resistive input impedance.
Fig. 2b	[17]	5 V; 0.2 A;	Si Schottky	RPC	N/A	Analysis of the topology at any duty cycle assuming an infinite impedance inductor (L).
Fig. 2b	[19]	28 V; 13.57 A;	SiC Schottky	RPC	74*	Same concept as in [10] with increased output power capability.
Fig. 2b	[20]	12 V; 1.5 A	Si Schottky	RPC	N/A	Topology developed to present low deviation in input phase as the dc load varies between 100% to 10%.
Fig. 2b	[21]	100 V; 1 A	Ultrafast Recovery	IPT	90*	Topology developed for a contactless IPT system based on numerical analysis.
Fig. 2b	[22]	24.5 V; 0.82 A	Silicon Schottky	IPT	84*	Analysis based on [17] but including component losses. Case study based on a short-range IPT system.
Fig. 2b	[25]	60 V; 2.5 A	SiC Schottky	IPT	90**	Design of the topology with an infinite impedance inductor (L), for presenting optimal loading to the IPT of [2].
Fig. 2c	[27]	5 V; 0.1 A	Si Schottky	RPC	91**	Analysis at any duty cycle of operation with the LC network resonating at the frequency of operation.
Fig. 2c	[23]	2.6 V; 0.05 A	N/A	RPC	N/A	First implementation of the circuit with an infinite impedance inductor (L).
Fig. 2c	[24]	5 V; 0.2 A	Fast Recovery	RPC	N/A	Analysis at any duty cycle of operation with an infinite impedance inductor (L).
Fig. 2d	[6]	5 V; 10 A	N/A	RPC	87*	First developed zero dv/dt Class-E rectifier. Developed from an isolated voltage driven Class-D rectifier.
Fig. 2d	[7]	24 V; 2.08 A	Si Schottky	RPC	81.6*	Integration of the topology in an isolated converter.
Fig. 2d	[15]	140 V; 0.85 A	SiC Schottky	IPT	90**	Design for operation below resonance to minimise the inductor size required by optimal IPT efficiency.
Fig. 2d	[16]	27 V; 0.36 A	Si Schottky	IPT	94**	State space analysis of the topology and integration in a short-range IPT system.
Fig. 2d	[26]	5 V; 0.1 A	Si Schottky	RPC	88.67**	Topology was analysed at any duty cycle for operation at the resonant frequency of the LC network.
Fig. 2d	[18]	33 V; 0.7 A	Si Schottky	RPC	87**	Topology developed for a VHF boost converter. Maximum reported frequency of operation.
Fig. 2d	[28]	11.57 V; 1.16 A	MOSFET IRF540	IPT	80*	Synchronous rectification. Absorption of L in the receiving coil of a short range IPT system.
Fig. 2d	[29]	18 V; 0.56 A	Si Schottky	IPT	92**	Absorption of L in the receiving coil of a contactless IPT system.

¹Inductive Power Transfer, ²Resonant Power Converters; *System Efficiency, **Rectifier Efficiency

resonance. In the other two modes the rectifier is operating away from resonance and A_r is either smaller than unity, for operation above resonance, or greater than unity, for operation below resonance. The functionality of L varies between the different Class-E topologies. In the hybrid topology of Fig. 2a (HVDR), the current driven topology of Fig. 2b (CDR) and the voltage driven topology with series capacitor of Fig. 2c (series- C VDR), L functions as a filter inductor and has a large harmonic distortion in the current through it (i_L). When the diode is forward biased, one end of the inductor is clamped to ground causing a constant rate of discharge of C_f through L . When the diode is reverse biased, i_L has a sinusoidal component superimposed to the output dc current. The magnitude of the ac component of i_L increases with A_r . When A_r approaches zero in operation above resonance, the current through L can be assumed to be dc. In the voltage driven rectifier with a series inductor of Fig. 2d (series- L VDR), the presence of L decreases the harmonic content of the current drawn from the voltage source and hence the ac component of the current through L can be assumed sinusoidal in all operating modes. The sinusoidal current component is superimposed to the output dc current.

The HVDR (Fig. 2a) was introduced in the case study of [23] where it was compared with the series- C VDR (Fig. 2c). Furthermore, the HVDR was empirically designed for operation at resonance and implemented in a SEPIC converter in [12]. Although not discussed in the aforementioned references, the HVDR is an improved design of the series- C VDR. Unlike the other rectifier topologies, the series- C VDR does not absorb the pn junction capacitance of the diode (C_{pn}) in its LC network. The non-constant behavior of C_{pn} with voltage makes the operation of the series- C VDR non-robust when C is in the same order of magnitude as C_{pn} . In the HVDR, C is split into C_s and C_p . Since an external capacitor is now put across the diode, C_{pn} can be physically absorbed by C_p . In this work, the HVDR is analysed for the first time in all Class-E rectifier operating modes, at all duty cycles, for any ratio of C_p to C_s .

In resonant power converter applications, the most widely used Class-E rectifier is the CDR (Fig. 2b). The topology was introduced in [17], where it was analysed at all duty cycles with an inductor (L) assumed to be of infinite impedance (A_r is zero). In [8]–[11], [13] and [20] more properties of the topology were exploited by utilising an inductor (L) of finite impedance. For a specific duty cycle and A_r , the topology can exhibit a resistive input impedance at the frequency operation, [8]–[11] and [13], as otherwise appears resistive and either capacitive [17] or inductive [20]. Over a dc load range between 100% to 10%, and hence a varying duty cycle, the CDR can have a low input phase deviation by selecting the appropriate A_r , [20]. The series- L VDR (Fig. 2d) was introduced in [6], where it was developed from an isolated voltage driven Class-D half-wave rectifier. The analysis of this topology at all duty cycles was reported in [26] for operation at resonance and in [30] for an ω varying around resonance. In [23] the first implementation of the series- C VDR (Fig. 2c) is reported. Its analysis at all duty cycles is reported in [24] with an L of infinite impedance and in [27] for operation at resonance.

Both the CDR (Fig. 2b) and the series- L VDR (Fig. 2d) were developed for IPT applications [15], [16], [21], [22], [25], [28] and [29]. Our work in [15] reports the first Class-E rectifier integrated in a mid-range multi-MHz IPT system. The circuit used was the series- L VDR. In [15] the implementation challenges of L , due to the large required inductance value at high frequency, were highlighted when the circuit is designed to emulate optimal link efficiency conditions for the inductive link in [2]. L is easier to fabricate when designing the topology at an A_r smaller than unity since, the required inductance decreases. Another improvement was introduced in the short range IPT system of [28] for sub-MHz operation, and in the contactless IPT of [29] for multi-MHz operation, by including L in the tuned receiving coil. While this method solves the implementation problem, the receiving coil is never exactly at resonance. Therefore, the link efficiency drops significantly when the coils operate at mid-range distances due to increased losses in the transmitting coil caused by the reduced reflected resistance as a result of the uncompensated reactance of the receiving coil.

The implementation of L in the other rectifiers of Fig. 2 does not impose such a great challenge as in the series- L VDR (Fig. 2d). Our work in [25] presented the design and implementation of the CDR (Fig. 2b) for the inductive link in [2] as an improvement on [15]. However, since the CDR is a current driven topology it will experience higher conduction losses than the voltage driven rectifiers when designed to present optimal loading for the same set of coils [1]. The CDR achieved the same efficiency as the series- L VDR but is more robust to the diode parasitic capacitance [15], [25]. Our study in [31] showed potential for improvement in the performance of the receiving end when the HVDR (Fig. 2a) is utilised instead of the conventional Class-E rectifiers of Fig. 2.

As can be seen, much work has been reported in the Class-E rectifiers in a range of applications which has highlighted some advantages, and disadvantages, of the topologies. However, there exists no formal analysis for structured comparison of these topologies over a range of operating scenarios. This paper provides a design framework for Class-E half-wave zero dv/dt rectifier topologies which allows the designer to select the optimal topology based on power levels, frequency of operation and inductive link properties. It will also be shown that rectifiers can be designed to present a low input reactance deviation and inherent output voltage regulation over a range of output load values. While the discussions focus on IPT applications, the rectifier analysis results are applicable for other applications. Section II, discusses the design of Class-E rectifiers that provides optimal link efficiency conditions and Section III, presents the behavior of rectifier design variables under several operating conditions. Section IV then discusses the case studies that took place after the analysis results of Section III and finally, Section V presents the conclusions.

II. DESIGN FOR INTEGRATION IN IPT SYSTEMS

For a successful Class-E rectifier integration in an IPT system, the input resistance of the topology must be set to an optimal value based on the configuration of the inductive

link. It is mathematically convenient to represent the input impedance of the voltage driven Class-E rectifiers as the parallel connection of a reactive component, $X_{in,p}$, and the input resistance, $R_{in,p}$. On the other hand, in the current driven topology it is more convenient to present the input impedance by a series combination between $X_{in,s}$ and $R_{in,s}$ [32].

When Class-E rectifiers are designed to provide optimal link efficiency conditions, designers can select the duty cycle, d_r , at full load and variable A_r :

$$A_r = \frac{\omega_r}{\omega}. \quad (1)$$

In the case of the HVDR (Fig. 2a) another degree of freedom is introduced in the selection of variable B defined as:

$$B = \frac{C_p}{C_s}, \quad (2)$$

where the sum of the two capacitances is:

$$C = C_s + C_p. \quad (3)$$

The passive components in the circuit are then evaluated such that the specified conditions are met. The duty cycle depends on the loaded quality factor (Q_r) of the rectifier, defined as:

$$Q_r = \frac{R_{dc}}{X}, \quad (4)$$

where R_{dc} is the rectifier's dc load and X is the reactance of the series component in the voltage driven topologies (L or C) or in the current driven topology, X is the reactance of capacitor C . The relationship between the dc resistance with the input resistance in the voltage driven rectifiers (assuming 100 % efficiency) is given by:

$$R_{dc} = 2M_V^2 R_{in,p} = 2M_V^2 R_{ac,par}, \quad (5)$$

where M_V is the ratio of output voltage to the peak of the ac input voltage (ac to dc voltage gain). In the current driven topology R_{dc} is given by:

$$R_{dc} = \frac{R_{in,s}}{2M_I^2} = \frac{R_{ac,ser}}{2M_I^2}, \quad (6)$$

where M_I is the ratio of output current to the peak of the ac input current (ac to dc current gain). In order to directly relate the input ac resistance to the required X value, (5) and (6) are substituted into (4) and the variables are rearranged such that an expression is formed relating the ratio of the ac resistance to the required X value. This ratio will be called input loaded quality factor, Q_{in} , and is given by the following expressions:

$$Q_{in} = \frac{Q_r}{2M_V^2} = \frac{R_{in,p}}{X}, \quad (7)$$

for the voltage driven topologies and

$$Q_{in} = 2M_I^2 Q_r = \frac{R_{in,s}}{X}, \quad (8)$$

for the current driven topology. Using the definition of variable A_r , the relationship between the reactances forming the LC network is given by:

$$A_r^2 = \frac{X_C}{X_L}. \quad (9)$$

In the case of the HVDR, C_s and C_p are evaluated from (2), (3) and (9). Finally, the ratio of input reactance to X is given by:

$$N_{in} = \frac{X_{in}}{X}. \quad (10)$$

The Class-E topologies of Fig. 2, were analysed for operation at any duty cycle, d_r , and an A_r range between 0 to 2, while the analysis of the hybrid Class-E rectifier, Fig. 2a, was also performed as a function of variable B . In the mathematical analysis of each rectifier, the diode and passive components were assumed ideal and lossless. The derivation of the design variables follows the same method as presented in [24], [32]–[34] which is summarised in Appendix A along with the equations of the design variables of the rectifiers of Fig. 2.

The choice of 50 % duty cycle at full load is considered to be optimum by the authors because it provides maximum power output capability ($c_{P_{dc}}$) in Class-E rectifiers and hence fully utilises the device [32]. From this starting point (100 % dc load), the duty cycle can only decrease as R_{dc} increases. Hence the analysis of this paper has not been applied to duty cycles greater than 50 %.

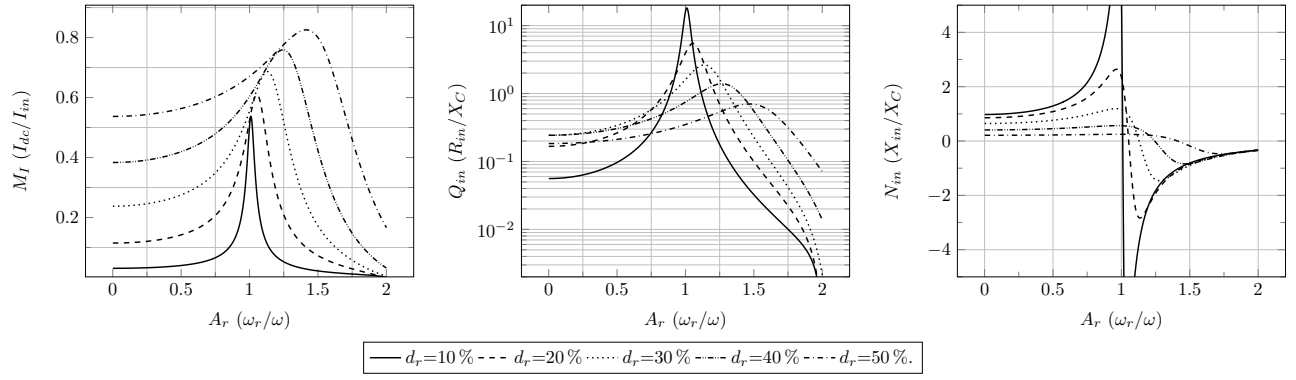
III. DISCUSSION OF RECTIFIER FEATURES

The design variables in (4) - (8) and (10), for the conventional Class-E topologies are presented in Fig. 4 as functions of A_r for duty cycle values from 50 % to 10 %, in steps of 10 %. In Fig. 5 the design variables are illustrated as functions of A_r for several values of B at 50 % duty cycle for the HVDR. The loaded quality factor (Q_r) is independent of variable B and is therefore the same for the HVDR (Fig. 2a) and the series- C VDR (Fig. 2c). Also, Q_r in the CDR (Fig. 2b) is the same as in HVDR and the series- C VDR since CDR forms the Norton equivalent circuit of the series- C VDR. Fig. 6 presents the diode stresses in half-wave Class-E rectifiers, and so along with Figs. 4 & 5, maps out the entire state space of rectifier designs and can be utilised to discuss in detail the performance and trade-offs of different rectifier designs operating across a range of conditions.

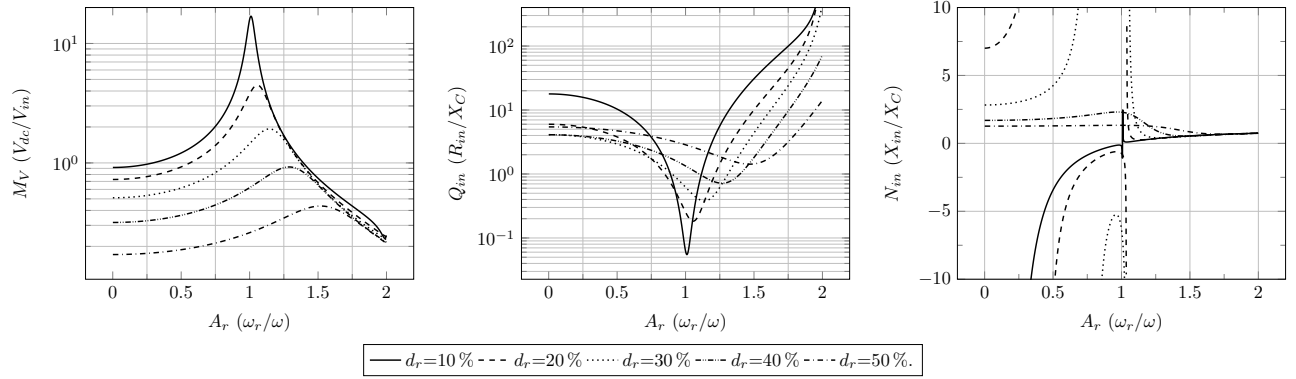
Positive and negative features of the candidate rectifier topologies when operating at duty cycles from 50 % and below will now be discussed using Figs. 4, 5 & 6. These discussions are based on the configuration of the inductive link of [2], the parameters of which are summarised in Table II (the optimal condition parameters were calculated using [1]).

A. Current Driven Class-E Rectifier (CDR)

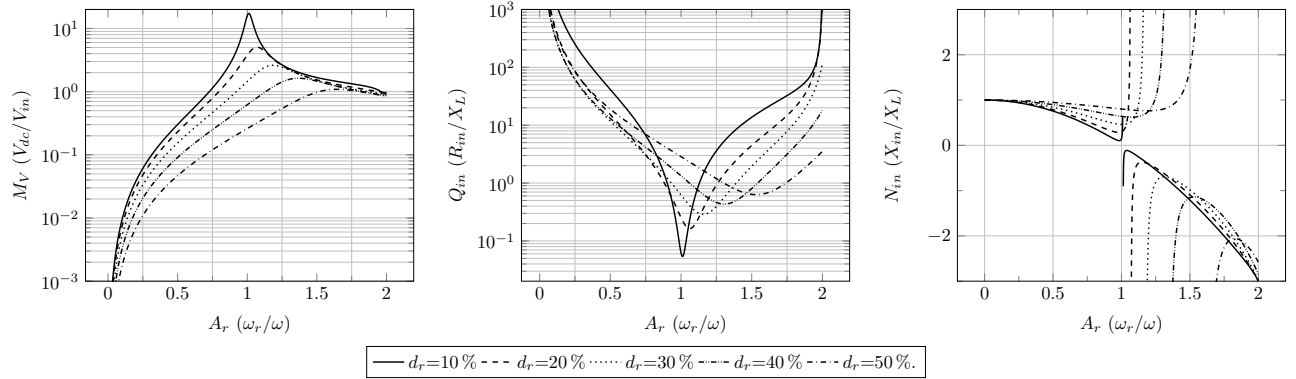
As shown in Table I, the CDR (Fig. 2b) is the most commonly implemented topology of the conventional half-wave Class-E rectifiers presented in the literature. It has previously been designed for values of A_r in the range of 0 to 1.42, [8]–[11], [13], [17]. However, a crucial property of the topology has been missed because as can be seen for N_{in} in Fig. 4a, an A_r between 1.75 to 2 has the additional advantage of compressing the input reactance of the topology, $X_{in,s}$, as the duty cycle decreases below 50 % (as a result of increasing R_{dc}). The maximum deviation in $X_{in,s}$ is 13 % from its initial



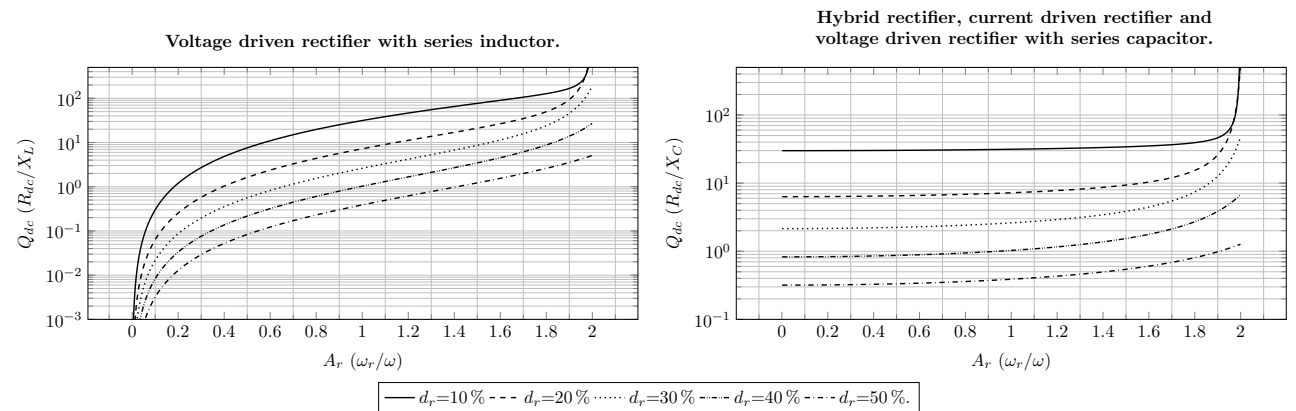
(a) Current driven rectifier (Fig. 2b).



(b) Voltage driven rectifier with series capacitor (Fig. 2c).



(c) Voltage driven rectifier with series inductor (Fig. 2d).



(d) Loaded quality factors of rectifiers of Fig. 2.

Fig. 4: Design variables of Class-E half-wave zero dv/dt rectifiers.

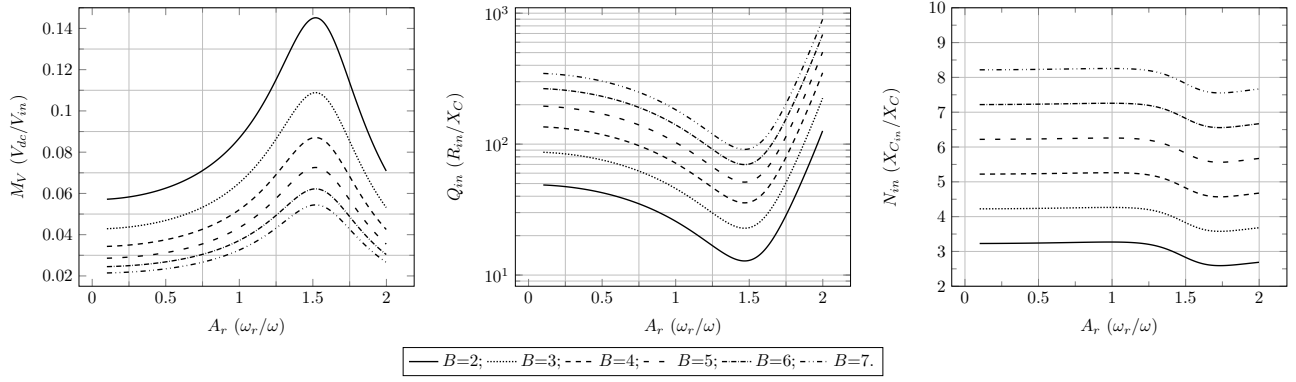


Fig. 5: Design variables of hybrid Class-E rectifier (Fig. 2a) for 50 % duty cycle.

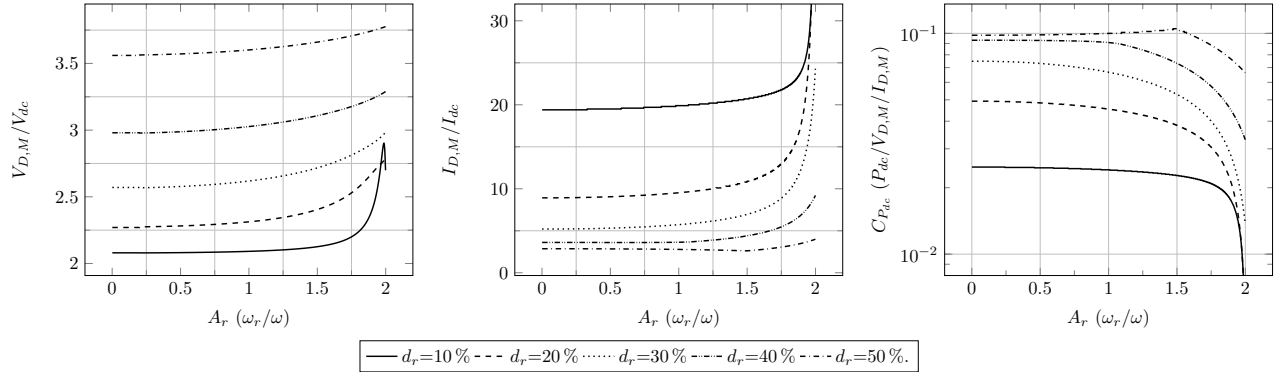


Fig. 6: Diode stresses for all examined Class-E half-wave topologies.

TABLE II: Characteristics of the inductive link in [2].

Parameter	Value	Optimal conditions	Value
f [MHz]	6.78	$\alpha_{opt,ser} \left(\frac{R_{ac,ser}}{X_{rx}} \right)$	0.044
k^* [%]	3.5	$\alpha_{opt,par} \left(\frac{R_{ac,par}}{X_{rx}} \right)$	22.77
L_{tx} [μ H]	4	$\eta_{link,opt}$ [%]	95
L_{rx} [μ H]	5.67	$R_{ac,ser}$ [Ω]	10.6
X_{tx} [$j\Omega$]	170.4	$R_{ac,par}$ [Ω]	5500
X_{rx} [$j\Omega$]	241.54	R_{ref} [Ω]	6
Q_{tx}	1300		
Q_{rx}	1000		

* At a center to center coil separation equal to one diameter of the transmitting coil.

value at an A_r equal to 1.75 when the duty cycle changes from 50 % to 43 %. When the duty cycle decreases below 43 % the deviation of input reactance reduces and approaches the input reactance value for 50 % duty cycle. As A_r increases above 1.75 the maximum deviation in $X_{in,s}$ decreases. The effect of the $X_{in,s}$ deviation on the receiving resonant tank depends on the absolute value of the input reactance, which depends on X_C and thus from (8), on Q_{in} and the required emulated input resistance ($R_{ac,ser}$ for the CDR). By evaluating $X_{in,s}$ using $\alpha_{opt,ser}$ from Table II and Q_{in} and N_{in} from Fig. 4a, it can be seen that a deviation in $X_{in,s}$ by 13 % will result in a residual reactance at the receiving end smaller than 1 % of the reactance of L_{rx} . Therefore, when the CDR is designed for

values of A_r in the range of 1.75 to 2, its effect on the tuning of the receiving coil will be negligible when R_{dc} increases.

In the same A_r range (1.75 to 2) unlike $X_{in,s}$ the input resistance ($R_{in,s}$) of the topology will change significantly with duty cycle. From the definition of Q_{in} and by considering the behavior of duty cycle with R_{dc} , the input resistance of the topology decreases as R_{dc} increases. In fact in the aforementioned A_r range, the input resistance of the circuit will be halved when R_{dc} is doubled. This behavior of $R_{in,s}$ provides an inherent output voltage regulation assuming a constant input current. The inherent output voltage regulation can be observed by multiplying M_I and Q_r . From the definitions of the two variables, their product gives a direct relationship between the input current and the output voltage: $V_{dc}/(X_C \cdot i_{in})$. By evaluating the product of the curves in Fig. 4a (left) with the curves in Fig. 4d (right), it can be observed that there is an insignificant deviation from the initial value of this product as the duty cycle decreases below 50 %. When A_r is 1.75, for an output dc load variation from 100 % to 10 % the factor $V_{dc}/(X_C \cdot i_{in})$ deviates by less than 10 % of its initial value. In fact the inherent voltage regulation actually occurs over a range of A_r from 1.6 to 2.

In resonant operation (A_r is one), a monotonic behavior of the input resistance of the topology can be observed in Q_{in} of Fig. 4a. $R_{in,s}$ increases with R_{dc} . Inherent output voltage regulation can exist in resonant operation by keeping the induced emf in the receiving coil constant. However, the error in output voltage regulation is more difficult to find in this case

without considering the value of the external capacitor added for the tuning of the receiving coil. Also in this operating mode, the system is not as well regulated as in operation at an A_r between 1.6 and 2.

Finally, when the topology is designed at an A_r that tends to zero the resultant inductance value (L) is large. This can be deduced from Q_{in} of Fig. 4a and (9). A high inductance results in an inductor current (i_L) with a small ac component. This small ac component eases the implementation of the output filter capacitor (C_f).

B. Voltage Driven Class-E Rectifier with Series Inductor (series-L VDR)

The series-L VDR (Fig. 2d) will generally introduce implementation challenges because the required inductance L will need to be in the μH range for most practical inductive links. Using the data from Table II and the definition of Q_{in} in the series-L VDR (Fig. 4c), it can be shown that the ratio of L to L_{rx} will be greater than unity when A_r is greater than 0.5. Realising these values of inductance requires a magnetic core which will be prohibitively lossy at MHz frequencies [15] and therefore we will not consider this topology any further here.

C. Voltage Driven Class-E Rectifier with Series Capacitor (series-C VDR)

This topology (Fig. 2c) can be thought as the voltage driven equivalent of the CDR (Fig. 2b) and therefore, it exhibits the same input impedance behavior with A_r . As A_r tends to zero a large L results from the design variables which eases the implementation of C_f . In resonant operation, a monotonic behavior of the input resistance of the topology ($R_{in,p}$) can be observed in Q_{in} of Fig. 4b (centre). $R_{in,p}$ decreases as R_{dc} increases and hence, as observed in the CDR (Fig. 2b), the equivalent series resistance seen by L_{rx} increases with R_{dc} resulting in inherent output voltage regulation when the induced emf is constant.

From N_{in} in Fig. 4b, it can be shown that the property of low input reactance ($X_{in,p}$) deviation with increasing R_{dc} occurs over the same A_r range as the CDR (from 1.75 to 2). In this topology however, the deviation of $X_{in,p}$ is smaller than the deviation of $X_{in,s}$ in the CDR. When A_r is 1.75, the input reactance of series-C VDR deviates less than 5% from its initial value as the duty cycle decreases below 50% due to the increase of R_{dc} . Furthermore, the inherent output voltage regulation at the aforementioned A_r range can be observed in M_V of Fig. 4b. In the A_r range from 1.75 to 2, M_V changes insignificantly (less than 10%) from its initial value as R_{dc} increases up to ten times its initial value. Hence, by keeping constant the voltage across the input terminals of the rectifier the output voltage will be regulated. In an IPT scenario the input voltage of the rectifier is the voltage across the tuning capacitor and will be kept constant by keeping constant the current in the receiving coil (as in the CDR). $R_{in,p}$ is an order of magnitude greater than $X_{in,p}$ to satisfy the optimal link efficiency conditions [1], therefore the magnitude of the voltage at the input terminals of the rectifier is primarily dependent on $X_{in,p}$. As $X_{in,p}$ remains within 5% of its initial

value at this A_r range, at a constant $i_{L_{rx}}$ the voltage across the input terminals of the rectifier remains constant.

In contrast to the other rectifier topologies, the operation of the series-C VDR is highly dependent on the output power level because the non-constant diode junction capacitance (C_{pn}) is not absorbed into a large fixed capacitor. Therefore, the HVDR (Fig. 2a) can be seen as an improvement to the series-C VDR because C_{pn} can be absorbed into C_p . Hence, the HVDR is more robust to changes in output voltage than the series-C VDR and introduces an additional degree of design freedom in the selection of variable B , which allows the provision of optimal load for a desirable A_r [31].

D. Hybrid Class-E Rectifier (HVDR)

The behavior of M_V , Q_{in} and X_{in} variables over A_r and d_r in both the HVDR (Fig. 2a) and the series-C VDR (Fig. 2c) is the same and hence, these two topologies share the advantageous properties discussed in the previous section. However, an additional important property of the HVDR (Fig. 2a) can be observed by considering the ac to dc gain (M_V) in Fig. 5. In this topology M_V depends on two variables, A_r and B . The series-C VDR does not have this property because it does not split C into two components. By selecting the appropriate A_r and B combination, the topology can be used to match the optimal ac load of an inductive link to any given value of R_{dc} to be powered by the IPT system. Furthermore, different HVDR topologies can present the same ac load while having the same R_{dc} but with different values of the other passive components. It should be noted that for A_r greater than 1.7, the input capacitance of the HVDR can become greater than C_{rx} . From the N_{in} in Fig. 5 it can be seen that by decreasing the value of B the value of the input capacitance also decreases. This comes at the expense of increasing the value of M_V at the same time. Hence for an A_r greater than 1.7, the range of $R_{in,p}$ that can be matched to an R_{dc} is smaller than for any other A_r value.

E. Summary of Derived Properties

Two properties appear in all Class-E rectifiers of Fig. 2. For all the rectifiers of Fig. 2 the maximum possible power output capability can be achieved by designing the rectifier at 50% duty cycle at an A_r equal to 1.52 according to Fig. 6. Moreover from Fig. 4, for different A_r and d_r combinations every topology can appear with a resistive input impedance at the frequency of operation. A summary of the properties of the candidate rectifiers is presented in Table III.

Given the disadvantages of the series-C VDR and series-L VDR, it can be concluded that the HVDR (Fig. 2a) and CDR (Fig. 2b) topologies are the leading candidate solutions for the IPT system of [2] and these will now be explored using several case studies which include practical implementations.

IV. CASE STUDIES

A. Rectifier Designs

The properties discussed in the previous section form the basis of the case studies. Five different rectifiers were implemented with five different A_r values and have the following properties:

TABLE III: Summary of Class-E rectifier properties based on design variable plots.

Property	HVDR	CDR	series- <i>C</i> VDR	series- <i>L</i> VDR
Low current ripple in C_f	$A_r \leq 0.5$	$A_r \leq 0.5$	$A_r \leq 0.5$	×
Low loss inductor (L) realisation	✓	✓	✓	$A_r \leq 0.5$
Matching of R_{dc} for any A_r	✓	×	×	×
Resistive input impedance	$A_r \leq 1$	$A_r \geq 1$	$A_r \leq 1$	$A_r \geq 1$
Low deviation in X_{in}	$1.75 \leq A_r \leq 2$	$1.75 \leq A_r \leq 2$	$1.75 \leq A_r \leq 2$	A_r tends to 0
Inherent output voltage regulation	$A_r = 1$ & $1.6 \leq A_r \leq 2$	$A_r = 1$ & $1.6 \leq A_r \leq 2$	$A_r = 1$ & $1.6 \leq A_r \leq 2$	$A_r = 1$ & $1.6 \leq A_r \leq 2$
Power robust operation	✓	✓	×	A_r tends to 0

- **Design #1:** HVDR operating at an A_r smaller than one providing a low ac current ripple through the output filter capacitor.
- **Design #2:** HVDR operating at resonance ($A_r = 1$) and exhibiting a monotonic behavior in its input resistance with varying R_{dc} .
- **Design #3:** HVDR operating at the maximum power output capability ($C_{P_{dc}}$) point of Fig. 6 ($A_r = 1.52$).
- **Design #4:** HVDR operating at an A_r equal to 1.75, exhibiting a low deviation input reactance and a monotonic behavior in input resistance with varying R_{dc} .
- **Design #5:** CDR with the same input impedance properties as Design #4 ($A_r = 1.8$).

The design values of the components in each design are presented in Table IV along with the actual values used in the experiments. The design variables of (5) to (8) were evaluated using the equations in Appendix A.

The four HVDR designs were implemented with a different combination of A_r and B to investigate which combination of LC network components will deliver the best efficiency and the required input resistance for the same R_{dc} . All the HVDR designs had the same M_V , except Design #4, since as discussed in Section III-D, B had to be evaluated to yield an input capacitance smaller than the tuning capacitance of L_{rx} . A_r in the CDR (Design #5) was selected to also result in a circuit with R_{dc} equal to the value for the other rectifiers.

For each design, the inductor (L) was implemented first. Based on its measured value the other passive components were chosen such that the initial selection of A_r and B , or just A_r for the CDR, was satisfied. In Table IV, the experimental values of the capacitor in parallel with the diode, C_p for Designs #1 to #4 and C for Design #5, do not include the pn-junction capacitance of the diode (C_{pn}) and are hence the capacitance of the physical capacitors added to the circuit which is equal to the design value. All inductors were implemented with Micrometals iron powder cores for RF applications. Specifically, in Design #1 a T106-3 core was used and in Designs #2 to #5 T106-2 cores were used. All capacitors were from the AVX high Q range. Component impedance measurements were made with a Keysight Technologies impedance analyzer. All rectifiers utilised a single Wolfspeed SiC Schottky diode, the C3D10065A, which has 10 A forward current capability and 650 V blocking voltage capability.

B. Experimental Test Rig

To allow careful characterisation of rectifiers and to avoid the need of an inductive link and its associated instrumentation for testing the rectifier, a test rig was developed that reproduces IPT conditions in the tuned Rx coil when a rectifier is added at the receiver. With this test rig calculation of the efficiency of the receiver (η_{Rx}) and the input resistance of the rectifier under test as seen from the output of the inverter, is possible without affecting any other part of the IPT system. More information about the test rig and the calculation of the worst case error in the experimental measurements can be found in Appendix B. Further implementation details for the test rig can be found from our work in [35].

C. Experimental Results and Discussion

The five implemented rectifiers will now be compared with respect to their efficiency and their effect on the inductive link. To ensure repeatability of results, a power sweep was performed in each experiment and measurements were recorded twice, when the output power was increasing from minimum to maximum and when the output power was decreasing from maximum to minimum. The results presented are the average.

The test rig enables measurement of the combined impedance of the receiving coil, external tuning capacitor and the rectifier under test. At resonance, this impedance is equal to the equivalent series input resistance of the rectifier, $R_{in,ser}$. In the current driven case, $R_{in,ser}$ is equal to $R_{in,s}$ and in the voltage driven case $R_{in,ser}$ is equal to the series transformation of $R_{in,p}$. When the rectifier is designed to reflect the optimal load this $R_{in,ser}$ value is equal to $R_{ac,ser}$ independent of series or parallel tuning (which is equal to 10.6Ω in this case study).

Fig. 7a presents the measured η_{Rx} and $R_{in,ser}$ for varying power (50 W to 200 W). Fig. 7b, Fig. 7c and Fig. 7d show the results of the variable R_{dc} experiments for Designs #2, #4 and #5 over a dc load range between 10 % to 100 %. At every dc load step, the $R_{in,ser}$ of the topology and the residual reactance at the resonant tank ($X_{in,res}$) were calculated. $X_{in,res}$ is the uncompensated reactance between the reactances of the Rx coil, the external tuning capacitor and the input reactance of the rectifier. To examine the inherent voltage regulation feature, the ratio between the output dc voltage to the current in the receiving coil (V_{dc}/i_{in}) was calculated in Designs #4 and #5 and in Design #2 the ratio between

TABLE IV: Design variables and experimental evaluation of components of implemented Class-E rectifiers.

	Design #1 Hybrid Rectifier			Design #2 Hybrid Rectifier			Design #3 Hybrid Rectifier			Design #4 Hybrid Rectifier			Design #5 Current Driven Rectifier		
Property	DC current output			Operation at resonance			Max power output capability			Low deviation $X_{in,p}$			Low deviation $X_{in,s}$		
A_r	0.35			1			1.52			1.75			1.8		
B	2.5			4			7.5			4			N/A		
M_V/M_I	0.05			0.05			0.05			0.0683			0.3862		
Q_{in}	62.1			71.53			105.6			79.49			0.2403		
N_{in}	3.73			5.26			8.28			4.601			-0.4573		
	Theory	Exp.	Error [%]	Theory	Exp.	Error [%]	Theory	Exp.	Error [%]	Theory	Exp.	Error [%]	Theory	Exp.	Error [%]
R_{dc} [Ω]	29	30.58	-5.45	29	29.1	-0.34	29	29.51	-1.76	50	50.51	-1.02	33.5	30	10.45
L [μ H]	16	16.31	-1.94	1.8	1.82	-1.11	0.529	0.596	-12.67	0.53	0.5	5.66	0.302	0.278	7.95
C [pF]	265	261	1.51	305	303	0.66	451	400	11.31	339	360	-6.19	564	575	-1.95
C_s [pF]	76	74	0.72	61	61	0.00	53	47	11.32	68	72	-5.88	N/A	N/A	N/A
C_p [pF]	189	186	1.59	244	242	0.82	398	353	11.31	271	280	-3.32	N/A	N/A	N/A
f [MHz]	6.78	6.78	0	6.78	6.84	-0.88	6.78	6.905	-1.84	6.78	6.741	0.58	6.78	6.76	0.29

the output dc voltage to the amplitude of the presented emf (V_{dc}/v_{in}) was calculated. The experimental results are compared with time-domain SPICE simulations. The simulations used the measured component values from the experimental work (Table IV).

According to the plots in Fig. 7a, all designs showed low deviation in efficiency over the entire output power range. The worst case deviation in efficiency over P_{dc} was in Design #2 and was 4%. Designs #2, #3 and #5 exhibited deviations in $R_{in,ser}$ lower than 3% from the nominal value while Designs #1 and #4 exhibited deviations of 7.2% and 9.4% respectively. Design #1 had the lowest capacitance across the diode amongst the implemented rectifiers and is therefore more sensitive to the variation of pn junction capacitance. Design #4 on the other hand, although having a significantly higher C_p , is more sensitive to variations in X_C than Design #1 due to the selection of A_r . Based on the Q_{in} profile in Fig. 5, it can be seen that a small variation in A_r , when it is greater than 1.6, will result in a large variation of Q_{in} and therefore in $R_{in,p}$. While Design #5, the current driven topology, operates in the same A_r region as Design #4, its $R_{in,ser}$ profile over output power has a much lower deviation than $R_{in,ser}$ of Design #4. This is because the capacitance across the diode in Design #5 is twice the magnitude of the respective capacitance in Design #4.

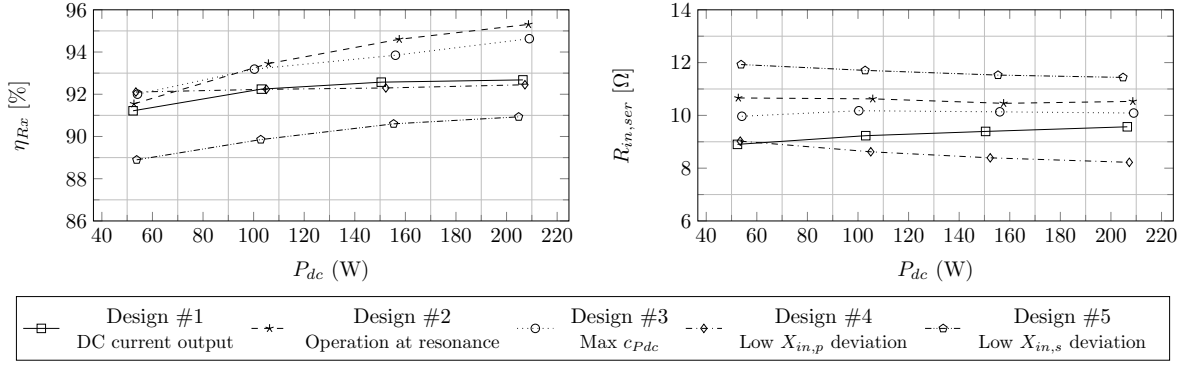
Design #5 (the CDR) has the lowest η_{Rx} because the losses in its L are the highest amongst the five designs. Since all the designs, apart from Design #4, have the same R_{dc} , the inductors (L) in Designs #1 to #3 and #5 experience identical voltage waveforms over a cycle. Thus, the highest inductor current amongst the designs occurs in Design #5 causing the highest losses. Comparing the HVDR circuits, Designs #1 to #4, the higher the presented $R_{in,ser}$ the higher receiving end efficiency was achieved. In general all the developed rectifiers presented an error in their $R_{in,ser}$ proportional to the error between theoretical and experimental values of R_{dc} . Error in the experiment is larger for solutions where the diode parasitic capacitance is significant compared to the external capacitance across the diode and where the sensitivity of Q_{in} to A_r is large. Hence, the greatest error was observed in Designs #4

and #5.

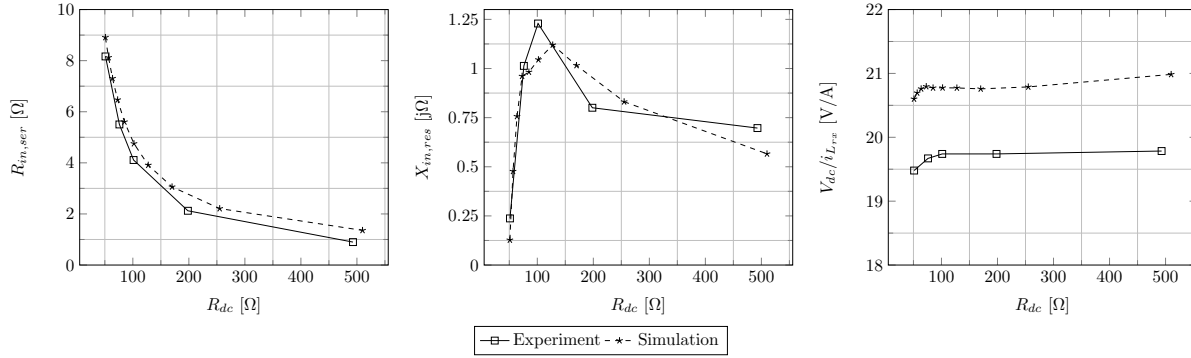
Figs. 7b, 7c & 7d show good agreement between simulation and experimental results. In simulations, the passive components were set equal to the measurements of the impedance analyzer. Designs #2, #4 and #5, performed as expected in that in Designs #4 and #5, $R_{in,ser}$ decreased with R_{dc} and in Design #2, $R_{in,ser}$ increased with R_{dc} . In terms of input reactance variation, Designs #4 and #5 presented residual reactances at the receiving end with magnitude smaller than 1% of the impedance of the receiving coil, X_{rx} . Furthermore, in these two designs the output voltage was inherently regulated when the current in the receiving coil was kept constant. The output voltage was regulated within 3% and 8% of its initial value in Design #4 and in Design #5 respectively. Design #2 also exhibits some inherent output voltage regulation with a deviation of 25% for constant input voltage.

To investigate further how the implemented rectifiers affect the efficiency of the inductive link and the reflected impedance at the transmitting coil, the measured values of Fig. 7b and Fig. 7d were mapped on the contour plots of Fig. 8. Figs. 8a, 8b and 8c show the contours of the inductive link efficiency (η_{link}), the reflected resistance at the transmitting coil (R_{ref}), and the reflected reactance at the transmitting coil (X_{ref}) respectively. All contours of Fig. 8 are plotted as functions of the normalised resistance seen by the receiving coil, $R_{in,ser}/R_{ac,ser}$, and the normalised residual reactance at the resonant receiving tank, $X_{in,res}/X_M$. Note that $R_{ac,ser}$ is the ac resistance at the receiving end that provides the optimal link efficiency and X_M is the impedance of the magnetising inductance between the coils forming the inductive link (which is 7.11 Ω at the frequency of operation). The data of the contours were derived from the parameters of the inductive link in [2] and the IPT expressions in [1]. Moreover, the contours of η_{link} and R_{ref} are normalised to their respective optimal values (shown in Table II). Finally, the contours of X_{ref} are normalised to X_M .

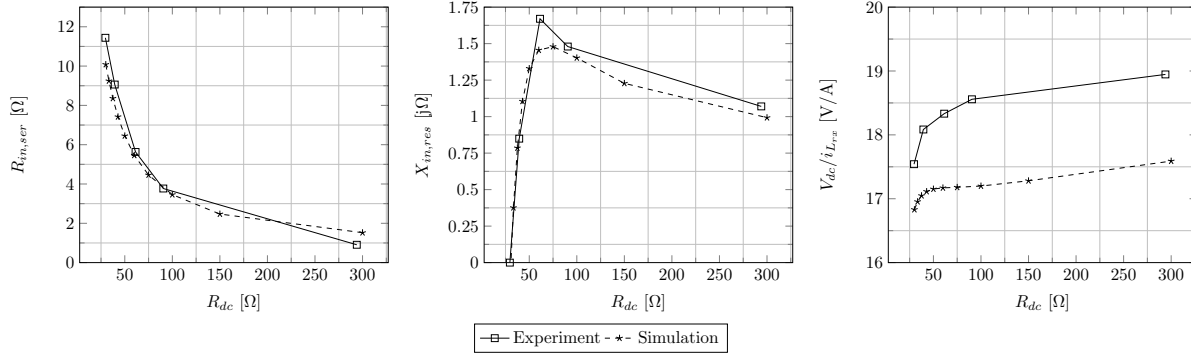
The trajectories of the normalised values of $R_{in,ser}$ and $X_{in,res}$ have been added to the contours plots of Fig. 8. Specifically, the experimental data of Designs #2 and #4 have been used as they both exhibit the desirable property of



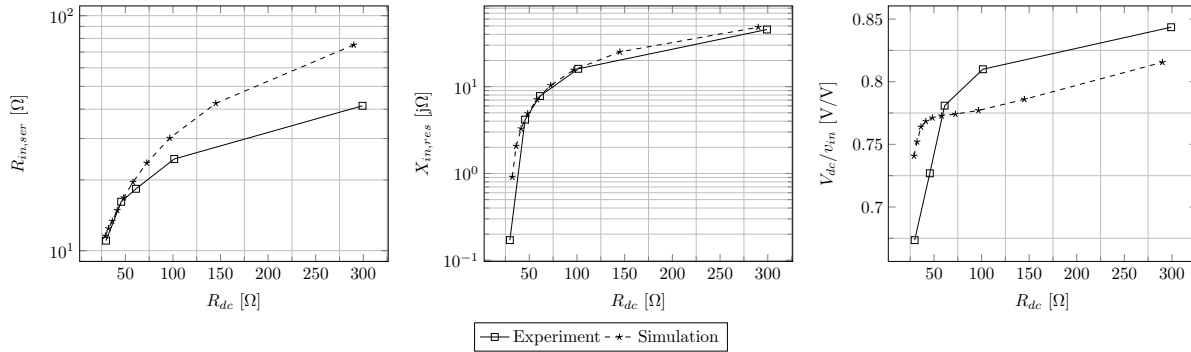
(a) Performance of all rectifier designs at a constant dc load resistance.



(b) Series input resistance and reactance of Design #4 (HVDR: Low $X_{in,p}$ deviation) at variable dc load. Output voltage was inherently regulated within 2.1 % of its initial value by keeping constant the current in the receiving coil.



(c) Series input resistance and reactance of Design #5 (CDR: Low $X_{in,s}$ deviation) at variable dc load. Output voltage was inherently regulated within 8 % of its initial value by keeping constant the current in the receiving coil.



(d) Series input resistance and reactance of Design #2 (HVDR: Operation at resonance) at variable dc load. Output voltage was inherently regulated within 25.3 % of its initial value by keeping constant the amplitude of the emulated induced emf in the receiving end.

Fig. 7: Case studies experimental results.

inherent voltage regulation for variable dc load and Design #4 also exhibits low deviation in input reactance with variation in dc load. As Design #5 behaves in the same way as Design #4 with regards to these parameters, only the data from Design #4 has been plotted in Fig. 8.

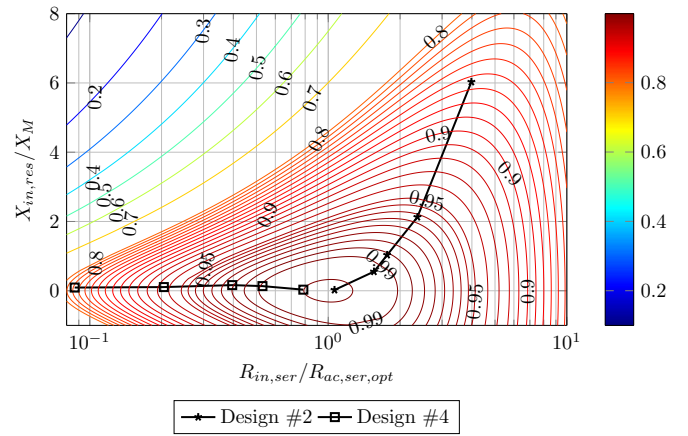
As shown in Fig. 8a, at 100% dc load all tested designs are within the $\eta_{link,opt}$ contour. As the load decreases down to 50%, all designs fall into lower efficiency contours but they are within 97% of the $\eta_{link,opt}$. Although Design #2 is detuning the receiving coil at dc loads lower than 100%, the resultant link efficiency is actually slightly higher than that for Design #4 for the same load value. This occurs because $R_{in,ser}$ of Design #2 increases from its initial value, rather than decreases as in the case of Design #4, where the link efficiency is more tolerant to the presence of residual reactance, as shown in the contours of Fig. 8a. At dc loads lower than 20%, the link efficiency in both designs falls below 90% of $\eta_{link,opt}$, however the losses in the inductive link would be smaller in magnitude than the losses when maximum power is transferred at $\eta_{link,opt}$.

In Fig. 8b and Fig. 8c, the reflected impedance at the transmitting coil behaves inversely to the input impedance of the utilised rectifier. This is a basic property of inductive links. In Design #2, R_{ref} decreases linearly as R_{dc} increases. On the other hand, in Design #4, R_{ref} increases linearly as R_{dc} increases. In terms of reflected reactance (X_{ref}), in Design #2 the reflected reactance does not increase beyond 0.15 times X_M , despite the residual reactance at the receiving coil reaching six times X_M . Comparing the magnitude of X_{ref} for Design #2 to the impedance of the transmitting coil (X_{Tx}), X_{ref} is always lower than 1% of X_{Tx} and will not affect the tuning of the Tx coil. On the contrary, while Design #4 does not introduce a $X_{in,res}$ greater than 25% of X_M , the X_{ref} for this design increases with R_{dc} and can reach almost three times the magnitude of X_M .

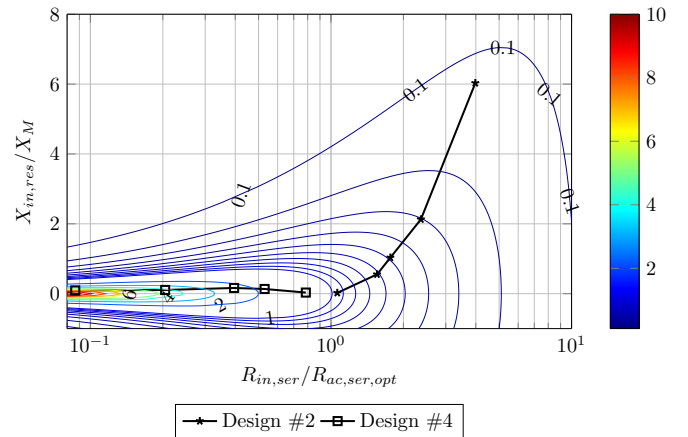
The inherent output voltage regulation feature can be achieved in both Design #2 and Design #4. For Design #2 a constant output current at the Tx will result in a constant induced voltage in the Rx coil, thus providing the condition for the output voltage regulation feature. In Design #2 the transmitting resonant tank will not be affected by the variation of R_{dc} . Hence, since R_{ref} decreases with R_{dc} , a constant output current Class-EF inverter such as the one presented in [36] will be compatible. In Design #4, inherent output voltage regulation occurs with a constant current in the Rx coil. This requires the variation of the magnitude of the induced voltage in the Rx coil and hence, the variation in the current in the Tx coil. Since the reflected impedance increases with R_{dc} a Class-D ZVS constant output voltage inverter such as the one presented in [37] will be capable to provide the conditions for inherent output voltage regulation and compensate for the variation in reflected reactance at the Tx coil.

V. CONCLUSIONS

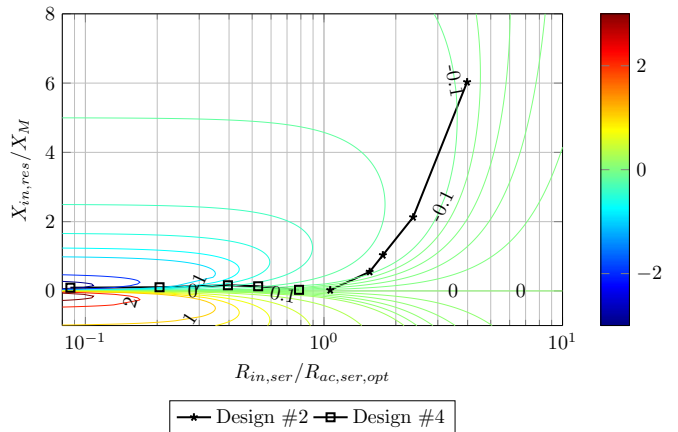
In this paper conventional and hybrid Class-E half-wave zero dv/dt rectifiers were analysed in terms of the parameter A_r , defined as the ratio of the resonant frequency of the



(a) Contours of link efficiency (η_{link}) normalised to the optimal link efficiency ($\eta_{link,opt}$). From 80% to 95% the contours appear in steps of 1% and from 95% to 99% in steps of 0.5%.



(b) Contours of reflected resistance (R_{ref}) to the transmitting coil (L_{tx}) normalised to the reflected resistance at optimal link efficiency conditions ($R_{ref,opt}$). From 0.1 to 1 the contours appear in steps of 0.1 and then in steps of 1.



(c) Contours of reflected reactance (X_{ref}) to the transmitting coil (L_{tx}) normalised to the impedance of the magnetizing inductance of the coils forming the inductive link (X_M). From 0 to 0.1 the contours appear in steps of 0.02, then from 0.1 to 0.2 in steps of 0.1 and then in steps of 0.2.

Fig. 8: Effect of implemented rectifiers on inductive link efficiency and loading on the transmitting coil.

utilised LC network to the operating frequency. The results of this analysis were illustrated in a way that designers are able to observe the variations in rectifier behavior over A_r and choose the best suited topology based on the requirements of the application. Based on the analytical results the following conclusions can be made about half-wave Class-E rectifiers operating with a duty cycle equal or lower than 50 % when designed for IPT:

- The voltage driven Class-E rectifier with a series inductor will always require an inductor of larger impedance than the impedance of the receiving coil to allow the input resistance required by optimal link efficiency conditions to be presented. Therefore, the implementation of the series inductor will always be a challenge when high Q , high impedance coils are forming the link.
- The voltage driven Class-E rectifier with a series capacitor does not absorb the parasitic capacitance of the diode in its LC network and its operation will be heavily affected when the pn junction capacitance is in the same order of magnitude as the series capacitor.
- There are specific regions of A_r where the behavior of the input resistance of the rectifiers is consistent with duty cycle variations. When A_r is unity the series input resistance of the rectifiers, whether being voltage or current driven, increases as the output dc resistance increases. On the other hand, when A_r is greater than 1.5, the series input resistance of the rectifiers decreases as the dc resistance increases.
- The current driven topology, the voltage driven topology with a series capacitor and the hybrid topology, exhibit a low deviation in their input reactance as the output dc resistance increases, when designed with an A_r between 1.75 and 2. In particular a deviation by less than 13 % is observed in the input reactance of the current driven topology and a deviation by less than 5 % is observed in the input reactance of the latter two rectifier topologies.

The case studies in this work were focused on making the use of Class-E rectifiers feasible and effective in IPT systems. Furthermore, the experiments aimed to investigate the effect of passives on the performances of the hybrid rectifier and to evaluate the behavior of input resistance and input reactance of the hybrid and current driven rectifiers. A test rig was developed that emulates IPT conditions and properly characterises rectifiers without the need of an inductive link. Based on the experimental results the following conclusions can be made:

- The best efficiency was recorded in the hybrid topology when designed to operate at a unity A_r .
- The sensitivity of the implemented rectifiers on the diode's pn junction capacitance becomes higher when A_r is smaller than 0.4 and greater than 1.6. In the former region, the external capacitor across the diode is lower than the resultant capacitance in any other A_r region when the rectifier is designed to present the same input resistance while having the same dc load. In the latter region, a small variation in A_r will result in a much larger variation in the input resistance of the topology.
- The hybrid and current driven Class-E rectifiers, when

designed at A_r between 1.75 to 2 can provide inherent output voltage regulation as their dc load decreases from 100 % to 10 %. This feature is feasible by keeping the current in the receiving coil constant. The achieved regulation was within 3 % and 8 % of the nominal output voltage for the hybrid and the current driven rectifier respectively.

In summary, the hybrid rectifier has been shown to be a good choice for weakly coupled inductive links as it can have a power robust operation and match any dc load to the desirable ac resistance while exhibiting any of the properties of the conventional Class-E half-wave zero dv/dt rectifiers. This includes low loss inductor realisation, low deviation in input reactance and inherent output voltage regulation.

APPENDIX A EQUATIONS AND GENERAL DERIVATION METHOD OF CLASS-E RECTIFIER DESIGN VARIABLES

The input sources were assumed sinusoidal and were expressed by:

$$v_{in}(\theta) = \frac{V_{dc}}{M_V} \sin(\theta + \phi), \quad (11)$$

in the voltage driven topologies, and:

$$i_{in}(\theta) = \frac{I_{dc}}{M_I} \sin(\theta + \phi), \quad (12)$$

in the current driven topology. In both (11) and (12) θ is the product of ω and time, t , and ϕ is the phase of the input source when the diode turns OFF. The following definitions were also used:

$$i_C(\theta) = \left(\frac{1}{X_C} \right) \frac{d}{d\theta} [v_D(\theta)], \quad (13)$$

$$v_L(\theta) = X_L \frac{d}{d\theta} [i_L(\theta)], \quad (14)$$

$$-V_{dc} = \frac{1}{2\pi} \int_0^\psi v_D(\theta) d\theta, \quad (15)$$

$$I_{dc} = \frac{1}{2\pi} \int_\psi^{2\pi} i_D(\theta) d\theta, \quad (16)$$

where (15) and (16) are derived by applying Kirchoff's voltage and current laws respectively. Variable ψ is the interval in which the diode is reverse biased:

$$\psi = 2\pi(1 - d_r). \quad (17)$$

From (15) and (16) the loaded quality factor as a function of ψ , and hence duty cycle, is given by:

$$Q_r = - \left(\frac{\int_0^\psi v_D(\theta) d\theta}{\int_\psi^{2\pi} i_D(\theta) d\theta} \right) \left(\frac{1}{X} \right). \quad (18)$$

In order for the topologies to achieve low dv_D/dt at turn OFF the following conditions must also be met:

$$v_D(0) = v_D(\psi) = \frac{d}{d\theta} [v_D(0)] = 0, \quad (19)$$

$$i_D(2\pi) = 0, \quad (20)$$

$$i_C(\psi^-) = i_D(\psi^+). \quad (21)$$

Finally the following expressions have to be used for deriving the input reactance of the rectifiers at the frequency of operation:

$$i_{in,1} = \frac{1}{\pi} \int_0^{2\pi} i_{v_{in}}(\theta) \cos(\theta + \phi) d\theta, \quad (22)$$

$$v_{in,1} = \frac{1}{\pi} \int_0^{2\pi} v_{i_{in}}(\theta) \cos(\theta + \phi) d\theta, \quad (23)$$

where $i_{in,1}$ is the first harmonic of the current $i_{v_{in}}$, which is drawn from the input source in the voltage driven rectifiers and $v_{in,1}$ is the first harmonic of the voltage $v_{i_{in}}$ across the input source in the CDR.

The equations of the design variables of the examined rectifiers are presented in Table V to Table VI. It should be noted that for the CDR (Fig. 2b) and the series-*C* VDR (Fig. 2c), there are different equations describing variables ϕ and Q_r , although their profiles over duty cycle and ratio A_r have the same evaluation. Furthermore, in the HVDR (Fig. 2a), variables ϕ and Q_r are independent of variable B and are therefore expressed by the equations of the respective variables in the series-*C* VDR. The process of deriving the design variables as functions of duty cycle and ratio A_r can be found in [26] for operation at resonance and in [30] for operation around resonance.

APPENDIX B

DESCRIPTION OF TESTING APPARATUS

Characterising a rectifier in terms of input resistance and efficiency while integrated in a multi-MHz IPT system is not a trivial task. Calculation of input power to the rectifier will be required and therefore the voltage across the receiving coil, $v_{L_{rx}}$, and the current through it have to be measured. In this frequency range the capacitance introduced by a voltage probe is not negligible and can affect the circuit under test. Therefore, measuring the voltage across L_{rx} while operating in a complete IPT system, will detune the receiving end and lead to wrong assumptions about the effect of the rectifier on the inductive link. Furthermore, while instrumentation via capacitive division could make the presence of a voltage probe intrinsic capacitance insignificant, the input power measurement will still be of great uncertainty because the phase between $v_{L_{rx}}$ and the current input to the rectifier will be nearly ninety degrees. Therefore, small errors in phase will cause large errors in the ac power measurement. Hence, a test rig for rectifier characterisation was developed that overcomes these challenges by taking the measurements separately from the inductive link.

The developed test rig, Fig. 9, is based on the voltage source Class-D inverter. The rig consists of a half-bridge, a resonant tank and the rectifier under test (RUT). The resonant tank is formed by the receiving coil, L_{rx} , and the tuning capacitor, C_{rx} . The half-bridge is driven by square wave gate drives to be able to generate voltages over a wide frequency band and it outputs a square wave voltage, v_{in} , which represents the voltage induced in a coil at the presence of an alternating magnetic field (IPT conditions). Due to the high quality factor of the resonant tank, which is essential for

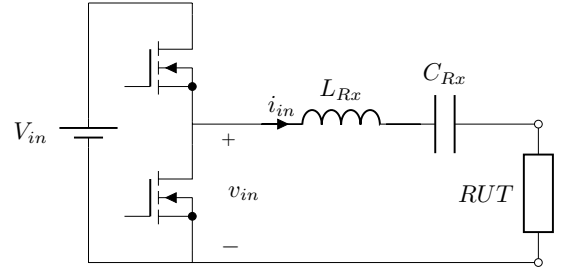


Fig. 9: Class-D inverter based test rig [25].

high link efficiencies at weakly coupled inductive links, only the fundamental harmonic of the square wave delivers power to the rectifier. Therefore, the current in L_{rx} , represented by i_{in} in Fig. 9, is sinusoidal. According to the tuning method of the receiving coil, the rig presents the appropriate ac source, voltage or current, for the RUT. As v_{in} , in Fig. 9, simulates the induced emf in the receiving coil it will be in phase with i_{in} when L_{rx} is properly tuned and small phase errors will be insignificant. Moreover, the presence of a voltage probe at the output of the half-bridge does not affect the tuning of the resonant tank. Hence, all the challenges from the presence of the inductive link are solved.

From Fig. 9, the average of the product of v_{in} and i_{in} at one period provides a measurement for the input power, P_{in} , which represents the power into the receiver (R_x) of an IPT system. Using the dc output power of the rectifier the efficiency of the receiver, η_{Rx} , can be calculated. Furthermore, using P_{in} and the rms of i_{in} the input resistance seen by the receiving coil, $R_{in,ser}$, can also be calculated. When a rectifier is added to the test rig, the amplitude of v_{in} is kept constant while its switching frequency is adjusted such that maximum dc output power is achieved. Maximum extracted dc power will be achieved only at the point where L_{rx} is at resonance.

Phase compensation for the instrumentation was performed to eliminate any time scale errors in the P_{in} measurement. Firstly, the phase introduced by the transfer impedance of the current probe was accounted for using data provided by the manufacturing company (Pearson Electronics). Secondly, a comparison was made between the propagation delays in the BNC cable connecting the output of the current probe to the oscilloscope and the voltage probe used to monitor v_{in} . No difference was found between the propagation delays in the two cables. For zero skew, v_{in} and i_{in} will be in phase during rectifier characterisation for a perfectly tuned circuit. Therefore, Fig. 7a shows the worst case efficiencies because any skew that is unaccounted for would result in the measured input power being lower than the actual input power and hence the actual efficiency would be higher than the recorded efficiency.

The instrumentation used to monitor each signal of the test rig is listed in Table IX, along with the maximum attenuation error and the worst case systematic error in the measurement of each signal. From the worst case error in each measurement, the worst case systematic error in parameters η_{Rx} and $R_{in,ser}$ was also calculated and is presented in Table X.

TABLE V: Design variables of current driven rectifier (Fig. 2b).

Operating away from resonance, $A_r \neq 1$,	
$\tan \phi = -Ar [(\cos(Ar \psi) - \cos \psi) (\sin(Ar \psi) + Ar (2\pi - \psi)) - (\sin(Ar \psi) - Ar \sin \psi) (\cos(Ar \psi) - 1)] / \{(\cos(Ar \psi) - 1) (Ar^2 (\cos \psi - 1) + 2 \sin((Ar \psi)/2)^2) - (\sin(Ar \psi) - Ar \sin \psi) [\sin(Ar \psi) + Ar (2\pi - \psi)]\}.$	(24)
$Q_r = -4\pi [\sin(Ar \psi) \sin \phi + Ar \cos(\phi + \psi) - Ar \cos(Ar \psi) \cos \phi] / \{-Ar^3 [2 \cos(\phi + \psi) (1 - \cos(Ar \psi)) + \cos \phi (2 (\cos(Ar \psi) - 1) + \cos \psi (2\pi - \psi)^2 - \cos(Ar \psi) (\psi - 2\pi)^2) + \sin \phi (2\pi - \psi) ((\psi - 2\pi) \sin \psi + 2 (\cos(Ar \psi) - 1))] - 2 Ar (\cos(Ar \psi) - 1) (\cos(\phi + \psi) - \cos \phi - 2\pi \sin \phi + \psi \sin \phi) - Ar^2 \sin(Ar \psi) \sin \phi (2\pi - \psi)^2\}.$	(25)
$M_I = [\sin(Ar \psi) \sin \phi + Ar \cos(\phi + \psi) - Ar \cos(Ar \psi) \cos \phi] / [Ar Q (Ar^2 - 1) (\cos(Ar \psi) - 1)].$	(26)
$N_{in} = -\psi / [2\pi (Ar^2 - 1)] - \{[(2 \sin(Ar \psi) (1 - Ar^2)) (\cos \phi)^2 + \sin \psi (2 Ar (1 - Ar^2)) (\sin \phi)^2 - 2 \sin(Ar \psi) \cos \psi + [Ar \sin(2\phi) (1 - Ar^2)] (\sin \psi)^2 + [Ar \sin(2\psi) (Ar^2 - 1)] / 2 + \sin \psi [2 Ar \cos(Ar \psi) - \sin(2\phi) \sin(Ar \psi) (1 - Ar^2)]] / [2 Ar \pi (Ar^2 - 1)^2] - K Q \{2 \cos(Ar \psi) \sin(\phi + \psi) - 2 Ar \sin(Ar \psi) \cos(\phi + \psi) + 2 \sin(\phi + \psi) (Ar^2 - 1) - 2 Ar^2 \sin \phi\} / [2\pi (Ar^2 - 1)].$	(27)
Operating at resonance, $A_r = 1$.	
$\tan \phi = -[\psi \sin \psi (\psi - 2\pi) + (\cos \psi - 1) (\psi + \sin \psi)] / [(\cos \psi)^2 + (\psi^2 - 2\pi \psi - 4) \cos \psi + (2\pi - 2\psi) \sin \psi + 3].$	(28)
$Q_r = 4\pi [\psi \sin(\phi + \psi) - \sin \phi \sin \psi] / \{4 \cos(\phi + \psi) + \cos \phi (4 (\cos \psi - 1) + \psi \sin \psi (\psi - 2\pi)^2) - 4 \cos(\phi + \psi) \cos \psi + \sin \phi (2\pi - \psi) [4 (\cos \psi - 1) + (2\pi - \psi) (\psi \cos \psi - \sin \psi)]\}.$	(29)
$M_I = [\psi \sin(\phi + \psi) - \sin \phi \sin \psi] / [2 Q_r (\cos \psi - 1)].$	(30)
$N_{in} = [2\psi + 2 \sin(2\phi) + \sin(2\psi) - 2 \sin(2(\phi + \psi)) - 4\psi (\sin \phi)^2 - 4\psi \sin(\phi + \psi)^2] / [16\pi] + [M_I Q_r (\sin(\phi + 2\psi) / 2 - 2 \sin(\phi + \psi) + (3 \sin \phi) / 2 + \psi \cos \phi)] / [2\pi].$	(31)

TABLE VI: Design variables of voltage driven rectifier with series inductor (Fig. 2d).

Operating away from resonance, $A_r \neq 1$.	
$\tan(\phi + \pi) = \{4 \sin((Ar \psi)/2)^2 (Ar^2 \sin(\psi/2)^2 - 1) + Ar \sin \psi (\sin(Ar \psi) - Ar (2\pi - \psi)) - Ar \sin(Ar \psi) (2\pi - \psi)\} / \{Ar [(1 - \cos \psi) \sin(Ar \psi) + (Ar (2\pi - \psi + \sin \psi)) \cos(Ar \psi) - Ar (\sin \psi + \cos \psi (2\pi - \psi))]\}.$	(32)
$M_V = \{Ar [\cos \phi (\sin(Ar \psi) - Ar \sin \psi) + Ar \sin \phi (\cos(Ar \psi) - \cos \psi)] / [(Ar^2 - 1) (\cos(Ar \psi) - 1)].$	(33)
$Q_r = 2 \{ (Ar^2 - 1) (Ar \psi - \sin(Ar \psi)) M_V + Ar^2 (\sin(Ar \psi) - Ar \sin \psi) \sin \phi + Ar (2 \sin((Ar \psi)/2)^2 + Ar^2 (\cos \psi - 1)) \cos \phi \} / \{Ar (Ar^2 - 1) (2 \sin(\phi + \psi) - 2 \sin \phi + 2 \cos \phi (2\pi - \psi) + M_V (\psi - 2\pi)^2)\}.$	(34)
$N_{in} = [4\pi Ar (Ar^2 - 1)^2] / \{[4\pi - 2\psi + 2 \sin(2\phi + \psi) - \sin(2\phi) - \sin(2\phi + 2\psi) + 2 \sin \psi - 4 M_V (\cos(\phi + \psi) - \cos \phi - \sin(\phi + \psi) (2\pi - \psi))] Ar^5 + [2\psi - 8\pi + 2 \sin(2\phi + \psi) (\cos(Ar \psi) - 2) + \sin(2\phi) + \sin(2\phi + 2\psi) - 2 \sin \psi (\cos(Ar \psi) + 2) - M_V (4 \cos(\phi + \psi) (\cos(Ar \psi) - 2) + 4 \cos \phi + 8 \sin(\phi + \psi) (2\pi - \psi))] Ar^3 + 4 \sin(Ar \psi) [(\cos \psi - M_V \sin(\phi + \psi)) Ar^2 + M_V \sin(\phi + \psi)] + [2 (2\pi - (\sin(2\phi + \psi) + \sin \psi) (\cos(Ar \psi) - 1)) + 4 M_V (\cos(\phi + \psi) (\cos(Ar \psi) - 1) + \sin(\phi + \psi) (2\pi - \psi))] Ar\}.$	(35)
Operating at resonance, $A_r = 1$ (Derived expressions same as in [26]).	
$\tan \phi = [2 \cos \psi (\cos \psi + \psi (\psi - 2\pi) - 4) + 4 \sin \psi (\pi - \psi) + 6] / [\sin(2\psi) + 2 ((\psi - 2\pi) \psi - 1) \sin \psi + 2\psi (\cos \psi - 1)].$	(36)
$M_V = [\psi \cos(\phi + \psi) - \cos \phi \sin \psi] / [2 (\cos \psi - 1)].$	(37)
$Q_r = [\cos(\phi - \psi) + 3 \cos(\phi + \psi) - 4 \cos \phi + 2\psi \sin(\phi + \psi) + 4 M_V (\psi - \sin \psi)] / [4 \sin(\phi + \psi) - 4 \sin \phi + 4 \cos \phi (2\pi - \psi) + 2 M_V (\psi - 2\pi)^2].$	(38)
$N_{in} = -16\pi / [4 \cos(\phi + 2\psi) + 16 \cos(\phi + \psi) - 20 \cos \phi + 16 (\psi - 2\pi) \sin(\phi + \psi) + 8\psi \sin \phi] M_V + 6\psi - 16\pi - 8 \sin(2\phi + \psi) + 4 \sin(2\phi) + \sin(2\psi) + 4 \sin(2\phi + 2\psi) - 8 \sin \psi + 2\psi \cos(2\phi) - 2\psi \cos(2\phi + 2\psi)].$	(39)

TABLE VII: Design variables of voltage driven rectifier with series capacitor (Fig. 2c).

Operating away from resonance, $A_r \neq 1$.	
$\tan \phi = \frac{[(\cos(A_r \psi) - 1)(A_r^2 (\cos \psi - 1) + 2 \sin((A_r \psi)/2)^2) - (\sin(A_r \psi) - A_r \sin \psi)(\sin(A_r \psi) + A_r (2\pi - \psi))]}{[A_r (\sin(A_r \psi) - A_r \sin \psi)(\cos(A_r \psi) - 1) - A_r (\cos(A_r \psi) - \cos \psi)(\sin(A_r \psi) + A_r (2\pi - \psi))]} \quad (40)$	
$M_V = (\sin(A_r \psi) \cos \phi - A_r (\sin(\phi + \psi) - \cos(A_r \psi) \sin \phi)) / (A_r (A_r^2 - 1) (\cos(A_r \psi) - 1)). \quad (41)$	
$Q_r = \frac{[4 \sin((A_r \psi)/2) \cos \phi + 2 A_r \sin(A_r \psi) (M_V + \sin \phi) - 2 A_r^2 (\cos \phi - \cos(\phi + \psi) + M_V \psi) - 2 A_r^3 M_V (\sin(A_r \psi) - A_r \psi)] / [A_r^4 (2 \sin(\phi + \psi) - 2 \sin \phi (\sin \psi (2\pi - \psi) + 1) + M_V (2\pi - \psi)^2 + 2 \cos \phi \cos \psi (2\pi - \psi)) - A_r^2 (2 \sin(\phi + \psi) - 2 \sin \phi + 2 \cos(A_r \psi) \cos \phi (2\pi - \psi)) - A_r^6 M_V (2\pi - \psi)^2 - 2 A_r^5 M_V \sin(A_r \psi) (2\pi - \psi) + 2 A_r^3 \sin(A_r \psi) (M_V + \sin \phi) (2\pi - \psi)]}{\quad} \quad (42)$	
$N_{in} = \frac{4\pi (A_r^2 - 1)^2 / \{[4\pi + M_V (4 (\cos(A_r \psi) \cos(\phi + \psi) - \cos \phi)) A_r^4 + M_V [4 \sin(A_r \psi) \sin(\phi + \psi)] A_r^3 + [2\psi - 8\pi + \sin(2\phi) + 2 \cos(A_r \psi) \sin \psi + \sin(2\phi + 2\psi) - M_V (4 (\cos(A_r \psi) \cos(\phi + \psi) - \cos \phi)) - 2 \sin(2\phi + \psi) \cos(A_r \psi)] A_r^2 - [M_V (4 \sin(A_r \psi) \sin(\phi + \psi)) + 4 \sin(A_r \psi) \cos \psi] A_r + 2 (2\pi - \psi) - \sin(2\phi) + 2 \cos(A_r \psi) \sin \psi - \sin(2\phi + 2\psi) + 2 \sin(2\phi + \psi) \cos(A_r \psi)]\}}{\quad} \quad (43)$	
Operating at resonance, $A_r = 1$ (Derived expressions same as in [33]).	
$\tan \phi = [2(\pi - \psi) \sin \psi + (\cos \psi)^2 + ((\psi - 2\pi) \psi - 4) \cos \psi + 3] / [(\cos \psi - 1) + (\psi - 2\pi) \psi \sin \psi + \psi (\cos \psi - 1)]. \quad (44)$	
$M_V = -[\cos \phi \sin \psi - \psi \cos(\phi + \psi)] / (2 \cos \psi - 2). \quad (45)$	
$Q_r = \frac{\{4 [(\sin \psi - \psi) M_V + \cos \phi] - 2 [\cos(\phi + \psi) + \cos \phi \cos \psi + \psi \sin(\phi + \psi)]\} / \{4 (2\pi - \psi) \sin \psi + 2 (\psi - 2\pi)^2 M_V + 4 \sin \phi + 3 \cos(\phi + \psi) (\psi - 2\pi) + (\psi - 2\pi) \cos(\phi - \psi) + 2 \sin(\phi + \psi) [(\psi - 2\pi) \psi - 2]\}}{\quad} \quad (46)$	
$N_{in} = (16\pi) / [4 M_V (\cos(\phi + 2\psi) - \cos \phi + 2 \psi \sin \phi) + 16\pi + \sin(2\psi) + 2 \psi (\cos(2\phi) - \cos(2\phi + 2\psi) - 1)]. \quad (47)$	

TABLE VIII: Design variables of hybrid rectifier (Fig. 2a).

Operating away from resonance, $A_r \neq 1$		
$\tan \phi = eq(40)$	$M_V = eq(41) / [B + 1]$	$Q_r = eq(42)$
$N_{in} = \frac{(4\pi (A_r^2 - 1)^2 (B + 1)^2) / \{[\cos \phi (4 \cos \psi (1 - A_r^2) (\cos(A_r \psi) - \cos \psi)) + 4 A_r M_V (A_r^2 - 1) (\sin(A_r \psi) \cos \psi - A_r \cos(A_r \psi) \sin \psi) (B + 1)] \sin \phi + 4\pi (B + 1) - 2\psi + \sin(2\psi) + A_r^4 (4\pi (B + 1)) - [4 \sin \psi (A_r^2 - 1) (\cos(A_r \psi) - \cos \psi)] \cos \phi^2 + \cos \phi [4 A_r M_V (A_r^2 - 1) (B + 1) (\sin(A_r \psi) \sin \psi + A_r (\cos(A_r \psi) \cos \psi - 1))] - A_r^2 (8\pi (B + 1) - 2\psi + \sin(2\psi) - 4 \cos(A_r \psi) \sin \psi) - 4 A_r \sin(A_r \psi) \cos \psi\}}{\quad} \quad (48)$		
Operating at resonance, $A_r = 1$		
$\tan \phi = eq(44)$	$M_V = eq(45) / [B + 1]$	$Q_r = eq(46)$
$N_{in} = 16\pi (B + 1)^2 / \{[8 M_V \psi \sin \phi + 16\pi + 4 M_V (\cos(\phi + 2\psi) - \cos \phi)] (B + 1) + \sin(2\psi) + 2 \psi (\cos(2\phi) - \cos(2\phi + 2\psi) - 1)\}. \quad (49)$		

TABLE IX: Worst case errors in test rig measurements.

Measured Quantity	Probe Part Number	Attenuation	Attenuation Error	Measurement Error
v_{in}	PPE 6kV	1000:1	2 %	1.96 %
i_{in}	6585 CM	1:1	N/A	1 %*
V_{dc}	N2891A	100:1	2 %	1.94 %
I_{dc}	N2783A	10:1	1 %	0.892 %

*Error in current to voltage transformation.

TABLE X: Worst case errors in receiving end efficiency (η_{Rx}) and rectifier input series resistance ($R_{in,ser}$).

Calculated Quantity	Positive Error	Negative Error
η_{Rx}	5.97 %	5.63 %
$R_{in,ser}$	2.99 %	2.93 %

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REFERENCES

- [1] K. van Schuylenbergh and R. Pueris, *Inductive Powering: Basic Theory and Application to Biomedical Systems*. Springer, 2009.
- [2] M. Pinuela, D. C. Yates, S. Lucyszyn, and P. D. Mitcheson, "Maximizing DC-to-load efficiency for inductive power transfer," *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2437–2447, 2013.
- [3] C. H. Kwan, G. Kkelis, S. Aldhafer, J. Lawson, D. C. Yates, P. C.-K. Luk, and P. D. Mitcheson, "Link efficiency-led design of mid-range inductive power transfer systems," in *IEEE PELS Workshop on Emerging Technologies: Wireless Power (WoW)*, 2015. IEEE, 2015, pp. 1–7.
- [4] M. K. Kazimierczuk and J. Jozwik, "Class-E zero-voltage-switching and zero-current-switching rectifiers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 37, no. 3, pp. 436–444, 1990.
- [5] S. Birca-Galateanu and A. Ivascu, "Class-E low dv/dt and low di/dt rectifiers: energy transfer, comparison, compact relationships," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl. (19932003)*, vol. 48, no. 9, pp. 1065–1074, Sep 2001.
- [6] W. Nitz, W. Bowman, F. Dickens, F. Magalhaes, W. Strauss, W. Suiter, and N. Ziesse, "A new family of resonant rectifier circuits for high frequency DC-DC converter applications," in *Third Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 1988. IEEE, 1988, pp. 12–22.
- [7] W. Cai, Z. Zhang, X. Ren, and Y.-F. Liu, "A 30-MHz isolated push-pull VHF resonant converter," in *Twenty-Ninth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2014. IEEE, 2014, pp. 1456–1460.
- [8] J. M. Rivas, D. Jackson, O. Leitermann, A. D. Sagneri, Y. Han, and D. J. Perreault, "Design considerations for very high frequency dc-dc converters," in *37th IEEE Power Electronics Specialists Conference, 2006. PESC'06*. IEEE, 2006, pp. 1–11.
- [9] Y. Han, O. Leitermann, D. Jackson, J. M. Rivas, D. J. Perreault *et al.*, "Resistance compression networks for radio-frequency power conversion," *IEEE Trans. Power Electron.*, vol. 22, no. 1, pp. 41–53, 2007.
- [10] J. M. Rivas, O. Leitermann, Y. Han, and D. J. Perreault, "A very high frequency DC-DC converter based on a class resonant inverter," *IEEE Trans. Power Electron.*, vol. 26, no. 10, pp. 2980–2992, 2011.
- [11] J. S. Glaser and J. M. Rivas, "A 500 W push-pull dc-dc power converter with a 30 MHz switching frequency," in *Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2010. IEEE, 2010, pp. 654–661.
- [12] Z. Zhang, J. Lin, Y. Zhou, and X. Ren, "Analysis and Decoupling Design of a 30 MHz Resonant SEPIC Converter," *IEEE Trans. Power Electron.*, vol. 31, no. 6, pp. 4536–4548, June 2016.
- [13] K. H. Lee, E. Chung, G. S. Seo, and J. I. Ha, "Design of GaN transistor-based class E DC-DC converter with resonant rectifier circuit," in *IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, 2015, Nov 2015, pp. 275–280.
- [14] S. Aldhafer, D. C. Yates, and P. D. Mitcheson, "Design and Development of a Class EF 2 Inverter and Rectifier for Multi-megahertz Wireless Power Transfer Systems," *IEEE Trans. Power Electron.*, vol. PP, no. 99, pp. 1–1, 2016.
- [15] G. Kkelis, J. Lawson, D. Yates, M. Pinuela, and P. Mitcheson, "Integration of a Class-E low DV/DT rectifier in a wireless power transfer system," in *Wireless Power Transfer Conference (WPTC)*, 2014 IEEE, May 2014, pp. 72–75.
- [16] S. Aldhafer, P. C.-K. Luk, K. El Khamlichi Drissi, and J. F. Whidborne, "High-Input-Voltage High-Frequency Class E Rectifiers for Resonant Inductive Links," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1328–1335, 2015.
- [17] M. K. Kazimierczuk, "Analysis of Class-E zero-voltage-switching rectifier," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 37, no. 6, pp. 747–755, Jun 1990.
- [18] R. C. Pilawa-Podgurski, A. D. Sagneri, J. M. Rivas, D. Anderson, D. J. Perreault *et al.*, "Very-high-frequency resonant boost converters," *IEEE Trans. Power Electron.*, vol. 24, no. 6, pp. 1654–1665, 2009.
- [19] W. Liang, J. Glaser, and J. Rivas, "13.56 MHz High Density DC-DC Converter With PCB Inductors," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4291–4301, Aug 2015.
- [20] J. Santiago-Gonzalez, K. M. Elbaggari, K. K. Afridi, D. J. Perreault *et al.*, "Design of Class E Resonant Rectifiers and Diode Evaluation for VHF Power Conversion," *IEEE Trans. Power Electron.*, vol. 30, no. 9, pp. 4960–4972, 2015.
- [21] K. Inoue, T. Nagashima, X. Wei, and H. Sekiya, "Design of high-efficiency inductive-coupled wireless power transfer system with class-DE transmitter and class-E rectifier," in *Industrial Electronics Society, IECON 2013 - 39th Annual Conference of the IEEE*, Nov 2013, pp. 613–618.
- [22] M. Liu, M. Fu, and C. Ma, "Parameter Design for A 6.78-MHz Wireless Power Transfer System Based on Analytical Derivation of Class E Current-Driven Rectifier," *IEEE Trans. Power Electron.*, vol. PP, no. 99, pp. 1–1, 2015.
- [23] M. K. Kazimierczuk and J. Jozwik, "Class E zero-voltage-switching rectifier with a series capacitor," *IEEE Transactions on Circuits and Systems*, vol. 36, no. 6, pp. 926–928, 1989.
- [24] M. Kazimierczuk and W. Szaraniec, "Analysis of a Class-E rectifier with a series capacitor," *IEE Proceedings G (Circuits, Devices and Systems)*, vol. 139, no. 3, Jun 1992.
- [25] G. Kkelis, D. C. Yates, and P. D. Mitcheson, "Comparison of current driven Class-D and Class-E half-wave rectifiers for 6.78 MHz high power IPT applications," in *Wireless Power Transfer Conference (WPTC)*, 2015 IEEE. IEEE, 2015, pp. 1–4.
- [26] A. Ivascu, M. Kazimierczuk, and S. Birca-Galateanu, "Class-E resonant low dv/dt rectifier," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl. (19932003)*, vol. 39, no. 8, pp. 604–613, Aug 1992.
- [27] M. Kazimierczuk, B. Tomescu, and A. Ivascu, "Class-E resonant rectifier with a series capacitor," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl. (1993-2003)*, vol. 41, no. 12, pp. 885–890, Dec 1994.
- [28] P. C.-K. Luk, S. Aldhafer, W. Fei, and J. F. Whidborne, "State-Space Modeling of a Class Converter for Inductive Links," *IEEE Trans. Power Electron.*, vol. 30, no. 6, pp. 3242–3251, 2015.
- [29] M. Liu, M. Fu, and C. Ma, "A compact Class E rectifier for megahertz wireless power transfer," in *IEEE PELS Workshop on Emerging Technologies: Wireless Power (WoW)*, 2015. IEEE, 2015, pp. 1–5.
- [30] S. Birca-Galateanu and J.-L. Cocquerelle, "Class-E half-wave low dv/dt rectifier operating in a range of frequencies around resonance," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl. (19932003)*, vol. 42, no. 2, pp. 83–94, Feb 1995.
- [31] G. Kkelis, D. C. Yates, and P. D. Mitcheson, "Hybrid Class-E low dv/dt rectifier for high frequency inductive power transfer," in *2016 IEEE Wireless Power Transfer Conference (WPTC)*. IEEE, 2016, pp. 1–4.
- [32] M. K. Kazimierczuk and D. Czarkowski, *Resonant power converters*. John Wiley & Sons, 2012.
- [33] M. Kazimierczuk and J. Jozwik, "Class-E zero-voltage-switching rectifier with a series capacitor," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 36, no. 6, pp. 926–928, Jun 1989.
- [34] M. Kazimierczuk, "Class-E low dv/dt rectifier," *IEE Proceedings B (Electric Power Applications)*, vol. 136, no. 6, pp. 257–262, Nov 1989.
- [35] G. Kkelis, D. C. Yates, and P. D. Mitcheson, "Multi-Frequency Class-D Inverter for Rectifier Characterisation in High Frequency Inductive Power Transfer Systems," in *8th IET International Conference on Power Electronics, Machines and Drives (PEMD 2016)*, April 2016.
- [36] S. Aldhafer, P. D. Mitcheson, and D. C. Yates, "Load-independent Class EF inverters for inductive wireless power transfer," in *2016 IEEE Wireless Power Transfer Conference (WPTC)*, May 2016, pp. 1–4.
- [37] M. de Rooij, "eGaN FET based Wireless Energy Transfer Topology Performance Comparisons," in *PCIM Europe 2014; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management; Proceedings of*. VDE, 2014, pp. 1–8.