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Indacenodithiophene–benzothiadiazole organic field-effect transistors with gravure-printed semiconductor and dielectric on plastic

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Abstract

We demonstrate the gravure printing of a high-performance indacenodithiophene (IDT) copolymer, indacenodithiophene–benzothiadiazole (C_{16}IDT–BT), onto self-aligned organic field-effect transistor architectures on flexible plastic substrates. We observed that the combination of a gravure-printed dielectric with gravure-printed semiconductor yielded devices with higher mean-effective mobility than devices manufactured using photolithographically patterned dielectric. Peak mobilities of $\mu = 0.1$ cm^2 V^{-1} s^{-1} were measured, and exceed previous reports for non-printed C_{16}IDT-BT on non-flexible silicon substrates.

Introduction

The field of organic electronics allows us to develop new technologies such as flexible displays, radio frequency identification (RFID) tags, and intelligent packaging.[1–3] The solubility of many organic semiconductors and dielectrics allows solution-based processes such as gravure, inkjet, and flexographic printing to be used,[4] introducing a manufacturing paradigm impossible with current silicon technology.

Gravure printing is well established as a manufacturing technique.[5] It facilitates high-speed, large-area printing and allows the patterning of multiple structures in parallel, providing a high-throughput solution. Gravure printing has already been demonstrated as viable for the manufacture of organic field-effect transistors (OFETs),[6–8] organic light-emitting diodes (OLEDs),[9] and other components vital for the development of flexible printed electronics.[10,11] To fully realize these devices, organic semiconductors that are both compatible with printing and yield robust electrical characteristics are required.

One such series of semiconductors are polymers based upon indacenodithiophene (IDT). A variety of IDT copolymers have been reported yielding good performance in OFETs as well as organic photovoltaic devices.[12–17] Good charge transport in these systems is attributed to the high rigidity of the polymer backbone, and correspondingly low conformational disorder.[12,18]

Recently Zhang et al. reported on an IDT copolymer, indacenodithiophene–benzothiadiazole (C_{16}IDT–BT),[19] with high field-effect mobilities that the authors found were relatively insensitive to processing conditions (tested using spin-coating in different laboratories). It is proposed that the dominant charge transport mechanism for the material is along the polymer backbone, which minimizes inter-chain hopping, and hence results in robust device characteristics.[20] C_{16}IDT–BT is therefore of particular relevance in printed electronics, where it is desirable to minimize process variations caused during printing. Here we demonstrate how C_{16}IDT–BT can be successfully gravure printed onto a flexible self-aligned OFET architecture. We note that in our results device characteristics are sensitive to the dielectric deposition method used.

In this work, we manufacture self-aligned OFETs on a plastic substrate. Self-aligned architectures provide significant gains in device AC performance, thanks to minimized electrode overlaps.[21] In addition, the layer-to-layer registration tolerance can be increased as the source and drain electrodes, as well as the effective channel length (L), are defined by a pre-patterned gate. Figure 1 illustrates a schematic of this architecture, along with the chemical structure of C_{16}IDT–BT and a photograph of a flexible substrate with gravure printed semiconductor.

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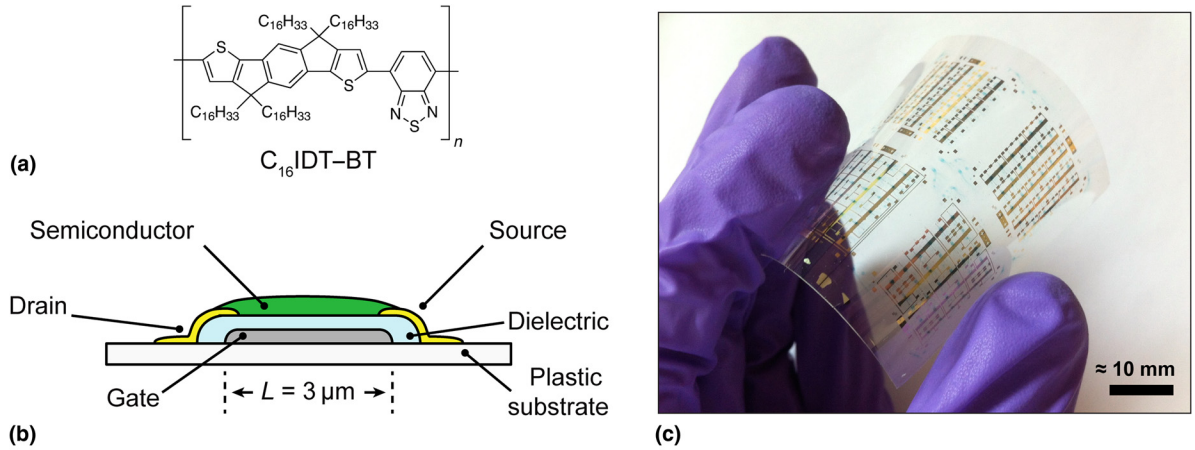

Figure 1. (a) Chemical structure of C_{16}IDT–BT. (b) Schematic representation of the BGBC device architecture used in this work. (c) Photograph of the C_{16}IDT–BT gravure printed onto self-aligned transistor substrate.

Experimental

Gate patterning

A 50 nm thick aluminum gate (≥99.9% purity, Testbourne Inc.) was evaporated onto a plastic foil, and patterned using photolithography (Microposit S1813, Rohm and Haas) via a mask aligner (MJB3, Süss).

Dielectric patterning

A proprietary dielectric system (GSID 938109-1, BASF SE), based upon a triacrylate cross-linking agent and high molecular weight poly(methyl methacrylate) (PMMA) viscosity modifier, was formulated into both photo-patternable and gravure-printable formulations,[22,23] and patterned on top of the gate. For photo-patterned dielectric a formulation containing photo-initiator was spin-coated onto the substrate, soft-baked for 5 min at 115 °C to drive off any remaining solvent, and selectively exposed in a mask aligner to partially cross-link an array of dielectric pads. Un-cross-linked material was removed by immersion in the formulation's solvent system and cross-linking completed by UV irradiation (ELC-500, Electro Lite Corporation) under nitrogen for 10 min. For gravure-printed dielectric the formulation was filtered through a 0.45 μm polytetrafluoroethylene (PTFE) filter onto an electrochemically etched gravure cliché (Goerz Gravurtechnik GmbH), with a screen density of $l_{SD} = 250$ lines/cm.

Self-aligned source–drain electrodes

A bilayer lift-off process was used to define a nominal channel length of $L = 3$ μm and width of $W = 5000$ μm, as well as interdigitated source–drain electrodes. We have previously reported full details of this process.[24] In summary, a bilayer stack of 100 nm of lift-off resist (LOR1A, MicroChem Corporation) and 500 nm of photoresist (Microposit S1805 G2, Rohm and Haas) is exposed in a mask aligner. However, the substrate is inverted, so the UV light passes through both a standard photolithography mask and also the back of the substrate. Hence, the gate structure stops the resist stack immediately above the gate being exposed, defining the source–drain electrode spacing. The source–drain electrodes comprise a chromium adhesion layer (~5 nm) and thermally evaporated gold (~50 nm). Given the previous observations of the predominantly p-type nature of C_{16}IDT–BT, substrates were immersed in a 5 mM solution of pentafluorobenzenethiol (Sigma Aldrich) in ethanol for 10 min to form a self-assembled monolayer (SAM) on the gold electrodes to improve charge injection.[25]

Gravure-printed semiconductor

A 5 mg/mL ink formulation of C_{16}IDT–BT (Flexink Ltd) in chlorobenzene (purity ≥ 99.0%, Merck) was prepared, with no further stirring required. The ink formulation was filtered through a 0.45 μm PTFE filter onto the cliché inking edge, immediately prior to printing. Gravure printing was performed using a Labratester (Norbert Schläfli Maschinen), with a polyester doctor blade (E600/25/22, Esterlam International), and at a nominal nip pressure of 500 N/cm^2. The copper-based chromium-coated gravure clichés feature electrochemically etched cells in the printing surface, which define the pattern to be printed. Here we used gravure screen densities of $l_{SD} = 100$ lines/cm and $l_{SD} = 250$ lines/cm, which correspond to a spacing of ~100 μm and ~40 μm between adjacent cells. In each print, four quadrants were patterned, each featuring a 5 × 6 array of semiconductor squares, each square having a nominal size of 2 × 2 mm^2. Printed substrates were annealed at 150 °C on a hotplate overnight in a glovebox. Electrical characterization was performed under nitrogen using a parameter analyzer (4156c, Agilent) and probe station (1260, Signatone).

Results and discussion

Gravure-printed C_{16}IDT–BT

The influence of both print speed and cliché screen density is shown in Fig. 2. It was found that at low print speeds (s = 0.27 m/s) significant slurring (an increase in the size of a printed

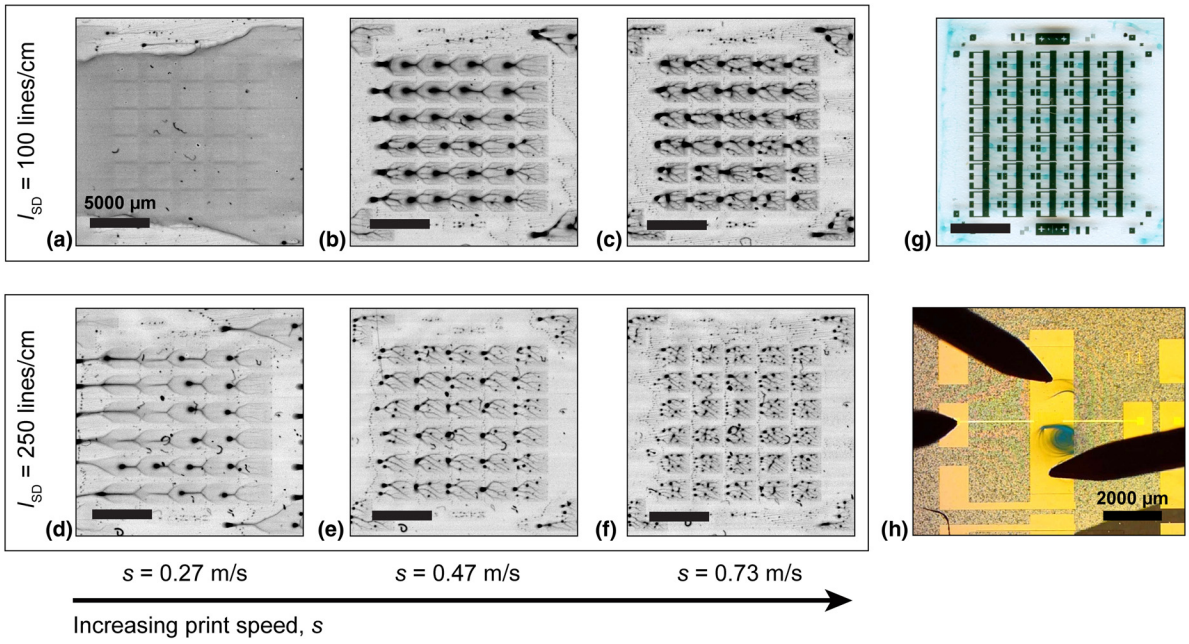

Figure 2. Scanned images of gravure-printed C_{16}IDT–BT on a plastic substrate, showing the impact of print speed and cliché screen density on print behavior. (a)–(c) l_{SD} = 100 lines/cm, (d)–(f) l_{SD} = 250 lines/cm. All scale bars equal for (a)–(g). Images are shown in grayscale and contrast-enhanced for clarity. (g) Scanned image of the final gravure-printed semiconductor on top of the device architecture. (h) Optical micrograph of a single device under test.

feature compared with the corresponding size defined by the cliché) was observed. In the extreme case, this resulted in the coalescence of adjacent features [Fig. 2(a)] whereby the combination of low print speed and screen density results in an excessive volume of ink transfer onto the substrate. Such coalescence can potentially result in poor device isolation and high leakage currents. A screen density of l_{SD} = 100 lines/cm was found to yield less macroscopic modulation of the semiconductor compared with l_{SD} = 250 lines/cm [compare the modulation present in Figs. 2(c) and 2(f)]. This behavior occurs as a result of the corresponding decrease in cliché cell spacing from ~100 to ~40 µm, resulting in a greater influence of the cell sidewalls.[23] Less modulation is desirable, at the expense of the two-dimensional (2D) semiconductor pad definition, as this minimizes variation of the semiconductor film thickness in the active device region. Film thickness variations can lead to incomplete semiconductor coverage in the channel region and differences in chain conformation and packing. These can impact channel conductivity, transport and trapping. Hence, a screen density of l_{SD} = 100 lines/cm was used to deposit the semiconductor in the devices presented below.

Figures 2(g) and 2(h) show a scanned image of the transistor array with gravure-printed semiconductor on top of the device architectures, as well as an optical micrograph of a single transistor under test. Thin-film semiconductors were very difficult to image in the final device architecture, with minimal contrast between the film and substrate; however, the excess of material in the center of the device in Fig. 2(h) suggests that some film modulation is present in the final devices, which agrees with the spread in device parameters shown in the electrical data discussed below (any variations in polymer coverage, chain conformation, and packing could impact the effective mobility, turn-on voltage, hysteresis, and off-current).

C_{16}IDT–BT organic field-effect transistors

Figure 3 shows the electrical data obtained from devices with photo-patterned and gravure-printed dielectric. In the case of photo-patterned dielectric, p-type transistor behavior is observed with a peak-effective mobility of $\mu = 0.02$ cm^2 V^{-1} s^{-1} at $V_{GS} = V_{DS} = -20$ V, and a median-effective mobility of $\mu \approx 10^{-4}$ cm^2 V^{-1} s^{-1} (taking into account both forward and reverse sweeps). Here we refer to our extracted values as an effective mobility, as they are a convolution of both the intrinsic mobility of the material and also other effects, such as contact resistance which acts to lower the measured mobility.[26] With this conservative estimate, these results compare well with the previous report of Zhang et al.[19] of $\mu \approx 0.02$ cm^2 V^{-1} s^{-1} for C_{16}IDT–BT spin-coated on bottom-gate bottom-contact (BGBC) OFETs on a silicon substrate. Although lower than the performance reported for top-gate top-contact devices, our BGBC geometry facilitates self-alignment, with numerous other benefits. The lack of electrode overlap between gate–drain and gate–source electrodes results in very low leakage currents (<0.1 nA for photo-patterned devices). This lack of overlap reduces capacitive coupling between electrodes, increasing the operational speed of devices.[27] The architecture also allows the semiconductor to be deposited last, minimizing the impact of subsequent processing.

For devices with a gravure-printed dielectric the peak-effective mobility increased to $\mu = 0.1$ cm^2 V^{-1} s^{-1} at V_{GS} =

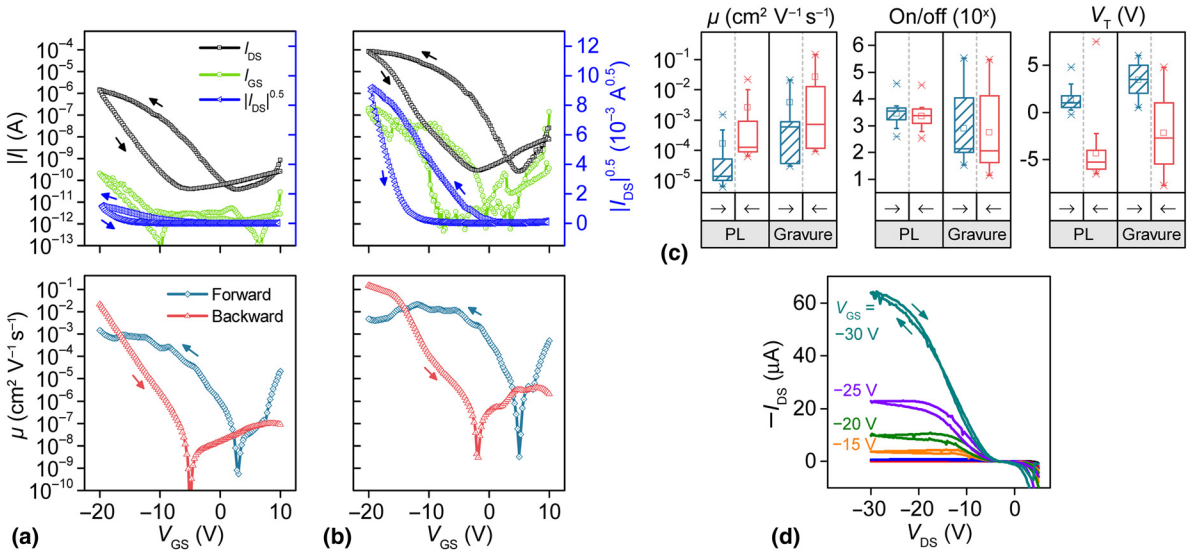

Figure 3. Electrical characterization data of gravure printed C_{16}IDT–BT OFETs on plastic. (a) Average transfer characteristics and extracted mobilities of 15 OFETs with photo-patterned dielectric. (b) Equivalent plots of average of six OFETs with gravure-printed dielectric. (c) Box plots summarizing the distribution of extracted figures of merit. Box represents 25th and 75th percentiles, horizontal line indicates median, square (□) the mean, whiskers the 10th and 90th percentiles, crosses (×) the min/max values. Values are extracted from forward (→) and reverse (←) sweeps. (d) Example of output characteristics obtained from the best-performing device (gravure-printed dielectric), corresponding to transfer characteristics shown in (b). Nominal device geometry is $W = 5000$ and $L = 3$ μm.

$V_{DS} = -20$ V, with a median-effective mobility of $\mu \approx 10^{-3}$ cm^2 V^{-1} s^{-1}. These results exceed previous reports and suggest that the dielectric layer formed by gravure printing facilitates better charge transport in C_{16}IDT–BT, at the expense of a slight increase in dielectric leakage. This leakage arises from the different film thicknesses of the photo-patterned and printed dielectric layers. Surface profilometry measurements of equivalent devices were used to determine film thicknesses of $t \approx 90$ nm and $t \approx 170$ nm for photo-patterned and printed dielectric layers, yielding specific capacitances $C' \approx 33$ nF/cm^2 and $C' \approx 17$ nF/cm^2, respectively. Similarly the yield for devices with gravure printed dielectric dropped to 18% ($^6/_{34}$ devices), compared to 44% for photo-patterned ($^{15}/_{34}$ devices). This is due to lower breakdown voltages for the thinner dielectric. Hence, increasing the dielectric thickness either through modifying the print parameters,[23] or overprinting, is desirable to reduce leakage and increase device robustness.[4]

It is important to consider the origin of the field-effect mobility enhancement observed in Fig. 3. Considering the standard OFET current–voltage relations,[28] an approximate 50% thinning of the dielectric layer would yield an increase of 2 in the effective mobility, assuming all other parameters remain constant. However, the parameter extraction presented here is corrected for the increased specific capacitance of the thinner layer. The main difference between the two dielectric deposition methods, other than film thickness, is that the gravure-printed dielectric is thermally cross-linked, rather than photo-patterned. The effective mobility of an OFET is strongly influenced by the dielectric–semiconductor interface,[29] as are other behaviors such as hysteresis and the threshold voltage (discussed below). We hypothesize that the presence of residual photo-initiator in the photo-patterned dielectric degrades device characteristics,[30] resulting in a lower-effective mobility compared with the gravure-printed devices.

Figure 3(c) summarizes the extracted figures of merit, illustrating the relative shift in mobility for devices with gravure-printed dielectric. Parameter extraction is performed on both the forward and reverse characterization sweeps to give a complete understanding of device behavior. Hysteresis is observed in both types of device, manifesting as a splitting of the threshold voltage on the forward and reverse sweeps, and indicating the presence of charge traps at the dielectric–semiconductor interface. We note that in previous reports using C_{16}IDT–BT a fluropolymer dielectric (CYTOP) was used,[19,20] suggesting that dielectric dipolar disorder between the PMMA viscosity modifier in our dielectric ink and the semiconductor at the interface may increase charge trapping.[29]

The architecture presented here was designed to target high-frequency OFET switching, hence the use of a relatively short-channel length ($L = 3$ μm). However, a consequence of this downscaling is an increase in the impact of contact resistance between the source–drain electrodes and semiconductor channel, as illustrated by the slight s-shaped slope in the output characteristics shown in Fig. 3(d). Further development of the contact interface (for example, through the exploration of different SAMs) is a route to minimizing this effect.[31–33]

Conclusions

Our findings show that C_{16}IDT–BT is a good candidate for high-performance printed electronics, yielding mobilities in

the range of $\mu \approx 0.02$–$0.1\ cm^2\ V^{-1}\ s^{-1}$ in our self-aligned BGBC architecture. Devices with gravure printed (rather than photo-patterned) dielectric yield higher mobilities, indicating an improved dielectric-semiconductor interface when both C_{16}IDT-BT and the dielectric are printed.

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