Polymer-sorted (6,5) single-walled carbon nanotubes for solution-processed low-voltage flexible microelectronics

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Abstract

We report on low operating voltage transistors based on polymer-sorted semiconducting (6,5) single-walled carbon nanotube (SWNT) networks processed from solution at room temperature. The (6,5) SWNTs were separated from the as-received carbon nanotubes mixture using a polyfluorene-based derivative as the sorting and dispersing polymer agent. As-prepared devices exhibit primarily p-type behavior with channel current on/off ratio $>10^3$ and hole mobility ≈ 2 cm^2 V^{-1}s^{-1}. These transistor characteristics enable realization of low-voltage unipolar inverters with wide noise margins and high signal gain (>5). Polymer/(6,5) SWNT transistors were also fabricated on free-standing polyimide foils. The devices exhibit even higher hole mobility (≈ 8 cm^2 V^{-1}s^{-1}) and on/off ratios ($>10^4$) while remaining fully functional when bent to a radius of 4 mm.

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Carbon nanotubes (CNTs) have attracted significant attention in recent years owing to their unique physical properties. For example, the high current driving capabilities and mechanical stability of metallic CNTs makes them attractive for application in microelectronic interconnects[1], whereas the tunable energy bandgap of semiconducting single-walled CNTs (SWNTs) renders them suitable for use in a range of emerging opto/electronics including light-emitting devices[2,3], photovoltaic devices[4], transistors[5,6] and integrated circuits.[7] Unfortunately, the vast majority of these devices have so far relied on SWNTs grown by chemical vapor deposition (CVD) directly onto rigid substrates at high temperatures (T ≈ 900 ℃) which makes the process expensive and incompatible with large-area applications.

To overcome the processing limitations associated with growth of CNTs via CVD, recent efforts have been devoted to disperse the as-grown nanotubes in suitable solvents and then processing them onto arbitrary substrates using different solution-based techniques.[5,8–12] Using such intrinsically simple approaches, flexible transistors and complementary logic circuits based on a solution-deposited random network of SWNTs have recently been reported.[8,13,14] Among the various processing methods available, drop-cast[5], dip-coating[8], inkjet printing[9], blade coating[10], self-assembly[11] and gravure printing[12] have proven suitable for large-area deposition of SWNTs at room temperature. However, purifying and sorting semiconducting SWNTs from metallic CNTs and/or catalyst residues before deposition is technologically challenging but of crucial importance for numerous device applications. To this end, recent studies have shown that conjugated polymers, such as polyfluorene-based derivatives, are effective in interacting and sorting CNTs with specific diameters.[15,16] This simple process has been demonstrated to enable precise separation of SWNTs with semiconducting properties[17], potentially overcoming problems with

residual metallic CNTs in the as-dispersed material. Despite the great promise of the approach, however, use of polymer-sorted semiconducting SWNTs for microelectronic applications has been surprisingly limited.

Here, we report the development of low operating voltage transistors and logic circuits fabricated using solution-deposited networks of semiconducting SWNTs that have been chirality sorted using a polyfluorene-based derivative.[15–17] Transistors prepared on rigid substrates exhibit strong p-type behavior with maximum hole mobility of ~2 cm^2 $V^{-1}s^{-1}$. By exploring the low-temperature processing advantage offered by the polymer/SWNTs dispersion, we were also able to fabricate transistors and circuits on free-standing polyimide foils that remain functional even when bent to a tensile radius of 4 mm.

Bottom-gate coplanar transistors were fabricated on silicon substrates with 1 µm thermally-grown SiO_2 and 500 nm SiN_X deposited by plasma-enhanced chemical vapor deposition (PECVD), acting as isolation and adhesion layers. A 30 nm-thick layer of Cr was subsequently e-beam evaporated and later patterned to form the bottom-gate electrodes via standard photolithography. Following, a 50 nm-thick Al_2O_3 gate dielectric (capacitance = 168 nF/cm^2) was deposited by atomic layer deposition (ALD) at 150 °C. Source and drain electrodes consisting of 10 nm/50 nm of Ti/Au were e-beam evaporated and patterned using a lift-off process. The samples were sequentially cleaned by ultra-sonication in acetone and in IPA baths for 5 minutes each, and exposed to UV-ozone for 20 minutes. **Figure 1(a)** shows the schematic of the resulting transistor architecture. The polymer/SWNTs dispersion was prepared by mixing 100 mg CoMoCat SWNTs (Sigma-Aldrich) and 200 mg poly[(9,9-dioctylfluorenyl-2,7-diyl)-alt-co-(6,6'-{2,2'-bipyridine})]

[PFO-BPy, **Fig. 1(b)**] (American Dye Source) in 200 ml of toluene. The mixture was then subjected to ultrasonication using a horn sonicator for 14 hours. Subsequently, the solution was centrifuged at 4000 rpm for 30 minutes, the supernatant was then selected[18] and the excess polymer was removed via vacuum filtration. The resulting (6,5) SWNTs were then re-dispersed in chlorobenzene through 20 minutes ultra-sonication and 1 h cup sonication. Solution deposition was performed in a nitrogen glovebox, by spin-coating the polymer/(6,5) SWNT solution at 1000 rpm for 30 seconds, followed by 15 minutes thermal annealing at 90 °C. The resulting transistors had channel length (L) and width (W) of 10 μm and 500 μm, respectively. Electrical characterization was performed under a nitrogen atmosphere while the device parameters were calculated using the gradual channel approximation model.[19]

The absorption characteristics of polymer/(6,5) SWNT dispersed in chlorobenzene was measured using a Varian Cary 5000 UV-Vis-NIR spectrophotometer in absorbance mode, with 1 mm light path cuvette. **Figure 1(b)** displays the as measured absorption spectrum of the polymer/(6,5) SWNT solution in chlorobenzene. Evidence of the nearly single chirality (6,5) SWNTs arises from the existence of the two sharp absorption peaks at 1000 nm and 575 nm, which correspond respectively to the first (E_{11}) and second (E_{22}) subband excitonic transitions of the (6,5) SWNT[18], highlighting the advantage of using polyfluorene-based polymers as the dispersant agents. On the basis of these results we argue that solution-deposited polymer-sorted (6,5) SWNT networks are expected to be semiconducting.[5,20,21]

The surface morphology of the as-spun polymer/(6,5) SWNT network was studied by tapping-mode atomic force microscopy (AFM). **Figure 2(a)** shows the AFM image of the surface

topography of a random polymer/(6,5) SWNT network deposited onto Al_2O_3, while **Figure 2(b)** displays the topography of the bare Al_2O_3 surface. Further information on the surface topography is provided by surface line scans (stacked) and the height distribution shown in **Figures 2(c)** and **(d)**, respectively. The topography of (6,5) SWNTs deposited onto atomically flat SiO_2 substrates has also been measured (**Fig. S1**).[22] The latter allows analysis of the surface coverage (**Fig. S2**), as well as estimation of the percolation threshold.[22]

The charge transporting characteristics of the polymer/(6,5) SWNT networks were studied using bottom-gate coplanar transistor architectures [**Figure 1(a)**]. **Figure 3** displays representative sets of the transfer **(a)** and output **(b)** characteristics of a transistor fabricated on a rigid substrate. The device exhibits low operating voltage and strong p-type character although weak electron transport at drain and gate voltages of V_D = -10 V and at V_G > 0 V is also observed. The predominantly p-type character of the channel conduction is attributed to the electron trapping nature of the SWNT/Al_2O_3 interface and the use of high work function (≈5 eV) Au S/D electrodes and /or to the presence of atmospheric oxidants that are known to behave as electron traps[23,24]. Therefore, use of staggered transistor architectures in combination with a suitable dielectric is expected to yield ambipolar behavior[20,21,25]. All transistors exhibit noticeable operating hysteresis (~3.4 V) and is attributed to the presence of surface adsorbates and water on the Al_2O_3 surface[11,26]. Despite this, all devices exhibit low operating voltages (< | 10 | V), appreciable channel current on/off ratio ($I_{ON}/I_{OFF} > 10^3$), low threshold voltage (V_{TH} ~ -1.1 V), a sub-threshold swing (SS) of ~ 1.73 V/dec, and linear (μ_{LIN}) and saturation (μ_{SAT}) hole mobility of 0.7 $cm^2 V^{-1}s^{-1}$, 2.3 $cm^2 V^{-1}s^{-1}$, respectively.

The promising operating characteristics of the polymer/(6,5) SWNT transistors prompted us to explore the potential of the technology for fabrication of unipolar integrated circuits. **Figure 4(a)** shows the circuitry of the p-type inverter used. The circuit consists of a driving transistor with L and W of 20 μm and 1.4 mm, respectively, and one passive load (R_L) with resistance 160 kΩ. The latter was formed using the gate metal itself (Cr with resistivity $\rho = 1.16\times10^{-6}$ Ω·m), patterned in the right dimensions, therefore eliminating the requirement for further process steps.

Figure 4(b) displays the voltage transfer characteristic and the corresponding static gain measured for a unipolar p-type inverter. The circuit exhibits high gain (G) for a unipolar circuit (~5.3 V/V) at the midpoint voltage (V_M ~ -1 V) even at low supply voltages of V_{DD} = -2 V. Importantly, the inverter exhibits nearly rail-to-rail output swing with the output high voltage approaching zero (V_{OH} = -0.02 V) and the output low voltage close to V_{DD} (V_{OL} = -1.81 V) with noise margin high (NM_H) and noise margin low (NM_L) of 0.4 V and 0.6 V, respectively. These results compare favorably with previously reported unipolar inverters based on solution-processed mixed SWNTs using diode-load[8,27] and voltage bootstrapping circuitries[28], although somewhat improved performances have been reported for inverters based on complementary/-like architectures.[13,14,29,20]

To further demonstrate the potential of the proposed technology we fabricated polymer/(6,5) SWNTs transistors directly on free-standing flexible polyimide foils. **Figure 4(c)** displays a representative set of transfer characteristics obtained from a low-voltage polymer/(6,5) SWNT transistor. The device exhibits strong p-type behavior with signs of ambipolar charge transport at V_D = -10 V and V_G > 0 V. Key device parameters include: $I_{ON}/I_{OFF} > 10^4$, V_{TH} = -3.1 V, SS = 1.09

V/dec, μ_{LIN} = 3.1 $cm^2 V^{-1}s^{-1}$ and μ_{SAT} = 8.1 $cm^2 V^{-1}s^{-1}$. The significantly higher hole mobility and on/off ratio of the transistor, as compared to devices fabricated on rigid substrates, is most likely attributed to improved substrate surface coverage with polymer/(6,5) SWNT due to different surface topography (**Fig. S3**).[22] To test the mechanical flexibility of the devices we performed bending tests by attaching the transistors onto a double-sided adhesive tape and winding them around metal rods of different radius, so that tensile strain was applied only parallel to the transistor channel. **Figure 4(d)** displays a typical set of transfer characteristics of a flexible polymer/(6,5) SWNT transistor measured while flat and bent to different tensile radii R_T of 5 mm and 4 mm. The inset shows a photograph of actual devices during testing. As can be seen, the polymer/(6,5) SWNT transistors are fully operational even when strained down to a 4 mm tensile radius (mechanical strain ε = 0.63 %)[30] with minor variations in the device performance (V_{TH} shift of -50 mV). Due to their high mechanical flexibility, the polymer/(6,5) SWNT network could in principle be bent to even smaller radii, but this is known to induce cracks in the brittle Cr gate.[31]

In conclusion, we have reported the development of transistors and integrated unipolar circuits based on solution-processed polymer-sorted semiconducting (6,5) SWNTs. The devices exhibit low operating voltage with hole mobility of ~2 $cm^2 V^{-1}s^{-1}$ and on/off ratio ~3×10^3, whereas unipolar inverters exhibit a signal gain of 5.3 V/V, wide noise margin and a low voltage operation (-2 V). Finally, polymer/(6,5) SWNT transistors were also fabricated on flexible polyimide foils exhibiting hole mobility of 8.1 $cm^2 V^{-1}s^{-1}$, on/off ratio of ~10^4, while remain fully functional when bent down to 4 mm tensile radius.

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Figure 1. (a) Schematic of the bottom-gate coplanar polymer/(6,5) SWNT transistor fabricated on a rigid substrate. (b) Absorption spectrum of the polymer/(6,5) SWNT solution in chlorobenzene, with 1 mm light path. The peaks at λ = 1000 nm and λ = 575 nm, respectively, correspond to the first and second excitonic transitions of the (6,5) nanotube. The peak at λ = 355 nm corresponds to the absorption of the sorting polymer PFO-BPy. Inset: Chemical structure of PFO-BPy.

Figure 2. (a, b) AFM topography images of the as-spun polymer/(6,5) SWNT network and of the Al_2O_3 gate dielectric surface prior to semiconductor deposition. (c) Corresponding stacked surface line scans (dashed lines). (d) Corresponding height distributions.

Figure 3. (a) Transfer characteristic of a polymer/(6,5) SWNT transistor with L/W of 10/500 µm, fabricated on a rigid substrate. (b) Corresponding output characteristic.

Figure 4. (a) Schematic of the unipolar p-type inverter circuitry used. (b) Voltage transfer characteristic and corresponding static gain of a polymer/(6,5) SWNT unipolar voltage inverter on a rigid substrate, exhibiting a gain of 5.3 V/V while measured at a supply voltage of V_{DD} = -2 V.

The p-type unipolar inverter consists of a driving polymer/(6,5) SWNT transistor with L/W of 20/1400 µm, and one passive load with resistance of 160 kΩ. (c) Transfer characteristic of a polymer/(6,5) SWNT transistor with L/W of 35/280 µm, fabricated on a free-standing flexible polyimide foil. (d) Transfer characteristic of a flexible polymer/(6,5) SWNT transistor with L/W of 35/280 µm, measured while flat and bent to tensile radii R_T of 5 mm and 4 mm. The inset shows a photograph of the actual transistors during testing, while bent to a tensile radius R_T of 4 mm.

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