# Mechanisms for Enhancement of Sensing Performance in CMOS ISFET Arrays using Reactive Ion Etching

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**Abstract**

In this work, we investigate the impact of successively removing the passivation layers of ISFET sensors implemented in a standard CMOS process to improve sensing performance. Reactive ion etching is used as a post-processing technique of the CMOS chips for uniform and accurate etching. The removal of the passivation layers addresses common issues with commercial implementation of ISFET sensors, including pH sensitivity, capacitive attenuation, trapped charge, drift and noise. The process for removing the three standard layers (polyimide, $Si_3N_4$ and $SiO_2$) is tailored to minimise the surface roughness of the sensing layer throughout an array of more than 4000 ISFET sensors. By careful calibration of the plasma recipe we perform material-wise etch steps at the top and middle of the nitride layer and top of the oxide layer. The characterisation of the ISFET array proves that the location of the trapped charge in the passivation layers is mainly at the interface of the layers. Etching to the top of the oxide layer is shown to induce an improvement of 80% in the offset range throughout the array and an increase in SNR of almost 40 dB compared to the non-processed configuration. The performance enhancement demonstrates the benefit of a controlled industry-standard etch process on CMOS ISFET array System-on-Chips.

*Keywords:* CMOS, ISFET, Reactive Ion Etching, ISFET array, Optimal sensing

## 1. Introduction

Ion-Sensitive Field-Effect Transistors (ISFETs) have had increasing success over the past decades as part of analogue front-end topologies for pH sensing [1]. The reason behind this success lies with the compatibility of the sensor with commercial Complementary Metal-Oxide-Semiconductor (CMOS) technology, enabled by extending the device gate to the top metal and using the passivation layer of the process as a sensing membrane to bind ions in solution and generate an electric field detected by the sensor [2]. In particular, certain materials in the standard CMOS passivation stack trap protons at their surface, typically $Si_3N_4$ and $SiO_2$, which provides pH sensitivity to the ISFET. The unmodified CMOS approach benefits from inherent monolithic integration, low cost of silicon implementation, and scalability as stated by Moore's law, without the need for post-processing the chip surface. The emergence and popularity of the ISFET as a CMOS sensor has been initiated by previous work on the well-established integration of a wide range of sensors in CMOS, including image sensors [3], light-emitting devices [4] and Radio-Frequency Micro-Electro-Mechanical Systems (RF-MEMS) [5]. We now leverage on monolithic integration for implementing robust chemical sensors and instrumentation on a microscopic scale.

One of the most successful applications of ISFET sensors involves DNA detection since the binding between nuceleotides releases protons which can be detected as a change in pH. In this context, we have recently demonstrated a platform able to perform fast diagnosis of infectious diseases at the point of care by performing on-chip nuclease amplification and detection on an array with more than 4000 ISFET sensors [6, 7]. Rothberg *et al.* [8] have also

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introduced their 1.2M sensor chip which is the basis of the Ion Torrent technology for genome sequencing, while Toumazou *et al.* [9] reported a system for the detection of DNA amplification focusing on Single Nucleotide Polymorphisms (SNPs).

The full passivation of a standard CMOS process involves three layers with a thickness of several microns : polyimide (PI), silicon nitride ($Si_3N_4$) and silicon dioxide ($SiO_2$), which are usually added at a wafer level for circuit protection and release of mechanical stress. This leads to three drawbacks for proper device operation: 1) the layers are not optimised for sensing and hence contain impurities, 2) the thickness induces signal attenuation and 3) PI, which is the top layer, exhibits low pH sensitivity. Recent papers published using a standard $Si_3N_4$ top passivation layer [6, 10, 11], reporting sensitivity of approximately 10 mV/pH, support the claim that unmodified CMOS technology provides far from ideal sensitivity. This is dictated by the quality of the passivation layer which, in the case of unmodified CMOS, is entirely dependent on the manufacturer and the deposition mechanisms. The technology described in this process relies on Plasma-Enhanced Chemical Vapour Deposition (PECVD) to form the passivation layer, with the main objective to protect circuits from nearby interference. As a result, it is not expected that the layers are optimised to minimise the amount of defects in the passivation, as opposed to several previous works which have been focused on improving the quality of the nitride layer by balancing the composition of gases in the chamber [12]. Overall, the reliance on commercial technology results in sub-optimal performance for a sensing platform.

Our previous work has focused on ISFET instrumentation to improve sensing resolution and compensate for device non-idealities, integrating thousands of sensors in large scale arrays [1, 13, 6]. In parallel, we have also reported our research on molecular methods for on-chip nucleic acid amplification [6, 7]. So far, this has been limited to an unmodified CMOS process. In this work, we deviate from the unprocessed technology by allowing simple techniques to modify the top passivation material and investigate the effect on sensing performance. In particular, we aim to reduce the passivation layer thickness using Reactive Ion Etching (RIE), which is a standard fabrication process technique and can be applied in the back-end of the CMOS process. At the expense of added surface processing, we postulate that this will significantly improve the ISFET as a sensor in systems with critical requirements towards healthcare and diagnostics.

This paper presents the methodology for RIE plasma etching the CMOS passivation layer and provides additional insights into 1) the physical origin and spatial distribution of trapped charge in CMOS ISFETs, which induces threshold voltage offset, 2) the impact of attenuation and its relation to passivation thickness and 3) the improvement in ISFET performance parameters. Using five etching configurations, we present a process for the successive etching of PI and $Si_3N_4$ by calibrating etching parameters including plasma pressure and power, gas flow rate, temperature and etch time for minimum surface roughness and ion implantation. The results of the plasma post-processing on an existing ISFET array-based System-on-Chip (SoC) are presented in terms of sensing parameters, specifically capacitive attenuation, pH sensitivity, offset, drift and noise. Finally, a Figure-of-Merit (FoM) is derived empirically to accurately quantify the trade-off of RIE on the ISFET sensing performance.

## 2. ISFET Sensing Array

### *2.1. Device Structure*

The ISFET is a solid-state sensor structured as a MOSFET with the gate oxide replaced by an insulating membrane and the gate voltage applied through a reference electrode immersed in solution. An extensive review of ISFET structure, behaviour and instrumentation is included in [1], in this section we summarise the main sensor characteristics. The sensor is implemented in unmodified CMOS by extending the gate with stacked vias to the top metal of the process which then defines the sensing area. The structure of the device is depicted in Fig. 1a. We generalise the cross-section for the case of wafer-level designs, where the foundry often imposes an extra layer of polyimide (PI) as part of the passivation layer. PI is typically added as the top passivation layer for its insulation and robustness to mechanical stress across the wafers. The thickness of the PI layer is 4 µm in a typical 0.35 µm process which leads to significantly higher signal attenuation. Additionally, PI is known to demonstrate very low pH sensitivity. Therefore, this layer is very undesirable for chemical sensors and it has been the starting point to justify removing the passivation. The rest of the passivation layer consists in 1 µm of $Si_3N_4$ and 1 µm of $SiO_2$ on top of the last metal layer used for sensing.

*2.2. Sensor Operation*

Fig. 1a presents the behavioural macromodel of the ISFET, where a change in pH is modelled as a shift in the threshold voltage ( as shown in Eq. (1)) of the device using the site-binding model for ions on the insulating membrane [14, 15]. The threshold voltage is shown to be dependent on several potentials following the relationship [16]

$$V_{th(ISFET)} = E_{ref} - \psi_0 + \chi_{sol} - \frac{\phi_m}{q} + V_{th(MOSFET)} \tag{1}$$

The contribution to the ISFET threshold voltage originates from several parameters [14];

- the potential due to the reference electrode $E_{ref}$, which is set to drive the device in proper the operating region;
- the potential due to the existence of dipole molecules in the solution $\chi_{sol}$ ;
- the work function of the metal contact $\phi_m$ divided by the charge of the electron $q$ to yield an equivalent voltage;
- the potential drop at the insulator-electrolyte interface $\psi_0$, which varies with ionic species in solution;
- the threshold voltage of the equivalent MOS transistor $V_{th(MOSFET)}$.

The chemical related terms can be grouped as a potential $V_{chem}$ such that $V_{th(ISFET)} = V_{th(MOSFET)} + V_{chem}$, written as

$$V_{chem} = E_{ref} - \psi_0 + \chi_{sol} - \frac{\phi_m}{q} \tag{2}$$

In Eq. (2), the sensitivity to ionic species is reflected in $\psi_0$, which is governed by two chemical phenomena: the site-binding of insulator and the capacitive double layer. The site-binding model [17] dictates the way that ions in solutions bind to discrete surface sites on the $Si_3N_4$ layer. To characterise the dependence, the effect of ions in solution is modelled as an equivalent capacitance $C_{eq}$, or double layer capacitance, at the surface of the sensor, originating from the combined contributions of a Helmholz plane and a Gouy-Chapman layer [14]. Assuming medium to high value of electrolyte concentration, for which the Gouy-Chapman diffuse layer capacitance can be modelled linearly, the chemical potential can be approximated as

$$\psi_0 = -\frac{\sigma_d}{C_{eq}} \tag{3}$$

where $\sigma_d$ is the charge density in the diffuse layer. In turn $C_{eq}$ can be expressed as

$$\frac{1}{C_{eq}} = 2\frac{kT}{q}\frac{1}{\sqrt{8\varepsilon_w kTc}} + \frac{1}{C_{stern}} \tag{4}$$

where $k$ is the Boltzmann constant, $T$ is the temperature, $\varepsilon_w$ is the dielectric constant of water, $c$ is the concentration of electrolyte in ion pairs/cm$^3$ and $C_{stern}$ is the value of the Stern capacitance associated with the Helmholz plane. Based on the relationship between the proton concentration in solution, reflected by the pH, and the potential $\psi_o$, the equation for surface equilibrium yields the following relationship for the potential drop across the electrolyte [14].

$$\psi_0 = 2.303\frac{kT}{q}\frac{\beta}{\beta+1}(pH_{pzc} - pH) \quad \text{with} \quad \beta = \frac{q^2 N_s \delta}{C_{eq} kT} \tag{5}$$

where $N_s$ is the number of surface sites, $\delta = 2\sqrt{K_a K_b}$ is a parameter dependent on the equilibrium constants for the acid and base reactions at the surface and $pH_{pzc}$ is the pH at which there is no charge at the insulator surface.

As a result, the chemical voltage $V_{chem}$ can be expressed specifically in terms of the pH of the solution [16]

$$V_{chem} = \gamma + \alpha S_N \text{ pH} \tag{6}$$

where $\gamma$ groups all potentials unrelated to ion activity, and $\alpha = \beta/(\beta+1)$ reflects the deviation from the Nernstian sensitivity $S_N = 2.303\ kT/q$. At ambient temperature, the ideal sensitivity is approximated by $S_N \approx 59\ mV$.

Overall, when considering design with an ISFET, there are four physical design parameters highlighted in Fig. 1a which can be adapted to vary sensor operation and performance : 1) passivation material and 2) passivation thickness are process related; 3) sensing area and 4) device dimensions are IC design related. When using unmodified CMOS, 1) and 2) cannot be tuned to optimise sensing performance without post-processing. As a result, the aim of this paper lies with the improvement of ISFET performance while minimising surface processing on sensors implemented in an unmodified CMOS process.

### 2.3. ISFET non-idealities

Non-idealities associated with the use of the ISFET as a sensor may cause its behaviour to deviate from this model. In particular, in this work we consider three sources of non-ideality, all illustrated in Fig. 1a.

#### 2.3.1. Capactive attenuation

In the macromodel of Fig. 1a, it was already mentioned that the additional passivation capacitance due to the implementation in standard CMOS processes led to extra attenuation of the signal. This can be computed as the capacitive division [16]

$$V_{G''} = V_{G'} \frac{C_{pass}}{C_{pass} + (C_{ox}C_d)/(C_{ox} + C_d)} \tag{7}$$

where $C_{ox}$ and $C_d$ are the oxide and depletion capacitances respectively. The passivation capacitance $C_{pass}$ can be approximated by considering the two passivation dielectrics $Si_3N_4$ and $SiO_2$ used for chip insulation, derived as

$$C_{pass} = (WL)_{chem}\varepsilon_0 \frac{\varepsilon_{Si_3N_4}\varepsilon_{SiO_2}}{\varepsilon_{Si_3N_4}t_{SiO_2} + \varepsilon_{SiO_2}t_{Si_3N_4}} \tag{8}$$

with $W$ and $L$ the dimensions of the sensing area, $\varepsilon_0$, $\varepsilon_{Si_3N_4}$ and $\varepsilon_{SiO_2}$ the permittivities of free space, silicon nitride and silicon dioxide respectively, and $t_{Si_3N_4}$ and $t_{SiO_2}$ the passivation thicknesses.

Integrating the sensor as part of a voltage-mode source follower front-end architecture allows to bootstrap the gate-source capacitance. This has been shown to be an efficient technique to compensate for the effect of the passivation capacitance on the output signal [13, 18, 19].

#### 2.3.2. Trapped charge

The definition of trapped charge relates to residual charge at the passivation layers or the floating gate injected during fabrication and without discharging path to ground [16]. Those charges are considered static and occupy energy levels in the bandgap of the material. As such, this effect is dependent on the purity of the material. It is expected that remaining energy levels in the passivation insulators contribute to noise and drift due to dynamic charge exchange.

On a device level, trapped charge generates an offset in the threshold voltage of each device [1]. This offset drives some pixels out of readout range and induces a mismatch in device behaviour throughout an array with millions of sensors, which sets constraint requirements on the dynamic range of the Analogue-to-Digital Converter (ADC) for output quantisation when scaling the system up to millions of pixels.

#### 2.3.3. Drift

Drift is exhibited through a slow monotonic change in the threshold voltage of the ISFET and originates from a transport phenomenon at the interface between the insulator and the solution, [20], related to buried surface sites or dangling bonds at the solid-liquid interface [21]. It is hypothesised that as the top surface of the passivation undergoes a slow hydration process, ionic species in solution disperse through the reactive layer and bind to buried surface sites and dangling bonds at the interface. In turn this causes residual charge to gradually occupy energy levels in the bandgap of the insulators. It is expected that the surface insulator provides a dominant contribution to this effect. This process is dynamic, although its frequency is typically in the low range.

An initial model for drift has been established by Jamasb *et al.* [20] in a device operating in the feedback mode with a constant current biasing i.e. where the reading is performed from the reference electrode voltage $V_{ref}$. Following the model, the slow change in capacitance due to the hydration of the passivation surface results in an equivalent change in gate voltage following

$$\Delta V_{drift} = -(Q_D + Q_I + Q_{inv}) \left( \frac{\varepsilon_{ins} - \varepsilon_{sl}}{\varepsilon_{ins}\varepsilon_{sl}} \right) x_{sl}(t) \tag{9}$$

where $Q_D$, $Q_I$ and $Q_{inv}$ represent the effective charge per unit area respectively induced in the depletion layer, in the insulator, and the inversion charge, $\varepsilon_{ins}$ and $\varepsilon_{sl}$ are the permittivities of the insulator and the surface-liquid interface respectively, and $x_{sl}$ is the thickness of the hydration layer. The relationship highlights the proportionality between this thickness and the drift voltage. Following Flick's law of diffusion, the latter thickness can be expressed depending on the time constant of the dispersive transport process [22].

$$x_{sl}(t) = x_{sl}(\infty) \left\{ 1 - \exp\left[ -(t/\tau)^{\beta} \right] \right\} \tag{10}$$

where $x_{sl}(\infty)$ is the final thickness of the hydration layer. This supports the exponential relationship of time generally observed when sampling drift. The same author has then quantified the variation as an average drift rate of 8.1 mV/min for the first minute [23].

Despite deriving a first approximation of the drifting process, the main challenge remains its unpredictable behaviour in terms of direction and drift rate. It has indeed been shown that drift depends on several factors, such as the solution pH, the surface material and the device size [24].

### *2.4. Noise*

Sensor noise ranges from low to high frequencies and is due to both chemical surface effects and device physics. Similarly to drift, the chemical noise contribution originates from energy levels of the insulator catching and releasing charge at several frequencies, generating both flicker (1/f) and thermal noise. This effect degrades the limit of detection for the sensor [25]. Overall, the noise has been expressed as shown in Eq. (11)

$$\bar{V_n^2} = \overline{V_n^2(MOSFET)} + \overline{V_n^2(Chem)} = \left(\frac{C_{pass} + C_{MOSFET}}{C_{pass}}\right)^2 \frac{K_f}{WLC'_{ox}f} + \frac{K}{f} \tag{11}$$

where $C_{MOSFET}$ is the equivalent MOSFET capacitance between the floating gate and ground, $K_f$ is the constant associated with flicker noise and K is the constant representing the long-term electrode degradation and surface chemical noise [25].

### *2.5. Sensor enhancement*

#### *2.5.1. Instrumentation*

So far, attempts have been made to counteract ISFET non-idealities by picking specific front-end instrumentation, and an exhaustive description of the most popular implementations has been included in our review [1]. For instance, a voltage-mode source follower architecture compensates for signal attenuation by bootstrapping the gate-source capacitance of the ISFET [26, 13]. Additionally, sensor offset can be modulated using several techniques which all present advantages and inconveniences. These include 1) adding a control voltage to the floating gate through a capacitor (designated as Programme Gate- or PG-ISFET) [27] at the expense of sensitivity reduction due to extra capacitive division of the signal, 2) performing reset through a switch [19] but with increased drift during readout due to leakage and 3) adapting the source voltage consequently to fix $V_{gs}$ [6] with the condition that the trapped charge is maintained in a narrow range of 1 V throughout the array.

#### *2.5.2. Physical modifications*

These methods have been demonstrated as part of large sensor arrays. However, they have reached a limit in terms of sensor performance which can only be pushed by modifying the physical structure of the chip surface. Looking at the ISFET model of Fig. 1a, signal attenuation can be improved by maximising the passivation capacitance $C_{pass}$. This can be achieved by 1) increasing the sensing area which has been discussed as an opportunity to include more digital processing in-pixel [28], 2) choosing a material with higher permittivity which is not under our control with the material provided as passivation and 3) decreasing the layer thickness. In this paper, we will attempt to characterise the effect of 3) on attenuation and pH sensitivity, which are correlated, as well as offset, drift and noise performance.

### *2.6. Lab-on-Chip platform*

Fig. 1b shows a microphotograph of the sensing chip, consisting of an array of 78x56 sensors introduced in [6]. Each pixel contains an analogue sensing front-end which quantises the signal internally and converts it in the time domain. Compensation of the offset due to trapped charge can be performed by tuning the source voltage $V_s$ of the ISFET, which is stored in the 10-bit Random-Access Memory (RAM) inside each pixel. An on-chip Time-to-Digital Converter (TDC) then provides a 16-bit output to the Serial Peripheral Interface (SPI) module.

The die is glued, bonded and encapsulated using glob-top epoxy on a small cartridge which is plugged onto the motherboard as shown in Fig. 2 The motherboard also contains the power module, biasing circuits and microcontroller. The latter handles calibration and readout, and sends the data through UART to a MatLab GUI.

A flow cell is clamped to seal the liquid at the surface of the chip and allow for a flow of pH buffer solutions. A chlorinated silver wire is used as an Ag/AgCl electrode to bias the sensors in the array.

## 3. Experimental Methods

### *3.1. Reactive Ion Etching*

We consider Reactive Ion Etching (RIE) for 1) its ease of implementation and post-processing in the context of surface etching of a CMOS chip and 2) its high precision and controllable etch rate compared to wet chemical etching.

Nevertheless, with plasma post-processing the resulting roughness of surface will vary and this will affect the performance of the ISFET. A rough top surface implies larger surface area, larger number of ion traps and longer overetch time to achieve the desired passivation thickness [29, 30, 31, 32]. These characteristics manifest larger passivation capacitance (according to the parallel plate capacitor model), larger chemical noise at the surface and larger trapped charge due to overetch with ion bombardment and implantation, respectively [33, 34, 35]. The increase of the passivation capacitance due to larger surface area is negligible compared to the increase by thinning of the insulating layers. Therefore, we hypothesise that using an RIE process that decreases the roughness of the surface would reduce trapped charge and noise together with decreasing capacitive attenuation.

To achieve a smooth surface we can use the passivation materials as etch stop layers and promote isotropic etching by varying the parameters of the plasma. RIE induces two types of etching: 1) chemical etching that occurs from the reaction of the ion species in the gas and the chip surface and 2) physical etching that happens from the ions transferring their kinetic energy and causing strong physical sputtering. The latter is mostly anisotropic due to mechanical bombardment perpendicular to the sample and as a consequence has poor material selectivity. Therefore, we need to promote chemical etching.

Achieving complete isolation of the etch method, i.e. only chemical or only physical, is nearly impossible. However, with increased plasma pressure (typically more than 50 mTorr [36]) there is more gas in the chamber, more collisions and scattering and less electron mean-free-path [37] and with lower RF power the DC bias and ion energy decrease, thus chemical etching dominates over sputtering. Additionally, to be able to etch a material with the plasma, volatile gases/compounds need to be formed during the process. So, the gas choice (reactive species: $O_2$, F, Cl etc.) is crucial and depends on the material to be etched.

### *3.2. Methodology*

In previous work on ISFETs [38], one etch step is used to remove all three layers. In this work, material-based step-wise etching of the passivation layers will be developed. Since, the polyimide layer is significantly less sensitive to pH than the nitride and oxide layers, it needs to be removed completely before testing the ISFETs. Subsequently, the pH sensitive layers ($Si_3N_4$ and $SiO_2$) will be thinned and ISFET testing will be performed on the top and at the middle of the nitride layer and at the top of the oxide layer.

### *3.3. Polyimide etch*

#### *3.3.1. Gas choice*

The polyimide is the thickest of the passivation layers and we are mostly interested in the texture of the surface left after removing it. So, the driving parameter for the choice of RIE process parameters is the surface roughness and material selectivity. Polyimide can be etched in pure oxygen plasma by oxidation of the hydrocarbon because volatile carbonyls and water are formed [39], or a combination of $O_2$ with fluorine containing gases such as $CF_4$ or $SF_6$ [40, 41, 42, 39]. Thus, the main etchants of polyimide are atomic oxygen and fluorine [40, 41]. $SF_6$ prevents the oxidation of the hydrocarbon since it makes stronger bonds (C-F) than oxygen (C-O) and will slow down the sputtering process, while promoting chemical etching and thus reduces the surface roughness [43]. However, adding F atoms in the plasma will etch $Si_3N_4$ too [38, 44, 45, 46, 47, 48]. This is not desired because it will eliminate material selectivity. Therefore, $O_2$ plasma is used and the surface roughness will be minimised by controlling the RF power and plasma pressure.

#### *3.3.2. Parameter calibration*

The flow rate and temperature are set constant at 50 sccm and 20 $^oC$, respectively, while the power and pressure are varied following the fractional-factorial method [49]. Power and pressure calibration were performed for 3 min post-processing in the plasma etcher 'Plasmalab 80 Plus' from 'Oxford Instruments PLC'. For each process parameter combination we calculate the average surface roughness using a Veeco Wyko NT9100 interferometer. Etch rate is

calculated by taking the ratio of the step from the contact pads to the top of the passivation layers, measured using a Veeco surface profilometer DekTak, and the etch time. Table 1 shows the average results from four measurement points on two dies. This approach will give a good first order approximation of the etch depth homogeneity.

The roughness of the CMOS dies before RIE processing has an average value of 47 nm and the 3D surface of one ISFET gate as measured with the interferometer is shown in Fig. 3a.

#### *3.3.3. Etch evaluation*

Table 1 shows that power and pressure have opposite effect on the DC bias which defines the kinetic energy of the ions in the plasma. That is, DC bias is proportional to RF power and inversely proportional to pressure, independently. When power is at 50 W, the effect of pressure is not significant. By performing two-way analysis of variance (ANOVA) in MATALB on Table 1, the conclusion is that the effect of power on the DC bias is much larger than that of pressure.

Table 1 also shows the etch rate as function of power and pressure. The effect of pressure changes according to the value of power. For 50 W, the etch rate is maximum at 150 mTorr but stays relatively unchanged with pressure when the power is at 100 W. Increasing the power to 150 W, the etch rate decreases with increasing pressure. This is a consequence of the DC bias which decreases with pressure. The plasma ions experience less scattering events when the plasma pressure is low, which results in less energy lost and hence higher impact on the surface to be etched. Therefore, more anisotropic and physical etching is achieved, increasing the etch rate.

Finally, table 1 shows the effect of RF power and plasma pressure on the surface roughness. When power or pressure are at their lowest value, the effect of the other parameter is minimal. Increasing one parameter increases the effect of the other, i.e. the effect of power on the roughness is more severe when the value of pressure is high and vice versa. Hence, to reduce the surface roughness after etching the polyimide layer, we need to choose a plasma pressure less than 150 mTorr.

#### *3.3.4. Final recipe*

To choose which value of power and pressure to use for the polyimide etch for minimum roughness and relatively fast etching, we calculate the percentage gain between the smallest roughness and maximum etch rate combinations. Based on the conclusions from Table 1, the recipe for the smoothest surface is 100 W and 50 mTorr and for the maximum etch rate 150 W at 50 mTorr. The recipe for highest etch rate comes at a cost of 13% loss in smoothness and for minimum roughness at a cost of 154% slower etch rate. Hence, the best recipe for fast etch rate and relatively smooth surface is 150 W and 50 mTorr in a 100% $O_2$ plasma at 50 sccm flow rate and temperature 20$^o$C.

This recipe has an etch rate 320 nm per minute. Hence, we need 12.5 min etch time for 4 µm of PI. However, the etch rate is not constant and to etch all the PI layer we etched for 18 min. To test the selectivity of the recipe, we etched for 25 min. The plasma did not affect the nitride layer underneath the PI apart from negligible increase in roughness. Thus, the oxygen plasma with the selected parameters gives excellent selectivity of the polyimide over the nitride layers. The 3D surface of one ISFET gate after 18 min of etching the polyimide is shown in Fig. 3b with average roughness 28 nm.

### *3.4. Nitride Etch*

#### *3.4.1. Gas choice*

As mentioned before, the $Si_3N_4$ layer can be etched in $O_2$ and $SF_6$ plasma [39]. We use two-level factorial investigation on the effect of power and pressure of the plasma while keeping gas composition (25 sccm $O_2$ : 25 sccm $SF_6$) and temperature (20 $^o$C) constant.

#### *3.4.2. Parameter calibration*

The DC voltage, roughness and etch rate are determined for 3 minutes etch for different power and pressure settings. The results are summarised in Table 2. Increasing power increases the DC bias but at the same time, low pressure also increases DC bias. For high power (150 W) the etch rate is more than 300 nm/min which means that after 3 min of etching, all the nitride is removed completely. This recipe gives some selectivity over the oxide layer beneath the nitride and hence a smoother surface is achieved than not having an etch stop layer.

For lower power values ($<$150 W), not all nitride layer is removed due to smaller etch rate. The remaining nitride layer is rougher for higher pressure values. This result is similar to that for etching polyimide. The roughness increases with pressure between 50 to 150 mTorr for 50 W power (Table 2).

*3.4.3. Final recipe*

To control the etch depth in $Si_3N_4$, the recipe with the smallest etch rate is chosen. Process parameters of 50 W and 50 mT also result in a relatively smooth surface. The etch rate is 212 nm/min. Etching for 3 min removes 600 nm and the result in surface roughness 77 nm (Fig. 3c). This roughness is larger than the 28 nm obtained after the polyimide removal with $Si_3N_4$ as etch stop layer. To remove the nitride layer completely, process parameters of 150 W, 150 mTorr, 25 sccm $O_2$, 25 sccm $SF_6$ at 20 $^o$C are chosen. This process is selective and stops on the $SiO_2$ layer after a 2 min etch, leaving a surface roughness of only 11 nm (Fig. 3d).

The etch selectivity of the fast $Si_3N_4$ etch recipe compared to $SiO_2$ etch, was found to be 18:1 by overetching the $Si_3N_4$ layer for 18 min. This results in a removal of 500 nm of $SiO_2$ and final average surface roughness of 63 nm.

*3.5. Summary*

All the RIE recipes used for each material and measured results for each recipe are summarised in Table 3 and Table 4, respectively. The smoothest surfaces are those obtained by the selective recipes with etch stop layers.

## 4. Results and Discussion

To characterise the effect of etching on sensing performance and compare the four chip configurations, we consider the following performance parameters : 1) capacitive attenuation, 2) pH sensitivity, 3) trapped charge, 4) drift and 5) noise. A Figure of Merit (FoM) is defined in Eq. (14) as a function of these five parameters and summarises the impact of all effects on the ISFET performance.

*4.1. Capacitive attenuation*

*Method.* The capacitive attenuation is the inverse of the scaling factor between the voltages at node G' and G" as defined in Eq. (7). To characterise its value across all etching configurations, the chip is exposed to a solution of pH 7 and the reference electrode voltage $V_{ref}$ in varied steps of 100 mV. The measured output source voltage indicates the scaling factor in units of V/V.

*Results.* As expected, $G_{pass}$ increases from 0.26 to 0.79 upon removal of the PI layer, whilst removing the $Si_3N_4$ layer increases this gain to 0.91. The ISFET-to-ISFET deviation in the array as a consequence of etch non-uniformity is highlighted in Fig. 4. We notice negligible influence of the standard deviation to the etch process.

*4.2. pH sensitivity*

*Method.* To test pH sensitivity, electrolyte buffers are sequentially flown on top of the sensing array using a flow cell, in the order pH 7-10-7-4-7. Drift is subtracted for the characterisation. The pH sensitivity is then defined as the equivalent change of floating gate voltage $V_{g''}$ as a result of a unit change in pH.

$$\mathrm{V_{g'',pH}} = \frac{\mathrm{dV_{g''}}}{\mathrm{dpH}} \tag{12}$$

*Results.* To highlight the correlation between the attenuation and the pH sensitivity, both are shown in Fig. 5. The top PI indeed exhibits nearly no pH sensitivity which is expected due to the low pH selectivity of the layer. Mid nitride and top oxide show the opposite scenario, with low attenuation and high pH sensitivity. When etched until the top of the nitride, which is another typical case of unmodified CMOS passivation surface, the chip exhibits low attenuation and low pH sensitivity. This is expected to originate from the residues of PI at the surface which do not allow for proton binding and hence limit the pH sensitivity.

*4.3. Trapped charge*

*Method.* To quantify the trapped charge, we vary the reference voltage $V_{ref}$ for the entire array from -10 V to 10 V and measure the resulting change in source voltage. For this particular case, we define the trapped charge voltage $V_{tc}$ as the voltage $V_{ref}$ at which the output is half the range i.e. 512 mV.

*Results.* The results are arranged as histograms in Fig. 6. Improvements are highlighted in terms of the offset range $\Delta V_{tc}$, which is the limiting factor for the instrumentation. Indeed variations in the absolute value $V_{tc}$ can be alleviated by adapting the reference electrode voltage $V_{ref}$. We demonstrate a significant reduction of 80% of the offset range, leading to a low $\Delta V_{tc}$ of 0.27 V for the top oxide configuration.

The offset range is shown to reduce when the interface changes and not at middle of the nitride layer. This observation confirms the hypothesis that residual charges are mostly trapped at the interface between passivation layers [16].

### *4.4. Drift*

*Method.* To characterise drift, the chips are exposed to pH 7 buffer for 2 hours. This has the effect of establishing a dynamic equilibrium between the chip surface and the solution. The rate of change referred back to the floating gate voltage is then defined as the drift voltage $V_{drift}$.

$$V_{drift} = \left( \frac{dV_{g''}}{dt} \right)_{pH=7} \tag{13}$$

*Results.* All chips exhibit on average decreased output drift as highlighted by the histograms of Fig 7. The drift rate on each configuration matches the trend set by the surface roughness as expected, and the top oxide surface leads to the lowest drift rate with more than half the drift of the non-etched prototype. The correlation between surface roughness and signal drift relates to the physical mechanism of drift, involving dangling bonds following hydration of the top surface layer [21]. Roughness increases the surface area and thus the number of sites for residual charge at the chip-solution interface and therefore, increases drift rate. A similar conclusion is drawn for the deviation of drift rate in the array decreasing with etching, with more than 100% deviation in the case of top PI and top oxide.

### *4.5. Noise*

*Method.* To measure noise, we sample the chip output at a constant bias and in a pH 7 buffer solution. To improve frame rate we consider a sub-array of 13x10 pixels, which allows better resolution in the high frequency spectrum.

*Results.* Fig. 8 shows the average curves for the 130 pixels in each etching configuration. The noise is generally shown to decrease with etching of the passivation layer, with the flicker noise particularly affected. The latter is associated with a similar phenomenon to drift, i.e. capture and release of charge at the interface, hence the behaviour is similarly directly related to surface roughness which decreases with etching. Flicker noise also originates from traps in the insulator of the MOSFET [50]. In this case, the passivation layer is bombarded with high energy ions in the plasma which damage the exposed surface by implantation [51, 52, 53]. The implanted ions penetrate the surface for a few nanometers and create charge traps in the band gap of the exposed material [33, 35]. The implanted ions' contribution to the voltage offset is negligible but the traps and surface damage add noise to the ISFET. With the aid of etch stop layers and highly selective plasma recipes, the post-processing of the chips at the top nitride and top oxide steps shows reduced noise due to smoother surface and fewer ion implantation than the middle of the nitride where there is no etch stop layer. The white noise follows a similar trend to the flicker noise which further improves the noise performance. Along with improved sensitivity, this is a significant benefit of applying RIE on the ISFET array.

Considering the pH sensitivity and the resolution, etching has allowed to boost SNR from 15.3 dB for the full PI passivation to 54.2 dB for the oxide exposed chip i.e. almost a 40 dB improvement has been achieved.

### *4.6. Figure of merit*

Table 5 summarises the performance parameters of the ISFET array after each etch step. This demonstrates the benefit of removing the insulation layers down to the oxide via selective etch steps. To quantify the trade-off of the RIE process on the CMOS ISFET performance, we define a Figure-of-Merit (FoM) as follows.

$$\mathrm{FoM} = \frac{\mathrm{G_{pass}} \times \mathrm{V_{g'',pH}}}{\Delta \mathrm{V_{tc}} \times \mathrm{V_{drift}} \times \bar{\mathrm{V}}_{\mathrm{n}}} \tag{14}$$

The FoM includes all the parameters described previously.

Overall, etching improves performance except for the mid nitride whose roughness and ion implantation induces a significant rise in chemical drift and noise which corrupts the signal more than the top nitride configuration. The top oxide chip achieves a performance better by three orders of magnitude, corresponding to a low offset range, attenuation, drift and noise floor. Therefore, the etching has indeed improved sensing performance of the ISFET array. Additional spatial considerations are provided are described in Appendix A, where it is highlighted that the deviation in sensing metrics are due to 1) pixel regions exhibiting discrepancies in the non-processed configuration originating from the chip fabrication and 2) slight array non-uniformity following etching.

## 5. Conclusion

In this work, we have developed an RIE process to thin down the polyimide and $Si_3N_4$ passivation layers of commercial CMOS ISFET sensor arrays uniformly and accurately. We have highlighted the methodology for calibrating and designing plasma recipes for each material to be etched selectively and achieve optimal surface roughness. For the latter, we have taken advantage of etch stop layers in the passivation, also minimising ion implantation by the plasma for better sensing, trapped charge, noise and drift performance of the ISFETs. With the etching of the passivation layers we were able to identify the spatial distribution of the trapped charge during fabrication which was found to be mostly at the interface between the material layers.

We have demonstrated a significant improvement in sensing performance of the ISFET sensing array, including a 62% reduction in drift, 80% decrease in sensor offset range and quasi 40 dB increase in SNR. These results highlight new surface processing methodologies which go hand-in-hand with the recent research in analogue front-end instrumentation to design an ISFET-based array platform with optimal sensing performance. It is expected that such a process can be streamlined as part of CMOS post-processing steps and used in ion imaging applications requiring high resolution sensing.

## 6. Acknowledgements

The authors would like to sincerely thank Dr. S. Wright, Dr. M. M. Ahmad, Prof R. R. A. Syms and Ms. K. M. Szostak for helpful advice and guidance. N. Moser and C. Panteli are fully funded by Engineering and Physical Sciences Research Council (EPSRC) doctoral training award.

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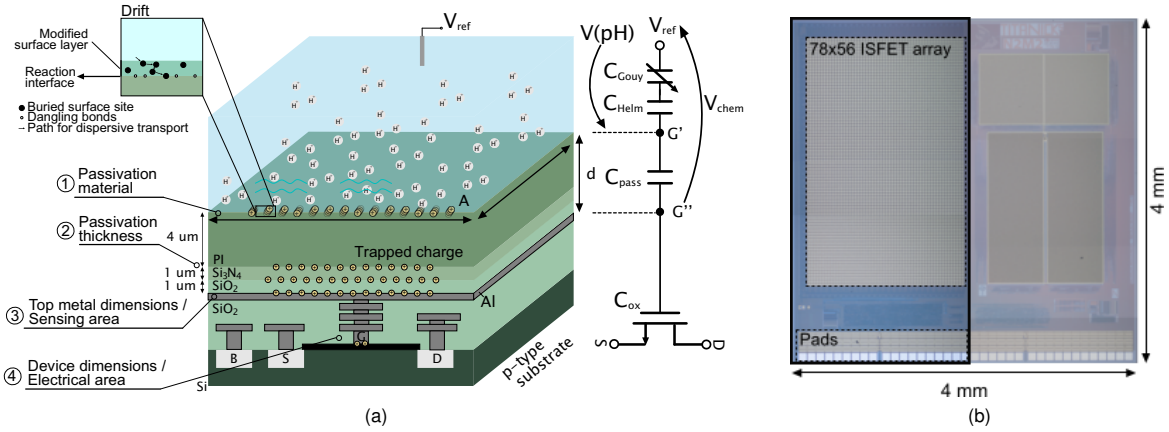



Figure 1: (a) Generalised ISFET cross-section and equivalent macromodel [1] highlighting the passivation capacitance $C_{pass}$. Maximising the capacitance is achieved by increasing the sensing area $A$, decreasing the passivation thickness $d$ or changing the material for improved permittivity. (b) Microphotograph of the CMOS chip highlighting the 78x56 ISFET array with bonpads at the bottom for ease of bonding and encapsulation.

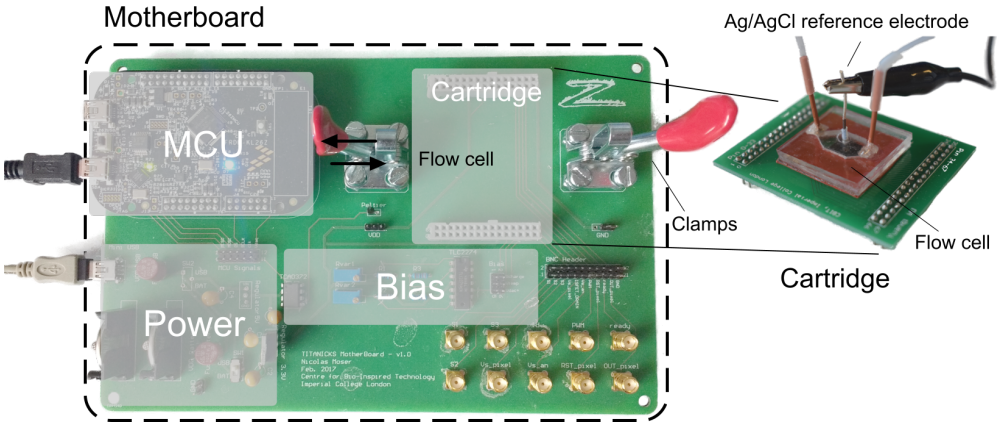



Figure 2: PCB platform and cartridge for the testing of the ISFET array.

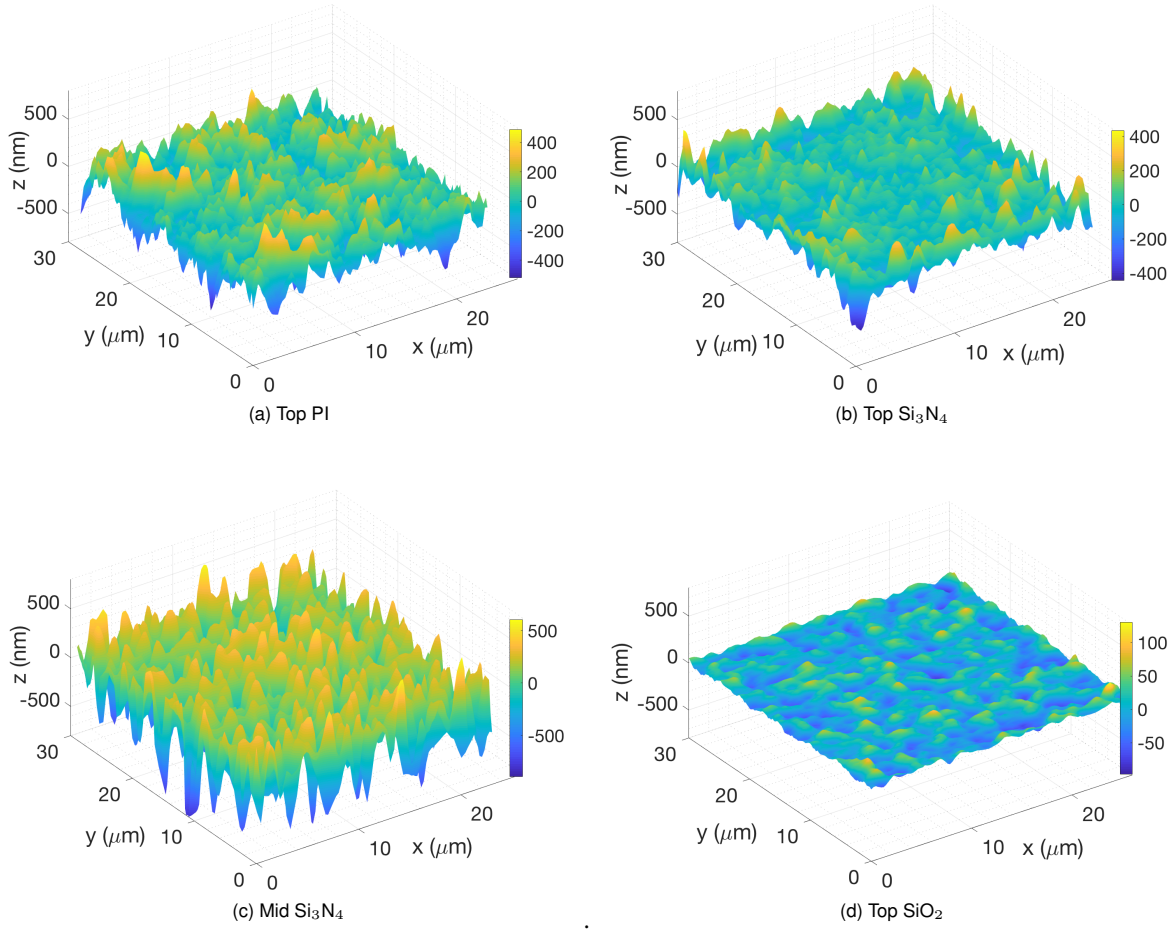



Figure 3: Interferometer measurement gives 3D surface roughness of the ISFET gate at each step of the etch (a) Top of Polyimide. (b) Top of $Si_3N_4$. (c) Middle of $Si_3N_4$. (d) Top of $SiO_2$

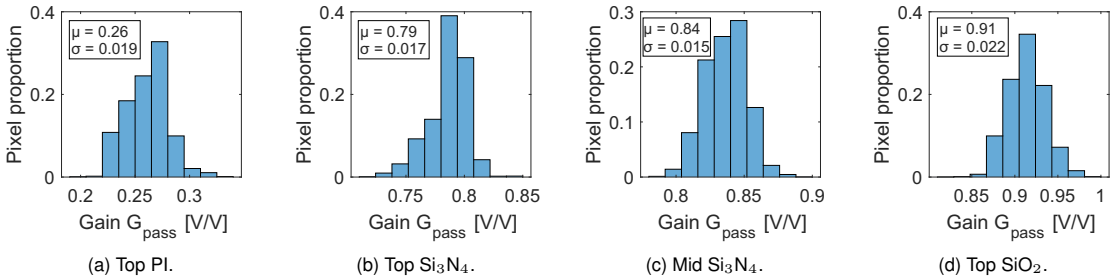



Figure 4: Histograms of the capacitive gain $G_{pass}$ throughout the array for all etching configurations. The average gain increases for decreasing passivation thickness following RIE.

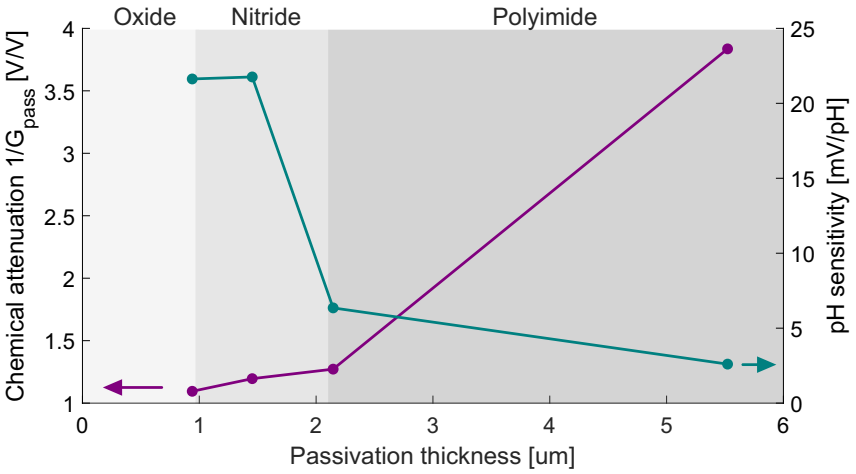
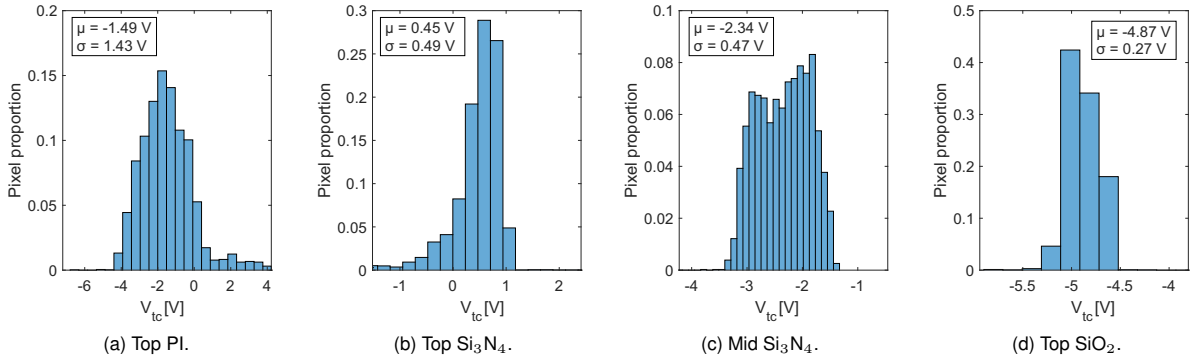
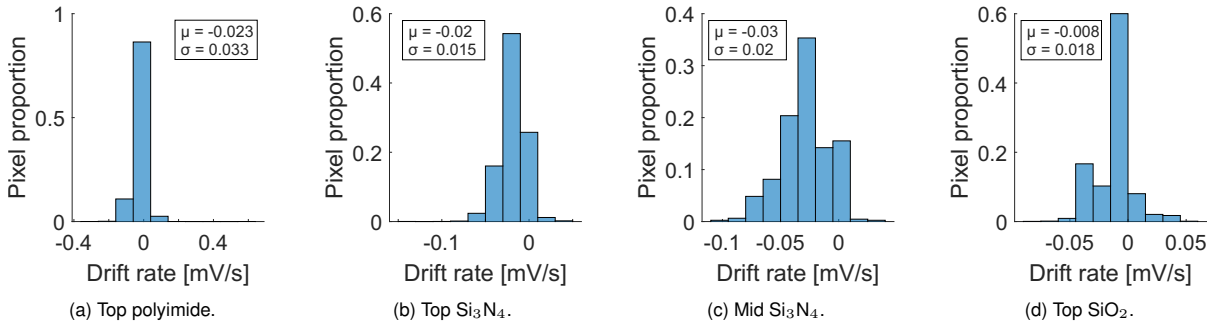



Figure 5: Average chemical attenuation $1/G_{pass}$ and pH sensitivity for each passivation thickness. The two metrics are shown to inversely correlate with etching except for the top nitride configuration.




(a) Top PI. (b) Top $Si_3N_4$. (c) Mid $Si_3N_4$. (d) Top $SiO_2$.

Figure 6: Evolution of offset voltage associated with trapped charge in the array with etching. We demonstrate steady decrease in range with etching.




(a) Top polyimide. (b) Top $Si_3N_4$. (c) Mid $Si_3N_4$. (d) Top $SiO_2$.

Figure 7: Histograms of the drift voltage $V_{drift}$ throughout the array for all etching configurations. Once again, etching is shown to decrease the predominance of drift in the sensor data.

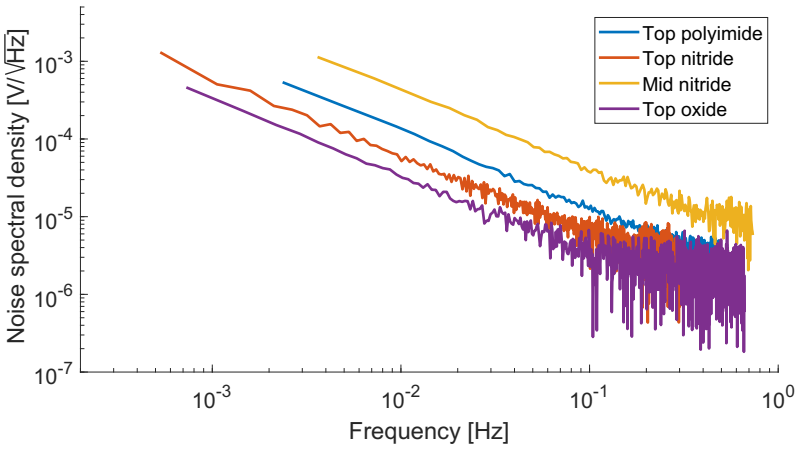



Figure 8: Noise spectral density for each etching configuration. The noise is shown to reduce with more etched surface.

| Pressure (mTorr) | Power (W) | | |
|---|---|---|---|
| | 50 | 100 | 150 |
| 50 | (a) 192 V<br>(b) 65.49 nm/min<br>(c) 5.49 nm | (a) 304 V<br>(b) 126.2 nm/min<br>(c) 4.9 nm | (a) 395 V<br>(b) 320.5 nm/min<br>(c) 5.57 nm |
| 100 | (a) 165 V<br>(b) 79.13 nm/min<br>(c) 5.12 nm | (a) 269 V<br>(b) 148.1 nm/min<br>(c) 5.75 nm | (a) 379 V<br>(b) 265.9 nm/min<br>(c) 6.20 nm |
| 150 | (a) 133 V<br>(b) 105.2 nm/min<br>(c) 5.76 nm | (a) 244 V<br>(b) 128.9 nm/min<br>(c) 6.26 nm | (a) 362 V<br>(b) 225.5 nm/min<br>(c) 6.30 nm |
| 200 | (a) 119 V<br>(b) 26.78 nm/min<br>(c) 5.42 nm | (a) 258 V<br>(b) 79.84 nm/min<br>(c) 7.70 nm | (a) 345 V<br>(b) 207.2 nm/min<br>(c) 8.11 nm |

Table 1: (a) DC bias, (b) Etch Rate and (c) Roughness as function of power and pressure for PI etch recipe after etching for 3 min.

| Pressure (mTorr) | Power (W) | | |
|---|---|---|---|
| | 50 | 100 | 150 |
| 50 | (a) 108 V<br>(b) 175.9 nm/min<br>(c) 43 nm | - | (a) 320 V<br>(b) 339.3 nm/min<br>(c) 16.5 nm |
| 100 | - | (a) 113 V<br>(b) 268.8 nm/min<br>(c) 122 nm | - |
| 150 | (a) 14 V<br>(b) 213.4 nm/min<br>(c) 219 nm | - | (a) 122 V<br>(b) 342.9 nm/min<br>(c) 15 nm |

Table 2: (a) DC bias, (b) Etch Rate and (c) Roughness as function of power and pressure for nitride etch recipe after etching for 3 min.

| Chip | Surface | Gas | Power [W] | Pressure [mTorr] | Flow rate [sscm] | Temp [$^{o}$C] | Time [mins] |
|---|---|---|---|---|---|---|---|
| 1 | Top PI | - | - | - | - | - | - |
| 2 | Top $Si_3N_4$ | $O_2$ | 150 | 50 | 50 | 20 | 22 |
| 3 | Mid $Si_3N_4$ | $O_2$, $SF_6$ | 150 | 150 | 25, 25 | 20 | 3 |
| 4 | Top $SiO_2$ | $O_2$, $SF_6$ | 150 | 150 | 25, 25 | 20 | 2 |

Table 3: Etching parameters for the optimal etching of each configuration. The recipe has been optimised to minimise surface roughness.

| Chip | Surface | Thickness [µm] | Etch rate [nm/min] | Pixel roughness [nm] | Array roughness [nm ] |
|---|---|---|---|---|---|
| 1 | Top PI | 5.5 | - | 47 | 98.4 |
| 2 | Top $Si_3N_4$ | 2.1 | 220 | 28 | 94.8 |
| 3 | Mid $Si_3N_4$ | 1.45 | 212 | 77 | 107 |
| 4 | Top $SiO_2$ | 0.95 | 300 | 10.6 | 92.2 |

Table 4: Measured results for the etching recipe of each layer. The results are obtained from the profiler and the interferometer.

| | Gain $G_{pass}$ [V/V] | pH sens [mV/pH] | Offset range $\Delta V_{tc}$ [V] | Drift rate [mV/s] | Noise $\bar{V}_n$ [µV] | FoM [dB] |
|---|---|---|---|---|---|---|
| **Top PI** | 0.26 | 2.6 | 1.43 | -22.7 | 115.9 | -37.46 |
| **Top $Si_3N_4$** | 0.79 | 6.35 | 0.49 | -19.6 | 90.8 | -22.4 |
| **Mid $Si_3N_4$** | 0.84 | 21.76 | 0.47 | -29.4 | 519.5 | -25.94 |
| **Top $SiO_2$** | 0.91 | 21.62 | 0.27 | -8.53 | 38.5 | -6.54 |

Table 5: Summary of sensing performance for each etching configuration with the Figure of Merit as a metric for comparison. The FoM confirms the significant improvement of the top oxide configuration over the unprocessed device.

## Appendix A. Spatial effects

Fig. A.9 illustrates the spatial variation of each performance parameters throughout the array. Spatial effects are highlighted on the top polyimide passivation due to the fabrication process which affect the deviation of parameters, including an offset of 3 V and a larger attenuation. This strengthens the case of etching to remove dependency of our sensors on all the deposition process and its defects.

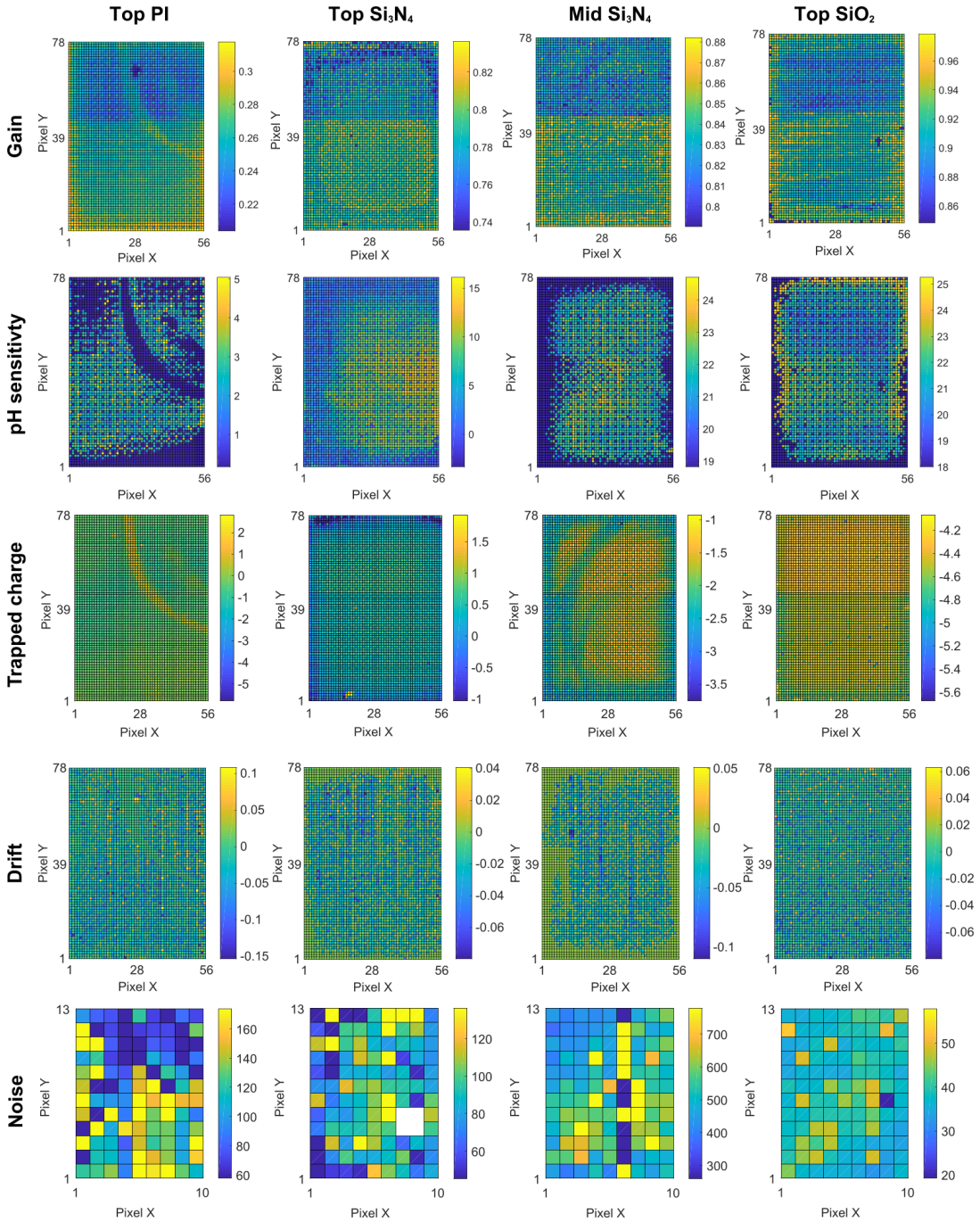



Figure A.9: Spatial variation of each performance parameter throughout the array. The metrics are correlated and generally show additional spatial non-uniformities up to the top oxide configuration. The scale for each plot is centred around the array mean μand spans on a range of 6 $\sigma$.