

Robust Low Power CMOS Methodologies for ISFETs Instrumentation

by

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To God,
my family,
friends,
JOHNNY, and MANNA

Abstract

I have developed a robust design methodology in a $0.18\ \mu\text{m}$ commercial CMOS process to circumvent the performance issues of the integrated Ions Sensitive Field Effect Transistor (ISFET) for pH detection. In circuit design, I have developed frequency domain signal processing, which transforms pH information into a frequency modulated signal. The frequency modulated signal is subsequently digitized and encoded into a bit-stream of data. The architecture of the instrumentation system consists of a) A novel front-end averaging amplifier to interface an array of ISFETs for converting pH into a voltage signal, b) A high linear voltage controlled oscillator for converting the voltage signal into a frequency modulated signal, and c) Digital gates for digitizing and differentiating the frequency modulated signal into an output bit-stream. The output bit stream is indistinguishable to a 1st order sigma delta modulation, whose noise floor is shaped by +20dB/decade.

The fabricated instrumentation system has a dimension of $1565\ \mu\text{m} \times 1565\ \mu\text{m}$. The chip responds linearly to the pH in a chemical solution and produces a digital output, with up to an 8-bit accuracy. Most importantly, the fabricated chips do not need any post-CMOS processing for neutralizing any trapped-charged effect, which can modulate on-chip ISFETs' threshold voltages into atypical values. As compared to other ISFET-related works in the literature, the instrumentation system proposed in this thesis can cope with the mismatched ISFETs on chip for analogue-to-digital conversions. The design methodology is thus very accurate and robust for chemical sensing.

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Introduction

There have been tremendous activities recently in both academic and industrial research on solid state chemical sensor applications, especially in areas related to healthcare. For instances, progress have been made to bring portable blood glucose monitoring systems [1], DNA sequencings [2], [3], brain pH monitoring [4], gastrointestinal (GI) tract pH monitoring [5], and many more. The fundamental to these studies is the application of the Ion-Sensitive Field Effect Transistor (ISFET), which was invented by Bergveld in 1970 [6]. The ISFET is a solid state pH-sensitive field effect transistor (FET) whose threshold voltage can be modulated by a change in the concentration of hydrogen ions over the ion-sensitive membrane. By depositing specific chemicals onto the ion-sensitive membrane, glucose sensors [7], DNA sensors [8], and many other types of chemical sensors can be realized in standard CMOS technologies.

Perhaps the question of whether or not the ISFETs and their electronic frontend interface should be integrated into a common substrate is still up for a debate [6]. But surely the integration of ISFETs into a single CMOS platform can attain a better signal to noise ratio (SNR) because such the integration minimize the space between the sensors and the electronic so that any noise sources cannot be coupled to the integrated system easily. In addition, the integration in CMOS provides a low cost, mass producible option which facilitates the development of disposable electronics for used in the chemical bionics [9]. Because of these advantages, this thesis supports the development of an integrated ISFETs instrumentation system, using unmodified commercial CMOS technologies.

A. Research Objective

The aim of this thesis is to investigate robust design methodologies to help circumvent a number of common performance issues, such as the accuracy and the trapped charges, encountered in the conventional ISFETs instrumentation systems in standard CMOS processes. To enhance the reliability of using ISFETs for pH measurement, this thesis proposes an array of 64 on-chip ISFETs such that any abnormality of the few ISFETs within the array will not affect the system's functionality.

The array of the on-chip ISFETs is directly interfaced with an averaging amplifier, which eliminates any post-CMOS processing to reduce the trapped charge effect. The unregulated trapped charges originate from the passivation layer and the intra-layers within their structure [10] - [13]. The trapped charges can modulate the ISFETs' threshold voltages into unknown values, and the unknowns will present difficulties in finding the suitable bias for the ISFETs, especially for analogue to digital conversions. Instead of finding the right bias for the ISFETs, this thesis pursues a reference-less sigma delta ($\Sigma\Delta$) modulator which is based on frequency domain signal processing [14]. A functional block diagram is shown in Figure A. Neither a voltage reference nor a current reference is required in this architecture because the signal of interest is in frequency. With only the external clock acting as a reference signal to the modulator, the reference-less $\Sigma\Delta$ modulator processes any mismatched ISFETs in the frequency domain and yields a digital output at the end.

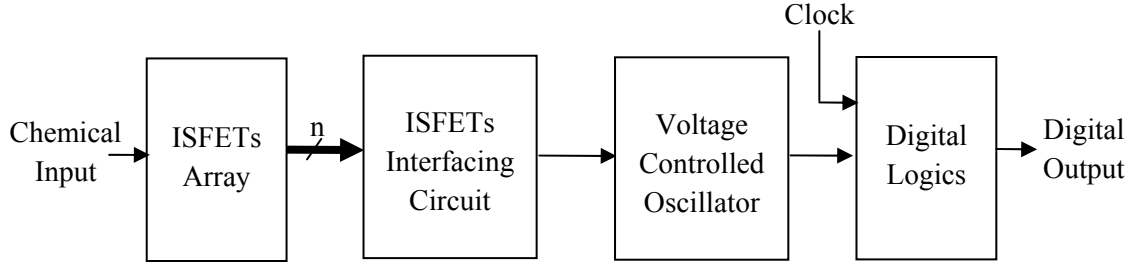


Figure A: Reference-less sigma delta modulator.

The first functional block to realize the reference-less sigma delta ($\Sigma\Delta$) modulator is a front end interface to linearize the ISFETs, whose output current is a non-linear function of pH input. Beside, the ISFETs in standard CMOS processes are prone to have mismatch of threshold voltages in intra- and inter-chips. Both the problem of the mismatch and the nonlinearity will be handled simultaneously by an averaging and a negative feedback. The impact of the threshold voltage variation can be reduced by using the mean response of an array of ISFETs, and the non-linearity of the ISFETs can be compensated by the use of a negative feedback.

The second functional block to realize the reference-less $\Sigma\Delta$ modulator is a voltage controlled oscillator (VCO) which linearly converts a baseband signal into a frequency modulated signal. The VCO plays a critical role in the $\Sigma\Delta$ modulator, because the linearity of the modulator is mainly determined by the VCO. It is not easy to design a CMOS VCO which is low noise, low power, and wide tuning. For instances, opamp RC oscillators such as the Wien-Bridge oscillators or the phase shift oscillators are low power; they are good at the

operating frequency up to hundreds of kHz [15]. However, they either suffer from a small tuning range or a large phase noise. In this thesis, a log domain VCO will be implemented to achieve a large tuning range, low phase noise, and low power operation. Circuit simulations and chip measurements will justify the performance of the log domain oscillator in the CMOS platform.

The last functional block to implement the $\Sigma\Delta$ modulator is a simple digital logic to digitize the frequency modulated signal into the digital output bit-stream. The digital gates only need a stable reference clock to oversample the phase of the frequency modulated signal. The output is a digital bit-stream, which is indistinguishable to a 1st order sigma delta modulation, in which the noise floor is shaped by +20dB/decade.

B. Thesis Organization

This thesis is organized into seven chapters.

- Chapter 1 reviews ISFETs in standard CMOS technology. The device's operating principles and its non-idealities are discussed. This chapter also brings up some existing ISFET interfacing circuits to explore various techniques to help circumvent the accuracy associated with the ISFETs.
- Chapter 2 describes the frequency domain signal processing which is the core processing environment in the proposed ISFETs instrumentation. The principle of operation, analysis, and behavioural simulations are provided to supplement the design requirements in the reference-less sigma delta modulator.

- Chapter 3 suggests the technique for linearising ISFET's responses to pH by using a global current feedback. Stability analysis of current feedback op-amp is discussed to address the closed loop dynamics. By adding multiple inputs to the current summing node in the architecture, a novel averaging amplifier which interfaces an array of ISFETs is invented. This chapter examines some of the merits of the proposed ISFET averaging array.
- Chapter 4 discusses a voltage controlled oscillator (VCO) based on the linear system theory, which generally involves negative feedback for implementation. By keeping the system's input/output unchanged, a VCO can be synthesized through a set of non-linear state space equations. A log domain VCO is illustrated from the point of views of circuit synthesis and circuit analysis.
- Chapter 5 summarizes various circuit building blocks to implement the ISFET64_CHIP, which was fabricated at the United Microelectronics Corporation (UMC) by the 0.18 μm CMOS process. System-level simulation results using Cadence® design environment are included to verify the functionalities and the performance of the chip.
- Chapter 6 presents the design constraints to assemble the ISFET64_CHIP on a printed circuit board. Laboratory set-up and measurement results under electrical and chemical stimuli are reported in this chapter.
- Chapter 7 concludes this thesis, and it suggests few ways to improve the proposed ISFETs instrumentation system.

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Chapter 1

Unmodified ISFETs in Standard CMOS Processes

In 1970, a new class of solid-state chemical sensors called an Ion-Sensitive Field Effect Transistor (ISFET) was invented by Bergveld [1]. The ISFET, fabricated in silicon technology, has an exposed ion-sensitive membrane which can chemically react with the hydrogen ions in a chemical solution to form a pH-dependent interfacial potential between the membrane and the solution. In the past, Abe [2] and Van Der Wal [3] investigated different types of materials in making the ion-sensitive membrane for ISFETs, and their findings are summarized here: Silicon nitride (Si_3N_4) has a sensitivity of 45-56 mV/pH . Tantalum pentoxide (Ta_2O_5) has almost a Nernstian sensitivity of 59 mV/pH . Silicon dioxide (SiO_2), which is a common dielectric used in standard CMOS processes, has a sensitivity of less than 35 mV/pH .

As mentioned in Introduction, realizing ISFETs in standard CMOS technology is the goal of this thesis because CMOS technology offers a low cost, mass producible option. The integration of this class of solid-state chemical sensors into standard CMOS technologies facilitates the development of disposable electronics in vast applications. Although there are still some technical challenges to make high quality ISFETs in standard CMOS processes, it is worthwhile to investigate the way how ISFETs can be adapted into standard CMOS chips.

Nonetheless, the ISFETs developed by Bergveld are not compatible to standard CMOS processes. The fabrication of the ISFETs involves etching of the passivation layer, the intra-metals and intra-dielectrics, and the polysilicon layer, all in precise shape. In addition, it requires depositing a layer of ion-sensitive membrane, which can be either silicon nitride or aluminium oxide, on top of the gate oxide to improve the pH sensitivity. All these post-CMOS processing steps add an extra cost and technical difficulties to the monolithic integration of the chemical sensors in silicon technologies.

The true integration of ISFET in CMOS was inspired by Cane who proposed the idea of extended gate [4] and later by Bausells who developed the floating electrode CMOS ISFETs [5]. The CMOS ISFETs basically are devices with a floating gate node such that the gate is electrically left floating. The formation of the floating gate is done by connecting the passivation layer to the gate oxide through the intra-metal layers, so the fabrication of these CMOS ISFETs are fully compatible with the standard CMOS processes. Therefore, the CMOS ISFETs are chosen to be investigated in this thesis.

This chapter will begin by revealing the operating principle of ISFETs as a CMOS-based pH sensor, using the passivation layer as the ion-sensitive membrane. It will then discuss some of the performance issues of the CMOS ISFETs, including the choices of selecting an electrode, the effect of trapped charges, the drift, the temperature sensitivity of the ISFETs, and the noise consideration. This chapter will end by analyzing some interfacing designs to illustrate the design objectives in using ISFETs for pH measurements.

1.1 ISFET Operating Principle

In this thesis, ISFETs have been implemented as the floating electrode CMOS ISFETs [5] – [7]. The realization of the ion-sensitive membrane is the use of the passivation layer, which is pH-sensitive. The floating gate is formed by connecting the passivation layer with all the available metals and the polysilicon layer. Any change in the potential of the passivation layer due to a change in chemical activity of the chemical solution can modulate the channel's conductivity of the ISFET. This transformation from chemical property to electrical response will be explained later by the site binding model.

This thesis assembles the ISFETs in a 1-Polysilicon-6-Metals (1P6M) CMOS process, and the cross-section of the ISFET is sketched in Figure 1-1. Note that the ISFET is fully compatible with standard CMOS fabrication, and it has been subjected a lot of studies over the past 10 years. A list of works on the ISFET researches fabricated in the commercial CMOS foundries is summarized in Table 1-1.

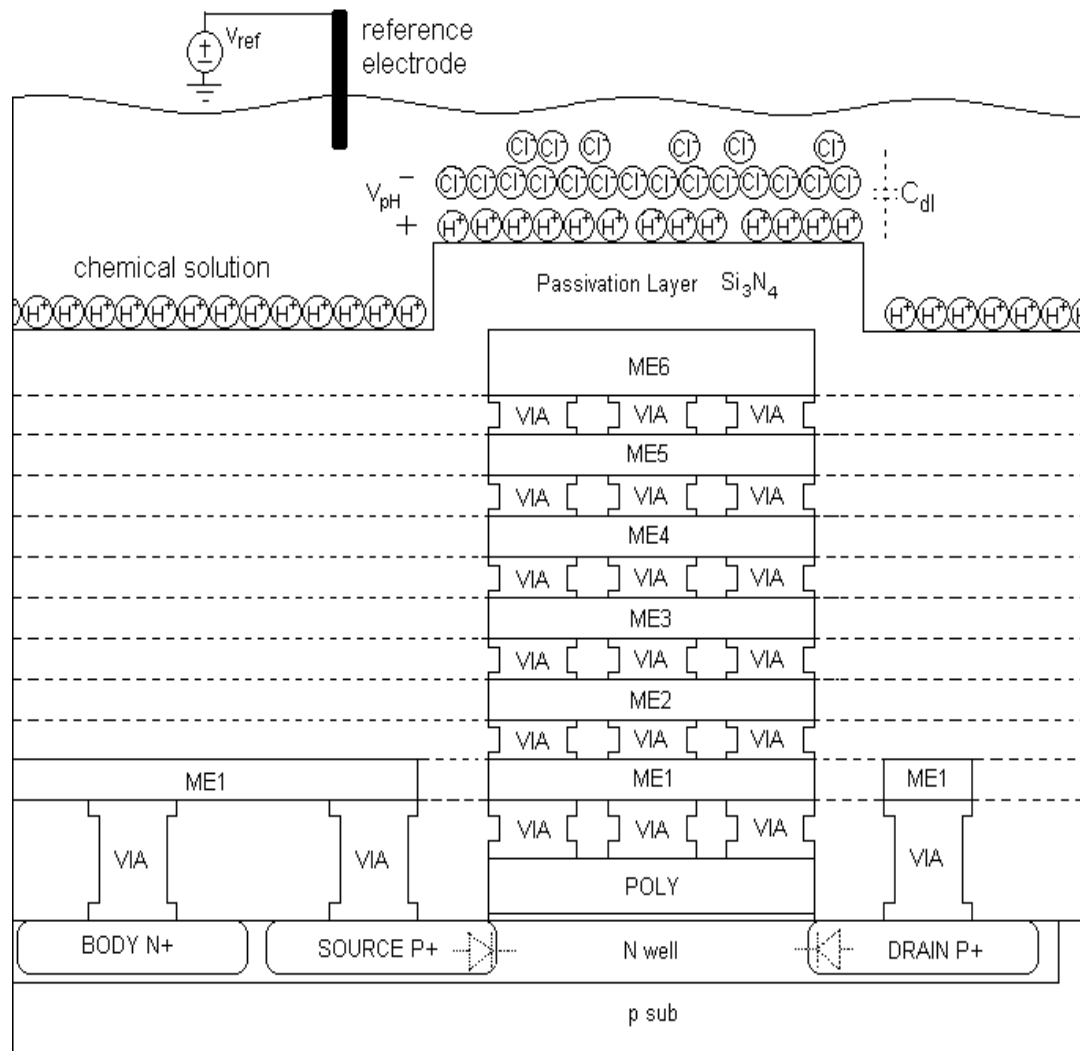


Figure 1-1: Cross-section of the Ion-Sensitive Field Effect Transistor (ISFET) in a 1-Poly-6-Metals (1P6M) CMOS process.

Table 1-1: ISFETs in commercial CMOS technologies

Year	Ref	Type	Passivation thickness	Threshold voltage	Sensitivity (mV/pH)	Technology
1996	[4]	n-type	1.5 μm	3.5 volts	41	Atmel 1 μm 1P2M
1999	[5]	n-type	1.5 μm	-7 to 6.5 volts	47	Atmel 1 μm 1P2M
2000	[8]	n-type	0.75 μm SiO ₂ / Si ₃ N ₄	8.5 volts	25	AMS 0.6 μm 2P3M
2002	[9]	p-type	0.4 μm Si ₃ N ₄ / 0.6 μm SiO _x N _y	-8 to -33 volts	42	AMS 0.6 μm 1P2M
2004	[10]	n-type	1 μm	< 0.4 volt	0.22 (Al ₂ O ₃)	AMI 1.6 μm 1P2M
2004	[11]	p-type	0.4 μm Si ₃ N ₄ / 0.6 μm SiO _x N _y	-5 volts	43	AMS 0.6 μm 2P3M
2005	[12]	n-type	-	-	31,51	AMI 1.5 μm 1P2M
2008	[13]	p-type	1.03 μm SiO ₂ / Si ₃ N ₄	-4 to -1 volt	46	AMS 0.35 μm 2P3M
2008	[14]	n-type	0.5 μm SiO ₂ / 0.7 μm Si ₃ N ₄	-1.03 volts to 4.17 volts	33.2	UMC 0.18 μm 1P6M
2008	[14]	n-type	0.6 μm SiO ₂ / 0.7 μm Si ₃ N ₄	-10 volts to -0.03 volt	36.6	UMC 0.25 μm 1P5M
2008	[14]	n-type	1.03 μm SiO ₂ / Si ₃ N ₄	0.97 volt to 1.73 volts	31.7	AMS 0.35 μm 2P4M
2010	This work	p-type	0.5 μm SiO ₂ / 0.7 μm Si ₃ N ₄	-0.8 volt (an average of 64 ISFETs)	37	UMC 0.18 μm 1P6M

The works listed in Table 1-1 indicates that CMOS ISFETs did exhibit a satisfactory sensitivity to pH (the only exception is the work from Lee [10] whose ISFETs achieved a sensitivity of 0.2 mV/pH), but they experienced variations of threshold voltages. By comparing the pH sensitivity found in [14] with this work, the pH sensitivity of the ISFETs is quite consistent for a given technology, but a random mismatch of the threshold voltages of the ISFETs can take place. Therefore, although it is possible to measure the pH of a chemical solution using a CMOS ISFET, but the mismatch in the threshold voltage of the devices can make them impractical to be used in few cases. In order to understand these phenomena, a fundamental study of the ISFET's operation is given below.

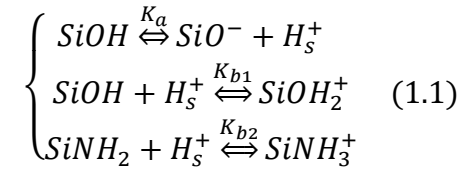
Figure 1-1 illustrated that the structure of the ISFET is almost identical to a primitive p-type Metal-Oxide-Semiconductor (pMOS) transistor; both the ISFET and a pMOS has the GATE, the SOURCE, the DRAIN, and the BODY terminals. Without any electrical bias, the path between the SOURCE and the DRAIN of the devices is blocked by the two reversed p-n junctions [15]. When a proper voltage bias is applied between the GATE and the SOURCE such that the corresponding gate source voltage exceeds the threshold of the devices, a channel current between the DRAIN and the SOURCE is formed. The conductivity of the channel increases as the corresponding gate source voltage is increased. The BODY is used to bias the N-well to minimize any leakage current between the DRAIN/SOURCE to the N-well. However, if the electrical potential between the SOURCE and the BODY is not equal, the body effect (also known as the back gate effect) will arise and will deteriorate the transconductance of the devices [15]. Nonetheless, the BODY is tied to the SOURCE as shown in Figure 1-1 so that the body effect is eliminated.

On the other hand, the GATE of the ISFET as shown in Figure 1-1 is composed of the reference electrode, the chemical solution, the passivation layer, and the intra-metals. The function of the reference electrode is acting as a voltage source to bias the chemical solution electrically. A reference electrode such as a silver/silver chloride can serve the purpose of transferring the electrical potential (V_{ref}) from the reference electrode to the chemical solution through a stable electrode/liquid interface [16]. The electrical potential V_{ref} can be transmitted to the surface of the passivation layer through the electrochemical double layer capacitor [17], [18]. In fact, the voltage developed at the passivation layer is depended on the V_{pH} developed across the double layer capacitor. It will be shown in later that the magnitude of V_{pH} depends on the concentration of the hydrogen ions in the chemical solution.

When the passivation layer, which is usually a layer of silicon nitride on top of silicon dioxide, is immersed in the chemical solution, the surface layer can be hydrolysed to form the amphoteric ($SiOH$) and the basic sites ($SiNH_2$) [6], [7], [19]. An amphoteric site can either accept or donate hydrogen ions whereas a basic site can only accept hydrogen ions from its surrounding solution. In other words, the surface of the passivation layer can be positively or negatively charged, depending on whether the hydrogen ions are leaving or entering the membrane. On the other hand, there will be an equal amount but opposite charged ions accumulated over the solution, and these two groups of opposite charges form the double layer capacitor [17], [18]. The origin of these charge distribution is the result of the electrostatic force exerted by the charges on the surface of the passivation layer, and this will be explained next in greater details by the site binding model [9], [20]. As a result, an electrical potential difference is set up across the double layer capacitor, and the value of the

potential depends on the amount of charges created in the passivation layer. In fact, the relationship between the potential and the charges obeys $Q = C_{dl}V_{pH}$ [17], where Q is the amount of charge in the passivation layer, C_{dl} is the double layer capacitor, and V_{pH} is the potential developed across the double layer capacitor.

When silicon nitride is hydrolyzed in a chemical solution, it forms $SiOH$ and $SiNH_2$. Both $SiOH$ and $SiNH_2$ associate and dissociate with the hydrogen ions to end up with the following chemical equilibriums [19], [21]:



where K_a , K_{b1} , and K_{b2} are the chemical equilibrium constants. In the following, the notation to represent the concentration of chemicals is done by using a bracket to enclose the chemical symbol.

The buffer capacity β of the passivation layer is defined as the ability of the silicon nitride layer to deliver or to take up hydrogen ions due to a change in pH over the passivation layer [21]:

$$\beta = \frac{d[B]}{dpH_s} \quad (1.2)$$

where $[B] = [SiO^-] - [SiOH_2^+] - [SiNH_3^+]$, and the brackets enclosing the chemical symbol represent the concentration of the chemicals. Note also that the quantity of $[B]$ can also be related to the surface charge density (σ_s) as [21]:

$$[B] = -\frac{\sigma_s}{q} \quad (1.3)$$

Assuming that there are net negative charges on the surface of the silicon nitride, there will be an equal amount of positive charges accumulated on the solution. In fact, the charge distribution over the solution is governed by the inner Stern layer and the outer diffuse layer [18], [20]. The chemical ions in the solution will arrange themselves into these two layers to balance the opposite charges formed in the passivation layer. The separation of these two opposite charges is governed by the double layer capacitance:

$$\sigma_s = \psi_s C_{dl} \quad (1.4)$$

where ψ_s is the electrical surface potential on the silicon nitride relative to the bulk potential. If Equation 1.4 is substituted back into Equation 1.3, the following relationship can be obtained:

$$[B] = \frac{-1}{q} (\psi_s C_{dl})$$

$$\Rightarrow \beta = \frac{d}{dpH_s} \left[\frac{-1}{q} (\psi_s C_{dl}) \right] = \frac{-C_{dl}}{q} \frac{d\psi_s}{dpH_s}$$

$$\therefore \frac{d\psi_s}{dpH_s} = -\frac{q\beta}{C_{dl}} \quad (1.5)$$

On the other hand, the concentration of the hydrogen ions on the surface of the silicon nitride is related to the concentration of the hydrogen ions in the bulk solution by the Boltzmann distribution [21]:

$$[H_s^+] = [H_{bulk}^+] \exp\left(\frac{-q\psi_s}{kT}\right) \quad (1.6)$$

By definition, $pH = -\log_{10}[H]^+$. Equation 1.6 can be reformulated as:

$$\psi_s = \ln(10) \frac{kT}{q} (pH_s - pH_{bulk})$$

$$\frac{d\psi_s}{dpH_{bulk}} = \ln(10) \frac{kT}{q} \left(\frac{dpH_s}{d\psi_s} \frac{d\psi_s}{dpH_{bulk}} - 1 \right)$$

$$\Rightarrow \frac{d\psi_s}{dpH_{bulk}} = \frac{2.3 \frac{kT}{q}}{2.3 \frac{kT}{q} \frac{dpH_s}{d\psi_s} - 1}$$

$$\frac{d\psi_s}{dpH_{bulk}} = \frac{2.3 \frac{kT}{q}}{2.3 \frac{kT}{q} \left(\frac{-C_{dl}}{q\beta} \right) - 1}$$

$$\therefore \frac{d\psi_s}{dpH_{bulk}} = -2.3\alpha U_T \quad (1.7)$$

where $\alpha = \frac{1}{2.3 \frac{kT C_{dl}}{q^2 \beta} + 1}$ is the sensitivity coefficient and $U_T = \frac{kT}{q}$ is the thermal voltage.

Equation 1.7 represents the sensitivity of silicon nitride to a change in the concentration of the bulk hydrogen ions in logarithmic scale. Note that for $\alpha = 1$, a Nernstian sensitivity, which is equal to 59 mV/pH at room temperature [17]. A Nernstian sensitivity can be realized in the materials having a large buffer capacity (β) value and a small double layer capacitance (C_{dl}) value. Materials such as tantalum pentoxide (Ta_2O_5) can attain Nernstian responses over a unit change in pH because Ta_2O_5 has a very large buffer capacity [17]. Silicon nitride (Si_3N_4) achieves a sensitivity of $45\text{-}56 \text{ mV/pH}$.

Finally, the threshold voltage of an ISFET can be derived with Equation 1.7 in order to simplify circuit analysis involving ISFETs. Some sophisticated ISFET's models were developed, and they were Simulation Program with Integrated Circuit Emphasis (SPICE) compatible [22], [23], but the simplest model to express the ISFET's threshold voltage is to segregate the pH-dependent terms from the pH-independent term. One of the simple expressions is [24]:

$$V_{th} = C + 2.3\alpha U_T pH \quad (1.8)$$

where C is a group of variables unrelated to the pH. In this thesis, Equation 1.8 is handy for analyzing ISFET interfacing designs. Nonetheless, the equation is valid only if the passivation layer is negatively charged. Equivalently speaking, Equation 1.8 can only be used when the pH of the chemical solution is larger than the point-of-zero charge (pH_{pzc}) of the passivation layer [17]. Silicon nitride has a point-of-zero charge of approximately 2.2 [9], so Equation 1.8 is valid to be used when the pH of a chemical solution is larger than 3.

To summarize the above discussion, a macromodel showing a p-type ISFET in standard CMOS processes is shown in Figure 1-2.

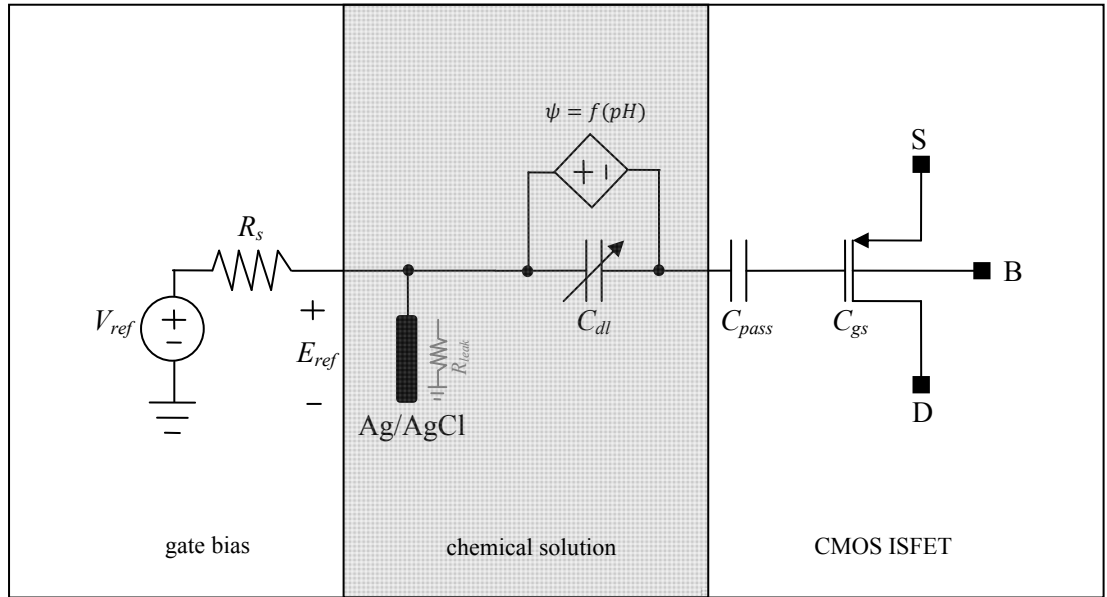
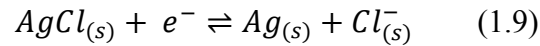


Figure 1-2: Unmodified p-type ISFET macromodel with an external silver/silver chloride (Ag/AgCl) reference electrode.

Comparing the ISFET's symbol shown in Figure 1-2 with a standard pMOS symbol, there are few distinctions between the ISFET and a standard pMOS. First, the gate bias (V_{ref}) of the ISFET is transferred to the chemical solution through the reference electrode. Second, there is the pH-dependent voltage source $\psi = f(pH)$ in series with the V_{ref} . The strength of the pH-dependent voltage source will be proportional to the pH and also to the temperature. This pH-dependent source will also experience drift. Third, the ISFET has the two extra capacitors connected in series with the gate oxide capacitor (C_{gs}). These two additional capacitors are the double layer capacitor (C_{dl}) and the passivation capacitor (C_{pass}). Note that trapped charges present in the floating gate node can modulate the threshold voltage of the ISFET in atypical values. A lot of works were done on each of the above characteristics over the past ten years, and they are discussed in the next few sections.

1.2 Reference Electrode

The standard method to set up a well-defined electrical potential in a chemical solution is by using a silver/silver chloride ($Ag/AgCl$) reference electrode. Consider the following chemical reaction which takes place in the silver chloride electrode [16]:



Whenever there is a transfer of electrons between the silver chloride electrode and the aqueous solution, a small amount of an electrical potential is set up at the interface between

the electrode and the surrounding chloride solution such that the surrounding chloride solution is at near the same potential as in the silver chloride electrode. In order to allow the potential of the chloride solution to be coupled to the external chemical solution as shown in Figure 1-3, a small frit is made at the bottom of the glass container, so that the frit allows only the diffusion of hydrogen ions in and out of the reference electrode system. The frit does not mix the internal chloride solution with the external chemical solutions, so it will not alter the concentration of the chemicals. The frit acts as a salt bridge between the two chemical solutions to permit electrical conductivity between them.

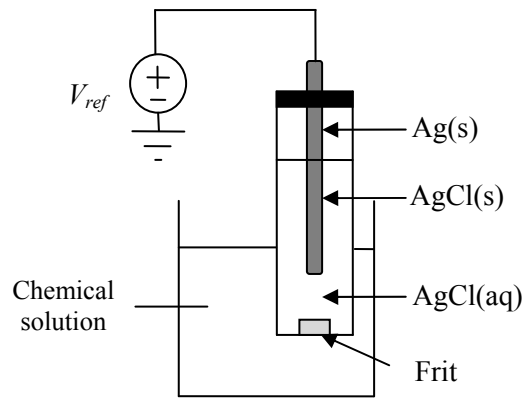


Figure 1-3: silver/silver chloride reference electrode.

Many works investigated whether a silver/silver chloride reference electrode can be integrated on chip. For instance, Huang [25] and Suzuki [26] experimented with fabricating a micro reference electrode on-chip using micromachining. They fabricated a micro-chamber with a silver chloride electrode in a concentrated potassium chloride solution by means of

photolithography and chemical etching. The drawback of fabricating the micro-reference electrode is the incompatibility with standard CMOS processes. Moreover, there is an uncertainty in keeping that tiny amount of the reference electrolyte into that micro-chamber. If the chamber is leaky, the concentration of the reference electrolyte can change drastically over time. The change in the concentration of the electrolyte will cause drifts in the interfacial potential between the electrode and the reference electrolyte. For instance, both Huang and Suzuki reported that the drifts were in the order of milli-volts at the beginning of their measurements, and the amount of the drifts changed at the later times.

Another approach was to develop an integrated solid state electrode on-chip. Previous work attempted to fabricate a pseudo-reference electrode, which is a piece of metal, on chip. For instance, platinum [27] and gold [28] were tried previously in making a pseudo-reference electrode. Nonetheless, those pseudo-reference electrodes suffered noisy interfacial potential between the electrode and the solution [16]. Therefore, a more effective way of using a solid-state pseudo reference electrode is to employ a differential mode of operation, one composed of an ISFET and the other one composed of an inert Reference FET (REFET). Any common mode noise, which originates from the interfacial potential between the pseudo-reference electrode and the chemical solution, can be reduced by a differential circuit. On the other hand, the difference between the sensitivity of an ISFET and a REFET stimulates the differential circuit to respond a change in the pH of the solution. One of the proposed ISFET interfacing circuits is sketched in Figure 1-4 to demonstrate the concept of the differential operation.

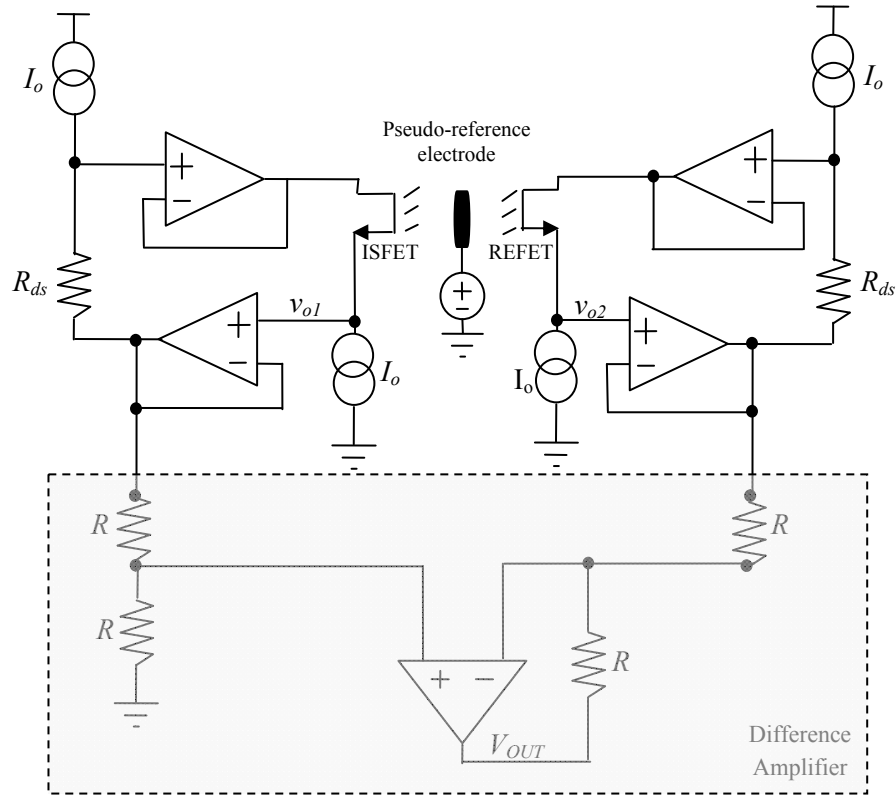


Figure 1-4: Pseudo-reference electrode with differential circuit operation [9].

In an ideal situation, the drain source voltage of the ISFET/REFET, as shown in Figure 1-4, is fixed by the positive feedback. The sensor's drain source voltage in this feedback configuration is equal to the voltage across the resistor $V_{DS} = I_o R_{ds}$. The drain current of the ISFET/REFET is biased by the constant current source I_o . Thus, the quiescent point ISFET/REFET is fixed by the constant drain source voltage and the constant drain current [29]. The differential output reading v_{o1} and v_{o2} are fed to the difference amplifier to produce the output $V_{OUT} = v_{o1} - v_{o2}$.

However, there is one hidden problem associated with the REFET: making a chemically inert REFET is not easy. Ideally, a REFET is not sensitive to pH, but it should respond identically to an ISFET in the presence of drift and noise. Some researchers proposed to use polyvinyl chloride (PVC) to cover the ion-sensitive membrane [30]. The response of the REFET relying on the PVC was not accurate and precise because the drift in the PVC is not the same as in silicon nitride. A similar case was reported when implementing two different ion-sensing materials with two ISFETs operated in the differential mode [28]. However, whether the two different ISFETs can retrieve the same bias information from the pseudo-reference electrode has to be verified first.

A Korean group explored a new dimension of implementing ISFETs on-chip by fabricating a pH-sensitive electrode on-chip. Kim used iridium oxide as a material to fabricate the solid-state ion-selective electrode [31]. This pH-sensitive electrode is different from the previous pseudo-reference electrode because the pH-sensitive electrode has a Nernstian response to pH. Therefore, by making an ISFET whose ion-sensitive membrane is different from iridium oxide, the ISFET can then be biased normally by using the integrated ion-selective electrode. The only uncertainty with this approach is whether or not the ion-sensitive electrode and the ion-sensitive membrane can respond to the same common mode signals. Nonetheless, the use of the ion-selective electrode opens up a new dimension of ISFET interfacing designs because the performance of the pH-sensitive electrode does not require matching of devices.

1.3 Trapped Charges in CMOS ISFETs

This section discusses the origin of the trapped charges in unmodified CMOS ISFETs and the possible ways to minimize their impact on the device/circuit operation. In standard CMOS transistors, the trapped charges buried in the gate oxide are the contamination of alkali metal ions, particularly sodium ions from the fabrication environment, the interface trap charges from the sudden termination of the semiconductor crystal lattice at the Si-SiO₂ interface, the oxide fixed charges from the various oxidation state of the silicon atom, and the oxide trapped charges from the radiation [15]. The influence of the trapped charges on the threshold voltage of a MOS transistor can be observed from the following expression:

$$V_{th} = \Phi_{ms} - \frac{Q_{trap}}{C_i} - \frac{Q_d}{C_i} + 2\phi_F \quad (1.10)$$

where the trapped charges (Q_{trap}) modulate the threshold voltage by an amount of $\frac{Q_{trap}}{C_i}$, and C_i is the gate oxide capacitance.

In standard CMOS technologies, the threshold voltage of MOS transistors can be adjusted by ion implantation. For example, boron implantation to the gate area of a pMOS can increase the value of the threshold voltage of the device, and the amount of the threshold voltage tuning can be controlled by the implant time or the implant concentration [15]. In the UMC 0.18 μm CMOS process, the values of the threshold voltages are +0.6 volt for 3.3 volt n-channel devices, -0.7 volt for 3.3 volt p-channel devices, +0.3 volt for 1.8 volt n-channel devices, and -0.45 volt for 1.8 volt p-channel devices [32].

On the other hand, the CMOS ISFET model shown in Figure 1-2 contains the additional passivation capacitor (C_{pass}) in series with the gate oxide capacitor (C_{gs}) through the electrically floating metal layers. The passivation layer is composed of a $0.5\mu\text{m}$ thick silicon dioxide and a $0.7\mu\text{m}$ thick silicon nitride [32]. Any trapped charges, if they exist in the floating gate (i.e., the passivation layer and the floating metal layers) of an ISFET, can offset the ISFETs' threshold voltages into atypical values. For instance, Bausells reported a threshold voltage of -7 volts to +6 volts in his n-type ISFETs [5], and Hammond reported a threshold voltage of -33 volts to -8 volts in his p-type ISFETs [9]. Several approaches have been proposed recently to reduce the impact of the trapped charges in the CMOS ISFETs.

First, a proven technique to remove the excess electrons in the floating gate of a p-type ISFET is by an UV radiation [9], and [33]. If an UV light is projected to the passivation layer and the floating metal layers associated with the ISFET, the UV light can excite the electrons from these layers to its neighbour. When enough electrons are discharged due to the UV radiation, the number of the trapped electrons in the floating gate will become less, and this causes an increase in the device's threshold voltage. In [9], Hammond showed how the UV radiation can increase the threshold voltage of his p-type ISFET from -22 volts to -2 volts.

Second, techniques such as electron tunnelling and hot electron injection are capable of removing and adding electrons to the floating gate node of a floating gate device respectively [34]. In electron tunnelling, a high electric field across the gate oxide can force the electrons in the floating gate tunnel through the gate oxide to the substrate whereas in hot electron injection, electron in the substrate can be injected into the floating gate. Therefore, these two approaches are able to remove the stored charges on the floating gate node of a floating gate

device. In [35], Georgiou reported a use of hot electron injection to program the threshold voltage of a p-type ISFET by an amount of 2.8 volts.

Third, Georgiou introduced a new concept of programmable gate ISFET [36], in which the structure of the CMOS ISFET is modified by adding a control-gate capacitor (C_{CG}) attaching to the floating gate of the device. The device operating point can therefore be adjusted by the control gate. The model is illustrated in Figure 1-5.

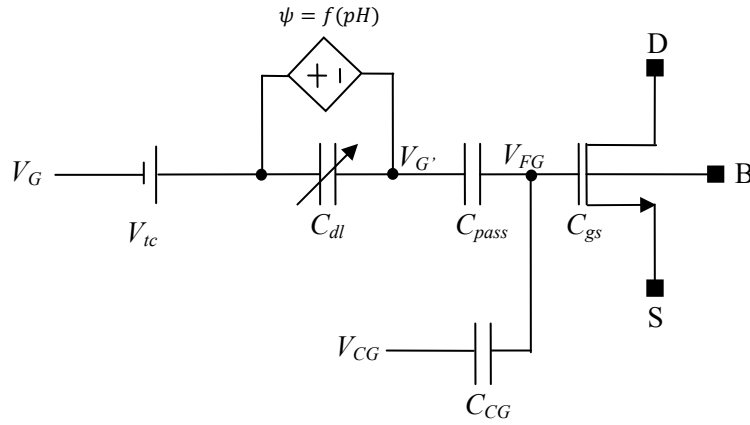


Figure 1-5: Programmable gate ISFET macromodel [36].

Note that the operation of the programmable gate ISFET follows the n-type transistor's device physics. The effect of the trapped charges can be compensated under the condition [36]:

$$C_{pass}V_{tc} = -C_{CG}V_{CG} \quad (2.11)$$

where V_{tc} is the equivalent voltage contributed by the trapped charges. Hence, the threshold voltage shift due to the trapped charges is cancelled by biasing the control gate with the voltage of $-\frac{C_{pass}}{C_{CG}}V_{tc}$.

This thesis has attempted to average the trapped charges within an array of ISFET [37]. The design of the averaging array will be discussed in Chapter 3. Recall that Table 1-1 summarizes the different findings on the threshold voltage mismatch of the on-chip ISFETs. Those findings justified that the trapped charges on the on-chip ISFETs are randomly distributed over the intra- and inter-chips. If the trapped charges are mutually independent, the sum (or the average) of those trapped charges, according to the Central Limit Theorem [38], will follow a normal distribution with the sample mean and the standard deviation, under the condition that the sample size is large enough¹. By considering all the geometrically isolated ISFETs as a global ISFET, the effect of the trapped charges is less significance by taking the average of all the individual ISFETs, provided that the mean of the trapped charges of all the samples closes to zero. The sample standard deviation can also be made lower by using a large sample size. However, as the size of the samples increases, the chip area will also be increased due to the increase in the number of the devices and the interconnects. In addition, more power is needed to supply to the chip as more bias currents are needed. Therefore, a trade-off has to be made in between the sample size, the chip area, and the power consumption.

¹ There is no conclusion to determine the size of samples which follow normal distribution, but a sample size of larger than 50 is commonly used.

1.4 Drift in ISFETs

Drift is a common property found in ISFETs [17]. It is a phenomenon in which the threshold voltage of ISFETs increases/decreases slowly and monotonically by a step change in the pH of the chemical solution. Typical short term drift is in the order of few milli-volts per hour when an ISFET has exposed to a chemical solution for the first few hours, while long term drift is in the order of several tenths of milli-volts per hour when the ISFET has been exposed to the solution for more than ten hours [39] - [41]. The presence of drift interferes with the actual measurement results, so corrections have to be made on the readings, using either a digital signal processing or a dedicated circuit to handle the drift.

The origin of the drift has not yet known, and in the past some theories were proposed to explain the drift behaviour. Jamasb hypothesized that the drift in ISFETs is a chemical modification on the surface of the ion-sensitive layer due to the exposure to an aqueous electrolyte [39] - [41]. He used silicon nitride as an example to illustrate the behaviour of the drift in the ISFETs. When silicon nitride is exposed to a chemical solution, the surface layer of the silicon nitride will be hydrated to form a mixture of silicon dioxide and silicon oxy-nitride. The hydration from the silicon nitride to the silicon dioxide is a slow process, and the transient response can be modelled by the stretched exponential time dependence [41]:

$$N(t) = N(\infty) \left(1 - \exp \left(- \left(\frac{t}{\tau} \right)^\beta \right) \right) \quad (1.12)$$

where $N(t)$ is the number of silicon nitride molecules undergoing the transformation at time t , $N(\infty)$ represents the total number of silicon nitride molecules that can undergo the transformation, τ is the time constant of the model, and β is the dispersion parameter. Equation 1.12 can be used to predict the rate of the growth of the hydrated silicon nitride layer, and it describes that the change in the chemical property of the ion-sensitive layer is a slow and monotonic process.

The solution to compensate the drift in real time is not easy, as the value of the drift can be pH dependent [40]. Moreover, the drift also behaves differently in different types of the silicon nitride lattice. Hammond observed that the drift in his CMOS ISFETs was larger than Jamasb's non-CMOS ISFETs, even though both types of the ISFETs were made of silicon nitride [7]. He explained that the CMOS ISFETs were made from the plasma enhanced chemical vapour deposition (PECVD), which is a low temperature fabrication step, while the non-CMOS ISFETs were made from the low pressure chemical vapour deposition (LPCVD), which is a high temperature process. These two different decomposition steps yield two different types of lattice, in which the LPCVD can grow a more crystalline silicon nitride structure, which has the lower drift [7].

The traditional method to correct the drift in the ISFET's responses to pH is to store the measurement data in memory. Then, an algorithm similar to Equation 1.12 can be implemented to correct the measurement data. In many cases, the drift correction is done in digital signal processing. On the other hand, if the drift rate is much smaller than the rate of change in the pH, the consecutive measurements taken in between a short period of time (e.g. in a minute) can be assumed free of drift [40]. This assumption is generally applicable to the

case when there is a relative big change in the pH, as the amount of the drift is about 0.1 pH per hour. Therefore, as long as the rate of change in the pH of the sample solution is much bigger than 0.1 pH per hour, the consecutive measurements taken between short intervals are relatively free of influence of the drift. Both Jamasb [40] and Bhusana [42] attempted to correct the drift of the ISFETs in their measurements, which were based on the aforementioned assumption that the drift is insignificant in between a short period of time.

1.5 Temperature Sensitivity of ISFET

Referring back to Equation 1-7, the maximum sensitivity of an ISFET is 59 mV/pH when the sensitivity constant α is equal to one. This is a Nernstian response to pH at room temperature of 25°C . At higher temperatures, the sensitivity will increase [43]. Equation 1-7 reveals that the sensitivity is linearly proportional to the thermal voltage ($U_T = \frac{kT}{q}$). In other words, the sensitivity is proportional to the absolute temperature. In order to illustrate the combined effect of both pH and temperature on the relative surface potential of an ion-sensitive membrane, Figure 1-6 plots the relative surface potential of an ion-sensitive layer as a function of pH and temperature in a Nernstian response characteristic.

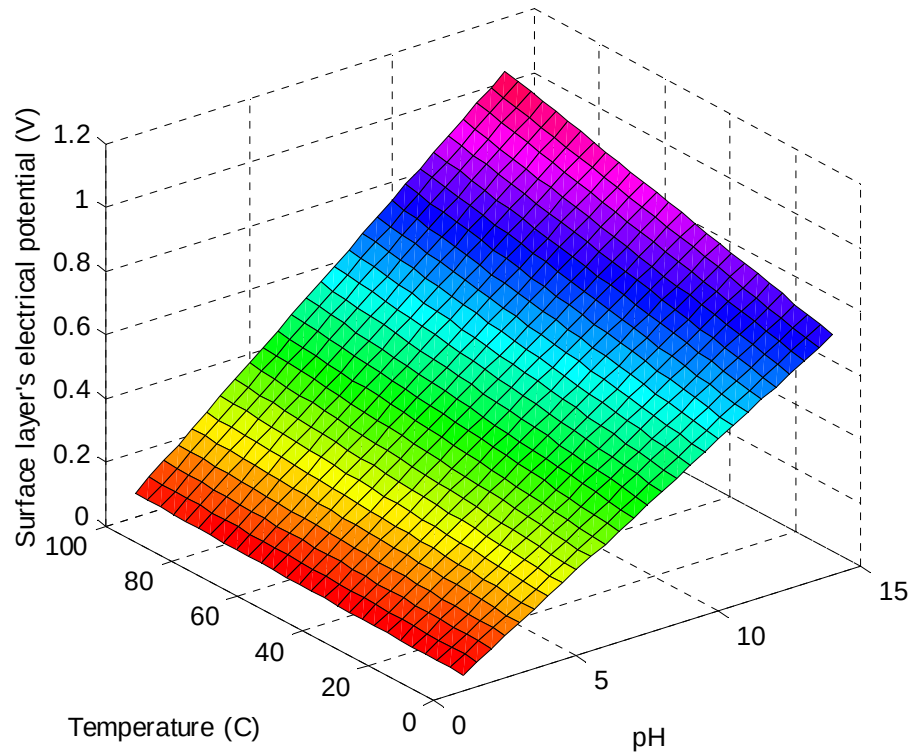


Figure 1-6: Relative surface potential versus pH and temperature.

Close examination of Figure 1-6 reveals that both pH and temperature can alter the surface layer's electrical potential. Therefore, a change in the surface potential of an ion-sensitive membrane can be based upon a larger change in pH at a lower temperature, or a smaller change in pH at a higher temperature. Ideally, a Nernstian sensitivity is linear to temperature, so it makes temperature compensation easier to accomplish. In literature, there are at least two different approaches to compensate the ISFET's temperature dependency. One is based on the software implementation [44], [45], and the other one is based on the H-cell concept [24], [46].

Chung's idea was a software-control temperature compensation circuit with two analogue inputs: one input captured the chip's temperature and the other input captured the pH. The temperature information was obtained by measuring the threshold voltage of the FET because the threshold voltage comprises of $2\phi_F$ which is directly proportional to the absolute temperature [15]. Therefore, the temperature information can be recorded by devising the threshold voltage extractor [44], [45]. The pH of a chemical solution was captured by the ISFET configured in the bridge-type sensing circuit, which showed a linear response to pH [45]. The information of these two channels, the pH and the temperature, were logged by the data acquisition card and post-processed in National Instruments® Labview. Thus, the correction to temperature variation in the measurement data can be done by either using a look-up table or a dedicated algorithm to correct the data.

Shepherd's idea was to use the transistors' dynamics in the weak inversion region to linearize the Nernst Equation [24], [46]. The Nernst Equation relates the chemical activities between the solution and the solid-state electrode [47]:

$$\Delta E = -\frac{RT}{F} \ln \left\{ \frac{a_x}{a_y} \right\} \quad (1.13)$$

where R and F are the gas constant and Faraday constant respectively, T is the absolute temperature, ΔE is interfacial potential between the solution and the electrode, and a_x and a_y are the activities of the ions in the solution and the electrode respectively. On the other hand, the drain current of a MOSFET operating in the weak inversion region has an exponential

relationship with the transistor's gate source voltage [15]. Therefore, there is an inverse relationship between the interfacial potential ΔE which has a natural logarithmic relationship with the chemical activities, and the drain current of a transistor operating in the weak inversion which is exponential to its gate source voltage. This inverse relationship evolves to the H-cell concept, which expresses the relationship between the output current of the H-cell and the concentration of the hydrogen ions as [24]:

$$I_D(V_{T0} + \Delta V_{T0}) = I_{DQ} \Delta[H^+]^{\alpha/n} \quad (1.14)$$

where α is the sensitivity coefficient identical to Equation 1.7, I_{DQ} is a constant, and n is the sub-threshold slope parameter. Equation 1.14 shows that the output current of the H-cell is temperature insensitive. It is not a linear function to the concentration of the hydrogen ions, and a CMOS log domain squarer was proposed to linearize Equation 1.14 [24], [48], based on the Translinear Principle. As a consequence, the H-cell concept in combination with the Translinear circuit can yield a low power ISFET interface with good linear response to the concentration of hydrogen ions.

1.6 Noise Sources in CMOS ISFETs

In this section, two noise mechanisms are described for CMOS ISFETs². They are thermal noise and flicker noise. The origin of thermal noise is the thermal excitation of the charge carriers over the conducting channel, and the magnitude of the noise is proportional to the absolute temperature. Thermal noise has a flat frequency spectrum. In a CMOS ISFET or a MOSFET, the thermal noise appears as the drain current of the device, and it can be modelled by Equation 1.15 [49].

$$I_d^2(f) = 4kT \left(\frac{2}{3} \right) g_m \quad (1.15)$$

where k is Boltzmann's constant, T is the absolute temperature, and g_m is the transconductance of the ISFET.

On the other hand, flicker noise in a conducting channel occurs because of the presence of traps, where charged carriers in the conducting channel are held and released randomly [49]. Flicker noise has a $1/f$ spectral density, and it is proportional to the active area of a device. It is also true that a p-type device has a lower flicker noise than a n-type device. In a CMOS ISFET or a MOSFET, flicker noise emerges as the gate voltage of the device, and it is modelled by Equation 1.16 [49].

$$v_g^2(f) = \frac{K}{WLC_{ox}f} \quad (1.16)$$

² In CMOS circuits, there are at least three noise mechanisms: Thermal noise, shot noise and the flicker noise [49].

where K is a constant, W and L is the width and the length of the gate, C_{ox} is the gate oxide capacitance, and f is the frequency.

Circuit techniques to reduce the noise of active devices can be done by correlated double sampling or chopper stabilization [50]. These two techniques are especially effective in dealing with the low frequency flicker noise, but they come with an expense of increasing the in-band noise of the system. This is because those two techniques can alias the wideband noise down to the baseband. In ISFET's application where the system baseband is below kHz , the choice of using correlated double sampling or chopper stabilization is good.

On the other hand, averaging can also be considered as an alternative to reduce noise in general, and the principle of averaging to achieve a low noise ISFET front-end interface will be discussed in Chapter 3.

1.7 Existing ISFET Interfacing Circuits

This section will review some circuit designs to interface ISFETs. The objective of those design solutions is to achieve a linear response with pH. So, an understanding of the ISFET's model in its different operating regions can simplify the circuit analysis. In MOSFETs, or similarly in ISFETs, there are four operating regions, depending on the gate source and the drain source biasing of the transistor. The four operating regions of a nMOS are summarized in Table 1-2 [49], [51].

Table 1-2: Large signal model in nMOS

Region	Equation	Condition
Cut – off	$I_D = 0$	$V_{GS} < V_T$ and $\phi_s < \phi_F$
Weak inversion	$I_D = I_t \frac{W}{L} \exp\left(\frac{V_{GS} - V_T}{nU_T}\right)$	$V_{GS} < V_T$, $\phi_F < \phi_s < 2\phi_F$, and $V_{DS} \geq 100 \text{ mV}$
Triode	$I_D = \frac{1}{2} \frac{W}{L} \mu_n C_{ox} [2(V_{GS} - V_T) - V_{DS}] V_{DS}$	$V_{GS} > V_T$ and $0 < V_{DS} < V_{GS} - V_T$
Active	$I_D = \frac{1}{2} \frac{W}{L} \mu_n C_{ox} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$	$V_{GS} > V_T$ and $0 < V_{GS} - V_T < V_{DS}$

Table 1-2 tells us that when the gate source voltage is smaller than the threshold voltage of the transistor, the surface potential ϕ_s on the bulk of the silicon will decide whether the device is operating in the weak inversion region or in the cut-off region. On the contrary, when the gate source voltage of the transistor is larger than the threshold voltage, the transistor can operate in either the triode region or the active region, depending on the drain source voltage of the transistor. The term lambda³, λ is used to model a finite output resistance across the drain source terminals of the transistor. Nonetheless, the drain current of the transistor is always non-linear related to the gate source voltage, even if the transistor is operating in the triode region in today's submicron CMOS processes⁴ [15]. Hence, most ISFET readout circuits in the literature used some kinds of negative feedback to linearize

³ Typical values of lambda (λ) vary approximately from 0.02 to 0.05 V^{-1} [32].

⁴ Secondary effects liked mobility degradation causes the drain current to increase sub-linearly with the gate bias.

ISFET's response to pH. Voltage mode and current mode approaches were exploited in designing such ISFET interfacing circuits. The designs are discussed in the following.

The first example is the constant voltage, constant current source follower system as illustrated in Figure 1-7 [52].

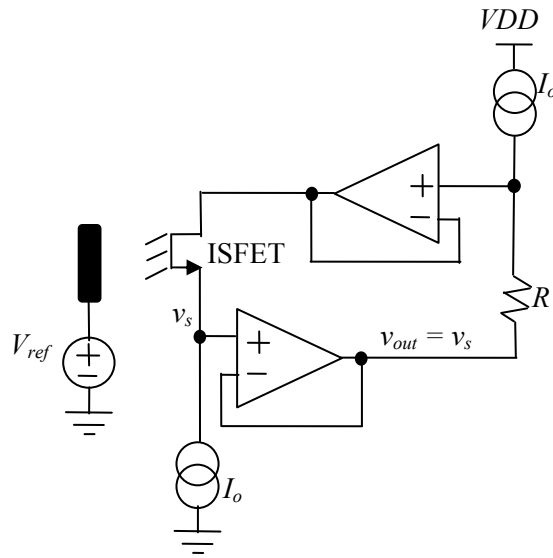


Figure 1-7: Constant voltage constant current source follower system.

This design is very popular in printed circuit board prototyping because the opamps, the current source/sink, and the resistor are all available in many electronic suppliers. The detailed printed circuit board (PCB) description is given in Figure 8-4 of the Appendix. The operation of this circuit is to provide a constant drain current and a constant drain source voltage to the ISFET. In the schematic, the drain source voltage of the ISFET is equal to $I_o R$; the voltage is fixed by the action of the positive feedback loop consisting of the opamps and the resistor. The drain current of the ISFET is maintained by the current sink I_o such that the

gate source voltage of the ISFET is fixed. Using Equation 1.8 and Table 1-2, the expressions of v_{out} can be determined and are summarized in Table 1-3 for the three operating regions of the ISFET.

Table 1-3: Expression of v_{out} in the three different operating regions

Operating region	Expression
Weak inversion	$v_{out} = V_{ref} - C - nU_T \ln \left[\frac{I_o}{I_t \frac{W}{L} \left(1 + \frac{I_o R}{V_A} \right)} \right] - 2.3\alpha U_T pH$
Triode	$v_{out} = V_{ref} - C - \frac{I_o R}{2} - \frac{1}{R \frac{W}{L} \mu_n C_{ox}} - 2.3\alpha U_T pH$
Active	$v_{out} = V_{ref} - C - \sqrt{\frac{2I_o}{\frac{W}{L} \mu_n C_{ox} (1 + \lambda I_o R)}} - 2.3\alpha U_T pH$

Table 1-3 shows that v_{out} is proportional to pH in all the operating regions. This is the direct consequence of using feedback to linearize the ISFET. The body effect of the ISFET has no impact on the linearity because the ISFET's substrate is tied to its source terminal.

The second example is an integrated ISFET voltage mode opamp in modified CMOS chips [28], [53]. Its front-end consists of the 1st stage differential long-tail pair in which the non-inverting input transistor is the ISFET. The output of the differential long-tail pair drives the second stage common source amplifier. A buffer stage can be added as the third stage if the opamp is intended for applications with a resistive loading. By feeding the output voltage

back into the inverting input, the opamp will have a closed loop gain of one. The schematic of the integrated ISFET opamp is shown in Figure 1-8.

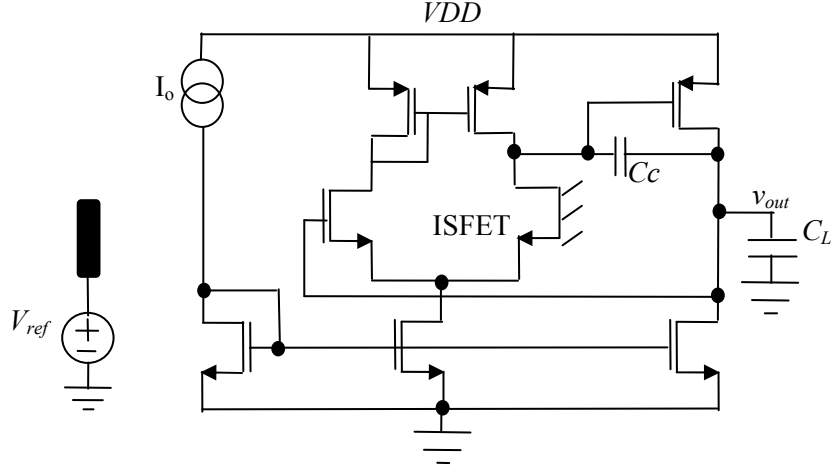


Figure 1-8: ISFET operational amplifier.

An approximation of v_{out} can be expressed as:

$$v_{out} = V_{ref} + V_{off} - 2.3\alpha U_T pH \quad (1.17)$$

where V_{off} is an offset voltage, which is temperature-sensitive but pH-insensitive [28]. Equation 1.17 shows that the output is proportional to pH. Thus, this design can be used as an integrated ISFET interface with good linearity. Beside, the ISFET and the MOSFET in the differential pair have the same potential in their source terminals, so the body effect experienced by the ISFET can be cancelled by the same body effect experienced by the

MOSFET if they are matched. Hence, either n-type ISFET or p-type ISFET can be incorporated into this design topology.

The third example is a use of current conveyors to interface ISFET. Smith and Sedra invented the second-generation current conveyor (CCII) in the early 70s. A CCII operates with the following matrix [54]:

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \quad (1.18)$$

where the $\pm$ indicates the direction of the current flow. Equation 1.18 reveals that a CCII consists of three terminals Y , X , and Z . The Y node has infinite input impedance, so the current at this node is zero. The output voltage at the X node conveys the voltage at the Y node. The output current at the Z node is mirrored from the current at the X node. These properties tell us that the impedance is zero at the X node and infinite at the Z node. Based on Equation 1.18, a CCII can be implemented as a voltage buffer, so a CCII can be used to substitute the unity gain opamp as illustrated in Figure 1-7. The current conveyor based ISFET interfacing circuit in printed circuit board (PCB) was exploited by Ghallab [55]. A schematic diagram illustrating the constant voltage, constant current source follower system is shown in Figure 1-9.

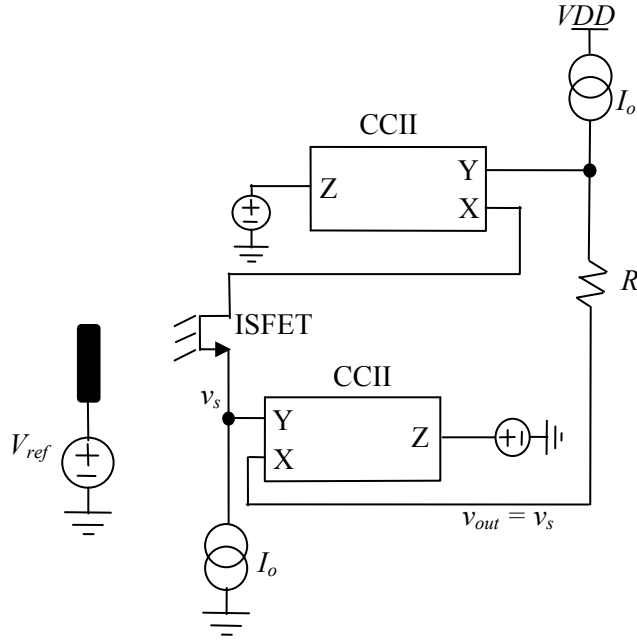


Figure 1-9: Constant voltage, constant current source follower system using 2nd generation current conveyor (CCII).

In Figure 1-9, the expressions of v_{out} in terms of pH are the same as those listed in Table 1-3 because both Figures 1-7 and 1-9 are working under the same principle and are subjected to the same bias conditions. Therefore, the expressions of v_{out} in terms of pH in Figure 1-9 are the same as in Figure 1-7..

An integrated CCII in conjunction with ISFETs is even more worthwhile to be exploited. By utilizing all the three terminals of a CCII, there are many ways to implement analogue computations such as voltage-controlled voltage source, voltage-controlled current source, integrator, differentiator, and so forth [54]. By replacing the input transistors of a class AB CCII with the ISFETs as shown in Figure 1-10, signal operation such as differentiation or integration can be implemented simply through the chemical current conveyor [56].

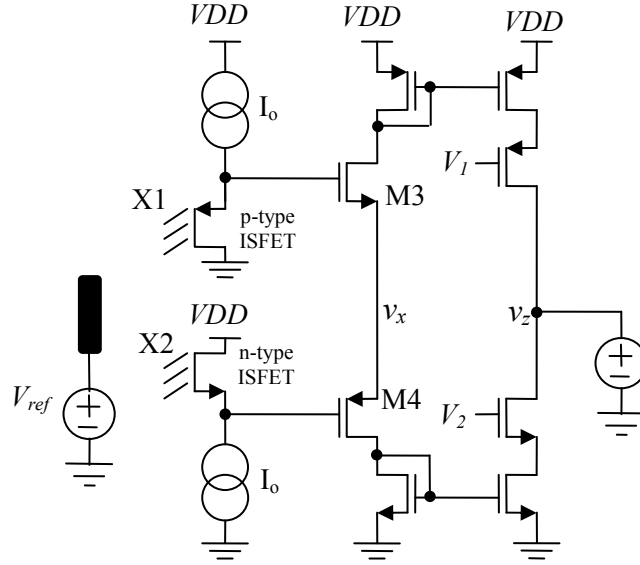


Figure 1-10: Integrated chemical current conveyor.

In Figure 1-10, node v_x is low impedance. The resistance at this node is about $1/g_m$, and this node is driven by 2 two-stage source followers. Depending on the remote gate bias, v_x can be driven by the X1-M3 two stage source followers, the X2-M4 two stage source followers, or both. When there is a change in pH of the chemical solution, the pH information will be transformed to a pH dependent voltage source in series with the remote gate bias V_{ref} . The electrical potential will push the p-type and the n-type ISFET source followers, and it will subsequently be conveyed to the node v_x . Therefore, the node v_x keeps track any change in pH. Nonetheless, the n-type devices' bulk terminals cannot be tied to their source terminals in standard p-substrate CMOS processes, so the body effect acts differently among the p-type FETs and the n-type FETs. Hence, the increase in dynamic range of this class AB chemical current conveyor comes with a non-linearity due to the

mismatch of the back gate effect. On the other hand, the node v_z is high impedance; the equivalent resistance found at this node is about $g_m r_{ds}^2$. The current flowing in the node v_z is mirrored from the current at the node v_x by the n-type and the p-type current mirrors. Thus, the operation of this integrated chemical current conveyor satisfies Equation 1.16.

1.8 Summary

This chapter has addressed the operation of ISFETs in standard CMOS chips, the non-ideal behaviour such as the trapped charges associated with ISFETs, the existing techniques to counteract the non-idealities, and a few examples of the ISFET interfacing designs. Unfortunately, the impact of the trapped charges on the ISFETs' threshold voltages can be very significant as it causes variations to circuit's operating point. In the next chapter, a well-proven design methodology will be discussed for a monolithic implementation of a robust pH to digital converter.

1.9 References

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Chapter 2

Frequency Domain Signal Processing in ISFETs Instrumentation System

In this chapter, a robust ISFETs instrumentation system which can convert analogue information due to a chemical reaction to digital signals will be investigated. In this thesis, the main consideration for building the instrumentation system in standard CMOS processes is the trapped charge effect associated with the on-chip ISFETs. Due to the unregulated trapped charges on the passivation layer and the floating metals, the ISFETs can experience variations in their threshold voltages. For instance, Bausells reported threshold voltages of ± 7 volts in his n-typed ISFETs [1], and Hammond reported threshold voltages of -33 volts to -8 volts in his p-typed ISFETs [2]. This is impossible in getting any on-chip voltage or current reference to bias these ISFETs with a 3.3 volt supply voltage. In addition, assuming that the degree of the variation of the threshold voltage can be reduced by some other means, the design of the on-chip reference is still difficult because of the uncertainty. Hence, a design solution which does not rely heavily on a voltage reference or a current reference will be pursued in this thesis. In addition, the instrumentation is targeted for hand-held applications, so low power consumption is the constraint. This chapter will discuss the operation, analysis, and simulation result of a reference-less sigma delta modulator, which does not need a voltage reference or a current reference in data conversions.

2.1 Sigma Delta Modulator Employing Voltage Controlled Oscillator: Principle of Operation

Nyquist rate data converters like integrating Analogue-to-Digital Converters (ADCs) [3], logarithmic ADCs [4], and oversampling converters like switched-cap sigma delta ADCs [5] were proposed in the past for doing a pH to digital conversion. A summary of their performance is tabulated in Table 2-1.

Table 2-1: Performance summary of pH to digital ADCs

ADC type	Number of bits	Accuracy	Power consumption	Sampling frequency	Power supply
Integrating ADC [3]	10	± 0.1 pH in pH2 to pH12	unknown	unknown	3 volts
Logarithmic ADC [4]	8	unknown	$3.3 \mu W$ in static condition	1 kHz	1 volt
$\Sigma\Delta$ ADC [5]	1	$< 2\%$ in pH2 to pH12	$9.8 mW$	6.25 MHz	1.8 volts
This work	8	$< 0.5\%$ in pH4 to pH10	$76 \mu W$ in static condition	500 kHz	1.8/3.3 volts

Although there are more converters' choices in literature than listed in Table 2-1, there is one common characteristic in those ADCs [3] – [5]. Most of the ADCs need a voltage reference or current reference for their operations, and any mismatch associated with ISFETs will bring a problem in designing the reference signal. As mentioned in the introduction of

this chapter, this thesis will pursue a reference-less instrumentation system in order to process on-chip ISFETs with mismatch. Even though the integrating ADC [3] has a higher accuracy or the logarithmic ADC [4] is a lower power, any mismatch in the ISFETs will degrade the signal to noise ratio of the system if the reference signal cannot be used efficiently. In fact, the integrating ADC [3] and the $\Sigma\Delta$ ADC [5] were evaluated only with off-chip ISFETs while the logarithmic ADC had not been verified experimentally, so it is not sure whether these ADCs can work reliably with on-chip ISFETs whose threshold voltages can be modulated by the trapped charges [6], [7].

The variation of the ISFETs' threshold voltages is an unknown to circuit designers, so the challenge to incorporate the on-chip ISFETs into the aforementioned ADCs is to determine the right level of the reference signal. In order to achieve the optimum signal to noise ratio (*SNR*) of a system with parameters mismatch, there are two possible ways. First, a built-in variable gain stage can dynamically adjust the level of the reference to achieve the best signal gain [8]. Second, with a reference-less data converter, data processing and conversions are done in frequency domain, which eliminates the dependency of a voltage or current reference. This thesis adopted a reference-less data converter because of its simple architecture, whose power consumption can be optimized more easily.

There were two distinct works in the past investigating the sigma delta frequency to digital modulators [9], [10], which are operated as 2nd order sigma delta modulation. Although they are very good at rejecting the in-band noise due to the 2nd order noise-shaping characteristics, they need a reference current in the design topology to support the operation. On the contrary, the only true reference-less sigma delta modulator were exploited in the

opened-loop 1st order sigma delta modulator [11], [12]. This reference-less sigma delta modulator uses an external sampling clock only to do the digitization of the frequency modulated signal. This type of modulator, which does not have a negative feedback loop nor require a reference signal, was further elaborated in a parallel configuration [13] to achieve a 24-bit converter. Besides, the modulator is almost independent to the power supply, and supply voltage as low as 0.3 volt was reported in the literature [14]. Therefore, there are strong motives in pursuing the opened-loop 1st order sigma delta modulator to implement an integrated ISFETs instrumentation system. The functional diagram of this reference-less sigma delta modulator is depicted in Figure 2-1 to illustrate its principles of operation.

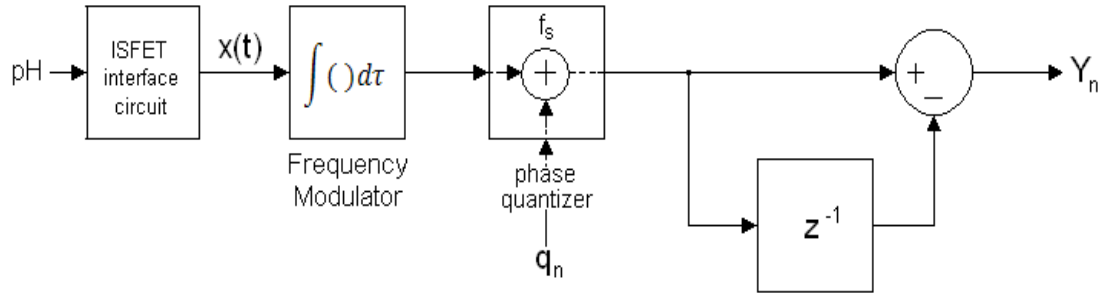


Figure 2-1: Opened-loop 1st order $\Sigma\Delta$ modulator employing a frequency modulator [11].

The modulator shown in Figure 2-1 consists of the frequency modulator⁵, the phase quantizer, the delay element, and the subtractor. The frequency modulator receives the baseband signal $x(t)$ in such a way that the baseband signal alters the carrier frequency of the frequency modulator into a new frequency or a band of frequencies. The amount of

⁵ The term “frequency modulator” and “voltage controlled oscillator” is used interchangeably in this thesis.

frequency modulation depends on the gain of the frequency modulator. Mathematically speaking, the frequency modulator is described as [15]:

$$\frac{\varphi(t)}{2\pi} = \int_{-\infty}^t (f_c + kx(\tau))d\tau \quad (2.1)$$

where $\varphi(t)$ is the instantaneous phase, f_c is the carrier frequency, and k is the gain of the frequency modulator. Equation 2.1 reveals that the phase of the frequency modulator's output carries the integral of the input signal $x(t)$. The tuning range of the frequency modulator is defined where the gain k of the frequency modulator is constant. This is illustrated in Figure 2-2.

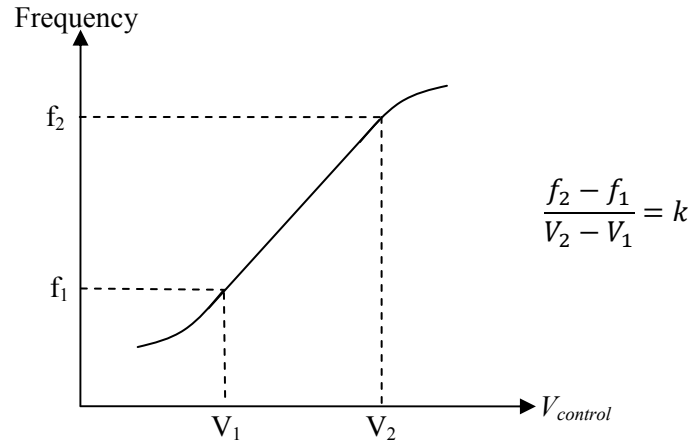


Figure 2-2: Typical frequency modulator's tuning curve

The tuning range can be specified in terms of the range of the control voltage $V_{control}$ or the range of the oscillation frequency. It will be shown in Section 2.2 that the linearity of the frequency modulator directly affects the Signal-to-Quantization Noise Ratio ($SQNR$) of the reference-less sigma delta modulator. Therefore, it is important to ensure that the frequency modulator can achieve high linearity with a large tuning range. A high linear frequency modulator is capable of achieving a higher $SQNR$, and having a large tuning range enhances the robustness of the frequency modulator to handle the mismatch of ISFETs' threshold voltages.

The function of the phase quantizer is to sample and quantize the instantaneous phase of the frequency modulated (FM) signal by the use of the sampling clock. Provided that the sampling frequency is larger than the twice of the maximum FM's frequency, a standard D flip-flop can do the phase quantization to the frequency modulated signal [11]. The phase quantization process can be thought as outputting the integer sum of the positive rising edges of the sampling clock at the current FM period; however, the quantization process adds quantized noise to the output. In other words, there is always a phase difference between the continuous FM input and the quantized output. When the sampling frequency is much larger than the twice of the maximum FM signal (i.e., oversampling), the phase of the quantized signal will match more closely to the incoming FM signal. On the contrary, when the sampling frequency is less than twice the maximum FM frequency, signal aliasing will occur. Nonetheless, the output of the phase sampler is a one-bit waveform, but it can be viewed as a serial representation of the sum of the positive rising edge of the FM signal. A graphical representation of the phase sampler's output is shown in Figure 2-2.

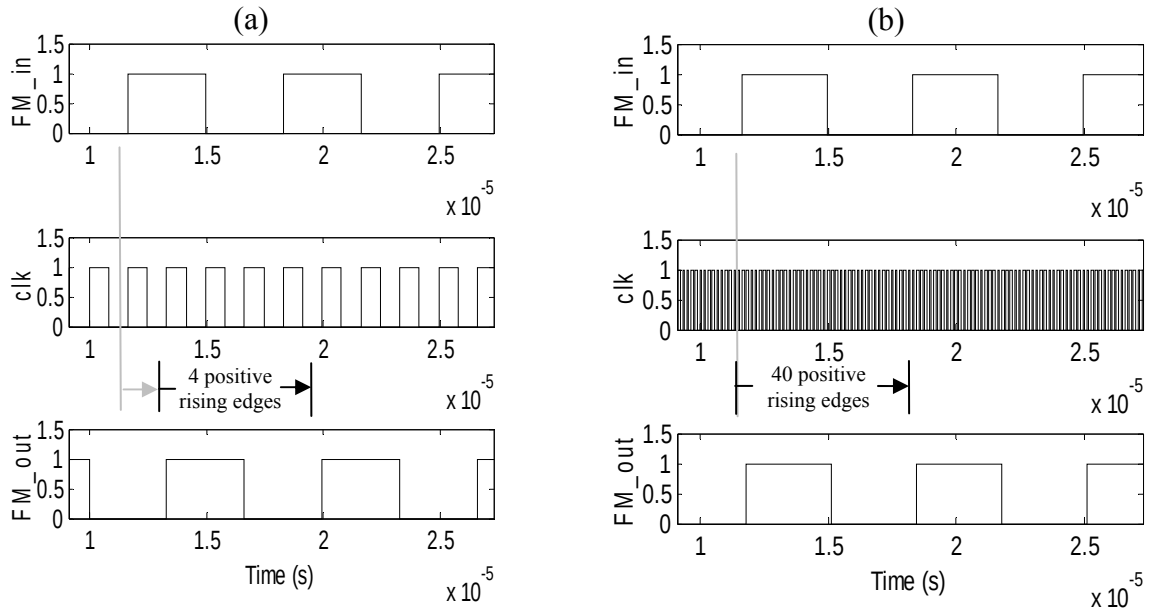


Figure 2-3: Signal waveform within the phase quantizer. (a) sampling frequency to carrier frequency of 4:1. (b) sampling frequency to carrier frequency of 40:1.

Figure 2-3a shows the input and the output waveforms of the D flip-flop with a 4:1 ratio of sampling frequency to carrier frequency. As shown, the output FM_out consumes 4 positive rising edges of the sampling clock at that current FM period. A 3-bit register can be used to represent the 4 positive rising edges of the sampling clock. To increase the resolution of the output, a higher sampling frequency can be used. Figure 2-3b shows the input and output waveforms of the flip-flop with a 40:1 ratio of sampling frequency to carrier frequency. Not only does the output phase match closely to the input phase, but the number of bits required to represent the output information also increases. In this case, a 6-bit register

is needed to represent the 40 positive rising edges of the sampling clock in that current FM period.

The delay element can be implemented simply by using a D flip-flop [11] because the input to the delay element is already synchronized to the sampling clock. The time delay added by the delay element is equal to the period of the sampling clock. The delay version of the quantized FM signal will be subtracted in the next stage.

The phase subtractor is a direct implementation of the phase differentiation by subtracting the quantized FM's phase from its previous one. In discrete time domain, it is approximating the differentiation of the FM's waveform. This can be understood by the following.

$$Y(n) = \Phi(n) - \Phi(n - 1) \quad (2.2)$$

where $Y(n)$ is the output, $\Phi(n)$ is the current quantized phase, and $\Phi(n - 1)$ is the previous quantized phase. Taking the z-transform,

$$Y(z) = \Phi(z) - z^{-1}\Phi(z)$$

$$\frac{Y(z)}{\Phi(z)} = 1 - z^{-1}$$

Substituting $z = e^{j2\pi f/f_s}$ where f_s is the sampling frequency,

$$\frac{Y(f)}{\Phi(f)} = (1 - e^{-j2\pi f/f_s}) \left(\frac{2j}{2j} \right) \left(\frac{e^{j\pi f/f_s}}{e^{j\pi f/f_s}} \right)$$

$$\frac{Y(f)}{\Phi(f)} = 2je^{-j\pi f/f_s} \sin\left(\frac{\pi f}{f_s}\right) \quad (2.3)$$

$$\left| \frac{Y(f)}{\Phi(f)} \right| = \frac{2\pi f}{f_s} \quad \text{when } f \ll f_s$$

Hence, Equation 2.3 reveals a differentiation of the quantized FM's phase in frequency domain when $f \ll f_s$. As a result, the baseband input $x(t)$ in Figure 2-1, which undergoes the analogue integration in cascade with the digital differentiation, is recovered in the digital bit-stream. In circuit implementation, the phase subtractor is achieved by using an XOR gate [11]. This is illustrated in Figure 2-4.

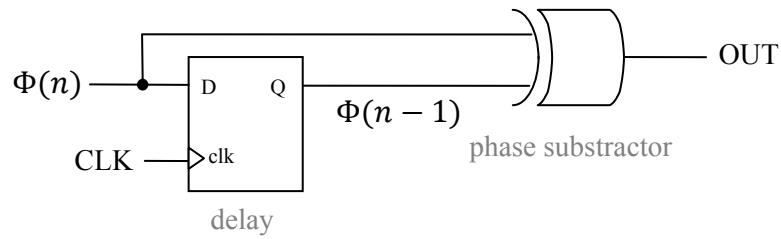


Figure 2-4: Phase subtractor

In Figure 2-4, the configuration of the D flip-flop with the XOR gate has been used elsewhere as synchronous edge detections [16], which act as a phase detector⁶ for random data. The higher is the sampling frequency; the better is the edge extraction. This is illustrated in Figure 2-5. Both Figure 2-5a and 2-5b demonstrate the edge extractions, where Figure 2-5b illustrates better edge extractions when the sampling frequency is 40 times than the input frequency.

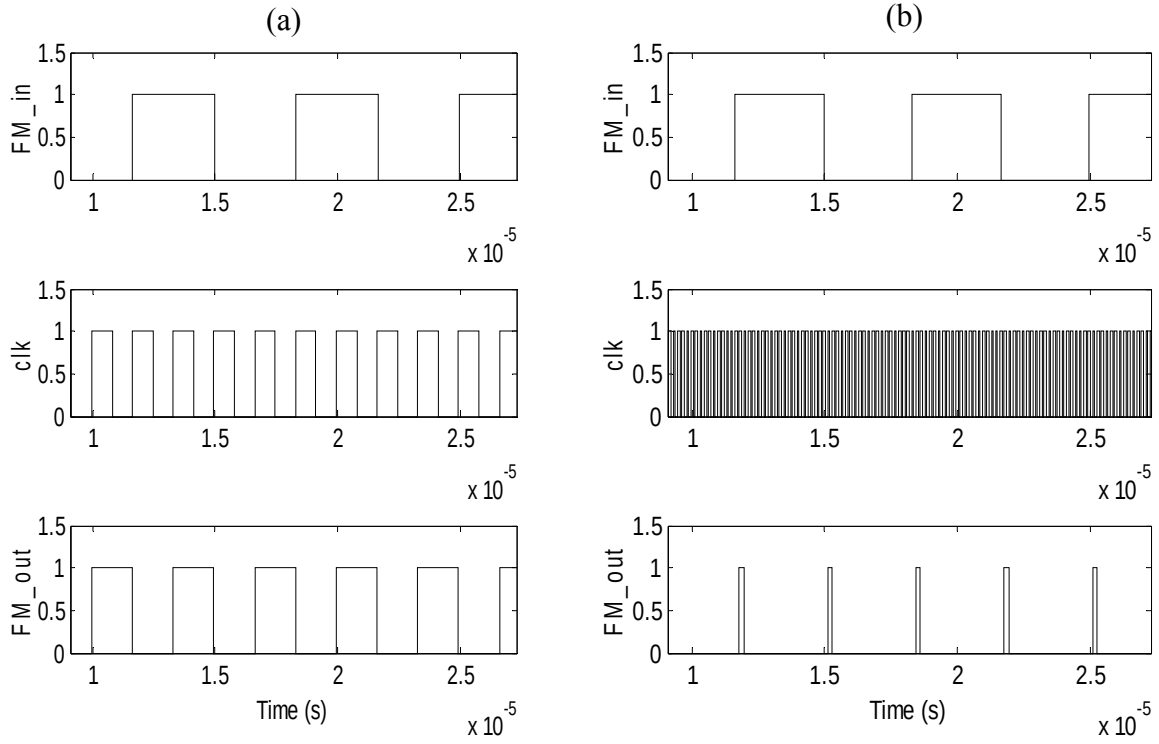


Figure 2-5: Signal representation showing frequency to digital sigma delta modulation. (a) 4:1 ratio of sampling frequency to carrier frequency. (b) 40:1 ratio of sampling frequency to carrier frequency.

⁶ In frequency domain, a phase detector subtracts two input phases [17].

Of course, the digital output Y_n as described in Figure 2-1 suffers a lot of higher frequency noise due to the first-order noise shaping characteristics [11], but the high frequency noise can be filtered by using a digital low pass filter. Beside, the oversampling nature of Y_n needs to be down-sampled to conform to the system requirement. Down-sampling can be achieved by using a digital decimator.

The entire architecture of the opened-loop $\Sigma\Delta$ modulator (or the reference-less sigma delta modulator) is very simple in terms of the circuits involved. Apart from the ISFET interface and the frequency modulator, all the remaining blocks are the digital gates. Therefore, the performance of this architecture mainly depends on the ISFETs interface and the frequency modulator. Both the ISFETs interface and the frequency modulator will be discussed in the following chapters. In the next section, a formula to compute the $SQNR$ of the reference-less $\Sigma\Delta$ modulator will be derived, and a simulation result compiled by MATLAB will be provided to assess the theoretical $SQNR$.

2.2 Sigma Delta Modulator Employing VCO: Analysis and Simulation

The relationship between the normalized phase of the continuous FM signal $\varphi(t)$ and the normalized phase of its quantized version $\varphi(n)$ is expressed as [12]:

$$\varphi(t) = \varphi(n) + \varepsilon \quad (2.4)$$

where $\varphi(n) = T_s \sum_{j=-\infty}^n [f_c + kx(j)]$, ε is the quantization error incurred during the quantization, and T_s is the sampling time. The delay element depicted in Figure 2-1 will generate a delayed version of $\varphi(n)$, which is $\varphi(n - 1)$. The digital output is obtained by subtracting $\varphi(n - 1)$ from $\varphi(n)$ [12]:

$$Y_n = \varphi(n) - \varphi(n - 1)$$

$$Y_n = T_s \sum_{j=-\infty}^n [f_c + kx(j)] + \varepsilon_n - T_s \sum_{j=-\infty}^{n-1} [f_c + kx(j - 1)] + \varepsilon_{n-1}$$

$$Y_n = T_s [f_c + kx(n)] + \varepsilon_n - \varepsilon_{n-1} \quad (2.5)$$

Equation 2.5 reveals that the output Y_n contains the baseband signal samples ($kx(nT_s)$), the offset term ($T_s f_c$), and the 1st order quantization noise ($\varepsilon_n - \varepsilon_{n-1}$). To evaluate the SQNR of this converter, the signal power and the noise power are evaluated individually; the two powers are recombined at the end to compute the overall SQNR. Assumed that the baseband signal $x(t)$ is $V_o \sin(2\pi f_b t + \phi)$. From Equation 2.5, the signal power at the output of the $\Sigma\Delta$ modulator can be expressed as:

$$S = (T_s k V_o)^2 \quad (2.6)$$

Equation 2.6 directly shows that the signal power is entirely determined by the VCO's gain k .

On the other hand, the quantization noise is assumed white⁷ to ease the calculation.

Consider the quantization error estimated from the $\Sigma\Delta$ modulator as shown in Figure 2-6.

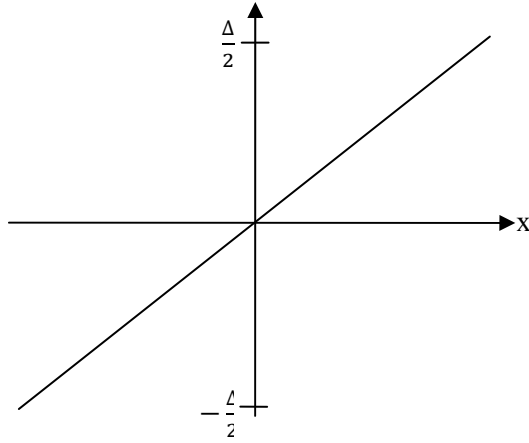


Figure 2-6: Quantization error versus input x [18].

The mean square quantization noise power can be expressed as [18]:

$$e_{rms}^2 = \frac{1}{\Delta} \int_{-\frac{\Delta}{2}}^{\frac{\Delta}{2}} x^2 dx$$

$$e_{rms}^2 = \frac{\Delta^2}{12} \quad (2.7)$$

⁷ In general, the quantization noise is not white, especially in the 1st order sigma delta modulators [18], but the quantization noise will be assumed white in this thesis in order to simplify the analysis.

where Δ is the least significant bit of the input signal. In a one-bit sigma delta modulator, $\Delta =$

1. The power spectral density of this quantization noise, when evaluated to half of the sampling frequency ($f_s/2$), is equal to:

$$N_i(f) = \begin{cases} \frac{e_{rms}^2}{f_s}, & 0 < f \leq \frac{f_s}{2} \\ 0, & \frac{f_s}{2} < f < f_s \end{cases} \quad (2.8)$$

In addition, the noise transfer function can be derived from Equation 2.5:

$$\begin{aligned} NTF &= 1 - z^{-1} \\ NTF &= (1 - e^{-j2\pi f/f_s}) \left(\frac{2j}{2j} \right) \left(\frac{e^{j\pi f/f_s}}{e^{j\pi f/f_s}} \right) \\ NTF &= 2je^{-j\pi f/f_s} \sin\left(\frac{\pi f}{f_s}\right) \end{aligned} \quad (2.9)$$

Hence, the output quantization noise power spectral density can be evaluated by multiplying the input quantization noise power spectral density with the noise transfer function:

$$\begin{aligned} N(f) &= N_i(f) \times |NTF|^2 \\ N(f) &= \frac{8e_{rms}^2}{f_s} \left[\sin\left(\frac{\pi f}{f_s}\right) \right]^2 \end{aligned} \quad (2.10)$$

Therefore, the output quantization noise power can be determined by integrating the output quantization noise power spectral density from $f = 0$ to $f = f_{max}$, where f_{max} is the bandwidth of the system.

$$\begin{aligned}
N &= \int_0^{f_{max}} N(f) df \\
N &= \int_0^{f_{max}} \frac{8}{f_s} \frac{\Delta^2}{12} \left[\sin\left(\frac{\pi f}{f_s}\right) \right]^2 df \\
N &\approx \frac{8\Delta^2}{12f_s} \int_0^{f_{max}} \frac{\pi^2 f^2}{f_s^2} df \\
N &= \frac{\pi^2 \Delta^2}{36} \left(\frac{2f_{max}}{f_s} \right)^3 \quad (2.11)
\end{aligned}$$

Combining Equations 2.6 and 2.11, the signal to quantization noise ratio can be expressed as:

$$\begin{aligned}
SQNR &= 10 \log \frac{S}{N} \\
SQNR &= 10 \log \left(\frac{kV_o}{f_s} \right)^2 - 10 \log \left[\frac{\pi^2}{36} \left(\frac{2f_{max}}{f_s} \right)^3 \right] \quad (2.12)
\end{aligned}$$

Equation 2.12 assumes that the least significant bit, $\Delta = 1$. The oversampling ratio (OSR) is defined as [18]:

$$\frac{1}{OSR} = \frac{2f_{max}}{f_s} \quad (2.13)$$

Therefore, another expression for the signal to quantization noise ratio is:

$$SQNR = 20\log\left(\frac{kV_o}{f_s}\right) - 10\log\left(\frac{\pi^2}{36} \frac{1}{OSR^3}\right) \quad (2.14)$$

From Equation 2.14, the $SQNR$ of the sigma delta modulator can be enhanced by increasing the oversampling ratio. However, increasing the OSR by increasing the sampling frequency is not efficient to improve the $SQNR$, as the signal power is inversely proportional to the sampling frequency. In fact, the $SQNR$ only improves by 3 dB for each doubling of the sampling frequency. A better way to improve the $SQNR$ is by increasing the gain k of the frequency modulator, but it is subjected to the FM's signal maximum frequency to be less than half the sampling frequency. As long as a very linear VCO is available, a high $SQNR$ can then be realized by using a higher sampling frequency with a high VCO gain [12].

For the purpose of this thesis, system level simulations in The MathWorksTM MATLAB were done to estimate the spectral characteristics of the output Y_n of the reference-less $\Sigma\Delta$ modulator. A baseband signal of $1.3 + 0.1 \times \sin(2\pi 110t)$ volts was applied into the input of an ideal VCO with transfer characteristics of $f_{FM} = 45\text{kHz} + 81 \frac{\text{kHz}}{\text{volt}} v_{in}$. The sampling frequency was 500 kHz. A Fast Fourier Transform (FFT) was carried out on the simulated output, and the power spectrum was post-processed. The spectrum is plotted in Figure 2-7.

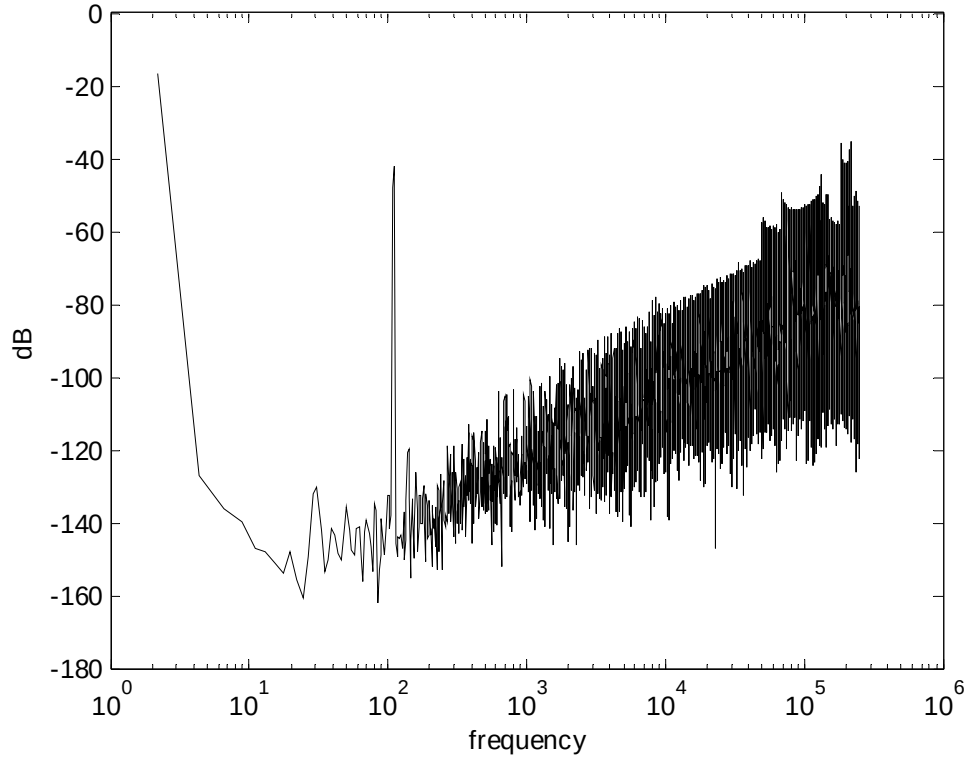


Figure 2-7: Power spectral density (input: $1.3 + 0.1 \cdot \sin(2 \cdot \pi \cdot 110 \cdot t)$ volts).

Figure 2-7 indicates that the output spectrum restores the baseband signal at 110 Hz. In addition, the noise power is shaped by +20 dB/decade in such a way that the noise is attenuated in the low frequency region. The simulated $SQNR$ is approximately 74.5 dB, while the theoretical $SQNR$ predicted by Equation 2.12 is 70.5 dB. The effective number of bit is about 13. In actual circuit implementation, however, the phase noise of the frequency modulator in silicon and the pattern noise associated with 1st order $\Sigma\Delta$ modulation will reduce the $SQNR$ [12].

2.3 Pattern Noise

For DC or slow varying input, the output of the 1st order $\Sigma\Delta$ modulator exhibits pattern noise [18]. Pattern noise also exists in the open loop sigma delta modulator [12]. The pattern noise shows various peaks at different DC input, and it appears as spurious tones in the frequency spectrum of the modulator. It is more severe in systems with a lower oversampling ratio. The effect of DC input on the in-band noise power is illustrated in Figure 2-8.

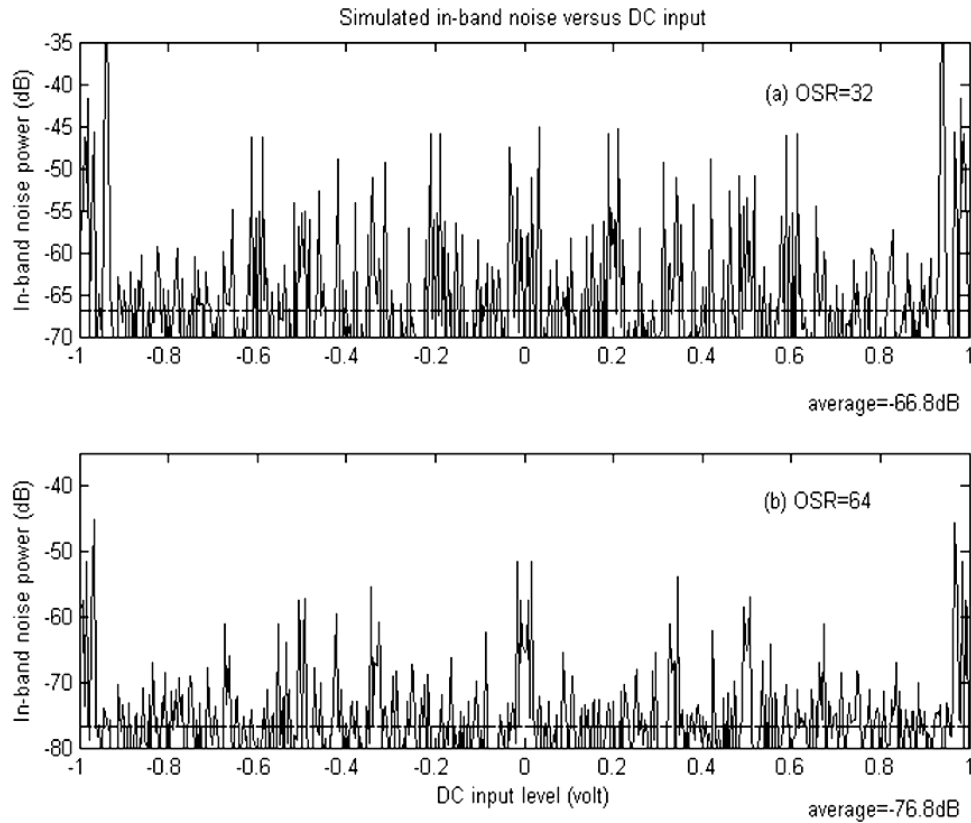


Figure 2-8: Simulated in-band noise power versus DC input. (a) Oversampling ratio of 32, and (b) oversampling ratio of 64.

Comparing Figure 2-8(a) and Figure 2-8(b), the average in-band noise power is more severe in the case of lower oversampling ratio. The height and the width of the peaks in Figure 2-8(b) are lower and lesser because of the higher oversampling ratio. Obviously, the $SQNR$ of the modulator is reduced by the pattern noise. In order to remove the pattern noise, dithering (i.e., by adding a random noise to the modulator) is commonly used.

2.4 Summary

This chapter has discussed the operation of the proposed instrumentation system based on a reference-less sigma delta modulator. The system's functional blocks have been studied, and formulae for finding the signal to quantization noise ratio have been derived to gain an insight of the modulator. System level simulation results in MATLAB have been provided to illustrate the functionality and the performance of the modulator.

2.5 References

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Chapter 3

ISFETs Averaging Array Employing Global Negative Current Feedback

Printed circuit board (PCB) prototypes evaluating the performance of using current feedback opamp as an ISFET interface were published previously in literature [1], [2]. This design topology is very robust in handling output with resistive or capacitive loading. Perhaps the simplicity of implementing an integrated averaging array which can be manipulated by this topology is the main novelty of this thesis, because the impact of the trapped charges on the on-chip ISFETs can be reduced by averaging. Thus, the use of the current feedback topology is chosen as the interface to an array of ISFETs. This chapter will start by reviewing the stability analysis and the operation of the current feedback amplifier. It will then show how the technique of using current feedback can be applied to linearize ISFETs in response to pH. A current feedback amplifier will then be modified and configured with an array of ISFETs for robust pH measurements, and the performance of the novel averaging amplifier will be analyzed by simulating a hypothetical example of 64 ISFETs with mismatch. This chapter will conclude by exploring some of the benefits in using the array of ISFETs for general pH measurements.

3.1 Stability Analysis

Figure 3-1a and 3-1b illustrate a signal flow representation of the current feedback opamp (CFOA) in non-inverting operation [3], while Figure 3-1c shows the small signal model of the CFOA's transimpedance gain, which is characterized by the dominant pole consisting of the R_T and C_T , and the output node with the capacitive load C_{OUT} . Note that the summing point in Figure 3-1b is a virtual ground, so the small signal voltage at this summing node is zero. Note also that v_{in} can be assumed to be equal to v_x in general.

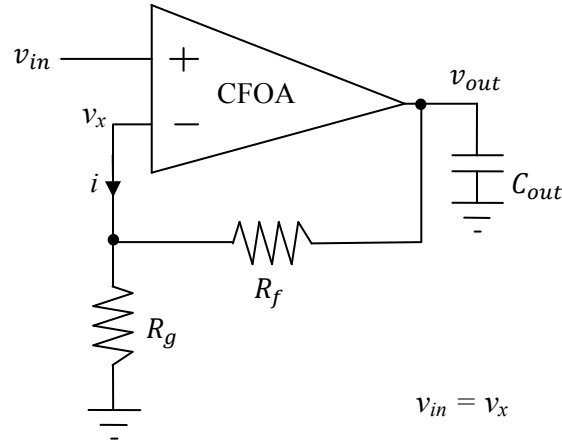


Figure 3-1a: Non-inverting voltage amplifier.

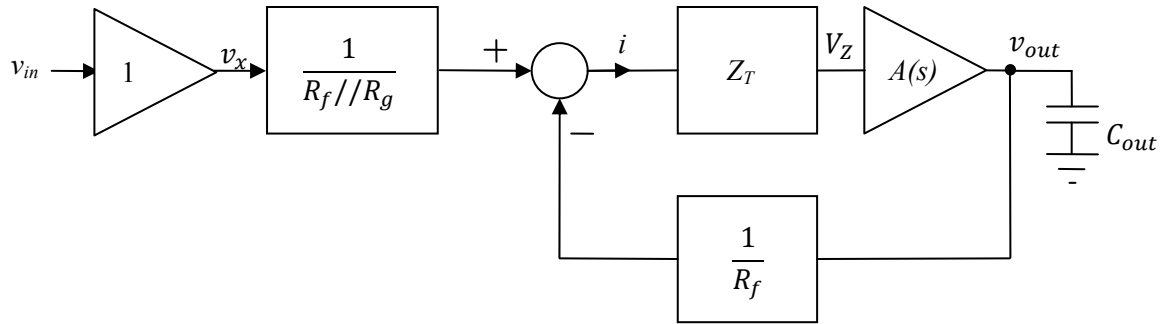


Figure 3-1b: Block diagram of the Current Feedback Opamp (CFOA) based non-inverting configuration.

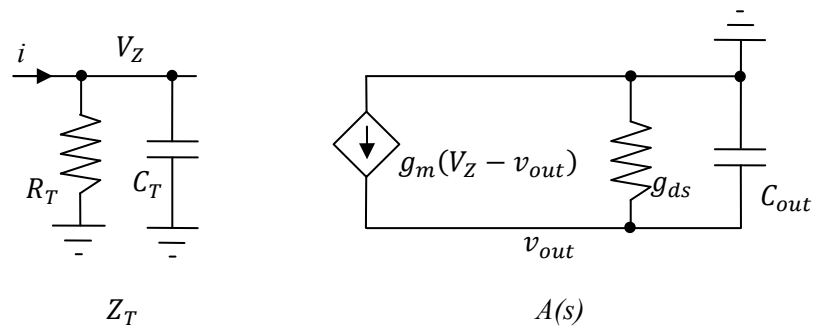


Figure 3-1c: Linear circuit representing Z_T and $A(s)$.

From Figure 3-1b, the small signal voltage gain can be expressed as:

$$\frac{v_{out}}{v_{in}} = \frac{1 + \frac{R_f}{R_g}}{1 + \frac{R_f}{Z_T A(s)}} \quad (3.1)$$

The expression of Z_T and $A(s)$ can be deduced from Figure 3-1c as:

$$Z_T = \frac{R_T}{1 + sR_T C_T} \quad (3.2)$$

$$A(s) = \frac{g_m}{g_m + g_{ds} + sC_{out}} \quad (3.3)$$

Let the small signal intrinsic gain be $\frac{g_m}{g_{ds}} = K$. It can be assumed much greater than one in the weak inversion region [4]. Equation 3.3 can be simplified as:

$$A(s) = \frac{1}{1 + s \frac{C_{out}}{g_m}} \quad (3.4)$$

Substituting Equations 3.2 and 3.4 back into Equation 3.1 and assuming that R_T is several orders of magnitude greater than the feedback resistor R_f , the small signal voltage gain in the closed loop configuration can be expressed as:

$$\frac{v_{out}}{v_{in}} = \frac{1 + \frac{R_f}{R_g}}{s^2 \frac{C_{out}}{g_m} R_f C_T + s R_f C_T + 1} \quad (3.5)$$

The small signal voltage gain at DC is reduced to $1 + \frac{R_f}{R_g}$ by taking $s = 0$ in Equation 3.5.

Note that the denominator of Equation 3.5 is a second-order polynomial of s . The pole frequency ω_n and the Quality factor Q can be derived as [5]:

$$\begin{cases} \omega_n = \sqrt{\frac{g_m}{C_{out} R_f C_T}} \\ Q = \sqrt{\frac{C_{out}}{g_m R_f C_T}} \end{cases} \quad (3.6)$$

In general, the Q should be designed to be equal to 0.707 for the amplifier to settle quickly with a step stimulus [6]. When the Q is greater than 0.707, the output will ring in response to the step stimulus [6], and it takes time for the ringing to cease. If the Q is smaller than 0.707, the amplifier will be sluggish [6]. In Equation 3.6, the magnitude of the Q is directly proportional to the square root of the ratio between the output pole $\frac{C_{out}}{g_m}$ and the dominant pole $R_f C_T$. The step responses with different Q values are shown in Figure 3-2. Note the ringing when Q is greater than 0.707.

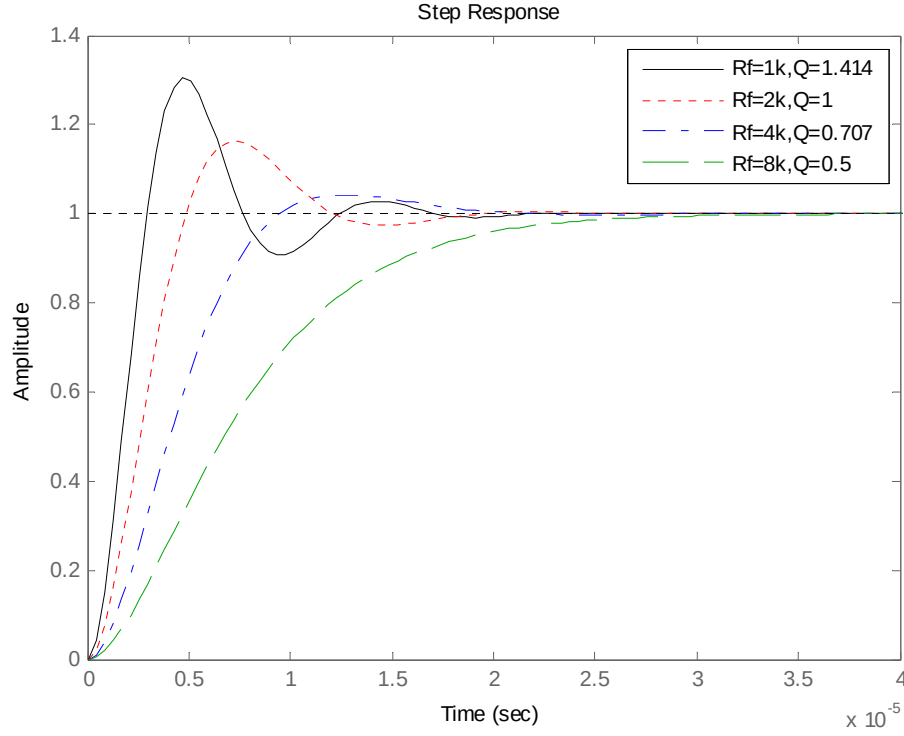


Figure 3-2: Step response under different feedback resistors (R_f) and the Quality factor (Q).

3.2 Integrated ISFET Current Feedback Opamp Design

From the discussion of the previous section, the small signal voltage gain of the CFOA is determined by the ratio of the two resistors R_f and R_g , only if Z_T is much larger than R_f . The closed loop gain at DC in non-inverting configuration is equal to $1 + \frac{R_f}{R_g}$. This gain is linear and accurate since the mismatch in the ratio of the on-chip resistors can be made less than 0.1% [7]. As a result, the linearity of this closed loop system is very good. Beside, the slew rate of CFOA is always much larger than the voltage opamp [8], [9]. Therefore, the CFOA architecture is actually a good choice for interfacing ISFET. The only drawback in using

current feedback opamp is a lower common mode rejection ratio as compared to voltage feedback opamp [9].

In n-well CMOS processes, all the p-type transistors can be isolated each other by placing the devices in their individual wells. Therefore, p-type ISFETs are used in this thesis. They can be designed to have no back gate effect by connecting their source terminals to their bulk terminals individually. They also exhibit lower flicker noise, which is the dominant noise source in ISFETs instrumentation systems, as compared to the use of the n-type FETs [7], [10]. A p-type ISFET configured with current feedback opamp topology is sketched in Figure 3-3.

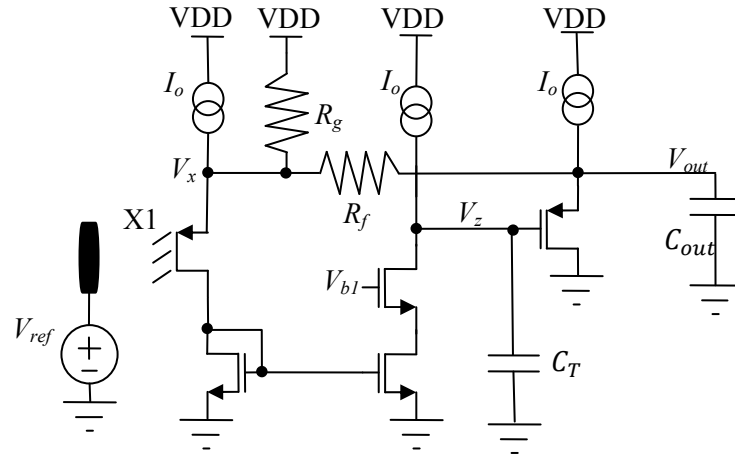


Figure 3-3: Schematic of p-type ISFET with current feedback opamp topology.

Note that in Figure 3-3, the source terminal of ISFET X1 is connected to its bulk terminal, so X1 does not experience any back gate effect. In addition, the channel length of the ISFET

is $2\ \mu m$. The channel length modulation effect is insignificant with this channel length under the $100\ nA$ current I_o . Since X1 is biased in the weak inversion region, the relationship between the biased current (I_o) and the reference electrode voltage (V_{ref}) can be expressed by Equation 3.7 [11]:

$$I_o = 2n \frac{W}{L} \mu_p C_{ox} U_T^2 \exp\left(\frac{V_x - V_{ref} + V_{th}}{nU_T}\right) \quad (3.7)$$

where $V_{th} = C + 2.3\alpha U_T pH$ is the threshold voltage of the p-type ISFET. Rearranging Equation 3.7, the expression for V_x is:

$$V_x = V_{ref} - V_{th} + nU_T \ln\left(\frac{I_o}{2n \frac{W}{L} \mu_p C_{ox} U_T^2}\right) \quad (3.8)$$

By combining the constants into K :

$$V_x = V_{ref} - K - 2.3\alpha U_T pH \quad (3.9)$$

Using Equation 3.5 by taking $s = 0$, the close loop gain of the current feedback opamp is $1 + \frac{R_f}{R_g}$. The relationship between V_{out} and V_{ref} can be expressed as:

$$V_{out} = \left(1 + \frac{R_f}{R_g}\right)(V_{ref} - K - 2.3\alpha U_T pH) \quad (3.10)$$

Equation 3.10 reveals that the amplifier can produce a linear response to pH. In addition, it has a gain of $1 + \frac{R_f}{R_g}$ added to the output, irrespective of any finite output loading. These attributes are attractive in designing ISFET's interfaces in standard CMOS technology. Nonetheless, the offset K in Equation 3.10 can be modulated by the trapped charges of the on-chip ISFET [12], [13], and it shows variations in intra- and inter-chips. In order to manage the trapped charges, averaging an array of ISFETs was developed. The averaging circuit will be treated in the next section.

3.3 ISFETs Averaging Array Employing Global Current Feedback

One modification to the topology of current feedback opamp is shown in Figure 3-4, which involves N-inputs and N-feedback networks. This is a novel topology modification of the CFOA, and it is discussed in detail now.

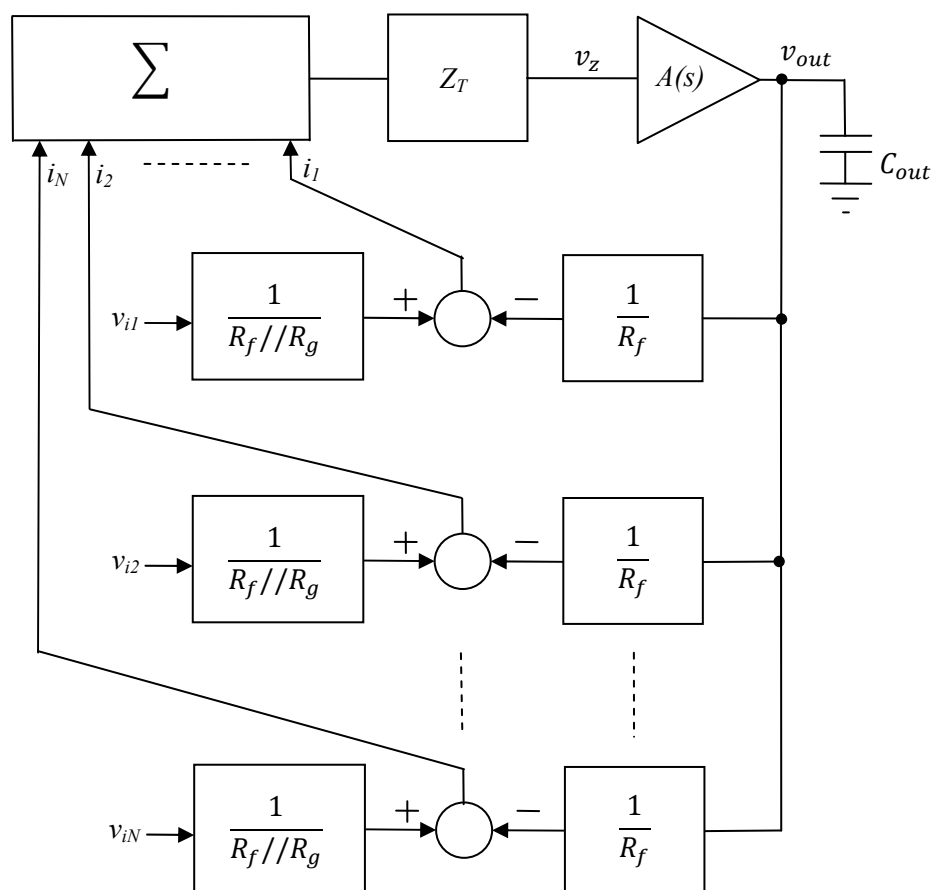


Figure 3-4: Block diagram of N- input Current Feedback Opamp (CFOA).

From Figure 3-4, the output voltage v_{out} can be expressed as:

$$v_{out} = \left(\sum_{k=1}^N i_k \right) Z_T A(s) \quad (3.11)$$

and the sum of the current i_k is:

$$\sum_{k=1}^N i_k = \sum_{k=1}^N \left[\frac{v_{i,k}}{\left(\frac{R_f R_g}{R_f + R_g} \right)} - \frac{v_{out}}{R_f} \right] \quad (3.12)$$

If Equation 3.12 is substituted back into Equation 3.11, v_{out} can be simplified as:

$$v_{out} = \left(1 + \frac{R_f}{R_g} \right) \frac{1}{s^2 \frac{R_f C_T C_{out}}{g_m} + s R_f C_T + N} \sum_{k=1}^N v_{i,k} \quad (3.13)$$

The pole frequency ω_n and the Quality factor Q^8 can be deduced from Equation 3.13:

⁸ Although a larger N increases the pole frequency of the closed loop system, it also enhances the Quality factor of the system. In other words, the stability of the closed loop system decreases as N increases. In Appendix, the mismatch of the Quality factor of a closed loop system having 2 inputs will be shown to increase due to the random variation of the feedback resistors R_f .

$$\begin{cases} \omega_n = \sqrt{\frac{Ng_m}{R_f C_T C_{out}}} \\ Q = \sqrt{\frac{NC_{out}}{R_f C_T g_m}} \end{cases} \quad (3.14)$$

From Equation 3.13, the output voltage at DC is equal to the average of the inputs times the closed loop gain:

$$v_{out} = \left(1 + \frac{R_f}{R_g}\right) \frac{1}{N} \sum_{k=1}^N v_{i,k} \quad (3.15)$$

If all the inputs, $v_{i,k}$ are originated from Equation 3.9, Equation 3.15 represents an average of the pH inputs of size N . Thus, this modified CFOA is named as an averaging array or an averaging amplifier in this thesis.

The closed loop dynamics of this averaging amplifier behave almost the same as the current feedback opamp with a single-input, as discussed in Section 3.1. The stability can only be increased if the ratio of the time constant $R_f C_T$ and the output pole increases. In addition, the 3-dB bandwidth is equal to the geometric mean of $R_f C_T$ and the output pole. This closed loop bandwidth is independent to the gain resistor R_g . Therefore, the closed loop gain and the closed loop bandwidth can be optimized individually.

An array of 64 p-type ISFETs employing global negative current feedback was investigated based on the multiple-inputs current feedback opamp [14]. The schematic is

shown in Figure 3-5, and the layout plot is displayed in Figure 3-6. On the left hand side of the layout plot, the 64 ISFETs are arranged in an 8x8 rectangular matrix.

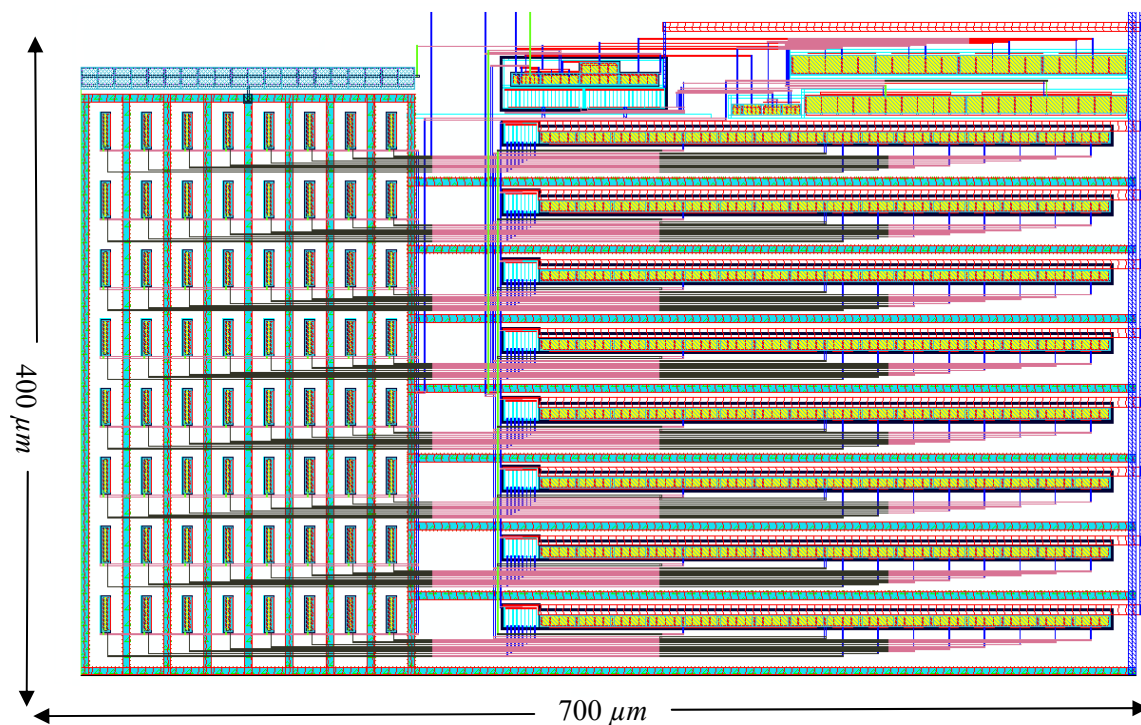


Figure 3-6: Layout plot of a 64 ISFETs averaging array.

The ISFETs averaging array shown in Figure 3-5 consists of the 64 integrated p-type ISFETs, each biased by the current sink I_o . All the ISFET's source terminals are tied to their individual wells in order to eliminate the back gate effects. By exposing the ion-sensitive layers to a chemical solution, the consequential change in the pH causes a voltage change in the source terminals V_{x1} to V_{x64} . Induced currents ($i_1, i_2, \dots, i_{64}$) are set up momentarily at their corresponding source terminal V_x , and these currents are summed together at the diode connected transistor M1. Transistor M2 mirrors the summation current from transistor M1 to the high impedance cascode node V_Z . The voltage developed at the V_Z node is immediately buffered to the output V_{out} through the source follower consisting of M6 and the bias current I_o . The output voltage is fed back to all the ISFETs' source terminals through the 64 identical resistive networks consisting of R_f and R_g ⁹. In this design, all the ISFETs are linearized by the global negative feedback from V_{out} . Thus, linearity is preserved in this closed loop system.

To enforce low power consumption, all the bias currents are restricted to 100 nA. The aspect ratio of the ISFETs is designed to be $\frac{20\mu m}{2\mu m}$ such that all the ISFETs are biased in the weak inversion region with the drain current of 100 nA. Therefore, the voltage of the source terminals V_x of the ISFETs will be the same as in Equation 3.9, and the expression is:

$$V_{x,m} = V_{ref} - K_m - 2.3\alpha_m U_T pH \quad m = 1, 2, \dots, 64 \quad (3.16)$$

⁹ In actual implementation, the R_f is 100 k Ω , and the R_g is infinite (i.e. open circuit) such that the closed loop gain of the system is one. The use of the feedback resistor R_f is a high resistive poly resistor, which has an absolute random variation of less than 15% if the resistors are spaced less than 1 μm [7].

The sum of the ISFETs' current is:

$$\sum_{m=1}^{64} i_m = \sum_{m=1}^{64} \left(\frac{V_{x,m}}{R_g} - \frac{V_{x,m} - V_{out}}{R_f} \right) \quad (3.17a)$$

The sum of feedback currents can be represented as:

$$\sum_{k=1}^N I_{feedback} = \sum_{k=1}^N I_0 - I_{M1} \quad (3.17b)$$

The output voltage is given by:

$$V_{out} = \left(\sum_{m=1}^{64} i_m \right) Z_T \frac{1}{1 + s \frac{C_{out}}{g_m}} \quad (3.18)$$

V_{out} can be derived by substituting Equations 3.16 and 3.17 into Equation 3.18:

$$V_{out} = \frac{\left(1 + \frac{R_f}{R_g} \right)}{s^2 \frac{C_{out} R_f C_T}{g_m} + s \left(R_f C_T + \frac{C_{out} R_f}{g_m R_T} \right) + \left(64 + \frac{R_f}{R_T} \right)} \sum_{m=1}^{64} (V_{ref} - K_m - 2.3 \alpha_m U_T pH) \quad (3.19)$$

The value of Z_T is very large, so V_{out} at DC can be simplified as:

$$V_{out} = \left(1 + \frac{R_f}{R_g}\right) \frac{1}{64} \sum_{m=1}^{64} (V_{ref} - K_m - 2.3\alpha_m U_T pH) \quad (3.20)$$

Therefore, the output voltage of the ISFETs averaging array is equal to the closed loop gain, $1 + \frac{R_f}{R_g}$ times the average of the 64 pH input channels. This result indicates that the unregulated trapped charges contributed to the offset K_m in Equation 3.20 are averaged with the 64 samples. The average value is very significant if it can fit the linear region of the amplifier. For instance, this thesis assumes that the trapped charges among the individual ISFETs are randomly distributed. Provided that the sample size is large enough, the mean of all the trapped charges (or the threshold voltages) of the samples will follow a normal distribution with a sample mean and a standard deviation.

Here, we used a hypothetical example of 64 ISFETs such that the mean threshold voltage of all the ISFETs is -0.7 volt with the standard deviation of 0.4 volt [15]. Although the statistics are assumed optimistically, the simulation results can reveal the characteristics of the samples and the impact of the averaging, which are illustrated in Figure 3-7. In Figure 3-7(a), it shows the assumption that there exist only few samples whose threshold voltages lying on the extreme values of either -1.7 volts or 0.2 volt. Most of the samples' threshold voltages are situated around -0.7 volts. This variation of the threshold voltages is justified by the trapped charge effects on the ISFETs. As a result of this variation, the drain current of the

individual samples can deviate significantly when the ISFETs are subjected to the same gate source voltage and the same drain source voltage. In Figure 3-7(b), there are about $700 \mu A$ differences of the samples when the ISFETs are biased under the same gate-source voltage and the same drain-source voltage.

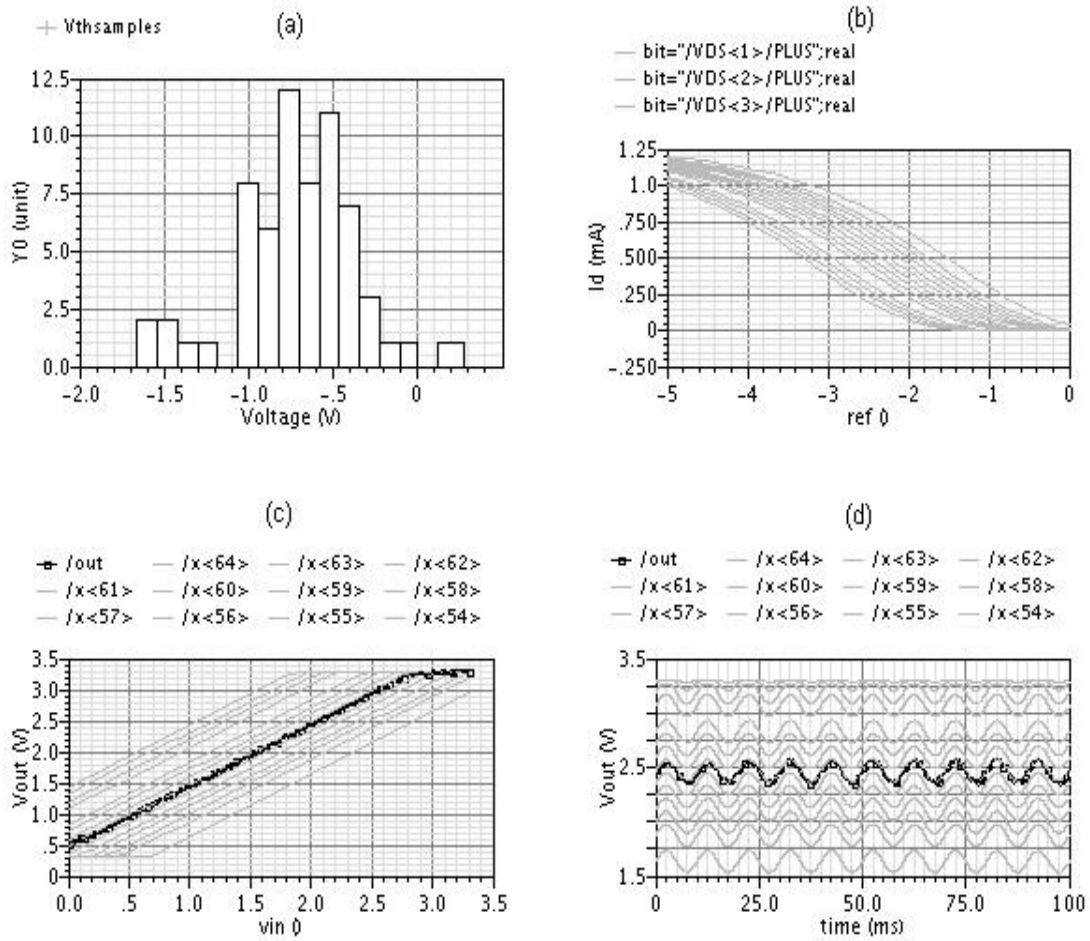


Figure 3-7: 64 pH-ISFETs averaging array with the trapped charges on 64 samples. (a) hypothetical threshold voltage's distribution, (b) simulated IV transfer characteristics, (c) DC simulation response, and (d) transient simulation response.

Figure 3-7(c) plots the output voltages of the 64-input CFOA and the 64 1-input CFOAs under a DC sweep of the reference electrode voltage. Even though some of the individual curves clip towards the power supply voltage, the output of the ISFETs averaging array, which emerges as the thicker line among all the curves, maintains a good linearity with an extended operating range. In fact, the output of this averaging array is roughly equal to the mean of the 64 single-input CFOAs. Lastly, Figure 3-7(d) plots the transient output voltages of the amplifiers versus the reference electrode voltage with a bias of $2 + 0.1 \times \sin(2\pi 100t)$ volts. Some of the samples' output of the single-input CFOA saturate to the power supply voltage, while the other single-input CFOA follow the sinusoids with different DC offsets. However, the output of the ISFETs averaging array, which is shown by the thicker line, does not distorted at all. This is because the few extreme samples have no significant impact on the aggregate average with a large sample size.

The suggestion of this ISFETs averaging array does not only reduce the impact of the trapped charges on the ISFETs' operation, but it also adds redundancy to the ISFETs on chip. The Scanning Electron Microscopy (SEM) image of the ISFETs array in which a region of the passivation layer had been accidentally scratched is shown in Figure 3-8. This mark might disturb the ISFETs' operating parameters, but there are at least 56 out of the 64 ISFETs in the averaging array operate in a normal fashion.

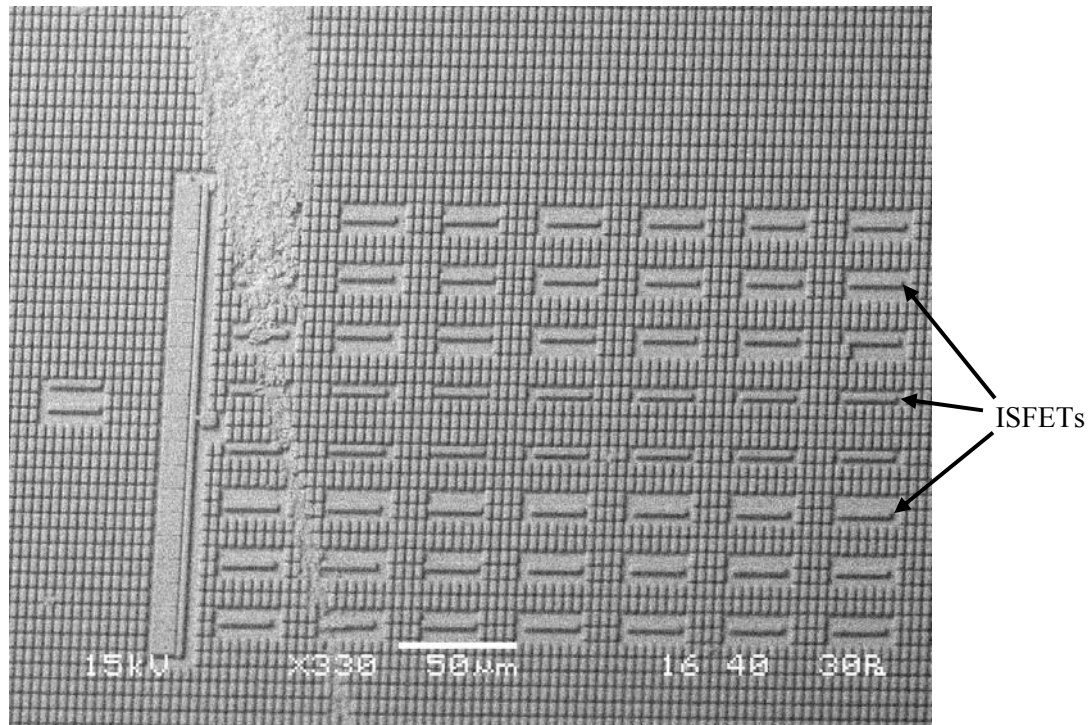


Figure 3-8: Scanning Electron Microscopy (SEM) image showing the ISFETs array with some deflections.

Apart from the redundancy, the use of an array of ISFETs could facilitate the rate of chemical equilibrium over its ion-sensitive membrane. There is an increase in the surface area to volume ratio associated with the ion-sensitive membrane in the array of ISFETs. Figure 3-9 shows the few samples of the ISFETs array. In this 3-dimensional view, the effective area to volume ratio of the ion sensitive membrane increases by splitting up a big ISFET into a number of smaller ISFETs. The array is expected to help speed up the chemical equilibrium between the hydrogen ions in a chemical solution and the passivation layer.

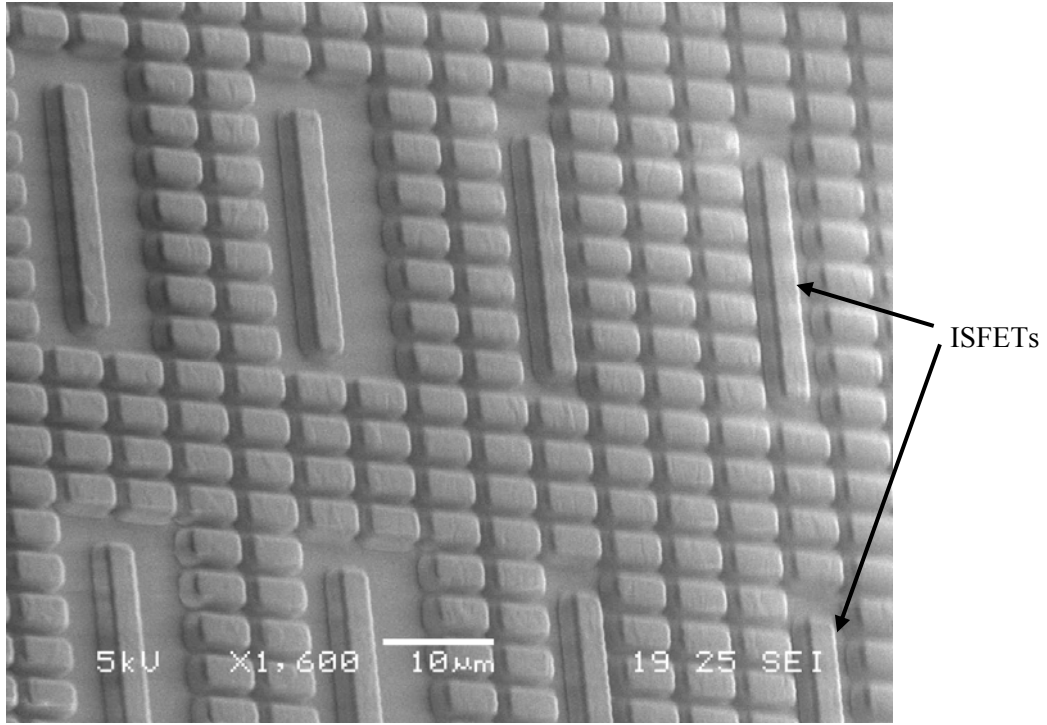


Figure 3-9: Scanning Electron Microscopy (SEM) image showing the ion-sensitive membrane in three dimensional view.

Lastly, averaging can improve the system's Signal to Noise Ratio (SNR) [16]. Consider the signal flow diagram as shown in Figure 3-10; the SNR for the single-input system can be defined as:

$$SNR_1 = 20 \log \frac{v_s}{n} \quad (3.21)$$

where v_s is the signal voltage and n is the noise voltage. On the other hand, assuming that signals can be added algebraically whereas noises are added orthogonally [16], the SNR for the k -input system can be defined as:

$$SNR_k = 10 \log \left(\frac{(\sum v_s)^2}{\sum n^2} \right) = 10 \log \frac{(k v_s)^2}{k n^2}$$

$$SNR_k = 10 \log (k) + 20 \log \frac{v_s}{n} \quad (3.22)$$

Therefore, there is $10 \log (k)$ dB improvement by taking the average of k samples.

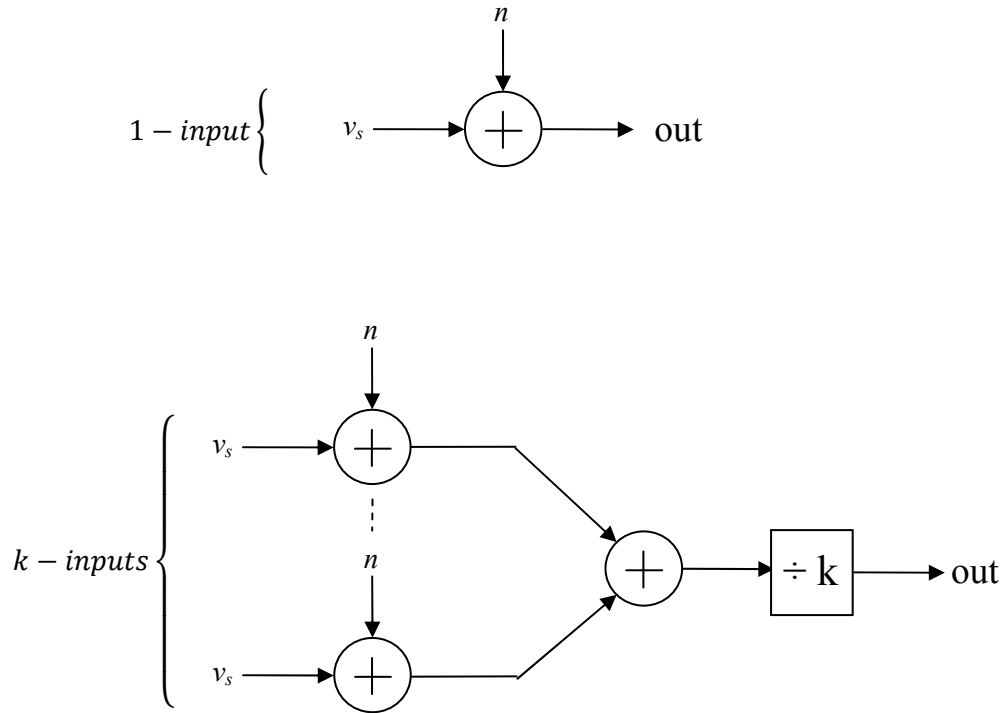


Figure 3-10: Signal flow diagram for the computation of signal to noise ratio (SNR).

The improvement of the SNR can be verified by running a transient noise analysis in Cadence® Spectre using United Microelectronics Corporation (UMC) $0.18 \mu m$ process parameters. A sinusoidal signal of $1.4 + 0.05 \times \sin(2\pi 100t)$ volts was applied to the remote gate of 64 ISFETs, each of them configured in unity-gain CFOAs. The same sinusoid also

went to a 64-input unity gain CFOA. Simulation time of 0.1 second was set to capture the output signals. The simulated data were then exported to The MathWorksTM MATLAB for undergoing a Fast Fourier transform (FFT) to obtain the power spectrum. Figure 3-11 plots the spectrum of the output V_{out} in the two different cases: 1-input and 64-input. The simulated signal power was about -30 *dBW* in both cases. However, the simulated noise floor for the 64-input was 15 *dB* lower than that for the 1-input. A signal to noise plus distortion ratio (*SNDR*) is plotted in Figure 3-12. It shows that the *SNDR* in the 64-input was about 15 *dB* higher than that with the 1-input.

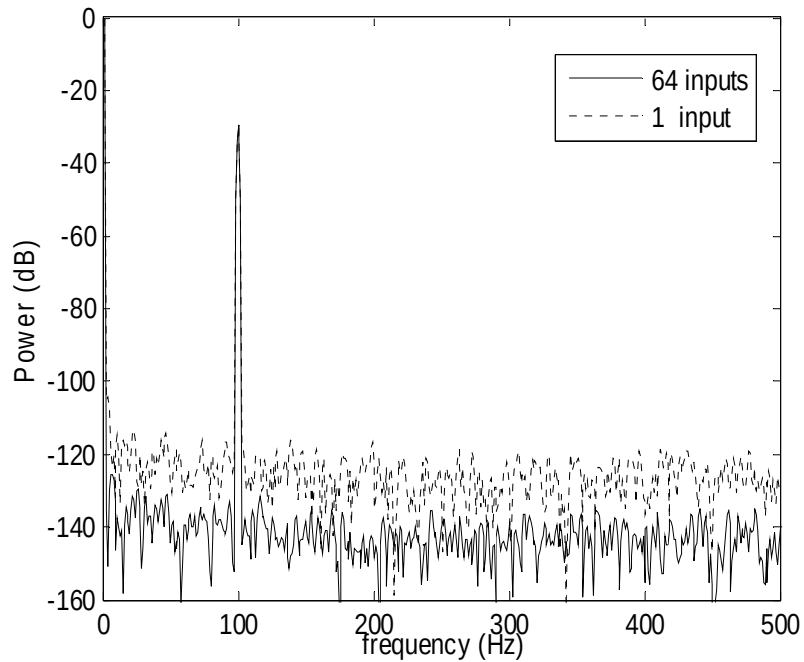


Figure 3-11: Simulated frequency spectrum of 1-ISFET and 64-ISFET input configured in unity gain current feedback opamp.

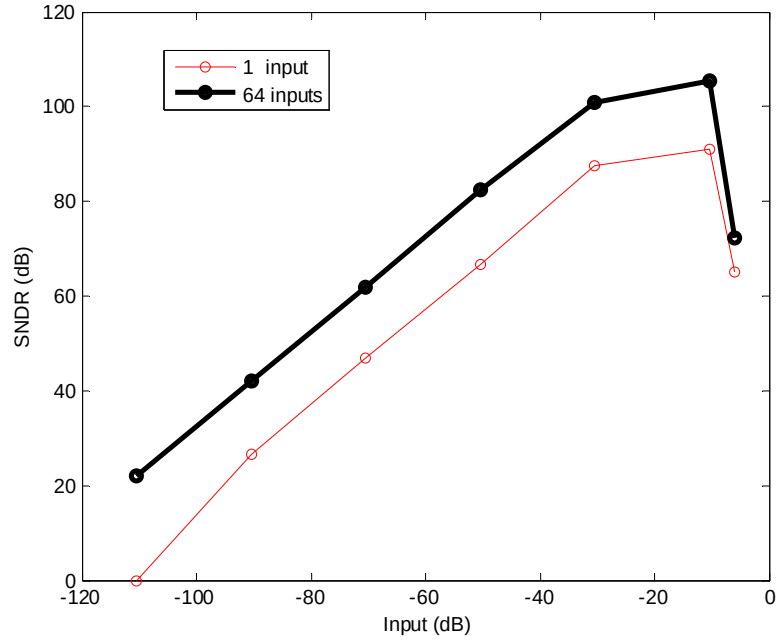


Figure 3-12: Power spectral density evaluation between 1-input and 64-input ISFETs averaging array configured in unity gain current feedback opamp.

3.4 Summary

This chapter has discussed the various aspects of using current feedback to interface ISFETs. A novel ISFET averaging array was discussed in an attempt to counter-balance the trapped charges of the individual CMOS ISFETs. Since the trapped charges can modulate the threshold voltage of an ISFET into unpredictable value, they can make the on-chip bias difficult to be applied on an array of ISFETs. On the other hand, not only does the averaging array achieve a linear response to pH, but also it provides redundancy to the system. In addition, this chapter has shown how the averaging array can improve the signal to noise

ratio (SNR) of the system by increasing the sample size. The signal to noise ratio can be enhance more by using a larger sample size, as more signals can be added algebraically whereas the noises can only be added orthogonally. However, as the sample size increase, both the power consumption and the chip area increase. Thus, there is a trade off between the accuracy, the power, and the chip area with the averaging array.

3.5 References

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Chapter 4

Log Domain Voltage Controlled Oscillator

This chapter will investigate the design of a high linear voltage controlled oscillator (VCO) suitable for the reference-less sigma delta modulator [1]. A VCO receives the baseband signal which modulates the VCO's oscillation frequency in the form of Equation 2.1. In practice, the frequency modulation is restricted to the tuning range so that the VCO is operating in its linear region. The amount of the frequency modulation depends on the gain of the VCO [2]. It was mentioned in Chapter 2 that the *SQNR* of the reference-less sigma delta modulator depends very much on the linearity of the VCO. Therefore, a high linear VCO is highly desirable in this thesis. It will be shown in terms of synthesis and analysis that the log domain voltage controlled oscillator is a very high linear VCO. The log domain VCO has never been reported in silicon implementation, so another aim of this thesis is to provide the silicon performance of a log domain VCO to literature.

4.1 Oscillator in Linear System Theory

A simple harmonic oscillator can be represented by the following transfer function:

$$\frac{Y(s)}{U(s)} = H(s) = \frac{\omega_o^2}{s^2 + \omega_o^2} \quad (4.1)$$

where ω_o represents the natural frequency of oscillation. The oscillator has an infinite Q factor, which means that the poles of the oscillator are located on the $j\omega$ axis of the s -plane [3]. There is no energy loss from the oscillator to its surrounding at that resonant frequency.

Equation 4.1 can be transformed to a set of state space equations. In fact, many state space representations can be mapped to Equation 4.1, and one of the expressions is [4]:

$$\begin{cases} \dot{X}_1 = \omega_o X_2 - \omega_o X_1 \\ \dot{X}_2 = \omega_o X_2 - 2\omega_o X_1 + \omega_o U \\ Y = X_1 \end{cases} \quad (4.2)$$

where variables $X_{1,2}$ and $\dot{X}_{1,2}$ are the internal state variables and the time derivatives of the state variables respectively. This set of state space equations can be transformed to a block diagram as shown in Figure 4-1:

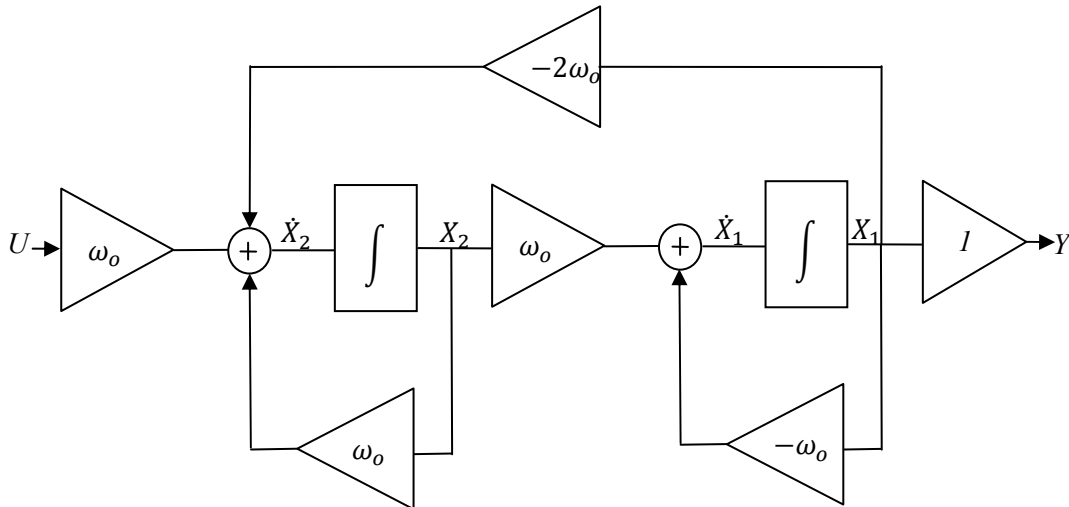


Figure 4-1: Signal flow representation of the simple harmonic oscillator.

Simulations in The MathWorksTM Simulink were done to probe the waveforms of the input signal U , the output signal Y , and the internal signals $X_{1,2}$ and $\dot{X}_{1,2}$. The value of ω_o was set to 2π , which corresponds to a frequency of 1 Hz. Figure 4-2 plots all the various waveforms associated with the oscillator in 10 oscillations.

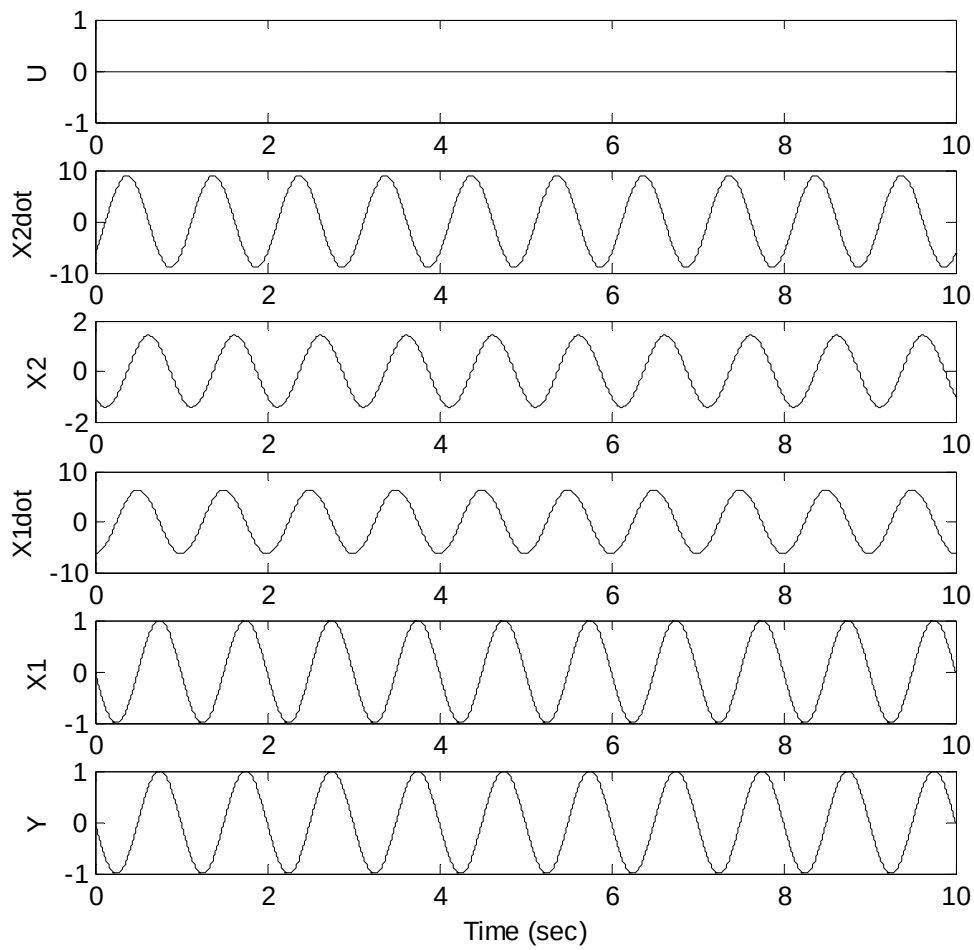


Figure 4-2: Plot of input, output, and internal signals of the simple harmonic oscillator over 10 seconds.

Figure 4-2 shows that except for the DC input U , all the other signals are a pure sinusoid of frequency 1Hz, but they have different amplitudes. The amplitude of the time derivative signals $\dot{X}_1$ and $\dot{X}_2$ is several times larger than the output Y , so design consideration needs to ensure that these internal signals are not distorted. Otherwise, harmonics, as well as the fundamental frequency, will be generated at the output. In circuit implementation, an opamp RC integrator shown in Figure 4-3 can be used to realize the integrator as shown in Figure 4-1.

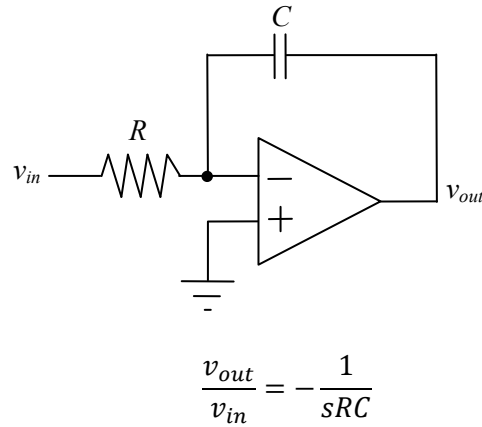


Figure 4-3: Opamp RC integrator.

Because of the negative feedback via the capacitor, the amplifier can become unstable if the amplifier is not internally frequency compensated. One way to compensate the frequency response of the amplifier is by adding a capacitor at the dominant pole of the opamp. This can increase the circuit stability, but it reduces the amplifier's speed [5]. In applications where the operating frequency is up to few hundred kHz, the use of the opamp RC integrator to construct the linear oscillator in Figure 4-1 presents no major problem.

Unfortunately, the use of the opamp RC integrator to synthesize a linear oscillator suffers from extra power dissipation associated with the opamp. In addition, the RC time constant is fixed, so the frequency of oscillation cannot be tuned. Furthermore, the noise generated from the opamp can deteriorate the phase noise of the oscillator. Therefore, using an opamp RC integrator to realize a voltage controlled oscillator might not be a good choice.

4.2 Log Domain Signal Processing

The pioneer work of log domain signal processing was done by Adams who applied the technique of compressing and expanding in signal processing. Adams' log domain filter starts by compressing the input signal so that the filter can handle a larger input dynamic range. After the signal filtering, the signal is expanded at the output so that it restores the input signal back without any distortion. The current mode log domain low pass filter proposed by Adams is shown in Figure 4-4 [6].

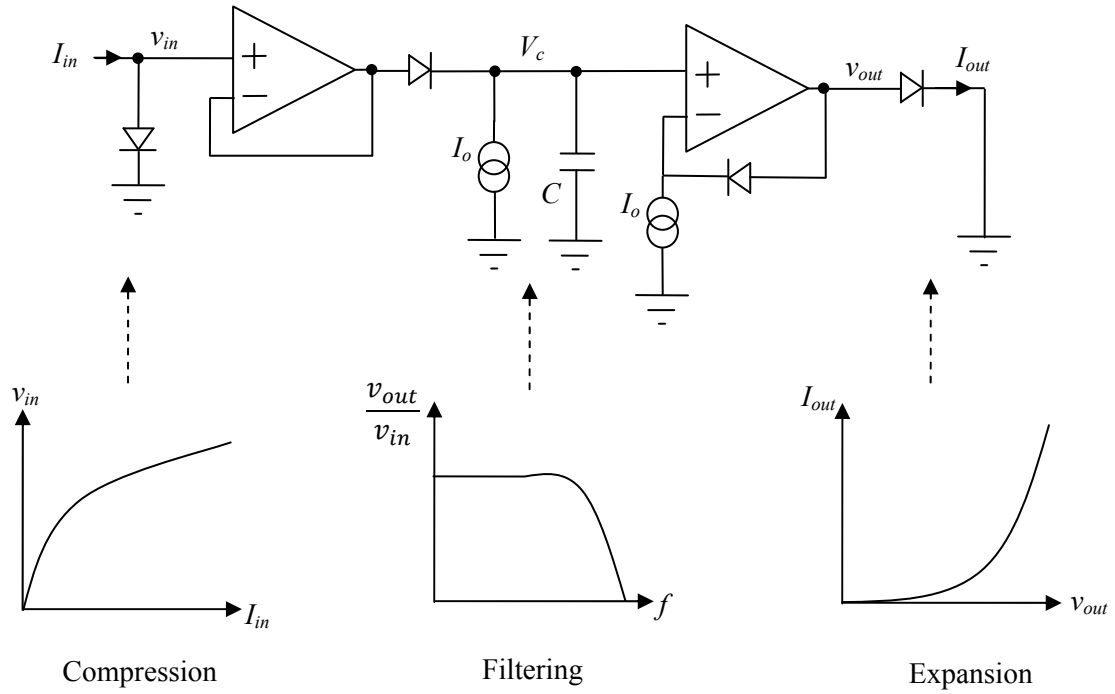


Figure 4-4: Adam's log domain filter.

Note that:

$$I_{out} = I_o \exp\left(\frac{V_c}{U_T}\right) \quad (4.3)$$

Taking a time derivative of Equation 4.3 and multiplying the result by C yields the following equation:

$$C\dot{V}_c = CU_T \frac{\dot{I}_{out}}{I_{out}} \quad (4.4)$$

KCL at node V_c results in the following equation:

$$C\dot{V}_c = I_s \exp\left(\frac{v_{in} - V_c}{U_T}\right) - I_o \quad (4.5)$$

and the input I_{in} and v_{in} have a exponential relationship:

$$I_{in} = I_s \exp\left(\frac{v_{in}}{U_T}\right) \quad (4.6)$$

Solving Equations 4.4, 4.5, and 4.6 together, the following linear 1st order differentiation equation is obtained:

$$\dot{I}_{out} + \frac{I_o}{CU_T} I_{out} = \frac{I_o}{CU_T} I_{in} \quad (4.7)$$

Subsequent work on the log domain signal processing was reported by Seevinck [7] who proposed an integrated class AB current mode integrator. The circuit operation was similar to Adams' idea, but the design was an integrated design with class AB performance. Years after Seevinck's work on the log domain integrator, Frey outlined a systematic procedure to synthesize linear filters based on the exponential state space concept [6], [8], [9]. Works following Frey's exponential state space synthesis were diversified by the signal flow graph approach from Perry and Robert [10], the modular approach from Mahattanakul and

Toumazou [11], the Dynamic Translinear Principle (DTP) approach from Mulder et al. [12], and the Bernoulli Cell approach by Drakakis [13].

The filter (or the oscillator) synthesis procedure adopted in this thesis is based on Frey's exponential state space variables mapping, which generally starts with a linear state space representation of a filter, such as an integrator whose linear state space representation can be expressed as:

$$\begin{cases} \dot{X} = \omega_o U \\ Y = X \end{cases} \quad (4.8)$$

The next step is to transform Equation 4.8 into a set of non-linear state space equations through the exponential state variable mappings. As studied by Tsvividis [14], the transformation from a linear system function into a non-linear system function is legitimate as long as the input/output and the initial state conditions remain unchanged. For instance, if the following exponential state variables mapping is chosen:

$$\begin{cases} X = I_x \exp(gV_x) \\ U = I_u \exp(gV_u) \end{cases} \quad (4.9)$$

where the value of g is equal to the inverse of the thermal voltage ($g = \frac{1}{U_T} = \frac{q}{kT}$) as in the case of a bipolar transistor, or a MOSFET in the weak inversion ($g = \frac{1}{nU_T} = \frac{q}{nkT}$).

Substituting Equation 4.9 back into Equation 4.8:

$$\begin{aligned}\dot{V}_x &= \frac{1}{g} \omega_o \frac{I_u}{I_x} \exp[g(V_u - V_x)] \\ C\dot{V}_x &= C\omega_o \frac{1}{g} \frac{I_u}{I_x} \exp[g(V_u - V_x)]\end{aligned}\quad (4.10)$$

Equation 4.10 reveals that a current ($C\dot{V}_x$) going into a capacitor at node V_x is supplied by a current bias in the form of $C\omega_o \frac{1}{g} \frac{I_u}{I_x} \exp[g(V_u - V_x)]$. Next, the following assignments were chosen in order to simplify Equation 4.10:

$$\begin{cases} C\omega_o \frac{1}{g} = I_o \\ I_x = I_o \\ I_u = I_s \end{cases} \quad (4.11)$$

Equation 4.10 and the output Y can now be formulated as:

$$\begin{cases} C\dot{V}_x = I_s \exp[g(V_u - V_x)] \\ Y = I_o \exp[g(V_x)] \end{cases} \quad (4.12)$$

Equation 4.12 reveals directly the details of the current mode integrator in CMOS implementation as shown in Figure 4-5.

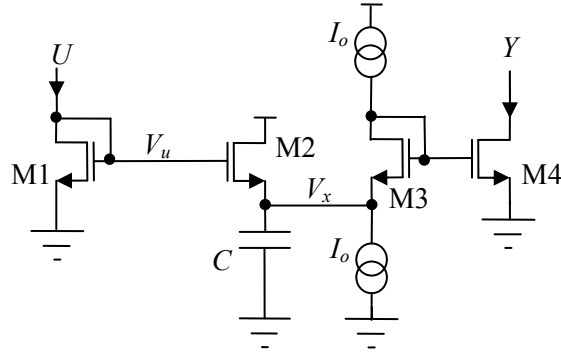


Figure 4-5: CMOS log domain integrator.

The choice to assign Equation 4.11 can yield different circuit topologies. For instance, if the assignments are:

$$\begin{cases} C\omega_o \frac{1}{g} = I_o \\ I_x = I_s \\ I_u = I_s \end{cases} \quad (4.13)$$

The non-linear state space representation will end up as:

$$\begin{cases} C\dot{V}_x = I_o \exp[g(V_u - V_x)] \\ Y = I_s \exp[g(V_x)] \end{cases} \quad (4.14)$$

The circuit topology becomes:

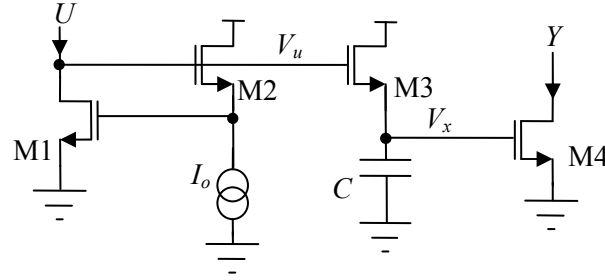


Figure 4-6: Another CMOS log domain integrator.

In order to verify that the circuit shown in Figure 4-5 is an integrator, the first step is to obtain the input/output relationship of the circuit. This can be done by examining the Translinear loop (TL) comprising the input and the output. In Figure 4-5, there is one Translinear loop consisting of transistors M1, M2, M3, and M4. Therefore, assuming that these transistors are matched, the product of the current densities in the clockwise direction of the loop is equal to the product of the current densities in the counter-clockwise direction of the loop. This is the application of the Translinear Principle [15]:

$$(I_{d1})(I_{d3}) = (I_{d2})(I_{d4})$$

$$(U)(I_o) = (i_c)(Y) \quad (4.15)$$

Note that the output Y is related to the capacitor's current by:

$$Y = I_o \exp[g(V_x)]$$

$$\begin{aligned}\dot{Y} &= gY\dot{V}_x \\ \therefore i_C &= C\dot{V}_x = \frac{C}{g} \frac{\dot{Y}}{Y}\end{aligned}\quad (4.16)$$

Substitution Equation 4.16 back into Equation 4.15 results in the equation:

$$\begin{aligned}UI_o &= \left(\frac{C}{g} \frac{\dot{Y}}{Y}\right) Y \\ \dot{Y} &= U \frac{gI_o}{C}\end{aligned}$$

Taking Laplace transform,

$$\frac{Y(s)}{U(s)} = \frac{gI_o}{sC} = \frac{\omega_o}{s} \quad (4.17)$$

where $\omega_o = \frac{gI_o}{C} = \frac{I_o}{nC U_T}$ is the pole frequency. Therefore, Equation 4.17 confirms that the circuit in Figure 4-5 is an integrator. The merit of this log domain integrator is that the pole frequency is linearly proportional to the bias current I_o . Thus, it allows a simple and a direct frequency tuning. In addition, the internal nodal voltage at the capacitor is compressed, so this integrator can work in a low supply voltage environment. Beside, this integrator does not need any frequency compensation because there is no negative feedback. Therefore, the

speed of this integrator can be maximized, subjected to the constraint of the power consumption.

Simulations in The MathWorksTM Simulink were done to probe all the signal waveforms of the CMOS log domain integrator, liked the one shown in Figure 4-5. The simulation results are plotted in Figure 4-7. Note that the internal nodal voltage V_x is compressed, which is caused by the non-linear transformation from a current signal to a voltage signal. Note also that the input U leads the output Y by 90 degrees, which verifies that the circuit is operating as an integrator.

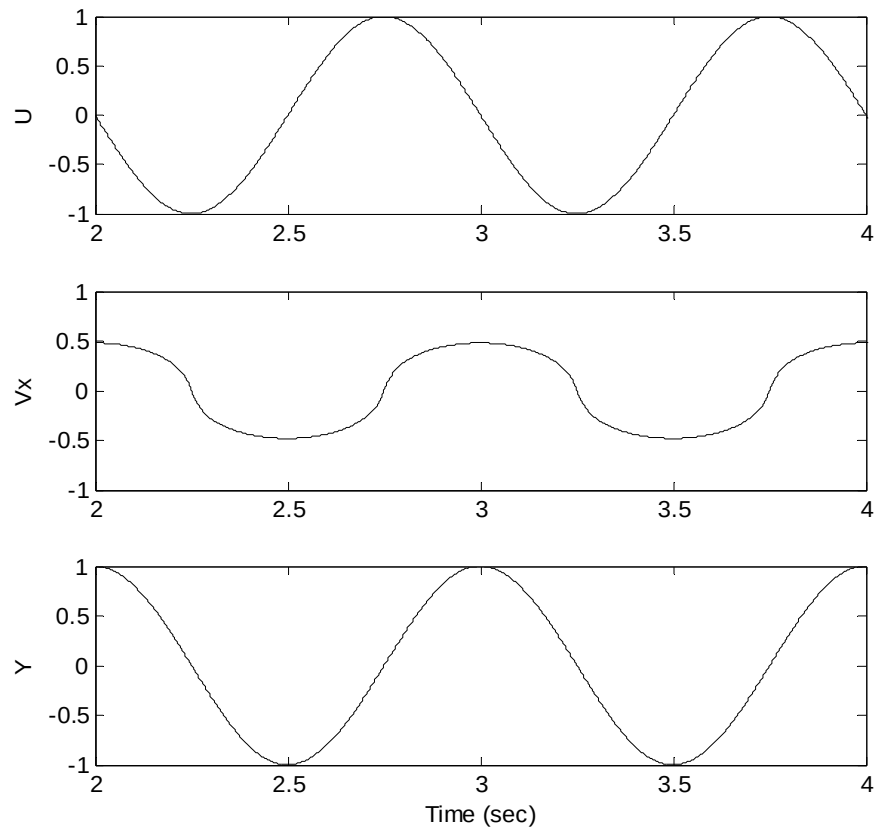


Figure 4-7: Signal waveforms in log domain integrator with input U , internal nodal V_x , and output Y .

4.3 Log Domain Oscillator Synthesis

This section outlines the steps required to synthesize a log domain oscillator by using the exponential state space variables approach. The reason of using a log domain oscillator in this thesis is that the oscillator is a very high linear VCO. In order to realize a log domain oscillator in CMOS, the transistors are biased in the weak inversion region in order to achieve the required dynamics. Thus, it is low power in general. Besides, both the Q value and the oscillation frequency of a log domain oscillator are tuned individually by 2 different bias currents. An oscillator with a high Q value can achieve low phase noise [16], [17].

The synthesis procedure starts by using the state space representation of a simple harmonic oscillator, which is expressed again as Equation 4.18:

$$\begin{cases} \dot{X}_2 = \omega_o X_2 - 2\omega_o X_1 + \omega_o U \\ \dot{X}_1 = \omega_o X_2 - \omega_o X_1 \\ Y = X_1 \end{cases} \quad (4.18)$$

This set of linear state space equations can be transformed into a set of exponential state space equations. First, the following exponential state variable mappings are applied [4].

The X_1 , X_2 , and U are current, while V_1 , V_2 , and V_u are voltage:

$$\begin{cases} X_1 = I_1 \exp\left(\frac{V_1}{nU_T}\right) \\ X_2 = I_2 \exp\left(\frac{V_2}{nU_T}\right) \\ U = I_u \exp\left(\frac{V_u}{nU_T}\right) \end{cases} \quad (4.19)$$

These exponential state variable mappings are analogous to the drain current of a MOSFET operating in the weak inversion region. Assuming that the back gate effect and the channel length modulation effect are not taken into consideration, the drain current of a MOSFET can be reduced to:

$$i_D = 2n \left(\frac{W}{L} \right) \mu C_{ox} U_T^2 \exp \left(\frac{v_{GS} - V_{th}}{nU_T} \right)$$

$$i_D = I_s \exp \left(\frac{v_{GS}}{nU_T} \right) \quad (4.20)$$

which is the same expression in Equation 4.19. The time derivative of the state variables X_1 and X_2 are expressed as:

$$\begin{cases} \dot{X}_2 = \frac{X_2}{nU_T} \dot{V}_2 \\ \dot{X}_1 = \frac{X_1}{nU_T} \dot{V}_1 \end{cases} \quad (4.21)$$

Substituting Equations 4.19 and 4.21 into Equation 4.18 gives the following result:

$$\begin{cases} \dot{V}_2 = n\omega_o U_T - 2n\omega_o U_T \frac{X_1}{X_2} + n\omega_o U_T \frac{U}{X_2} \\ \dot{V}_1 = n\omega_o U_T \frac{X_2}{X_1} - n\omega_o U_T \\ Y = I_1 \exp \left(\frac{V_1}{nU_T} \right) \end{cases}$$

$$\begin{cases} C\dot{V}_2 = nC\omega_o U_T - 2nC\omega_o U_T \frac{X_1}{X_2} + nC\omega_o U_T \frac{U}{X_2} \\ C\dot{V}_1 = nC\omega_o U_T \frac{X_2}{X_1} - nC\omega_o U_T \\ Y = I_1 \exp\left(\frac{V_1}{nU_T}\right) \end{cases} \quad (4.22)$$

Next, the following assignments are chosen to manipulate Equation 4.22 [69]:

$$\begin{cases} I_o = nC\omega_o U_T \\ I_1 = I_o \\ I_2 = I_s \\ I_u = \frac{I_s^2}{I_o} \end{cases} \quad (4.23)$$

With Equation 4.23, Equation 4.22 can be simplified to:

$$\begin{cases} C\dot{V}_2 = I_o - 2\frac{I_o^2}{I_s} \exp\left(\frac{V_1 - V_2}{nU_T}\right) + I_s \exp\left(\frac{V_u - V_2}{nU_T}\right) \end{cases} \quad (4.24a)$$

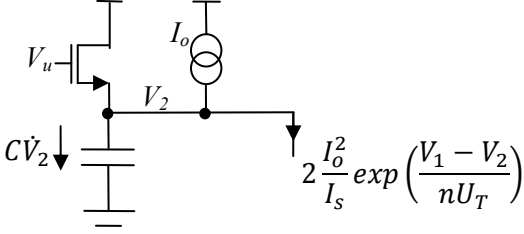
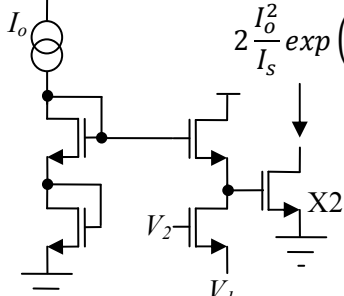
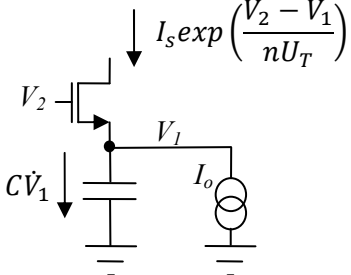
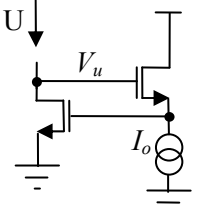
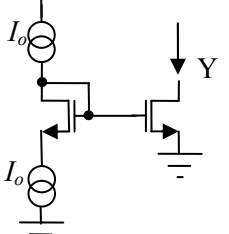
$$C\dot{V}_1 = I_s \exp\left(\frac{V_2 - V_1}{nU_T}\right) - I_o \quad (4.24b)$$

$$U = \frac{I_s^2}{I_o} \exp\left(\frac{V_u}{nU_T}\right) \quad (4.24c)$$

$$Y = I_o \exp\left(\frac{V_1}{nU_T}\right) \quad (4.24d)$$

To realize Equation 4.24 in terms of circuit implementations, Table 4-I shows the possible circuit building blocks [4].

Table 4-I: Circuit building blocks to realize Equation 4.24 [4].

	Equation 4.24a
	Equation 4.24a supplementary
	Equation 4.24b
	Equation 4.24c
	Equation 4.24d

A complete schematic of the log domain oscillator with controlled voltage is shown in Figure 4-8.

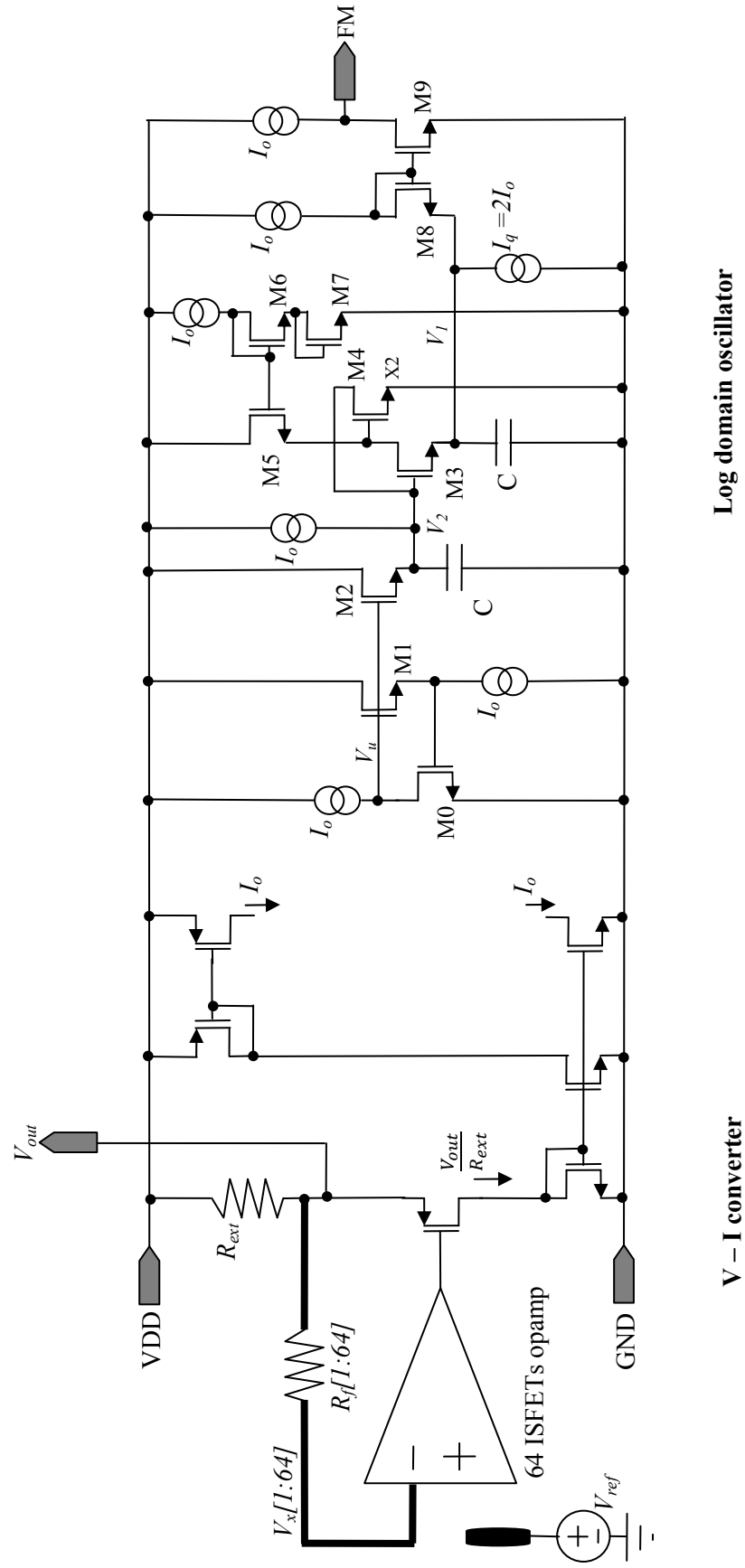


Figure 4-8: Schematic diagram showing the CMOS log domain VCO. The current bias (I_o) is established by the V - I converter consisting of the ISFETs averaging array and the external resistor R_{ext} [18].

Figure 4-8 is composed of the V – I converter cascaded with the log domain oscillator. In the figure, the V – I converter is realized by the ISFETs averaging amplifier loaded with the external resistor R_{ext} . The load current of $\frac{V_{out}}{R_{ext}}$ is set up. This current will generate all the necessary current sinks and the current sources I_o , which are used to bias the log domain oscillator. When $I_q = 2I_o$, the oscillation frequency is reduced to:

$$f_{osc} = \frac{1}{2\pi} \frac{I_o}{nC U_T} = \frac{1}{2\pi} \frac{V_{out}}{nR_{ext} C U_T} \quad (4.25)$$

Equation 4.25 predicts that the oscillation frequency of the oscillator is linearly proportional to the voltage signal V_{out} . Recall in Equation 3.20, the output voltage of the ISFETs averaging amplifier is linearly proportional to the reference electrode voltage V_{ref} and the pH, so the oscillation frequency is linear to the reference electrode voltage and the pH. In addition, the sensitivity of the log domain oscillator is equal to $\frac{1}{2\pi} \frac{1}{nR_{ext} C U_T}$, which can be adjusted directly by the external resistor R_{ext} . This adds an additional flexibility in adjusting the gain of the log domain oscillator. Transistor simulations were done using 0.18 μm CMOS process parameters to investigate the effect of the reference electrode voltage on the oscillation frequency f_{osc} . The simulation results were exported to MATLAB, and they are displayed in Figure 4-9.

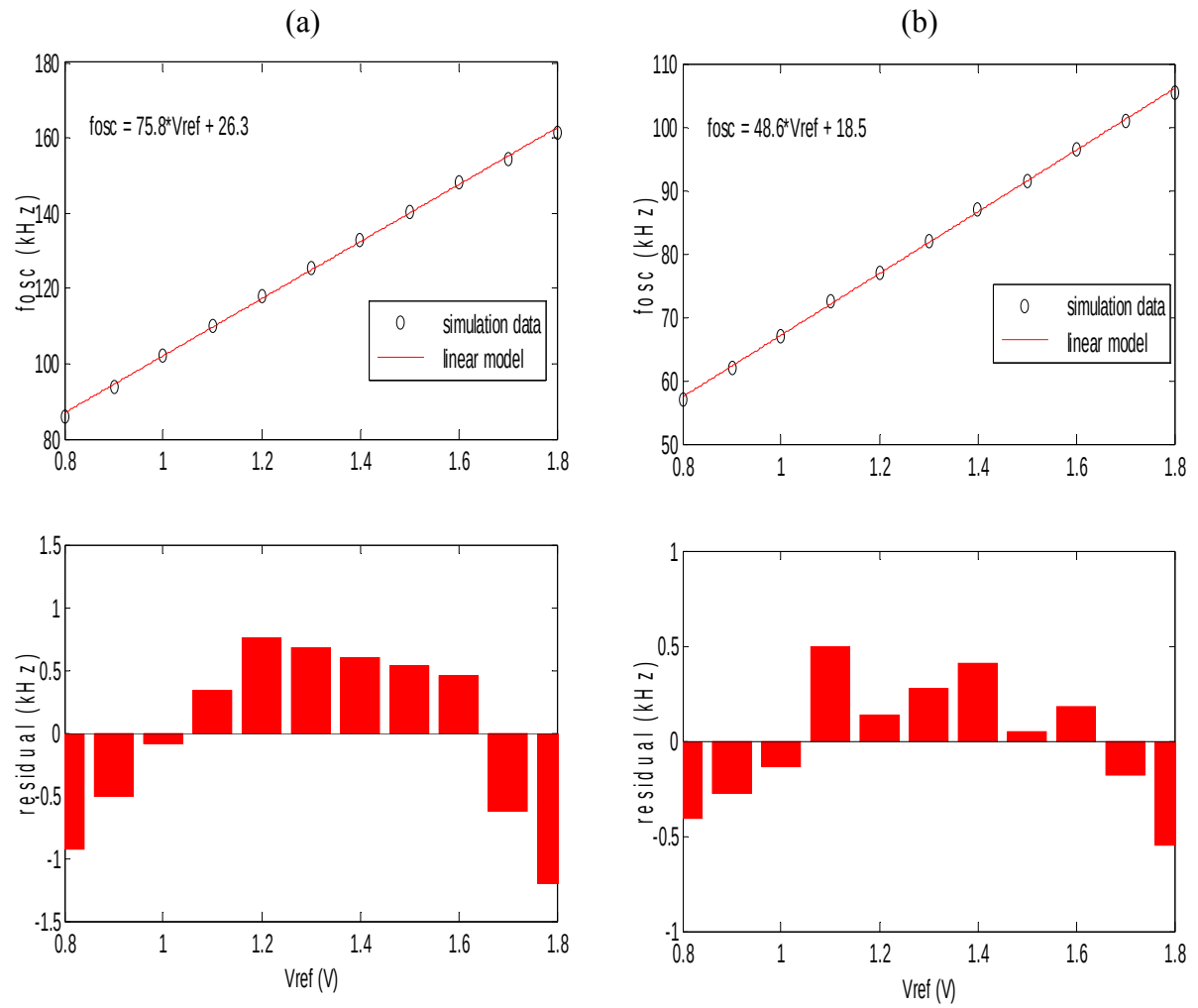


Figure 4-9: Simulation result showing the oscillation frequency (f_{osc}) versus reference electrode voltage (V_{ref}). (a) External resistor (R_{ext}) = 10 MΩ. (b) External resistor (R_{ext}) = 18 MΩ.

From Figure 4-9, the gain error of the log domain oscillator is staying within 1% for the one-volt input. Besides, the operating frequency ranges from several tens of kHz to 200 kHz, depending on the value of the external resistor. These results indicate that the log domain oscillator has a wide tuning range with a high linearity.

4.4 Derivation of log domain oscillator's transfer function

In this section, the log domain oscillator's transfer function will be derived heuristically. Nevertheless, the derivation addressed in this section is just an attempt to analyze the log domain circuit. Figure 4-10 begins the circuit analysis.

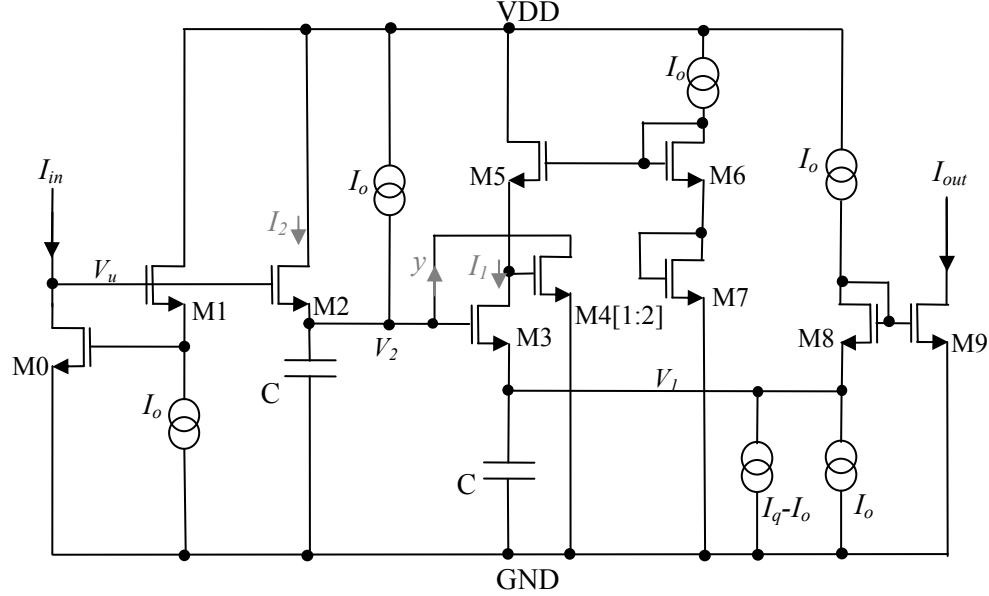


Figure 4-10: Log domain oscillator analysis.

Considering the Translinear loop comprising the matched transistors M0, M1, M2, M3, M8, and M9 in Figure 4-10, the product of the current densities in the clockwise direction of the loop is equal to the product of the current densities in the counter-clockwise direction of the loop [75].

$$(I_o)(I_o)(I_{in}) = (I_1)(I_2)(I_{out}) \quad (4.26)$$

To derive the input/output relationship of the oscillator, I_1 and I_2 from Figure 4-10 have to be expressed in terms of I_{out} and the time derivatives of I_{out} . First, I_1 can be expressed as:

$$I_1 = C\dot{V}_1 + I_q - I_o$$

$$\text{Where } I_{out} = I_o \exp\left(\frac{V_1}{nU_T}\right)$$

$$\Rightarrow \dot{I}_{out} = \frac{I_{out}}{nU_T} \dot{V}_1$$

$$\Rightarrow C\dot{V}_1 = \frac{\dot{I}_{out}}{I_{out}} nCU_T \quad (4.27)$$

$$\therefore \begin{cases} I_1 = nCU_T \frac{\dot{I}_{out}}{I_{out}} + I_q - I_o \\ \dot{I}_1 = nCU_T \left(\frac{\ddot{I}_{out}}{I_{out}} - \left(\frac{\dot{I}_{out}}{I_{out}} \right)^2 \right) \end{cases} \quad (4.28)$$

Next, the expression of I_2 can be deduced from Figure 4-10 as:

$$I_2 = C\dot{V}_2 - I_o + y \quad (4.29)$$

The variables $C\dot{V}_2$ and y in Equation 4.29 can be solved as follows. Considering the Translinear loop comprising M4, M5, M6, and M7, the product of the current densities in the clockwise is equal to the product of the current densities in the counter-clockwise direction:

$$\left(\frac{y}{2}\right)(I_1) = (I_o)(I_o)$$

$$y = \frac{2I_o^2}{I_1} \quad (4.30)$$

Thus, the expression of y in Equation 4.30 can be substituted back into Equation 4.29. In addition, the relationship between the gate source voltage and the drain current of transistor M2 is:

$$I_1 = I_s \exp\left(\frac{V_2 - V_1}{nU_T}\right)$$

$$\Rightarrow C\dot{V}_2 = C\dot{V}_1 + nCU_T \frac{\dot{I}_1}{I_1} \quad (4.31)$$

Substituting Equations 4.27, 4.30 and 4.31 into Equation 4.29, I_2 can be manipulated as:

$$I_2 = nCU_T \frac{\dot{I}_{out}}{I_{out}} + nCU_T \frac{\dot{I}_1}{I_1} + \frac{2I_o^2}{I_1} - I_o \quad (4.32)$$

Last, substituting Equations 4.28 and 4.32 back into Equation 4.26:

$$I_o^2 I_{in} = (nCU_T)^2 \ddot{I}_{out} + (I_q - 2I_o)(nCU_T) \dot{I}_{out} + 3I_o^2 - I_q I_o \quad (4.33)$$

In s -domain representation:

$$\frac{I_{out}(s)}{I_{in}(s)} = \frac{\left(\frac{I_o}{nCU_T}\right)^2}{s^2 + s \frac{I_q - 2I_o}{nCU_T} + \frac{3I_o^2 - I_q I_o}{(nCU_T)^2}} \quad (4.34)$$

Equation 4.34 is a second-order system in which the Q value and the natural frequency ω_n can be expressed as [13]:

$$\begin{cases} \omega_n = \frac{\sqrt{3I_o^2 - I_q I_o}}{nCU_T} \\ \frac{\omega_n}{Q} = \frac{I_q - 2I_o}{nCU_T} \end{cases} \quad (4.35)$$

When $I_q = 2I_o$, Equation 4.34 is reduced to Equation 4.1, which represents the transfer function of a simple harmonic oscillator. When that happens, the oscillation frequency will be reduced to $f_{osc} = \frac{1}{2\pi} \frac{I_o}{nC U_T}$. The oscillation frequency will be directly proportional to the bias current I_o . Moreover, since the Q value is maximized under the condition $I_q = 2I_o$, the phase change of the oscillator in the open loop will be maximized at the oscillation frequency under this relationship [16]:

$$Q = \frac{\omega_0}{2} \frac{d\phi}{d\omega} \quad (4.36)$$

where $\frac{d\phi}{d\omega}$ is the phase change. Accordingly, the phase noise can be minimized when the Q value is maximized [16], [17].

To conclude, transistor simulations were done using 0.18 μm CMOS process parameters to investigate the opened loop phase change and the closed loop phase noise of the log domain oscillator. The emphasis of the simulations is on the phase noise and the phase change by the DC current I_q . The simulation results are plotted in Figures 4-11 and 4-12.

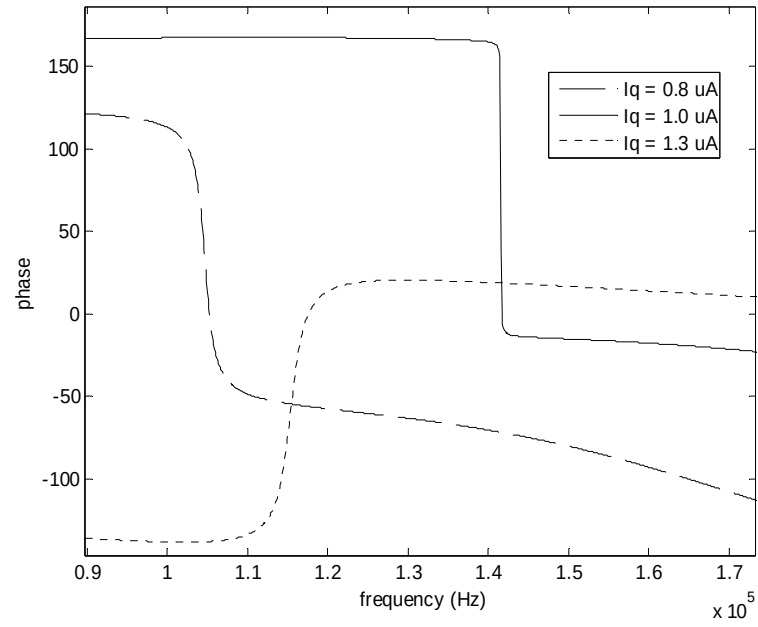


Figure 4-11: Simulated opened loop phase change under different bias current I_q .

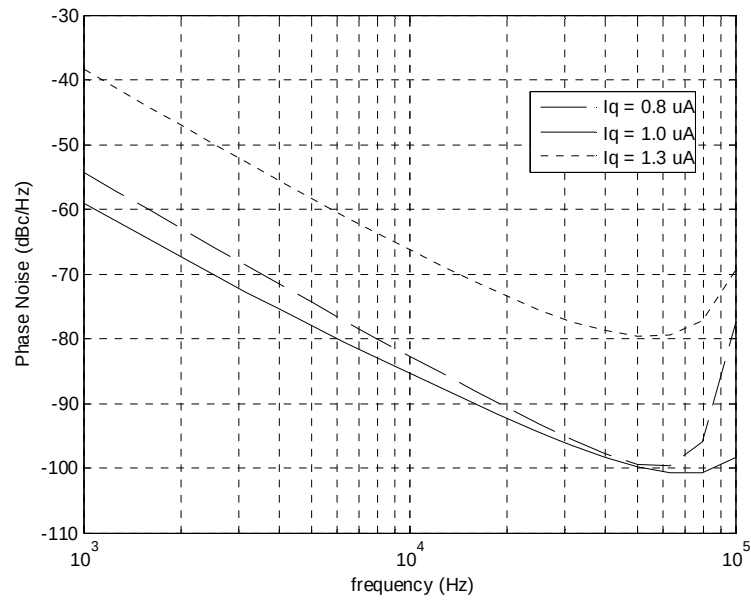


Figure 4-12: Simulated closed loop phase noise under different bias current I_q .

Figure 4-11 shows the open loop phase change of the log domain oscillator. The test bench was configured by setting the bias current I_q to $0.8 \mu A$, $1 \mu A$, and $1.3 \mu A$ whereas the bias current I_o was set to $0.5 \mu A$. When I_q is 2 times of I_o , the phase change had the steepest slope at the oscillation frequency around 140 kHz , where the phase was at zero degree. The ratio of I_q to 2 times of I_o maximizes the Q value of the system, while all the other ratios show the non-optimal Q value. Therefore, the phase noise should be at minimum when I_q was $1 \mu A$ and I_o was $0.5 \mu A$. Figure 4-12 plots the closed loop phase noise simulation of the log domain oscillator, and it confirms that the phase noise is the lowest when I_q and I_o were set to $1 \mu A$ and $0.5 \mu A$ respectively. Having a low phase noise VCO is very important to build the reference-less sigma delta modulator because any noise generated by the VCO can stay remain in the output of the modulator. This pulls down the SNR of the system.

4.5 Summary

This chapter have discussed the application of the log domain signal processing to implement the voltage controlled oscillator in standard CMOS technologies. In simulations, the oscillator has shown very linearly to the controlled voltage, which is proportional to the reference electrode voltage and the pH. In addition, the phase noise of this oscillator can be minimized by using a ratio of the matched bias currents. Moreover, this oscillator is micro-watt power operated. These attributes suggest that the log domain VCO satisfy the design requirements to build the integrated ISFETs instrumentation system.

4.6 References

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Chapter 5

ISFET64_CHIP Architecture

Having discussed the various circuit building blocks in the previous chapters, this chapter is dedicated to the discussion of the fabricated circuit for the ISFETs instrumentation: ISFET64_CHIP. Before looking into the chip's architecture, the on-chip bias generator for the ISFETs averaging array will be discussed first. There are many ways to implement on-chip bias. In this thesis, a bandgap voltage is implemented on chip to generate the bias currents for the ISFETs averaging array. The use of the bandgap voltage to derive the bias currents can improve the ability of the chip to resist power supply and temperature variation. This ensures that the chip's power consumption can be well regulated. The digital logic will then be discussed later in this chapter to complete the description of the integrated ISFETs instrumentation system. Finally, schematic simulation results will be provided to verify the functionality of the overall system.

5.1 Bias Generator

The core component of the bias network in ISFET64_CHIP is the classical bandgap voltage reference with vertical pn junctions in standard CMOS process [1]. The bandgap voltage schematic is illustrated in the left hand side of Figure 5-1. The bandgap voltage is

composed of 2 components: A Proportional-to-Absolute-Temperature (PTAT) and A Complementary-to-Absolute-Temperature (CTAT).

The PATA current is generated by considering the voltage drop across the loop ($V_{BE,Q1} - V_{GS,MN3} - V_{GS,MN4} - I_{PTAT}R_1 - V_{BE,Q2}$):

$$V_{BE,Q1} + V_{GS,MN3} = V_{GS,MN4} + I_{PTAT}R_1 + V_{BE,Q2}$$

$$I_{PTAT} = \frac{U_T}{R_1} \ln(n) \quad (5.1)$$

On the other hand, the base emitter voltage of the vertical pnp is inversely proportional to the absolute temperature, so adding the base emitter voltage of the pnp with a PTAT component can eliminate the temperature dependency.

$$V_{BG} = I_{PTAT}R_2 + V_{BE,Q3}$$

$$\therefore V_{BG} = \frac{R_2}{R_1} U_T \ln(n) + V_{BE,Q3} \quad (5.2)$$

Equation 5.2 consists of two components. The term $\frac{R_2}{R_1} U_T \ln(n)$ is proportional to the absolute temperature (PTAT), while the term $V_{BE,Q3}$ is complementary to the absolute temperature (CTAT). The bandgap voltage is said to be 1st order temperature compensated. In addition, Equation 5.2 is free from the influence of the power supply. Therefore, this bandgap voltage is in-sensitive to variation of the supply voltage and the temperature.

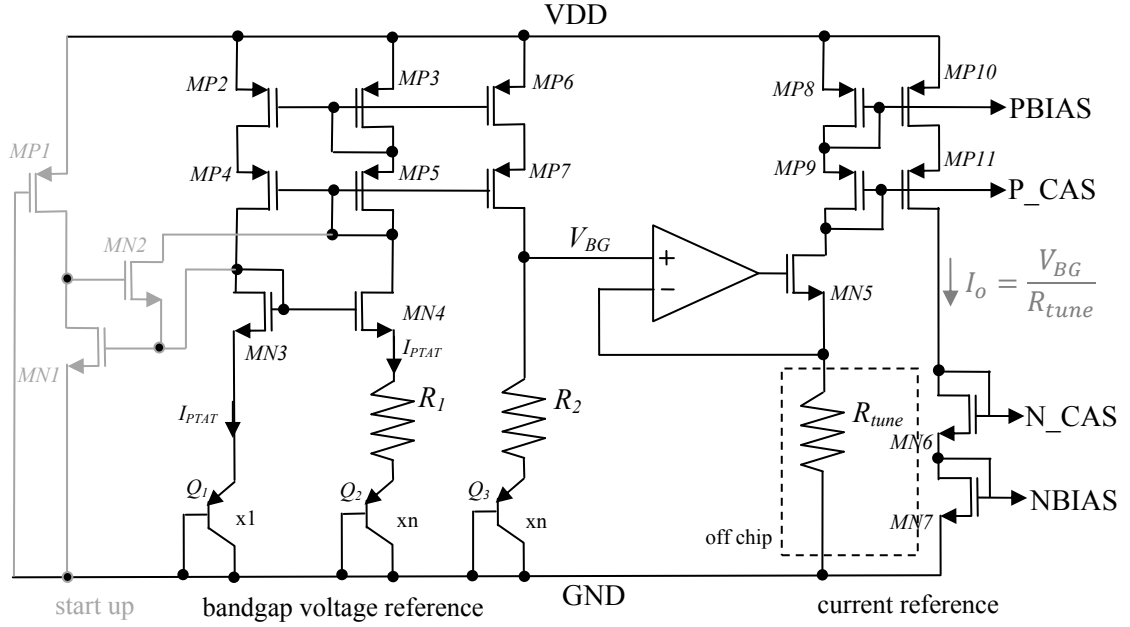


Figure 5-1: ISFET64_CHIP's sub-block, BIAS GEN, is used to generate the bias voltages and the bias current.

A voltage amplifier configured in a closed loop gain of one is used to create a supply voltage and temperature independent bias current from the bandgap voltage. The external resistor R_{tune} is loaded to the inverting terminal of the opamp. The reference current I_o , which is equal to $\frac{V_{BG}}{R_{tune}}$, is generated. This reference current is replicated to a number of current sinks and current sources using cascode current mirrors. The current sources and the current sinks are then used to bias the ISFETs averaging array.

Transistor simulations were done using UMC 0.18 μm 1P6M CMOS process parameters to examine the robustness of the bandgap voltage and the reference current in the presence of

supply voltage and temperature's variation. The test benches were simulated under three different corners: typical, slow, and fast. Simulation settings are summarized in Table 5-I.

Table 5-1: Corner simulation setup

	Typical	Slow	Fast
Circuit elements' model	Typ	Slow	Fast
Temperature	27 ⁰ C	125 ⁰ C	0 ⁰ C
Supply voltage	3.3 Volts	3.0 Volts	3.6 Volts

With the above simulation setup, temperature sweep analyses were performed under Cadence Spectre[®] simulator. The simulation results were exported to The MathWorks[™] MATLAB for plotting. Figure 5-2 shows the bandgap voltage over a temperature sweep from 0 ⁰C to 125 ⁰C under the three different corners. The nominal voltage in the typical condition is 1.252 volts, and the temperature sensitivity of the bandgap voltage is found to be about 64 *ppm* at this typical condition. On the other hand, Figure 5-3 plots the reference current under the same simulation environment. The nominal current in the typical condition is 125.2 *nA*, and the temperature sensitivity of the reference current is found to be less than 65 *ppm* at this typical condition. To conclude, the reference voltage and the reference current are stable enough for biasing the ISFETs averaging array.

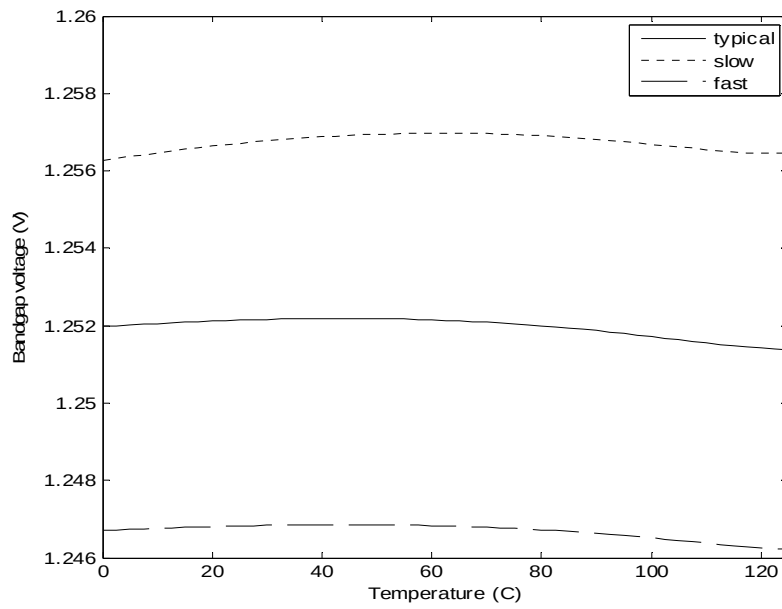


Figure 5-2: Bandgap voltage reference versus Temperature.

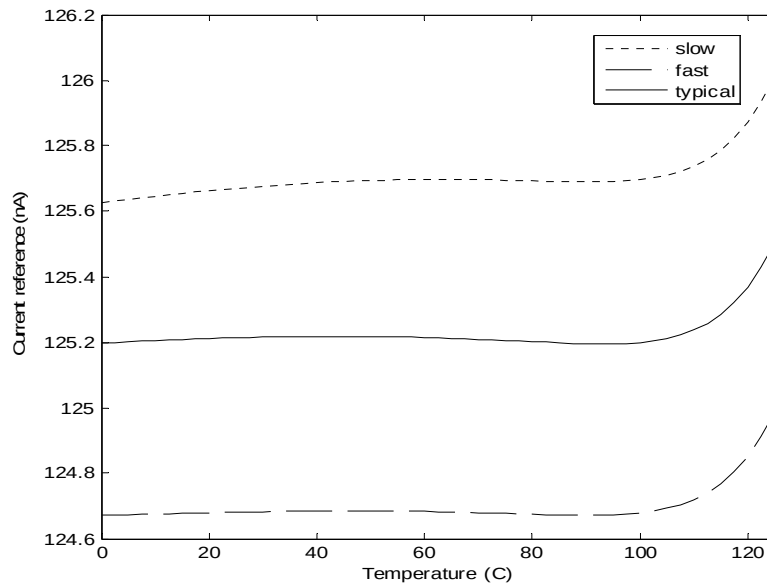


Figure 5-3: Reference current versus Temperature.

5.2 Digital Logic for Frequency to Digital Sigma Delta Modulator

In Chapter 2, it was shown that a frequency modulated (FM) signal can be digitized in a 1st order sigma delta manner by using a pair of D flip-flops and an XOR gate. The first D flip-flop serves as the phase quantizer. The second D flip-flop in cascade with the XOR gate serves as the edge extractor, which is identical to the differentiation in time domain. The overall schematic for the digital logic is illustrated in Figure 5-4.

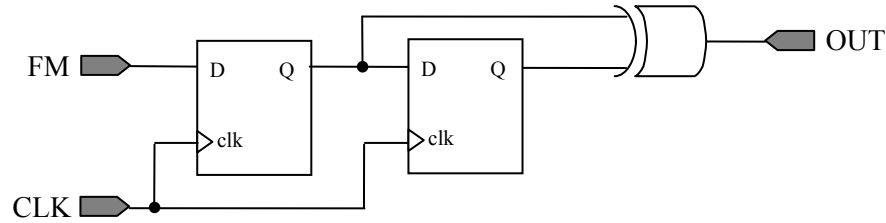


Figure 5-4: Digital sigma delta modulator using frequency modulated (FM) signal.

There are two approaches to design the digital sigma delta modulator as shown in Figure 5-4 in ISFET64_CHIP. One way is by doing a full custom design, in which both the design of schematics and layouts are done at the transistor level. The other way is by doing a semi-custom approach, in which both the schematics and the layouts are done at the gate level. Faraday Technology Corporation [2] provides a comprehensive set of standard cells, IO cells, and some other Intellectual Property (IP) blocks for designing digital chips in UMC 0.18 μm CMOS process. In this thesis, the digital logic within ISFET64_CHIP was designed by using the design kit from Faraday Technology Corporation.

Verilog simulations were carried out to verify the functionality of the FM to digital sigma delta modulator. The simulation results were exported to The MathWorksTM MATLAB for plotting, and they are displayed in Figure 5-5. The input signal FM is a square wave having a frequency of 10 kHz. The clock signal CLK is 50 kHz in case (a), and 1 MHz in case (b).

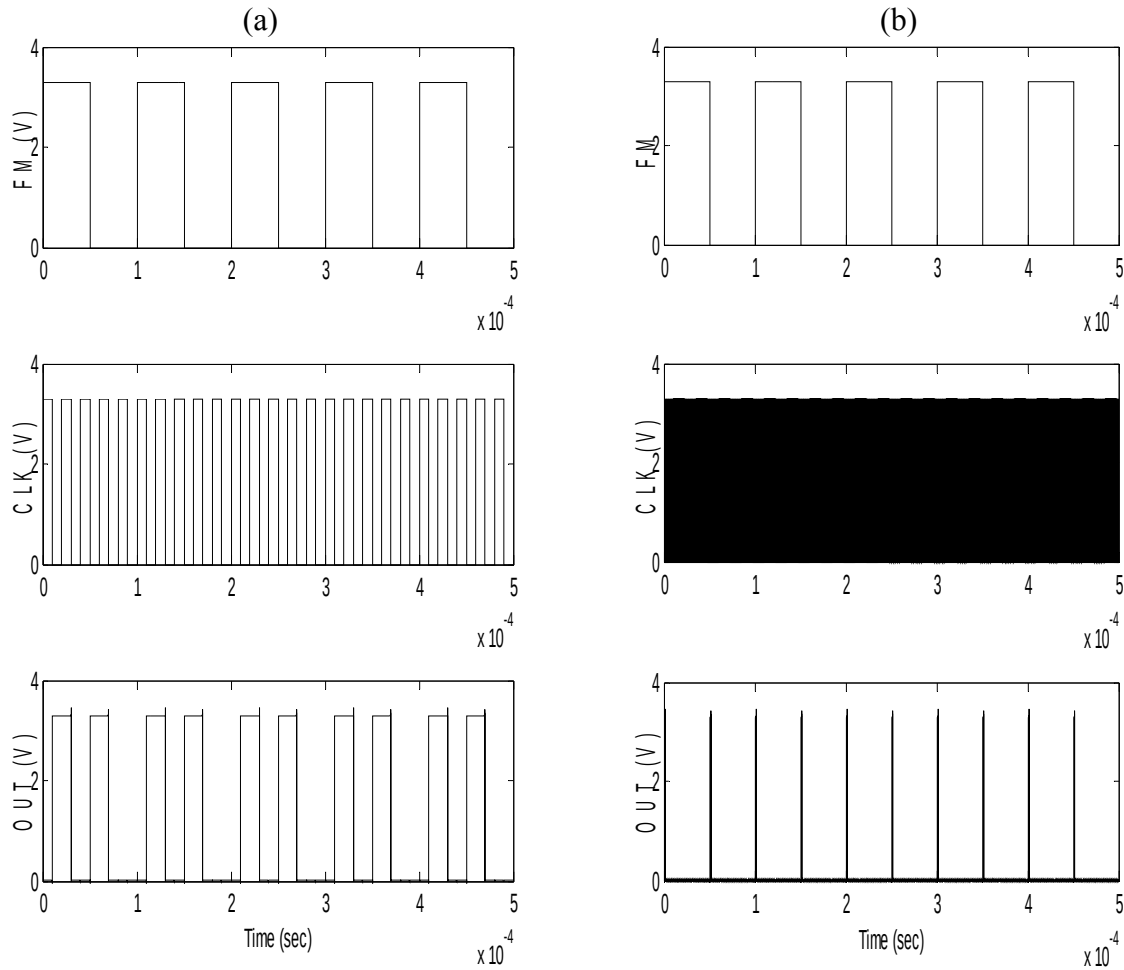


Figure 5-5: Simulation results showing frequency modulation (FM) to digital sigma delta modulator. The FM signal is a 10 kHz square wave. Case (a) has a 50 kHz clock signal, while case (b) has a 1 MHz signal.

Figure 5-5b shows clearly that the function of the digital logic is to extract the rising and the falling edges of the input signal. In other words, the modulator is differentiating the input signal FM in such a way that the spikes in the output signal OUT correspond to the rising and the falling edges of FM. Even in the result as shown in Figure 5-5a, the digital logic is still able to extract the edges of FM even when the ratio of CLK's frequency to FM's frequency is 5:1. In fact, as long as the CLK's frequency is bigger than twice the maximum FM frequency, the D flip-flops in conjunction with the XOR gate can quantize and differentiate the phase of FM without signal aliasing.

5.3 ISFET64_CHIP System Architecture

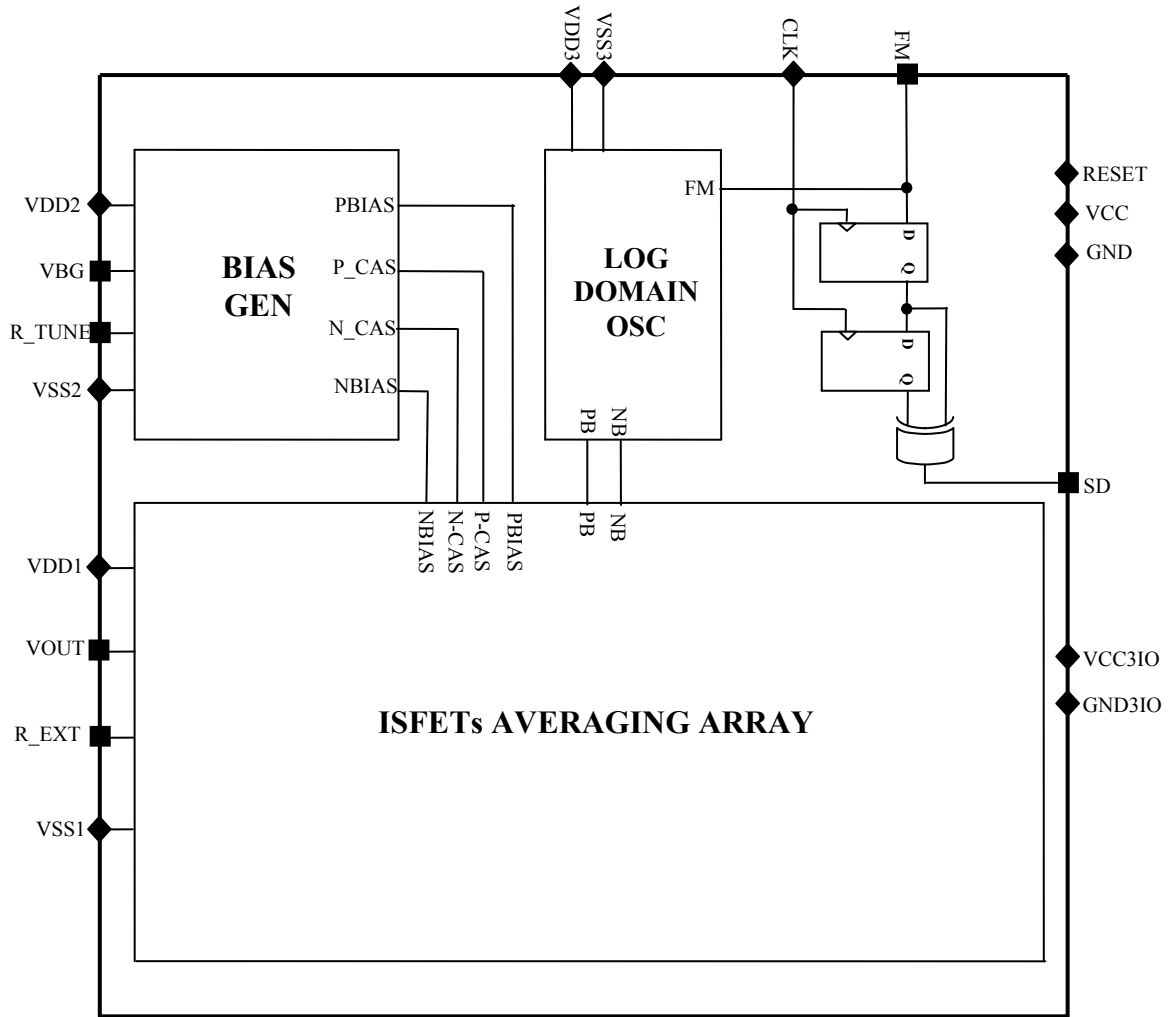


Figure 5-6: Functional diagram of ISFET64_CHIP.

The architecture of ISFET64_CHIP is shown in Figure 5-6. There are five sets of independent power supplies; each of those is responsible for a specific functional block so that power consumption can be measured individually. Moreover, having a dedicated power

supply for each functional block will minimize any noise coupling [2]. For examples, the power supply noise from LOG DOMAIN OSC or the power supply noise from the digital logic can be coupled to the high sensitive analogue functional blocks in ISFET64_CHIP, such as BIAS GEN or ISFETs AVERAGING ARRAY. Except for the digital core supply VCC, which is at 1.8 volts, all the other positive power supplies are at 3.3 volts, whereas all the most negative power supplies are at 0 volt.

As discussed previously, the value of the external resistor R_{TUNE} regulates the bias current for the ISFETs averaging array. The nominal value is $10\text{ M}\Omega$, and the bias current will be set up approximately to 120 nA . A further increase or decrease in R_{TUNE} is not recommended as the ISFETs averaging array is frequency compensated by the on-chip resistors and the capacitor based on 100 nA bias current formulation. Besides, the nominal value of the external resistor R_{EXT} , which sets the sensitivity of the log domain oscillator, is also $10\text{ M}\Omega$. This value fits the operating frequency range of the log domain oscillator.

There is the RESET pin, which can reset all the flip-flops to zero by users. There is also the CLK pin, which clocks the on-chip flip-flops. The operating frequency driving the CLK pin is 500 kHz, and it can be increased by up to tens of megahertz. However, higher clock frequency leads to higher dynamic power consumption as the rate of the switching events increases within the digital logic. The lower bound of the clock frequency has to be greater than twice the maximum frequency of the VCO's frequency to prevent signal aliasing.

ISFET64_CHIP was confined to a layout of $1565\mu\text{m} \times 1565\mu\text{m}$ in UMC 0.18um MM/RF CMOS process. This dimension complies with the Europractice's mini@sic, a Multi Wafer

Project (MWP) run for universities and research labs in fabricating application-specific integrated circuit (ASIC) prototypes. The layout plot is displayed in Figure 5-7.

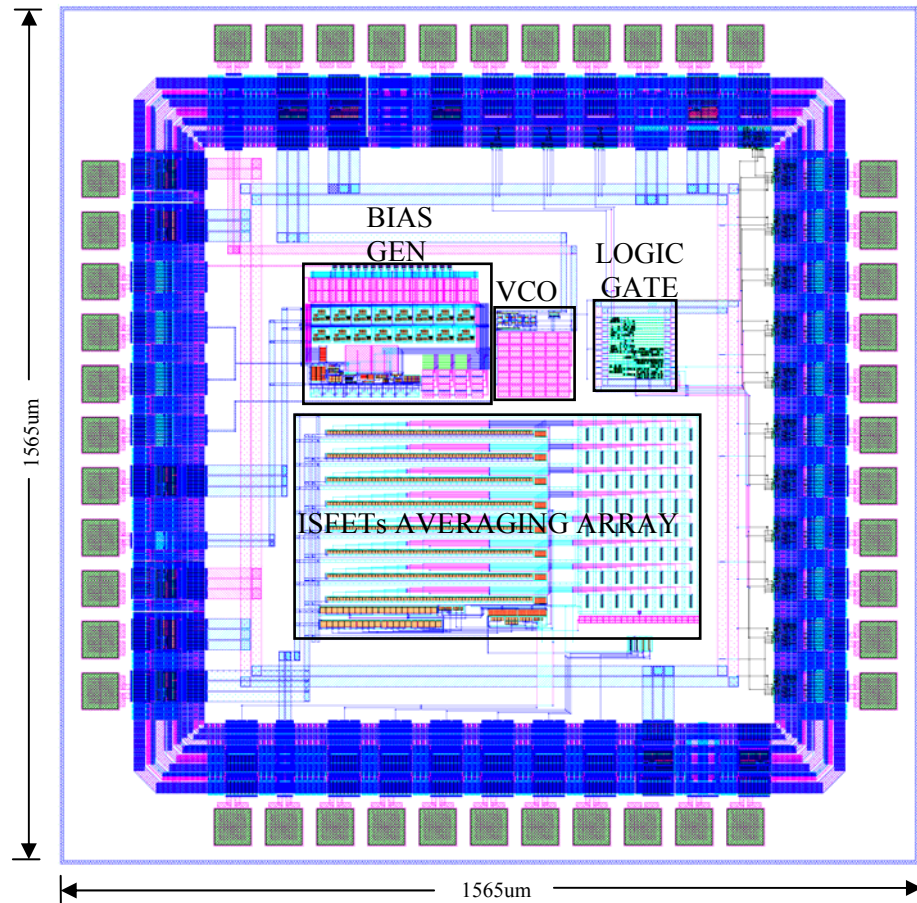


Figure 5-7: Layout of ISFET64_CHIP.

Finally, the performance of ISFET64_CHIP was evaluated with a full chip mixed-signal simulation. The analogue input to ISFET64_CHIP was a sinusoidal voltage with a frequency of 100 Hz and a voltage amplitude of 0.1 volt. To enable the Spectre® to accept the electrochemical domain associated with the ISFET's model, VerilogA was used to model the

ISFET's electrochemical behaviour, similar to Martinoia's macro-model [3]. A 500 kHz clock was used to drive the clock pin of the ISFET64_CHIP. The internal bias network was managed by the BIAS_GEN block, which had the resistor R_TUNE with 10 $M\Omega$ to set the operating point. Three outputs: V_{OUT} , FM, and SD were probed and saved. V_{OUT} got a copy of the analogue input sinusoid as the ISFETs averaging array was configured with a closed loop gain of one. FM was a square waveform whose frequency was modulated by the baseband signal. The frequency spectrum was wideband since the input to the VCO was a sinusoid. SD was the digital output bit-stream whose frequency spectrum contained the input sinusoid (i.e., the signal with a frequency of 100 Hz) and the 1st order noise shaped spectrum.

Simulations were done using Cadence® IC Design package in Sun® Microsystem Blade 2500's environment. The circuit has 582 MOSFETs and other passive elements. The circuit size has 396 nodes in total. Since the baseband signal is a sinusoid with a frequency of 100 Hz, a 100 ms transient simulation can produce 10 waveforms, which gives a frequency resolution of 10 Hz to reconstruct the baseband signal. Total simulation time took more than 1 week to finish, and the results were post-processed in The MathWorks™ MATLAB to produce the following Figures.

Figure 5-8 and Figure 5-9 plot of the signal V_{OUT} in time domain and frequency domain respectively. In Figure 5-8, the signal's waveform swings from 1.85 volts to 2.05 volts, indicating that the amplitude of the output signal remains at 0.1 volt. Despite the offset existed in between the input and output, Figure 5-8 verifies the ISFETs averaging array is operating as a source follower system. Besides, Figure 5-9 reveals that the simulated SNR of

the ISFETs averaging array can achieve more than 100 dB, which equivalently represents 16 bits of information. By comparing the noise floor of Figure 5-9 with Figure 3-11, they experience the same level of the noise floor. This shows that the noise floor was pushed down by the action of the averaging. Therefore, the ISFETs averaging array can improve the SNR of the system by using a large number of samples.

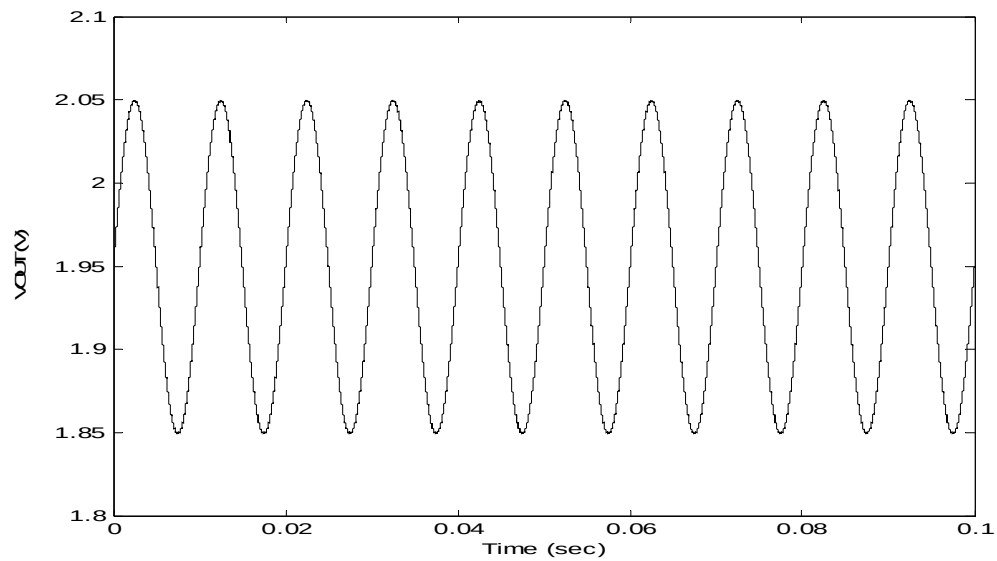


Figure 5-8: Time domain simulation showing V_{OUT} for 100ms.

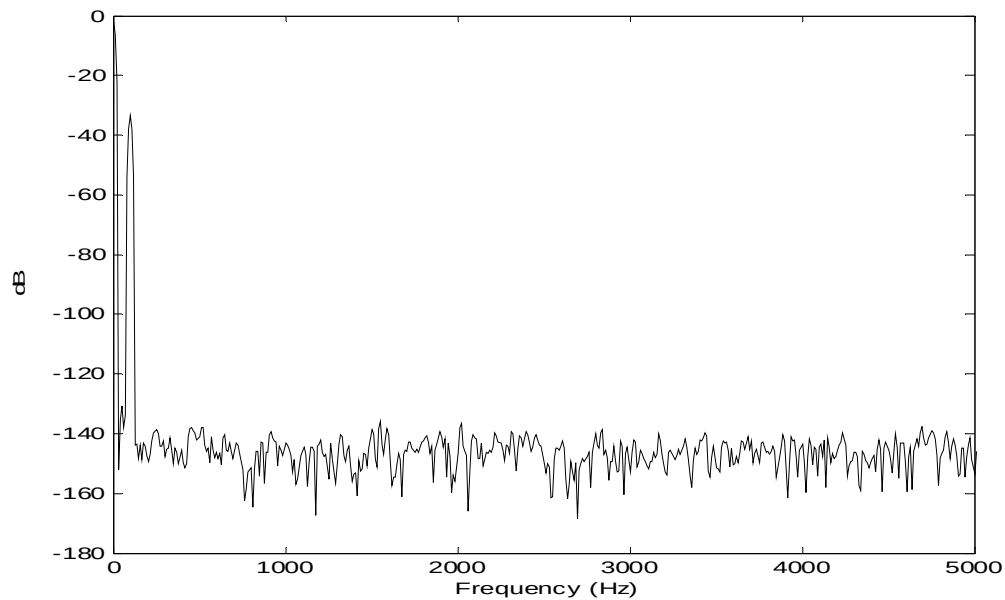


Figure 5-9: Simulated frequency spectrum showing V_{OUT} .

Figure 5-10 plots of the power spectrum of the signal FM from the log domain oscillator's output. Since the log domain oscillator was frequency modulated by the input sinusoid with a voltage amplitude of 0.1 volt and a frequency of 100Hz, the oscillator produced a band of frequencies. From Figure 5-10, the maximum frequency deviation from the carrier is 7.59 kHz, so the bandwidth of the signal FM is about 15.2 kHz.

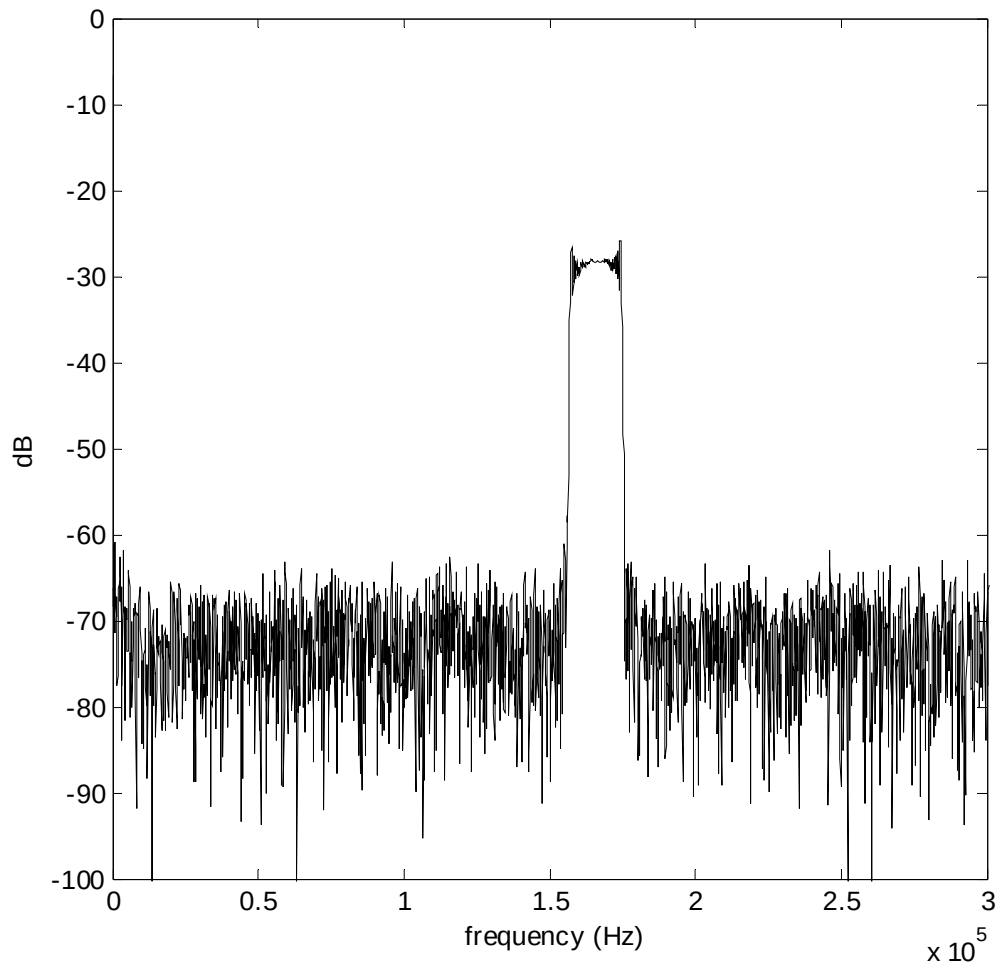


Figure 5-10: Simulated frequency spectrum showing the frequency modulated (FM) signal.

Figure 5-11 plots of the power spectrum of the digital output SD. This is a one-bit signal with a sampling frequency of 500 kHz. The baseband signal with the frequency of 100 Hz can be easily located from the spectrum. Moreover, the noise floor is shaped by +20 *dB/decade*, which indicates a 1st order sigma delta modulation. Nonetheless, there are harmonics occurred in the spectrum. The existence of these harmonics mainly comes from

the non-linearity of the log domain oscillator. Nonetheless, the harmonics are almost 60 dB lower than the fundamental. Since the reference electrode noise associated with an ISFET can be larger than $1\mu W$ [4], the presence of the harmonics might not be strong enough to interfere with a pH measurement when the electrode noise is considered.

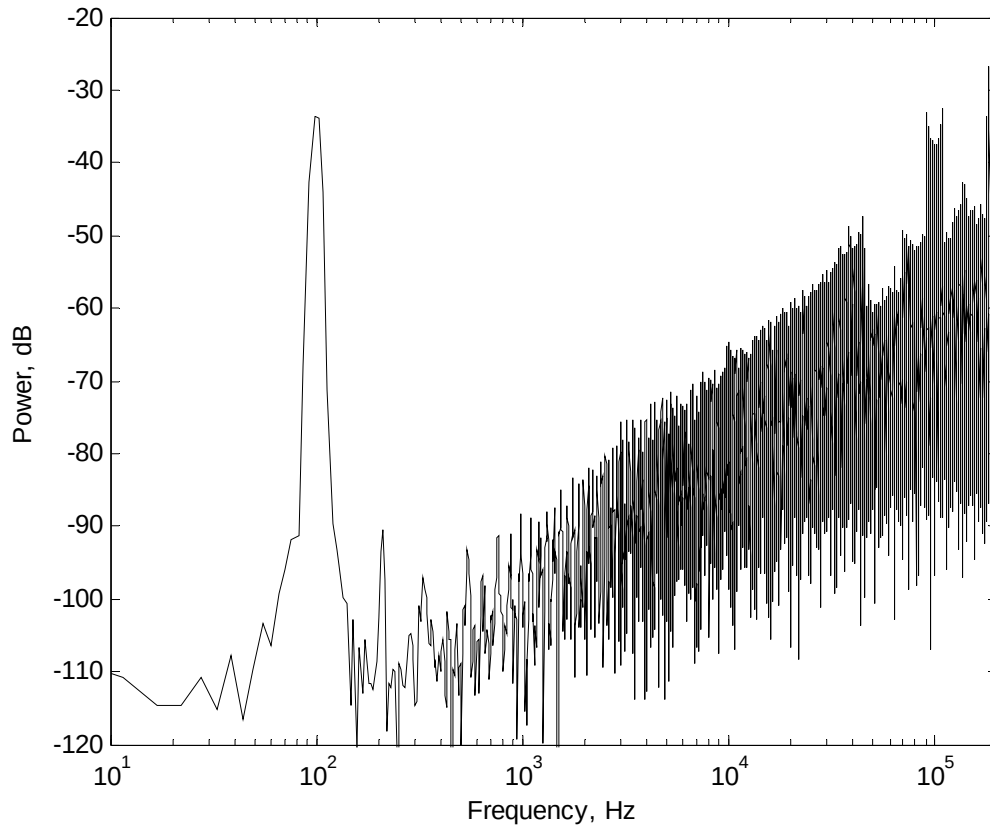


Figure 5-11: Simulated frequency spectrum showing the signal SD.

5.4 Summary

This chapter has discussed the internal details of ISFET64_CHIP, the chip implementation of the integrated ISFETs instrumentation system. On-chip power supply and temperature insensitive bandgap voltage and reference current have been implemented in order to provide biasing to the ISFETs averaging array. In addition, behavioural simulation results have been used to verify the functionality of the digital logic. Finally, a full chip mixed signal simulation results have been presented to verify the performance of the ISFETs instrumentation system. The simulation results on the ISFETs averaging array have justified the advantages of using the ISFETs averaging array. On the other hand, the simulated digital output achieved a 1st order sigma delta characteristic, but it contained harmonics which cannot be eliminated. In the presence of reference electrode noise, the harmonics might not be strong enough to interfere with pH measurements.

5.5 References

- [1] P.R. Gray, P.J. Hurst, S.H. Lewis, and R.G. Meyer, *Analysis and Design of Analog Integrated Circuits*. Wiley, 2001.
- [2] Faraday Design kit for UMC 0.18 um MM/RF CMOS restricted documents. 2009.
- [3] S. Martinoia, and G. Massobrio, "A behavioral macromodel of the ISFET in SPICE," *Sensors and Actuators B*, vol. 62, pp. 182-189, 2000.
- [4] C. Jakobson, and Y. Nemirovsky, "1/f Noise Ion Sensitive Field Effect Transistors from Subthreshold to Saturation," *Electron Devices, IEEE Transactions on*, vol.46, pp. 259-260, 1999.

Chapter 6

ISFET64_CHIP Measurement

Having discussed the architecture of ISFET64_CHIP in Chapter 5, this chapter presents the measurement results. ISFET64_CHIP was designed to have 44 bond pads in total, 11 pads on each side. The chips were packaged in 44-pin J-Leaded Ceramic Chip Carrier (JLCC44), and they were also glued on the printed circuit board (PCB) directly. Epoxy was applied to encapsulate the chip periphery and the bond-wires, exposed only a tiny region on the passivation layer which is used for chemical sensing. Encapsulation is very important in this step to ensure that the chip can be tested in a chemical solution without exposing its bond-wires to the solution. The final step to construct the prototype was to mount a cylinder on top of the encapsulated chip so that a chemical solution tank can be made to run experiments. Various measurement results from the ISFETs averaging amplifier, the log domain oscillator, and the complete instrumentation system will be presented in this chapter.

6.1 Test Board Preparation

In order to connect a PCB with ISFET64_CHIP, a footprint for the chip was made for the PCB. A footprint not only defines the boundary of the chip, but it also defines the layout for the electrical connections between the board and the chip. Figure 6-1 illustrates the footprint for ISFET64_CHIP. The footprint contains 44 rectangular pad-stacks that are 45 mil by 12

mil (1.14 mm by 0.3 mm) in size. Each pad-stack is separated by 10 mil (0.25 mm). The distance between the pad-stack and the chip is about 92 mil (2.34 mm). These geometrical spacing requirements ensure that the bond-wires between the chip and the PCB can be bonded with enough space clearance.

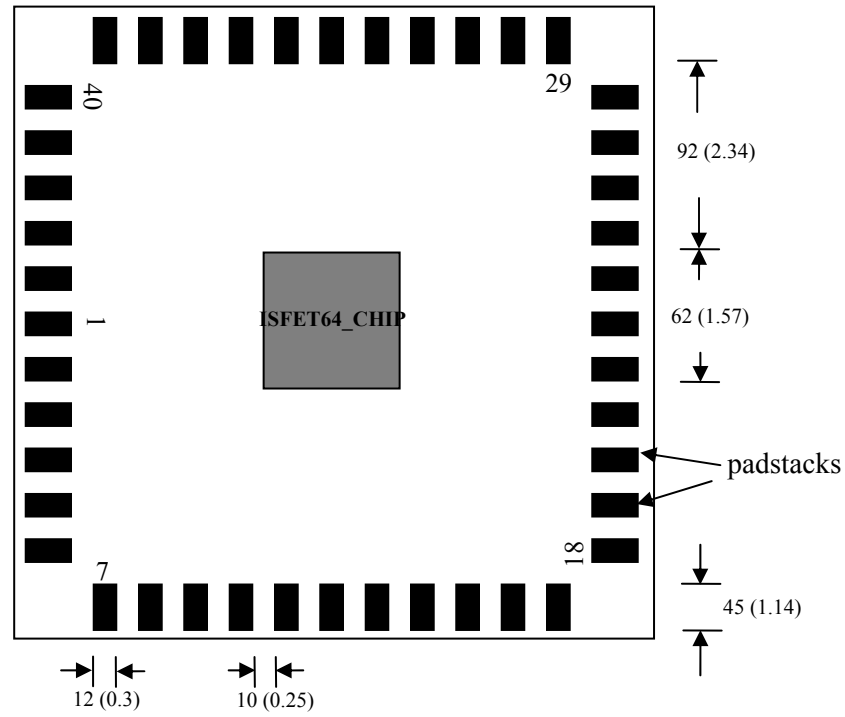


Figure 6-1: ISFET64_CHIP footprint. All sizes are in mil (mm).

Some of the pins on ISFET64_CHIP were not used. Figure 6-2 shows the actual wirebondings of ISFET64_CHIP under a microscope. The unused bondpads on the right hand side of the chip are for other testing purposes, and these are not relevant in this thesis. Table 8-I in Appendix describes the actual pin usage in ISFET64_CHIP.

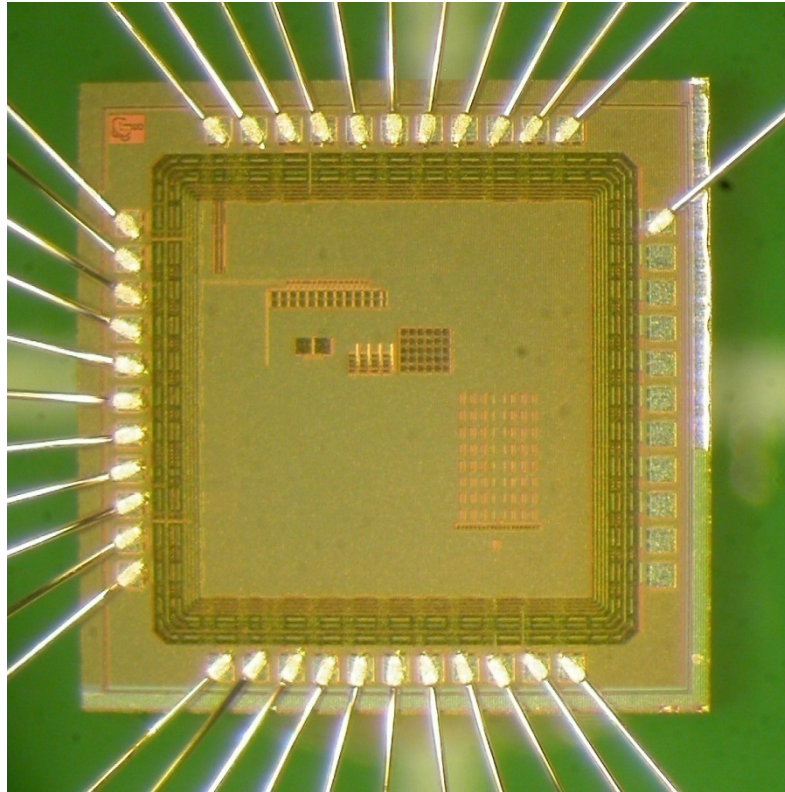


Figure 6-2: ISFET64_CHIP microphotograph.

A 2-layer PCB of 4.5 inches by 4 inches was designed in Cadence[®] OrCAD Layout Editor, and its layout plot is shown in Figure 6-3. The bottom side of the PCB is a ground plane which is shown in red. The aim of using a large plane is to provide a low impedance path in order to minimize any voltage drop (IR) on the ground plane. Besides, there are four distinct power supplies on the chip with four dedicated power planes. These power planes are shown in blue in Figure 6-3. Finally, the ISFET64_CHIP footprint was located on the bottom half of the PCB. This region has the extra spacing to ease the mounting of the plastic beaker

to enclose the chip. The epoxy-encapsulated chip is shown in Figure 6-4. The yellow lines indicate various signals and powers, while the black paste is the epoxy. The centre region of the epoxy is clear in order to expose the passivation layer for chemical sensing. The size of the active window is approximately 14 mil by 8 mil.

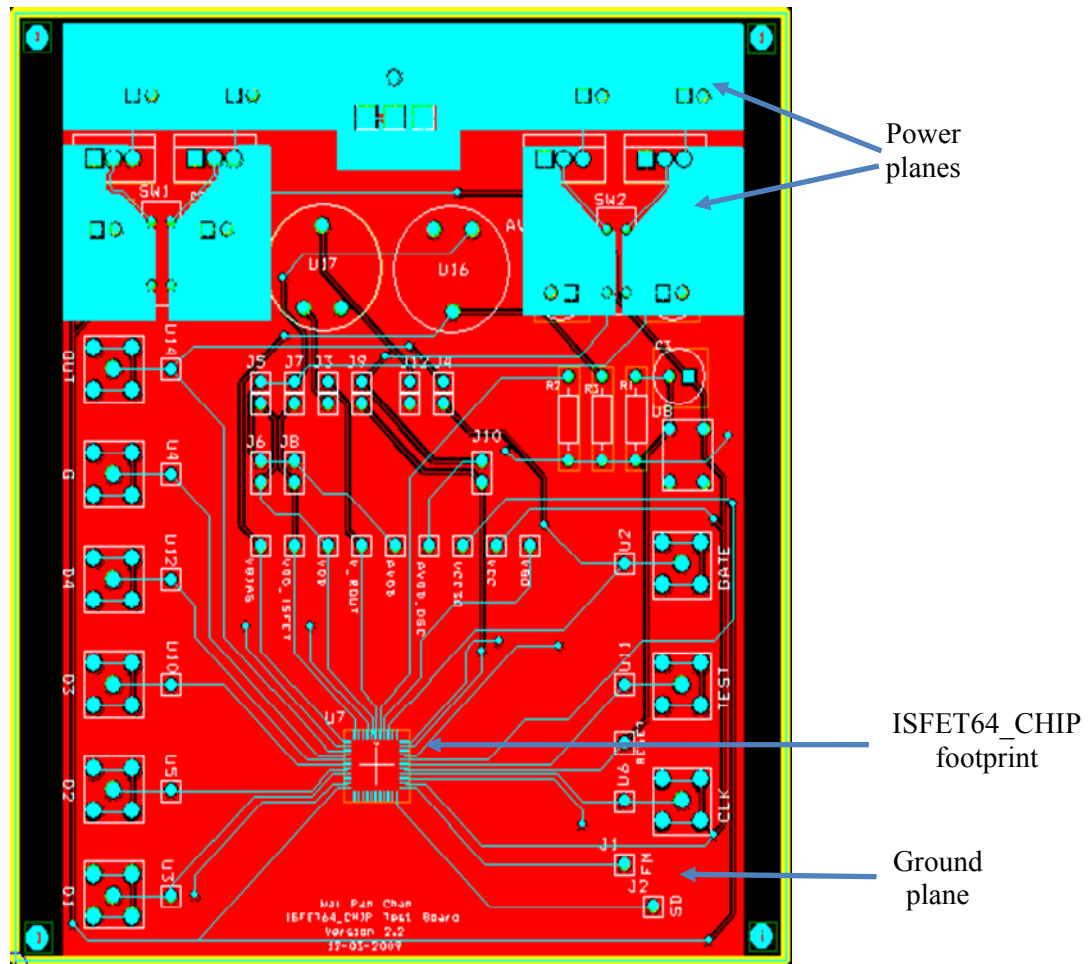


Figure 6-3: Layout plot showing ISFET64_CHIP test board where the red indicates the bottom ground plane and blue indicates the top power and signal lines.

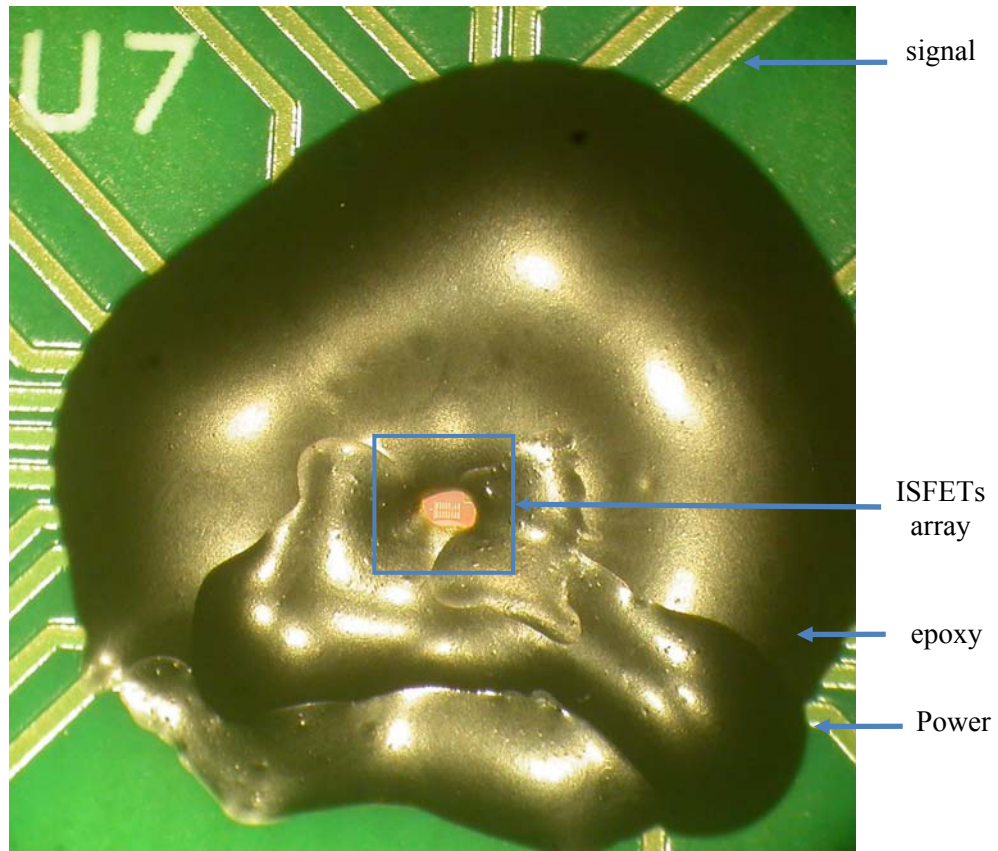


Figure 6-4: Encapsulated ISFET64_CHIP on printed circuit board (PCB).

In order to hold a chemical solution, a plastic cylinder is glued on the board to enclose the chip as shown in Figure 6-5. The board also illustrates the other PCB-components such as the SMA inputs/outputs, the pots, the switches, and the jumpers. The measurement results will be reported in the next section.

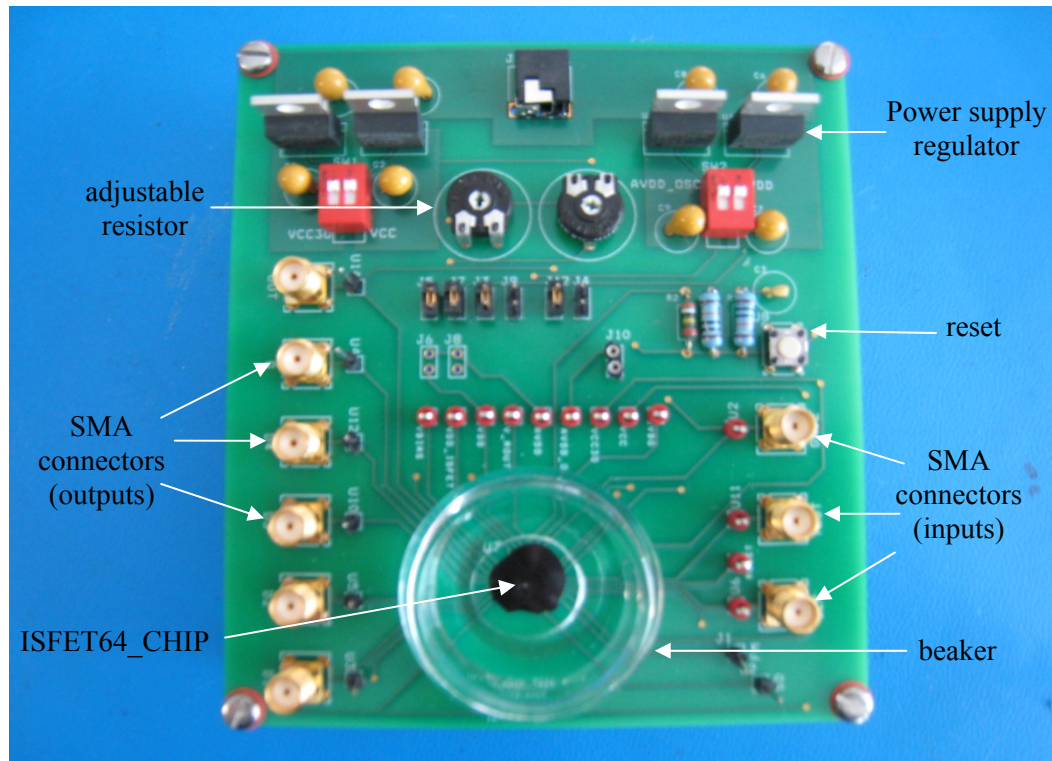


Figure 6-5: Complete test board for ISFET64_CHIP.

6.2 ISFETs Averaging Array Measurements

The performance of the ISFETs averaging array implemented in ISFET64_CHIP was evaluated in this section. There are few dimensions of the ISFETs averaging array which can be evaluated. They are the linearity, the sensitivity to pH, and the dynamics of the ISFETs averaging array in response to change in pH in real time.

6.2.1 Linearity

This subsection is to look at the linear operating range of the ISFETs averaging array. Ideally, the operating range of the averaging array should be bound by the positive and the

negative supply voltage, which are from 3.3 volts to 0 volt. However, this ideal range does not exist in reality because a finite amount of the drain-source voltage will be dissipated in the output transistors [1], [2], [3]. Nonetheless, it is not necessary for the ISFETs averaging array to have a 3.3-volt operating range. Since there are only 14 units of pH in scale, the maximum voltage consumption is about 0.826 volt in a Nernstian response. Therefore, having a 1-volt linear output range of the ISFETs averaging array is sufficient to represent the entire pH scale. However, an extended linear operating range allows more headroom to counteract any offset introduced by the mismatched CMOS ISFETs, so it is good to have a large dynamic range provided the averaging array. The experimental set up for this subsection is shown in Figure 6-6:

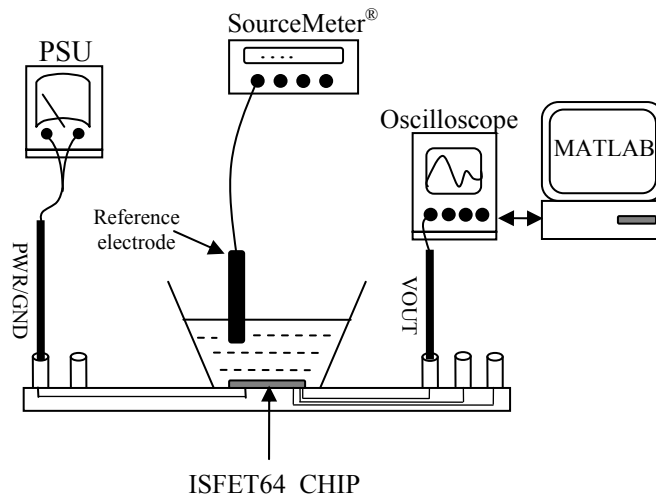


Figure 6-6: Experimental setup for the ISFETs averaging array

The test board was power supplied by Thurlby Thandar Instruments Ltd's PL320 32V-2A Power Supply Unit (PSU). The chemical buffer chosen for this experiment was HEPES (N-2-Hydroxyethylpiperazine-N'2-ethanesulfonic acid). The reference electrode was a standard silver/silver chloride (Ag/AgCl) from CHS Instruments, and the electrode's voltage was supplied by Keithley 6430 SourceMeter®. This SourceMeter can supply a voltage to the reference electrode and simultaneously measure the leakage current from the electrode. In this experiment, the reference electrode voltage was swept from 0 volt to 1.8 volts in 0.1 volt increments. The output V_{OUT} of the ISFETs averaging array was probed and displayed by LeCroy Wavepro® 7300A. All post-processing of these measurement results were done by The MathWorks™ MATLAB.

Figure 6-7 plots the output signal of the ISFET averaging array, V_{OUT} against the reference electrode voltage V_{ref} , and Figure 6-8 plots the leakage current associated with the reference electrode against the electrode's voltage. The V_{OUT} is very linear to V_{ref} in the region from 0.1 to 1.8 volts. A linear model relating V_{out} and V_{ref} can be expressed as:

$$V_{OUT} = 0.992V_{ref} + 0.47 \quad (6.1)$$

The error, or the residual, predicted by Equation 6.1 is less than 2% in the 0.1 volt to 1.8 volt range. This result suggests that the ISFETs averaging array is very linear to the reference electrode voltage.

On the other hand, the leakage current of the reference electrode seems to be bias dependent. As illustrated in Figure 6-8, a higher leakage current is the result of higher

reference electrode voltage. Therefore, it is in-conclusive to use a zero-volt to bias the reference electrode. The optimal voltage bias to the reference electrode has to be determined experimentally.

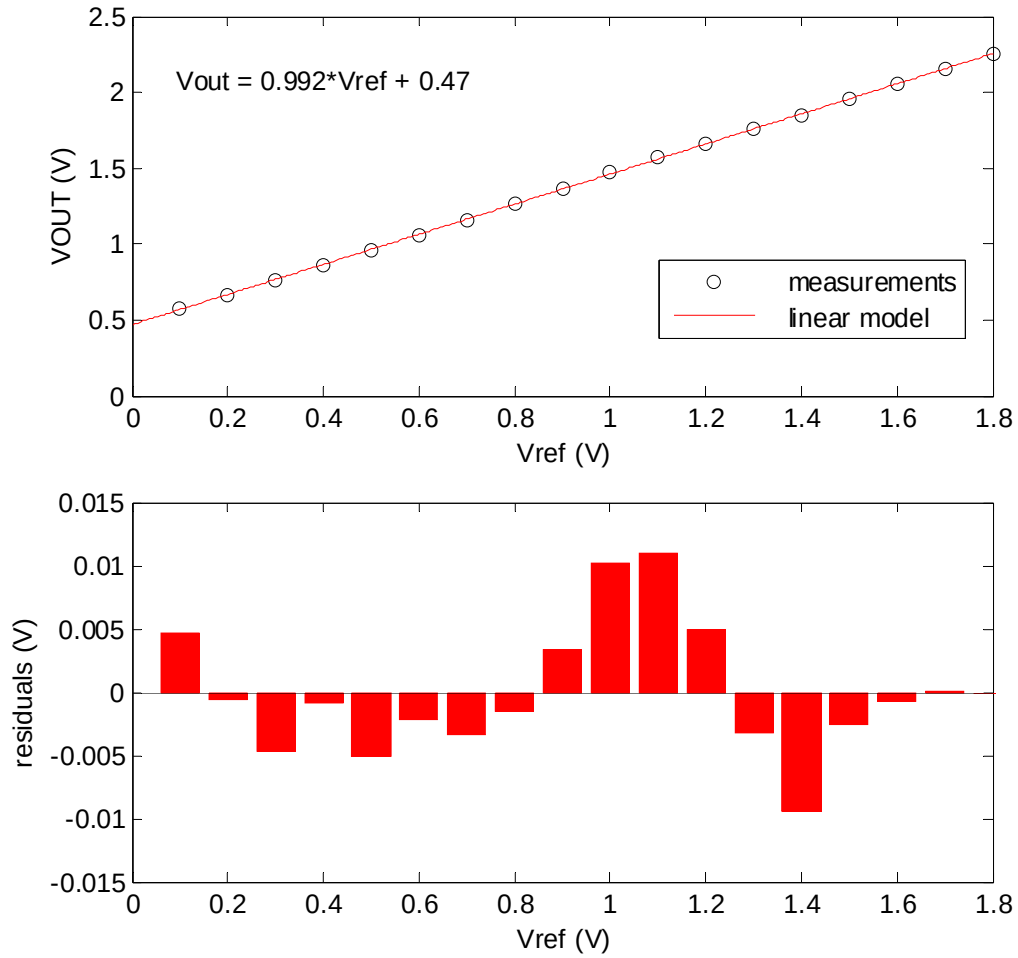


Figure 6-7: Measured output (V_{OUT}) of the ISFETs averaging array versus reference electrode voltage (V_{ref}).

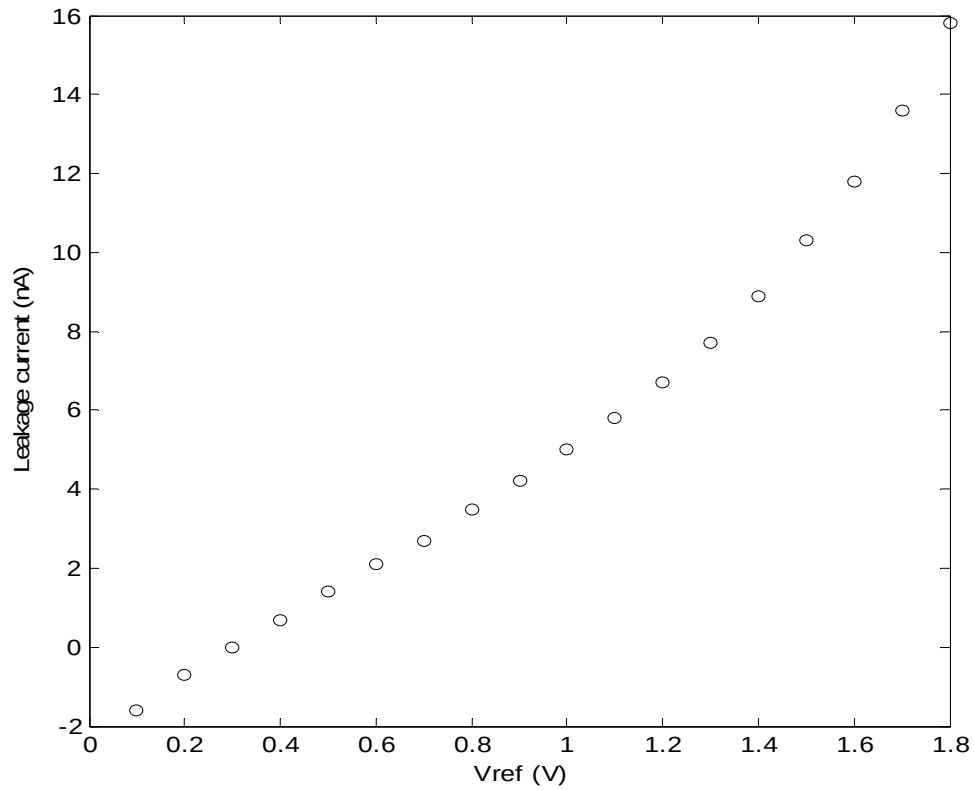


Figure 6-8: Measured reference electrode's leakage current versus bias voltage (V_{ref}).

6.2.2 Sensitivity to pH

This subsection is to determine the sensitivity of the ISFETs averaging array to pH. The maximum pH sensitivity, also known as Nernstian sensitivity, is 59 mV/pH at room temperature [4]. For instance, glass electrodes have a Nernstian sensitivity to pH. Nernstian sensitivity can also be found in tantalum pentoxide [4]. LPCVD-made silicon nitride shows sub-Nernstian responses from $45 - 56 \text{ mV/pH}$ [5], [6]. The variation of the sensitivity to pH in silicon nitride depends on the quality of the silicon nitride lattice in the sensing layer.

The experimental setup in this subsection was identical to Figure 6-6 with some minor modifications. Instead of using the custom prepared HEPES buffer solution, standard buffer solutions with a pH of 4.0, 7.4, and 10.0 were used in turn for this experiment. These standard chemical buffers, purchased from Hanna Instruments, have an accuracy of ± 0.01 pH. The measurements were taken in two hours for every pH buffer solution. This allowed enough time for the ISFETs' drift to settle. For instance, Figure 6-9 shows a typical response of the ISFET averaging array in the initial 80 minutes after testing with the chemical buffer having a pH of 4. This result indicates that the ISFETs did drift with the standard chemical buffer solutions, but the drift got smaller at the later times. It is therefore important to keep letting the experiment run until a steady state is reached. In the same figure, the output V_{OUT} is stabilized after 80 minutes, so the output can be taken after this instant.

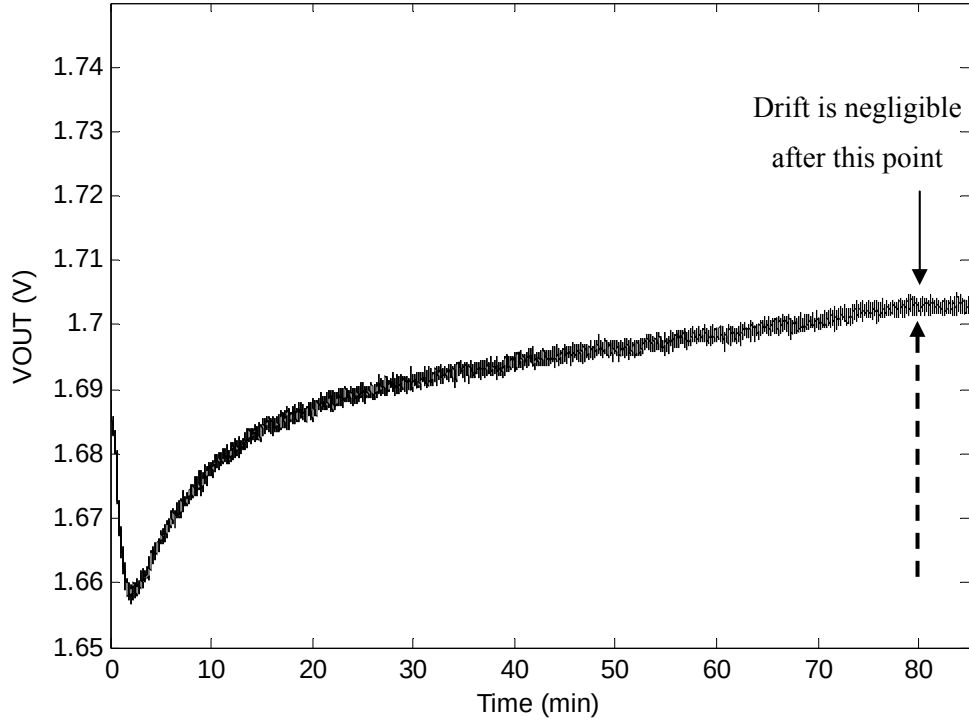


Figure 6-9: Measured transient response of ISFETs averaging array at pH=4.

The sensitivity of the ISFETs averaging array to pH is calculated based on the three sets of measured data calibrated at pH = 4.0, 7.4, and 10.0. The results of these experiments are plotted in Figure 6-10, and they show a linear trend between the output V_{OUT} and the pH. Next, a linear regression is used to determine the sensitivity to pH based on the three sets of measured data. The regression analysis predicts a sensitivity of 37.1 mV/pH . This sensitivity is less than the published values with the LPCVD-made silicon nitride, which have a sensitivity of $45 - 56 \text{ mV/pH}$. The error in predicting the linear regression model is less than 3 %. Note that the sensitivity was obtained from the average of the 64 on-chip ISFETs, which might have different offset voltages due to the trapped charges.

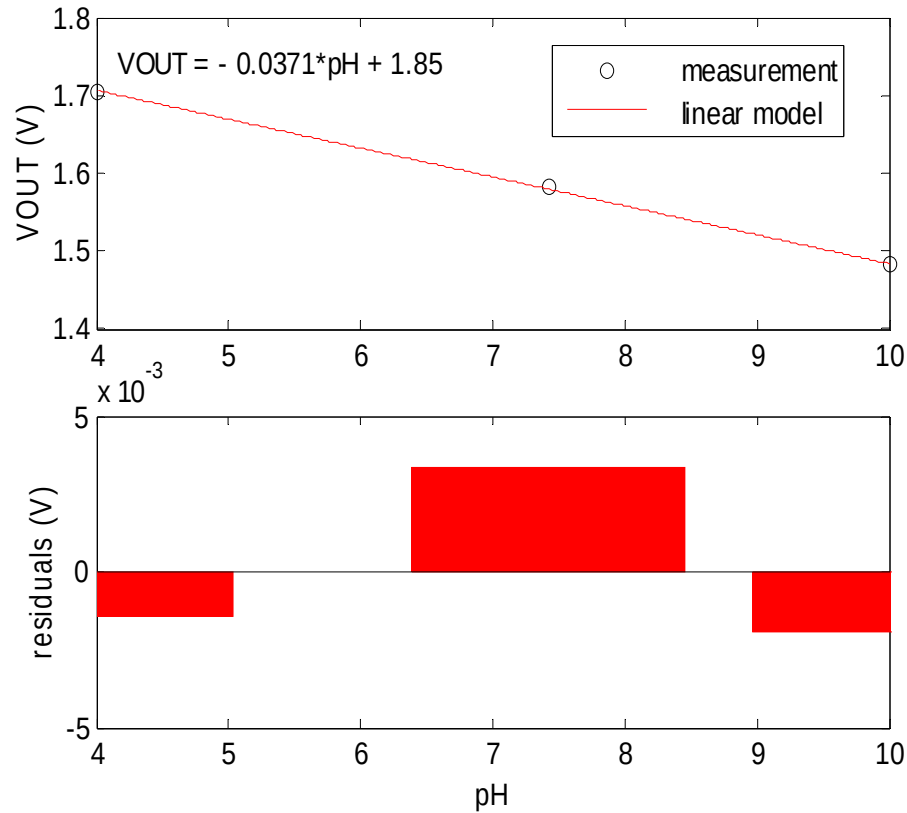


Figure 6-10: Measured output (V_{OUT}) of ISFETs averaging array versus pH. The error in predicting the linear equation is less than 3 %, which can be derived from the residuals.

6.2.3 Acid Titration

The objective of this subsection is to qualitatively look at the transient response of the ISFETs averaging array. In other words, how does the ISFETs array respond to a change in pH of a chemical solution in real time? Here, a custom-made chemical buffer, HEPES, was used because its pH can be altered relatively easily, as compared to the standard pH buffer solutions. The HEPES solution in test was 5 mL and had a pH of 7.6 initially. The acid used for the titration was a sulphuric acid in three different concentrations: 0.005M, 0.05M, and

0.5M. The volume of the acid to be added each time was 200 μL . Figures 6-11a, 6-11b, and 6-11c show the oscilloscope image during the titration events against the three different concentrations of the sulphuric acid. These figures show that the ISFETs averaging array can respond to a change in pH. In particular, Figures 6-11a and 6-11b show the discrete step responses for the acid added at the 400-second intervals. The more the acid added, the more the voltage increased. However, the settling time is also longer when a higher concentration of the acid was added. Figure 6-11c reveals that the response of the ISFETs averaging array was unable to settle even after 1800 seconds when the 0.5M acid was added at the time = 200 seconds.

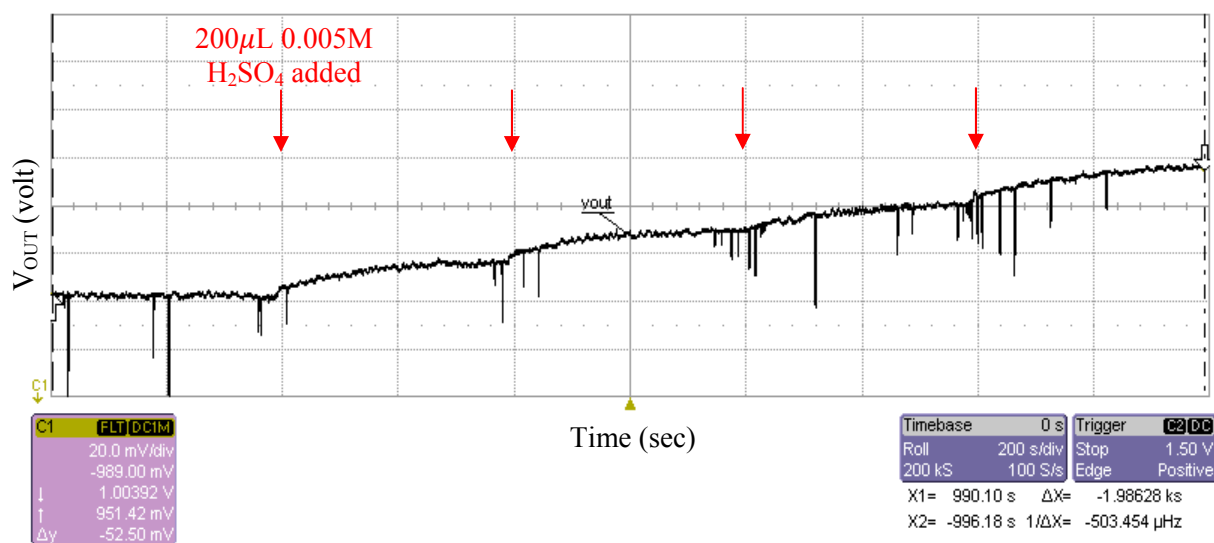


Figure 6-11a: Measured transient response showing 0.005M sulphuric acid added at 400 sec intervals.

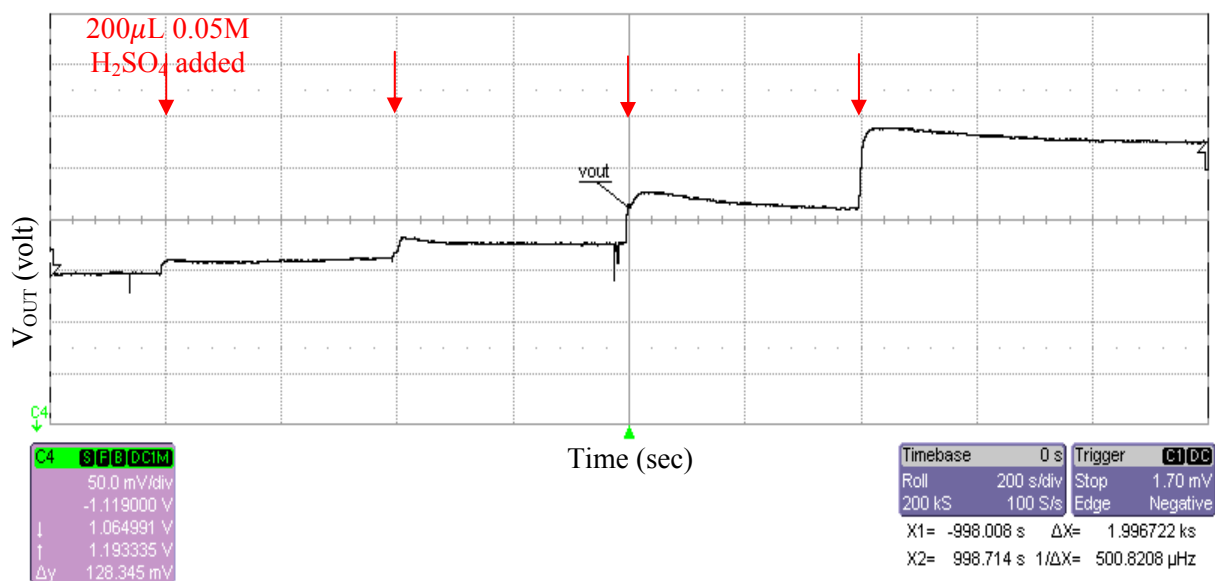


Figure 6-11b: Measured transient response showing 0.05M sulphuric acid added at 400 sec intervals.

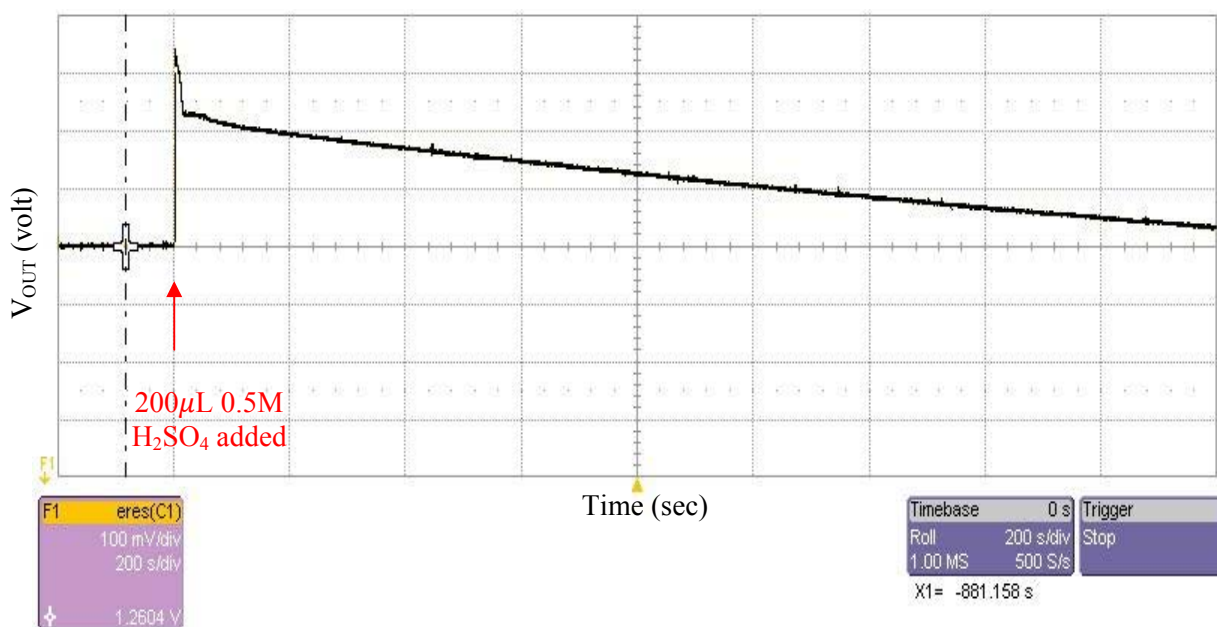


Figure 6-11c: Measured transient response showing 0.5M sulphuric acid added at time = 200 sec intervals.

6.2.4 Performance Evaluation between Sentron's ISFET and CMOS ISEFT on Acid Titration

This subsection evaluates qualitatively the dynamics between the Sentron's ISFET and the CMOS ISFET in respond to pH. The Sentron's ISFET is a non-CMOS discrete device; the drain and the source terminal are the only available pins on the dip-shaped PCB. Figure 6-12 shows the schematic used to interface Sentron's ISFET. The breadboard layout and the circuit components of this schematic are provided in the Figure 8-4 of Appendix. Basically, the drain source voltage of the ISFET was set to 0.51 volt, which is equal to the voltage dropped across the 5.1k resistor. The 100 μA current source and the current sink, which were chosen the same value as in Hammond's circuit [7], were used to bias the ISFET's drain current. Therefore, the ISFET was operating at the predefined operating point, and any change in the pH of the chemical solution will cause a change in the ISFET's source terminal voltage, which will be buffered to the output V_{out} .

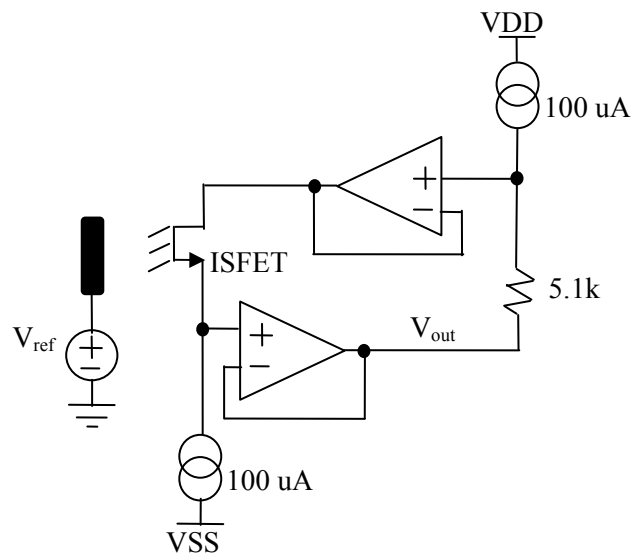


Figure 6-12: Sentron's ISFET front-end interface [7].

The Sentron's ISFET front-end interface was assembled entirely by the breadboard, and Figure 6-13 shows the actual placement of the Sentron's ISFET and the Ag/AgCl reference electrode.

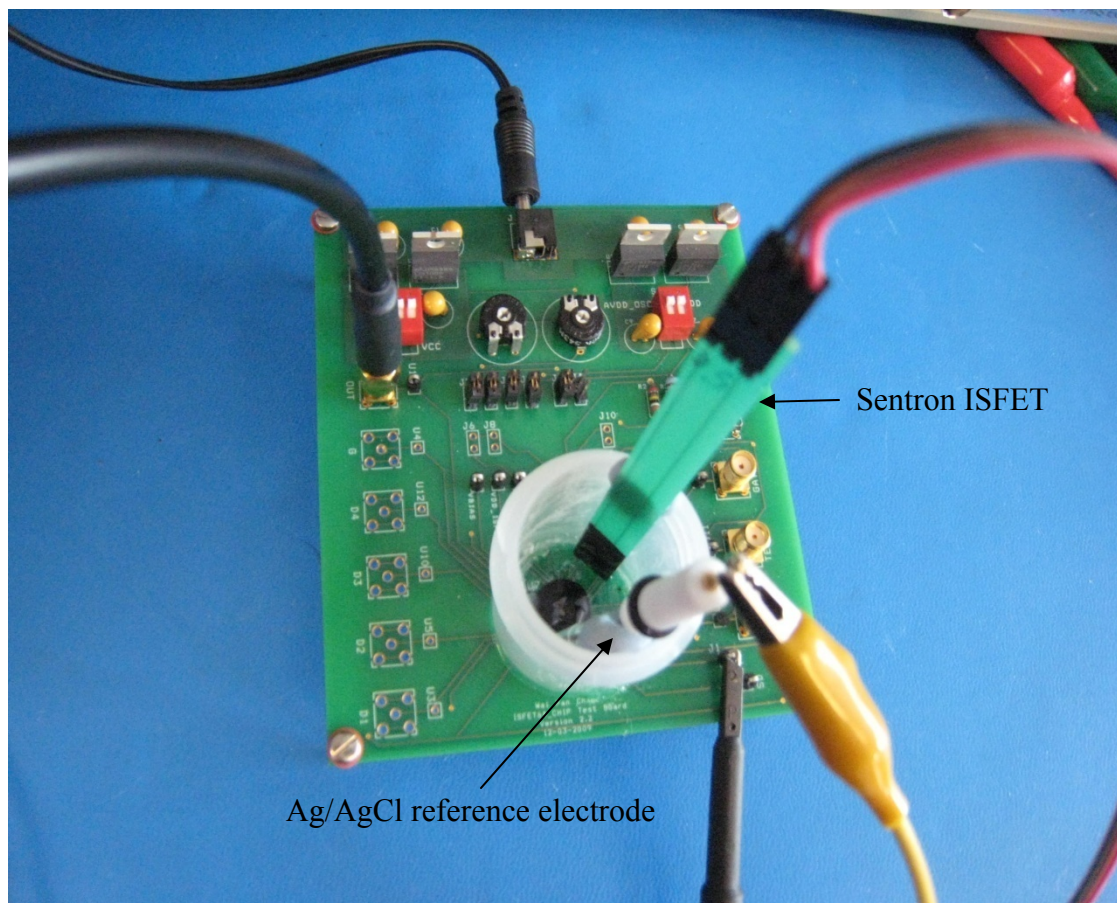


Figure 6-13: Experimental setup for Sentron ISFET and ISFET64_CHIP.

The experiment started by transferring 5 mL HEPES buffer solution (pH = 7.6) into the beaker on the PCB. Both the Sentron's ISFET and the CMOS ISFET are voltage biased by the same silver/silver chloride (Ag/AgCl) reference electrode at 0.5 volt. Then, a 100 μ L of 0.005M sulphuric acid was pipetted into the buffer solution at time = 200 sec and 600 sec.

Figure 6-14 captured the oscilloscope image during the titration events. There are two observations. First, both circuits responded to a step change in pH, with the Sentron's ISFET showing a larger amplitude change. This is because the Sentron's ISFET has a sensitivity of 50 mV/pH , while the CMOS ISFET was found to have 37.1 mV/pH . Thus, the step response from the Sentron's ISFET should be larger. Second, both circuits showed fast response, indicating that they are able to detect a small change in pH without experiencing significant drift. Nonetheless, it is unfair to compare their performance because of the two different types of ISFETs. On the other hand, the ISFETs averaging array consumed less than $66\text{ }\mu\text{W}$, while the constant current constant voltage source follower system used to interface the Sentron's ISFET consumed more than 1 mW . Therefore, the hardware implementation of the ISFETs averaging array developed in this thesis is more power efficient than the Sentron's design without trade-off accuracy.

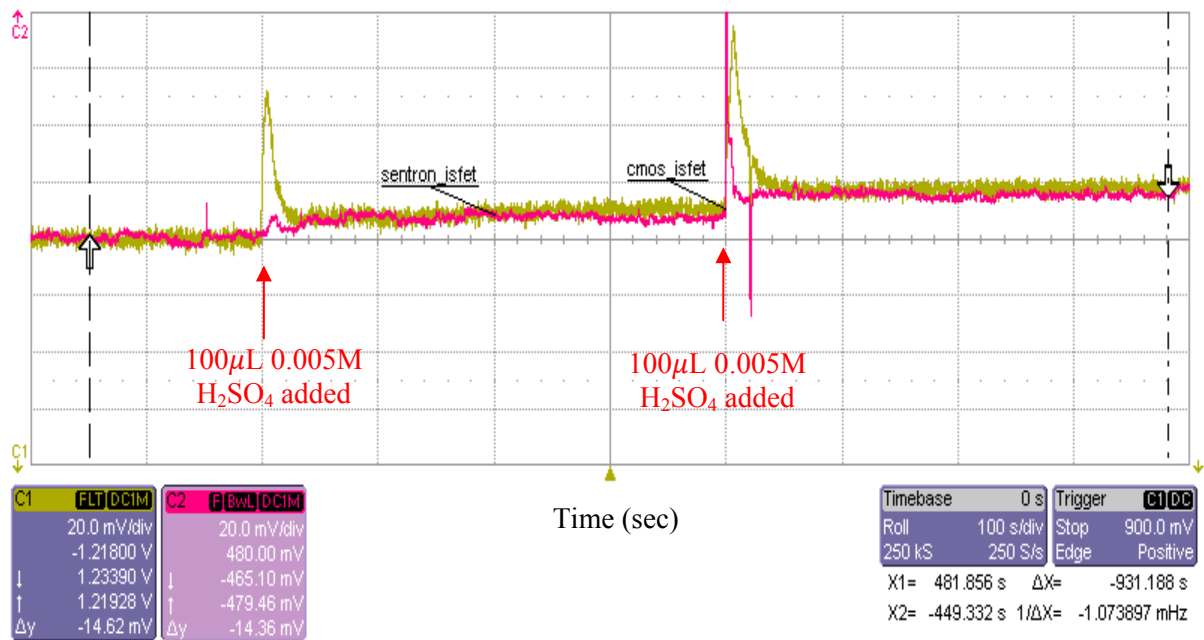


Figure 6-14: Measured transient response showing Sentron's ISFET (green) and CMOS ISFET (red).

6.3 Log Domain Oscillator Measurements

In this section, the measurement results of the log domain voltage controlled oscillator will be presented. The first set of results focuses on the oscillator transfer characteristics. The second set of results deals with the spectral characteristics of the oscillator.

6.3.1 VCO Transfer Characteristics

The aim of this subsection is to measure the log domain oscillator transfer characteristics. Figure 6-15 was the experimental setup to measure the VCO's transfer characteristics.

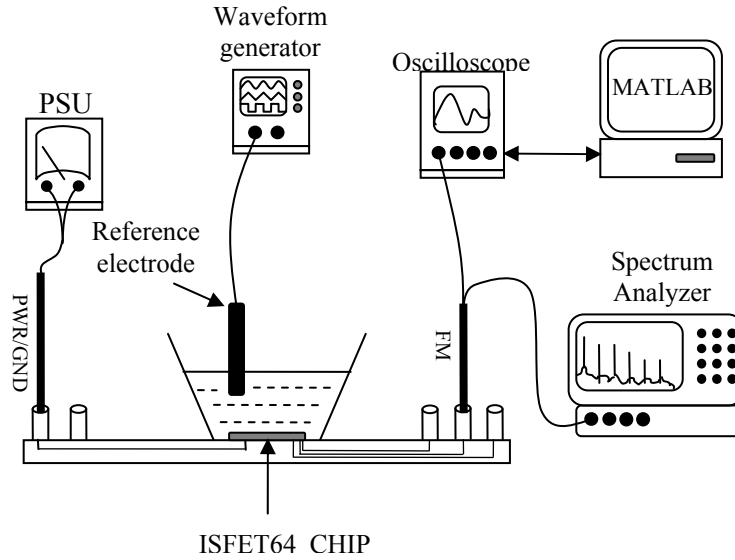


Figure 6-15: Experimental setup for the log domain oscillator.

The signal generator used in the experimental setup was Tektronix AWG 420, and the spectrum analyzer used in the measurement was Agilent 4395A. With the signal generator, any sinusoidal or other arbitrary waveforms can be transferred to the Ag/AgCl reference electrode. The frequency spectrums of the log domain VCO were captured almost instantaneously from the spectrum analyzer.

In order to measure the transfer characteristic of the log domain VCO, a DC voltage sweep on the reference electrode was performed from 0 volt to 2 volts in 0.1 volt increments. The oscillation frequency of the VCO was recorded from the spectrum analyzer. Figure 6-16 shows the oscilloscope image of the VCO's output when the bias voltage of the reference electrode was at 0.6 volt. The output of the log domain oscillator was a square waveform due

to hard-limiting by the inverters on-chip. The oscillation frequency was 90.8 *kHz* at that bias condition.

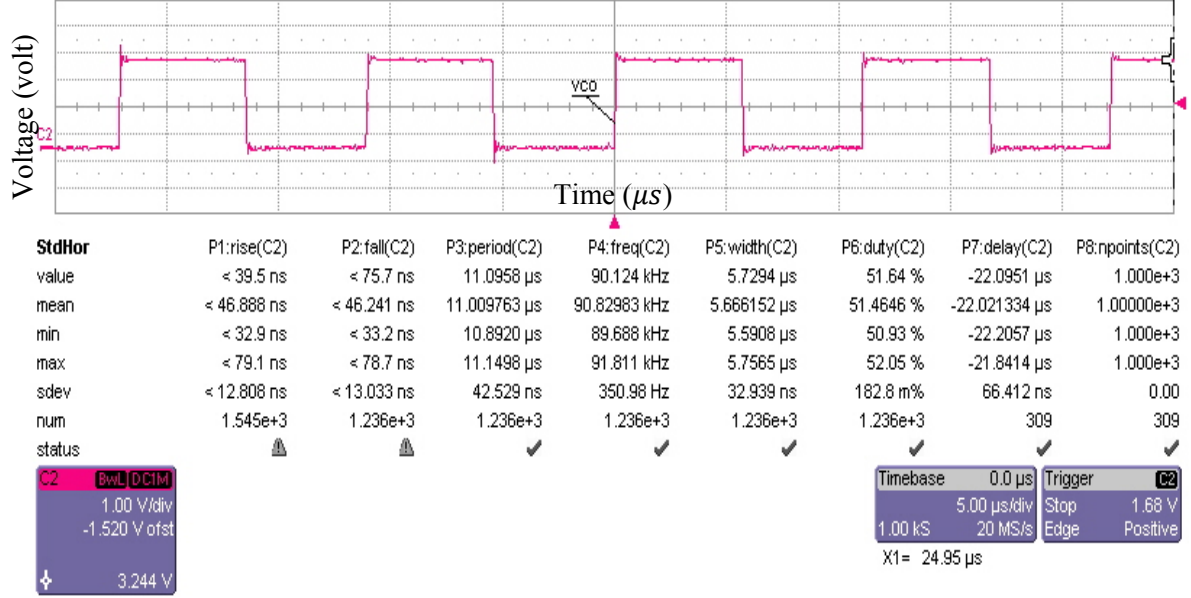


Figure 6-16: Measured transient of the log domain VCO.

Figure 6-17 plots of the oscillation frequency against the reference electrode voltage. The oscillator received the controlled voltage from 0 volt to 2 volts in 0.1 volt increments. However, the linear operating range was valid only in the region from 0.5 volt to 1.9 volts. The VCO transfer characteristic can be formulated as:

$$f_{osc} = 81V_{ref} + 43.1 \quad \text{where } V_{ref} = [0.5, 1.9] \text{ volts} \quad (6.2)$$

The sensitivity of the log domain VCO is 81 *kHz/volt* when the reference electrode bias voltage was operating from 0.5 volt to 1.9 volts. The error in predicting the sensitivity is less

than 1 % in this linear range. Note that the external resistor can adjust the gain of the VCO without any trade-off from the tuning range. The power consumption was predicted to be less than $10\ \mu W$ for the whole voltage sweep. In conclusion, the measurements results are closed to the simulation results.

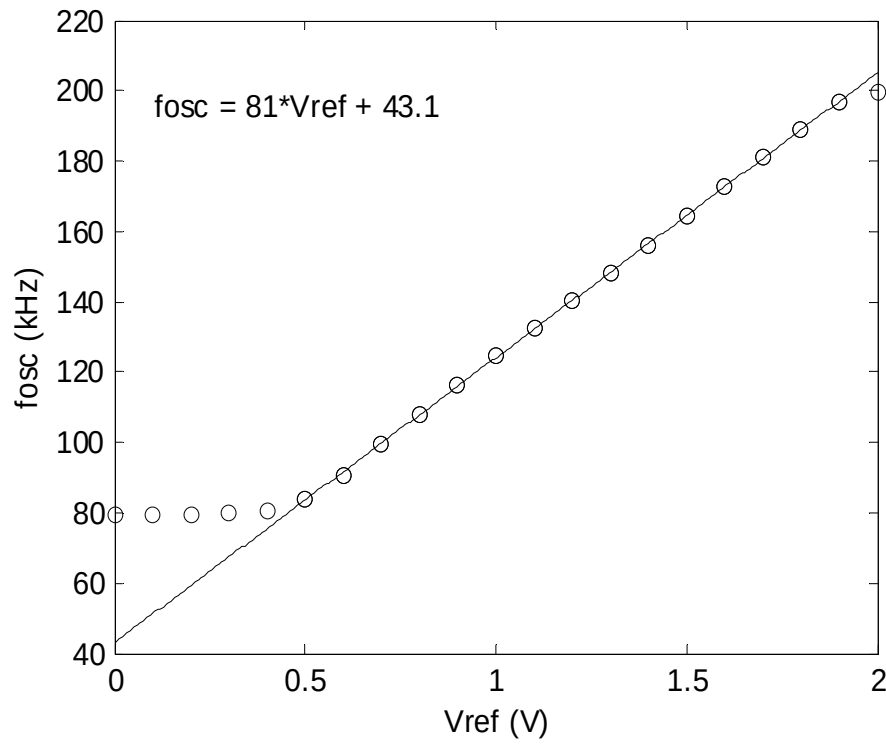


Figure 6-17: Measured VCO's oscillation frequency (f_{osc}) versus reference electrode voltage (V_{ref}).

6.3.2 VCO Spectrum Characteristic

There are two attributes to look at the frequency spectrum of the oscillator. What does the frequency spectrum of the log domain VCO look like when the reference electrode is biased

by (1) a DC voltage, and (2) a sinusoid? In this subsection, we present the measurement results which were obtained directly from the spectrum analyzer.

Figure 6-18 shows the spectrum of the VCO when it receives a DC voltage of 1.4 volts. There is about a 0 *dBm* signal located at 165 *kHz*, and this frequency corresponds to the oscillation frequency at that DC input. However, there are phase noise and spurs at the output. According to Figure 6-18, the phase noise is about -70 *dBc/Hz* at 10 *kHz* offset from the fundamental frequency. The phase noise at this frequency offset is about 10 *dB* higher than the simulation result. Besides, the same Figure shows some spurs, which are at least 50 *dB* lower than the sinusoidal power. Nonetheless, there is no spur predicted by the simulation. The discrepancy between the simulation and the measurement result could be attributed to (1) any modulated noise source from the power supply unit, (2) any modulated source from the laboratory's instruments, and (3) sub-harmonic distortions from the log domain oscillator.

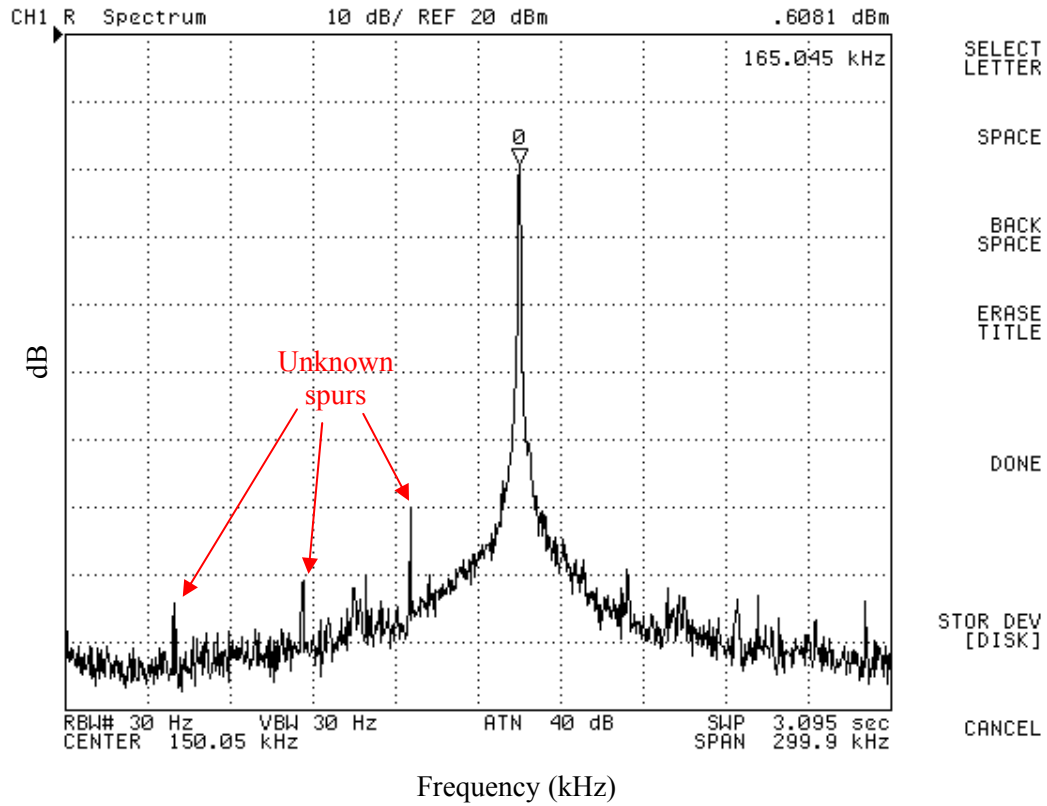


Figure 6-18: Measured frequency spectrum with DC input.

Figure 6-19 shows the spectrum of the VCO when it was driven by the sinusoidal signal. It shows that there was a band of signals generated at the output of the oscillator. The bandwidth of this signal is determined by the modulation index as well as the baseband's bandwidth. This is governed by Carson's rule [8]:

$$BW = 2f_m(1 + m_f) \quad (6.3)$$

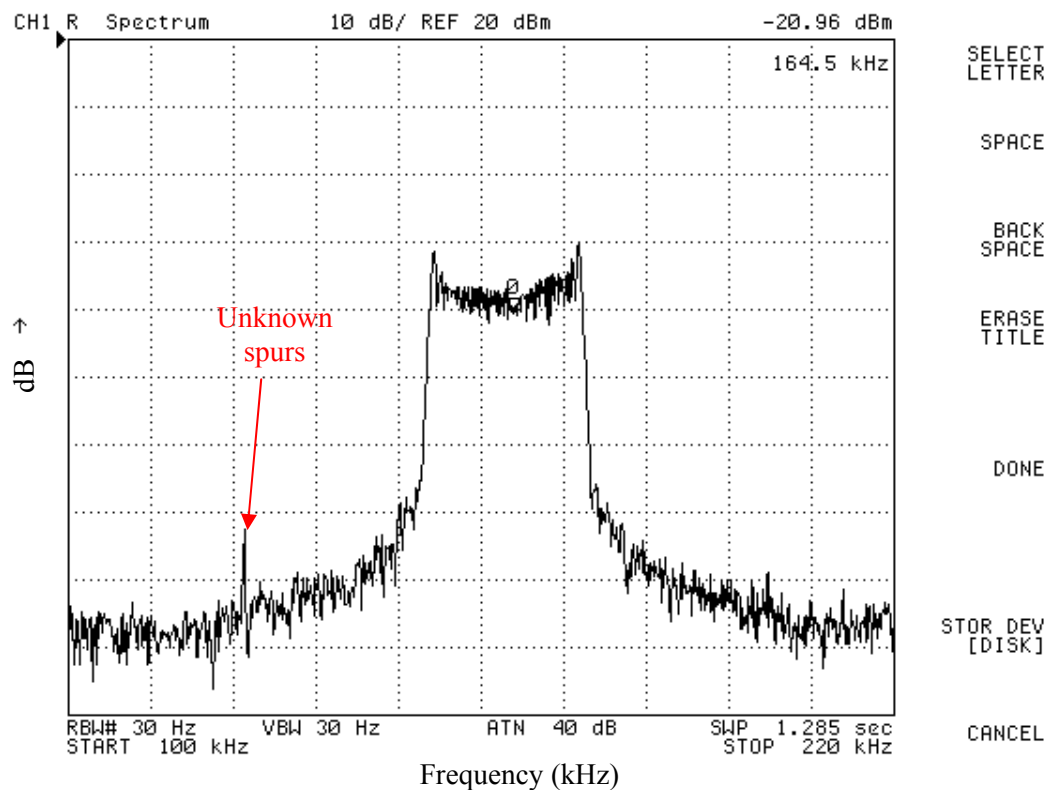


Figure 6-19: Measured frequency spectrum with sinusoidal voltage input.

The modulation signal in this case was $0.1 \times \sin(2\pi 100t)$ and the VCO gain was 81 kHz/Volt; hence, the modulation index is 81. According to Carson's rule, the predicted bandwidth is about 16.4 kHz. However, the bandwidth measured from Figure 6-19 was about 18.3 kHz. Therefore, the measured bandwidth is a bit larger than the simulated bandwidth. Other than this discrepancy, the measured spectrum also contains the unknown spur, which is just 30 dB lower than the FM's signal.

6.4 Sigma Delta Modulator Measurements

The performance of the reference-less sigma delta modulator is evaluated in this section. The $\Sigma\Delta$ modulator is composed of the ISFETs averaging array, the log domain VCO, and the digital logic. Figure 6-20 illustrates the experimental setup.

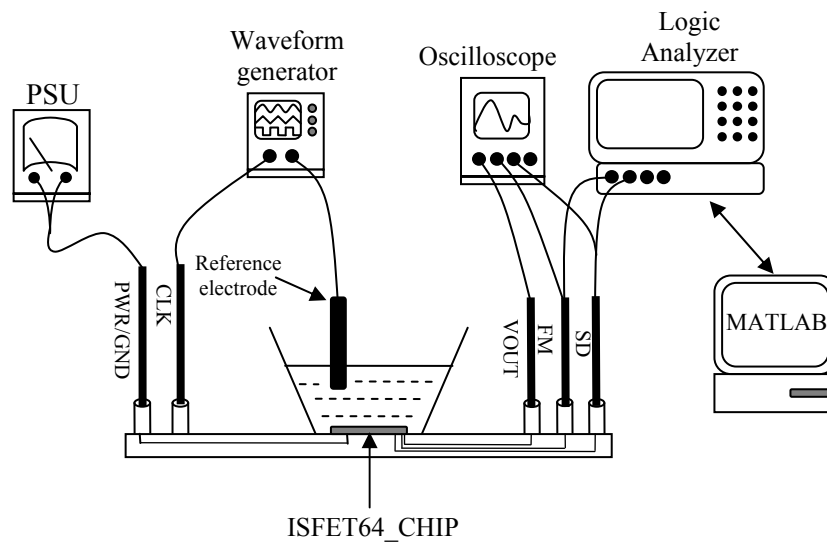


Figure 6-20: Experimental setup for reference-less $\Sigma\Delta$ modulator

Tektronix AWG420 was used to generate both the clock signal CLK with a frequency of 500 kHz and the input signals to the reference electrode. The input signals to the reference electrode was (a) a DC of 1.4 volts, (b) a sinusoid of $1.4 + 0.12\sin(2\pi 100t)$ volts, and (c) a sinusoid of $1.4 + 0.12\sin(2\pi 500t)$ volts for three tests. The output SD was data-logged by Tektronix TLA5202 Logic Analyzer.

Figure 6-21 captured the transient response from the sigma delta modulator, which consists of the FM as the intermediate output of the modulator, the CLK as the input to the modulator, and the output SD. Note that the output SD is synchronized by the input CLK.

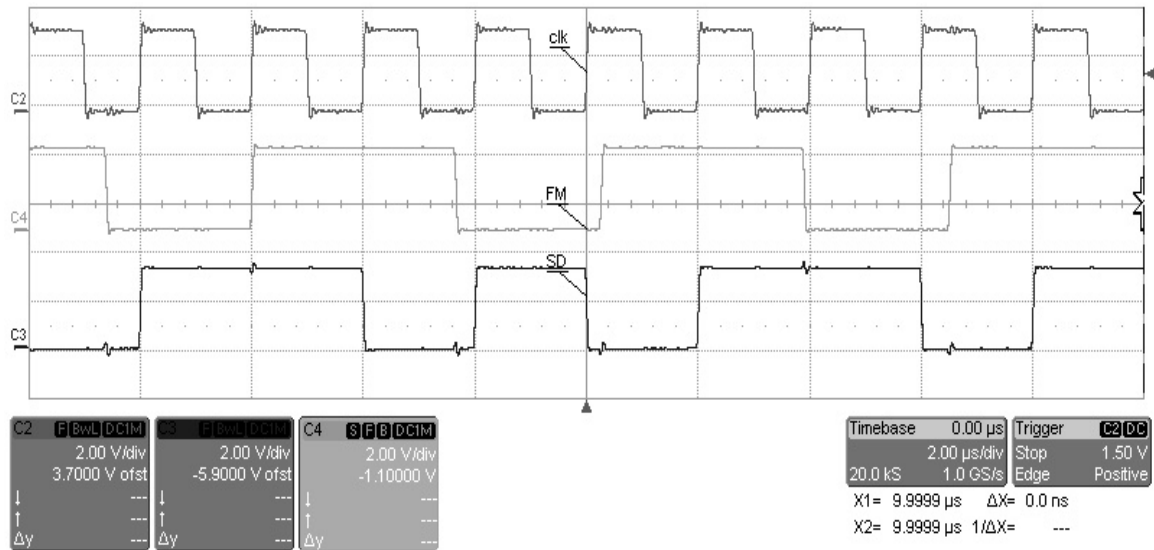


Figure 6-21: Measured transient response of the sigma delta modulator using VCO where CLK represents a clock input, FM represents an intermediate output, and SD represents the output of the sigma delta modulator.

The power spectral density (psd) of the output SD was estimated by MATLAB from its 2^{16} samples using a Hanning window, and the results are plotted in Figure 6-22. Both Figure 6-22 (a) and (b) show the existence of the baseband signals, one at 100 Hz and the other at 500 Hz for the two separate cases. On the other hand, the noise floors shown in Figure 6-22 exhibit a 1st order noise shaping at frequency above 10 kHz. The flat noise floor situated below 10 kHz could be the noise generated from the chip. The overall Signal-to- Noise Ratio

(*SNR*) was predicted to be about 45 *dB*, effectively representing 8-bit information. The fact that the modulator can produce a *SNR* of about 45 *dB* with the 500 *Hz* baseband signal suggests that the bandwidth of the instrumentation system can occupy 1 *kHz*. From the above discussions and results, the reference-less sigma delta modulator achieves 8-bit accuracy under 80 μW .

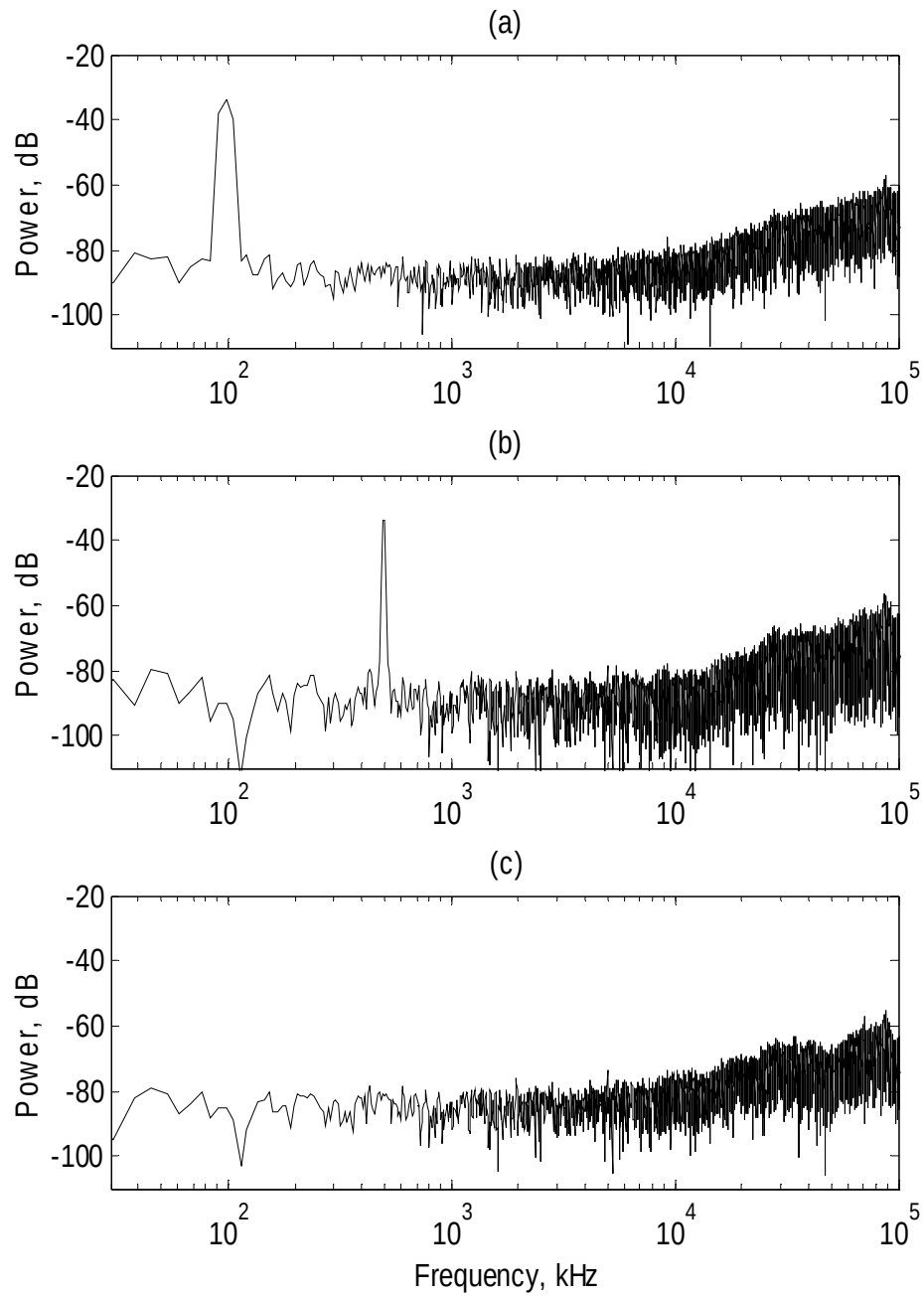


Figure 6-22: Measured power spectral density. (a) Input: $1.4 + 0.12 \times \sin(2\pi 100t)$ volts, (b) Input: $1.4 + 0.12 \times \sin(2\pi 500t)$ volts, and (c) Input: DC of 1.4 volts [9].

6.5 pH to digital conversion.

To evaluate the sigma modulator performance against pH inputs, spectral analysis might not be a good way to look at because the pH of a chemical solution changes very slowly in real time. Since the pH in a solution is almost unchanging in case of no chemical disturbance, the modulator will only output a bit-stream data, whose average value in a given period of time is the scaled version of the FM's carrier frequency, as seen in Equation 2.5. Recall that the free running frequency of the FM signal is depended on a steady pH, so the other way to examine the relationship between the pH and the sigma delta output is to evaluate the DC content of the sigma delta bit-stream. By counting the number of ones in the sigma delta output in a 100 *ms* period, the DC value of the bit-stream could be estimated. However, the counting procedure was post-processed in MATLAB.

The experiment consisted of testing the three pH buffer solutions, pH = 4, 7.42, and 10 with the ISFET64_CHIP. The oscilloscope monitored the output voltage of the ISFETs averaging amplifier. When the ISFETs' response stabilized, the logic analyzer started recording the sigma delta output bit-stream. When the recording finished, the data in the logic analyzer were exported to MATLAB for post-processing. The result is displayed in Figure 6-23. The circle represents the measured number of ones, while the straight line represents the linear regression model. It showed a very good match between the digital output and the pH input with less than 0.5 % of error.

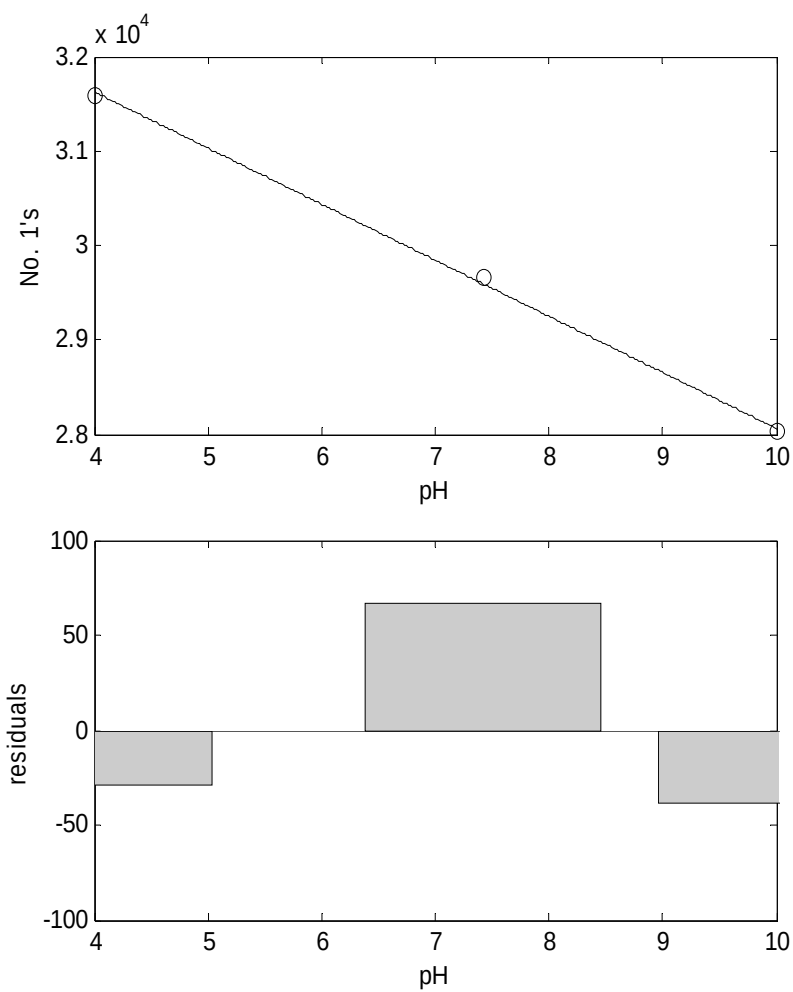


Figure 6-23: Measured sigma delta modulator's output versus pH

6.6 Performance of ISFET64_CHIP

To comprehend the performance of ISFET64_CHIP, all the various circuit building blocks including the ISFETs averaging amplifier, the log domain VCO, and the whole instrumentation system (the reference-less sigma delta modulator) have been tested in hardware and reported in this chapter. Except for the wire-bonding and the chip encapsulation, the chip has not had any CMOS post-processing. Thus, the ISFET64_CHIP is a truly monolithic ISFETs instrumentation system fabricated in standard CMOS process.

First, the ISFETs averaging amplifier has been verified as a linear pH to voltage converter. The averaging array is configured as a source follower system on chip. The averaging amplifier was configured with a closed loop gain of one, and the gain error stays within 1% in response to a reference electrode voltage over 1.8-volt range. This range is far enough to cover the 14 units of pH measurement. In fact, because the ISFETs array only achieved a sensitivity of 37 mV/pH from $\text{pH}=4$ to 10, the 1.8-volt dynamic range is more than enough for the pH measurements used in this thesis. In regarding the trapped charges associated with the floating gate node of the on-chip ISFETs, which can cause a large offset voltage to the system. Based on the measurements, however, the effect of the trapped charges did not appear on the aggregate average of the ISFETs averaging array.

Second, the log domain VCO has been shown to have a linear transfer gain in about 1.5-volt controlled voltage input. The carrier frequency is adjustable from 80 kHz to 200 kHz . Based on the $10\text{ M}\Omega$ external loading, the sensitivity of the VCO is determined to be 81 kHz/volt . The only under-achieved performance is the phase noise, which is about 10 dB

higher than the simulated phase noise at 10 *kHz* offset from the fundamental frequency. Anyway, the log domain VCO in this thesis is the first reported working oscillator in literature.

Last, the reference-less sigma delta modulator has been tested electronically and chemically. The modulator was operated by a 500 *kHz* clock in normal condition. When the input to the $\Sigma\Delta$ modulator is a sinusoid, it can attain a maximum *SNR* of about 45 dB, effectively representing 8-bit information. On the other hand, using a counter-based logic, the $\Sigma\Delta$ modulator is able to reveal a linear response to pH input.

The performance summary of the ISFET64_CHIP is tabulated in Table 6-I.

Table 6-1: Performance summary of ISFET64_CHIP [9]

Technology	0.18 μm 1 POLY 6 METAL CMOS process
Supply voltage	1.8V/3.3V
Chip area	1.6 mm x 1.6 mm
Power consumption	76 μW (excluding digital core and IO)
ISFET size	20 μm by 2 μm
Chemical sensitivity	37 mV/pH (an average of 64 ISFETs)
Reference electrode	Off chip (Ag/AgCl)
VCO gain	81 kHz/V (adjustable by off chip resistor)
Frequency range	80 $\leftrightarrow$ 200 kHz
Accuracy	8 bits
Bandwidth	1 kHz
Sampling frequency	500 kHz

6.7 Summary

This chapter has reported various measurement results of the fabricated ISFETs instrumentation system, called ISFET64_CHIP. Particularly, the ISFETs averaging amplifier, the log domain VCO, and the reference-less $\Sigma\Delta$ modulator have been tested in different ways to validate their functional performance. The chip's measurement results indicate that the proposed instrumentation system is able to achieve a linear relationship between a pH input and the digital output, with an accuracy of up to 8-bit of information. Most importantly, the effects of the trapped charges have not been observed in the instrumentation system. The most likely explanation to the diminished trapped charge effect, other than by a random event, is the action of the ISFETs averaging array.

6.8 References

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Chapter 7

Conclusion and Future Work

7.1 Conclusion

This thesis has discussed the design methodology for pH to digital conversions, using an array of ISFETs in an unmodified CMOS process. Unlike logarithmic or integrating ADCs which rely upon amplitude domain signal processing, the system suggested in this thesis has adopted the open loop, reference-less architecture which uses a voltage controlled oscillator to transform analogue signals due to chemical information into a pH-dependent frequency. A very simple digital logic is used at the end to digitize the intermediate FM signal to yield the bit-stream output which is spectrally identical to a 1st order sigma delta modulation.

The conversion from pH to electronic signals requires a frontend circuit to interface an ISFET, which is a pH sensor. In Chapter 3, a novel 64-input current feedback op-amp architecture has been discussed as an interface to an array of 64 on-chip ISFETs. Not only does this design provide redundancy to the system, but also it can minimize the impact of the trapped charges through the averaging. The signal-to-noise ratio of the system can be improved as more inputs are used. Note that the use of current feedback is to linearize the ISFETs in response to pH, and this is very important as ISFETs are a non-linear voltage to current converter.

Another important achievement made in this thesis is the successful implementation of the log domain voltage controlled oscillator in a working silicon chip. Chapter 4 has discussed how the log domain oscillator operates. Apart from the low power operation, the frequency of the oscillation in this oscillator is linear proportional to the reference electrode's voltage and the pH. Since the $SQNR$ of the instrumentation system is depended on the linearity of the VCO, the log domain VCO highly meets the system's requirement.

Chapter 5 has validated the system functionality under the various circuit simulations, and Chapter 6 has illustrated the experimental setup and reported the measurement results in ISFET64_CHIP, which was fabricated by the UMC 0.18 μm CMOS process. The chips were wire-bonded and encapsulated in a custom designed PCB, and various static and dynamic measurement results have been presented to verify the performance of ISFET64_CHIP. The strong point of this instrumentation system is that the unmodified chips can produce a very linear pH response, with a maximum accuracy of 8-bit of information.

7.2 Future Work

The proposed ISFETs instrumentation can be better performed in silicon through (1) device perspective, (2) circuit perspective, and (3) system perspective. Each of these perspectives will be discussed briefly in the following paragraphs.

7.2.1 Device Perspective

Recall from Chapter 2 that the ion-sensitive membrane in the CMOS ISFET is the topmost passivation layer. The effective surface of the ion-sensitive membrane is a rectangular block. This thesis postulates that the rate of the chemical reactions over the membrane can be enhanced by an array of ISFETs, so the drift can be reduced. This is based upon the fact that the surface area to volume ratio of the ion-sensitive membrane can be increased by using an array of ISFETs. Nonetheless, a more effective way to increase the surface area to volume ration is to use a needle-shaped membrane as shown in Figure 7-1.

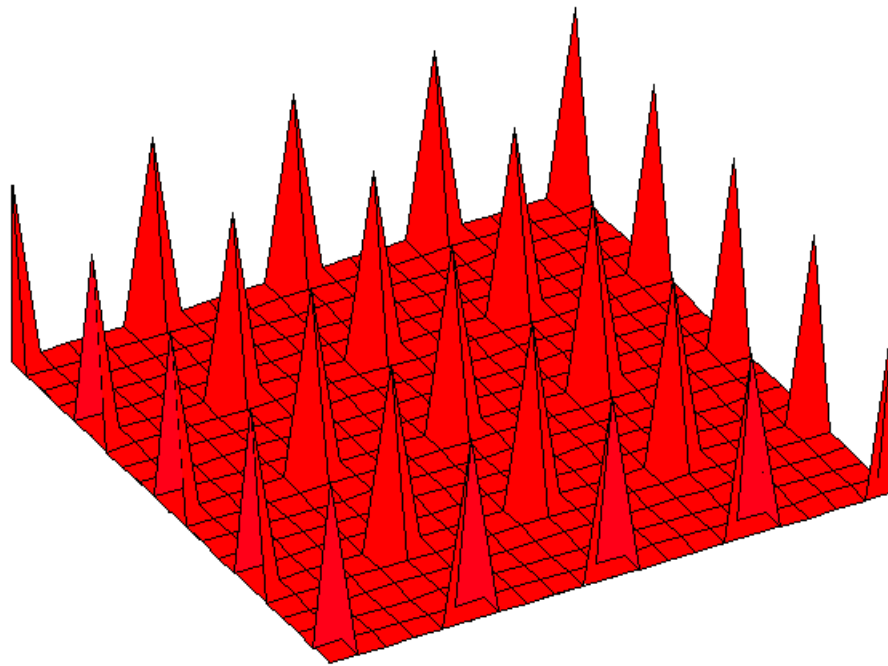


Figure 7-1: Sketch of a micro-needle based ion-sensitive membrane

However, the fabrication of these micro-needles is not compatible to standard CMOS process, so the concept is not readily available to be tested. At the moment, this structural modification to the passivation layer can only be made in laboratories using micromachining.

7.2.2 Circuit Perspective

The proposed log domain oscillator described in this thesis is sensitive to temperature. In fact, Equation 4.25 reveals that the oscillation frequency is inversely proportional to the absolute temperature. To reduce the temperature sensitivity, a proportional to absolute temperature (PTAT) bias current can be applied in Equation 4.25 such that the temperature effect on the PTAT current can be cancelled by the temperature effect on the oscillation frequency. Coincidentally, the bias current generated from the ISFETs averaging array is proportional to the temperature. Therefore, there is a chance where the temperature sensitivity from the log domain oscillator can be reduced by the temperature sensitivity of the ISFETs in response to pH. Future work can be focused on circuit designs to optimize the temperature compensation.

7.2.3 System Perspective

The measured signal to noise ratio of the sigma delta modulator in silicon cannot be attained more than 45 dB, where in simulation the *SNR* can be attained more than 70 dB. The discrepancy between the simulation results and the silicon measurements is the underestimation of the phase noise in simulation. The origin of the phase noise is the device

noises, which include the flicker noise and the thermal noise. One way to reduce the device noise in a silicon chip, especially the flicker noise, is to optimize the device's aspect ratio or the transconductance in order to achieve lower noise. Another way to improve the SNR of the system is to employ parallel sigma delta conversions using a delay line [1]. This parallelism of the sigma delta conversions can increase the SNR of the system by pushing down the noise floor. Recall that signals are added algebraically whereas noises are added orthogonally. However, any harmonics generated in the system cannot be removed by the averaging or the parallelism because the harmonics are very much correlated to each other, so techniques to reduce any non-linearity can be explored in the future.

In conclusion, the thesis has shown a good proof of concept as frequency to digital conversion with on-chip ISFETs. Further work will be aimed at improving general performance.

7.3 Reference

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Chapter 8

Appendix

Consider a 2-input current feedback opamp's macromodel configured with a closed loop gain of one as shown in Figure 8-1.

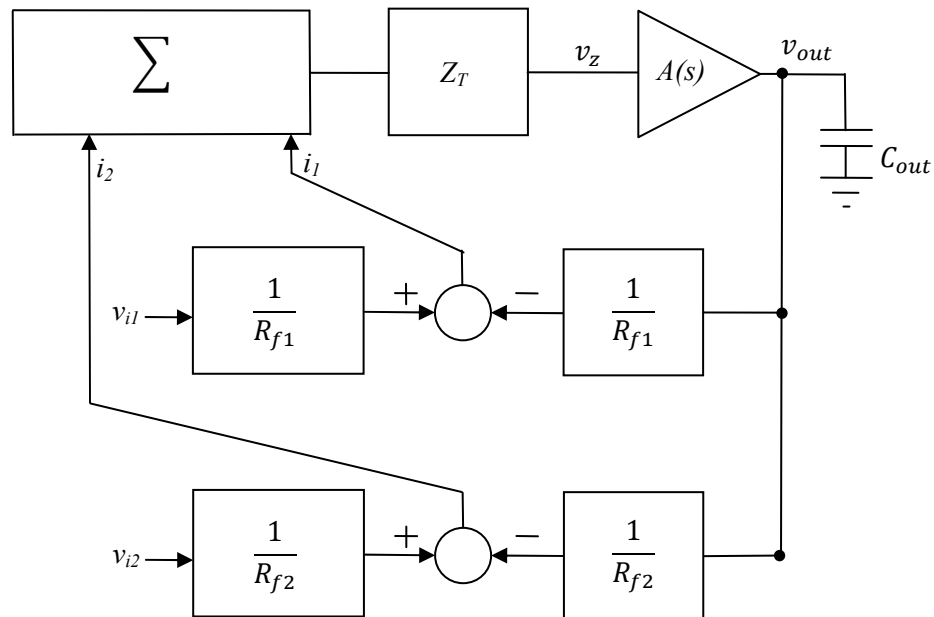


Figure 8-1: 2-input current feedback opamp macromodel.

v_{out} can be obtained as:

$$v_{out} = \frac{v_{i1}R_{f2} + v_{i2}R_{f1}}{\frac{R_{f1}R_{f2}}{Z_T A(s)} + R_{f1} + R_{f2}} \quad (8.1)$$

where $Z_T = \frac{R_T}{1+sR_TC_T}$ and $A(s) = \frac{1}{1+s\frac{C_{OUT}}{g_m}}$. The characteristic equation (i.e., the denominator

of Equation 8.1) is a 2nd order polynomial of s , and this is expressed in Equation 8.2.

$$(1 + sR_TC_T) \left(1 + s\frac{C_{OUT}}{g_m} \right) R_{f1}R_{f2} + R_T(R_{f1} + R_{f2}) = 0 \quad (8.2)$$

Assuming that R_T is several orders of magnitude greater than R_{f1} and R_{f2} , Equation 8.2 can be simplified to Equation 8.3.

$$s^2 + s\frac{g_m}{C_{OUT}} + \frac{(R_{f1} + R_{f2})g_m}{R_{f1}R_{f2}C_TC_{OUT}} = 0 \quad (8.3)$$

Therefore, the pole frequency ω_n and the quality factor Q can be expressed as:

$$\begin{cases} \omega_n = \sqrt{\frac{(R_{f1} + R_{f2})g_m}{R_{f1}R_{f2}C_TC_{out}}} \\ Q = \sqrt{\frac{(R_{f1} + R_{f2})C_{OUT}}{R_{f1}R_{f2}g_mC_T}} \end{cases} \quad (8.4)$$

Let δ_1 and δ_2 be the random variation of the resistor R_{f1} and R_{f2} respectively, the mismatch of ω_n and Q are both proportional to the following expression:

$$\Delta\omega_n, \Delta Q \propto \sqrt{\frac{R_{f1}(1 \pm \delta_1) + R_{f2}(1 \pm \delta_2)}{R_{f1}(1 \pm \delta_1)R_{f2}(1 \pm \delta_2)}} \quad (8.5)$$

Assuming that $\delta_1 \times \delta_2 \ll 1$, Equation 8.5 can be approximated to Equation 8.6.

$$\Delta\omega_n, \Delta Q \propto \sqrt{\frac{R_{f1}(1 \pm \delta_2) + R_{f2}(1 \pm \delta_1)}{R_{f1}R_{f2}}} \quad (8.6)$$

Equation 8.6 suggests that the random variation of the resistors will increase the mismatch of ω_n and Q , so a good layout is needed to place the feedback resistors R_f in good matching. The above analysis can also be generalized for a N-input current feedback model with N mismatched resistors, but it will not be derived further here in this thesis.



Table 8-1: ISFET64_CHIP's pin connections. Pins with shaded area are used in the printed circuit board (PCB).

Pin #	Name	Description	Attributes
1	R_EXT	External resistor to set up the gain of the VCO	Analogue signal output
2	VDD2	3.3 volt power supply to BIAS GEN	Analogue power
3	VSS2	BIAS GEN's ground (0 volt)	Analogue ground
4	RCUT	Power cut for VDD2 from the right	NC
5	LCUT	Power cut for VDD1	NC
6	VDD1	3.3 volt power supply to ISFET averaging array	Analogue power
7	PBIAS	Bias voltage used in ISFETs averaging array	Analogue signal out
8	VSS1	ISFETs averaging array's ground (0 volt)	Analogue ground
9	VOUT	ISFETs averaging array output	Analogue signal output
10	G	Gate bias for test devices	NC
11	D4	Drain bias for test device A	NC
12	D3	Drain bias for test device B	NC
13	D2	Drain bias for test device C	NC
14	D1	Drain bias for test device D	NC
15	RCUT	Power cut for VDD1	NC
16	GND3O	IO pad ring ground (0 volt)	Chip's ground
17	VCC3O	IO pad ring power (3.3 volts)	Chip's power
18	OUT[1]	Test circuit output	NC
19	OUT[2]	Test circuit output	NC
20	OUT[3]	Test circuit output	NC
21	OUT[4]	Test circuit output	NC
22	OUT[5]	Test circuit output	NC
23	OUT[6]	Test circuit output	NC
24	OUT[7]	Test circuit output	NC
25	OUT[8]	Test circuit output	NC
26	OUT[9]	Test circuit output	NC

27	OUT[10]	Test circuit output	NC
28	SD	Sigma delta output	Digital output signal
29	FM	VCO output	Digital output signal
30	VCC	1.8 volt power supply to digital circuits	Digital power
31	GND	Digital ground (0 volt)	Digital ground
32	CLK	Digital clock	Digital signal input
33	RESET	Digital reset	Digital signal input
34	TEST	Active when RESET is high	Digital signal input
35	VCC3O	IO pad ring power (3.3 volts)	Chip's power
36	GND3O	IO pad ring ground (0 volt)	Chip's ground
37	LCUT	Power cut for VDD3	NC
38	VDD3	3.3 volts power supply to VCO	Analogue power
39	VSS3	VCO's ground (0 volt)	Analogue ground
40	RCUT	Power cut for VDD3	NC
41	LCUT	Power cut for VDD2	NC
42	GATE	Gate bias for test circuit	NC
43	VBG	Bandgap voltage reference	Analogue signal output
44	R_TUNE	External resistor to set up the bias current	Analogue signal output

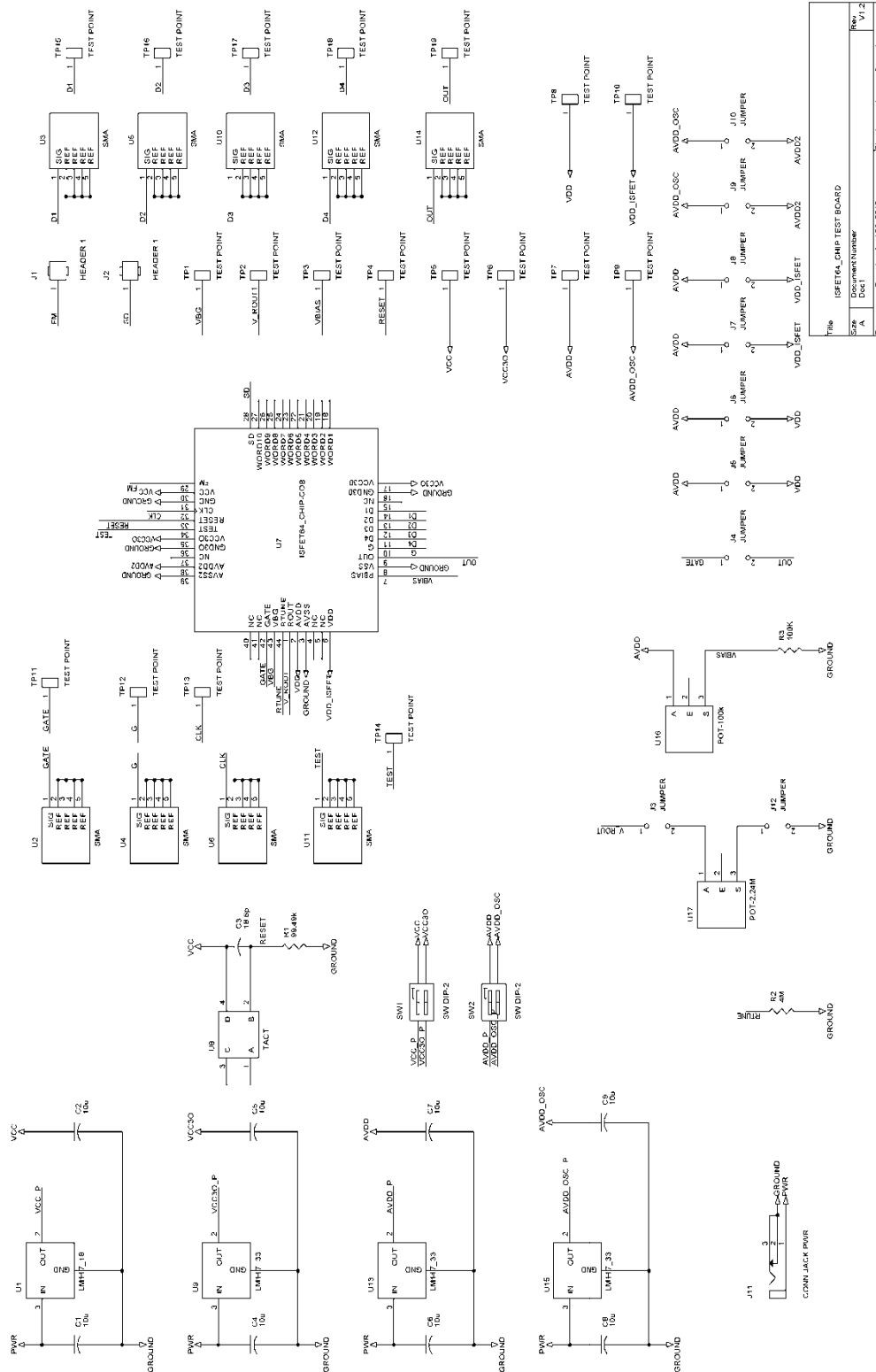


Figure 8-2: ISFET64 CHIP test board schematic.

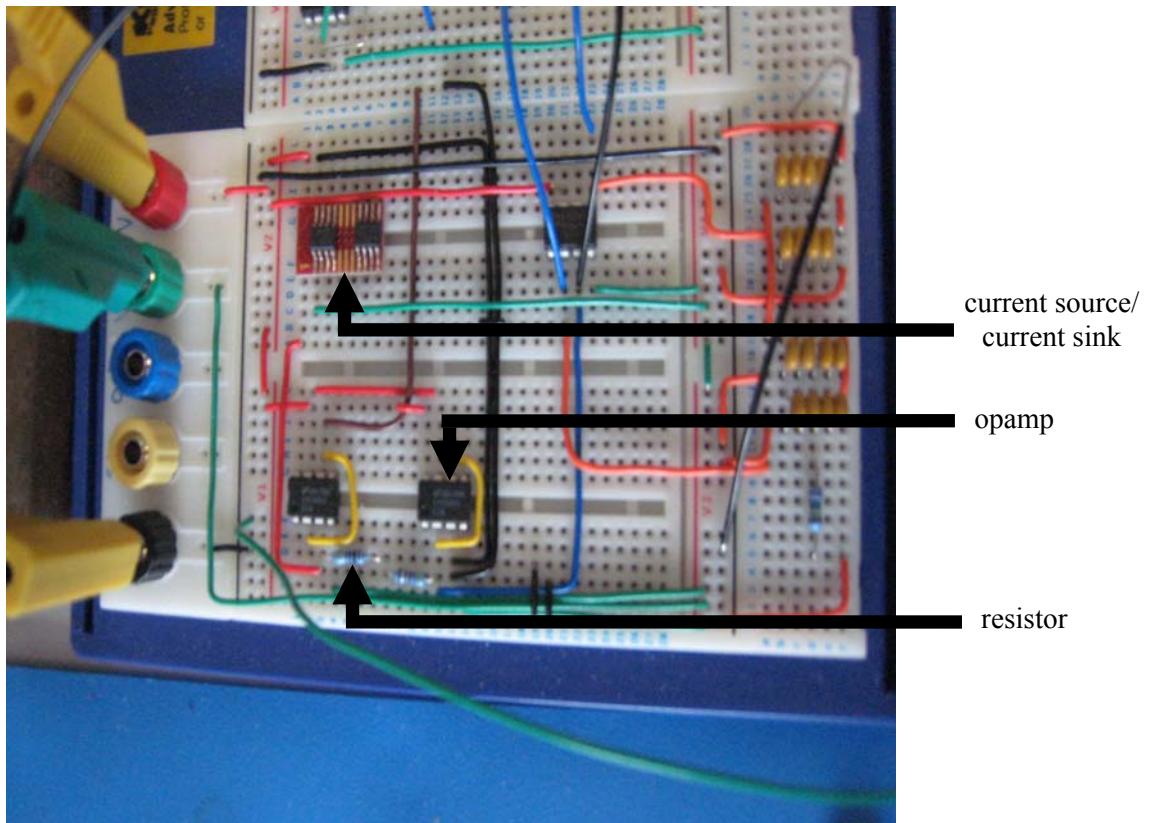


Figure 8-3: Sentron's ISFET frontend interface

Opamp: LMC6042 CMOS dual micropower operational amplifier

ISFET: Sentron ISFET, not shown in this figure.

Current source and current sink: REF200 dual current source/current sink of $100\ \mu\text{A}$.

Resistor: $510\ \Omega$