Published in IEEE Trans. Ind. Electr., DOI: 10.1109/TIE.2024.3522467

Dual Storage Power Management for Energy Autonomous Microsystems

Michail. E. Kiziroglou, Senior Member, IEEE, Steven W. Wright,
Eric M. Yeatman, Fellow, IEEE and Andrew S. Holmes, Member IEEE.

***Abstract*—A major challenge towards enabling energy autonomous microsystems is cold-starting, especially in real use case environments which are often uncertain and involve long inactivity periods. In this paper, a dual supercapacitor storage power management architecture is proposed, with the primary storage capacitor providing fast start-up and the secondary providing a large energy buffer. The circuit introduces a combination of a MOSFET switch and a buck converter that can handle efficient charge transport and eliminate leakage between the two storage capacitors, leading to faster cold starting. A start-up time reduction of more than two orders of magnitude over conventional solutions is experimentally demonstrated, for a 1.5 mF / 470 mF supercapacitor combination, without a compromise in overall efficiency. The various functional modes of the system are experimentally analyzed, using an inductive power line energy harvester with currents that correspond to an industrially defined aircraft sensor use case. For example, 11 mW and 32 mW regulated output was measured from a 10 A and 15 A RMS, 500 Hz power line respectively. The architecture is configurable and can be dynamically parametrized and controlled to optimize power routing according to functional priorities by the microcontroller of the powered system.**

***Index Terms*—Energy Harvesting, Power Autonomy, Microsystems, Supercapacitor, Power Management, Sensors.**

I. Introduction

THE emergence of low-power microprocessor cores, solid-state non-volatile memory, wireless communication and integrated silicon microsystems has allowed the implementation of portable multitasking electronic devices with unprecedented capabilities. This technology has been widely integrated into personal electronic devices, particularly in smartphone and laptop platforms. Its application to industrial, infrastructure, vehicle, medical and environmental applications is expected to enable equally significant new possibilities in the sustainable development of global life quality. The implementation of the so-called Internet-Of-Things (IoT) is however more challenging to implement, mainly because the corresponding microdevices need to operate autonomously, without user attention, especially for battery replacement or recharging. While control and machine-to-machine interaction technologies have addressed a range of autonomous functionalities [1], the requirement for portable power has remained a key limiting factor for the development of IoT infrastructure and services [2].

The provision of power by harvesting energy from the local environment or by wireless power transfer has been investigated extensively in the last couple of decades. This research has delivered various new methods for energy transduction as well as a range of autonomous power supplies with power densities in the 1 mW/cm^2 order of magnitude under realistic environmental conditions [2, 3], enough for enabling, for example, a wide range of key medical microsystem applications [4]. In parallel, advanced power extraction methods have been developed for energy harvesting transducers [5], including capacitor switching [6, 7], reactance cancellation [8], maximum power-point tracking (MPPT) [9, 10], load-inclusive MPPT [11], synchronous switching [12-14], and pre-biasing [15, 16]. Nevertheless, industrial adoption of energy harvesting power supplies is very slow due to:

- The reliance on very specific environmental conditions, such as vibration at a defined frequency, local temperature difference or direct sunlight. Hence, existing solutions and products are suitable only for a narrow range of use cases.
- Intermittent power availability. Autonomous power supplies must include energy buffers and operate regularly in cold-starting mode, to ensure functionality after long and irregular inactive periods.

To address these limitations, various cold-starting power management techniques have been developed. They include passive rectification [17, 18] as well as very low input voltage boosters with bootstrapping functionality, employing transformer components [19-21], relays [22], switched inductors [23-27] and capacitors [28, 29] as well as combinations with ring oscillators [30-32]. These approaches focus on achieving passive low-voltage startup, at the expense of low efficiency during the cold-starting period. Therefore, a fast transition to active mode power management is desirable. For systems requiring energy buffering, the benefit of using two storage elements has been recognized. A first layer of low capacity is used to allow fast charging to a voltage adequate for active mode rectification and boosting, and the second is a high capacity element that serves as the main energy buffer. However, commercially available power management systems are designed for using electrochemical batteries as the second layer energy buffer, which are not desirable due to reliability, unpredictable status after long inactivity periods and limited

Manuscript received April 22, 2024; revised October 29, 2024; accepted December 19, 2024.

The authors are with the Department of Electrical and Electronic Engineering, Imperial College London, SW7 2AZ, U.K. (e-mail: m.kiziroglou@imperial.ac.uk)
M. E. Kiziroglou is also with the Department of Industrial Engineering and Management, International Hellenic University, 57400, Greece.

number of recharging cycles. In addition, the charge transfer between the first and the second storage layer during cold-starting is typically not optimized for efficiency. This may be because the charging of the second storage element from depletion to an active-mode voltage (e.g. 2 V) is still regarded as a less critical transition mode.

In industrial applications of energy harvesting power supplies, the intermittent and unpredictable environmental conditions result in regular operation in cold-starting mode [33, 34]. Therefore, the efficiency of buffer storage charging is a critical performance parameter. When environmental power becomes available, an effective power management system should provide:

a. Fast passive-to-active mode transition
b. Fast output power activation
c. Efficient transfer of excess power to the storage buffer, even if the latter is depleted.

While these requirements have been occasionally recognized and dual storage solutions have been proposed, a battery-less system with these features suitable for systematic cold-starting operation has not yet been proposed. In this paper we propose a dual storage power management system with a simple switching architecture that addresses these requirements. The proposed circuit design follows a different approach than the current power management state-of-art [17-32], as it focuses on achieving fast cold-starting without an efficiency compromise.

The concept and a theoretical analysis are described in Sections II and III. The design and fabrication of a printed circuit board (PCB) implementation is presented in Section IV. The system is characterized using a power line inductive energy harvester presented in [34] and summarized in Section V. Experimental performance results are presented and discussed in Section VI. Typically, energy autonomous microsystems such as wireless sensors present an intermittent load to the power source, as they switch among complete shut-down, active, sleep and deep-sleep operation modes. Therefore, in Section VI, the performance is evaluated separately for two testing scenarios. In Section VI.A the cold-starting operation without load is tested, allowing a simple and undisturbed evaluation of output-enable speed and passive and active charging efficiency. In Section VI.B the cold-starting operation with a connected load is tested, evaluating the capability of supporting loads in selectable duty-cycle operation and the capability of splitting the incoming energy between the load and the buffer storage. Conclusions are summarized in Section VII.

II. Circuit Concept

In a cold-starting energy harvesting power management system a capacitor is typically charged initially by a low-threshold switched mode converter, to provide a quick transition to active mode power management. If the same capacitor, or the same circuit node, is also used for energy buffering, a compromise must be made between cold-starting speed and power autonomy. This case is illustrated in Fig. 1a. A small storage capacitor C_{S1}, e.g. in the sub-mF range can allow fast startup and efficient operation. However, such a case barely provides any energy buffering and an intermittent input power availability would result in frequent sudden black-outs at the output, without much time for providing the load with advance notice. On the other hand, a large C_{S1}, e.g. ≥ 100 mF would allow a more reliable output, but cold-starting operation would be significantly prolonged, leading to functional delays and inefficient power management.

To address this functional challenge, some commercial micro-power management integrated circuits support separate storage elements for fast cold-starting and bulk storage. An indicative architecture is illustrated in Fig. 1b. The power management electronics are powered by the first storage layer C_{S1}. Once an adequate voltage on this primary storage is reached, a secondary storage element, C_{S2} is connected in parallel to the first through a metal-oxide-semiconductor field-effect transistor (MOSFET) switch. These implementations are typically intended for batteries, which maintain a significant voltage even when they are nearly depleted. However, in practical energy harvesting installations, supercapacitor storage is often preferable, for its long-term reliability features. In addition, the charging of C_{S2} from zero or low (below 2 V) voltage is expected to occur regularly due to scheduled or incidental inactivity periods, for example when a vehicle monitored by energy autonomous wireless sensors is parked or inactive for maintenance works for more than a few days.

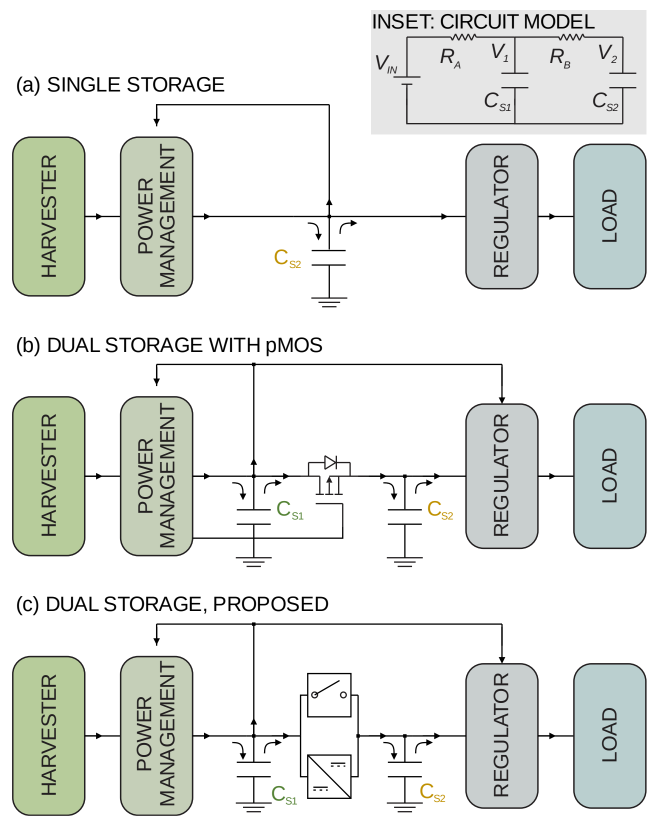

Fig. 1. Conceptual description of (a) a single storage system, (b) dual storage with a pMOS switch between the two storage elements and (c) a dual storage system with a dedicated DC/DC converter and switching system. A circuit model is shown in the top-right inset.

Hence, the efficiency of charge transfer between C_{S1} and C_{S2} becomes significant, and the single MOSFET direct bridging solutions of Fig. 1b, are not suitable due to body-diode leakage during the off-state as well as to the low efficiency of direct capacitor-to-capacitor charge transfer during the on-state.

The power management concept proposed in this paper is illustrated in Fig. 1c. An additional power management circuit between the two storage layers is introduced, dedicated to efficient and dynamically configurable power splitting between the main storage element (C_{S2}) and the output load. This circuit comprises a buck converter and a dedicated discrete low-leakage switching component, as well as comparator circuitry for suitable operation mode activation control. This control can be based on the C_{S1} and C_{S2} voltage levels, or handled by digital control signals from power management or the micro-controller-unit (MCU) of the load system. During cold-starting C_{S2} is fully disconnected allowing fast charging of C_{S1} to a voltage adequate for running all electronic units in active mode, typically at 2 V. Then, power supply to the load is activated and any excess energy is supplied to C_{S2} via a buck converter. During this operation mode, control signals can balance the power flow to the storage and to the load as needed. When the voltage on C_{S2} reaches that of C_{S1} the two supercapacitors are short-circuited through the switch, to further reduce charge transfer losses. In this operation mode any excess power not used by the load is stored in the combined C_{S1} and C_{S2} capacitance, up to a maximum voltage of 5 V. If the input power is reduced or stopped, the output power is supplied by storage until the storage voltage falls below 2 V. Then, the output power is disabled and the switch opens, disconnecting the two storage elements. In this way, if the system remains inactive for a long period and the stored energy is fully depleted or reduced below 2 V, the system can again provide fast cold-starting using C_{S1} when input power becomes available again.

III. Theoretical Analysis

In the three power management systems of Fig. 1, the charging of C_{S1} and C_{S2} follow an overall exponential trend with an effective time constant. Therefore, to evaluate timing performance, the circuits between the energy harvesting source V_{IN} and C_{S1}, and between C_{S1} and C_{S2} can be abstracted by effective resistances R_A and R_B respectively. The corresponding circuit is shown in the top-right inset of Fig. 1. The differential equations for the C_{S1} voltage V_1 is calculated to be:

$$R_A R_B C_{S1} C_{S2} \ddot{V_1} + (R_A(C_{S1}+C_{S2}) + R_B C_{S2})\dot{V_1} + V_1 = V_{IN} \quad (1)$$

The corresponding equation for the C_{S2} voltage V_2 is the same. The solution for initial conditions $V_1(0) = V_2(0) = 0$ is:

$$V_1 = V_{IN}\left(1 - \frac{\tau_1 - R_B C_{S2}}{\tau_1 - \tau_2} e^{-t/\tau_1} + \frac{\tau_2 - R_B C_{S2}}{\tau_1 - \tau_2} e^{-t/\tau_2}\right) \quad (2)$$

$$V_2 = V_{IN}\left(1 - \frac{\tau_1}{\tau_1 - \tau_2} e^{-t/\tau_1} + \frac{\tau_2}{\tau_1 - \tau_2} e^{-t/\tau_2}\right) \quad (3)$$

, where:

$$\tau_{1,2} = \frac{R_A(C_{S1}+C_{S2}) + R_B C_{S2} \pm \sqrt{\Delta}}{2} \quad (4)$$

$$\Delta = R_A^2 C_{S1}^2 + 2R_A C_{S1} C_{S2}(R_A - R_B) + C_{S2}^2 (R_A + R_B)^2 \quad (5)$$

In this analysis, the single storage system of Fig. 1a corresponds to $C_{S1} = 0$ and $R_B = 0$, in which case $\sqrt{\Delta}=R_A C_{S2}$ and, using equations (4) and (2), the cold-starting duration is found to be determined by the time constant $R_A C_{S2}$.

In the case of the dual storage system with a pMOS switch connection between C_{S1} and C_{S2}, (**Fig. 1**b), the circuit behaviour can be analysed by assuming an ideal pMOS bulk diode behaviour. For $V_1 - V_2 < 0.7\,V$, the diode doesn't conduct, corresponding to a very large R_B in the model of **Fig. 1**, inset. For $R_B \gg R_A$, taking the limit of equations (4) and (2) as $R_B \to +\infty$ gives an exponential increase of V_1 with time constant $R_A C_{S1}$. A $V_1 - V_2 = 0.7\,V$ is reached at time $t_{ON} = R_A C_{S1} \ln(\mathrm{V_{IN}}/(\mathrm{V_{IN}} - 0.7\ \mathrm{V})$, after which the bulk diode conducts, maintaining a constant $V_1 - V_2$. In this case the differential equation of the system is:

$$(C_{S1} + C_{S2}) R_A \dot{V_1} + V_1 = V_{IN} \quad (6)$$

and V_1 and V_2 both increase exponentially with a time constant $\tau_3 = (C_{S1} + C_{S2}) R_A$. Overall:

$$V_1 = \begin{cases} V_{IN}(1 - e^{-t/R_A C_{S1}}) & for\ t < t_{ON} \\ V_{IN} - (V_{IN} - 0.7\ V) e^{-(t - t_{ON})/\tau_3}) & for\ t \geq t_{ON} \end{cases} \quad (7)$$

The overall cold starting duration of this system is dominated by the much larger time constant τ_3.

Finally, in the proposed architecture, a high effective R_B is achieved as both the MOSFET switch and buck converter are off throughout cold-starting. Again, the large R_B results in an exponential V_1 increase with time constant $R_A C_{S1}$. This analysis, shows that the proposed architecture, for a typical system with $C_{S2} \gg C_{S1}$ offers faster cold starting by a factor of C_{S2}/C_{S1}.

The power transfer efficiency is determined by the power management block in Fig. 1, which is the same in all three architectures, with the exception of additional bulk diode conduction loss in the pMOS case during cold-starting. On the other hand, the power overhead of the additional buck converter, comparator and MOSFET of the proposed system can be reduced by selecting state-of-art low power components.

In the proposed architecture, the benefit of using a MOSFET to bridge C_{S1} and C_{S2} when $V_1 = V_2$ instead of continuing using the buck converter can be theoretically evaluated by comparing the corresponding power transfer losses. When the MOSFET is on, at a current I between C_{S1} and C_{S2}, the incoming power is $P_{IN} = IV_2$ and the MOSFET loss is $P_{LOSS} = I^2 R_{ON}$, where R_{ON} is the MOSFET on-state resistance. The loss factor is $\eta = IR_{ON}/V_2$. This is typically more than an order of magnitude less than the nominal efficiency of state-of-art buck converters. Indicatively, the TI TPS62737 buck converter and the TI TS5A4624 MOSFET employed in the implementation of this work have a 6% loss and a $R_{ON} = 1.1\,\Omega$ respectively. The corresponding MOSFET loss at the current range of up to 10 mA expected for energy harvesting applications and at $V_2 > 2\,V$ is less than 0.55%, over 10 times lower than the buck converter.

IV. CIRCUIT DESIGN AND FABRICATION

An implementation of the proposed concept is presented in Fig. 2. It includes a reactance cancellation capacitor C_S and a passive voltage doubler rectification circuit with low threshold and leakage Schottky diodes (Comchip RB521G-30HF [35]) described in [36]. The rectified voltage is supplied to the first supercapacitor, C_{S1}, through an inductor switching boost converter circuit, including MPPT and bootstrap functionality. This is implemented using a Texas Instruments (TI) BQ25570 microchip [23]. A regulated 1.8 V output is provided through another switched inductor, also handled by the same chip. An additional buck converter and a MOSFET switch are connected between C_{S1} and the second supercapacitor, C_{S2}, using the TI TPS62737 [37] and TS5A4624 [38] chips respectively. The switch is controlled by a comparator such that it is normally open. It closes when the voltage on C_{S2} is over 2 V, $V_2 > 2\,V$. This comparator is implemented using an Analog Devices LTC1540 chip [39] . The storage buck converter is enabled when the C_{S1} voltage surpasses 2.5 V: $V_1 > 2.5\,V$ while charging, and $V_2 < 2\,V$. It is disabled when V_1 drops below 2 V while discharging, or when V_2 reaches 2 V. This logic is implemented by setting the $V_{BAT,OK}$ flag signal of the BQ25570 to the appropriate hysteresis thresholds, using the corresponding configuration resistors as shown in the Appendix, and feeding it to a NAND gate along with the inverted output logic of the LTC1540 comparator. This is implemented using the TI SN74AUP2G00 dual NAND chip [40], with one of the NAND gates connected to serve as an inverter of the LTC1540 output. Threshold hysteresis is provided by the BQ25570 chip and hence the LTC1540 hysteresis is not utilized. Interference between the storage and output buck converter switching is prevented by the large C_{S1} supercapacitor value which suppresses transients. In addition, both converters switch off when V_1 drops below 2 V.

A range of circuit variations was designed and fabricated in PCB form, with multiple connector pins that allowed testing for different external supercapacitor (C_{S1} and C_{S2}) values and under different conditions. The value of C_{S1} must be small enough to ensure fast start-up and large enough to allow a digital microcontroller load to boot, set a suitable duty-cycle and sleep.

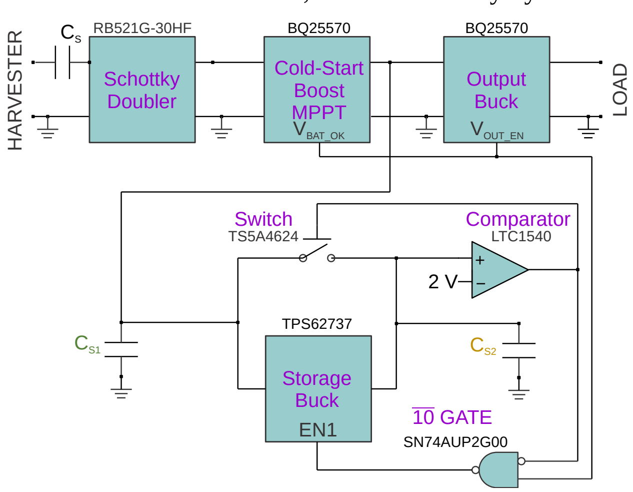

Fig. 2. Block diagram of a dual storage power management system.

The value of C_{S2} should be large enough to provide the required energy autonomy and support any desirable power burst functionalities of the load. In practice, their specific values can be chosen according to the use case functional specifications. A circuit diagram of the implementation including an input, an output and a configuration port is presented in the Appendix, along with a list of component values used. A photograph of the PCB including external supercapacitors is shown in Fig. 3.

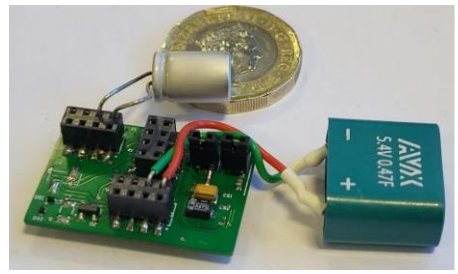

Fig. 3. Image of the circuit fabricated as a printed circuit board.

V. POWER LINE HARVESTING USE CASE

To evaluate the performance of the proposed architecture in a real use case, the circuit was tested using an inductive power line energy harvester as power source, developed for energy autonomous aircraft sensors. This is a use case of key industrial importance due to the high reliability, weight, autonomy and wireless installation requirements of avionic sensor systems, and because of the high frequency range (300 Hz to 800 Hz) of aircraft power lines, which offers high inductive coupling [34].

The energy harvester comprises a closed-loop flux funnelling soft magnetic core structure with a 200-turn Cu coil, integrated into a modular package that allows clamping-on without cutting or interrupting the power line. This energy harvester was introduced and studied in [8, 41] and it is shown, in connection with the power management system of this paper in Fig. 4. To measure the performance of the power management system for various power inputs, a custom evaluation setup was developed, emulating an aircraft power line with currents up to 40 A root-mean-square (RMS) at frequencies between 50 Hz and 1 kHz. This evaluation setup is shown in Fig. 5. It consists of a signal generator driving an audio amplifier. The amplifier output is connected to the primary winding of a custom 20:1 turns ratio current transformer. The secondary winding is formed by a large (>2.5 mm^2) cross-section area cable loop.

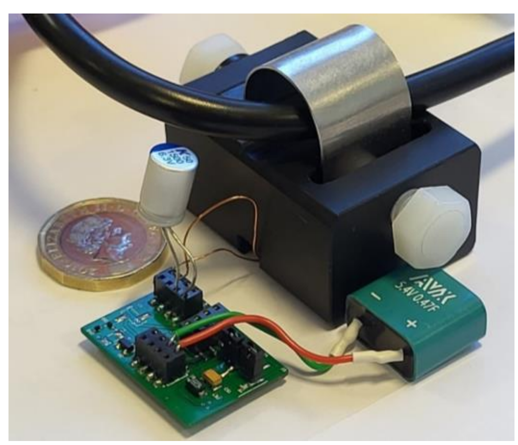

Fig. 4. Photograph of the energy autonomous power supply.

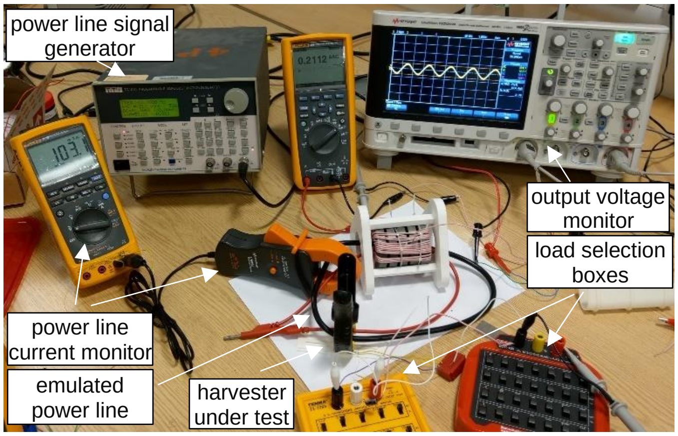

Fig. 5. Photograph of the experimental setup used for testing the energy autonomous power supply on an emulated power line.

This single loop emulates a current-carrying aircraft power line. The RMS current value is monitored by a Keysight U1583 inductive current clamp connected to a Fluke 787B multimeter.The AC input, storage voltages (V_1 and V_2) and the regulated output voltage (V_{OUT}) of the power management system were monitored using a 4-channel Keysight DSOX 2024A oscilloscope. Measurements under various power line currents, system configurations and output load conditions were taken to evaluate the benefit of the proposed concept, as discussed in the next section. In [8, 41] the energy harvester was characterized without a power management system, in open-circuit conditions as well as by direct connection of the harvester output to various impedances, including reactance compensation. These measurements indicate the maximum possible power output of the energy harvester, and hence they can be used as reference for power management efficiency calculations. Indicatively, the measured power output for different ohmic loads, with and without impedance cancellation from a 10 A RMS power line at various frequencies is presented in Fig. 6 [8].

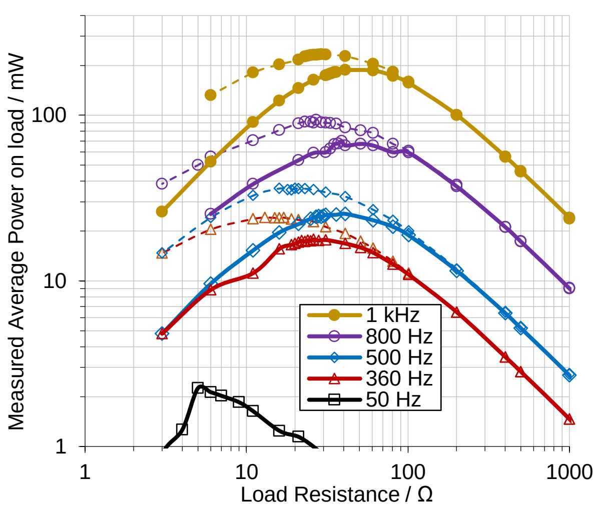

Fig. 6. Energy harvester output power from a 10 A RMS power line measured on resistive loads without power management circuitry, from [8].

VI. Experimental Evaluation

For the experiments of this section the power supply was installed on the evaluation setup described in Section V and as shown in Fig. 5. The cold-starting performance was evaluated by measuring its response to turning on the power line current while all capacitors were fully discharged. In a first operating scenario, the performance without an output load was studied, in order to measure the output-enable speed and charging efficiency. In a second operating scenario, the cold-starting with a connected load was tested. These scenarios are discussed in Sections VI.A and VI.B respectively.

A. Cold Starting without Load

For a comparative performance benefit evaluation of the proposed dual-storage power management architecture, the response to power line current of various amplitudes and frequencies, switched on at time $t = 0\ s$ was measured for three different configurations. In all three, the storage and reactance cancellation capacitors were C_{S1} = 1.5 mF, C_{S2} = 0.47 F and C_S = 10 μF, and no load was connected to the regulated output V_{OUT}. These values were selected for a startup time in the 1 s range and a 2.5 J (4 V – 5 V) energy buffer. In the first configuration, the two storage supercapacitors were connected together, and the dual storage power management circuitry (storage buck converter, comparator, gates and bridging switch) was disabled, emulating the conventional single-storage system of Fig. 1a. In the second, a pMOS connection between the supercapacitors was employed as shown in Fig. 1b. This case corresponds to commercially available solutions for dual-storage, which are however usually designed and intended for battery storage [23]. In the third, the full dual-storage system corresponding toFig. 1c as shown in Fig. 2 was used.

Indicative supercapactor and output voltages for a 10 A RMS, 500 Hz power line current, as measured by the oscilloscope channels in a single start-up sequence are shown in Fig. 7 top, middle and bottom respectively. These results illustrate a much faster output voltage enabling, obtained by the proposed system. In comparison to the single storage system this is due to the much smaller startup capacitor (C_{S1}) used. In comparison to the pMOS switch system, which uses the same startup capacitor, this is due to the pMOS body leakage to the large C_{S2} throughout the cold-starting phase, as shown Fig. 7 middle. The start-up detail of Fig. 7 bottom is shown in Fig. 8. While the measurements of Fig. 7 were taken without a power load for experimental clarity, the output power can in practice be utilized as soon as it is enabled.

The measurements are also compared with the theoretical timing model of Section III in Fig. 7 and Fig. 8. The single-storage measurements of Fig. 7 top were fitted by an exponential curve with an $R_A C_{S2}$ time constant, using a $V_{IN} = 5.5V$, the nominal value of $C_{S2} = 0.47\,F$ used and R_A as a fitting parameter. Applying a fitting step of 0.1 kΩ, an effective R_A value of 0.5 kΩ was determined. For the pMOS dual storage system measurements of Fig. 7 middle, the same time constant is expected to occur after $V_1 > 0.7\,V$, and the corresponding exponential curves for V_1 and V_2 are plotted without any further fitting. The measurements follow the expected trends at a slower rate, which is attributed to additional bulk leakage losses beyond the ideal diode model. For the proposed system, the fast-cold starting performance shown in Fig. 8 is expected to have a $R_A C_{S1}$ time constant, with the nominal value of $C_{S_1} = 1.5\,mF$ used, and the same effective R_A of the other two systems. The corresponding theoretical exponential increase, without further fitting, is plotted in Fig. 8 and it is in agreement with the measured performance. Beyond the fast cold-starting phase, the C_{S2} is connected through the buck converter, and subsequently through the MOSFET. The corresponding V_2 increase of Fig. 7 bottom shows a slower increase in comparison with the theoretical $R_A C_{S1}$ time constant. The difference is attributed to losses of the additional circuitry used.

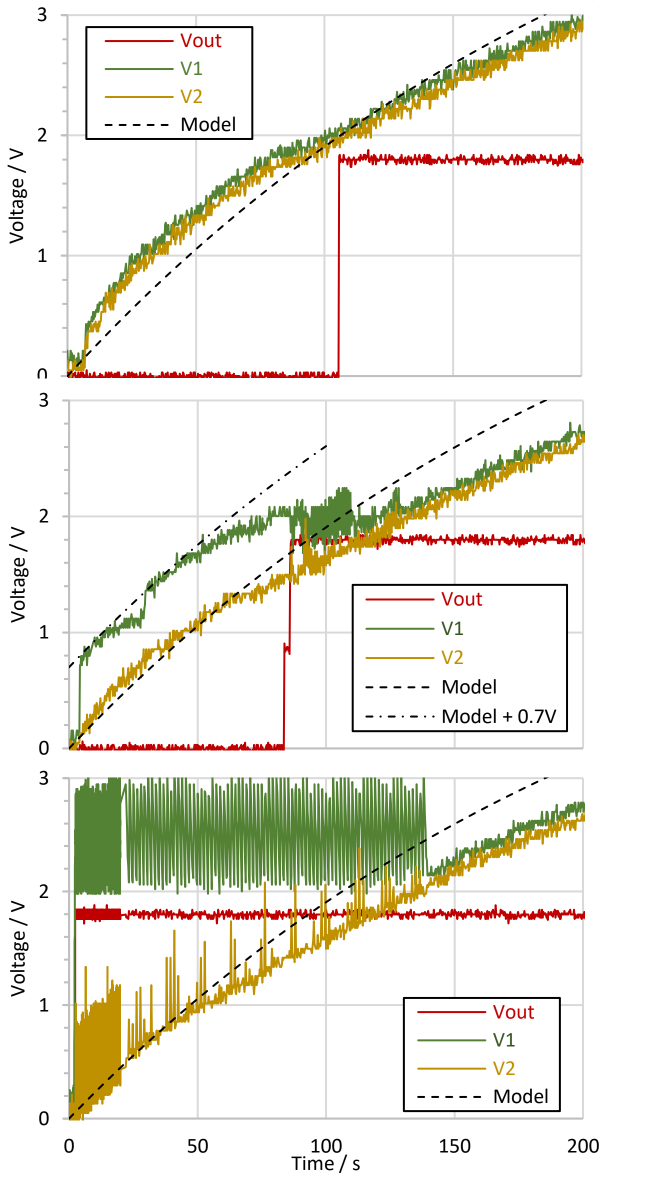

Fig. 7. Measured cold-starting storage and output voltages for: (top) a single storage system implemented by bridging C_{S1} and C_{S2}, (middle) a double storage system with a pMOS switch and (bottom) the proposed dual storage system. A 10 A RMS, 500 Hz power line current was used, with $C_{S1} = 1.5$ mF, $C_{S2} = 0.47$ F and $C_S = 10$ μF and without output load. Corresponding exponential charging curves calculated using the theoretical timing model of Section III are also plotted for comparison.

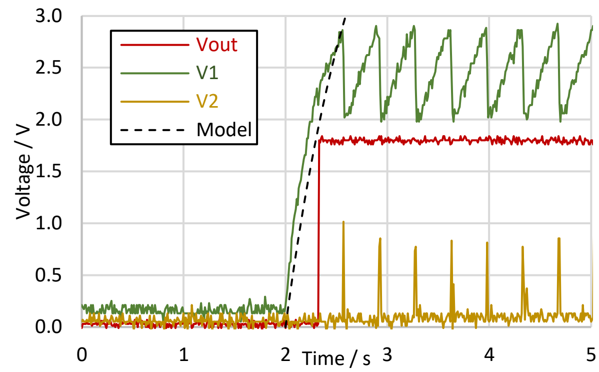

Fig. 8. Start-up detail of the measurements presented in Fig. 7 bottom.

In the start-up detail of Fig. 8, the power line is enabled at $t = 2\,s$, and an output activation at around $t = 2.33\,s$ is obtained. The measurements also illustrate the fast charging of C_{S1} and the subsequent pumping of charge to C_{S2} through the impedance L_B shown in Fig. A1, handled by the storage buck converter. From such measurements, the output enable and full-charge ($V_{S2} = 5\,V$) times for the three different architectures can be extracted.

Corresponding results for four different representative power line current cases, namely 10 A RMS at 360 Hz, 8 A RMS at 500 Hz, 10 A RMS at 500 Hz, and 28 A RMS at 800 Hz are plotted in a logarithmic scale in Fig. 9 top. They demonstrate a two-orders of magnitude faster output activation for the proposed architecture. The time to full-charge ($V_2 = 5\,V$) is plotted in Fig. 9 middle, showing similar performance for all three cases. This indicates a small overall power management efficiency difference among the different approaches. The consistently slower charging of the pMOS switch implementation (blue) compared to the single storage system (yellow) is due to leakage and conduction losses on the monolithic pMOS switch. To evaluate this further, the overall cold-starting input-to-storage efficiency from flat to full-charge was calculated by dividing the total stored energy by the full-charge time to find the average storage power and dividing by the maximum corresponding possible power of the energy harvesting transducer as measured in Fig. 6 without reactance cancellation. The results are presented in Fig. 9 bottom.

The transducer-to-storage cold-starting efficiency is in the 10% range for the 10 A RMS, 360 Hz power line current for all approaches and increases to over 35% for larger and higher frequency power line currents. The losses are partly due to the reactance mismatch at the harvester / rectifier interface, where a fixed $C_S = 10\,\mu F$ was used. This corresponds to 44 Ω, 32 Ω, and 20 Ω at 360 Hz, 500 Hz and 800 Hz respectively, compared to harvester output resistance which is around 20 Ω, as measured in Fig. 6. This is in line with the efficiency increase with frequency illustrated in Fig. 9 bottom. Further losses originate from the voltage doubler rectification diodes, but also from the rectified input-to-supercapacitor charge transfer which can't be operated at the maximum power point, for example by setting the C_{S2} voltage to near half the transducer open-circuit voltage as shown in [42].

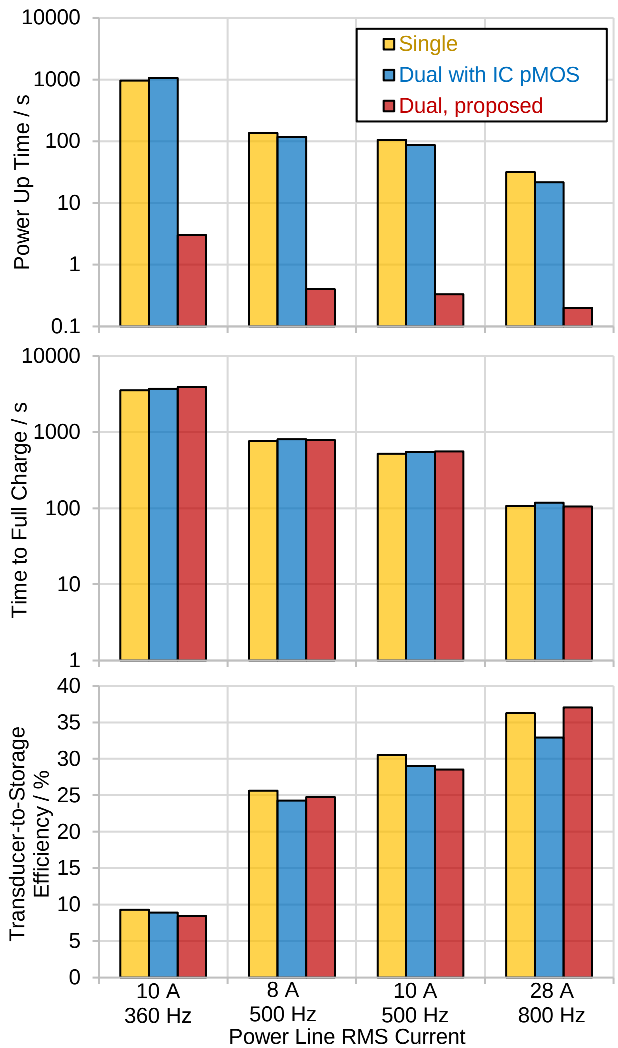

Fig. 9. Power-up time (top), time to full-charge (middle) and efficiency (bottom) of single, standard dual and the proposed architecture for $C_1 = 1.5$ mF, $C_2 = 0.47$ F, $C_S = 10$ µF, and no output load, for different power line currents.

This is because the objective of the system during this cold-starting operation phase is to store the maximum possible energy. Higher efficiency can be obtained by adjusting the output power load consumption for an overall maximum power transfer, but the practicality of such an operation mode will depend on functional and duty cycling requirements of the load.

The overall input-to-storage efficiency is similar among the three architectures, demonstrating a small consumption overhead introduced by the additional components required for the proposed approach. The IC pMOS dual storage case includes some additional losses due to the body leakage charge transfer during its passive cold-starting stage (0 s to 83 s in Fig. 7 middle). This is apparent in the 28 A RMS, 800 Hz case where the IC pMOS architecture shows a lower efficiency.

In conclusion, a two orders of magnitude faster output power activation is experimentally demonstrated for the proposed dual storage architecture compared to the industrial state of art. This is a key advantage for supercapacitor-based energy autonomous systems because they are expected to operate typically at low main storage voltage (indicatively 0 V to 2 V) charging mode.

B. Cold Starting with Load

To evaluate the ability of the proposed circuit to cold-start while a load is connected to the output, a series of experiments for different load, supercapacitor storage and power line current values was performed. For these experiments, the implementation used (Fig. 3) was configured to enable both the regulated 1.8 V output and secondary storage buck converters when $V_{S1} > 2.5\,V$. In this way the system is providing output power to the load as soon as possible, and transfers any excessive energy to C_{S2}. If the power demand from both buck converters is higher than the incoming power, a duty-cycle operation occurs, balancing the power flow. When C_{S2} is charged to 2 V, the two supercapacitors are bridged and the duty cycled output provision continues at a higher rate. If the load power drops below the input power, the voltage on the supercapacitors increases storing the excess energy as in single storage implementations.

To observe and evaluate this behavior experimentally at adequate time resolution, 1.5 mF supercapacitors were selected for both C_{S1} and C_{S2} and a 100 Ω resistor was used as load, corresponding to 32.4 mW at 1.8 V. The power line current was enabled with the load on, and the system response was monitored until the capacitor bridging functionality is observed. After a few more seconds, the load was disconnected, allowing the observation of storage charging to the 5 V maximum. Finally, the power line input was disabled and the load was re-connected to evaluate the storage-to-output power provision functionality. An indicative such measurement for a 10 A RMS, 500 Hz power line current is shown in Fig. 10.

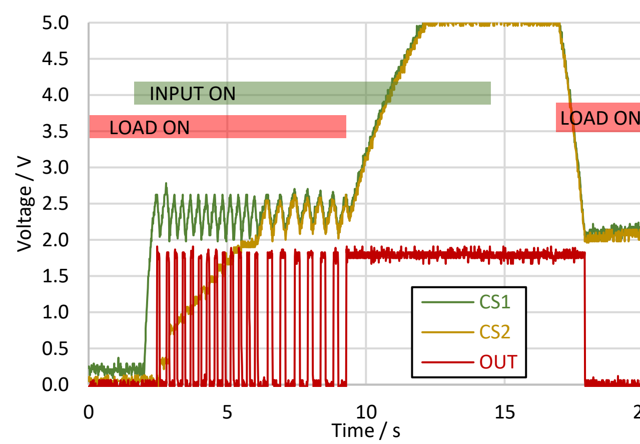

Fig. 10. Measured voltages on C_{S1} and C_{S2} and output during cold-starting, with a 100 Ω (32.4 mW) load connected to the regulated output, for a 10 A RMS, 500 Hz power line current. The input is turned on with the load connected. After C_{S1} is fully charged and charge starts being pumped into C_{S2} by the buck converter, the load is disconnected to allow a fast full charge. Then, the input is disconnected and the load is reconnected demonstrating energy autonomy and output voltage cut-off operation.

As expected, V_{S1} is raised rapidly (0.42 s after power line activation) to 2.5 V. Then, the output, and the storage buck converter are enabled. The operation at this stage is shown in higher time resolution in Fig. 11. An output duty cycle of 33% is observed, with 100 ms on-state duration. In practical use cases, the storage buffer may be much larger, providing longer operating windows, for example 30 s at $C_{S2} = 0.47\,F$. In addition, the output enable threshold voltage can be pre-configured at PCB design level, or could be dynamically adjustable by the microcontroller depending on system functionality requirements.

The V_{S2} reaches 2 V after around 4 s from power line activation. The supercapacitors are bridged and operate as a single-storage system, providing an output duty cycle of 35% with 170 ms on-state duration. Subsequently the load is manually disconnected allowing the system to fully charge, within 2.65 s from 2.5 V to 5 V corresponding to an average power income of 10.6 mW. Finally, the power line is disabled and the output load is connected, resulting in the 5 V to 2 V discharge between $t = 17\,s$ and $t = 18\,s$ in Fig. 10.

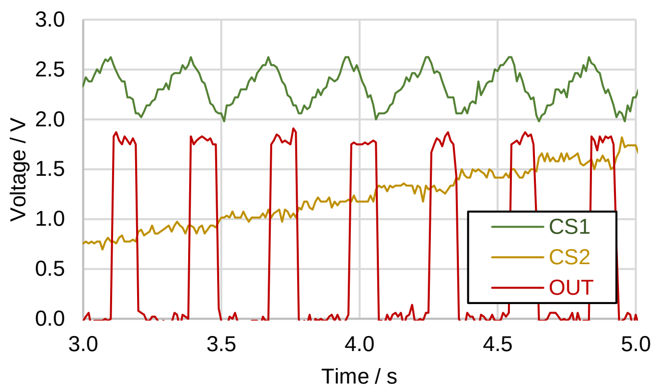

Fig. 11. Detail of the measurements presented in Fig. 10 illustrating the output voltage duty cycling and partial energy transfer into C_{S2}.

Using the method followed for the measurements of Fig. 10, the functionality of the dual storage systems using the IC pMOS switch (Fig. 1b) and the method proposed in this paper (Fig. 1c) was experimentally verified and analyzed for various power line currents. The resulting output duty cycle and corresponding average power, during the bridged C_{S1} - C_{S2} operation phase, are shown in Fig. 12. The results are similar for the two systems, in-line with the efficiency similarity observed in the experiments of Fig. 9. However, the fast cold-starting and power output provision supported by the proposed architecture is not available in the conventional IC pMOS implementation. The output power duty cycle provided by the proposed system while C_{S2} is being charged is shown as a dashed line in Fig. 12. The lower duty cycle reflects that some of the power is rooted to C_{S2}. This power splitting can be dynamically configured, through the storage buck converter enable pin, to fit operational priorities handled by the microcontroller of the load system.

The storage-to-output efficiency, extracted from the input-off, load-on discharge curves was similar for all power line currents and system configurations and over 95%. This similarity is expected as the same buck converter is handling the storage-to-load discharge in all three systems.

It is noted that in the specific implementation presented here, the use of a simple buck converter between the second storage layer C_{S2} and the output, restricts the minimum V_{S2} to around 0.2 V higher than the regulated voltage output (1.8 V in this implementation). Hence, the C_{S2} energy for V_{S2} up to 2 V remains unused and does not contribute to the energy autonomy of the system. In the present implementation this limitation is small and may be preferable, as the threshold for maintaining the more efficient bridged C_{S1} - C_{S2} operation is also set at 2 V. However, in other cases, for example when a higher voltage output is desirable, the resulting V_{S2} restriction, and hence the unusable stored energy may be significant. In such cases, the employment of a buck/boost converter, instead of the simple buck converter can extend the energy autonomy provided for a given C_{S2} component value.

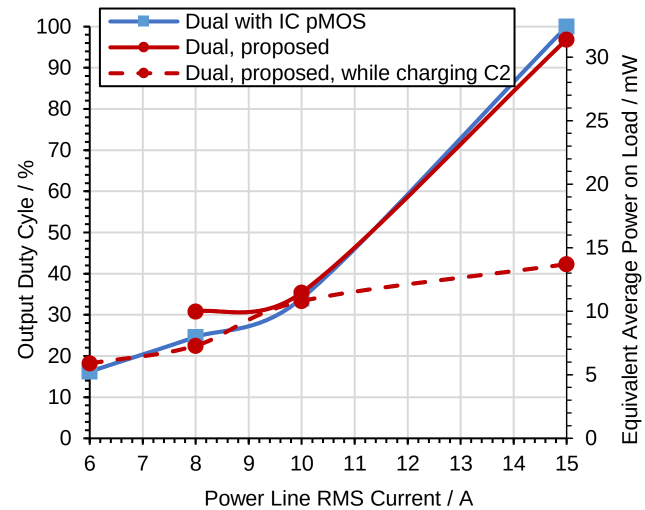

Fig. 12. Output duty cycle and corresponding average power delivery on load during cold-starting for different power line currents at 500 Hz. All curves correspond to both vertical axes. The equivalent average power was calculated as the product of nominal load power and the duty cycle percentage.

VII. Conclusions

A dual-storage handling circuit was introduced in this paper, that allows efficient and configurable energy transfer from a small, fast cold-starting first stage, to a large supercapacitor energy buffering second stage. This is achieved by a combination of an isolating external MOSFET switch component and a buck converter employed to allow efficient and controllable charge transfer. In this way, the start-up speed increase reaches the capacitance ratio of the two storage elements, which is the theoretical benefit limit of the dual-storage cold starting system concept. The main functional modes of the system were demonstrated and analyzed by adopting a measurement method that captures a full cycle of modes including cold-starting, output power duty cycling, charge transfer between storage elements, full charging and discharging at zero input power, all in one oscilloscope measurement sweep (Fig. 10).

The experimental results demonstrate a faster cold-starting response by over two orders of magnitude in comparison with the conventional single storage and double storage architectures. It was also shown that the additional circuitry does not add significant power consumption overhead, as the overall efficiency was measured to be within a ±2% margin in comparison to the state-of-art implementations. In terms of circuit implementation cost, complexity and reliability, the additional comparator, buck converter, and two logic gates represent a moderate overhead in comparison to the conventional architecture which typically involves several buck/boost converters, comparators and logic gates. This overhead can in practice be minimized by integration into a single power management chip, employing an isolated bulk layer for the MOSFET switch.

The experimental validation of the proposed concept was performed using an inductive power line energy harvester developed for aircraft sensors, for power line currents corresponding to real aircraft conditions [8, 34]. Indicatively, a regulated power of 11 mW and 32 mW was demonstrated for a 10 A and 15 A RMS, 500 Hz power line current respectively, using the harvester introduced in [8]. The introduced architecture allows independent selection of a fast cold-starting first storage layer and a second, large supercapacitor storage layer for energy buffering, without compromising the overall system efficiency. It provides selectable and configurable functionalities that could potentially be digitally controlled by the load microcontroller for dynamic power routing prioritization. Overall, the demonstrated system addresses the key requirement of efficient cold-starting for energy autonomous microsystems.

Appendix

The full circuit schematic implemented for the evaluation of the architecture proposed in this paper is shown in Figure A1. The corresponding component values are listed in Table I.

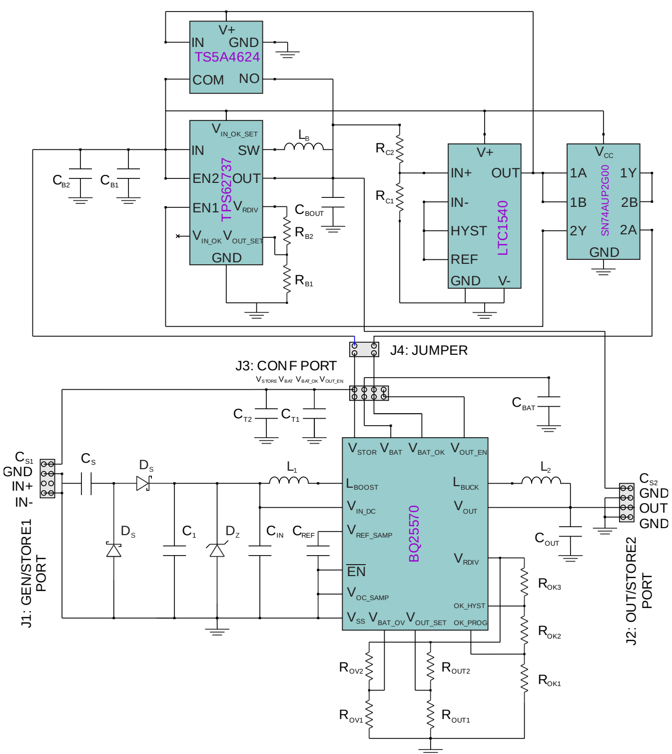

Fig. A1. Full circuit of the implemented dual storage power management system. C_{S1} and C_{S2} are connected to pin 1 of J1 and J2 respectively.

TABLE I
COMPONENT VALUES/MODELS USED IN THE CIRCUIT OF FIG. A.

Part	Value / Model	Part	Value / Model
C_1	10 μF	R_{B1}	3.16 MΩ
C_{B1}	0.1 μF	R_{B2}	9.76 MΩ
C_{B2}, C_{BOUT}	22 μF	R_{C1}	7.15 MΩ
C_{BAT}	100 μF	R_{C2}	5.90 MΩ
C_{IN}, C_{T2}	4.7 μF	R_{OK1}	6.34 MΩ
C_{OUT}	22 μF	R_{OK2}	4.64 MΩ
C_{REF}, C_{T1}	10 nF	R_{OK3}	2.10 MΩ
C_S	10 μF, external	R_{OUT1}	8.66 MΩ
C_{S1}	1.5 mF, external	R_{OUT2}	4.22 MΩ
C_{S2}	0.47 F, external	R_{OV1}	4.75 MΩ
D_S	Schottky, 0.2 V@2mA	R_{OV2}	8.25 MΩ
D_Z	Zenner, 5.1 V	U_1	TI TS5A4624
J_1, J_2, J_5	2.54 mm, 2×4 female	U_2	TI SN74AUP2G00
J_3, J_4	2.54 mm, 2×1 male	U_3	AD LTC1540
L_1	22 μH	U_4	TI TPS62737
L_2, L_B	10 μH	U_5	TI BQ25570

Note: Resistors: 1%, Capacitors: Low ESR, >5.1 V, Inductors: > 110 mA

For C_{S1} a Kemet 1.5 mF, 6.3 V supercapacitor with 14 mΩ equivalent series resistance (ESR) and -55 ºC to 105 ºC operating temperature was used. For C_{S2} an AVX 0.47 F, 5.4 V supercapacitor with 1 Ω ESR and -40 ºC to 85 ºC operating temperature was used. For the experiments in Section VI.B, the Kemet model was used for both C_{S1} and C_{S2}.

References

[1] Al-Fuqaha *et al*, "Internet of Things: A Survey on Enabling Technologies, Protocols, and Applications," *IEEE Communications Surveys and Tutorials*, vol. 17, no. 4, pp. 2347-2376, 2015.

[2] T. Becker *et al.*, *Energy Harvesting for a Green Internet of Things* (PSMA White Paper). Power Supply Manufacturers Association, 2021.

[3] M. E. Kiziroglou and E. M. Yeatman, "Energy Harvesters and Power Management," in *More-than-Moore Devices and Integration for Semiconductors*, Cham: Springer Int. Pub., 2023, pp. 1-45.

[4] Roy *et al*, "Powering Solutions for Biomedical Sensors and Implants Inside the Human Body: A Comprehensive Review on Energy Harvesting Units, Energy Storage, and Wireless Power Transfer Techniques," *IEEE Trans. Power Electr.*, 37 (10), 12237, 2022.

[5] D. Newell and M. Duffy, "Review of Power Conversion and Energy Management for Low-Power, Low-Voltage Energy Harvesting Powered Wireless Sensors," *IEEE Trans. Power Electr.*, 34 (10), 9794, 2019.

[6] N. Qi, K. Dai, X. Wang, and Z. You, "Adaptive Capacitor Charging Circuit With Simplified Configuration for Efficient Piezoelectric Energy Harvesting," *IEEE Trans. Power Electr.*, 37 (9), 10267, 2022.

[7] Z. Liu *et al.*, "A Novel Method for Magnetic Energy Harvesting Based on Capacitive Energy Storage and Core Saturation Modulation," *IEEE Trans. Ind. Electr*. vol. 70, no. 3, pp. 2586-2595, 2023.

[8] Wright *et al*, "Inductive Power Line Harvester With Flux Guidance for Self-Powered Sensors," *IEEE Sens. Jour.* 23 (18), 20474, 2023.

[9] M. Ferracini *et al.*, "Design of a Wireless Sensor Node for Overhead High Voltage Transmission Power Lines," *IEEE Transactions on Power Delivery*, vol. 38, no. 2, pp. 1472-1482, 2023.

[10] N. Shah, P. Lajevardi, K. Wojciechowski, C. Lang, and B. Murmann, "An Energy Harvester Using Image Sensor Pixels With Cold Start and Over 96% MPPT Efficiency," *IEEE Sol.-St. Circ. Lett.*, 2 (9), 207, 2019.

[11] E. Lee, V. C. K. Chekuri, and S. Mukhopadhyay, "A PFM Boost Harvester With System-Level Self-Tuned Maximum Power Point Tracking," *IEEE Trans. Power Electr*, 37 (8), 9428, 2022.

[12] Xie *et al*, "A Self-Powered Synchronous Switch Energy Extraction Circuit for Electromagnetic Energy Harvesting Enhancement," *IEEE IEEE Trans. Power Electr*, 38 (8), 9972, 2023.

[13] M. Lallart, "High Gain, Load-Tolerant Self-Powered Series–Parallel Synchronized Switching Technique for Piezoelectric Energy Harvesting," *IEEE Trans. Power Electr*, 37 (7), 8649, 2022.

[14] L. Gao, L. Teng, H. Wang, Y. Liu, M. Fu, and J. Liang, "A Self-Sensing Synchronous Switch Circuit for Bidirectional Piezoelectric Energy Conversion," *IEEE Trans. Ind. Electr.*, pp. 1-10, 2023.
[15] J. Dicken *et al* , "Power-Extraction Circuits for Piezoelectric Energy Harvesters in Miniature and Low-Power Applications," *IEEE Trans. Power Electr* 27 (11), 4514, 2012.
[16] M. Pathak and R. Kumar, "Synchronous Pre-biasing of Triboelectric Nanogenerator for Enhanced Energy Extraction," *IEEE Transactions on Power Electronics,* vol. 37, no. 10, pp. 11552-11566, 2022.
[17] T. T. Toh, S. W. Wright, M. E. Kiziroglou, P. D. Mitcheson, and E. M. Yeatman, "A dual polarity, cold-starting interface circuit for heat storage energy harvesters," *Sens. Act. A-Phys.*, 211, 38, 2014.
[18] Z. J. Chew and M. L. Zhu, "Adaptive Self-Configurable Rectifier for Extended Operating Range of Piezoelectric Energy Harvesting," *IEEE IEEE Trans. Ind. Electr*, 67 (4), 3267, 2020.
[19] Analog, "LTC3109, Auto-Polarity, Ultralow Voltage Step-Up Converter and Power Manager, Datasheet. ," 2018, Available: www.analog.com/en/products/ltc3109.html.
[20] P. Spies, "Micro Energy Power Management ASIC 2 (ME-PMA2)," Fraunhofer IIS, 2021
[21] S. Patra, K. P. Muthe, and A. Singh, "Low Voltage and Low Power Self-Startup Oscillator-Driven Boost Converter for Thermoelectric Generator Operating at Low Temperature," *IEEE Trans. Ind. Electr*, pp. 1-11, 2024.
[22] K. Kozalakis and S. Siskos, "Electromechanical switching voltage converters with application to cold start for thermoelectric generators," *Engineering Research Express,* vol. 4, no. 3, Sep 2022, Art. no. 03lt01.
[23] "Texas Instruments BQ25570 nano power boost charger and buck converter for energy harvester powered applications," 2019, Available: www.ti.com/product/BQ25570.
[24] M. R. Pollak, M. E. Kiziroglou, S. W. Wright, P. Spies, and Ieee, "Cold-Starting Switched-Inductor Bipolar Power Management for Dynamic Thermoelectric Harvesting," PowerMEMS 2021, pp. 116-119, 2021.
[25] S. Bose, T. Anand, M. L. Johnston, "A 3.5 mV Input, 82% Peak Efficiency Boost Converter with Loss-Optimized MPPT and 50 mV Integrated Cold-Start for Thermoelectric Energy Harvesting," in *40th Annual IEEE Custom Integr. Cir. Conf. (CICC),* Austin, TX, 2019.
[26] Z. H. Long, P. Y. Li, J. Chen, H. R. Chung, and Z. B. Yang, "Self-Powered Single-Inductor Rectifier-Less SSHI Array Interface With the MPPT Technique for Piezoelectric Energy Harvesting," *IEEE Trans. Ind. Electr,* vol. 69, no. 10, pp. 10172-10181, Oct 2022.
[27] S. Fang *et al*., "An Efficient Piezoelectric Energy Harvesting Circuit With Series-SSHI Rectifier and FNOV-MPPT Control Technique," *IEEE Trans. Ind. Electr,* vol. 68, no. 8, pp. 7146-7155, 2021.
[28] L. F. M. Dutra, P. C. C. de Aguirre, A. G. Girardi, and L. Compassi-Severo, "A Fast Cold-Start Integrated System for Ultra-Low Voltage SC Energy-Harvesting Circuits," in *14th IEEE Latin American Symposium on Circuits and Systems (LASCAS)*, Quito, Ecuador, pp. 40-43, 2023.
[29] D. K. W. Li, *et al*, "Integrated Switched-Capacitor-Based Cold-Start Circuit for DC-DC Energy Harvesters with Wide Input/Output Voltage Range and Low Inductance in 40-nm CMOS," in *33nd Annual IEEE App. Power Electr. Conf. Exp. (APEC)*, San Antonio, TX, 2104, 2018.
[30] X. H. Yu *et al*., "An Integrated Circuit of A Cold Start-up Circuit for A Thermoelectric Energy Harvesting System," in *56th IEEE Int. Symp. Circ. Syst. (ISCAS),* Monterey, CA, 2023, 2023.
[31] M. Coustans, F. Krummenacher, and M. Kayal, "A Fully Integrated 60 mV Cold-Start Circuit for Single Coil DC-DC Boost Converter for Thermoelectric Energy Harvesting," *IEEE Transactions on Circuits and Systems Ii-Express Briefs,* vol. 66, no. 10, pp. 1668-1672, Oct 2019.
[32] H. W. Yu, M. Y. Chen, C. D. Wu, K. T. Tang, G. X. Wang, and Ieee, "A Batteryless and Single-Inductor DC-DC Boost Converter for Thermoelectric Energy Harvesting Application with 190mV Cold-Start Voltage," in *IEEE Int. Symp. Circ. Syst. (ISCAS),* Florence, Italy, 2018.
[33] L. v. Allmen *et al.*, "Aircraft Strain WSN powered by Heat Storage Harvesting," *IEEE Trans. Ind. Electr,* 64 (9), 7284, 2017.
[34] M. Blagojevic *et al*., "Autonomous Electrical Current Monitoring System for Aircraft," *IEEE Transactions on Aerospace and Electronic Systems,* vol. 59, no. 3, pp. 3345-3358, 2023.
[35] Comchip, "Comchip RB521G-30HF Schottky Diode Datasheet," 2023, Available: https://www.comchiptech.com/product.php?id=3567.
[36] M. E. Kiziroglou, S. W. Wright, and E. M. Yeatman, "Power Supply Based on Inductive Harvesting From Structural Currents," *IEEE Internet of Things Journal,* vol. 9, no. 10, pp. 7166-7177, 2022.
[37] "Texas Instruments TPS62737 Buck Converter Datasheet," Available: https://www.ti.com/product/TPS62737, 2024
[38] "Texas Instruments TS5A4624 Analogue Switch Datasheet," Available: https://www.ti.com/product/TS5A4624, 2024
[39] Analog Devices LTC1540 Nanopower Comparator with Reference, Available: https://www.analog.com/en/products/ltc1540.html, 2024
[40] *Texas Instruments SN74AUP2G00 low power NAND gates*. Available: https://www.ti.com/product/SN74AUP2G00, 2024
[41] S. W. Wright, M. E. Kiziroglou, and E. M. Yeatman, "Clamped Closed-Loop Flux Guides for Power Line Inductive Harvesting," PowerMEMS 2022, pp. 82-85.
[42] R. Jiang, G. Lepipas, S. K. E. Yang, and A. S. Holmes, "Batteryless Bluetooth Anemometer employing 2 cm Axial Turbine as both Power Source and Wind Speed Transducer," *IEEE Sens. Journal,* pp. 1-1, 2024.

MICHAIL E. KIZIROGLOU (M'04-SM'14) obtained his diploma in electrical and computer engineering from Aristotle University of Thessaloniki, Greece, in 2000 his master in microelectronics and nanoelectronics from Democritus University of Thrace, Greece, in 2003 and his Ph.D. in microelectronics from the University of Southampton in 2007. He is a Research Fellow in the Department of Electrical and Electronic Engineering, Imperial College London and Assistant Professor at the International Hellenic University. His research interests include energy harvesting devices, energy autonomous sensors and microsystems.

STEVEN W WRIGHT has worked in the Electrical Engineering Department at Imperial College London researching the fabrication methods and properties of compound semiconductor thin film transistors, their use in addressing flat panel displays and integrated drive circuits for displays. More recent work has been on the development of materials and methods for producing high resistance, low TCR materials for high value resistors in integrated circuits, and also high dielectric constant materials for ICs. His current research interests include energy harvesting systems and their associated electronic interfaces.

ERIC M. YEATMAN (M'01, SM'05, F'13) obtained his B.Sc from Dalhousie University, Canada, in 1983, and his Ph.D. from Imperial College London in 1989. He is currently a professor of micro-engineering and head of the electrical and electronic engineering department at Imperial College London. His research interests include motion and thermal energy harvesting for wireless devices, pervasive sensing, and sensor networks. He is a Fellow and Silver Medalist of the Royal Academy of Engineering, and was a cofounder of Microsaic Systems, which develops and markets miniature mass spectrometers for portable chemical analysis.

ANDREW S. HOLMES (M'03) received the BA degree in natural sciences from Cambridge University, U.K., in 1987, and the Ph.D. degree in electrical engineering from Imperial College London, U.K., in 1992. He is currently Professor of Micro-Electro-Mechanical Systems (MEMS) with the Department of Electrical and Electronic Engineering, Imperial College London. His research interests include micropower generation by energy harvesting, power conditioning for energy harvesters, tribology of microscale mechanical systems, novel microassembly techniques, and laser processing for MEMS and electronics manufacture.