Active Power Losses Distribution Methods for the Modular Multilevel Converter

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***Abstract*—Modular Converters such as the MMC have become the new standard in VSC-HVDC applications. Their modularity has brought many industrial advantages but also increased the complexity of their operation. This paper looks at how a range of techniques may alter the balance of power losses between the IGBT modules. These techniques are based on circulating currents at the (i) fundamental frequency and (ii) second harmonic and (iii) DC voltage offset on the converter voltage waveform. Finally, conclusions on the effectiveness and potential drawbacks of these techniques are discussed.**

Keywords— Modular Multilevel Converter, Power Losses, Circulating Current, IGBT Modules

I. INTRODUCTION

HVDC power converters must excel in all their characteristics, from power efficiency to reliability. The latest generation of Voltage Source Converter (VSC) topologies are all based on the Modular Multilevel Converter (MMC) [1] which established a new standard [2],[3] for converters and is illustrated in Figure 1. The MMC consists of stacks of Sub-Modules (SM) which switch their internal charged capacitors in or out of the current conduction path, with the objective to construct the voltage waveform required to construct this same current. The relatively small voltage magnitude of the SM (albeit in the 1 - 10 kV range), compared to the full AC or DC bus voltage magnitudes, results in numerous advantages such as smooth current waveforms, modularity of the valve hall arrangement and low switching frequency of the individual semiconductor devices. Several other topologies have since then been suggested in order to further improve on the standard half-bridge MMC topology, such as reduced stack volume [4],[5] or DC fault blocking capability [6],[7]. A notable aspect common to all these new converter topologies consists in the fact that most of these gains on the electrical side have been made available mainly thanks to the extensive (yet complex) controllability [8]-[12] of the stacks of SM.

Once commissioned, an HVDC power converter station must ensure the highest degree of operational reliability under any circumstances or, in other terms, the ability to operate with the minimum number of outages between two maintenance sessions. The MMC has been commissioned for the first time only a few years ago, meaning that little data has been published with regards to their reliability level, making present and future investments challenging. Of particular interest, the notion of State of Health (SoH) for the IGBT modules can be a critical aspect of the converter station which needs to monitored and maintain at the highest technically possible level over long periods of operating time windows. Numerous stress factors could influence the SoH of a semiconductor device such as the number and timing of switching instances, average and peak conducting current. Most importantly, the temperature regime of the semiconductor die is a significant factor of the SoH and is directly influenced by the power losses of the semiconductor device.

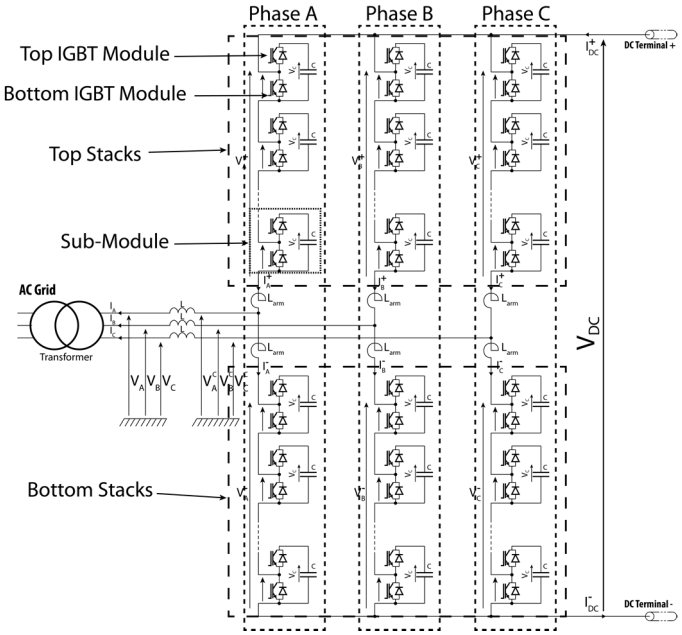

Figure 1 – Topology of the MMC

This paper explores some control techniques which aim at altering the balance of power losses between the semiconductor devices within an MMC. Starting by the methodology used in this study and the definition of the basic operating state of the MMC under normal operating conditions in Section II, the three developed techniques are detailed in Section III, followed by the simulation results in Section IV and conclusive remarks on the observed pros and cons of this approach.

II. METHODOLOGY

A. Elements of the MMC

The MMC, as illustrated in Figure 1, consists of 3 phase units of 2 stacks each, themselves comprising of hundreds of SM. The focus of this study lies on the IGBT modules within the SM of the stacks. Each half-bridge SM consists of a Top and Bottom IGBT modules which conduct current alternately. When the Top IGBT module is conducting, the SM is generating a positive voltage, and vice and versa. However, the power loss distribution between the SM within the same stack is beyond the scope of this work. Therefore, the model developed in this study describes the Top and Bottom IGBT modules in what can be considered an average SM in each stack of the MMC.

B. Equations of Electrical Quantities

The electrical quantities in the studied MMC can be written as follow. The AC grid voltage consists of a sinusoid waveform and a DC offset:

$$V_A(t) = \hat{V}_{AC}\sin(\omega t) + V_{offset}$$
$$V_B(t) = \hat{V}_{AC}\sin\left(\omega t - \frac{2\pi}{3}\right) + V_{offset}$$
$$V_A(t) = \hat{V}_{AC}\sin\left(\omega t + \frac{2\pi}{3}\right) + V_{offset}$$

The AC grid currents are only sinusoidal:

$$I_A(t) = \hat{I}_{AC}\sin(\omega t)$$
$$I_B(t) = I_{AC}\sin\left(\omega t - \frac{2\pi}{3}\right)$$
$$I_A(t) = \hat{I}_{AC}\sin\left(\omega t + \frac{2\pi}{3}\right)$$

The stack voltages result from their DC and AC connection points into the sum of half the DC bus voltage and the AC grid voltage:

$$V_A^+(t) = \frac{V_{DC}}{2} - V_A(t)$$
$$V_A^-(t) = \frac{V_{DC}}{2} + V_A(t)$$
$$V_B^+(t) = \frac{V_{DC}}{2} - V_B(t)$$
$$V_B^-(t) = \frac{V_{DC}}{2} + V_B(t)$$
$$V_C^+(t) = \frac{V_{DC}}{2} - V_C(t)$$
$$V_C^-(t) = \frac{V_{DC}}{2} + V_C(t)$$

The stack currents however consist of 3 elements. The AC current is split between the top and bottom stacks with a ratio k_{AC}. The DC current splits equally between the 3 phase units. A circulating current is also taken into account as being one of the main means for the developed balancing techniques. These facts result in the following equations:

$$I_A^+(t) = k_{AC}\, I_A(t) + \frac{I_{DC}}{3} + I_A^{Circ}(t)$$
$$I_A^-(t) = (k_{AC} - 1)\, I_A(t) + \frac{I_{DC}}{3} + I_A^{Circ}(t)$$
$$I_B^+(t) = k_{AC}\, I_B(t) + \frac{I_{DC}}{3} + I_B^{Circ}(t)$$
$$I_B^-(t) = (k_{AC} - 1)\, I_B(t) + \frac{I_{DC}}{3} + I_B^{Circ}(t)$$
$$I_C^+(t) = k_{AC}\, I_C(t) + \frac{I_{DC}}{3} + I_C^{Circ}(t)$$
$$I_C^-(t) = (k_{AC} - 1)\, I_C(t) + \frac{I_{DC}}{3} + I_C^{Circ}(t)$$

C. Power Losses Calculation

Thanks to the low switching frequency of its semiconductor devices, the MMC sees its power losses dominated by the conduction losses which this study will focus on. The IGBT modules have been modelled as a fixed voltage source and a series resistance, leading to the power loss equation:

$$P_{Conduction} = V_0\,|I_{IGBT}| + R_0\, I_{IGBT}^2$$

The semiconductor device selected for use in this study is the FZ1200R33HE3 IGBT module with integrated anti-parallel diode from Infineon. Its main characteristics are listed in the table below. Given its electrical characteristics, the SM nominal voltage has been set at 1.8 kV.

Table 1 – Electrical Characteristics of FZ1200R33HE3 IGBT

Blocking Voltage	*3,300 V*
Nominal Sub-Module Voltage	*1,800 V*
Nominal Current Rating	*1,200 A*
Peak turn Off Current	*2,400 A*
Initial Voltage (V_0)	*1.38 V*
On-state Resistance (R_0)	*1.38 mΩ*

D. Original State

In its original operating state, the MMC is controlled to have (i) a modulation index of 90% between the DC terminal voltage and the AC peak voltage, (ii) no circulating current and (iii) no DC offset on the AC grid voltage. Figure 2 illustrates the electrical waveforms of this MMC, normalized for graphical convenience using the DC bus voltage and current as the unit system. These waveforms form the benchmark case.

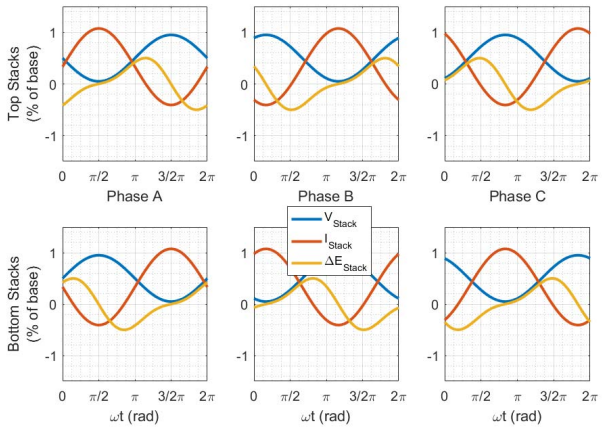

Figure 2 – Original stack voltage, current and energy deviation waveforms with all the balancing technique deactivated

The conduction losses in this scenario have been assessed and listed in Table 2. The main observations out of the results listed in Table 2 consist in the facts that (i) the symmetry of the topology between the phases and top-to-bottom stacks is reflected in the power loss distribution between the SM and (ii) the Bottom IGBTs generate most of the power losses, especially compared to the Top IGBTs. This fact has already been reported in the literature [11] and can be explained that the arm current magnitude is on average higher when the stacks are generated a low voltage magnitude, resulting in a higher proportion of Bottom IGBT modules to conduction, leading to more power losses.

Table 2 –Power loss distribution within an MMC sorted by location of the IGBT modules within the SM of the different stacks

		Phase A	Phase B	Phase C
Top Stack	**Top IGBT**	*354 W*	*354 W*	*354 W*
	Bottom IGBT	*1,101 W*	*1,101 W*	*1,101 W*
Bottom Stack	**Top IGBT**	*354 W*	*354 W*	*354 W*
	Bottom IGBT	*1,101 W*	*1,101 W*	*1,101 W*

III. Power Loss Distribution Techniques

This paper explores some control techniques which aim at altering the balance of power losses between the semiconductor devices within an MMC. These techniques are based on either the addition of controlled circulating currents or DC offset on the stack voltage reference, and are intended to be usable continuously if required. For this purpose, these developed techniques must preserve the good operation of the converter during normal operation. First, this means that the energy level inside the stacks of the MMC must remain constant over time. The energy deviation waveforms within the course of the fundamental cycle can be altered but no drift should be allowed to happen. Second, the AC and DC current waveforms should not be affected by the operation inside the MMC station in retain the filter-less feature of the MMC. Therefore, the techniques based on the addition of currents through the arms must be restricted to the use of circulating currents which sum to zero before reaching the DC terminals or AC connection points.

The studied techniques fall into 3 different categories: (i) circulating current at the fundamental frequency, (ii) circulating currents at the second harmonic and (iii) DC offset on the AC voltage waveform.

A. Circulating Current at the fundamental frequency

Using circulating current at the fundamental frequency as the advantage of being perfectly synchronized with the live modulation index of the stack, but also presents the direct risk of altering the energy equilibrium of the same stacks. The only solution consists in only using circulating current in quadrature (i.e. 90° angle) to the phase angle reference which will thus not exchange any active power with the stacks. This type of circulating current can thus be expressed using this equation:

$$I_{\{A,B,C\}}^{Circ}(t) = I_Q(t) = k_Q\,\hat{I}_{AC}\sin\left(\omega t + \frac{\pi}{2}\right)$$

B. Circulating Current at the second harmonic

Moving away from the fundamental frequency frees the stacks from the power and energy interactions with the involved circulating currents. In order to mitigate, the effect of higher switching losses on the system, only waveforms at the second harmonic frequency will be consider. In this scenario, these circulating currents can take any amplitude ($k_2\,\hat{I}_{AC}$) and phase angle (ϕ_2) values without the danger of unsettling the average energy level of the stacks. The only constraints here consist in ensuring that all the circulating currents from the 3 phase units in the MMC cancel together (i.e. sum to zero) in order to leave a clean DC current waveforms at the DC terminal points.

This leaves with the following equation for the second harmonic circulating current in each phase unit:

$$I_{\{A,B,C\}}^{Circ}(t) = I_2(t) = k_2\,\hat{I}_{AC}\sin(2\omega t + \phi_2)$$

C. DC voltage offset on the converter waveform

With the two techniques detailed above, the circulating current methods are mostly exhausted. The final technique consists thus in modifying the voltage waveforms inside the MMC. However, most of these values are fixed by the network, apart from the DC offset on the converter AC voltage waveform. By adding a DC offset, the upper stacks will generate less voltage thus utilizing more its bottom IGBT modules. To ensure a correct energy equilibrium inside the MMC, the spit of the AC current between the top and bottom stacks must also be altered. This further modifies the distribution of the power losses between the different elements of the MMC.

The DC offset is expressed using the following equation:

$$V_{offset} = k_V\frac{V_{DC}}{2}$$

In order to rebalance the energy between the top and bottom stacks, the split ratio of the AC current has to be adapted to the amount of added DC offset. Following these power equations:

$$P_A^+ = V_A^+(t)\,I_A^+(t)$$
$$= \left(\frac{V_{DC}}{2} - \hat{V}_{AC}\sin(\omega t) - k_V\frac{V_{DC}}{2}\right)\left(k_{AC}\,\hat{I}_{AC}\sin(\omega t) + \frac{I_{DC}}{3}\right)$$

Taking the average over a fundamental cycle to zero power:

$$< P_A^+ > = 0$$
$$\frac{1-k_V}{2}V_{DC}\frac{I_{DC}}{3} - \frac{k_{AC}\,\hat{V}_{AC}\,\hat{I}_{AC}}{2} = 0$$

Using the conversion power equality between AC and DC:

$$V_{DC}\,I_{DC} = \frac{3\,\hat{V}_{AC}\,\hat{I}_{AC}}{2}$$

This leads to:

$$k_{AC} = \frac{1-k_V}{2}$$

IV. Results for the DC offset technique

All the techniques described in Section III have been simulated and their influence on the MMC both in terms of waveforms and power loss distribution have been examined.

A. Circulating Current at the Fundamental Frequency

Since these injected circulating currents are at the same frequency as the AC current, there is no major changes to the electrical waveforms of the stacks. As shown in Figure 3, the changes are limited to a slight phase shift of the current waveform and a small increase of the total energy deviation.

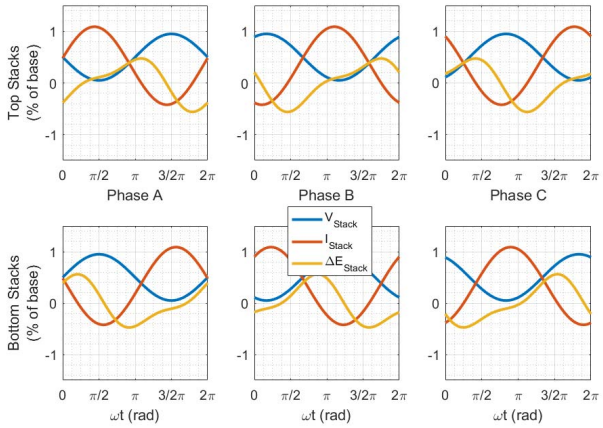

Figure 3 – Stack voltage, current and energy deviation waveforms with circulating currents at the fundamental frequency

These observations are confirmed by the values reported in Figure 4. The stack energy deviation went up by 3% but, most importantly, all the IGBT modules (both Top and Bottom) are affected in the same way. This last point can be explained by the lack of freedom in the design of this technique where all the currents have the same phase angle. This means that this technique has little to no use for power loss balancing purposes.

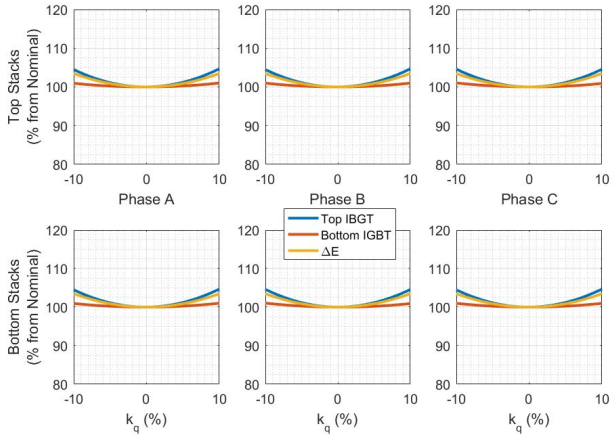

Figure 4 – – IGBT module power loss and energy deviation magnitude using circulating currents at the fundamental frequency

B. Second Harmonic Circulating Currents

This technique has the benefit of offering an additional degree of freedom compared to the previous one, as both the magnitude and phase angle of the circulating currents through the three phase unit can be changed. The only constraint consists in the sum to zero of all these currents at the DC terminals. In this scenario, these circulating currents have a clear impact on the waveforms of the stacks, as shown in Figure 5. The second harmonic distorts the stack currents as well as altering the energy deviation waveform.

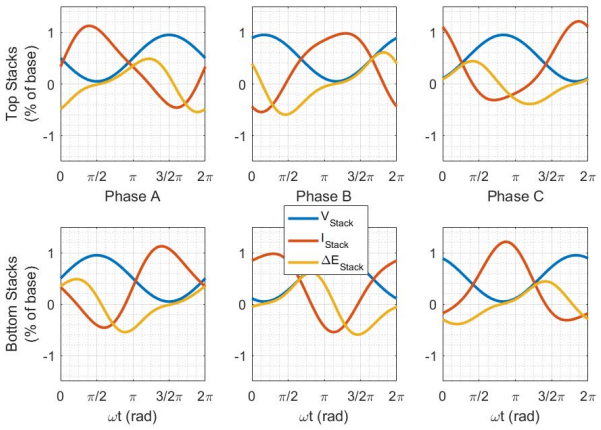

Figure 5 – Stack voltage, current and energy deviation waveforms with second harmonic circulating currents (relative phase angles A: 0°, B: -120°, C: 120°)

Figure 6 confirms also that this technique has a more pronounced impact on the IGBT modules. The Bottom IGBT modules are the least impacted as their power losses have only changed by around 5%, while the Top IGBT modules are changed by close to 25%. Besides a clear pattern of phase to phase power loss exchange emerges. The two stacks of a same phase unit (e.g. bottom stack in top stack in phase B) exhibit the same power loss change but also in total opposition to the adjacent phase unit (e.g. bottom stack in top stack in phase C). This indicate that the power loss saved in one phase can be transferred to another phase.

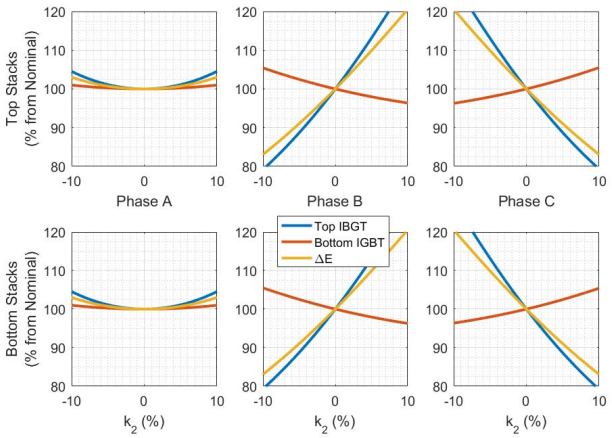

Figure 6 – IGBT module power loss and energy deviation magnitude using second harmonic circulating currents (relative phase angles A: 0°, B: -120°, C: 120°)

A closer look at the influence of the phase angle on the power loss fluctuation is reported in Figure 7. This confirms the difference in influence of this technique between the Top and Bottom IGBT modules but also highlights a sinusoidal shape of these same influences. This fact combined with the summing to zero of all 3 circulating currents confirms the phase-to-phase power loss transfer observed in Figure 6.

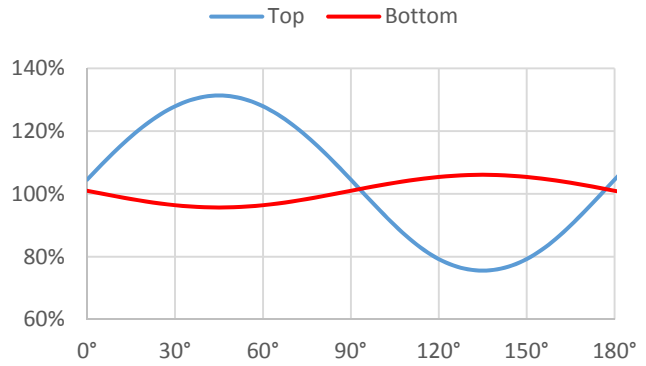

Figure 7 – Effects on the IGBT module relative power loss when varying the phase angle of the second harmonic circulating currents set at 10% relative magnitude

C. DC Voltage Offset

Figure 8 shows how the electrical quantities inside the MMC are modified when a DC offset is introduced. Figure 9 indicates the relationship between the relative power losses distribution and the magnitude of the DC offset techniques. The main observations can be summarized as: (i) the split of the AC current has to be modified in order to keep the top and bottom stacks at the energy equilibrium, (ii) the energy deviation profile is increased for the stacks at the opposite of the DC offset technique, (iii) the bottom IGBT modules in the bottom stacks generate significantly more power losses to the benefit of the bottom IGBT modules in the top stacks and (iv) the magnitude of the effects is proportional with the magnitude of the DC offset applied to the MMC.

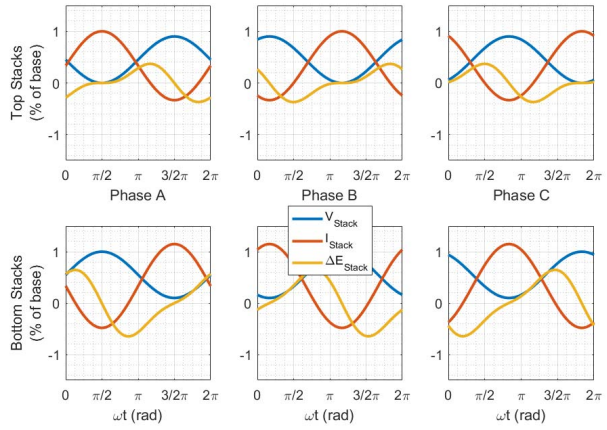

Figure 8 – Stack voltage, current and energy deviation waveforms with the DC voltage offset technique active

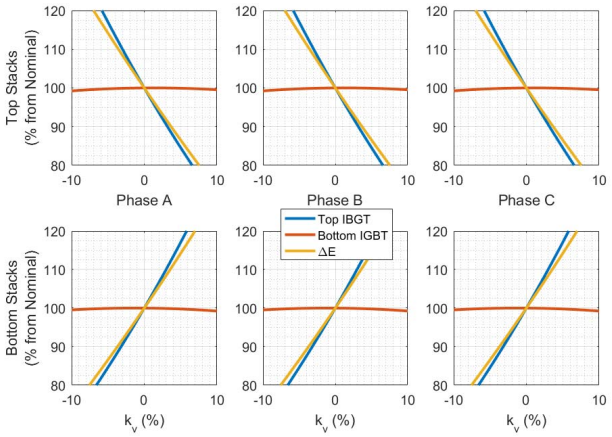

Figure 9 – IGBT module power loss and energy deviation magnitude using the DC voltage offset technique

D. Overall Power Losses

The results above only present the variation of power losses for each IGBT modules relative to their original state, as described in Section II.D. However, the use of these power loss balancing technique has undoubtedly an impact on the overall power loss of the all converter station. By combining of the power loss figures, the total power loss of the MMC for each of these techniques is shown in Figure 10.

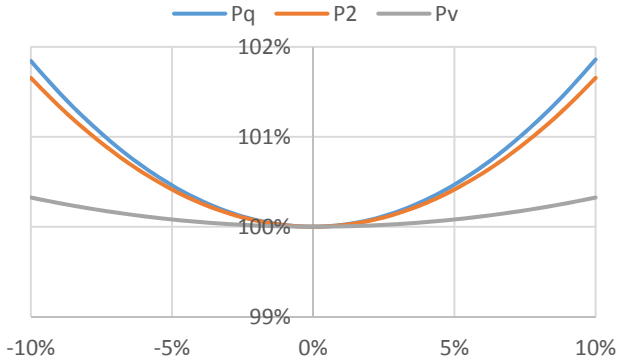

Figure 10 – Relative effects of the presented balancing techniques on the total power loss of the converter station

As this results show, the two circulating current-based techniques have the largest impact on the power losses, by increasing them by almost 2%, whereas the DC voltage offset technique has a much more moderate impact at around +0.3%.

V. Conclusion

Three techniques intended to change the balance of power losses between the IGBT devices in an MMC have been studied. All these techniques are designed to be used during normal steady state operation and thus not to interfere with the average energy level in the stacks.

The first technique relies on adding a circulating current at the fundamental frequency but in quadrature with the stack voltage waveform. However, only negligible amounts of power

loss differences were obtained and with no difference between the IGBT devices, thus concluding on the inability of this technique to be used in the context of temperature balancing.

The second technique is also based on circulating current but, this time, at the second harmonic. The use of a frequency different than the fundamental frees this current from the angle constraint as it does not affect the average energy level of the stacks of SM. The results show a good (±30%) inter-phase balancing of the power losses for the top IGBT modules in the SM but only a moderate (±5%) effect on the bottom IGBT modules.

The third and last technique adds a DC offset on the AC voltage waveform of the converter. This forces the top and bottom stacks to change their respective modulation index. The results show a good (±35%) top-to-bottom balancing of the power losses for the top IGBT modules in the SM but only a negligible (±1%) effect on the bottom IGBT modules.

All in all, only two of the three studied techniques have yielded positive results but almost exclusively for the top IGBT modules. Only little impact has been observed on the bottom IGBT modules even though they are the ones generating most of the losses, thus more likely to require support. Furthermore, all these techniques have a negative impact on the overall power losses of the converter (+2%) and an even more pronounced negative impact (+5-25%) on the peak-to-peak energy deviation of the stacks. The latter point implies that the SM capacitor would have their size to be increase accordingly in order to keep the SM voltage fluctuation within acceptable limits.

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