

Imperial College London
Department of Physics

**Solution-processable organic blend
semiconductors for next generation thin-film
transistor applications**

by
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A thesis submitted in partial fulfilment of the degree of
Doctor of Philosophy

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This thesis describes the work carried out between October 2012 and September 2015 in the Experimental Solid State Physics group of Imperial College London, under the supervision of Prof. Thomas D. Anthopoulos. The material in this thesis has not been previously submitted for a degree at any University, and except where explicitly stated is the product of my own work.

Simon Hunter
London, February 2016

Abstract

Organic semiconductors display a wide array of enticing properties for the fabrication of novel electronic devices. Mechanical flexibility provides the potential for robust, conformable devices; while wide-area and low-temperature deposition enables the manufacture of low-cost, disposable electronics. This means that the commercial applications should be wide-ranging, as long as the performance and stability of devices based on organic semiconductors are sufficient. One of the most promising organic thin-film transistor (OTFT) systems that have been demonstrated in recent years involves the blending of small molecule and polymer organic semiconductors.

A blend of the high hole mobility small molecule 2,8-difluoro 5,11 triethylsilylethynyl anthradithiophene (diF-TES ADT) with the amorphous semiconducting polymer poly(triarylamine) (PTAA) is investigated in this thesis. This blend system has been shown to allow considerable control over processing from solution and charge carrier mobilities of up to $3 \text{ cm}^2/\text{Vs}$. The aim of this thesis is to provide a deeper understanding of the critical charge transport and stability characteristics of this blend system, while also investigating the systems suitability to a high-throughput spray-deposition technique.

In the first part of this thesis the fundamental charge transport characteristics of the diF-TES ADT:PTAA blend system are investigated. The densities of band-gap tail states in blend films of differing composition are found to exhibit considerable thermal broadening at low temperatures, and at high temperatures are controlled by the concentration of the small molecule component in the blend. In the second part of the work the electrical and environmental stability of blend OTFTs is studied. The devices exhibit state-of-the-art bias stability in an inert environment, however exposure to air and elevated temperatures highlights some interesting degradation pathways which are investigated. Finally, the blend system was used with a high-throughput spray deposition technique. Subsequent spray deposition of semiconductor and ultra-thin dielectric layers was demonstrated, resulting in the fabrication of low-power OTFTs operating at -4 V and exhibiting hole mobilities on the order of $1 \text{ cm}^2/\text{Vs}$.

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List of Symbols and Acronyms

a -Si	Amorphous silicon
AM-OLED	Active matrix OLED
C_i	Capacitance per unit area (nF/cm ²)
diF-TESADT	2,8-difluoro 5,11 triethylsilylethynyl anthradithiophene
E_0	Width of trap state energetic distribution (eV)
HMDS	hexamethyldisilazane (SAM)
HOMO	Highest occupied molecular orbital
IGZO	Indium gallium zinc oxide
I_{on}	Drain current of TFT in ‘on’ state
I_{off}	Drain current of TFT in ‘off’ state
I_D	Drain current (A)
L	Channel length (μm)
LUMO	Lowest unoccupied molecular orbital
MNR	Mayer-Neldel Rule
MTR	Multiple trapping and release
N_{tr}	Trap density (cm ⁻²)
OLED	Organic light emitting diode
OSC	Organic semiconductor
OTFT	Organic thin film transistor
POM	Polarised optical microscope

PTAA	poly(triarylamine)
RFID	Radio frequency identification
SAM	Self assembled monolayer
SKPM	Scanning Kelvin Probe microscopy
T	Temperature (K)
Tetralin	1,2,3,4-tetrahydronaphthalene
TFT	Thin film transistor
V_G	Gate voltage (V)
V_{DS}	Source-drain voltage (V)
V_T	Threshold Voltage (V)
W	Channel width (μm)
$\mu_{\text{lin}, \text{sat}}$	Field effect mobility in linear/saturation regime (cm^2/Vs)

“Is it a pimpled adolescent, now awkward, but promising future vigor? Or has it arrived at maturity, full of languor, surrounded by disappointments?”

Donald G. Fink on the transistor's commercial future, 1953.

Chapter 1

Introduction

1.1 Background

In 1954 the first transistor radio hit the shelves. This, coming almost thirty years after Lilienfeld patented the first transistor-type device, demonstrates the practical difficulties that new technologies often face when making the transition from paper to the real world [1]. Indeed even in 1953 doubts still remained over whether problems with transistor stability would prevent the devices hitting the mainstream [2]. However, in 1955 Tokyo Telecommunications Engineering Corporation released a transistor radio onto the Japanese market. The company launched their product under the snappier-sounding brand Sony, and their entry into the transistor market is widely regarded as one of the main factors in kick-starting the rapid expansion of transistor technology into all aspects of daily life. The TR-55, Sony's debut transistor radio, incorporated five transistors; nowadays smart watches pack tens of millions of them into a device that can be worn on the wrist.

Of even more pertinence to this work is the specific example of the thin film transistor (TFT), a type of transistor architecture that lends itself to large-scale manufacture and is found in the backplanes of LCD displays. While the TFT is now a truly ubiquitous technology, its history, as with earlier transistor technologies, was fraught with false starts and remained a technology in need of a problem to solve for several decades. Indeed, some

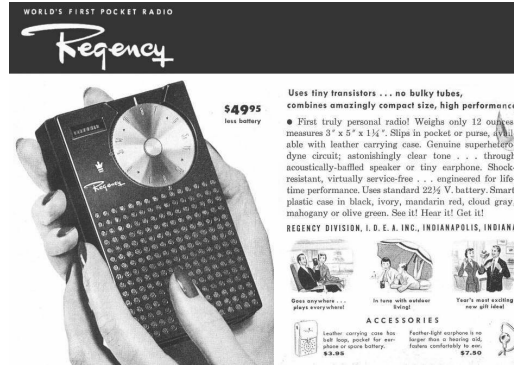


Figure 1.1: A 1954 newspaper advert for the Regency TR-1, the first commercial transistor radio.

of the earliest work on transistors of any kind was on devices operating in fundamentally the same way as modern TFTs [3]. Ultimately this was unsuccessful and so the research focus at Bell Labs turned to point contact transistors. Had this initial work been pursued further, the history of solid state electronics could have been very different. TFT technology had a resurgence in the 1960's when it battled the metal-oxide-semiconductor field effect transistor (MOSFET) technology for dominance in the integrated circuit industry. Again it lost and research funding was slashed. However, refusing to die, demonstrations of exciting TFT applications started to emerge from Westinghouse in the late 1960's, including that of a flexible audio amplifier [3]. And yet, it took a further two decades for the first commercially available TFT-based display to hit the market (Figure 1.2).

These two examples highlight considerable parallels between the history of the inorganic transistor and that of the organic transistor. Research has been conducted in laboratories around the world for over two decades towards the goal of low-cost, large area, solution-processed electronics based on organic semiconductors (OSCs), and yet the technology has still not hit the commercial mainstream. Despite this, huge advancements have been achieved in this time, with charge carrier mobilities - the ease with which charge carriers can flow through a material - improving by four orders of magnitude (Figure 1.3). Many organic semiconductors now exhibit performance bettering that of amorphous silicon, the semiconductor of choice for liquid crystal displays and low-cost solar cells. And yet, as with their inorganic counterparts sixty years ago, issues with device stability and



Figure 1.2: A Casio TV-10, the world’s first commercially available LCD, TFT-based display, released in 1983.

uniformity, as well as finding an initial commercial niche, still plague the technology.

Despite the similarities in the path to commercialisation of both inorganic and organic transistors, it is the vast differences in these technologies that is of greatest interest. Crystalline silicon, the inorganic semiconductor of choice for the vast majority of applications, is inherently brittle and expensive to manufacture. As such, it is impossible to cover large areas with transistors or make flexible devices. Organic semiconductors on the other hand are usually soluble in common solvents and inherently mechanically flexible. These properties promise to revolutionise technologies such as photovoltaics and large-area displays as well as enabling completely new product classes in large-area power transmission [4], chemical and biological sensing [5], thermoelectrics [6] and implantable medical devices [7].

As is commonly seen with disruptive technologies the path to commercialisation for organic transistors has not been easy. Typically, a new technology performs considerably worse than the incumbent by most means of comparison but has a unique advantage in one or two areas. For organic transistors this is assumed to be solution processing and large-area manufacturability. When the transistor radio hit the market in the 1950s its sound quality was far below that possible with vacuum tube radios at the time, and yet the compact form that it enabled created a new product class. The same was seen with the advent of the 1.8" hard drive: it had far too low a capacity to be useful in laptops at the time it was launched and yet its compact size ultimately lead to the creation of the

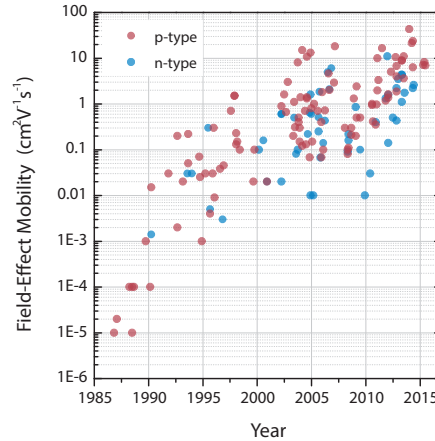


Figure 1.3: The increasing charge carrier mobility reported in TFT devices employing organic semiconductors.

iPod.

Currently, most research efforts in the field of organic transistors are aiming at the goal of being able to employ them in the backplanes of active matrix organic LED (OLED) displays. This would enable the creation of large-area, flexible or conformable displays. For this to happen it is understood that semiconductors with charge carrier mobilities of around $10 \text{ cm}^2/\text{Vs}$ will be needed [8]. The number of organic semiconductors being reported with mobilities of between 1 and $10 \text{ cm}^2/\text{Vs}$ has increased dramatically in recent years, lending weight to the argument that organic thin film transistor (OTFT) technology is on the cusp of a wide commercial breakthrough. Plastic Logic, a company based in Cambridge has shown that OTFT technology can successfully be transferred to industrial scale fabrication and have recently demonstrated a prototype flexible OLED display with OTFT backplane (Figure 1.4(b)). However, organic TFT isn't the only technology competing to provide the control electronics for next generation displays. Recently, LG brought curved OLED televisions to the market, using the transparent indium gallium zinc oxide (IGZO) TFT technology (Figure 1.4(a)). IGZO TFTs can comfortably achieve charge carrier mobilities of up to $50 \text{ cm}^2/\text{Vs}$. Therefore, while the performance of OTFTs are continually improving, the performance required to muscle into the mature display market becomes ever higher.

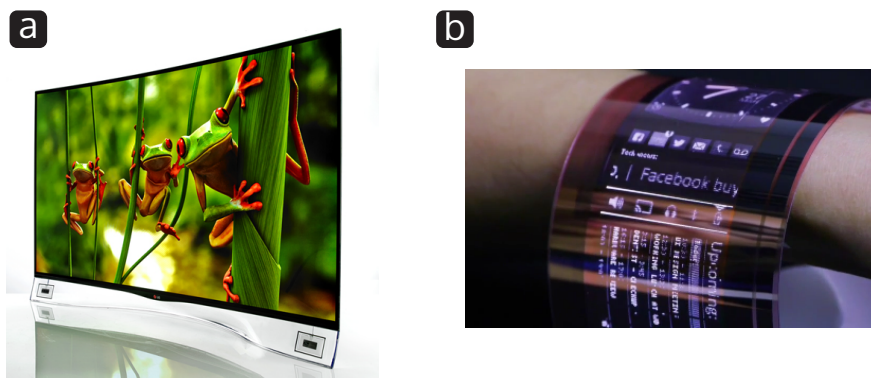


Figure 1.4: **(a)** A curved 55" display based on IGZO and OLED technology from LG. **(b)** A flexible OLED and OTFT display prototype from Plastic Logic.

Ultimately, it may not be within the display market that OTFTs initially make their greatest impact, but the efforts of companies like Plastic Logic are vital to find product-market fit with a technology that hasn't yet reached maturity.

1.2 Motivation and applications

Organic semiconductors hold a number of advantages over their inorganic counterparts. As they are the product of synthetic chemistry, molecular design presents infinite opportunities to tailor the electrical and optical properties of individual molecules. Further, by adding side chains or different chemical units and increasing the molecular weight the solubility and level of crystallisation that they achieve can be tailored to the requirements of their intended use. Highly crystalline small molecules [9, 10, 11, 12] to high molecular weight polymers [13, 14] have all been shown to exhibit excellent semiconducting properties.

This ability to tailor the molecular weight and solubility of organic semiconductors enables them to be used to produce inks with a controllable viscosity for use in additive and continuous manufacturing methods such as roll-to-roll, gravure, spray coating and inkjet printing [15]. Such techniques are well known in the printing industry, however the printing resolution required for electronic circuitry is generally much finer than that

required for standard graphical applications and engineering issues remain to be solved before such techniques will be able to produce large area electronics at high throughput [16].

High-throughput processing of organic electronics onto flexible substrates such as plastic or paper is the goal of many, and it is their inherent mechanical flexibility that may enable truly innovative products to be conceived. While inorganic oxide semiconductors may have enabled the first curved displays their lack of inherent flexibility means it may well be organic semiconductors that win the battle for rollable and foldable displays.

Beyond the fabrication of displays, the application of organic semiconductors to flexible and low-cost integrated circuits has also received considerable attention. Radio frequency identification (RFID) tags, near-field communication devices and disposable sensors are all examples of the type of product families which could be achieved by realising organic integrated circuitry. To achieve this, however, high charge carrier mobility, considerable device miniaturisation and high resolution electrode alignment will be required, as well as balanced performance of both n- and p-type TFT devices to ensure low power consumption.

With headline charge carrier mobility values in organic semiconductors surpassing that of amorphous silicon (Figure 1.3), and approaching that required for AM-OLED displays, other issues such as device stability and ease of processing become increasingly important. AM-OLED displays in particular place demanding requirements on the stability of TFTs; the prolonged application of large biases and need to reliably support high current densities are both very challenging for organic TFTs [17, 18]. Additionally, to realise high-throughput manufacturing of flexible displays it is critically important to be able to deposit thin layers, with tolerances of only a few nanometres, over large areas. The deposition method of choice in research laboratories around the world is overwhelmingly spin coating, whereby a solution is deposited onto a substrate which is then spun at >1000 rpm to create a very thin, smooth film. This technique gives great results on small wafers, however issues with film-nonuniformity and significant material waste present themselves in the coating of larger wafers [19]. As such, deposition methods such as doctor blading,

spray coating, slot-die and inkjet printing are being investigated as means of thin film deposition over large areas.

In the past few years one of the most promising avenues of research for future OTFT applications has been the development of organic transistors based on a blend of polymer and small molecule semiconductors. Such systems have demonstrated p-type charge carrier mobilities of up to $5 \text{ cm}^2/\text{Vs}$ (close to AM-OLED requirements) and simple processing, both on glass and flexible plastic substrates [20, 21]. Importantly, this method of blending semiconductors has also been employed in the fabrication of n-type transistors [22]. Realising both n- and p-type OTFTs is vital to the development of integrated circuits based on complementary logic. However, to further improve the chances of such a system moving out of the lab and into commercial use further work on understanding the fundamental charge transport processes in these systems, as well as characterisation of device stability is required. Additionally, demonstrating the fabrication of such devices using high-throughput processing techniques will prove the potential of such semiconductor blend systems in next generation electronic devices.

1.3 Thesis outline

The work described in this thesis aims to deliver a greater understanding of the performance of organic transistors based on a blend of p-type polymer and small molecule semiconductors. In the second chapter the processes of charge transport in organic semiconductors are described, along with the theory governing organic thin-film transistor performance. The chapter then proceeds to a description of the mechanisms of charge trapping and device instability that must be minimised or eliminated.

The third chapter is concerned with the materials used in fabricating organic electronic devices, and how they can be combined to create high performance transistors based on a blend of semiconductors. Processing methods are then discussed, from simple spin casting techniques, to high-throughput-compatible spray-casting. Following this is a description of the experimental methods used in this work, from device fabrication to

electrical and materials characterisation.

The fifth chapter investigates the effect of morphology and blend composition on the performance of blend OTFTs. A range of techniques including lateral conductive atomic force microscopy as well as low temperature electrical characterisation are used to develop an understanding of the distribution of band-gap trap states in blend TFTs and their effect on device performance. This provides a greater understanding of the charge transport processes in the unique blend system.

The sixth chapter develops an understanding of the electronic and ambient stability of blend OTFTs. High performing TFTs are tested for their ability to maintain high current densities over prolonged bias application as well as observations of threshold voltage shifts caused by extended application of large gate biases. These investigations deliver a deep understanding of the dominant charge trapping processes inherent in the blend system combined with a polymer dielectric.

Finally, blend OTFTs are fabricated using the high-throughput solution deposition method of spray coating. Further, this method is used to demonstrate low voltage blend OTFTs, operating down to -4 V, as well as simple inverter circuits, demonstrating the suitability of blend devices for large area, solution processed electronics. Chapter 8 discusses the conclusions of the thesis and the direction of future research on organic blend transistors.

Chapter 2

Theory

2.1 Charge transport in organic semiconductors

2.1.1 Molecular orbitals and conjugation

The electronic structure of Carbon is $1s^2 2s^2 2p^2$, however what is interesting about this is the number of ways the electronic orbitals hybridize when bonding with other elements. Specifically, the two $2s$ and $2p$ electrons form hybrid orbitals that exhibit joint s and p characteristics. The mode of hybridization which gives rise to the semiconducting behaviour in certain organic molecules is known as sp^2 hybridization, whereby one of the $2s$ electrons is promoted to the empty $2p$ orbital, causing the remaining $2s$ and two of the $2p$ electrons to create three sp^2 hybrid orbitals and one p_z orbital (Figure 2.1). Whereas the three sp^2 orbitals form strong inter-atomic σ bonds, the weaker p_z orbitals are able to delocalise along the backbone of the molecule, forming π and π^* bonds. π , or bonding-, orbitals are formed when two adjacent p_z orbitals are in-phase, leading to a reduced energy configuration. Counter to this, when adjacent p_z orbitals are out of phase the resulting wave function is higher in energy and forms a π^* , or antibonding-, molecular orbital. These two states are more commonly referred to as the highest occupied molecular orbital (HOMO) and lowest unoccupied molecular orbital (LUMO), respectively. This is demonstrated in

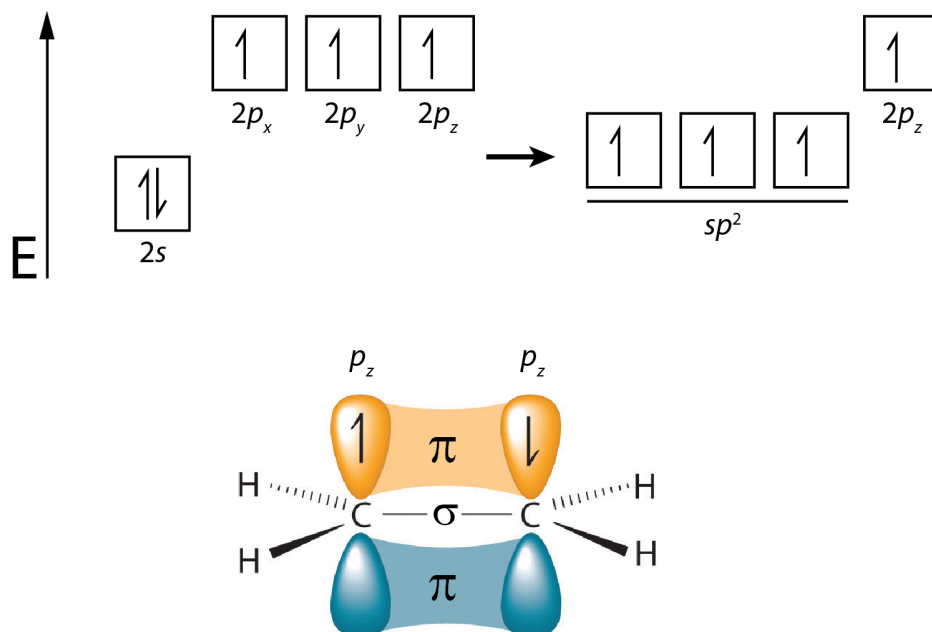


Figure 2.1: Schematic depicting the sp^2 hybridization of atomic orbitals, a process which is responsible for the semiconducting nature of certain carbon-based molecules. Below, a representation of π -bonding in the simple molecule, ethylene. π bonds above and below the plane of the molecular backbone consist of weakly-bound electrons which enable charge transport between molecules.

the simple case of ethylene in Figure 2.1. In isolation, π electrons would occupy states up to and including the HOMO level, while the LUMO would remain vacant. It is the gap between the HOMO and LUMO levels that gives rise to the opto-electronic properties of organic semiconductors and, generally speaking, the larger the molecule, the smaller the energy gap between these two states. However, except in very specific circumstances, molecules do not exist in isolation but are influenced by the molecules around them and indeed by delocalised charge carriers residing on the molecule itself [23, 24].

When a hole or electron is delocalised along the backbone of a π -conjugated molecule it perturbs the electronic structure of the molecule creating a bound state between the carrier and the molecule known as a small polaron. The result of this is that charge transport must now be considered as the interaction of carriers with the energy landscape

of the molecules it moves between. This is a fundamental difference to charge transport in ordered inorganic semiconductors, where atomic lattices form well-defined energy bands along which charge carriers are free to travel while being occasionally slowed down by phonon scattering. Such phonons, or molecular vibrations, have the opposite effect in disordered organic systems where they act to aid the hopping of localised charges from one molecule to another. While band-like transport has been reported in highly pure single crystal organic semiconductors, most practical applications of these materials result in much more disordered systems [25, 26, 27, 28].

Widely accepted theory on charge transport in organic crystals, however, fails to predict the presence of the negative mobility-temperature differential which defines band transport. Rather, the theory of charge transport has been largely built on the concept of the small polaron, and described using Marcus theory [29]. Marcus theory was developed in the 1960's to describe electron transfer reactions between weakly coupled chemical species. When applied to organic crystals the theory considers the energy required to reorganise the bond lengths of the two molecules between which the charge hops, and the energetic disorder caused by differing HOMO levels of conjugated molecules.

While this theory has been employed widely, no complete understanding of charge transport mechanisms in both pure single crystals and disordered polymers has been borne from it. Recently, Troisi suggested moving away from the reliance on Marcus theory and abandoning the concept of the small polaron [30]. He argues that it is incorrect to consider organic molecules as weakly interacting, and that in single crystals charge carriers are not localised on molecules by reorganisation of the molecular bond structure, but by the dynamic disorder of neighbouring molecules. In this model carriers do not exist in energy bands but are localised by the vibrational disorder of adjacent molecules. As such, increasing temperature reduces the probability of charge transfer and so the negative mobility-temperature differential is recovered without resorting to band theory.

Ultimately, it is accepted that a comprehensive theory of charge transport in molecular crystals is only a starting point. For theory to be able to describe and predict practical, solution processed organic semiconductors an understanding of how defects, grain bound-

aries and dopants interact is critical. In the absence of such a fundamental understanding of charge transport, models have been developed to bridge the gap between semiconductor properties and device performance.

2.1.2 Charge Transport Models

Multiple Trapping and Release

Several models have been developed to describe the process of charge transport in organic semiconductors and those most relevant to the operation of TFTs i.e. incorporating effects of charge accumulation layers, will be discussed here. One model that is frequently used, and which originates from studies into α -Si performed in the 1970's, is that of multiple trapping and release (MTR) [31]. This theory considers charge transport to occur through repeated trapping of charge carriers to states where their mobility is zero, after being thermally promoted to a conduction band-like level. The density of shallow trap states (tail states) is usually considered to decay exponentially into the band gap, thus accounting for the thermal and gate bias dependence of charge carrier mobility in TFTs [32]. At low temperatures (T), the probability of carriers being thermally released to the transport band is decreased and so transport becomes dominated by thermally activated hopping between trap sites. The number of free carriers in a semiconductor (and hence charge carrier mobility) is also determined by the quasi-Fermi level. The quasi-Fermi level is defined as the point where the occupation of states is half due to the application of an external bias, provided by a gate electrode in a TFT. Moving the quasi-Fermi level closer to the mobility edge (defined as the energy level separating trapped and free carriers) results in the filling of tail states, with charge transport occurring through multiple trapping between the transport band and shallow traps (Figure 2.2).

The consideration of a delocalised transport band is highly analogous to charge transport in ordered semiconductors; which organic semiconductors typically are not. Despite this, the multiple trapping and release model has been shown to be successful in describing charge transport in polycrystalline organic semiconductors such as sexithio-

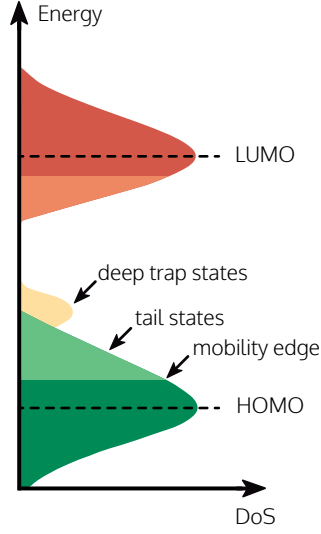


Figure 2.2: Energy level diagram showing the molecular HOMO and LUMO energy levels along with the mobility edge and distributions of tail and deep trap states in the case of a p-type semiconductor.

phene [32], pentacene [33] and tentatively in the polycrystalline poly(thiophene) polymers [34, 35, 36]. In polycrystalline materials this consideration of a conduction band-like energy level may be valid, however the MTR model ignores the effect of grain boundaries on conduction and while adjustments to the model have been proposed [37], the model is still far from comprehensive. Finally, and the main reason the model cannot be comprehensive, is that band-like transport is unrealistic for amorphous polymers where charges are typically delocalised over only one part of a single polymer chain, the conjugation length (and therefore energy) of which depends on local effects such as planarization of the polymer chain and interactions from neighbouring molecules.

The MTR model is built on the concept that at any point in time a number of charge carriers are either in a trap state, n_{tr} , or mobile state, n_f , and that the carrier mobility measured in a FET is determined by the fraction of total carriers that are in mobile states,

$$\mu_{\text{FET}} = \frac{n_f}{n_{tr} + n_f} \mu_0 \quad (2.1)$$

where μ_0 is the intrinsic carrier mobility of the material.

If, instead of a tail state distribution, we consider a discrete trap level in the semiconductor, then the number of carriers in that trap state will be determined by the energy gap between the trap and transport state, the relative density of the two states, and temperature. As the intrinsic carrier mobility of a semiconductor is gate bias independent by definition, the discrete trap situation also returns a FET mobility that is gate bias independent,

$$\mu_{\text{FET}} = \mu_0 \frac{N_f}{N_{tr}} \exp\left(-\frac{E_{tr} - E_V}{k_B T}\right) = \mu_0 \frac{N_f}{N_{tr}} \exp\left(-\frac{E_A}{k_B T}\right) \quad (2.2)$$

assuming $n_{tr} \gg n_f$ and where N_f is the density of mobile states, N_{tr} is the density of trap states, E_{tr} is the discrete trap energy, E_V is the energy of the transport level and k_B is Boltzmann's constant. The activation energy for charge transport, i.e. the energy required to move a carrier from a trap state into the transport state, E_A , is then $E_{tr} - E_V$ and can then be extracted from an Arrhenius plot ($\log \mu$ versus reciprocal T).

However, assuming a single trap energy in a disordered organic system (especially one which is polycrystalline in nature) greatly over-simplifies the distribution of states within the band gap. First described by Shur and Hack, and developed for *a*-Si TFTs, the concept of having two exponentially-distributed sets of trap states within the HOMO-LUMO band gap is now widely used in explaining the performance of organic semiconductors [38]. The first set of traps is known as the tail states; these are energetically close to, and allow hopping into, the transport level. The second set is the deep trap states, which extend further into the band gap and determine the sub-threshold performance of TFTs (see section 2.2). In reality, trap distributions may not be so easily distinguished, and tail states will often control the rate at which a TFT switches from its 'off' to 'on' state.

We replace the discrete trap level with an exponentially distributed set of traps, giving

$$N_{tr}(E) = N_{tr}^0 \exp\left(-\frac{E_V - E}{k_B T_0}\right) \quad (2.3)$$

where N_{tr}^0 is the density of trap states present at E_V , E is the energy and $k_B T_0$ is

the characteristic width of the trap distribution. The major consequence of introducing an energetically dependent trap distribution is that the carrier mobility becomes gate bias dependent. Depending on the V_G range this analysis is conducted on, one can develop an understanding of the trap distribution at different points within the band gap [32].

Thus, assuming an exponential distribution of trap states influencing a temperature-activated charge transport mechanism we arrive at the following expression for carrier mobility:

$$\mu_{\text{FET}} = \mu_{00} \exp\left(-\frac{E_A}{k_B T} + \frac{E_A}{k_B T_0}\right) \quad (2.4)$$

where μ_{00} is a mobility prefactor containing the intrinsic carrier mobility of the semiconductor.

This result is actually nothing more than the Meyer Neldel Rule (MNR) applied to charge carrier mobility. The MNR is an empirical relationship that is found to describe thermally activated processes such as ionic conduction, thermally activated hopping and atomic diffusion. It states that when a process follows an Arrhenius relationship, the prefactor (in this case μ_0) is itself exponentially distributed. This relationship has been experimentally verified in the case of many disordered (organic and inorganic) semiconductor systems, and the exponential distribution in charge traps is how this phenomenon is commonly explained [39, 40, 41, 42, 43].

Variable Range Hopping

The variable range hopping model, put forward by Vissenberg and Matters, approaches the consideration of charge transport from a very different starting point to that of the MTR model [44]. Here, the emphasis is placed on the concept of hopping between neighbouring molecules as opposed to repeated access of a charge carrier to a transport level between trapping. Physically, this is intuitively a more appropriate starting point for highly disordered materials such as amorphous polymers. The model incorporates the energetic considerations of distance between hopping sites and the activation energy associated with transport between two states of different energy.

Ultimately, however, the fitting parameters that arise from this approach (an ill-defined conductivity pre factor and a wave function overlap parameter) bear little physical meaning when compared to those defined in the MTR model. While the model can be comfortably fit to data from amorphous polymers, polycrystalline polymers and even crystalline small molecules [44, 34], it does not provide the same level of intuitive insight as the MTR model.

2.1.3 Quantifying trap states in TFTs

Application of a negative (relative to source electrode) gate bias in a TFT employing a p-type semiconductor induces an accumulation of holes in the TFT channel; this is the basis of transistor operation. However, the rate at which these holes accumulate in the channel with increasing gate bias is determined by trap states in the semiconductor, and manifests as the subthreshold slope. Therefore a measure of the transconductance of a TFT can be used to estimate the DOS function.

The Grünwald method of DOS estimation was developed to describe trap states in *a*-Si TFTs and is based on the MTR model of charge transport [45, 46, 47]. Despite its origins in inorganic semiconductor analysis the method has been applied to a range of disordered semiconductor systems [48, 47, 49, 50]. The model provides a means of extracting a DOS function from a single transfer curve, whereas most methods of DOS function estimation require transfer curves to be measured as a function of temperature. As large temperature variations can lead to DOS change in semiconductors, this method is undesirable. An excellent comparison of the different methods of DOS estimation has been conducted by Kalb *et al.* [51].

Assumptions made in the Grünwald method of DOS estimation are limited but include:

- The charge density in the TFT channel is uniform, i.e. the device is operating in the linear regime.
- The semiconductor is homogenous perpendicular and parallel to the interface.

2.1. Charge transport in organic semiconductors

- The interfacial potential, V_0 , is continuous across the semiconductor-dielectric interface, i.e. taking into account gate bias-induced band bending.

In a TFT the gate-induced electric potential above flat-band is given by

$$U_g = |V_G - V_{FB}| \quad (2.5)$$

The interface potential as a function of gate bias can be calculated from the implicit function [48]:

$$\exp\left(\frac{eV_0}{k_B T}\right) - \frac{eV_0}{k_B T} - 1 = \frac{e}{k_B T} \frac{\epsilon_i d}{\epsilon_s l \sigma_0} \left[U_g \sigma(U_g) - \int_0^{U_g} \sigma(U_g) d(U_g) \right] \quad (2.6)$$

d is the semiconductor thickness; ϵ_i and ϵ_s are the relative permittivities of the dielectric and semiconductor films, respectively; l is the dielectric thickness and σ is the semiconductor conductivity, with $\sigma_0 = \sigma(U_g = 0)$: the conductivity at flatband, or in the TFT off state. At every gate voltage Equation 2.6 is used with the corresponding drain current (and hence, σ) to solve for the interfacial potential.

It is then assumed that the electric potential and field drop to zero within the semiconductor film (see Appendix B). Secondly, as the dielectric strength is constant across an interface the following relationship holds true:

$$\epsilon_i \frac{V_G - V_0}{l} = -\epsilon_s \frac{dV}{dx} \Big|_{x=0} \quad (2.7)$$

Use of the Poisson equation with these two boundary conditions enables the calculation of an expression for the total hole density (p) as a function of interface potential:

$$p(V_0) = \frac{\epsilon_0 \epsilon_i^2}{\epsilon_s l^2 e} U_g \left(\frac{dV_0}{dU_g} \right)^{-1} \quad (2.8)$$

As the hole density in a semiconductor is the convolution of the DOS with the Fermi function, deconvoluting this function provides the DOS. By invoking the zero-temperature

approximation (treating the Fermi function as a step function) the following equation describing the DOS can then be arrived at:

$$N(E_F - eV_0) \simeq \frac{1}{e} \frac{dp(V_0)}{dV_0} \quad (2.9)$$

which is a function of energy, eV_0 , relative to the Fermi energy, E_F .

2.1.4 Microstructural effects on charge transport

Polycrystalline Films

Whether a polymer that exhibits some measure of molecular ordering, a small molecule or even a combination of different types of organic semiconductor, most materials that exhibit high charge carrier mobility in a TFT exhibit a measure of crystallinity. Unfortunately the standard MTR model assumes a homogeneous distribution of charge traps (which is not the case for polycrystalline films) and as we have seen, the variable range hopping model isn't particularly instructive. This means that in trying to understand charge transport in practical devices we are missing a very important part of the story.

Much work has been done by Salleo *et al.* on the effect of polycrystallinity in polymers and how it affects charge transport [34, 35, 36, 52], however as the work presented in this thesis uses an amorphous polymer in combination with a small molecule component, polycrystalline polymers will not be discussed further.

An understanding of charge transport through polycrystalline organic small molecule films is, however, much more relevant to the blend systems employed in this work, as charge transport in these blend films occurs predominantly through the small molecule-rich layer at the dielectric interface. The literature on charge transport through small molecule films widely supports the theory that it is limited by grain boundaries [53, 54, 55]. The proposal being that grain boundaries trap charges, leading to band-bending and the formation of potential barriers between grains, thus limiting current flow [56]. Horowitz developed a grain boundary-limited transport model for polycrystalline oligothiophene films based on

a thermally activated current through the grain boundaries [54]. The model assumes high conductivity domains (the grains) linked, in series, with low conductivity domains (the grain boundaries) such that the effective mobility in the medium is given by

$$\frac{1}{\mu} = \frac{1}{\mu_G} + \frac{1}{\mu_{GB}} \quad (2.10)$$

where μ_G is the grain mobility and μ_{GB} is the grain boundary mobility. If $\mu_G \gg \mu_{GB}$, we have conductivity that is limited by grain boundaries. This model had been developed previously for describing electrical transport through inorganic polycrystalline films and is described well by Orton and Powell in ref. [53]. Chen *et al.* applied the model to solution-processed TIPS pentacene transistors in order to explain the crystal size-dependent mobility that they observed, extracting a grain boundary mobility of $5 \times 10^{-7} \text{ cm}^2/\text{Vs}$ [55].

Despite this, most work done to investigate the effect of grain boundaries in organic thin films has been conducted on evaporated films. Due to the differing growth methods between evaporated and solution-deposited films, the very nature of grain boundaries is likely to be starkly different in these two types of semiconductor film.

The resistive effect of grain boundaries in solution processed TES ADT films has recently been investigated [57]. The TES ADT molecule used in the study is a close relation of the diF-TES ADT molecule studied in this thesis: the difference being removal of the Fluorine atom on the thiophene units of the diF-TES ADT molecule. However, TES ADT, like diF-TES ADT, is known to form large spherulite crystals, 100's μm in diameter. The authors of the study observed the thermal activation energy for hole transport within grains and across high and low-angle grain boundaries. They found that the barriers to charge transport provided by these grain boundaries were much lower than those presented by grain boundaries in evaporated films of α -sexithiophene [58].

Most interestingly, however, the authors found evidence that low-angle grain boundaries do not actually increase the density of charge traps within a polycrystalline thin film, only that the traps in these regions are deeper than those within spherulites. High-angle

grain boundaries, on the other hand, presented both a greater density and deeper trap states.

Small Molecule - Polymer Blend Films

The added complexity of having two distinct molecular species present in a semiconducting film, such as in the small molecule-polymer blends, has prevented any model of charge transport in such a system being developed. However given the lack of consensus on a model of charge transport for single component systems, it is not hard to see why. Rather, it has been the norm to explain the electrical properties of devices based on blend films in terms of percolation. Percolation theory describes how in a two-component medium whose components have significantly different conductivities (as in the case of a low mobility polymer and a high mobility small molecule), the overall conductivity is determined by the relative volume fractions of the two components. Below a certain concentration of the high conductivity medium (the percolation threshold), the conductivity of the film is determined by that of the low conductivity fraction. Above the percolation threshold, which is typically about 20-40%, the film conductivity is determined by that of the high mobility component. Quantitatively, the mobility of a given pathway through the blend is given by

$$\mu_{path}(f) = \frac{\mu_H}{1 + f(\frac{\mu_H}{\mu_L} - 1)} \quad (2.11)$$

where f and μ_L are the volume fraction and mobility of low conductivity material, respectively, and μ_H is the mobility of the high conductivity material.

Both Smith and Russell have shown electrical transport in these small molecule : polymer blend systems to be described accurately by this theory [59, 60]. It is, however, trivial to fabricate blend devices with component fractions above the percolation threshold. In this regime percolation theory is unable to give a precise description of transport through the high volume fraction, high mobility small molecule grains and the boundaries

between them. Recent work by myself and T. Anthopoulos suggests that the electrical characteristics of grain boundaries in blend films are rather complex and likely influenced by physical features such as whether the grains are coincident or separated by a gap, and whether fractions of the low mobility polymer exist at these boundaries, potentially providing additional pathways to charge carriers across the boundary [61]. As such, a grain boundary-limited model for these blend systems is likely to be an over-simplification and much more importance is expected to lie with the *type* of grain boundary that is involved, just as described by Hailey *et al.* [57].

2.1.5 Origins of charge traps in organic semiconductors

In general, charge traps are detrimental to the performance of organic transistors. They lead to a reduction in the current density a TFT can support at a given gate bias, and increase the voltages required to turn the device on. Some trap states require extended periods of time (seconds to many hours) for charges to relax into. These states are attributed to electrical instabilities and are discussed in section 2.4, whereas in this section traps at thermal equilibrium during device operation are discussed.

An interesting starting point when discussing causes of charge trapping in organic semiconductors is what *doesn't* cause traps to form. The level of charge conjugation in a molecule determines the width of its band-gap: long, planar molecules exhibit greater charge conjugation and therefore have a small band-gap. Should a defect be introduced (e.g. twisting of the molecular backbone) this would break the conjugation, forming two conjugated regions with larger band-gaps than the single molecule. Therefore, such a process cannot lead to the formation of trap sites.

Instead, the opposite is true: a localised increase in the level of charge conjugation reduces the band-gap and creates a charge trap. This can be caused by strain in a crystal leading to regions of varying inter-molecular coupling. Such traps are likely to be most common at interfaces with other materials, for example at the dielectric interface.

The theory of traps arising from inter-molecular strain and positional variations is

most relevant to crystalline materials such as small molecule semiconductors, and to some extent, polycrystalline polymer semiconductors.

Brédas and coworkers proposed that molecular sliding of up to 2.5 Å at the dielectric interface in pentacene TFTs is responsible for the creation of symmetric hole and electron traps [62]. Such states would exist up to 100 meV in depth from the transport level and the degree of displacement between adjacent molecules would be responsible for the trap depth.

An obvious further place to lay culpability for trap states in polycrystalline materials is with grain boundaries. However, the observation that the presence of grain boundaries usually leads to a decrease in carrier mobility does not imply that this is due to a high density of traps in these regions; simply the generation of a potential barrier would have the same effect. In fact, contrary to the idea that grain boundaries are sources of traps, according to the conjugation argument of trap formation a greater separation of molecules at grain boundaries would lead to reduced conjugation. This would mean that grain boundaries could not trap charge carriers.

The reality of grain boundaries is unlikely to be as simple as this, however, and multitudinous defects and microstrains in these regions are likely to lead to a complex energetic landscape. Indeed, scanning probe techniques have been used to detect charge trapping sites both at grain boundaries and within crystallites.

Frisbie *et al.* used scanning kelvin probe microscopy to reveal potential wells of a few 10's of meV in depth both at grain boundaries and within the crystals of pentacene monolayers [63]. These were hypothesised as sources of shallow traps, though no explanation of their origin was proposed. Further evidence for the existence of charge traps existing at least as much within crystallites as between them comes from work by Marohn and coworkers using electrostatic AFM techniques on TES ADT films [64].

In contrast to crystalline semiconductors, charge trapping in amorphous polymer semiconductors is much less dependent on microstructure and therefore is more difficult to analyse with conventional techniques. Additionally, according to the variable range

hopping model of charge transport, which perhaps best describes charge transport through these materials, all states can be considered as traps. In reality however, energy levels are found that mark a peak in hopping efficiency, and these can be thought of as the amorphous polymer's mobility edge. A Gaussian distribution of tail states is then used to describe the band-gap DOS [65]. Despite the general consideration that amorphous polymers are much more energetically disordered than single crystals, close to the HOMO level it has been shown that the two can exhibit very similar tail state functions [66].

2.2 Field-effect transistors

Thin film transistors are a type of field-effect transistor that lend themselves to the application of organic electronics due to their relative ease of processing and suitability to high throughput manufacturing techniques. Unlike high-performance, single crystal silicon based devices that are found in processors and amplifiers, TFTs find application in less demanding areas such as controlling pixels in liquid crystal displays. The TFT active layers are typically deposited on a structural but non-conductive substrate and over the past couple of decades the semiconductor of choice has been amorphous and polycrystalline silicon. As such, a considerable body of theoretical work has been assembled to describe the operation of these materials, indeed the models described in this section were developed for application to MOSFET devices. While the fundamentals of charge transport in these inorganic devices are different to their organic counterparts, the models actually describe OTFT performance very well.

2.2.1 Thin Film Transistor Model

A TFT is a three terminal device, the first of these (the gate) is used to modulate the conductivity of a region between the other two terminals (the source and drain). The gate terminal is isolated from the semiconducting layer with a dielectric which acts as a capacitor once a bias is applied to the gate. Unlike in inorganic devices, organic TFTs always work in accumulation mode whereby the gate bias (V_G) draws majority carriers in

the semiconductor to the dielectric-semiconductor interface. This moves the Fermi level in this region towards the conduction band (for n-type devices) or valence band (for p-type devices), exponentially increasing the conductivity of this region (typically several nm into the semiconductor layer) for gate biases below the threshold level. Once this threshold voltage (V_T) has been reached the device can be considered as being ‘on’ and further increasing V_G only increases the conductivity proportionally to V_G^2 as is described in the source-drain current relations in the linear regime (for $V_{SD} \ll (V_G - V_T)$ - eqn 2.12) and saturation ($V_{SD} \approx (V_G - V_T)$ - eqn 2.13).

$$I_{SD} = \frac{W}{L} C_i \mu_{\text{lin}} (V_G - V_T - \frac{V_{SD}}{2}) \quad (2.12)$$

$$I_{SD} = \frac{W}{2L} C_i \mu_{\text{sat}} (V_G - V_T)^2 \quad (2.13)$$

Here I_{SD} represents the current flowing through the transistor channel, W and L are the width and length of the transistor channel, respectively, C_i is the geometric capacitance of the dielectric and $\mu_{\text{lin, sat}}$ is the charge carrier mobility in the linear and saturation regimes.

Equations 2.12 and 2.13 result from the gradual channel approximation which assumes that carrier mobility is constant through the channel i.e. independent of $V(x)$ and hence x , where x is any position the in transistor channel. This has been shown not to be strictly true in some systems, however the impact to the applicability of the model is minor [67]. The second assumption is that the channel length, L , is much larger than the dielectric thickness and therefore the electric field in the x -direction is negligible compared to that provided by the gate.

2.2.2 Parameter Extraction

The performance of a transistor can be simply tested by measuring the drain current as a function of gate bias and drain voltage to produce transfer and output curves, respectively. A range of parameters describing the transistor performance can be extracted from

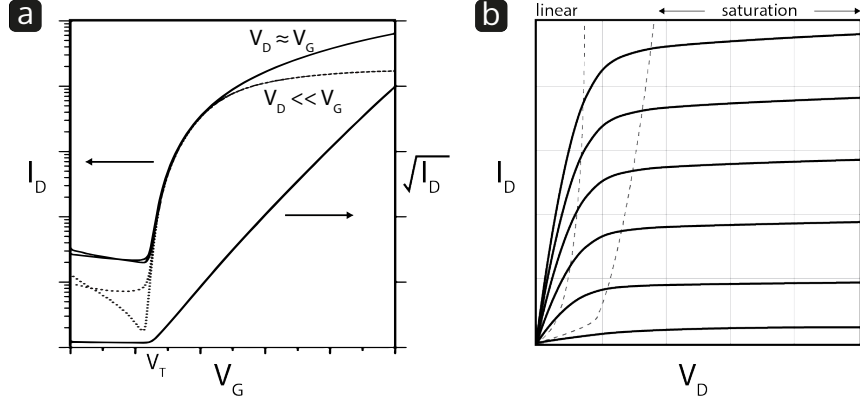


Figure 2.3: Diagrams of idealised transfer (a) and output (b) curves.

the transfer curve, while the output curve gives a good insight into the onset of current saturation as well as the efficiency of charge injection and extraction at the source and drain terminals. From the transfer curve it is possible to extract the linear and saturation mobilities $\mu_{\text{lin,sat}}$, threshold voltage, V_T , the ratio of ‘on’ to ‘off’ current, $I_{\text{on}}/I_{\text{off}}$, the switch-on voltage, V_{on} , and the subthreshold slope, S . From these parameters further insight into the microscopic characteristics of the device can also be inferred. Figure 2.3 depicts ideal transfer and output curves and how the above parameters can be extracted.

By differentiating equations 2.12 and 2.13 one can arrive at the commonly used expressions for calculating the charge carrier mobility of the semiconductor in the device being tested:

$$\mu_{\text{lin}} = \frac{L}{WC_i V_D} \left(\frac{\partial I_{D\text{lin}}}{\partial V_G} \right) \quad (2.14)$$

$$\mu_{\text{sat}} = \frac{L}{WC_i} \left(\frac{\partial^2 I_{D\text{sat}}}{\partial V_G^2} \right) \quad (2.15)$$

The main deviation of OTFT behaviour from this model, which was devised for MOSFET devices, comes from the assumption inherent in the model that carrier mobility is not a function of charge carrier density, and hence, V_G . In reality, however, this feature is

commonly seen with the inherently disordered microstructure of organic semiconductors and is the consequence of the lack of well-defined transport level [54, 68]. The Vissenberg and Matters model of variable range hopping takes this into consideration, resulting in a power-law dependence of mobility on gate bias [44].

An alternative way of accounting for this is to consider an ‘effective’ mobility, μ_{eff} , of the semiconductor which counts the average mobility of all carriers that are present in localised states, filled in the subthreshold region of the transfer curve, as well as those in the more mobile states post-threshold. The effective mobility is then found by replacing V_T with V_{on} in equation 2.12, resulting in

$$\mu_{\text{eff}} = \frac{L}{WC_iV_D} \left(\frac{I_{D\text{lin}}}{V_G - V_{\text{on}}} \right) \quad (2.16)$$

The threshold voltage of a device marks the point at which trap states have been passivated with immobile carriers and the Fermi level has reached a level that promotes sufficient carriers into the mobile states around the HOMO or LUMO level, for p- and n-type semiconductors, respectively. This definition is not as clear as that given for inorganic devices where V_T is defined by the creation of an inversion layer in the semiconductor, and organic semiconductors exhibit a much stronger temperature dependence of V_T than do their inorganic counterparts [69]. The presence of a large number of trap states will increase the threshold voltage, while free charges present in the semiconductor at $V_G = 0\text{V}$ will shift V_T in the opposite direction. The threshold voltage is found by plotting $\sqrt{I_{D\text{sat}}}$ against V_G . This returns a linear relationship and V_T is taken as the intersection of a fit with $\sqrt{I_{D\text{sat}}} = 0$ (Figure 2.3). Naturally, a threshold voltage close to zero volts is desirable to enable the creation of low-power circuitry.

The on-off ratio of a device is calculated by the difference in the maximum drain current in the ‘on’ state and the drain current seen below V_{on} . The larger $I_{\text{on}}/I_{\text{off}}$, the better as this improves the high noise margins in circuitry and reduces power consumption. I_{off} can be compromised by doping of the semiconductor by atmospheric species such as O_2 and H_2O , high leakage current through the gate dielectric, and intrinsically high bulk

conductivity of the semiconductor. More demanding applications such as the creation of robust logic circuitry as well as charging of capacitors in display backplanes require especially low values of I_{off} . Typically, an $I_{\text{on}}/I_{\text{off}}$ ratio of $> 10^4$ is needed.

V_{on} is defined as the gate bias required to bring a transistor to flat-band. In this state there exists no bending of the energy bands and so any increase of V_G results in the promotion of carriers into mobile states. If static charges exist in the dielectric or at the dielectric/semiconductor interface, e.g. as the result of unintentional doping, this perturbs the HOMO or LUMO level away from the Fermi energy and so a gate bias must be applied to account for this before any accumulation of mobile charges can occur. In the absence of such charges, V_{on} should be at zero volts [70].

The subthreshold slope is another important parameter in judging a device's ultimate performance. However, treatment of the subthreshold behaviour of a device with various models also enables an insight into the microstructural energy state distribution which governs the device's behaviour. S is simply the increase in V_G required to raise the drain current by a decade in the subthreshold regime. A natural, theoretical limit to this exists at 58.5 mV/dec at room temperature, calculated from considering a case where no trap states exist in the semiconductor at the interface with the dielectric. As such, S values in disordered organic semiconductors are typically much larger than this. Low values of S are desirable for achieving low-voltage operation and also indicate a high quality interface between the semiconductor and dielectric layers.

2.2.3 Influence of Device Architecture

There are three main device architectures employed in the fabrication of OTFTs. While the choice of which architecture to use is often determined by the materials and processing methods, there are fundamental differences in the operation of the different architectures. Often, the simplest method of testing an organic semiconductor's suitability for use in TFTs is to deposit it on a pre-patterned bottom gate substrate with the architecture shown in Figure 2.4a. In bottom gate devices, it is critical that the dielectric surface

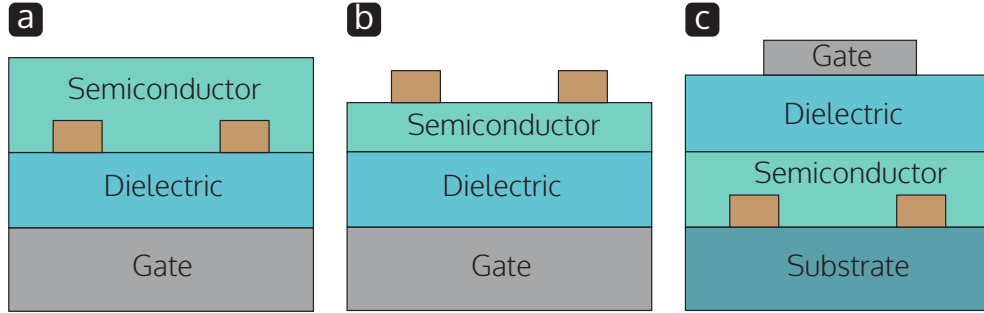


Figure 2.4: **(a)** Bottom gate, bottom contact TFT **(b)** Bottom gate, top contact TFT **(c)** Top gate, bottom contact TFT, employing a polymer dielectric.

has been cleaned extremely well so that it may form a high quality interface with the semiconductor film deposited on top. Often the dielectric surface is passivated with a self-assembling monolayer (SAM) to remove trap states. Top gate devices (Figure 2.4c) on the other hand rely on the semiconductor film being very smooth so as to reduce leakage current and allow the formation of an even accumulation layer upon application of a gate bias.

In addition to controlling the dielectric-semiconductor interface, the position of the source and drain electrodes also affect the performance of a device. Figure 2.4a depicts a commonly-used architecture in which the source and drain electrodes are coplanar with the dielectric. Coplanar electrodes typically exhibit a much larger barrier to charge injection, or contact resistance, R_c . This has been explained in several ways. The first effect is one of geometry: in the staggered electrode architecture seen in Figures 2.4b and 2.4c the gate field is able to form an accumulation layer above the source and drain electrodes, thus enabling injection of carriers from the top of electrodes, whereas coplanar electrodes will only inject from the electrode edges [71]. The second factor is concerned with the distribution of carrier density in the channel. Simulations have shown that upon application of a gate bias the carrier density in the region immediately adjacent to the source and drain electrodes is much lower than that in the channel [72, 73]. This effectively creates a resistance to the flow of carriers between the electrode and the channel. Staggered electrode architectures, therefore, demonstrate a V_G -dependent R_c , while also providing a reduced contact resistance compared to coplanar electrodes.

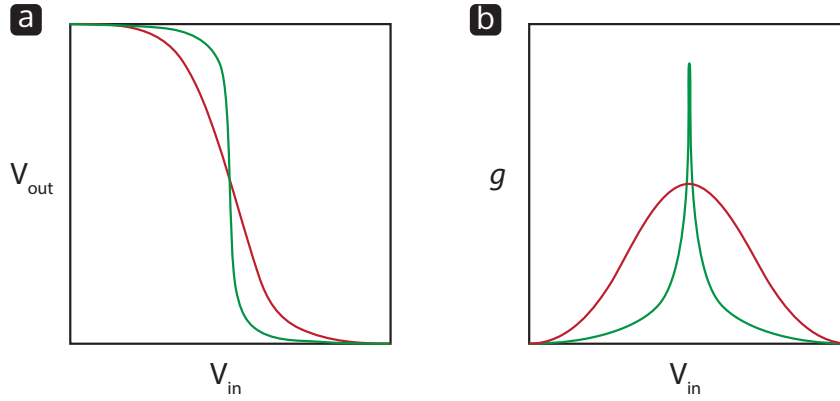


Figure 2.5: Example inverter transfer (a) and gain (b) plots shown for an inverter with high gain and large noise margin (green curve) and an inverter with lower gain and poorer resistance to noise (red curve).

2.3 Logic Circuits

Aside from use in display backplanes the main application of transistors is to create integrated circuitry. This involves the integration of hundreds of transistors in a single circuit to create components such as ring oscillators and logic gates [74]. There are three main routes to creating integrated circuitry: unipolar, complementary and complementary-like. The relative benefits and draw-backs of these will be discussed in the consideration of the fundamental building block of integrated circuitry: the inverter.

An inverter is a simple two transistor circuit which converts a high input voltage to a low output voltage, and vice versa. The inverter can be used in isolation as a NOT gate or combined with many others to create a ring oscillator [75]. The inverter effectively acts as a potential divider: At low V_{in} the drive transistor is switched off and so has a large resistance ($R_D \gg R_L$), the supply voltage is therefore dropped over R_D and the potential measured at V_{out} is that of the supply voltage, V_{DD} . Conversely, increasing V_{in} changes the relative resistances of the two transistors until the drive FET exhibits a lower resistance and the supply voltage drops across the load FET, pulling V_{out} to zero volts. Illustrative inverter transfer and gain curves are depicted in Figure 2.5.

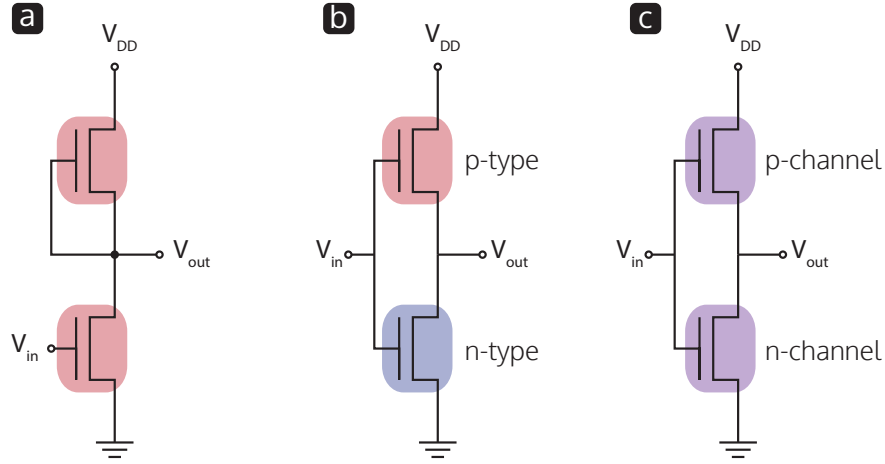


Figure 2.6: Circuit diagrams of (a) unipolar, (b) complementary and (c) complementary-like inverters.

The circuit architectures for unipolar, complementary and complementary-like inverters are depicted in Figure 2.6. Unipolar circuitry employs only FETs of the same conductivity type i.e. n-type or p-type. Such circuitry is relatively simple to achieve as it requires only a single semiconductor deposition step. This method has been used to integrate almost 2000 transistors into a single circuit, creating an e-ink display able to operate at 75 Hz [76]. However, unipolar inverters suffer from high power consumption as both transistors are ‘on’ in the high V_{in} state. Additionally, unipolar inverters also suffer from low gain and low noise margins.

Complementary inverters on the other hand require the use of both p- and n-type semiconductors which makes fabrication considerably more complex. However, the benefits to this are that complementary inverters only consume power when switching between high and low input voltage, they provide higher gain and improved resilience against noise. Complementary logic has been demonstrated with inkjet-printed n- and p-type polymer semiconductors, creating ring oscillators operating at 50 kHz [77]. In silicon microelectronics complementary circuitry is used due to the relative ease of achieving localised n- or p- doping through ion implantation; achieving high-throughput, patterned organic semiconductors will require the development of extremely high resolution printing

processes.

Finally, complementary-like inverters achieve the best of both unipolar and complementary worlds. By using a single, ambipolar semiconductor the ease of processing found in unipolar circuitry can be combined with the improved performance of complementary circuitry [78]. The main problem with this scheme, however, is that achieving a semiconductor material that performs as well under electron transport as it does under hole transport (or vice versa) has not proved to be straight forward; for high frequency operation one requires a semiconductor with balanced high mobility.

The gain of an inverter is simply found from the differential of the output voltage against the input voltage:

$$g = \frac{\partial V_{\text{out}}}{\partial V_{\text{in}}} \quad (2.17)$$

The minimum requirement for a functioning circuit is for $g > 1$, however to produce a circuit with a sufficient noise margin, in reality, the gain will need to be many times higher.

2.4 Electrical stability of organic semiconductors

Stability of transistor devices has been one of the major engineering challenges throughout the history of their development. Despite stability issues being overcome in the 1950's to enable the first generation of portable electronics, decades later stability was still a huge problem in developing TFT technology. Indeed it wasn't until the idea of incorporating hydrogen into *a*-Si, and creating *a*-Si:H, was developed that industry was able to eliminate crippling charge trapping and stability problems. Unfortunately, organic semiconductors are no different in this respect. There are many potential pitfalls for organic devices in terms of long-term stability as many of the active materials are highly sensitive to light, water and oxygen. In addition to this, one of organic electronics' main advantages - the ability to be processed at low temperatures - means that devices are typically unstable at elevated temperatures, which can aid oxidation or simply cause morphology changes [79]. Just as the inorganic electronics community did in the 1980's for amorphous silicon

development, much work must now be done with organic electronics to understand the root of device degradation pathways and, ultimately, ways of mitigating them.

Through encapsulation [80] and clever synthetic design [81, 79] device degradation due to oxidation and thermal effects can be reduced, however instabilities caused by the application of electric fields and currents are always going to be a concern. While there is no shortage of published reports on the electrical stability of organic transistors, conflicting evidence and non-standardised stressing procedures make comparisons difficult. What is typically agreed on is that under application of an electrical bias charge carriers occasionally become promoted to isolated energy levels in the semiconductor, the dielectric or at the interface between the two, and become trapped. This immobile electron or hole contributes to the charge balance but not to the electrical current through the device. This has the effect of shifting the threshold voltage towards that of the applied gate bias i.e. for p-type devices operating under negative bias, the threshold voltage becomes more negative under stressing. Additionally, when fixed gate and drain biases are applied, the current through the device will decrease over time which is of particular concern for current-driven applications such as the backplanes of emissive displays.

2.4.1 Electric Field Induced Trapping in OTFTs

Many studies of threshold voltage instabilities are conducted by applying a bias to the gate electrode while holding the source and drain at ground. Therefore no current is flowing through the device during the stressing and charge trapping occurs due to the applied electric field.

If we assume that charges become trapped with a density N_{tr} , then the competing electric field that these charges provide leads to a threshold voltage shift given by $\Delta V_T = eN_{tr}/C_i$. The rate at which this charge trapping occurs is proportional to the free-carrier density N_f and, for an exponential distribution of trap states, is given by

$$\frac{dV_T}{dt} \propto \frac{dN_{tr}}{dt} \propto N_f(t) \frac{t^{\beta-1}}{\tau^\beta} \quad (2.18)$$

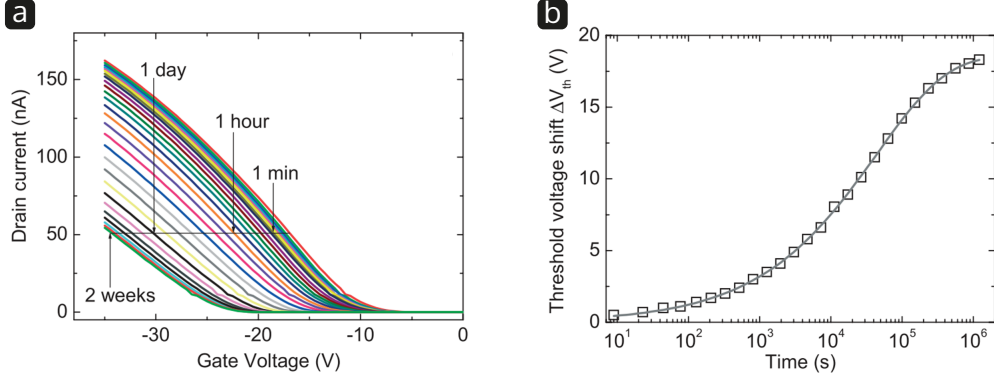


Figure 2.7: Time evolution of the threshold voltage of an OTFT under prolonged bias stress (a) showing a stretched exponential behaviour (b). Figure reproduced from [82].

τ is the characteristic relaxation time and β is the dispersion parameter ($0 < \beta < 1$). Solving this differential equation leads to the stretched exponential function that is usually fit to the V_T time evolution:

$$\Delta V_T(t) = [V_T(\infty) - V_T^0] \left[1 - \exp \left(- \left(\frac{t}{\tau} \right)^\beta \right) \right] \quad (2.19)$$

where $V_T(\infty)$ is the equilibrium, stressed threshold voltage which is usually close to the applied gate voltage and V_T^0 is the initially unstressed threshold voltage. The stretched exponential is a function that can describe a process which, while exponential in nature, exhibits a distribution of time constants. This range of time constants can be justified by considering that trap sites are themselves distributed in energy and as such will trap charges at different rates. A β value close to 1 implies little variation in trap energies while a β close to zero suggests a highly disordered system.

Work conducted on OTFTs fabricated using a BGBC architecture with a polymer semiconductor on a SiO_2 dielectric allows for direct comparison between the bias stability of polymer and a -Si semiconductors as both employ the same dielectric. Such an experiment was demonstrated by Mathijssen *et al.* and showed that the bias stability of polymer semiconductors can be as good as that exhibited by a -Si devices [82]. However, despite SiO_2 being an extremely robust dielectric material it is not appropriate for use in flexi-

ble, low cost electronics and indeed shows much poorer bias stability compared to devices where polymer dielectrics are used [83, 84, 85].

2.4.2 Current Decay in the ‘On’ State

While it has already been mentioned that a threshold voltage shift and current decay in OTFTs are both consequences of charge trapping, the non-uniform carrier concentration in the transistor channel when the device is turned ‘on’ suggests that the two phenomena should be considered separately as they are likely to include slightly different trapping processes. Typically, current decay occurs sharply within the first 100 seconds of the device being turned on before becoming more uniform or even plateauing. As with measuring the threshold voltage shift, a stretched exponential is frequently used to model the current decay in a device. The familiar relationship is given by

$$I_{SD}(t) = I_0 e^{-(t/\tau)^\beta} \quad (2.20)$$

where I_0 is the initial current that flows through the device and τ and β are the usual fitting parameters but have slightly different physical meanings from their equivalents in equation 2.19. By taking the ratio of equation 2.13 for $t = 0$ and some future time where V_T is replaced by $V_T^0 + \Delta V_T$ we can relate a current decrease (assuming saturation regime operation) to a threshold voltage shift such that

$$\Delta V_T(t) = (V_G - V_T^0) \left(1 - \left(\frac{I_{SD}(t)}{I_{SD}^0} \right)^{\frac{1}{\beta}} \right) \quad (2.21)$$

where I_{SD}^0 is the initial drain current.

The effect that atmospheric species can have on the rate of charge trapping has been clearly demonstrated in work by Matters *et al.*: The current decay seen over almost three hours of continuous operation was studied for a polymer semiconductor in vacuum, as well as in atmospheres of oxygen and water vapour [86]. A water vapour atmosphere

proved extremely detrimental to the device which suffered a 93% drop in current during the experiment. The device tested under vacuum suffered a 75% drop in current, while the device tested in O₂ dropped in conductivity by 80% though will also have suffered from doping effects. That a 75% decrease in current was observed under vacuum shows that the intrinsic stability of the devices was low, but the impact of O₂ and H₂O is also clearly of concern.

To avoid these clearly damaging effects of O₂ and H₂O, as well as replacing the SiO₂ dielectric, Sekitani *et al.* used a polyimide dielectric with pentacene semiconductor and parylene encapsulation to create robust devices and study their bias stability [87]. Post-annealing of the devices for prolonged times of 12 hours proved extremely effective in increasing the stability of the devices, which exhibited a current decay of only 3% after almost three hours. This was compared with using SiO₂ as the dielectric, with such devices suffering a current decay of almost 60% over the same time period. This not only shows that SiO₂ truly is an unsuitable dielectric material for the long-term stability of organic TFTs, but also that with the correct fabrication and encapsulation organic TFTs should be able to perform as well as their inorganic counterparts.

2.4.3 Mechanisms for electrically-induced charge trapping in OTFTs

Several different mechanisms have been proposed to explain the trap formation and filling during the application of bias stress. In *a*-Si TFTs the observed threshold voltage shifts are attributed to carrier trapping by dangling bond defects in the *a*-Si channel or charge injection into the silicon nitride dielectric [88, 89]. However, the breaking of covalent bonds which leads to dangling bond defects occur rarely in organic semiconductors (one example is when the organic molecules oxidise). To explain the equivalent process in organic TFTs new ideas are obviously needed. While trap sites in even disordered inorganic semiconductors are usually attributed only to defects or impurities, the polaronic nature (strong electronic-nuclear coupling) of charge transport in organic semiconductors means that intrinsic charge trapping in the semiconductor needs to be considered.

Chabinye, Salleo and Street proposed the slow formation of bipolarons as a process through which mobile carriers are removed from the transistor channel [90, 91]. The authors showed that the rate of decrease of the hole concentration in a polymer TFT is proportional to the square of the free hole concentration, supporting the two polaron kinetics of the authors' model. Unfortunately, all evidence for this mechanism is indirect.

For small molecule organic semiconductors, however, Jaquith *et al.* reported no evidence of such a process, showing that the rate of trap formation was linearly proportional to the free carrier concentration [92]. Contrary to the smooth polymer films investigated by Chabinye *et al.*, rougher films were fabricated which aided the electric-force microscopy imaging of trapped charge due to morphological features. The authors concluded that charge trapping in small molecule organic films is strongly dependent on local film morphology. In particular, trapped charges were seen to form at the grain boundaries in TES ADT films.

Inter-grain charge trapping was also investigated by Tello *et al.* for evaporated pentacene transistors [93]. Evaporated pentacene films, which form through the growth of island-like crystals, were shown to be susceptible to charge trapping at the boundary of grains and in gaps between them. Additionally, Teague *et al.* observed the charging of diF-TES ADT single crystals during device operation, showing that charge trapping doesn't solely occur at boundaries/defects in small molecule crystals [94].

As has been shown in a few reports already discussed [95, 87, 83], SiO₂ is not an ideal dielectric in terms of device stability. Mathijssen *et al.* employed scanning kelvin probe microscopy (SKPM) to show charge trapping occurring on the surface of an HMDS-treated SiO₂ substrate *without* the organic semiconductor [96]. The authors argued that this was evidence of charge trapping due to water at the interface, however did not repeat the experiment with alternative, polymeric dielectrics. Alternatively, Sharma *et al.* proposed that protons are produced via a reaction between holes and water at the interface [97, 98]. The protons then migrate into the SiO₂ layer and act to shield the gate field, thus causing a V_T shift.

The effect of the presence of water on the bias stability of OTFTs employing a

polymer dielectric was studied by Zilker *et al.* [99]. They showed that under the presence of atmospheric water a *positive* ΔV_T was observed for a p-type semiconductor operated under negative bias. Over short timescales (<100 s) the usual carrier trapping is observed, leading to negative ΔV_T , however over longer times the effect of water in the device strongly reverses this shift. The exact mechanism for how this occurs, however, is not understood.

2.4.4 Bias Stress Reversal

Fortunately, the instabilities seen in device performance under bias stressing have been shown to be widely reversible. When left in the dark under zero applied voltage the trapped charges will gradually be released from their localised states and the threshold voltage shift will gradually reverse. In organic devices this has been shown to occur on a similar time-scale to the prior trapping, whereas in *a*-Si devices the recovery rate is orders of magnitudes slower than the trap rate [100]. This is naturally an advantage for OTFTs because the ability of a device to quickly return to its initial state after bias is removed is as important as the bias stability of the device in the first place.

Ways of increasing the speed of bias stress recovery have also been reported. By applying a positive gate bias following stressing under negative bias increased recovery rates have been achieved [86]. However, this approach runs the risk of further injection and trapping of electrons which has also been described in references [101] and [102].

Salleo and Street described the recovery of stressed polyfluorene TFTs under illumination of device with above band gap light for the polymer [103]. They proposed that excitons generated by the absorption of light are quenched by the trapped holes, providing enough energy for the hole to escape its trap. Separate work conducted by Bürgi *et al.* arrived at similar conclusions [104].

Chapter 3

Materials and processing methods for organic electronics

In recent years advances in the performance of OTFTs based on polymer or small molecule organic semiconductors have taken somewhat divergent paths. Due to their inherent greater complexity, polymers present greater opportunity for intelligent synthetic design, and it is mainly this that has increased the performance of devices based on semiconducting polymers. On the other hand, innovation in the synthetic design of small molecule semiconductors has been less prominent than innovation in materials processing methods, which have boosted small molecule OTFTs to exhibit record performance. However, blending of semiconducting polymers and small molecules continues to exhibit extremely impressive performance in OTFTs.

3.1 Polymer Semiconductors

For most of the mid-2000's polymer semiconductors were considerably outshone by the advances being made in solution-processable small molecule semiconductors. Polythiophene semiconductors introduced the benefits of molecular packing to achieve a polycrystalline microstructure and hole mobilities of $> 0.1 \text{ cm}^2/\text{Vs}$. By ensuring organisation of the poly-

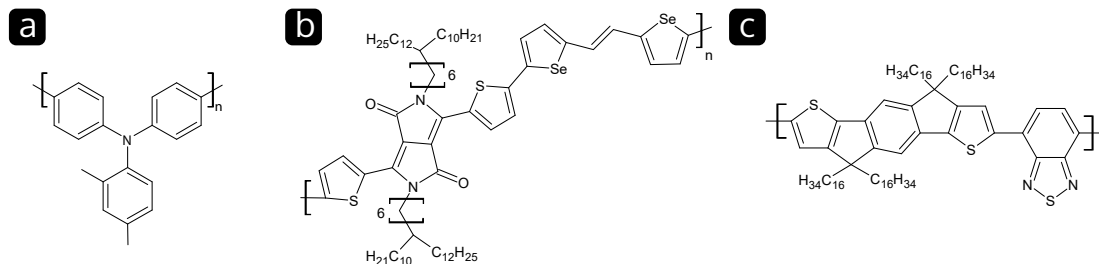


Figure 3.1: Chemical diagrams of three p-type semiconducting polymers: (a) poly(triarylamine), (b) diketopyrrolopyrrole and (c) indacenodithiophenebenzothiadiazole

mer chain backbones into lamellae oriented perpendicular to the semiconductor-dielectric interface improvements in charge transport could be achieved over the amorphous semiconductors that preceded these polycrystalline materials [105, 106]. However, by the mid 2000's the performance of these thiophene-based semiconductors had plateaued at a level below what was necessary for most industrial applications.

More recently, new molecular design considerations have once again improved charge carrier mobilities by over an order of magnitude. Instead of designing polymers to exhibit large scale crystallisation, ensuring that efficient charge transport can occur on much smaller length scales has been shown to be even more important [107, 108]. Indeed, thin films of these new breed of high performance semiconductors appear to exhibit no crystallinity at all when observed using traditional x-ray diffraction and differential scanning calorimetry techniques. This has lead to a greater understanding of the importance of non-covalent bridging connections, such as those arising from dipolar and steric interactions, which enable charge transport between domains. Additionally, through demonstrating high performance polymers with rigid backbones it has been argued that charge transport through these materials may be significantly 1-dimensional in nature, with charge carriers travelling predominantly along, and occasionally hopping between, polymer chains [109, 110].

Due to the molecular design route described above, the number of polymer semiconductors exhibiting hole mobilities of $> 1 \text{ cm}^2/\text{Vs}$ has risen dramatically. Zhang *et al.* demonstrated a polymer semiconductor with a very rigid and planar backbone (Figure

3.1c), exhibiting hole mobilities of over $3 \text{ cm}^2/\text{Vs}$ despite thin films being devoid of long range order [109]. The electro-deficient and dipolar monomer unit isoindigo has been employed with considerable success in polymers with alternating electron rich and electron poor units (so-called push-pull polymers) [111]. While originally demonstrated in organic photovoltaic devices, isoindigo-based polymers have also been shown to exhibit charge carrier mobilities of over $2 \text{ cm}^2/\text{Vs}$ [112]. A further dipolar monomer unit that has been employed in high hole mobility polymers is diketopyrrolopyrrole, which again has demonstrated mobilities of $> 2 \text{ cm}^2/\text{Vs}$ and indeed up to $12 \text{ cm}^2/\text{Vs}$ upon annealing (Figure 3.1b) [113, 114].

Beyond clever synthetic design, processing methods which aid alignment of the polymer chains has also been demonstrated. Directional drying of a semiconductor solution on a nanoscopically-patterned substrate has been demonstrated with a copolymer to increase anisotropy in the film and create OTFTs with charge carrier mobilities of $> 5 \text{ cm}^2$ [115]. It has even been reported that carrier mobilities of up to 20 cm^2 can be achieved with this method [110].

Despite the considerable improvements achieved in the performance of p-type polymer semiconductors, issues still remain in the complex synthesis routes required to create them, and often the high molecular weights needed for optimum performance. This potentially means that many of the high-performing polymeric semiconductors being demonstrated in a lab environment will simply turn out to be un-manufacturable in industrial quantities. Further, to get the best performance out of this new generation of polymeric semiconductors, high annealing temperatures of $> 200 \text{ }^\circ\text{C}$ are often needed, preventing true low-temperature deposition being achieved.

3.2 Small Molecule Semiconductors

Small molecule semiconductors benefit from generally much simpler synthesis routes and lower processing temperatures than their polymeric counterparts. By their very nature they form highly crystalline films and reasonable carrier mobilities of $0.1 - 1 \text{ cm}^2/\text{Vs}$

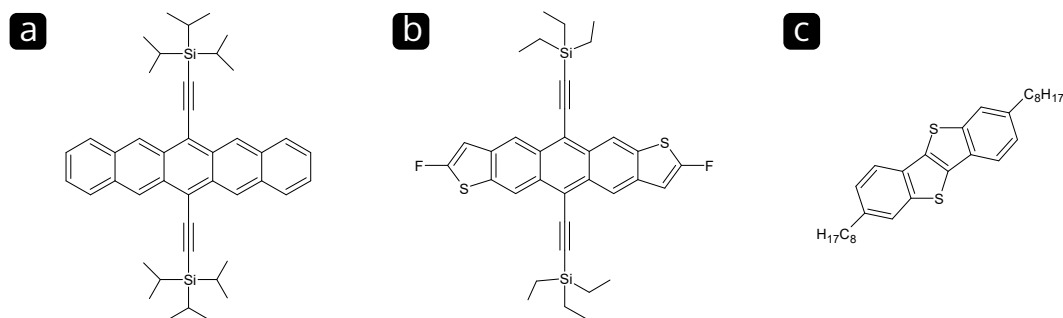


Figure 3.2: Chemical diagrams of three p-type semiconducting small molecules: (a) TIPS-pentacene, (b) diF-TES ADT and (c) C₈-BTBT

have been readily achievable for well over a decade [116]. As was seen in the field of polymer semiconductors, the advent of soluble small molecule semiconductors produced a step change in the performance of these materials. Carrier mobilities were achieved that remained gold-standard for almost a decade.

Typically, small molecule semiconductors are based on an acene core with between three and five linearly fused benzene rings. Molecules such as pentacene and anthracene (and further derivatives) had previously been shown to perform well in TFT devices when thermally evaporated, but weren't soluble in common organic solvents, preventing them from being solution processed. When Anthony and co-workers developed the soluble molecules 6,13-Bis(triisopropylsilylethynyl)pentacene (TIPS-pentacene) (Figure 3.2a) and 5,11-bis(triethylsilylethynyl) anthradithiophene (TES ADT), not only were previously insoluble molecules now able to be solution processed, but the side chains attached to the molecular backbone, and which provided the solubility, aided the π - π stacking of the molecules and thereby improved their performance [116, 117]. The TES ADT molecule was further improved through addition of fluorine units onto the outer thiophene rings. These electron-withdrawing units reduce the electron density on the backbone of the molecule and improve its stability, while dropping the HOMO level. Further, the interaction between the fluorine units and the sulphur of the thiophene have also been shown to promote closer packing of the molecules, thereby improving charge transport [81, 118]. This fluorinated version of TES ADT (2,8-Difluoro-TES ADT, or diF-TES ADT) (Figure 3.2b) has been shown to exhibit hole mobility of up to $6 \text{ cm}^2/\text{Vs}$ in single crystal form [11].

Almost concurrently with the rise of new high-mobility polymers, derivatives of the [1]benzothieno[3,2-b]benzothienophene (BTBT) (Figure 3.2c) molecule started to gain attention due to their relatively high reported hole mobilities of $> 3 \text{ cm}^2/\text{Vs}$ [119, 120]. However, it wasn't until three years later, when Minemawari and co-workers inkjet printed C₈-BTBT, that devices exhibiting carrier mobilities of $> 10 \text{ cm}^2/\text{Vs}$ could be demonstrated from solution [9]. The technique the authors used involved the use of dissimilar solvents to control the crystallisation process of the small molecule to create confined regions of single crystal.

In recent years, reported device mobilities have pushed ever-higher as new methods of solution deposition are demonstrated which aim to give much finer control over the crystal growth than is achieved through techniques such as spin-coating. In 2008, around the same time the first reports of the high mobility BTBT molecules were published, Becerril *et al.* described a method of solution deposition which involved gradually drawing a hydrophobic plate over a solution-covered substrate [121]. Evaporation quickly occurs at the leading edge of the shearing plate, seeding the small molecule and providing continuous nucleation points as the shearing plate recedes. This results in a film of long needle-like single crystals. When this technique was later applied to TIPS-pentacene, record mobilities for the molecule were achieved of up to $11 \text{ cm}^2/\text{Vs}$, almost an order of magnitude above what had been achieved with solution-processing the molecule before [122, 123]. Most recently, however, C₈-BTBT has been employed in an off-centre spin coating process which makes use of the centrifugal force to create aligned crystals [10]. Further than this, the authors argued that this process created a meta-stable crystalline phase different to what is achieved with other processing methods, and that it is this phase which is responsible for the exceedingly high hole saturation mobilities of over $35 \text{ cm}^2/\text{Vs}$ reported in 10% of devices tested, and $25 \text{ cm}^2/\text{Vs}$ on average.

While these headline values are impressive and suggest that a breakthrough into commercial display applications is imminent, small molecule semiconductors, as polymers, have their drawbacks. Firstly, processing is typically more difficult than for polymer semiconductors which exhibit greater wettability onto the substrate of choice and solubility

in common organic solvents. Further, due to the polycrystalline nature of most deposited films, grain boundaries between crystals can reduce the film conductivity and create charge trapping sites [93, 124, 125]. These effects, combined with the charge transport anisotropy frequently seen in small molecule crystals, mean that device-to-device uniformity can be much lower than for polymer OTFTs. Being able to create thousands of TFTs on a single substrate which perform uniformly is very important to applications such as OLED display backplanes. The addition of further circuitry can account for TFT variation but inherently increases complexity and cost.

3.3 Semiconductor Blends

It is with the drawbacks of both small molecule and polymer semiconductors in mind that the concept of blending the two components together arises. By combining the processability of the polymer, with the high charge carrier mobility of the small molecule, the best of both worlds could be achieved. However, to achieve this it is critical that while the two components can be deposited from a single solution, the final film constitutes a pristine layer of crystalline small molecule. Therefore the process of phase separation has to be optimized.

3.3.1 Thermodynamics of Blending

How different materials behave when combined in a solution or in the solid state is determined by the energetic considerations of two different species existing in intimate proximity. Determining whether two species will exist in a mixed state begins with consideration of the change in Gibbs free energy upon mixing:

$$\Delta G_m = \Delta H_m - T\Delta S_m \quad (3.1)$$

ΔG_m is the change in free energy upon mixing, ΔH_m is the change in enthalpy, ΔS_m is the change in entropy and T is temperature. For mixing to occur, two conditions must

3.3. Semiconductor Blends

be satisfied: firstly, the free energy of the system must decrease upon mixing, $\Delta G_m < 0$, and secondly, the second derivative of ΔG_m with volume fraction, ϕ_i , of one of the phases, i , must be positive:

$$\left(\frac{\partial^2 \Delta G_m}{\partial \phi_i^2} \right)_{T,P} > 0 \quad (3.2)$$

where P is pressure. If these two conditions aren't both satisfied then the mixture will phase separate. According to the Flory-Huggins theory, which describes this interaction in the case of polymer-polymer or polymer-solvent systems using a lattice model, the Gibbs free energy is given by:

$$\Delta G_m = RT \left(\frac{\rho_1}{M_1} \phi_1 \ln \phi_1 + \frac{\rho_2}{M_2} \phi_2 \ln \phi_2 + \chi_{12} \phi_1 \phi_2 \right) \quad (3.3)$$

where R is the gas constant, ρ and M are the component density and molecular weights, respectively, ϕ is the volume fraction and χ is the Flory-Huggins interaction parameter between the two phases. For high molecular weight molecules, such as polymers, the entropy component of the free energy is low and so equation 3.3 is governed by the enthalpy component, χ_{12} , which describes the interaction energy between the two phases, which can be estimated from their level of solubility.

An example phase diagram for a two component system is shown in Figure 3.3. It shows that there are three states that the system can occupy, depending on the relative concentrations of the components and the temperature of the system. In the stable state, typically at high asymmetry in composition, or at elevated temperature the system will exist in a mixed state. In the meta-stable state, the system will remain mixed unless interrupted by a large composition fluctuation, such as the formation of a nucleating site, at which point the system will begin to phase separate. In the unstable state, however, the system will spontaneously phase separate, initially through short range composition variations which grow into full scale lateral and vertical phase separation [126].

The type of phase diagram depicted in Figure 3.3 is able to describe a two-component

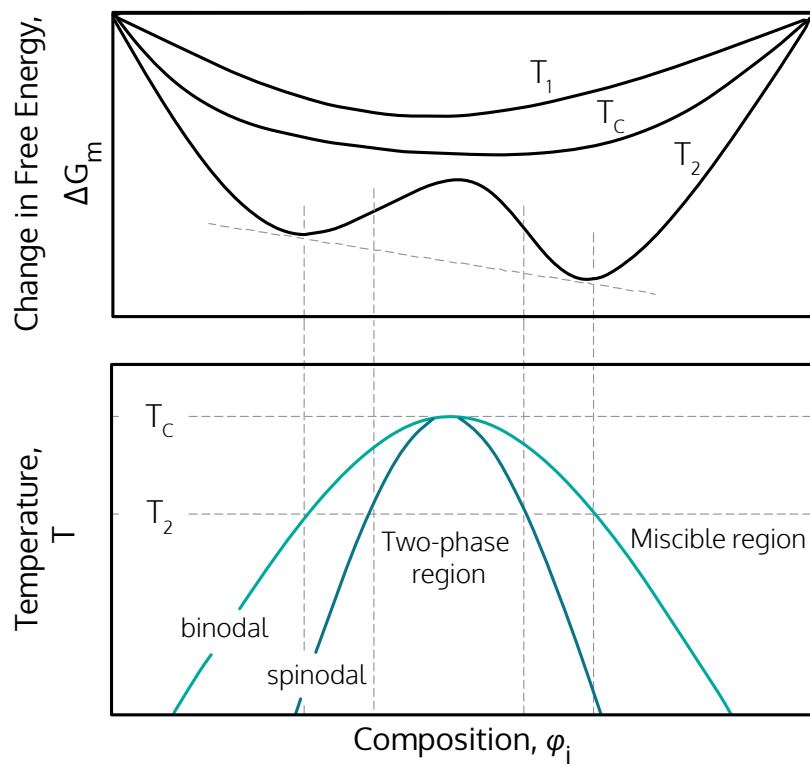


Figure 3.3: Phase diagram describing mixing in a two-phase system. At different temperatures the two phases may exist in either a miscible state, or separate through either the binodal or spinodal route, depending on composition and temperature.

system such as a polymer-solvent interaction, or a polymer-polymer system. However, in the case where a polymer, a small molecule and a solvent co-exist, the behaviour is more complicated: Not only do variations in the ratio of polymer to small molecule impact phase separation, but so does the concentration of solvent, or how viscous the solution is. Consideration of the Flory-Huggins theory has been used to rationalise the performance of blends of TIPS-pentacene with a polymer and various solvents [127]. By maximising the interaction parameter, χ , through choosing an appropriate polymer, and maximising ΔG_m , through investigating different volume fractions of the components, the blend was put in an unstable state to ensure efficient phase separation of the TIPS-pentacene from the polymer. The best performing devices were shown to be found when χ and ΔG_m were both maximised.

To ensure high performing TFT devices, ensuring that the polymer and semiconductor components phase separate isn't sufficient. Rather, it has been shown that the optimum microstructure is found in creating a single, well-defined layer of the small molecule at the film-air or film-substrate interfaces [127, 128, 129, 130, 131, 132]. This means that the driving force for vertical phase separation has to be much greater than that for lateral phase separation, which can be achieved by increasing the surface energy of the substrate and controlling the rate of solvent removal from the film. Vertical phase separation has been shown to occur on much shorter time scales than lateral phase separation and so as long as the interface between the stratified polymer and small molecule layers is energetically stable, well defined vertical phase separation can be achieved [133].

Depending on the relative rates of solvent removal and polymer-small molecule liquid phase separation, there are two mechanisms through which vertical phase separation could progress. If the rate of solvent evaporation is the prominent process and the interaction between the polymer-small molecule components is low, then the most soluble component will be drawn to the solution-air interface, while the less-soluble component will remain in the bulk of the film. However, if the Flory-Huggins interaction parameter is sufficiently large, phase separation of the components will commence while the solution is still very much dilute, and the small molecule component will be expelled to the edge of the film.

The fact that once dry the ideal film thickness for TFTs is on the order of only 50 nm means that it is wholly reasonable to expect only two or three phase-separated domains in the vertical dimension, and that the resulting morphology is strongly influenced by interactions at the surface. Indeed, it has been shown that surface energy differences of blend components can be the driving factor in determining which component gets expelled to the film surface [134]. In bulk heterojunction organic photovoltaic thin films, a somewhat analogous system usually consisting of polymer and fullerene components, vertical and lateral phase separation is observed and lateral domains are typically on the order of 100 nm, depending on the level of fullerene clustering [135, 136].

A final consideration that also has an impact on the rate and level of phase separation is the concentration of the solution. A dilute solution will enable faster phase separation of the components than a viscous one. In such a system the interaction of the polymer and small molecule components can be ignored, and rather it is the interaction with the solvent which drives any initial phase separation. On the other hand, by creating films from a highly viscous solution, or removing the solvent too quickly, incomplete phase separation may occur and the mixed state may be frozen in.

3.3.2 Polymer-small molecule blends for organic TFTs

The benefit to TFT fabrication of achieving a high level of vertical phase separation in polymer-small molecule blends is that this process can be controlled through the choice of polymer, the relative composition of the components, the concentration of the solution and the rate of solvent removal. By optimizing these parameters it is possible to extend the time given to the small molecule component to arrange into extended crystals. This greater ordering reduces the number of grain boundaries in the film and increases that carrier mobility [137].

The small molecule semiconductors for which deposition from a blend has proved most successful are the acene-based TIPS-pentacene and diF-TES ADT. The first demonstrations of improving device performance by achieving vertical phase separation in TIPS-

pentacene polymer blends was performed Madec *et al.*, and soon after by Kang *et al.* and Ohe *et al.* [138, 128, 129]. They found that by blending the small molecule with high molecular weight polystyrene, the TIPS-pentacene was expelled to the interfaces with the substrate and air. This created a layer of almost pure TIPS-pentacene at the dielectric interface and enabled them to create BGBC devices with improved performance over devices where TIPS-pentacene had been deposited in isolation. Additionally, Madec and co-workers demonstrated that phase separation of the two components could be strongly influenced by the level of crystallinity of the polymer binder. If semicrystalline polymers were used in which the crystallisation occurred on a longer time scale than that of TIPS-pentacene, then sufficient phase separation could be achieved with small molecule weight fractions down to 10%, as opposed to the 40 wt.% required using an amorphous polymer binder [138].

Hamilton and Smith then went on to show that by employing the blend system in a top-gate TFT architecture and replacing the insulating polymer with a p-type semiconducting polymer: PTAA, the device performance could be improved even further [139, 21, 137, 59]. A high boiling point solvent was used to enable controlled solvent removal after spin-coating of the films, and achieve varying microstructure depending on the rate at which this occurred. Through this method, diF-TES ADT:PTAA devices with carrier mobilities of $> 2 \text{ cm}^2/\text{Vs}$ were demonstrated, this was later shown to be pushed to $> 5 \text{ cm}^2/\text{Vs}$ with the use of a higher mobility polymer [20].

Semiconductor blends have also been shown to perform well using a range of deposition methods, as well as in both bottom gate and top gate architectures. Inkjet printing, bar coating and coronal discharge deposition have all been used and demonstrate the versatility of the system [140, 127, 131, 141]. Indeed it is the extended processing window which blending semiconductors provides, that means the resulting film morphology is not simply determined by the deposition method, but also by how the film is processed post-deposition to ensure phase separation and growth of extended crystals.

An interesting feature of the blend systems is their low apparent grain boundary resistance. Through analysis of TFTs based on the diF-TES ADT:PTAA blend with large

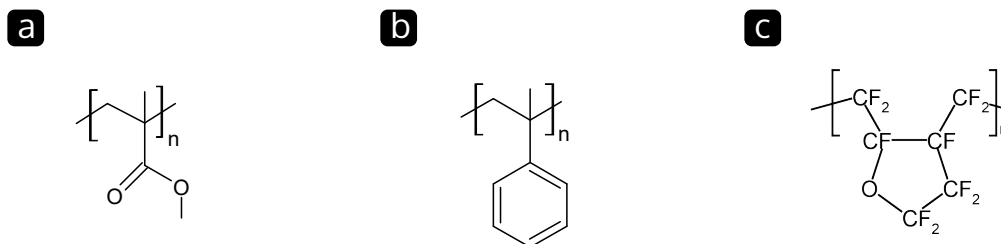


Figure 3.4: Chemical diagrams of three commonly used polymer dielectrics: (a) PMMA, (b) Polystyrene and (c) Cytop.

grain and small grain microstructures, no significant difference in carrier mobility was observed, an insight supported by conductive-atomic force microscopy analysis [61]. This is important as it demonstrates that TFTs fabricated from semiconductor blends are not reliant high-tolerance processing conditions to achieve high performance.

Even when the aim is not to employ a top gate architecture, blending polymer and small molecule components has been shown to be beneficial to the performance of simple bottom gate devices. In this case the (generally thinner) polymer layer may act as a passivation layer on the dielectric, reduce energetic disorder at the dielectric interface, or simply enable improved microstructure of the small molecule crystals [140, 142, 143, 144]. Indeed the record device performance reported for solution processed organic TFTs to date uses a blend of C₈-BTBT with polystyrene [10].

A final way of utilising the sharp vertical phase separation seen in polymer-small molecule blends is to use the polymer layer as the TFT gate dielectric. This simple method of fabricating both the dielectric and semiconductor in a single step has been demonstrated by Lee and co-workers, resulting in devices with carrier mobilities of $> 0.1 \text{ cm}^2/\text{Vs}$ [130].

3.4 Dielectrics

While the development of organic semiconductors has received a huge amount of research, work on creating suitable dielectric materials has been much less prominent. This is partly due to the ease with which semiconductors can be quickly screened using pre-patterned

SiO₂ substrates, and partly because the few polymer dielectrics that are widely used perform reasonably well. However, leakage current through the dielectric can still be significant, especially in devices employing small molecule semiconductors where the films are typically much rougher than their polymer counterparts.

The dielectric provides two crucial roles in the performance of OTFTs. Firstly, it is what enables charge carriers to be accumulated at the semiconductor-insulator interface. Secondly, it can determine the microstructure and energetic landscape at that interface. From Equations 2.12 and 2.13 it is clear that the accumulated charge, and hence conductivity of the channel, is determined by the capacitance of the dielectric, C_i . For high current and low operating voltage applications such as OLED display backplanes achieving a high capacitance is extremely advantageous and there are generally two routes through which this is achieved. Firstly, the dielectric thickness can be reduced as capacitance is inversely proportional to the dielectric thickness. This is a straightforward step to make, however decreasing the insulator thickness can increase the leakage current and the possibility of dielectric breakdown. At best this can cause high power consumption, and at worst can cause the complete failure of the TFT. The second method of increasing dielectric capacitance is employing an insulator with a high electric permittivity, ϵ . A highly polar material will exhibit a large capacitance and can be used to fabricate low-voltage devices with relatively thick layers of > 100 nm. However, devices fabricated using a dielectric with high permittivity (known as high-k dielectrics) have been shown to exhibit lower carrier mobilities than their low-k counterparts [144, 145]. This has been explained by considering the effect of polar molecules on the semiconductor interface. The dipolar interaction of a high permittivity dielectric with a disordered semiconductor will shift the local energy states at different locations in the semiconductor, having the combined effect of broadening the density of states and introducing more energetic disorder into the semiconductor. As such, more states will provide greater localisation for charge carriers and the mobility will drop.

Most polymer dielectrics, however, exhibit low permittivities. Commonly used dielectric materials are shown in Figure 3.4. Solution processable polymers such as

Poly(methyl methacrylate) (PMMA, $\epsilon = 3.5$), and polyvinylpyrrolidone (PVP, $\epsilon = 4.5$) were commonly used with evaporated semiconductors in a bottom gate configuration. However, in solution processing of the subsequent semiconductor layer, these films are commonly re-dissolved. Techniques such as UV-crosslinking have been used to prevent re-dissolution, but using a polymer that is soluble in orthogonal solvents to the semiconductor is a more robust way of creating all solution-processed devices [101, 10].

Fluoropolymers such as Cytop (Figure 3.4c) are only soluble in fluorinated solvents and so are especially suitable for the fabrication of top gate TFTs. Additionally, Cytop is extremely hydrophobic and so provides an encapsulation to air and water-sensitive semiconductors [146, 147]. The dielectric has an extremely low relative permittivity of 2.1 and so avoids generating energetic disorder at the semiconductor interface.

Self-assembled monolayers and oxidised metal layers have also been used to demonstrate ultra low-voltage OTFT operation, however device fabrication is typically much more difficult and high gate leakage a common problem [148, 102, 79].

3.5 Thin film processing

3.5.1 Spin coating

Spin coating is a method of depositing highly uniform sub-micron films from solution. The technique is widely used in industry for creating photoresists as well as depositing functional materials such as organic semiconductors. A quantity of solution is deposited on a planar substrate which is then rapidly accelerated to spin at 100's to 1000's of rpm, depending on the desired film thickness. Typically, the process of film formation can then be considered as progressing in two parts: First, the centrifugal force generated by the spin coated radially ejects the majority of the solution, while creating a liquid film on top of the substrate, typically $1\ \mu\text{m}$ thick. In the second phase solvent evaporation becomes the driving force behind film thinning, until the film viscosity rises to such a level that the film is 'dry' and remaining solvent molecules are trapped within the film [149]. Thermal

annealing is then typically used to ensure complete removal of the solvent. The resulting film thickness, as demonstrated empirically and derived from first principles obeys the following proportionality,

$$h_f \sim \eta_0^{1/3} \omega^{1/2} \quad (3.4)$$

where η_0 is the initial viscosity of the solution and ω is the angular velocity of rotation [150].

Whether spin-coating can be accurately considered as two independent sub-processes is dependent on the volatility of the solvent. For low boiling point solvents such as chloroform equation 3.4 can underestimate the film thickness, however for high boiling point solvents such as those typically used in the deposition of blend films, this is typically not an issue.

Spin speed, and therefore rate of film-thinning, can have a considerable impact on the growth of blend films with optimum vertical phase separation. It has been demonstrated that by initially spinning a solution at a relatively low spin speed the blend components are given time to begin phase separation, before increasing the speed to reduce the film thickness to a level suitable for the creation of well-defined bilayer films [139]. In most applications of spin coating, the film microstructure is determined during the film-forming process [151], however when spin-coating films from high boiling point solutions this may not be the case and control over the microstructure may be retained and utilized through thermal solvent removal. This is the method used in the fabrication of blend films in this report.

3.5.2 Spray coating

Spray-coating is a simple deposition technique well suited to large area deposition of thin films. Compared to spin coating, spray deposition enables continuous coating over large areas and is much less wasteful in terms of solution use. The process works by using an

inert carrier gas such as argon or nitrogen to atomize a reservoir of material in solution and deliver it to a substrate below. To achieve uniformity of deposition the carrier gas pressure, solvent choice, solution concentration and flow rate, substrate surface energy and temperature, airbrush-substrate distance and spray duration can all be controlled [152]. However, despite the control enabled by this wide range of parameters, the smoothness and uniformity of the film is usually less than that achieved by spin-coating [153, 154, 155]. Patterning of the deposited film can be achieved by spraying through a shadow mask, however poor edge resolution means that this may not be suitable for fine features such as electrodes [156].

Typically, droplets of the solution land on the substrate and their kinetic energy enables them to join with other droplets to form a continuous film. However, should the droplets not form a uniform film before the solvent evaporates then isolated regions of material can form and create a ‘coffee-stain’ effect. Balancing the need to deposit enough solution to create a continuous film, and not depositing too much solution such that the film becomes extremely uneven is one of the major optimization processes in developing the spray-coating technique for a particular application [157].

Unlike for spin-coating, where solvent evaporation usually occurs during the film formation process, the two processes can be controlled independently when spray-coating. This enables greater control over microstructure such as crystal growth [158]. That the film deposition and solvent removal can occur in successive steps means that the process has significant similarities to film formation of semiconducting blends by spin-coating from a high boiling point solvent, as was discussed above.

3.5.3 Other high-throughput manufacturing techniques

While not being investigated in this work, other manufacturing techniques for the mass-manufacture of organic electronics devices are briefly discussed to provide context for the work performed using the spray-casting technique.

Methods of depositing precise layers of functional organic materials over large areas

have widely been adapted from those used by the traditional printing industry. Broadly the techniques fall under two categories: “direct write printing” and “transfer printing” [159]. Direct write printing refers to a means of non-contact film deposition, such as spray-casting and inkjet printing. Transfer printing, on the other hand, describes processes that are widely used in the mass-production printing industry: Gravure, flexographic and screen printing are contained in this category and are characterised by the technique of transferring a pattern from a stamp or roll onto a substrate.

Inkjet printing has been successfully employed in the on-demand deposition of crystalline semiconductors and source/drain electrodes [9, 160, 161]. The benefits of inkjet printing include the highly efficient use of material and the simple, relatively low-cost equipment required. Unfortunately, inkjet printing is not suitable for the formation of uniform thin films and therefore it is unlikely that the technique will be able to be employed alone in the high-throughput manufacture of electronic devices.

In contrast to inkjet printing, gravure, flexographic and screen printing are much more suitable for creating uniform thin films, as long as a low-viscosity solution is used [162]. The technique of gravure, for example, uses a rotating, patterned metal cylinder that holds the solution in small cells, before depositing the ink onto a substrate when the two objects come into contact. The cell dimensions determine the minimum feature size possible, though in contrast to the requirements for uniform films over large area, high viscosity inks are required for high-resolution printing [163].

Historically, demonstrations of OTFT fabrication using high-throughput techniques have not produced devices with performance on-par with that possible using techniques which enable more control of the film formation. The reason is that achieving molecular ordering of a semiconductor is crucial to achieving high carrier mobilities, something that is often missed in the effort to deposit films over large area. Spray casting is potentially an exception to this as solution deposition and film formation can occur in subsequent steps. It is this property that makes the technique appealing for the formation of semiconductor films using small molecule : polymer blends.

Chapter 4

Experimental methods

4.1 Device fabrication techniques

4.1.1 Substrate preparation

All of the devices fabricated and tested in this report employed the top gate, bottom contact device architecture (Figure 2.4c) as this enabled the highly crystalline upper surface of the blend film to be at the semiconductor-dielectric interface. The structural substrate used for fabrication of the devices was 2 cm x 2 cm borosilicate float glass. Prior to patterning of the source and drain contacts the substrates were twice cleaned in a 2% solution of Decon 90 in deionised water. Five minute periods of cleaning in an ultrasonic bath were conducted before being rinsed in deionised water and dried in a stream of N₂. The cleaning through sonication in a detergent not only helps remove potential contaminants, but also increases the surface energy of the substrate, which aids in film formation.

4.1.2 Thermal evaporation of contacts

Thermal evaporation of Al-Au was used to pattern source and drain contacts. Firstly, a 5 nm layer of Al was evaporated through a shadow mask. This functioned as an adhesion

layer for the 25 nm Au layer that was subsequently evaporated on top. Au was chosen as the contact metal as it has a high workfunction, allowing for good hole injection into the p-type organic semiconductors being studied. The evaporation was conducted through thin steel shadow masks patterned with a range of transistor dimensions: channel lengths, L , were typically 30 – 50 μm , and widths, W , between 100 μm and 1500 μm (though larger channel widths are preferable as this minimizes edge effects of channel conduction which can result in overestimation of charge carrier mobility). The evaporation itself was conducted at around 10^{-6} mbar and a deposition rate of 1 $\text{\AA s}^{-1}$ up to a total thickness of 30 nm. Evaporation of the Al gate electrodes was conducted under the same conditions but a slightly thicker layer of 40 - 50 nm was used to create a more robust contact.

4.1.3 Self assembled monolayer treatment

To ensure proper alignment of the Au work function to the semiconductor’s HOMO level at the source and drain interfaces, the electrodes were treated with a monolayer of pentafluorobenzenethiol (PFBT). The PFBT was prepared in solution with IPA at a concentration of 0.1 vol% and pipetted onto the substrate so that all the electrodes were covered. The substrates were then covered and left for five minutes to allow the monolayer to form. Finally, substrates were rinsed with IPA and dried in N_2 .

4.1.4 Spin casting

Semiconductor layers were deposited from solution in a N_2 environment. Small molecule : polymer blends were spin-coated at a speed of 500 rpm for 10 sec before increasing the speed to 2000 rpm for a further 20 sec. This had the effect of ensuring full coverage of the solution over the substrate before achieving the desired film thickness. The chosen small molecule component was the high mobility p-type semiconductor, diF-TES ADT, while the polymer matrix component was PTAA. The blends were typically formulated with a 1:1 mass ratio of small molecule to polymer (unless otherwise stated) in a total 4 wt% solution with 1,2,3,4-tetrahydronaphthalene (tetralin). Tetralin is a high boiling

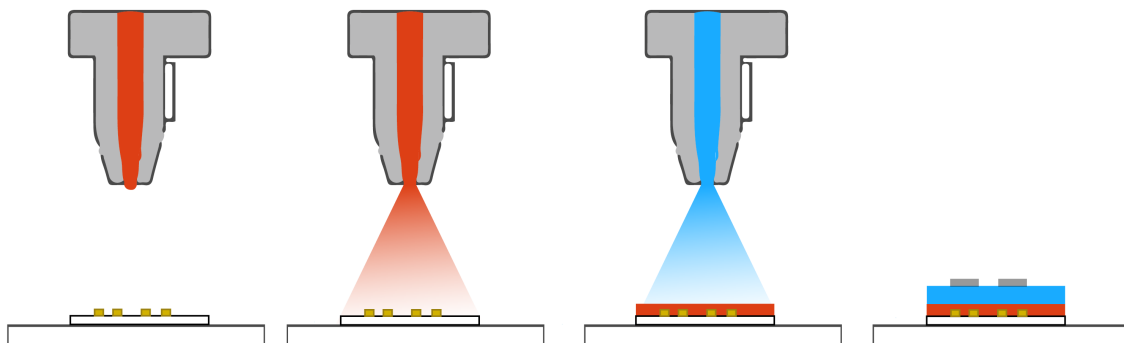


Figure 4.1: Cartoon depicting the subsequent deposition of semiconductor and dielectric layers for top gate TFTs using a spray deposition technique.

point (180 °C) solvent meaning that after spin coating, the films needed to be annealed at 100 °C for roughly five minutes to ensure removal of residual solvent. Single component small molecule or polymer films were deposited from a 1-2 wt% toluene solution and spin coated at 2000 rpm for 20 sec. In all cases 60 μl of solution was deemed sufficient to form a high quality film.

The dielectric layer was then deposited, also by spin coating. Cytop (Asahi Glass Co.) was the chosen material as it utilises a fluorinated solvent which is orthogonal to the layer below, meaning no re-dissolution of the semiconductor layer occurs [145]. Cytop is highly viscous meaning a spin speed of 2000 rpm for 60 sec was required to form an even film. The whole device was then annealed a second time at 100 °C to remove excess solvent.

4.1.5 Spray casting

Spray casting of blend devices was conducted in a fume hood using a hand-held airbrush. An N_2 carrier gas was used to atomize a reservoir of semiconductor or dielectric solution and deliver it to a substrate, forming a continuous film. The airbrush used was a Simair XL2000 with a nozzle diameter of 0.4 mm. The carrier gas was pressurised at 15 psi and the airbrush held statically at a height of 30 cm above the substrates during deposition. Spraying time for both the semiconductor and dielectric layers was approximately two

seconds and a constant deposition rate was achieved by shielding the substrates at the beginning and end of the spray. The spray casting was conducted in ambient atmosphere onto substrates at 20 °C. Four 2 cm x 2 cm substrates were typically coated in a single pass.

The diF-TES ADT:PTAA blend was combined in a 50 wt.% ratio and deposited from a 20 mg/ml solution using tetralin solvent. The concentration was reduced to half that of the spin casting solutions as the spray deposition resulted in a larger volume of solution being deposited on the substrates. The blend films were annealed at 150 °C after solution deposition. This is higher than the temperature used for spin casting as the volume of solvent in the spray cast films is higher and a higher temperature anneal provided more even solvent removal and therefore a more uniform semiconductor film.

Cytop was diluted with the fluorinated solvent, FC-43 (boiling point = 174 °C, Acota Ltd [164]), to achieve control over the dielectric thickness. A ratio of 1:3, by volume, Cytop-to-solvent was used for a film thickness of 600 nm, and a 1:4 ratio, combined with shorter deposition time, for a dielectric thicknesses down to 100 nm. The Cytop films were dried at 100 °C for 20 minutes before being slowly cooled to room temperature.

4.2 Electrical characterisation

4.2.1 Capacitance measurements

Impedance spectroscopy was used in this work to compare the geometrical capacitance of dielectric films of Cytop, deposited from spin and spray casting. When an alternating voltage is applied to a capacitor it gives rise to a phase difference between the current and voltage. It is from this phase change and change in signal amplitude that the geometrical capacitance can be calculated, according to

$$C_i = \frac{1}{A \omega \text{Im}(z)} \quad (4.1)$$

This is typically extracted from a curve of $1/\text{Im}(z)$ versus ω . A Solartron 1260 was used to conduct these measurements, which were taken on eight capacitors of different dimensions. The applied voltage was swept from 1 MHz to 10 Hz, with an AC amplitude of 20 mV and DC level of 1 V.

4.2.2 Transistor current-voltage measurements

In order to extract key parameters such as charge carrier mobility and threshold voltage of TFTs the drain current of a TFT was measured as a function of gate voltage and drain voltage. This enabled the creation of transfer and output curves, respectively. Additionally, the gate leakage current, I_G was also measured to determine the quality of the insulator layer and ensure that the flow of charge through the entire device during operation is accounted for.

Electrical device characterisation was generally conducted in a nitrogen atmosphere (typically, $\text{H}_2\text{O} < 2.5$ ppm, $\text{O}_2 < 0.5$ ppm), but also in air and under vacuum (10^{-5} mbar). The vacuum probe station had the capability for temperature control between 78 K and 370 K, through the use of liquid nitrogen and a heated stage equipped with a proportional-integral-differential (PID) controller for achieving stable temperatures. Temperature-controlled measurements were performed by cooling the vacuum chamber and test stage to 78 K and slowly increasing the stage temperature by 10 K intervals, with a 10 minute hold time at each to ensure that thermal equilibrium between the stage and the sample was reached.

The devices themselves were contacted by micropositioners attached to source measurement units and either Keithley 4200 or Agilent B2902 parameter analysers. Gate bias stressing experiments were conducted using the Keithley 4200 whereby a constant bias was applied to the gate and periodically interrupted for the measurement of a transfer curve.

4.3 Materials characterisation

4.3.1 Polarised optical microscopy

Polarised optical microscopy (POM) is a tool for quickly assessing the morphology of a crystalline film. Understanding the size and distribution of semiconductor crystals can be a good indicator of whether the film will perform well in a TFT, as well as performing as a simple diagnostic tool for rationalising the behaviour of a TFT. Obviously POM is only able to give a very superficial description of the device, for instance it is unable to give any information on the quality of the dielectric-semiconductor interface, but for providing a basic understanding of the semiconductor morphology it can be very helpful.

Polarised microscopy utilises the principle of birefringence exhibited by asymmetrically-ordered materials, such as crystalline semiconductors. When a beam of light of a certain polarity is incident on a birefringent medium it is split into two perpendicularly polarised beams. These two beams, named the ordinary and extraordinary, observe a different refractive index of the crystal and so travel through the medium at different speeds. Due to this speed difference, when the two beams exit the medium they are out of phase with one-another.

By placing a polarising filter before the birefringent medium the light is forced to assume only two polarisations as it passes through the medium. These two beams are then be combined at the other side by passing them through a second polarising filter oriented perpendicular to the first. The interference between the two out-of-phase waves determines the colour of the light that is then visible. That the two polarising filters are oriented perpendicular to one-another means that any light that does not pass through a birefringent material is blocked by the second filter.

The polarising optical microscope used in this report was a Nikon LV100, equipped with 5x - 50x magnification and connected to a CCD camera for capturing images.

4.3.2 Atomic force microscopy

Atomic force microscopy (AFM) is a surface imaging technique able to map morphological features on the order of 10 nm, while scanning regions up to 50 x 50 μm in size. The resolution in the z-axis, however, can be sub-nm. As such, the technique is versatile enough to be able to map the finest of morphological features, such as crystalline boundaries and molecular terracing, as well as imaging full TFT channels.

AFM is typically operated in one of two regimes: contact or AC mode. In contact mode a microfabricated Si probe is raster scanned over the sample to be imaged. Physical interaction between the probe and the sample causes the cantilever to bend in reaction to the topography of the sample. A laser beam is reflected off the cantilever onto a split-diode photodetector. Any bending of the cantilever changes the position of the reflected beam on the photodetector, the signal from which can then be used to reconstruct the topography of the sample. As the probe is constantly in contact with the sample, both the probe and the material it is imaging are susceptible to damage, which can convolute the image produced.

In AC mode, on the other hand, the AFM probe does not come into prolonged contact with the sample, enabling higher-resolution and destruction-free imaging. A piezo-electric oscillator is used to vibrate the cantilever at close to its natural frequency. When the probe approaches the sample it is imaging, the electrostatic repulsion between the sample and the probe damps the oscillation while a feedback loop adjusts the tip height to maintain constant oscillation amplitude, thus the sample topography may be imaged.

In addition to a purely topographical understanding of the sample being imaged, the lateral force on the probe may also be mapped concurrently with topography. This lateral force is a function of the material properties that the probe interacts with. For instance a soft polymer will provide greater friction than a hard glass sample. Therefore, this information may be used to highlight the presence of different material phases or crystal orientation when it is not obvious from the topography.

4.3.3 Conductive atomic force microscopy

Conductive atomic force microscopy (C-AFM) is an extension of contact mode AFM. In this instance a metal-coated probe (typically Pt) is scanned over a sample held at some electrical potential. The cantilever is grounded and connected to a pre-amp in the nose-cone to measure the electrical current which flows between the probe and the sample. as such, sample conductivity can be mapped with a resolution of a few 10's nm concurrently with topography. Typically the probe is scanned vertically above a biased electrode and separated by a thin semiconducting or insulating film, the electrical properties of which are to be investigated. This is instructive for materials and devices through which vertical current flows, such as solar cells and OLEDs, however for TFTs, which rely on lateral charge transport, this is not particularly instructive. Recently, I demonstrated a method of measuring lateral current flow through a semiconductor thin film, therefore being directly applicable to the performance of TFTs [61].

AFM measurements, both AC and C-AFM, were conducted using an Agilent Technologies 5500 atomic force microscope. In all cases the sample was scanned at between 0.3 - 1 line/s as this was deemed to give an acceptable balance between speed and resolution, while also avoiding sample drift which can be an issue at low scan speeds. The resulting data was analysed in Gwyddion [165]. AC-AFM analysis was conducted using Budget Sensors Tap300Al probes which exhibit a nominal force constant of 40 N/m and resonant frequency of 300 kHz. Conductive probes used for C-AFM imaging were triangular Mikro-Masch CSC11 cantilevers with Pt-coated probes, of radius 20 nm. Two cantilever sizes were used, with force constants of 6 and 0.5 N/m. No difference was observed between the cantilevers on imaging the samples used in this report. During scanning a thermally evaporated electrode on the sample to be imaged was positively biased, with the probe held at ground. This ensured hole injection from the electrode into the sample, and extraction through the probe. This was observed to be a more stable method of current mapping than injection of holes through the probe which generates a large electrical field due to its extreme aspect ratio.

Chapter 5

Charge transport and trapping in organic blend transistors

5.1 Introduction

The thin film transistor achieved little commercial success for many decades. That was until, in the late 1970s, Le Comber, Spear and Ghaith found a method of creating robust amorphous silicon TFTs, through doping the semiconductor with hydrogen gas to pacify the dangling bond trap states [166, 167]. This demonstrates the importance of understanding semiconductor band-gap states to the creation of high performance, robust TFT devices. Simply, the shape of a semiconductors density of states (DOS) and its occupied fraction determine the electron/hole transport properties, and ultimately whether it is a viable material for use in TFTs.

The trap states present in single crystal [168, 169, 170], polycrystalline small molecule [171, 172, 173, 174, 175] and polymer [176, 177, 91, 36] semiconductors has been investigated relatively widely, with a few reports looking at the consistency between them [169, 173, 51].

This chapter describes two approaches used to gain a better understanding of the

nature of charge transport and trap states in diF-TES ADT:PTAA blend transistors. Initially, the performance of OTFTs fabricated using a range of semiconductor blend compositions is investigated, alongside single-component devices. Variations in performance are rationalised in terms of microstructural observations. Secondly, the multiple trapping and release model is used to gain a simple view of the energetics of charge transport, before a more thorough investigation into the density of states function of blend devices is conducted, based on the method developed by Grünewald (Section 2.1.3). Lastly, the results of these two analyses are compared.

5.2 Control of semiconducting blend film microstructure and TFT performance

While the technique of creating organic transistors from blends of semiconducting materials has been shown to be extremely promising for several years now, there has been no systematic study into how the semiconductor microstructure influences the energetics of the system. It is well known that the microstructure of semiconducting films, especially the presence of grain boundaries and different crystal orientations, can have a pronounced effect on the TFT performance. Add to this the presence of a polymer phase and the result is an extremely complicated semiconductor system.

This section describes the performance of blend TFTs fabricated from a range of small molecule to polymer blend ratios. The different blend ratios show the evolving microstructure of the surface of a blend film with increasing small molecule component. These films were then characterised using lateral conductive atomic force microscopy (C-AFM) to correlate device performance with microscale conductivity features in the small molecule : polymer blends.

Top gate TFTs were fabricated from spin-cast diF-TES ADT:PTAA blend films with a range of compositions between 30 - 70 wt.% diF-TES ADT, increasing in 10 wt.% intervals. An 800 nm layer of Cytop was used as the dielectric. Films with a small molecule weight fraction below 30% exhibited no phase separation and crystallisation (as observed

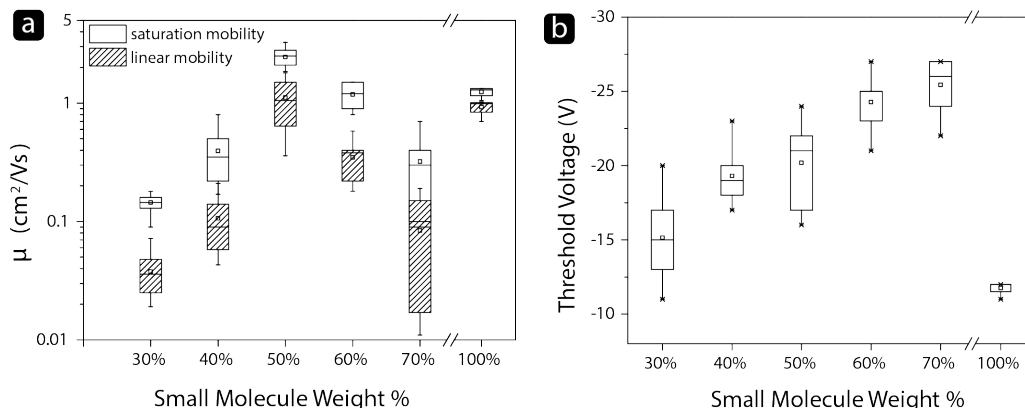


Figure 5.1: Plots of hole mobility (a) and threshold voltage (b) as a function of blend composition for top-gate TFTs fabricated using a diF-TES ADT:PTAA semiconductor blend.

by polarised optical microscopy). Conversely, semiconductor blends with > 70 wt.% diF-TES ADT were not sufficiently viscous to create a uniform thin film for TFT fabrication. At least ten devices were fabricated and tested for each of the blend ratios and their key performance parameters are shown in Figure 5.1. As has been previously demonstrated, the 50 wt.% blend films exhibited the highest hole mobility with a saturation mobility of $2.4 \pm 0.4 \text{ cm}^2/\text{Vs}$ and linear mobility of $1.1 \pm 0.5 \text{ cm}^2/\text{Vs}$, with the error ascribed to these mean values being the estimated standard deviation of the distribution [139]. With decreasing small molecule concentration the hole mobility in these devices drops away sharply, with the change from 50 wt.% to 40 wt.% causing an order of magnitude drop in both linear and saturation mobilities. Similarly, above the optimum 50 wt.% composition mobility decreases and device to device variation increases.

To rationalise the stark performance variation seen in devices fabricated from different blend ratios, C-AFM mapping was used to investigate the morphology and microscale conductivity features in these films. The resulting topography and conductivity maps, as well as wider-area POM images, are shown in Figure 5.2. The 30 wt.% films exhibit thin crystallites with varying degrees of interconnectivity. It is evident that despite the high concentration of polymer in the blend, phase separation has still occurred, with the crystallites protruding from the featureless surface of the amorphous under-layer. As can

be seen in the POM image, crystallite growth still occurs through the nucleation and growth of spherulites, as is seen in all the blend films, however there either isn't sufficient diF-TES ADT to form continuous crystals, or the high concentration of polymer has suppressed complete vertical phase separation of the two components. A region of high crystal connectivity is shown in the 30 wt.% AFM images. The connected crystals exhibit high conductivity compared to the amorphous layer underneath, while a region of lower connectivity in the upper left corner of the maps exhibits reduced conductivity. The simple fact that less of a transistor channel will be connected by high-mobility diF-TES ADT crystals is likely to account for a proportion of the mobility drop compared to a film of optimized crystals. However, the film still exhibits around 45 % coverage of crystals, suggesting that the drop in coverage of high mobility semiconductor would not account for the $\sim 50\times$ mobility drop seen between devices fabricated from 50 wt.% and 30 wt.% blend films. Instead, it is likely that while crystallite coverage in the 30 wt.% film is significant, many of these crystallites do not provide efficient pathways for holes due to their lack of alignment with the channel and considerable number of isolated crystallite regions which act as 'dead ends' for charge carriers.

At 40 wt.% diF-TES ADT crystals exhibiting high interconnectivity are formed. Voids in the surface crystal layer still exist, but with much larger features i.e. both regions of connected crystal and voids in the crystal are larger in size than those in the 30 wt.% films. As a result of the larger crystals and complete connection between them, device performance is improved, with hole mobilities around 3x greater than the 30 wt.% TFTs.

At 50 wt.%, the optimal ratio, larger spherulitic crystals are formed that frequently span the entire TFT channel and are only occasionally interrupted by voids at boundaries between crystals. This improvement in microstructure leads not only to a further improvement in hole mobility, but also to a reduction in device to device variation, as the microstructure is much more uniform.

Increasing the concentration of diF-TES ADT above this level, however, begins to disrupt the evenness of this layer. At 60 wt.% diF-TES ADT a second mode of crys-

5.2. Control of semiconducting blend film microstructure and TFT performance

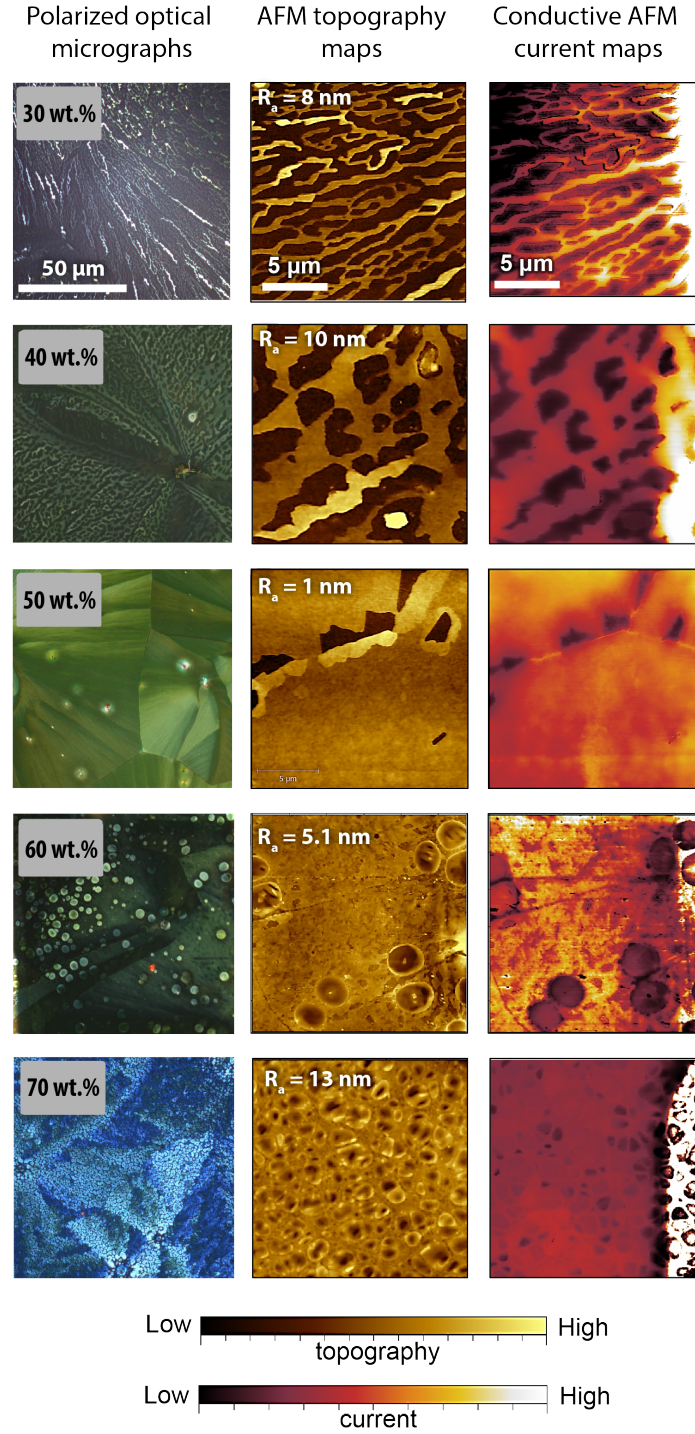


Figure 5.2: Polarized optical micrographs, AFM topography maps and lateral conductive AFM maps of diF-TES ADT blend films with a diF-TES ADT weight percentage of 30 - 70 %. A buried electrode is situated at the right-hand side of the AFM images and the conductivity values are normalized to account for variations in tip-sample contact resistances.

tallisation becomes apparent. Individual craters of crystalline diF-TES ADT (as verified by the friction map in the AFM scan) form in the middle of spherulitic crystals. Not only do these features increase the surface roughness of the film, but they are also highly insulating, as show the the C-AFM map of Figure 5.2. At 70 wt.% diF-TES ADT this apparently homogenous crystallisation, caused by the supersaturation of diF-TES ADT molecules, becomes the dominant feature in the film morphology [178]. Nucleation and growth of spherulitic crystallites is still somewhat evident in Figure 5.2, however this is suppressed by the process of homogenous crystallisation whereby solvent is removed from the film faster than the molecules can rearrange to create a more ordered microstructure. The considerably lower conductivity of this crystallisation regime, combined with the increased roughness and disorder in the film, mean that not only is hole mobility dramatically reduced, but the device variation also increases.

This investigation showed that by altering the blend ratio a wide variety of film microstructures can be achieved, and the microscale conductivity of different morphologies can explain the considerable variation in device performance. However, to gain an understanding of how these different microstructural features effect the energetic distribution of states at the edge of the band gap, further investigation was conducted.

5.3 Activation energy analysis of charge transport in blend TFTs

In order to connect the microstructural and TFT performance characteristics discussed in section 5.2 to a more fundamental understanding of the density of states (DOS) in the semiconductor band-gap, the devices previously discussed were tested at temperatures between 90 K and 320 K. This enabled an investigation into both the impact of gate doping and temperature on the transport mechanisms in the blend films.

According to the multiple trapping and release (MTR) model of charge transport (as discussed in section 2.1.2), in organic semiconductors the density of trap states at the band gap edge is a function of temperature, while charge carrier mobility is both temperature

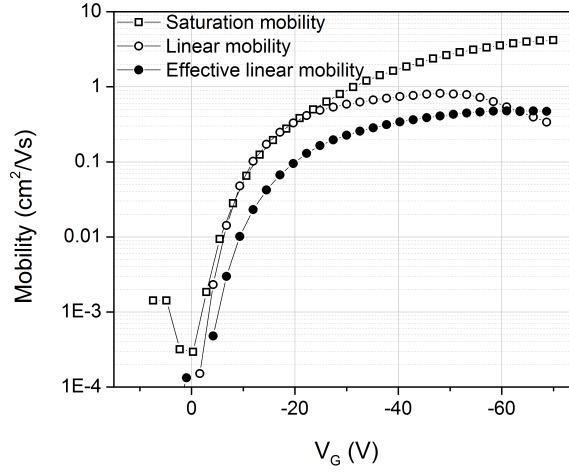


Figure 5.3: Comparison of linear and saturation hole mobility values of a 50 wt.% blend device measured at room temperature. The linear mobility calculated using the gradual channel approximation exhibits an unphysical mobility decrease at high gate bias. This is eliminated by the effective linear mobility calculation.

and gate field dependent. In measuring the temperature dependence of carrier mobility the effective hole mobility in the linear regime was considered. Considering carrier mobility in the linear regime ensures that the charge distribution, and therefore mobility, is constant across the channel. Taking the effective mobility, μ_{eff} counts the contribution of all mobile and trap states into the mobility calculation and so is more suitable for systems where the semiconductor is inherently disordered, which is typical for organic systems. A comparison between saturation and linear mobilities calculated using equations 2.15 and 2.14, and the effective linear hole mobility of a 50 wt.% blend device at room temperature is shown in Figure 5.3. The linear mobility calculated using the usual gradual channel approximation exhibits decreasing mobility at high V_G , which is unphysical for a disordered system such as this. The effective mobility, on the other hand, demonstrates a more realistic function of $\mu = \mu(V_G)$. The difference between the linear and saturation mobilities is expected to be due to contact resistances between the source/drain electrodes and the high mobility TFT channel.

Plots of μ_{eff} against temperature and gate bias, are shown in Figure 5.4. Added to the comparison are TFTs based on pristine PTAA and diF-TES ADT semiconduct-

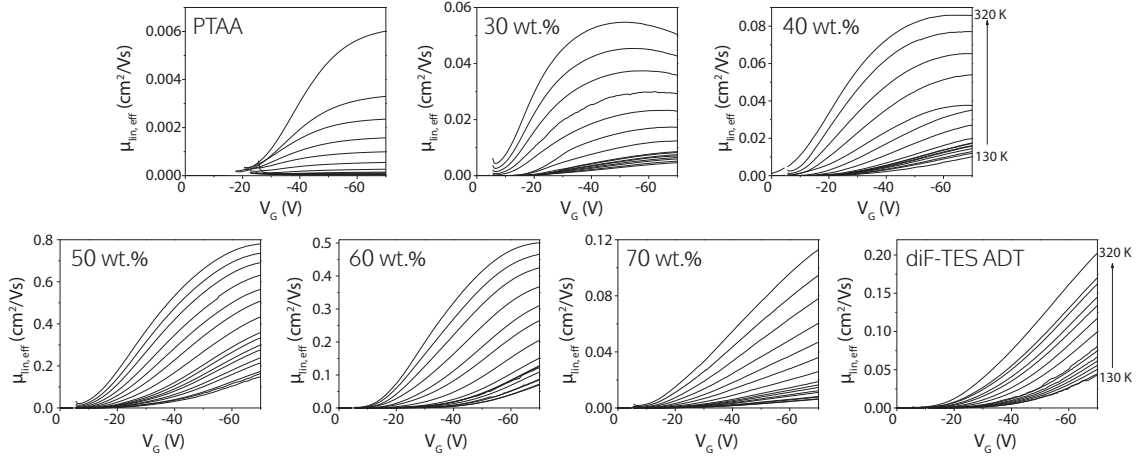


Figure 5.4: Hole mobility as a function of temperature and gate bias for a range of semiconductor compositions. PTAA-predominant films exhibit a ‘freezing-out’ of charge transport at low temperatures, while diF-TES ADT-predominant films exhibit no saturation of carrier mobility at high temperature and gate bias.

ing films. Unlike the blend films, the pristine films were spin cast from chloroform and hence the film formation took place during the spin coating process as opposed to during the thermal solvent removal in the blend device fabrication. The PTAA film was completely amorphous while the diF-TES ADT film was polycrystalline without the ordered spherulitic growth observed in the optimized blend films.

One immediately obvious feature in the evolution from a pristine PTAA device to an optimized blend device is the increasing efficiency of charge transport at low temperatures. In the pristine PTAA device, charge transport is effectively ‘frozen out’ below temperatures of 180 K. This is in contrast with the 50 wt.% blend and pristine diF-TES ADT devices which exhibit much greater carrier mobilities at these temperatures. The PTAA device exhibits a carrier mobility only 0.6 % of its 320 K value at 130 K, whereas for devices with a complete diF-TES ADT channel, the value is 25%.

The fact that the low temperature device performance is determined by the fraction of the channel composed of crystalline diF-TES ADT most likely arises from the fundamental differences between polymer and small molecule inter-molecular interactions. The molecular packing inherent in the small molecule films enables much greater elec-

tronic overlap between conjugated units on the anthradithiophene backbone of the small molecule, than between conjugated units of the amorphous PTAA molecule. Therefore, charge transport through the amorphous polymer is much more dependent on thermal energy to achieve the necessary orbital overlap between molecules for charge hopping to occur [44].

The second trend that can be observed in Figure 5.4 is that in devices with a diF-TES ADT loading fraction of over 50 wt.% the carrier mobility no longer saturates at high gate bias. This suggests that while carrier mobilities comparable to those exhibited in the 50 wt.% device may be achievable with the higher small molecule fractions, the increased morphological disorder in the films translates to an increased energetic disorder and, as such, a greater density of trap states.

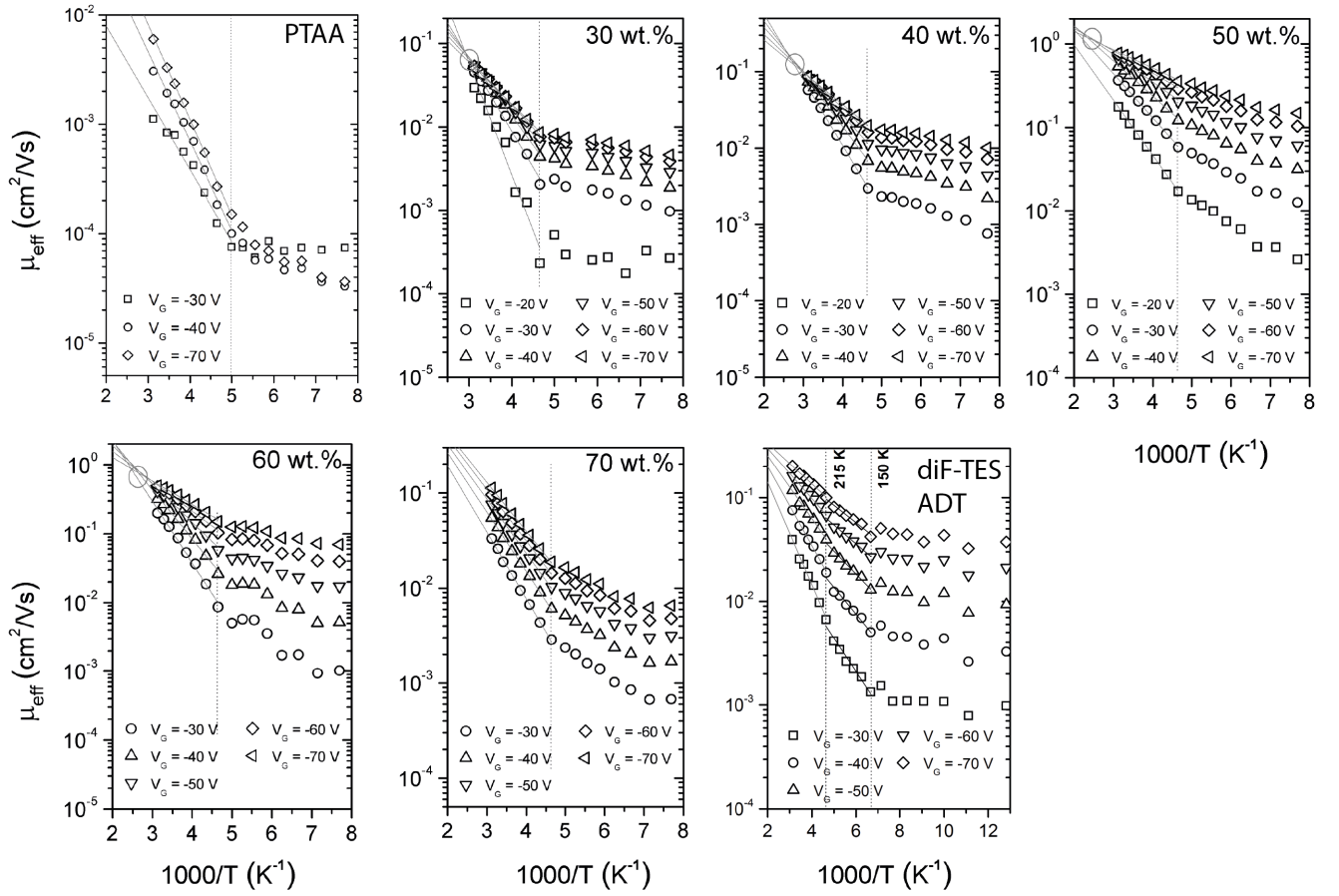


Figure 5.5: Arrhenius plots of hole mobility for blend and pristine TFT devices.

Arrhenius plots of μ_{eff} versus $1/T$ were constructed in order to use the popular MTR and Meyer-Neldel models for describing charge transport in disordered semiconductors (Figure 5.5). This simple analysis does not consider dual exponential trap distributions - separating deep traps from tail states - but averages all the trap states in the band gap. All diF-TES ADT-containing devices exhibited two temperature regimes separated at 210 K, with higher temperature dependence of mobility above this critical temperature. The pristine PTAA device also exhibited a slightly lower critical temperature of 200 K. Finally, diF-TES ADT-rich (> 50 wt.%) devices demonstrated an additional, virtually temperature independent, charge transport regime below 150 K.

The multiple temperature regimes of hole transport exhibited in these devices was also reported by Bourguiga *et al.* in vapour-deposited octithiophene films. The authors attributed the two regimes to conduction being grain-boundary limited at low temperatures, preventing transport between grains [179]. However, the fact that the same two temperature regimes were observed in the amorphous PTAA devices suggests that this is not the origin of the separate regimes in the blend system. Rather, temperature dependence of charge injection at the source/drain contacts could be the limiting factor at temperatures below 215 K, as has been demonstrated previously in organic semiconductor systems [180, 175]. Charge injection into the semiconductor could also be the reason why the 215 K critical temperature becomes less pronounced in blends with decreasing wt.% PTAA, and why an entirely new critical temperature at 150 K arises in the pristine diF-TES ADT device.

It has previously been shown that diF-TES ADT exhibits two phase transitions in the temperature range 175 - 350 K; the first at approximately 205 K, and the second at 300 K [181, 182]. The change in hole transport characteristics either side of 210 K, as demonstrated by diF-TES ADT-containing devices, may be a result of this change in crystal polymorph. However, the field effect hole mobility provides no evidence of the other, high temperature, phase transition which would be visible at $1000/T = 3.3 \text{ K}^{-1}$ (Figure 5.5). It is possible that the third, low-temperature ($< 150 \text{ K}$), charge transport regime in diF-TES ADT-rich devices is evidence of a further diF-TES ADT polymorph,

though this would need to be verified by further differential scanning calorimetry and X-ray diffraction analysis. Additionally this conclusion as to the origin of the transport regimes cannot be supported by the PTAA semiconductor, for which the concept of differing crystal polymorphs does not apply.

Interestingly, the thermal activation of charge transport in the single-component diF-TES ADT TFTs measured in this work (Figure 5.5) is somewhat different to that observed by Ward *et al.* in bottom-gate, bottom-contact diF-TES ADT TFTs on SiO₂ [182]. As in this work, the authors of the study observed different charge transport regimes, which they ascribed to the varying presence of the three crystal polymorphs that they identified. However, the activation energies of these transport regimes are noticeably different to those depicted in Figure 5.5, which are characterised by increasing thermal activation at higher temperatures. By contrast, the authors demonstrate a reduction in the activation energy of hole transport for $T > 280$ K which is explained as evidence for an additional high-temperature polymorph. The differences in the report by Ward *et al.* and the results presented here may be due to the different dielectric-semiconductor interfaces in the two studies. It is possible that the differing interfaces (SiO₂ versus Cytop) impact the diF-TES ADT molecules' mobility at the interface and therefore ability to change polymorph. As a result, the thermal characteristics of charge transport would be impacted.

The Arrhenius plots of Figure 5.5 were used to extract the activation energy for charge transport, E_A , for the different blend ratio and pristine devices. This activation energy is plotted as a function of gate voltage in Figure 5.6. The activation energy of charge transport is noted to decrease at larger gate biases, and is explained through gate-induced trap filling: With the quasi-Fermi level closer to the HOMO level of the semiconductor, the average thermal energy required to promote a carrier into a transport state is decreased.

The pristine PTAA and diF-TES ADT devices exhibit relatively low activation energy of hole transport. At 17 - 40 meV, E_A in pristine diF-TES ADT devices is at the lower end of previous reports on TES ADT and diF-TES ADT films [57, 182]. In the TES ADT study the authors found that for intra-crystallite transport $E_A = 34$ meV; rising to 66 meV for hole transport across high-angle grain boundaries. However, both of these

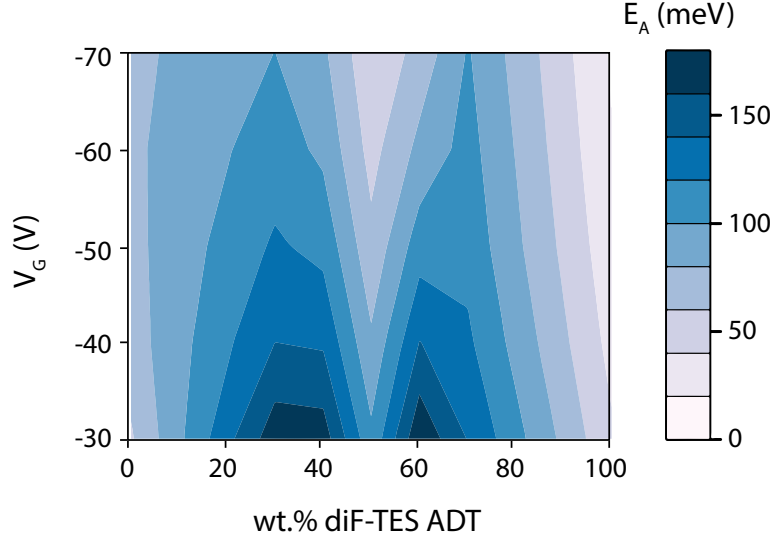


Figure 5.6: Contour map of charge transport activation energy in blend and pristine TFTs as a function of composition and gate bias. Note that for $0 < \text{wt.}\% < 30$ and $70 < \text{wt.}\% < 100$, the values of E_A plotted here are interpolated.

studies were performed on TFTs fabricated using SiO_2 substrates, which is well known for creating additional trapping sites at the TFT interface. As the average crystal size in spin-cast diF-TES ADT films is $10 \mu\text{m}$ (Figure 5.7), compared to a TFT channel length of $30 \mu\text{m}$, the inherent presence of multiple grain boundaries means that it is, however, somewhat surprising that the E_A observed here is so low.

For blend films, however, the story is quite different. TFTs fabricated using unbalanced semiconductor blends exhibit an activation energy that increases sharply at low V_G , becoming strongly carrier-density dependent. This is likely a result of the increased crystal disorder in high wt.% devices and unfavourable charge transport between polymer and small molecule phases in low wt.% devices. Importantly, however, with the blend ratio balanced (i.e. a 50 wt.% blend) the activation energy exists in a local minimum. There still exists a strong gate bias dependence, which is considerably larger than the pristine diF-TES ADT, despite the more disordered microstructure in the pristine semiconductor. This suggests that simply the presence of two material phases, and the transport barriers that exist between them, leads to a strong carrier density dependence of E_A . Despite this, the comparatively low E_A in 50 wt.% blends (especially at large V_G) suggests that

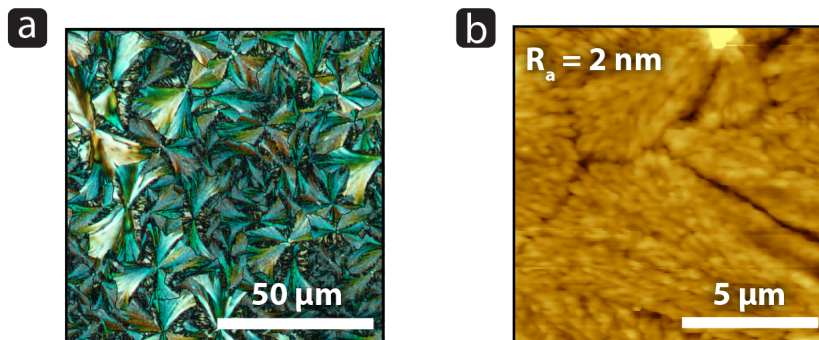


Figure 5.7: Morphology of a spin-cast film of single-component diF-TES ADT. (a) Polarized optical microscope image and (b) an AFM topography map.

the greater ordering of the small molecule in this instance provides a minimum of crystal disorder and grain-boundary transport barriers.

There exists a strong correlation between the film roughness and the activation energy within the blend devices (Figure 5.8). While roughness is simply a feature of the topology of a film, and therefore cannot be used to fully describe the actual crystal microstructure, it acts as a useful metric for quantifying the level of disorder present. Interestingly, the relationship between film roughness and E_A is specific to the blend system, and does not extend to pristine PTAA and diF-TES ADT devices. diF-TES ADT exhibits a comparatively low E_A given the roughness of the film, which highlights the role that the PTAA plays in the creation of charge traps in blend devices. PTAA itself exhibits a comparatively high activation energy.

This analysis shows that while the blending of polymer and small molecule semiconductors can be beneficial to the processing of the high mobility small molecule, the added complexity of the system can in fact be detrimental to device performance if not optimized fully. For example the characteristic trap energy, or the energy required by a molecule to initiate hopping of a charge carrier to a neighbouring molecule, is 43 meV for the optimized blend, but this more than doubles to > 100 meV for the 30 wt.% and 70 wt.% blends.

The fact that all semiconductor compositions (except pristine PTAA) exhibit $E_A =$

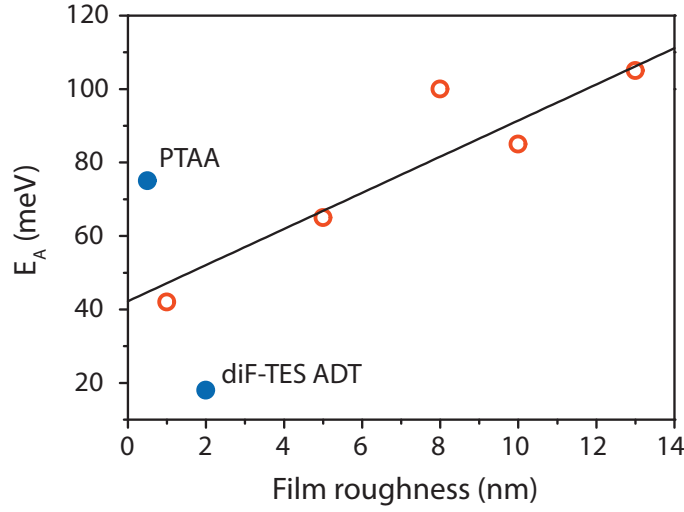


Figure 5.8: The relationship between the roughness of a semiconductor blend film (orange open circles) and the activation energy for charge transport. Added for context are the values for pristine diF-TES ADT and PTAA devices (filled blue circles).

$E_A(V_G)$ demonstrates that (in the high temperature regime - $T > 215$ K) there exists, not a single trap level in these devices, but an exponential distribution of trap states. Therefore, this distribution can be estimated using the Meyer-Neldel rule (MNR), as given by equation 2.3. The pristine PTAA device did not exhibit a temperature dependence of mobility that was, in turn, gate field dependent, i.e. the Arrhenius curves in Figure 5.5 are parallel with increasing gate bias. As such, the temperature and gate bias performance of the PTAA device did not agree with the Meyer-Neldel theory and so the polymer device would be described by a single activation energy of 75 meV [41].

All of the diF-TES ADT-containing devices, however, exhibited a $\ln \mu_0 \propto E_A$ relationship and so obeyed the MNR. The trap distribution width, kT_0 of the blend films in the range 30 - 60 wt.% diF-TES ADT was fairly constant and in the range $25 < kT_0 < 40$ meV, demonstrating little dependence on composition. These values agree with other trap distributions seen in organic semiconductors, as well as other disordered systems such as α -Si and chalcogenide glasses [183, 184, 172, 185, 186]. That inorganic semiconductors exhibit similar trap distributions to those observed in organic systems is quite surprising, given the fundamental differences in the origins of these states.

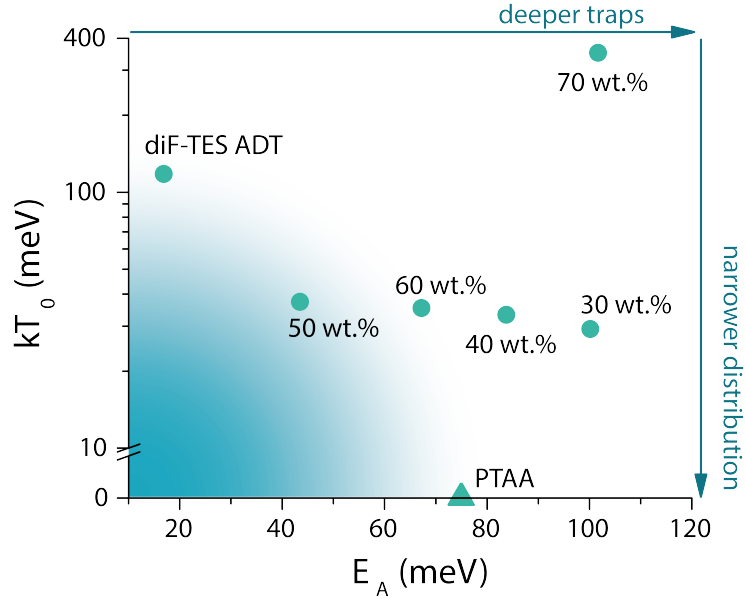


Figure 5.9: Band gap trap distribution versus characteristic trap depth for organic blend and pristine TFTs as calculated using the Meyer Neldel Rule. Shaded is the optimum region of low trap energy and narrow distribution. The PTAA data is added for reference despite not obeying the MNR and therefore not exhibiting a kT_0 value.

Counter to this, however, the pristine diF-TES ADT and 70 wt.% blend device appear to exhibit extremely large trap width distributions, pointing to the severe level of microstructural disorder present in these systems.

The characteristic trap depth and distribution in trap energy of TFTs employing PTAA, diF-TES ADT and blends thereof is illustrated in Figure 5.9. Initially focusing on the pristine semiconductor devices we can see that PTAA films demonstrate an effectively single trap state which is of moderate depth. On the other hand, this analysis suggests that diF-TES ADT films exhibit an extremely low inherent trap depth. Despite this, the fact that films of diF-TES ADT are comprised of a high density of small, unoriented grains leads to a large distribution of these trap states.

It is through balancing these contrasting semiconductors that an improvement on the performance of both can be achieved. The PTAA, used as a binder, controls the crystallisation of the diF-TES ADT, aiding in narrowing the distribution of trap states. However, the small molecule component exhibits a surprisingly low activation energy for

charge transport, and so introducing a polymer phase into the TFT channel unfortunately has the effect of increasing the activation energy for charge transport. As the number of mobile carriers in the TFT channel is dependent on both the depth and distribution of traps, these two parameters must both be minimized in order to improve upon the performance of pristine diF-TES ADT.

Blending the semiconductor components in an even 50 wt.% ratio achieves both an increase in hole mobility and improved subthreshold characteristics, while the 60 wt.% diF-TES ADT blend suffers from slightly deeper traps but a narrower distribution than the diF-TES ADT. As such, the 60 wt.% devices demonstrate reduced subthreshold slope, however do not improve upon the hole mobility of pristine diF-TES ADT devices.

The combination of the MTR model and MNR gives a very simple description of the trap states in a disordered semiconductor, but one that is instructive. However, it does not enable the identification of the origin of trap states, nor does it give a detailed picture of the DOS within the band gap. While it is likely that in the blend system grain boundaries, crystal defects and small molecule-polymer interfaces provide trapping sites, and barriers to transport it is not possible from the analysis conducted above to identify the contributions of each.

5.4 Distribution of tail states and deep traps

5.4.1 Considering the energetic distribution of trap states

The analysis performed in section 5.3 provides a simple insight into the energetics of charge transport in pristine and blend OTFTs. This analysis, however does not consider an energetic distribution of charge traps so much as an average over all states. Further, as the temperature dependence of charge transport is required to extract the activation energy it is not possible to investigate the effect that temperature has on the distribution of charge traps.

The approach proposed by Grünwald *et al.* for estimating the underlying density of

states function allows for a much more detailed appraisal of the trap states in a transistor (section 2.1.3). This section discusses the insights gained by applying this method to the same experimental data used with the activation energy / Meyer-Neldel approaches in section 5.3.

First, however, it is necessary to address the assumptions made by the Grünwald method of DOS analysis and what implications they have on the following analysis. The Grünwald model is based on the multiple trapping and release theory of charge transport and therefore assumes an effective band energy in the semiconductor, with a carrier mobility considerably higher than that of surrounding states. This is an assumption that is widely accepted in the analysis of crystalline organic semiconductors, however the concept of a transport level is also frequently used in the development of models used to describe hopping transport in amorphous materials such as PTAA [44, 187, 188]. The second assumption made by the Grünwald method is homogeneity of the semiconductor both parallel and normal to the TFT interface. However, Figure 5.2 clearly demonstrates that the semiconductor morphology in these polycrystalline films is not homogeneous. As such, this impacts the conclusions that can be made about the nature of grain boundaries and other morphological features using the Grünwald method. Importantly, it also implies that the extracted DOS functions are likely to not be fully representative of the semiconductor under investigation, but will be influenced by the presence and density of features such as grain boundaries in the TFT channel, which may vary between devices.

Shape of the DOS function

The density of states function derived in the Grünwald model (equation 2.9) describes the distribution of tail states in a semiconductor relative to the Fermi level. The Grünwald model itself does not provide an estimate for the position of the Fermi level in the semiconductor, and therefore, in its most basic form, the DOS estimated from the Grünwald model is not anchored to absolute values of either the mobility edge or the Fermi level.

The result of extracting the DOS functions from a 50 wt.% blend device at temperatures ranging from 90 K to 320 K is shown in Figure 5.10. The DOS is plotted on a natural

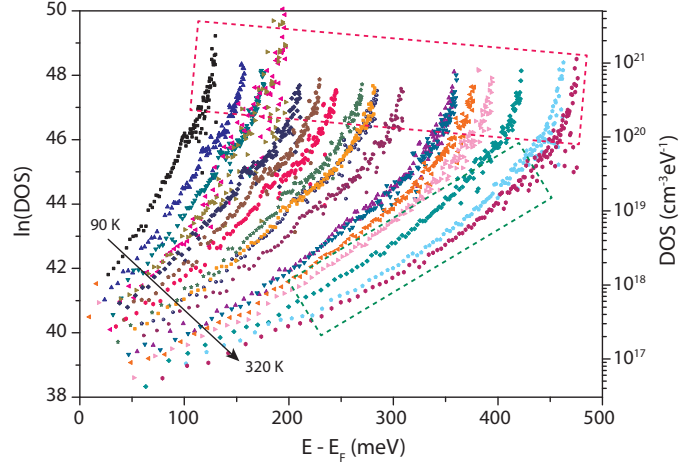


Figure 5.10: Density of states functions of a 50 wt.% blend device, calculated using the Grünwald model, at a range of temperatures. The pink dashed box highlights the region where the model begins to break down, while the green dashed box highlights superexponential characteristics.

log scale against energy relative to the Fermi level. This shows that, for low temperatures in-particular, it is reasonable to model the DOS as exponential functions: The DOS covers 100's meV of the band-gap and spans three orders of magnitude. However, there are two regions of the plot in Figure 5.10 where this conclusion appears incorrect. The first of these is highlighted by the pink dashed box. In this region the DOS function appears to increase superexponentially. However, this may actually be a result of a breakdown in the Grünwald method observed when the quasi-Fermi energy reaches the extended states. In this scenario, the Boltzmann approximation is no longer valid, an assumption integral to the derivation of the Grünwald analysis. Therefore, it can be argued that these states are not physical and therefore can be ignored. The second region where modelling the DOS functions as single exponentials appears to break down is highlighted by the green dashed box in Figure 5.10. At high temperatures (> 250 K) the measured DOS functions extend over 300 - 400 meV within the band gap and begin to exhibit greater than exponential growth, as evidenced by the slight curvature of these data. It is proposed that over such large energy ranges the measured DOS is composed of both tail states and deep states which have different physical origins and therefore there is no reason that the distributions of the tail and deep states should be consistent. In this analysis, the tail states are focused

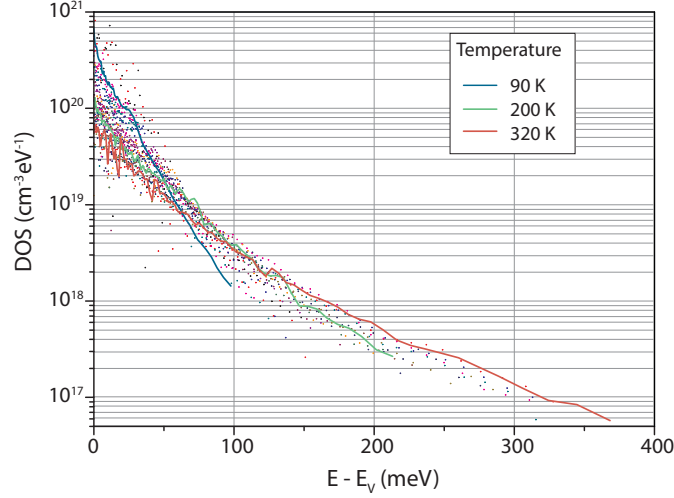


Figure 5.11: Density of states of a 50 wt.% device relative to the mobility edge. DOS functions at temperatures between 90 K and 320 K are plotted as a scatter, while 90 K, 200 K and 320 K data are plotted as lines to highlight the trend of DOS broadening at elevated temperatures.

on and so exponential fits to these high-temperature data will be taken for large $E - E_F$.

To ensure that the DOS function calculated using this method is relevant, it is necessary to either measure the Fermi level (relative to the HOMO energy) or make an assumption as to its position relative to the mobility edge. Smith *et al.* used ultraviolet photoemission spectroscopy (UPS) to calculate the Fermi level in diF-TES ADT:PTAA blend films of 50 wt.%, finding a Fermi level of approximately 0.6 eV, relative to the HOMO [137]. However, UPS is not a particularly precise technique, and an uncertainty of 0.1 - 0.15 eV is inherent to the measurement [189]. This uncertainty arises due to the experimental nature of illuminating the sample and interfacial interactions of the semiconductor with metals or other organic layers.

In this work a different approach is taken. As discussed above, the breakdown of the Grünwald method for large $E - E_F$ suggests pinning of the quasi-Fermi level at (or very close to) the mobility edge and the onset of the extended states. As such, the data may be aligned about this position to provide a description of the DOS as a function of energy from the mobility edge, and temperature. The result of aligning the DOS functions in this manner is shown for the case of a 50 wt.% blend device in Figure 5.11.

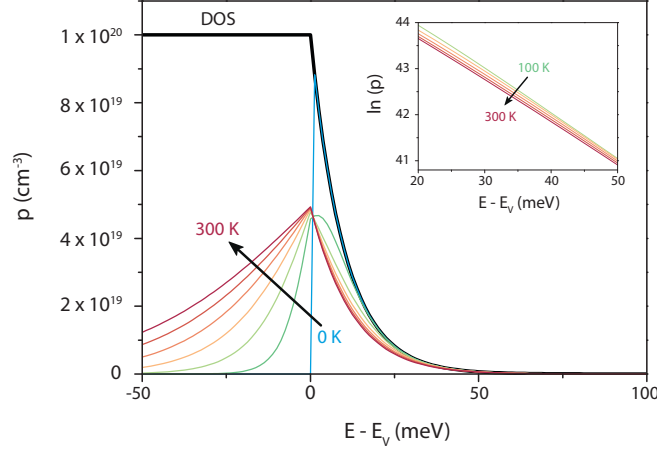


Figure 5.12: Distribution of accumulated holes with the quasi-Fermi level at the valence band edge (E_V). Increased temperature leads to a broader distribution of holes, however on a $\ln$ scale (inset) the broadening within the band-gap is negligible between 100 and 300 K.

Once aligned, the evolution of the DOS with increasing temperature becomes clear. At low temperature the DOS is characterised by a large density of trap states at the mobility edge which decays sharply into the band gap. As temperature increases the density of tail states at the mobility edge appears to decrease and the distribution broadens. This change is greatest between 90 K and 200 K; above ~ 250 K thermal DOS broadening ceases.

At this point it is important to determine whether this apparent thermal broadening of tail states is physical or an artefact of modelling. The Grünwald model makes the zero-temperature approximation when deconvoluting the DOS function from the hole density (Section 2.1.3). In practical measurements the temperature is never 0 K and indeed in the work here, the point is to examine the DOS across a range of temperatures. To examine the effect of temperature-dependent Fermi statistics, and to determine whether the apparent DOS broadening is just a result of this, a hole density function ($p(E, T)$) was simulated by convoluting the Fermi function with an arbitrary exponential DOS. The hypothetical DOS function was chosen to be similar to that seen in the semiconductors measured here and characterised by $N_0 = 10^{20} \text{ cm}^{-3} \text{ eV}^{-1}$ and $E_0 = 10 \text{ meV}$ (which, as will be seen, is similar to the estimated $T = 0 \text{ K}$ characteristic energy in these semiconductors). The resulting hole

density functions, with the quasi-Fermi level at the valence band, are plotted on a linear scale in Figure 5.12. Clearly, increasing temperature broadens this distribution of hole states as would be expected. By using a $T = 0$ K approximation in deconvoluting these functions the extracted DOS function would be broader than the actual DOS, especially at elevated temperature. This suggests that thermal effects on Fermi statistics could be the cause of the apparent DOS broadening. In reality, however, the hole density characteristic energy $E_{p,0}$ broadens by only 10 % between 50 and 300 K, and only does so very close to the mobility edge. As is shown in the next section E_0 at high temperature can be as much as $3\times$ that at 100 K. Therefore such it can be concluded that the observed thermal broadening of tail states is physical after-all.

Density of states in TFTs of varying composition

The density of trap states, at 290 K, for all the semiconductor compositions studied here are presented in Figure 5.13. Devices containing a high fraction of diF-TES ADT (specifically the 70 wt.% blend and the pristine device) exhibit an increased density of trap states across the spectrum compared to other blend devices. This is likely caused by the more disordered microstructure exhibited by these two semiconductor thin-films (Figures 5.2 and 5.7). The characteristic trap energy, E_0 , of the diF-TES ADT-containing devices appears broadly composition-independent at 290 K, and greater than that exhibited by the PTAA device. At this temperature the characteristic trap energy is ~ 40 meV for diF-TES ADT-saturated blends and ~ 20 meV for the PTAA film. These values are comparable to other reports of tail state distributions in disordered semiconductors. The PTAA DOS has a large density of tail states at the mobility edge ($> 10^{20} \text{ cm}^{-3}\text{eV}^{-1}$) which decays at a greater rate than any of the diF-TES ADT-containing devices within the tail state region (< 150 meV). For $E - E_V > 150$ meV the decay rate appears approximately consistent across all devices.

With a maximum density of tail states between 4×10^{19} and $3 \times 10^{20} \text{ cm}^{-3}\text{eV}^{-1}$, the devices studied in this work exhibit magnitudes of trap states consistent with solution processed OTFTs (and, indeed, *a*-Si TFTs) described in the literature [173, 38].

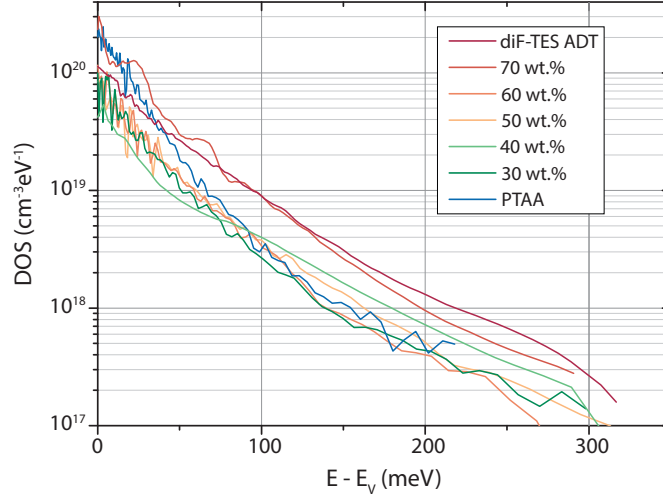


Figure 5.13: Density of band gap states in blend and pristine semiconductors at 290 K, relative to the mobility edge.

TFTs of all blend compositions (including pristine semiconductor) exhibit a DOS function that is, to varying degrees, temperature dependent; similar to that observed in the data plotted in Figure 5.11. This is most clearly tracked through the temperature dependence of the characteristic trap energy, E_0 . Temperature dependence of the tail state distribution has previously been described in amorphous oxide semiconductors [190]. The DOS at the mobility edge also decreases with increasing temperature, however N_0 is also highly dependent on the actual position of the DOS relative to the mobility edge, and as this is very difficult to estimate, this parameter is not studied in depth. To extract E_0 exponential fits were made to the DOS functions of all semiconductor compositions, with operating temperatures ranging from 90 K to 320 K; these fits are shown in Appendix C.

Figure 5.14 plots E_0 for all the semiconductor compositions studied here, as a function of temperature. Several interesting trends become immediately apparent. Firstly, the rate of thermal DOS broadening at temperatures below 225 K is consistent among all diF-TES ADT-containing devices, and significantly different to that of PTAA (orange dashed box, Figure 5.14). For diF-TES ADT-containing devices operating at < 225 K the adjusted r^2 coefficient for E_0 with T as the predictor is 0.68, or equivalently, 68 % of the variance in the width of tail states in this temperature range can be ascribed to temperature variation.

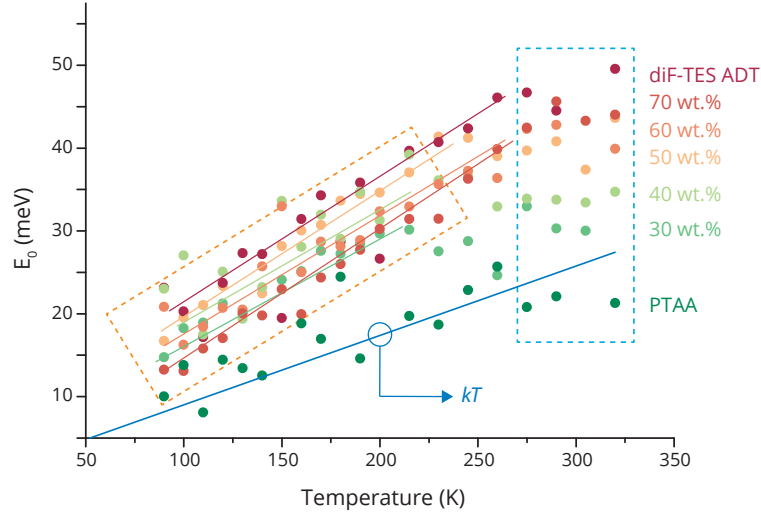


Figure 5.14: Characteristic trap depth of blend and pristine semiconductor thin-films as a function of temperature and semiconductor composition. The dashed orange box highlights the similarities between the thermal broadening of diF-TES ADT-containing devices at low temperature and the blue dashed box highlights the constant high-temperature characteristic energies of the semiconductor films. Thermal energy, kT , is added for reference.

Interestingly, the variance in the composition-specific data is much better described by the operating temperature than the population of diF-TES ADT-containing devices as a whole. The mean r^2 value for linear regressions performed on composition-specific data was 0.8, with $r^2 > 0.95$ for the 30, 50 and 70 wt.% blends, compared to $r^2 = 0.68$ for the population. Despite the excellent linear fit to the composition-specific data the wt.% diF-TES ADT does not act as a predictor for the population E_0 (as verified by multiple regression analysis). This means that the remaining 32 % of population variance in E_0 is expected to be due to a combination of errors in estimating E_0 , systematic errors in the extraction of the DOS function from transfer curves, and other underlying relationships that are not resolved by this analysis, rather than the specific composition or morphology of the semiconductor film itself. Therefore, morphology of the diF-TES ADT semiconductor layer plays a smaller role in the low-temperature thermal characteristics of tail states than simply the presence of the material (compared to pristine PTAA).

Down to low temperature the characteristic trap energy of pristine PTAA is approximately equal to kT , and at high temperatures is $< kT$. This suggests that hole

conduction in the PTAA semiconductor does not satisfy the assumption that transport is trap-limited. Rather, the equivalence of kT and E_0 suggests that the number of carriers trapped in tail states is comparable to the number of free carriers. This is not the case in diF-TES ADT-containing blends and pristine films, where $E_0 > kT$ implies that charge transport is trap-limited at all temperatures.

An interesting result from this analysis concerns the evolution of tail states in 30 and 40 wt.% blends with temperature. At low- T the 30 wt.% blend DOS resembles the semiconductor blends with a higher saturation of diF-TES ADT despite only $\sim 40\%$ of the film surface being covered by crystalline diF-TES ADT. That the DOS more closely represents the diF-TES ADT-saturated blends than the pristine PTAA points to the freezing-out of hole conduction through the polymer/mixed phase for $T < 230$ K. This conclusion is supported by the observation made in Section 5.3 that hole conductivity is significantly suppressed in devices with low or zero diF-TES ADT content at low temperature. At high temperatures, however, the characteristic tail state energy (at ~ 30 meV) lies between that exhibited by the PTAA (~ 20 meV) and the diF-TES ADT-saturated films ($\sim 40 - 45$ meV), suggesting that for high temperatures the polymer/mixed phase plays a non-negligible role in the conduction of holes, causing the measured DOS to include contributions from both crystalline and amorphous semiconductor phases.

As described, above a certain critical temperature, E_0 plateaus (blue dashed box, Figure 5.14). This high-temperature characteristic energy is a function of the semiconductor composition, with more diF-TES ADT-saturated films exhibiting a broader tail state distribution. This relationship is shown in Figure 5.15 and exhibits a broad sigmoidal relationship. A sigmoidal fit to the data, fixing the upper and lower bounds at the diF-TES ADT and PTAA values of E_0 , results in the following model:

$$E_0(\rho) = E_{0,\text{diF-T}} - \frac{E_{0,\text{diF-T}} - E_{0,\text{PTAA}}}{1 + \exp\left(\frac{\rho - \rho_0}{d\rho}\right)} \quad (5.1)$$

where ρ is the weight-percentage diF-TES ADT in the blend, ρ_0 is the critical composition, and $d\rho$ is the rate of change between the upper and lower states. Performing

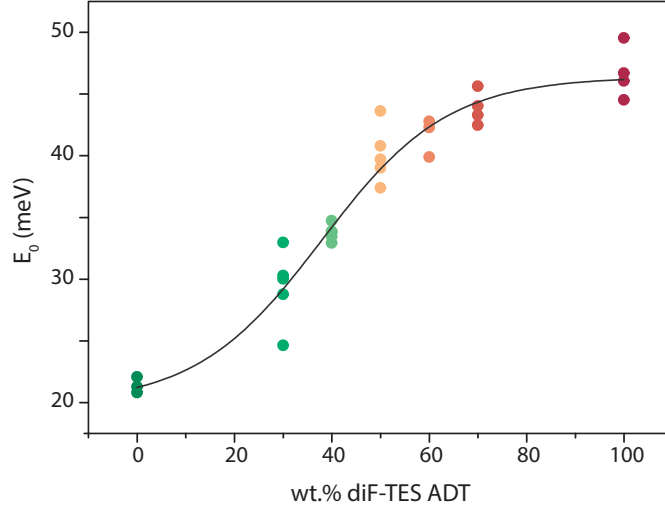


Figure 5.15: Evolution of the high-temperature DOS distribution with blend composition. The characteristic trap energy is plotted as a function of semiconductor composition and fitted with a sigmoid function.

the fit returns the following parameters: $E_{0,\text{diF-T}} = 46$ meV, $E_{0,\text{PTAA}} = 21$ meV, $d\rho = 12$ wt.% and $\rho_0 = 39$ wt.%. Interestingly, the critical composition of this sigmoidal function is identical to that found by Smith *et al.* when modelling the hole mobility in this blend system with a sigmoidal function [59]. Contrastingly, however, the modulation in carrier mobility occurs at a much greater rate than that of E_0 , with $d\rho = 2$ wt.%. Whereas the modulation in the hole mobility of blend TFTs is controlled by the formation of percolation pathways, the modulation of the high-temperature DOS distribution appears to be less dependent on the binary presence of percolation pathways, than the gradual evolution of the blend film morphology.

It is not surprising that the crystalline semiconductor films exhibit greater thermal broadening of their DOS; this has been demonstrated widely in inorganic semiconductors [50, 191, 192]. Unfortunately, there has been limited work on quantifying the DOS in amorphous organic semiconductors and so evidence remains sparse [193].

However, the above analysis doesn't cover the whole story. Rather than the DOS simply becoming temperature-independent at high-temperatures, a distribution of deep trap states emerges with a characteristic energy significantly greater than that of the tail

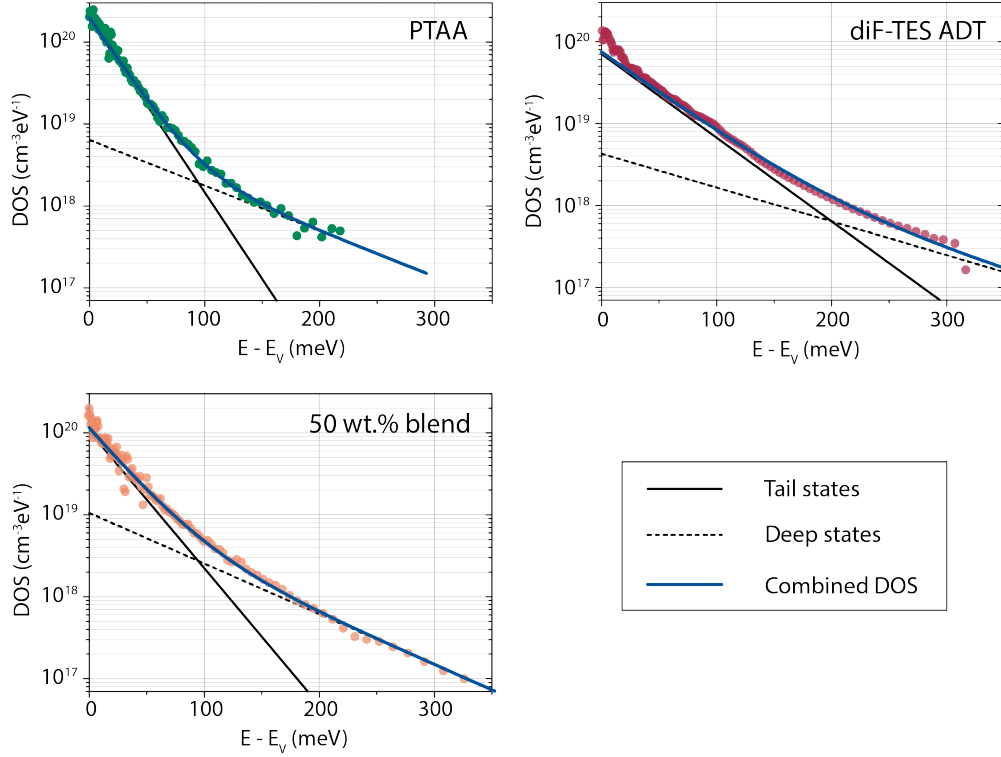


Figure 5.16: Modelled DOS functions of PTAA, diF-TES ADT and 50 wt.% blend TFTs as a sum of separate exponential tail and deep state distributions shown along with experimental data. Data shown was measured at 290 K.

states (5.11). Whereas at low temperatures the quasi-Fermi level only explores ~ 100 meV of the band-gap (the tail states), at 290 K the quasi-Fermi level at flat-band exists > 200 meV from the mobility edge and hence the measured DOS covers both deep and tail states.

Figure 5.16 demonstrates how, at high-temperature, the density of states functions of the blend and pristine semiconductors studied in this work can accurately be described as a sum of separate tail and deep state distributions. Modelling the DOS functions in this way estimates a deep trap characteristic energy of $80 (\pm 10)$ meV which is independent of semiconductor blend composition and is also consistent with that observed in PTAA. The pristine diF-TES ADT provides a deep trap characteristic energy estimate of 100 meV, however (as can be seen in Figure 5.16) only a small region of the DOS is governed by the deep states, making this estimate vulnerable to error. In addition, the magnitude of deep

trap states shows no significant dependence on semiconductor composition. Together, these observations suggest that the origin of deep traps in these devices share the same origin.

5.5 The origin of trap states in blend transistors

The origin of trap states in disordered semiconductors is generally attributed to chemical impurities, structural defects and small-scale fluctuations of molecular conformation. In addition, the dielectric has also been demonstrated to hold the potential of dramatically increasing the density of trap states at the semiconductor interface due to the presence of certain chemical groups [96, 194]. Small-scale fluctuations of molecular packing give rise to the exponential DOS that is inherent in all organic semiconductor systems, including single crystals. On the other hand, chemical impurities and larger structural defects lead to the creation of deep trap states and may give rise to peaks in the DOS at specific energies.

The TFTs fabricated in this study all employ the fluoropolymer Cytop as the dielectric layer. It has previously been shown that Cytop introduces minimal energetic disorder and trapping sites to the semiconductor interface; this a result of its low dielectric constant and hydrophobic nature [84, 83, 144]. As such, it can be assumed that the majority of the traps in (and the variation observed between) the blend and pristine devices are a result of the semiconductor film itself.

At low temperatures (~ 100 K) the tail state distribution width drops to 10 - 20 meV across all semiconductor compositions studied in this chapter. Interestingly, this is close to the tail state distribution measured at low temperature in single crystal rubrene, which was shown to exhibit $E_0 = 11$ meV [195]. In fact even at high temperature, the tail state distributions of single crystal rubrene and poly(3-hexylthiophene) films have been shown to be very similar in the shallow trap region, with characteristic tail state energies around 35 meV in both cases and very similar to the values observed in the blend and single-component films studied here [66]. This suggests that the origin of tail states

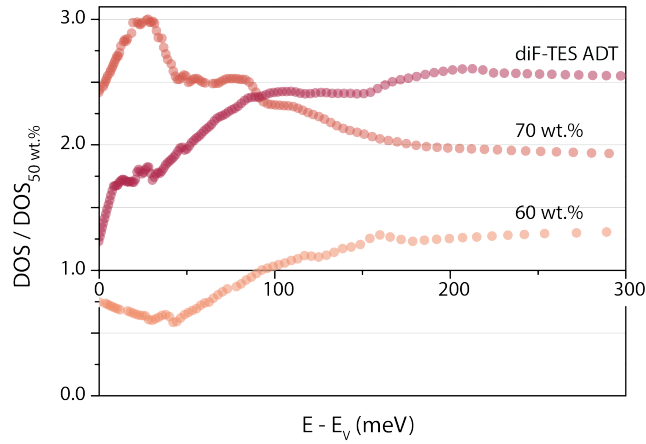


Figure 5.17: Density of states in high-wt.% diF-TES ADT films, as multiples of the 50 wt.% blend.

may in-fact be similar in both single crystal and solution-processed semiconductors. The reason for the considerable performance difference between transistors fabricated using each of these two processing methods is a matter of scale. Whereas solution-processed semiconductors typically exhibit tail state densities on the order of $10^{21} \text{ cm}^{-3} \text{ eV}^{-1}$, single crystals exhibit densities 100 - 1000 $\times$ less than this and an almost complete absence of deep traps [195, 173].

In crystalline organic semiconductors it has been shown that variation in molecular alignment of up to 2.5 Å along the long axis of the molecule leads to the creation of hole and electron traps up to a depth of 100 meV [62]. While not breaking the 2D crystal structure, this disorder would be responsible for the underlying shape of the tail DOS in the blend system at low temperature. This explanation is also consistent with the broadening of the DOS with increasing temperature, as greater kinetic energy of diF-TES ADT molecules leads to greater disorder and strain between adjacent molecules in the crystal. Furthermore, the fact that the PTAA film exhibited minimal thermal broadening of the DOS also supports this theory, due to the lack of inter-molecular structure in amorphous polymer films.

At high temperatures increasing the thermal energy of the semiconductor has no

further effect on the distribution of tail states, suggesting that the maximum vibrational disorder has been reached. This appears to occur in the temperature region of 200 - 250 K, or equivalently, at a thermal energy of between 17 and 22 meV.

Figure 5.17 depicts the density of tail and deep trap states in the > 50 wt.% blend films, relative to that of the optimum 50 wt.% blend. The increasing morphological disorder exhibited by these films clearly affects not only the field-effect hole mobility in devices using these semiconductor compositions (Figure 5.1a), but also the density of trap states in the semiconductor. The 60 wt.% blend film exhibits a density of deep traps no more than 25 % greater than that exhibited by the 50 wt.% blend. Instructively, the morphological disorder is only slightly greater in these films than in the 50 wt.% blend. Contrastingly, however, the 70 wt.% and pristine diF-TES ADT films exhibit deep trap densities 2 - $2.5\times$ greater than that exhibited by the 50 wt.% blend across the spectrum of trap states.

The additional charge traps shown in Figure 5.17 manifest themselves in the subthreshold characteristics of the TFTs they inhabit. The quasi-Fermi level fills deep traps (> 100 meV) with a gate bias of approximately -20 V for the 50 wt.% devices, yet the devices with a higher diF-TES ADT content require a gate bias of approximately -28 V to fill these extra trap states. As such, the subthreshold swing in the higher-concentration-diF-TES ADT blend devices increases from < 4 V/dec in the 50 wt.% devices to over 6 V/dec in pristine diF-TES ADT devices (Figure 5.18).

One assumption that is made by the Gr̈unewald method is that the semiconductor is homogeneous both normal and parallel to the TFT interface. Clearly, features such as grain boundaries do not satisfy this assumption. As such, one limitation to this analysis is that it is not possible to suggest possible trap depths of the specific morphological features observed in Figure 5.2, nor is it possible to draw specific conclusions about the differences in the energetic landscape of the amorphous and crystalline phases observed in 30 wt.% and 40 wt.% blends.

In PTAA-rich films traps must originate through different phenomena to the crystal defects, grain boundaries and thermal broadening of the crystalline films. Indeed, given that charge transport in amorphous polymers is commonly described as occurring through

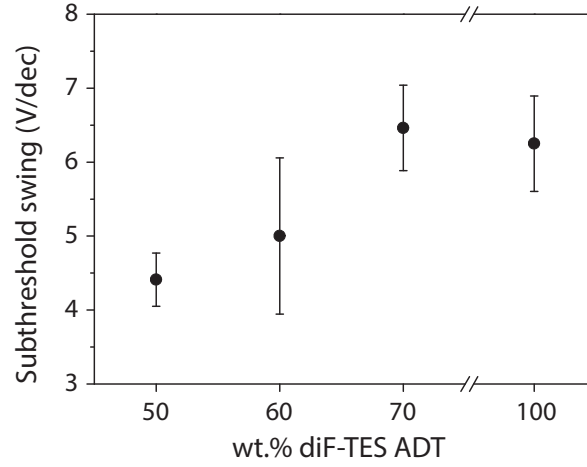


Figure 5.18: Subthreshold swing measured in the saturation regime of TFTs fabricated from a range of diF-TES ADT-rich semiconductor compositions.

thermally assisted hops of carriers between localized states, it is difficult to conceptualise an energy state that isn't a trap. Instead, the disordered nature of the semiconductor presents many states that all offer slightly different charge transfer integrals for hopping. In contrast to the other semiconductor compositions, the pristine PTAA fully satisfies the assumption of homogeneity used by the Gr unewald method. As such, the trap distributions measured in this section are expected to accurately describe PTAA as a material, rather than a convolution of intrinsic states and states originating from morphological features.

5.6 Comparison of models and conclusions

The analyses described in sections 5.3 and 5.4 come from quite different starting points, though definite similarities exist. Section 5.3 considered hole transport in the blend and pristine devices as a thermally activated phenomenon with a characteristic activation energy, E_A , that was a function of gate bias. The activation energy can be thought of as an average trap depth and the gate bias dependence on this due to the quasi-Fermi level moving through an exponential density of states in the band-gap. This DOS itself is characterised by a distribution width, kT_0 , which is estimated from Arrhenius plots of the carrier mobility.

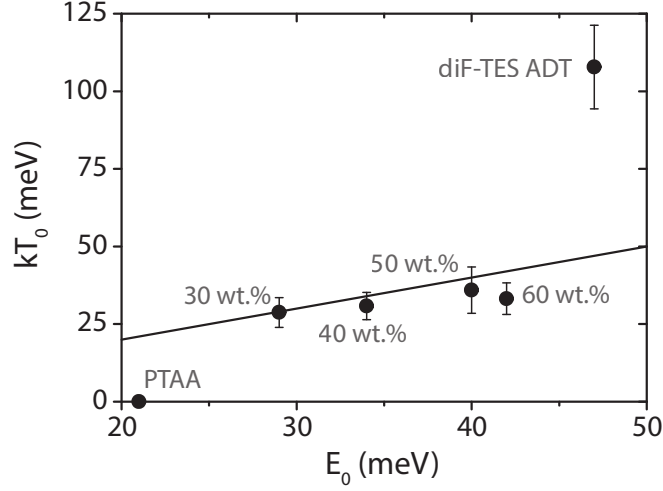


Figure 5.19: Comparison of tail state distributions estimated using the Meyer-Neldel Rule (kT_0) and the Grünwald method (E_0). $kT_0 = E_0$ (i.e. perfect correlation) is also plotted for reference. The 70 wt.% estimate of kT_0 is not shown as it is too large for the y axis, at > 300 meV.

In many ways this approach is superficially similar to the Grünwald approach. Contrastingly, however, the method (described in section 5.4) extracts the interfacial electrical potential in the TFT from a single transfer curve and uses this to calculate a spectral function of band-gap states. By fitting exponential or dual exponential functions to this the mobility-edge trap density, N_0 , and DOS function width, E_0 , can be extracted both from a single $I - V$ curve and as a function of temperature by performing a range of measurements.

Therefore, kT_0 , extracted from the Meyer-Neldel rule, and E_0 would be expected to return similar values and are plotted in Figure 5.19. The closest agreement between kT_0 and E_0 is achieved when the high-T mean value of E_0 is used and this is shown here. While the two analyses agree relatively well on the distribution of trap states in blend ratios of 30 wt.% to 60 wt.% diF-TES ADT, for the 70 wt.% diF-TES ADT blend and pristine devices the results diverge to a huge degree. Given the extremely high values in the cases of diF-TES ADT and 70 wt.%, it is likely that these result from limitations in the method of extracting kT_0 .

It is apparent that kT_0 is vastly overstated when the effective carrier mobility does

not saturate in the range of gate field investigated (Figure 5.4), and therefore the complete distribution of tail states is not explored. Due to the $1/T$ Arrhenius relationship, small errors in the isothermal temperature can lead to large errors in kT_0 . Conversely, when there is little influence of the gate field on the thermal activation of charge transport (as seen in the PTAA TFT, Figure 5.5), it is not possible to estimate kT_0 . Therefore, it is assumed that the system does not obey the MNR and instead can be considered as having a single trap energy. This is clearly a gross simplification (given the highly disordered nature of the semiconductor), and in reality any trap distribution width below ~ 25 meV becomes very difficult to estimate using the MNR. However, this is not a failing of the approach as such; as the Grünwald method showed, the distribution of tail states in the PTAA was indeed very shallow and comparable to kT at all temperatures. In this aspect both models return the same conclusion.

It is clear, however, that use of an activation energy-approach is a much less precise method of probing band-gap tail states in disordered semiconductors than the method laid out by Grünwald. The Grünwald analysis further quantifies the density of tail states as a function of energy, rather than simply providing an estimate of their distribution. This resolves tail states from deep trap states and enables a much more intuitive understanding of the distribution of band-gap states and their temperature-dependence. Despite this, the Grünwald method is not free from short-comings. While few in number, the assumptions of homogeneity of the semiconductor and the ambiguity of dealing with both charge transport mechanisms present in crystalline and amorphous materials place limitations on the conclusions that may be drawn. Additionally, the Grünwald method provides no anchoring of the DOS function to the mobility edge, making the positioning of these functions, and N_0 subject to interpretation. Ultimately, the blend system is extremely complex and the Grünwald method of DOS analysis was certainly not devised with this materials system in mind. For a more comprehensive analysis of the gap states in blend semiconductors the models presented in this chapter need extending to account for the peculiarities of this specific materials system, including the polycrystalline microstructure and the presence of multiple material phases.

Chapter 6

Environmental and electrical stability of the blend system

6.1 Introduction

Achieving high charge carrier mobilities and acceptable sub-threshold characteristics is, unfortunately, not a sufficient requirement for the application of OTFT technology in the majority of next generation electronics applications. Not only must OTFTs remain unaffected by exposure to moderate atmospheric humidity and elevated temperatures, they must also do so while providing high current densities for prolonged periods of time. While the shelf-life and resilience to periodic gate biases of current OTFT technology is sufficient to enable employment in devices such as electrophoretic displays, pushing beyond this into the requirements of OLED displays has not yet been achieved commercially. The most common device degradation characteristic under the extended application of a gate bias is the reduction in current that the device is able to provide in its ‘on’ state. The consequence of this instability when applied to an OLED pixel would be that the light intensity provided by the pixel would fade over time, something that would be unacceptable from a commercial standpoint.

In this chapter the operational stability of high performance 50 wt.% blend devices

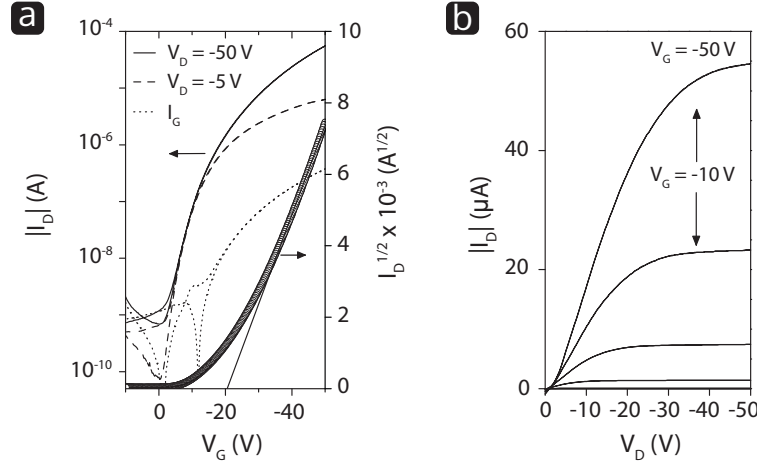


Figure 6.1: Transfer **(a)** and output **(b)** curves of a typical high performing blend-OTFT device.

employing a Cytop dielectric is investigated. Two operation regimes are tested, firstly the prolonged application of a gate bias to the device, and secondly driving a high current through the device for extended periods of time. In addition, atmospheric factors such as stressing the devices in ambient conditions and, separately, at high temperatures is investigated. This is important as most literature reports ignore performance in these critical situations. Overall the blend devices studied here performed well in comparison to the majority of literature reports, however interesting instability characteristics were highlighted when stressing in ambient conditions and at elevated temperatures.

6.2 Constant gate bias stress

6.2.1 Bias stressing under inert conditions

Prior to stressing, the fabricated TFTs were tested for high performance (the requirements chosen to be $\mu > 1 \text{ cm}^2/\text{Vs}$, $I_{\text{off}} < 10^{-8} \text{ A}$, indicating low leakage current). Typical electronic performance of a well-performing device is shown in Figure 6.1. Such a device, with large grain microstructure of the diF-TES ADT component, was stressed in the dark in an N_2 atmosphere with a constant gate bias of -50 V for $3 \times 10^5 \text{ s}$, or three and a half

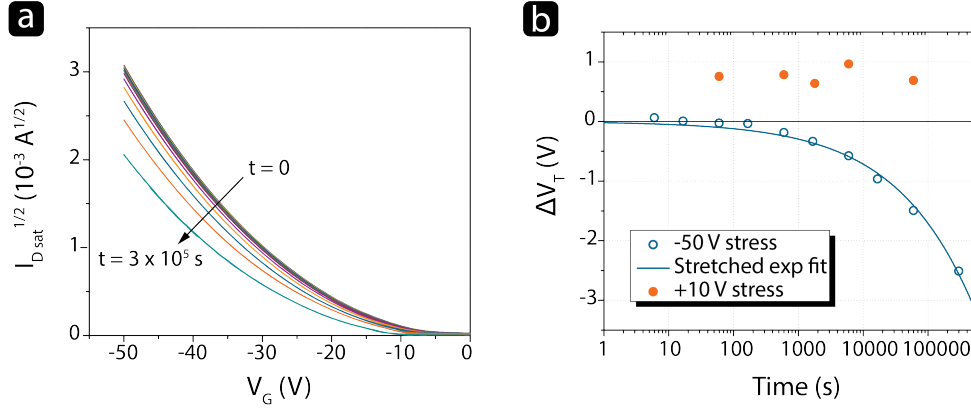


Figure 6.2: **(a)** Time evolution of transfer characteristics under gate stressing. **(b)** Time evolution of threshold voltage under bias stressing. Overlaid is a stretched exponential fit to the data.

days. Stressing was conducted in the dark to eliminate the process of de-trapping of holes by the absorption of photons.

The time evolution of transfer characteristics measured in the saturation regime are shown in Figure 6.2a. A negative shift in the curve is observed, while the shape of the curve remains constant. This shows that while charge trapping is occurring, the conductivity of the channel is not changing, thus suggesting that the process should be reversible. In Figure 6.2b the threshold voltage is plotted as a function of time on a semi-log plot. We observe that after $3 \times 10^5 s$ (3.5 days) a modest threshold voltage shift of -2.5 V has occurred, which is 5 % of the applied gate voltage. This stability is excellent and compares well with the devices reported by Umeda *et al.* which used pentacene in conjunction with a Cytop dielectric and, as far as I am aware, is the best performing system for OTFTs in the literature [83]. The result of stressing a device with a positive gate bias is also shown in Figure 6.2b. A quick, positive ΔV_T is seen which appears to remain constant with time.

Figure 6.3 shows the transfer characteristics of this device before and after stressing. The stressed curve shows a drop in current consistent with its change in V_T , however the shape of the curve remains the same and, as such, the hole mobility is unchanged. Interestingly, the ‘off’ current drops by an order of magnitude. This is tentatively attributed

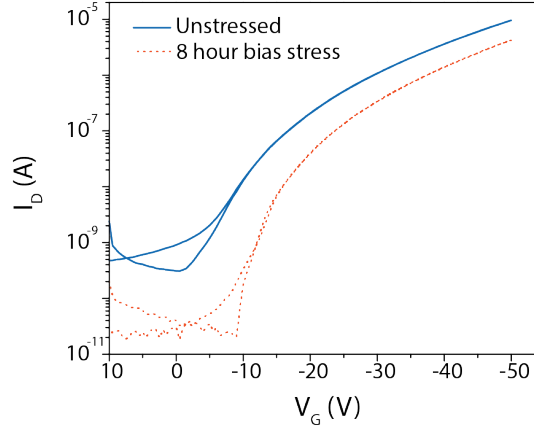


Figure 6.3: Transfer characteristics of a device pre and post bias stressing with a gate voltage of -50 V.

to the trapping of mobile carriers present in the diF-TES ADT bulk, thus reducing the ‘off’ conductivity.

Devices were fabricated using a single semiconductor component to gain an insight to how electrically stable both the PTAA and diF-TES ADT are when implemented alone. The device structure used was the same TGBC architecture with Cytop dielectric and as such any variations in the stressing behaviour should be entirely due to differences in the semiconductor layer and the semiconductor-insulator interface. The results are shown in Figure 6.4. Firstly comparing the blend devices exhibiting small grain and large grain microstructures (micrographs of which are shown in Figure 6.4a), we see that the small grain blend appears less stable than the large grain equivalent. This could be attributed to the higher density of grain boundaries in the small grain film providing increased trapping sites for charge carriers, as was suggested by Jaquith *et al.* [92]. Comparing the individual components we can see that PTAA stresses over shorter time-scales than does the diF-TES ADT.

Explaining the differences and similarities in stressing characteristics between the single component and blend devices is more difficult. Due to the sharp phase separation of the polymer and small molecule components during the processing of blend films it is reasonable to expect there to be little PTAA present in the transistor channel. There-

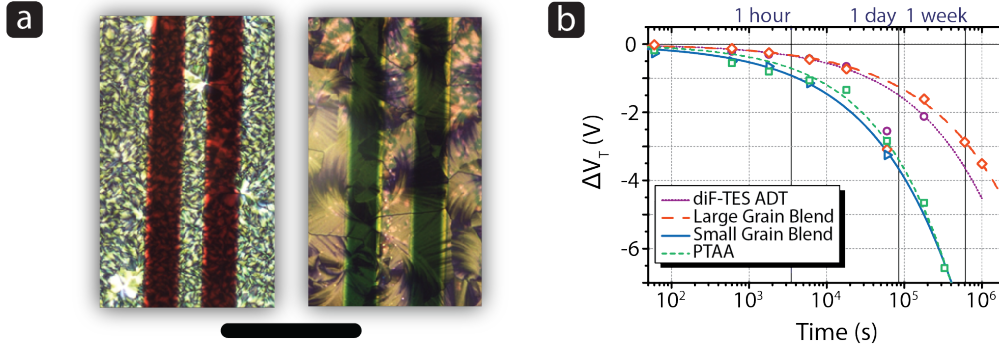


Figure 6.4: **(a)** Polarized optical micrographs of the blend transistors stressed for the data in **(b)**, showing small grain (left) and large grain (right) morphologies. The scale bar represents $200\ \mu\text{m}$. **(b)** Time evolution of threshold voltage shift for different blend morphologies and individual semiconductor devices. Stretched exponential fits are overlaid onto the data.

fore, it would be easy to come to the conclusion that stressing characteristics of the small grain blend should be similar to that of the diF-TES ADT device, given their similar morphologies (compare Figures 6.4a and 5.7). However, this conclusion is not supported by the evidence in Figure 6.4b where the diF-TES ADT device is observed to exhibit stressing characteristics closer to that of the large grain blend. It is therefore hypothesized that the measured bias stability is not due to morphology alone, but rather chemical composition must be more carefully considered. In earlier work it has been shown that the grain boundaries in blend devices are unique, and that a mixed phase may exist in these regions, with the PTAA phase potentially bridging adjacent diF-TES ADT spherulites [61, 57]. The presence of PTAA in the grain boundaries could therefore provide additional trapping sites, leading to greater gate-bias instability in films with a higher density of grain boundaries. This may explain why a greater V_T shift is observed in blend devices rather than pristine diF-TES ADT devices, despite their apparently similar morphology.

Figures 6.2b and 6.4 demonstrate that stretched exponential functions accurately describe the temporal dependence of bias stressing in the TFTs tested here. By fitting equation 2.19 to the bias stress data the stress relaxation constant, τ , and exponential dispersion parameter, β , can be extracted. These values are stated along with others stated in the literature in Table 6.1. What this comparison tells us is that the blend

6.2. Constant gate bias stress

Semiconductor	Dielectric	Temp. (°C)	τ (s)	β	Reference
PTAA	SiO ₂	30	1×10^7	0.32	[82]
PTAA	SiO ₂	140	2×10^4	0.44	[82]
P3HT	SiO ₂	30	4×10^7	–	[82]
Pentacene	SiO ₂	–	3.6×10^4	0.28	[85]
Pentacene	Polyimide	–15 → 70	4×10^2	0.35	[196]
diF-TES ADT:PTAA	Cytop	25	2×10^8	0.43	This study
diF-TES ADT	Cytop	25	6×10^7	0.47	”
PTAA	Cytop	25	9×10^6	0.50	”
<i>a</i> -Si	SiO ₂ /SiN _x		8×10^7		[82]
μ c-Si	SiO ₂ /SiN _x		1×10^{12}		[82]

Table 6.1: Stress parameters for OTFTs fabricated from a range of semiconductors and dielectrics

system produces some of the most stable devices on record. With $\tau = 2 \times 10^8$ s the devices stress slower than any other OTFT and slower than *a*-Si. It is true that a slow rate of threshold voltage shift does not guarantee device stability - ideally the device should recover quickly as well - but these results are promising none-the-less. β values, which are governed by the trap energy distribution, are also given in Table 6.1. The higher β values for the devices described in this study compared to those in the literature suggest a tighter distribution of trap energies and as this is seen across devices fabricated using a range of semiconductors it further suggests that this could be due to the Cytop dielectric having minimal influence on the stressing characteristics. Conversely, for devices on SiO₂ dielectrics, modifying the interface with a SAM layer has been shown to reduce β , introducing a broader distribution of traps [96, 95].

6.2.2 Bias stressing under ambient conditions

While the bias stress characteristics exhibited by the blend devices in Section 6.2.1 were exceptional, the experimental conditions for the bias stressing involved testing in an inert N₂ atmosphere, with O₂ and H₂O levels below 0.5 and 2.5 ppm, respectively. This compares with ambient concentrations of O₂ and H₂O of 210,000 ppm and 4,000 ppm, respectively. For organic TFTs to be successful outside of the lab they must be able to

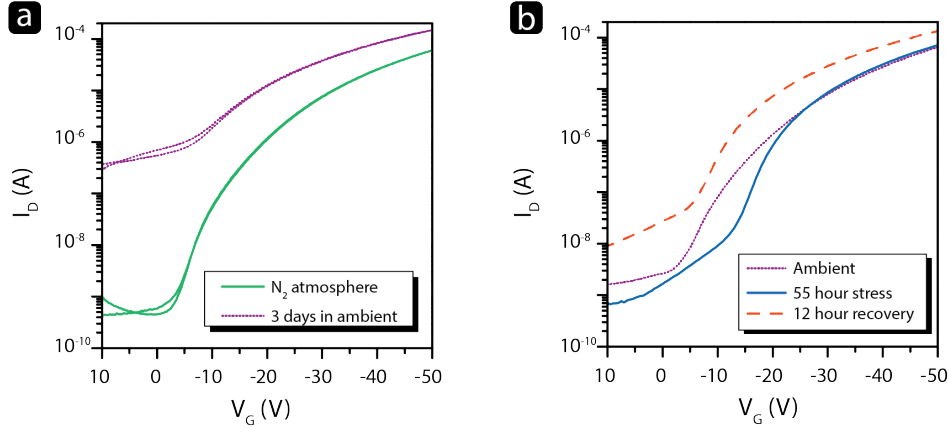


Figure 6.5: **(a)** Transfer curves showing degradation of device performance upon storage in air for 3 days. **(b)** Transfer curves showing the process of a device being initially tested in ambient air and then gate bias stressed for 8 hours. The device was then tested again following 12 hours recovery in air.

exhibit high bias stability in ambient conditions.

As such, the stability of devices in air was tested. No encapsulation was applied to the devices beyond the hydrophobic Cytop dielectric layer that should offer at least some protection to the TFT from dopant species such as O₂ and H₂O.

Figure 6.5a shows the effect of device degradation due to atmospheric species on a blend OTFT. After 3 days the on/off ratio has reduced from 10^5 to less than 10^3 , due mainly to an increase in I_{off} of 3 orders of magnitude. Clearly the Cytop dielectric is not sufficient in preventing doping of the semiconductor, likely through absorption of O₂ [197].

With this process in mind, a similar device was gate bias stressed at -50 V for 2×10^5 s (55 hours) in ambient air, at 22 °C. The first thing to notice from Figure 6.5b is the almost immediate increase in I_{off} upon removal of the device from an N₂ atmosphere (the device was exposed to air for 10 minutes prior to the measurement). Tested under N₂ the same device exhibited an ‘off’ current of 3×10^{-10} A. This demonstrates the speed at which doping occurs. The field-effect conductivity is, however, unchanged after this time.

Gate bias stressing in ambient conditions appears to occur through the same process as is seen when performed in an N₂ atmosphere. Specifically, I_{off} is held down - the

suggestion being free carriers in the bulk (both intrinsic and generated charges due to $\text{O}_2/\text{H}_2\text{O}$ doping) becoming trapped within deep states. The change in shape of the transfer curve is, however, an effect of atmospheric doping.

The gate bias now controls conductivity in two sub-threshold regimes: the first $10 < (-)V_G < -13$ V and the second $-13\text{V} < (-)V_G < -20$ V. This suggests two trap-filling regimes. The first (shallow slope over 20 V V_G range) is due to the doping of the semiconductor, and can be described by a region in the deep tail states that exhibits an increased density of charge traps, compared to an undoped TFT. The second regime, due to the intrinsic nature of the semiconductor, is unchanged from normal operation in N_2 . This suggests that doping has little effect on the tail states in the vicinity of the mobility edge.

Once bias stressing has stopped and the device is left to recover in ambient conditions the doping has a more pronounced effect on the conductivity of the device (“12 hour recovery” plot, Figure 6.5b). I_D increases significantly across the sweep range, whilst having most notable an effect on I_{off} , which increases by over an order of magnitude. The threshold voltage shift reverses due to trapped holes being gradually released, however the additional doping-related subthreshold regime remains, as would be expected. Beyond this the transfer characteristics of the TFT will tend to that depicted by the transfer curve in Figure 6.5a, measured after 3 days spent in ambient conditions.

6.2.3 Bias stressing under elevated temperatures

To understand how elevated operating temperatures influence the process of bias stressing it was first necessary to test the performance of the blend OTFTs across a range of raised temperatures. This was conducted under vacuum with the devices tested on a heated stage. The results, shown in Figure 6.6, highlight the increased conductivity and carrier mobility of the transistor channel at elevated temperatures - the hole mobility increases from $1.3 \text{ cm}^2/\text{Vs}$ at 300 K to $2 \text{ cm}^2/\text{Vs}$ by raising the operating temperature to 360 K. This is explained by the thermally activated nature of charge transport in organic semiconductors.

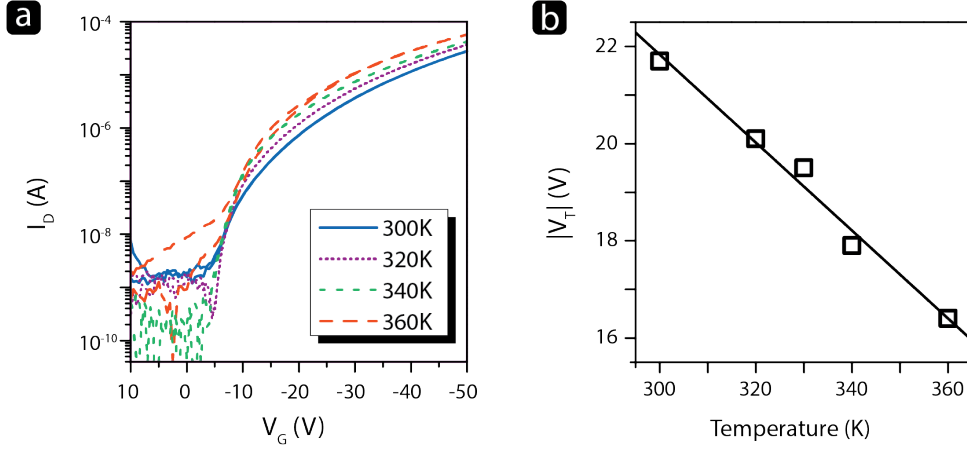


Figure 6.6: **(a)** Temperature dependence of device performance. **(b)** Temperature dependence of threshold voltage.

It should be noted that, as per the results described in Sec. 5.3, no evidence of a diF-TES ADT phase transition was observed below 360 K. In this temperature regime there is no apparent degradation to the on/off ratio and, due to the steeper subthreshold slope, the threshold voltage decreases linearly with temperature, by over 20 % (Figure 6.6b). At 360 K, however, degradation of the device's subthreshold performance is observed. This temperature is comparable to the annealing temperature used during fabrication of the device and as such suggests that morphological changes could be occurring, disrupting the quality of the TFT channel. Upon cooling the device back to room temperature this degradation was observed to be non-reversible, suggesting an upper limit for stable device performance at ~ 70 °C.

Gate bias stressing a blend TFT at 330 K for 17 hours initially shows a rapid increase in I_{off} during the first 10 mins, before a significant decrease in I_{on} which reduces the on/off ratio to less than 10^2 while destroying the subthreshold slope that marks the onset of accumulation (Figure 6.7). Bias stressing with a strong negative gate bias at elevated temperatures appears to cause a large increase in the bulk conductivity of the semiconductor, meaning that large positive gate biases are required to deplete the channel of charge carriers. Note how this is different from simply operating the device at high temperatures, where no increase in I_{off} is seen at 330 K (Figure 6.6a). This result shows

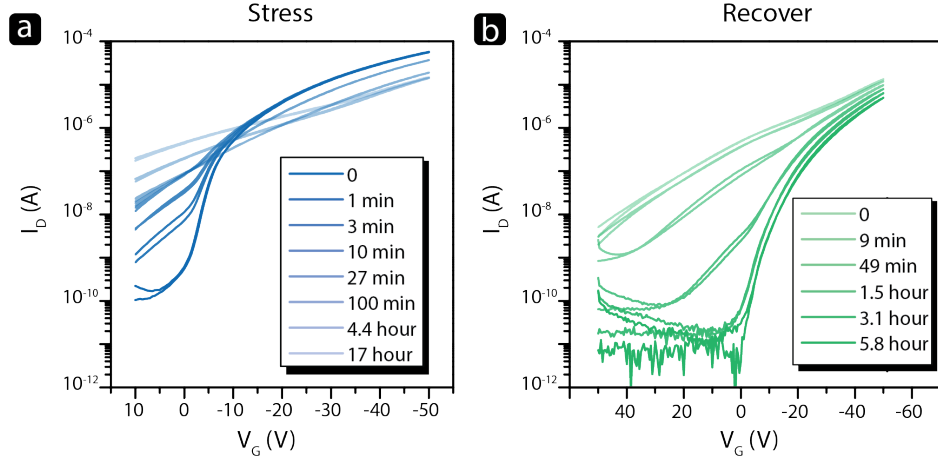


Figure 6.7: **(a)** Gate bias stressing of a blend OTFT device operating at 330 K. Sampling of transfer characteristics is done on a log time scale. **(b)** Recovery of stressed device held in the dark and at 330 K.

that at elevated temperatures the devices do not stress in the usual way and further work needs to be done to elucidate the cause of such dramatic device degradation. However, as the stressing was conducted under vacuum any chemical origins of the stress effects would have to be as a result of species already present in the device.

Upon removal of the gate bias, while keeping the device at 330 K and in the dark, the ‘off’ current decreases reasonably quickly such that within 6 hours of the bias being removed the on/off ratio is restored to 10^5 (Figure 6.7b). Unfortunately, the device degradation appears not to be fully reversible as I_{on} is an order of magnitude lower than for the unstressed device and the subthreshold slope is also reduced. This further suggests some morphological change either at the source/drain contacts or in the transistor channel itself, leading to the creation of additional trap states and reduced hole mobility. Separately, prolonged annealing of a device at 330 K and over 17 hours, without the application of any bias was observed to decrease I_{off} by an order of magnitude and I_{on} by 15 %. This demonstrates that the order of magnitude decrease in I_{on} observed after prolonged stressing at 330 K is a result not solely of thermal effects, but the combination of bias stressing and elevated temperatures.

There is a dearth of reports in the literature on the temperature effects of bias

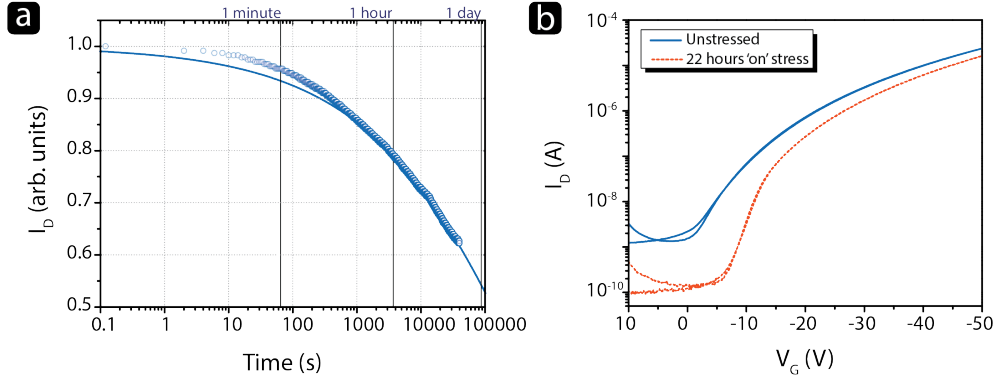


Figure 6.8: **(a)** Current decay of a blend OTFT device operated in the saturation regime for a prolonged period of time. A stretched exponential curve is fit to the data. **(b)** Saturation transfer characteristics of the blend device before and after stressing in the ‘on’ regime.

stressing on organic TFTs. In amorphous silicon TFTs an increased rate of threshold voltage shift is observed at elevated temperatures [198]. This is explained by an increased mobility of hydrogen in the a-Si:H semiconductor leading to an elevated rate of dangling bond trap creation. The bias instability in the blend transistors studied here, however, is not primarily characterised by a threshold voltage shift. Rather, the transfer curve evolution in Fig 6.7a is more indicative of a rapid doping process. The post-stressing recovery may then be explained by a removal of the dopant species from the TFT channel, which in turn presents degraded hole transport qualities of the channel. The origin of the proposed dopant is unclear, however residual ionic species on the substrate could provide an explanation. The elevated temperature could be sufficient to mobilise the ions within the semiconductor, under the application of a strong vertical electric field. These ions would then migrate to within the bulk of the semiconductor film, doping the semiconductor and increasing the TFT’s I_{off} .

6.3 Current decay

6.3.1 Current decay under inert conditions

In order for organic TFTs to find application in OLED displays, they need to be extremely robust at providing high levels of current for prolonged periods. Unlike LCD displays OLED panels are current-driven and so the TFTs powering the OLED pixels need to supply constant current over time scales of several hours. Stressing under application of a constant gate and drain bias is much more demanding on TFTs than simply gate bias stressing and as such devices that perform well under prolonged application of gate bias may not be well-suited to current-driven applications. Compensation circuits can account for a certain level of threshold voltage shift due to charge trapping, however this takes up additional space on the pixel and only acts to compensate the current decay by driving the TFT at a higher bias, thus potentially exacerbating the rate of charge trapping [8]. Oxide TFT technology, a technology that has recently been applied to large OLED displays, has been demonstrated to exhibit extremely high stability, with $\Delta V_T < 1$ V after 100 hours of applying a high drain current, therefore the bar for TFT stability is high [199].

50 wt.% blend OTFT devices were stressed in the dark under application of a -50 V gate and drain bias while the current through the drain electrode was sampled every 2 seconds. The resulting current decay is shown in Figure 6.8a. After 11 hours of device operation the current had decayed by almost 40 %, however within an hour the device had already suffered a drop of 20 %. The cause of this drop can be attributed the same process of charge trapping that was observed in the previous section, as from Figure 6.8b the same negative translation of the transfer curve, along with drop in I_{off} , is observed. This threshold voltage shift is consistent with that observed under pure gate bias stressing, as was presented in Figure 6.3.

However, this device degradation occurs over much shorter time scales than the gate bias stress and the resulting threshold voltage shift, at -2.5 V after 22 hours, is twice that of the worst performing devices measured by gate bias stressing alone (Figure 6.4). This threshold voltage shift corresponds to 5 % of the applied gate voltage.

In the literature, a wide range of stabilities have been published. Of the best, Sekitani *et al.* described flexible devices that after extended post annealing and encapsulation exhibited a current decay of only 3 % after 3 hours [87]. Despite this, most reports of organic semiconductors do not provide this level of stability, and current decays of > 50 % within an hour of operation are commonly observed [95, 98]. Typical current decay in *a*-Si transistors stands at $\sim 10^6$ s (1 month) to reach the 40 % current decay we observe, and further improvements on this have been reported (though significantly lower gate biases were used) [200].

It has previously been reported that the transient electronic performance of blend OTFTs employing the small molecule diF-TES ADT shows negligible light dependence [201]. Similarly, gate bias stressing of the blend OTFTs exhibited no noticeable difference whether the stressing occurred entirely in the dark or under ambient illumination. Despite this, there appears to exist some quite significant effects of light on the current decay of these blend OTFT devices. Figure 6.9 shows the current decay of a device that was stressed under ambient light conditions; everything else about the experiment was identical to that which yielded Figure 6.8, tested in the dark. The first difference is the vastly improved apparent stability of the device tested in the light. After 1 hour the current in the device tested in the dark had dropped by 20 %, whereas the device tested in ambient light had dropped by only 8 %.

As was discussed in section 2.4.4, illumination of the transistor channel can aid the reversal of bias stress effects and in this case it appears that constant low-intensity illumination can stabilise the device against bias stress by providing a counter de-trapping mechanism. This light-assisted de-trapping of carriers can be assumed to reduce the rate of current decay. Using equation 2.21 the current decay can be related to an equivalent threshold voltage shift of -1 ± 0.2 V after 10^3 s which is in agreement with the data displayed in Figure 6.4 for gate bias stressing. This is an extremely interesting observation as it points to the possibility of taking advantage of the emitted light from an OLED pixel to help prevent serious degradation of TFT performance.

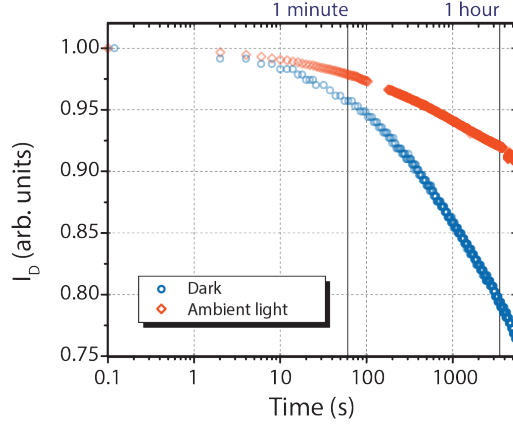


Figure 6.9: Current decay of blend OTFT devices operated in the saturation regime in the dark and exposed to ambient light.

6.3.2 Current decay under elevated temperatures

To further investigate the effects of raised temperature on the stressing behaviour of blend OTFT devices, the current decay in such a device was measured in the dark and under vacuum at temperatures between 300 K and 360 K (Figure 6.10a).

The stress measurements were conducted over shorter time periods than in Figures 6.8 and 6.9 in order to ensure full reversal of bias stress effects between measurements. Temperature increases were conducted slowly and the device was left to dwell for 10 minutes at each successive temperature prior to testing. The first measurement, at 300 K, showed the classic decay characteristics that has been seen previously at low temperatures. At 320 K the rate of current decay is increased by 50 %, although this from a higher initial current (Figure 6.6a), and the monotonic decay is still observed.

At 340 K, however, current decay occurs for < 1000 s, before proceeding to increase for the remainder of the measurement, finishing slightly higher than the initial observed current. This feature is significantly exaggerated at 360 K where the current was only observed to decrease for 30 s before increasing sharply and plateauing at 120 % of I_0 .

By then reducing the temperature to 330 K and repeating the measurement a current-time evolution is seen that also fits into the pattern of increasing rate of initial

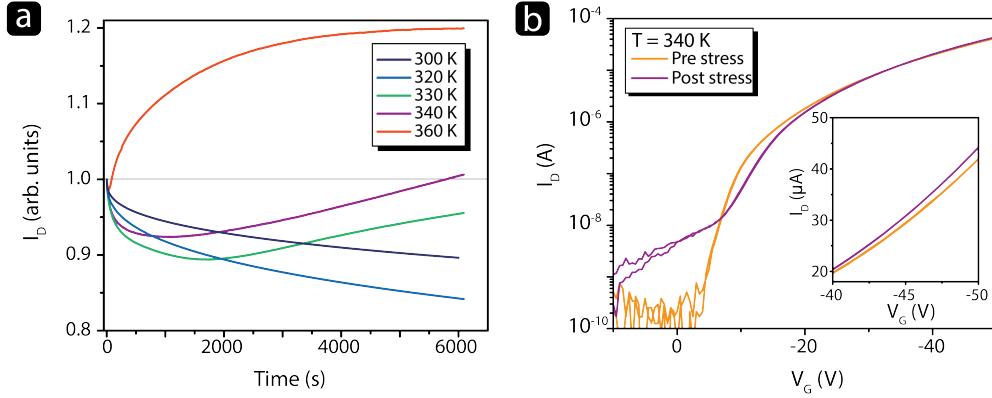


Figure 6.10: **(a)** Time evolution of drain current magnitude of a blend OTFT device at various elevated temperatures. The order of stress testing proceeded as 300 K $\rightarrow$ 320 K $\rightarrow$ 340 K $\rightarrow$ 360 K $\rightarrow$ 330 K. **(b)** Transfer curves of a blend TFT operating at 340 K before and after 6000 s ‘on’ stress. Inset shows a portion of the transfer curves on a linear scale.

current decay for increased T and subsequent current recovery. This rules out the possibility of temperature variation within the device during the measurement causing the increase in conductivity, and also discounts the possibility of the increased temperature causing a gradual, permanent morphology change within the device.

A similar response to stressing at elevated temperatures has been reported by Ng and co-workers with devices fabricated also using a polymer dielectric [194]. They observed a 15 % increase in conductivity in a polythiophene:PVP dielectric device operated at 363 K and explained this through increased injection of carriers into the gate dielectric which proceeded to increase the capacitance of the dielectric layer. However no evidence of this was observed in the transfer curves taken immediately after stressing in this study (Figure 6.10), only the usual threshold voltage shift and moderate increase in I_{off} (which was significantly less than seen in Figure 6.7a). Additionally, an increase in gate leakage current cannot be used to explain the increase in I_D as I_G decreased by almost 60 % during the measurement.

Separately, the phenomenon of increased drain current over prolonged operation has been observed in devices exposed to atmospheric moisture [202, 203]. In these reports the increase in drain current is observed over much shorter time-scales (10’s of seconds)

and is attributed to water molecules and other ionic species in the dielectric creating a polarization field at the semiconductor-dielectric interface. Such an effect is not supported by the evidence from the blend-Cytop system, however. An increased polarisation of the channel could describe the increase in drain current seen in Figure 6.10a, however this approach would not explain the *decrease* in I_{on} observed through gate stressing alone (Figure 6.7a).

Indeed, this phenomenon may be explained under the same hypothesis that was given for the increase in bulk semiconductor conductivity at elevated temperatures in section 6.2.3. Positively charged ions, made increasingly mobile by the elevated temperature, migrating into the semiconductor under the presence of a vertical gate field will remain in the semiconductor bulk or drift towards the interface [204]. In a TFT that also presents a lateral electric field, i.e. when the TFT is biased ‘on’, these ions would drift towards the drain electrode. Such a process has been described in OTFTs exposed to water, with H_3O^+ ions causing an increase in channel conductivity [205].

Due to the source-drain field ions would not remain dispersed in the semiconductor bulk, and so they would not cause an increase in the ‘off’ current. This, in contrast to was observed under high-T gate stressing alone. The hypothesis is supported by the observation that I_{off} remains low in TFTs operated at elevated temperatures for prolonged periods of time (Figure 6.10b). Finally, it should be noted that while this discussion refers to mobile ions, their mobility would still be comparatively low: The transverse movement of ions through the semiconductor or dielectric on the time-scales of seconds would give rise to hysteresis in the transfer curves, which is not evident in either Figure 6.7 or Figure 6.10b.

6.4 Conclusions

In summary, OTFT devices based on a blend of diF-TES ADT:PTAA semiconductors and employing a Cytop gate dielectric have been shown to perform robustly under bias stressing. After a week of gate bias stressing an extremely low threshold voltage shift of 6

% of gate bias was observed. Devices that exhibited a larger density of grain boundaries (small grain blend devices and pristine diF-TES ADT TFTs) stressed at a faster rate than blend devices with crystallites on the order of $100\text{ }\mu\text{m}$ in diameter; hence supporting the theory that grain boundaries are a source of deep charge trapping sites. Interesting TFT degradation processes were observed both when testing under ambient conditions and elevated temperature. Under ambient conditions the blend devices are gradually doped by atmospheric species. When combined with bias stressing of these devices a second subthreshold region of TFT operation is generated, pointing towards the creation of a large density of shallow trap sites below the mobility edge. A reversible doping-like effect was also observed when stressing blend TFTs at elevated temperatures, potentially due to the activation of ordinarily-immobile ionic species within the TFT. The same process was attributed to the increase in drain current observed when devices are stressed for prolonged periods in the ‘on’ regime and at elevated temperatures. Finally it was found that ambient illumination of blend devices reduced the rate of drain current decay seen when the TFT is biased ‘on’ for prolonged periods. This, likely due to a light-assisted hole de-trapping process.

Therefore, the blend system is promising in terms of long-term bias stability. However, the specific degradation mechanisms due to exposure to ambient air and elevated temperatures should be investigated further in order to mitigate such effects.

Chapter 7

Spray deposition for large-area electronics

7.1 Introduction

Through chapters 5 and 6 it has been demonstrated that not only is a high level of morphological control afforded through fabrication of blend OTFTs, but that they show promise in realising the stability required of OTFTs in demanding applications. However, up to this point, all devices have been fabricated using a spin-coating technique that is not suitable for high-throughput manufacture of OTFT devices. Indeed, all reports in the literature concerning the use of semiconducting blends in OTFTs rely on low-volume manufacturing techniques, such as spin-coating. To truly demonstrate this materials system's applicability to next generation ubiquitous electronics, the fabrication of OTFT devices using high-throughput techniques must be demonstrated.

An extremely simple method of achieving this rapid wide-area deposition is through spraying the semiconductor and dielectric solutions using an air gun and a carrier gas. While this technique is simple in principle, it presents unique challenges as previously described in section 3.5.2; one of which being the sequential deposition of semiconductor and dielectric films. Achieving this is not just a challenge for spray deposition of films, but

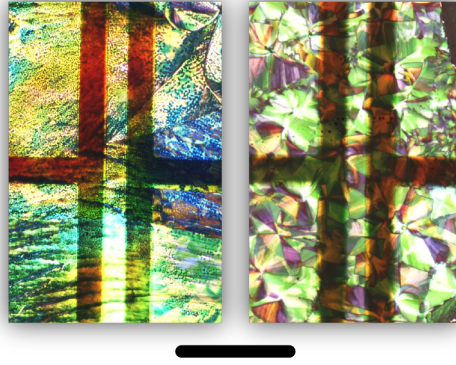


Figure 7.1: Polarised optical micrographs of blend films created via spray casting (left) and spin coating (right) over source and drain electrodes. The scale bar represents 200 μm .

also other high-throughput manufacturing techniques. Despite this, reports of complete device manufacture using high-throughput techniques are not common in the literature.

To address this, in this chapter the fabrication of blend OTFTs is demonstrated through spray deposition of the semiconductor and dielectric layers. This method is used to achieve device performance on-par with similar spin-coated OTFTs, as well as enabling the fabrication of devices operating at sub-10 V. Finally, spray-fabricated devices are combined to demonstrate the potential of this method in the fabrication of low voltage inverter circuits.

7.2 Morphological analysis of sprayed films

Spray deposition of thin films typically returns much rougher films than is achieved through deposition techniques such as spin coating or thermal evaporation [157, 153]. While this is potentially manageable for bottom gate devices, where the channel roughness is largely defined by the planarity of the layer below, for top gate devices the roughness of the semiconductor layer is critical [206].

By depositing a film of the diF-TES ADT:PTAA blend from a solution with half the semiconductor concentration (20 mg/ml) as is used for spin coating, a surprisingly flat

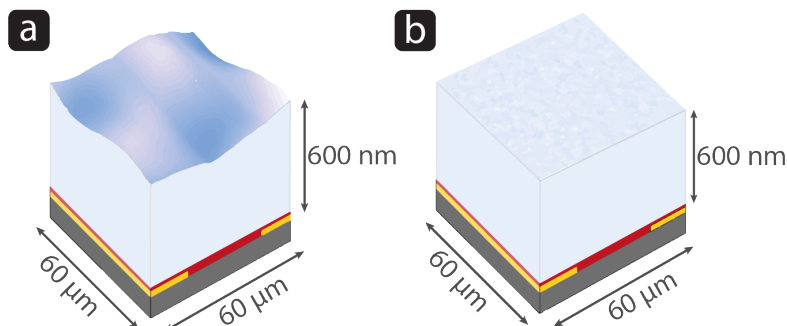


Figure 7.2: AFM cartoons of devices with **(a)** spray and **(b)** spin cast Cytop layers. The z-axis in both cases has been magnified relative to the x and y axes for clarity.

film is achieved. This is because the fundamental process of film formation is the same as that observed in spin-coating i.e. the solid state film is produced subsequent to the deposition step, by driving solvent from the liquid film using a hot plate. As such the morphology and roughness of the films deposited via an air brush is similar to the films produced by spin coating.

Polarised optical micrographs of a spin-coated and spray-coated blend film are shown in Figure 7.1. Spray deposited films rarely exhibited the uniform spherulitic crystal motif that is seen in high-performing films deposited by spin coating; instead, spray cast films exhibit less uniform crystallisation across the substrate. Despite this, the formation of large, extended diF-TES ADT crystals was frequently observed, commonly 100's μm in diameter.

The most critical problem that is encountered when spray depositing blend films is the formation thick, disordered regions of semiconductor at the position the final solvent is removed. These regions can only be avoided by ensuring that the quantity of semiconductor solution deposited in the first instance is no more than necessary, something that can be achieved through fine control of spray duration, carrier gas pressure, solution temperature and surface energy of the substrate. However, even using a simple hand-held spray set up this can be largely achieved.

Spray deposition of Cytop provides a separate challenge in that the solution in which

it is shipped is highly viscous which leads to extremely uneven film formation upon spray deposition. To avoid this the solution was diluted with a separate fluorinated solvent, FC-43 (Acota [164]). The topography of two spray and spin-cast 600 nm Cytop films are depicted in Figure 7.2. It is clear that the spray-coated Cytop, with a roughness of 40 nm is considerably less even than the spin-cast film with a roughness of 0.4 nm. Despite this disparity in roughness the actual channel interface of the TFT should be of high quality due to no coffee-stain features being observed, which are indicative of individual droplets being deposited, rather than a consistent film.

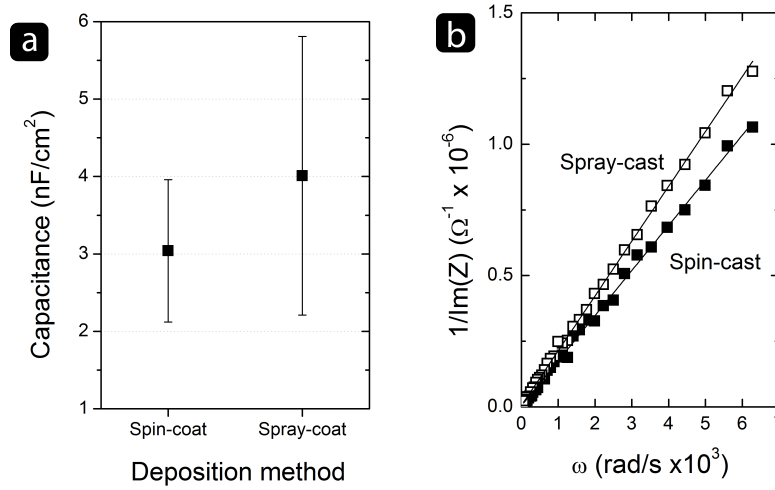


Figure 7.3: **(a)** Comparison of geometrical capacitance of eight spin-coated and spray-coated Cytop films, with the error defined as the standard deviation. **(b)** Example impedance-frequency plots for two 0.04 cm² capacitors.

To characterise the capacitance of the spray-cast Cytop and the resulting uncertainty due to the increased surface roughness, impedance spectroscopy was performed. The measured capacitance of eight sprayed capacitors was then compared to eight spin-cast Cytop capacitors. It was found that spray deposition according to the procedure in section 4.1.5 provided 600 nm films with a mean geometric capacitance of 4 ± 2 nF/cm², compared to a value of 3 ± 1 nF/cm² for the thicker spin-coated films (Figure 7.3a). The larger uncertainty of dielectric capacitance for the sprayed films is not surprising, however the magnitude of uncertainty is somewhat higher than would perhaps be expected. For a 600

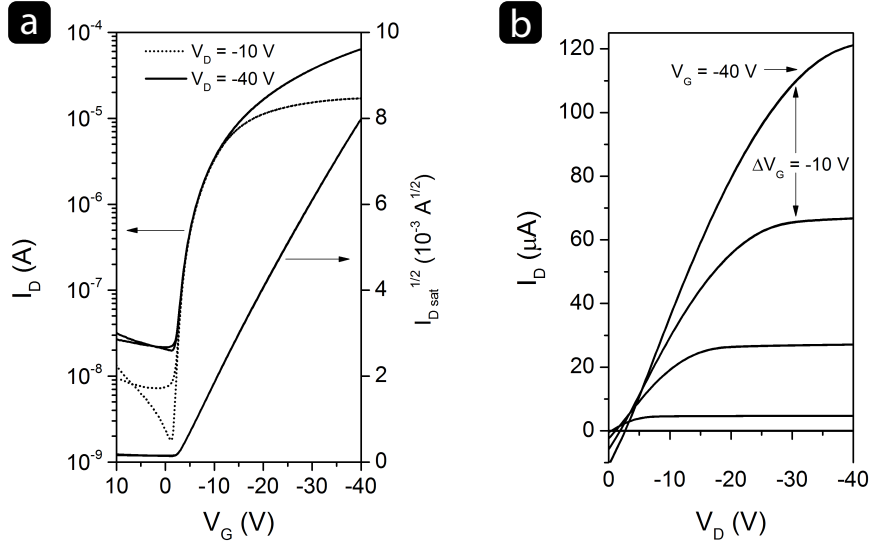


Figure 7.4: (a) Transfer characteristics of a blend device fabricated through spray deposition of both the semiconductor and Cytop layers, with $W/L = 1000/50$ and (b) the output characteristics of the same device.

nm Cytop film with a peak-to-trough height of 100 nm, a maximum capacitance difference of around 20 % would be expected. For a spin coated film, this uncertainty would be negligible. It is most likely that this uncertainty originates from the overstatement of capacitance for smaller capacitors, due to edge effects. This is less noticeable in larger capacitors and so one would expect the true capacitance of the Cytop films to be towards the lower end of their experimental distribution.

7.3 Blend TFTs fabricated by spray deposition

TFT devices were initially fabricated by spraying the semiconductor solution at the same concentration as is used when spin-coating the blend film. These films were then coated with a spin-cast layer of Cytop, following the usual recipe. While these sprayed films demonstrated operational devices, the yield was low because of film non-uniformities and parameters such as subthreshold swing and ‘off’ current were considerably worse than their spin-coated equivalents.

7.3. Blend TFTs fabricated by spray deposition

To improve the general film quality the solution concentration was halved to 20 mg/ml. Not only did this reduced solution concentration aid in creating more uniform thin films and improving the yield, but the on/off ratio and subthreshold swing were improved relative to devices fabricated using a 40 mg/ml solution. This was due to thinner films providing lower bulk conductivity and therefore lower values of I_{off} . The mean on/off ratio was increased by an order of magnitude to 10^5 , the subthreshold swing was halved to 4 V/decade, and the device-to-device variation was also reduced for these parameters. The carrier mobilities remained consistent, with a mean saturation mobility of $0.75 \text{ cm}^2/\text{Vs}$.

The technique was developed further by depositing the dielectric layer also via spray deposition, such that only the metal contacts were not deposited via a high-throughput manufacturing method. This was achieved by reducing the Cytop solution concentration; diluting it 1:3, by volume, in FC-43. In several ways the sprayed Cytop films actually lead to improved device performance compared to spin cast films. A statistical comparison of devices fabricated entirely through spin and spray deposition is shown in Figure 7.5, while histograms demonstrating the distribution in device parameters for spray-cast devices are shown in Figure 7.6. Table 7.1 highlights the mean values and standard deviations of key device parameters for the two data sets.

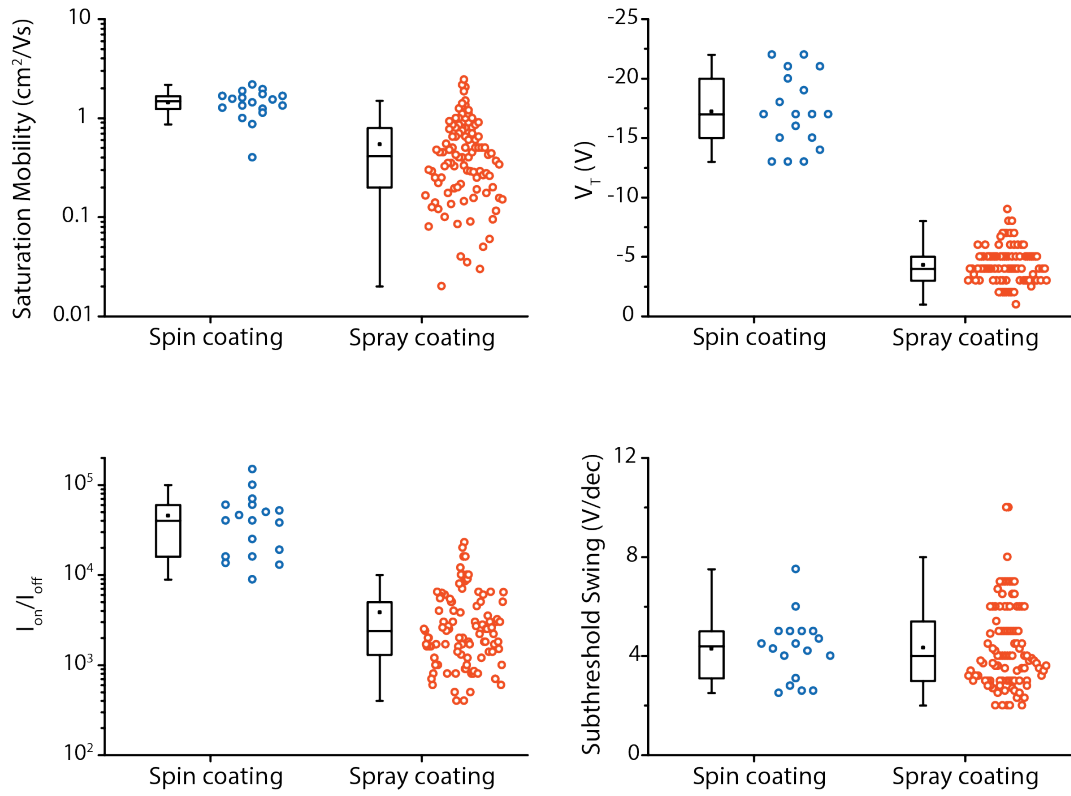


Figure 7.5: Box-whisker plots comparing the performance of diF-TES ADT:PTAA blend OTFTs fabricated through either spin-coating or spray-coating both the semiconductor and dielectric layers.

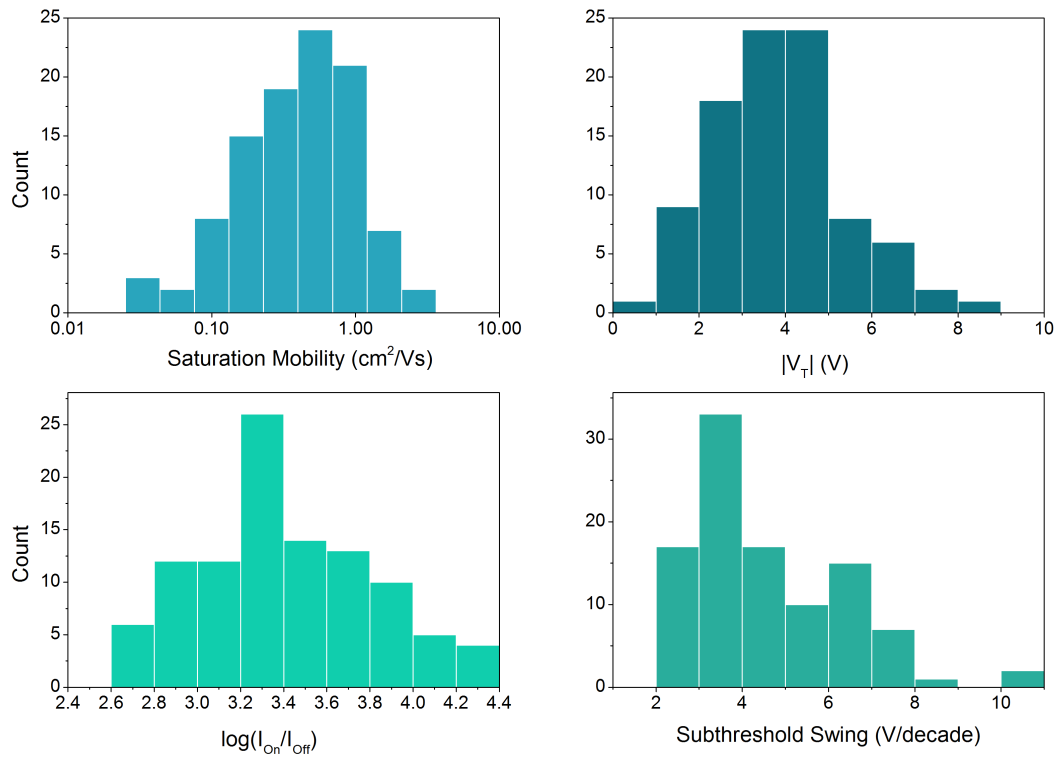


Figure 7.6: Histograms describing the distribution of operating parameters exhibited by > 70 TFTs fabricated through spray deposition of the semiconductor and dielectric layers.

7.3. Blend TFTs fabricated by spray deposition

Method	μ_{sat} (cm ² /Vs)	μ_{lin} (cm ² /Vs)	V_T (V)	$I_{\text{on}}/I_{\text{off}}$	S (V/decade)
Spray-coating	0.6 ± 0.5	0.5 ± 0.4	-4.5 ± 1.5	4000	4.0 ± 1.7
Spin-coating	1.4 ± 0.4	0.8 ± 0.3	-17 ± 3	45000	4.4 ± 1.3

Table 7.1: Device parameters of diF-TES ADT:PTAA OTFTs fabricated by spin-coating and spray-coating techniques

Due to the reduced morphological control achieved with the manual spray-coating process, the mean saturation hole mobility values was roughly half that of the spin-cast films, and the standard deviation > 80% of the mean for the spray cast devices, as opposed to < 30% for spin-cast devices. Interestingly, the threshold voltage for the spray-cast devices was almost four times lower than that of the of the spin-cast devices. This is undoubtedly in part due to the higher capacitance of the dielectric layer compared to the thicker spin coated dielectric, however the magnitude of capacitance increase compared to the reduction in V_T does not agree if one considers a simple definition of the threshold voltage. In the most simple model, V_T is the gate bias required to fill hole traps with charge carriers such that further induced carriers lie in mobile states i.e.

$$V_T = N_{tr} e / C_i \quad (7.1)$$

As such, if the the trap density is constant, this relationship describes an inverse proportionality between V_T and dielectric capacitance. However, the data in Table 7.1 shows a 75% decrease in V_T due to a 30% increase in capacitance (Figure 7.3). This suggests that the change in subthreshold characteristics of the TFTs is a result not only of the increase in dielectric capacitance but, more fundamentally, a reduction in the density of charge traps.

The subthreshold region is strongly influenced by the semiconductor-dielectric interface, and the effect this has on the density of band-gap tail states. Following the same analytical technique that was used to extract the density of tail states in section 5.4, the DOS of the device described by Figure 7.4 was analysed. The result, compared to an

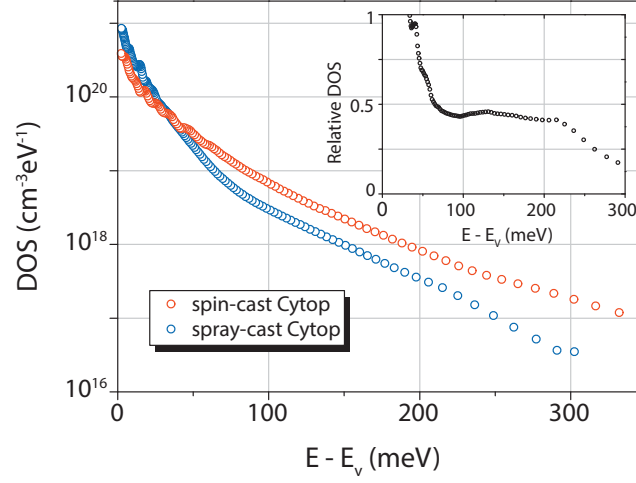


Figure 7.7: Density of tail states of diF-TES ADT:PTAA blend TFTs with the Cytop dielectric processed either by spin or spray casting. Inset: Density of tail states in a spray-cast Cytop TFT, relative to a spin-cast Cytop TFT.

equivalent spin-cast device, is shown in Figure 7.7. Clearly, beyond the first 50 meV from the mobility edge, the spin-cast device exhibits a larger density of tail states. Indeed the spray-cast Cytop provides an approximately constant 50 % reduction in the density of tail states across a 200 meV spectral range. This is interesting as it suggests that rather than the process of spin-casting Cytop creating additional trap states at a particular energy, it acts simply to broaden the distribution of tail states.

This analysis, therefore, suggests that the more gentle spray deposition of Cytop compared to spin coating, which provides high shear forces, enables the creation of a better semiconductor-dielectric interface. As a result, the improved interface reduces the density of trap sites and provides improved subthreshold performance.

While the morphological control of the semiconductor film showed room for improvement, the hole mobility of the best performing devices were on par with the best devices achieved by spin coating. This, combined with the observation that low threshold voltages could be achieved with spray deposited Cytop, highlighted the potential for this system in the fabrication of low-voltage TFT devices.

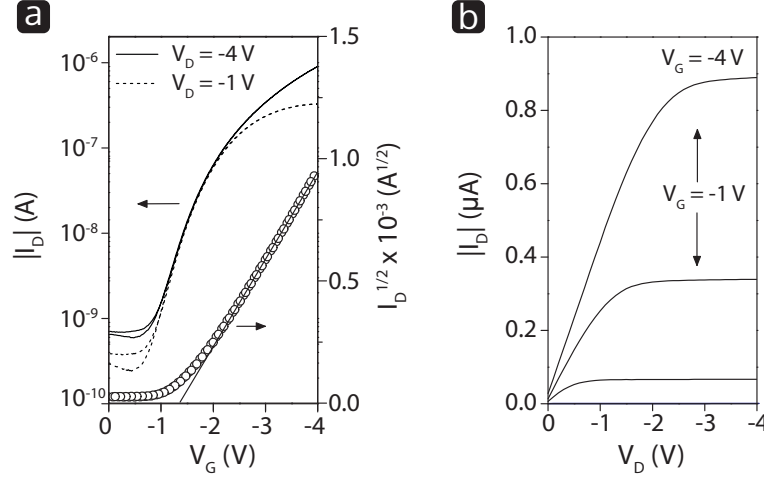


Figure 7.8: (a) Transfer and (b) output curves of a low-voltage blend TFT fabricated via spray deposition of both semiconductor and dielectric layers. Device dimensions were $W = 1000 \mu\text{m}$ and $L = 30 \mu\text{m}$.

7.4 Low voltage TFTs and circuits

Beyond fabricating OTFTs in a scalable manner, many of the envisioned applications for organic electronic devices require low-power operation. Specifically, the industry standard supply voltages in mobile electronic devices ranges from 1.2 to 3.3 V. To reduce the operating voltage and power consumption of spray-cast blend OTFTs the capacitance of the dielectric film needed to be increased. Rather than moving to a high- k dielectric material, this was attempted by depositing thinner Cytop layers.

By reducing the dielectric solution concentration further, to 1:4 Cytop solution:FC-43, and limiting the spray duration, dielectric films of 120 nm were achieved; an 80 % reduction on the film thickness demonstrated in section 7.3. The reduction in volume of Cytop deposited also helped reduce the film roughness from ~ 40 nm to ~ 10 nm. However, due to the films being thinner, this still represents almost 10 % of the film's total thickness.

TFTs fabricated in this way, via hand-held spray deposition, performed remarkably well, with hole mobilities of up to $1.8 \text{ cm}^2/\text{Vs}$ being recorded at gate and drain voltages down to -4 V. Unfortunately, due to the variation in both the semiconductor (morphology and thickness) and Cytop (thickness) films across the substrate the parameter spread

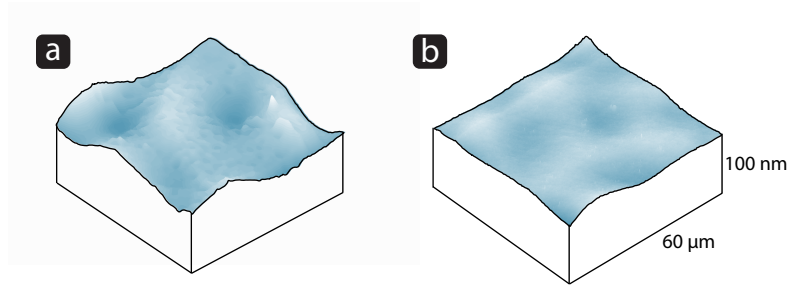


Figure 7.9: AFM topography maps of hand-sprayed (a) and automated-sprayed (b) Cytop films. Films were approximately 100 nm thick and the surface roughness of the films shown by the maps is consistent with the 100 nm height of the drawings. AFM scan areas were 60 x 60 μm .

for these devices was quite large. The mean saturation mobility of these devices was 0.7 cm^2/Vs , however the standard deviation of measured saturation mobilities across the population of devices was 0.4 cm^2/Vs , i.e. almost 60 % of the mean.

To address this issue an automated spray-deposition process was trialled in collaboration with Jeremy Ward and Professor Oana Jurchescu at Wake Forest University. The system was home-built and based on a 3D printer framework. This enabled accurate control over the deposition rate, travel rate and nozzle-substrate distance. The system at Wake Forest sprayed Cytop solution at a concentration of 8:1 wt.% ratio of fluorinated solvent (CT-Solv 180, Asahi Glass) to Cytop. The nozzle was positioned 6 cm above the substrate and N_2 was used as a carrier gas at a pressure of 8 psi. The travel rate of the airbrush was constant, at 2 cm s^{-1} .

The result was the creation of Cytop films that were completely free of coffee-stain features and exhibited a film roughness of 3 nm; a 70 % reduction on the roughness of equivalent hand-sprayed films. AFM maps of hand-sprayed and automated-sprayed Cytop films are shown in Figure 7.9. The standard deviation of saturation hole mobilities exhibited by devices fabricated with automated-sprayed Cytop films was reduced to 0.2 from 0.4 cm^2/Vs . This is attributed to the more uniform dielectric layer thickness achieved, and therefore more uniform capacitance. While small variations in the capacitance of the dielectric layer should not impact the carrier mobility of a semiconductor, the uncertainty in the actual dielectric thickness for each TFT meant that estimations of the carrier mobil-

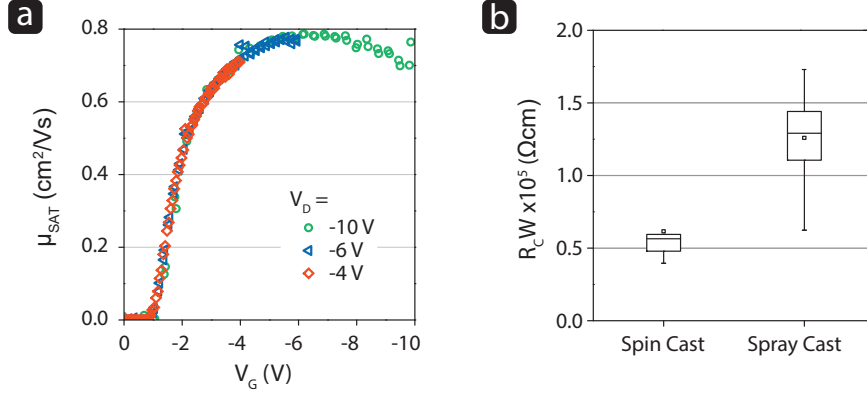


Figure 7.10: (a) Saturation hole mobility in a low-V sprayed OTFT as a function of gate and drain bias. (b) Comparison of the contact resistance measured in spin cast and spray cast devices.

ity would also be subject to this uncertainty. The success of automated-spray deposition of the Cytop layer suggests that improvements to the semiconductor film uniformity could also be achieved by employing a similar approach.

With the best performing spray-cast devices exhibiting carrier mobilities almost on-par with spin-cast, high-voltage TFTs, the potential for this manufacturing technique is evident. However, the saturation mobility of devices was broadly spread between the upper bound of $1.8 \text{ cm}^2/\text{Vs}$ and the minimum value of $0.2 \text{ cm}^2/\text{Vs}$. To begin tackling this broad tail of hole mobility values and reduced mean saturation mobility in these low-voltage devices an understanding of the origins was needed. The lateral field dependence of hole mobility was investigated to determine whether these devices were subject to the Poole-Frenkel effect, whereby charge transport is activated by large source-drain fields. This is typically evidence of a poor semiconductor layer with considerable disorder. However, the low-V sprayed devices exhibited negligible field dependence of carrier mobility, as has been shown previously in spin-cast, high-voltage diF-TES ADT:PTAA blend TFTs [20]. Figure 7.10a demonstrates the lack of lateral field influence on the linear-regime hole mobility of a spray-cast device.

Rather than Poole-Frenkel effects, it appears that the greatest contributor to the reduced mean hole mobility and increased variance is contact resistances. Blend OTFTs

rely on the fine balance of vertical phase separation and control of film thickness to achieve optimum performance. The PTAA polymer binder in the blend exhibits a low hole mobility of $10^{-3} \text{ cm}^2/\text{Vs}$, however its relatively shallow HOMO level (-5.2 eV [207]) makes it easy to inject holes into the semiconductor from high work-function metal electrodes (5.8 eV) [208]. This means that as long as any PTAA or amorphous mixed phase layer coating the source/drain electrodes is thin enough, holes can be efficiently transported from the electrode to the diF-TES ADT channel. Due to the reduced control over film thickness and uniformity in spray-cast blend films, however, this critical contact region is much more difficult to control. Figure 7.10b shows that not only is the mean contact resistance higher in spray-cast devices but the range of contact resistances is also increased relative to spin-cast devices. It is therefore likely that the root cause of the lower hole mobility and increased variance in these spray-cast devices is a contact resistance effect. This observation, however, suggests that by increasing the blend film uniformity, potentially through use of an automated spray system, low-V OTFTs with hole mobilities of $\sim 2 \text{ cm}^2/\text{Vs}$ should be consistently achievable.

Finally, to demonstrate a potential application of low-voltage blend OTFTs simple unipolar inverters were fabricated. Two diF-TES ADT:PTAA blend TFTs, fabricated via spray deposition, were connected to create a unipolar inverter using the saturated load configuration (inset of Figure 7.11a). In this configuration TFTs are chosen with asimilar channel widths such as to create a large ratio in the conductivity of the load and drive TFTs: in this instance the ratio of drive to load TFT W was 10:1. The resulting transfer and gain curves of such a device is shown in Figure 7.11a. The inverter operated well at a drive voltage of -6 V, exhibiting a gain of 6 which demonstrates that such devices would be suitable for integration into larger logic circuits such as ring oscillators. Unipolar inverters exhibit inherently lower gain values than complementary inverters, however a value of 6 is respectable in this instance. Higher gain values on the order of 20 can be achieved in low voltage, unipolar organic inverters through the use of high capacitance dielectrics, however the downside to this approach is increased hysteresis in the transfer curve [209]. Additionally, these higher gain values have typically been achieved with the use of inorganic dielectrics and processing that is not suitable for large-area deposition

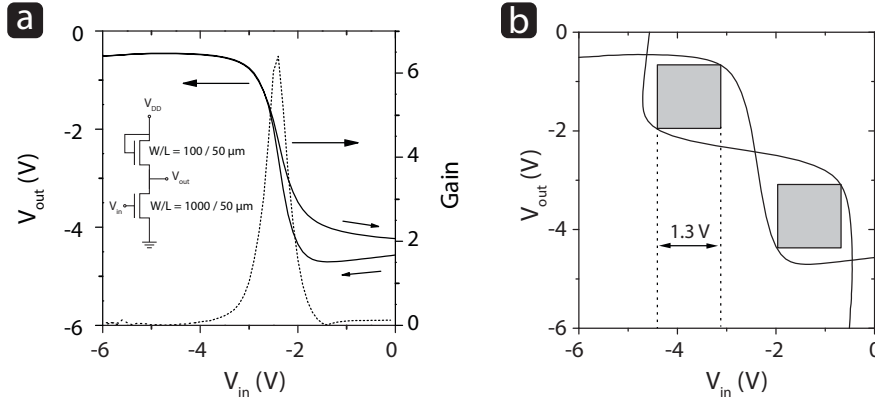


Figure 7.11: (a) Transfer and gain characteristics of a low-voltage unipolar inverter, based on sprayed blend OTFTs. (b) Extraction of the noise margin from the inverter transfer curve.

[210].

The inverter shown in Figure 7.11a suffers from only minor hysteresis, however complete inversion is not achieved i.e. V_{out} exists between -0.5 and -4.5 V, despite V_{DD} being held at -6 V and V_{in} being swept from 0 to -6 V and back. The robustness of an inverter to noise (i.e. how likely it is to correctly return High or Low) is judged by its noise margin. The noise margin is a function of both the gain of the inverter and its V_{out} range, as demonstrated by Figure 7.11b. In this instance a noise margin of 1.3 V (43 %) is achieved, which is respectable for unipolar inverters operating at low voltage.

7.5 Conclusions

In summary, the technique of spray deposition has been evaluated for the high-throughput manufacture of OTFTs based on semiconductor blends. It was found that hand-held spray deposition of both the semiconductor and dielectric layers can be used to achieve OTFTs of comparable performance to those fabricated using the low-throughput but commonly used technique of spin-coating. Despite this, the uniformity of hole mobility measured over 10's of devices is lower than that of spin-cast devices, a fact arising from the reduced control over film formation afforded by spray deposition.

Spray cast devices were seen to exhibit good subthreshold characteristics and low threshold voltages. A density of tail states analysis showed that spray deposition of the dielectric Cytop may produce a reduction in the distribution of band-gap states. This suggests that the gentler method of film formation, compared to spin casting, produces a better semiconductor-dielectric interface.

Spray deposition of 100 nm-thick Cytop films was achieved and used to fabricate sprayed blend OTFTs operating down to -4 V, with the best devices performing on-par with high-voltage spin-cast devices. However, an analysis of the spray-cast devices showed an increase in the mean contact resistance - and increased parameter spread - compared to spin cast devices. This was attributed to the reduction in semiconductor film uniformity, and charged with the origin of lower mean hole mobility. Automated spray casting of Cytop was performed at Wake Forest University, demonstrating greatly improved film uniformity of the dielectric, suggesting that this approach could also be employed to improve the semiconductor film uniformity and, therefore, device parameter spread.

Finally, unipolar low-voltage inverters were fabricated using hand-held spray deposition. The devices exhibited good performance and demonstrated the potential for spray deposition as a technique for the manufacture of large-area, low power electronics.

Chapter 8

Summary and conclusions

The work described in this thesis covers advances in the understanding of diF-TES ADT:PTAA semiconductor blend OTFTs, along with advances in the fabrication thereof. This chapter will lay out the key findings from chapters 5-7 of this thesis. The chapter will also look to provide a conversation on possible future directions for research into this particular materials system, and blend OTFTs in general.

Chapter 5 begins by introducing diF-TES ADT:PTAA blend transistors and describing their performance as a function of the small molecule to polymer ratio. It is shown that a blending ratio of 1:1 diF-TES ADT:PTAA is optimal for high mobility devices with good operational characteristics and device uniformity. The technique of conductive-AFM was used in an effort to provide a morphological explanation of the variation in device performance with semiconductor composition. The formation of charge carrier percolation pathways through diF-TES ADT surface crystals was observed through mapping the electrical conductivity of the film on the nanoscale. In blends with high concentrations of diF-TES ADT (≥ 60 wt.%) ‘cratering’ of the film and increased roughness was shown to be the source of worsening electrical conductivity.

To gain a better understanding of the electrical characteristics of semiconductor blend films, the effect blend composition has on the density of shallow trap states, or tail states, was investigated. Firstly this was done from a consideration of activation

energy for charge transport, which required that OTFTs of a range of semiconductor blend compositions be tested at temperatures down to 130 K. At these temperatures hole transport in PTAA TFTs is effectively frozen out, while diF-TES ADT-rich devices suffer from only a 75% reduction in hole mobility compared to room temperature operation. This is ascribed to the fundamental difference in charge transport through amorphous polymers compared to ordered crystalline small molecule semiconductors, which are generally less reliant on thermal activation for charge transport.

In comparison to the pristine diF-TES ADT and PTAA materials, blend films generally exhibit an increase in the activation energy for hole transport, evidence of increased energetic disorder created in the blend films. The exception to this rule, however, lies with the 50 wt.% blend which minimizes E_A , and therefore ensures that more holes induced by the gate field exist in mobile states, leading to the optimal TFT performance that is observed. Additionally, it was found that semiconductor film roughness is a strong predictor of E_A for the blend devices. While this wasn't a surprise in itself, the fact that the pristine PTAA and diF-TES ADT devices did not follow the same relationship highlighted the role that charge transport between the two phases has in controlling the performance of blend devices.

The Meyer Neldel rule was applied to semiconductor compositions whose calculated E_A were a function of V_G (and therefore exhibited evidence of a distribution of tail states). This was the case for all the diF-TES ADT-containing devices, but not so for PTAA, which was left with the unsatisfying implication that PTAA devices do not exhibit a distribution of tail states but rather a single trap energy. The characteristic tail state distribution width for diF-TES ADT-containing devices, as estimated from the MNR, was broadly consistent for blend devices with compositions between 30 - 60 wt.%, however pristine diF-TES ADT and 70 wt.% blend devices were observed to exhibit much broader tail states distributions. It was concluded that optimum performance of a semiconductor blend is achieved when the polymer component is at the correct concentration to enable controlled crystal growth of the diF-TES ADT and therefore reduce the large tail-state distribution observed in the pristine diF-TES ADT, while preventing the larger E_A values observed in other blend

ratios.

To provide a counter interpretation of the tail state distributions calculated using the E_A and MNR approach, as well as to provide a critique on the reliability of two popular tail state estimation methods, the Grünwald model of tail state estimation was used. In agreement with the MNR approach the Grünwald method also returned tail state distribution widths that increased with small molecule content. Further, the distribution of these tail states was observed to broaden at increased operating temperature in diF-TES ADT-containing devices. This was assumed to be due to the increased thermal energy of diF-TES ADT molecules leading to a more disordered energetic landscape.

However, above a critical temperature (between 200 and 250 K, but depending on the semiconductor composition) thermal broadening of the tails states ceases. Below the critical temperature there exists no significant relationship between the distribution of tail states and the semiconductor composition, yet at high temperatures (> 250 K) the tail state distribution becomes composition dependent: Semiconductor blends with a higher concentration of diF-TES ADT exhibit a broader distribution of tail states. Of greatest interest in this analysis was the performance of the 30 wt.% and 40 wt.% blends. Below the critical temperature the tail state distribution in these semiconductor films is indistinguishable from that of more diF-TES ADT-rich films. At high temperature, however the tail state distribution showed significant influence from the PTAA phase. This points to two different hole transport mechanisms occurring in these blends depending on the temperature: At low temperature hole transport is ‘frozen out’ of the polymer phase, while providing a significant contribution to the film’s hole conductivity above the critical temperature.

At high temperature the Grünwald method was also used to probe the deep trap states in the blend and pristine semiconductor films. The distribution of deep trap states was found to be semiconductor-independent, with a characteristic width of ~ 80 meV, compared to 20 - 45 meV for the tail states.

In comparing the two methods of investigating band-gap tail states in OTFTs it was found that the Grünwald method not only provided a more intuitive analysis of the tail

state distribution, but was also more reliable: Over the the blend composition range of 30 - 60 wt.% diF-TES ADT the tail state distribution width estimated by the Gr unewald and the MNR agreed to within ~ 15 %. However, for distribution widths < 25 meV the MNR failed to identify a distribution of tail states, and for disordered 70 wt.% blend and pristine diF-TES ADT films the distribution was vastly overestimated. The cause of this latter issue being that the hole mobility of the devices did not saturate as a function of V_G within the operating voltages used (which, at up to -70 V, where high). As such, conclusions drawn from the MNR approach must be done so with care.

In chapter 6 diF-TES ADT:PTAA OTFTs were shown to perform robustly under bias stressing. However, interesting TFT degradation processes were also observed both when testing under ambient conditions and elevated temperature.

Firstly, devices were stressed under the application of a gate bias for up to a week, periodically being interrupted to measure threshold voltage shifts due to charge trapping. After a week of applied bias, the threshold voltage had typically shifted by -3 V, or 6% of the -50 V applied gate bias. This was accompanied by a significant decrease in I_{off} which was attributed to trapping of free carriers residing in the semiconductor bulk.

Individual semiconductor component devices were fabricated, along with blend devices exhibiting small and large grain microstructures to investigate the influence of the semiconductor on the stressing characteristics. All devices exhibited minor threshold voltage shift, suggesting that the Cytop dielectric aids stability in all devices. Of the variations that did exist between the devices, the small grain device exhibited a quicker rate of V_T shift than the large grain device, with the increased grain boundary density in the small grain device potentially providing an increased source of trap sites.

The ambient stability of blend devices was then investigated. An un-encapsulated device showed significant doping after being exposed to air for 3 days. During the same period a device was stressed in air, exhibiting a more pronounced ΔV_T than was observed under N_2 , while trapping of the carriers generated by doping of the semiconductor lead to an additional subthreshold regime of trap filling in the transfer characteristics.

Operating blend OTFTs at elevated temperatures lead to serious device degradation under prolonged application of gate bias. The bulk semiconductor conductivity increased dramatically (a feature that is reversible through removal of the gate bias), while I_{on} decreases (a feature that appears to be permanent). It was hypothesised that this process could be a result of doping of the bulk semiconductor by ionic species. These ions would be ordinarily trapped at the substrate at ambient temperatures.

The rate and magnitude of current decay in blend devices biased ‘on’ was investigated. Stressing in the dark showed the same V_T shift and I_{off} decrease as gate stressing, however in contrast to gate stressing the presence of ambient light was seen to strongly decrease the rate of current decay. It is concluded that the presence of light provides a de-trapping mechanism, helping to stabilise the current through the device. However why this effect isn’t evident during gate stressing is unknown.

Elevated temperature measurements of current decay also provided interesting insights. Devices operating at above room temperature and under bias stress demonstrated accelerated current decay, and therefore carrier trapping, over short time scales. However for temperatures of 330 K and above, the current magnitude recovered after a time and even proceeded to increase to levels above the initial current.

It was hypothesized that the interesting device degradation phenomena observed while stressing the blend TFTs at elevated temperatures is due to the increased mobility of ionic species ordinarily trapped on the substrate surface. The process of migration of these positive ions could potentially explain both the increased I_{off} of devices under gate bias stressing, and the gradual increase in I_{on} of TFTs biased ‘on’ for prolonged periods of time, due to doping of the semiconductor.

Finally, in chapter 7, the fabrication of blend devices using a high-throughput, hand-held spray deposition, manufacturing technique was investigated. To form semiconductor films the solution was deposited onto the substrate in a liquid film, the solvent was then removed using a hot plate as in spin-casting. This method of film formation enabled the growth of large diF-TES ADT crystals and low film roughness. However, thick film regions of high roughness were often observed over small parts of the substrate. This is something

that could be avoided with more precise control of the solution deposition e.g. by an automated spray system. Subsequent spray deposition of Cytop layers create a very high quality interface with the blend film as evidenced by the excellent device subthreshold characteristics. A tail states analysis of spin-cast versus spray-cast devices highlighted a 50 % reduction in the density of states over the majority of the spectrum of band-gap states. Over 70 spray-cast TFTs were fabricated, exhibiting a mean saturation mobility of $0.6 \text{ cm}^2/\text{Vs}$ and low threshold voltage of -4.5 V . The hole mobility in spray cast devices was around half that achieved by spin casting.

By reducing the Cytop solution concentration and the spray duration it was possible to deposit 120 nm-thick films by hand-held spray deposition. The increased capacitance that this resulted in enables the fabrication of TFTs operating down to -4 V . The saturation hole mobility was unchanged from the high-voltage spray-cast devices, however the best performing devices exhibited hole mobilities on par with the best spin-cast devices, hinting at significant possible improvements with the correct manufacturing optimisation: Automated spray deposition of the Cytop film succeeded in reducing the dielectric film roughness and brought down the device variation. The origin of the reduced hole mobility in the spray cast films was attributed to the increased magnitude and variance of contact resistance, brought about due to the (on average) thicker and less-uniform semiconductor films produced by hand-held spray deposition. Finally, to demonstrate the potential of the deposition technique for the fabrication of large-area electronics, low-voltage inverters were created, operating at -6 V . Such devices performed well and gains of up to 6, combined with noise margins of 43 %, were achieved.

In conclusion, an extensive investigation into the electrical characteristics and operational stability of the diF-TES ADT:PTAA blend system has been presented. Further, this blend system was used to demonstrate the potential for blend TFTs to be employed in the large area manufacture of organic electronic devices. Previous work had shown the blend system to offer numerous advantages for the fabrication of OTFTs, namely high carrier mobility (greater than amorphous silicon), ease of processing and improved control over the small-molecule microstructure. This work addresses further requirements on or-

ganic semiconductors that are needed for their commercial success in applications such as display backplanes, sensors and logic circuits. A greater understanding of the tail states in blend OTFTs means that approaches can be taken to ensure that the density of such states can be minimized. Characterising the operational instability mechanisms in blend OTFTs will mean that safeguards can be put in place to ensure that the OTFTs are not exposed to such damaging conditions. For example, encapsulation will be needed to protect blend OTFTs from atmospheric species, and exposure to ambient light can prevent the worst of threshold voltage shifts in current-driven applications. Demonstrating that spray-casting blend devices is possible, using an extremely lo-fidelity hand-held method, opens up the field for further refinement and research into the use of this technique as a means of fabricating large-area low-cost electronic devices.

Despite the continued promise shown by this materials system, further work will be required to ensure its commercial success. Firstly, while charge carrier mobilities greater than that of amorphous silicon is a significant milestone for organic semiconductors, they are not sufficient to open the door to next-generation electronics applications, such as conformable displays based on OLED technology. For this, carrier mobilities on the order of $10 \text{ cm}^2/\text{Vs}$ will be required. Organic small-molecule semiconductors with hole mobilities at this level have been demonstrated and should they be amenable to processing as part of a small-molecule : polymer blend then this materials system would be among the very best yet reported. The blend devices tested in chapter 6 exhibited some of the best bias stability reported in the literature. Despite this, degradation of device performance was observed due to the effects of exposure to ambient air and elevated temperatures. For blend devices to be commercially viable these degradation pathways need to be further understood so that they can be mitigated. A density of states analysis performed on the field-effect measurements taken during device degradation may shed light on the origins of these damaging phenomena. Further, testing the blend devices under anticipated real-world conditions is also important. A simple first step here would be to investigate the stability of a blend OTFT when powering an OLED pixel under real-world conditions. Finally, further work is needed to develop the printing processes that will be needed to create electronic devices on a large scale. The work in this thesis makes a good first

step, though the technique of spray deposition needs to be optimized to achieve the high hole mobilities and device uniformity displayed by spin-casting. It is expected that many improvements may be easily achieved simply through automating the process of spraying the blend solution, which would enable much greater control of the deposition parameters. The beauty of the spray deposition technique is its simplicity, however with further work it may be possible to achieve laterally resolved patterning of both p- and n-type organic semiconductors. This would open the door to complementary logic circuits which achieve much greater operating characteristics than using a single semiconductor type alone.

The beginning of this thesis began with a quote from Donald G. Fink, an American electrical engineer and pioneer of radio navigation and television standards. Referring to the commercial future of the transistor, in 1953 he posed the question: “Is it a pimpled adolescent, now awkward, but promising future vigor? Or has it arrived at maturity, full of languor, surrounded by disappointments?” The same question could be posed about the future of the organic transistors. Much has been made of their potential to change how we think of electronic devices, and yet after years of research much work still remains. However, just as Fink’s concerns proved unfounded, organic transistors are constantly improving, with much work being conducted both at research institutions and industrially. The year after Fink posed his question the first transistor radio became publicly available, precipitating a revolution in electronic devices.

Appendix A

List of publications

Hunter S., Chen J., Anthopoulos T.D. Microstructural Control of Charge Transport in Organic Blend Thin-Film Transistors. *Advanced Functional Materials*, 24(38):5969-5976, 2014

Hunter S., Ward J.W., Payne M.M., Anthony J.E., Jurchescu O.D., Anthopoulos T.D. Low-voltage polymer/small-molecule blend organic thin-film transistors and circuits fabricated via spray deposition. *Applied Physics Letters*, 106(24):223304, 2015

Pitsalidis C.Pappa A-M., Hunter S., Payne, M.M., Anthony, J.E., Anthopoulos T.D., Logothetidis S. Electrospray-Processed Soluble Acenes toward the Realization of High-Performance Field-Effect Transistors. *ACS Applied Materials & Interfaces*, 7(12):6496-6504, 2015

Arumugam S. Cortizo-Lacalle D., Rossbauer S., Hunter S., Kanibolotsky A.L., Inigo A.R., Lane P.A., Anthopoulos T.D., Skabara P.J. An Air-Stable DPP-thieno-TTF Copolymer for Single-Material Solar Cell Devices and Field Effect Transistors. *ACS Applied Materials & Interfaces*, 2015

Appendix B

Decay of electric field strength in an organic semiconductor thin-film

As part of the derivation of the Grünewald model, it is assumed that the electric potential and electric field drop to zero within the semiconductor. To calculate the decay length of the gate field inside the semiconductor, the method proposed by Skinner for a film of finite thickness (t_{sc}) is used [211].

In equilibrium, i.e. constant gate field, the current in the semiconductor is equal to zero. Therefore the drift and diffusion components of current density must be equal to each other:

$$\mu p(x)F(x) = D \frac{dp(x)}{dx} \quad (\text{B.1})$$

where $p(x)$ is the hole density as a function of distance, x from the interface, D is the diffusion coefficient and $F(x)$ is the electric field in the material. Using Gauss' law which relates charge density to resulting electric field along with the Einstein relation, $D/\mu = k_B T/q$, this becomes:

$$F(x) \frac{dF(x)}{dx} = \frac{k_B T}{e} \frac{d^2 F(x)}{dx^2} \quad (\text{B.2})$$

Simplifying and integrating this produces the result:

$$\frac{2k_B T}{e} \frac{dF(x)}{dx} - F^2(x) = -g^2 \quad (\text{B.3})$$

where g^2 is constant of integration. The solution for this can be shown to be:

$$F(x) = \frac{2k_B T g}{e} \cot(g(x + x_0)) \quad (\text{B.4})$$

where x_0 is a constant of integration. By invoking the boundary conditions that the field at the semiconductor-insulator interface is F_0 and at the opposite side of the film $F(t_{sc}) = 0$ the final equation for hole density in a p-type semiconductor can be arrived at:

$$p(x) = \frac{2k_B T \epsilon_{sc} g^2}{e^2} \sec^2(g(t_{sc} - x)) \quad (\text{B.5})$$

where ϵ_{sc} is the dielectric constant of the semiconductor. g is derived numerically from the following equation:

$$\ln(\cos(gt_{sc})) - \frac{\epsilon_{sc} g}{C_{ins}} \tan(gt_{sc}) + \frac{eV_G}{2k_B T} = 0 \quad (\text{B.6})$$

The result of this calculation, using the typical gate biases of -10 to -60 V and a semiconductor dielectric constant of 3.5 is plotted in Figure B.1.

The decay length is estimated to be 1 nm (approximately the size of a single diF-TES ADT molecule [11]), while the thickness of the phase-separated crystalline layer in the blend devices is 20 nm [20]. Hence, the assumption of complete field decay within the semiconductor is valid.

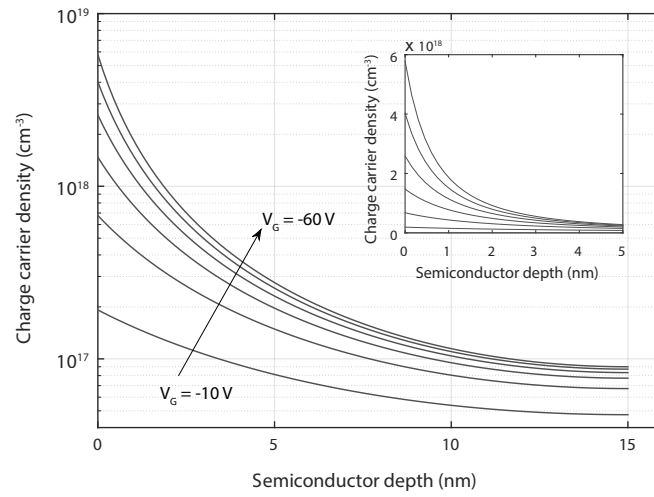
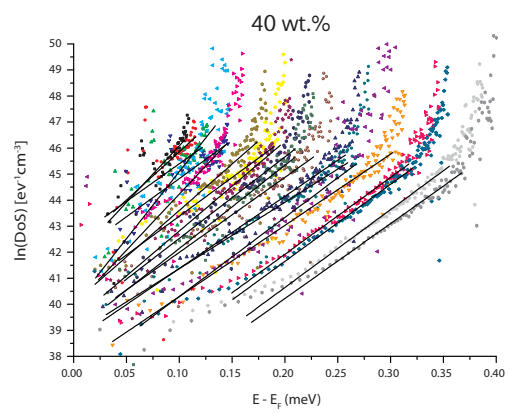
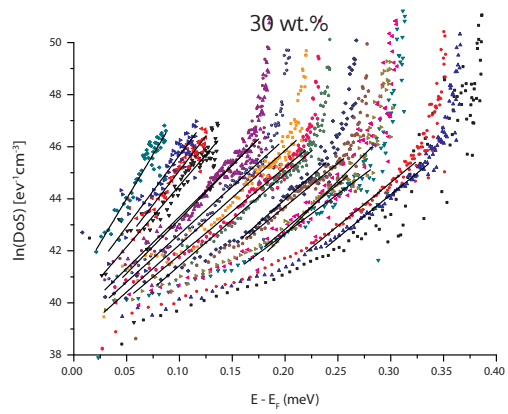
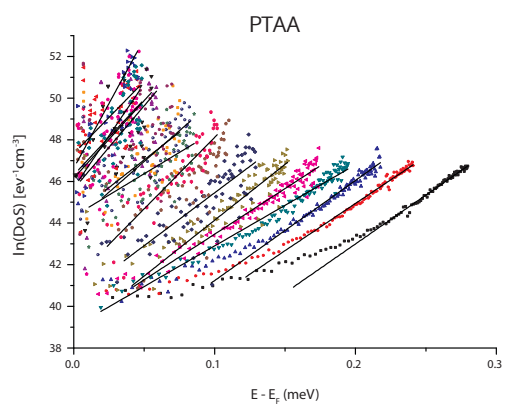
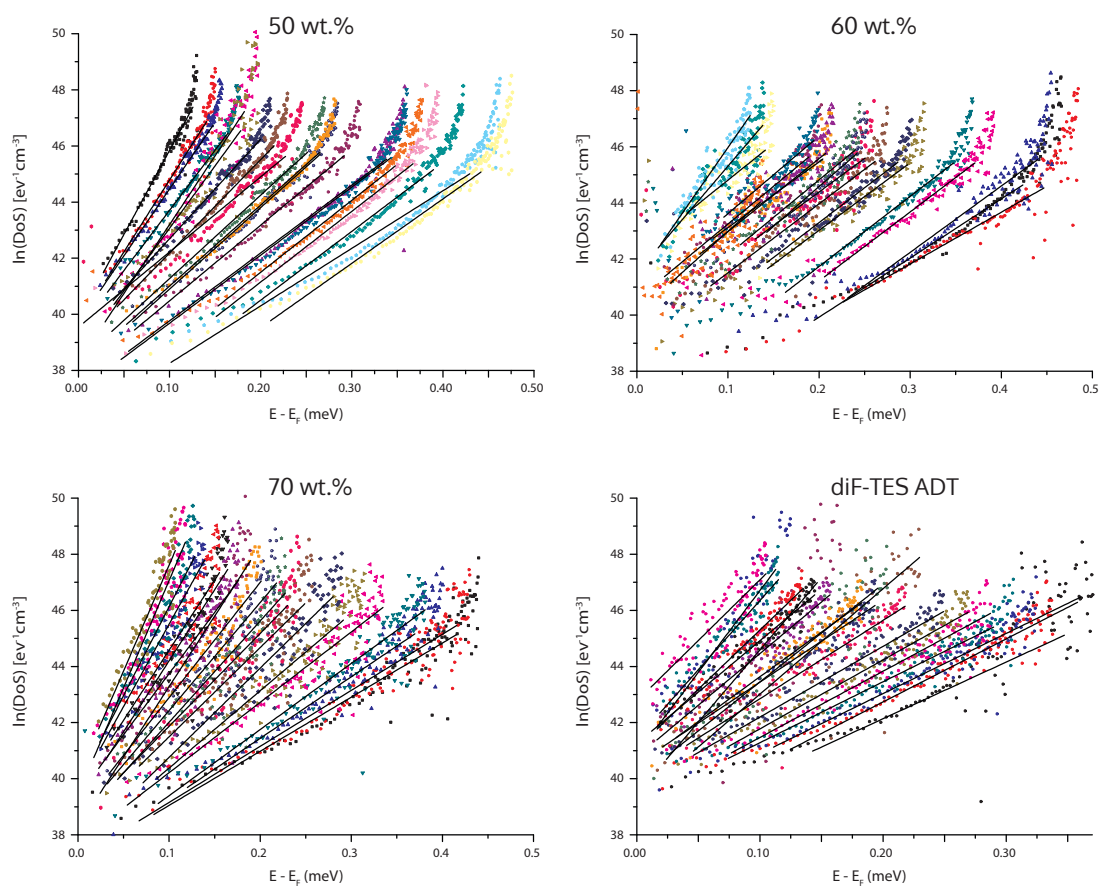


Figure B.1: Charge carrier density in a diF-TES ADT containing TFTs as a function of semiconductor depth from the channel, and at a range of gate biases.

Appendix C

Density of states plots and exponential fitting





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