A 1.5 μW NEO-based Spike Detector with Adaptive-Threshold for Calibration-free Multichannel Neural Interfaces

Ermis Koutsos*†, Sivylla E. Paraskevopoulou*† and Timothy G. Constandinou*†
*Department of Electrical and Electronic Engineering, Imperial College London, SW7 2BT, UK
†Centre for Bio-Inspired Technology, Institute of Biomedical Engineering, Imperial College London, SW7 2AZ, UK
Email: {e.koutsos11, s.paraskevopoulou09, t.constandinou}@imperial.ac.uk

***Abstract*—This paper presents a novel front-end circuit for detecting action potentials in extracellular neural recordings. By implementing a real-time, adaptive algorithm to determine an effective threshold for robustly detecting a spike, the need for calibration and/or external monitoring is eliminated. The input signal is first pre-processed by utilising a non-linear energy operator (NEO) to effectively boost the signal-to-noise ratio (SNR) of the spike feature of interest. The spike detection threshold is then determined by tracking the peak NEO response and applying a non-linear gain to realise an adaptive response to different spike amplitudes and background noise levels. The proposed algorithm and its implementation is shown to achieve both accurate and robust spike detection, by minimising falsely detected spikes and/or missed spikes. The system has been implemented in a commercially available 0.18 μm technology requiring a total power consumption of 1.5 μW from a 1.8 V supply and occupying a compact footprint of only 0.03 mm^2 silicon area. The proposed circuit is thus ideally suited for high-channel count, calibration-free, neural interfaces.**

I. Introduction

With the advert of microtechnology and the increased capability of neuroprosthetic devices has led to the development of fully implantable wireless systems, capable of monitoring hundreds of neurons. Moreover, with ever-advancing high density micro-electrode arrays (MEAs) the capability will soon be extended from recording 100s to 1000s of channels simultaneously [1], [2].

Extracellular action potentials (EAPs) typically have amplitudes between 25 μV and 1 mV, with a frequency spectrum of between 300 Hz to 3 kHz. The variation in amplitude (from neuron to neuron) depends on each neuron's morphology, as well as its proximity and orientation relative to the recording electrode. Using current MEAs (eg. Utah arrays), each channel can observe the activity of up to five neurons [3]. In order to extract the maximum amount of information from every channel, each spike must be classified to specific neuron activities. To achieve this, current systems amplify, condition, digitise and transmit the raw neural recordings to an external device for post-processing (eg. a workstation). Considering a typical MEA (eg. 100 channels), with the recording sampled at 10-bit resolution, at 30 kS/sec, the required data-rate is 30 Mbit/sec. It is however a significant challenge to increase the communication bandwidth due to limitations imposed by the maximum allowable thermal dissipation [4], [5].

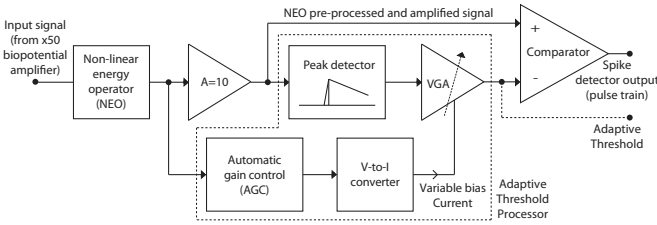


Fig. 1. System-level block diagram of the adaptive-threshold spike detector.

The desire, therefore, to increase the number of channels requires the amount of data transmitted per channel to decrease. One solution is to only transmit specific spike features, for example a simple spike event timing. There as been much work on front-end spike detection, eg. [6]–[8]. The simplest designs use a constant threshold to detect the spike using a comparator. However, due to both the noisy nature of neural recordings (eg. background activity, electrode noise/offset, etc) and the large variability in spike shapes and amplitudes, predefining a set threshold in not sufficient.

The need for external monitoring and calibrating each channel's threshold is thus essential for maintaining spike detection accuracy. This has given rise to adaptive algorithms for selecting this threshold level. The basic concept behind such methods is to estimate the background noise level of the input signal and set the threshold as a constant multiple of that value [4], [9]–[11]. Other methods utilise a signal pre-processor, for example, a non-linear energy operator (NEO) [12], [13] to boost the effective SNR. The NEO gives an estimate of the signals instantaneous change in amplitude and frequency and this makes it ideal for spike detection [14]. Nevertheless, applying constant thresholds to this for spike detection is not still universally robust.

This paper presents a novel CMOS neural spike detector circuit with adaptive threshold and NEO pre-processor. This paper is organised as follows: Section II presents the spike detector system concept, Section III the circuit implementation, Section IV the results, and finally Section V the conclusion.

II. Adaptive Threshold Algorithm

A system-level block diagram of the proposed adaptive threshold spike detector is shown in Fig. 1. This consists of a NEO pre-processor feeding an adaptive threshold processor to set the detection level. The NEO output is then compared

to the adaptive threshold using a 2-stage comparator. It should be noted that the spike detector has been designed to take its input after front-end pre-amplification and high-pass filtering. Specifically a front-end gain of 50× is assumed, mapping to a 1.25 mV to 50 mV EAP input range.

The adaptive threshold processor is is annotated in Fig. 1 (within dotted line). The input signal is fed to the NEO and then, amplified by a constant gain of 10. A peak detector tracks the amplified-NEO maxima, but in the absence of a spike, the output signal decreases with time due to leakage. The non-amplified NEO signal is fed to a variable gain stage, where the threshold is calculated. The variable threshold is initially set at 60% of the peak-detector's output. As the NEO signal increases in amplitude, the variable threshold decreases, reaching a minimum of 15% of the peak-detector output. This essentially reduces the sensitivity for small spikes compared to larger ones and ensures that even when the peak-detector output has leaked to a very low value, the threshold will still be above the background noise. Furthermore, this system exploits the peak detector leakage, by physically lowering the threshold as time progresses, assuring the detection of a small spike following a much larger spike. A V-to-I converter controls the gain of the variable gain amplifier. Finally, a spike is detected when the amplified-NEO signal crosses the variable threshold.

III. Circuit Implementation

The circuit has been implemented in a commercially available 0.18 μm CMOS technology provided by AMS (C18A4).

A. Non-linear Energy Operator

The Non-linear Energy Operator (a.k.a. Tieger operator) is known to be very effective in spike detection, especially for signals with very low SNR. The NEO output is proportional to the square of the instantaneous product of a signals amplitude and frequency, described by Eq. 1:

$$v_{(x(t))} = \left(\frac{dx(t)}{dt}\right)^2 - x(t) \cdot \left(\frac{d^2x(t)}{dt^2}\right) \tag{1}$$

The analog NEO implementation has been adapted from [13]. Fig. 2(a) shows the circuit diagram of the analog NEO implementation. The sub-threshold OTAs used in the NEO circuit (shown in Fig. 2(b)) use source degeneration (M_{s1}, M_{s2}) and bulk linearisation (M_{b1}, M_{b2}) to achieve low transconductances and an increased linear input range. Since the OTAs are operating in the sub-threshold region, the transconductance g_m is lineally proportional to the bias current I_{bias}. The relation is shown below in Eq. 2,

$$g_m = \frac{I_D}{nV_T} \tag{2}$$

Where V_T is the thermal voltage. The differentiator implementation is shown in Fig. 2(c). Considering the transfer function of the differentiator (Eq. 3), in order to achieve the required magnitude in the output signal of the NEO, a gain of 10 was selected. To achieve this, g_{m1} and g_{m3} are biased with a current of 5 nA and g_{m2} with a current of 50 nA.

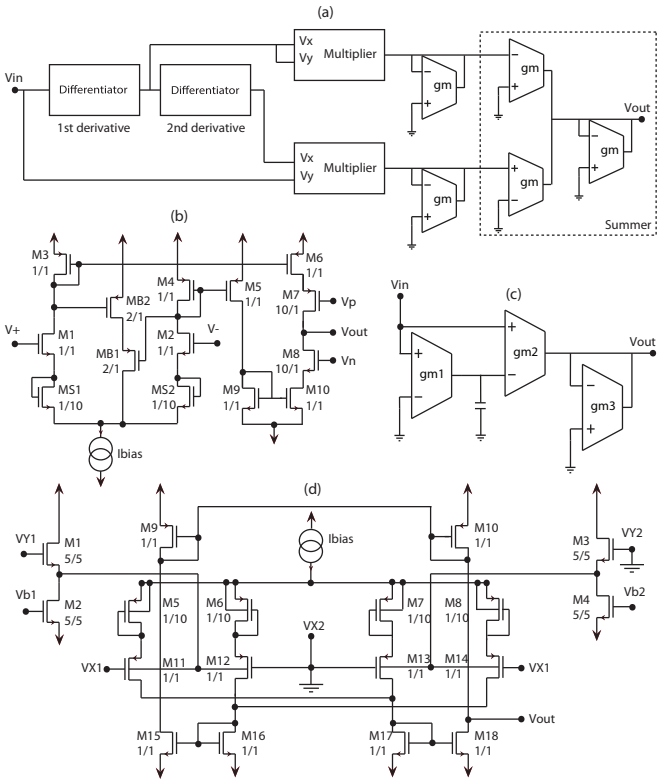


Fig. 2. Circuit implementation of the NEO. Shown are: (a) NEO system-level block diagram, (b) sub-threshold OTA circuit, (c) differentiator circuit, (d) four-quadrant analog inverting multiplier circuit.

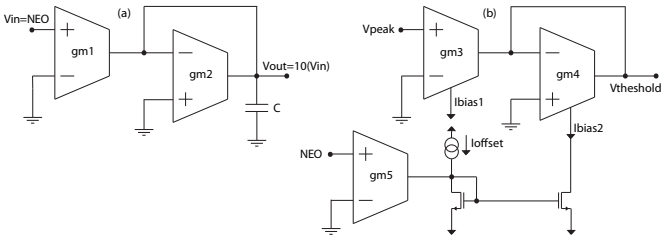


Fig. 3. Circuit implementations of: (a) fixed-gain non-inverting amplifier, (b) variable gain non-inverting amplifier feeding the automatic gain control.

$$\frac{V_{out}}{V_{in}} = \frac{j\omega C}{j\omega C + g_{m1}} \cdot \frac{g_{m2}}{g_{m3}} \tag{3}$$

Finally, Fig. 2(d) presents the four-quadrant analog multiplier used, for a bias current of 30 nA and achieving a 40 mV linear range. Transistors (M_1, M_2) and (M_3, M_4) level-shift $V_{y1}, V_{y2})$ down by 500 mV (from 900 mV to 400 mV).

B. Fixed Gain Amplifier

The non-inverting amplifier used to amplify the NEO signal is shown in Fig. 3(a). This utilises a similar OTA as to those used in the NEO circuit (Fig. 2(b)), but with an increased linear output range (300 mV). This is achieved by designing transistors (M_{b1}, M_{b2}) to have an aspect ratio of (W/L)=8/2 (μm/μm). The gain of the amplifier is set by the ratio (g_{m1}/g_{m2}) and since the OTAs are operating in the sub-threshold region, this becomes (I_{bias1}/I_{bias2}). The gain of the amplifier is fixed to 10 (I_{bias1}=50 nA and I_{bias2}=5 nA).

C. Peak Detector

The purpose of the peak detector is to track the input signal as it increases, but not as it decreases, thus storing the maximum amplitude of the signal. The design and operation of the peak detector circuit are detailed in [3]. The basic operation uses a switch to charge a capacitor for increasing signals. For decreasing signals the switch is left open so a decay is implemented by adding a leakage. To match the dynamics of the peak detector to the NEO output for the minimum controllable leakage, the NEO signal is pre-amplified with a gain of 10 and a capacitor of 3 pF is used.

D. VGA and AGC

The circuit for the VGA and AGC is shown in Fig. 3(b). The gain of the variable gain amplifier (VGA) is controlled by the current ratio (I_{bias1}/I_{bias2}). This ratio is controlled by the automatic gain control (AGC) which takes the NEO input and provides a varying bias current I_{bias2}. The OTAs used in this circuit are similar to those in Fig. 2(b), but without source degeneration or bulk linearization. Assuming a voltage input to the OTA with a range of 30 mV (typical NEO output), the output current of the OTA will vary from 300 pA to 30 nA. A bias current of 300 pA would however be too low to drive the VGA (for linear operation) and thus an offset bias is added (I_{offset}=10 nA). The total current is mirrored and forms the I_{bias2} current, with I_{bias1}=6 nA. Thus, the variable threshold is $V_{th} = V_{peak} \times G$, where G is the variable gain $(0.6 \leq G \leq 0.15)$ and V_{peak} is the output of the peak detector.

E. Comparator

The comparator used for the evaluating the spike detection is a standard two-stage topology with regeneration (i.e. utilising symmetric cross-coupling) using I_{bias}=40 nA per stage.

IV. Simulated Results

The complete system was simulated using the Cadence Spectre (5.1.41isr1) simulator, with foundry supplied PSP models. The datasets used for the simulations were obtained from [15] containing 4 datasets (easy1, easy2, difficult1, difficult2) each created with different noise levels (0.05, 0.1, 0.15, 0.2) and sampled at 24 kHz. For these simulations, the test datasets have been scaled to a 50 mV full-scale range (i.e. corresponding to approximately a $\times$50 pre-amplification).

1) Transient Analysis: A simulation over a 40 ms period of the test signal containing three spikes is shown in Fig. 4. This illustrates the operation of the adaptive threshold, in particular observing: (1) the SNR of the input signal is boosted by the NEO pre-processor, (2) the peak signal tracks the NEO maxima, (3) in the absence of a spike, the adaptive threshold follows the peak signal trend, and (4) in the presence of a spike, the adaptive threshold dips (see magnified feature), effectively increasing the spike detection sensitivity.

An extended transient analysis over a 1 s period is shown in Fig. 5 illustrating the longer term operation of the circuit. In particular, this demonstrates the operation of the variable threshold achieves good robustness to noise and varying spike amplitudes. The delay between the action potential and the output pulse is negligible (less than 100 μs).

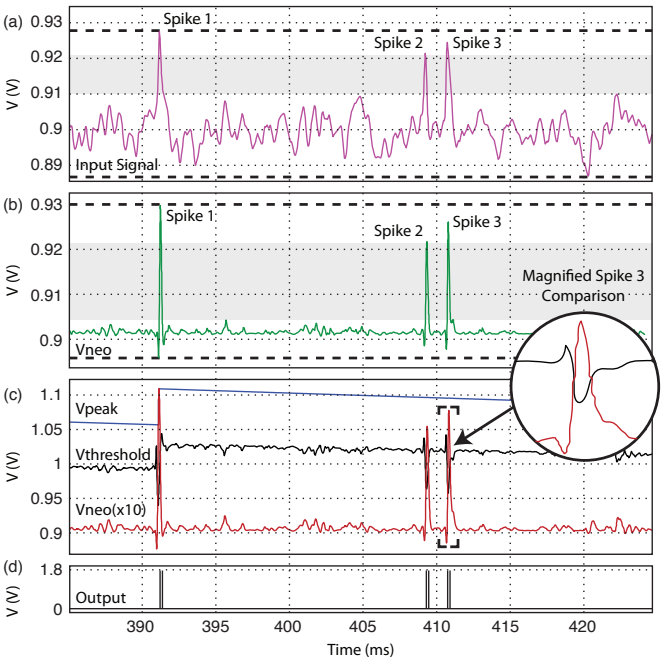


Fig. 4. Operation of the adaptive threshold detector over a 40 ms period (for difficult01 dataset at 0.2 noise level [15]). Shown are: (a) input, (b) NEO signal, (c) amplified NEO, peak tracking and adaptive threshold, and (c) comparator output. For (a, b): shaded area indicates the signal to noise margin, and horizontal dashed lines indicate the signal range (for 40 ms segment).

2) Spike Detection Sensitivity: The performance of the proposed method (i.e. adaptive-threshold spike detection) has been quantified through a series of MATLAB simulations. This is compared to 3 spike detection methods utilising optimally-set thresholds, based on: (A) input signal compared to $\alpha\times(V_{peak})$, (B) NEO signal compared to $\beta\times$(average

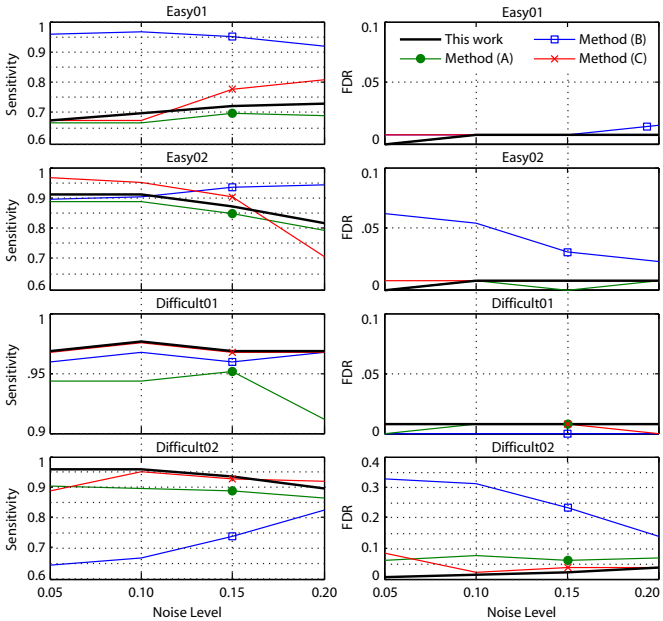


Fig. 6. Spike detection sensitivity and FDR of spike detection using the proposed adaptive threshold method compared to applying optimally-selected thresholds (across multiple test datasets and noise levels) [15].

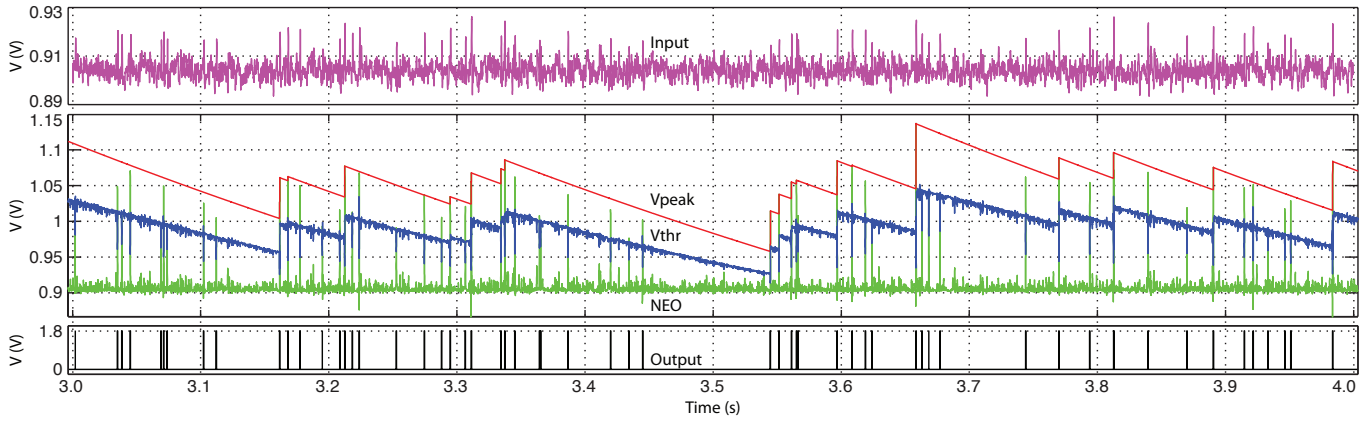


Fig. 5. Spike detector operation over a 1 s period (for difficult01 dataset at 0.2 noise level [15]). Shown are: (a) input, (b) amplified NEO, peak tracking and adaptive threshold, and (c) output.

NEO signal), (C) NEO signal compared to $\gamma\times$(maximum NEO amplitude). Each of these threshold-selection constants (α, β, γ) have been obtained through an exhaustive search across all datasets and noise levels. The proposed method however does not require any calibration. Fig. 6 shows the sensitivity ($=\frac{detected\ \ spikes}{present\ \ spikes}$) and false detection rates (FDR=$\frac{false\ \ positives}{total\ \ detections}$) for each method. It can be observed that the proposed method achieves good performance through multiple datasets and noise levels.

V. Conclusion

This paper has presented a novel fully-autonomous spike detector detailing its circuit implementation. The system is capable of detecting spikes in real-time and with minimal delay, without the aid of external monitoring and/or the need for calibration. The system features a NEO pre-processor and adaptive threshold engineered to maximize both the accuracy (minimising false positives and/or false negatives) and robustness (to signal variability). The total area required for this design has been estimated by summing all the active device areas and adding an additional 400% overheard to account for contacts and interconnects. This results in a total (estimated) area requirement of 0.03 mm^2, implemented in a commercially available 0.18 μm CMOS technology. The circuit consumes a total power of 1.5 μW (excluding bias generation) from a 1.8 V supply. A comparison between this work and the state-of-the-art is shown in Table I.

TABLE I
Table comparing this system with the state-of-the-art.

Detector	Pre-Processor	Adaptive Threshold	Area (mm^2)	Power (μW)	Tech. (μm)
[4]	✗	✓	0.09	57	1.5
[6]	✓	✗	0.06	1	0.5
[8]	✓	✗	0.09	0.8	1.5
[9]	✓	✓	0.17	1	0.13
[10]	✓	✓	9	110	0.6
[13]	✓	✗	0.07	0.78	0.18
[16]	✓	✗	0.06	1	0.5
This work	✓	✓	0.03 (est.)	1.5	0.18

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