

Fabrication Techniques for a Tuneable Room Temperature Hybrid Single-electron Transistor and Field-effect Transistor

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ARTICLE INFO

Keywords:

Room-temperature single-electron transistor
finFET
Nanofabrication
Silicon quantum dots
electron beam lithography
Coulomb blockade

ABSTRACT

Hybrid room-temperature (RT) silicon single-electron – field effect transistors (SET-FETs) provide a means to switch between ‘classical’, high current FET, and low-power SET operation, using a gate voltage. While operating as a SET, charge on a silicon quantum dot (QD) within the current channel, can be controlled at the one-electron level using the Coulomb blockade effect. This paper investigates nanofabrication methods for sub-10 nm ‘fin’ channel hybrid RT SET-FETs, and their influence on the energy band diagram, and formation of tunnel barriers and QDs, along the channel. Devices are fabricated in heavily *n*-doped SOI material using electron beam lithography, with thermal oxidation to reduce the as-defined fin width. Effective channel dimensions, following oxidation and excluding Si/SiO₂ interface dopant deactivation, are $\sim 2.4 \text{ nm} \times 32 \text{ nm} \times 20 \text{ nm}$. Dopant disorder, fin width variation at the nanometre scale, and quantum confinement effects are considered as mechanisms for the formation of tunnel barriers and QDs, with dopant disorder the most likely reason. Arrhenius plots of I_{ds} vs. $1/T$ allow extraction of a potential barrier energy $\sim 0.2 \text{ eV}$ along the fin channel. For 180 devices fabricated on four chips, 37% show RT SET-FET operation, ~ 3 times higher than the corresponding yield observed in previous work on point-contact silicon SETs.

1. Introduction

In recent years, the continuation of Moore’s law has led to a reduction in minimum feature size of Si fin metal-oxide-semiconductor field-effect transistors (MOSFETs) to sub-10 nm scales. Minimum length scales for planar MOSFET structures were reduced from $\sim 10 \mu\text{m}$ in 1971 to $\sim 32 \text{ nm}$ in 2009 (Fig. 1(a)) [1]. For minimum lengths below $\sim 20 \text{ nm}$, increasing difficulty in controlling short channel effects led to a transition from planar to 3D channel structures, e.g. FinFETs and gate-all-around (GAA) FETs. These devices, which create stronger gate control using a gate covering three or all four sides of the channel (Fig. 1(a)) have enabled a continuation of Moore’s law scaling from the 16 nm fabrication node onwards [1,2]. However, the complexity of fabrication and associated costs are increased for sub-10 nm fin and GAA FETs and the use of advanced lithographic techniques, e.g., extreme ultraviolet (EUV) lithography, is expected [3–5]. Apart from the complex fabrication process, a further reduction in channel dimensions to the few nanometre scale raises the possibility of significant quantum mechanical effects, leading at the minimum to increases in the threshold voltage V_{th}

[6,7]. Furthermore, the presence of structural or material disorder along the channel can lead to the formation of tunnel barriers along the fin near V_{th} [8], confining quantum dots (QDs) in between these barriers. Single-electron charging and quantum confinement effects can occur in the QDs, and for the case of QD size $< 10 \text{ nm}$, quantum confinement energy E_k and single-electron charging energy $E_c = \frac{e^2}{2C} \gg k_B T = 26 \text{ meV}$ at room temperature (RT, temperature $T = 300 \text{ K}$), where QD capacitance $C \sim 10^{-18} \text{ F}$ or less [9–11]. This leads to single-electron transistor (SET) behaviour in the electrical characteristics even at RT. While these effects complicate classical FET operation, they raise simultaneously the possibility of devices where digital bits are defined by only a few, or even single electrons enabling the fabrication of ultra-low power nanoelectronic circuits [9–11].

Room temperature QD SETs in silicon can use various QD geometries, e.g., nanochannels [12–15], nanocrystals [16–18], and nanowires [19,20]. In our previous work, we have demonstrated RT QD SETs with very large single-electron addition energies, $E_a = E_k + E_c \sim 0.1\text{--}0.4 \text{ eV}$ [21–23], using Si/SiO₂/Si point-contact SETs fabricated in silicon-on-insulator (SOI) material. Hence, the QDs are formed by phosphorous

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(P) dopant atoms embedded in SiO₂ tunnel barriers. Recently [8], we have demonstrated hybrid RT SET-FET operation in Si FinFETs using a few nanometre wide Si channel. The electrical characteristics of these devices show classical FET operation for a gate voltage $V_{gs} > V_{th}$ and SET operation for $V_{gs} \sim V_{th}$.

In this work, we investigate the nanofabrication of sub-10 nm ‘fin’ channel hybrid SET-FETs, and mechanisms for formation of tunnel barriers and QDs along the channel. The effective dimensions of the fin channel in our devices are $\sim 2.4 \text{ nm} \times 32 \text{ nm} \times 20 \text{ nm}$, following oxidation and excluding a Si/SiO₂ interface dopant deactivation layer. Devices are defined in heavily *n*-doped (phosphorous doping at $\sim 3 \times 10^{19} \text{ cm}^{-3}$) SOI material using high-resolution electron beam lithography (EBL), pattern transfer by reactive ion etching, and thermal oxidation to reduce channel width. The devices consist of source (S) and drain (D) areas connected by a fin or ‘point-contact’ channel, with two side gates (G) for channel current modulation (Fig. 1(b-c)). Arrhenius plots of the device drain-source current (I_{ds}) vs. inverse temperature are measured, allowing extraction of the energies of potential barriers along the fin channel. Statistics for functional/non-functional devices on four chips, each containing 45 devices, are presented. It is found that $\sim 37\%$ of devices show RT SET-FET operation. Finally, an energy band model is presented for the device, to explain the mechanism for QD and tunnel barrier formation and hence the electrical characteristics.

2. Device fabrication

A summary of the fabrication steps is shown in Fig. 2(a). A $\langle 100 \rangle$ oriented silicon-on-insulator (SOI) wafer was used, where the thickness of top Si layer was 120 nm and of the buried oxide (BOX) layer was 2 μm , Fig. 2(b). However, for SET-FET operation, the thickness of the top Si layer needed to be 30–50 nm, with a doping density of $\sim 10^{19}$ – 10^{20} cm^{-3} P atoms. To achieve this, the SOI wafer was first oxidised in a furnace at 1000 °C for 4 h, resulting in $\sim 70 \text{ nm}$ of the top Si layer oxidised to SiO₂. This layer was then removed by HF etching, to obtain a top Si layer thickness of $\sim 50 \text{ nm}$ or less. The thinned top Si layer was doped using spin-on dopant solution containing P atoms, PCD1–2000. This was spin coated, initially at 500 rpm for 10 s, followed by 1500 rpm for 50 s (Fig. 2(c)). A hot-plate bake at 200 °C for 10 min was used to drive-off solvent, followed by rapid thermal annealing (RTA) at 950 °C for one

minute to drive in dopant atoms. Four-point probe electrical measurements were conducted (see Supplementary material, Fig. S1) to measure the top Si resistivity and hence extract carrier concentration and estimate doping density. The sheet resistance $R_s = 772 \Omega$, was extracted using a correction factor $CF \sim 4.54$ for our probe separation. This corresponded to resistivity $\rho = R_s \times W = 3.08 \times 10^{-3} \Omega \cdot \text{cm}$, where W is the thickness of the top Si layer, and hence doping concentration $\sim 3 \times 10^{19} \text{ cm}^{-3}$ [24].

The RT SET-FET pattern had a central device region, which comprised source, drain, 20 $\times$ 20 nm fin channel, and gate electrode regions. The gate-fin separation was 200 nm (see Fig. 1(b)). Electrical lead-in regions were taken out from the device region to 200 μm square contact pads defined around the chip perimeter. Electron beam pattern exposure was performed using a Raith VB6-UHR machine at 100 kV. To minimise overall write times, the pattern data was split, with the high-resolution central region, i.e., the device area, exposed using a beam current of 7.8 nA and beam diameter of $\sim 3 \text{ nm}$. The low-resolution areas, i.e. lead-in and contact pad areas, were exposed with a beam current of 184 nA and beam diameter of $\sim 70 \text{ nm}$. Bilayer poly(methyl methacrylate) (PMMA) resist was used for pattern generation and subsequent ‘lift-off’ to define an aluminium (Al) hard mask. The lower layer had molecular weight MW of $\sim 100 \text{ k}$ and the top layer $\sim 950 \text{ k}$, with each layer baked after coating, at 180 °C for 3 min. Both layers had a thickness of 50 nm. Resist was developed in MEK: MIBK: IPA in the ratio of 1: 5: 10 for 10 s, rinsed in IPA and blown dry. A 30 nm thick layer of Al was then deposited by thermal evaporation at a rate of $\sim 0.7 \text{ \AA/s}$ at $\sim 10^{-6}$ mbar. The chip was soaked in acetone overnight to remove the excess metal by lift-off.

The patterned 30 nm layer of Al acted as a hard mask for etching the top silicon layer using reactive ion etching (RIE) (Fig. 2(e)). A gas flow of 30 sccm SF₆ and 10 sccm O₂ was used, at 50 mTorr pressure and 100 V bias. After 50 s, an etch depth of $\sim 70 \text{ nm}$ was obtained, sufficient to transfer the Al hard mask pattern into the top Si layer. The RIE parameters had to be tuned precisely to avoid over-etching, which could result in a significant undercut because of the different etch rates of Si and SiO₂ (Supplementary material, Fig. S2). The Al hard mask was removed by immersion in ‘type A’ Al etchant, a mixture of H₃PO₄: CH₃COOH: HNO₃ in the ratio of 7: 2: 1, for 15 min (Fig. 2(f)).

Following the RIE process, the chip was oxidised in a furnace at 1000

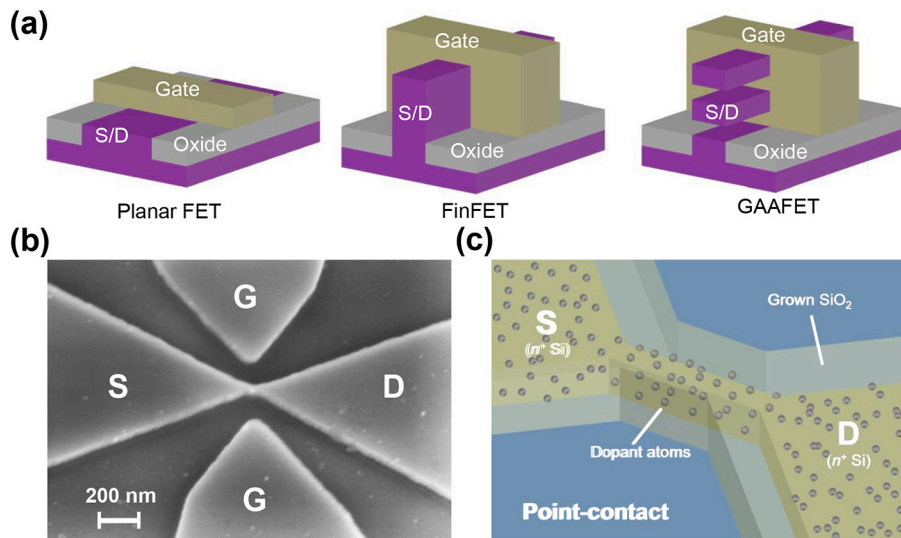


Fig. 1. (a) Schematic diagrams for planar FET (left), FinFET (middle), and GAAFET (right). (b) Scanning electron micrograph of an RT SET-FET, fabricated in SOI material. (c) Schematic diagram of the RT SET-FET. Source, drain, and fin channel point-contact regions are defined in the highly doped top Si layer. Dopant atoms (P) lie within the fin, with position randomness around average separation $\sim 2 \text{ nm}$. Dopant atoms may be isolated by depleted silicon regions for greater dopant separation, or channel pinch-off regions due to non-uniform growth of surface SiO₂ (not shown in schematic for clarity), tunnel-isolating quantum dots for SET operation.

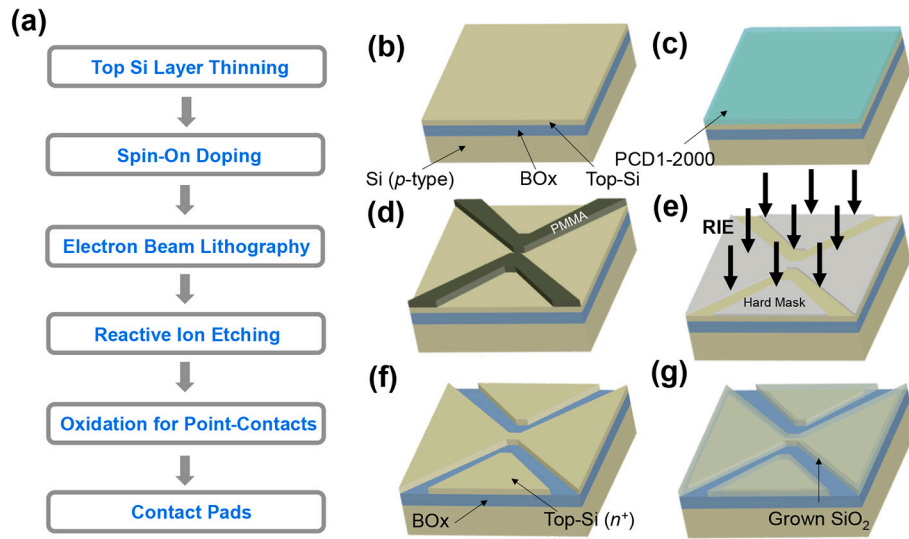


Fig. 2. (a) RT SET-FET fabrication process flow. (b-g) Device region schematic diagrams, at different stages of the process flow. (b) Schematic diagram of silicon-on-insulator wafer after thinning process which ensures a small volume for the subsequent Si fin and hence a small number of dopant atoms. (c) A layer of PCD1-2000, dopant solution with phosphorous atoms for spin-on doping process, is spin-coated and baked on the thinned top Si layer. (d) Electron-beam lithographic patterning with bilayer PMMA, for Al hard-mask definition. (e) Reactive ion etching to transfer the hard-mask drain, source, and point-contact pattern into the top Si layer. (f) Silicon fin on BOx. (g) SET-FET fin channel and dopant atom quantum dots are formed following reduction of the fin volume by oxidation.

°C for 15 min to grow ~16 nm thick SiO₂ to thin the fin channel region. The fin dimensions before oxidation were ~20 nm (width W) × 20 nm (length L) × 50 nm (height H). ~7 nm thick regions of the Si fin surfaces were converted to SiO₂ during oxidation, reducing the volume of the Si

channel region to ~6 nm (W) × 20 nm (L) × 36 nm (H), surrounded by ~16 nm thick SiO₂ (Fig. 2(g)). The thickness of oxide was measured using HF etch back on a dummy sample, oxidised at the same time as the SET-FET sample. Assuming that 45% of the grown oxide was associated

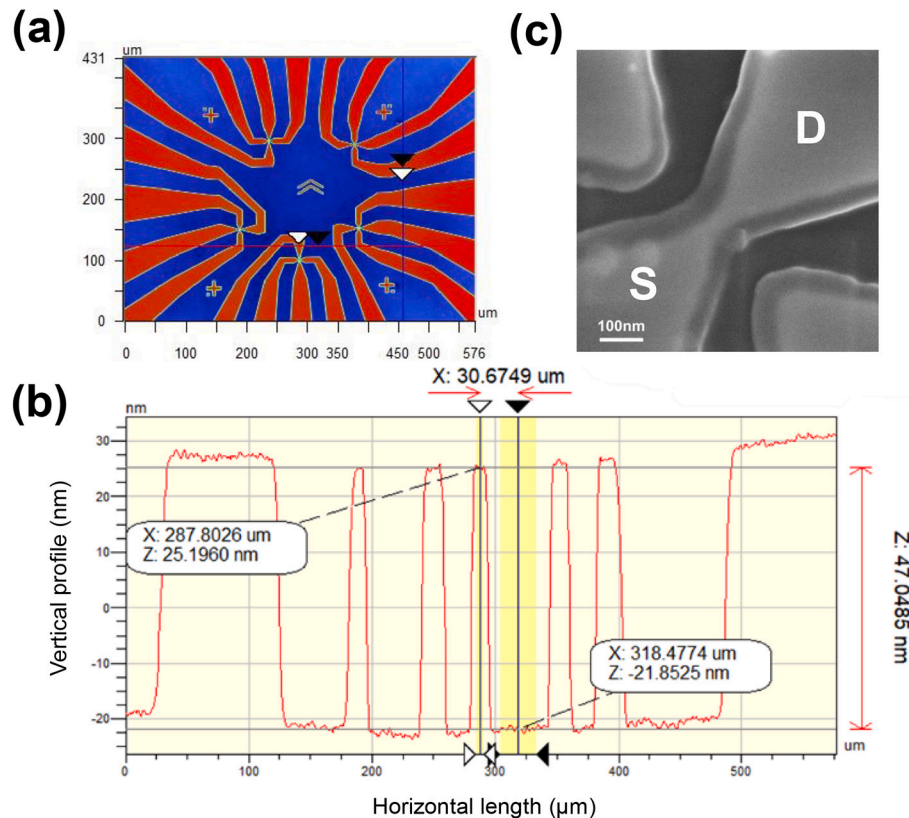


Fig. 3. (a) and (b) Interferometry measurements of etched SET-FET structures. (a) 2D map of the interferometry result, where the change of colour from red to blue indicates the lowest to highest point in the measured area. (b) Line scan profile corresponded to (a). The z-axis shows the topographical profile of the etched structures along the x-axis. The highlighted area is used for etched depth determination. (c) SEM micrograph of a SET-FET device, where the brighter Si channel, embedded in a darker oxide region can be resolved. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

with consumption of Si, an estimation of the width of the silicon fin region was possible. To form a hybrid RT SET-FET, the thickness of oxide needed to be precise. On the one hand, over-oxidation resulted in a fully oxidised fin region without a Si channel for FET operation mode, whereas on the other, under oxidation resulted in a resistive channel without transistor behaviour (Supplementary material, Fig. S3).

The final process step in the fabrication sequence was to evaporate contact pads on the chip, for subsequent electrical measurement. To define the contact pad regions, a photolithography process was used, with a Quintel Q4000 mask aligner and S1813 photoresist. The resist was spin-coated on the chip using 1000rpm/s acceleration to 5000 rpm spin speed, then held for 60 s, before baking on a hot plate at 110 °C for 10 min. The contact pad regions were exposed under UV light for 60 s and developed in MF-319 for 60 s. The chip with contact pad patterns was dipped in HF for 10 s to remove SiO₂ in the contact pad windows. A 30 nm thick layer of chromium (Cr) was evaporated at a deposition rate of 0.5 Å/s on the top Si layer at chamber pressure $\sim 10^6$ mbar. This was followed by a 300 nm thick layer of Al, evaporated on the Cr layer, at a deposition rate of 7 Å/s. The thin layer of Cr was used to improve contact adhesion between the Al and top Si, with Al chosen as the main Ohmic electrode material. Finally, the S1813 photoresist and excess metal was removed by lift-off in acetone.

Fig. 3(a) shows a false colour image of the central device and electrical lead-in regions in a 5-device group, obtained using a Veeco NT9100 surface profiler, via phase-shift interferometry. Fig. 3(b) shows a 580 μm long line scan through this region. Interferometry allows single nanometre scale measurement of surface roughness and etch depths, following completion of fabrication, over a large planar area $\sim 500 \mu\text{m}$ square. In Fig. 3(b), the mesa regions correspond to unetched areas, and the valleys correspond to etched areas. An etched depth of ~ 47 nm, just into the BOx layer, is measured using average values within the dark yellow shaded region. Surface roughness in the unetched area can be created during the top-Si thinning process. However, the surface roughness is within the noise floor amplitude of our measurement, <5

nm. This is further confirmed by atomic force microscopy (AFM) of the fin region (see Supplementary material, Fig. S4), where a surface roughness ~ 1 nm is observed.

Fig. 3(c) shows a scanning electron micrograph (5 kV accelerating voltage) of a test SET-FET device post-oxidation, for investigation of the Si/SiO₂ interface and calibration of device thermal oxidation. High resolution scanning-electron microscopy has been shown previously to enable imaging of Si nanowires embedded within SiO₂ in planar FETs/SETs. [25]. In Fig. 3(c), the contrast between the brighter Si channel (40 nm minimum width) and encapsulating, darker SiO₂ region (58 nm wide on both sides) can be observed. There is a gradual transition in width from the source/drain regions into Si channel and roughness or sharp corners are not observed, implying that abrupt changes in stress due to external morphology are unlikely.

3. Electrical characterisation

The electrical characteristics of a RT SET-FET are shown in Fig. 4. Fig. 4(a) shows I_{ds} in colour scale vs. V_{ds} and V_{gs} . The characteristics in (a) can be divided into three operational modes. These comprise device ‘off mode’, ‘SET mode’, and ‘FET mode’, as a function of V_{gs} , indicated by the vertical white lines at threshold voltages $V_{th} \sim -0.6$ V (threshold above which SET mode begins) and $V_{th}^+ \sim 0.2$ V (threshold above which FET mode begins). A classical fin channel is formed for the FET mode, for $V_{ds} = 0.1$ V (white line). For $V_{gs} > V_{th}^+$, the device is operated in a ‘FET mode’ and behaves as a classical FET with classical linear and current saturation features. Both linear and current saturation regions can be observed in the I_{ds} vs. V_{ds} output characteristics (Fig. 4(b)). For the near threshold region, $V_{th}^+ > V_{gs} > V_{th}$, diamond-like lower current regions (marked by white solid lines, drawn parallel to contour lines of constant current of ~ 1 nA) are observed. As our measurement is at 300 K, a thermally activated current is observed down to our noise floor of ~ 10 pA even within the diamond-like regions. As current increases more rapidly from ~ 1 nA, this value may be chosen as a current threshold and

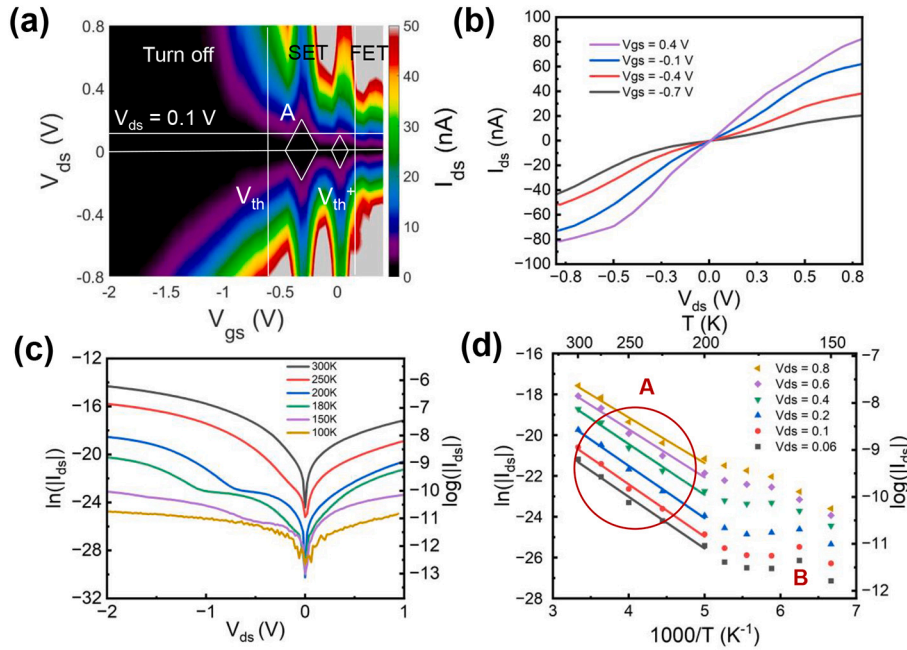


Fig. 4. I_{ds} vs. V_{ds} and V_{gs} characteristics for a SET-FET, shown in colour scale (a). Measurement obtained at room temperature, 300 K. These characteristics can be divided into three operational modes with different V_{gs} : (i) Off mode, (ii) SET mode, and (iii) FET mode, see (a). Edges of two Coulomb diamond regions in the device in SET mode are marked with white lines, where the large diamond is labelled as ‘A’. (b) The I_{ds} vs. V_{ds} characteristics in FET mode. The curve shows conventional FET behaviour for different values of $V_{gs} = 0.4$ V (purple), -0.1 V (blue), -0.4 V (red), and -0.7 V (grey). (c) $\ln(|I_{ds}|)$ vs. V_{ds} characteristics from 300 K to 150 K with the gate terminal floating. (d) Arrhenius plot of $\ln(|I_{ds}|)$ vs. $1000/T$ corresponding to the measurements in (c). $\ln(|I_{ds}|)$ is linear with $1000/T$ from 300 K to 200 K (region A) and current peak (B) is observed at lower temperature. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

contours at this value allow the diamond-like regions to be more clearly defined. These regions (Fig. 4(a)) may be attributed to single-electron Coulomb blockade regions in the presence of thermally activated current. Our measurements are performed at 300 K and at lower temperatures, the current within the Coulomb diamond regions reduces greatly (e.g., I_{ds} - V_{ds} characteristics vs. T in Fig. 4(c)). The larger diamond is more prominent and is adjacent to the current oscillation peak marked 'A' in Fig. 4(a). Coulomb blockade effects occur in I_{ds} , due to single-electron charging of dopant atoms or Si nanocrystal QDs [8], tunnel coupled by tunnel barriers formed by the dielectric along the Si channel, e.g. by dopant fluctuation and/or non-uniform growth of SiO_2 (discussed in detail in Section 5). This operation mode is referred as 'SET mode'. An increase in the diamond size implies either an electrostatic squeezing of QD size with reducing V_{gs} , and/or an increase in the QD electron addition energy $E_{add} = E_c + E_k$, where $E_c = e/C$ is the Coulomb gap for QD total effective capacitance C , and E_k is the quantum confinement energy for energy level k . Assuming equal voltage drops across the left and right QD tunnel barriers, the total width of the diamonds parallel to V_{ds} corresponds to $2 \times E_{add}$, giving $E_{add} = 0.2$ eV and 0.1 eV, for the two marked diamonds. In the case of further voltage drops along the conduction path, e.g. along additional series QDs or due to a potential energy offset between the source and fin region band edges, this value of E_{add} would be a maximum bound for the corresponding QD. The widths of the diamonds along the V_{gs} axis $\Delta V_{gs} = e/C_g \sim 0.28$ V and 0.18 V, corresponding to effective gate capacitance $C_g \sim 0.57$ aF and 0.9 aF respectively. As before, C_g is modulated by V_{gs} due to squeezing of the QD. Finally, for $V_{gs} < V_{th}$, the device is in 'off mode' and begins to turn-off, with an increase in width of the centre low current region along V_{ds} axis. The separation of the operation modes in V_{gs} allows the device to be switched between classical FET (where saturation in the I_{ds} - V_{ds} output characteristics is seen) and ultra-low power single-electron QD transistor (where I_{ds} - V_{gs} oscillations are seen) via the gate voltage.

Temperature dependence of log-scaled absolute drain current $\ln(|I_{ds}|)$ vs. V_{ds} characteristics from 300 K to 200 K, with the gate terminal floating, are shown in Fig. 4(c). Current steps can be observed from $T =$

250 K and become clearer for $T < 200$ K. These steps may be associated with a Coulomb staircase behaviour, created by asymmetry in the tunnel barrier coupling to the charging QDs. Apart from the Coulomb staircase, the strong temperature dependence characteristics can be used to extract information regarding the potential energy barriers along the current path. A $\ln(|I_{ds}|)$ vs. $1000/T$ Arrhenius plot, which is usually used to extract potential energy barriers [16,26–29], corresponding to Fig. 4(c) is shown in Fig. 4(d). For higher temperature e.g. 300 K to 200 K (labelled as A), the drain current is given by $I_{ds} = I_0 \cdot e^{-\frac{E_a}{kT}}$ where E_a is the activation energy which is the potential energy barrier height, I_0 is a constant related to effective Richardson constant, and k is the Boltzmann constant. Therefore, E_a can be extracted from the slopes of the Arrhenius plot characteristics in region A. The activation energy E_a along the Si fin may be created due to (i) the conduction band offset between the Si and the source drain areas, (ii) the Coulomb charging energy of QDs along the current path, and (iii) tunnel barriers along the current path. In these three cases, and (iii) is likely to lead the higher energy barriers and dominate at higher temperatures. At a lower temperature $T \sim 160$ K, current peaks (labelled as B) are observed in the Arrhenius plot. These current peaks correspond to the mobility peaks in heavily n-doped Si at the doping level $\sim 3 \times 10^{19} \text{ cm}^{-3}$, where the dominating scattering switches from acoustic scattering to impurity scattering at $T \sim 160$ K [30,31].

E_a can be extracted from the Arrhenius plot in Fig. 4(d). A linear relationship in the $\ln(|I_{ds}|)$ vs. $1000/T$ characteristics implies an activation energy E_a which may be associated with a corresponding potential barrier energy along the current path. Fig. 5(a) shows E_a vs. V_{ds} , extracted from the data of Fig. 4(d). A decrease of E_a with increasing V_{ds} implies smaller activation energy, i.e. a reduction in potential barrier height, at higher bias. $E_a \sim 0.2$ eV $\gg$ thermal energy $kT \sim 26$ meV at RT = 300 K. This value, of similar order-of-magnitude or larger than the addition energies extracted from the Coulomb diamond characteristics, corresponds to the net energy barrier necessary to be overcome at the onset of conduction. The barrier is likely to correspond to any potential energy band offset between the source and fin regions, plus the single-

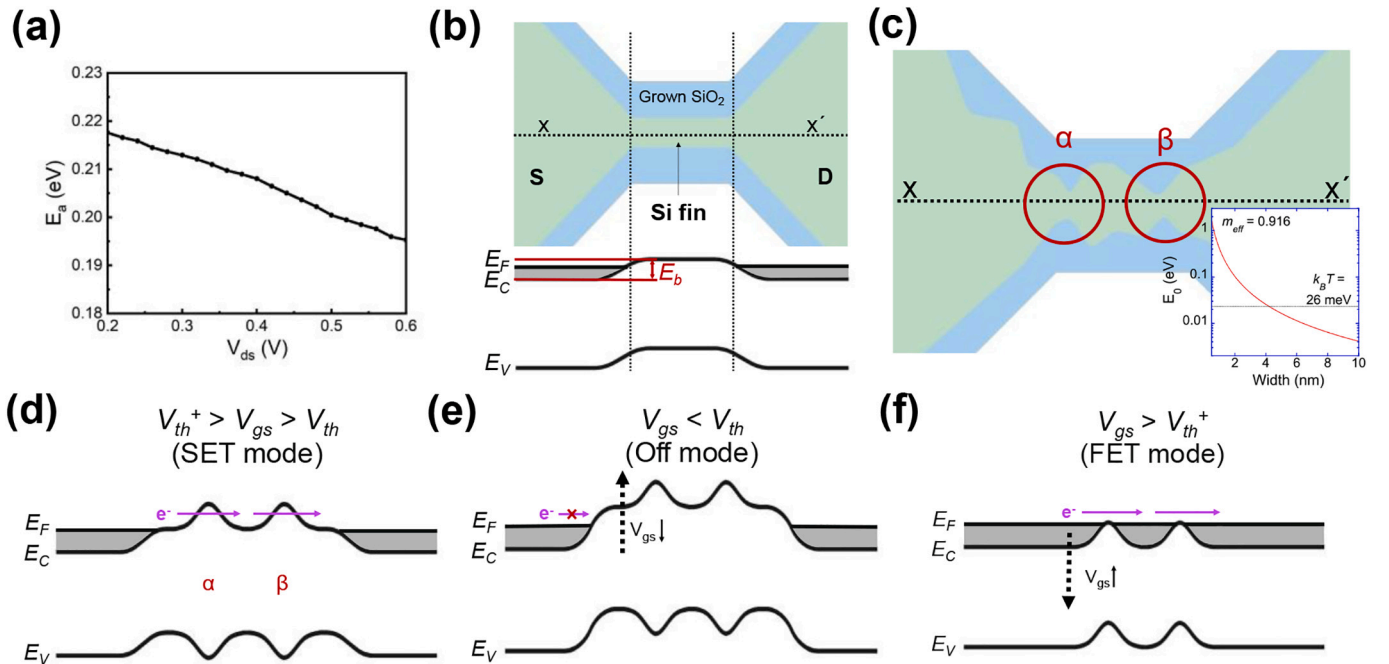


Fig. 5. (a) Activation energy E_a vs. V_{ds} , extracted from the Arrhenius plot in Fig. 4(d), note the decreasing value of E_a as V_{ds} is increased. (b) The upper figure is a plan view of an ideal fin in the point-contact region, and the lower one the corresponding energy band diagram. (c) A plan view of the fin in the presence of SiO_2 thickness variation. The thickness variation is shown exaggerated in the schematic diagram for clarity. The inset shows quantum confinement energy E_0 as a function of W . Figs (d)-(f) show the band diagrams of RT SET-FET in three different modes. (d) SET mode with single-electron effect due to tunnel barriers and intermediate QDs. (e) Off mode with higher potential barriers. (f) FET mode where the Fermi levels in the Si fin are pulled matching or even below the Fermi level in source.

electron addition energy for the dominant QD along the conduction path.

4. Discussion

We now consider the formation of tunnel barriers and QDs along the Si fin channel. Fig. 5(b) shows a plain view (top) and energy band diagram (bottom) for an ideal fin. The SiO₂ region (blue) is of constant thickness, leaving a Si fin (green) with parallel sides connecting the wider source (S) and drain (D) regions. The nominal *n*-type doping level in the top-Si, corresponding to the carrier density, is $N_D \sim 3 \times 10^{19} \text{ cm}^{-3}$, considering activated dopants, well above the degenerate doping level in Si ($\sim 10^{18} \text{ cm}^{-3}$) [32]. This doping level implies metallic source and drain regions (Fig. 5(b) bottom). However, the electron concentration n in the narrow Si fin is lower than N_D , due to (i) deactivation of donors at the Si/SiO₂ interface [33] and (ii) electron trapping in the defect states within the SiO₂. To calculate n , assuming donors (phosphor atoms) with Bohr radius $a_B = 1.8 \text{ nm}$ [34] at the Si/SiO₂ interface are deactivated, the effective volume V_{eff} can be derived from a_B and the original Si fin volume $V_0 = 6 \times 36 \times 20 = 4320 \text{ nm}^3$. Given that $V_{\text{eff}} = (W - 2a_B) \times (H - 2a_B) \times L = 2.4 \times 32.4 \times 20 \cong 1550 \text{ nm}^3$ where W , H , and L are the original Si fin channel width, height, and length. With $N_D = 3 \times 10^{19} \text{ cm}^{-3}$, approximately only 45 dopant atoms lie within the fin, and the effective, activated carrier concentration $n_{\text{eff}} = N_D \times (V_{\text{eff}} / V_0) = 10^{19} \text{ cm}^{-3}$, which remains above the degenerate doping limit. For our nanoscale fin dimensions, the effective Si/SiO₂ interface surface (i.e., excluding fin-source/drain areas) to volume ratio, $S_{\text{eff}}/V_{\text{eff}} = 1390 / 1550 = 0.9 \text{ nm}^{-1}$, is high and 85 dopants lying within a_B of the interface are deactivated. Apart from the deactivation, trapping of electrons in the SiO₂ region (case ii) can reduce n_{eff} even further. This degradation of electron concentration leads to a small potential barrier offset E_b in the fin conduction band with reference to the source/drain region (Fig. 5(b) bottom).

As nanofabricated, the Si fin has an effective fin width $W_{\text{eff}} = W - 2a_B = 2.4 \text{ nm}$. Hence the presence of a small amount of structural disorder can lead to the formation of tunnel barriers and QDs. Fig. 5(c) shows schematically a plan view of the fin in the presence of SiO₂ thickness variation (case iii). Here, the thickness variation in the schematic is exaggerated for clarity. As is argued in the discussion below, the effect of thickness variation is likely to be secondary to dopant fluctuations along the fin. If thickness variation is present, this can lead to a narrower Si fin width which may be close to ‘pinch-off’ as shown in regions α and β . In the Si fin with a fully pinched-off SiO₂ region, classical FET behaviour for $V_{\text{gs}} > V_{\text{th}}$ is unlikely to be observed. The FET behaviour of the RT SET-FET implies a continuous Si channel exists. This RT SET-FET with Si channel is in contrast to our previous work on Si/SiO₂/Si fully oxidised point-contacts [23,35] where FET behaviour is not observed and dopant atom QDs are formed in SiO₂. In the near pinch-off regions, which can be considered as nanowire like regions α and β , enhanced quantum confinement effects along the fin width form potential barriers, leading to the energy band diagram shown in Fig. 5(d). The inset to Fig. 5(c) shows the quantum confinement energy $E_0 = \frac{\pi^2 \hbar^2}{2mW^2}$ vs. W , where $m = m_{\text{eff}} \times m_0$, m_0 is the electron rest mass, and $m_{\text{eff}} = 0.916$ is the longitudinal effective mass along the (100) Si planes [36]. Hence, the $\frac{1}{W^2}$ dependence implies $E_k > k_B T$ is sensitive to changes in W (e.g., in the α and β regions) for $W < 4 \text{ nm}$. Furthermore, (case iv) the stochastic variation in doping concentration may also cause the formation of potential barrier confining QDs. In the Si fin with $V_{\text{eff}} = 1550 \text{ nm}^3$ with $N_D = 3 \times 10^{19} \text{ cm}^{-3}$, the average dopant separation is $\sim 3.23 \text{ nm}$. Therefore, $W_{\text{eff}} = 2.4 \text{ nm}$ implies only 1 donor can exist across the fin width, and stochastic variation have a strong effect on the donor separation. Finally, a self-limiting of oxidation (Case v) may occur due to a build-up of compressive strain in the fin, leading to the formation of Si nanocrystal regions. However, as the fin sides are nominally parallel, this effect becomes significant only if variations in fin dimensions and SiO₂ thickness also

exist.

While cases (i - v) all may contribute to the formation of tunnel barriers and QDs along the fin, given that surface roughness is relatively small, $\sim 1 \text{ nm}$, from interferometry measurements (Fig. 3(a-b)), and there is only gradual variation in Si fin width, from SEM imaging (Fig. 3(c)), doping fluctuation appears to be the most likely reason for QD formation. This mechanism is similar to other reported works [15,23]. In our case, doping fluctuations are random, leading to variation in the electrical characteristics of different devices, e.g. in the value of V_{th} , QD capacitance C , etc. In principle, single-ion implantation techniques [37] may enable better control of QD size and location, though these have yet to be applied to RT SET fabrication.

Formation of a QD along a nanometre scale Si channel explains our SET-FET hybrid behaviour. Fig. 5(d) shows schematically the situation for $V_{\text{th}} < V_{\text{gs}} < V_{\text{th}}^+$, where the presence of tunnel barriers and an intermediate QD leads to the observation of single-electron effects (SET mode). For $V_{\text{gs}} < V_{\text{th}}$, bands in the fin region rise in energy (Fig. 5(e)) and $I_{\text{ds}} \sim 0$ (Off mode). Finally, for $V_{\text{gs}} > V_{\text{th}}^+$, potential barriers in the fin are pulled below the source Fermi energy and depletion mode, and FET behaviour is observed (FET mode).

The role of dopants in QD formation in SET-FETs is now considered further by comparing our heavily doped, ‘fin’ device to published work on SETs based on nanowire, nanochannel FET, and point-contact geometries [15,23,38–42] where a range of doping levels (undoped, to $>10^{20} \text{ cm}^{-3}$) exist. Room-temperature SET operation has been observed in both semi-insulating moderately doped (*p*-type $\sim 10^{15} \text{ cm}^{-3}$) [38] and undoped [39,40] SOI nanowire devices. In the former case, QDs were created by a combination of nanowire roughness and quantum confinement effects and gated using top and bottom gates. A high proportion (75%, 15 out of 20) of devices were reported to show Coulomb blockade at room temperatures [38]. In the latter case, patterned gates [39,40] were used to confine QDs. In both these cases, the effect of dopant atoms or impurities forming QDs in the channel is greatly reduced. SETs have also been demonstrated using QDs defined by nanochannel geometry and doped at moderate to degenerate ($\sim 10^{18} \text{ cm}^{-3}$) levels [41]. Here, SET operation was observed at low temperature only as the nanochannel dimensions were comparatively large ($\sim 50 \text{ nm} \times 20 \text{ nm}$). Dopant atom QD operation has also been observed explicitly [15], via measurement of energy spectra of individual donor atoms in nanochannel FETs, at cryogenic temperature ($\sim 10 \text{ K}$ or less). Here, operation was limited to low temperatures due to the shallow donor potential wells ($\sim 50 \text{ meV}$ depth) in silicon. Finally, SET behaviour can be observed with very high doping levels ($3 \times 10^{18} \text{ cm}^{-3}$) devices [42]. Even higher doping levels ($>10^{20} \text{ cm}^{-3}$), produced by ion-implantation, have been investigated in our previous work on Si/SiO₂/Si point-contacts [23], where the deep potential wells associated with donor atoms embedded in SiO₂ enabled room-temperature operation.

The SET-FETs in this work form a hybrid system, where the device channel size is $<10 \text{ nm}$, and doping concentration $\sim 3 \times 10^{19} \text{ cm}^{-3}$ is well above the degenerate level $\sim 10^{18} \text{ cm}^{-3}$ and in a range where single-electron charging effects have been reported. In this regime, comparison with published works suggest that QDs may form due to more than one reason (case i - v for our device, see above). However, this helps towards obtaining a high percentage of devices ($\sim 37\%$) with room-temperature single-electron effects while retaining a side-gate geometry, simplifying fabrication in comparison with patterned top gates.

In order to measure the processing yield for functional devices, four $15 \times 15 \text{ mm}^2$ chips (Chip A, B, C, and D) with 45 devices on each chip, were fabricated and characterised. Fig. 6 shows a colour map for these chips, with observed behaviour for devices indicated using four different colours. Boxes marked in dark blue refer to the devices showing RT SET-FET functionality with the three different operation modes discussed earlier. In chips A-C, $>40\%$ of devices show RT SET-FET behaviour. For chip D, in the top-right region, diode-like or fully off behaviour (yellow) predominates. The full yield for devices where FET operation occurs in

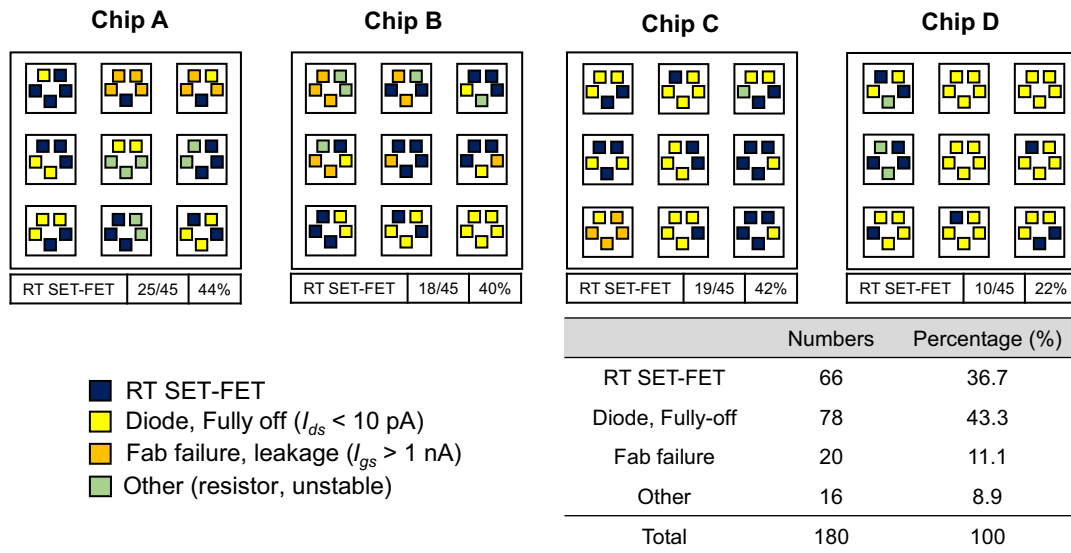


Fig. 6. A colour coded map for observed device operation for devices fabricated in four 15 mm × 15 mm chips (A, B, C, and D). Blue: SET-FET. Yellow: Diode like without gate effect or fully off. Orange: Fabrication failure. Green: Other (resistor, unstable). Percentages for these cases are shown in the table (right-bottom). (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

combination with at least weak oscillations in I_{ds} vs. V_{gs} , with the later forming signatures of the likely presence of single-electron effects, is 66 out of 180 devices in total (~37%). This is much higher than the ~10% observed in our previous work using Si/SiO₂/Si RT SETs [21], though lower than the 75% (15/20 devices) reported for nanowire based RT SETs with fluctuation in width [38]. SET-FET characteristics for 8 representative devices showing the range of I_{ds} vs. V_{gs} oscillations observed where the gate capacitance C_g varies from ~0.2–0.8 aF, are provided in supplementary material, Fig. S5 Oscillations may be very strong and regular, comparable to those in Fig. 4, or much weaker, such that FET behaviour is more prominent. Our fabrication process is relatively conventional and simple and suitable for a laboratory environment. However, stochastic variation in the dopant atom distribution and oxide thickness, combined with the ~2.4 nm effective fin thickness, impacts strongly on device behaviour and leads to a quantitative variation in characteristics. A non-uniform or overgrown SiO₂ layer even at the scale of 1 nm, or a lack of dopant atoms within the Si fin, leads to diode-like or fully off devices. On the other hand, an under oxidised Si fin, or lithography failure in the fin or gate regions also leads to non-functional devices. Further fabrication process control would require an industrial clean-room environment.

5. Summary

In summary, the nanofabrication of sub-10 nm ‘fin’ channel hybrid SET-FETs, and mechanisms for formation of tunnel barriers and QDs along the channel, have been investigated. Devices were fabricated in heavily *n*-doped SOI material using high-resolution EBL, RIE, and thermal oxidation to reduce Si channel width. The fin channel effective dimensions in our devices were ~2.4 nm × 32 nm × 20 nm, following oxidation and excluding a Si/SiO₂ interface dopant deactivation layer. Arrhenius plots of I_{ds} vs. $1/T$ allow extraction of potential barrier energies ~0.2 eV along the fin channel. Statistics for functional/non-functional devices on four chips, each containing 45 devices, are presented. It is found that ~37% of devices showed RT SET-FET operation. Finally, an energy band model is presented for the device, to explain the mechanism for QD and tunnel barrier formation, with the most likely cause being dopant fluctuations.

Declaration of competing interest

The authors declare the following financial interests/personal relationships which may be considered as potential competing interests:

Zahid Durrani reports financial support was provided by Engineering and Physical Sciences Research Council. If there are other authors, they declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

Acknowledgements

The authors acknowledge Dr. Jon Griffiths, University of Cambridge, for electron beam lithography of devices, Prof. Andrew Yacoot, National Physical Laboratory (NPL), for atomic force micrography of devices, and useful discussion with Dr. Aleksey Andreev. This research has been supported by the UK EPSRC Single Atom Quantum Electronics project, grant number EP/V030035/1. K-L Chu would like to acknowledge the support of the Taiwan Ministry of Education: Government Scholarship to Study Abroad (GSSA).

Appendix A. Supplementary data

Supplementary data to this article can be found online at <https://doi.org/10.1016/j.mne.2024.100275>.

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