

# Comparative Optimization Design of a Modular Multilevel Converter Tapping Cells and a 2L-VSC for Hybrid LV ac/dc Microgrids

A. Lachichi, Member, IEEE, A. Junyent-Ferre, Senior Member, IEEE, T. C. Green, Fellow, IEEE  
Control & Power Research Group, Imperial College London,  
South Kensington Campus London SW7 2AZ, UK  
a.lachichi@imperial.ac.uk

**Abstract** -- The paper presents the performance of the modular multilevel converter *tapping cells* associated with an ac filter in term of efficiency and power density in a hybrid LV ac/dc microgrid application and compares it to the performance of the conventional topology used in LV application, i.e., the Two-Level voltage source converter (2L VSC). A bi-objective optimization based on the Genetic Algorithm is hence developed, providing details on designing the components of the LCL filter, the MMC and the 2L VSC. The MMC reaches an efficiency of 99.4% when the main dc-grid is left floating. However, due to its modularity and scalability, offering multiport connections option, the MMC tapping cells has the disadvantage of low power density. Exploring the filtering capability of the equivalent arm inductance of the MMC seen from the ac grid side, optimization design results show that higher switching frequencies allow a significant volume reduction of the inductive components of the MMC/LCL filter while higher switching frequencies have little impact on the switching losses of the MMC. This has the benefit of reducing the overall footprint of the converter and encouraging the use of the MMC in LV application.

**Index Terms**-- Hybrid ac/dc microgrid, interlink converter, MMC, GA based optimization, tapping cells, two-level VSC.

## I. INTRODUCTION

The electrical grid system is continually experiencing unprecedented changes driven mainly by key technology trends. It is becoming more decentralized due to the growing penetration of renewable sources and technology advances in energy storage systems, and it is already preconized by many industries that a return to a purely centralized grid system will not happen [1]. These changes are happening at all levels of the grid system: from transmission and utility grids to distributed grids. At the distributed grid level, hybrid microgrids configurations, combining ac and dc microgrids are gaining momentum as such configurations improve the power flow and facilitate the integration of different type of distributed sources and loads [2]. An example of such microgrid is shown in Figure 1. It is characterized by a combination of distributed generation units, storage systems and loads which are connected to either an ac or a dc grid via a *local* interface. Both grids are connected to the main distributed ac grid via an interlink converter capable of handling different energy conversions. Although, such hybrid microgrids can bring significant improvement for key applications as in commercial buildings, there are few papers that cover their development.

In this paper, we investigate the design of the interlink converter, with multiport characteristics required to interface the main ac distributed grid with different *local* ac and dc grids. It is assumed that the converter should feature a set of functionalities such as disturbance isolation, effective protection and availability of local LV ac and dc grids. These *new* requirements for the design of the multiport power converter are not fully covered by standards for this

specific application. In addition, the required voltage and

Fig. 1. Example of a hybrid LV ac/dc microgrid in commercial buildings.

power levels that are needed to build a hybrid ac/dc microgrid are still not well defined for the dc part of the hybrid microgrid. Initial designs are proposed in [3-7] to either set the power and dc voltage levels or to propose a topology for the multiport converter. For example, authors in [3] propose a bipolar dc grid with three voltage levels that are available to supply dc loads:  $\pm 170\text{V}$  and  $340\text{V}$ . In [4], the authors propose a bidirectional high density 2-L voltage source converter, using SiC devices and rated at  $100\text{kW}$ , as an interface between the main ac utility grid and a  $380\text{V}$  dc distribution grid and compare it to an existing topology used in data centres, consisting of  $7 \times 15\text{kW}$  unidirectional single-phase dual boost rectifiers connected to each output phase of the three-phase ac grid. Similarly, authors in [5] propose the 2-L voltage source converter and present protection schemes for limiting or clearing fault currents occurring at dc grids. Other advanced converter topologies have been proposed as an interlink converter which is more dependent on the hybrid microgrid structure. Authors in [6] propose a hybrid ac/dc microgrid with one ac port and two separate dc grids. The interlink converter is a three ports topology and it is formed by a cascaded multilevel converter in which all the three phases H-bridge cells of the converter are connected to DABs whose output are parallel connected in group of two. Each group is then connected to one dc grid. Authors in [7] propose a hybrid microgrid structure with a dc grid connected through a back to back converter. The main challenge for both arrangements remains the power flow control.

Even though, the modular multilevel converter (MMC) is predominantly proposed in high power HVDC and medium voltage drive applications, authors in [8-10] introduce for the first time the MMC as an interlink converter in hybrid LV ac/dc microgrids while authors in [11] analyze power density benefits of multilevel approaches for low power applications. A comparative analysis in term of efficiency is carried out in [9] between a 5-level MMC using Si MOSFET devices, a 3-level MMC using GaN HEMT and a 2-L voltage source converter using SiC MOSFET, all rated at  $10\text{kW}$ . It shows that Si MOSFET MMC is the most efficient as well in LVDC applications. However, performance limits of the 2-level voltage source converter and the MMC have not been covered in [9]. Authors in [12] carry out a bi-objective optimization with respect to the efficiency and power density for a MMC rated at  $15\text{kVA}$  and  $400\text{kVA}$ , and present the Pareto front, defining hence the performance limit of the MMC.

Due to its modular feature, the MMC is investigated in our work as a multiport interface capable of exchanging power among its building blocks in which many distributed sources and loads available in the hybrid microgrid are connected. Based on [13], an additional design case is considered in this paper depending on how the main dc-grid

is connected. Hence, two cases are envisioned in this paper, i.e., either the main dc-grid of the MMC is left floating and the power is exchanged only from the ac-grid and/or distributed sources to the microgrid loads or the main dc-grid is interconnected to a nearby LV hybrid microgrids or energy storage system. This arrangement brings not only new challenges in designing and energy managing the LV hybrid ac/dc microgrid but as well in operating the MMC in LV applications. It is worth noting that the proposed MMC can be applied in other applications such as microgrid-like EV parking deck systems.

The contribution of the paper is to introduce the modular multilevel converter *tapping cells* as a multiport interlink converter to a hybrid LV ac/dc microgrid in which the main dc-grid of the MMC can be left floating. In order to assess the feasibility of such arrangement, performance limits in term of power density and efficiency of the LV modular multilevel converter topology and its ac filter are carried out and compared to the conventional Two-Level voltage source converter and its ac filter using a bi-objective optimization algorithm in which the design parameters space takes into account the ac filter inductor parameters design and the converter parameters design, capturing hence the interaction between them in the design stage itself. The optimization-based design approach used throughout this investigation relies on a population-based algorithm, i.e., the Genetic Algorithm (GA). The latter has been extensively used to determine the performance trends and limitations of Power Electronics systems [14-17]. The aim of the algorithm is to evolve the population in such a way it becomes a set of non-dominated designs, i.e., the best designs which is referred as Pareto-optimal front [18, 19].

The paper is structured as follows: Section II covers basic design concepts in optimization. In section III, the overall system under investigation is presented and design parameters related to the interlink converter are highlighted. In section IV, the ac filter model is presented while section V presents the converter loss model. In section VI optimization design criteria for each topology and their respective ac filter are summarized and simulation results are presented in section VII. A conclusion is given at the end of the paper.

## II. BASIC CONCEPTS IN OPTIMIZATION

The mathematical formulation of an optimization problem that is based on the Genetic Algorithm relies on finding the minimum of the objective function  $f_i(\vec{x}^i)$  which is evaluated based on the  $i^{\text{th}}$  population of the design parameter vector  $\vec{x}^i$  expressed as

$$\vec{x}^i = [x_1^i, x_2^i, \dots, x_n^i]^T \quad (1)$$

where  $n$  is the number of design parameter inputs. Parameters in  $\vec{x}^i$  define the system design variables such as active and passive components technology and ratings of the converter or geometrical parameters of filter inductors.

Our design approach is a constrained optimization problem which is transformed to an unconstrained problem by associating a penalty  $P(\vec{x}^i)$  with all constraint violations [19]. The penalty is included in the objective function evaluation ensuring an acceptable operating conditions. Elements of the objective function are hence defined as

$$f_i(\vec{x}^i) = \begin{cases} \varepsilon(P(\vec{x}^i) - 1)[1, \dots, 1]^T & P(\vec{x}^i) < 1 \\ \left[ \frac{1}{O_1(\vec{x}^i)}, \dots, \frac{1}{O_k(\vec{x}^i)} \right]^T & P(\vec{x}^i) = 1 \end{cases} \quad (2)$$

with

$$P(\vec{x}^i) = \frac{1}{CS} \sum_{j=1}^{CS} CS_j(\vec{x}^i) \quad (3)$$

$CS_j(\vec{x}^i)$  is the status of the  $j^{\text{th}}$  constraint,  $CS$  is the number of constraints and  $O_k(\vec{x}^i)$  is the design quantity to be minimized such as the volume or the losses,  $k$  is the number of objectives.  $\varepsilon$  is a positive number commonly chosen to be in the order of  $10^{-10}$ .

In the next sections, design considerations used to build the design parameters vector, the constraints and the objective function related to the optimization of the converters and the filters are presented step-by-step.

## III. TOPOLOGIES DESCRIPTION AND COMPONENTS

### A. Topologies description

The multiport power converter is designed to provide different voltage levels for facilitating the integration of renewable sources and batteries energy storage, and supplying different ac and dc loads, or for implementing future local dc grids, for example. In order to determine the most suitable power converter that would satisfy the above requirements and would allow as well lower semiconductor losses and hence lower semiconductor expense and realization costs, two topologies are presented and are compared in order to get insights on the achievable performances in this specific application.

Figure 2 depicts the topologies under investigation. The 2-L voltage source converter predominantly used in LV applications is shown in Fig. 2 (a). It has its 3 ac terminals connected to the distributed ac grid via a LCL filter to attenuate higher order harmonics while the two poles dc terminals are connected to the dc grid with a neutral mid-point, providing at the best three dc voltage levels. Distributed sources and different loads are connected to the dc grid via their own local interface. It offers 4 ports, i.e., one ac port and three dc ports. The 2-L VSC comprises a pair of switches with freewheeling diodes. The carrier phase-shift modulation is considered throughout the analysis.

In order to explore the possibility to have a multiport converter, the modular multilevel converter is considered for this application as shown in Fig. 2 (b). Similarly to the 2-L VSC, the MMC has its 3 ac terminals connected to the distributed ac grid via a LCL filter while a number of half bridge cells of the MMC has their terminal connected to a distributed generation source or a load via a local interface which regulates the dc voltage according to sources/loads requirements. The dc terminals of the MMC can be left floating or used to suit many purposes, connecting battery energy storage system for example, or interlinking with a nearby dc microgrid. Two cases are hence considered depending on whether the dc-link is connected or not. In the first case where the dc-link is connected, the arm currents of the MMC are the sum of an ac component that is related to the ac output phase current and a dc component that is related to the dc circulating current component. In the second case where the dc-link voltage is floating, the arm currents are sinusoidal without any dc current offset. The power flow is hence solely made from the ac-grid and/or

(a)  
(b)

Fig. 2. Interlink power converter topologies for hybrid ac/dc microgrid in commercial building application. (a) Two-Level voltage source converter. (b) Modular multilevel converter tapping cells with dc-link connected or floating.

from the distributed generation sources connected to the cells, to the loads that are tapped into a number of cells. Fig. 3 depicts simulation results of such arrangement, i.e., the ac-grid is supplying the loads while the main dc-grid is floating. The balancing of the cells is well achieved and the dc-grid voltage is maintained to the required voltage level. Multicarrier phase-shift modulation is considered throughout the analysis for operating the MMC. It is worth noting that the analysis of the energy management between ports is left for future publications.

The requirement of the system is summarized in Table 1. It is worth noting that there is no specific requirement set by standards in term of voltage and power level for the dc grid in buildings as of today. The choice of the values of the ac grid shown in Table I have been selected to find the best performance of each topology without paralleling any converters or devices.

TABLE I. BASIC GRID AND CONVERTER PARAMETERS

| Parameters             | Value        | Description                 |
|------------------------|--------------|-----------------------------|
| <b>Grid</b>            |              |                             |
| $P$                    | 10 kW        | Rated active power          |
| $V_{ll,g}$             | 400 V        | ac grid voltage             |
| $f_g$                  | 50 Hz        | ac grid frequency           |
| Power factor           | 1            |                             |
| <b>Converter</b>       |              |                             |
| $f_s - 2\text{-L VSC}$ | 5 – 10 kHz   | Switching frequency         |
| $f_s - \text{MMC}$     | 300 – 600 Hz | Switching frequency         |
| $U_c$                  | 87.5 V       | MMC nominal cell voltage    |
| $N$                    | 8            | MMC number of cells per arm |
| $M$                    | 0.8          | Modulation index            |
| $U_d$                  | 700 V        | Pole to pole dc voltage     |

## B. Components

The design methodology of both converters from an optimization problem viewpoint involves the allocation of values to the design parameters vector. The latter includes passive and active components technology and ratings of each converter. It is worth noting that the design of power semiconductor devices and the capacitors cannot anymore be influenced and are rather limited to the selection of the suitable component in such a way a high efficiency design is obtained. The selection is hence evaluated according to the following procedure

1) *Capacitor rating:* The capacitance of each cell of the MMC is estimated by evaluating the maximum energy variation of each arm  $\Delta E_{\max}$ , and is expressed as [20]

$$\Delta E_{\max} = \frac{C_{c,\min}}{2N} u_d^2 (k_{\max}^2 - k_{dc}^2) \quad (4)$$

where  $N$  is the number of cell in each arm,  $C_{c,\min}$  is the minimum required capacitance of the cell,  $k_{\max}$  is a coefficient related to the maximum allowable capacitor voltage variation,  $k_{dc}$  is a coefficient related to the capacitor voltage nominal value, and  $u_d$  is the pole to pole dc voltage.

Figure 3. MMC with 8 cells per arm and the main dc-grid floating, microgrid loads tapped into the cells. (a) Voltage across the cells (upper), pole-to-pole voltage (middle), arm voltage (bottom). (b) Arm currents.

$k_{\max}$  is used as a variable design parameter by assuming a capacitor voltage variation of 5 to 20 % around the nominal capacitor voltage. From (4), the minimum value of the capacitance  $C_{c,\min}$  is deduced and is expressed as

$$C_{c,\min} = \frac{2N\Delta E_{\max}}{u_d^2 (k_{\max}^2 - k_{dc}^2)} \quad (5)$$

For the 2-level voltage source converter, the dc capacitance is designed to limit the dc-link voltage ripple to a specified value. Assuming a steady state operation of the converter and neglecting the losses, the minimum required capacitance is expressed as follows

$$C_{\min} = \frac{I_g + P/u_{dc}}{2\Delta u_{dc} f_c} \quad (6)$$

where  $I_g$  is the peak ac output phase current,  $\Delta u_{dc}$  is the peak to peak voltage ripple. Typical values of  $\Delta u_{dc}$  are between 1 to 2% [21] and is used as a variable design parameter.

In this analysis, film capacitors are considered. This is motivated by the fact that they exhibit lower ESR and leakage current compared to electrolytic capacitors and hence are, as a rule of thumb, required for high efficiency designs. In addition, with film capacitors, the volume scales linearly with the stored energy since the thickness of the capacitor is mainly determined by the thickness of the dielectric layers. We have considered Electronicon manufacturer which gives the volume for each selected capacitor.

2) *Semiconductors rating:* Generally, semiconductor devices with higher blocking voltage exhibit higher switching losses while more series connected semiconductor devices lead to potentially higher conduction losses. Hence different semiconductor devices class are considered ranging from 100V to 1.2kV using Si or SiC, MOSFET or IGBT in order to investigate the best achievable efficiency of each topology.

The volume occupied by the semiconductor is estimated by evaluating the heatsink volume requirement and assuming that two semiconductor devices are mounted on one heatsink. A forced air cooling is considered in this work to remove the excess heat from the semiconductor devices. Optimization of heatsinks has been thoroughly carried out in [22], and a relationship between the volume and the thermal resistance is given by the Cooling System Performance Index referred as CSPI and equal to

$$CSPI = 1/(R_{th,S-a} Vol_i) \quad (7)$$

where  $R_{th,S-a}$  is the thermal resistance of the heatsink-to-ambient expressed in K/W and  $Vol_i$  is the volume of the heatsink, expressed in Liters.

CSPI has been chosen equal to 20 W.K<sup>-1</sup>.Liter<sup>-1</sup>. This is motivated by the fact that highly optimized heatsinks attain values in the range of 20 to 30 W.K<sup>-1</sup>.Liter<sup>-1</sup> [22]. Solving (7) for  $Vol_i$ , the total volume share of the semiconductor devices is the sum of all individual heatsink obtained through the optimization design.

3) *Magnetics*: In each arm of the modular multilevel converter an inductor  $L_{arm}$  is series-connected with the cells. To avoid higher semiconductor device losses due to the potential presence of a higher second harmonic component of the circulating current,  $L_{arm}$  should be set to a value far enough from resonance inductances appearing at the 2<sup>nd</sup> and 4<sup>th</sup> harmonic circulating current [23]. The highest resonance frequency should be smaller than the grid frequency which puts a constraint on the capacitor and arm inductor design given by the following

$$L_{arm}C_c > \frac{5N}{24\omega_g} \quad (8)$$

Equation (8) is used as a design constraint as it will be presented in section VI. For protection point of view, a low value of the arm inductance would make the converter to be subject to high fault currents in case of a short-circuit on the dc bus. However, due to the filter inductance  $L_{fconv}$ , it is still possible to combine the design of the arm inductance and the ac filter inductance as highlighted in [24] as the arm inductance is equivalent to an ac output phase inductor. An index factor  $k_1$  is then introduced to assess the filtering contribution of the arm inductance and is defined as

$$k_1 = \frac{L_{arm}}{2L_{fconv}} \quad (9)$$

#### IV. AC FILTER DESCRIPTION AND COMPONENTS

ac filters are required to attenuate the current distortion between each converter and the main ac grid in order to comply with grid-standard such as IEEE-519 [25] which states that the maximum harmonic current for harmonic numbers higher than 35 must be limited to 0.3% of the rated grid current for a short circuit ratio (SCR) lower than 20. The latter reflects the amount of the grid impedance  $L_g$  in the distribution network. For this analysis, we have extended the filtering option presented in [13] to the LCL filter as its structure is the basis for other filter structures and it has the best trade-off for components size and weight, and for attenuation performance, i.e., 60-dB/dec attenuation at high frequency.

Most design procedures of LCL filter presented in the literature are based on minimizing the stored energy as a measure for the size of the components. However, in applications where compactness is a design requirement, it is important to have a precise design for the filter components in order to obtain an estimation of the filter volume as accurate as possible, as they can sometimes be bigger than the power converter. In the following subsections the design procedure of the LCL filter is presented as well as the design parameters vector for the optimization algorithm.

##### A. LCL parameters estimation

The LCL filter parameters are calculated to reduce high order current harmonic on the grid-side. This is done in the frequency-domain by estimating the switching current ripple attenuation passing from the converter-side to the grid-side  $i_g(s)/i_{conv}(s)$ . At high frequencies, the converter is a harmonic generator while the grid is considered as a short circuit, the transfer function between the grid current  $i_g$  and the converter current  $i_{conv}$  is then expressed as

$$\frac{i_g(s)}{i_{conv}(s)} = \frac{1}{1 + \frac{r+1}{\omega_{res}^2} s^2} \quad (10)$$

where  $\omega_{res}$  is the LCL filter angular resonance frequency and  $r$  is a ratio defined as the relation between the inductance at the converter-side and the one at the grid side [26]

$$r = \frac{L_{g,t}}{L_{fconv,t}} \quad (11)$$

where

$$L_{fconv,t} = L_{fconv} \quad \text{for 2L-VSC}$$

$$L_{fconv,t} = L_{fconv} + \frac{L_{arm}}{2} \quad \text{for MMC}$$

The total inductance per unit value required to limit the amplitude of the  $h^{th}$  order grid current harmonic to  $I_{g,h\%}$  at no load condition is expressed as

$$L_{fconv,t,pu} = \frac{V_{conv,h,\%}}{I_{g,h,\%} \left[ 1 - (1+r) \left( \frac{\omega_h}{\omega_{res}} \right)^2 \right]} \left( \frac{\omega_g}{\omega_h} \right) \quad (12)$$

where  $V_{conv,h,\%}$  is the amplitude of the dominant harmonic voltage at no load conditions in percent of the rated grid voltage, and  $I_{g,h,\%}$  is the amplitude of the dominant harmonic current at no load conditions in percent of the rated grid current.  $\omega_h$  is the  $h^{th}$  highest order angular frequency.

The expression of  $V_{conv,h}$  is dependent on the PWM strategy used to operate both converters. In this analysis, a Phase Shifted Carrier Pulse Width Modulation (PSCPWM) strategy is adopted. According to [27, 28], the amplitude of the dominant harmonic voltage in percent of the rated grid voltage  $V_{conv,h,\%}$  is then expressed as

$$V_{conv,h,\%} = 100 \frac{2}{\pi M} J_2 \left( \pi \frac{V_g}{V_{dc}} \right) \quad \text{For 2-L VSC} \quad (13)$$

$$V_{conv,h,\%} = 100 \frac{2}{MN\pi} J_{2N-3} \left( 2N\pi \frac{V_g}{V_{dc}} \right) \quad \text{For MMC} \quad (14)$$

Substituting (12) into (11) and solving (11) for  $L_{g,t}$  gives the value of the grid-side inductance, which is expressed in per unit value as

$$L_{fg,t,pu} = r \frac{V_{conv,h,\%}}{I_{g,h,\%} \left[ 1 - (1+r) \left( \frac{\omega_h}{\omega_{res}} \right)^2 \right]} \left( \frac{\omega_g}{\omega_h} \right) \quad (15)$$

Solving the expression of the LCL filter angular resonance frequency for  $C_f$  gives the value of the capacitance which is expressed in per unit value as

$$C_{f,pu} = \frac{r+1}{\omega_{res}^2 r} \frac{\omega_g V_g}{I_g} \quad (16)$$

The voltage drop across the LCL filter will set a limitation on the minimum dc-link voltage and hence on the modulation index. In order to calculate the required modulation index at nominal load, a simplified Thevenin equivalent circuit is considered as shown in Fig. 4 where circuit parameters are defined as follows

$$L_{th} = \frac{L_{fconv,t}}{X_{LC}}$$

$$X_{LC} = 1 - L_{fconv,t} C_f \omega \quad (17)$$

$$\vec{v}_{th} = \frac{\vec{v}_{conv}}{X_{LC}}$$

The amplitude of the most dominant grid current harmonic is then determined and LCL parameters are iteratively evaluated to meet the requirement of IEEE-519 standard [25].

### B. Inductor volume estimation

Figure 5 shows the UI core used throughout the analysis. The choice of this geometry is motivated by the fact that this core forms a simple magnetic path. In addition, the window area can be completely filled with copper resulting in a high window utilization factor [29]. Losses which are function of the geometry of the core are as well easily derived.

The design of the inductors includes different design variables such as core and wire materials, core geometry, winding arrangement, etc. Design factors and dimensional ratios are used as defined in [29, 30] and are reported in the paper for clarity. The reader is referred to [29, 30] for further explanations.

- **Insulation factor  $K_w$ :** this factor takes into account the insulation of the conductor plus the area between the insulated conductors that is filled with air. A typical

Fig. 4. Thevenin equivalent circuit for LCL.

value is  $k_w = 0.84 - 0.5$ .

- **Cross-sectional area of the winding conductor:** The cross-sectional area of the bare wire determines the current-carrying capability and it is estimated by  $A_w = \frac{I_{Lrms}}{J_{rms}}$  where  $I_{Lrms}$  and  $J_{rms}$  are the rms values of the inductor current and the current density respectively. The diameter of the winding conductor is then calculated and rounded to the nearest value according to the AWG standardized system.
- For a square pattern, the number of turns per layer of the coil is  $N_{tl} = \frac{w_c}{K_w d_i}$  and the number of layers is  $N_l = \frac{h_c}{K_w d_i}$  where  $w_c$ ,  $h_c$  and  $d_i$  are the width and the height of the coil winding window, and the outer diameter of the bar winding wire respectively. The number of turns is estimated as  $N = N_{tl} N_l$ .  $N_{tl}$  and  $N_l$  are the desired number of the coil in term of the number of wires. The width and the height of the coil winding window is then estimated from the above equations.
- **Coil factor  $K_b$ :** It defines how much of the available window space may be used for the winding. The coil factor is defined as  $K_b = 1 - \frac{w_c}{w_a}$  where  $w_a$  is the core window area. Typical values of the coil factor varies from 0.55 to 0.75 for ferrites.
- **The volume of the inductor:** defined as the sum of volume of the core  $V_{cr}$  and the volume of the coil laying outside the core  $V_{cl}$ .
- The inductance of each ac filter inductors can be expressed as a function of the magnetic core characteristics and its dimension. It is used as a

design constraint which will be explained in Section VI.

### C. Inductor loss estimation

Losses in the inductors are classified in two main categories, i.e., the winding losses  $P_w$  and the core losses  $P_c$ . Winding losses are straightforward obtained [32, 33]. They are mainly due to skin and proximity effects. While the latter are found to be insignificant in our analysis, the former are evaluated at the most dominant harmonic component given in Section IV.A.

Magnetic core losses  $P_c$  are more difficult to obtain [29-30]. However, the Generalized Steinmetz Equation (iGSE) which estimates the core losses per unit volume remains the most applied approach as it does not require extra characterization of material parameters beyond those given by manufacturers. In this analysis, the iGSE is applied and is expressed as

Fig. 5. Core sections of inductors employed in the ac filters.

$$P_c = \frac{1}{T} \int_0^T k_i \left| \frac{dB}{dt} \right|^\alpha (B)^{\beta-\alpha} dt \quad (18)$$

where  $B$  is the flux density,  $\Delta B$  is the peak-to-peak flux density and  $k_i$  is given by

$$k_i = \frac{k}{(2\pi)^{\alpha-1} \int_0^{2\pi} |\cos\theta|^\alpha |\cos\theta|^{\beta-\alpha} d\theta} \quad (19)$$

$k$ ,  $\alpha$  and  $\beta$  are material parameters that are given by core manufacturers,  $\theta$  is the variable of integration.

It is worth noting that, in order to obtain the flux density, current waveforms are simulated. It is assumed that the current has the fundamental frequency component and a superimposed predominant frequency component. Note that, similar to the winding losses, only the predominant harmonic component is considered and is given in Section IV.A.

### D. Capacitor loss estimation

For the filter capacitor, film capacitors are as well considered as they are well suited for high efficiency designs.

Losses are estimated according to the following

$$P_{cap} = u_c^2 \pi f_0 C_f \tan \delta_0 + i_c^2 R_{ESR} \quad (20)$$

where  $u_c$  and  $i_c$  are the voltage across the capacitor and the current flowing through it.  $\tan \delta_0$  and  $R_{ESR}$  are the loss tangent and the internal resistance of the chosen capacitor and are given by manufacturers datasheet.

The hottest spot is evaluated according to the following

$$T_h = T_{amb} + R_{th,c} P_{cap} \quad (21)$$

where  $R_{th,c}$  is the thermal resistance and  $T_{amb}$  is the maximum ambient temperature. The latter will be set a constraint design.

## V. CONVERTERS LOSS MODELS

Switching and conduction losses of the semiconductor devices are estimated according to the average current/voltage waveforms obtained for each topology which is detailed in [34]. Depending on the semiconductor devices considered, i.e., MOSFET, IGBT or diode, the conduction losses are expressed as follows

$$P_{cond,MOSFET} = I_{sw,T}^2 R_{DS,On} \quad (22)$$

where  $R_{DS,On}$  is the device on-state resistance and  $I_{sw,T}$  is the rms current flowing through the device.

$$P_{cond,IGBT} = \bar{I}_{sw,T} V_{ce0} + I_{sw,T}^2 R_{ce,On} \quad (23)$$

where  $V_{ce0}$  is the on-state zero-current collector-emitter voltage and  $R_{ce}$  is the device on-state resistance,  $\bar{I}_{sw,T}$  is the average value of the current flowing through the device.

$$P_{cond,diode} = \bar{I}_{sw,D} V_{F0} + I_{sw,D}^2 R_{D,On} \quad (24)$$

where  $V_{F0}$  is the on-state zero-current forward voltage and  $R_{D,On}$  is the device on-state resistance.  $\bar{I}_{sw,D}$  and  $I_{sw,D}$  are the average and RMS value of the current flowing through the diode.

Switching losses of either a MOSFET or an IGBT device are expressed as

$$P_{sw,T} = f_s \left( \frac{W_{on} + W_{off}}{V_{ref} I_{ref}} \right) \bar{V}_{sw,T} \bar{I}_{sw,T} \quad (25)$$

where  $W_{on}$  and  $W_{off}$  are the turn-on and turn-off switching energy of the device measured at the reference point  $V_{ref}$  and  $I_{ref}$ .  $\bar{V}_{sw,T}$  is the average voltage across the device and  $f_s$  is the switching frequency.

The switching losses of the diode is expressed as

$$P_{sw,D} = f_s \left( \frac{W_{rec}}{V_{ref} I_{ref}} \right) \bar{V}_{sw,D} \bar{I}_{sw,D} \quad (26)$$

where  $W_{rec}$  is the reverse recovery energy of the diode measured at the reference point  $V_{ref}$  and  $I_{ref}$ .  $\bar{V}_{sw,D}$  is the average voltage across the diode.

Losses of the cell capacitor of the MMC are estimated in the same way as in Section IV. D.

## VI. IMPLEMENTATION OF THE OPTIMIZATION PROCEDURE

The optimization design of the LCL filter and each converter is performed using the same design parameters vector  $\vec{x}$  in order to highlight the influence of the switching frequency on the inductance volume and the losses of the converter. The optimization algorithm determines the optimal parameter values of  $\vec{x}$  defined in section VI. A. A design is optimal when it meets all the constraints defined in section VI. B. through the objective function given by (2) and constructed to minimize the losses and the volume of the filter inductance. The set of optimized solutions are then plotted to obtain the Pareto-optimal Front.

### A. Optimization variables

The design parameters vector includes all geometrical parameters of the inductor, the magnetic material and the type of conductor used. Also, the number of turns of the

conductor and the cross-sectional area of the wire are specified. It includes as well the maximum allowable capacitor voltage ripple of the converter, the per unit arm inductance (only for the MMC), the semiconductor type and the capacitor type used.

The parameter vector that characterizes the design of the  $i^{th}$  population is defined as

$$\vec{x}^i = (\vec{x}_{LCL}^i \quad \vec{x}_{conv}^i)^T \quad (27)$$

where  $\vec{x}_{LCL}^i$  and  $\vec{x}_{conv}^i$  are expressed as

$$\vec{x}_{LCL}^i = (CR_i \ CD_i \ g_i \ l_{c,i} \ w_{e,i} \ a_i \ N_i \ N_{w,i} \ N_{d,i} \ c_{w,i} \ c_{d,i})^T$$

$$\vec{x}_{conv}^i = (SM_i \ CAP_i \ k_{max} \ k_1)^T$$

$CR_i$  and  $CD_i$  designate respectively the type of core material and the type of conductor material from a preselected list.  $g_i$ ,  $l_{c,i}$ ,  $w_{e,i}$ ,  $a_i$  are respectively the value of the air gap, the core length, the core width and the conductor area as defined in Fig. 6.  $N_i$ ,  $N_{w,i}$ ,  $N_{d,i}$  are respectively the number of coil turns, the coil width and the coil depth.  $c_{w,i}$  and  $c_{d,i}$  are respectively coil width and depth clearance.

$SM_i$  and  $CAP_i$  designate the type of the semiconductor and the type of capacitor from a preselected list in which all parameters are extracted from manufacturers datasheet.  $k_{max}$  and  $k_1$  are defined in Section III. B.

### B. Optimization constraints

To ensure a realistic and feasible design solutions, constraints  $cs_i$  have been set on operating conditions and physical limits.

The LCL design constraints are set as follows

- $cs_1$ : The insulation factor  $k_w$  should be smaller than the maximum value set to 0.9.
- $cs_2$ : The coil factor  $k_b$  should be smaller than the maximum value set to 0.7.
- $cs_3$ : The current density  $J$  should be smaller than the maximum value set to 7A/mm<sup>2</sup>.
- $cs_4$ : The inductor volume is limited to 10 Liters.
- $cs_5$ : The losses should not exceed 100 W.
- $cs_6$ : The hotspot temperature  $T_h$  of the capacitor should not exceed 85°C.

(a)

(b)

Fig. 19. Simulation results for MMC. Grid current waveform and corresponding harmonic spectrum. (a) Without ac filter. (b) With ac filter.

Fig. 7. 2L-VSC. (a) Effect of the switching frequency on the inductance volume and the converter losses. (b) Semiconductor device losses.

Fig. 8. 2L-VSC. Impact of the switching frequency on the dc-bus capacitance.

Fig. 9. 2L-VSC. Inductances filter variation in function of the switching frequency.

Fig. 10. 2L-VSC. (a) Converter power density. (b) Converter efficiency.

- cs<sub>7</sub>: The highest resonance between  $L_{arm}$  and  $C_c$  should be smaller than the grid frequency.

The converter design constraints are set as follows

- cs<sub>8</sub>: The semiconductor junction temperature should not exceed 120 °C.
- cs<sub>9</sub>: The hotspot temperature  $T_h$  of the capacitor should not exceed 85°C.
- cs<sub>10</sub>: The losses should not exceed 2% of the nominal power rating of the converter.

## VII. RESULTS

The design of the filter and each converter is carried out with the requirement listed in Table I. The optimization was run with a population size of 1000 over 1000 generation. It estimates a high number of design for each requirement and for multiple runs in order to ensure the convergence of the solution. The Pareto optimal Front is obtained, highlighting the power loss and the volume of non-dominated designs of the converter-side filter inductor.

For the 400V/10kW 2L VSC, Fig. 6 depicts the Pareto-optimal Front obtained for the design of the converter-side inductor filter. Designs lying in between the ‘knee’ represents the best trade-off between objectives (lower losses and lower volume) as a design choice in either direction along the front leads to a large increase in one of the objectives. An example of such design is shown in a red star. This design corresponds to a switching frequency of 5.4kHz. Influence of the switching frequency on the inductor volume and losses is depicted in Fig. 7 (a). While the inductance volume decreases with the increase of the switching frequency, the converter losses increase due mainly to the increase of the switching losses as shown in Fig. 7 (b) for one semiconductor device. On the other hand, impact of the switching frequency on the dc-bus capacitor is insignificant as shown in Fig. (8) in which for one design choice of the capacitor technology, the losses remains constant. Fig. 9 depicts the filters inductance versus the

Fig. 11. MMC. Converter-side filter inductor Pareto-optimal Front. Trade-off design (red).

(a)

(b)

Fig. 12. MMC with dc-link connection. (a) Effect of the switching frequency on the inductance volume and the converter losses. (b) Semiconductor device losses per cell.

(a)

(b)

Fig. 13. MMC power density vs efficiency. (a) MMC with dc-link connected. (b) MMC with dc-link floating.

(a)

(b)

Fig 14. MMC. (a) Capacitance cell. (b) Arm inductance.

Fig. 15. MMC. Filter inductances variation in function of the switching frequency.

Fig. 16. MMC. Filter capacitance variation in function of the switching frequency.

Fig. 17. Simulation results. MMC with dc-connected or floating. Voltage variation across the cells capacitors in one arm.

Fig. 18. Losses of one arm. With dc link connected (Top). With dc-link floating (Bottom).

switching frequency. As expected, the inductance values decrease with the switching frequency. The power density of the converter remains high as shown in Fig. 10 (a) with an average value of 4.2 kW/Liters while the efficiency of the converter remains above 99 %. For the design choice on the Pareto optimal Front at 5.4 kHz, the converter efficiency reaches 99.1%.

For the 400V/10kW MMC with both options, the optimization algorithm was run by varying the switching frequency between 300 to 600Hz in such a way to obtain an effective switching frequency similar to the switching frequency of the 2L VSC. The coefficient  $k_{max}$  is varied from 1.05 to 1.2 and  $k_1$  is set to 0.5. The latter is a conservative coefficient to assure an inductor value lower than the resonance inductance occurring at the 4<sup>th</sup> harmonic. The nominal value of the cell capacitor voltage was set to 87.5 V to allow a maximum number of cells of 8. Fig. 11 depicts the optimal Pareto-front for the design of the converter-side inductor. A design choice located in between the ‘knee’ of the Pareto-Front is highlighted. The corresponding filters

and MMC components rating for this specific design will be set in the simulation model

Influence of the switching frequency on the inductor volume and the converter losses is depicted in Fig. 12 (a). Non-dominant designs lie between 586 and 600 Hz with little influence on the converter losses. This is due to the fact that the device switching losses are weakly dependent on the switching frequency and do not impact on the overall device losses as depicted in Fig. 12 (b). This suggests that a reduction of the power dissipation may be achieved most

(a)

(b)

Fig. 20. Simulation results for 2L VSC. (a) Converter-side output phase current waveforms and corresponding harmonic spectrum. (b) Grid-side output phase current waveforms and corresponding harmonic spectrum.

effectively by minimizing the conduction losses. However, there is a substantial decrease of the inductance volume. This is a useful indication for the design of the inductor in which lower volume designs can be chosen with little impact on the MMC efficiency. The power density of the converter versus the efficiency is depicted in Fig. 13. For both options, the power density of the converter can reach 30 W/Liters. This remains low compared to the 2L VSC. However, for the case of a floating dc-link, the efficiency exceeds 99.4%. This is due to the fact that the arm current does not have any dc component as exemplified in Fig. 3 and hence the conduction losses are reduced by 25%. In addition, the semiconductor devices are equally stressed and hence, the temperatures are evenly distributed in each cell of the MMC when the dc-link is floating. This has the benefit of designing a more efficient cooling system. For both options, the design of the passive components are similar. Fig. 14 (a) depicts the capacitance value vs the switching frequency, while Fig. 14 (b) depicts the arm inductance value which was chosen with a split factor of 0.5. As mentioned previously, the arm inductance contributes to the ac filtering and hence lower ac filter designs are obtained for both options as shown in Fig. 15. The capacitance of the filter is shown in Fig. 16. The choice of the resonance frequency of the filter was made in such a way the obtained capacitance value leads to a consumption of reactive power lower than 5% of the rated active power.

TABLE II. OPTIMIZATION DESIGN COMPARISON

| 3 $\phi$ LCL filter | 2-L VSC              | MMC with dc link     | MMC without dc link |
|---------------------|----------------------|----------------------|---------------------|
| $L_{fconv}$         | 600 $\mu$ H          | 230 $\mu$ H          | 230 $\mu$ H         |
| $L_{fg}$            | 550 $\mu$ H          | 140 $\mu$ H          | 140 $\mu$ H         |
| $C_f$               | 22 $\mu$ F           | 22 $\mu$ F           | 22 $\mu$ F          |
| Volume              | 6 L                  | 4 L                  | 4 L                 |
| Efficiency          | 99.3 %               | 99.6 %               | 99.6 %              |
| <b>Converter</b>    |                      |                      |                     |
| $L_{arm}$           | ---                  | 230 $\mu$ H          | 230 $\mu$ H         |
| $C_c$               | ---                  | 1.2 mF               | 1.2 mF              |
| $C_{min}$           | 300 $\mu$ F          | ---                  | ---                 |
| Devices             | Si IGBT<br>1.2kV/40A | SiC MOSFET 650V/118A |                     |

|               |          |        |        |
|---------------|----------|--------|--------|
| Power density | 4.2 kW/L | 30 W/L | 38 W/L |
| Volume        | 3 L      | 320 L  | 160 L  |
| Efficiency    | 99.1 %   | 99.2 % | 99.4 % |

For comparison purpose, Table II summarizes the main results of the highlighted design on the respective optimal Pareto-Front. Though, the MMC occupies more space, it exhibits better performance in term of efficiency. This suggests that the MMC is suitable for LV application. Besides, it offers the option of tapping source/loads into the cells and hence allowing to have a multiport converter.

In order to ascertain the feasibility of the optimization design, a simulation model of each converter was built in PSCAD software in which the parameters of the ac filter and the converter components are given in Table II.

Note that for the MMC with both options, i.e., with a dc link connected or left floating, the design of the filter and the converter components are identical. Through the optimization design, results indicated a peak voltage variation of 4.57% across the cell capacitor with  $k_{max}=1.045$  (refer to (5)) and a capacitance equal to 1.2mF. The latter value was implemented in the simulation model. Fig. 17 depicts the voltage variation across the cells capacitors of one arm of the converter. The peak voltage variation is equal to 3.4 % of the rated cell voltage. The error introduced between both approaches comes from the fact that in the optimization algorithm, averaged waveforms are considered.

For losses estimation of the MMC, data parameters of SiC MOSFET 650V/118A from Rohm with the reference SCT3017AL was implemented in the simulation model. Fig. 18 indicates the total arm losses obtained through the simulation. It is worth noting that the method used in the simulation model relies on instantaneous current waveforms whereas the model implemented in the optimization algorithm relies on averaged current values. However, this indicates a very good match between both approaches with an error less than 1% between the simulated model and the optimization algorithm.

Fig. 19 depicts the grid output phase current. The highest harmonic current amplitude is approximately equal to 3% of the rated grid current (Fig. 19 (a)). This is above the limit set by IEEE 519-1992 [25]. With the LCL filter and the arm inductance designed through the optimization to limit the dominant harmonic to 0.3 %, we are able to limit the highest harmonic current amplitude to approximately 0.35% of the rated grid current as shown in Fig. 19 (b). The close match between these values indicates that the developed optimization algorithm accurately predict the parameters design of the filter and the converter.

Similarly, the model of 2L VSC was run with parameters listed in Table II. One of the important design is the LCL filter. Fig. 20 (a) shows the converter-side output phase current in which the highest current harmonic is approximately equal to 2%. The filter capacitance is able to absorb all harmonics and the grid-side output phase current is almost exempt of all harmonics as shown in Fig. 20 (b). Losses were estimated with data parameters of Si IGBT 1.2kV/40A from Infineon with the reference IKQ40N120CT2, 1% higher losses were observed in the simulation model.

## VIII. CONCLUSION

In this paper, a modular multilevel converter tapping cells is proposed as a multiport converter for a hybrid LV

ac/dc microgrid. The performance of the MMC-tapping cells, associated with a LCL filter in term of efficiency and power density has been assessed using a bi-objective optimization based on the Genetic Algorithm and has been compared with the conventional 2L VSC. It is shown that the MMC exhibits higher efficiency, reaching 99.4 % when the main dc-grid is left floating. Simulation results showed that the optimized converter parameters ratings estimation and the choice of the semiconductor device technology was accurate with less than 1% error on losses estimation. However, due to the modularity and the scalability of the MMC, offering multiport connections option, low power densities of the MMC remain the main disadvantage.

The design of the converter-side filter inductor was combined with the design of the arm inductance of the MMC. Results showed that the converter-side inductor was much smaller for the MMC compared to the filtering inductance used for the 2-L VSC. This implies that ac filters are not bulky anymore and encourages the use of the MMC tapping cells in LV application.

#### ACKNOWLEDGMENT

This work was supported by the Engineering and Physical Sciences Research Council under Grant EP/N034570/1. Data supporting this publication can be obtained on request from [cappublications@imperial.ac.uk](mailto:cappublications@imperial.ac.uk)

#### REFERENCES

- [1] G. Strbac, N. Hatziaargyriou, J. P. Lopes, C. Moreira, A. Dimeas, D. Papadaskalopoulos, "Microgrids –Enhancing the Resilience of the European Megagrid," *IEEE Power and Energy Magazine*, vol. 13, no. 3, pp. 35-43, May-Jun. 2015.
- [2] E. Unamuno, J. A. Barrena, "Hybrid ac/dc microgrids –Part I: Review and classification of topologies," *Elsevier, Renewable and Sustainable Energy Reviews*, vol. 15, pp. 1251-1259, Dec. 2015.
- [3] H. Kakigano, Y. Miura, T. Ise, "Low-Voltage Bipolar-Type DC Microgrid for Super High Quality Distribution," *IEEE Trans. Power Electronics*, vol. 25, no. 12, pp. 3066-3075, Dec. 2010.
- [4] Y. Hahashi, M. Mino, "High-density Bidirectional Rectifier for Next Generation 380-V DC Distribution System," in *Proc. 2012 IEEE Applied Power Electronics Conf.*, pp. 2455-2460.
- [5] M. Corti, E. Tironi, G. Ubezio, "DC Networks Including Multiport DC/DC Converters: Fault Analysis," *IEEE Trans. Industry Applications*, vol. 52, no. 5, pp. 3655/3662, Sept.-Oct. 2016.
- [6] Q. Xiao, H. Jia, B. Liang, J. He, "Current Balancing Control for Multiport Hybrid AC/DC Microgrid," in *Proc. 2017 IEEE Power and Energy Society General Meeting*, pp. 1-5.
- [7] R. Majumder, "A Hybrid Microgrid with DC Connection at Back to Back Converters," *IEEE Trans. Smart Grid*, vol. 5, no. 1, pp. 251-259, Jan. 2014.
- [8] L. Zhang, F. Gao, N. Li, Q. Zhang, C. Wang, "Interlinking Modular Multilevel Converter of Hybrid AC-DC Distribution System with Integrated Battery Energy Storage," in *Proc. 2015 IEEE Energy Conversion Congress and Exposition*, pp. 70-77.
- [9] Y. Zhong, N. M. Roscoe, D. Holliday, S. J. Finney, "MMC with Parallel-connected MOSFETs as an alternative to Wide Bandgap for LVDC Distribution Networks," *The Journal of Engineering*, vol. 2017, no.5, pp. 149-157, May 2017.
- [10] J. Kolb, F. Kammerer, P. Grabherr, M. Gommeringer, M. Braun, "Boosting the efficiency of Low Voltage Modular Multilevel Converters beyond 99%," in *Proc. PCIM Europe 2013 -International Exhibition and Conf. for Power Electronics, Intelligent Motion, Renewable Energy and Energy management*, pp. 1157-1164.
- [11] T. Kinjo, Y. Hayashi, Y. Sato, H. Ohashi, "Study on high power density integration of multilevel converters," in *Proc. 4th International Conf. On Integrated Power Systems*, pp. 1-4.
- [12] S. Am, P. Lefranc, D. Frey, M. Ibrahim, "A Generic Virtual Prototyping Tool for Multilevel Modular Converters (MMCs)," in *Proc. IECON 2015 - 41st Annual Conf. of the IEEE Industrial Electronics Society*, pp. 1489-1494.
- [13] A. Lachichi, A. Junyent-Ferre, T. Green, "Power Converters Design for Hybrid LV ac/dc Microgrids," in *Proc. 2017 IEEE 6th International Conf. on Renewable Energy Research and Applications*, pp. 850-854.
- [14] M. L. Heldwein, J. W. Kolar, "Impact of EMC Filters on the Power Density of Modern Three-Phase PWM Converters," *IEEE Trans. Power Electronics*, vol. 24, no. 6, pp. 1577-1588, Jun. 2009.
- [15] R. Beres, X. Wang, F. Blaabjerg, C. L. Bak, H. Matsumori, T. Shimizu, "Evaluation of Iron Loss of AC Filter Inductor Used in Three-Phase PWM Inverters Based on an Iron Loss Analyzer," *IEEE Trans Power Electronics*, vol. 31, no. 4, pp. 3080-3095, Apr. 2016.
- [16] J.W. Kolar, J. Biela, S. Waffler, T. Friedli, U. Badstuebner, "Performance Trends and Limitations of Power Electronics Systems," in *Proc. 2010 6th International Conf. on Integrated Power Electronics Systems*, pp. 1-20.
- [17] R. Burkart and J. W. Kolar, "Comparative  $\eta$ - $p$ - $\sigma$  Pareto Optimization of Si and SiC Multi-Level Dual Active Bridge Topologies with Wide Input Voltage Range," *IEEE Trans. Power Electronics*, vol. 32, no. 7, pp. 5258-5270, Jul. 2017.
- [18] E. K. Chong, S. H. Zak, *An introduction to Optimization*, 3rd ed., Hoboken, NJ: John Wiley & Sons, 2008.
- [19] D. E. Goldberg, *Genetic Algorithms in Search, Optimization, and Machine Learning*, Boston: Addison Wesley Longman, 1989.
- [20] K. Ilves, S. Norrga, L. Harnefors, H.-P. Nee, "On Energy Storage Requirements in Modular Multilevel Converters," *IEEE Trans. Power Electronics*, vol. 29, no. 1, pp. 77-88, Jan. 2014.
- [21] S. Kwak, H. A. Toliyat, "Design and Rating Comparisons of PWM Voltage Source Rectifiers and Active Power Filters for AC Drives With Unity Power Factor," *IEEE Trans Power Electronics*, vol. 20, no.5, pp. 1133-1142, Sept. 2005.
- [22] U. Drofenik, G. Laimer, J. W. Kolar, "Theoretical Converter Power Density Limits for Forced Convection Cooling," in *Proc. 2005 International Conf. on Power Electronics Intelligent Power Quality*, pp. 608-619.
- [23] K. Ilves, A. Antonopoulos, S. Norrga, H-P. Nee, "Steady-State Analysis of Interaction Between Harmonic Components of Arm and Line Quantities of Modular Multilevel Converters," *IEEE Trans. Power Electronics*, vol. 27, no. 1, pp. 57-68, Jan. 2012.
- [24] A. Marzoughi, R. Burgos, D. Boroyevich, "Optimum Design Guidelines for the Modular Multilevel Converter in Active Front-End Applications: Considerations for Passive Component Reduction," *IEEE Power Electronics Magazine*, vol. 5, no. 2, pp. 56-65, Jun. 2018.
- [25] *IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems*, IEEE Standard 519-1992, May 1992.
- [26] M. Liserre, F. Blaabjerg, S. Hansen, "Design and Control of an LCL-Filter-Based Three-Phase Active Rectifier," *IEEE Trans. Industry Applications*, vol. 41, no. 5, pp. 1281-1291, Sept.-Oct. 2005.
- [27] G. Holmes, T. A. Lipo, *Pulse Width Modulation for Power Converters: Principles and Practice*, Hoboken, NJ: John Wiley, 2003.
- [28] B. P. McGrath, C. A. Teixeira, D.G. Holmes, "Optimised Phase Disposition (PD) Modulation of a Modular Multilevel Converter," *IEEE Trans. Industry Applications*, vol. 53, no. 5, pp. 4624-4633, Sept.-Oct. 2017.
- [29] M. K. Kazimierczuk, *High-Frequency Magnetic Components*, 2nd ed., Hoboken, NJ: John Wiley & Sons, 2014.
- [30] C. W. T. McLyman, *Transformer and Inductor Design Handbook*, 3rd ed, Hoboken, NY: Marcel Dekker, 2004.
- [31] R. Beres, X. Wang, F. Blaabjerg, C. L. Bak, H. Matsumori, T. Shimizu, "Evaluation of Core Loss in Magnetic Materials Employed in Utility Grid AC Filters," in *Proc. 2016 IEEE Applied Power Electronics Conf.*, pp. 3051-3057.
- [32] M. Bartoli, A. Reatti, M. K. Kazimierczuk, "Minimum Copper and Core Losses Power Inductor Design", in *Proc. 1996 IEEE Industry Applications Conf. 31st IAS Annual Meeting*, pp. 1369-1376.
- [33] M. Bartoli, N. Noferi, A. Reatti, "Modeling Litz-Wire Winding Losses in High Frequency Power Inductors," in *Proc. 1996 IEEE Power Electronics Specialists Conf.*, vol. 2, pp. 1690-1696.
- [34] S. Allebrod, R. Hamerski, R. Marquardt, "New Transformerless, Scalable Modular Multilevel Converters for HVDC-Transmission," in *Proc. 2008 IEEE Power Electronics Specialists Conf.*, pp. 174-179.

**Amel Lachichi** received the Engineering degree from Ecole Nationale Polytechnique of Algiers, Algeria in 1996, the DEA from Ecole Nationale Supérieure d'Electricité et de Mécanique, Nancy, France in 2000, and the Ph.D. degree from the Université of Franche Comte, France, in 2005. From 1997 to 1999, she worked on designing grid

distribution networks in airports, Algeria. After two years of Post doctorate Research at the University of Manchester, UK, she joined ABB Corporate research, Vasteras, Sweden in 2010 as a scientist in Power Electronics. From 2016 to 2018 she was a research associate at Imperial College London, UK. Since 2019, she is a research fellow with the University of Warwick, UK, investigating the reliability of Power converters for offshore application.

**Adria Junyent-Ferre** (S'09–M'11–SM'19) obtained his Industrial Engineering degree from the School of Industrial Eng. of Barcelona (ETSEIB), Technical University of Catalonia (UPC) in 2007, and the Ph.D. in Electrical Eng. from the UPC in 2011. He was a Researcher at CITCEA-UPC from 2006 to 2012 and a Lecturer at the Barcelona College of Industrial Engineering (EUETIB) in 2012. He joined the Dept. of Electrical and Electronic Eng. at Imperial College London in 2013 and became a Lecturer in 2014. His research focuses on control of power electronic converters and their design, with specific focus on wind power, VSC-HVDC and microgrids.

**Tim C. Green** received a B.Sc. (Eng) (first class honours) from Imperial College London, UK in 1986 and a Ph.D. from Heriot-Watt University, Edinburgh, UK in 1990. He is a Professor of Electrical Power Engineering at Imperial College London, and Director of the Energy Futures Lab with a role of fostering interdisciplinary energy research across the university. His research uses the flexibility of power electronics to create electricity networks that can accommodate greater amounts of low carbon technologies. In HVDC, he has contributed converter designs that strike improved trade-offs between power losses, physical size and fault handling. In distribution systems, he has pioneered the use of soft open points and the study of stability of grid connected inverters. Prof. Green is a Chartered Engineering in the UK and a Fellow of the Royal Academy of Engineering.