
Reconfigurable Nanowires for Thermo-Electric Applications

By

ALI HAMID

Department of Electrical and Electronic Engineering
IMPERIAL COLLEGE LONDON

Dissertation submitted to the Imperial College London
in accordance with the requirements of the degree of
DOCTOR OF PHILOSOPHY in the Faculty of Engineering.

OCTOBER 2020

STATEMENT OF ORIGINALITY

I hereby confirm that the content of this dissertation is original work carried out by the author in Department of Electrical and Electronic Engineering in Imperial College London.

COPYRIGHT

The copyright of this thesis rests with the author. Unless otherwise indicated, its contents are licensed under a Creative Commons Attribution-Non Commercial 4.0 International Licence (CC BY-NC).

ABSTRACT

Nano-structuration of bulk into nanowires and nanosheets has led to massive changes in device behaviour and to opportunities for designing novel devices that exploit these changes. The combination of these two consequences of nanoscale devices in integrated circuits will lead to further enhancements in their performance in the future.

In this project, different novel device structures have been designed and their performance investigated using Sentaurus Technology Computer Aided Design (TCAD) software. Sentaurus TCAD is a commercial software package that is used in the semiconductor industry to predict the behaviour of nanoscale devices. Its transport models have been tuned and calibrated over at least the last decade to give realistic performance parameters of novel device structures.

One current trend in semiconductor device technology that we have embraced in this work is the replacement of n^+/p (p^+/n) junctions as contacts to the external world by metal/semiconductor Schottky contacts. This resolves the $\frac{k_B T}{q}$ limitation of diffusive processes leading to better device performance parameters.

In this work, doping has been avoided in order to maximise the mobility of the carriers and minimise the challenges with doping control in nanostructures. Carrier modulation techniques have been implemented to control the thermal and electrical conductivities of the novel devices designed in this work.

This project focused on two areas of research. One is the solution of the traditional a-symmetric current-voltage characteristics of the p- and n-FET in CMOS. A novel reconfigurable double gate nanowire structure with oxide bridges that controls the symmetry of operation of the p- and n-FET in CMOS was designed. Not only can the approach be integrated in CMOS technology, it is also relatively tolerant to small geometrical deviations. The challenge in this design lies in the oxide bridge perpendicular to the gate length direction.

Nano-structuration of Si also leads to a reduction of the thermal conductivity. Although this is a problem for nanowire and nanosheet FETs due to increased self-heating,

it also leads to opportunities offered for on-chip thermo-electric power generation, TEG (or thermoelectric cooling (TEC)) and temperature sensors.

We propose a carrier modulation technique based on the workfunction difference between the gate metal and the intrinsic NW - a technique similar to a nanoFET process and thus compatible with CMOS technology - that shows an increase in the TEG's performance.

Another application where thermo-electrics can be used is in on-chip temperature sensing. Currently on-chip temperature sensors suffer from high power consumption and high real estate on the chip. We use a gated reconfigurable Si nanowire FET as temperature sensor that in principle works on the same supply rail as the circuits and is sufficiently small to be placed close to where hotspots will occur. The gate voltage that needs to be applied to keep the current constant as a function of temperature difference is a measure of heating. Due to the weak electrical conductivity of the nanowire, an efficient temperature difference can be maintained between the hotspot and the surrounding thermal mass minimising the need for re-calibration.

Journal

1. Hamid, A., and Fobelets, K., "Simulation Study: Reconfigurable Nanowire Transistors with Bridged Program Gates", (to be submitted), 2020.
2. Hamid, A., and Fobelets, K., "Gated silicon nanowire for thermo-electric power generation and temperature sensing", (to be submitted), 2020.

Conference papers/presentations

3. Hamid, A., Fobelets, K., and Velazquez-Perez, J.E., "Reconfigurable Nanowires Phononics for Temperature Sensing and Thermoelectric Applications" , ICON 2017, Athens, 2017.
4. Hamid, A., Fobelets, K., and Velazquez-Perez, J.E., "Thermo-Electric Power Generators Using Gated Silicon Nanowires". In 2017 European Modelling Symposium (EMS) (pp.

168-173). IEEE, 2017.

5. Hamid, A., Fobelets, K., and Velazquez-Perez, J.E., "Thermoelectric power generation by gated silicon nanowires" , UK Thermoelectric Network Meeting, 14th Feb 2018, Edinburgh, 2018.

6. Hamid, A., Fobelets, K., and Velazquez-Perez, J.E., "Reconfigurable Nanowires Phononics for Temperature Sensing and Thermoelectric Applications", ICON 2018, London, 2018.

7. Hamid, A., Fobelets, K., and Velazquez-Perez, J.E., "TCAD study of gated-thermoelectrics in $Si_{1-x}Ge_x$ nanowires" , ISTDM / ICSI 2018 conference , 27th May 2018, Potsdam, 2018.

TABLE OF CONTENTS

Journal	vi
Conference papers/presentations	vi
	Page
List of Figures	xi
1 Introduction	1
2 Metal oxide field effect transistor (MOSFETs)	3
2.1 Building blocks of FETs	4
2.1.1 p-n junctions	4
2.1.2 Schottky contacts	5
2.1.3 Metal/oxide/semiconductor (MOS) interfaces	8
2.1.4 Tunable Schottky barriers to control current flow across an intrinsic channel	8
2.2 From MOSFETs to NanoFETs	11
2.3 Performance evaluation of FETs	14
2.4 Intrinsic gated Si RNW-FETs	17
2.5 Deposition of interconnect layers	20
2.6 Summary	21
3 Thermo-electric power generation and temperature sensing	23
3.1 Theory of thermo-electric power generation	24
3.1.1 Seebeck coefficient and voltage difference	26
3.1.2 Figure of merit	26
3.2 Optimising power generators	31
3.2.1 Reducing thermal conductivity	31
3.2.2 Optimising the power factor via carrier modulation	34
3.3 On-chip temperature sensing	38

3.4	Summary	41
4	Sentaurus technology computer aided design (TCAD)	43
4.1	Poisson equation, conduction band, and valence band	45
4.2	Simulation of Schottky barriers	46
4.3	Simulation of contacts on insulators	47
4.4	Hydrodynamic model for current and temperature	48
4.4.1	The hydrodynamic model	48
4.4.2	Initial guess in hydrodynamic model	52
4.5	Sources of Mobility degradation and models used for their calculation . .	53
4.5.1	Philips mobility model (PhuMob)	54
4.5.2	Enormal model	56
4.5.3	High field saturation (HFE) model	57
4.6	Boundary conditions	58
4.7	Summary	59
5	Reconfigurable nanowire transistors with bridged program gates	61
5.1	Model evaluation and calibration	63
5.2	Asymmetric gates for n-FET and p-FET	66
5.3	Bridging the program gates of the p-FET	69
5.4	Physics and performance differences between asymmetric gates and the bridged method	74
5.5	Fabrication process of bridged method and effect of subsequent processing step	76
5.6	Impact of fabrication inaccuracies in gate length and bridge dimensions .	78
5.7	Conclusion	79
6	Gated Silicon nanowire for thermo-electric power generation and tem- perature sensing	81
6.1	Gated i-Si for thermo-electric power generation	81
6.2	Gated structure for temperature sensing	89
6.3	Conclusion	93
7	Grading carrier density to optimise thermo-electric power generation	95
7.1	Grading mole fraction of gated $Si_{1-x}Ge_x$	96
7.2	Grading the area of gated Si NW	104
7.3	Conclusion	109

TABLE OF CONTENTS

8 Summary and conclusion	111
Bibliography	113

LIST OF FIGURES

FIGURE	Page
2.1 Uniformly doped n-type and p-type semiconductor (a) before, and (b) after contact. P-n junction at (c) forward (V_F), and (d) reverse (V_R) bias voltage. Where E_{fn} (E_{fp}) is quasi Fermi level of electrons (holes), E_i is intrinsic Fermi level, E_c is conduction band, and E_v is valence band; and $q\psi_n$ ($q\psi_p$) is the difference of E_i with E_{fn} (E_{fp}).	4
2.2 Ideal metal/i-semiconductor with $\phi_m > \phi_s$ (a) before contact, and (b) after contact at zero external voltage.	6
2.3 Shows electric field dispersion of a charge in a semiconductor (a) before, and (b) after contact with metal. (c) Schottky barrier lowering due to introduction of image potential energy. x_m is x at maximum barrier height, $\Delta\phi_B$ is barrier lowering	7
2.4 Metal/oxide/i-semiconductor with $\phi_m = \phi_s$ at (a) $V_{gate} = 0$ V, (b) $V_{gate} > 0$ V (accumulation of electrons), and (c) $V_{gate} < 0$ V (accumulation of holes).	8
2.5 (a) Shows a double gated RNW-FET with Schottky contacts at source and drain; and a control gate and a program gate. (b) Barriers faced by carriers in metal and semiconductor. Thermionic field emission (TFE) and field emission (FE) in (c) forward and (d) reverse bias.	9
2.6 3D view of a simple n-type MOSFET structure.	11
2.7 Gate length and number of transistors on chip starting from 1965.	12
2.8 Shows (a) gated FET with ultra-thin body (UTB-FET), (b) top and back gated FET, (c) finFET, and (d) gate-all-around FET (GAA-FET).	13
2.9 Shows I_d - V_d characteristic of an ideal MOSFET. The saturation current increases as V_{gate} increases.	14

LIST OF FIGURES

2.10	Shows a metal/ SiO_2 /p-semiconductor (a) with flat band at $V_{gate} = 0$ V, and (b) in inversion with $V_{gate} = V_{th} < 0$ V. Metal/ SiO_2 /n-semiconductor (c) with flat band at $V_{gate} = 0$ V, and (d) in inversion with $V_{gate} = V_{th} > 0$ V. Work functions and electron affinity are given in electron volt (eV)	15
2.11	For an NMOS (a) $\sqrt{I_d}$ - V_{gate} graph for extracting V_{th} in saturation region, and (b) I_d - V_{gate} graph for SS extraction.	16
2.12	Shows ON and OFF state of p- and n- configuration for (a) TG Si RNW-FET, and (b) DG Si RNW-FET with aligned mid-band gap with Fermi level of metal	18
2.13	Shows the interconnect layers on top of the pre-metal dielectric layer and tungsten contact plug, to connect the fabricated NMOS and PMOS to other parts on the IC.	20
3.1	Schematic of (a) a two legged TEG containing a series connection of an n-type and p-type legs sandwiched between a hot (T_h) and cold (T_c) plate; and (b) a single legged TEG with arrays of parallel connected n-type Si-NWs in between hot source and cold sink.	25
3.2	(a) The Seebeck coefficient (S), electrical conductivity (σ), σS^2 , and (b) total thermal conductivity (κ), lattice thermal conductivity (κ_L), and electronic thermal conductivity (κ_e) of metal, semiconductor, and insulator as a function of electron density (n) in log scale.	27
3.3	(a) Thermal conductivity as a function of diameter for rough surface (Houchbaum et al.), smooth surface (Li et al.), lowly Boron doped = $1 \times 10^{13} \text{ cm}^{-3}$ (Shi et al), and highly boron doped = $1 \times 10^{19} \text{ cm}^{-3}$ (Shi et al). (b) Thermal conductivity of bulk Silicon doped with $4.875 \times 10^{20} \text{ cm}^{-3}$ of boron (B), arsenic (As), phosphorus (P), and aluminum (Al). Thermal conductivity variation due to mass difference, bond strength, and strain were individually studied in simulation, while other effects were assumed constant, to better understand their impact on total κ_L ($\kappa_{SiX}(\text{total})$)	32
3.4	(a) Thermal conductivity of $Si_{1-x}Ge_x$ as a function of mole fraction (x) for different diameters (D) of NWs. (b) thermal conductivity of $Si_{1-x}Ge_x$ as a function of diameter (D) for different mole fractions (x).	33

3.5	(a) 3D view of p^+ -Si/i-Si shell/core structure, to modulate hole concentration in i-Si. (b) Sketched band diagram of p^+ -Si/i-Si/ p^+ -Si before and after contact with each other, to explain the theory of this method. (c) 3D gated heterostructure to further control the modulated holes in i-Ge, due to its contact with p^+ -Ge/i-Si. (d) Energy band (left axis) and hole concentration (right axis) across the radius of the structure; where red is for i-Ge ($d = 6$ nm)/ p^+ -Ge ($d = 1$ nm)/i-Si ($d = 2$ nm) with p^+ -Ge = 1×10^{19} ; and dashed line is for i-Ge ($d = 7$ nm)/ p^+ -Ge ($d = 2$ nm)/i-Si ($d = 2$ nm) with p^+ -Ge = 2.2×10^{18}	35
3.6	(a) Transmission electron microscopy image of a fabricated i-AlGaIn/i-AlN/i-GaN to modulate electron concentration in i-GaN, where i stands for intrinsic. (b) Fabricated i-Si/i-Ge structure to accumulate holes in intrinsic Ge. (c) Band diagram of (b), showing the accumulated holes in germanium while Si remained intrinsic.	36
3.7	(a) σS^2 - n , (b) $\kappa_{(e, Si)}$ - n , (c) ZT - n for gated and doped Si with $d_{Si} = 12$ nm and $\kappa_{(L, Si)} = 1 \frac{W}{mK}$; and (d) ZT - n of the simulated NW in Neophytou et al work with $\kappa_{(L, Si)} (= 6.47 \frac{W}{mK})$ obtained in Shi et al theoretical work. The blue solid lines are the results for gated Si NW considering phonon scattering only, blue dotted lines are the data for gated Si NW considering both phonon scattering and surface roughness scattering (SRS), and black lines are results for doped Si.	37
4.1	(a) Diagram of simulation flow of these projects using sentaurus TCAD. (b) Cross section of the meshed designed geometry.	44
4.2	(a) 3D view of a RNW-FET with triple gates, (b) cross section of the RNW-FETs with gate voltages of V_{gate1} , V_{gate2} , and V_{gate3} , and drain voltage of V_d	44
5.1	(a) SEM image of optimised nanowire stacks. (b) image of the device after program gate deposition. (c) Image of the device after control gate deposition using self aligned method.	63
5.2	(a) Schematic of the simulated nanowire with 2D source and drain metal contacts, to predict the experimental results shown in De Marchi's work. (b) The drain current (I_d) as a function of control gate voltage (V_{CG}) for the simulated (sim.) structure and the experimented (exp.) device in De Marchi's work. I_d - V_{CG} is shown for different program gate voltages (V_{PG}); and constant drain voltage (V_d) of 2V, for all the of the shown results.	65

- 5.3 (a) shows both the simulations and experiments for Si based RNWs with (a) $\langle 112 \rangle$ orientation channel, and (b) strained $\langle 110 \rangle$ orientation channel. 65
- 5.4 (a) 3D view and (b) front view of simulated Si RNW-FETs with $L_{Gn} = 20$ nm and $L_{Gp} = 43$ nm gate lengths for n-FET and p-FET respectively. (c) Cross section of FETs shown in (a). L_{ug} is length of un-gated region. S_n , S_p , D_n , and D_p are n-FET source, p-FET source, n-FET drain, and p-FET drain respectively. Online colour: Light blue regions are the Ti gates, burgundy is SiO_2 , the grey areas are the $NiSi_2$ contacts, dark blue is intrinsic Si. 66
- 5.5 (a) Conduction band (E_c) along the the length of the n-FETs with $L_{Gn} : 20$ nm, 30 nm, 40 nm, 50 nm, and 60 nm. (b) Carrier concentration- L_{Gn} at the centre of gated region (X_g) and at un-gated region (X_{ug}). E_c and carrier concentration of n-FETs are plotted in the middle of the channel along x. E_{fn} is the Fermi level of the n-FETs. ϕ_{cug} is the height of the potential barrier. N-FETs are at $V_{PG_n} = V_{CG_n} = 2$ V and $V_{d_n} = 0$ V 67
- 5.6 (a) I_d - V_d graph for n-FET and p-FET at $|V_{PG_{n,p}}| = 2$ V and (1) $|V_{CG_{n,p}}| = 2$ V, (2) $|V_{CG_{n,p}}| = 1.75$ V, (3) and $|V_{CG_{n,p}}| = 1.5$ V, where $V_{PG_{n,p}}$, $V_{CG_{n,p}}$, and $V_{d_{n,p}}$ are the program gate, control gate, and drain voltage of n- and p-FETs, respectively. (b) $I_d - V_{CG}$ with $|V_{PG_{n,p}}| = |V_{d_{n,p}}| = 2$ V. (c) I_{on} - L_G for both FETs at $|V_{PG_{n,p}}| = |V_{CG_{n,p}}| = |V_{d_{n,p}}| = 2$ V. (d) $\frac{I_{on}}{I_{off}} - L_G$ for both modes. I_{on} and $\frac{I_{on}}{I_{off}}$ for n-FET with $L_{Gn} = 20$ nm and p-FET with $L_{Gp} = 43$ nm are shown by lines (1) and (2), respectively. L_{Gn} (L_{Gp}) in (c) and (d) is varied while $L_{Gp} = 43$ nm ($L_{Gn} = 20$ nm), respectively. 68
- 5.7 (a) 3D and (b) cross section of bridged method. Online colour: Light blue regions are the Ti gates, burgundy is SiO_2 , the grey areas are the $NiSi_2$ contacts, dark blue is intrinsic Si. 69
- 5.8 (a) Carrier concentration of the un-bridged n-FET with $L_G = 30$ nm when $V_{PG_n} = V_{CG_n} = 2$ V and $V_{d_n} = 0$ V, (b) carrier concentration of the bridged n-FET with $L_G = 30$ nm, $L_{ox} = 52$ nm, and $W_{ox} = 18$ nm when $V_{CG_n} = V_{PG_n} = 2$ V, $V_{d_n} = V_{d_p} = 0$ V, and $V_{PG_p} = -2$ V. (c) Conduction band (E_c) along x-direction for the un-bridged (red) and bridged (blue) n-FETs shown in (a) and (b). (d) The electron density of n-FET with $L_G = 30$ nm in (x_2, z_2) under the $PG_p/SiO_2/i$ -Si capacitor as a function of W_{ox} and L_{ox} at same bias as in (b). 70

5.9	(a) I_{on} - L_{ox} for the bridged n-FET with $L_G = 30$ nm (diamond) and $L_G = 40$ nm (circle) at $V_{CG_n} = V_{PG_n} = V_{d_n} = 2$ V and $V_{PG_p} = -2$ V; and (b) I_{on} - L_{ox} for the bridged p-FET with $L_G = 30$ nm (diamond) and $L_G = 40$ nm (circle) at $V_{CG_p} = V_{PG_p} = V_{d_p} = -2$ V and $V_{PG_n} = 2$ V. The positions of n-FET and p-FET are shown in fig 5.7 (a).	71
5.10	E_c along x-direction of the bridged n-FET channel for $L_G = 30$ nm and 40 nm. Both FETs have $L_{ox} = 50$ nm and $W_{ox} = 18$ nm when $V_{CG_n} = V_{PG_n} = 2$ V, $V_{d_n} = 0$ V, and $V_{PG_p} = -2$ V.	72
5.11	Output characteristic of n- and p-FET in bridged approach for (a) $L_G = 30$ nm, $W_{ox} = 18$ nm, $L_{ox} = 52$ nm; and (b) $L_G = 40$ nm, $W_{ox} = 18$ nm, $L_{ox} = 50$ nm when $ V_{PG_{n,p}} = 2$ V and (1) $ V_{CG_{n,p}} = 2$ V, (2) $ V_{CG_{n,p}} = 1.75$ V, (3) and $ V_{CG_{n,p}} = 1.5$ V. Transfer characteristic of n- and p-FET for (c) $L_G = 30$ nm and (d) $L_G = 40$ nm in bridged method (solid lines), and un-bridged n-FET (dotted lines) when $ V_{PG_{n,p}} = V_{d_{n,p}} = 2$ V. $W_{ox} = 18$ nm, $L_{ox} = 52$ nm for bridged n-FET with $L_G = 30$ nm in (c); and $W_{ox} = 18$ nm, $L_{ox} = 50$ nm for bridged n-FET with $L_G = 40$ nm in (d).	73
5.12	Comparing ON current symmetry factors for n- and p-FETs of this work with previous works shown in table 2.1.	73
5.13	E_c along the length of the studied nanowires are plotted along z_1 (solid) and z_2 (dotted), when $V_{CG_n} = V_{PG_n} = 2$ V, $V_{d_n} = 0$ V, and $V_{PG_p} = -2$ V. The red lines are the conduction bands of un-bridged n-FET ($L_{ox} = 0$ V) with $L_{Gn} = L_{Gp} = 40$ nm. E_c of bridged method with $L_G = 40$ nm and $W_{ox} = 18$ nm are shown in blue; and conduction band of n-FET shown in fig 5.4 (c) are plotted in green.	74
5.14	(a) SOI wafer with 1 μm of buried SiO_2 and 10 nm of device layer. (b) E-beam written Si NWs after RIE. (c) The formed $NiSi_2$, after annealing the Ni.	76
5.15		77
5.16	Final schematic of the device, after deposition of titanium.	77
5.17	(a) ON current as a function of variation from the mean, and (b) E_c at z_1 along the channel for bridged n-FET with $L_G = 40$ nm, $L_{ox} = 50$ nm, and $W_{ox} = 18$ nm.	78
6.1	(a) The energy band diagram of the metal/ SiO_2 /i-Si structure before contact. (b) Metal/ SiO_2 /i-Si structure after contact when (b) $\phi_m < \phi_{Ti}$, and (c) $\phi_m > \phi_{Ti}$, leading to accumulation of electrons and holes at Si/ SiO_2 , respectively.	82
6.2	(a) Front view, (b) cross section of simulated gated i-Si. For the sake of simulation efficiency, all metals are defined as 2D contacts only.	82

LIST OF FIGURES

6.3	(a) electron density and (b) electron mobility of gated i-Si with $d_{Si} = 12$ nm. Both at middle of the NW length. (c) electron density and, (d) electron mobility as a function of ϕ_m of metal gate and d_{Si} for gated i-Si at $\Delta T = 0$ K. Labeling: C refers to the middle of the NW and int is interface. The values are given at $int = r_{Si}-1$ nm and C is the core of the NW (centre), where r_{Si} is the radius. .	84
6.4	(a) Normalised σ - ϕ_m (dashed) and S - ϕ_m (solid), (b) normalised σS^2 - ϕ_m , (c) ΔV - ϕ_m , and (d) I_g - ϕ_m at $\Delta T = 15$ K for $d_{Si} = 12$ nm, 37 nm, and 62 nm. Normalised amount = $\frac{x-x_{min}}{x_{max}-x_{min}}$, where x can be S , σ , or σS^2 ; and x_{min} (S_{min} , σ_{min} , or σS^2_{min}) is the minimum amount, and x_{max} (S_{max} , σ_{max} , or σS^2_{max}) is the maximum amount.	85
6.5		86
6.6	(a) Power-time, and (b) ΔT -time of simulated NWs with d_{Si} : 12, 37, and 62 nm. Heat sink loses its temperature at time > 0	87
6.7	Power- D_{it} for GAA i-Si NW with $d_{Si} = 12$ nm, $\Delta T = 15$ K, and two ϕ_m : 3.9, and 4.1 eV.	88
6.8	(a) Electron density- V_{gate} , and (b) power- V_{gate} for $d_{Si} = 12$ nm, $d_{ox} = 8$ nm, and $D_{it} = 10^{12} cm^{-2}eV^{-1}$	89
6.9	(a) Schematic of a DG temperature sensor with program gate (PG) and control gate (CG). (b) E_c along the length of the SG and DG (CG lengths of 30 or 50 nm) GAA NW for $-0.4 V < V_{gate,CG} < 0 V$. The NW length is 220 nm and $d_{Si} = 12$ nm.	90
6.10	(a) I_g - T_h in the SG NW for $d = 12$ nm, 37 nm, and 62 nm. (b) The variation of I_g as a function of the control voltage V_G and V_{CG} for the SG and DG NWs at a $\Delta T = 1$ K.	91
6.11		93
7.1	(a) Energy and electron density of the un-gated graded SiGe from $x_1 = 0$ to $x_2 = 0.8$. (b) Cross section of the gated graded ($x_1 \rightarrow x_2$) SiGe with temperature T_{x_1} at x_1 and T_{x_2} at x_2	96
7.2	Shows (a) electron density, and (b) electron mobility of graded ($x_1 = 0 \rightarrow x_2 = 0.8$) SiGe with $\phi_m = 4.0$ eV metal gate at $\Delta T = 0$ K.	98
7.3	Shows electron density along the length of the gated ($\phi_m = 4$ eV) graded ($x_1 = 0 \rightarrow x_2 = 0.8$) and un-graded SiGe, plotted at (a) interface and (b) centre shown in fig 7.2. $\ln\left(\frac{N_c}{n}\right)$ -X of the gated ($\phi_m = 4$ eV) graded ($x_1 = 0 \rightarrow x_2 = 0.8$) and un-graded SiGe, plotted at (c) interface and (d) centre. The NWs are in open circuit.	99

7.4	Shows E_c along the length of the gated ($\phi_m = 4$ eV) graded ($x_1 = 0 \rightarrow x_2 = 0.8$) and un-grdaed SiGe, plotted at (a) interface (Int) and (b) centre of the NWs shown in fig 7.2. The nanowires are in open circuit.	100
7.5	Shows m_n^* along the length of un-graded ($x = 0.4$) and graded ($x_1 = 0 \rightarrow x_2 = 0.8$) NWs with $\Delta T = 0$ K.	100
7.6	Shows (a) electron density and (b) electron mobility of the graded NW ($x_1 = 0 \rightarrow x_2 = 0.8$) in open circuit with $\Delta T = 0$ K, 10 K, and 90 K. The graphs are plotted for the centre of NW's cross section.	101
7.7	Shows output power as a function of ΔT for gated ($\phi_m = 4.0$ eV) graded ($x_1 = 0 \rightarrow x_2 = 0.8$) structures connected to load resistor (R_L) in a closed circuit, compared to gated ($\phi_m = 4.0$ eV) un-graded ($x = 0.4$) structure.	102
7.8	S_{ave-x_d} for the gated ($\phi_m = 4$ eV) graded ($x_1 = 0.4 - x_d \rightarrow x_2 = 0.4 + x_d$) NWs in a closed circuit. S is studied for default values of parameters and setting one or more parameters to a constant (const) value. mob and EDoS stand for mobility and carrier effective density of states respectively. The NWs are connected to a load resistor, where $R_L = R$, in a closed circuit.	102
7.9	Shows (a) σ - ΔT for gated ($\phi_m = 4$ eV) graded ($x_1 = 0 \rightarrow x_2 = 0.8$) NW compared to gated ($\phi_m = 4$ eV) un-graded ($x = 0.4$). (b) σ - x_d for gated ($\phi_m = 4$ eV) graded ($x_1 = 0.4 - x_d \rightarrow x_2 = 0.4 + x_d$) NWs with $\Delta T = 90$ K. σ is studied for default values of parameters and setting one or more parameters to a constant (const) value. mob and EDoS stand for mobility and carrier effective density of states respectively. The NWs are connected to a load resistor, where $R_L = R$, in a closed circuit.	103
7.10	Shows (a) power factor and (b) output power of gated ($\phi_m = 4$ eV) graded ($x_1 = 0.4 - x_d \rightarrow x_2 = 0.4 + x_d$) NWs with $\Delta T = 90$ K and $R_L = R$	104
7.11	Shows the cross section of graded area of Si with reference to 12 nm diameter. d_{x_1} is the diameter of Si at T_{x_1} obtained by subtracting d_{dif} from d_{ref} ; and d_{x_2} is the diameter of Si at T_{x_2} due to adding d_{dif} to d_{ref}	104
7.12	Shows E_c at the (a) centre and (b) interface; electron density at the (c) centre and (d) interface; and $\ln\left(\frac{N_c}{n}\right)$ -X at the (e) centre and (f) interface of the gated ($\phi_m = 4.1$ eV) graded ($d_{x_1} = 11$ nm $\rightarrow$ $d_{x_2} = 13$ nm) NWs compared to the gated ($\phi_m = 4.1$ eV) un-graded ($d_{Si} = 12$ nm). The NWs are in open circuit.	106
7.13	Shows (a) S , (b) σ , (c) power factor, and (d) power of gated ($\phi_m = 4.1$ eV) graded ($d_{x_1} = 11$ nm and $d_{x_2} = 13$) Si compared to gated ($\phi_m = 4.1$ eV) un-graded ($d_{Si} = 12$ nm) Si. The NWs are connected to a load resistor with $R_L = R$	107

LIST OF FIGURES

7.14 Shows maximum power and power factor of gated ($\phi_m = 4.1$ eV) graded $(d_{ref} - d_{dif} \rightarrow d_{ref} + d_{dif})$ NWs at $\Delta T = 90$ K, as a function of d_{dif} . The NW are connected to a load resistor, having $R_L = R$	108
---	-----

INTRODUCTION

Downscaling of electronic devices introduced new challenges such as forming doping profiles with high accuracy and reproducibility [1]. The random distribution of doping atoms leads to large variations in device characteristics at the nano-scale. Doping electronic devices also degrades their mobility as a result of ionized impurity scattering [2]. Elimination of doping from the fabrication process can lead to improvement of mobility and continuation of Moore's law [3]. In this project, we propose and study new applications of un-doped nanowires, including gated intrinsic thermo-electric power generators (TEGs), gated intrinsic temperature sensors, and gated intrinsic reconfigurable nanowire transistors positioned in parallel, connected by an oxide bridge. Gated TEGs and temperature sensors are designed for power generation and heat management in electronic devices. Gated reconfigurable nanowire transistors are designed for higher symmetry in I-V characteristics for n- and p-FETs. The similarity of these devices are their un-doped metal/semiconductor/metal structure wrapped by oxide and metal. Metal/semiconductor interfaces can control the injection of charge carriers in the intrinsic semiconductor (channel), as a replacement to n^+ -doped/ p^+ -doped junctions in conventional FETs [4]. Since these devices are not doped, the gates can

control the charge carrier type and its concentration in the channel [1].

This thesis is organised as follows. Chapter 2, gives an overview of field effect transistors. Chapter 3, presents background of TEGs and temperature sensors. Chapter 4, gives an overview of tools used in Sentaurus Technology Computer Aided Design (TCAD) software. Chapter 5, shows the novel design and simulated reconfigurable nanowire transistor with bridged program gates. Chapter 6, studies the effect of gating intrinsic silicon nanowires for thermo-electric power generation and temperature sensing. Chapter 7, shows the effect of grading carrier concentration across the channel on thermo-electric power generation optimisation. Chapter 8, concludes the work.

This project is partly funded by the International consortium of nanotechnology (ICON). It is a requirement for ICON funding to collaborate on an international basis for this project. In this project, collaboration is with the University of Salamanca, Spain.

METAL OXIDE FIELD EFFECT TRANSISTOR (MOSFETs)

Transistors were initially used as electrical switches. Their purpose was solely allowing (switched ON) or blocking (switched OFF) the flow of carriers [5, 6]. A simple transistor has a source/channel/drain structure with a gate, which controls the flow of carriers in the channel. The gate is basically the key, which switches ON or switches OFF the flow [4, 6, 7]. Since the creation of transistors in 1947 [5], different designs and optimisations have been proposed to minimise the leakage and increase the switching performance [4, 7].

In this chapter, the different building blocks of field effect transistors (FETs) are explained in section 2.1. Down-scaling metal oxide field effect transistors (MOSFETs) to nano-FETs is discussed in section 2.2. Performance characteristics of FETs are shown in 2.3. The background and literature of Si reconfigurable nanowire field effect transistors (RNW-FETs) are presented in section 2.4. Deposition of interconnects and their purpose are explained in section 2.5. Finally, the summary of the chapter is shown in section 2.6.

2.1 Building blocks of FETs

To better understand the working principle of these devices, one has to understand the physics of p-n junctions, Schottky contacts, and contacts on insulators. In this section, the physics of building blocks is explained.

2.1.1 p-n junctions

P-n junctions are one of the building blocks in doped transistors [4]. A simple p-n junction is formed by having an n-type doped region in contact with a p-type doped region [4, 8, 9].

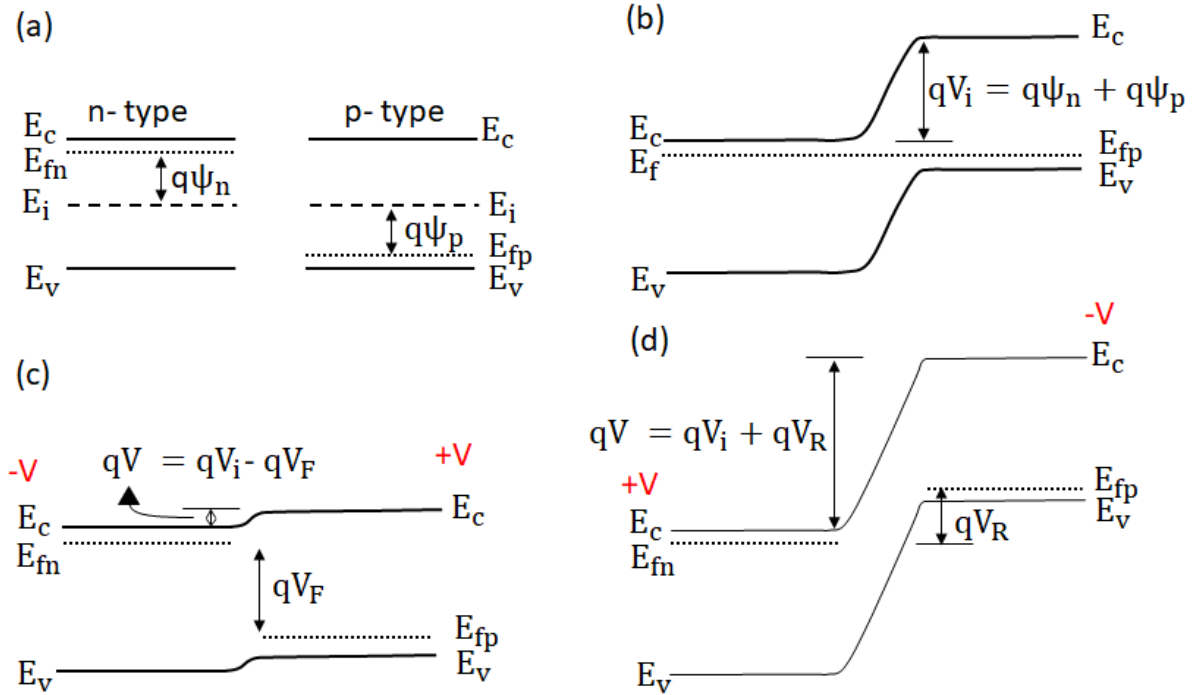


Figure 2.1: Uniformly doped n-type and p-type semiconductor (a) before, and (b) after contact. P-n junction at (c) forward (V_F), and (d) reverse (V_R) bias voltage. Where E_{fn} (E_{fp}) is quasi Fermi level of electrons (holes), E_i is intrinsic Fermi level, E_c is conduction band, and E_v is valence band; and $q\psi_n$ ($q\psi_p$) is the difference of E_i with E_{fn} (E_{fp}).

Fig 2.1 (a) and (b) show p-n junctions before and after contact at zero external applied voltage, respectively. The electron concentration is much larger in n-Si than p-Si; and vice versa, the hole concentration in p-Si is larger than in n-Si. After the contact, the

equilibrium state of p-n junction at zero bias is achieved by diffusion of electrons (holes) across the interface from n-type (p-type) to p-type (n-type) material. The initial diffusion of electrons and holes, to reach equilibrium, leads to formation of depletion regions and a potential barrier (qV_i) faced by carriers at zero bias [4, 8, 9].

The built-in potential (qV_i), barrier faced by carriers at zero external voltage, can be found using eq. 2.1:

$$qV_i = k_B T \ln\left(\frac{n}{n_i}\right) + k_B T \ln\left(\frac{p}{n_i}\right) \quad (2.1)$$

Where k_B is Boltzmann constant, T is temperature, $|q|$ is charge, n is electron density, n_i is intrinsic carrier concentration, and p is hole density.

The p-n junction is a diode, meaning that it allows current flow in only one direction. Applying forward bias (V_F), allows current flow by reducing the barrier faced by carriers (fig 2.1 (c)); while applying reverse bias, blocks the flow of carriers due to increasing the barrier height (fig 2.1 (d)) [4, 8, 9].

2.1.2 Schottky contacts

Schottky contacts are formed by putting a metal in contact with a semiconductor [4, 9]. Fig. 2.2 (a) and (b) shows contacting a metal with work function (ϕ_m) equal to an intrinsic semiconductor's work function (ϕ_s).

In the ideal case, the Schottky barrier height (ϕ_B) at the metal/i-semiconductor interface (ϕ_B) is fixed despite any change in carrier concentration and external applied voltage to metal [10], eq. 2.2:

$$\phi_B = \phi_m - \chi_s \quad (2.2)$$

Where χ_s is semiconductor's electron affinity.

In ideal case, contacting a metal with a semiconductor leads to a potential energy of $-q\xi x$ at the semiconductor and a fixed ϕ_B faced by electrons in the metal (fig. 2.3 (c)), where ξ is electric field due to band bending and x is distance. In reality, any

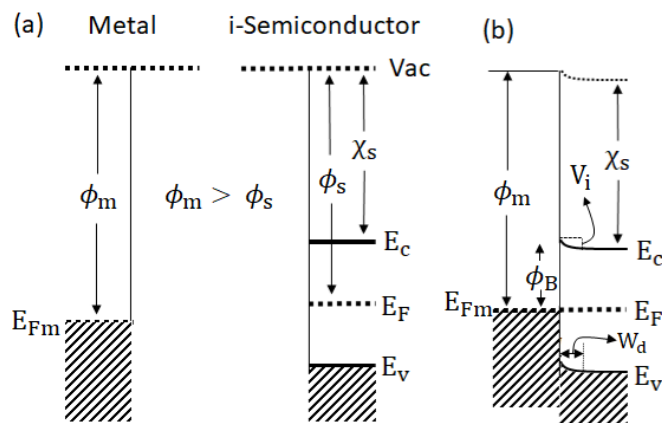


Figure 2.2: Ideal metal/i-semiconductor with $\phi_m > \phi_s$ (a) before contact, and (b) after contact with depletion width W_d at zero external voltage.

change in external voltage (V_{ext}) applied to metal leads to barrier lowering ($\Delta\phi_B$). To better understand the effect of image barrier lowering, one has to compare the electric field dispersion of a charge near the metal/semiconductor interface before (fig. 2.3 (a)) and after (fig. 2.3 (b)) the metal gets in contact with the semiconductor. Prior to metal contact, the electric field ($\xi \propto \frac{1}{x}$) of a single charge disperse uniformly and its magnitude reduce linearly as a function of distance (x). When the metal is in contact with the semiconductor, an opposite charge with similar distance to the interface, compared to the one in semiconductor, is assumed. As a consequence of the opposite charge in the metal, the electric field direction of the charge in the semiconductors bends and its magnitude changes. The Coulomb force between the two charges results in the formation of an image potential energy, reducing the potential energy formed by $-q\xi x$ in the ideal case (fig 2.3 (c)). Theoretically, $\Delta\phi_B$ can be calculated as [4, 10]:

$$\Delta\phi_B = \left[\frac{q^3 n}{8\pi^2 \epsilon_s^3} (V_i - V_{ext}) \right]^{1/4} = \sqrt{\frac{q \xi_m}{4\pi \epsilon_s}} \quad (2.3)$$

Where,

$$\xi_m = \sqrt{\frac{2qn(V_i - V_{ext})}{\epsilon_s}} \quad (2.4)$$

Where ϵ_s is static permittivity, ξ_m is maximum value of electric field, and V_{ext} is the

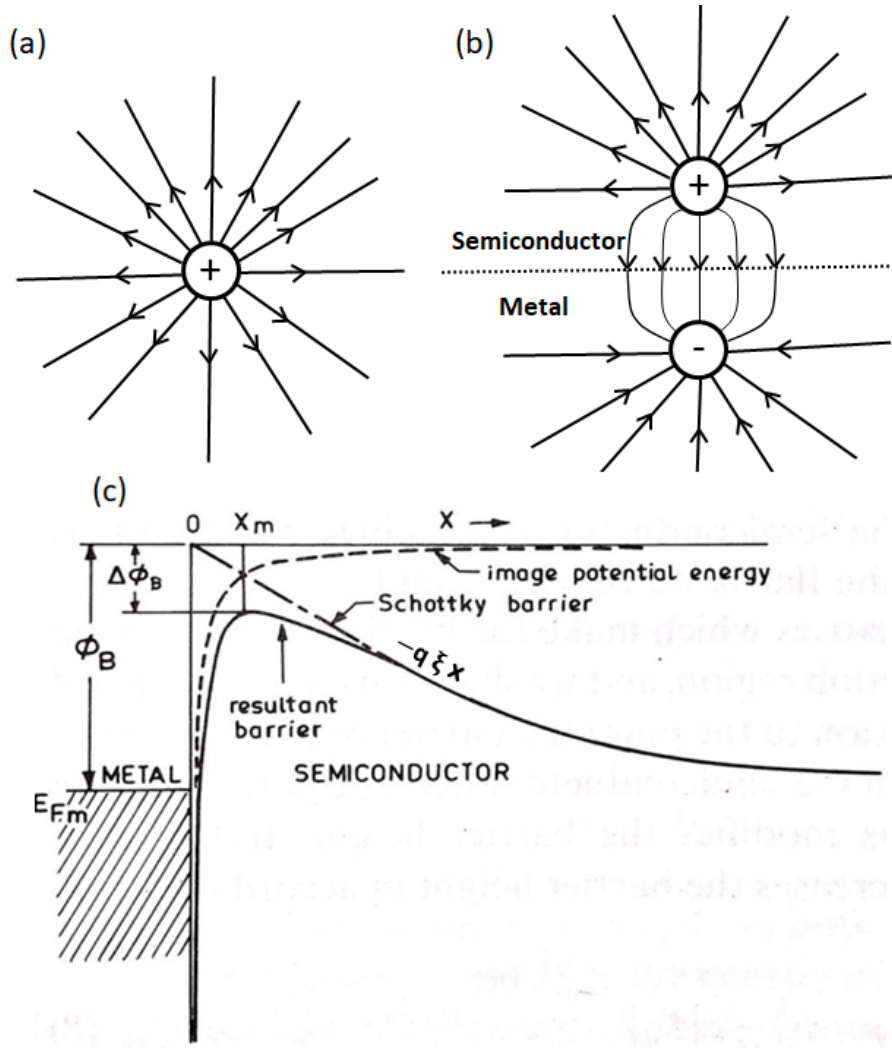


Figure 2.3: Shows electric field dispersion of a charge in a semiconductor (a) before, and (b) after contact with metal. (c) Schottky barrier lowering due to introduction of image potential energy [10]. x_m is x at maximum barrier height, $\Delta\phi_B$ is barrier lowering .

external voltage applied to metal. Therefore, the final barrier (ϕ_{Bf}) as the result of barrier lowering ($\Delta\phi_B$) is calculated as [11]:

$$\phi_{Bf} = \phi_B - \Delta\phi_B \quad (2.5)$$

2.1.3 Metal/oxide/semiconductor (MOS) interfaces

Metal gates control the injection of carriers into the channel from the source. Fig 2.4 shows the response of a metal/ SiO_2 /i-Si (MOS) to gate voltage (V_{gate}) with $\phi_m = \phi_s$. Generally, applying a positive voltage ($V_{gate} > 0$) to the metal with respect to the underlying intrinsic silicon (p-type doped), accumulates electrons at the Si/ SiO_2 interface (inverts the interface to n-type Si). Whereas, applying negative voltage ($V_{gate} < 0$) to the contact with respect to underlying intrinsic silicon (n-doped Si), attracts holes at the Si/ SiO_2 interface (inverts the Si to p-type) [4, 11, 12].

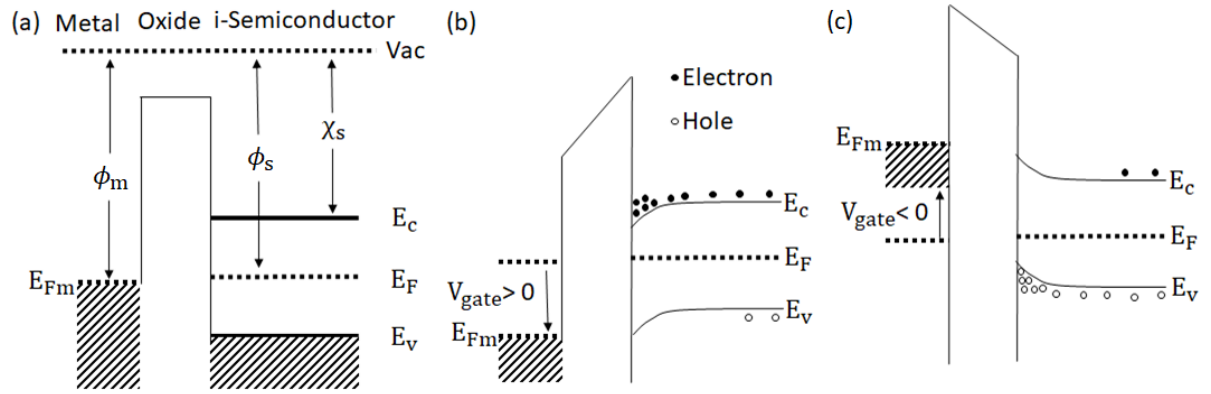


Figure 2.4: Metal/oxide/i-semiconductor with $\phi_m = \phi_s$ at (a) $V_{gate} = 0$ V, (b) $V_{gate} > 0$ V (accumulation of electrons), and (c) $V_{gate} < 0$ V (accumulation of holes).

2.1.4 Tunable Schottky barriers to control current flow across an intrinsic channel

The gates on top of an intrinsic channel with Schottky contacts can either program the type of the carriers (program gate (PG)) or control the magnitude of the injected carriers (control gate (CG)), fig. 2.5 (a). The gates above the metal/semiconductor interface can tune ϕ_B and depletion width (W_d) of the formed Schottky barriers, and thereby control the injection of carriers to the channel [1]. There are three types of carrier injection (fig. 2.5 (b) to (d)), (i) thermionic emission over the barrier, (ii) thermionic-field emission

through the upper part of the barrier (TFE), and (iii) field emission through the barrier at the fermi level (FE). Carriers can be injected or blocked depending on their energy [10].

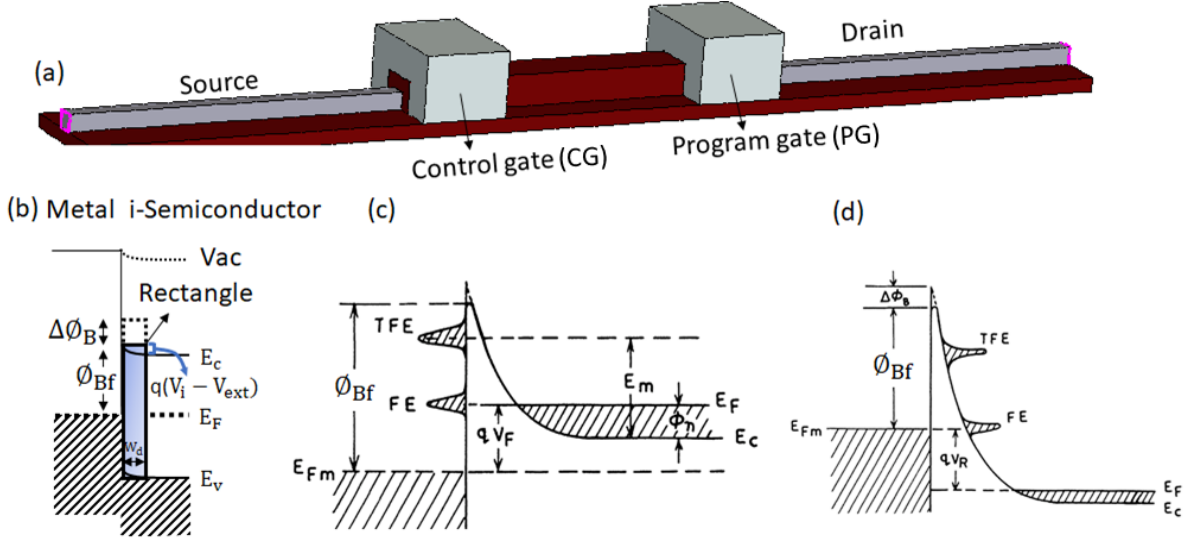


Figure 2.5: (a) Shows a double gated RNW-FET with Schottky contacts at source and drain; and a control gate and a program gate. (b) Barriers faced by carriers in metal and semiconductor. Thermionic field emission (TFE) and field emission (FE) in (c) forward [13], and (d) reverse bias [13].

The barrier faced by carriers at forward and reverse bias is different. The carriers in the metal see a wall with ϕ_{Bf} (fig 2.5 (b)), whereas, electrons in the semiconductor have to overcome the electrostatic potential ($q\psi$) with $q\psi = q(V_i - V_{ext})$ height. The actual shape of the barriers in both biases are immaterial in the calculation of thermionic emission current. In other words, for the sole calculation of thermionic emission current, the Schottky barrier can be drawn as an impenetrable rectangular (blue rectangle in fig 2.5 (b)). Carriers in metal and semiconductor with energy greater than $E_{Fm} + q\phi_B$ and ($q\psi = q(V_i - V_{ext})$) can cross the assumed rectangular shaped barrier respectively. The height of these barriers faced by carriers at either side can be tuned by the applied voltages to Schottky contacts (V_{ext}) and gate (V_{gate}). Current density (J_{th}) of carries from the semiconductor to metal ($s \rightarrow m$) and metal to semiconductor ($m \rightarrow s$) are calculated

as shown below [4, 10, 14]:

$$J_{th(s \rightarrow m)} = A^* T^2 \exp \left[-\frac{q\phi_{Bf}}{k_B T} \right] \exp \left[\frac{qV_{ext}}{k_B T} \right] \quad (2.6)$$

and

$$J_{th(m \rightarrow s)} = A^* T^2 \exp \left[-\frac{q\phi_{Bf}}{k_B T} \right] \quad (2.7)$$

where

$$A^* = \frac{4\pi q m^* k_B^2}{h^3} \quad (2.8)$$

Unlike thermionic emission current calculation, where the barrier is assumed to be an un-penetrable wall, current due to quantum mechanical tunneling is achieved solely through penetration of carriers through the barrier. Similar to thermionic emission where a certain condition is required so that the crossing of carriers over the wall can take place, requirements for quantum tunnelling must be met. In an intrinsic gated semiconductor, the carrier concentration as the result of gate voltage bias must increase to thin the depletion region (W_d), to increase tunneling probability. At low temperature, field emission (FE) takes place for carriers with similar energies to the Fermi level at the other side (fig 2.5 (c) and (d)). At high temperatures, carriers can tunnel through the upper part of the barrier (fig 2.5 (c) and (d)) and leads to thermionic field emission (TFE). The tunneling current (J_t) can be calculated using the following formula [13–15]:

$$J_t = A^* T^2 \exp \left[-\frac{q\phi_{Bf}}{k_B T} \right] \exp \left[\frac{qV_{ext}}{E_0} \right] \quad (2.9)$$

where

$$E_0 = E_{00} \coth \left(\frac{E_{00}}{k_B T} \right) \quad (2.10)$$

and

$$E_{00} = \frac{qh}{4\pi} \left(\frac{n}{m^* \epsilon_s} \right)^{1/2} \quad (2.11)$$

The ratio $\frac{k_B T}{E_{00}}$ indicates the relative importance of tunneling and thermionic emission, where E_{00} is the energy as a function of effective mass (m^*) and carrier concentration

(n). At low temperatures, $E_0 = E_{00}$, showing that field emission is dominant. At high temperatures, $E_0 = k_B T$, meaning that thermionic emission is dominant [13]. At $E_0 = k_B T$, eq. 2.9 becomes similar to eq. 2.6.

2.2 From MOSFETs to NanoFETs

The concept of metal oxide field effect transistor (MOSFET) was first introduced as early as 1930s. However, low quality Si/SiO₂ postponed fabrication of MOS based transistors for about twenty years. In 1960, the first MOSFET with thermally grown oxide (SiO₂) for MOS structure was reported [4]. Fig 2.6 shows a simple 3D view of an n-type MOSFET (NMOS) structure with width W . NMOS (PMOS) is fabricated by forming two heavily n-type (p-type) regions on a p-type (n-type) substrate. The heavily doped regions form the source and drain of the MOSFET. The MOS structure is formed between source and drain, with oxide thickness t_{ox} . The aimed channel length to be fabricated (L_{drawn}) is always different from the actual channel length (L_{eff}) after fabrication. The difference (L_D) of planned L_{drawn} and obtained L_{eff} in fabricated MOSFET is due to unwanted and unavoidable diffusion of dopants in all directions during fabrication. Although these heavily doped regions are symmetric, one is called source and the other is named drain. In the ON state of transistor, source is responsible for providing carriers to be injected

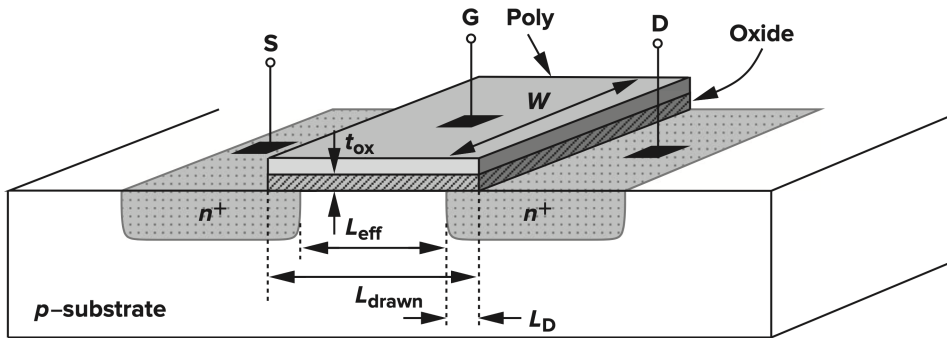


Figure 2.6: 3D view of a simple n-type MOSFET structure [6].

into the channel; and the drain is responsible for collecting of the carriers from the channel [6].

MOSFETs are one of the popular choices to be used for microprocessors and semiconductor memories. The performance of these devices were found to increase by higher number of transistors in a unit area [4]. A road-map predicting the expected reduction of gate length (L_G) until 2020 was shown in [7], published in 2016. In early 2000, shrinking the gate length to $0.1 \mu\text{m}$ led to placement of more than a billion transistor per chip (fig. 2.7) [4, 7]. Although approximately linear relation for L_G -year (Moore's law) was experienced until 2007, the expected L_G reduction rate was predicted to slow down starting from 2007. This prediction is due to increase of cost caused by rise of fabrication challenges [4]; and increase of drain influence on tuning the source/channel barrier height as channel length reduces [7]. In long channel MOSFETs, the barrier, especially at source/channel interface, is mainly defined by transverse electric field ($E_{\perp}$) generated by the MOS structure. However, as channel length reduces, the influence of drain voltage and thus longitudinal electric field ($E_{\parallel}$) on electrostatic potential across the channel increases, such that $E_{\parallel}$ can result in barrier lowering at source/channel even at $V_{gate} = 0$. This phenomena is called drain induced barrier lowering (DIBL) [4].

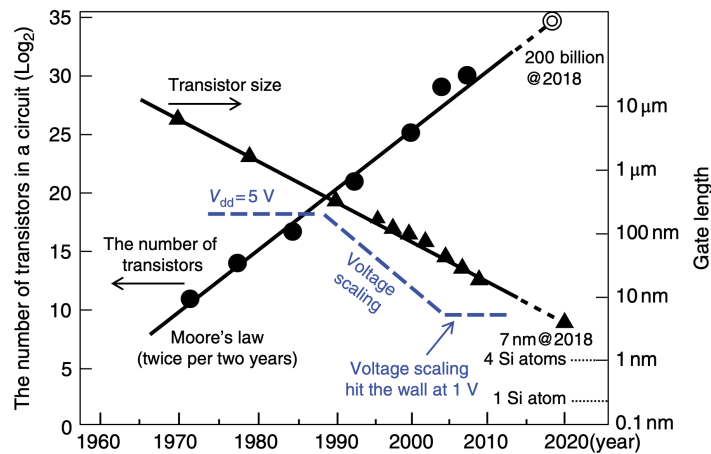


Figure 2.7: Gate length and number of transistors on chip starting from 1965 [7].

DIBL results in leakage of carriers from source to drain in the OFF state ($V_{gate} = 0$ V), leading to increase of the OFF current (I_{off}). Since waste of power consumption is $P_w = I_{off}V_{dd}$ with V_{dd} the supply voltage, an increase of I_{off} leads to reduction of battery life in electronic devices and increase of heat dissipation. Minimisation of P_w in short channel FETs is possible by introducing designs offering more gate control on the channel than conventional MOSFETs with a single planar gate and a bulk substrate (fig. 2.6). Higher control is achieved by thinning the planar channel positioned on an insulator (ultra-thin FET), controlling the channel by multiple gates positioned on top and back, covering the channel (finFET), or wrapping the channel with metal gate (gate-all-around FET) [7], fig. 2.8.

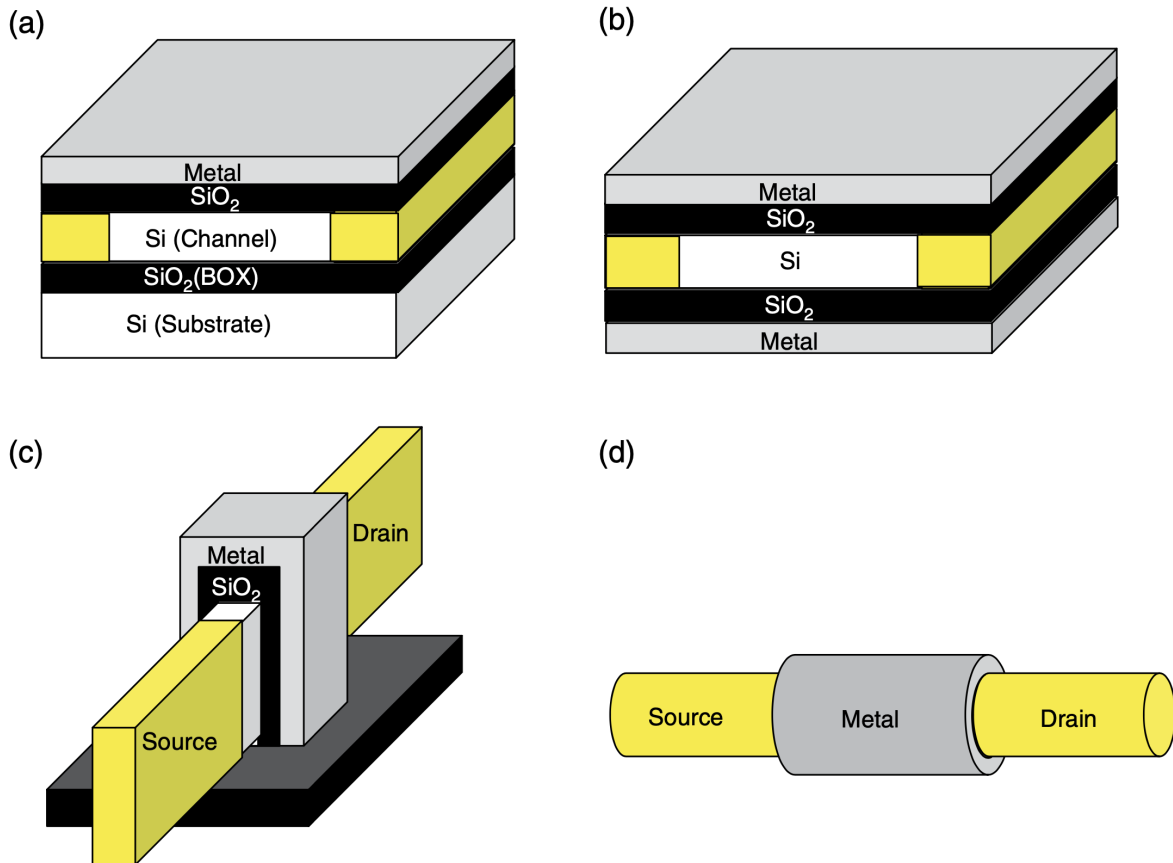


Figure 2.8: Shows (a) gated FET with ultra-thin body, (b) top and back gated FET, (c) finFET, and (d) gate-all-around FET (GAA-FET) [7].

Similar to conventional MOSFETs, barriers at source/channel (channel/drain) are formed by the p-n junction concept to form the core structure, source/channel/drain [7, 16–18]. Ultra-thin FETs and finFETs controlled by double and triple gates were reported to reduce DIBL [17, 19, 20]; as increasing number of gates shield and suppresses the effect of the drain voltage at the source [17, 19–21]. Although DIBL can be reduced by novel device architects and using multiple gates, further down-scaling of these FETs magnifies the challenge of DIBL. Intrinsic gated Si reconfigurable nanowire transistor (Si RNW-FET) with Schottky barriers is a potential candidate to resolve the bottleneck [1]. Prior to introducing intrinsic Si RNW-FETs, one has to understand the performance parameters of FETs.

2.3 Performance evaluation of FETs

Transistors can operate in non-saturation (triode region) or saturation region [4, 22], fig. 2.9. The performance parameters of a FETs to be used in ICs can be evaluated by their threshold voltage (V_{th}), sub-threshold swing (SS), and ON and OFF current ratio ($\frac{I_{on}}{I_{off}}$) in saturation region.

The required gate voltage to switch the transistor ON is called the threshold voltage

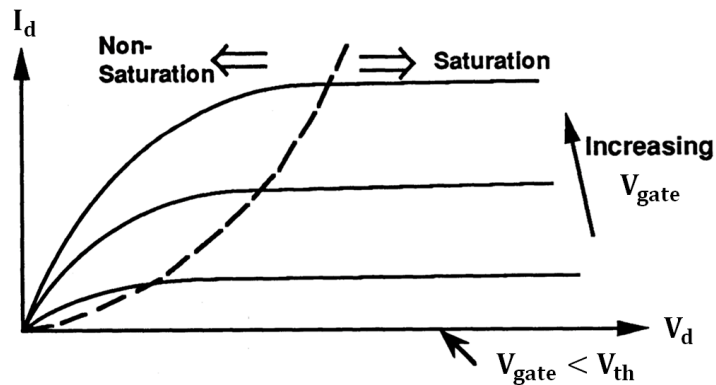
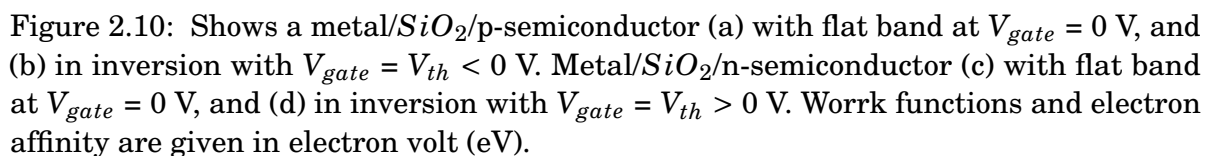


Figure 2.9: Shows I_d - V_d characteristic of an ideal MOSFET. The saturation current increases as V_{gate} increases [22].



15

show full inversion ($2\phi_f$) of n- and p-type semiconductors respectively, where ϕ_f is the difference of intrinsic Fermi energy (E_i) with quasi Fermi level of majority carriers. This means that the carrier concentration density at interface is equal, but opposite type with the one in the bulk. In doped FETs, V_{th} is the required gate voltage to fully invert carrier type and density at the semiconductor/ SiO_2 interface. Inversion of the channel, enables the flow of carriers from source to drain [6]. V_{th} can be calculated using eq. 2.12 [4, 6]:

$$V_{th} = \phi_{ms} + 2\phi_f + \frac{Q_{dep}}{C_{ox}} \quad (2.12)$$

Where [6, 22],

$$\phi_f = \frac{k_B T}{q} \ln \left(\frac{N_{sub}}{n_i} \right) \quad (2.13)$$

And [6],

$$Q_{dep} = \sqrt{4q\epsilon_{semi}|\phi_f|N_{sub}} \quad (2.14)$$

Where C_{ox} is gate oxide capacitance, N_{sub} is doping concentration in substrate, Q_{dep} is depletion region charge, ϕ_{ms} is the difference of metal gate work function with semiconductor work function, and ϵ_{semi} is the dielectric constant of semiconductors.

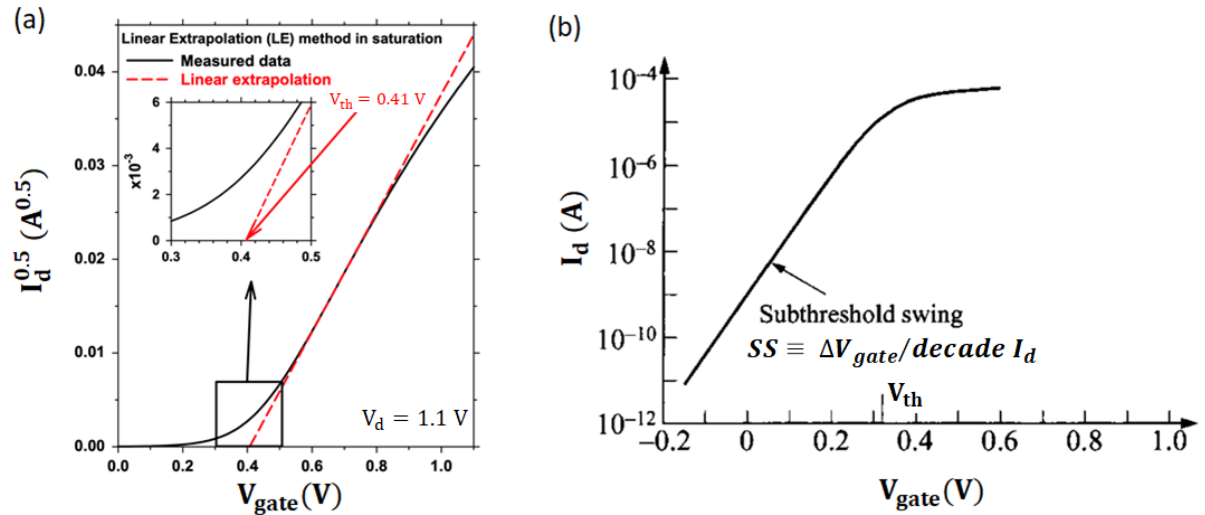


Figure 2.11: For an NMOS (a) $\sqrt{I_d}$ - V_{gate} graph for extracting V_{th} in saturation region [23], and (b) I_d - V_{gate} graph for SS extraction [4].

In ideal transistors, the drain current (I_d) is zero at $V_{gate} < V_{th}$ ($V_{gate} > V_{th}$) for NMOS (PMOS); and current can flow only at $V_{gate} > V_{th}$ ($V_{gate} < V_{th}$) for NMOS (PMOS) [22]. In reality, sub-threshold current exist in weak inversion in the sub-threshold region, $V_{gate} < V_{th}$ for NMOS and $V_{th} < V_{gate}$ for PMOS. In weak inversion, the drift current is low; and the drain current is mainly diffusion current due to carrier gradients across the channel. The sub-threshold region tells how sharp current drops with respect to reducing (increasing) V_{gate} below (above) V_{th} for NMOS (PMOS); and sub-threshold swing (SS) defines how sharply a transistor turns OFF with respect to V_{gate} [4]. The lowest possible SS is $60 \frac{mV}{dec}$ [24]. SS can be found using eq. 2.15 [25]:

$$SS = \frac{\partial V_{gate}}{\partial \log(I_d)} \quad (2.15)$$

Fig 2.11 shows methods of extracting V_{th} (fig 2.11 (a)) and SS (fig 2.11 (b)) from I_d - V_{gate} graph of an NMOS .

The ON (I_{on}) and OFF (I_{off}) currents can be extracted from I_d - V_{gate} graphs. (I_{on}) is I_d at $V_d = V_{gate}$, where V_d is drain voltage; and I_{off} is I_d at $V_{gate} = 0$ [26].

2.4 Intrinsic gated Si RNW-FETs

Intrinsic gated Si reconfigurable nanowire FETs (Si RNW-FETs) were introduced by Weber et al. in 2008. These transistors eliminate the doping requirement and enables reconfiguring the FET between n- and p-FETs. Generally, transistors that are reversible, can be supplied via a single power supply, have symmetric I-V characteristics for their n- and p-FET, and are scalable have high potential to be used in ICs [1]. Previously, performance of a single gate (SG) [27], double gate (DG) [27, 28], and triple gated (TG) intrinsic Si RNW-FETs have been studied [29]. SG RNW-FET have received the least attention among all types of Si RNW-FETs. This type of RNW-FETs have a gate at the top of source/channel to control both the injection and polarity of the carriers. Since a

single gate is used for both purposes, the performance of the transistor is highly sensitive to the length of the gate [27].

DG Si RNW-FETs (fig. 2.12 (b)) have a control gate (CG) and a program gate (PG) above the source/channel and channel/drain interface, respectively. Program gate controls the type of the majority carriers (electrons or holes), and control gate tunes the injection magnitude of majority carriers into the channel [1, 30]. The concept of TG RNW-FETs (fig. 2.12 (a)) are similar to DG RNW-FETs. However, an extra gate has been positioned in the centre to gain higher control on carriers in the channel. In this design, the flow of carriers is controlled at the centre via CG, and the type of carriers are defined at the Schottky contacts by the PGs [1, 30].

The approach to switch to ON and OFF state for n- and p-configuration is similar for both DG (fig 2.12 (b)) and TG (fig 2.12 (a)) Si RNW-FETs. Setting $V_{PG} > 0$ ($V_{PG} < 0$) configures the channel to n-FET (p-FET), where V_{PG} is the program gate voltage. At $V_{PG} = V_{CG} = V_d > 0$ ($V_{PG} = V_{CG} = V_d < 0$), electrons (holes) are free to cross the channel and therefore n-FET (p-FET) is ON, where V_{CG} and V_d are control and drain voltages respectively. At $V_{PG} = V_d > 0$ and $V_{CG} \leq 0$ ($V_{PG} = V_d < 0$ and $V_{CG} \geq 0$), electrons (holes) are blocked and therefore n-FET (p-FET) is OFF [1, 30].

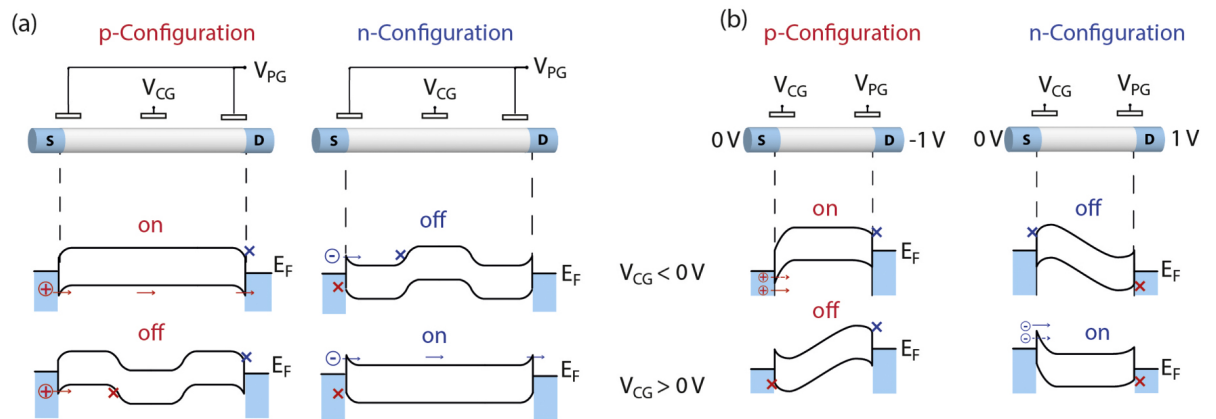


Figure 2.12: Shows ON and OFF state of p- and n- configuration for (a) TG Si RNW-FET, and (b) DG Si RNW-FET with mid-band gap metals [30]

Precise alignment of the mid-gap of silicon with contacts provide equal barriers (≈ 0.56 eV) for electrons (ϕ_B) and holes (ϕ_{Bh}) for tunneling, and minimises the leakage current in OFF state [1, 30]. The silicon crystallographic orientation plays a key role in I-V characteristic of n-FET and p-FET. Crystallographic orientation manipulates the Schottky barrier height, mobility, and effective mass of electrons and holes [1, 31].

Generally, the difference in mobility of electrons and holes lead to asymmetric I-V characteristic. To form approximately symmetric n- and p-configuration, the channel of the Si RNW-FET can be compressively strained by thermal oxidation at certain temperature and $\langle 110 \rangle$ crystal orientation [32]. The metal gate work function on top of the channel is chosen such, that the carrier concentration of the channel remains intrinsic at no bias voltage [1]. The core structure of these transistors are mainly formed by annealing nickel to the sides of an intrinsic silicon with certain crystallographic orientation, aiming to align the Fermi level of contacts (E_{Fm}) with mid gap of silicon ($\frac{E_g}{2}$) [28, 29, 32–39]. Some previous efforts on optimisation of Si RNW-FETs to achieve symmetric barriers and sub-threshold (SS) swings for electrons (ϕ_B , SS_n) and holes (ϕ_{Bh} , SS_h) are summarised in table 2.1.

Table 2.1: Previous works on Si RNW-FETs, where NCh, exp, and sim stands for number of channels, experiment, and simulation respectively.

Ref/work	Contact	ϕ_B/ϕ_{Bh} (eV)	d_{Si} (nm)	L_{Si} (nm)	NCh	V_{PG_n}/V_{PG_p} (V)	$ V_{d_{n,p}} $ (V)	SS_n/SS_p ($\frac{mV}{dec}$)
[28]/exp	NiSi ₂	0.66/0.46	15 to 27	680	1	3/-3	1	220/90
[32]/exp	NiSi ₂	not known	12	220	1	2/-2	2	150/150
[27]/(sim)	NiSi ₂	0.58/0.54	12 nm	220	1	2/-2	2	not known
[33]/exp	NiSi	0.67/0.45	$d_{Si} < 20$ nm	350	4	4/-4	2	70/64
[34]/exp	NiSi	0.67/0.45	not known	1000	1	3/-3	0.5	343/428
[29]/exp	NiSi	0.73/0.39	30	350	4	3/0	2	217/155

Although symmetric I-V can be achieved using compressive strain engineering [32], this method is limited to $\langle 110 \rangle$ crystal orientation, insulating material (SiO_2 for Si), and thermal oxidation temperature. Therefore, other strategies with more flexible fabrication steps must be introduced. In chapter 5, a novel approaches to achieve this is presented.

2.5 Deposition of interconnect layers

After fabrication of FETs, metal layers are required to connect the fabricated transistors with other units on the IC [40]. This process starts by covering the FETs with a pre-metal dielectric (PMD) and contact plugs [41]. Typical materials used/studied as PMD layer are SiO_2 [41], boron-phosphor-silicate-glass (BPSG) [42, 43], tetraethyl-ortho-silicate (TEOS), oxynitride, nitride [44], phosphosilicate glass (PSG) [43], hydrogen-silsesquioxane (HSQ), and methyl-silsesquioxane (MSQ) [45]. The interconnect structures, also called back end of the line (BEOL), are formed on top of the PMD layer [40], fig 2.13.

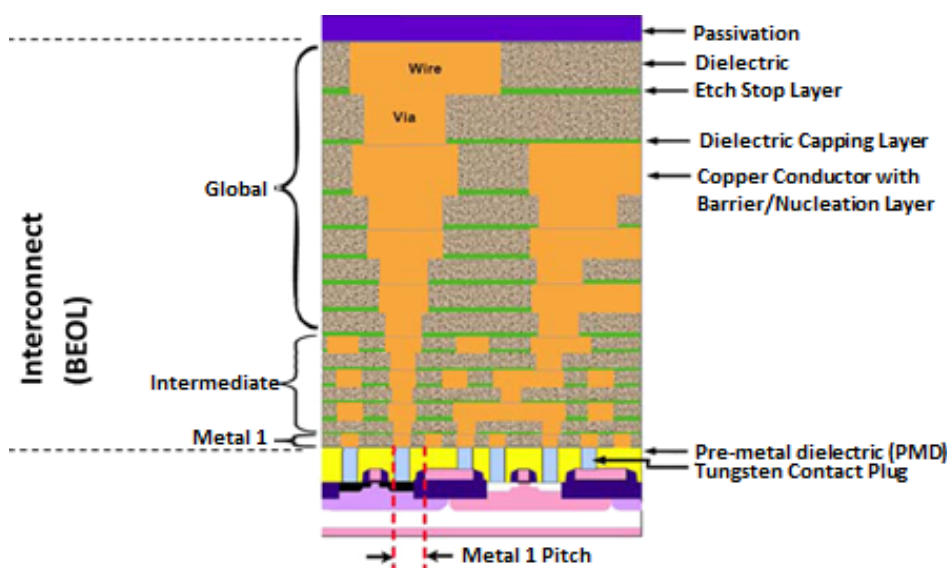


Figure 2.13: Shows the interconnect layers on top of the pre-metal dielectric layer and tungsten contact plug, to connect the fabricated NMOS and PMOS to other parts on the IC [40].

Conventionally, SiO_2 and aluminum were used as dielectric and metal for the interconnect layers, respectively. However, with device down-scaling, metals and dielectrics with lower resistance and dielectric constants, respectively, are used to reduce RC-delays [46]. According to the International Technology Roadmap for Semiconductors, further down-scaling of devices require using ultra-low- k dielectrics (≈ 1.5) for interconnect

stacks [47, 48], where k is dielectric constant of the insulator. For 90 nm technology, aluminum was replaced by Cu [40], as Cu has 36 % less resistivity than Al [46]; and SiO_2 ($k = 4.1$) by SiCOH ($k = 3$), in 2004 [40, 49]. Introduction of porosity (air pockets) to SiCOH reduced its k to 2.4 [48]. On 2019, Hong et al [48] has suggested usage of low- k amorphous boron nitride (a-BN) as the dielectric for interconnects. He has found that a-BN ($k = 1.16$ & 1.78) is electrically and mechanically stable; and can be grown on SiO_2 , Si, and Cu via low temperature (200 K-400 K) inductively coupled plasma chemical vapour deposition [48].

2.6 Summary

Classical MOSFETs rely on ohmic contacts for source and drain. For nano-FET, this requires doping implantation in nanostructures. As FETs down-scale, achieving uniform doping profile across all units are challenging. In addition, the diffusion-based carrier injection process limits the reduction of sub-threshold swing to minimum of $60 \frac{mV}{dec}$.

The reconfigurable nanowire FET (RNW-FET) resolves these problems as it is based on intrinsic material and the carrier injection process is controlled by tunneling through Schottky contacts. The added advantage of RNW-FET is the ability to be reconfigured between n- and p-FET.

THERMO-ELECTRIC POWER GENERATION AND TEMPERATURE SENSING

Agressive down-scaling of silicon field effect transistors (FETs) has led to fabrication of novel FETs, such as Nano-Sheet FETs (NS-FETs) [50–52], and gate-all-around (GAA) FETs [53–56]. However, low thermal conductivity of GAA-FETs and NS-FETs have led to generation and preservation of hot spots with $T \leq 353\text{K}$ leading to degradation in their performance [57]. Simultaneously, thermo-electric characteristics of silicon have improved due to nano-structuration [58–61]. This seemingly conflicting behaviour introduces an opportunity for thermo-electric power generation and temperature sensing within integrated circuits based on nano-sheet or nanowire devices [57, 62, 63].

In thermo-electric materials (TEMs), the Seebeck effect is used for temperature sensing [64–66] and thermo-electric power generation [67]. Figure of merit (ZT) is used to evaluate the performance of TEMs by correlating their thermal and electrical properties [68, 69], eq. 3.1:

$$ZT = \frac{\sigma S^2 T}{\kappa_e + \kappa_L} \quad (3.1)$$

Where σ is electrical conductivity of carriers, S is the Seebeck coefficient, κ_e is the thermal conductivity of electrons, κ_L is lattice thermal conductivity, and T is temperature.

At least $ZT = 2$ is required for practical usage of a thermo-electric power generators in industry [60, 70]. This can be done by either increasing the power factor (σS^2) or decreasing κ of nanostructured TEMs [60, 70, 71]. The most widely used TEM in industry is bulk Be_2Te_3 with $ZT \approx 1$. However, further improvement of ZT for Be_2Te_3 is difficult and expensive. Therefore, one has to improve ZT of an alternative material with cheaper fabrication cost, like Si [67]. In bulk Si, the coupling of σS^2 with κ , Wiedemann-Franz law, limits ZT to 0.01 [59, 72, 73]. However, partial de-coupling of σS^2 from κ by shrinking bulk materials to the nano-scale resolves this bottleneck. Phonon confinements and increase of boundary scattering in 2D sheets and nanowires reduce κ significantly, while σS^2 remains relatively un-changed [58–60]. Conventionally, tuning the carrier concentration of nano-structures via doping would optimise σS^2 , while κ remained partially un-changed [74]. However, the increased impurity scattering due to doping will result in significant mobility degradation [75, 76]. Significant improvement in mobility and σS^2 have been reported by introducing new strategies to modulate carriers without doping requirement [76–85]

This chapter is organised as follows. Section 3.1, explains the theories of thermo-electric power generation. Section 3.2, introduces previous approaches for optimisation of thermo-electric power generation. Section 3.3, gives an overview of on chip temperature sensing. Section 3.4, summarises the chapter.

3.1 Theory of thermo-electric power generation

TEMs have the ability to convert temperature differences (ΔT) into voltage differences (ΔV). A traditional thermoelectric power generator (TEG) is obtained by connecting multiple p- and n-type TEMs in series electrically, and thermally in parallel. A load

allows extraction of currents. The current (I) can be found as shown in eq. 3.2 [72, 86]:

$$I = \frac{\Delta V}{R_L + R} \quad (3.2)$$

Where R and R_L are the resistance of the TEG and load, respectively. Fig 3.1 (a) gives a simple TEG based on one n- and one p-type leg. Electron and hole flux are from hot to cold, thus electron and hole currents sum in this configuration. Fig. 3.2 (b) shows the schematic and circuit of a "single legged" TEG. In this work, rather than using p- and n-legs in series, a parallel connection of n-legs only is considered.

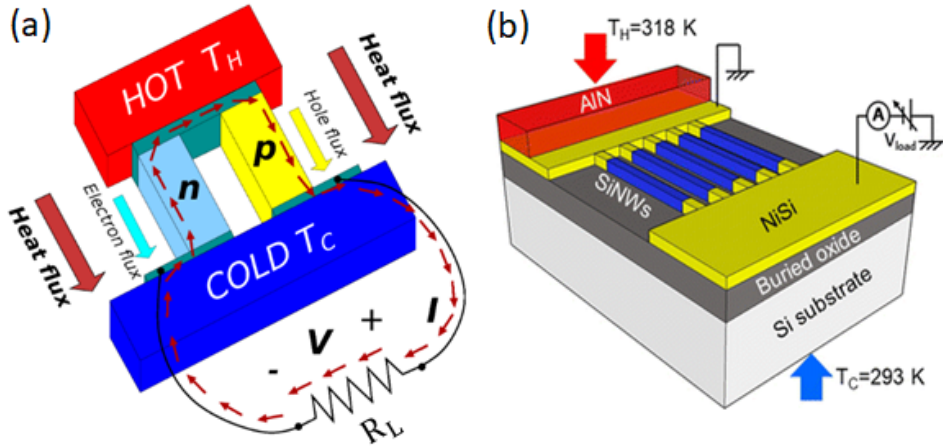


Figure 3.1: Schematic of (a) a two legged TEG containing a series connection of an n-type and p-type legs sandwiched between a hot (T_h) and cold (T_c) plate [87]; and (b) a single legged TEG with arrays of parallel connected n-type Si-NWs in between hot source and cold sink [88].

The ZT for the structure in fig. 3.1 (a) is:

$$ZT = \frac{(S_p - S_n)^2 T}{\sqrt{\kappa_p \rho_p} + \sqrt{\kappa_n \rho_n}} \quad (3.3)$$

Where S_n (S_p), κ_n (κ_p), and ρ_n (ρ_p) are Seebeck coefficients, total thermal conductivity, and resistivity of n-(p-type) leg, respectively. While that of fig 3.1 (b) is given by eq. 3.1.

3.1.1 Seebeck coefficient and voltage difference

Seebeck coefficient (S) expresses the ability of materials to convert a temperature difference (ΔT) into a voltage difference (ΔV) [72, 86]. Total Seebeck coefficient (S) for a two legged TEG can be calculated using eq. 3.4 [87].

$$S = S_p - S_n = \frac{\Delta V}{\Delta T} \quad (3.4)$$

In case of a single n-type (p-type) legged TEG, $S = S_n$ ($S = S_p$). S_n (S_p) in non-degenerate semiconductors are highly dependant on the difference between E_{Fn} (E_{Fp}) and conduction (valence) band for n-type (p-type) material, carrier-phonon scattering, and ionised impurity scattering. The analytical expressions for S_n and S_p are shown in eq. 3.5 and eq. 3.6 [89].

$$S_n = -\frac{k_B}{q} \left[\frac{5}{2} + s - \left(\frac{E_c - E_{Fn}}{k_B T} \right) \right] = -\frac{k_B}{q} \left[\frac{5}{2} + s + \ln \left(\frac{N_c}{n} \right) \right] \quad (3.5)$$

and

$$S_p = \frac{k_B}{q} \left[\frac{5}{2} + s - \left(\frac{E_v - E_{Fp}}{k_B T} \right) \right] = \frac{k_B}{q} \left[\frac{5}{2} + s - \ln \left(\frac{N_v}{p} \right) \right] \quad (3.6)$$

Where N_c (N_v) is the effective density of states for electrons (holes) and s is the scattering mechanism parameter.

3.1.2 Figure of merit

As explained earlier, ZT evaluates the performance of the TEMs by correlating the electrical and thermal parameters. For high ZT, the power factor (σS^2) must be high while κ must remain low [77–81]. In this sub-section, the impact of each parameter on TEGs is explained.

As seen in eq. 3.4, S is vital for calculating ΔV . While, electrical conductivity (σ_c) is a key parameter for both current (I_c) and resistance of channel (R_{ch}), with $c = n$ or p . For a simulated single legged TEG with 2D metal contacts (without thickness), $R = R_{ch}$. The electrical conductivity (σ_c) for electrons (σ_n) and holes (σ_p) can be found using eq. 3.7

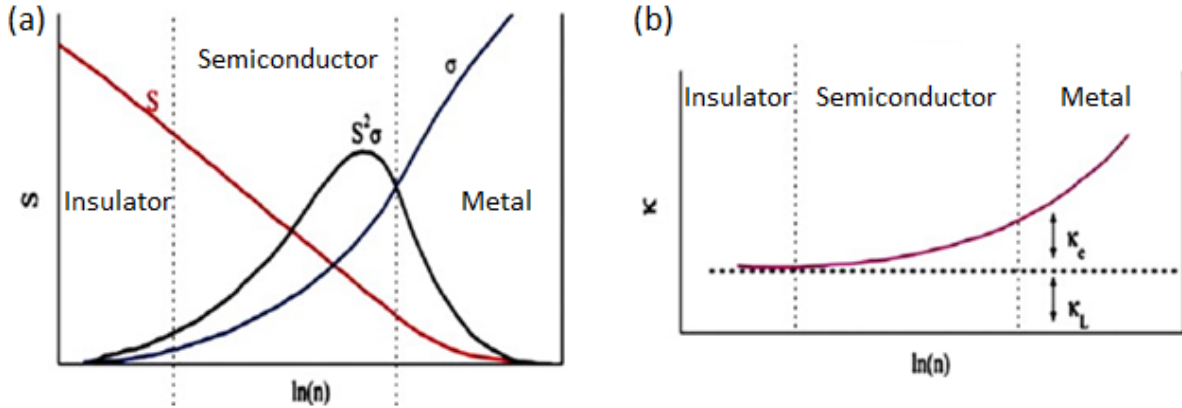


Figure 3.2: (a) The Seebeck coefficient (S), electrical conductivity (σ), σS^2 , and (b) total thermal conductivity (κ), lattice thermal conductivity (κ_L), and electronic thermal conductivity (κ_e) of metal, semiconductor, and insulator as a function of electron density (n) in log scale [90].

and eq. 3.8, in order [90], where n , p , $\mu_{(i=e,tot)}$, and $\mu_{(i=h,tot)}$ are electron concentration, hole concentration, total electron mobility, and total hole mobility respectively. For $i=e$ ($i=h$), $c=n$ ($c=p$).

$$\sigma_n = qn\mu_{(e,tot)} \quad (3.7)$$

and,

$$\sigma_p = qp\mu_{(h,tot)} \quad (3.8)$$

σ_c and S_c are in direct and inverse relation with carrier concentration respectively. Therefore, semiconductors are a better choice than metal and insulator, as one of the parameters (σ or S) in σS^2 becomes negligible in metal and insulator [90, 91].

The hydrodynamic model is a comprehensive approach for current calculation [11]. However, simplified expressions for current of n-type (I_n) or p-type (I_p) NWs in thermoelectric systems can be derived based on total electric field ($\vec{E}_c$), eq. 3.9 [73, 92, 93]:

$$\vec{I}_c = \sigma_c \vec{E}_c \quad (3.9)$$

The resistance of the channel (R_{ch}) is inversely proportional to the area (A) and σ of the majority carriers. Eq. 3.10 shows the importance of increasing mobility for further

reduction of resistance in a NW with electrons as majority carriers [72]:

$$R_{ch} = \frac{L_{ch}}{\sigma_n A} = \frac{L_{ch}}{qn\mu_{(e,tot)}A} \quad (3.10)$$

Where L_{ch} is length of the TEM.

Thermal conductivity ($\kappa = \kappa_e + \kappa_L$) refers to the ability of materials to conduct heat [94]. Reducing the thermal conductivity leads to better temperature difference (ΔT) maintenance across the NW, due to suppression of heat transfer. Thermal conductivity is the sum of heat transport by carriers (κ_e) and phonons in the lattice (κ_L) [90, 94, 95], fig 3.2 (b). The challenge to increase ZT in bulk materials is due to the direct relation of σS^2 and κ_e with carrier concentration, while κ_L remains mainly constant [90]. Electronic thermal conductivity (κ_e) can be calculated using eq. 3.11 [69, 90, 94]:

$$\kappa_e = L_0 \sigma_c T \quad (3.11)$$

Where the Lorentz number (L_0) can be estimated using eq. 3.12 [69, 94],

$$L_0 = \frac{\pi^2}{3} \frac{k_B^2}{e^2} = 2.44 \times 10^{-8} \text{ W}\Omega\text{K}^{-2} \quad (3.12)$$

Lattice thermal conductivity (κ_L) can be reduced by nano-structuration of materials, leading to phonon confinement [58–60, 90]. Since κ_L is the dominant mechanism in heat conduction through semiconductors [95–97], κ can be reduced significantly due to phonon confinement. κ_L is calculated using eq. 3.13 [95]. Lattice thermal conductivity is dependent on phonon angular frequency (ω), group velocity of phonon's propagation (v_g), Debye temperature of materials (T_D), temperature of lattice (T_L), and total scattering relaxation time (τ_c) [94, 95].

$$\kappa_L = \frac{1}{3} \int_0^{\frac{T_D}{T}} v_g^2 \tau_c C_v(x) dx = \frac{k_B}{2\pi^2 v_g} \left(\frac{k_B}{\hbar} \right)^3 T^3 \int_0^{\frac{T_D}{T}} \frac{\tau_c x^4 e^x}{(e^x - 1)^2} dx \quad (3.13)$$

Where,

$$x = \frac{\hbar\omega}{k_B T} \quad (3.14)$$

Heat capacity (C_v) required for computation of κ_L is calculated by using Debye model [94]. C_v in this model is proportional to T^3 at low temperatures ($T \ll T_D$) and $3Nk_B$ at high temperatures ($T \gg T_D$) [98], where N is number of atoms in a crystal. The constant Debye temperature is an inherent property of materials; and is in direct relation with maximum allowed angular frequency of atom's vibration, also called Debye angular frequency (ω_D). Eq. 3.15 shows the relation of T_D with ω_D [94, 98].

$$T_D = \frac{\hbar\omega_D}{k_B} \quad (3.15)$$

Angular frequency (ω) range as a function of wave vector (k) for two atoms with mass M_i and M , lattice constant a , distance of $\frac{a}{2}$, interaction energy of K , propagating in optical (ω_+) or acoustic manner (ω_-) are shown in eq. 3.16 [99]. At low ω_- and high ω_+ , atoms are moving in and out of phase respectively [94].

$$\omega_{\pm}^2 = K \left(\frac{1}{M_i} + \frac{1}{M} \right) \pm K \sqrt{\left(\frac{1}{M_i} + \frac{1}{M} \right)^2 - \frac{4\sin^2(qa/2)}{M_i M}} \quad (3.16)$$

Other than frequency of phonons, the group velocity of acoustic phonons (v_g) has a significant effect on heat conduction, eq. 3.17. Although optical phonons have negligible effect in heat transport propagation, their possible interaction with acoustic phonons can impact κ_L [94, 100].

$$v_g = \frac{\partial\omega_-}{\partial k} \quad (3.17)$$

The total scattering relaxation time is the result of different scattering mechanisms in which their contribution depend on ω , v_g , dimension, and doping concentration of the channel. Mathissen's rule can be used to combine relaxation times of major scattering mechanisms to obtain estimation of τ_c , eq. 3.18 [95, 100]:

$$\frac{1}{\tau_c} = \frac{1}{\tau_M} + \frac{1}{\tau_B} + \frac{1}{\tau_U} \quad (3.18)$$

Mass difference scattering (τ_M) occurs when dopants or another material with atom mass M_i is added to a host semiconductor with average atom mass of M [95], where $M \neq M_i$. The mole fraction, doping concentration, mass, and volume (V_i) of the added atoms significantly impact the scattering rate. Higher doping concentration, mass, and volume of the added atoms lead to lower κ_L [101, 102]. τ_M can be found using eq. 3.19 [95, 100].

$$\frac{1}{\tau_M} = \frac{V_0 \omega^4}{4\pi v_g^3} f_i \left[\left(\frac{M - M_i}{\sum_i f_i M_i} \right)^2 + \left[\left(\frac{G - G_i}{G} \right) - 6.4\gamma \left(\frac{V^{1/3} - V_i^{1/3}}{\sum_i \frac{f_i V_i^{-2/3}}{3}} \right) \right]^2 \right] \quad (3.19)$$

Where f_i is the fraction of the added atoms with respect to overall atoms, V_0 is the volume per unit atom, V is the volume of hosted atom, and γ is average inharmonicity of bonds between hosted and added atoms [95]. Increasing inharmonicity (defects) in the lattice has high importance in reducing κ_L . Phonon-phonon scattering increases as γ increases, which leads to thermal conductivity reduction [96]. G and G_i are bond stiffness constants of host and foreign atoms, as the result of repulsive or attractive forces due to nearest neighboring atoms [95, 103].

At diameters of NWs (d_{NW}) comparable with phonon mean free path (λ_{ph}), boundary scattering plays a key role in reducing κ_L [60, 104]. For better understanding of the range of the diameter, phonon mean free path can be estimated using eq. 3.20 [60]:

$$\lambda_{ph} \approx \frac{2\pi v_s}{x_d k_B T} \quad (3.20)$$

Where v_s is velocity of sound; and x_d is approximately equal to 3, 4, and 5 for 1D, 2D, and 3D structures respectively [60].

At these diameters, phonons approaching the interface with normal velocity, divert from their direction as they scatter from the boundary. The diverted phonons destruct the motion of phonons along the channel, and therefore reduce the conduction of heat. Eq. 3.21 shows the phonon scattering relaxation rate (τ_B) [95, 100].

$$\frac{1}{\tau_B} = \frac{v_g}{d_{NW}} (1 - p) \quad (3.21)$$

Where p is surface roughness of the boundary, $p = 1$ and $p = 0$ represent extremely rough and smooth surface, respectively.

Generally, there are two types of phonon-phonon scattering, (i) normal scattering, and (ii) umklapp phonon-phonon scattering. Energy is conserved in both types, meaning that angular frequency of first (ω_1) and second phonon (ω_2) after collision in both cases lead to total angular frequency of $\omega_3 = \omega_1 + \omega_2$. However, momentum is not conserved in umklapp scattering. The collision of phonons in umklapp scattering leads to a flip over in resultant momentum, which generates thermal resistance. Unlike umklapp phonon-phonon scattering, normal phonon-phonon scattering does not contribute to κ_L reduction [96]. The umklapp scattering relaxation time τ_U can be estimated using eq. 3.22 [100]:

$$\frac{1}{\tau_U} = 2\gamma^2 \frac{k_B T}{\mu_{sh} V_0} \frac{\omega^2}{\omega_D} \quad (3.22)$$

Where μ_{sh} is shear modulus.

3.2 Optimising power generators

As explained earlier, low thermal conductivity and high power factor is vital to achieve high figure of merit [77–81]. In this section, previous works on reducing κ , and increasing power factor are reviewed.

3.2.1 Reducing thermal conductivity

As shown in the analytical formulas (eq. 3.16 to eq. 3.21), atom mass differences in semiconductor, diameter of nanowire, and surface roughness have significant impact on κ [95, 100]. In this part, the actual significance of these parameters on the thermal conductivity (κ) is presented.

Fig. 3.3 (a) compares simulation & experimental results as a function of Si nanowire diameter (d_{Si}) [60]. The experimental results are consistent with analytical formulas for k_L . As seen in fig. 3.3, Monte Carlo simulations in Shi et al [60] work for lowly doped Si with smooth surface approximately matches the experimental results of Li et al. [105] for intrinsic silicon with minimised surface roughness. Houchbaum et al. [59] have experimentally shown significant degradation in κ by increasing boundary scattering, as the result of introducing surface roughness. Introduction of surface roughness reduces thermal conductivity by $\approx 80\%$, in comparison to smooth surface ($p \approx 0$ in eq. 3.21). As seen in fig 3.3 (a), boundary scattering of phonons is the dominant mechanism in down-scaled intrinsic/lowly doped Si [59, 105].

To better understand the effect of doping on κ , one has to add impurities to a bulk Si. Since boundary scattering and umklapp scattering rate is less in bulk Si than nano-structured Si [106], the impact of scatterings due to doping on κ in bulk is higher than

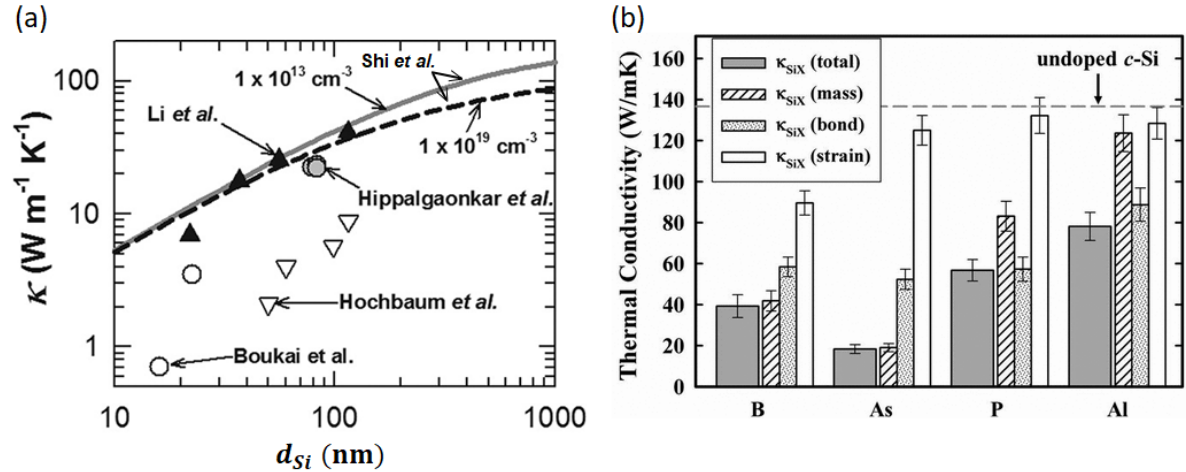


Figure 3.3: (a) Thermal conductivity as a function of diameter for rough surface (Houchbaum et al. [59]), smooth surface (Li et al. [105]), lowly boron doped = $1 \times 10^{13} \text{ cm}^{-3}$ (Shi et al [60]), and highly boron doped = $1 \times 10^{19} \text{ cm}^{-3}$ (Shi et al [60]). The figure is taken from [60]. (b) Thermal conductivity of bulk silicon doped with $4.875 \times 10^{20} \text{ cm}^{-3}$ of boron (B), arsenic (As), phosphorus (P), and aluminum (Al) [97]. Thermal conductivity variation due to mass difference, bond strength, and strain were individually studied in simulation, while other effects were assumed constant, to better understand their impact on total κ_L ($\kappa_{SiX}(\text{total})$) [97].

the other two mechanisms.

Simulation (fig 3.3 (b)) shows that impurities with higher mass and radius form higher mass disorder and lattice strain, which leads to higher phonon scattering rates [95, 97]. As seen in fig 3.3 (b), the effect of lattice straining due dopant's mass and radius is negligible; and the main contribution to κ reduction is due to mass difference of hosted atoms with dopants [97]. In addition, as analytically shown in eq. 3.19 and eq. 3.22, bond disorder (γ) has significant impact on reducing κ [95, 97], fig. 3.3 (b). As seen in fig 3.3, equal κ is achieved for As-doped ($4.875 \times 10^{20} \text{ cm}^{-3}$) bulk Si and lowly B-doped ($1 \times 10^{13} \text{ cm}^{-3}$) silicon NW with $d_{Si} = 36 \text{ nm}$. Although heavily doping of bulk materials are effective to reduce κ , high doping results in mobility degradation due to ionised impurity scattering [11, 75].

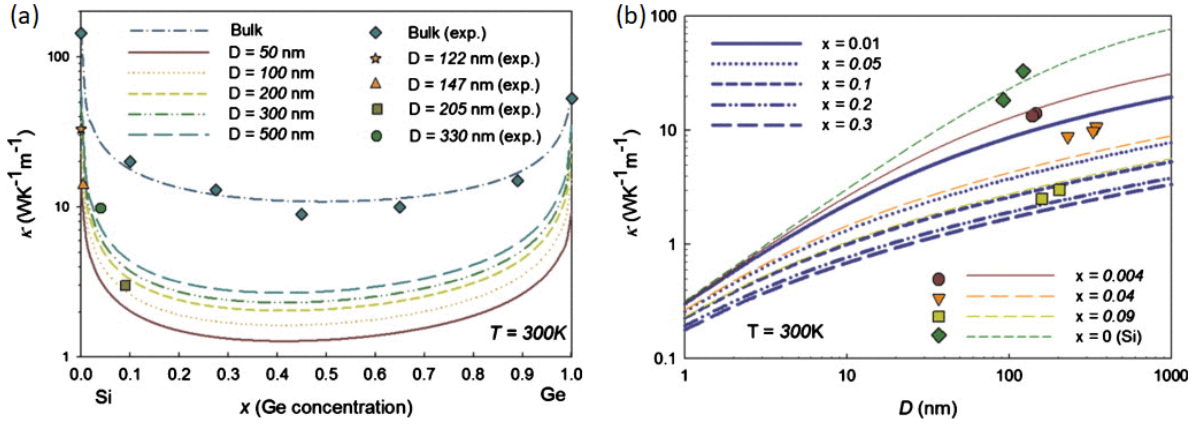


Figure 3.4: (a) Thermal conductivity of $\text{Si}_{1-x}\text{Ge}_x$ as a function of mole fraction (x) for different diameters (D) of NWs [107]. (b) thermal conductivity of $\text{Si}_{1-x}\text{Ge}_x$ as a function of diameter d_{SiGe} (or D) for different mole fractions (x) of germanium [107].

Similar to doping, mass and volume differences of atoms in alloys lead to phonon scattering [108]. Fig 3.4 shows mole fraction (x) and diameter dependence (D) of silicon germanium, $\text{Si}_{1-x}\text{Ge}_x$. Combination of boundary and mass difference scattering have led to lower thermal conductivity for SiGe than Si [107], fig. 3.4.

3.2.2 Optimising the power factor via carrier modulation

Other than reducing κ , minimisation of ionised impurity scattering has been another area of interest to increase σS^2 . Reducing mobility degradation, increases electrical conductivity without change in Seebeck coefficient [109]. As explained earlier, doping materials lead to mobility degradation [11, 75]. Different approaches have been taken to accumulate carriers in an intrinsic channel, leading to minimisation of impurity scattering. In this sub-section, these approaches are discussed and compared.

Doping modulation of an intrinsic or lowly doped channel via hetero-structural layers is one of the approaches taken by researches. This is mainly done by wrapping (fig. 3.5 (a) and (c)) a lowly/intrinsic material (channel) with heavily doped regions. As a consequence of this approach, the majority carriers in heavily doped structure are injected into the lowly/intrinsic material, leading to accumulation of carriers and band bending in the channel (fig. 3.5 (b) and (d)) [76, 82, 83, 109]. Although experimental [82, 83, 109] and simulation [82, 109] results confirm the ability of doping modulation to form carrier concentration in the channel, possibility of forming uniform doping profiles across all units decreases as TEGs down-scale [1].

To eliminate the bottleneck of having to dope every unit of TEG in doping modulation approach, completely intrinsic core/shell structures for carrier modulation in the channel have been researched. In carrier modulation approach, band offset between shell and core results in a strong internal electric field at the interface [83–85]. The electric field accumulates carriers to the interface of the core (channel). Depending on the relative positions of conduction and valence bands, the electric field at the interface leads to either electron or hole accumulation in the channel [84, 85]. Fig. 3.6 (a) shows a deposited intrinsic AlN and AlGaIn on triangular shaped intrinsic GaN. The deposited i-AlGaIn has higher conduction band than i-GaN. This means that electrons above AlGaIn conduction band has higher energy than GaN. The difference in energy of electrons in these materials

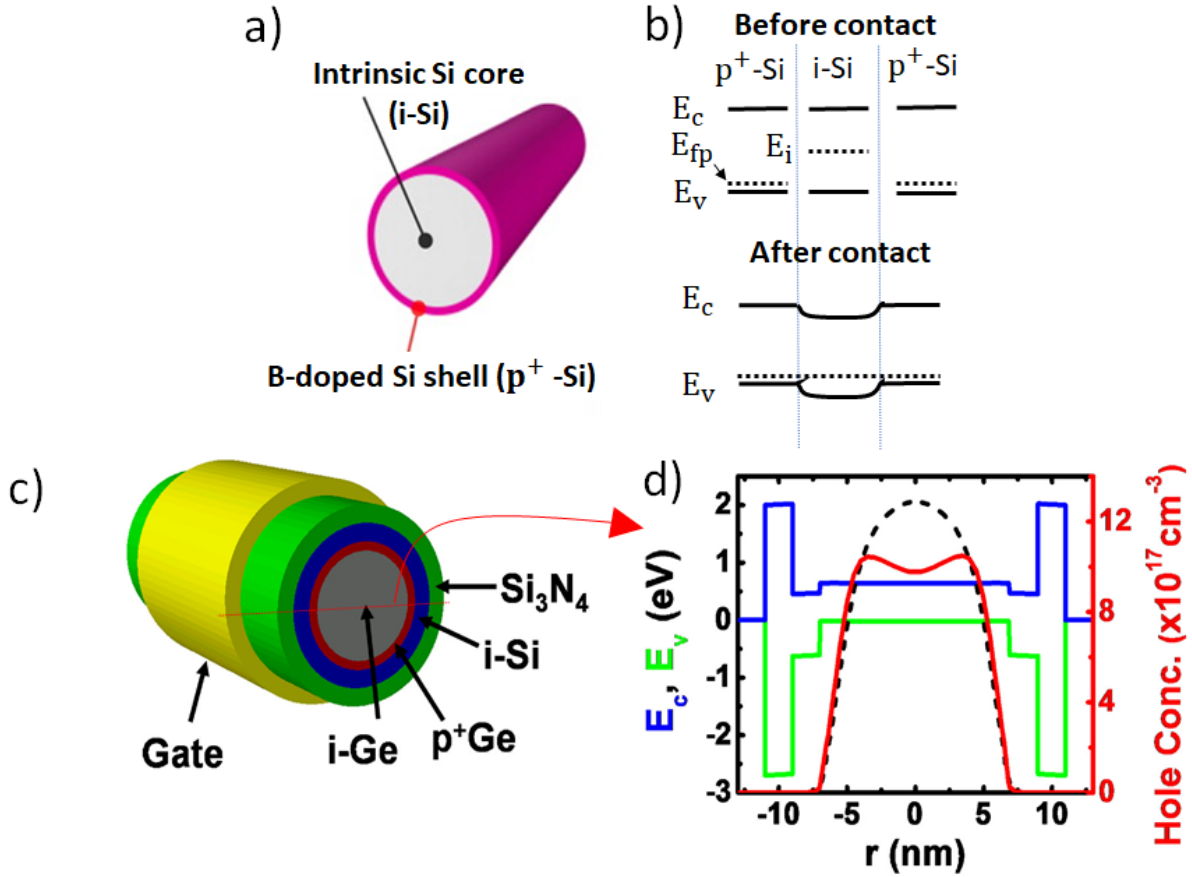


Figure 3.5: (a) 3D view of p^+ -Si/i-Si shell/core structure, to modulate hole concentration in i-Si [109]. (b) Sketched band diagram of p^+ -Si/i-Si/ p^+ -Si before and after contact with each other, to explain the theory of this method. (c) 3D gated hetero-structure to further control the modulated holes in i-Ge, due to its contact with p^+ -Ge/i-Si [82]. (d) Energy band (left axis) and hole concentration (right axis) across the radius of the structure; where red is for i-Ge ($d = 6$ nm)/ p^+ -Ge ($d = 1$ nm)/i-Si ($d = 2$ nm) with p^+ -Ge = 1×10^{19} ; and dashed line is for i-Ge ($d = 7$ nm)/ p^+ -Ge ($d = 2$ nm)/i-Si ($d = 2$ nm) with p^+ -Ge = 2.2×10^{18} [82].

result in flow of electrons from i-AlGa_{0.3}N to i-GaN, leading to accumulation of electrons in GaN. 2nm AlN was deposited to reduce alloy scattering, to preserve the conduction band difference at AlGa_{0.3}N/GaN interface [84].

Fig. 3.6 (b) shows an intrinsic silicon wrapped around an intrinsic germanium. Following similar concept as [84], the difference in valence bands of the intrinsic silicon and intrinsic germanium leads to accumulation of holes in germanium (fig 3.6 (c)).

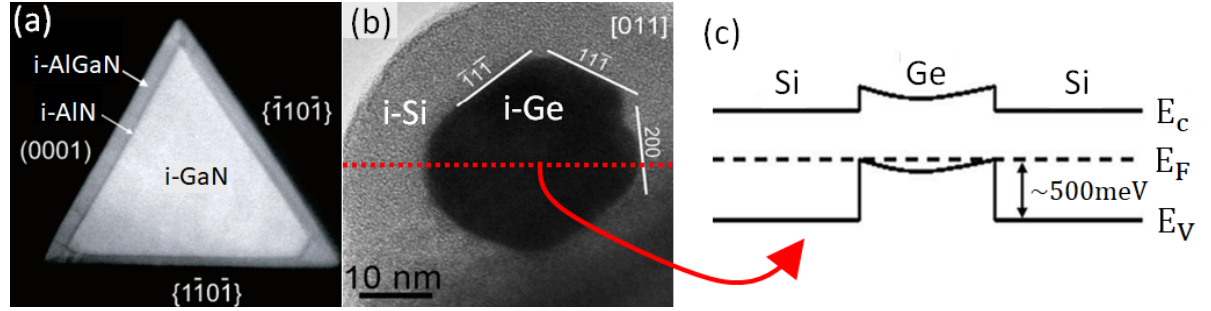


Figure 3.6: (a) Transmission electron microscopy image of a fabricated i-AlGaN/i-AlN/i-GaN to modulate electron concentration in i-GaN, where i stands for intrinsic [84]. (b) Fabricated i-Si/i-Ge structure to accumulate holes in intrinsic Ge [85]. (c) Band diagram of (b), showing the accumulated holes in germanium while Si remained intrinsic [85].

As seen in fig 3.6 (c), the internal electric field solely accumulates germanium with holes, while silicon remains approximately intrinsic [85]. Insulation and gating of these structures require at least 3 and four layers of materials as shown in fig 3.5 (c). Adding interfaces to the structure increases the complexity, and increases probability of errors. In addition, one has to find methods to modulate both electron and hole concentrations for widely used and abundant material, like Si [59].

Gating a lowly doped/intrinsic channel is another method for carrier modulation [77–81]. In this approach, a core structure is wrapped by an oxide and metal. The applied voltage to the metal gate modulates the carrier type and its concentration, therefore, tunes σS^2 . Previously, gate voltage was found to tune σS^2 of Bi_2Te_3 [78], Ge/Si core/shell [81], InAs [79], PbSe [80], and Si [77]. Although σS^2 is accurately tuned via gating, the requirement of voltage bias to generate voltage difference is not desirable.

Despite the observations that carrier-modulation improves σS^2 due to rise of mobility [109], κ_e also increases, eq. 3.11. Although κ_L is a dominant mechanism in heat conduction in semiconductors [95–97], the contribution of κ_e to overall thermal conductivity increases as σ increases or $\kappa_L \rightarrow 0$. Therefore, one has to calculate ZT and κ_e to evaluate the actual improvement of TEGs due to carrier modulation. Neophytou et al [74] have done simulations to investigate the effect of carrier modulation via gate bias on the

power factor (fig. 3.7 (a)), electron conductivity (fig. 3.7 (b)), and therefore, ZT (fig. 3.7 (c)). Despite the increase in electronic thermal conductivity of Si ($\kappa_{(e,Si)}$) as a function of carrier concentration (n), he has shown approximately 3.4 times higher ZT for gated than doped Si NW (fig. 3.7 (c)). Neophytou et al [74] have assumed lattice thermal conductivity of $1 \frac{W}{mK}$ for Si ($\kappa_{(L,Si)}$) with diameter of 12 nm, to calculate the upper boundary of ZT. Fig. 3.7 (d) uses the calculated $\kappa_{(L,Si)}$ for a Si with 12 nm diameter (d_{Si}) in [60], to estimate ZT based on the obtained σS^2 and $\kappa_{(e,Si)}$ in [74] for the studied gated Si NW.

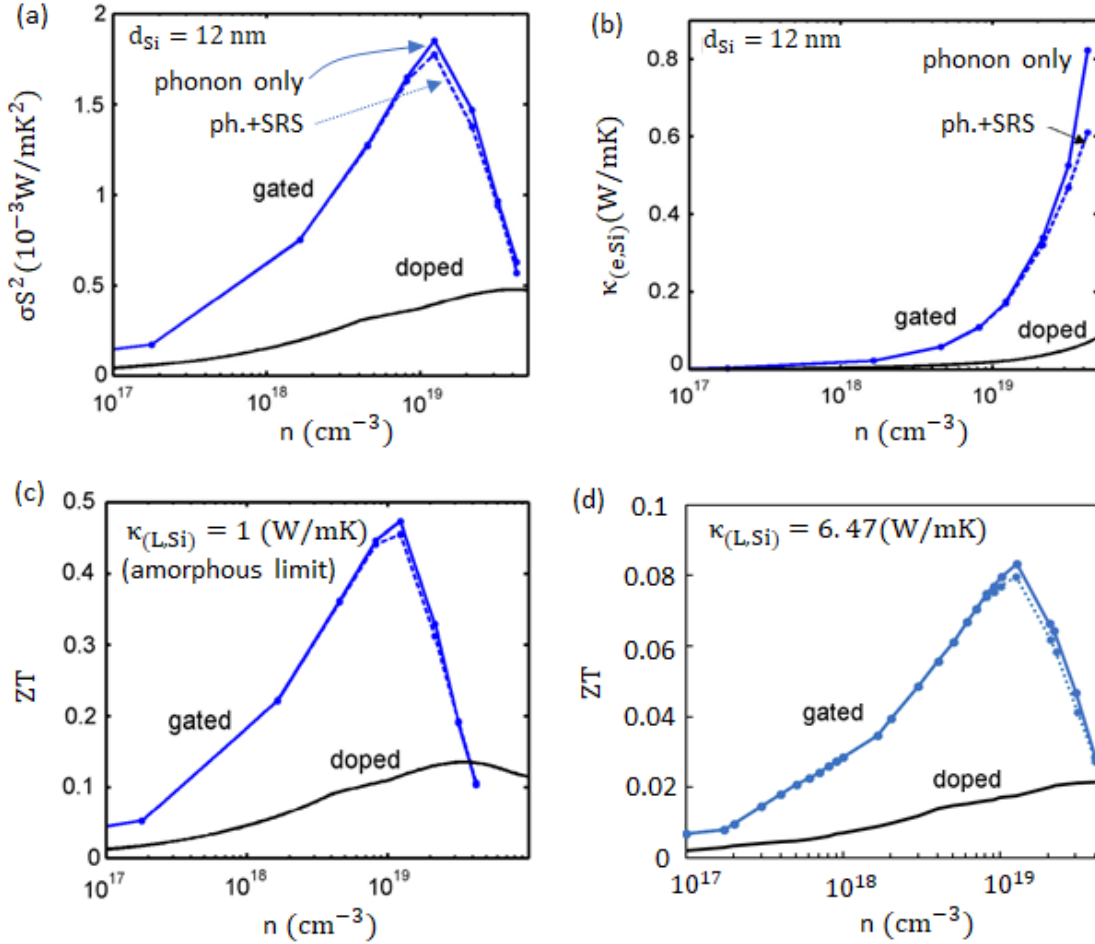


Figure 3.7: (a) σS^2 - n , (b) $\kappa_{(e,Si)}$ - n , (c) ZT- n for gated and doped Si with $d_{Si} = 12 \text{ nm}$ and $\kappa_{(L,Si)} = 1 \frac{W}{mK}$ [74]; and (d) ZT- n of the simulated NW in [74] with $\kappa_{(L,Si)} (= 6.47 \frac{W}{mK})$ obtained in [60]. The blue solid lines are the results for gated Si NW considering phonon scattering only, blue dotted lines are the data for gated Si NW considering both phonon scattering and surface roughness scattering (SRS), and black lines are results for doped Si.

3.3 On-chip temperature sensing

Down-scaling of transistors is vital to increase the performance of microprocessors. The power density of microprocessors rises by placing more transistors in a unit area [110]. Denser transistor blocks and smaller transistors lead to introduction of hot spots in integrated circuits (ICs) [57, 62, 111]. To prevent failure or loss of building blocks, one has to place temperature sensors to monitor the temperature [111–114].

The temperature sensor must be compatible with CMOS technology, scalable, stable over a wide range of temperatures, accurate, ability (adoptable) to be powered with the local supply voltage, and immune to fluctuations (noise) in supply voltage [110, 115–117]. Error (inaccuracy) of the sensed temperature might be due to error in sensor (sensor inaccuracy), and/or error due to its distance from the hot spot [110]. The distance error is caused by failure of detecting hot spots across the microprocessor or/and large scale of the fabricated temperature sensor, such that the sensor can not be placed in a building block of transistors [110, 114, 118]. To minimise the error of not being able to detect hot spots, up to 44 temperature sensors are placed in modern microprocessors [114, 118].

In addition to the mentioned requirements, since temperature sensors must be spread across the processor, placing sensors with requirement of an external reference signal, calibration, voltage supply, or bias current, increases the cost and complexity of circuit design and fabrication [114, 115]. Furthermore, the accuracy of doped sensors can degrade by unwanted fluctuations in doping [111]. Therefore, elimination of any or all of these fluctuations is preferable. Currently, resistors [119–125], MOSFETs [112, 115, 126, 127], bipolar junction transistors (BJTs) [111, 128–132], and thermal diffusivity of bulk silicon [114, 118, 133] are used for temperature sensing in integrated circuits.

Temperature can be sensed in two approaches using resistors: (i) frequency based sensing, where phase of frequency shifts as a function of temperature; and (ii) resis-

tance based, which the resistance of the sensor is in direct relation with the change of temperature [116, 120, 123]. In the first case, a stable external frequency source is used as a reference signal, to be compared with the temperature dependence signal, generated in resistance-capacitance (RC) filter circuit. In the second case, the resistance of a temperature dependant resistor is compared with a reference resistor [120, 123]. Since metal-insulator-metal capacitors (MIMs) in RC filters are more stable than on-chip resistors, frequency based resistors are more accurate than temperature based resistor. However, the disadvantage of frequency based resistors is the requirement of an external frequency source [120]. Table 3.1 includes recent works on frequency based resistors. Although good accuracy is shown (table 3.1) for resistors, they are large and require costly multi-point calibration for nano-scale CMOS [111, 114, 117]

Table 3.1: Shows performance of recent works on some sensors compatible with CMOS technology.

Ref/year	Sensor type	Size (mm^2)	V_s (V)	Range ($^{\circ}C$)	Sensor inaccuracy ($^{\circ}C$)
[125]/2015	Resistor	0.09	3.3	-40 to 85	± 0.12
[121]/2019	Resistor	0.12	1.8	-40 to 180	± 0.1
[120]/2018	Resistor	0.25	1.8	-55 to 125	± 0.12
[116]/2017	Resistor	0.72	1.8	-40 to 85	± 0.03
[122]/2015	Resistor	1.12	0.75	0 to 90	± 0.2
[126]/2019	MOSFET	0.0014	1.1	-60 to 40	± 0.2
[115]/2016	MOSFET	0.004	0.8 to 1.1	0 to 100	± 0.9
[134]/2014	MOSFET	0.022	0.4	0 to 100	± 1.3
[127]/2014	MOSFET	0.085	0.85	-40 to 125	± 0.4
[113]/2018	BJT	0.003	1.3	-10 to 110	± 1.35
[117]/2019	BJT	0.0146	2 to 2.7	-40 to 125	± 1.7
[111]/2019	BJT	0.03	1.2	-20 to 100	± 0.8
[129]/2020	BJT	0.2	1.125	-35 to 95	NK
[114]/2017	TD	0.00165	0.9	-40 to 125	± 0.75
[118]/2015	TD	0.0028	1.8	-35 to 125	± 1.2
[135]/2014	TD	0.008	NK	-40 to 125	± 0.65

The MOSFET's source-drain current (I_{ds}) is temperature sensitive, the source-gate

voltage difference ($\Delta V_{GS} = V_{GS_f} - V_{GS_i}$) applied to keep I_{ds} constant is a measure of $\Delta T = T_f - T_i$; where V_{GS_i} is initial voltage at initial temperature T_i and V_{GS_f} is voltage after rise of temperature to T_f . As temperature increases in a MOSFET, mobility of carriers and threshold voltage reduces [11, 112, 136]. Reduction of mobility (reduction of threshold) increases (reduces) the ΔV_{GS} due to ΔT . The linear relation of ΔV_{GS} with ΔT at constant I_{ds} is used for temperature sensing. The sensitivity of MOSFETs can be increased by using higher current supply or reducing $\frac{W}{L}$ ratio, where W and L are width and length of the MOSFET's channel [112]. Unlike BJT and resistors, MOSFETs are relatively small in size, down to 0.0014 mm^2 . However, they require multi-point calibration and are sensitive to fabrication process variation [111, 112, 114, 137].

Similar to MOSFETs, performance of BJTs degrade linearly as temperature increases. The base-emitter voltage (V_{BE}) reduces as temperature of the transistor increases. The linear relation of ΔV_{BE} ($\Delta V_{BE} = V_{BE_f} - V_{BE_i}$) as a function of ($\Delta T = T_f - T_i$) is used to sense the temperature. V_{BE_i} and V_{BE_f} are base-emitter voltage at T_i and T_f respectively [111, 129]. BJTs are less sensitive to fabrication process variation than MOSFETs [112], and in some circuit designs don't require multi-point calibration [111]. However, they generally have high power and voltage supply consumption [126].

The rate of heat spreading from hot source to other cold areas of a material is defined by thermal diffusivity (D) [138]. Temperature dependence of D in bulk Si can be used to sense temperature variations in ICs. Thermal diffusivity based temperature sensors (TD) have a heater, generating a heat pulse, placed at a certain distance from a temperature sensor. Temperature variation in ICs affects the time taken for the generated heat pulse to reach the sensor. The amount of shift in time, defines the temperature in TD sensors [114, 118, 133, 137]. Similar to BJTs, TD sensor benefit from low non-calibrated inaccuracy ($\approx \pm 1.4$). However, TD sensors are power-hungry, due to requirement of a heater [113].

3.4 Summary

Nano-structuration of FETs leads to improved performance but also to increased self-heating. The reduction of thermal conductivity in nano-structures can be used for thermo-electric power generation as well as temperature sensing. Doping modulation, intrinsic core/ intrinsic shell carrier modulation, and gating can be used to improve thermo-electric power generation, due to minimisation of ionised impurity scattering. In addition, gated structures, such as, MOSFETs and BJTs have been previously used as temperature sensors. Further improvement on temperature sensing and thermo-electric power generation can be achieved by using gated intrinsic nanowires.

SENTAURUS TECHNOLOGY COMPUTER AIDED DESIGN (TCAD)

Sentaurus Technology Computer Aided Design (TCAD) is a commercial software package for studying electrical and thermal properties of 1D, 2D, or 3D shaped semiconducting devices. Sentaurus TCAD is used for the evaluation of novel devices in this work. Typical simulation steps in this project are shown in fig. 4.1 (a). A concept geometry can be built and meshed in sentaurus structure editor (SDE). The meshing point are points in which physics models calculate the electrical and thermal properties of the device. The areas that require high precision, such as interfaces, must have dense mesh points (fig. 4.1 (b)). SDE generates the required meshed geometry in two ways, (i) generating a script followed by msh.tdr format file based on the designed 1D, 2D, or 3D geometry in SDE, or (ii) generating a msh.tdr format based on running a written script in a command file (.cmd format). The prepared msh.tdr file can then be sent to sentaurus device (sdevice) for studying its transport characteristics. The properties of the designed device is studied based on the physics models defined in sdevice. Although the physics models are supported by a library of constants for different materials, these

data can be modified in the "parameter name.par" file and fed to the physics models [11].

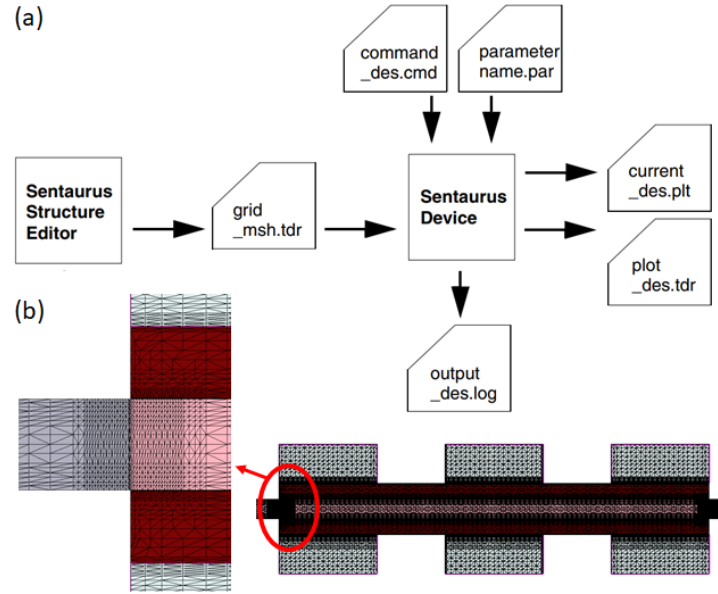


Figure 4.1: (a) Diagram of simulation flow of these projects using sentaurus TCAD [11]. (b) Cross section of the meshed designed geometry.

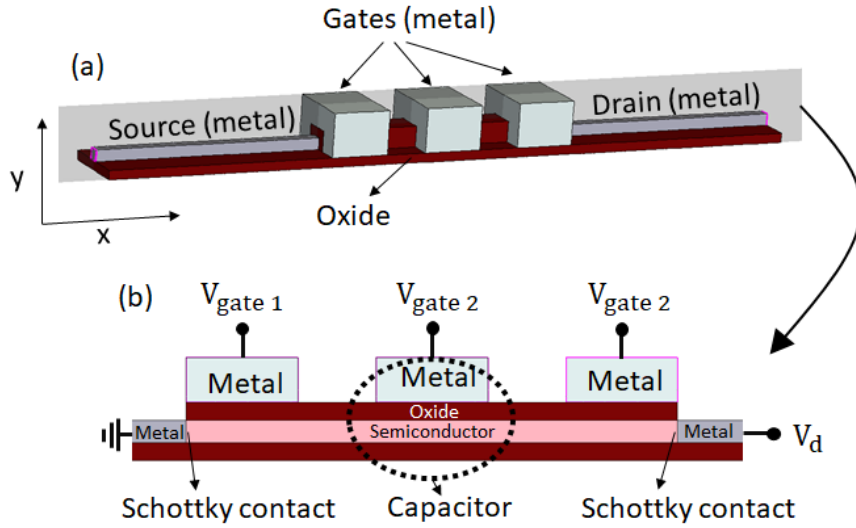


Figure 4.2: (a) 3D view of a RNW-FET with triple gates, (b) cross section of the RNW-FETs with gate voltages of V_{gate1} , V_{gate2} , and V_{gate3} , and drain voltage of V_d .

Fig. 4.2 shows a cubical RNW-FET. TEGs and Si RNW-FETs in this work are based

on intrinsic channels, connected to two Schottky contacts (metal/i-semiconductor/metal), covered by an insulator and metal gate(s). The performance of these devices is highly dependent on phenomenons at interfaces, mobility degradation of carriers, and carrier distribution. This section introduces the used models for simulation of the gated structures; and boundary conditions of the simulations.

4.1 Poisson equation, conduction band, and valence band

The energy band diagram of the semiconductor can be plotted by solving the Poisson equation (eq. 4.1). The electrostatic potential of semiconductor (ϕ_s), required to plot the conduction band (E_c) and valence band (E_v), is the solution of the Poisson equation. Electrostatic potential is dependent to variation of electron concentration (n), holes concentration (p), acceptor concentration (N_A), donor concentration (N_D), traps and fixed charges (ρ_{trap}) [11, 139].

$$\nabla \cdot (\epsilon \nabla \phi_s) = -q(p - n + N_D - N_A) - \rho_{trap} \quad (4.1)$$

For intrinsic gated structures ($N_D = N_A = 0$), it simplifies to:

$$\nabla \cdot (\epsilon \nabla \phi_s) = -q(p - n) - \rho_{trap} \quad (4.2)$$

Consequently, the E_c (eq. 4.3) and E_v (eq. 4.4) across the channel can be calculated by the solution of Poisson equation (ϕ_s), electron affinity of semiconductor (χ_s), effective band gap of the semiconductor ($E_{g,eff}$) and putting electrostatic potential of the intrinsic semiconductor as a reference point (ϕ_{ref}) [11].

$$E_c = -\chi_s - q(\phi_s - \phi_{ref}) \quad (4.3)$$

and,

$$E_v = -\chi_s - E_{g,eff} - q(\phi_s - \phi_{ref}) \quad (4.4)$$

Where effective band gap ($E_{g,eff}$) can be found as shown below:

$$E_{g,eff}(T) = E_g(T) - E_{bgn} \quad (4.5)$$

E_{bgn} is the difference of actual band gap (E_g) with $E_{g,eff}$. Band gap narrowing (E_{bgn}) occurs due to heavy doping. Both E_g and $E_{g,eff}$ are temperature dependent. Since gated structures are intrinsic, $E_{bgn} = 0$ and $E_{g,eff}(T) = E_g(T)$.

Variation in energy of E_c and E_v is highly dependent to parameters that change the carrier concentration at every meshing point of the semiconductor. These parameters will be explained later.

4.2 Simulation of Schottky barriers

Eq. 2.5 is used for Schottky barrier height calculation at the interface. As explained in 2.1.2, precise calculation of ϕ_B is subject to accurate calculation of barrier lowering for electrons ($\Delta\phi_B$) and holes ($\Delta\phi_{Bh}$). $\Delta\phi_B$ and $\Delta\phi_{Bh}$ due to the image force are calculated using a model shown in eq. 4.6 and eq. 4.7 in sentaurus TCAD [11]:

$$\Delta\phi_B(\vec{E}) = \begin{cases} a_e \left(\left(\frac{\vec{E} \cdot \hat{n}}{E_{ref}} \right)^{p_e} - \left(\frac{\vec{E}_{eq} \cdot \hat{n}}{E_{ref}} \right)^{p_e} \right) & \text{if } \vec{E} \cdot \hat{n} > 0 \\ 0 & \text{if } \vec{E} \cdot \hat{n} \leq 0 \end{cases} \quad (4.6)$$

and

$$\Delta\phi_{Bh}(\vec{E}) = \begin{cases} a_h \left(\left(\frac{\vec{E} \cdot \hat{n}}{E_{ref}} \right)^{p_h} - \left(\frac{\vec{E}_{eq} \cdot \hat{n}}{E_{ref}} \right)^{p_h} \right) & \text{if } \vec{E} \cdot \hat{n} \leq 0 \\ 0 & \text{if } \vec{E} \cdot \hat{n} > 0 \end{cases} \quad (4.7)$$

The reference electric field (E_{ref}) in this model is constant ($1 \frac{V}{cm}$); and values of constants are $a_e = a_h = 2.6 \times 10^{-4} eV$ and $p_e = p_h = 0.5$ [11]. $\vec{E} \cdot \hat{n}$ and $\vec{E}_{eq} \cdot \hat{n}$ are the total

electric field normal to the metal/semiconductor after and before the applied voltage bias, where $\vec{E}$, $\vec{E}_{eq}$, and $\hat{n}$ are total electric field in the presence of voltage bias, total electric field at zero bias, and gradient of the distance to the interface, respectively.

The electron density (n_B) and hole density (p_B) at the interface considering the difference of ϕ_m and χ_s , barrier lowering due to carrier concentration manipulation as a function of gate voltage, and external voltage applied to source ($V_{ext} = V_s$) or drain ($V_{ext} = V_d$), are calculated as shown below [11, 14]:

$$n_B = N_C \exp\left(\frac{-q\phi_{B_f}}{kT}\right) \quad (4.8)$$

And,

$$p_B = N_V \exp\left(\frac{-E_{g,eff} + q\phi_{B_f}}{kT}\right) \quad (4.9)$$

The overall electrostatic potential (ϕ_s) in TCAD at source/channel and channel/drain is defined by knowing ϕ_{B_f} due to barrier lowering, $V_{d,s}$, temperature, N_c , and effective intrinsic density [11], eq. 4.10:

$$\phi_s = V_{d,s} - \phi_{B_f} + \frac{k_B T}{q} \ln\left(\frac{N_c}{n_{i,eff}}\right) \quad (4.10)$$

where $n_{i,eff}$ is the variation of intrinsic carrier density (n_i) with respect to the amount of band gap narrowing (E_{bgn}). $n_{i,eff}$ can be calculated as shown below [11]:

$$n_{(i,eff)} = n_i \exp\left(\frac{E_{bgn}}{2k_B T}\right) \quad (4.11)$$

4.3 Simulation of contacts on insulators

The electrostatic potential (ϕ_s) calculated using TCAD at the interface of the semiconductor/ SiO_2 as a function of V_{gate} , and $\phi_m - \phi_s$ are calculated by eq. 4.12, assuming no trapped charges at the interface [11]:

$$\phi_s = V_{gate} - (\phi_m - \phi_s) \quad (4.12)$$

4.4 Hydrodynamic model for current and temperature

Accurate calculation of current and ΔV is highly dependent on accurate calculation of carrier temperature at every point across the NW, since effective density of states and carrier concentration are dependant to temperature [4, 72, 86, 139]. The hydrodynamic model is used to calculate the temperature of electrons (T_n), holes (T_p), and lattice (T_L) individually. This is done by obeying conservation of energy and balancing the energy loss and gain of carriers with reference to overall initial energy [11, 140]. This section is divided in two parts. Sub-section 4.4.1, gives the theory behind the hydrodynamic model. Sub-section 4.4.2, explains the approach for the initial guess in hydrodynamic model.

4.4.1 The hydrodynamic model

Temperature of carriers is found by calculating the gained kinetic energy density due to electric field via the gradient of energy bands $\left(\frac{\nabla E_{(c,v)}}{q}\right)$, gained energy due to heat flux ($\vec{S}_n$ for electrons, $\vec{S}_p$ for holes, and $\vec{S}_L$ for lattice), and energy loss rate of carriers due to carrier-phonon scattering [140]. Hydrodynamic model for electrons and holes is shown in eq. 4.13 [11]:

$$\left(\frac{\partial W_c}{\partial t} + \nabla \cdot \vec{S}_c\right) - \frac{\partial W_c}{\partial t} \Big|_{collision} = \vec{J}_c \cdot \frac{\nabla E_{(c,v)}}{q} \quad (4.13)$$

And for the lattice in eq. 4.14 [11]:

$$\left(\frac{\partial W_L}{\partial t} + \nabla \cdot \vec{S}_L\right) - \frac{\partial W_L}{\partial t} \Big|_{collision} = 0 \quad (4.14)$$

The average kinetic energy of the carriers ($\frac{3}{2}k_B T_c$) increase as the electric field $\left(\frac{\nabla E_{(c,v)}}{q}\right)$ increases [140]; consequently, the energy density of carriers (W_c) rises. W_c is shown in eq 4.15 [11]:

$$W_c = \frac{3k_B T_c}{2} \quad (4.15)$$

With T_c the carrier temperature.

And lattice energy density W_L is the product of lattice heat capacity (C_v) with lattice temperature (T_L), eq. 4.16 [11]:

$$W_L = C_v T_L \quad (4.16)$$

The carrier heat flux vectors $\vec{S}_c$ for electrons ($\vec{S}_{c=n}$) and holes ($\vec{S}_{c=p}$), and lattice heat flux vector $\vec{S}_L$ are given in eq. 4.17 and eq. 4.18, respectively [11, 140, 141]:

$$\vec{S}_c = -\frac{3k_B}{2q} \left(\pm T_c \vec{J}_c + k_B c \mu_{(i,tot)} T_c \nabla T_c \right) = \mp \left(\frac{3k_B T_c}{2q} \vec{J}_c \right) - \left(\frac{3}{2} \kappa_i \nabla T_c \right) \quad (4.17)$$

and,

$$\vec{S}_L = -\kappa_L \nabla T_L \quad (4.18)$$

Where $\kappa_{i=e}$ is the thermal conductivity of electrons, $\kappa_{i=h}$ thermal conductivity of holes, and κ_L lattice thermal conductivity. The total mobility of electrons ($\mu_{(i=e,tot)}$) and holes ($\mu_{(i=h,tot)}$) are calculated based on models introduced in section 4.5.

The carrier-phonon collision rate increases as the temperature of carriers increase ($T_c > T_{c0}$), where T_{c0} and T_c are initial and final carrier temperature. The collision rate for electrons and holes is given in eq 4.19 [11]:

$$\frac{\partial W_c}{\partial t} \Big|_{collision} = -\xi_c \frac{W_c - W_{c0}}{\tau_{e,c}} \quad (4.19)$$

Where W_{c0} is the initial carrier energy density, and $\tau_{e,c}$ is the energy relaxation time of electrons $\tau_{e,n}$ or holes $\tau_{e,p}$. ξ_c is a fitting parameter which tunes the collision rate, based on carrier density of the channel. $\xi_c \approx 1$ at high carrier density.

Collision term for the lattice is the result of both electron-phonon and hole-phonon scattering, eq. 4.20:

$$\frac{\partial W_L}{\partial t} \Big|_{collision} = \xi_n \frac{W_n - W_{n0}}{\tau_{e,n}} + \xi_p \frac{W_p - W_{p0}}{\tau_{e,p}} \quad (4.20)$$

The current density of electrons ($\overrightarrow{J_{c=n}}$) or holes ($\overrightarrow{J_{c=p}}$) are calculated based on variations in energy bands (∇E_c or ∇E_v), carrier density (n or p), and the effective mass of carriers (m_n^* for electrons or m_p^* for holes) [11]. $\overrightarrow{J_{c=n}}$ and $\overrightarrow{J_{c=p}}$ are calculated as shown in eq. 4.21 and eq. 4.22 respectively. Eq. 4.21 and 4.22 show the large impact of total electron $\mu_{(e,Tot)}$ and hole mobility $\mu_{(h,Tot)}$ on electron and hole current densities.

$$\overrightarrow{J_n} = qn\mu_{(e,Tot)} \left(\frac{\nabla E_c}{q} + \frac{k_B T_n \nabla n}{qn} - \frac{1.5k_B T_n \nabla \ln m_n^*}{q} \right) \quad (4.21)$$

and,

$$\overrightarrow{J_p} = qp\mu_{(h,Tot)} \left(\frac{\nabla E_v}{q} - \frac{k_B T_p \nabla p}{qp} + \frac{1.5k_B T_p \nabla \ln m_p^*}{q} \right) \quad (4.22)$$

Where,

$$\overrightarrow{E_c} = \frac{\nabla E_{c,v}}{q} \pm \frac{k_B T_c \nabla c}{qc} \mp \frac{1.5k_B T_c \nabla \ln m_c^*}{q} \quad (4.23)$$

Multiplying the right hand side of eq. 4.21 and eq. 4.22 by $A \times \frac{L_{ch}}{L_{ch}}$ would lead to current, voltage difference (ΔV_c) due to carrier electric field, and resistance:

$$\overrightarrow{I_c} = \left(\frac{qAc\mu_{(i,Tot)}}{L_{ch}} \right) \left[L_{ch} \left(\frac{\nabla E_{c,v}}{q} \pm \frac{k_B T_c \nabla c}{qc} \mp \frac{1.5k_B T_c \nabla \ln m_c^*}{q} \right) \right] \quad (4.24)$$

Where,

$$\Delta V_c = L_{ch} \left(\frac{\nabla E_{c,v}}{q} \pm \frac{k_B T_c \nabla c}{qc} \mp \frac{1.5k_B T_c \nabla \ln m_c^*}{q} \right) \quad (4.25)$$

As seen in eq. 4.23, $\overrightarrow{E_c}$ is generated as the result of the energy band gradient, carrier density gradient, and effective mass gradient across the NW. Due to relations of these parameters with carrier temperature [11, 141], applying ΔT grades the named parameters, and therefore generates ΔV_c (eq. 4.25). Boltzmann statistics (eq. 4.26 and eq. 4.27) is used to calculate the electron (n) and holes (p) densities across the nanowire based on the difference between the energy band edges (E_c or E_v) and the Fermi level (E_{fn} for electrons and E_{fp} for holes), [11].

$$n = N_c \exp \left(-\frac{E_c - E_{fn}}{k_B T_n} \right) \quad (4.26)$$

And,

$$p = N_v \exp\left(\frac{E_v - E_{fp}}{k_B T_h}\right) \quad (4.27)$$

Electron (n_B) and hole (p_B) concentration at metal/semiconductor interface can be calculated using eq. 4.8 and 4.9, respectively.

m_n^* and m_p^* across the channel can be calculated based on temperature of carriers (T_n and T_p) and/or effective density of states (N_c and N_v) [4, 11, 139]. Different models are used for Si and alloys, such as SiGe, to calculate carrier effective mass and effective density of states in Sentaurus TCAD [11].

4.4.1.1 Model used for calculation of $N_{c,v}$ and $m_{n,p}^*$ in Si

The effective density of states for Si is calculated using [11]:

$$N_{c,v} = 2.5094 \times 10^{19} \left(\frac{m_{n,p}^*}{m_0}\right)^{3/2} \left(\frac{T_{n,p}}{300K}\right)^{3/2} \text{ cm}^{-3} \quad (4.28)$$

m_n^* and m_p^* calculation for Si is dependent to the lattice temperature (T_L). In this model, m_n^* is calculated using the following relation:

$$\frac{m_n^*}{m_0} = ((6m_t)^2 m_l)^{1/3} \quad (4.29)$$

where,

$$m_t(T_L) = a_e \frac{E_g(0K)}{E_g(T_L)} \quad (4.30)$$

and,

$$E_g(T_L) = E_g(0K) - \frac{\alpha T_L^2}{T_L + \beta} \quad (4.31)$$

Where m_0 is the electron mass, m_l is longitudinal effective mass, m_t is transverse effective mass, $E_g(0K)$ is the Si band gap at 0 K (= 1.1696 eV [11]), and $E_g(T_L)$ is band gap variation as the function of T_L .

In addition, lattice temperature dependent m_p^* is calculated using the equation below:

$$m_p^* = \left(\frac{a_h + bT_L + cT_L^2 + dT_L^3 + eT_L^4}{1 + fT_L + gT_L^2 + hT_L^3 + iT_L^4} \right)^{2/3} m_0 \quad (4.32)$$

The parameters for calculation of m_n^* and m_p^* in Si are shown in table 4.1.

Table 4.1: Parameters for calculation of carrier effective mass in Si [11]

Parameter name	value	Unit	Parameter name	value	Unit
a_e	0.1905	1	d	0.1263218×10^{-5}	$1/K^3$
m_l	0.9163	1	e	0.3025581×10^{-8}	$1/K^4$
α	4.73×10^{-4}	eV/K	f	0.4683382×10^{-2}	$1/K$
β	636	K	g	0.2286895×10^{-3}	$1/K^2$
a_h	0.4435870	1	h	0.7469271×10^{-6}	$1/K^3$
b	0.3609528×10^{-2}	$1/K$	i	0.1727481×10^{-8}	$1/K^4$
c	0.1173515×10^{-3}	$1/K^2$			

4.4.1.2 Model used for calculation of $N_{c,v}$ and $m_{n,p}^*$ in SiGe

Variation of N_c and N_v for $Si_{(1-x)}Ge_x$ at room temperature ($N_c(300K)$ and $N_v(300K)$) as a function of mole fraction (x) is estimated using eq. 4.33:

$$N_{c,v}(300K) = (1-x)(N_{c,v-Si}) + x(N_{c,v-Ge}) \quad (4.33)$$

Where N_{c-Si} and N_{v-Si} are the electron ($2.89 \times 10^{19} cm^{-3}$) and hole ($3.14 \times 10^{19} cm^{-3}$) effective density of states for Si; and N_{c-Ge} and N_{v-Ge} are electron ($1.02 \times 10^{19} cm^{-3}$) and hole ($0.5 \times 10^{19} cm^{-3}$) effective density of states for Ge, extracted from [11]. The temperature dependence of N_c and N_v at every mole fraction is calculated as shown below [11]:

$$N_{c,v}(T_{n,p}) = N_{c,v}(300K) \left(\frac{T_{n,p}}{300K} \right)^{3/2} \quad (4.34)$$

The carrier effective mass in this model is temperature independent. m_n^* and m_p^* for alloys are calculated using equation below [11]:

$$\frac{m_{n,p}^*}{m_0} = \left(\frac{N_{c,v}(300K)}{2.5094 \times 10^{19} cm^{-3}} \right)^{2/3} \quad (4.35)$$

4.4.2 Initial guess in hydrodynamic model

At the beginning of the simulation, the hydrodynamic model uses an average temperature (T_{ave}) as an initial guess. As an example, $T_{ave} \approx \frac{T_h - T_c}{2}$ for TEGs with temperature difference ($\Delta T = T_h - T_c$) due to hot source (T_h) and cold sink (T_c) at both ends. In

addition, for devices without imposed ΔT , $T_{ave} = 300$ K is used. At the initial guess, $T_{ave} = T_{L0} = T_{n0} = T_{p0}$, where T_{L0} , T_{n0} , and T_{p0} are the initial lattice temperature, electron temperature, and hole temperature [11]. In this case, eq 4.13 simplifies to:

$$\nabla \cdot \vec{S}_c = \vec{J}_c \cdot \frac{\nabla E_{(c,v)}}{q} \quad (4.36)$$

Where $\vec{S}_c$ in eq. 4.17 simplifies to:

$$\vec{S}_c = \left(-\frac{3k_B T_{c0}}{2} \right) \left(\frac{\pm \vec{J}_c}{q} \right) \quad (4.37)$$

Using eq. 4.37 in eq. 4.36 leads to eq. 4.38 showing the relation of initial average kinetic energy with electric field due to energy bands $\left(\frac{\nabla E_{(c,v)}}{q} \right)$.

$$\nabla \cdot \left[\left(-\frac{3k_B T_{c0}}{2} \right) \left(\frac{\pm \vec{J}_c}{q} \right) \right] = \vec{J}_c \cdot \frac{\nabla E_{(c,v)}}{q} \quad (4.38)$$

4.5 Sources of Mobility degradation and models used for their calculation

Mobility of electrons and holes is a key parameter in the performance of transistors, and therefore, CMOS inverters. The difference in mobility of carriers are one of the main reasons for the asymmetry in I-V characteristics of n- and p-FETs [1, 32]. Therefore, Philips mobility model ($\mu_{i,PhuMob}$), enormal model ($\mu_{i,enormal}$), and high field saturation ($\mu_{i,HFE}$) model have been used for accurate calculation of carrier mobility, where i is electron or hole. Mattheisen's rule eq. 4.39 is used to calculate the overall carrier mobility ($\mu_{i,Tot}$) by combining the resultant mobility due to degradations, using different mobility models [11, 75]:

$$\frac{1}{\mu_{(i,Tot)}} = \frac{1}{\mu_{(i,PhuMob)}} + \frac{D}{\mu_{(i,enormal)}} + \frac{1}{\mu_{(i,HFE)}} \quad (4.39)$$

Where D can be found using eq. 4.40:

$$D = \exp\left(\frac{-y}{10^{-6}cm}\right) \quad (4.40)$$

With y to be the distance from the oxide/semiconductor interface.

4.5.1 Philips mobility model (PhuMob)

Philips mobility model (PhuMob) considers the mobility degradation caused by temperature, donor concentration (N_D), acceptor concentration (N_A), and electron-hole scattering. PhuMob is derived from a fit to the experimental results obtained by Massetti et al [75]. The range of mobility, considering every type of scattering, for electrons (μ_e) and holes (μ_h) in silicon are $52.2 \frac{cm^2}{Vs}$ - $1417 \frac{cm^2}{Vs}$ and $44.9 \frac{cm^2}{Vs}$ - $470.5 \frac{cm^2}{Vs}$, respectively. The overall mobility in PhuMob (eq. 4.41) depends on three terms, (i) mobility due to lattice temperature ($\mu_{(i,T)}$), (ii) mobility due to ionised dopants ($\mu_{(i,I)}$), and (iii) electron-hole scattering ($\mu_{(i,e-h)}$) [11, 75].

$$\frac{1}{\mu_{(i,PhuMob)}} = \frac{1}{\mu_{(i,T)}} + \frac{1}{\mu_{(i,I)}} + \frac{1}{\mu_{(i,e-h)}} \quad (4.41)$$

Average thermal energy ($\frac{3}{2}k_B T_L$) of Si atoms, contributing to lattice vibration, changes as a function of lattice temperature (T_L). The absorbed thermal energy by the atoms increases their displacement amplitude, resulting in an increase in electron-phonon scattering rate [142]. Eq. 4.42 is obtained by fitting the experimental results of mobility ($\mu_{(i,T)}$) as a function of temperature [11, 136].

$$\mu_{(i,T)} = \mu_{(i,max)} \left(\frac{T_L}{300K} \right)^{-c_i} \quad (4.42)$$

Where $\mu_{(i=e,max)} = 1417 \frac{cm^2}{Vs}$, $\mu_{(i=h,max)} = 470.5 \frac{cm^2}{Vs}$, $c_{i=e} = 2.5$, and $c_{i=h} = 2.2$.

N- and p-type conventional FETs are formed by adding dopant atoms to the semiconductor [4]. However, the Coulomb electric field of the ionised dopants repulses the

4.5. SOURCES OF MOBILITY DEGRADATION AND MODELS USED FOR THEIR CALCULATION

carriers, and therefore, deviate the carriers from their actual path [142]. Ionised impurity scattering effect, increases as the doping concentration increases [75, 143]. The reduced mobility due to this scattering for majority carriers as a function of donors ($N_{I=D}$), acceptors ($(N_{I=A})$), electron concentration (n), and hole concentration (p) in the channel can be calculated using equation 4.43 [11, 75].

$$\mu_{(i,I)}(N_I, c) = \left(\frac{\mu_{max}^2}{\mu_{max} - \mu_{min}} \right) \left(\frac{N_{(ref,i)}}{N_I} \right)^{\alpha_1} + \left(\frac{\mu_{min}\mu_{max}}{\mu_{max} - \mu_{min}} \right) \left(\frac{n+p}{N_I} \right) \quad (4.43)$$

At $N_I = N_D = N_A = 0$, $\mu_{(i,I)} = \infty$; which means that contribution of ionised impurity scattering in equation 4.41 is zero. Table 4.2 summarises the constants used in eq. 4.43.

Table 4.2: Table of constants for $\mu_{i,I}$ of Si doped by Arsenic, Phosphorus, or Boron [75].

Parameter (unit)	Arsenic	Phosphorus	Boron
$\mu_{min}(\frac{cm^2}{Vs})$	52.2	68.5	44.9
$\mu_{max}(\frac{cm^2}{Vs})$	1417	1414	470.5
$N_{ref}(cm^3)$	9.68×10^{16}	9.20×10^{16}	2.23×10^{17}
α_1	0.68	0.711	0.719

Mobility of minority carriers due to ionised impurity scattering can be found using the following relation [75]:

$$G(P) = \frac{\mu_{majority}}{\mu_{minority}} \quad (4.44)$$

Where,

$$G(P_c) = 1 - \frac{0.89233}{\left(0.41372 + \left(\frac{m_0}{m_c^*} \frac{T}{300} \right)^{0.28227} P_c \right)^{0.19778}} + \frac{0.005978}{\left(\left(\frac{m_c^*}{m_0} \frac{300}{T} \right)^{0.72169} P_c \right)^{1.80618}} \quad (4.45)$$

and

$$P_c = \frac{1.36 \times 10^{20}}{n+p} \left(\frac{m_c^*}{m_0} \right) \left(\frac{T}{300} \right)^2 \quad (4.46)$$

The attractive force between the electrons and holes results in having another type of scattering in the channel, electron-hole scattering. Majority carriers, electrons (holes), in

the channel see the holes (electrons) as donors (acceptors) in which they can collide with. To be able to estimate $\mu_{(i,e-h)}$ (eq. 4.47 and eq. 4.48), one has to assume that the donor (acceptor) concentration for the electrons (holes) as majority carriers are equal to the concentration of minority carriers in eq. 4.43. The mobility degradation due to $\mu_{(i,e-h)}$ is the product of $\mu_{(i,I)}$ with $F(P_c)$. F is analytical fit of experimental data for $\frac{m_c^*}{m_j^*}$ variation, where j is the minority carrier [75].

$$\mu_{(e,e-h)}(N_D, c) = F(P_n) \mu_{(e,D)}(N_D = p, c) \quad (4.47)$$

and,

$$\mu_{(h,e-h)}(N_A, c) = F(P_p) \mu_{(h,A)}(N_A = n, c) \quad (4.48)$$

Where,

$$F(P_c) = \frac{0.7643P_c^{0.6478} + 2.2999 + 6.5502\frac{m_c^*}{m_j^*}}{P_c^{0.6478} + 2.3670 - 0.01552\frac{m_c^*}{m_j^*}} \quad (4.49)$$

4.5.2 Enormal model

Carriers in the channel undergo an influence of two electric fields. One longitudinal due to V_{ds} and one transverse due to V_{gate} . The MOS capacitor of the FET accumulate or deplete carriers at the semiconductor/ SiO_2 interface by generating an electric field perpendicular to the motion of carriers (enormal). Enormal ($E_{\perp}$) deviates the motion of carriers, from the longitudinal direction, toward the semiconductor/ SiO_2 interface leading to surface roughness ($\mu_{(sr)}$) and acoustic phonon ($\mu_{(sph)}$) scattering. Analytical formulas for $\mu_{(sph)}$ (eq. 4.50) and $\mu_{(sr)}$ (eq. 4.51) are [11, 144]:

$$\mu_{sph} = \frac{B}{E_{\perp}} + \frac{C \left(\frac{(N_A + N_D + N_2)}{N_0} \right)^{\lambda}}{E_{\perp}^{\frac{1}{3}} \left(\frac{T}{300K} \right)^k} \quad (4.50)$$

4.5. SOURCES OF MOBILITY DEGRADATION AND MODELS USED FOR THEIR CALCULATION

$$\mu_{sr} = \left(\frac{\left(\frac{E_{\perp}}{E_{ref}} \right)^{A_i^*}}{\delta} + \frac{E_{\perp}^3}{\eta} \right)^{-1} \quad (4.51)$$

Where,

$$A_h^* = A + \frac{\alpha_{(\perp)} p N_{ref}^v}{(N_A + N_D + N_1)^v} \quad (4.52)$$

and

$$A_e^* = A + \frac{\alpha_{(\perp)} n N_{ref}^v}{(N_A + N_D + N_1)^v} \quad (4.53)$$

Table 4.3: Fitting parameters based on experiments for μ_{sph} and μ_{sr} of Silicon [11].

Parameter (unit)	Electrons	Holes	Parameter (unit)	Electrons	Holes
A(1)	2	2	$N_{ref}(\text{cm}^{-3})$	1	1
$B(\frac{cm}{s})$	4.75×10^7	9.925×10^6	$E_{ref}(\frac{V}{cm})$	1	1
$C \left(\frac{cm^{\frac{5}{3}}}{V^{\frac{2}{3}} s} \right)$	5.8×10^2	2.947×10^3	$\lambda(1)$	0.125	0.0317
$N_0(\text{cm}^{-3})$	1	1	$\alpha_{\perp}(\text{cm}^{-3})$	0	0
$N_1(\text{cm}^{-3})$	1	1	$\delta \left(\frac{cm^2}{Vs} \right)$	5.82×10^{14}	2.0546×10^{14}
$N_2(\text{cm}^{-3})$	1	1	$\eta \left(\frac{V^2}{cms} \right)$	5.82×10^{30}	2.0546×10^{30}

4.5.3 High field saturation (HFE) model

Experimental results show that the linear relation ($v_i = \mu_i E$ [4, 145]) of electric field (E) with velocity of electrons (v_e) and holes (v_h) with respect to constant mobility (μ_i) hold solely for $E = E_{Low} < 10^4 \frac{V}{cm}$ in Si [146]. At high electric field ($E = E_{high} \geq 10^4 \frac{V}{cm}$), the gained energy due to E balances with the energy loss caused by electron-phonon scattering [145]. As the result, mobility degrades, and velocity of electrons ($v_{(e0,sat)}$) and holes ($v_{(h0,sat)}$) at 300 K in Si saturates at approximately $1.0 \times 10^7 \frac{cm}{s}$ and $8 \times 10^6 \frac{cm}{s}$, respectively [11, 147, 148]. Mobility degradation model as a function of E ($\mu_{(i,E)}$) has been derived based on experimental results, and shown in eq. 4.54 [11]. The field dependence

of mobility ($\mu_{i,E}$) becomes significant at $E = E_{high} \geq 10^4 \frac{V}{cm}$, where the temperature of carriers as a function of E is sufficient to impact the mobility. Therefore, $E (= E_{Low}) < E_{high}$ is assumed to be zero in this model, which leads to no mobility degradation ($\mu_{(i,E)} = \mu_{(i,E_{low})}$) as a function of E [11, 149].

$$\mu_{(i,E)}(E) = \frac{(\alpha + 1)\mu_{(i,E_{Low})}}{\alpha + \left(1 + \left(\frac{(\alpha+1)\mu_{(i,E_{Low})}E}{v_{(i,sat)}}\right)^\beta\right)^{\frac{1}{\beta}}} \quad (4.54)$$

Where,

$$\beta(T) = \beta_0 \left(\frac{T}{300K}\right)^{\beta_c} \quad (4.55)$$

and

$$v_{(i,sat)}(T) = v_{(i0,sat)} \left(\frac{300K}{T}\right)^{v_{sat_c}} \quad (4.56)$$

Table 4.4: Parameters based on experiments for $\mu_{(i,E)}$, β , and $v_{(i,sat)}$ of Si [11].

Parameter (unit)	Electrons	Holes		Parameter (unit)	Electrons	Holes
$\alpha(1)$	0	0		$\beta_c(1)$	0.66	0.17
$\beta_0(1)$	1.109	1.213		$v_{sat_c}(1)$	0.87	0.52

4.6 Boundary conditions

Thermal and electrical behaviours are defined by thermode and electrode in Sentauros. The temperature and surface thermal resistance of the thermode can be set to a constant value. In this work, surface thermal resistance of the thermodes is negligible. The electrode, unless otherwise specified, maintains equilibrium for the defined Ohmic or Schottky contact. At equilibrium, charge neutrality is assumed for an Ohmic contact, leading to a flat band in case of electrode/semiconductor interface; while band bending

occurs for Schottky contact, as shown in eq. 2.5. The calculations of electron density (eq. 4.8), hole density (eq. 4.9), and electrostatic potential (eq. 4.10) at the interface of the Schottky contact have already been discussed at section 4.1. Electrodes are also used as electrical contacts on insulators, as for gates (section 4.3). In this work, two contacts are placed at both ends of the nanowire, acting as both Schottky electrodes and thermodes; and a contact is placed as Ohmic electrode of the gate. No resistive voltage drop is assumed across the defined Schottky, Ohmic, or Ohmic on insulator electrodes [150].

Similar to [151], there are no heat loss/leak, due to convection or radiation, from the studied TEGs to the ambient or load resistor. Although heat transfer among different regions of the TEG is considered in the simulations, temperature loss of the semiconductor to SiO_2 is negligible. Low heat loss of the semiconductor to the SiO_2 is due to thin thickness of the simulated oxide ($=8$ nm) for the TEGs. Similar to [76], SiO_2 is mainly used as a gate insulator for TEGs. Increasing the oxide thickness (gate insulator) would reduce the electrical conductivity and increase heat transfer from the semiconductor to the oxide. The generated output power in studied TEGs degrades, if solely oxide thickness increases, while metal gate work function, voltage biases ($= 0$ V), and other dimensions remain unchanged.

4.7 Summary

Sentaurus TCAD is a powerful tool to design and simulate the performance of current and new devices. It has an extensive library of physics, based on experimentally verified models that ensure the different processes influencing the carrier can be realistically simulated.

When simulating nano-scale devices, the hydrodynamic model must be used to take drift, diffusion, temperature of carriers, temperature of lattice, scatterings, and

environmental parameters into account.

RECONFIGURABLE NANOWIRE TRANSISTORS WITH BRIDGED PROGRAM GATES

Complementary metal oxide semiconductors (CMOS) are one of the key elements of digital circuits. Combinations of CMOS inverters with AND logic gates can build all other logic gates in digital circuits [152]. Low supply voltage requirement, high frequency performance, and linear transition region of this device have motivated researchers to use CMOS in analog circuits. Other than being a NOT gate in digital circuits, analog circuits use CMOS inverters as buffers [153], amplifiers [154–156], output drivers [155], transconductors [157], comparators [156, 158, 159], and delay elements [160]. Implementation of CMOS inverters have improved analog-to-digital conversion for radio frequency and ethernet [158], biosensing [161], and signal receivers for healthcare and biomedical systems [162, 163]. Further CMOS optimisations or introduction of new designs are vital for the creation of new opportunities of using these devices in other applications [155]. The design or optimisation of CMOS inverters are highly dependent on the application. As an example, analog circuits require linear transition region, whereas logic circuits need steep transition region for high accuracy of

representing binary numbers [157].

Conventional CMOS inverters contain n- and p-doped field effect transistors (FETs) using a single power supply [1]. Due to difference in mobility electrons and holes [31], symmetric I-V characteristic could not be achieved with the same geometry of n- and p-FET. Strategies for symmetric conventional n- and p-FETs included having un-equal gate and channel lengths [164], contacts with different work functions [30], different channel materials for n- and p-FET [152, 164], and different doping profiles [30]. However, due to down-scaling of transistors for further continuation of Moore's law, obtaining uniform and accurate doping profiles for each unit of CMOS is challenging. Therefore, un-doped gated structures seems to be a better option for lower gate length CMOS technologies. Silicon reconfigurable nanowire field effect transistors (Si RNW-FETs) have attracted the attention of researchers, as the channel of these FETs are intrinsic. Symmetric I-V characteristics of n- and p-modes in Si RNW-FETs were achieved by compressive strain engineering [32].

In this chapter, Sentarus TCAD software [11] is used to design a CMOS inverter with a flexible fabrication process using two Si RNW-FETs without the need for strain engineering.

This chapter is organised as follows. Section 5.1, discusses the model evaluation and calibration methodology. Section 5.2, studies the effect of having dissimilar gates for n- and p-FETs on their characteristic and forming symmetric I-V. Section 5.3, introduces the novel capacitive bridged method to form symmetric characteristic for n- and p-FET. Section 5.4, performance differences between asymmetric gates and the bridged method. Section 5.5, shows the fabrication process of the bridged method, and explains the impact of subsequent process on the bridged method. Section 5.6, studies the effect of fabrication errors on performance of bridged method. Section 5.7, concludes the findings.

5.1 Model evaluation and calibration

In order to evaluate the accuracy of the simulations, a previously experimented device must be simulated to evaluate the used models and their parameters. Since silicon substrate with $\langle 100 \rangle$ orientation were used in this work, only experiments with $\langle 100 \rangle$ orientation of Si can be used for evaluation/calibration. Previously, De Marchi [165] have fabricated a polarity controllable transistor, containing four stacks of Si $\langle 100 \rangle$ nanowires. Fig 5.1 (a) shows the optimised fabricated p-type ($1 \times 10^{-15} \text{ cm}^{-3}$) nanowire stacks with dissimilar diameters in [165]. The diameters of the Si NWs are estimated to be around 10 nm, using the 100 nm scanning electron microscopy (SEM) image bar. Fig 5.1 (b) shows the deposited poly-silicons used as program gates (PG), after 5 nm to 8 nm growth of SiO_2 via thermal oxidation. The length of the nanowire stacks and program gates are estimated, using the 200 nm SEM bar in fig 5.1 (b). Fig 5.1 (c) shows the deposited control gate (CG), after 5 nm to 8 nm of oxide growth. The second thermal oxidation is done to isolate the program gates from the control gate. Finally, nickel is deposited and then annealed, to form a NiSi with 0.45 eV barrier for holes [165].

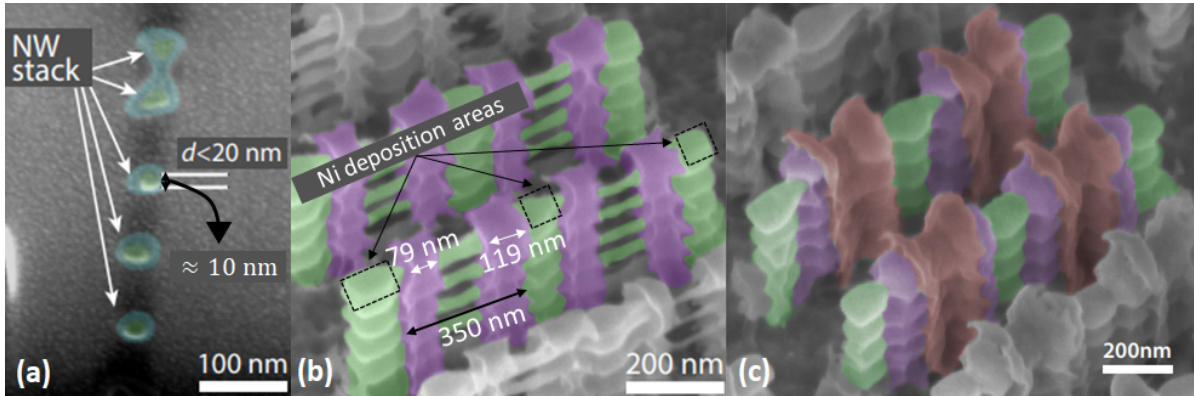


Figure 5.1: (a) SEM image of optimised nanowire stacks [165]. (b) Image of the device after program gate deposition [165]. (c) Image of the device after control gate deposition using self aligned method [165].

Fig 5.2 (a) shows a single nanowire, simulated to evaluate the used model. Param-

ters of the simulated device are shown in table 5.1. The obtained drain current of the simulated device, as a function of control gate voltage (V_{CG}), is multiplied by four to predict the I-V characteristic of the fabricated device with four stacked NWs. Note that due to number of fluctuations and uncertainties in the fabricated device, the simulated device can't achieve exact I-V behaviour as the obtained experiment. The uncertainties and fluctuations are, (i) fluctuations in Si NW diameters, (ii) fluctuations in oxide thickness, covering the Si NWs, (iii) fluctuations in oxide thickness between the PG and CG, and (IV) fluctuations in the distance of the NiSi/Si interface from the gated regions.

Table 5.1: Parameters and values of the quantities in the simulated device shown in fig. 5.2 (a).

Quantity	parameter values and units
SiO_2 relative permittivity	3.9
Si band gap	1.12 eV
Si electron affinity	4.07 eV
Si electron mobility	1400 $\frac{cm^2}{Vs}$
Si hole mobility	470.5 $\frac{cm^2}{Vs}$
Schottky barrier height for electrons	0.67 eV
Schottky barrier height for holes	0.45 eV
Poly-Si band gap	1.169 eV
Poly-Si electron affinity	4.05 eV

Fig. 5.2 (b) shows the drain current (I_d) as a function of control gate voltage (V_{CG}), at different program gate voltages (V_{PG}). The ON current (I_{on}) of the simulated device approximately matches with that of the experimented transistor. However, the OFF current (I_{off}) of the simulated device deviates from the experimented transistor. Average I_{off} (I_{off}) for the experimented (simulated) transistor at n-mode is 6.74×10^{-11} A (6.61×10^{-12} A). In addition, the average I_{off} (I_{off}) for the experimented (simulated) transistor at p-mode and $V_{PG} = 0$ V is 1.55×10^{-10} (2.14×10^{-10} A); and for experimented (simulated) p-mode at $V_{PG} = -2$ V are 1.06×10^{-10} A (8.88×10^{-10} A). Although I_{off} for experimented and simulated transistors are dissimilar, the range of these differences

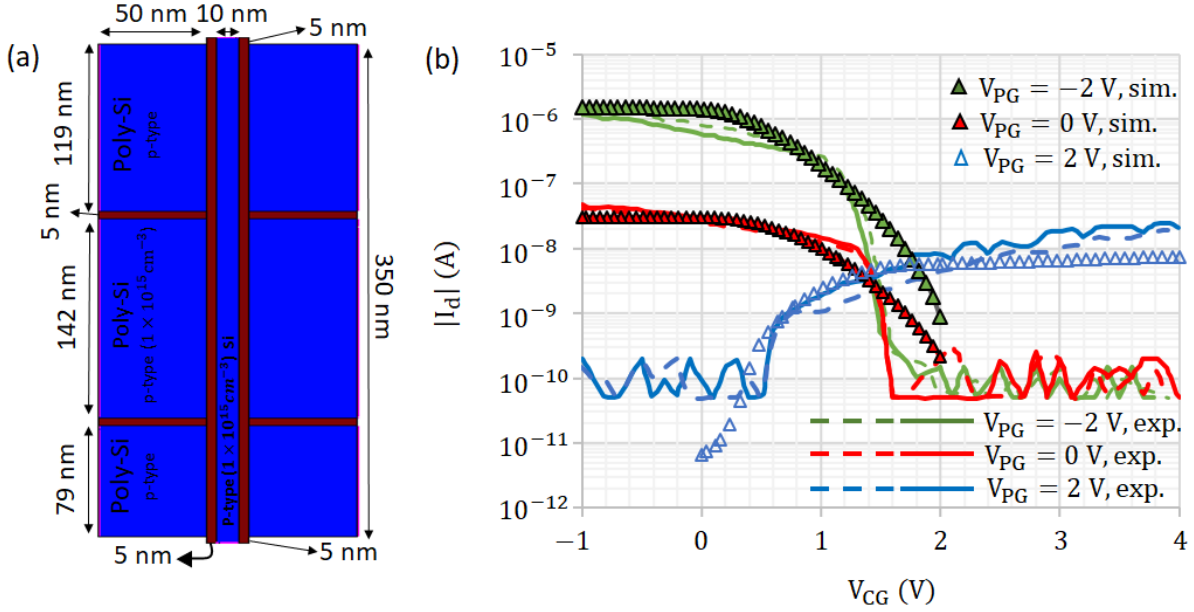


Figure 5.2: (a) Schematic of the simulated nanowire with 2D source and drain metal contacts, to predict the experimental results shown in [165]. (b) The drain current (I_d) as a function of control gate voltage (V_{CG}) for the simulated (sim.) structure and the experimented (exp.) device in [165]. I_d - V_{CG} is shown for different program gate voltages (V_{PG}); and constant drain voltage (V_d) of 2V, for all the of the shown results.

are in the order of previously reported simulations, for other experiments (fig. 5.3).

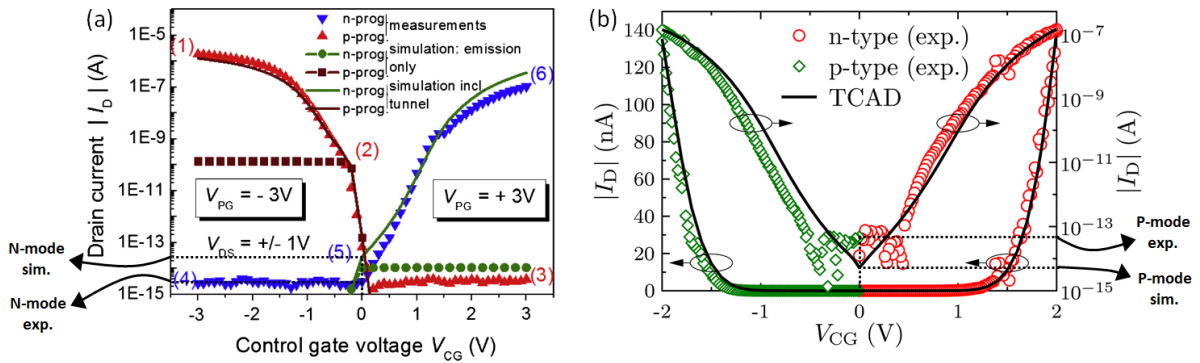


Figure 5.3: (a) shows both the simulations and experiments for Si based RNWs with (a) $\langle 112 \rangle$ orientation channel [1], and (b) strained $\langle 110 \rangle$ orientation channel [27].

Although $V_{PG} > 2$ V is not used in this work, it worth noting that the used model under-estimates short channel effect at high program gate voltages ($V_{PG} \geq 4$ V).

5.2 Asymmetric gates for n-FET and p-FET

Fig. 5.4 shows the simulated double gated Si RNW-FETs with $L_{Gn} = 20$ nm and $L_{Gp} = 43$ nm for n-FET and p-FET, where L_{Gn} and L_{Gp} are gate lengths of n-FET and p-FET, respectively. Carrier type is defined by program gate (PG_n for n-FET and PG_p for p-FET) at the channel/drain interface. The injection of carriers is controlled by a control gate (CG_n for n-FET and CG_p for p-FET) placed at source/channel interface. The square shaped core structure with 10 nm sides is formed by contacting 100 nm of $NiSi_2$ at both ends of a 145 nm long intrinsic Si beam. The core structure with two Schottky contacts is then covered with 8 nm of SiO_2 and 20 nm of metal gates (titanium). The distance between the FETs (L_d) is constant and equal to 91 nm. The work functions of Ti and $NiSi_2$ are set to 4.63 eV and 4.65 eV, respectively [27]. In this part of the investigation,

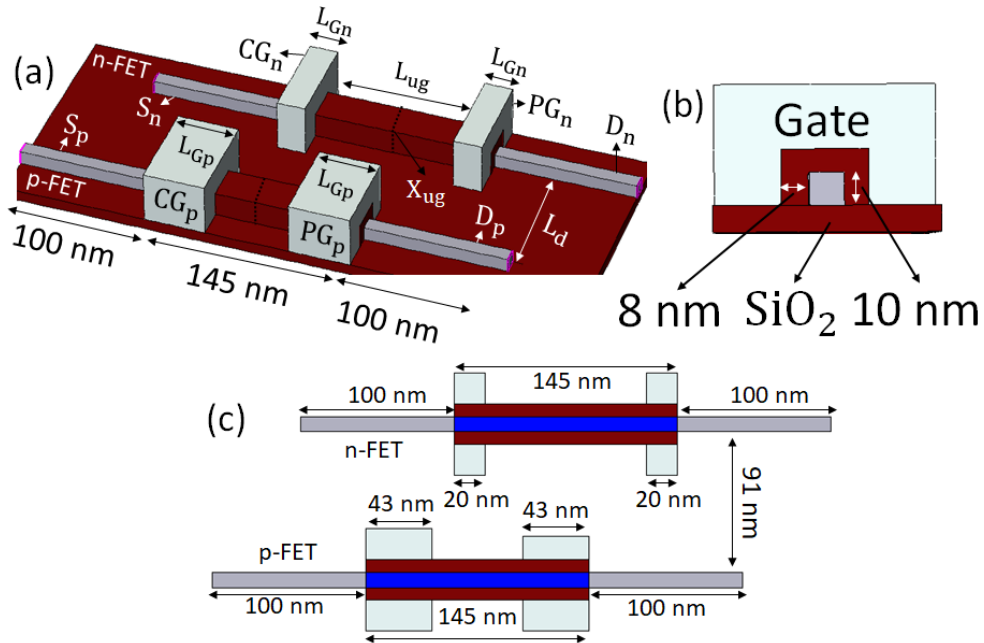


Figure 5.4: (a) 3D view and (b) front view of simulated Si RNW-FETs with $L_{Gn} = 20$ nm and $L_{Gp} = 43$ nm gate lengths for n-FET and p-FET respectively. (c) Cross section of FETs shown in (a). L_{ug} is length of un-gated region. S_n , S_p , D_n , and D_p are n-FET source, p-FET source, n-FET drain, and p-FET drain respectively. Online colour: Light blue regions are the Ti gates, burgundy is SiO_2 , the grey areas are the $NiSi_2$ contacts, dark blue is intrinsic Si.

gate lengths of n-FET (L_{Gn}) is dissimilar to p-FET gate lengths (L_{Gp}), to compensate for the difference in electron and hole mobility.

Fig. 5.5 (a) shows the conduction band of the simulated n-FET Si RNW with four different gate lengths and $V_{CGn} = V_{PGn} = 2V$ and $V_{dn} = 0V$, where V_{CGn} , V_{PGn} , and V_{dn} are voltages of control gate, program gate, and drain; while $L_{Gp} = 43$ nm.

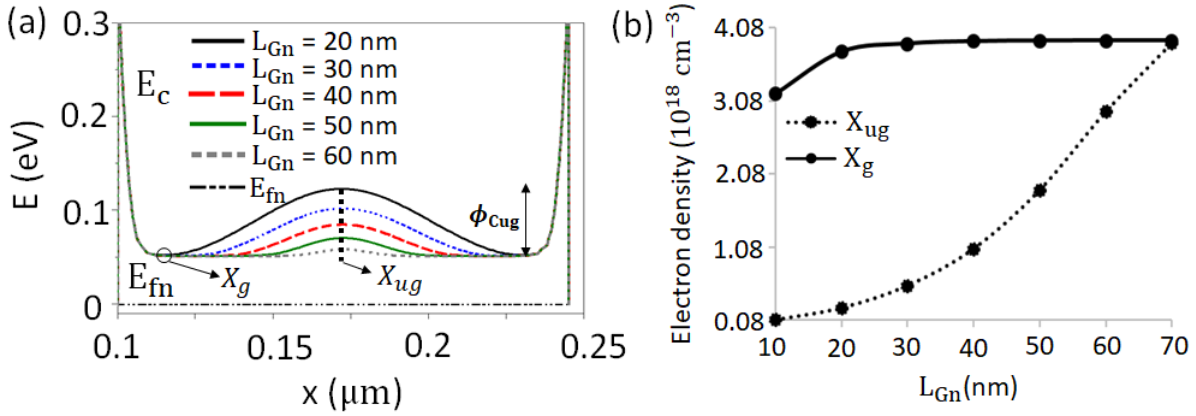


Figure 5.5: (a) Conduction band (E_c) along the the length of the n-FETs with L_{Gn} : 20 nm, 30 nm, 40 nm, 50 nm, and 60 nm. (b) Carrier concentration- L_{Gn} at the centre of gated region (X_g) and at un-gated region (X_{ug}). E_c and carrier concentration of n-FETs are plotted in the middle of the channel along x . E_{fn} is the Fermi level of the n-FETs. ϕ_{cug} is the height of the potential barrier. N-FETs are at $V_{PGn} = V_{CGn} = 2$ V and $V_{dn} = 0$ V.

From fig 5.5 (a), we observe that the width and height of the potential barrier ϕ_{cug} at $x = X_{ug}$ increases as the gate length L_{Gn} decreases. Due to L_{Gn} reduction, the length of the un-gated region (L_{ug}) increases. Consequently, thermionic emission and tunneling probability at the centre of the n-FET's channel for carriers with lower gate length reduces. Therefore, the ON current of the n-FET reduces at shorter gate lengths. Fig 5.5 (b) shows that the carrier concentration in the middle of un-gated regions (X_{ug}) approaches the gated regions (X_g) as gate length of n-FET (L_{Gn}) increases. This behaviour is the same for p-FET.

Symmetric I-V characteristics of n-FET and p-FET with dissimilar gate lengths, $L_{Gn} = 20$ nm and $L_{Gp} = 43$ nm, are shown in fig 5.6 (a) and (b). Although approximately

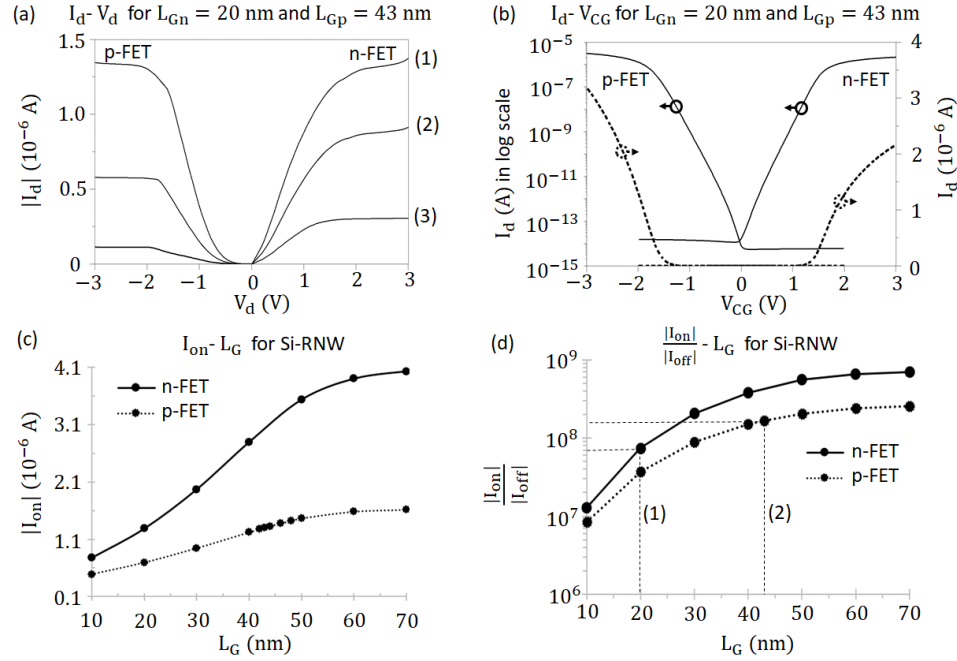


Figure 5.6: (a) I_d - V_d graph for n-FET and p-FET at $|V_{PGn,p}| = 2$ V and (1) $|V_{CGn,p}| = 2$ V, (2) $|V_{CGn,p}| = 1.75$ V, (3) and $|V_{CGn,p}| = 1.5$ V, where $V_{PGn,p}$, $V_{CGn,p}$, and $V_{dn,p}$ are the program gate, control gate, and drain voltage of n- and p-FETs, respectively. (b) I_d - V_{CG} with $|V_{PGn,p}| = |V_{dn,p}| = 2$ V. (c) I_{on} - L_G for both FETs at $|V_{PGn,p}| = |V_{CGn,p}| = |V_{dn,p}| = 2$ V. (d) $\frac{I_{on}}{I_{off}}$ - L_G for both modes. I_{on} and $\frac{I_{on}}{I_{off}}$ for n-FET with $L_{Gn} = 20$ nm and p-FET with $L_{Gp} = 43$ nm are shown by lines (1) and (2), respectively. L_{Gn} (L_{Gp}) in (c) and (d) is varied while $L_{Gp} = 43$ nm ($L_{Gn} = 20$ nm), respectively.

equal I_{on} is achievable, this method has two weaknesses, (i) I_{on} as a function of L_{Gp} saturates for $L_{Gp} > 60$ nm (fig. 5.6 (c)) as carrier concentration at X_g approaches that at X_{ug} (fig. 5.5 (b)), (ii) the requirement of dissimilar gate lengths leads to dissimilar $\frac{I_{on}}{I_{off}}$ (fig. 5.6 (d)). In addition, as seen in fig. 5.4 (c) the gate length of the p-FET needs to be approximately 2.15 times longer than the n-FET, to achieve symmetric I-V. Due to high $\frac{L_{Gp}}{L_{Gn}}$ ratio, the process control complexity of metal gate fabrication increases as transistors down-scale; especially for sub-10 nm gate length technology regime. As an example, for $L_{Gp} = 7$ nm (28 Si atom long [7]), L_{Gn} must be approximately 3.25 nm (13 Si atoms long [7]). 3.75 nm gate length difference between n- and p-FETs require introduction of additional strategies to design, to achieve comparable I_{off} . A study on

n-type GaN-based transistors have shown 325 times increase in I_{off} when gate length is reduced by only 4 nm, from 10 nm to 6 nm [166].

5.3 Bridging the program gates of the p-FET

In this approach, oxide bridges are introduced between the n-FET and p-FET with equal gate lengths ($L_{Gn} = L_{Gp} = L_G$), fig. 5.7 (a). The oxide bridges connect the PG of the FET with lower mobility (p-FET) at $x = X_{ug}$ of the FET with higher mobility (n-FET). The capacitive behaviour of the PG_p /oxide/i-Si controls the flow of carriers in the channel of the FET with higher ON current. As bias voltages are applied to PG_n ($V_{PG_n} > 0$ V) and PG_p ($V_{PG_p} < 0$ V) to define the carrier type of FETs, potential barriers are formed at $x = X_{ug}$ in the n-FET. Similar to section 5.2, the $NiSi_2$ (100 nm)/i-Si(145 nm)/ $NiSi_2$ (100 nm) core structure is formed on an SiO_2 layer. The channel is wrapped by 8 nm of SiO_2 and 20 nm of Ti. L_d is constant and equal to 91 nm. The potential barrier height and width are controlled by the bridge width (W_{ox}) and length (L_{ox}). To better understand the effect of gate length on potential barrier's width and height, simulations are done for two gate lengths: $L_{Gn} = L_{Gp} = L_G = 30$ nm and 40 nm.

Generally, the electron (hole) concentration in the channel of the un-bridge n-(p-)FET

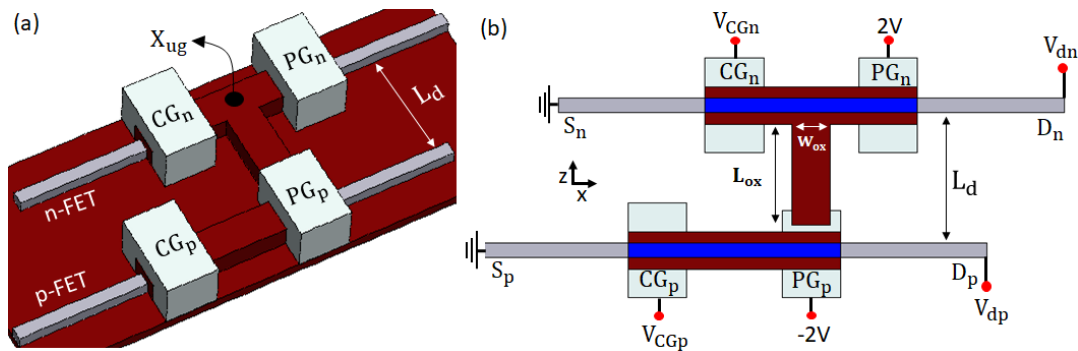


Figure 5.7: (a) 3D and (b) cross section of bridged method. Online colour: Light blue regions are the Ti gates, burgundy is SiO_2 , the grey areas are the $NiSi_2$ contacts, dark blue is intrinsic Si.

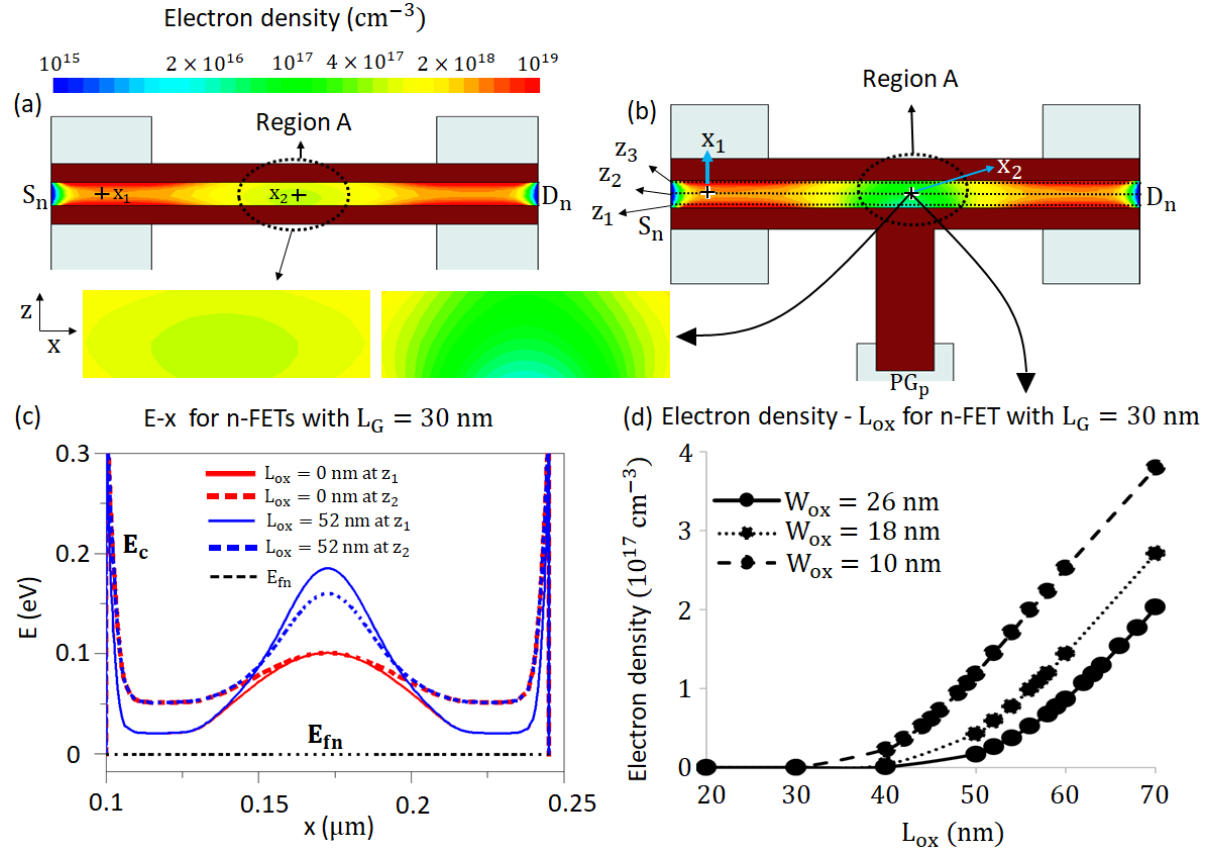


Figure 5.8: (a) Carrier concentration of the un-bridged n-FET with $L_G = 30$ nm when $V_{PG_n} = V_{CG_n} = 2$ V and $V_{d_n} = 0$ V, (b) carrier concentration of the bridged n-FET with $L_G = 30$ nm, $L_{ox} = 52$ nm, and $W_{ox} = 18$ nm when $V_{CG_n} = V_{PG_n} = 2$ V, $V_{d_n} = V_{d_p} = 0$ V, and $V_{PG_p} = -2$ V. (c) Conduction band (E_c) along x-direction for the un-bridged (red) and bridged (blue) n-FETs shown in (a) and (b). (d) The electron density of n-FET with $L_G = 30$ nm in (x_2, z_2) under the $PG_p/SiO_2/i$ -Si capacitor as a function of W_{ox} and L_{ox} at same bias as in (b).

is higher in gated (x_1) than un-gated (x_2) areas when $|V_{CG}| > 0$ (fig. 5.8 (a)). The electron concentration at x_1 and x_2 (region A) of the un-bridged FET with $L_G = 30$ nm (fig. 5.8 (a)) when $V_{PG_n} = V_{CG_n} = 2$ V and $V_{d_n} = 0$ V are 3.85×10^{18} cm⁻³ and 5.72×10^{17} cm⁻³, respectively.

Introduction of the bridge further reduces the carrier concentration at region A (fig. 5.8 (b)). Since the bridge is connected to only one side of the n-FET, gradual increase in carrier concentration occurs starting from z_1 to z_3 . Therefore, a higher barrier height is

faced by electrons at z_1 compared to z_3 . Fig. 5.8 (c) shows higher barrier for the bridged n-FET than un-bridged at (x_2, z_1) and (x_2, z_2) . The slight inhomogeneous behaviour in fig 5.8 (a) for un-bridged n-FET is due to the parasitic capacitance between neighbouring transistors.

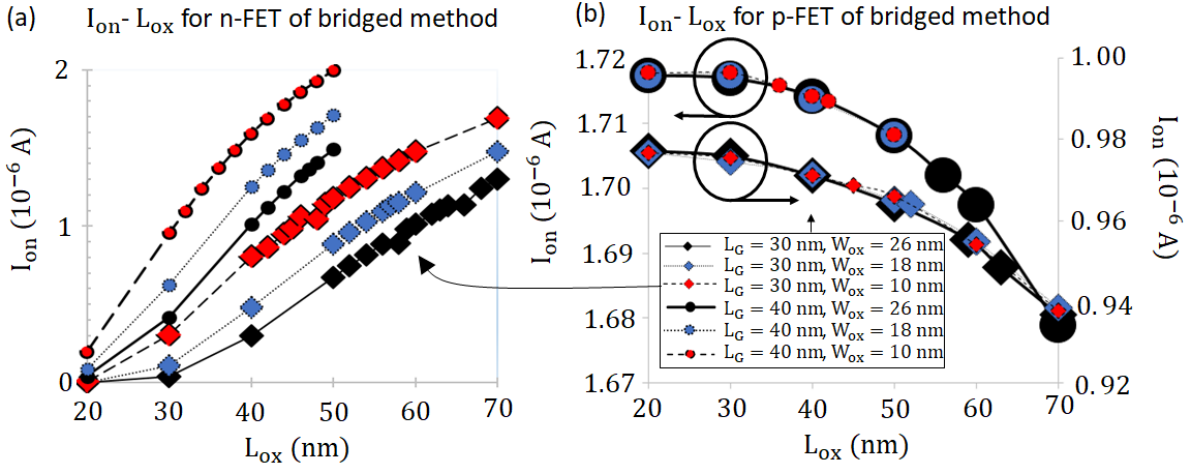


Figure 5.9: (a) I_{on} - L_{ox} for the bridged n-FET with $L_G = 30$ nm (diamond) and $L_G = 40$ nm (circle) at $V_{CG_n} = V_{PG_n} = V_{d_n} = 2$ V and $V_{PG_p} = -2$ V; and (b) I_{on} - L_{ox} for the bridged p-FET with $L_G = 30$ nm (diamond) and $L_G = 40$ nm (circle) at $V_{CG_p} = V_{PG_p} = V_{d_p} = -2$ V and $V_{PG_n} = 2$ V. The positions of n-FET and p-FET are shown in fig 5.7 (a).

Fig. 5.8 (d) shows carrier concentration of the bridged n-FET with $L_G = 30$ nm as functions of W_{ox} and L_{ox} . It can be seen that higher L_{ox} is required for shorter W_{ox} to reach to a certain carrier concentration.

Fig. 5.9 (a) shows the ON current of the bridged n-FETs with $L_G = 30$ nm, and 40 nm as a function of L_{ox} and W_{ox} when $V_{CG_n} = V_{PG_n} = V_{d_n} = 2$ V and $V_{PG_p} = -2$ V. Reducing L_{ox} of $PG_p/SiO_2/i$ -Si capacitor, depletes the electron concentration at region A (fig. 5.8 (d)) and therefore reduces the ON current for the n-FET. The bridged method offers high flexibility in fabrication process, since symmetry can be achieved through different combinations of W_{ox} , L_{ox} , or L_G . In addition, the slight increase of p-FET's ON current (fig 5.9 (b)) is due to the following reasons, (i) parasitic capacitance between the PG_p and centre of the p-FET's channel as L_{ox} reduces and length of PG_p increases, and (ii)

parasitic capacitance between the neighbouring transistors.

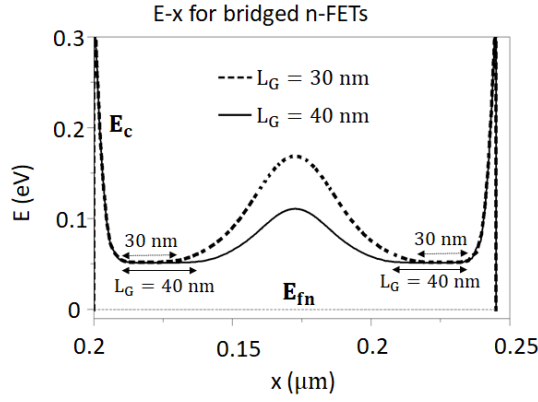


Figure 5.10: E_c along x-direction of the bridged n-FET channel for $L_G = 30$ nm and 40 nm. Both FETs have $L_{ox} = 50$ nm and $W_{ox} = 18$ nm when $V_{CG_n} = V_{PG_n} = 2$ V, $V_{d_n} = 0$ V, and $V_{PG_p} = -2$ V.

Fig. 5.10 shows the conduction band of the bridged n-FETs with $L_G = 30$ nm and 40 nm along the length of the channel crossing z_1 , both have equal $L_{ox}(= 50$ nm) and $W_{ox}(= 18$ nm). A lower potential barrier is seen for $L_G = 40$ nm than $L_G = 30$ nm, as longer gate lengths have higher control on carrier concentration of un-gated regions (L_{ug}).

Fig. 5.11 (a) & (b) shows symmetric n-FET and p-FET $I_d - V_d$ for the bridged method with $L_G = 30$ nm and 40 nm. Although symmetric $I_d - V_d$ (black lines) can be achieved by configuring the FETs as shown in fig. 5.11 (a), re-configuring the FETs lead to asymmetric n-FET and p-FET behaviour (grey lines). The impact of bridging is shown by comparing transfer characteristics (Fig. 5.11 (c) & (d)) of simulated bridged n-FET (solid line) and un-bridged n-FETs (dotted line) with reference to the p-FET. The left and right axes are I_d in logarithmic and linear scale, respectively. The right axis shows lower I_{on} for bridged compared to un-bridged n-FET, leading to alignment of slightly changed I_{on} of p-FET with bridged n-FET.

Fig. 5.12 compares the I_{on} for n- and p-FETs in bridged method ($L_G = 40$ nm, $W_{ox} = 18$ nm, $L_{ox} = 50$ nm) with Si RNW-FETs in previous works (shown in table 2.1) having equal gate lengths for n- and p-FET.

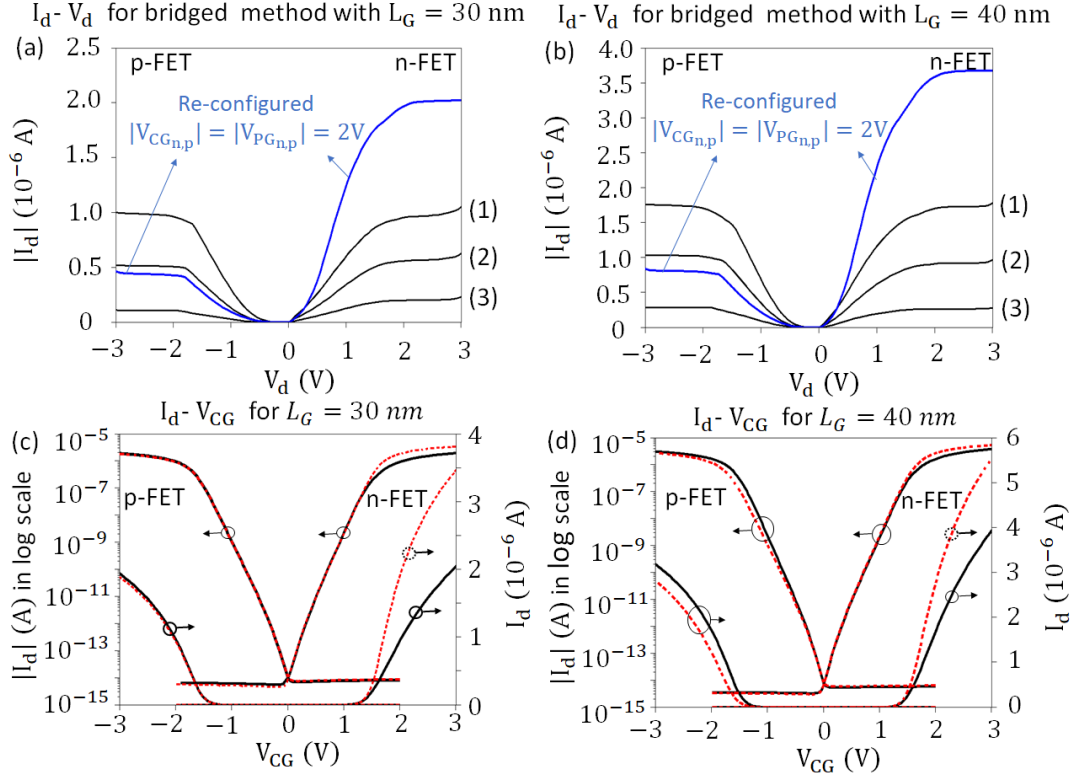


Figure 5.11: Output characteristic of n- and p-FET in bridged approach for (a) $L_G = 30$ nm, $W_{ox} = 18$ nm, $L_{ox} = 52$ nm; and (b) $L_G = 40$ nm, $W_{ox} = 18$ nm, $L_{ox} = 50$ nm when $|V_{PG_{n,p}}| = 2$ V and (1) $|V_{CG_{n,p}}| = 2$ V, (2) $|V_{CG_{n,p}}| = 1.75$ V, (3) and $|V_{CG_{n,p}}| = 1.5$ V. Transfer characteristic of n- and p-FET for (c) $L_G = 30$ nm and (d) $L_G = 40$ nm in bridged method (solid lines), and un-bridged n-FET (dotted lines) when $|V_{PG_{n,p}}| = |V_{d_{n,p}}| = 2$ V. $W_{ox} = 18$ nm, $L_{ox} = 52$ nm for bridged n-FET with $L_G = 30$ nm in (c); and $W_{ox} = 18$ nm, $L_{ox} = 50$ nm for bridged n-FET with $L_G = 40$ nm in (d).

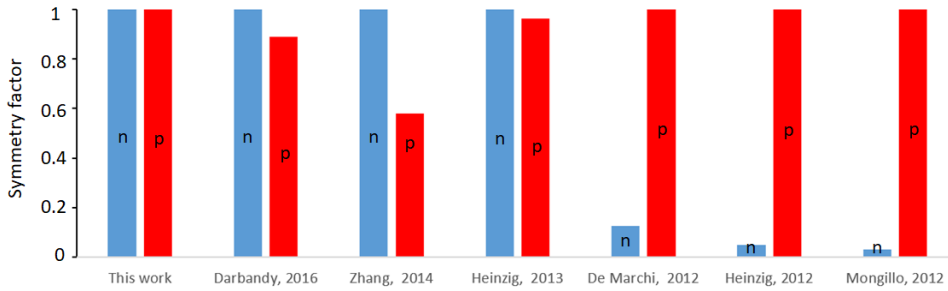


Figure 5.12: Comparing ON current symmetry factors for n- and p-FETs of this work with [27] (Darbandy, 2016), [29] (Zhang, 2014), [32] (Heinzig, 2013), [33] (De Marchi, 2012), [28] (Heinzig, 2012), and [34] (Mongillo, 2012) shown in table 2.1.

5.4 Physics and performance differences between asymmetric gates and the bridged method

As seen in fig. 5.5 (a) and 5.8 (c), both approaches form a barrier in the middle of the n-FET's channel, to compensate for the difference in electron and hole mobility. Since L_{Gp} ($= 43$ nm) of p-FET in the asymmetric gates method (fig. 5.4 (c)) has approximately similar gate length as the bridged method with $L_G = 40$ nm, E_c of their n-FETs to achieve I-V symmetry can be compared (fig 5.13). As a reference, E_c of n-FET in un-bridged method (red) with $L_{Gn} = L_{Gp} = 40$ nm is plotted. As seen in fig 5.13, the barrier height at the centre of the channel with $L_{Gn} = 20$ nm is either approximately equal (at z_1) or higher (at z_2) than the bridged method with $L_G = 40$ nm. This leads to lower thermionic emission of the carriers in un-bridged n-FET with $L_{Gn} = 20$ nm, than other shown cases in fig 5.13. In addition, wider depletion width of the un-bridged method with asymmetric gates ($L_{Gp} = 43$ nm and $L_{Gn} = 20$ nm) results in lower tunneling of carriers, through the barrier, than the other two cases (fig 5.13). Therefore, lower ON current is resulted

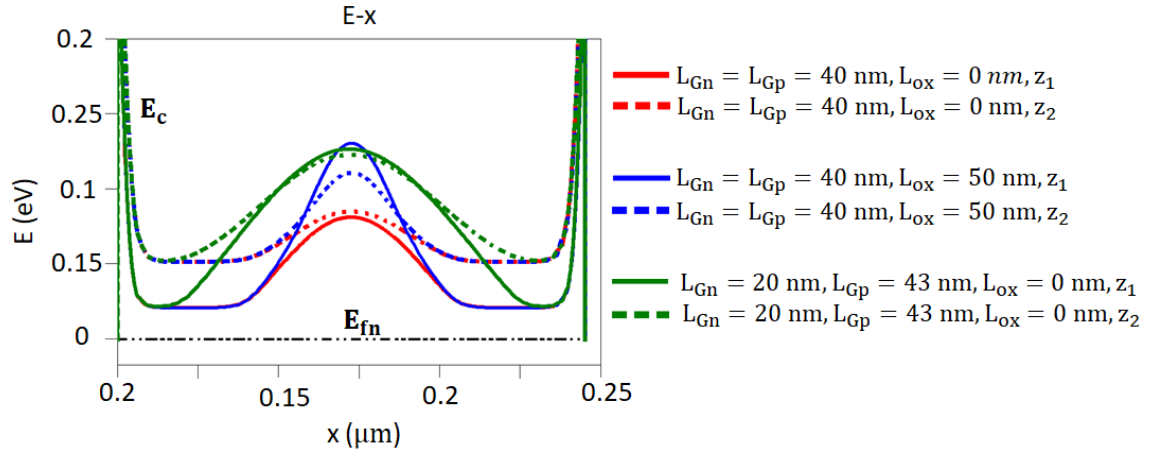


Figure 5.13: E_c along the length of the studied nanowires are plotted along z_1 (solid) and z_2 (dotted), when $V_{CG_n} = V_{PG_n} = 2$ V, $V_{d_n} = 0$ V, and $V_{PG_p} = -2$ V. The red lines are the conduction bands of un-bridged n-FET ($L_{ox} = 0$ V) with $L_{Gn} = L_{Gp} = 40$ nm. E_c of bridged method with $L_G = 40$ nm and $W_{ox} = 18$ nm are shown in blue; and conduction band of n-FET shown in fig 5.4 (c) are plotted in green .

5.4. PHYSICS AND PERFORMANCE DIFFERENCES BETWEEN ASYMMETRIC GATES AND THE BRIDGED METHOD

for n-FET of un-bridged method with $L_{Gn} = 20$ nm, than other two cases. Since the propagation delay, the time taken for the inverter to respond to the change of gate voltage (change of input), of an inverter is in inverse relation with the drain currents of n-FET and p-FET [5], degrading the current of n-FET results in higher propagation delay; and therefore, reduces the switching speed.

In addition, reduction of L_{Gn} in asymmetric method increases the OFF current [167], leading to an increase in power dissipation, when the n-FET in fig 5.4 (c) is off [5, 7]. Introduction of a capacitive bridge at the centre of n-FET eliminates the need of requiring asymmetric gates to achieve symmetric I-V, and therefore, minimises the static power dissipation. The performance characteristics of n- and p-FET for asymmetric gates and bridged methods are shown in table 5.2.

Table 5.2: Performance parameters for n- and p-FETs of both methods at $|V_{PG_{n,p}}| = |V_{CG_{n,p}}| = |V_{d_{n,p}}| = 2V$. GL is gate length, SS is subthreshold swing, V_{th} threshold voltage, and I_{off} current at $|V_{PG_{n,p}}| = |V_{d_{n,p}}| = 2$ V and $|V_{CG_{n,p}}| = 0$ V; and g_m is maximum trans-conductance at $|V_{PG_{n,p}}| = 2$ V and $|V_{d_{n,p}}| = 0.01$ V.

Method	Type-GL (nm)	I_{on} (μA)	V_{th} (V)	SS ($\frac{mV}{dec}$)	$\frac{I_{on}}{I_{off}}$	DIBL ($\frac{mV}{V}$)	g_m ($\frac{A}{V}$)
Asymmetric	n - 20	1.29	1.16	159.6	7.4×10^7	70.35	1.02×10^{-8}
	p - 43	1.30	1.27	134.1	1.68×10^8	8.04	6.7×10^{-11}
Bridged	n - 40	1.709	1.15	131.1	2.29×10^8	145.72	1.7×10^{-8}
	p - 40	1.708	1.19	130.0	2.17×10^8	65.32	9×10^{-11}
Bridged	n - 30	0.957	1.08	149.4	8.89×10^7	97.98	8.72×10^{-9}
	p - 30	0.964	1.25	143.5	9.50×10^7	5.02	6.6×10^{-11}

In comparison to the shown methods, the I_{on} (and threshold voltage) of the un-bridged n-FETs with $L_{Gn} = L_{Gp} = 30$ nm and 40 nm are $1.92 \mu A$ (1.20 V) and $2.79 \mu A$ (1.22 V), respectively.

5.5 Fabrication process of bridged method and effect of subsequent processing step

The Si RNW-FETs with bridge control can be fabricated on a silicon on oxide (SOI) wafer. A possible fabrication flow is given in this section. Similar to previously fabricated Si RNWs, e-beam lithography and reactive ion etching (RIE) is used to create the Si NWs [33], (fig. 5.14 (b)). Then, Ni is deposited on both ends of the NWs, using e-beam lithography followed by metal evaporation. Nickel is axially diffused to the silicon via annealing, to form abrupt $NiSi_2$ /Si Schottky contacts [28, 28], fig. 5.14 (c).

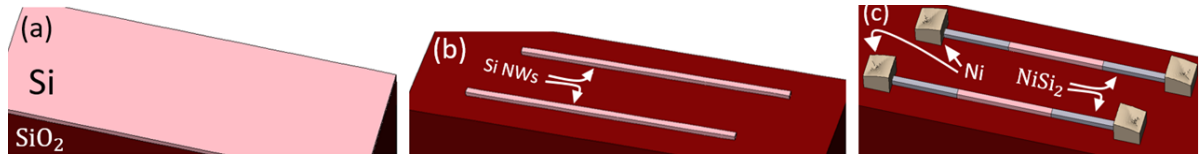


Figure 5.14: (a) SOI wafer with 1 μm of buried SiO_2 and 10 nm of device layer. (b) E-beam written Si NWs after RIE. (c) The formed $NiSi_2$, after annealing the Ni.

The next step is formation of gate insulators and the bridge via oxide deposition. Since introduction of the bridge might introduce new phenomena into Si-RNW fabrication process, the following steps are simulated. Due to initial height difference of the buried oxide with the top of the Si NWs, and top of nickel pads, using a thin photo-resist (fig. 5.15 (a)) leads to formation of non-uniform SiO_2 (fig 5.15 (b)). To optimise this step, the sample is firstly covered by a thick photo-resist (2 μm); and then etched, prior to e-beam lithography, to reach final photo-resist thickness of 50 nm. Fig 5.15 (c) shows the 50 nm thickness of photo-resist, after e-beam lithography and the subsequent etching. Fig. 5.15 (d) shows a deposited SiO_2 with uniform thickness. Similar procedure in fig 5.15 (c) & (d) must be followed to deposit the titanium, used as gates (fig. 5.16).

To minimise the alignment error, the deposited SiO_2 , as gate insulator, cover 50 nm of source and drain; and the titanium gates cover 30 nm of the $NiSi_2$.

5.5. FABRICATION PROCESS OF BRIDGED METHOD AND EFFECT OF SUBSEQUENT PROCESSING STEP

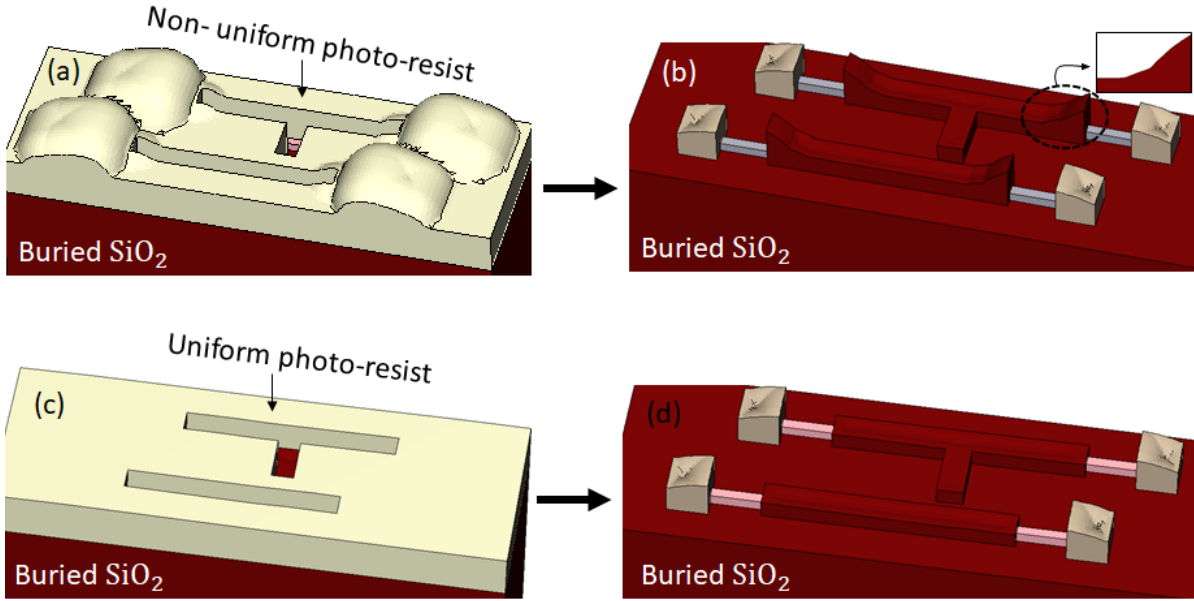


Figure 5.15: (a) The deposited photo-resist with 50 nm of thickness, after e-beam lithography and etching. (b) the final non-uniform SiO_2 , due to non-uniform thin photo-resist coverage, shown in (a). (c) The reduced thickness of photo-resist (from 2 μm to 50 nm), after e-beam lithography and etching. (d) The uniform SiO_2 , due to uniform thin photo-resist, shown in (c).

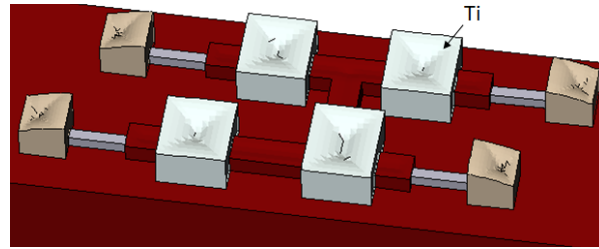


Figure 5.16: Final schematic of the device, after deposition of titanium.

As explained in section 2.5, the sample must be covered with a low-k PMD [45, 168]. The dielectric constant of the used PMD must be less than the gate insulator and the bridge dielectric constant, for three main reasons, (i) to minimise the parasitic gate/PMD/gate capacitance between the neighbouring gates, (ii) to minimise the parasitic capacitance formed in gate/PMD/oxide/channel, and (iii) to minimise the added parasitic capacitance to PG_p /oxide/i-Si capacitor (bridge). If the chosen PMD has higher dielectric constant than the bridge and gate insulators, the generated parasitic capaci-

tance between the mentioned areas increases. Other than using low- k PMD, high- k gate insulators and bridge (such as HfO_2) can be used to minimise the mentioned negative effects of PMD.

5.6 Impact of fabrication inaccuracies in gate length and bridge dimensions

In this section, the response of n-FET's I_{on} to possible deviations of L_{ox} , W_{ox} , and L_G from the ideal dimensions during the fabrication process is studied. Due to the nano-scale dimensions of these parameters, errors in the fabrication process are likely. To study the effect of deviations, every parameter is varied in a range of ± 4 nm while other parameters are kept constant.

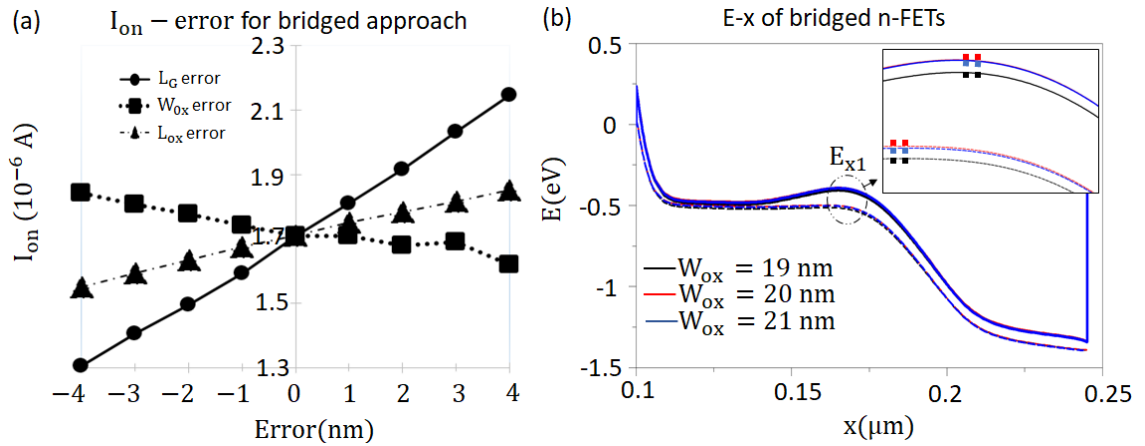


Figure 5.17: (a) ON current as a function of variation from the mean, and (b) E_c at z_1 along the channel for bridged n-FET with $L_G = 40$ nm, $L_{ox} = 50$ nm, and $W_{ox} = 18$ nm.

As seen in fig. 5.17 (a), minor change in I_{on} occurs as L_{ox} or W_{ox} are varied. I_{on} for bridged n-FETs with $W_{ox} = 20$ nm and $W_{ox} = 21$ nm is approximately similar. This occurs because I_{on} reduction due to rise of potential barriers (ϕ_{Cug}) gets compensated with rise of current due to increase in electric field (E_{x1}), fig. 5.17 (b).

However, inaccuracy in L_G leads to higher I_{on} variation than L_{ox} and W_{ox} . This is due to two main reasons, (i) L_G tunes the ability of the gate to control carriers in the channel, and (ii) L_G has high impact on the barriers formed across the channel.

5.7 Conclusion

Symmetric I-V characteristics for n- and p-FET is vital for Si RNW-FET CMOS inverters. Previously, implementation of compressive strain engineering on Si was found to result in approximately symmetric I-V characteristics. However, this method is highly sensitive to crystallographic orientation and insulator's material.

In this work, TCAD study is carried out to design FETs with symmetric I-V characteristics. A new approach with equal gates for n- and p-FET, based on a capacitive oxide bridge between the un-gated regions of the n-FET and program gates of p-FET (bridged method), is compared with having dissimilar gates for n- and p-FET. Equal I_{on} can be achieved using dissimilar gates. However, dissimilar gate lengths lead to un-equal $\frac{I_{on}}{I_{off}}$ ratio. In addition, the I_{on} tuning in this approach is limited to gate lengths less than 60 nm for the double gated RNW, as carrier concentration in un-gated regions becomes similar to gated regions at this gate length. However, equal ON and comparable OFF current is achieved for n- and p-FETs in the bridged method, as a consequence of decreasing ON current of the n-FET. This method has shown good tolerance toward variation in fabrication process.

GATED SILICON NANOWIRE FOR THERMO-ELECTRIC POWER GENERATION AND TEMPERATURE SENSING

In this study, TCAD simulations [11] are firstly conducted to study the effect of using an appropriate gate metal work function to control the carrier concentration in intrinsic Si NWs, and therefore, σS^2 across the nanowire. Then, the gated structure is used to sense the temperature using multiple approaches. Section 6.1, introduces the simulated gated intrinsic Si NWs of this work for thermo-electric power generation. Section 6.2, explains the methodologies to sense the temperature based on the simulated gated Si-NWs. Section 6.3, concludes the work.

6.1 Gated i-Si for thermo-electric power generation

The metal gate work function was found to be highly important in nano-scaled transistors. Ti metal gate on intrinsic Si-RNW transistors (section 2.4) was deliberately chosen, as the silicon work function ($\phi_{Si} = 4.634$ eV) is equal to the titanium work function (ϕ_{Ti}) [1, 27, 150], fig. 6.1 (a). $\phi_{Ti} = \phi_{Si} \approx 4.63$ eV [27] leads to flat band, and therefore leave the NW intrinsic at zero gate bias. However, $\phi_m \neq \phi_{Si}$ results in band bending at the

Si/SiO₂ interface, and causes an internal electric field (E_{int}) across SiO₂ [169]. Choosing an appropriate gate metal with ϕ_m at $\phi_{Ti} > \phi_m$ ($\phi_{Ti} < \phi_m$) can lead to accumulation of electrons (holes) at the Si/SiO₂ interface at zero gate bias (fig. 6.1 (b) & (c)).

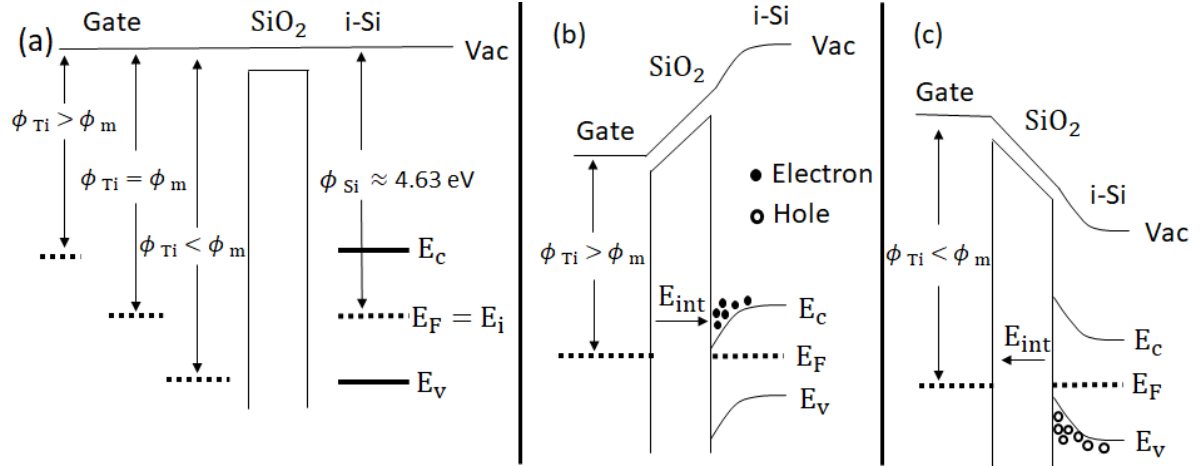


Figure 6.1: (a) The energy band diagram of the metal/SiO₂/i-Si structure before contact. (b) Metal/SiO₂/i-Si structure after contact when (b) $\phi_m < \phi_{Ti}$, and (c) $\phi_m > \phi_{Ti}$, leading to accumulation of electrons and holes at Si/SiO₂, respectively.

In this work, electron modulation and its effect on power generation is studied via tuning ϕ_m of the metal gate wrapped around the i-Si NW. This approach is similar to applying a gate voltage to flatten the bands in MOSFETs due to work function difference of metal gate and Si, leading to accumulation/depletion of charges at zero gate bias. Figure 6.2 shows the simulated gate-all-around (GAA) structure. A circular Si-NW with

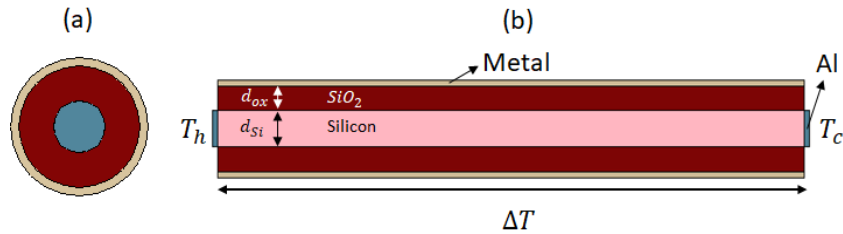


Figure 6.2: (a) Front view, (b) cross section of simulated gated i-Si. For the sake of simulation efficiency, all metals are defined as 2D contacts only.

diameter d_{Si} and length $L_{Si} = 220$ nm is wrapped by SiO₂ with thickness $d_{ox} = 8$ nm.

L_{Si} and d_{ox} are kept constant while d_{Si} is varied. The metal layers in gated structure are assumed as 2D surfaces without thickness in Sentaurus. The contacts at both ends of the nanowire are aluminum with work function $\phi_{Al} = 4.1$ eV, within the range of reported work functions for aluminum ($4.06 \text{ eV} \leq \phi_{Al} \leq 4.28 \text{ eV}$) in [170]. The metal gate work function is varied between $3.7 \text{ eV} \leq \phi_m \leq 4.2 \text{ eV}$ to tune the electron accumulations in the channel. The lattice thermal conductivity of smooth circular Si-NW ($\kappa_{(L,Si)}$) as a function of d_{Si} is extracted from [60] and SiO_2 thermal conductivity (κ_{ox}) is kept constant for all d_{Si} at $\kappa_{ox} = 0.014 \frac{W}{cmK}$ [4]. $\kappa_{(L,Si)}$ for $d_{Si} = 12 \text{ nm}$, 37 nm , and 62 nm are $0.064 \frac{W}{cmK}$, $0.182 \frac{W}{cmK}$, and $0.292 \frac{W}{cmK}$ respectively. The overall thermal conductivity of Si is $\kappa_{Si} = \kappa_{(L,Si)} + \kappa_{(e,Si)}$, where $\kappa_{(e,Si)}$ is thermal conductivity due to electrons in Si. ΔT is formed by having a constant cold sink ($T_c = 300 \text{ K}$) and a hot sink (T_h).

Fig. 6.3 shows the influence of metal gate work function (ϕ_m) on electron density and electron mobility. Since carrier modulation is achieved by band bending at Si/ SiO_2 interface due to internal electric field (E_{int}), electron concentration (n) and mobility experience a non-homogeneous variation across the cross section (fig 6.3 (a) & (b)). Unlike doping where power is generated across the cross-section uniformly, gated structures have non-homogeneous power generation. As seen in fig 6.3 (c) and (d), carrier concentration (mobility) increases (reduces) as ϕ_m reduces. As expected, higher carrier concentration (lower mobility) is achieved for smaller d_{Si} , due to higher control on carriers.

Due to the inverse relation of Seebeck coefficient (S) with electron concentration (n), non-homogeneous behaviour of n leads to variation in S . Along the cross section of the NW, S is highest at the centre of the cross section (C), and reaches to its minimum at the Si/ SiO_2 interface (int). Since carrier control for smaller d_{Si} is higher, reducing ϕ_m leads to higher average n ($\langle n \rangle$) and therefore higher average σ ($\langle \sigma \rangle$) for $d_{Si} = 12 \text{ nm}$ than larger diameters (fig 6.4 (a)). Although the average $\langle S \rangle$ for $d_{Si} = 12 \text{ nm}$ is less than for larger diameters (fig 6.4 (a)), higher $\langle \sigma \rangle$ for smaller d_{Si} compensates

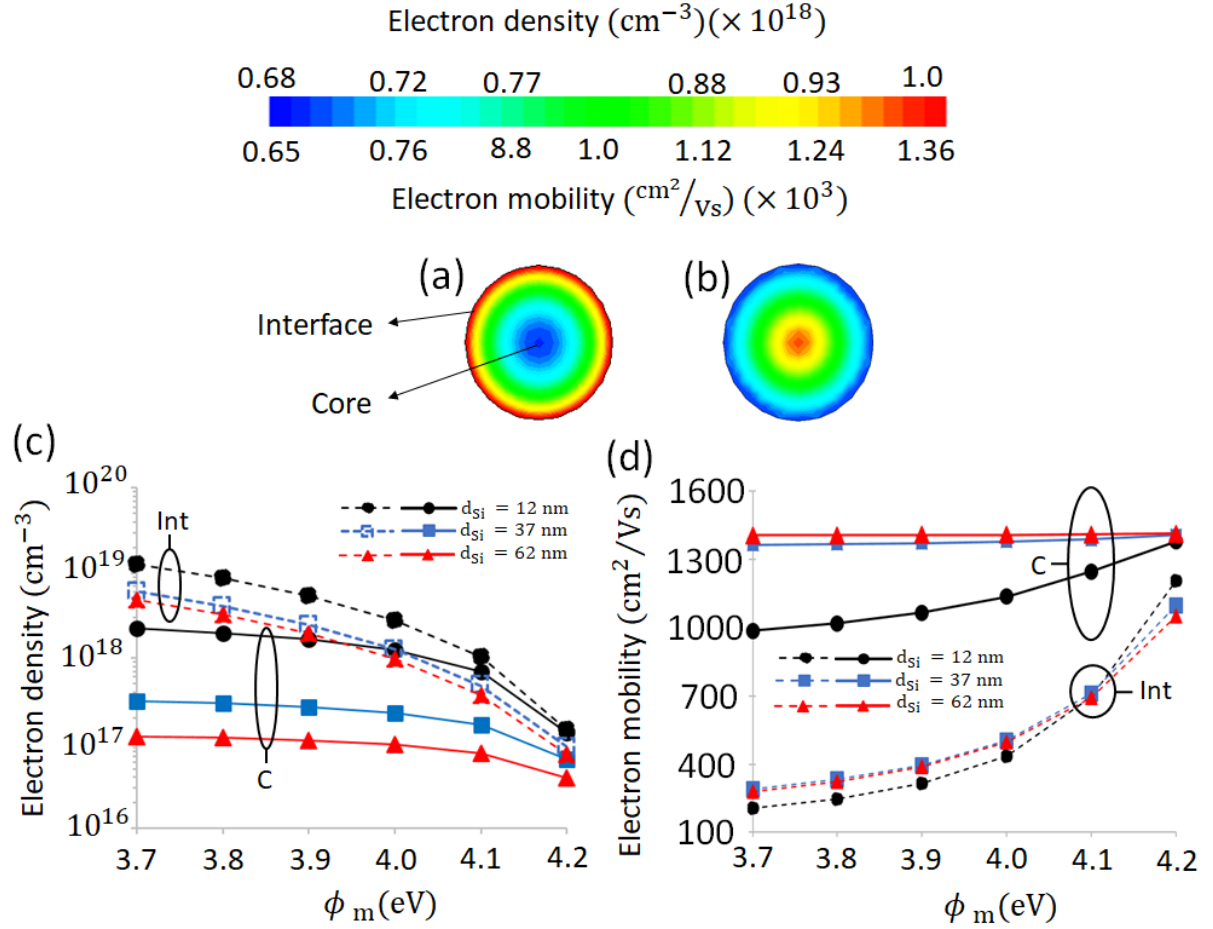


Figure 6.3: (a) electron density and (b) electron mobility of gated i-Si with $d_{Si} = 12$ nm. Both at middle of the NW length. (c) electron density and, (d) electron mobility as a function of ϕ_m of metal gate and d_{Si} for gated i-Si at $\Delta T = 0$ K. Labeling: C refers to the middle of the NW and int is interface. The values are given at $\text{int} = r_{Si} - 1$ nm and C is the core of the NW (centre), where r_{Si} is the radius.

with reducing $\langle S \rangle$. This compensation leads to maximum σS^2 for $d_{Si} = 12$ nm (fig 6.4 (b)). The voltage difference (ΔV) and generated current (I_g) show trend consistent with: $\langle \sigma \rangle$, $\langle S \rangle$, and area (A). Higher average $\langle S \rangle$ leads to higher ΔV . In addition, lower current density at larger diameters were compensated by their larger area.

The maximum output power (P_{max}) of the simulated structures at $T_h - T_c = \Delta T = 15$ K are shown in fig. 6.5. P_{max} is the peak power as a function of varying R_L , where R_L is load resistance. At P_{max} , $R_L = R$, where R is resistance of the TEG. P_{max} of simulated

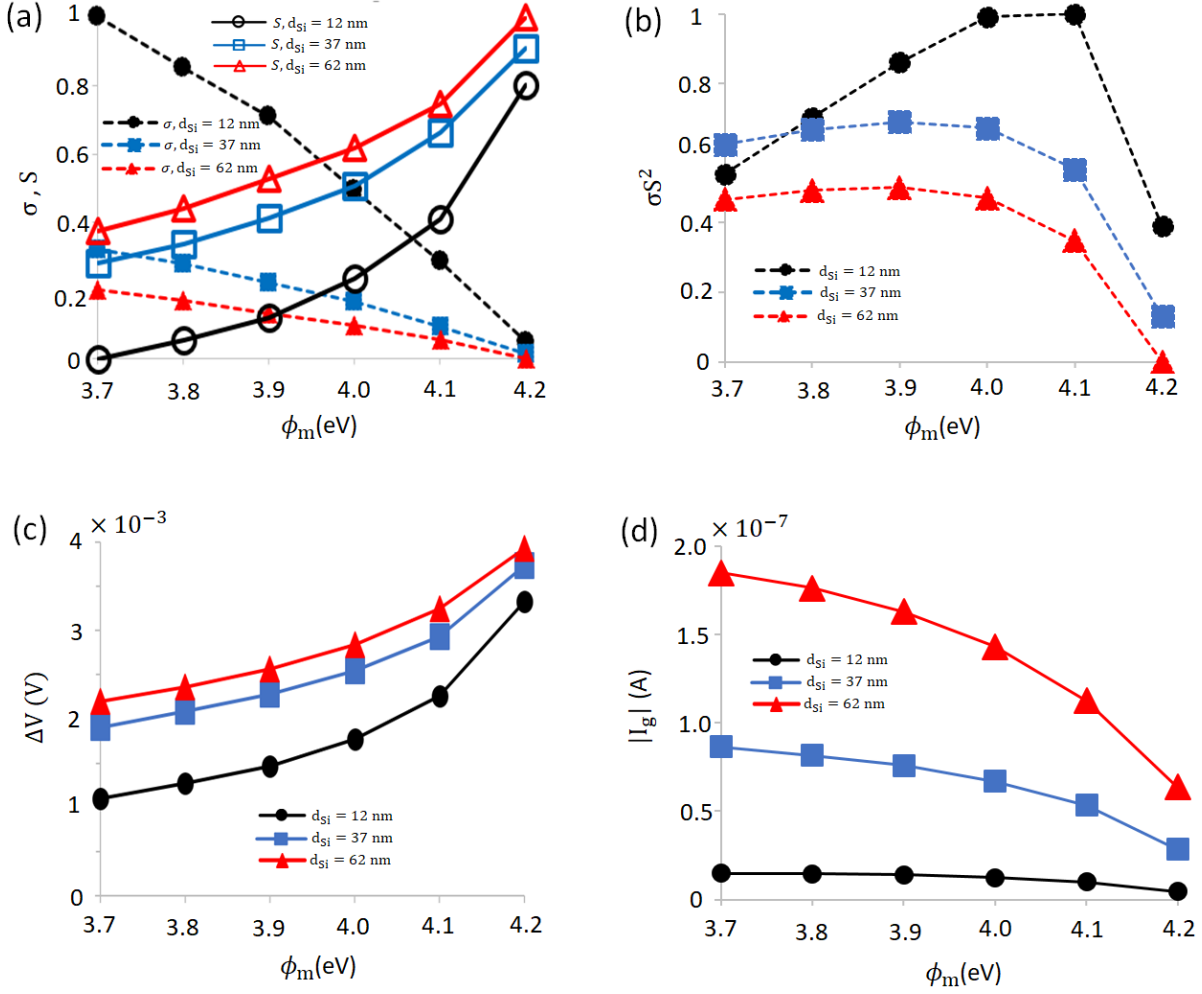


Figure 6.4: (a) Normalised σ - ϕ_m (dashed) and S - ϕ_m (solid), (b) normalised σS^2 - ϕ_m , (c) ΔV - ϕ_m , and (d) I_g - ϕ_m at $\Delta T = 15$ K for $d_{Si} = 12$ nm, 37 nm, and 62 nm. Normalised amount = $\frac{x - x_{min}}{x_{max} - x_{min}}$, where x can be S , σ , or σS^2 ; and x_{min} (S_{min} , σ_{min} , or σS^2_{min}) is the minimum amount, and x_{max} (S_{max} , σ_{max} , or σS^2_{max}) is the maximum amount.

NWs were achieved at different R_L , since the average mobility and $\langle n \rangle$ were different for different d_{Si} and ϕ_m .

Fig 6.5 (a) shows P_{max} of NWs with d_{Si} : 12, 37, and 62 nm. To understand the effect of mobility scattering on P_{max} , the graph of P_{max} - ϕ_m for $d_{Si} = 12$ nm is plotted with and without implementing mobility models (fig 6.5 (a)). The results of the gated i-Si with 12 nm Si diameter is also compared with the doped Si-NW having similar d_{Si} (fig. 6.5 (b)). Simulations show that mobility scattering in gated i-Si causes 32 % degradation in

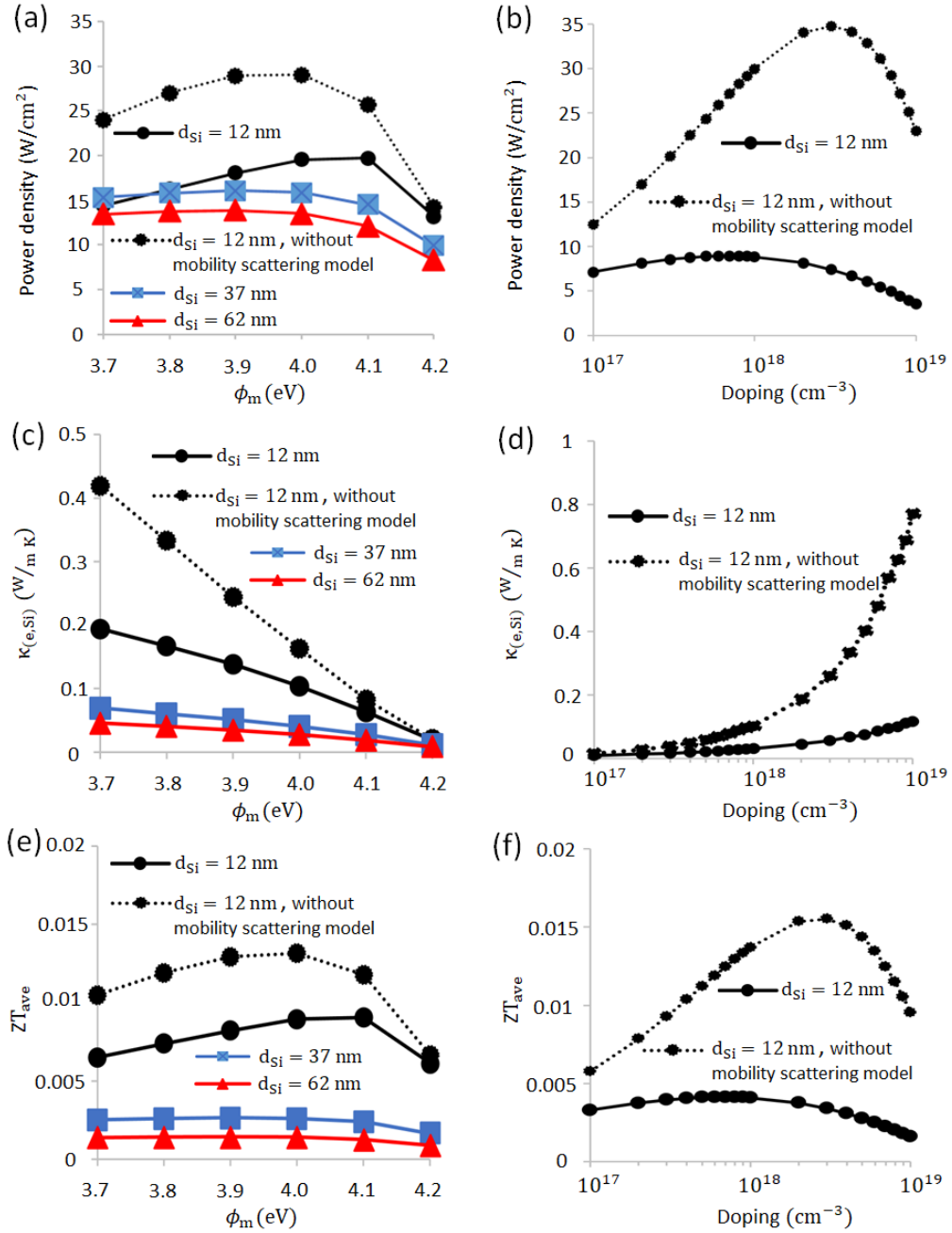


Figure 6.5: (a) Power density- ϕ_m graph of the gated i-Si with $d_{si} = 12$ nm, 37 nm, and 62 nm; and (b) power density-doping of doped NWs with $d_{si} = 12$ nm at $\Delta T = 15K$. (c) $\kappa_{(e,Si)}$ - ϕ_m for gated intrinsic NWs, and (d) $\kappa_{(e,Si)}$ - doping of doped NW with $d_{si} = 12$ nm. (e) ZT_{ave} - ϕ_m for gated i-Si NWs and (f) ZT_{ave} - doping of doped NW with $d_{si} = 12$ nm. $T_{ave} = \frac{T_h + T_c}{2}$, where $T_h = 315$ K and $T_c = 300$ K.

P_{max} . In addition, due to reduced control in larger d_{Si} , P_{max} of gated NWs with larger diameters are achieved at lower ϕ_m . Fig 6.5 (b) shows 74 % degradation in P_{max} of doped structures, caused by mobility scattering. Higher degradation in doped structures is expected, due to introduction of ionised impurity scattering. The interface mobility of gated i-Si with $d_{Si} = 12$ nm and $\phi_m = 4.1$ eV ($n = 1.03 \times 10^{18} \text{ cm}^{-3}$ at the interface) is 2.44 times higher than the doped structure, having similar carrier concentration. P_{max} of gated i-Si NWs with $d_{Si} = 12$ nm is 2.20 times larger than the doped structure with similar d_{Si} . To better understand the effect of carrier modulation on TEG performance, one has to calculate $\kappa_{(e,Si)}$, and therefore, ZT_{ave} . $\kappa_{(e,Si)}$ is calculated using eq. 3.11 for doped and gated i-Si. Although significant rise is seen (fig. 6.5 (c) & (d)) for $\kappa_{(e,Si)}$ as carrier concentration increases, $\kappa_{(L,Si)}$ remains dominant. Improvement of σS^2 in gated structures, compared to doped structures, have led to higher ZT_{ave} for gated structures than doped Si.

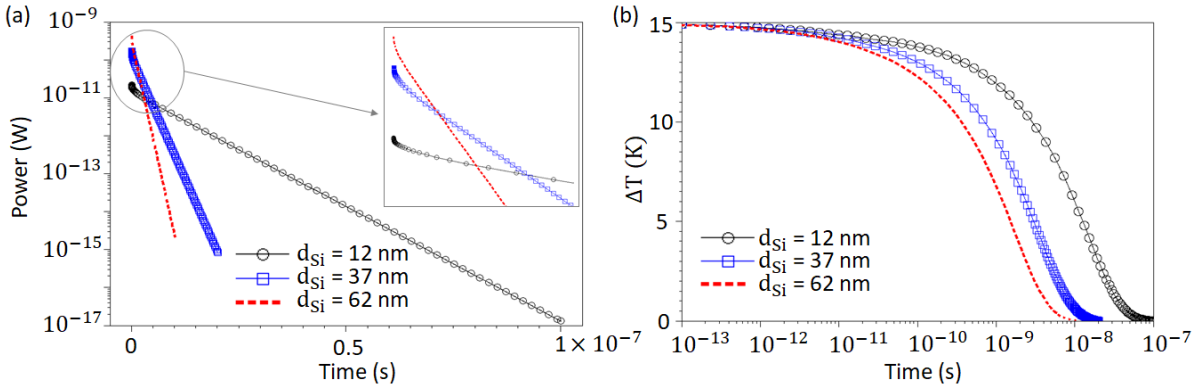


Figure 6.6: (a) Power-time, and (b) ΔT -time of simulated NWs with d_{Si} : 12, 37, and 62 nm. Heat sink loses its temperature at time > 0 .

In this part of the study, T_c is constant while T_h is exceptionally lost as a function of time, to study the effect of thermal conductivity. Fig. 6.6 shows the response of power and ΔT to temperate loss at T_h as a function of time, where time = 0 is the instance prior to temperature loss. Within the range of simulated NWs and time = 0 (fig. 6.6 (a)), we find that maximum output power is achieved for higher d_{Si} . At time = 0, $T_h (= 15 \text{ K})$

is constant and steady. However, heat sink starts losing its temperature at time > 0 , and preservation of ΔT becomes solely dependent to κ_{Si} . As seen in fig. 6.6 (a), NWs with smaller d_{Si} , and therefore lower κ_{Si} , have longer time of power generation. The time taken for $d_{Si} = 12$ nm to lose 14 K of ΔT is 76 % and 88 % more than NWs with 37 nm and 62 nm diameters respectively (fig. 6.6 (b)).

We have also compared the performance of GAA to Ω -gated NW [171], both shapes had $\phi_m = 4.1$ eV, $\Delta T = 15$, and $d_{ox} = 8$ nm. The P_{max} of Ω -gated NWs with 12 nm, 37 nm, and 62 nm were 0.09 %, 3.47 %, and 4.30 % less than that of the GAA NWs with similar diameters respectively.

Previously, extensive research is done in [172–174] to study the effect of fixed charges (Q_f) and interface trapped charges (Q_i) on silicon devices. Among the two charges, interface trapped charge at Si/ SiO_2 interface has considerable impact on carrier concentration. A typical density range for Q_i is $10^{10} < D_{it} < 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ [172]. Fig 6.7 shows the maximum output power of GAA i-Si with $d_{Si} = 12$ nm as a function of D_{it} . A sharp decrease in P_{max} is seen after $D_{it} \geq 2 \times 10^{11}$ for GAA with $\phi_m = 4.1$ eV. However, reducing the work function to 3.9 eV recovers P_{max} at $D_{it} \approx 8 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$.

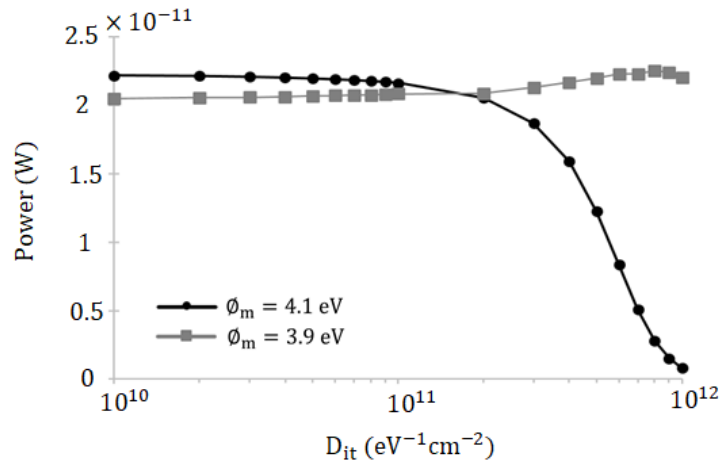


Figure 6.7: Power- D_{it} for GAA i-Si NW with $d_{Si} = 12$ nm, $\Delta T = 15$ K, and two ϕ_m : 3.9, and 4.1 eV.

For completeness, the effect of applying gate voltage (V_{gate}) on P_{max} for GAA i-Si

with $d_{Si} = 12$ nm, $\phi_m = 4.1$ eV, and $D_{it} = 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ was also studied. As seen in fig. 6.8, $V_{gate} = 0.25$ V is required to reach the optimised $\langle n \rangle$. The optimised carrier concentration leads to equal P_{max} as the NW with $d_{Si} = 12$ nm, $\phi_m = 4.1$ eV, and $D_{it} = 0$ (ideal).

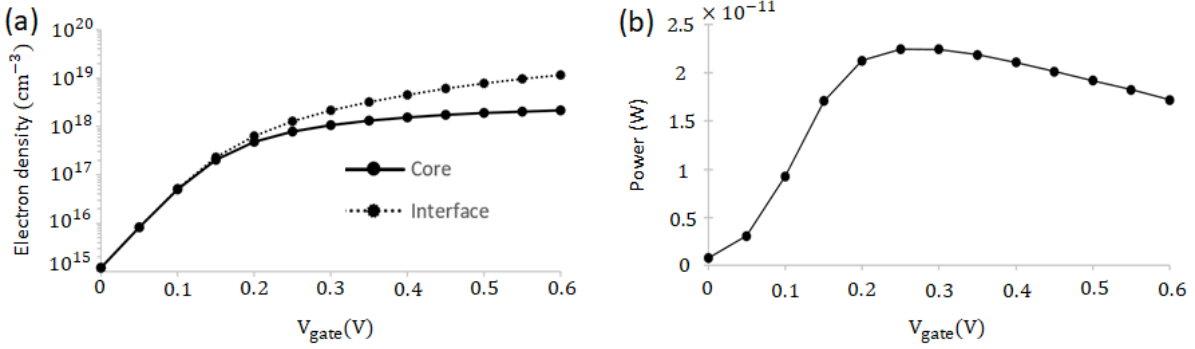


Figure 6.8: (a) Electron density- V_{gate} , and (b) power- V_{gate} for $d_{Si} = 12$ nm, $d_{ox} = 8$ nm, and $D_{it} = 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$.

6.2 Gated structure for temperature sensing

Reconfigurable GAA RNW structures with a single gate (SG) (fig 6.2) and double gate (DG) (fig 6.9 (a)) can be used for temperature sensing. The core of these structures are Al/i-Si/Al wrapped by SiO_2 , having similar dimensions as in section 6.1. In DG GAA RNWs, the type of carriers in the channel and the control of carrier injection into the channel is done by program gate (PG) and control gate (CG), respectively. The gap between CG and PG is 10 nm for all DG GAA RNWs. Work function of gates (ϕ_m) and D_{it} are set to 4.1 eV and $0 \text{ cm}^{-2} \text{ eV}^{-1}$ (ideal), respectively. V_{CG} is varied, while $V_{PG} = 0$ V for all simulations. A variable ΔT is defined by having constant $T_c (= 300 \text{ K})$ and varied T_h . The temperature sensor is connected to load resistance (R_L) with $R_L = R$.

Fig. 6.9 (b) shows the conduction band (E_c) along the length of the GAA RNWs. At zero V_{CG} , E_c is approximately flat across the nanowire, as work functions of contacts and gates are equal to 4.1 eV. However, applying a negative voltage to V_{CG} increases

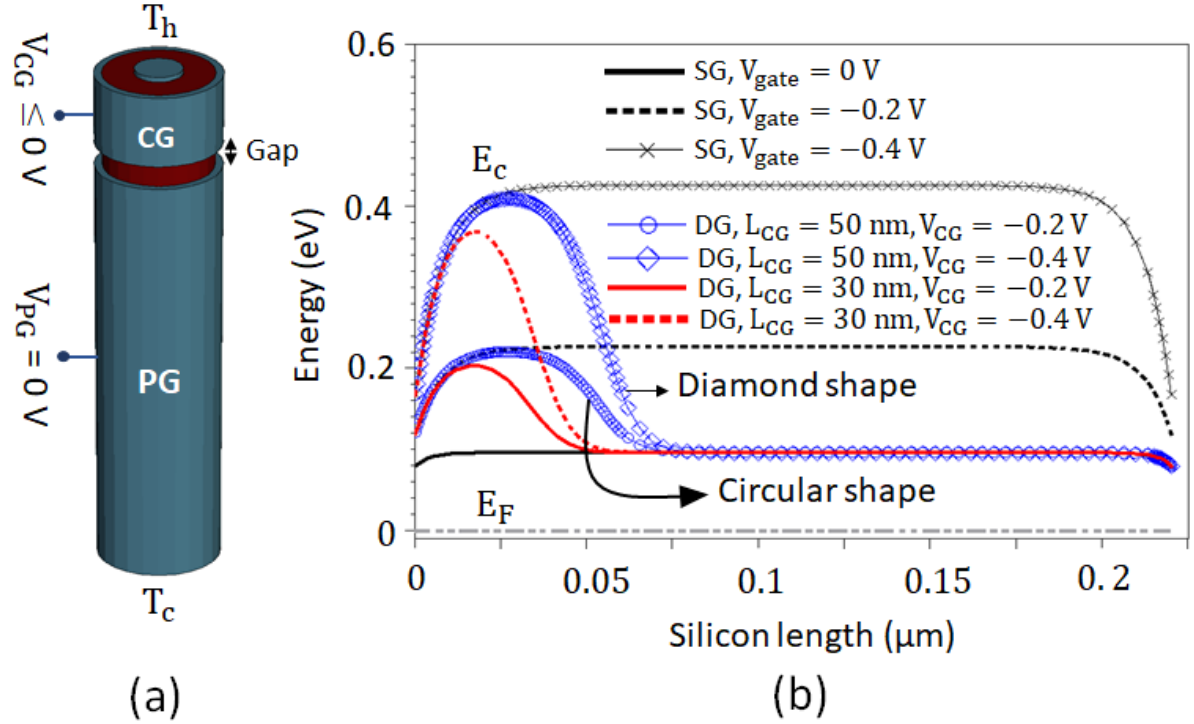


Figure 6.9: (a) Schematic of a DG temperature sensor with program gate (PG) and control gate (CG). (b) E_c along the length of the SG and DG (CG lengths of 30 or 50 nm) GAA NW for -0.4 V $< V_{gate,CG} < 0$ V. The NW length is 220 nm and $d_{Si} = 12$ nm.

the barrier ϕ_B faced by electrons at the metal/semiconductor interface under CG. On the other hand, increasing the temperature T_h , increases the density of electrons with energies higher than ϕ_B . Higher density of electrons with greater energy than ϕ_B , increases the generated current (I_g) across the NW. In this type of sensor, temperature sensing can be done in one or two steps, for higher accuracy. Temperature of the hot spot can be sensed by, (i) the linear relation of generated current (I_g) with T_h at $V_{CG} = 0$ V (fig. 6.10 (a)), and/or (ii) by tuning V_{CG} to keep I_g constant as T_h is varied. In the second case, the value of V_{CG} (V_G) to keep I_g constant is the reading of the hot spot temperature (T_h).

The depletion width and barrier height (ϕ_B) as a function of V_{CG} ($V_{CG} < 0$ V) are defined by CG length (L_{CG}). The effect of L_{CG} on depletion width and ϕ_B are studied for $d_{Si} = 12$ nm, 37 nm, and 62 nm, and compared with SG GAA NW, fig. 6.9 (b).

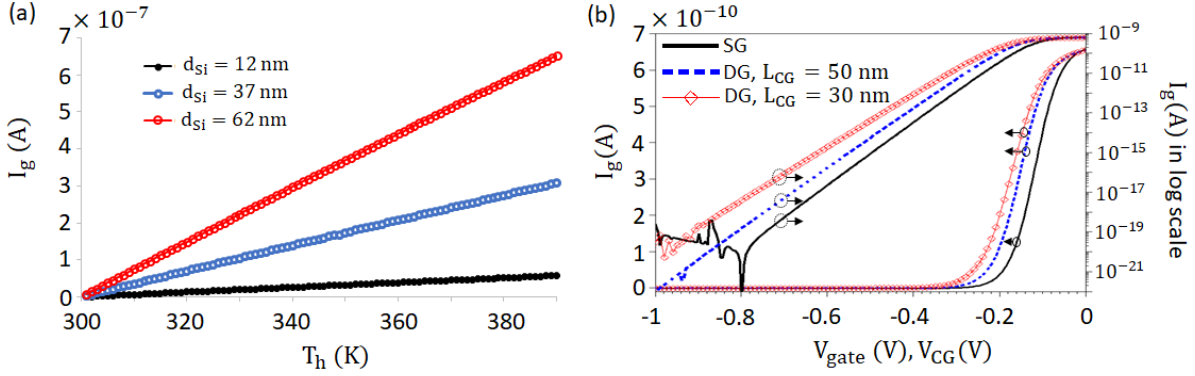


Figure 6.10: (a) I_g - T_h in the SG NW for $d = 12$ nm, 37 nm, and 62 nm. (b) The variation of I_g as a function of the control voltage V_G and V_{CG} for the SG and DG NWs at a $\Delta T = 1$ K.

Fig. 6.10 (a) shows the linear relation of I_g with T_h for SG NWs with different diameters and $V_{gate} = 0$ V. Due to the short gap (= 10 nm) between CG and PG of DG NWs (not shown), I_g - T_h follows a similar trend as SG NWs with equal d_{Si} . The formula of I_g as a function of T_h (eq. 6.1) can be derived based on equation of current in [73, 92, 93, 175].

$$I_g = -\frac{qAn\mu_{(e,tot)}}{L}S(T_h - T_c) \quad (6.1)$$

Where q is charge, A is cross sectional area of the channel, $\mu_{(e,tot)}$ is mobility of electrons, and L (= 220 nm) is length of the nanowire. As seen in eq. 6.1, the variability of $\mu_{(e,tot)}$, n , and A , tunes the response of I_g to T_h . A has significant impact on I_g , as it will affect $\mu_{(e,tot)}$ and n (fig. 6.3) as well. As d_{Si} increases, $\mu_{(e,tot)}$ increases and n reduces.

The sensitivity of I_g to changes in temperature ($\Delta I_{1K} = \frac{\Delta I_g}{\Delta T}$ with $\Delta T = 1$ K) is highly dependent to d_{Si} . $\Delta I_{1K} = 0.63 \frac{nA}{K}$, $3.40 \frac{nA}{K}$, $7.22 \frac{nA}{K}$ for $d_{Si} = 12$ nm, 37 nm, and 62 nm, respectively. Fig 6.10 (b), shows the impact of L_{CG} and gate voltage (V_{gate} for SG and V_{CG} for DG) on I_g at $\Delta T = 1$ K. Similar to FETs in weak inversion, I_g reduces exponentially over wide range of negative V_{gate} or V_{CG} bias for SG or DG respectively. The sub-threshold swing (inverse of the slope of $\log_{10}(I_g)$ - V_{CG}) gets lower as L_{CG}

increases (table 6.1), while the weak inversion region gets wider for shorter L_{CG} .

Table 6.1: Shows sub-threshold (SS) slope of the GAA NWs for $d_{Si} = 12$ nm at $\Delta T = 1$ K, 5 K, and 10 K ; and $d_{Si} = 37$ nm and 62 nm at $\Delta T = 1$ K. $SS_{DG,50}$ and $SS_{DG,30}$ are SS for DG NWs with $L_{CG} = 50$ nm and 30 nm respectively.

$d_{Si}(nm)$	$\Delta T(K)$	$SS_{SG}(\frac{mV}{dec})$	$SS_{DG,50}(\frac{mV}{dec})$	$SS_{DG,30}(\frac{mV}{dec})$
12	1	62.36	65.16	74.29
12	5	62.75	66.09	75.12
12	10	63.41	66.97	76.24
37	1	62.84	84.38	123.8
62	1	63.53	115.30	198.96

The results for T_h detection as a function of gate bias is given in fig. 6.11. The reference generated current (I_{gref}) is the generated current at $T_h = 301$ K (and therefore $\Delta T = 1K$) when zero voltage is applied to gate(s). I_{gref} for different diameters are different. At $T_h > 301$ K, a gate voltage is applied to keep the current equal to I_{gref} . I_{gref} is 0.65 nA, 3.51 nA, and 7.51 nA for $d_{Si} = 12$ nm, 37 nm, and 62 nm, respectively. As seen in fig 6.11, the required gate voltage to operate sensors increase as d_{Si} increases. In addition, shorter L_{CG} leads to higher gate voltage supply for sensing operation.

In the two-step temperature sensing implementation, the generated current (I_g) at zero gate voltage in step (i) can be used to find the required $V_{gate,CG}$ (V_{gate} for SG and V_{CG} for DG) in (ii) to maintain I_{gref} . Equation 6.2 calculates the required $V_{gate,CG}$ as the function of generated current (I_g) in (i).

$$V_{G,CG} = \frac{ab + cI_g^d}{b + I_g^d} \quad (6.2)$$

Where a, b, and c are constants that are dependent to d_{Si} and gate length. These parameters are given in table 6.2.

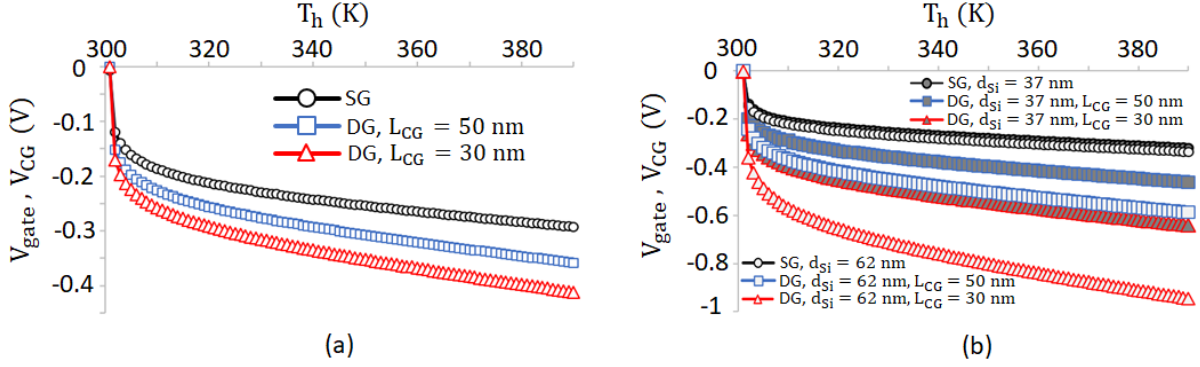


Figure 6.11: $V_{gate,CG}-T_h$ for (a) $d_{Si} = 12$ nm, (b) $d_{Si} = 37$ nm, and 62 nm to achieve their $I_{g_{ref}}$. $I_{g_{ref}}$ is 0.65 nA, 3.51 nA, and 7.51 nA for $d_{Si} = 12$ nm, 37 nm and 62 nm, respectively.

Table 6.2: The parameters of equation 6.2; and the accuracy of the parameters in correlating I_g with required $V_{gate,CG}$ for the mentioned GAA i-Si sensors. The maning of the sensors are as follows: $SG_{d_{Si}}$ and $DG_{d_{Si},L_{CG}}$, where d_{Si} and L_{CG} are in nm.

Name	SG ₈	SG ₃₇	SG ₆₂	DG _{8,50}	DG _{37,50}	DG _{62,50}	DG _{8,30}	DG _{37,30}	DG _{62,30}
a	3.1922	4.9519	7.4352	2.6332	5.3730	6.5968	1.8983	1.8621	1.3579
b	0.0085	0.0082	0.0044	0.0103	0.0199	0.0342	0.0170	0.0403	0.0575
c	-0.5920	-0.6394	-0.6171	-0.7143	-1.0848	-1.5785	-0.8718	-1.5318	-2.4840
d	0.1409	0.1356	0.1505	0.1492	0.1141	0.0995	0.1501	0.1477	0.1747
Accuracy	% 95.2	% 94.5	% 94.3	% 93.8	% 93.7	% 94.3	% 93.9	% 94.1	% 94.9

6.3 Conclusion

Carrier modulation via metal gate work function (ϕ_m) tuning of gated intrinsic Si was studied using TCAD simulation, and compared with doped structures. Significant improvement in mobility in gated structures at zero gate bias led to 2.2 higher power than for doped structures. In addition, significant degradation in output power of gated i-Si, caused by interface trapped charges, can be compensated with reduced ϕ_m . Furthermore, larger diameter (d_{Si}) of gated Si can lead to higher output power, only in the presence of steady and constant heat source. However, as heat source loses its temperature, NWs with smaller d_{Si} (lower thermal conductivity) is preferable for longer heat preservation and power generation.

In addition, it was found that single gated (SG) and double gated (DG) i-Si can be used for temperature sensing. Due to the existence of a gate at the metal/i-Si interface,

injection of carriers into the channel from the source can be controlled. At zero gate bias, the current generated (I_g) increases linearly with temperature at hot side (T_h). The I_g is thus a measure for T_h . Alternatively, a gate voltage can be applied such that the current remain constant at all temperatures of T_h . It was found that larger Si NW diameter and shorter gate length lead higher gate voltage requirement for operation.

GRADING CARRIER DENSITY TO OPTIMISE THERMO-ELECTRIC POWER GENERATION

Previously, we have shown that work-function tuning of the metal gate can modulate carrier concentration in an intrinsic material. This approach increased the power of Si TEGs by 2.2 times compared to doped structures, due to reduction in mobility degradation. In this chapter, temperature dependent carrier concentration, effective density of states, and conduction band are graded to further optimise the output power. Grading the conduction band of a NW with electrons as majority carriers can introduce an internal electric field (E_{int}), in the same direction as the current generated by ΔT (I_g). Similar direction of I_g with E_{int} can lead to an increase in overall current. In addition, as seen in eq. 3.5, Seebeck coefficient of S_n can increase by increasing $\ln\left(\frac{N_c}{n}\right)$. Therefore, reduction of carrier concentration and/or increase of effective density of states can improve S_n in non-degenerate semiconductors.

This chapter is organised as follows. Section 7.1, studies the effect of grading mole fraction of SiGe on improvement of power generation. Section 7.2, investigates the effect of grading the diameter of Si NW on the gradient of carrier concentration, and therefore,

its output power. Section 7.3, concludes the work.

7.1 Grading mole fraction of gated $Si_{1-x}Ge_x$

In this approach, mole fraction (x) of intrinsic $Si_{1-x}Ge_x$ is graded ($x = x_1 \rightarrow x = x_2$) to tune its electrical and thermal properties. Band gap, electron affinity, mobility, effective density of states [11], and thermal conductivity [107] of SiGe changes as a function of x . Variation of band gap and electron affinity of graded intrinsic SiGe leads to grading of carrier concentration even when the NW is is not gated (fig. 7.1 (a)). Similar to chapter 6, SiGe is covered by 8 nm of SiO_2 and a 2D metal gate (fig 7.1 (b)); and diameter (d_{SiGe}) and length of the SiGe are constant and equal to 12 nm and 220 nm respectively.

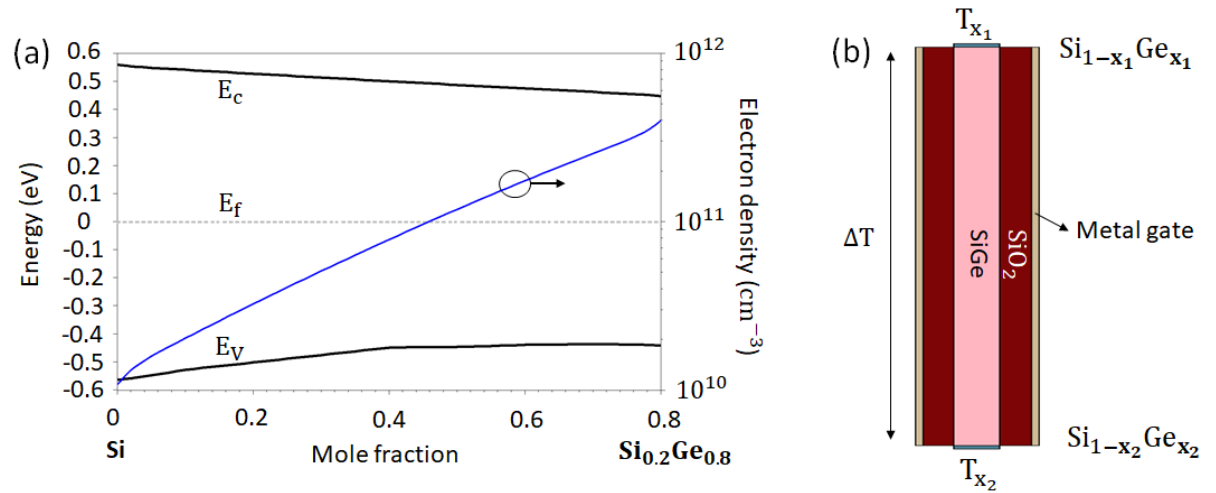


Figure 7.1: (a) Energy and electron density of the un-gated graded SiGe from $x_1 = 0$ to $x_2 = 0.8$. (b) Cross section of the gated graded ($x_1 \rightarrow x_2$) SiGe with temperature T_{x_1} at x_1 and T_{x_2} at x_2 .

The work function of 2D contacts at both ends of the channel are chosen such to form approximately flat bands at the metal/SiGe interfaces for all simulations. Flat band at both ends of the NW ensures that the changes in output power is solely due to effect of grading. κ_{ox} is kept constant at $0.014 \frac{W}{cmK}$ [4]; and the curvature relation of SiGe lattice thermal conductivity ($\kappa_{(L,SiGe)}$) with mole fraction x (shown in fig. 3.4 (a)) is

used to estimate $\kappa_{(L,SiGe)}$ for $d_{SiGe} = 12$ nm. In this case, $\kappa_{(L,SiGe)}-x$ for $d_{SiGe} = 12$ nm is found by fitting the calculated lattice thermal conductivity of Si in [60], $Si_{0.99}Ge_{0.01}$, $Si_{0.95}Ge_{0.05}$, $Si_{0.9}Ge_{0.1}$, $Si_{0.8}Ge_{0.2}$, and $Si_{0.7}Ge_{0.3}$ in [107] in to the $\kappa_{(L,SiGe)}-x$ curve obtained in [107] to estimate $\kappa_{(L,SiGe)}$ for $x = 0.4$ to $x = 0.8$. The amount of electron affinity, band gap, and mobility at room temperature as a function of SiGe mole fraction is extracted from Sentaurus TCAD library [11].

As a reference, an un-graded gated $Si_{0.6}Ge_{0.4}$ with temperature difference ΔT is simulated. Similar to chapter 6, metal gate work function for NW with $D_{it} = 0$ is varied between $3.7 \text{ eV} \leq \phi_m \leq 4.2 \text{ eV}$ to tune electron accumulations across the channel, to achieve the maximum possible output power. The mole fraction of SiGe is then graded with reference to $x = 0.4$ between mole fractions of 0 and 0.8, having equal metal gate work function ($\phi_m = 4.0 \text{ eV}$) as gated $Si_{0.6}Ge_{0.4}$ with maximum output power. Fig. 7.2 shows the graded ($x_1 = 0 \rightarrow x_2 = 0.8$) gated ($\phi_m = 4.0 \text{ eV}$) SiGe presenting the range of electron and mobility distribution across the NW at $\Delta T = 0 \text{ K}$.

Table 7.1 shows the studied graded structures with metal gate work function of 4.0 eV and $\Delta T = 0 \text{ K}$. Due to slight band bending at metal/SiGe interface, the electron density variation as the result of grading mole fraction is studied at $X = 0.01 \mu\text{m}$ and $X = 0.21 \mu\text{m}$, instead of $X = 0 \mu\text{m}$ and $X = 0.22 \mu\text{m}$ respectively (fig. 7.2 (b)).

$x_1 \rightarrow x_2$	$N_{C_{x1}} \rightarrow N_{C_{x2}} (\times 10^{19} \text{ cm}^{-3})$	$n_{(0.01,c)} \rightarrow n_{(0.21,c)} (\times 10^{18} \text{ cm}^{-3})$	$n_{(0.01,int)} \rightarrow n_{(0.21,int)} (\times 10^{18} \text{ cm}^{-3})$
0.4 $\rightarrow$ 0.4	2.14 $\rightarrow$ 2.14	1.110 $\rightarrow$ 1.110	1.980 $\rightarrow$ 1.980
0.3 $\rightarrow$ 0.5	2.33 $\rightarrow$ 1.95	1.151 $\rightarrow$ 1.067	2.143 $\rightarrow$ 1.815
0.2 $\rightarrow$ 0.6	2.51 $\rightarrow$ 1.77	1.187 $\rightarrow$ 1.019	2.317 $\rightarrow$ 1.660
0.1 $\rightarrow$ 0.7	2.70 $\rightarrow$ 1.58	1.220 $\rightarrow$ 0.9684	2.499 $\rightarrow$ 1.512
0 $\rightarrow$ 0.8	2.89 $\rightarrow$ 1.40	1.248 $\rightarrow$ 0.911	2.687 $\rightarrow$ 1.365

Table 7.1: Shows effective density of states of graded NW ($x_1 \rightarrow x_2$) at $x = x_1$ ($N_{C_{x1}}$ and $x = x_2$ ($N_{C_{x2}}$) respectively; and electron density at position of $X = 0.01 \mu\text{m}$ ($n_{(0.01,c)}$ for centre and $n_{(0.01,int)}$ for interface) and at $X = 0.21 \mu\text{m}$ ($n_{(0.21,c)}$ for centre and $n_{(0.21,int)}$ for interface). The NWs are in open circuit and $\Delta T = 0 \text{ K}$.

Since the amount of temperature dependent carrier concentration, effective density of states (table 7.1), and mobility at both ends of the NW are un-equal, swapping T_h

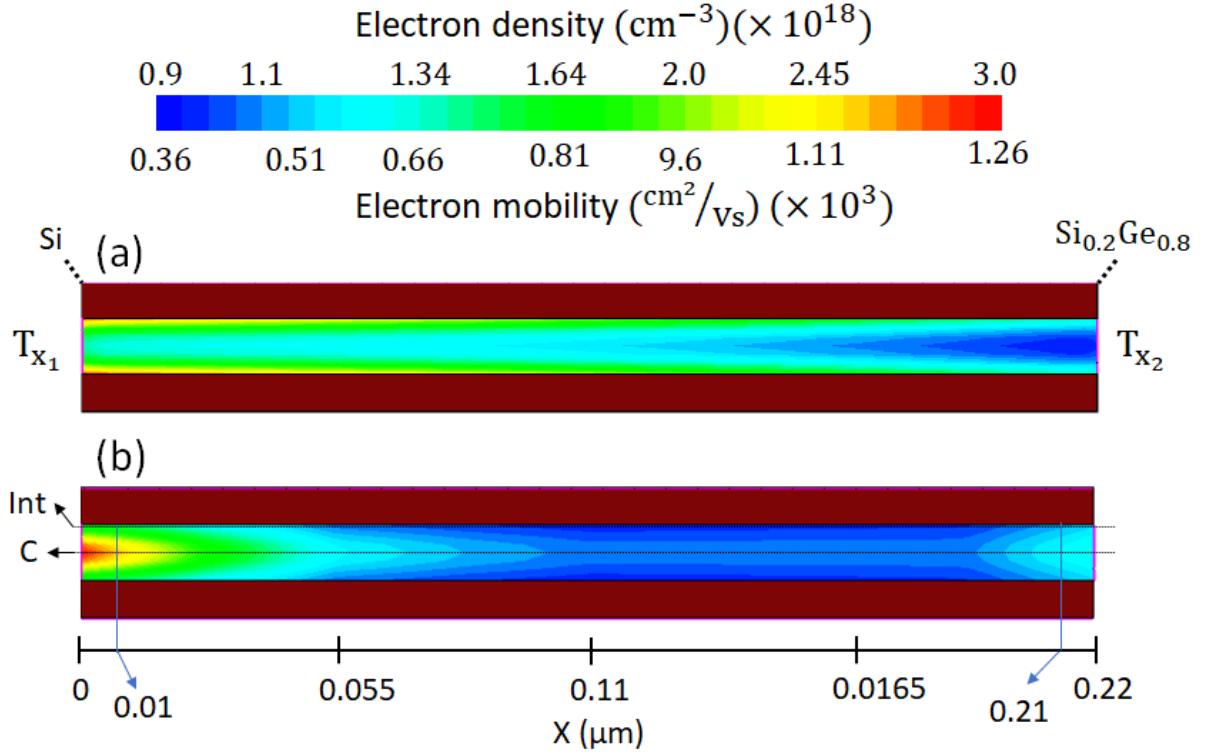


Figure 7.2: Shows (a) electron density, and (b) electron mobility of graded ($x_1 = 0 \rightarrow x_2 = 0.8$) SiGe with $\phi_m = 4.0$ eV metal gate at $\Delta T = 0$ K.

with T_c at sides of the NW to form ΔT would lead to different Seebeck coefficient and electrical conductivity. Therefore, two cases are studied, case 1: $T_{x_1} = T_h$ and $T_{x_2} = T_c$, and case 2: $T_{x_1} = T_c$ and $T_{x_2} = T_h$ (fig. 7.1 (b)).

As seen in section 4.4, both current and voltage across the nanowire can rise by increasing the total electric field of carriers ($\vec{E}_{c=n}$ for electrons and $\vec{E}_{c=p}$ for holes). $\vec{E}_n$ ($\vec{E}_p$) is highly dependant on temperature dependant gradient of electrons (holes) concentration, slope of E_c (E_v), and gradient of electron (hole) effective mass across the NW [11].

Fig. 7.3 (a) & (b) shows the dependence of electron density (n) on temperature for the reference $\text{Si}_{1-x}\text{Ge}_x$ ($x = 0.4$) NW and the graded ($x_1 = 0 \rightarrow x_2 = 0.8$) SiGe NW. As temperature increases, the density of available states (N_c) and the probability of occupation of these states increases, which leads to an increase in electron concentration.

In case 1 ($T_{x_1} = 310$ K and $T_{x_2} = 300$ K), ΔT increases the gradient of electron density; while in case 2 ($T_{x_1} = 300$ K and $T_{x_2} = 310$ K), ΔT reduces the gradient. Fig. 7.3 (c) and (d) shows $\ln\left(\frac{N_c}{n}\right)$ -X of the studied SiGe NWs at $\Delta T = 0$ K and 10 K. Increasing $\ln\left(\frac{N_c}{n}\right)$ is vital to improve S_n (eq. 3.5) of non-degenerate semiconductors. The average $\ln\left(\frac{N_c}{n}\right)$ at the centre of the NW and $\Delta T = 10$ K for case 1, case 2, and referenced NW are 2.921, 2.885, and 2.914, respectively; and at the interface of Si/ SiO_2 are 2.324, 2.290, and 2.319 for case 1, case 2, and referenced NW, respectively.

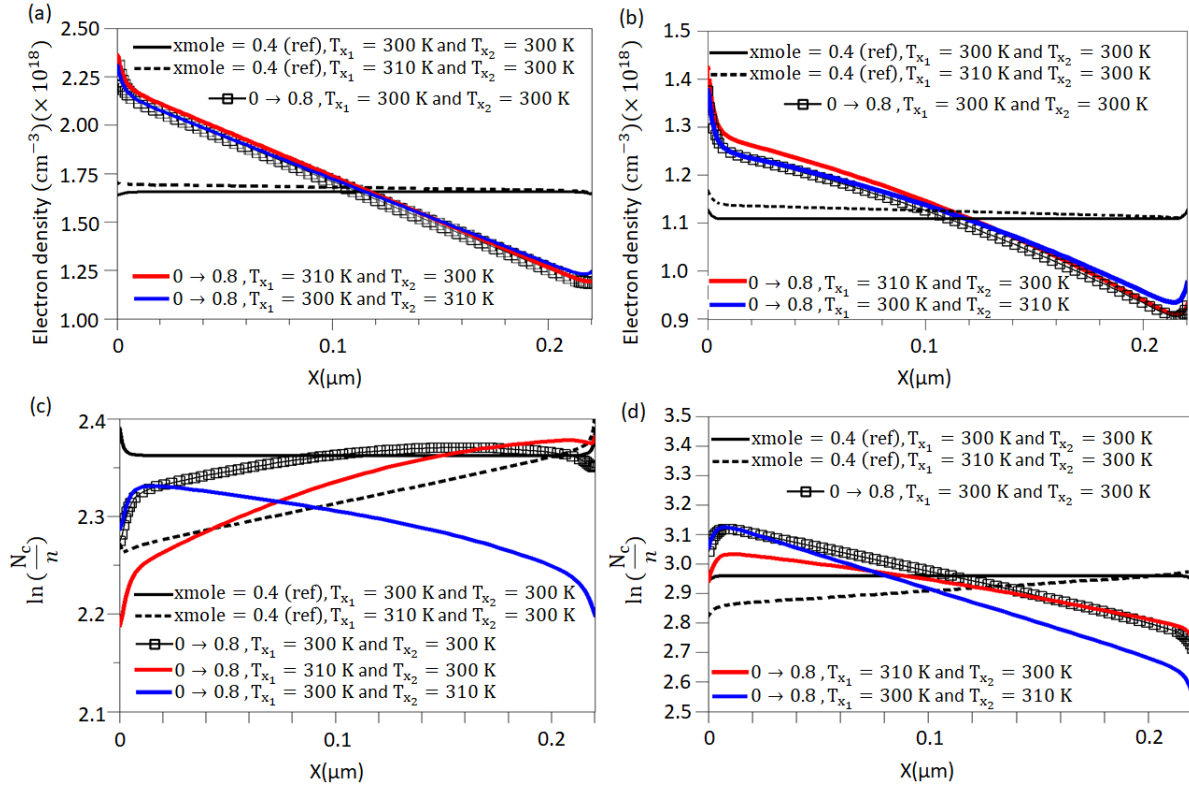


Figure 7.3: Shows electron density along the length of the gated ($\phi_m = 4$ eV) graded ($x_1 = 0 \rightarrow x_2 = 0.8$) and un-graded SiGe, plotted at (a) interface and (b) centre shown in fig 7.2. $\ln\left(\frac{N_c}{n}\right)$ -X of the gated ($\phi_m = 4$ eV) graded ($x_1 = 0 \rightarrow x_2 = 0.8$) and un-graded SiGe, plotted at (c) interface and (d) centre. The NWs are in open circuit.

Fig. 7.4 shows conduction bands (E_c) of gated ($\phi_m = 4$ eV) graded ($x_1 = 0 \rightarrow x_2 = 0.8$) SiGe, compared to gated ($\phi_m = 4$ eV) un-graded ($x = 0.4$ eV) SiGe with $\Delta T = 0$ K and $\Delta T = 10$ K in open circuit. As seen in fig 7.4, the gap between conduction bands of graded NW

CHAPTER 7. GRADING CARRIER DENSITY TO OPTIMISE THERMO-ELECTRIC POWER GENERATION

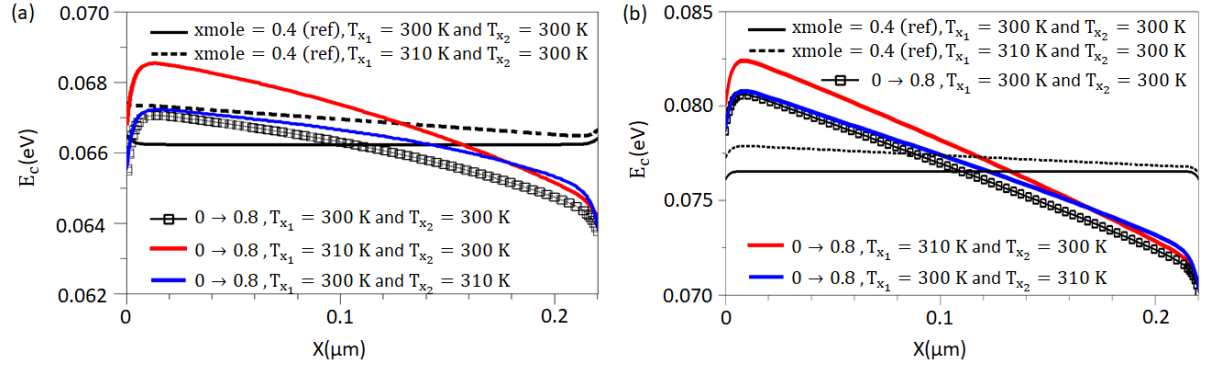


Figure 7.4: Shows E_c along the length of the gated ($\phi_m = 4$ eV) graded ($x_1 = 0 \rightarrow x_2 = 0.8$) and un-grdaed SiGe, plotted at (a) interface (Int) and (b) centre of the NWs shown in fig 7.2. The nanowires are in open circuit.

at $\Delta T = 10$ K and graded NW with $\Delta T = 0$ K is higher for case 1 ($T_{x_1} = 310$ K and $T_{x_2} = 300$ K) than case 2 ($T_{x_1} = 300$ K and $T_{x_2} = 310$ K). This difference is due to dissimilarity in $k_B T_n \ln(\frac{N_c}{n})$ at both ends of the graded NW. In addition, larger conduction band energy difference for case 1 than case 2, results in higher $\frac{dE_c}{dx}$, and therefore higher internal electric field (E_{int}), for case 1 than case 2. Similar direction of conduction band gradient (fig 7.4) with electron density slope (fig 7.3), aligns the current due to internal electric field in the same direction as current resulted by diffusion of carriers from T_h to T_c .

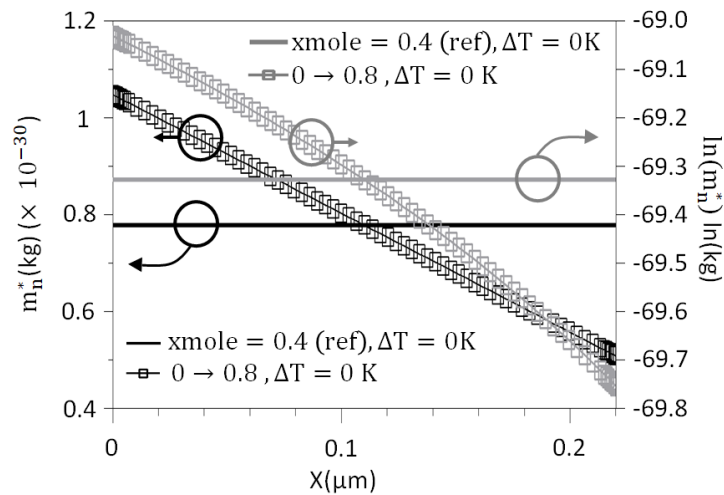


Figure 7.5: Shows m_n^* along the length of un-graded ($x = 0.4$) and graded ($x_1 = 0 \rightarrow x_2 = 0.8$) NWs with $\Delta T = 0$ K.

Figure 7.5 shows the effective mass of studied NWs along their length. As explained in chapter 4, the model for m_c^* calculation of alloys assumes the carrier effective mass to be temperature independent. Therefore, the third term $\left(\frac{d(\ln m_c^*)}{dx}\right)$ is solely dependant to variation of $N_c(300K)$ (or $N_v(300K)$) as a function of mole fraction. Although $\left(\frac{d(\ln m_c^*)}{dx}\right)$ is equal for both cases (case 1 and case 2), swapping the hot source would lead to dissimilar $\left(\frac{1.5k_B T_c \nabla \ln m_c^*}{q}\right)$. This is because T_c across the channel of case 1 is different from case 2.

Other than $\vec{E}_n$, electrical conductivity (σ_n) has high impact on the generated current. Fig 7.6 (a) shows the electron density of the graded NW ($x_1 = 0 \rightarrow x_2 = 0.8$) with $\Delta T = 0$ K, 10 K and 90 K. As expected, increase of electron density due to rise of temperature, reduces the electron mobility relatively (fig 7.6 (b)). Mole fraction dependent mobility and electron density leads to non-uniform σ across the nanowire. σ at hot side of the case 1 ($T_{x_1} = T_h$ and $T_{x_2} = T_c$) is higher than hot side of case 2 ($T_{x_1} = T_c$ and $T_{x_2} = T_h$).

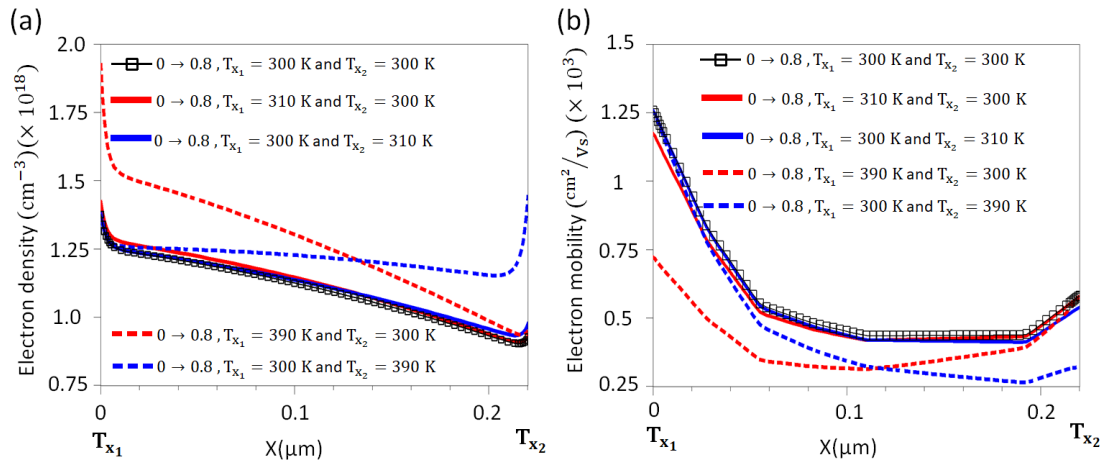


Figure 7.6: Shows (a) electron density and (b) electron mobility of the graded NW ($x_1 = 0 \rightarrow x_2 = 0.8$) in open circuit with $\Delta T = 0$ K, 10 K, and 90 K. The graphs are plotted for the centre of NW's cross section.

Fig. 7.7 shows the maximum output power of gated ($\phi_m = 4$ eV) graded ($x_1 = 0 \rightarrow x_2 = 0.8$) and un-graded structures connected to load resistor (R_L), when $R_L = R$, as a function of temperature. As seen in fig 7.7, the maximum output power for case 1 of graded structure ($x_1 = 0 \rightarrow x_2 = 0.8$) is 1.326 times higher than the un-graded structure

($x = 0.4$). However, output power of gated ($\phi_m = 4$ eV) ungraded ($x = 0.4$) structure is 1.213 times higher than case 2 of graded ($x_1 = 0 \rightarrow x_2 = 0.8$) structure at $\Delta T = 90$ K.

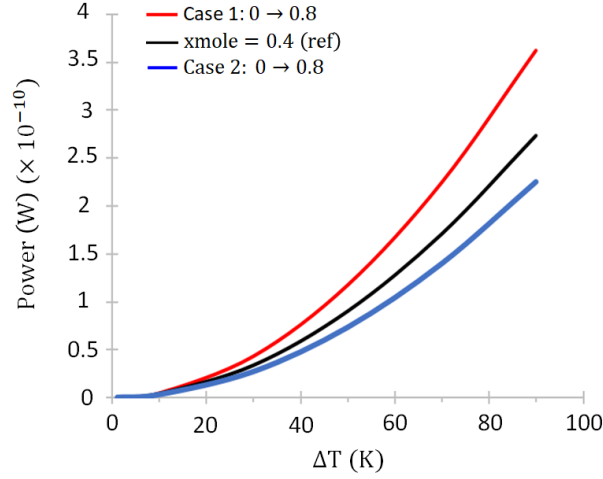


Figure 7.7: Shows output power as a function of ΔT for gated ($\phi_m = 4.0$ eV) graded ($x_1 = 0 \rightarrow x_2 = 0.8$) structures connected to load resistor (R_L) in a closed circuit, compared to gated ($\phi_m = 4.0$ eV) un-graded ($x = 0.4$) structure.

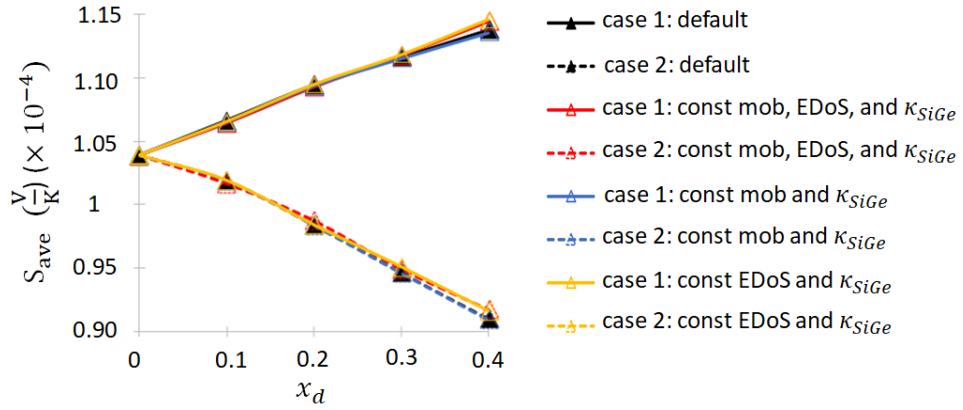


Figure 7.8: $S_{ave}-x_d$ for the gated ($\phi_m = 4$ eV) graded ($x_1 = 0.4 - x_d \rightarrow x_2 = 0.4 + x_d$) NWs in a closed circuit. S is studied for default values of parameters and setting one or more parameters to a constant (const) value. mob and EDoS stand for mobility and carrier effective density of states respectively. The NWs are connected to a load resistor, where $R_L = R$, in a closed circuit.

As explained earlier, due to graded mole fraction across the NW, carrier density, N_c , and mobility are dissimilar at both ends of the channel. To better understand the effect of these parameters on average Seebeck coefficient (S_{ave}) and σ , one has to deliberately

set the initial amount of one or all of these parameters to a constant value. The initial amount is the value of the parameter at $\Delta T = 0$ K, prior to its decrease or increase as a response to temperature. The constant mobility, constant carrier effective density of states, and constant κ_{SiGe} are equal to their values for un-graded NW with $x = 0.4$. Fig. 7.8 shows S_{ave} as a function of x_d ($x_1 = 0.4 - x_d \rightarrow x_2 = 0.4 + x_d$). As expected, setting mobility and κ_{SiGe} to a constant value would not influence the S_{ave} . However, setting N_c to a constant amount, leads to a slight increase in both cases. As the consequence of constant N_c , the gradient of E_c and carrier density experience a slight reduction, while $\left(\frac{d(\ln m_c^*)}{dx}\right)$ becomes equal to zero. $\left(\frac{d(\ln m_c^*)}{dx}\right) = 0$ leads to higher S_{ave} for graded NWs with constant N_c than graded NWs with default parameters.

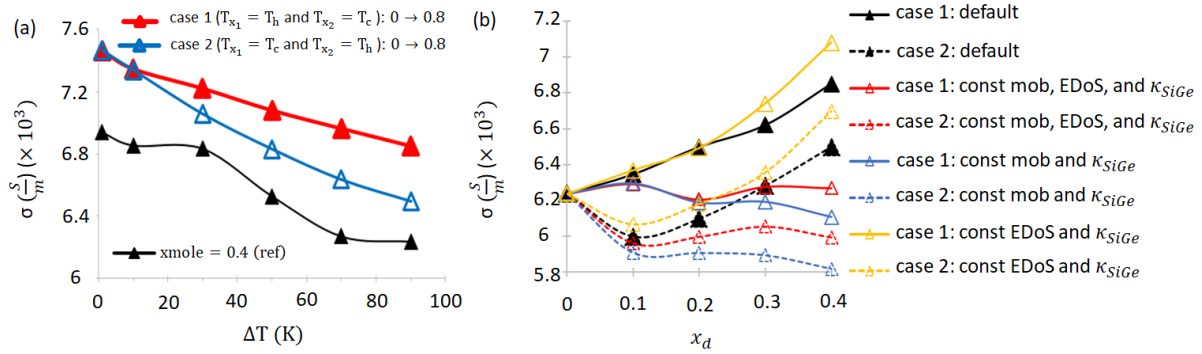


Figure 7.9: Shows (a) σ - ΔT for gated ($\phi_m = 4$ eV) graded ($x_1 = 0 \rightarrow x_2 = 0.8$) NW compared to gated ($\phi_m = 4$ eV) un-graded ($x = 0.4$). (b) σ - x_d for gated ($\phi_m = 4$ eV) graded ($x_1 = 0.4 - x_d \rightarrow x_2 = 0.4 + x_d$) NWs with $\Delta T = 90$ K. σ is studied for default values of parameters and setting one or more parameters to a constant (const) value. mob and EDoS stand for mobility and carrier effective density of states respectively. The NWs are connected to a load resistor, where $R_L = R$, in a closed circuit.

Fig 7.9 shows the response of σ to grading and ΔT , when NWs are connected to R_L in a closed circuit. The product of electron density and mobility of case 1 leads to higher σ than case 2. For default values of mobility and N_c , graded NWs have higher σ than un-graded NW, due to lower mobility of un-graded NW. Fig 7.9 (b) clarifies the importance of having high mobility materials for achieving high σ . For case 1: default and case 2: default, the electron mobility is between $450 \frac{cm^2}{Vs}$ and $1417 \frac{cm^2}{Vs}$; whereas, the

assumed constant electron mobility for graded NWs is $450 \frac{cm^2}{Vs}$, which is the electron mobility of un-graded nanowire with $x = 0.4$.

Fig 7.10 shows the power factor and output power of the graded NWs as the consequence of modifying the mentioned parameters, when $\Delta T = 90$ K and $R_L = R$.

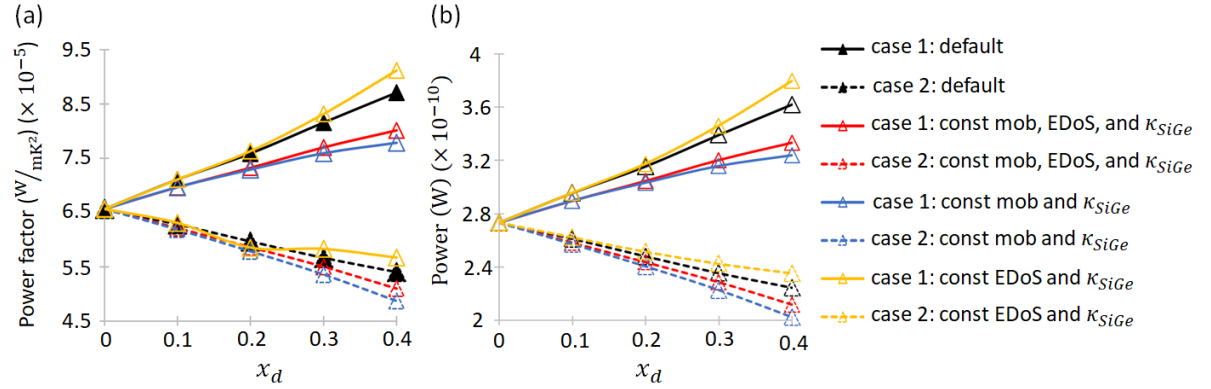


Figure 7.10: Shows (a) power factor and (b) output power of gated ($\phi_m = 4$ eV) graded ($x_1 = 0.4 - x_d \rightarrow x_2 = 0.4 + x_d$) NWs with $\Delta T = 90$ K and $R_L = R$.

7.2 Grading the area of gated Si NW

In this work, the area of gated intrinsic Si NW is graded with reference to un-graded intrinsic Si with 12 nm diameter (d_{ref}), fig 7.11. The carrier density at the core of the Si grades along the length of the NW, as area is graded. Similar to section 7.1, the graded Si with 220 nm length is covered by 8 nm thickness of SiO_2 (d_{ox}) and a 2D metal gate. The

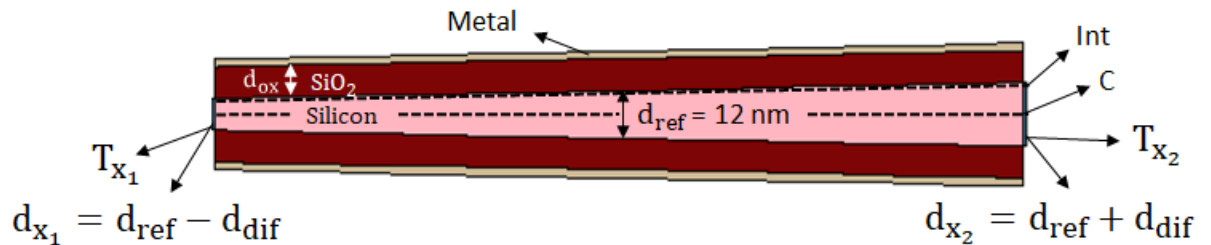


Figure 7.11: Shows the cross section of graded area of Si with reference to 12 nm diameter. d_{x1} is the diameter of Si at T_{x1} obtained by subtracting d_{dif} from d_{ref} ; and d_{x2} is the diameter of Si at T_{x2} due to adding d_{dif} to d_{ref} .

work function of the metal gate is 4.1 eV, which is the ϕ_m leading to maximum output power for un-graded Si NW with 12 nm diameter. In addition, the work function of 2D metal contacts are chosen such to form approximately flat band at metal/Si interface.

κ_{ox} is kept constant at $0.014 \frac{W}{cmK}$ [4]; and Connolly thermal conductivity model [11] is used to vary lattice thermal conductivity of Si with respect to its diameter. The thickness (diameter) dependence parameter of this model is tuned such to approximately match with the shown diameter dependence $\kappa_{(L,Si)}$ results in [60]. Unlike section 7.1, the m_n^* is temperature dependant; and $N_c(300K)$ and $N_v(300K)$ of Si is constant, since a single non-compound material is used. The electron density across the graded NWs are shown in table 7.2.

$d_{ref} - d_{dif} \rightarrow d_{ref} + d_{dif}$ (nm)	$n_{(0.01,c)} \rightarrow n_{(0.21,c)} (\times 10^{18} cm^{-3})$	$n_{(0.01,int)} \rightarrow n_{(0.21,int)} (\times 10^{18} cm^{-3})$
12 $\rightarrow$ 12	0.687 $\rightarrow$ 0.687	0.965 $\rightarrow$ 0.965
11 $\rightarrow$ 13	0.753 $\rightarrow$ 0.630	1.031 $\rightarrow$ 0.913
10 $\rightarrow$ 14	0.830 $\rightarrow$ 0.583	1.104 $\rightarrow$ 0.867
9 $\rightarrow$ 15	0.925 $\rightarrow$ 0.539	1.191 $\rightarrow$ 0.824
8 $\rightarrow$ 16	1.032 $\rightarrow$ 0.502	1.295 $\rightarrow$ 0.789

Table 7.2: Shows electron density of graded NW ($d_{ref} - d_{dif} \rightarrow d_{ref} + d_{dif}$) at position of $X = 0.01 \mu m$ ($n_{(0.01,c)}$ for centre and $n_{(0.01,int)}$ for interface) and at $X = 0.21 \mu m$ ($n_{(0.21,c)}$ for centre and $n_{(0.21,int)}$ for interface). The NWs are in open circuit and $\Delta T = 0K$.

Fig 7.12 shows the electron density and conduction band of the graded NW with $d_{x_1} = 11$ nm and $d_{x_2} = 13$ nm. Unlike graded SiGe, the sign of conduction band gradient is opposite to carrier concentration gradient, leading to a bottleneck in increasing overall current and Seebeck coefficient. As shown in chapter 4, electron mass in Si is dependent to lattice temperature; meaning that the mass gradient of case 1 ($T_{x_1} = T_h$ and $T_{x_2} = T_c$), case 2 ($T_{x_1} = T_c$ and $T_{x_2} = T_h$), and un-graded NWs are equal, under the condition of having equal ΔT . Equal mass gradient, for the studied NWs (with electrons as majority carriers), indicate that S modification is highly dependent to tuning the conduction band gradient with the electron density slope. In addition, the current can be further increased by tuning the carrier concentration and graded area of the NW, to achieve

CHAPTER 7. GRADING CARRIER DENSITY TO OPTIMISE THERMO-ELECTRIC POWER GENERATION

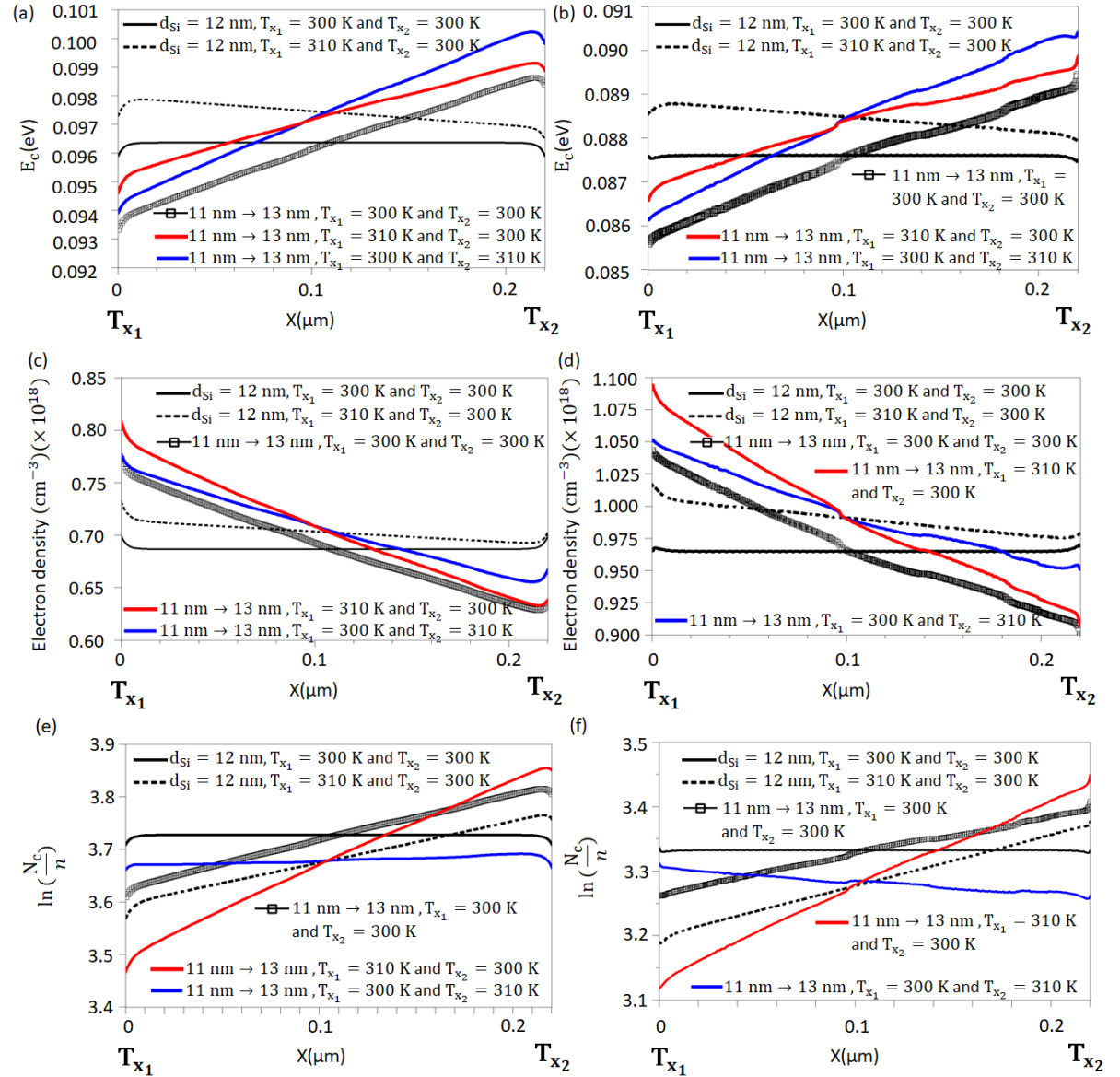


Figure 7.12: Shows E_c at the (a) centre and (b) interface; electron density at the (c) centre and (d) interface; and $\ln\left(\frac{N_c}{n}\right)$ - X at the (e) centre and (f) interface of the gated ($\phi_m = 4.1$ eV) graded ($d_{x1} = 11$ nm $\rightarrow$ $d_{x2} = 13$ nm) NWs compared to the gated ($\phi_m = 4.1$ eV) un-graded ($d_{Si} = 12$ nm). The NWs are in open circuit.

the maximum possible σ . Fig. 7.12 (e) and (f) shows $\ln\left(\frac{N_c}{n}\right)$ along the X -direction of the studied Si NWs at $\Delta T = 0$ K and 10 K. The average $\ln\left(\frac{N_c}{n}\right)$ at the centre of the NW and $\Delta T = 10$ K for case 1, case 2, and referenced NW are 3.684, 3.679, and 3.682, respectively; and at the interface are 3.287, 3.282, and 3.285 for case 1, case 2, and

referenced NW, respectively. Although approximately equal average $\ln\left(\frac{N_c}{n}\right)$ is seen for the studied Si NWs, the scattering mechanism parameter (eq. 3.5) are different for the graded and ungraded Si NWs. This is due to the difference in amount of electron-phonon scattering, caused by perpendicular electric field (enormal), across the length of graded and un-graded Si NWs.

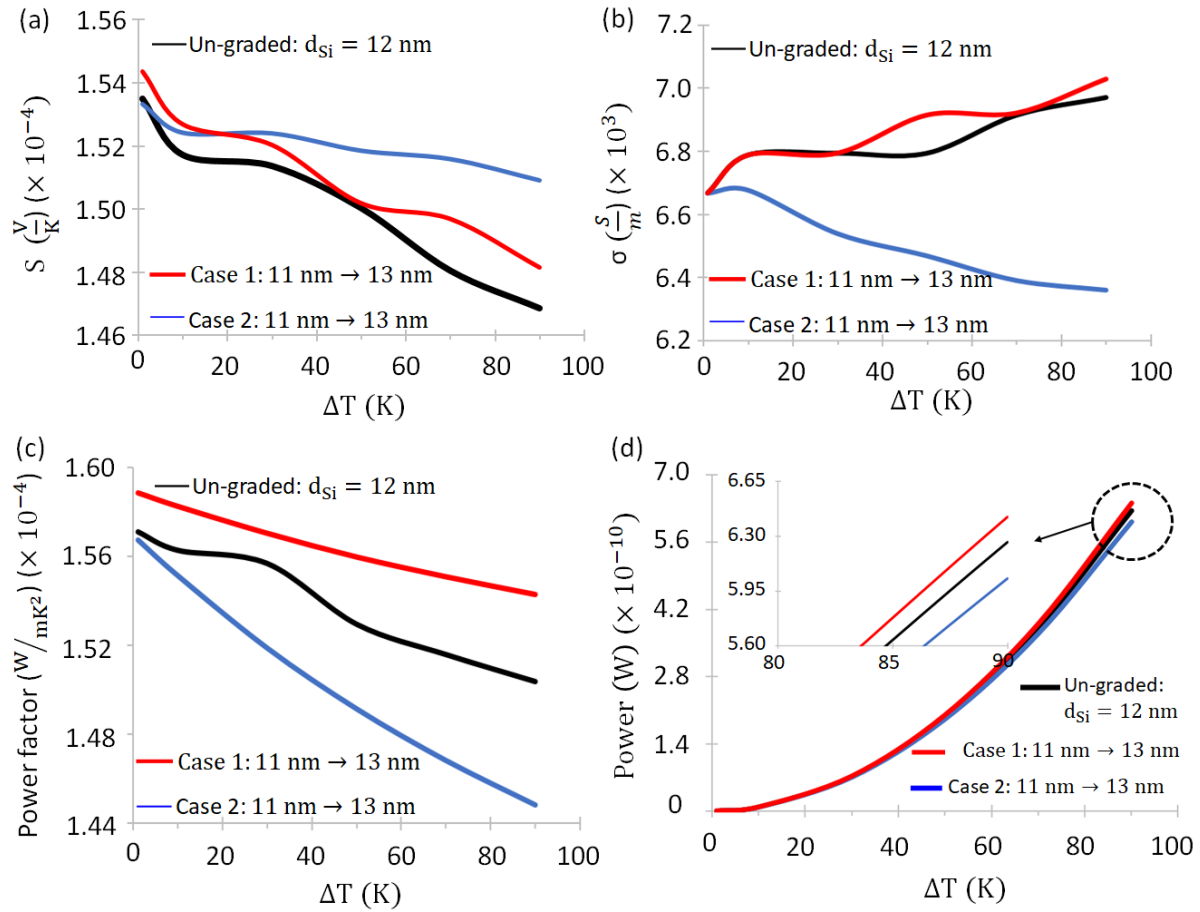


Figure 7.13: Shows (a) S , (b) σ , (c) power factor, and (d) power of gated ($\phi_m = 4.1$ eV) graded ($d_{x_1} = 11$ nm and $d_{x_2} = 13$) Si compared to gated ($\phi_m = 4.1$ eV) un-graded ($d_{Si} = 12$ nm) Si. The NWs are connected to a load resistor with $R_L = R$.

The optimal value of power factor in graded Si structure was achieved for the NW with $d_{x_1} = 11$ nm and $d_{x_2} = 13$ nm. Fig 7.13 compares Seebeck coefficient, σ , and power factor of the mentioned graded ($d_{x_1} = 11$ nm and $d_{x_2} = 13$) NW with un-graded (d_{Si}) NW. As seen in fig 7.13 (a), lower difference of temperature dependence E_c with electron

density gradients have led to lower S for case 1 than case 2, for $\Delta T > 20$ K. Seebeck coefficient of un-graded NW was found to be lower than graded structure for all ΔT . In addition, electron density grading in the NW resulted in greater (or equal) σ for case 1 than the referenced NW. The obtained results for S and σ have led to the highest power factor for case 1.

Fig 7.13 (d) shows the maximum power for the graded and un-graded structure. The maximum achieved power for case 1 of graded structure ($d_{x1} = 11 \text{ nm} \rightarrow d_{x1} = 13 \text{ nm}$) is 1.03 times higher than un-graded at $\Delta T = 90$ K. Unlike SiGe, the opposite direction of E_c gradient with electron density gradient, limits the improvement of power via grading the carrier concentration across the Si.

Fig 7.14 shows the power factor and power of gated ($\phi_m = 4.1 \text{ eV}$) graded ($d_{ref} - d_{dif} \rightarrow d_{ref} + d_{dif}$) NWs as a function of d_{dif} .

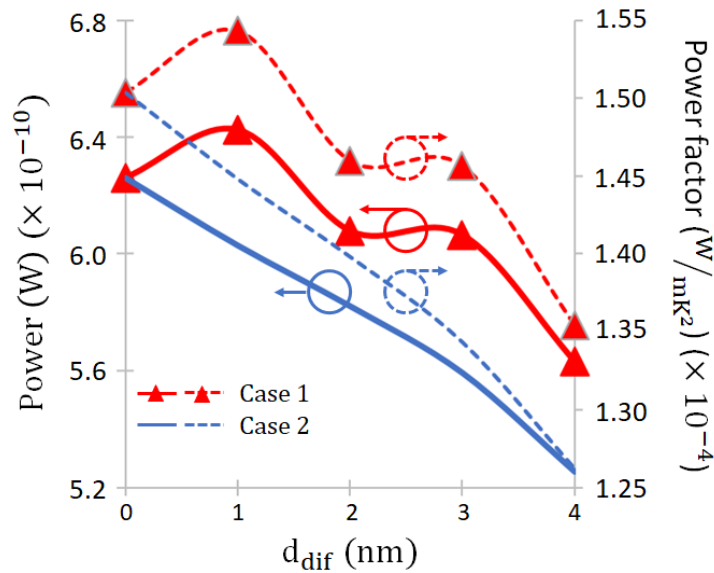


Figure 7.14: Shows maximum power and power factor of gated ($\phi_m = 4.1 \text{ eV}$) graded ($d_{ref} - d_{dif} \rightarrow d_{ref} + d_{dif}$) NWs at $\Delta T = 90$ K, as a function of d_{dif} . The NW are connected to a load resistor, having $R_L = R$.

7.3 Conclusion

In this work, grading the electron density of a gated NW with work function ϕ_m on improving its output power was studied. $Si_{1-x}Ge_x$ was graded via grading its mole fraction (x) from $x = x_1$ to $x = x_2$, leading to grading of carrier effective density of states (N_c for electrons and N_v for holes), carrier effective mass (m_n^* for electrons and m_p^* for holes), and carrier concentration. However, Si was graded by increasing the diameter along the length of the NW, resulted in variation of electron density and area; while effective density of states and carrier mass remained constant.

At $\phi_m < 4.65$ eV, the conduction band slope of the graded $Si_{1-x}Ge_x$ gets in the same direction as electron density gradient. Similar direction of these gradients led to 1.32 times higher output power generation for the gated ($\phi_m = 4.0$ eV) graded ($x_1 = 0 \rightarrow x_2 = 0.8$) structure, than the gated ($\phi_m = 4.0$ eV) un-graded ($x = 0.4$) NW, mainly due to increase of total electric field. However, the opposite direction of the mentioned gradients in gated ($\phi_m = 4.1$ eV) graded Si limits the ability to increase the voltage difference and current, compared to un-graded Si NW.

SUMMARY AND CONCLUSION

The main aims of this project was using gated intrinsic metal/semiconductor/metal structures for carrier modulation in thermo-electric power generation, carrier injection control for temperature sensing, and forming symmetric I-V characteristics between n-FET and p-FET. Proposing and developing the mentioned doping-free devices improve their performance due to elimination of ionised impurity scattering, and opportunity to further down-scale the devices.

Carrier modulation via gating an intrinsic Si was found to improve thermo-electric power generation by 2.2 times compared to doped structures, due to minimisation of ionised impurity scattering. This study was followed by grading the carrier concentration of both Si and SiGe via grading the area and mole fraction respectively, aiming to further increase the output power via introduction of an internal electric field (E_{int}). Unlike Si carrier grading, which the opposite direction of current due to internal electric field (E_{int}) with current resulted by thermal diffusion limits the increase of power, grading the mole fraction of SiGe has significant impact on increasing power generation. Carrier modulation ($\phi_m < 4.65$ eV) in gated SiGe grades the conduction band, and therefore E_{int} , in the same direction as diffusion of carriers, where ϕ_m is metal gate work function.

Similar direction of current generated by E_{int} with the generated current due to thermal diffusion increases the overall power.

In addition, carrier modulation in gated structures introduces the opportunity to propose a temperature sensor, with the ability to sense the temperature in two different methods. In addition to linear relation of temperature with the generated current, a tunable barrier via applying gate voltage can keep the current constant at all temperatures. The required gate voltage to maintain the constant current is the reading of temperature.

Finally, the ability of forming symmetric I-V characteristics between n-FET and p-FET was studied by introducing a bridge between the FETs. In this method, higher current of n-FET was degraded, and therefore aligned with the p-FET, by introducing a capacitor, connecting the program gate of p-FET to the middle of the n-FET channel. This method have led to the highest achieved current symmetry, compared to previous works. However, the symmetry can not be achieved for both configurations.

BIBLIOGRAPHY

- [1] WM Weber, A Heinzig, J Trommer, D Martin, M Grube, and T Mikolajick.
Reconfigurable nanowire electronics—a review.
Solid-State Electronics, 102:12–24, 2014.
- [2] JM Dorkel and Ph Leturcq.
Carrier mobilities in silicon semi-empirically related to temperature, doping and injection level.
Solid-State Electronics, 24(9):821–825, 1981.
- [3] Gordon Moore.
Moore’s law.
Electronics Magazine, 38(8):114, 1965.
- [4] Simon M Sze and Kwok K Ng.
Physics of semiconductor devices.
John wiley & sons, 2006.
- [5] Jan M Rabaey, Anantha P Chandrakasan, and Borivoje Nikolić.
Digital integrated circuits: a design perspective, volume 7.
Pearson Education Upper Saddle River, NJ, 2003.
- [6] Behzad Razavi.
Design of analog CMOS integrated circuits.
Tata McGraw-Hill Education, 2017.
- [7] Hideaki Tsuchiya and Yoshinari Kamakura.
Carrier Transport in Nanoscale MOS Transistors.
John Wiley & Sons, 2016.
- [8] KM Gupta and Nishu Gupta.
Pn junctions and their breakdown mechanisms.

- In *Advanced Semiconducting Materials and Devices*, pages 193–234. Springer, 2016.
- [9] Manijeh Razeghi.
Fundamentals of solid state engineering.
Springer, 2006.
- [10] BL Sharma.
Metal-semiconductor Schottky barrier junctions and their applications.
Plenum publishing corporation, 1984.
- [11] Synopsys.
Sentaurus Device User Guide TCAD Version k-2015.06.
2015.
- [12] Walter M Weber, Jens Trommer, Dominik Martin, Matthias Grube, André Heinzig, and Thomas Mikolajick.
Reconfigurable nanowire electronics device principles and circuit prospects.
In *2013 Proceedings of the European Solid-State Device Research Conference (ESSDERC)*, pages 246–251. IEEE, 2013.
- [13] MS Tyagi.
Physics of schottky barrier junctions.
In *Metal-semiconductor Schottky barrier junctions and their applications*, pages 1–60. Springer, 1984.
- [14] Emlyn Huw Rhoderick.
Metal-semiconductor contacts.
IEE Proceedings I-Solid-State and Electron Devices, 129(1):1, 1982.
- [15] FA Padovani.
The voltage-current characteristic of metal-semiconductor contacts.
In *Semiconductors and Semimetals*, volume 7, pages 75–146. Elsevier, 1971.
- [16] Xia An, Ru Huang, Baoying Zhao, Xing Zhang, and Yangyuan Wang.
Design guideline of an ultra-thin body SOI MOSFET for low-power and high-performance applications.
Semiconductor science and technology, 19(3):347, 2003.

- [17] Ravi Shankar Pal, Savitesh Sharma, and S Dasgupta.
Recent trend of FinFET devices and its challenges: A review.
In *2017 Conference on Emerging Devices and Smart Systems (ICEDSS)*, pages 150–154. IEEE, 2017.
- [18] Kunihiro Suzuki, Tetsu Tanaka, Yoshiharu Tosaka, Hiroshi Horie, and Yoshihiro Arimoto.
Scaling theory for double-gate SOI MOSFET's.
IEEE Transactions on Electron Devices, 40(12):2326–2329, 1993.
- [19] Sufen Wei, Guohe Zhang, Zhibiao Shao, Li Geng, and Cheng-Fu Yang.
Analysis of a high-performance ultra-thin body ultra-thin box silicon-on-insulator MOSFET with the lateral dual-gates: featuring the suppression of the DIBL.
Microsystem technologies, 24(10):3949–3956, 2018.
- [20] Chris Auth, C Allen, A Blattner, D Bergstrom, M Brazier, M Bost, M Buehler, V Chikarmane, T Ghani, T Glassman, et al.
A 22nm high performance and low-power CMOS technology featuring fully-depleted tri-gate transistors, self-aligned contacts and high density MIM capacitors.
In *2012 symposium on VLSI technology (VLSIT)*, pages 131–132. IEEE, 2012.
- [21] Jean-Pierre Colinge et al.
FinFETs and other multi-gate transistors, volume 73.
Springer, 2008.
- [22] John P Uyemura.
Circuit design for CMOS VLSI.
Springer Science & Business Media, 2012.
- [23] Adelmo Ortiz-Conde, Francisco J García-Sánchez, Juan Muci, Alberto Terán Barrios, Juin J Liou, and Ching-Sung Ho.
Revisiting MOSFET threshold voltage extraction methods.
Microelectronics Reliability, 53(1):90–104, 2013.
- [24] Chinmay K Maiti.
Introducing Technology Computer-Aided Design (TCAD): Fundamentals, Simulations, and Applications.
CRC Press, 2017.

- [25] Iraj Sadegh Amiri, Hossein Mohammadi, and Mahdiar Hosseinghadiry. *Device Physics, Modeling, Technology, and Analysis for Silicon MESFET*. Springer, 2019.
- [26] Synopsys. Inspect4: Extracting standard parameters. http://www.sentaurus.dsod.pl/insp/insp_d.html, 2015. Last accessed 22 August 2020.
- [27] Ghader Darbandy, Martin Claus, and Michael Schröter. High-performance reconfigurable Si nanowire field-effect transistor based on simplified device design. *IEEE Transactions on Nanotechnology*, 15(2):289–294, 2016.
- [28] André Heinzig, Stefan Slesazeck, Franz Kreupl, Thomas Mikolajick, and Walter M Weber. Reconfigurable silicon nanowire transistors. *Nano letters*, 12(1):119–124, 2012.
- [29] Jian Zhang, Michele De Marchi, Davide Sacchetto, Pierre-Emmanuel Gaillardon, Yusuf Leblebici, and Giovanni De Micheli. Polarity-controllable silicon nanowire transistors with dual threshold voltages. *IEEE Transactions on Electron Devices*, 61(11):3654–3660, 2014.
- [30] Thomas Mikolajick, A Heinzig, J Trommer, T Baldauf, and WM Weber. The RFET—a reconfigurable nanowire transistor and its application to novel electronic circuits and systems. *Semiconductor Science and Technology*, 32(4):043001, 2017.
- [31] Yann-Michel Niquet, Christophe Delerue, and Christophe Krzeminski. Effects of strain on the carrier mobility in silicon nanowires. *Nano letters*, 12(7):3545–3550, 2012.
- [32] André Heinzig, Thomas Mikolajick, Jens Trommer, Daniel Grimm, and Walter M Weber. Dually active silicon nanowire transistors and circuits with equal electron and hole transport. *Nano letters*, 13(9):4176–4181, 2013.

- [33] Michele De Marchi, Davide Sacchetto, Stefano Frache, Jian Zhang, P-E Gaillardon, Yusuf Leblebici, and Giovanni De Micheli.
Polarity control in double-gate, gate-all-around vertically stacked silicon nanowire FETs.
In *2012 International Electron Devices Meeting*, pages 8–4. IEEE, 2012.
- [34] Massimo Mongillo, Panayotis Spathis, Georgios Katsaros, Pascal Gentile, and Silvano De Franceschi.
Multifunctional devices and logic gates with undoped silicon nanowires.
Nano letters, 12(6):3074–3079, 2012.
- [35] F Wessely, T Krauss, and U Schwalke.
CMOS without doping: Multi-gate silicon-nanowire field-effect-transistors.
Solid-state electronics, 70:33–38, 2012.
- [36] Jens Trommer, Maik Simon, Stefan Slesazeck, Walter M Weber, and Thomas Mikolajick.
Eliminating charge sharing in clocked logic gates on the device level employing transistors with multiple independent inputs.
In *ESSDERC 2019-49th European Solid-State Device Research Conference (ESSDERC)*, pages 134–137. IEEE, 2019.
- [37] Jens Trommer, André Heinzig, Tim Baldauf, Stefan Slesazeck, Thomas Mikolajick, and Walter M Weber.
Functionality-enhanced logic gate design enabled by symmetrical reconfigurable silicon nanowire transistors.
IEEE Transactions on Nanotechnology, 14(4):689–698, 2015.
- [38] Jens Trommer, André Heinzig, Tim Baldauf, Thomas Mikolajick, Walter M Weber, Michael Raitza, and Marcus Völp.
Reconfigurable nanowire transistors with multiple independent gates for efficient and programmable combinational circuits.
In *2016 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, pages 169–174. IEEE, 2016.
- [39] M Simon, J Trommer, B Liang, D Fischer, T Baldauf, MB Khan, A Heinzig, M Knaut, YM Georgiev, A Erbe, et al.
A wired-AND transistor: Polarity controllable FET with multiple inputs.

- In *2018 76th Device Research Conference (DRC)*, pages 1–2. IEEE, 2018.
- [40] Alfred Grill, Stephen M Gates, Todd E Ryan, Son V Nguyen, and Deepika Priyadarshini.
Progress in the development and understanding of advanced low k and ultralow k dielectrics for very large-scale integrated interconnects,Âstate of the art.
Applied Physics Reviews, 1(1):011306, 2014.
- [41] Howard Tigelaar.
How transistor area shrank by 1 million fold, 2020.
- [42] Ameer F Roslan, F Salehuddin, ASM Zain, KE Kaharudin, and I Ahmad.
Enhanced performance of 19 single gate mosfet with high permittivity dielectric material.
Indonesian Journal of Electrical Engineering and Computer Science, 18(2):724–730, 2020.
- [43] Jengyi Yu, Prabhuram Gopalan, and Jeff Feng.
Comparative study of pe-bpsg and hdp-psg as pmd for 0.25/spl mu/m memory device.
In *Proceedings of the IEEE 1999 International Interconnect Technology Conference (Cat. No. 99EX247)*, pages 35–37. IEEE, 1999.
- [44] Yong-Jin Seo, Sang-Yong Kim, and Woo-Sun Lee.
Optimization of pre-metal dielectric (pmd) materials.
Journal of materials science: materials in electronics, 12(9):551–554, 2001.
- [45] Dai Ishikawa, Akinori Nakano, Shintaro Ueda, Hiroshi Kou, Hirofumi Arai, Akiko Kobayashi, Kiyohiro Matsushita, and Nobuyoshi Kobayashi.
Plasma-enhanced cvd low-k process enabling global planarity by controlling flowability.
In *IEEE International Interconnect Technology Conference*, pages 135–138. IEEE, 2014.
- [46] Denis Shamiryan, Thomas Abell, Francesca Iacopi, and Karen Maex.
Low-k dielectric materials.
Materials Today, 7(1):34–39, 2004.
- [47] C Jin, S Lin, and JT Wetzal.

- Evaluation of ultra-low-k dielectric materials for advanced interconnects.
Journal of electronic materials, 30(4):284–289, 2001.
- [48] Seokmo Hong, Chang-Seok Lee, Min-Hyun Lee, Yeongdong Lee, Kyung Yeol Ma, Gwangwoo Kim, Seong In Yoon, Kyuwook Ihm, Ki-Jeong Kim, Tae Joo Shin, et al.
Ultralow-dielectric-constant amorphous boron nitride.
Nature, 582(7813):511–514, 2020.
- [49] Alfred Grill.
Plasma enhanced chemical vapor deposited silicon dielectrics: from low-k to extreme low-k interconnect materials.
Journal of Applied Physics, 93(3):1785–1790, 2003.
- [50] D Yakimets, M Garcia Bardon, D Jang, P Schuddinck, Y Sherazi, P Weckx, K Miyaguchi, B Parvais, P Raghavan, A Spessot, et al.
Power aware FinFET and lateral nanosheet FET targeting for 3nm CMOS technology.
In *2017 IEEE International Electron Devices Meeting (IEDM)*, pages 20–4. IEEE, 2017.
- [51] Doyoung Jang, Dmitry Yakimets, Geert Eneman, Pieter Schuddinck, Marie Garcia Bardon, Praveen Raghavan, Alessio Spessot, Diederik Verkest, and Anda Mocuta.
Device exploration of nanosheet transistors for sub-7-nm technology node.
IEEE Transactions on Electron Devices, 64(6):2707–2713, 2017.
- [52] Jun-Sik Yoon, Jinsu Jeong, Seunghwan Lee, and Rock-Hyun Baek.
Multi- V_{th} strategies of 7-nm node nanosheet FETs with limited nanosheet spacing.
IEEE Journal of the Electron Devices Society, 6:861–865, 2018.
- [53] Davide Sacchetto, M Haykel Ben-Jamaa, Giovanni DeMicheli, and Yusuf Leblebici.
Fabrication and characterization of vertically stacked gate-all-around Si nanowire FET arrays.
In *2009 Proceedings of the European Solid State Device Research Conference*, pages 245–248. IEEE, 2009.

- [54] X Zhou, N Waldron, G Boccardi, F Sebaai, C Merckling, G Eneman, S Sioncke, L Nyns, A Opdebeeck, JW Maes, et al.
Scalability of InGaAs gate-all-around FET integrated on 300mm Si platform: Demonstration of channel width down to 7nm and Lg down to 36nm.
In *2016 IEEE Symposium on VLSI Technology*, pages 1–2. IEEE, 2016.
- [55] Tao Wang, Liang Lou, and Chengkuo Lee.
A junctionless gate-all-around silicon nanowire FET of high linearity and its potential applications.
IEEE electron device letters, 34(4):478–480, 2013.
- [56] Michele De Marchi, Davide Sacchetto, Jian Zhang, Stefano Frache, Pierre-Emmanuel Gaillardon, Yusuf Leblebici, and Giovanni De Micheli.
Top-down fabrication of gate-all-around vertically stacked silicon nanowire FETs with controllable polarity.
IEEE Transactions on Nanotechnology, 13(6):1029–1038, 2014.
- [57] Yida Li, Kavitha Buddharaju, Bui Cong Tinh, Navab Singh, and Sung Joo Lee.
Improved vertical silicon nanowire based thermoelectric power generator with polyimide filling.
IEEE electron device letters, 33(5):715–717, 2012.
- [58] Akiou Kikuchi, Akifumi Yao, Isamu Mori, Takahito Ono, and Seiji Samukawa.
Extremely low thermal conductivity of high density and ordered 10 nm-diameter silicon nanowires array.
Applied Physics Letters, 110(9):091908, 2017.
- [59] Allon I Hochbaum, Renkun Chen, Raul Diaz Delgado, Wenjie Liang, Erik C Garnett, Mark Najarian, Arun Majumdar, and Peidong Yang.
Enhanced thermoelectric performance of rough silicon nanowires.
Nature, 451(7175):163–167, 2008.
- [60] Li Shi.
Thermal and thermoelectric transport in nanostructures and low-dimensional systems.
Nanoscale and Microscale Thermophysical Engineering, 16(2):79–116, 2012.
- [61] Mildred S Dresselhaus, Gang Chen, Ming Y Tang, RG Yang, Hohyun Lee, DZ Wang, ZF Ren, J-P Fleurial, and Pawan Gogna.

- New directions for low-dimensional thermoelectric materials.
Advanced materials, 19(8):1043–1053, 2007.
- [62] G Jeffrey Snyder, Marco Soto, Randy Alley, David Koester, and Bob Conner.
Hot spot cooling using embedded thermoelectric coolers.
In *Twenty-Second Annual IEEE Semiconductor Thermal Measurement And Management Symposium*, pages 135–143. IEEE, 2006.
- [63] Peng Wang, Avram Bar-Cohen, Bao Yang, Gary L Solbrekken, and Ali Shakouri.
Analytical modeling of silicon thermoelectric microcooler.
Journal of Applied Physics, 100(1):014501, 2006.
- [64] FL Bakker, J Flipse, and BJ Van Wees.
Nanoscale temperature sensing using the seebeck effect.
Journal of Applied Physics, 111(8):084306, 2012.
- [65] Lars Rebenklau, Paul Gierth, Angelika Paproth, Klaus Irrgang, Lutz Lippmann, Axel Wodtke, Lars Niedermeyer, Klaus Augsburg, and Franz Bechtold.
Temperature sensors based on thermoelectric effect.
In *2015 European Microelectronics Packaging Conference (EMPC)*, pages 1–5. IEEE, 2015.
- [66] Yangyang Xin, Jian Zhou, and Gilles Lubineau.
A highly stretchable strain-insensitive temperature sensor exploits the seebeck effect in nanoparticle-based printed circuits.
Journal of Materials Chemistry A, 7(42):24493–24501, 2019.
- [67] Mohamed Hamid Elsheikh, Dhafer Abdulameer Shnawah, Mohd Faizul Mohd Sabri, Suhana Binti Mohd Said, Masjuki Haji Hassan, Mohamed Bashir Ali Bashir, and Mahazani Mohamad.
A review on thermoelectric renewable energy: Principle parameters that affect their performance.
Renewable and sustainable energy reviews, 30:337–355, 2014.
- [68] Ran He, Gabi Schierning, and Kornelius Nielsch.
Thermoelectric devices: a review of devices, architectures, and contact optimization.
Advanced Materials Technologies, 3(4):1700256, 2018.

- [69] Hyun-Sik Kim, Zachary M Gibbs, Yinglu Tang, Heng Wang, and G Jeffrey Snyder. Characterization of lorenz number with seebeck coefficient measurement. *APL materials*, 3(4):041506, 2015.
- [70] Chengyun Hua and Austin J Minnich. Importance of frequency-dependent grain boundary scattering in nanocrystalline silicon and silicon–germanium thermoelectrics. *Semiconductor Science and Technology*, 29(12):124004, 2014.
- [71] Ken Kurosaki, Aikebaier Yusufu, Yoshinobu Miyazaki, Yuji Ohishi, Hiroaki Muta, and Shinsuke Yamanaka. Enhanced thermoelectric properties of silicon via nanostructuring. *MATERIALS TRANSACTIONS*, 57(7):1018–1021, 2016.
- [72] Julian Goldsmid. *The physics of thermoelectric energy conversion*. Morgan & Claypool Publishers, 2017.
- [73] Dongliang Zhao and Gang Tan. A review of thermoelectric cooling: materials, modeling and applications. *Applied Thermal Engineering*, 66(1-2):15–24, 2014.
- [74] Neophytos Neophytou, Hossein Karamitaheri, and Hans Kosina. Use of field-effect density modulation to increase zT for si nanowires: A simulation study. *Journal of Electronic Materials*, 44(6):1599–1605, 2015.
- [75] DBM Klaassen. A unified mobility model for device simulation—I. model equations and concentration dependence. *Solid-State Electronics*, 35(7):953–959, 1992.
- [76] Neophytos Neophytou and Mischa Thesberg. Modulation doping and energy filtering as effective ways to improve the thermoelectric power factor. *Journal of Computational Electronics*, 15(1):16–26, 2016.
- [77] Benjamin M Curtin, Emilio A Codecido, Stephan Krämer, and John E Bowers.

- Field-effect modulation of thermoelectric properties in multigated silicon nanowires.
Nano letters, 13(11):5503–5508, 2013.
- [78] Igor Bejenari, Valeriu Kantser, and Alexander A Balandin.
Thermoelectric properties of electrically gated bismuth telluride nanowires.
Physical Review B, 81(7):075316, 2010.
- [79] Yuan Tian, Mohammed R Sakr, Jesse M Kinder, Dong Liang, Michael J MacDonald, Richard LJ Qiu, Hong-Jun Gao, and Xuan PA Gao.
One-dimensional quantum confinement effect modulated thermoelectric properties in InAs nanowires.
Nano letters, 12(12):6492–6497, 2012.
- [80] Wenjie Liang, Allon I Hochbaum, Melissa Fardy, Oded Rabin, Minjuan Zhang, and Peidong Yang.
Field-effect modulation of seebeck coefficient in single PbSe nanowires.
Nano letters, 9(4):1689–1693, 2009.
- [81] Jaeyun Moon, Ji-Hun Kim, Zack CY Chen, Jie Xiang, and Renkun Chen.
Gate-modulated thermoelectric power factor of hole gas in Ge–Si core–shell nanowires.
Nano letters, 13(3):1196–1202, 2013.
- [82] SA Dayeh, AV Gin, and ST Picraux.
Advanced core/multishell germanium/silicon nanowire heterostructures: Morphology and transport.
Applied Physics Letters, 98(16):163112, 2011.
- [83] Lincoln J Lauhon, Mark S Gudiksen, Deli Wang, and Charles M Lieber.
Epitaxial core–shell and core–multishell nanowire heterostructures.
Nature, 420(6911):57–61, 2002.
- [84] Yat Li, Jie Xiang, Fang Qian, Silvija Gradecak, Yue Wu, Hao Yan, Douglas A Blom, and Charles M Lieber.
Dopant-free GaN/AlN/AlGaIn radial nanowire heterostructures as high electron mobility transistors.
Nano letters, 6(7):1468–1473, 2006.

- [85] Luying Li, DJ Smith, P Madras, E Dailey, J Drucker, and MR McCartney.
Hole accumulation in Ge/Si core/shell nanowires studied by electron holography.
Microscopy and Microanalysis, 16(S2):566–567, 2010.
- [86] Diana Enescu.
Thermoelectric energy harvesting: Basic principles and applications.
In *Green Energy Advances*. IntechOpen, 2019.
- [87] Giovanni Pennelli.
Review of nanostructured devices for thermoelectric applications.
Beilstein Journal of Nanotechnology, 5(1):1268–1284, 2014.
- [88] Tianzhuo Zhan, Ryo Yamato, Shuichiro Hashimoto, Motohiro Tomita, Shunsuke Oba, Yuya Himeda, Kohei Mesaki, Hiroki Takezawa, Ryo Yokogawa, Yibin Xu, et al.
Miniaturized planar si-nanowire micro-thermoelectric generator using exuded thermal field for power generation.
Science and Technology of advanced MaTerialS, 19(1):443–453, 2018.
- [89] Yoshinao Mishima, Yoshisato Kimura, and Sung Wng Kim.
Enhancement of thermoelectric figure of merit through nanostructural control on intermetallic semiconductors toward high-temperature applications.
Nanomaterials: Research Towards Applications, 161:383, 2006.
- [90] Zhi-Gang Chen, Guang Han, Lei Yang, Lina Cheng, and Jin Zou.
Nanostructured thermoelectric materials: Current research and future challenge.
Progress in Natural Science: Materials International, 22(6):535–549, 2012.
- [91] Maciej Haras and Thomas Skotnicki.
Thermoelectricity for IoT—a review.
Nano Energy, 54:461–476, 2018.
- [92] GD Mahan.
Good thermoelectrics.
Solid state physics (New York. 1955), 51:81–157, 1997.
- [93] Xiao-Dong Wang, Yu-Xian Huang, Chin-Hsiang Cheng, David Ta-Wei Lin, and Chung-Hao Kang.

- A three-dimensional numerical modeling of thermoelectric device with consideration of coupling of temperature field and electric potential field.
Energy, 47(1):488–497, 2012.
- [94] Terry M Tritt.
Thermal conductivity: theory, properties, and applications.
Springer Science & Business Media, 2005.
- [95] A Khitun, A Balandin, and KL Wang.
Modification of the lattice thermal conductivity in silicon quantum wires due to spatial confinement of acoustic phonons.
Superlattices and microstructures, 26(3):181–193, 1999.
- [96] AA Maznev and OB Wright.
Demystifying umklapp vs normal scattering in lattice thermal conductivity.
American journal of physics, 82(11):1062–1066, 2014.
- [97] Yongjin Lee and Gyeong S Hwang.
Mechanism of thermal conductivity suppression in doped silicon studied with nonequilibrium molecular dynamics.
Physical Review B, 86(7):075202, 2012.
- [98] Terrell L Hill.
An introduction to statistical thermodynamics.
Courier Corporation, 1986.
- [99] Prasanta Misra.
Physics of condensed matter.
Academic Press, 2011.
- [100] Jie Zou and Alexander Balandin.
Phonon heat conduction in a semiconductor nanowire.
Journal of Applied Physics, 89(5):2932–2938, 2001.
- [101] Shozo Takeno.
Mass-difference scattering and lattice thermal conductivity.
Progress of Theoretical Physics, 30(1):144–145, 1963.
- [102] Xiao Yan, Weishu Liu, Hui Wang, Shuo Chen, Junichiro Shiomi, Keivan Esfarjani, Hengzhi Wang, Dezhi Wang, Gang Chen, and Zhifeng Ren.

- Stronger phonon scattering by larger differences in atomic mass and size in p-type half-heuslers $\text{Hf}_{1-x}\text{Ti}_x\text{CoSb}_{0.8}\text{Sn}_{0.2}$.
Energy & Environmental Science, 5(6):7543–7548, 2012.
- [103] Michael F Ashby, Hugh Shercliff, and David Cebon.
Materials: engineering, science, processing and design.
Butterworth-Heinemann, 2018.
- [104] GH Tang, Y Zhao, GX Zhai, and C Bi.
Phonon boundary scattering effect on thermal conductivity of thin films, 2011.
- [105] Deyu Li, Yiyang Wu, Philip Kim, Li Shi, Peidong Yang, and Arun Majumdar.
Thermal conductivity of individual silicon nanowires.
Applied Physics Letters, 83(14):2934–2936, 2003.
- [106] Yunfei Chen, Deyu Li, Jennifer R Lukes, and Arun Majumdar.
Monte carlo simulation of silicon nanowire thermal conductivity.
2005.
- [107] Zhao Wang and Natalio Mingo.
Diameter dependence of SiGe nanowire thermal conductivity.
Applied Physics Letters, 97(10):101903, 2010.
- [108] Ramya Gurunathan, Riley Hanus, and G Jeffrey Snyder.
Alloy scattering of phonons.
Materials Horizons, 2020.
- [109] Fuwei Zhuge, Takeshi Yanagida, Naoki Fukata, Ken Uchida, Masaki Kanai, Kazuki Nagashima, Gang Meng, Yong He, Sakon Rahong, Xiaomin Li, et al.
Modulation of thermoelectric power factor via radial dopant inhomogeneity in B-doped Si nanowires.
Journal of the American Chemical Society, 136(40):14100–14106, 2014.
- [110] Pavan Kumar Chundi, Yini Zhou, Martha Kim, Eren Kursun, and Mingoo Seok.
Hotspot monitoring and temperature estimation with miniature on-chip temperature sensors.
In *2017 IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED)*, pages 1–6. IEEE, 2017.

- [111] Tan-Tan Zhang and Yuan Gao.
A BJT-based temperature sensor in 40-nm CMOS with $\pm 0.8^\circ\text{C}$ (3σ) untrimmed inaccuracy.
In *2019 32nd IEEE International System-on-Chip Conference (SOCC)*, pages 1–4. IEEE, 2019.
- [112] Ferran Reverter and Josep Altet.
MOSFET temperature sensors for on-chip thermal testing.
Sensors and Actuators A: Physical, 203:234–240, 2013.
- [113] Ori Bass and Joseph Shor.
Ultra-miniature 0.003 mm^2 PNP-based thermal sensor for CPU thermal monitoring.
In *ESSCIRC 2018-IEEE 44th European Solid State Circuits Conference (ESSCIRC)*, pages 334–337. IEEE, 2018.
- [114] Uğur Sönmez, Fabio Sebastiano, and Kofi AA Makinwa.
Compact thermal-diffusivity-based temperature sensors in 40-nm CMOS for SoC thermal monitoring.
IEEE Journal of Solid-State Circuits, 52(3):834–843, 2017.
- [115] Tejasvi Anand, Kofi AA Makinwa, and Pavan Kumar Hanumolu.
A VCO based highly digital temperature sensor with 0.034 c/mV supply sensitivity.
IEEE Journal of Solid-State Circuits, 51(11):2651–2663, 2016.
- [116] Sining Pan, Yanquan Luo, Saleh Heidary Shalmany, and Kofi AA Makinwa.
A resistor-based temperature sensor with a 0.13 pJ.K^2 resolution FoM.
IEEE Journal of Solid-State Circuits, 53(1):164–173, 2017.
- [117] Zhong Tang, Yun Fang, Zhenyan Huang, Xiao-Peng Yu, Zheng Shi, and Nick Ni-anxiong Tan.
An untrimmed BJT-based temperature sensor with dynamic current-gain compensation in 55-nm CMOS process.
IEEE Transactions on Circuits and Systems II: Express Briefs, 66(10):1613–1617, 2019.
- [118] Jan Angevare, Lorenzo Pedalà, Uğur Sönmez, Fabio Sebastiano, and Kofi AA Makinwa.

- A 2800- μm^2 thermal-diffusivity temperature sensor with VCO-based readout in 160-nm CMOS.
In *2015 IEEE Asian Solid-State Circuits Conference (A-SSCC)*, pages 1–4. IEEE, 2015.
- [119] Chan-Hsiang Weng, Chun-Kuan Wu, and Tsung-Hsien Lin.
A CMOS thermistor-embedded continuous-time delta-sigma temperature sensor with a resolution FoM of $0.65 \text{ pJ } ^\circ\text{C}^2$.
IEEE Journal of Solid-State Circuits, 50(11):2491–2500, 2015.
- [120] Sining Pan and Kofi AA Makinwa.
A 0.25 mm² 2-resistor-based temperature sensor with an inaccuracy of $0.12 ^\circ\text{C}$ (3σ) from $-55 ^\circ\text{C}$ to $125 ^\circ\text{C}$.
IEEE Journal of Solid-State Circuits, 53(12):3347–3355, 2018.
- [121] Sining Pan, Çağrı Gürleyük, Matheus F Pimenta, and Kofi AA Makinwa.
10.3 a 0.12 mm² wien-bridge temperature sensor with $0.1 ^\circ\text{C}$ (3σ) inaccuracy from $-40 ^\circ\text{C}$ to $180 ^\circ\text{C}$.
In *2019 IEEE International Solid-State Circuits Conference-(ISSCC)*, pages 184–186. IEEE, 2019.
- [122] Kannan A Sankaragomathi, Jabeom Koo, Richard Ruby, and Brian P Otis.
25.9 a $\pm 3\text{ppm}$ 1.1 mW FBAR frequency reference with 750MHz output and 750mV supply.
In *2015 IEEE International Solid-State Circuits Conference-(ISSCC) Digest of Technical Papers*, pages 1–3. IEEE, 2015.
- [123] Mina Shahmohammadi, Kianoush Souri, and Kofi AA Makinwa.
A resistor-based temperature sensor for MEMS frequency references.
In *2013 Proceedings of the ESSCIRC (ESSCIRC)*, pages 225–228. IEEE, 2013.
- [124] Michael H Perrott, James C Salvia, Fred S Lee, Aaron Partridge, Shouvik Mukherjee, Carl Arft, Jintae Kim, Niveditha Arumugam, Pavan Gupta, Sassan Tabatabaei, et al.
A temperature-to-digital converter for a MEMS-based programmable oscillator with $< \pm 0.5 - \text{ppm}$ frequency stability and $< 1 - \text{ps}$ integrated jitter.
IEEE Journal of Solid-State Circuits, 48(1):276–291, 2012.
- [125] Pyoungwon Park, David Ruffieux, and Kofi AA Makinwa.

- A thermistor-based temperature sensor for a real-time clock with ± 2 ppm frequency stability.
IEEE Journal of Solid-State Circuits, 50(7):1571–1580, 2015.
- [126] Wendi Yang, Hanjun Jiang, and Zhihua Wang.
 A 0.0014 mm² 150 nW CMOS temperature sensor with nonlinearity characterization and calibration for the -60 to +40 °C measurement range.
Sensors, 19(8):1777, 2019.
- [127] Kamran Souri, Youngcheol Chae, Frank Thus, and Kofi Makinwa.
 A 0.85 V 600nW all-CMOS temperature sensor with an inaccuracy of ± 0.4 °C (3s) from -40 to 125 °C.
 In *2014 61st IEEE International Solid-State Circuits Conference, ISSCC 2014*, pages 222–223. Institute of Electrical and Electronics Engineers Inc., 2014.
- [128] Takao Oshita, Joseph Shor, David E Duarte, Avner Kornfeld, and Dror Zilberman.
 Compact BJT-based thermal sensor for processor applications in a 14 nm tri-gate CMOS process.
IEEE Journal of Solid-State Circuits, 50(3):799–807, 2015.
- [129] Saleh Heidary Shalmany, Kamran Souri, Uaur Sonmez, Kianoush Souri, Michele D’Urbino, Said Hussaini, Darryl Tauro, and Sassan Tabatabaei.
 3.7 A 620 μ W BJT-based temperature-to-digital converter with 0.65 mK resolution and FoM of 190fJ.K².
 In *2020 IEEE International Solid-State Circuits Conference-(ISSCC)*, pages 70–72. IEEE, 2020.
- [130] Michiel AP Pertijs, Kofi AA Makinwa, and Johan H Huijsing.
 A CMOS smart temperature sensor with a 3σ inaccuracy of ± 0.1 °C from -55 °C to 125 °C.
IEEE Journal of Solid-State Circuits, 40 (12), 2005.
- [131] Guijie Wang, Ali Heidari, Kofi AA Makinwa, and Gerard CM Meijer.
 An accurate BJT-based CMOS temperature sensor with duty-cycle-modulated output.
IEEE Transactions on Industrial Electronics, 64(2):1572–1580, 2016.
- [132] Bahman Yousefzadeh, Saleh Heidary Shalmany, and Kofi AA Makinwa.

- A BJT-based temperature-to-digital converter with ± 60 mK (3σ) inaccuracy from -55°C to $+125^\circ\text{C}$ in $0.16\text{-}\mu\text{m}$ CMOS.
IEEE Journal of Solid-State Circuits, 52(4):1044–1052, 2017.
- [133] Caspar PL van Vroonhoven, Dan d’Aquino, and Kofi AA Makinwa.
A thermal-diffusivity-based temperature sensor with an untrimmed inaccuracy of $\pm 0.2^\circ\text{C}$ (3s) from -55°C to 125°C .
In *2010 IEEE International Solid-State Circuits Conference (ISSCC)*, pages 314–315. IEEE, 2010.
- [134] Wenfeng Zhao, Rui Pan, Yajun Ha, and Zhi Yang.
A 0.4 V 280-nW frequency reference-less nearly all-digital hybrid domain temperature sensor.
In *2014 IEEE Asian Solid-State Circuits Conference (A-SSCC)*, pages 301–304. IEEE, 2014.
- [135] Uğur Sönmez, Rui Quan, Fabio Sebastiano, and Kofi AA Makinwa.
A 0.008-mm² area-optimized thermal-diffusivity-based temperature sensor in 160-nm CMOS for SoC thermal monitoring.
In *ESSCIRC 2014-40th European Solid State Circuits Conference (ESSCIRC)*, pages 395–398. IEEE, 2014.
- [136] Claudio Lombardi, Stefano Manzini, Antonio Saporito, and Massimo Vanzi.
A physically based mobility model for numerical simulation of nonplanar devices.
IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 7(11):1164–1171, 1988.
- [137] Caspar PL van Vroonhoven and Kofi AA Makinwa.
Thermal diffusivity sensing: A new temperature sensing paradigm.
In *2011 IEEE Custom Integrated Circuits Conference (CICC)*, pages 1–6. IEEE, 2011.
- [138] Rajesh Mishra and Jiri Militky.
Nanotechnology in Textiles: Theory and Application.
Woodhead Publishing, 2018.
- [139] Karl Hess.
Advanced theory of semiconductor devices.
IEEE, 2000.

- [140] R Stratton.
Diffusion of hot and cold electrons in semiconductor barriers.
Physical Review, 126(6):2002, 1962.
- [141] Y Apanovich, E Lyumkis, B Polsky, A Shur, and P Blakey.
Steady-state and transient analysis of submicron devices using energy balance and simplified hydrodynamic models.
IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 13(6):702–711, 1994.
- [142] Chih Tang Sah.
Fundamentals of solid state electronics.
World Scientific Publishing Company, 1991.
- [143] Sheng S Li and W Robert Thurber.
The dopant density and temperature dependence of electron mobility and resistivity in n-type silicon.
Solid-State Electronics, 20(7):609–616, 1977.
- [144] S Reggiani, M Valdinoci, L Colalongo, and G Baccarani.
A unified analytical model for bulk and surface mobility in Si n-and p-channel MOSFETs.
In *29th European Solid-State Device Research Conference*, volume 1, pages 240–243. IEEE, 1999.
- [145] Megan A Yamoah, Wenmin Yang, Eric Pop, and David Goldhaber-Gordon.
High-velocity saturation in graphene encapsulated by hexagonal boron nitride.
ACS nano, 11(10):9914–9919, 2017.
- [146] Shin-ichi Takagi and Akira Toriumi.
New experimental findings on hot carrier transport under velocity saturation regime in Si MOSFETs.
IEDM Tech. Dig., 711, 1992.
- [147] Ikunori Takata.
A simple new model for the saturation velocity and the voltage dependency of leakage current.
In *Proceedings of 9th International Symposium on Power Semiconductor Devices and IC's*, pages 133–136. IEEE, 1997.

- [148] C Canali, G Majni, R Minder, and G Ottaviani.
Electron and hole drift velocity measurements in silicon and their empirical relation to electric field and temperature.
IEEE Transactions on electron devices, 22(11):1045–1047, 1975.
- [149] Bhalachandra V Paranjape.
Field dependence of mobility in semiconductors.
Proceedings of the Physical Society. Section B, 70(6):628, 1957.
- [150] TCAD Sentaurus.
Sdevice user guide, ver.
G-2012.06, Synopsys, 2012.
- [151] Ahmet Z Sahin and Bekir S Yilbas.
The thermoelement as thermoelectric power generator: effect of leg geometry on the efficiency and power generation.
Energy Conversion and Management, 65:26–32, 2013.
- [152] Anil W Dey, Johannes Svensson, B Mattias Borg, Martin Ek, and Lars-Erik Wernersson.
Single InAs/GaSb nanowire low-power CMOS inverter.
Nano letters, 12(11):5593–5597, 2012.
- [153] Sandeep Saini.
Low power interconnect design.
Springer, 2015.
- [154] Sherif M Sharroush.
Design of the CMOS inverter-based amplifier: A quantitative approach.
International Journal of Circuit Theory and Applications, 47(7):1006–1036, 2019.
- [155] Woorham Bae.
CMOS inverter as analog circuit: An overview.
Journal of Low Power Electronics and Applications, 9(3):26, 2019.
- [156] Che-Yu Lin, Kristan Bryan Simbulan, Chuan-Jie Hong, Kai-Shin Li, Yuan-Liang Zhong, Yan-Kuin Su, and Yann-Wen Lan.
Polarity-controllable MoS_2 transistor for adjustable complementary logic inverter applications.
Nanoscale Horizons, 5(1):163–170, 2020.

- [157] Hervé Barthélemy, Stéphane Meillere, Jean Gaubert, and Edith Kussener.
Transconductance CMOS inverter based AC coupling amplifier.
In *2014 IEEE 12th International New Circuits and Systems Conference (NEWCAS)*,
pages 9–12. IEEE, 2014.
- [158] Dinesh Kumar, Sumit K Pandey, Navneet Gupta, and Hitesh Shrimali.
Design of hybrid flash-SAR ADC using an inverter based comparator in 28 nm
CMOS.
Microelectronics Journal, 95:104666, 2020.
- [159] Satheesh Rao et al.
Design of 3-bit flash ADC using inverter threshold comparator in 45 nm CMOS
technology.
In *2017 International Conference on Intelligent Computing, Instrumentation and
Control Technologies (ICICICT)*, pages 1621–1624. IEEE, 2017.
- [160] Shakti Prasad Senapati.
Design of a simple digital ADC using only digital blocks and delay element circuit.
In *2016 IEEE International Conference on Recent Trends in Electronics, Informa-
tion & Communication Technology (RTEICT)*, pages 311–315. IEEE, 2016.
- [161] Ryan Selby, Tucker Kern, William Wilson, and Tom Chen.
A 0.18 μm CMOS switched-capacitor amplifier using current-starving inverter
based op-amp for low-power biosensor applications.
In *2013 IEEE 4th Latin American Symposium on Circuits and Systems (LASCAS)*,
pages 1–4. IEEE, 2013.
- [162] Ricardo Póvoa, António Canelas, Ricardo Martins, Nuno Horta, Nuno Lourenço,
and João Goes.
A new family of CMOS inverter-based OTAs for biomedical and healthcare appli-
cations.
Integration, 71:38–48, 2020.
- [163] Ricardo Póvoa, António Canelas, Ricardo Martins, Nuno Horta, Nuno Lourenço,
and João Goes.
A low noise CMOS inverter-based OTA for and healthcare signal receivers.
In *2019 16th International Conference on Synthesis, Modeling, Analysis and Simu-
lation Methods and Applications to Circuit Design (SMACD)*, pages 1–4. IEEE,
2019.

- [164] Suchismita De, Suchismita Tewari, Abhijit Biswas, and Abhijit Mallik.
Improved digital performance of hybrid CMOS inverter with Si p-MOSFET and InGaAs n-MOSFET in the nanometer regime.
Microelectronic Engineering, 211:18–25, 2019.
- [165] M De Marchi.
Polarity control at runtime: From circuit concept to device fabrication.
PhD thesis, Ph. D. dissertation, École Polytechnique Fédérale de Lausanne, Lausanne, 2015.
- [166] Md Rokib Hasan, Muniyat Siddiqui Rafa, Marwan Hossain, Farah Rafia, and Maisha Rashid Nidhi.
Gate length engineering impact of sub-10 nm GaN-based DG-MOSFETs.
In *2017 IEEE International WIE Conference on Electrical and Computer Engineering (WIECON-ECE)*, pages 117–120. IEEE, 2017.
- [167] Nam Sung Kim, Todd Austin, David Baauw, Trevor Mudge, Krisztián Flautner, Jie S Hu, Mary Jane Irwin, Mahmut Kandemir, and Vijaykrishnan Narayanan.
Leakage current: Moore’s law meets static power.
computer, 36(12):68–75, 2003.
- [168] S Demuynck, JF De Marneffe, QT Le, I Vos, K Devriendt, M Van Hove, J Waeterloos, K Howard, P Popa, L Wilson, et al.
Integrating ensemble, $\tilde{N}_c$ pmd low-k at the pmd level of cmos logic circuits.
Microelectronic engineering, 83(11-12):2303–2308, 2006.
- [169] Amalendu Bhushan Bhattacharyya.
Compact MOSFET models for VLSI design.
John Wiley & Sons, 2009.
- [170] Herbert B Michaelson.
The work function of the elements and its periodicity.
Journal of applied physics, 48(11):4729–4733, 1977.
- [171] S Barraud, R Coquand, M Casse, M Koyama, J-M Hartmann, V Maffini-Alvaro, C Comboroure, C Vizioz, F Aussenac, O Faynot, et al.
Performance of omega-shaped-gate silicon nanowire MOSFET with diameter down to 8 nm.
IEEE Electron Device Letters, 33(11):1526–1528, 2012.

- [172] V Schmidt, S Senz, and U Gösele.
Influence of the Si/SiO₂ interface on the charge carrier density of Si nanowires.
Applied Physics A, 86(2):187–191, 2007.
- [173] Hans Mertens, Romain Ritzenthaler, Hiroaki Arimura, Jacopo Franco, Farid Sebaai, Andriy Hikavyi, BJ Pawlak, Vladimir Machkaoutsan, Katia Devriendt, Diana Tsvetanova, et al.
Si-cap-free SiGe p-channel FinFETs and gate-all-around transistors in a replacement metal gate process: Interface trap density reduction and performance improvement by high-pressure deuterium anneal.
In *2015 Symposium on VLSI Technology (VLSI Technology)*, pages T142–T143. IEEE, 2015.
- [174] Faraz Najam, Yun Seop Yu, Keun Hwi Cho, Kyoung Hwan Yeo, Dong-Won Kim, Jong Seung Hwang, Sansig Kim, and Sung Woo Hwang.
Interface trap density of gate-all-around silicon nanowire field-effect transistors with TiN gate: Extraction and compact model.
IEEE transactions on electron devices, 60(8):2457–2463, 2013.
- [175] José L Pérez-Aparicio, Roberto Palma, and RL Taylor.
Finite element analysis and material sensitivity of Peltier thermoelectric cells coolers.
International Journal of Heat and Mass Transfer, 55(4):1363–1374, 2012.

