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Department of Bioengineering

Log-domain Implementation of a Processor for Cochlear Implant Stimulators

Yacine Belgaid

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Declaration

I hereby declare that all the work presented here is my own work and all else is referenced when appropriate.

-Yacine Belgaid

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Abstract

Globally, the number of people that live with disabling hearing loss as reported by the World Health Organisation is 430 million, with an additional 1 billion young adults at increased risk of hearing loss. In certain cases cochlear implants are prescribed, consisting of a visible, external processor which transmits signals across the skull to electrodes in the cochlea.

The aim of this thesis is to demonstrate that the contemporary digital signal processing (DSP) used in the processor can be replaced by log-domain, analogue circuits operating in the continuous-time, continuous-value domain. This work presents two such novel solutions. Firstly, a novel architecture that utilises an integrator core to estimate the Hilbert transform to extract the envelope and instantaneous frequency of signals. The design was simulated and then fabricated in 0.35 µm AMS technology and consumed 6.7 µW of power. Secondly, a novel memory-less n-of-m channel selector circuit implementation is proposed with O(n) complexity based on a hierarchical Winner Takes All (WTA) architecture. The implementation allows for a variable number of channels to be selected with each clock cycle by setting a single bias current. Channel selection number can be either of an integer value or based on the power spectral content contribution of the channels. The transistor-level design of a 16-channel selector was simulated and shown to support selection frequencies to at least 10 kHz. Combined with the filter-bank from previous research, the two blocks enable the implementation of all the speech coding strategies used in commercial cochlear implants, including fine-spectral processing (FSP). The thesis therefore demonstrated that it is feasible to implement cochlear implant processing in a single ultra-low power chip appropriate for a fully-implantable cochlear implant. Such a chip would be expected to provide high speech comprehension for cochlear implant users.

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List of Abbreviations

ACE	Advanced Combinational Encoder
ADC	Analogue to Digital Convertor
AGC	Automatic Gain Control
AM	Amplitude Modulation
CA	Compressed Analogue
CC	Current Conveyor
CIS	Continuous Interleaved Sampling
DRC	Design Rule Check
DSP	Digital Signal Processing
EE	Enhanced Envelope
FM	Frequency Modulation
FSP	Fine Structure Processing
GMS	Geometric Mean Splitter
HPF	High Pass Filter
IF	Intermodulation Frequency
LNA	Low Noise Amplifier
LPF	Low Pass Filter
LVS	Layout Vs Schematic
MAV	Mean Average Value
MEMS	Miniature Electro-Mechanical Systems
OTA	Operational Transimpedance Amplifier
OZGF	One-Zero Gammatone Filter
RMS	Root Mean Squared
SPEAK	Spectral PEAK
STFT	Short Time Fourier Transform
WTA	Winner Takes All

Chapter 1

Preface

1.1 Motivation

Significant advancements in cochlear implant technology have been achieved since the advent of single-channel electrodes. Notably, the most prominent improvements have been observed in the increasing complexity of stimulation strategies, which are now largely implemented via increasingly sophisticated software algorithms running on an external processor positioned behind the ear.

These external processors have been miniaturised since the inception of the first cochlear implants. However, these devices are easily visible on users, affecting their day-to-day life and self-esteem. In order to realise the long-term vision of a fully implantable cochlear implant, greater research effort is required to focus on realising a full system on chip cochlear implant. Therefore, the main motivation for this work is to implement a fully analogue hardware-based solution to extract envelope and instantaneous frequency information from audio signals. In addition, the second motivation is to realise a channel selector block with enough flexibility to implement many of the currently used strategies.

1.2 Objectives

This work has two major objectives:

- The first is an analogue-based hardware implementation of an audio feature extraction, which estimates the instantaneous frequency and analytic envelope.
- The second major objective is the realisation of an N-of-M selector block with the following features:
    - The ability to choose the highest amplitude channels from a set of M channels.
    - The ability to choose channels based on power contribution.

1.3 Thesis Organisation

The thesis presented here is organised as follows:

- The first background section provides an overview the biological process of hearing as well as some background knowledge on the operation of cochlear implants and its history. It also describes the surgical process of implanting a device and the role of stimulation strategies in the cochlear implant environment. It also highlights the role of audio features in stimulation strategies and the merits of the different stimulation strategies.
- The second chapter details the theoretical background for the Hilbert transform as well as the definition of the analytic signal; accompanied with some intuition to the role of the analytic signal and its relation to instantaneous frequency and analytic envelope. Furthermore, the proposed system is described and verified. This system is simulated in MATLAB to verify the operation of the proposed system.
- The third chapter details the first major research output, which is the implementation of the proposed system in silicon. Transistor level blocks are proposed and optimised to ensure the correct operation of the entire system.

- The fifth chapter presents the fabricated chip a series of tests which validate the operation of the subblocks, subsystems and the entire proposed system. The results are also shown and explained.
- The sixth chapter presents the proposed N-of-M channel selector block. The principle of operation and modes of operation are described, this chapter also presents simulated results for the block. This is the second major research contribution.
- Lastly the conclusion contains some overall closing remarks commenting on this work and some future work proposals.

Chapter 2

Background

2.1 Anatomy and Physiology of Human Hearing

In this chapter, the anatomy of the ear as well as the physiology of hearing will be explored. Additionally, a brief history of cochlear implants and its various stimulation strategies will be explained in order to lay out the foundation and form the main motivation for this thesis.

2.1.1 Gross Anatomy and Physiology of the Ear

The ear is an organ which is a biological interface for perceiving the environment through sound. Sound travels through the environment in the form of a pressure wave. Once the travelling pressure wave reaches the ear, travelling along where its internal organs transduce these pressure variations into electrical signals to be sent through the auditory pathway. It will then be processed by the auditory cortex and perceived as sound [1]. The anatomy of the ear

shown in Figure 1 is categorised into several sections: the outer ear (external ear), the middle ear, and the inner ear.

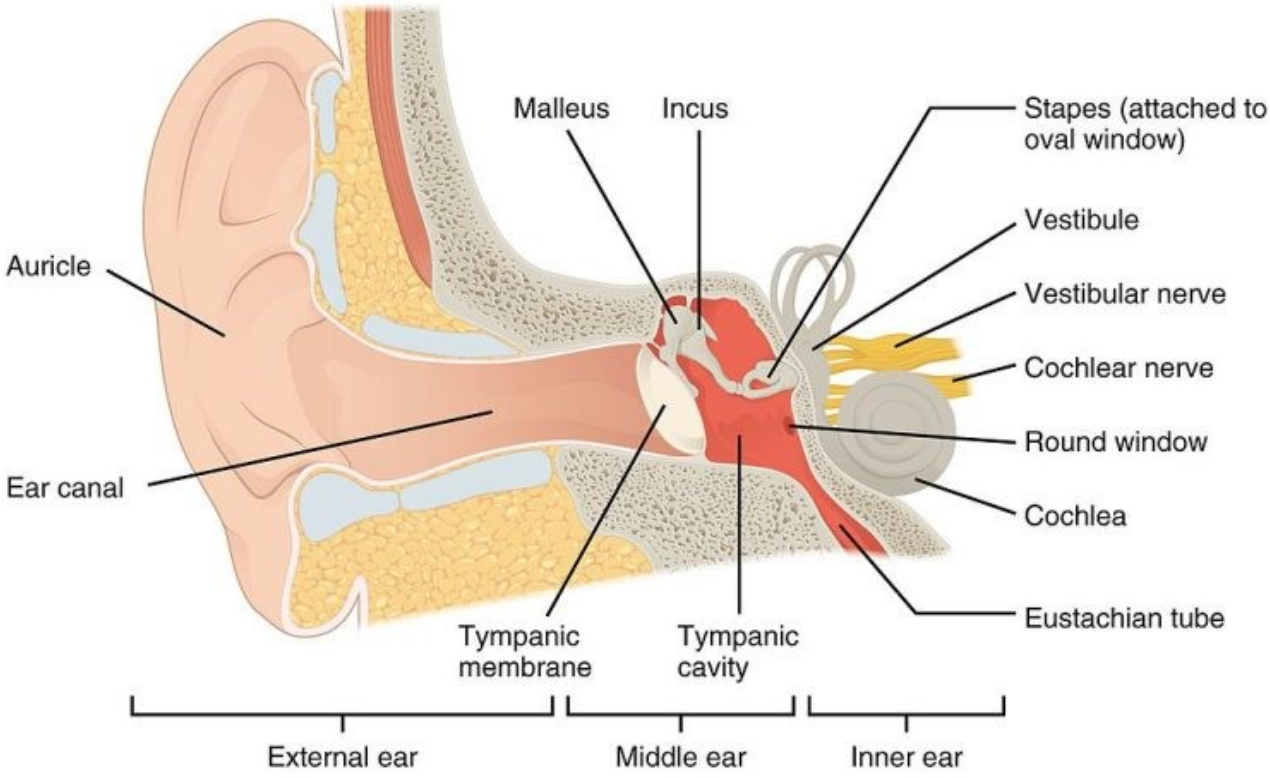


Figure 1: The major anatomical structures of the ear. The ear consists of the outer ear, middle-ear and inner ear. The cochlea is the anatomical structure in which mechanotransduction takes place, from [2].

The outer ear contains the auricle, which is the protruding fleshy receptacle on the outside of the head. Its primary function is to receive and focus incoming sound waves. Sound waves are then transmitted along the external auditory canal and into the middle ear section. The middle ear is formed of the tympanic membrane, sometimes referred to as the eardrum, which is attached to a set of three bones, called the ossicles, all connected in series: the malleus, stapes and incus. In humans, these three bones are the smallest bones present in the human body.

As sound waves reach and interact with the tympanic membrane, the pressure variations in the air vibrate the tympanic membrane. As the tympanic membrane vibrates so too does the

malleus, due to it being attached to the membrane. This vibration also transfers to the stapes and then the incus finally ending at the opening of the cochlea [3].

The ossicles in the middle ear serve two purposes, the first of which is impedance matching [4]. This is important due to the size difference between the tympanic membrane and the oval window and because vibrations from the air need to be converted properly into vibrations inside the fluid-filled chambers of the cochlea. The second function is what is known as biological amplification, that is to say small incoming vibrations are amplified which uses the lever action to achieve a mechanical advantage [5]. The middle ear also contains the eustachian tube, which is responsible for equalising the pressures between the middle ear cavity and the environment.

2.1.2 Anatomy and Transduction of Sound in the Cochlea

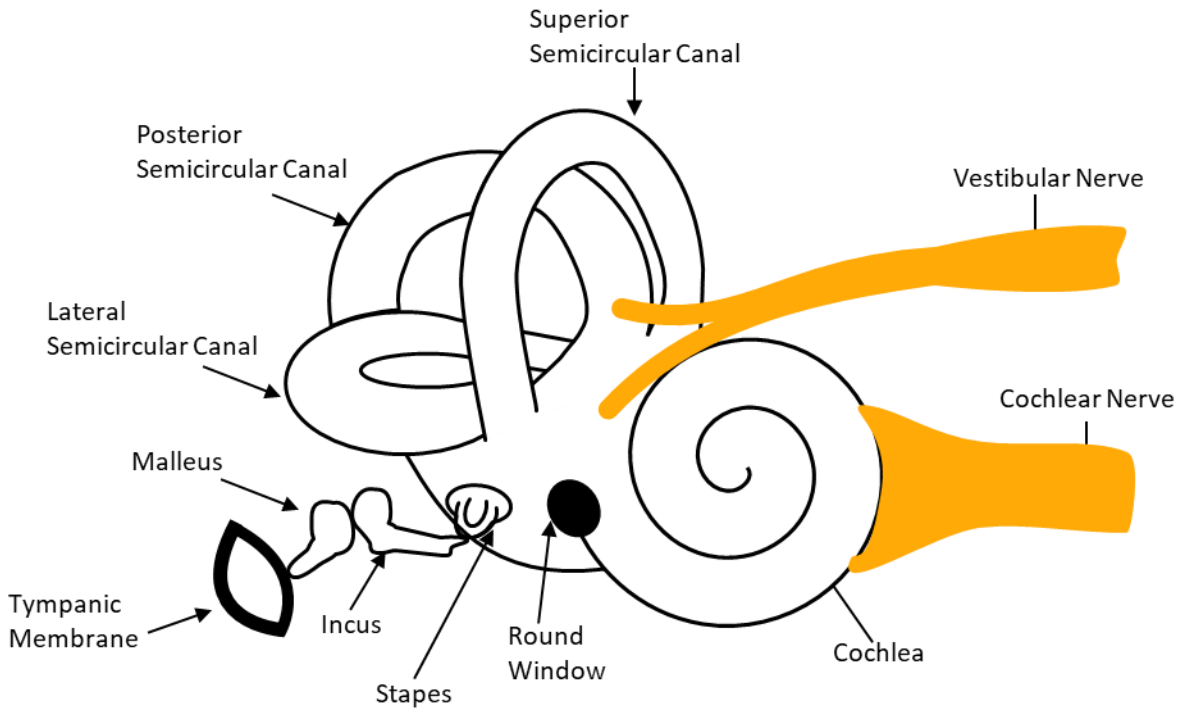


Figure 2: Components of the inner ear, including the semi-circular canals and cochlea adapted from [6].

Inside the inner ear, the cochlea is contained within. The cochlea as shown in Figure 2 is a very small yet complex organ serving many different functions. The cochlea is a helical structure which is attached to three protruding semi-circular canals. These canals are responsible for balance however, they are not involved in the mechanotransduction of sound [7], [8].

The cochlear spiral is also fluid-filled with perilymph and endolymph which are conductive. The two fluids are separated by Reissner's membrane and the organ of Corti as shown in Figure 3. The membrane structure running across the length of the cochlea is called the basilar membrane. The surface of the basilar membrane is lined with a series of specialised cells called hair cells whose primary function is mechanotransduction [9], which is the process in which sound is converted from a pressure wave into an electrical signal.

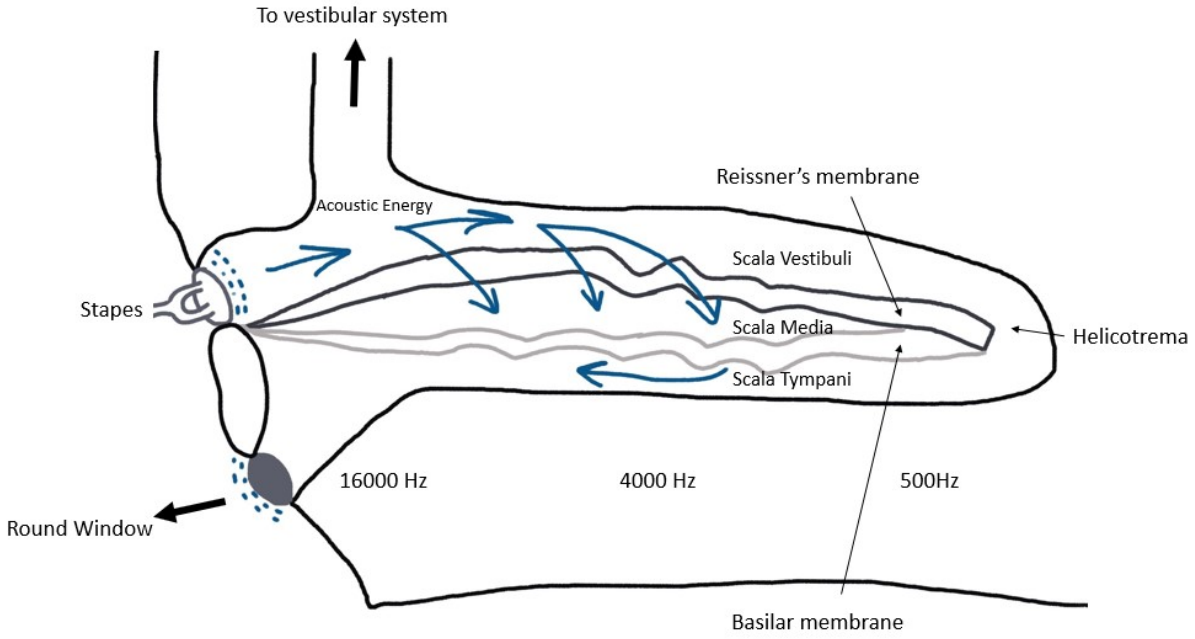


Figure 3: The pathway a sound wave takes when travelling along the cochlea and reflecting back, out of the round window.

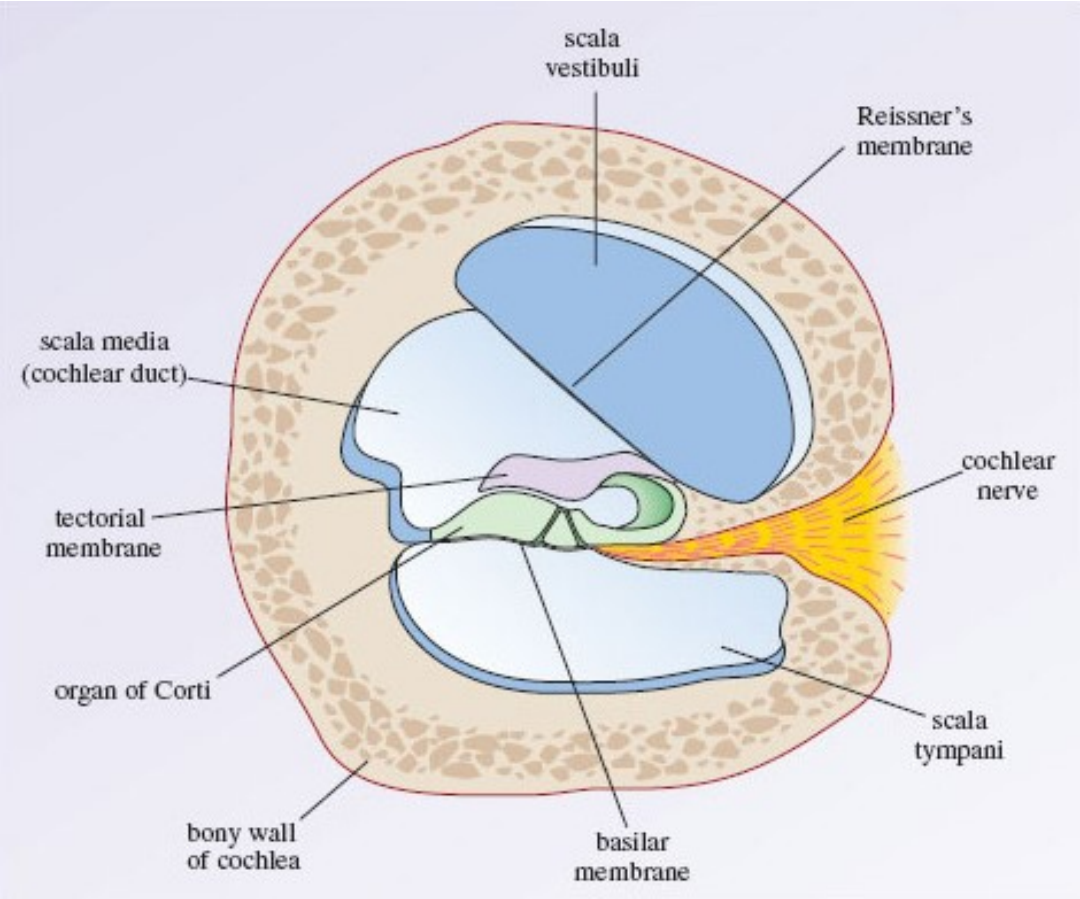


Figure 4: The cross section of the cochlea showing the different sections inside. The organ of Corti and the Reissner's membrane separate the scala media from the scala vestibuli and scala tympani respectively. The organ of Corti contains inner hair cells which are in contact with the tectorial membrane, the deflection of which is the main process behind mechanotransduction [2].

Inside the cochlea, the organ of Corti, shown in Figure 5, is present which is adjacent to the basilar membrane and houses the specialised hair cells. The cochlea, as illustrated in Figure 4, also contains various other structures: the Reissner's membrane. This is a membrane which separates the scala vestibuli from the scala media as illustrated in Figure 3. The basilar membrane is a specialised structure which separates the scala media from the scala tympani, the scala tympani and the scala vestibuli meet at the apex of the cochlea called the helicotrema. The basilar membrane has as a varying width and stiffness, which increases along its length towards the helicotrema. The basilar membrane at the basal end has a higher stiffness and lower

width, which resonates at higher frequencies. Further along the length of the membrane towards the apical end, that width as well as the stiffness decreases, which results in a frequency selectivity towards the apex resonating at lower frequencies.

When sound pressure waves cause the stapes to vibrate, it results in a travelling pressure wave originating from the oval window through the fluid filled scala vestibuli, as it travels along the length of the cochlea towards the helicotrema, the pressure waves bounce back along the scala tympani and towards the round window [10].

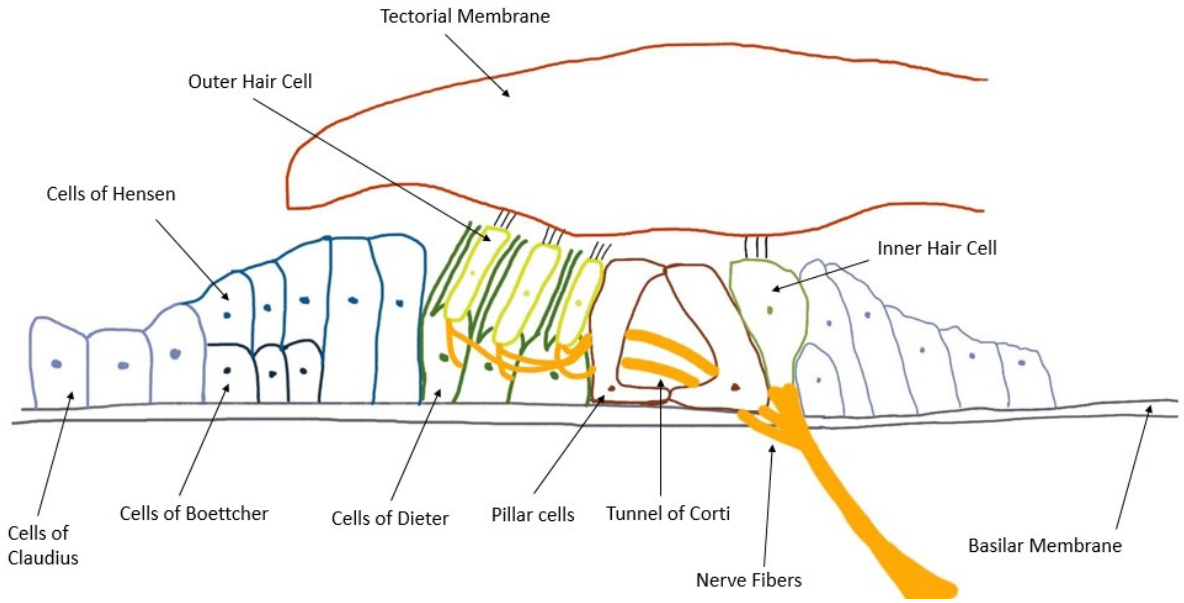


Figure 5: The structure of the Organ of Corti in the human ear adapted from [6].

Due to the varying thickness and stiffness of the basilar membrane, the travelling wave will resonate sections of the basilar membrane based on the frequency of the vibration. These vibrations are then detected by the hair cells giving the cochlea a tonotopic frequency map. Hair cells are specialised cells with hair-like protrusions called stereocilia forming a bundle [9]. There are two types of hair cells, the inner hair cells and the outer hair cells, both are attached to the cochlear nerve fibres. The stereocilia are arranged in such a way as to maximise the deflection in the direction of wave travel [11]. When a sound wave causes a section of the basilar membrane to resonate, the basilar membrane which is in contact with the surface of the hair cells causes the protrusions to deflect. This deflection opens mechanically sensitive ion gates allowing for ion flow. Consequently, this flow causes a depolarization in the cell,

resulting in a neuron signal to fire. The tonotopic mapping of the basilar membrane, is maintained along the entirety of the auditory pathway up to the auditory cortex, the brain then processes the incoming signals, firing at a particular frequency which is translated into a sound perception.

In the cochlea, there are two types of specialized cells which line the basilar membrane called the hair cells. Hair cells are of two types of inner hair cells (IHCs), which connect to the majority of the auditory nerve fibres, and outer hair cells (OHCs) which outnumber the IHCs with a ratio of 3:1 in a healthy cochlea. Additionally, there are functional differences between these two types of cells, IHCs are mainly responsible for the mechanotransduction step which converts mechanical vibrations detected by the stereocilia into electrical signals, these signals are then sent along afferent nerve fibres along the auditory pathway. In contrast, OHCs connect to efferent nerve fibres, these signals modulate the stiffness of the stereocilia which results in a variable amplification within the cochlea, enhancing the overall hearing sensitivity.

The nerve fibres from the hair cells form the cochlear nerve, which is the primary electrical pathway along the auditory pathway. The cochlear nerve is a bundle of around 30,000 nerve fibres in each ear, the tonotopic mapping of the cochlea is preserved along these nerve bundles all the way along the auditory pathway where each sub-bundle codes for a specific frequency range.

Sound coding can be categorized into two distinct phenomena, place coding and time coding. Place coding is a mechanism in which the different sections of the cochlea encode different frequencies determined by the spatial arrangement of the hair cells along the length of the basilar membrane. Due to the difference in stiffness along the length of the basilar membrane, higher frequency tones are detected closer to the base of the cochlea where the membrane is narrower and stiffer. Whereas lower frequency tones are detected closer to the apical end of the cochlea where the membrane is wider and flexible. Place coding results in a tonotopically arranged spatial mapping along the auditory pathway.

There is another mechanism in which sound frequency is encoded which is called time coding or phase locking. Specific nerve fibres closer to the apical end (lower frequencies) are able to fire an action potential in sync with the phase of incoming sound. These fibres therefore can encode a sound's frequency by the firing rate of the nerve fibres.

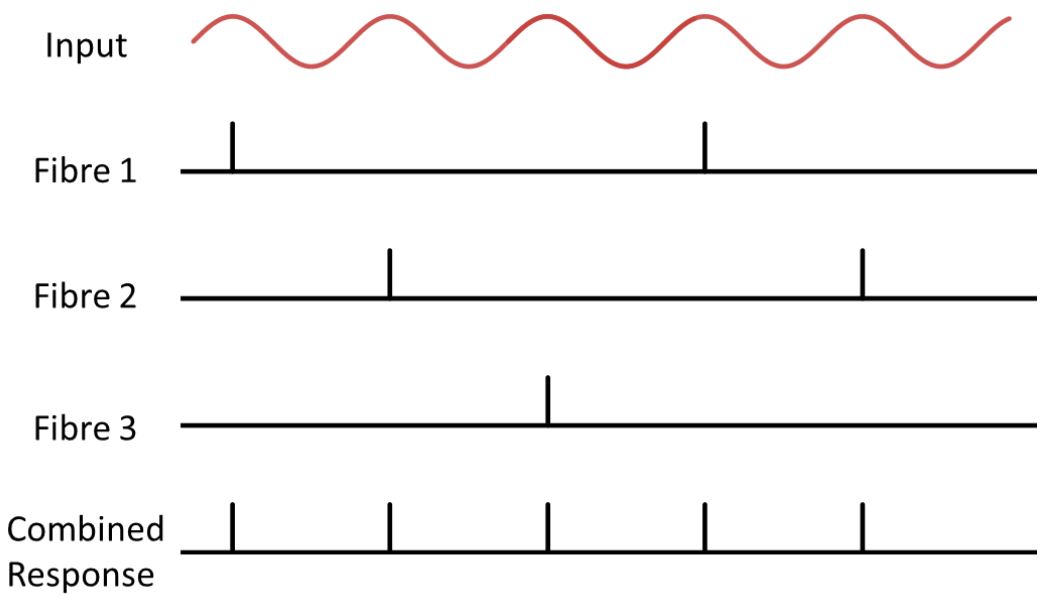


Figure 6: The volley principle, a bundle of nerve fibres has combined firing rate that exceeds the maximum rate of a single nerve fibre.

However, there is a limit to the nerve fibre's firing rate as the sound's frequency increases, an additional phenomenon called the volley effect becomes dominant. The volley principle, illustrated in Figure 6, is when the individual nerve fibres fire sequentially producing an effective higher firing rate in the overall nerve bundle. The volley principle is effective up to 4-5 kHz, beyond which place coding becomes the dominant frequency coding mechanism [12].

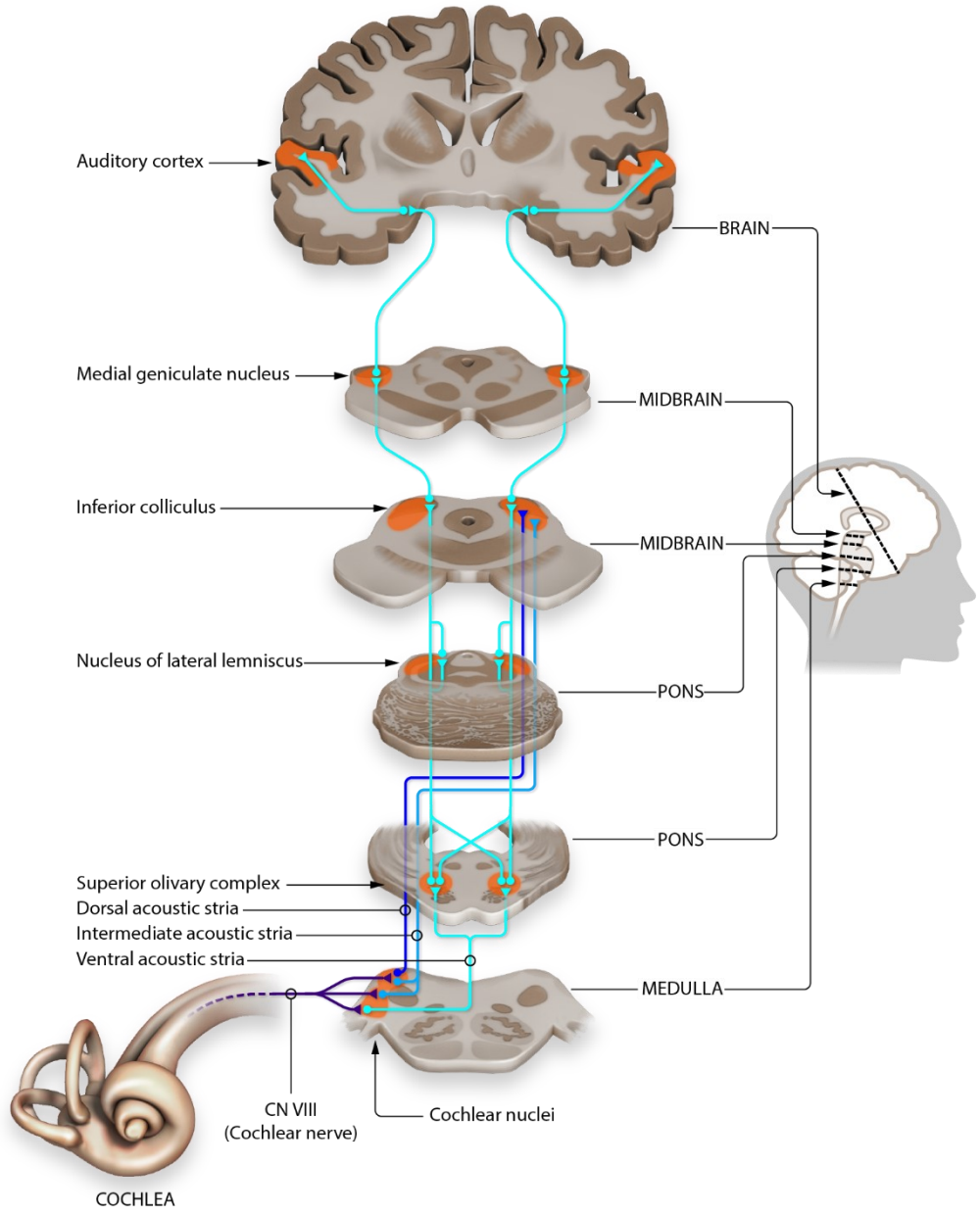


Figure 7: The human auditory pathway, which starts at the cochlear nerve, each stage involves higher level signal processing which is eventually interpreted by the auditory cortex as meaningful sound [13].

The electrical pulses travel along the cochlear nerve to the cochlear nucleus illustrated in Figure 7, which is the first processing centre interpreting basic spectral and temporal features of sound. These electrical signals travel along the auditory pathway shown in Figure 7 passing through more complex structures which perform more complex and higher-level processing such as sound localization, speech perception and interpretation.

2.2 Sensorineural Hearing Loss

Hearing loss is a structural degradation that reduces auditory function. It can be divided into two main types: sensorineural, linked to inner ear or neural pathway damage; and conductive, caused by obstructions in the middle ear. There are several causes for sensorineural hearing loss, the most common cause among younger people is due to exposure to loud sounds for extended periods of time [14]. These include but are not limited to working around loud machines in construction environments or listening to loud music for extended periods of time. Acquired hearing loss can also be caused by diseases such as meningitis, which if left untreated can permanently damage the delicate auditory structures. Additionally, hearing loss can also have genetic causes leading to poor cochlear development during the foetal stages inside the mother's womb [15].

The hair cells, stereocilia and the nerve fibres which constitute the intricate cochlear mechanisms are vulnerable to a multitude of factors. Damage which occurs to these structures can lead to profound hearing loss. Some examples of the possible causes of trauma include diseases such as bacterial meningitis, autoimmune inner ear disease, or genetic disorders which affects the cochlea's development and hence its function. Certain pharmaceutical side effects are ototoxic [16] and can also have an effect on the auditory system which can range from temporary hearing loss to permanent. Additionally, one of the more common causes of hearing loss is due to noise exposure. Prolonged exposure to intense loud noises, whether in occupational (heavy machinery) or recreational (rave concerts) settings, can result in noise-induced hearing loss. This type of exposure can often lead to permanent damage to the hair cells and the cochlea's delicate structures, resulting in moderate to profound hearing loss depending on the severity of the damage.

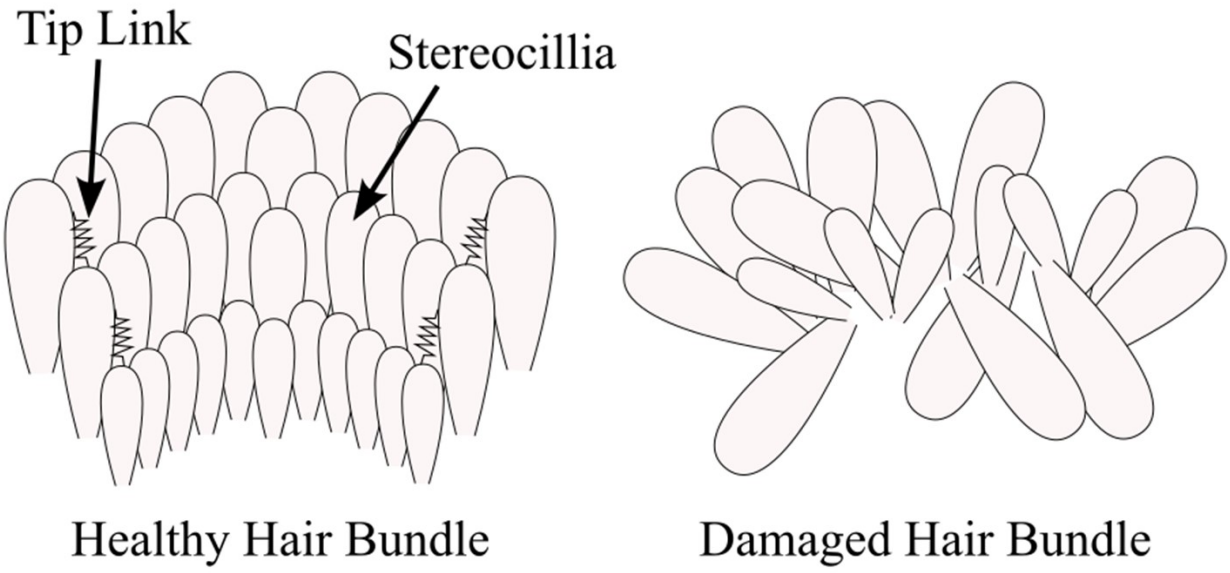


Figure 8: (Left) Healthy IHC stereocilia bundle with connected tip links. (Right) Damage to the hair bundle leads to a loss of hearing due to mechanical failure.

Hair cells are essential for the transduction of vibrations into electrical signals, when a significant number of hair cells are damaged or lost the ability to detect and process sound is severely compromised leading to profound hearing impairment. This can be in the form of damaged stereocilia, shown in Figure 8, which can lose its structure and damaged tip links. In addition, the nerve fibres connecting to the hair cells can also be damaged which can greatly impact hearing as shown in Figure 9. The spiral ganglion cells, which are the primary neurons that transmit auditory information from hair cells to the brain can also be damaged, the number of surviving spiral ganglion cells decreases with increased severity of hearing loss, with factors such as age which tends to be the major contributor.

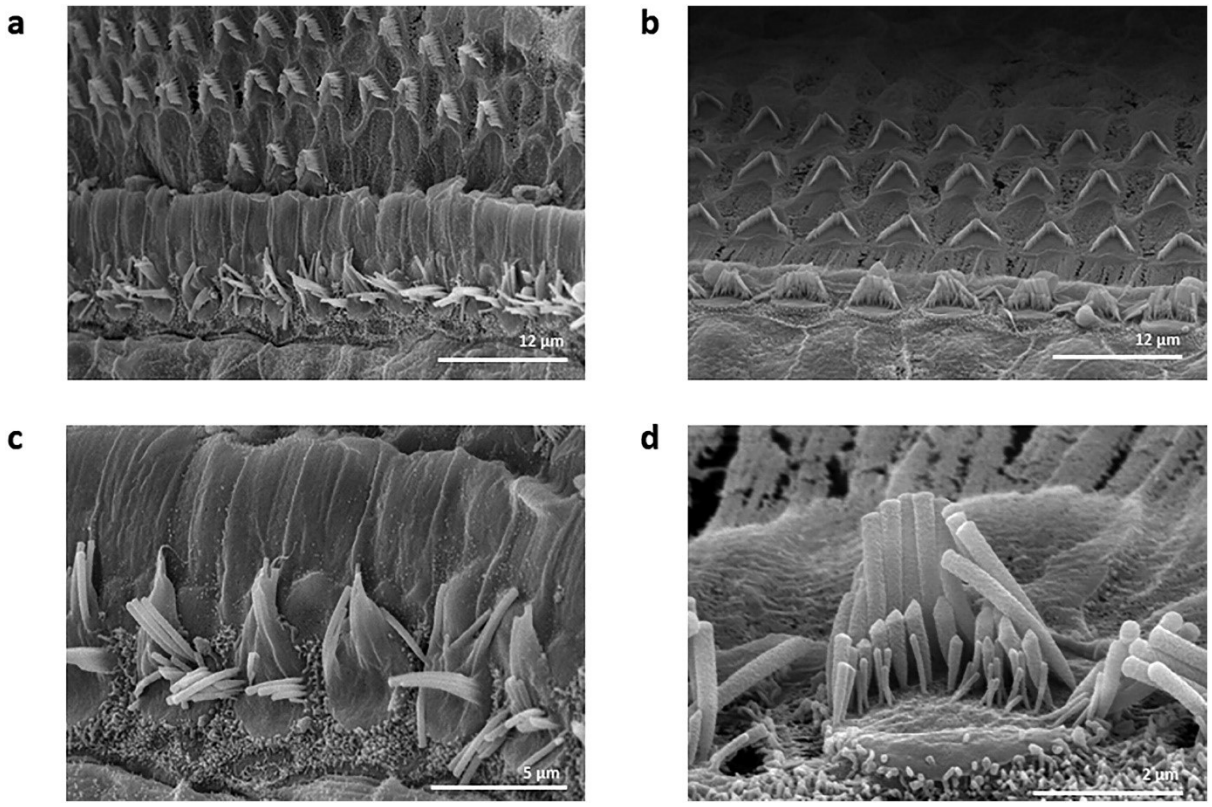


Figure 9: (Top) Healthy hair cells connected to healthy nerve fibres, eventually forming the cochlear nerve bundle. (Bottom) Degradation of both the nerve fibres and the hair cells, image extracted from [17] with the permission of the publisher.

Sensorineural hearing loss is classified into several categories based on the condition's severity. Summarised in Table 1 is the classification for hearing loss recorded in dB HL. For mild to moderate degrees of hearing loss a hearing aid is generally recommended. However, for severe to profound hearing loss a cochlear implant is generally the only treatment path available.

Table 1: Degrees of hearing loss severity in terms of a decibel measure relative to normal hearing according to the British Society of Audiology [18].

Hearing Loss Severity	
Degree of hearing loss	**Hearing loss range (dB HL)**
Mild	21 to 40
Moderate	41 to 70
Severe	71 to 95
Profound	95+

Sensorineural hearing loss is assessed and diagnosed by an audiologist; whereby a set of tests are presented to the patient to assess their frequency sensitivity. A collection of pure tones (single frequency tones) is played to the person to measure the minimum amplitude at a specific frequency in decibels required to trigger a response from the listener. This is repeated up to 4 kHz, which is then plotted to produce a patient specific audiogram. This generates a visual representation of the patient's auditory health. Physical damage to the delicate structures inside the ear, especially those in the cochlea, are typically permanent and cannot be reversed by modern medicines. However, acute cases of temporary hearing loss can be caused by certain drugs [19]. This is due to the fragile mechanical nature of mechanotransduction. Currently, the only way to alleviate the effects of sensorineural hearing loss is by either wearing hearing assistive devices such as hearing aids, cochlear implants, or brain stem implants, depending on the severity of the hearing loss. Hearing aids are specialised amplifiers, which are tuned to the patient's specific audiogram, and they work by selectively amplifying difficult to detect sounds at specific frequencies which are picked up by an external microphone. This is because in this case the damage done to the internal cochlear structures is not as severe with the person retaining some residual hearing. In contrast, for more severe hearing loss cases in which a hearing aid amplification is not sufficient to result in intelligible speech, then the only way to circumvent this issue is to bypass the mechanotransduction step and to stimulate the cochlear nerve directly.

2.3 Cochlear Implants

The cochlear implant is a device which is designed to bypass the mechanotransduction step that happens naturally in the ear. The typical cochlear implant system is split into two separate devices across the skin, an external and internal component, the external systems includes an external microphone, a processor and a wireless transmitter. The sound processor takes in the audio input from the microphone and processes it according to a sound coding strategy, which in modern cochlear implants is implemented using digital signal processing (DSP) techniques. The output is then sent to the wireless transmitter which communicates with the internal part the cochlear implant as shown in Figure 10.

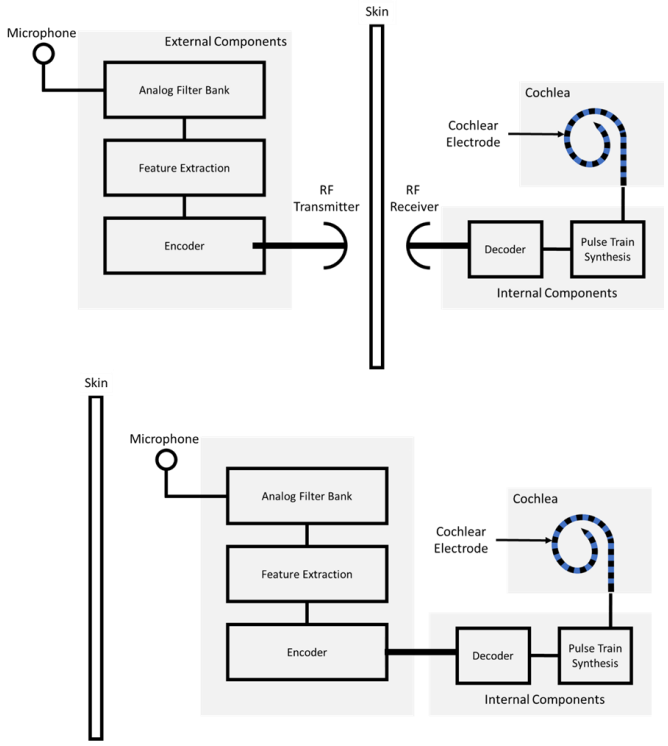


Figure 10: Summary of the major components of the cochlear implant system. (Top) The typical components of a modern cochlear implant system consisting of an external audio processor, encoder, RF transmitter and an internal decoder with a stimulation circuit. The external sound processor is powered with a battery and the internal components are powered via an RF link (Bottom) The potential future architecture of a cochlear implant which consists of entirely internal components powered by an implantable battery which is rechargeable wirelessly.

The internal part of the cochlear implant includes a wireless receiver and a stimulation encoder, which translates the incoming signals into a series of train pulses for pulsatile stimulation or continuous signals for analogue stimulation. This is then sent to a multichannel electrode array which is embedded inside the cochlea. Depending on the strength of the signal, the frequency content and the patient specific parameters the electrical stimulus is then sent to the corresponding position inside the cochlea to stimulate the specific bundle of cochlear nerve fibres, to be then interpreted by the auditory cortex as sound [20].

In cases where there is an almost total loss of cochlear nerve fibres, the brainstem implant is used instead. It works by stimulating the nerves in the brainstem, which is further along the auditory pathway. An important CI limitation worth considering is that the parameters change not only with each individual patient but can also change over time as well because of the body's response to electrodes. As a result of this, the electrodes will have a higher impedance overtime.

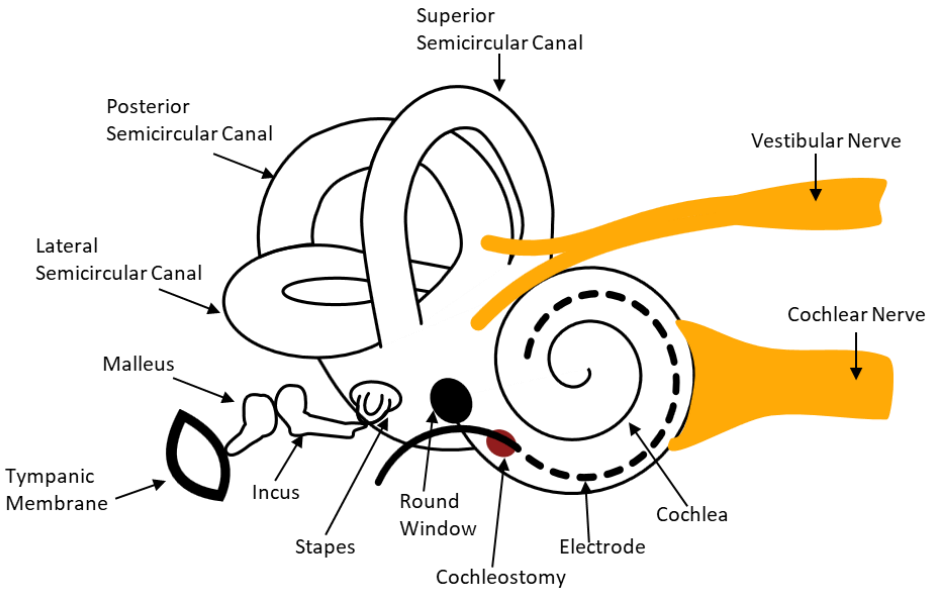


Figure 11: Schematic highlighting the site of where a cochleostomy is performed close to the round window.

When the doctor recommends a cochlear implant, the patient's cochlea is imaged to determine the best approach to surgery. The patient is placed under anaesthesia and a cochleostomy is

performed, this typically involves removing a piece of the cochlea close to the round window, as shown in Figure 7, to provide an entrance point for the electrode or by inserting the electrode through the round window [21], [22]. The receiver and stimulator is placed behind the ear under the scalp and above the skull [23]. The electrode array, which is a thin, soft, and flexible material is inserted into the newly formed hole in the cochlea and as the electrode is pushed inside the electrode bends to match the shape of the cochlea whilst the surgeon also checks that the electrode is placed in roughly the correct position [24]. However, due to patient variability the electrode is only pushed in as far as resistance is felt [25]–[30], which means that the post-surgery procedure is critical in tuning the performance to match the patient's unique profile.

The electrode array typically consists of multiple electrodes, arranged along its length. This multichannel array enables spatial representation of sound frequencies along the cochlea, mimicking the place coding mechanism. Each electrode corresponds to a specific frequency region within the cochlea. This arrangement allows for more precise stimulation of auditory nerve fibres, improving the perception of complex sounds.

There are three major stimulation modalities in the electrode namely monopolar, bipolar and tripolar stimulation. In monopolar stimulation, one electrode serves as the active electrode, while the return electrode is a distant reference which is usually located outside of the cochlea. Monopolar stimulation tends to have the broadest current spread compared to bipolar and tripolar stimulation, typically requiring lower current levels for excitation [31].

Bipolar stimulation uses two adjacent electrodes. One as the active electrode and the other as the return electrode. It offers better spatial selectivity than monopolar stimulation, with a narrower current spread and higher stimulus threshold.

Tripolar stimulation instead involves three adjacent electrodes, with the middle electrode acting as the active electrode and the outer two as return electrodes. It provides further enhanced spatial selectivity and a higher stimulus threshold which increases the power requirements compared to monopolar stimulation.

Charge balancing is essential in cochlear implants to prevent tissue damage at the electrode-tissue interface. Ensuring that the amount of electrical charge delivered to the cochlea contains equal amounts of positive and negative charge helps to maintain the long-term safety and functionality of the implant. This is typically achieved by delivering a balanced biphasic pulse with equal positive or negative charge.

The way in which a stimulus (amplitude and timing) is delivered to the cochlea is important and is the final step of a signal processing pipeline called a sound coding strategy or a stimulation strategy. A sound coding strategy refers to the method used to translate incoming acoustic information into electrical signals that stimulate the auditory nerve. Continuous Interleaved Sampling (CIS), Compressed Analogue (CA), Advanced Combination Encoder (ACE), are examples of the more commonly used strategies [32]. These strategies determine how the speech processor maps acoustic signal features like frequency, intensity, and timing onto the electrical pulses delivered by the electrode array.

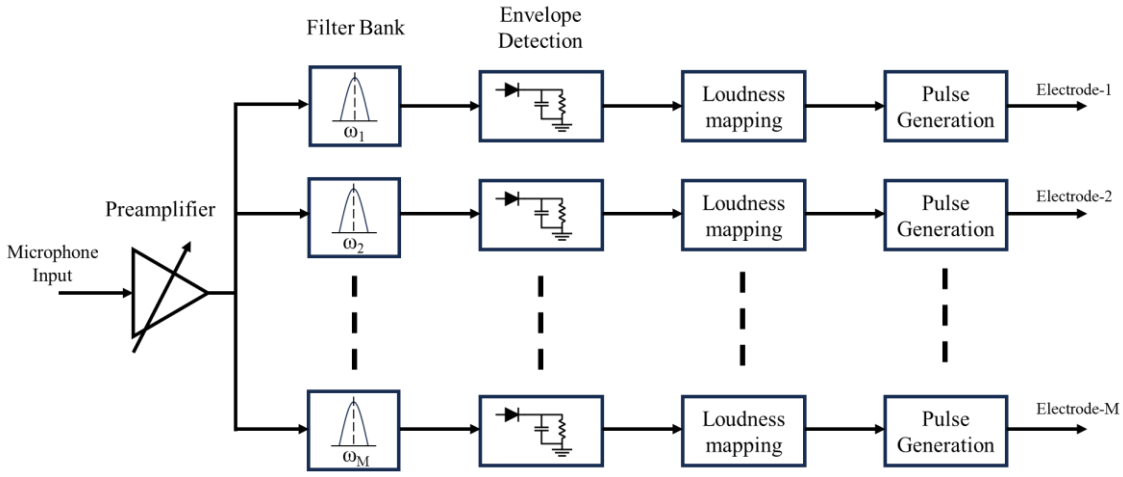


Figure 12: A typical architecture of a CI system which includes the filterbank, envelope detector, signal compression and pulse generation.

A typical sound processing pipeline for a multi-electrode CI is shown in Figure 12 and it involves several stages. Firstly, the preamplifier which is generally an automatic gain control (AGC) adjusts the amplification of incoming sounds based on their intensity, conditioning the signals before further processing. The signals are then passed through a series of bandpass filters, called a filterbank, which splits the wideband signal into different frequency bands, each with a different centre frequency, aligning with the corresponding electrode channels. Next the filterbank outputs are passed through an envelope detector block, typically consisting of a rectified low-pass filter block, which extracts the incoming signal's envelope. The envelopes of the frequency bands are compressed following a patient specific loudness mapping based on

the dynamic range of each channel. These signals are then converted into a series of pulses based on the specific coding strategy protocol.

Cochlear implants have shown remarkable success in improving speech perception for individuals with severe to profound hearing loss [33]. Many CI users achieve speech comprehension and communication abilities comparable to individuals with normal hearing. However, the degree of success can vary among individuals, influenced by factors such as duration of deafness, and age at implantation [34].

2.4 Multichannel Sound Coding Strategies

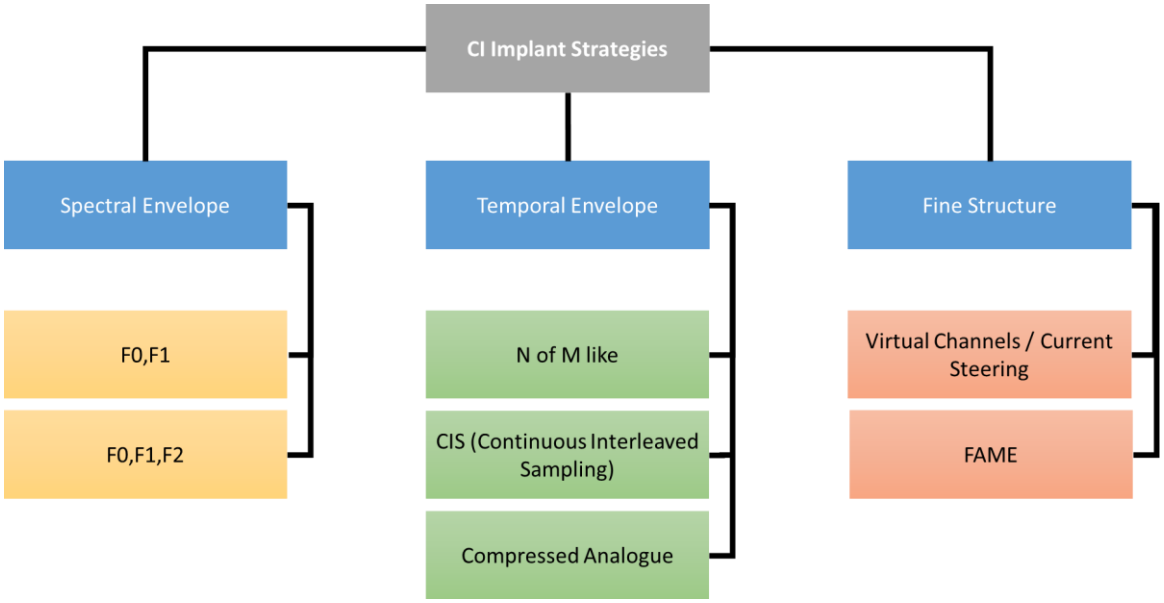


Figure 13: An overview of the stimulation strategy paradigms. Spectral envelope-based strategies rely on extracting the formants of speech (F0, F1 and F2) for stimulation. Temporal envelope-based strategies extract the temporal envelopes for stimulation delivery in either a continuous or pulsatile approach. Fine structure-based strategies incorporate the temporal or spectral fine structures such as instantaneous frequency or fast envelope.

The type of stimulation strategy is important in the context of cochlear implants because it forms the basis of the type of information conveyed to the person to then help enrich the person's hearing experience. There are several paradigms in which a stimulation strategy can be developed as shown in Figure 13, the first is by using spectral features [35] and the second

is by incorporating temporal features [36]. In both cases, both the envelope and the channel frequencies are considered [37]. There are two main modalities of stimulation strategies, analogue and pulsatile approaches [32]. Understanding the differences between these strategies is essential for optimizing cochlear implant design when considering physical implementation.

2.4.1 Spectral Envelope

The spectral envelope is the envelope that is obtained across the filterbank channels after band-limiting audio [38]. The spectral envelope contains important information about the frequency content of sound and is used to generate the electrical stimuli that will then be delivered to the auditory nerve.

A prominent strategy that relies heavily on the spectral envelope is the SPEAK or ACE strategy [32]. These two strategies use the spectral envelope in combination with a fundamental frequency estimator to achieve high levels of speech intelligibility. By using the fundamental frequency as a control for the rate of stimulation, the encoding frequency information present in formants can be incorporated during stimulation [39].

The SPEAK strategy uses a simplified version of the spectral envelope. In this strategy, the envelope is calculated for a limited number of frequency bands and the resulting electrical stimuli are delivered to the auditory nerve at a fixed rate.

The ACE strategy, on the other hand, builds upon the SPEAK strategy. In this strategy the spectral envelopes are calculated for a larger number of frequency channels, and the resulting electrical stimuli are then delivered to the auditory nerve at a variable rate based on the estimated formants of the speech signal (F0, F1 and F2). This strategy has been shown to provide improved speech perception in noisy environments compared to the SPEAK strategy [40].

2.4.2 Temporal Envelope and Fine Structures

Temporal envelopes, as the name suggests are envelopes which enhance, isolate, or incorporate features present in time on the envelope [41]. The most prominent strategy, which uses this approach, is the EE or excited envelope strategy [42]. The temporal envelope is sometimes also known as the analytic envelope or the fast envelope. This is a name given for the envelope where the features or landmarks in time are given extra importance, due to being important in speech intelligibility in noise. An example of an envelope for an AM and FM wave is shown in Figure 14.

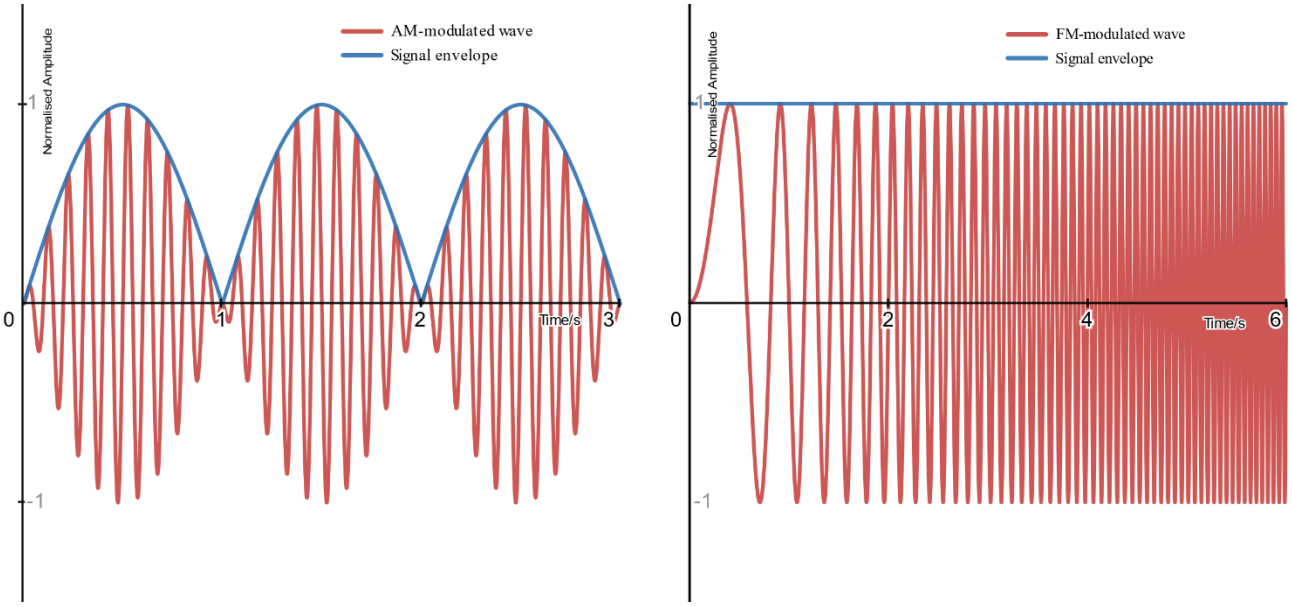


Figure 14: (Left)Envelope of an amplitude modulated signal (Right) Envelope of a frequency modulated signal.

Fine structures include both the instantaneous frequency information as well as features in the temporal envelope. Fine structures have been shown to be of vital importance when it comes to speech intelligibility especially in the case of tonal based languages [43]–[45]. As a result, more strategies are adopting algorithms where these structures are incorporated into the strategy [46]–[50]. The most common of these strategies are ones which use a dynamic stimulation rate, where the stimulation rate is directly controlled by the instantaneous frequency

of each channel. Doing this has been shown to marginally increase the ability to distinguish between different musical instruments [51], [52].

There are several ways in which fine structure and instantaneous frequency information has been incorporated into strategies, The most prominent method is by using zero crossings [53] which is a technique to estimate the local instantaneous frequency by counting the number of times a signal goes through a sign change when crossing zero DC. Other methods use a technique called temporal masking to enhance the temporal features in sound using various methods such as modulation [54] with either the temporal envelope or with the instantaneous frequency, which can be extracted using the Hilbert transform [55]–[57]. In addition, there are strategies which instead focus on increasing the spatial selectivity and compensating for the deviation in electrode placement [58], [59] by utilising a technique called virtual channels [39], [60], [61] which is a technique where nearby channels are stimulated simultaneously with a weighted contribution in order to stimulate the basilar membrane in between the channels.

This is important because normal hearing depends on both temporal and place coding mechanisms for the perception of sound [62]–[65]. Temporal coding is the dominant contributor for low frequency signals in the basilar membrane, the rate at which low frequency channels are stimulated encode information which is then processed in the auditory cortex [66]. In contrast place coding is more prominent for high frequency channels, meaning that the location where the basilar membrane is stimulated in high frequencies encodes frequency information for higher frequencies as opposed to the rate of stimulation as is the case with temporal coding.

2.4.3 Analogue Cochlear Implant Strategies

In the early days of cochlear implants, the prevailing stimulation strategy implemented was called compressed analogue (CA), which is an analogue sound coding strategy. This involves stimulating the cochlea with a continuous-value, continuous-time, low current signal [67]. However, it was realised that crosstalk due to current spread inside the cochlea meant that the quality of the audio perceived by the patient was very poor and noise prone.

An analogue stimulation strategy involves the direct representation of continuous auditory signals within the cochlea. In this approach, the incoming sound wave is captured by a microphone and transformed into an electrical signal. This electrical signal, which retains the continuous nature of the sound wave, is then delivered to the cochlea through an array of electrodes. Each electrode corresponds to a specific frequency region along the cochlea's tonotopic map. By maintaining the analogue nature of the input signal, this strategy attempts to preserve the fine spectral and temporal details of sound. Interestingly, some cochlear implant users exhibit a preference for analogue strategies over pulsatile ones, particularly those individuals with a greater degree of surviving auditory nerve fibres [68]. This preference is often mirrored in improved performance when using analogue strategies. Users who demonstrate a heightened preference for or benefit from analogue strategies typically exhibit greater nerve survival.

However, the issue of current spread, where electrical currents unintentionally stimulates neighbouring nerve fibres, means that bipolar stimulation is used over monopolar stimulation, where the electrical current flows between adjacent electrodes rather than through the common ground, to reduce current spread. The use of bipolar stimulation along with the simultaneous activation of all electrodes in this strategy translates to higher power consumption. Even when monopolar stimulation was tested, CA demands substantial power due to its simultaneous stimulation of all electrodes [69].

2.4.4 Pulsatile Cochlear Implant Strategies

Pulsatile cochlear implant strategies offer an alternative approach to sound representation, relying on the discretization of auditory signals into electrical pulses. Within this paradigm, many approaches to feature extraction strategies can be implemented. This section delves into these strategies, their mechanisms, and the implications they hold for enhanced auditory perception.

Feature extraction in the context of stimulation strategies used in CIs typically refers to the formants of speech such as the fundamental frequency f0. However, since this work does not involve exploring formants, the term “feature extraction” is used in this thesis in the with its

more general engineering understanding, which are the physical properties that describes a sinusoidal wave such as envelope and frequency.

2.4.4.1 F0/F1 and F0/F1/F2

F0/F1/F2 based strategies represent a departure from continuous analogue stimulation, aiming to capture specific attributes of sound signals. Focusing instead on delivering elements such as the fundamental frequency (F0) and the first two formants of speech (F1 and F2), these strategies seek to encapsulate crucial spectral information within a pulsatile framework.

The F0/F1/F2 strategies the use of a single current source and a reduced number of electrodes. This current source generates monopolar electrical pulses. By discretising sound information into pulse patterns, these strategies effectively encode critical spectral features. Moving from F0/F1 strategy to F0/F1/F2 leads to enhanced speech perception, as the inclusion of additional formant frequency conveys a more comprehensive representation of speech sounds [70]. This improvement is particularly valuable for enabling clearer and more accurate speech perception for cochlear implant users.

The monopolar and bipolar stimulation modes demonstrate comparable performance in terms of speech recognition and sound perception [71]. This suggests that despite the method of stimulation, the encapsulated spectral information remains intact in both approaches. Additionally, monopolar stimulation is lower power hence it is the most common form of stimulation delivery for F0/F1/F2.

2.4.2.2 Continuous Interleaved Sampling (CIS)

This electrode channel crosstalk issue was mitigated with the CIS strategy [72], also known as continuous interleaved sampling which is a pulsatile strategy. CIS converts the continuous signal into a discrete time signal, by interleaving the pulse trains across the channels during stimulation, this greatly reduced the effect of crosstalk. As a result, this increased the quality of the perceived audio. Furthermore, several iterations of the CIS strategy have been

implemented, mainly focusing on increasing the rate of stimulation. However, it has been found that increasing the number of channels or the stimulation rate beyond a certain point yielded worse results [73]–[76], hence due to the marginal improvement in intelligibility and the problem of speech in noise an alternative approach to speech processing would be required to alleviate the issues present in CIS.

Continuous Interleaved Sampling (CIS) is the most significant advancement within the realm of cochlear implant strategies. Developed concurrently with analogue strategies, CIS aimed to combine the strengths of both analogue and pulsatile approaches. F1/F0/F2 strategies, introduced around the same time as analogue strategies, presented an alternative to continuous analogue stimulation. While early evaluations suggested that analogue strategies, such as those presented by Tyler in 1987 [77], yielded superior outcomes, they were often consumed higher power in comparison. CIS emerged as a solution, aiming to retain the advantages of analogue stimulation whilst reducing energy demands.

CIS benefits from the temporal coding inherent in pulsatile strategies while mitigating the high-energy costs associated with continuous analogue stimulation. A key assumption that informs CIS design is that cochlear implant users are unable to effectively exploit time coding beyond a certain frequency threshold, typically set around 400 Hz [72]. This assumption aligns with the concept of pitch saturation frequency, the point beyond which additional temporal details do not contribute significantly to pitch perception [78].

Studies such as the one conducted by Stupak, Padilla et al. in 2018 assessed the performance of CIS against analogue strategies, where the researchers found that people tend to prefer a pulsatile strategy due to it sounding “cleaner” however, the exact mechanism for these observed differences is yet to be fully explained [68].

Continuous Interleaved Sampling (CIS) signifies a significant innovation within pulsatile cochlear implant strategies. By synthesizing the benefits of both analogue and pulsatile approaches, CIS addresses the challenge of power consumption while offering valuable auditory information representation. While assumptions regarding the importance of time coding limitations persist, ongoing research and critical evaluations continue to shape the evolution of CIS-like variants and its role in optimizing cochlear implant sound coding strategies.

2.4.2.3 Variants of Continuous Interleaved Sampling

With the success of CIS, a landscape of diverse approaches has emerged across different cochlear implant manufacturers, including Advanced Bionics, Cochlear, Med-El. This section delves into the implementation differences among these CIS-like variants.

Variants of the CIS strategy are able to strike a balance between information representation and power conservation makes it an attractive choice across diverse user populations. One notable divergence across implementations lies in the pattern of electrode stimulation. While some strategies stimulate all electrodes, others opt for a subset of electrodes to be activated concurrently. This "n-of-m" approach provides a degree of flexibility, adapting to the unique needs of different individuals [79].

Additionally, some manufacturers employ current steering, such as in the case of HiRes, a technique that allows for the virtual creation of additional electrodes [80]. This innovative approach expands the number of active channels and enhances auditory perceptual outcomes.

The method of envelope extraction, a pivotal aspect of CIS strategies, can also differ among cochlear implant companies. While some strategies utilize rectification and lowpass filtering for envelope extraction, others employ the Hilbert transform, which is the mathematical definition of a given signal’s envelope, this is explained with a reference and in detail in Chapter 3.

Variants of continuous interleaved sampling (CIS) strategies demonstrate the adaptability and ingenuity of cochlear implant manufacturers in tailoring auditory prosthetics to individual users. Through variations in electrode count, stimulation patterns, current steering, and envelope extraction methods, these strategies address diverse user needs and offer unique combinations of advantages.

2.5 Cochlear Implant Design Trends

Cochlear implants consist of an internal implantable stimulator and an external audio processor, the external audio processor consists of a filter bank with each channel representing a band limited frequency output. Generally, the number of channels present in modern cochlear implants can range anywhere between 8 and 22 electrodes depending on the device manufacturer. The implant made by Cochlear has 22 intracochlear electrodes and 2 ground electrodes. Additionally, the audio processor processes the filtered channel outputs into a series of train pulses to be sent for stimulation. The research trends in both the stimulator and processor can be organised into four categories of paradigms:

1. Hardware implementation
2. Software implementation
3. Stimulation delivery
4. Electrode design

Firstly, for processors there have been efforts in implementing a biomimetic design to better match physiological responses that are found in biology. The motivation to do this stems from using nature together with engineering principles to develop efficient solutions to various engineering problems [81]–[84]. Biomimetic design in the context of cochlear implants requires the synthesis of filter banks which approximate the response found in the sections of the basilar membrane [85]–[87] the most prominent family of auditory filters are the gammatone filters [88]–[90] which have very selective frequency bands characterised by high-resonant peaks with a sharp roll of at high frequencies. A One-Zero Gammatone filter (OZGF) has been developed using log domain-based blocks together with a two-tone suppression functionality across channels to reduce the effects of current spread at the signal processing step and to improve spectral resolution [91].

Secondly, various methods have been investigated for reducing or avoiding current spread. Besides the use of bipolar and tripolar stimulation [92], which was introduced earlier, there has been research into using different pulse shapes [93] and using optogenetic techniques [94].

All these advancements improve our understanding of human hearing which will eventually lead to implementing a complete system-on-chip design such as the preliminary results

presented in [95]–[101] which include modules such as filter banks, feature extraction and stimulation blocks.

The progression of cochlear implant technology and the increased understanding of human hearing has profoundly impacted design choices. CIs have transitioned from large body-worn devices to behind-the-ear and low profile devices. As technology advances, individuals with varying degrees of hearing impairment seek solutions that cater to their unique needs. This shift in perspective underscores the importance of creating compact, effective cochlear implant devices capable of addressing a broader range of hearing deficits in a wider range of hearing scenarios.

The shift from large, body-worn cochlear implant devices to compact, behind-the-ear configurations has been a defining feature of this quest for miniaturization. Smaller devices enhance comfort, convenience, and aesthetics, ultimately improving user acceptance and discreet design. As technology becomes less obtrusive, it aligns more seamlessly with the lifestyles of individuals seeking solutions for their hearing impairments. Technological innovations such as streaming audio from devices such as phones or televisions directly to the processor or policies, which include induction loops in public places such as train stations, theatres and stadiums reduce the problem of background noise or the multiple speaker problem which is yet to be fully solved otherwise.

The energy budget of modern cochlear implants is a critical factor in their design and operation. Cochlear implants must efficiently allocate energy resources to essential components such as the digital signal processor (DSP), radiofrequency (RF) link, and nerve stimulation. Each of these components plays a pivotal role in processing sound signals, transmitting data, and delivering electrical stimuli to the auditory nerve. By transitioning to a totally implantable solution blocks such as the RF link would not be required to continuously transmit and receive data.

Designing cochlear implants which optimise miniaturization and energy efficiency presents a set of unique challenges. Efficient power management is crucial to ensure optimal performance and battery life longevity. Advances in low-power DSP architectures (driven by mass adoption of mobile devices), wireless communication protocols, and efficient electrode stimulation techniques have collectively contributed directly or indirectly to the development of modern cochlear implant systems.

As cochlear implant technology continues to evolve, researchers are exploring multiple avenues to enhance auditory experiences for users. A persistent challenge faced by CI users is understanding speech in noisy environments with pure signal processing techniques. Ongoing research seeks to refine strategies that improve speech perception in the presence of background noise, aiming to enhance communication in real-world scenarios. Strategies that emphasize spectral cues along with sound directionality coupled with temporal cues show some promise in addressing this issue.

While cochlear implant technology has made remarkable progress in speech perception, music appreciation remains an area of complexity. Researchers are delving into strategies that better convey the nuances of musical sounds, including timbre, harmony, and rhythm. Customized stimulation patterns and approaches that prioritize temporal fine structure are being explored to enrich the musical experience of CI users. In a similar approach, tonal languages where variations in pitch convey distinct meanings, cochlear implant strategies are being tailored to effectively transmit changes in instantaneous frequency. Moreover, there is a growing recognition that cochlear implant users may possess the capacity to exploit temporal coding beyond the conventional assumption of 400 Hz as a pitch saturation frequency. Recent studies challenge this threshold, suggesting that individuals can perceive temporal information at higher frequencies, which requires additional research.

The introduction of fine time structure representation within cochlear implant strategies such as Fine Structure Processing (FSP), used in MED-EL devices [102], aim to capture and transmit rapid temporal information to improve speech perception. By enhancing the representation of speech cues like harmonics and formants, these approaches address the limitations of previous strategies and open doors to tonal sound perception.

Power efficiency is a central concern in cochlear implant technology because they are battery powered. Research efforts are directed toward strategies that reduce power consumption while maintaining or even improving auditory perceptual outcomes. The MP3000 strategy is one such example [103], aiming to strike a balance between energy efficiency and auditory performance by selecting 4-6 spectral components instead of the 8-10 found in SPEAK/ACE strategies.

2.5.1 Totally-Implantable Cochlear Implants

The pursuit of enhancing cochlear implant hardware has led to the exploration of totally implantable cochlear implant systems, which pose unique engineering challenges. This section delves into the pros and cons of fully implantable cochlear implants, examines the obstacles hindering their adoption and commercialisation.

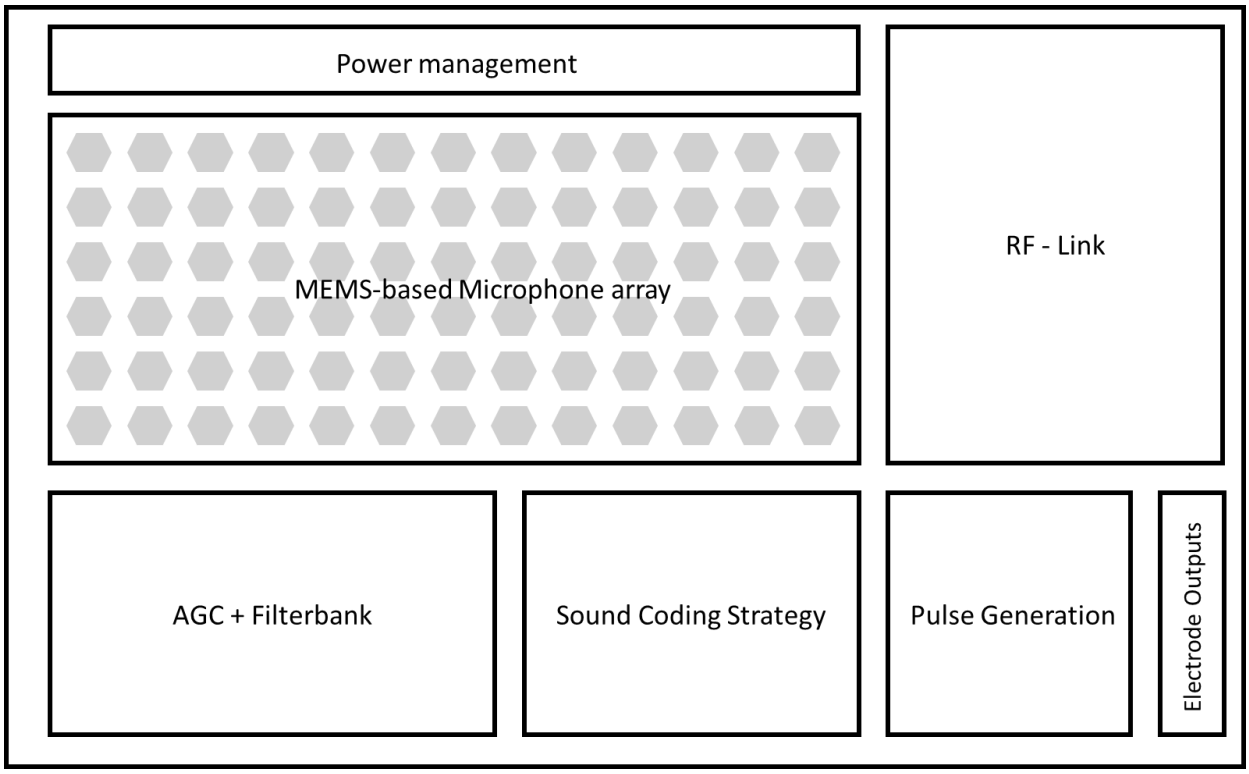


Figure 15: The potential components necessary for a complete CI on a chip system, which would include blocks such as a microphone, RF-link for data communication with digital devices in addition to signal processing blocks.

Fully implantable cochlear implants eliminate the need for external components, resulting in a discreet appearance that aligns with users' desires for a more inconspicuous solution. With all components internalized, these implants are less susceptible to external damage, moisture, and impact, promoting longevity and reliability [104]. Additionally, the lack of external components improves user comfort and convenience, as there's no need to worry about device placement, maintenance, or removal. The absence of externally visible components can reduce the stigma associated with hearing loss and the use of hearing devices.

However, implantation of fully internal devices requires additional surgery, increasing the inherent risks and complexities associated with the procedure and future upgradability. Unlike external components, fully implantable devices may lack the ease of adjustability and customization for users, which means that totally implantable devices must first outperform current devices before it can be accepted by CI users. Additionally, a fully implantable CI will require a surgically-implanted battery. Given that the battery will need periodic recharging or replacement, efficient power management is crucial.

Another challenge for fully-implantable CIs is the design of an implantable microphone that is as effective as an external microphone [104]. An experimental fully-implantable cochlear implant by Cochlear Corporation used a subcutaneous microphone [105], [106]. The microphone, however, had low sensitivity and speech perception was substantially inferior to that from a comparative external microphone. Furthermore, such microphones are affected by tissue movement such as head-turning and head scratching and even hair movement can lead to signal interference. In a recent study with a middle-ear microphone using miniature electro-mechanical systems (MEMS) technology [107], cochlear implant speech recognition was comparable to that of an external microphone at normal sounds levels (70 dB SPL), but was still notably worse at quiet levels (55 dB SPL).

Developing compact, long-lasting batteries that can support the energy requirements of cochlear implant systems remains a technical hurdle which is not fully solved yet. Implementing low-power digital signal processing (DSP) within the implant or analogue processing techniques while managing power constraints is a complex task that is yet to be fully explored in research when compared with sound coding strategies.

Chapter 3

Proposed Hilbert Transform Approximation

In the field of cochlear implants, speech processing is an extremely critical part of the cochlear implant system [108]. Several methods have been employed to extract both the envelope and instantaneous frequency information from audio, as research tends to focus towards fine structure in audio [109]. Therefore, there is a need to develop efficient algorithms and processes to extract not only the signal envelope but also the fine structures and instantaneous frequency found in audio [110].

Typically audio is processed with brick-wall filter characteristics or by using DSP techniques to extract the envelope and frequency information [111]–[113]. However, there are limitations to such approaches, the most significant of which is the high-power consumption as well as limitations in the area.

In this chapter, an alternative approach to extracting envelope and instantaneous frequency will be presented, this will be achieved by approximating the Hilbert transform to produce an analytic signal representation using log-domain analogue circuits. The advantage of using log-domain circuits is the fact that they operate in weak inversion, where the gate-source voltage (V_{gs}) is below the threshold voltage (V_{th}), and thus operate in the ultra-low power regime. Additionally, the log domain-based blocks that were implemented are compatible with the previously designed iteration of the OZGF filter bank. The theory of the operation will be

presented, established, and the results of simulation will then be summarised using both MATLAB and SIMULINK. The simulation results will then be shown and discussed, validating the realisation of the proposed architecture.

3.1 The Hilbert Transform

In this sub-section, the Hilbert transform will be formalized using its mathematical description and the utility of this transform compared to other transforms, such as the Fourier transform [114]. This will be explored in the context of audio processing by comparing both approaches. The Hilbert transform is a type of signal transformation which is defined as follows [115], [116]:

$$H[x(t)] = \frac{1}{\pi}\int_{-\infty}^{\infty}\frac{x(\tau)}{t-\tau}d\tau \tag{3.1.1}$$

Where the function $x(t)$ is the input signal, which is a generic function that varies with time and the variable τ is the time transformation variable. The Hilbert transform is then the convolution of $x(t)$ with the kernel $\frac{1}{\pi t}$ across all time.

The Hilbert transform has some special properties that need to be considered. Firstly, the Hilbert transform output is a signal that has all of its positive frequency components shifted by -90° in time and all of its negative frequency components shifted by +90°. Secondly, The Hilbert transform when performed on the output of a Hilbert transform i.e. $H\big[H\big(x(t)\big)\big]$ the resulting output is equal to $-x(t)$ which is equivalent to a -180° phase shift in time. Lastly, and most importantly the Hilbert transform is a linear time-invariant operation, which is to say that if the Hilbert transform is performed individually on a differential signal $H[{V_{out}}^{+}(t)] - H[{V_{out}}^{-}(t)]$ it is equivalent to performing the Hilbert transform on the entire differential output $H[V_{out}] = H[{V_{out}}^{+}(t) - {V_{out}}^{-}(t)]$.

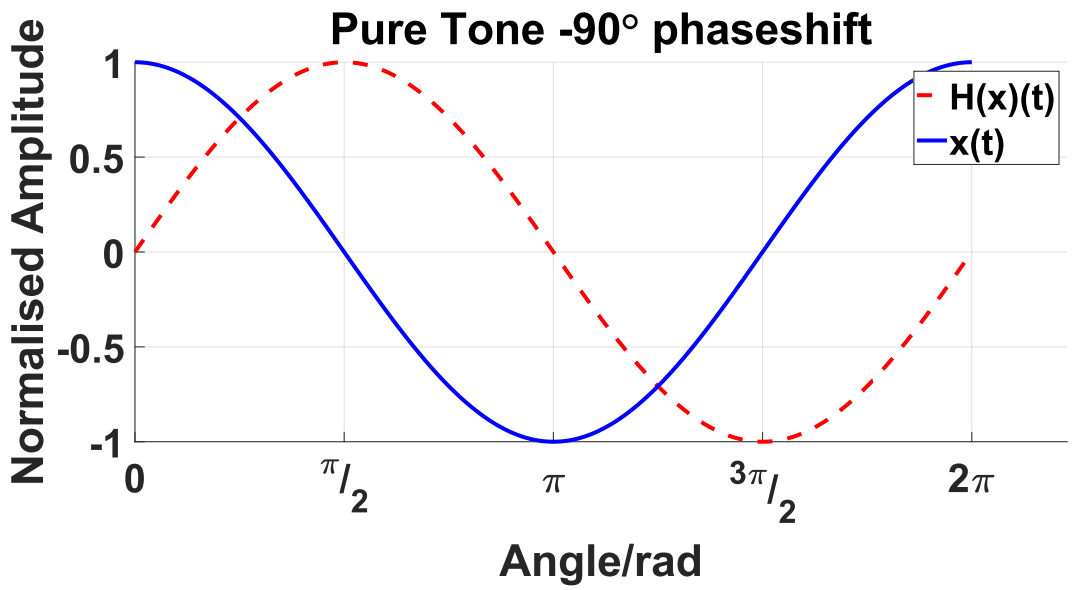


Figure 16: Normalised transient plot depicting the output of the Hilbert transform to illustrate the effect of a pure (-90° or $-\frac{\pi}{2}$ rad) phase shift on a cosine function over a time period of one wavelength.

The Hilbert transform can also be shown as a transformation in time as a pure -90 degrees phase shift as shown in Figure 16. The frequency definition of this approach can be written as a piecewise function as:

$$Phase\ Shift = \begin{cases} -90^o, & \omega > 0 \\ 0, & \omega = 0 \\ +90^o, & \omega < 0 \end{cases} \quad (3.1.2)$$

This definition of the Hilbert transform is more intuitive to understand than the traditional integration-based definition. As such, this will be the definition that will be in all future references to the Hilbert transform.

The utility of the Hilbert transform is made apparent in its powerful representation of a time-varying signal as a complex signal called the analytic signal. The analytic signal is a complex signal representation with real and imaginary parts [117], where the input signal is the real part of the analytic signal and the output of the Hilbert transform is the imaginary part of the analytic signal. In this new complex domain representation of the signal, the analytic signal has specific properties. The real part and imaginary part of the complex signal are 90 degrees out of phase. Additionally, due to this phase relationship between the imaginary and real parts of this analytic

signal, when the vector magnitude is computed for the real and imaginary parts of the signals, which is done by squaring both signals, adding them and then taking the square root, the resulting vector magnitude signal is equal to the analytic envelope. The analytic envelope is an exact representation of the signal's envelope, capturing more of the fine temporal details of a signal in comparison to the standard low-pass filter approaches. Furthermore, if the arctan of the ratio of the imaginary and real parts of the analytic signal is taken, then this will be equal to the instantaneous signal phase, and when the instantaneous phase signal is differentiated with respect to time, then this yields the instantaneous frequency.

These characteristics of the Hilbert transform are important to exploit when implementing the proposed architecture. The analytic signal, the analytic envelope, as well as the instantaneous frequency are all defined as shown below:

$$Analytic\ Signal: S(t) = X(t) + \boldsymbol{j}H\{X(t)\} \tag{3.1.3}$$

$$Signal\ Envelope\ < S(t) \geq \sqrt{\boldsymbol{Re}[S(t)]^2 + \boldsymbol{Im}[S(t)]^2} \tag{3.1.4}$$

$$Instantaneous\ Frequency: f(t) = \frac{d}{dt}\left[\arctan\left(\frac{\boldsymbol{Im}[S(t)]}{\boldsymbol{Re}[S(t)]}\right)\right] \tag{3.1.5}$$

The Hilbert transform does contain characteristics that seem, at first glance, similar to the Fourier transform. However, the Fourier transform is a signal decomposition technique that produces as an output a set of pure frequency tones whose amplitude contribution is such that the combined ratio of these frequency tones sums up to the original signal. As shown in the Figure 16, the Fourier transform will produce peaks at $\pm f_0$ for a pure tone with a frequency of f0, the difference is that for even functions, the negative frequency components are copies of the positive frequency components, whereas for odd functions, the negative frequency components are mirrors of the positive frequency contributions.

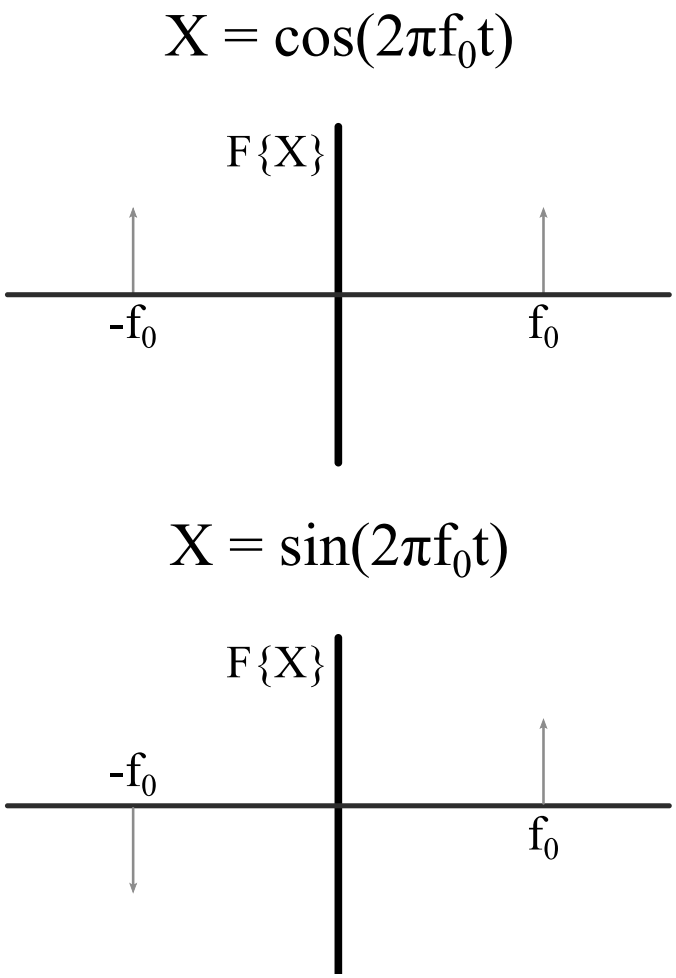


Figure 17: Outputs of the Fourier transform when applied on a pure tone with frequency of f0 for both even (top) and odd (bottom) functions.

The Fourier transform is a special decomposition technique, illustrated in Figure 17 with pure tones, where one of the main differences with the Hilbert transform is that the frequency output of the Fourier transform is the sum of all pure tone contributions, which span all time. On the other hand, the Hilbert transform can be used to obtain the instantaneous frequency of a signal from the resulting complex signal. Note that this comparison between the Fourier transform and the Hilbert transform resembles the attributes of the short-time Fourier transform. The short-time Fourier transform is a type of Fourier transform where the transformation is only applied to the signal at a specific time window. This window is bound in time, which shifts along with the signal. With a narrow enough window, the signal's instantaneous frequency can be approximated. However, this method of calculating frequency is still an average of the frequency content over the time window.

When it comes to audio decomposition in the context of cochlear implants, the Hilbert transform is more effective since it generates two crucial signals, the first of which is the analytic envelope. The analytic envelope differs from the standard low-pass filtered envelope in that it contains fine structures in its signal, which are landmarks or features in time. During nerve stimulation, these fine structures present in the signal provide additional information. Secondly, the analytic signal obtained from the Hilbert transform also provides an instantaneous frequency, which is extremely useful when it comes to stimulation. Knowledge of the instantaneous frequency means that an algorithm can be conceived, whereby the electrodes which are controlled during stimulation can be tuned in such a way that their stimulation rate is a mapping of the instantaneous frequency. In summary, the Hilbert transform is a very powerful and effective approach to signal decomposition. However, when considering its hardware implementation in circuit form, that is to say, implementing it as an analogue circuit, poses a far greater challenge; considering the area and power limitations given the type of computation that would generally be required.

3.1.1 Complex Demodulation

Complex demodulation is a technique commonly used in RF (Radio Frequency) electronics to upsample and downsample (right shift and left shift in frequency-domain) signals in preparation for wireless transmission and reception. Complex demodulation uses complex signal processing: [118]–[124] it treats signals as complex signals. An incoming signal is processed in a way such that two components are generated, the real part (also termed the in-phase/I component) and the imaginary part (quadrature/Q component) is a -90° phase shifted copy of the original.

3.1.2 LPF/HPF Phase Shifter

The second method for approximating the analytic signal uses both a LPF (Low Pass Filter) and HPF (High Pass Filter). The phase difference [125]–[129] between an LPF and a HPF always differs by 90° at all frequencies. Thus, if the corner frequencies are made equal, they

will have the same output amplitude only at the cut-off frequency for both filters. By passing the input signal through both filters in parallel it is possible to estimate the analytic signal in the same manner as described in the previous complex demodulation section.

3.2 Temporal Versus Spectral Signal Decomposition

When discussing signal decomposition in the context of cochlear implants for speech processing applications, two major paradigms emerge spectral signal decomposition and temporal signal decomposition. The first strategy decomposes the incoming audio signal in the frequency domain, whereas the second approach decomposes the audio signal in the time domain. Both approaches have their benefits and drawbacks. Nevertheless, no modern cochlear implant implementation always prioritises one approach over another. It is therefore critical to recognise that both approaches have their strengths and shortcomings and to use the strategy that is most effective when necessary. To emphasise the distinctions, the terms spectral decomposition and temporal decomposition must first be properly defined.

The spectral decomposition method is the first type of signal decomposition. This is accomplished by decomposing the incoming signal into several frequency bands. The resolution of these individual frequency bands can be adjusted to approximate the instantaneous frequency or maintained within the band pass filter's frequency resolution. For example, in a cochlear implant, spectral decomposition often occurs during the filter bank stage. That is, incoming audio is filtered through a series of band pass filters that constitute the filter bank. The output of each channel is equal to the input signal's band limited output, resulting in a coarse frequency mapping for each individual channel. Additionally, the benefit of spectral decomposition is that the information contained in each channel may be compared across channels by estimating the output signal strength across channels. Comparing frequency channels in this manner is especially advantageous when using algorithms for stimulation, as it will be required to determine which channels convey the most information.

Time decomposition, on the other hand, typically occurs following the filter bank stage. This is because once the frequency bands are determined, the time-varying information or signal features in time must be extracted. This includes frequency variations captured by the instantaneous frequency computation and amplitude changes captured by the analytic signal.

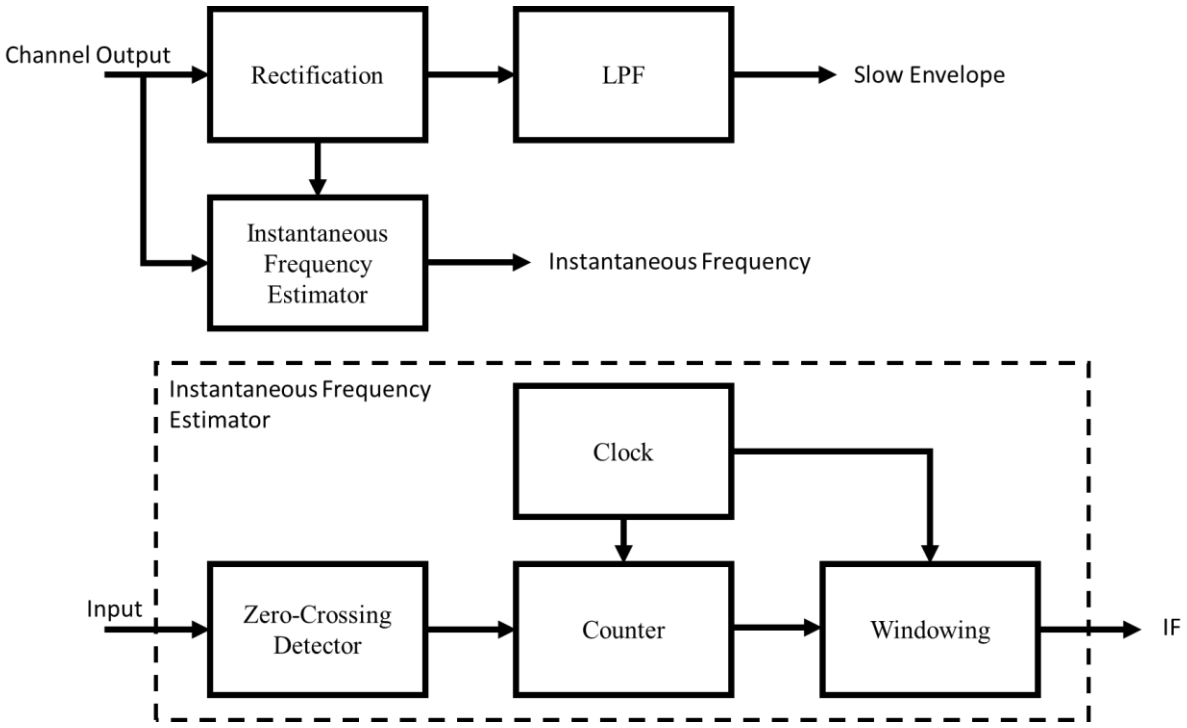


Figure 18: The top-level schematic showing the typical architecture used for estimating the instantaneous frequency using the zero-crossing detector method.

Accurately measuring and computing these features in audio is crucial if designers are to provide the listener with more enriching sounds. In general, the only approach to raise the resolution of spectral decomposition algorithms is to increase the number of channels in the filter bank. A cochlear implant with 16 channels, for example, will have a higher frequency resolution than one with only eight channels, provided the bandpass channel bands are equally spaced in the log frequency domain, this is because the number of channels replicate the place coding in the cochlea. When it comes to temporal decomposition methods, however, there are a plethora of alternative approaches to extracting this information [130]–[138]. Whether by detailed mathematical formulations that are computationally implemented in algorithms or through simple hardware approximations such as using zero-crossings as shown in Figure 18, understanding and acknowledging the limitations of each strategy when applied practically is important. This is because comprehending the algorithm's constraints entails fully exploiting the stimulation strategy that is chosen. The following sections will detail the proposed method to temporal decomposition in terms of what the top-level system design demonstrates and illustrates.

3.3 Lossy Integrator

The lossless integrator's transfer function is equal to $\frac{1}{s}$, where the variable s is the Laplace operator and has a complex frequency value equal to $j\omega$. However, it is impossible to design a perfect integrator at the transistor level since stray parasitics will always provide additional poles and zeros due, a pure capacitive or inductive load would result in a polar rotation as shown in Figure 19. As a result, the implementation employs a lossy integrator [139], [140], with a much larger operating region than is usually regarded normal in order to mimic the transfer function of a lossless integrator.

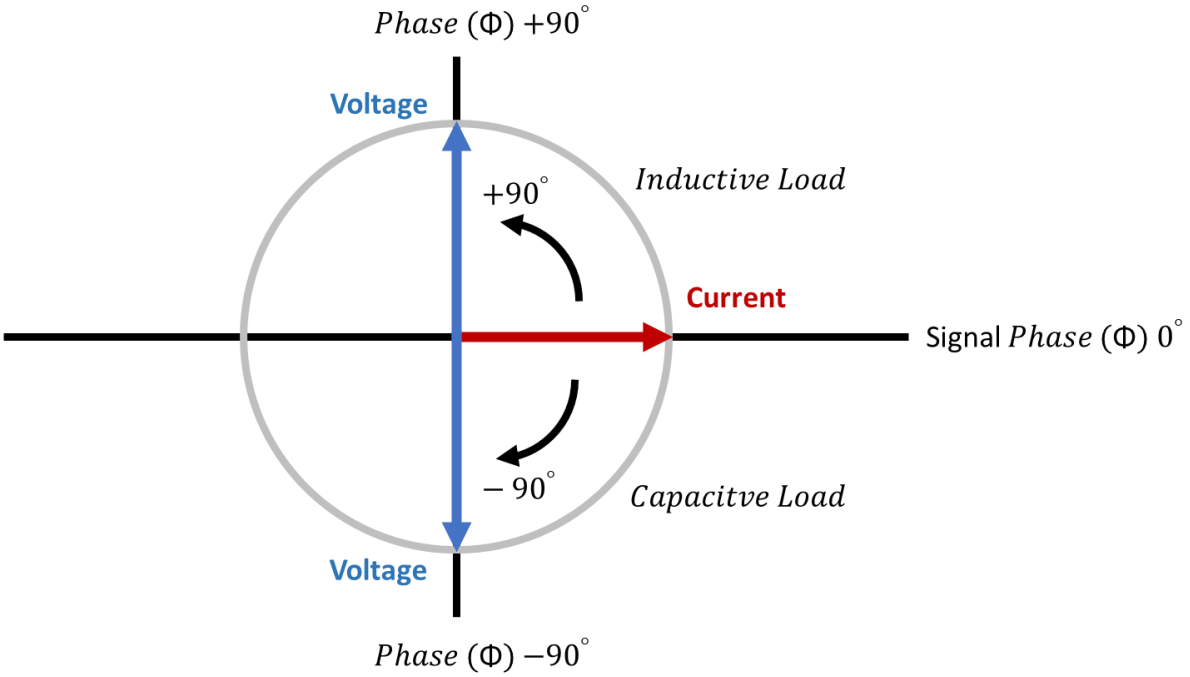


Figure 19: 90 degrees rotation in the complex plane. Note that -90 degrees phase shift corresponds to clockwise rotation whereas positive phase shift results in an anticlockwise rotation in the complex plane.

However, another disadvantage of this technique when contemplating a hardware implementation is that signals can only flow in one direction. That is to say that the signals are

only positive in log domain analogue circuits as described in more detail in Chapter 4. As a result, the lossless integrator is approximated as a lossy integrator, requiring an extremely high DC gain. Tuning the integrator's centre frequency would position it such that frequencies below the centre frequency are amplified while frequencies above the centre frequency are attenuated, leading to a mapping of frequency to gain.

If the resulting gain is dynamically or continuously computed, the instantaneous frequency can be determined continuously as a continuous-time continuous value signal. This can be accomplished computationally by calculating the rms values of the input and output signals and then the ratio of these two signals.

3.3.1 System Architecture

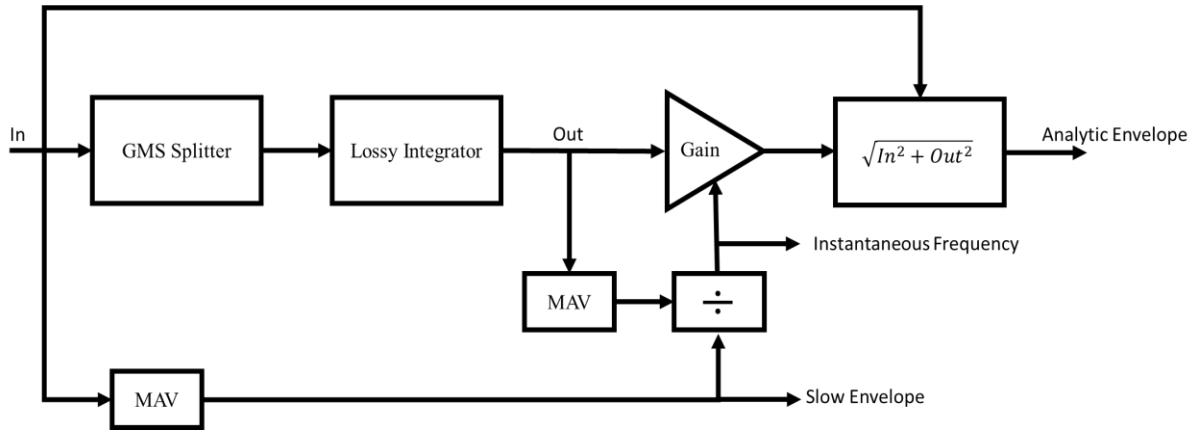


Figure 20: Schematic of the top-level block diagram illustrating the proposed system architecture for computing the slow envelope, the analytic envelope, and the instantaneous frequency in a continuous-time continuous value approach. The system uses a lossy integrator as its core for implementing the -90 degree phase shift.

Having described the architecture as shown in Figure 20 as well as the lossy integrator, this part will detail the proposed approach and demonstrate and discuss the results obtained using SIMULINK and MATLAB.

To verify and validate both the serial operation and implementation, this part will present the mathematical formulas necessary to comprehend the proposed system's operation. The technique has been implemented and validated using pure tones, modulated tones, chirp signals, and audio. This is modelled in SIMULINK as a lossy integrator of the form $\frac{k}{s+d}$ with a *k* of + 30, where k is a very large DC gain to match the gain normally achieved in practice and *d* is the cut-off frequency which is equal to 0 in the loss-less integrator. The following chapter will discuss and illustrate the proposed architecture's transistor-level implementation.

3.3.2 Feedback Versus Feedforward

To accommodate the broadest possible range of input frequencies, the system must be able to tune the filter response of the lossy integrator. As described in more detail in Chapter 4, this can be done by setting the bias current in the Seevinck integrator used to perform the lossy integration. The bias current could be set using either feed-forward or feedback circuitry. The feedforward strategy was chosen due to its simplicity and straightforwardness, as well as the fact that it eliminates the risk of the filter oscillating or becoming unstable. Additionally, the integrator is biased with a large current to ensure that the frequency is centred at the correct location and to cover the needed frequency ranges.

If, on the other hand, a feedback approach is used, a control signal must be continuously monitored to guarantee that the filter is always centred on the optimal frequency point. Implementing the feedback strategy will necessitate the addition of extra blocks to control the system's stability and responsiveness. A feedback system would be preferable for a long-term solution, as it allows for greater control over the approximations.

3.3.3 Theory of Operation

The work shown in this subsection has been developed in collaboration with Mr. George Gryparis. The mathematical derivation was done by Mr George Gryparis and validated with MATLAB simulations shown in (Figure 27- Figure 30) inclusive. The author developed and

optimised the system for cochlear implant applications shown in (Figure 20-Figure 26). The mathematical formulation for this approach builds a more natural intuition to the reader. The top level of the architecture of the system is shown in the Figure 20 and the mathematical descriptions used below reference the signals shown in this Figure.

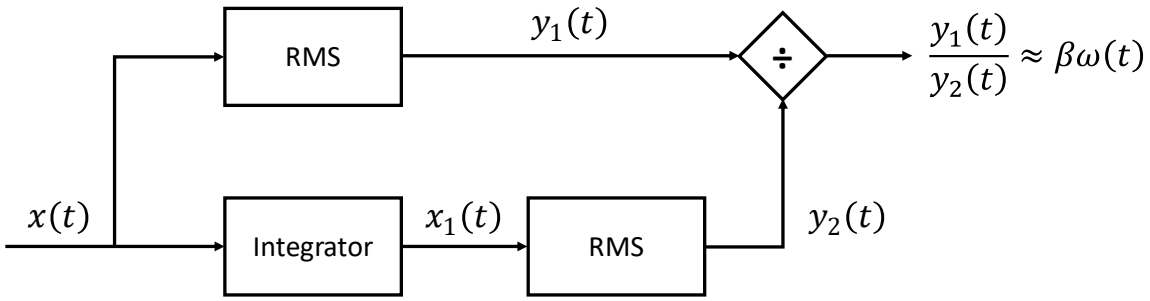


Figure 21: Top-level system of the proposed architecture, with the top branch output signal labelled as $y_1(t)$ and the bottom branch signal labelled as $y_2(t)$. The ratio of these two signals is a signal that is proportional to the input instantaneous frequency.

Figure 21 illustrates the top-level diagram of the proposed architecture. Firstly, some background on estimating, instantaneous frequency is required to understand the derivations shown here. The average frequency of a signal *s(t)* is the first moment of $|S(\omega)|^2$ about frequency ω this can be shown as:

$$\omega_{AV} = \frac{\int_0^\infty \omega|S(\omega)|^2 d\omega}{\int_0^\infty |S(\omega)|^2 d\omega} = \int_0^\infty \omega|S_n(\omega)|^2 d\omega \qquad (3.2.3.1)$$

Where $S_n(\omega)$ is equal to:

$$S_n(\omega) = \frac{S(\omega)}{\sqrt{\int_0^\infty |S(\omega)|^2 d\omega}} \qquad (3.2.3.2)$$

This expression can be intuitively interpreted as the weighted average of ω where the weight function is the normalised power spectrum, or alternatively, as the mean (μ) of the distribution which can be expressed as:

$$|S_n(\omega)|^2 : X \sim |S_n(\omega)|^2 \Rightarrow \omega_{AV} = E(X) \qquad (3.2.3.3)$$

Replacing $S(\omega)$ with the time-varying $S \leq (\tau, \omega)$ (obtained by using the STFT) allows for an estimation of the instantaneous frequency:

$$\omega_{inst}(\tau) = \frac{\int_0^\infty \omega|S(\tau,\omega)|^2 d\omega}{\int_0^\infty |S(\tau,\omega)|^2 d\omega} = \int_0^\infty \omega|S_n(\tau,\omega)|^2 d\omega \quad (3.2.3.4)$$

The STFT (short-time Fourier transform) is obtained by using a window function $\gamma(\tau)$ (Hann, Gaussian, Kaiser etc.) and applying the Fourier transform resulting in:

$$S(\tau,\omega) = \int_{-\infty}^{\infty} s(t)\gamma(t-\tau)e^{-j\omega t}dt \quad (3.2.3.5)$$

the mathematical derivation for the proposed approach utilises the Parseval theorem, which states that the sum of the square of the signal in time is equal to the sum of the square of the signal after the Fourier transform in frequency, this can be expressed as:

$$\int_{-\infty}^{\infty} |s(\mathrm{t})|^2 dt = \frac{1}{2\pi}\int_{-\infty}^{\infty} |S(\omega)|^2 d\omega \quad (3.2.3.6)$$

If it is assumed that the signal contains no negative frequency components, which is a valid assumption because the number of wave reflections inside a chip is negligible. In addition, if we assume that the signal at 0 time and 0 frequency is equal to 0, then the above expression can be expressed as:

$$\frac{1}{2\pi}\int_{-\infty}^{\infty} |S(\omega)|^2 d\omega = \frac{1}{\pi}\int_0^{\infty} |S(\omega)|^2 d\omega \quad (3.2.3.7)$$

And hence:

$$F\left\{\int_{-\infty}^{t} s(\tau)d\tau\right\} = \frac{1}{j\omega}S(\omega) \quad (3.2.3.8)$$

By utilising the above expressions, the following expression can be generated:

$$\int_{-\infty}^{\infty}\left|\int_{-\infty}^{t} s(\tau)d\tau\right|^2 dt = \frac{1}{2\pi}\int_{-\infty}^{\infty}\frac{1}{\omega^2}|S(\omega)|^2 d\omega = \frac{1}{\pi}\int_0^{\infty}\frac{1}{\omega^2}|S(\omega)|^2 d\omega \quad (3.2.3.9)$$

And the instantaneous frequency will therefore be equal to:

$$\omega_{est} = \frac{RMS\{s(t)\}}{RMS\left\{\int_{-\infty}^{t} s(\tau)d\tau\right\}} = \sqrt{\frac{\int_0^\infty |S(\omega)|^2 d\omega}{\int_0^\infty \frac{1}{\omega^2}|S(\omega)|^2 d\omega}} = \frac{1}{\sqrt{\int_0^\infty \frac{1}{\omega^2}|S_n(\omega)|^2 d\omega}} = \frac{1}{\sqrt{E\{X^{-2}\}}} \quad (3.2.3.10)$$

$$(for\ X \sim |S_n(x)|^2) \tag{3.2.3.11}$$

The instantaneous frequency ω_{est} would need to be compared to the average frequency by examining the deviation. It can be shown that if $s(t)$ is bandlimited to $[\omega_-, \omega_+] = [\omega_0(1-a), \omega_0(1+a)]$ then:

$$\frac{1-a^2}{1+a^2} \leq \frac{\omega_{est}}{\omega_{AV}} \leq \sqrt{\frac{1-a^2}{1-2a^2}} \tag{3.2.3.12}$$

This expression captures the worst-case scenario, however, commonly in audio applications $a \approx \frac{1}{4}$ and hence the above relation becomes:

$$0.88 \leq \frac{\omega_{est}}{\omega_{AV}} \leq 1.04 \tag{3.2.3.13}$$

In summary, by replacing $S(\omega)$ with the time-varying $S(\tau,\omega)$ (obtained by using the STFT) allows for an estimation of the instantaneous frequency:

$$\omega_{est} = \frac{1}{\sqrt{\int_0^\infty \frac{1}{\omega^2} |S_n(\tau, \omega)|^2 d\omega}} \tag{3.2.3.14}$$

3.4 Simulation Results

Having described the proposed architecture's theory of operation, this subsection will show results from both SIMULINK and MATLAB simulations.

The mathematical formulas necessary to check and validate both the operation theory and the robustness of the subsection's implementation will be described. SIMULINK and MALTAB results and figures will be displayed. The proposed method is implemented in SIMULINK and MATLAB and validated using pure tones, modulated tones, chirp and audio signals. SIMULINK approximates the integrator block as $\frac{k}{s+d}$ integrated block, where k is a very large gain to replicate the Seevinck integrator's large DC gain. After that, the system is tested and confirmed using the signals indicated above. Additionally, the following chapter will explore a proposed transistor level implementation of the system described in this chapter.

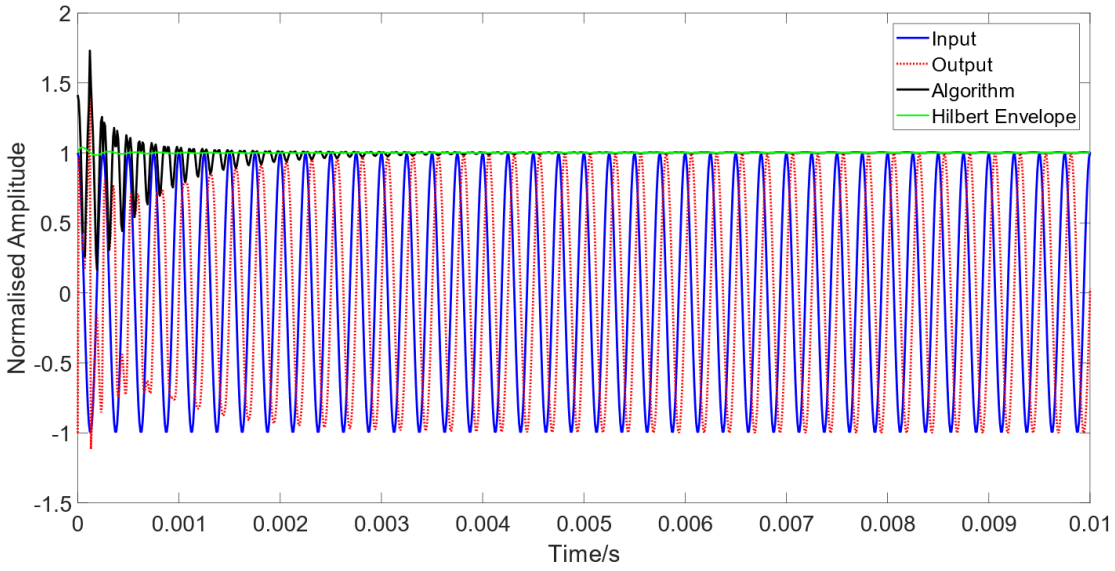


Figure 22: Pure tone wave with a frequency of 4 kHz shows both the ideal Hilbert envelope as well as the system output, which can be seen as a 90 degree phase shift with respect to the input. Using the input and output signals to generate the analytic envelope by calculating the vector magnitude which is shown in black.

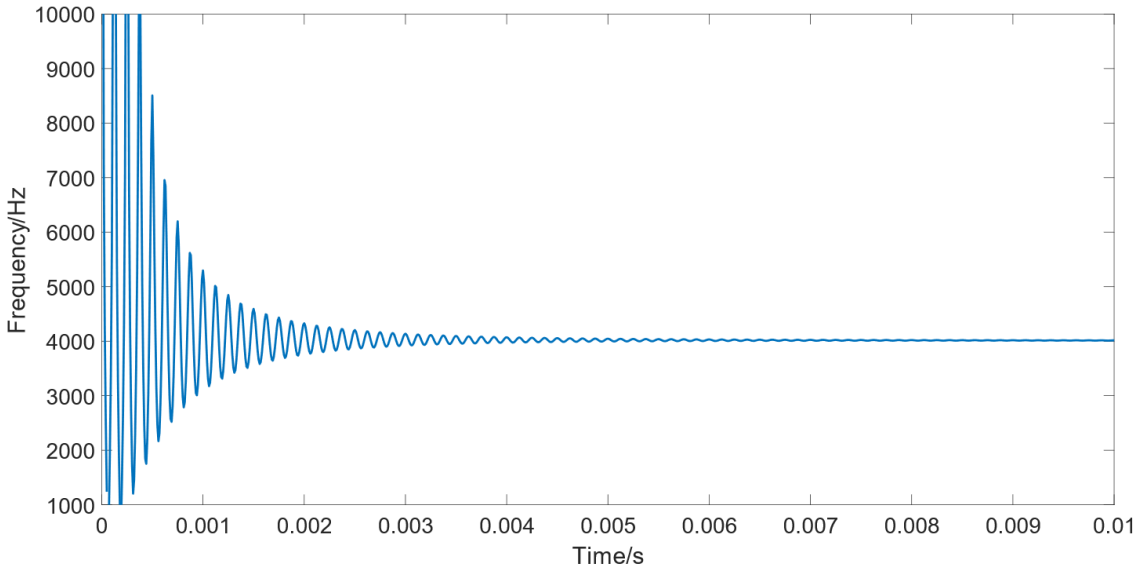


Figure 23: The instantaneous frequency measurement of the pure tone sine wave shown in Figure 22. The initial time before 0.003 s is the time it takes for the output signal to settle, but once the transitional dynamics have settled, the frequency signal stabilises.

Figure 22 and Figure 23 demonstrate the outputs of a pure tone sinusoidal wave with a frequency of 4 kHz. In Figure 22 the proposed algorithm envelope output is compared against the built-in MATLAB Hilbert envelope function. In the first 0.003 s the proposed system dynamics produces transients which then settle down to match the response of the Hilbert envelope, this is due to the HPF block present in the simulation which cause this decaying transient response.

In Figure 23 the graph shows the instantaneous frequency approximation, which also experiences a decaying transient before settling around 4 kHz.

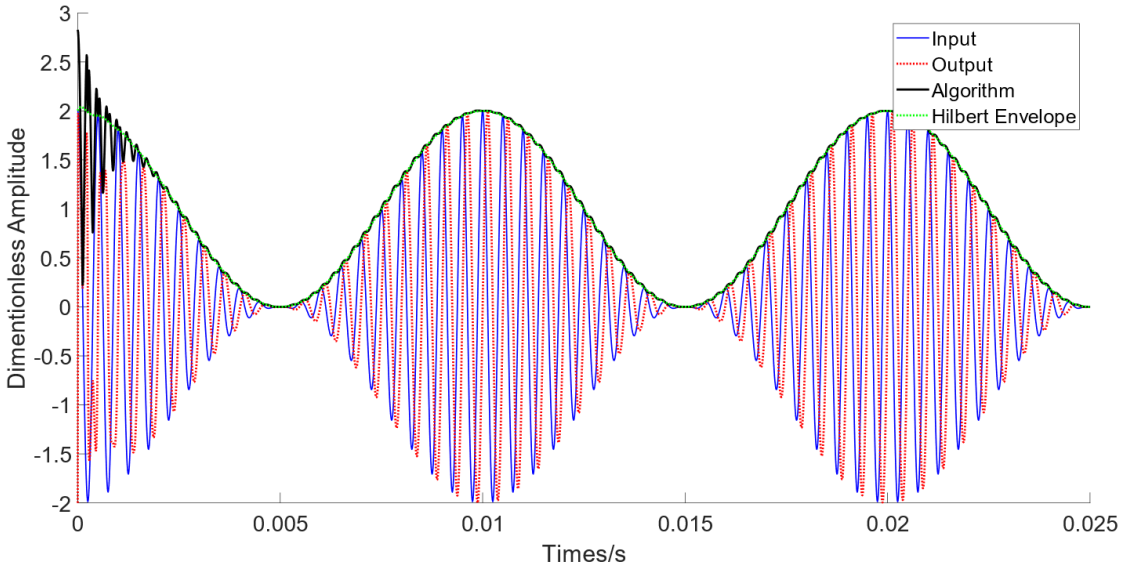


Figure 24: An AM (amplitude modulated) wave with a carrier frequency of 2 kHz and a modulating frequency of 100 Hz, which, according to the Fourier transform, consists of multiple frequency peaks. On the other hand, when utilising the proposed system, the output shown in red is in a 90-degree phase with the signal carrier. The analytic signal is calculated by computing the vector magnitude of the input and output signals, which is shown in black. This can be compared with the Hilbert envelope, which is shown in green.

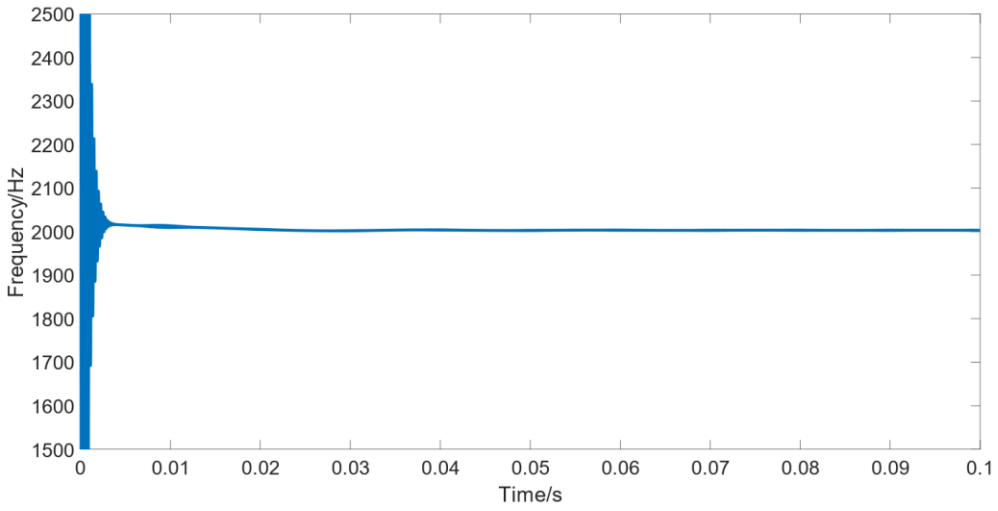


Figure 25: The instantaneous frequency of the amplitude modulated wave signal shown in Figure 24, with a carrier frequency of 2000 Hz. Note that the envelope frequency is not captured by this signal.

Figure 24 and Figure 25 illustrate the envelope and instantaneous frequency outputs of an AM (Amplitude Modulated) sine wave with a carrier frequency of 2 kHz and a modulating signal frequency of 100 Hz. In Figure 24 the proposed algorithm tracks the modulating envelope, closely matching the response of the Hilbert envelope. There still exists a decaying transient in both Figure 24 and Figure 25, which is also due to the HPF block. In Figure 25 this instantaneous frequency algorithm output also settles at the carrier frequency of 2 kHz matching the aforementioned AM signal input settings.

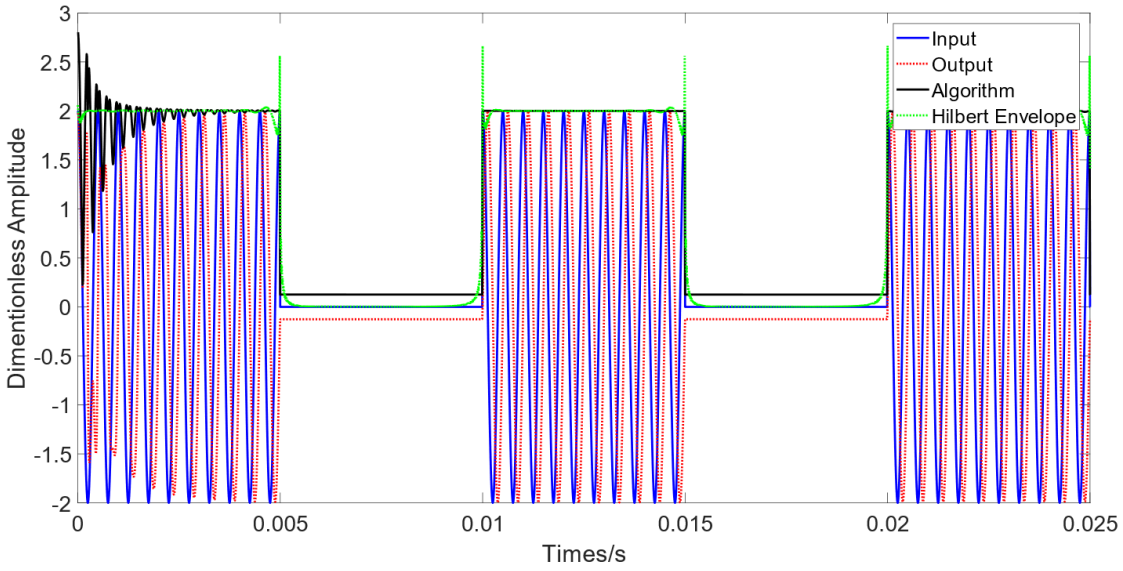


Figure 26: A sine wave modulated by a square wave. The modulated output highlights time instances where the frequency, as defined by the instantaneous frequency, should be zero, while this is not the case with the Fourier transform definition. The plot also shows the analytic envelope as calculated by the proposed algorithm as well as using the built-in Hilbert analytic signal function in MATLAB.

Figure 26 depicts an AM signal with a square wave modulation, this simulation was performed to showcase the system's response to sharp amplitude changes which is a limitation of obtaining the envelope using a filtered rectified wave. Although the system is able to track the signal's envelope it does not reach zero during the 'off' cycles this is due to numerical integration by the solver which would not occur in practice.

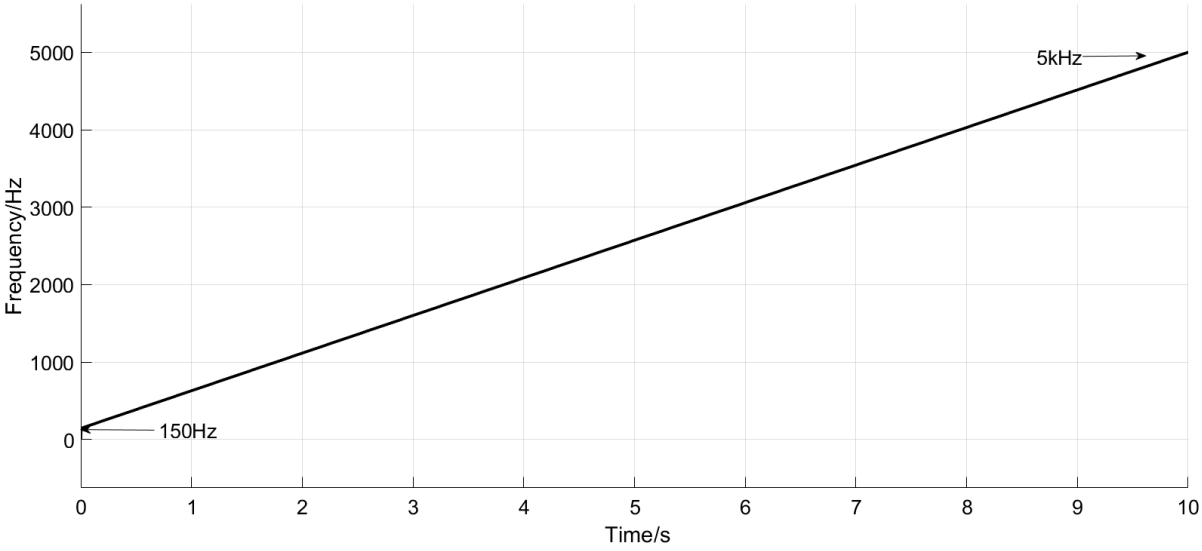


Figure 27: The instantaneous frequency signal obtained when simulating the test case of a chirp signal. The output plot shows the starting frequency of 150 Hz and a final frequency of 5kHz.

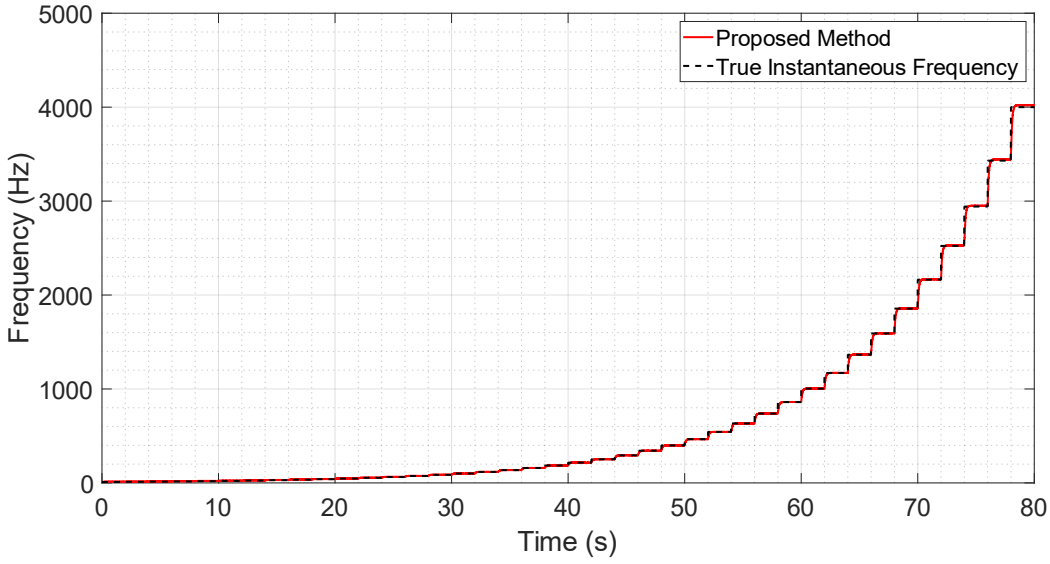


Figure 28: (Simulation by Mr George Gryparis) Time plots showing the comparison between the instantaneous frequency method and the true instantaneous frequency of a chirp signal plotted on top of each other across time. With a duration of 80 seconds and a frequency starting from 0 Hz to 4000 Hz.

Figure 27 illustrates the proposed system's response to a linear chirp signal which starts at 150 Hz and ramps up to 5 kHz over a period of 10 seconds. The decaying transient still exists in

this test case however, the system is able to track the frequency after the transients have settled. Figure 28 is another system simulation with a chirp input although the chirp frequency is increasing exponentially in this case in steps, from a starting frequency of 0 Hz to a frequency of 4 kHz over a period of 80 seconds. The proposed method matches very closely with the true known instantaneous frequency.

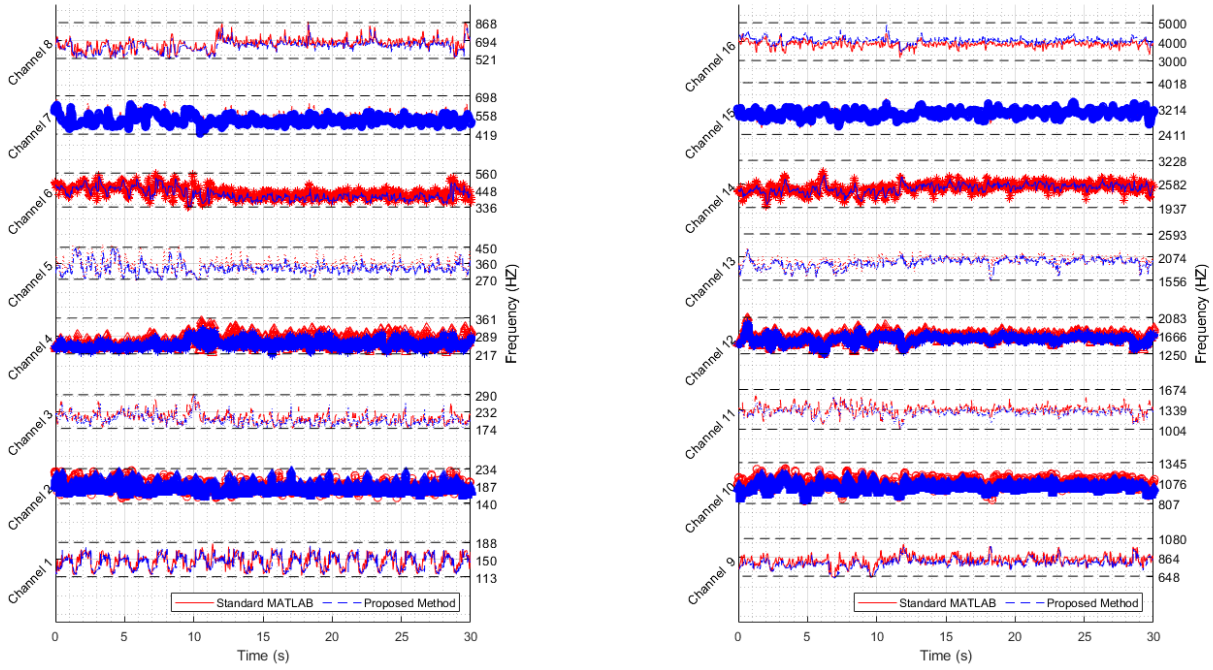


Figure 29: (Simulation by Mr George Gryparis) Plot showing the outputs of 16 logarithmically spaced bandpass filters. Each bandpass filter represents the channel of a cochlear implant with audio input. The outputs shown are the instantaneous frequencies of both the MATLAB built-in functions and the proposed method.

Figure 29 is a simulation test where the outputs of 16 logarithmically spaced bandpass filters are input into the proposed system, the performance of the proposed system and the standard MATLAB instantaneous frequency measurements are compared in each of the 16 channels. The outputs seem to match in shape with the standard method although as will be shown in the next set of results the performance of the system is dependent on the cut-off frequency of each channel with respect to the channel's centre frequency.

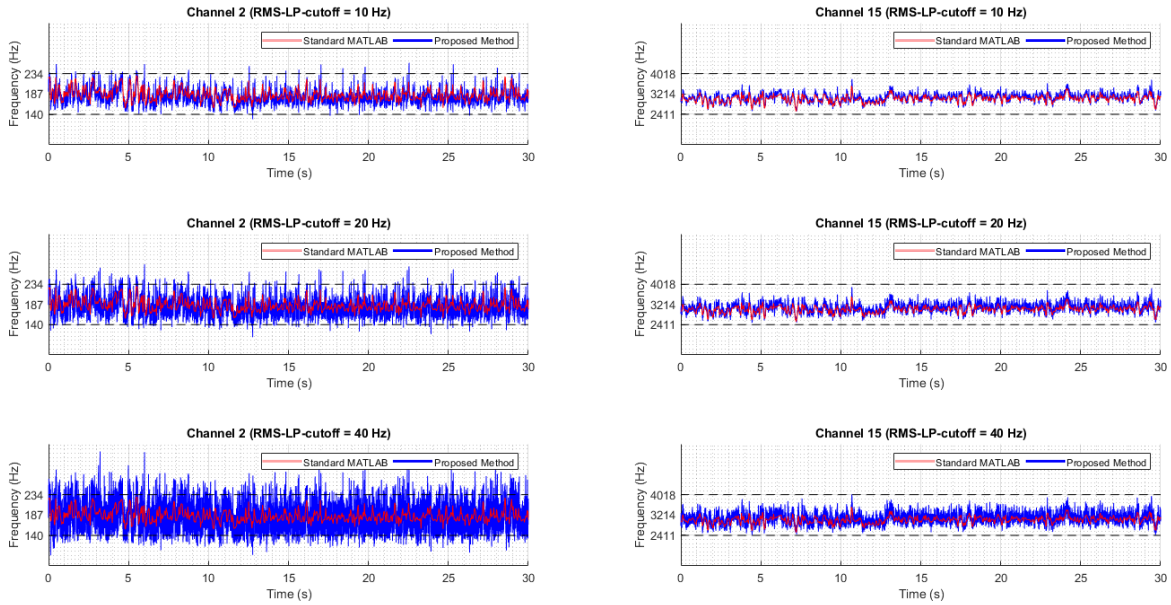


Figure 30: (Simulation by Mr George Gryparis) Comparing the outputs and the accuracy of the proposed method versus the MALTAB standard function when the window of the RMS block is changed, this is done by changing the cut-off of the low pass filter. On the left-hand side, the graphs shown are for a low frequency channel, and the graphs shown on the right are for high frequency channels. Note that a lower cut-off for the RMS is preferable for the MATLAB function. Whereas for higher cut-offs, the proposed method outperforms the standard MATLAB function when it comes to low frequency channels.

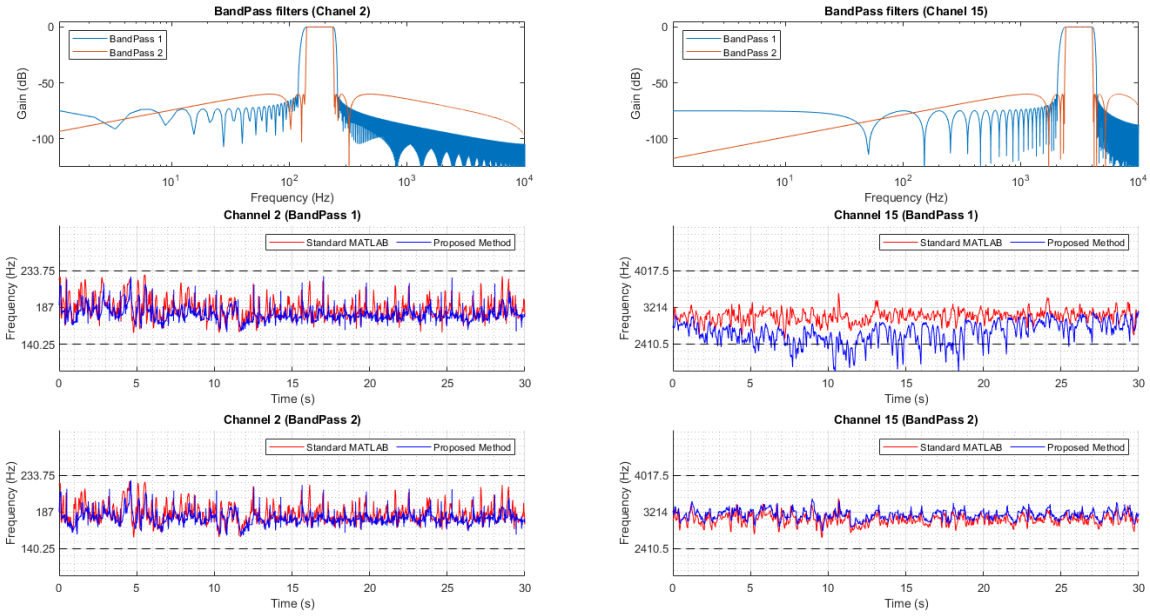


Figure 31: (Simulation by Mr George Gryparis) The effect of bandpass filter choice on low frequency channels and high frequency channels. For low-frequency channels, or higher-order bandpass filters, it appears that there is not much of a difference between the proposed method and using higher-order bandpass filters; however, for high frequency channels, it appears that the proposed method works better for steeper bandpass filters.

Figure 30 and Figure 31 showcase the effects of the RMS cut-off frequency and the bandpass filterbank order. *Figure 30* depicts the change in performance of the proposed method as the cut-off of the RMS changes for both low and high frequency channels. For low channels a lower RMS cut-off is desirable to reduce errors and conversely a higher RMS cut-off increases the instantaneous frequency measurement error for low frequency channels. On the other hand, for higher frequency channels the RMS cut-off has very little effect on the instantaneous frequency error. Figure 31 shows that the order of the bandpass filter i.e., its steepness, has little effect on low frequency channels on the frequency estimation error, whereas the bandpass filter order is critical in obtaining an accurate frequency estimation for higher frequency channels.

In summary the proposed method is to be implemented on a per channel basis such that the estimation errors can be reduced. For low frequency channels a combination of a low cut-off

RMS and a low order bandpass should be used. Conversely, for higher frequency channels high order bandpass must be used while the effects of the RMS cut-off are negligible.

Chapter 4

Transistor Level Design of the Log-domain Implementation of the Hilbert Transform approximation

4.1 System Transistor Level Blocks in Weak Inversion

To implement a transistor-level topology which estimates both the analytic signal envelope and instantaneous frequency, a novel approach would need to be taken into consideration. The primary reason for using a hardware-based solution to approximate these signals is that transistors enable the designer to optimise the performance by utilising ultra-low-power operation throughout the entire system [141]–[150]. The result of this approach yields a design which can then be integrated into a more complex system on chip solution, advancing the aim of a completely implantable cochlear implant device [151].

However, implementing signal processing algorithms in hardware, particularly transistors, adds another layer of complexity and rigidity in contrast to software-based approaches. Transistors are physical objects and, unlike software algorithms, cannot be easily modified in response to external environmental drifts. As a result of this, the expected outputs which should change and adapt in accordance with external stimuli, is not able to shift its mode of operation. Therefore, this means that the proposed system would be required to reach a comparable degree of flexibility when compared to software algorithms. This would result in a topology that is not only flexible, but also consumes very little power and has a wide input dynamic range. All of the above can be accomplished by operating the transistors in the subthreshold regime.

Classical circuit design approaches usually involve synthesizing voltage-mode circuit blocks that operate in strong inversion, this is further explained in Section 4.1.1. In contrast to this, the subthreshold regime allows for the design of log-domain circuits, enabling a wide input dynamic range whilst maintaining a very low voltage headroom typically between 1 to 3 V for the AMS 0.35µm CMOS technology. The choice of transistor technology was selected due to its maturity and is well characterised for analogue based circuits. This allows the designer to reduce the total number of blocks using signal companding techniques by swapping out voltage-mode blocks with current-mode blocks. This is possible because the signals flowing between different log domain blocks are current signals. Current based signals can be added and subtracted more simply than voltage-based signals. Additionally, it is possible to compute the multiplication, division, and other more complicated relations between signals with a very small number of log domain blocks. This makes the log-domain approach incredibly block efficient, and further highlights the benefits of why the log-domain blocks were chosen for this system.

The goal, and hence the objective of the proposed system, is to accomplish continuous-time, continuous-value signal processing. This is realistically achievable using log domain blocks since all operations are performed on current based signals. Thus, the design objectives for this proposed system include approximating the analytic signal envelope, slow envelope and estimating the instantaneous frequency of the signal. The results of operating in a low power environment whilst allowing a high input dynamic range will be demonstrated and explained in this chapter. The demonstrated findings are encouraging, confirming the validity of the proposed approach.

4.1.1 Log-domain Principle and the Proposed Architecture

A MOSFET device is of two types, a p-type (pmos) and n-type (nmos). Moreover, the nmos device has four terminals a source, drain, bulk and gate. The voltages at these particular terminal nodes are typically labelled as V_S, V_D, V_B and V_G respectively as shown in Figure 32.

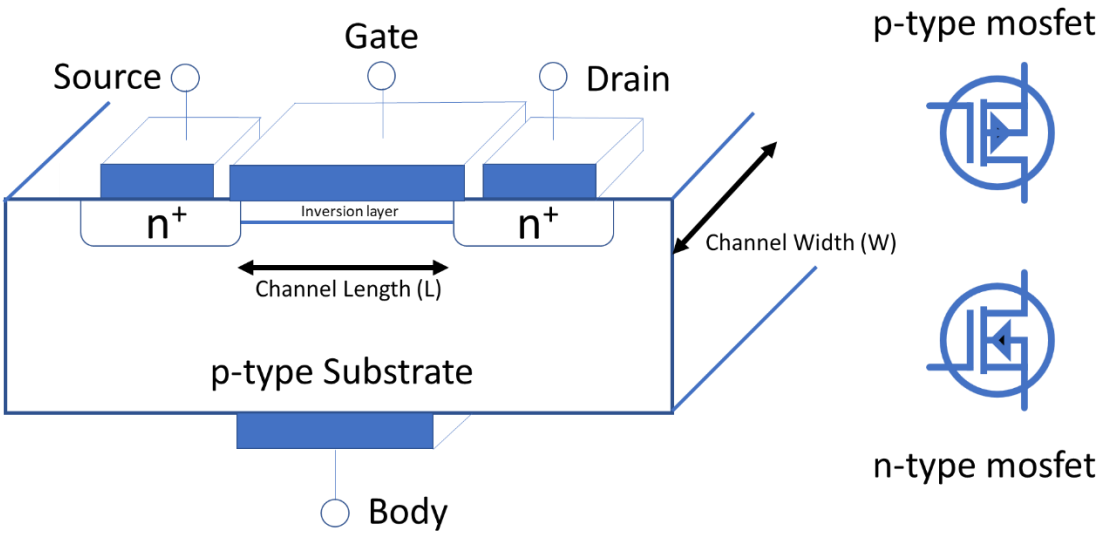


Figure 32: The cross-section of a n-type mosfet showing the various doped regions with 4 terminals the source, gate, drain and body. The right side shows the symbol view as is used in schematic designs.

In the case of strong inversion the current, I_D, flowing through the drain of a MOS device is defined by the following relationship:

$$I_D = \frac{W}{L}\mu C_{ox}\left(V_{GS} - V_{TH} - \frac{V_{DS}}{2}\right)V_{DS}, \tag{4.1.1.1}$$

$$V_{DS} \leq V_{GS} - V_{TH} \tag{4.1.1.2}$$

$$I_D = \frac{1}{2} \cdot \frac{W}{L} \mu C_{ox} (V_{GS} - V_{TH})^2, \tag{4.1.1.3}$$

$$V_{DS} \geq V_{GS} - V_{TH} \tag{4.1.1.4}$$

I_D indicates the drain current, $\frac{W}{L}$ is the aspect ratio of the mosfet device, where W is the width of the device and L is the channel length between the source and drain terminals. C_{ox} is the oxide capacitance, a technology specific parameter. Lastly, V_{GS}, V_{DS} and V_{TH} are the gate-source voltage, the drain source voltage and the threshold voltage respectively. When V_{DS} is larger than (V_{GS} - V_{TH}) then the MOSFET device is considered in strong inversion, which is also sometimes referred to as the square current relationship of the transistor.

In order to build log domain devices, the transistors must operate in subthreshold. This is also sometimes known as the weak inversion regime. The current flowing through the drain during subthreshold operation can be expressed by the following equations:

$$I_D = \frac{W}{L} I_S e^{\frac{V_{GS} - V_T}{nV_T}} \left(1 - e^{-\frac{V_{DS}}{V_T}}\right) \tag{4.1.1.5}$$

$$When: V_{DS} \geq 4V_T \tag{4.1.1.6}$$

$$\Rightarrow I_D = \frac{W}{L} I_S e^{\frac{V_{GS} - V_T}{nV_T}} \tag{4.1.1.7}$$

Where n is an unitless characteristic constant that ranges from 1 to 2, V_T is the thermal voltage typically around 26 mV at 300 K, and I_S is the characteristic current of the transistor, which is a technology specific parameter. All the transistor devices in this section operate in weak inversion unless specifically mentioned otherwise.

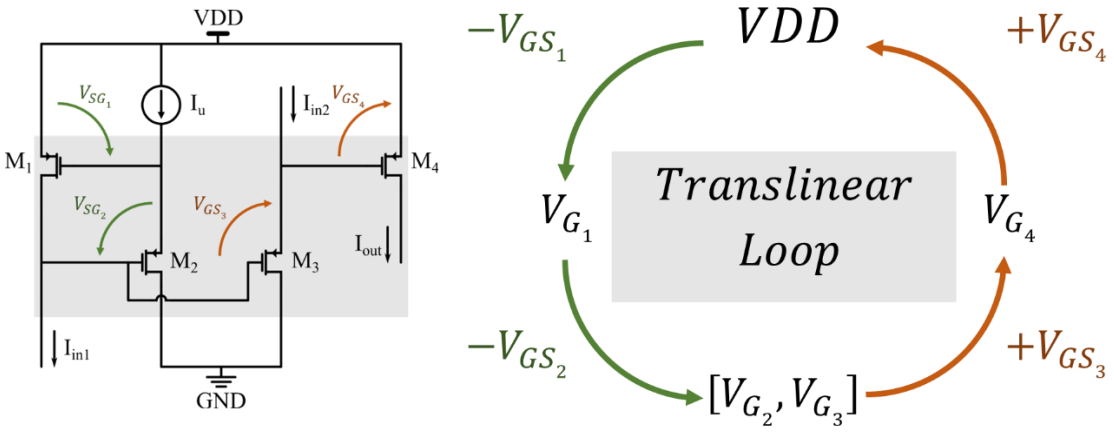


Figure 33: (Left) Log domain multiplier circuit depicting the gate source voltages is across all four devices forming a translinear loop. (Right) Voltage loop diagram depicting the log domain multiplier illustrating the translinear loop as a series of negative and positive gate-source voltages starting at VDD and ending at VDD.

Figure 33 depicts a log domain multiplier, consisting of four p-type devices. To calculate the value of I_{out} the analytical derivation is as follows:

$$I_{D_n} = \frac{W_n}{L_n} I_S e^{\frac{V_{GS_n} - V_T}{nV_T}} \tag{4.1.1.8}$$

$$V_{GS_n} = nV_T \cdot ln\left(\frac{L_n}{W_n} \cdot \frac{I_{D_n}}{I_S}\right) + V_T \tag{4.1.1.9}$$

From the above translinear loop:

$$V_{GS_1} + V_{GS_2} = V_{GS_3} + V_{GS_4} \tag{4.1.1.10}$$

$$\left[nV_T \cdot ln\left(\frac{L_1}{W_1} \cdot \frac{I_{D_1}}{I_S}\right)\right] + \left[nV_T \cdot ln\left(\frac{L_2}{W_2} \cdot \frac{I_{D_2}}{I_S}\right)\right] = \left[nV_T \cdot ln\left(\frac{L_3}{W_3} \cdot \frac{I_{D_3}}{I_S}\right)\right] + \left[nV_T \cdot ln\left(\frac{L_3}{W_3} \cdot \frac{I_{D_3}}{I_S}\right)\right] \tag{4.1.1.11}$$

By keeping the aspect ratio of all devices equal, the above equation can be reduced to:

$$\ln(I_{D_1}) + \ln(I_{D_2}) = \ln(I_{D_3}) + \ln(I_{D_4}) \tag{4.1.1.12}$$

$$I_{D_1} \times I_{D_2} = I_{D_3} \times I_{D_4} \tag{4.1.1.13}$$

After setting the above currents to the following constraints:

$$I_{D_1} = I_{in_1} \tag{4.1.1.14}$$

$$I_{D_2} = I_u \tag{4.1.1.15}$$

$$I_{D_3} = I_{in_2} \tag{4.1.1.16}$$

$$I_{D_4} = I_{out} \tag{4.1.1.17}$$

This leads to the following signal operation to be obtained:

$$I_{out} = \frac{I_{in_1}}{I_{in_2}} \cdot I_u \tag{4.1.1.18}$$

Where I_u is the unit current, the above example divides I_{in1} and I_{in2}. However, if the current I_{in2} and I_u are swapped around then multiplication can instead be achieved. The log-domain principle is a powerful approach to circuit design, and especially for current-mode signal processing, which is realised by constructing translinear loops using devices operating in the subthreshold regime. As long as the devices are of the same size, and a complete voltage loop is constructed such that the voltage difference across the entire loop is 0 V as shown in the example above, it is therefore possible to employ several signal processing blocks by constructing translinear loops in an efficient manner.

4.2 The Proposed Architecture

In the previous chapter, the top-level schematic of the proposed architecture was described and explained. However, migrating the same signal flow from concept to transistor level requires modifying the blocks and considering the limitations of signal processing in hardware. This involves taking into account several constraints, such as size, computational accuracy, power consumption, signal integrity, and directional signal flow paths, which are physical phenomena.

Shown in Figure 34 is the proposed schematic architecture implemented at the circuit level. The input bi-directional signal, which is the output to the filter bank, passes through a geometric mean splitter creating a differential signal, this new signal pair is positive only. This is designed as such to increase both the dynamic range as well as the ability to use log domain signal processing blocks. This new differential input signal is copied using current mirrors, the first

copy through a differential Seevinck lossy integrator and the second copy passes through a mean absolute value block.

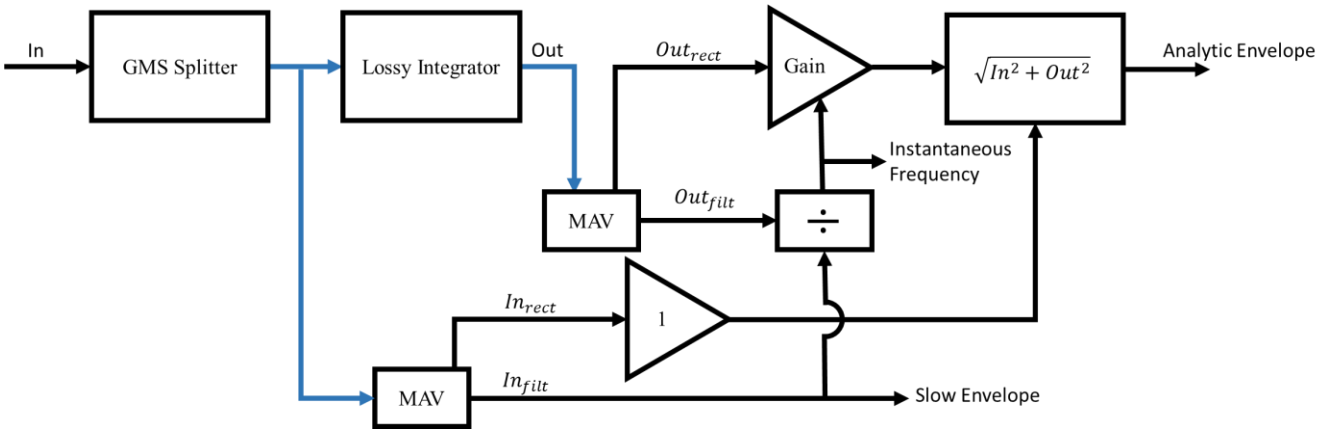


Figure 34: Top level block diagram showing the circuit implementation of the proposed architecture estimating the slow envelope, analytic envelope and the instantaneous frequency. The signals shown in blue represent differential pairs of signals.

The MAV (Mean Absolute Value) blocks produces two signals the first of which is a rectified signal $[In_{rect},\ Out_{rect}]$, and the second signal is a filtered signal $[In_{filt},\ Out_{filt}]$; the latter output produces the slow envelope. The output of the lossy integrator produces a differential output with a phase shift as well as a gain which is frequency dependant. The output signal passes through an identical MAV block to also produce a rectified output signal and a filtered output signal. The current ratio of the filtered output and the filtered input signal is then computed using a log multiplier to obtain a current signal corresponding to the instantaneous frequency. This signal, due to its frequency dependence, can be used to control the gain of a log multiplier block to adjust the amplitude of the rectified output signal.

To obtain the final analytic envelope signal, the output rectified signal must be first adjusted such that it matches the amplitude of the filtered input signal. The reason for applying this gain on the rectified input and output signals is because the vector magnitude block only accepts unidirectional signals in one of the inputs. However, in order to maintain the phase relationship between the input and output signal, it becomes critical to maintain the same signal pathways between the input and output signals. Therefore, as depicted in the figure above, the rectified input signal passes through a unity gain log domain multiplier. The rectified input signal and

the gain adjusted rectified output signal are then fed into a vector magnitude block which computes the analytic envelope.

4.2.1 GMS Splitter

The first block in the signal processing pipeline is the geometric mean splitter shown in Figure 35, which is a log domain block that accepts a bidirectional current signal as an input and generates two output signals, obeying the following relationships:

$$I_{out}^{u,l} = \frac{1}{2}\sqrt{4I_{bias}^2 + I_{in}^2} \pm I_{in} \quad (4.2.1.1)$$

$$I_{in} = I_{out}^{u} - I_{out}^{l} \quad (4.2.1.2)$$

Where I_{in} is the input current, $I_{out}^{u,l}$ are the upper and lower output current signals respectively and I_{bias} is the biasing current. The GMS splitter is a log domain circuit that consists of a left and right side which are mirrored; M1-M4 form the left-hand side translinear loop, and M5-M8 form the right-hand side translinear loop. The balanced design allows the sourcing and sinking of the input current on the right- and left-hand side respectively.

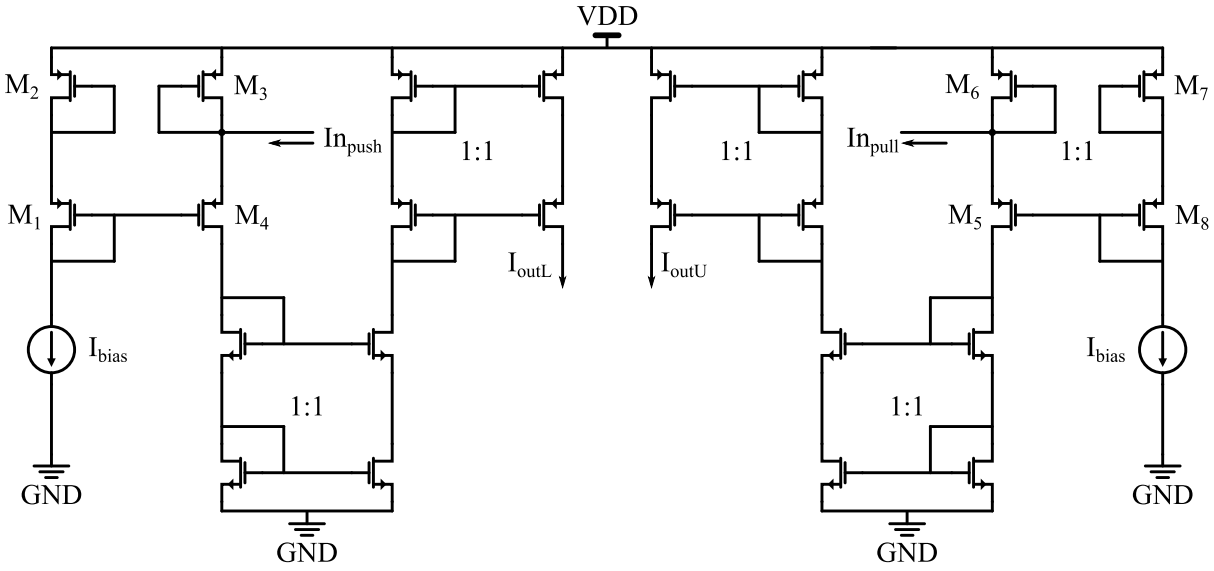


Figure 35: Transistor level implementation of the balanced log domain GMS circuit, M_1 - M_4 form the first translinear loop and M_5-M_6 form the second translinear loop. The balanced design allows the input current to be both sourced and sinked enabling bi-directional input current flow.

The positive only output signals ($I_{out}^{u,l}$) are synthesised in a way such that their difference is equal to the original input signal. This is referred to as a geometric mean splitter; by splitting an input current-based signal into complementary positive-only output signals whose difference equals the original signal. The output signals' features allow for parallel computation of linear and time invariant operations as long as the mathematical operation obeys the cumulative, associative and distributive laws.

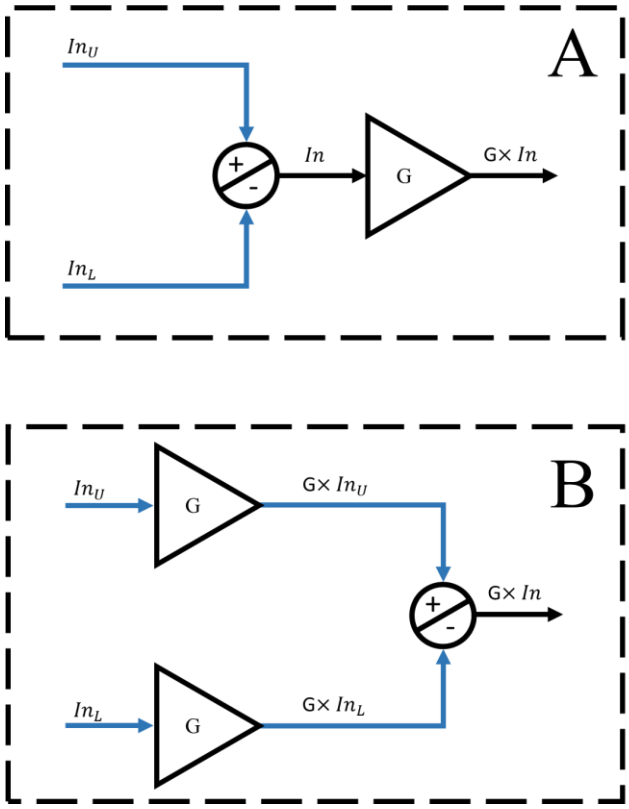


Figure 36: (Top) signal flow diagram showing a gain applied to the difference of two signals. (Bottom) signal flow diagram showing gain applied to individual signals resulting in an overall gain to the differential signal. Both of these approaches yield the same output expression. However, in the bottom case the resulting topology yields a greater dynamic range.

By employing a differential signal processing technique as shown in Figure 36, it is possible to generate a very wide input dynamic range by separating the bidirectional signals into positive only signals. Additionally, because the signal is split into two halves with each half generating a unidirectional signal, log domain blocks can be optimised assuming no directional current reversal, which would destroy the log domain relationship.

The GMS splitter operates in two primary modes. The first mode of operation is known as class-A operation, which occurs when the input signal has a very large DC component in comparison to its AC amplitude, for example in the case of small AC signals present in bio-signals such as EEG. The second mode of operation of the GMS splitter is known as pseudo class AB operation. This mode is used when the incoming signal has a very large AC amplitude in comparison to its DC bias, as is the case with the generated large output signals from the OZGF filter bank, which are considered pseudo-class AB, meaning that both output signals

contain only half of the original sound wave. By having these two modes of operation, a high dynamic range can be achieved irrespective of the input AC amplitude size in relation to its DC bias, up to a certain limit. Both types of operation impose two constraints on the output signals: firstly, the current can only flow in one direction, and secondly, the difference between the output signals is the original input signal.

If the subsequent blocks are all executed by time-invariant systems, the difference between the resulting operations would be equivalent to performing the same operation on the bi-directional input signal as depicted in Figure 34. However, log-domain blocks for bidirectional currents are not necessarily feasible for all types of signal operations. The dimensions of the mosfet devices and the biasing currents used are shown in Table 2.

Table 2: Device sizes and bias current values for the balanced GMS circuit.

Differential Balanced GMS	
Parameter	**Value**
VDD	1.8 V
W_{PMOS}	300 µm
L_{PMOS}	1.5 µm
W_{NMOS}	60 µm
L_{NMOS}	8 µm
I_{bias_GMS}*	20 nA

* The current value shown is the nominal value.

4.3 Seevinck Integrator

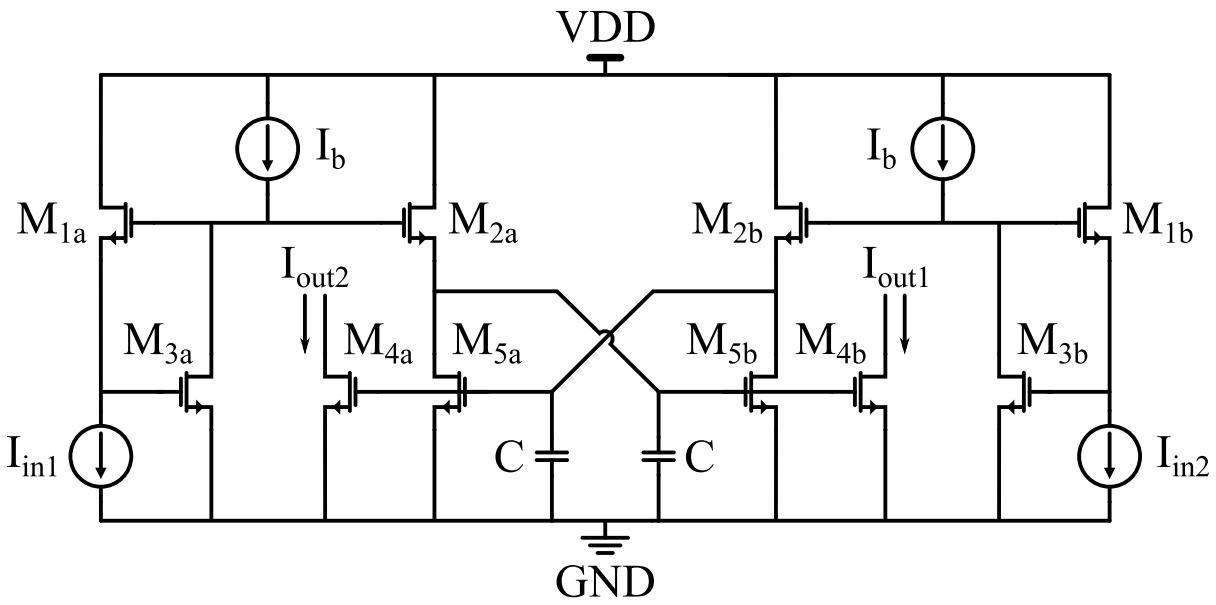


Figure 37: Log domain circuit of the fully differential input Seevinck integrator. The left and right capacitors should have the same capacitance value to reduce phase errors.

To produce a -90° phase shift at the output, the input signal is integrated. By ensuring that incoming audio signals are narrowband signals, in which the frequency bandwidth of the signal is much lower than its carrier frequency, the approximation is considered valid such as in the case of the filterbank outputs from audio signals. In this case an integrator block can be used to produce this phase shift.

Simply defined, an integrator is an amplifier with a capacitor connected in its feedback loop. Capacitors have a voltage to current relationship which are described by the following equivalent equations:

$$I_{cap} = C\frac{dV_{cap}}{dt} \tag{4.3.1}$$

$$V_{cap} = \frac{1}{C}\int I_{cap}dt \tag{4.3.2}$$

Where C is the capacitance, I_{cap} is the current through the capacitor and V_{cap} is the voltage across the capacitor. If the capacitor's input is a current based signal, this results in a voltage

equal to the integral of the current flowing through the capacitor. However, in order to convert an integrated voltage into a current, the integrated voltage must be transformed back to a current. This is achieved by exponentiating the output voltage node back into a current (Equation 4.1.1.8).

The Seevinck integrator shown in Figure 37 was chosen over other types of integrators [152]–[158] due to its fully differential architecture [159], [160], which allows the GMS splitter to output current directly to the Seevinck integrator. Due to the integrator's differential construction, it is also a balanced design, with a capacitor on both the left and right branches. These capacitors integrate the current that flows through them, which is subsequently exponentiated into a current signal (Equation 4.1.1.8) from an integrated voltage signal. The Seevinck integrator contains two translinear loops, on the left-hand side the first loop is formed by $M_{3a,1a,2a,5a}$ with M_{4a} simply mirroring the current passing through and M_{5a}. The right-hand side has an identical version of the translinear loop, with the two loops connected by cross coupling the two halves at the integrating capacitive node. The differential output current is equal to the following expression:

$$I_{out1} - I_{out2} = \frac{I_b}{nCV_T} \int I_{in1} - I_{in2}\, dt \tag{4.3.3}$$

Where $I_{in1,2}$ and $I_{out1,2}$ are the differential input and output currents respectively, I_b is the biasing current and n is the unitless value typically between 1-2, C is the capacitance value of the capacitor and V_T is the thermal voltage.

The Seevinck integrator's additional advantages include its robustness and frequency tunability. The Seevinck integrator's centre frequency can be tuned by altering the bias current on the left and right branches; as long as these two branches remain equal, the entire system remains balanced. Furthermore, the Seevinck integrator has an interesting characteristic compared to the lossy integrator model, as discussed in Chapter 4: the DC gain of 0 dB can be centered around a centre frequency (f_c). This avoids the previously mentioned issue of high gain or attenuation requirement at low and high frequencies respectively. As a result, the Seevinck integrator reduces the required amplification by around one order of magnitude, such that the gain compensation stage can be feasibly implemented with a log-domain multiplier. The device dimensions and biasing currents used for the Seevinck integrator are shown in Table 3.

Table 3: Table containing the device dimensions and biasing current values for the differential Seevinck integrator.

Differential Seevinck Integrator	
Parameter	**Value**
VDD	1.8 V
W_{PMOS}	300 µm
L_{PMOS}	1.5 µm
W_{NMOS}	60 µm
L_{NMOS}	8 µm
$I_{bias_Seevinck}$	280 nA

4.3.1 Ratiometric MAV

This subsection will describe and discuss the ratiometric MAV (Mean Average Value) topology as shown in Figure 38, which involves computing the signal strength ratio of two signals. This ratiometric signal is a signal that is proportionate to the instantaneous frequency as described in the previous chapter. An MAV block was used to accomplish this operation, which is composed of several substages.

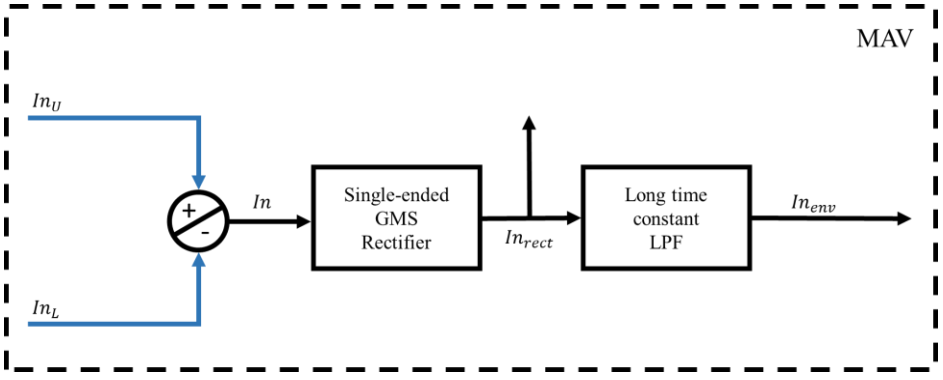


Figure 38: Top level diagram showing the signal flow path of the mean absolute value block. This block has two outputs the rectified signal in and the slow envelope.

The first stage is a rectifying block, which is implemented as shown in Figure 37 using a single-ended GMS splitter that is biased with a very low current (1- 9 nA) to ensure that the biassing current is negligible in comparison to the input signal's amplitude. This low biassing current forces the GMS splitter to operate in its class A mode which reduces the output signal to near zero amps at its lowest points. This is important to reduce the accumulating DC errors in the subsequent blocks.

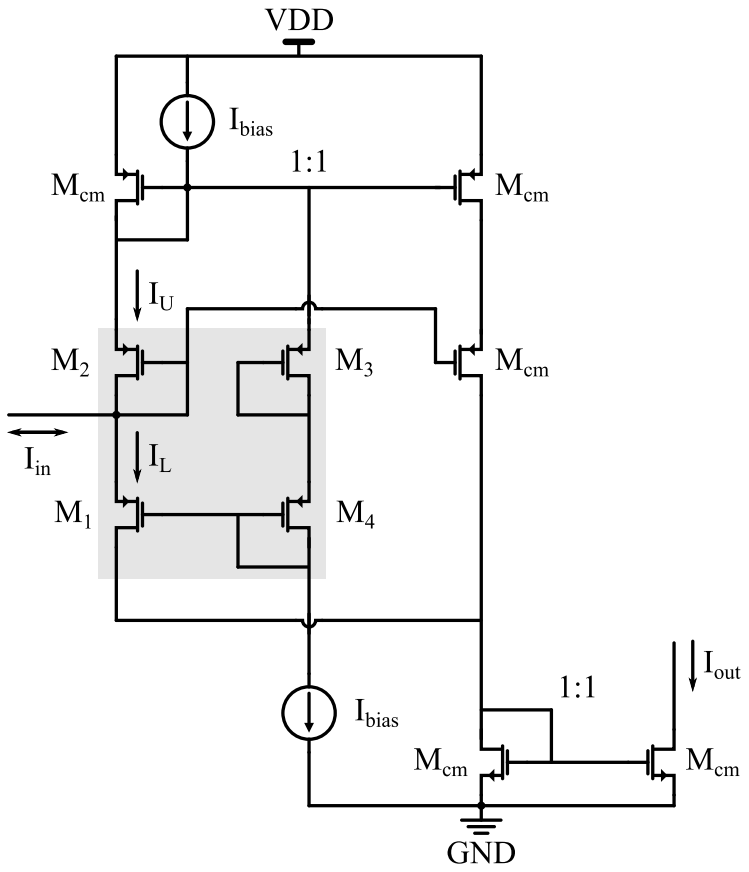


Figure 39: Single sided GMS splitter circuit, M_1 – M_4 form the translinear loop, converting a bi-directional input signal into a rectified output signal where the lowest point is defined by the I_{bias} current. M_{CM} are current mirror transistors sharing the same aspect ratio.

Figure 39 illustrates the circuit diagram of a single ended GMS block used as a rectifier. The transistors M_1 - M_4 form a translinear loop. The input current I_{in} connects to the source of M_1, by connecting the input between M_1 and M_2 the current I_{in} is allowed to fully swing in both directions, to both source and sink current. The circuit is biased at around 1-9 nA via two current sources which are placed at the top and bottom to ensure that the current flowing through M_3 and M_4 is fixed at I_{bias}. The effect of this is that the current flowing through M_2 is

equal to I_{in}^{U} and the current flowing through M_1 is I_{in}^{L}. Since I_{in} is equal to ($I_{in}^{U} - I_{in}^{L}$) which is achieved by mirroring both currents and summing them using a series of current mirrors the final output current is a rectified version of the input current where its lowest point is determined by I_{bias}.

$$I_{in}^{u,l} = \frac{1}{2}\sqrt{4I_{bias}^2 + I_{in}^2} \pm I_{in} \tag{4.3.1.1}$$

By summing I_{in}^{u} and I_{in}^{l}

$$I_{in}^{u} + I_{in}^{l} = \sqrt{4I_{bias}^2 + I_{in}^2} \tag{4.3.1.2}$$

From the above equation it is therefore possible to approximate a rectification operation by ensuring that I_{bias} is much smaller than I_{in}. Summarised in Table 4 is the list of physical device parameters used for the chip layout.

Table 4: Table summarising the physical parameters and bias current value used for the single and the GMS rectifier.

Single-ended GMS rectifier	
Parameter	**Value**
Vdd	1.8 V
W_{PMOS}	300 µm
L_{PMOS}	1.5 µm
W_{NMOS}	60 µm
L_{NMOS}	8 µm
I_{bias}	~7 nA

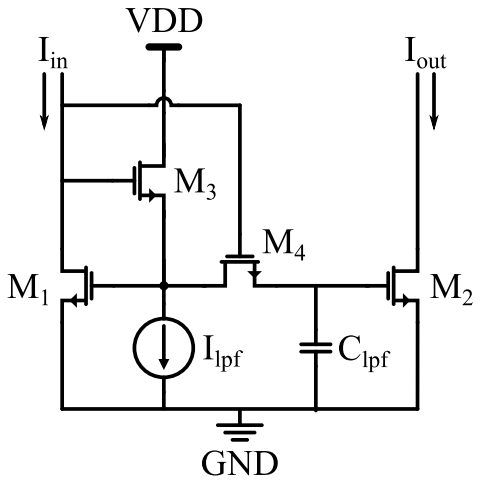


Figure 40: Long time constant LPF circuit. The aspect ratio of M_3 and M_4 is a multiplier to the time constant enabling very long-time constants to be implemented in this small form factor.

The second stage is a long-time constant low-pass filter which is shown in Figure 40, which filters the incoming rectified signal from the previous GMS block output. This generates a quasi-DC signal that is proportional to the input signal's strength. The low-pass filter architecture utilised in this system is a modified Shoemaker topology [161] with a tuneable bias current controlling the time constant following Equation (4.3.1.3) which in turn controls the low-pass filter's cut-off frequency. The devices M3 and M4 operate in strong inversion and the ratio of the M3 and M4 aspect ratio can dramatically increase the time constant by 3 orders of magnitude as opposed to other filter designs [162], [163], whilst still maintaining a small form factor.

$$\tau = C_{lpf} \cdot \frac{2\pi V_T}{I_{lpf} \cdot \frac{W_4/L_4}{W_3/L_3}} \tag{4.3.1.3}$$

The parameters used for the LPF block were matched with the sizes used by Guang.Y (2014) and are shown in Table 5.

Table 5: Physical device parameters and bias current values used for the LPF.

Large τ Lowpass Filter	
Parameter	**Value**
Vdd	1.8 V
$(W/L)_1$	60 µm / 8 µm
$(W/L)_2$	60 µm / 8 µm
$(W/L)_3$	300 µm / 1.5 µm
$(W/L)_4$	8 µm / 40 µm
C_{LPF}	10 pF
I_{LPF}*	~18 nA

* The current value shown is the nominal value.

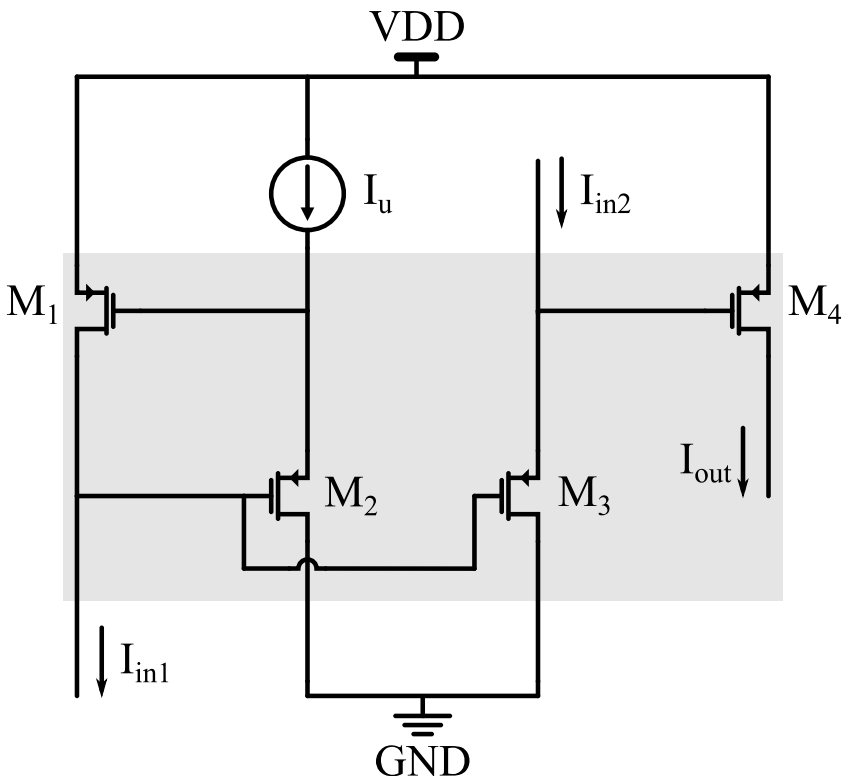


Figure 41: Log-domain multiplier circuit, the pmos devices M_1-M_4 form a translinear loop.

The third stage is a log domain multiplier as shown in Figure 41 which computes the MAV ratio of the output and input signals. M_1-M_4 form a translinear loop yielding the following expression:

$$I_{out} = \frac{I_{in_1}}{I_{in_2}} \cdot I_u \tag{4.3.1.4}$$

The resulting output signal is not only proportional to the instantaneous frequency, but also proportional to the gain required to compensate for the Seevinck integrator's output gain. All the blocks discussed earlier operate in the weak inversion regime, unless stated otherwise.

The log domain multiplier was chosen for its simplicity and low transistor count. However, the biggest limitation of the log domain multiplier, is that it has a very limited gain range, for gain values beyond 10 the block is very error prone. The sizes of the devices used as well as the biasing currents are shown in Table 6.

Table 6: the physical device parameters and biasing current values used for the log domain multiplier.

Log domain multiplier	
Parameter	**Value**
VDD	1.8 V
W_{PMOS}	300 µm
L_{PMOS}	1.5 µm
I_u	1nA

4.3.2 Log-domain Vector Magnitude

The final block in the signal processing pipeline is the vector magnitude operation, the vector magnitude must be computed to generate the analytic envelope. The log-domain vector magnitude block accepts two input signals: the input current and the amplitude-adjusted output signal. To generate the output signal that has been gain-adjusted, the Seevinck integrator output is sent into a log multiplier with the output of the ratiometric MAV signal as the second input.

The log multiplier's output signal is the amplitude adjusted output signal. This operation is necessary to ensure equal amplitudes between the input and output signals.

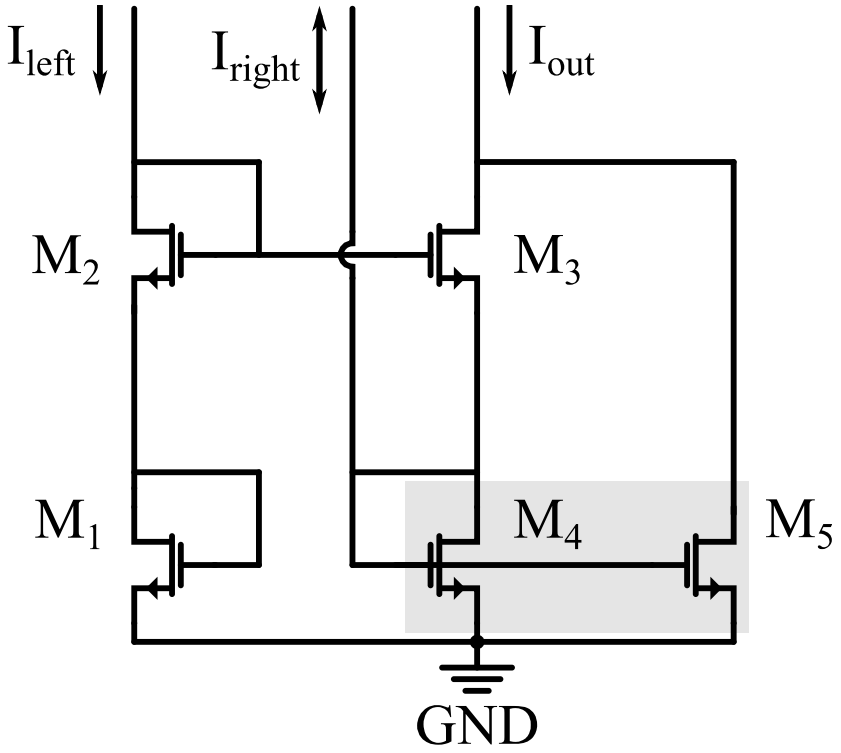


Figure 42: Log domain vector multiplier circuit, (M1,M2,M3,M4) form the first translinear loop and (M1,M2,M3,M5) forms the second translinear loop. The drain current through M3 and M5 sums up to the vector magnitude. The set of equations which describe the operation of the vector magnitude block is shown below.

The vector magnitude block shown in Figure 42 supports bidirectional current in one input but only unidirectional current in the second. However, both inputs are rectified to ensure that both signal paths are treated equally to reduce phase errors. Additionally, unlike the previous GMS splitter which required a DC biassing current, the log-domain vector magnitude block does not require a biassing current, because the input currents provide sufficient bias to the circuit.

$$I_{M1} = I_{M2} = I_{left} \tag{4.3.2.1}$$

$$Setting\ a\ variable\ substitute\ for\ I_{M3}:$$
$$I_{M3} = I_w \tag{4.3.2.2}$$

$$I_{M4} = I_{M5} \tag{4.3.2.3}$$

$$I_{M4} = I_w + I_{right} \tag{4.3.2.4}$$

$$I_{out} = 2I_w + I_{right} \tag{4.3.2.5}$$

Constructing the translinear loop:

$$\frac{I_{M1}}{2} \cdot \frac{I_{M2}}{2} = I_{M3} \cdot I_{M5} \tag{4.3.2.6}$$

$$\frac{I_{left}}{2} \cdot \frac{I_{left}}{2} = I_w \cdot \left(I_w + I_{right}\right) \tag{4.3.2.7}$$

$$\frac{{I_{left}}^2}{4} = I_w I_{right} + {I_w}^2 \tag{4.3.2.8}$$

$$\frac{{I_{left}}^2}{4} = \frac{\left(I_{out} - I_{right}\right)^2}{4} + I_{right}\frac{\left(I_{out} - I_{right}\right)}{2} \tag{4.3.2.9}$$

$${I_{left}}^2 = \left(I_{out} - I_{right}\right)^2 + 2I_{right}\left(I_{out} - I_{right}\right) \tag{4.3.2.10}$$

$${I_{left}}^2 = {I_{out}}^2 - 2I_{out}I_{right} + {I_{right}}^2 + 2I_{out}I_{right} - 2{I_{right}}^2 \tag{4.3.2.11}$$

$$I_{out} = \sqrt{{I_{left}}^2 + {I_{right}}^2} \tag{4.3.2.12}$$

The output current I_{out} is the vector magnitude operation as shown in Equation (4.3.2.12). The parameters used for the vector magnitude block are listed in *Table 7*.

Table 7: The physical device parameters of the log domain vector magnitude block.

Log-domain vector magnitude	
Parameter	**Value**
VDD	1.8 V
$(W/L)_1$	120 µm / 8 µm
$(W/L)_2$	120 µm / 8 µm
$(W/L)_3$	60 µm / 8 µm
$(W/L)_4$	60 µm / 8 µm
$(W/L)_5$	60 µm / 8 µm

Chapter 5

Layout and Chip Results for the Log-domain Implementation of the Hilbert Transform Chip

5.1 Layout

The approach to layout adhered to a set of design rules as well as methodologies to ensure uniformity across the system, subsystems, and individual blocks. Each block was laid out in a rectangular form factor, to ensure easy access to pins from all sides. Transistors were folded and laid out using standard common centroid techniques with an alternating pattern (ABBA) to ensure that devices are properly matched, the resulting effect of this approach means that devices are less prone to physical variations across the chip.

Device spacing was also kept to a minimum, this was achieved by using detached body ties to connect transistors to the n-well. However, in certain instances guard rings were instead used

to establish a stronger bulk connection and electrical shielding. However, this is only possible when all the transistors share a common body connection.

Routing nets and interconnections is another aspect that was optimised to reduce device spacing. Metals 1,2, and 3 were used to form the interconnections shown in Figure 44 and Figure 45. Metals in the same layer were routed in the same orientation to minimise capacitive parasitics. All metal 1 wires were vertical, metal 2 wires were horizontal, and metal 3 wires were vertical. This was done to ensure minimum crosstalk between the metal layers. Moreover, to establish connections between the layers a via connection is necessary. Vias were always placed in multiples of two or more to ensure that the connection persists even if a single via were to fail on device start-up which adds redundancy to the design. A picture of the final fabricated chip is shown in Figure 43.

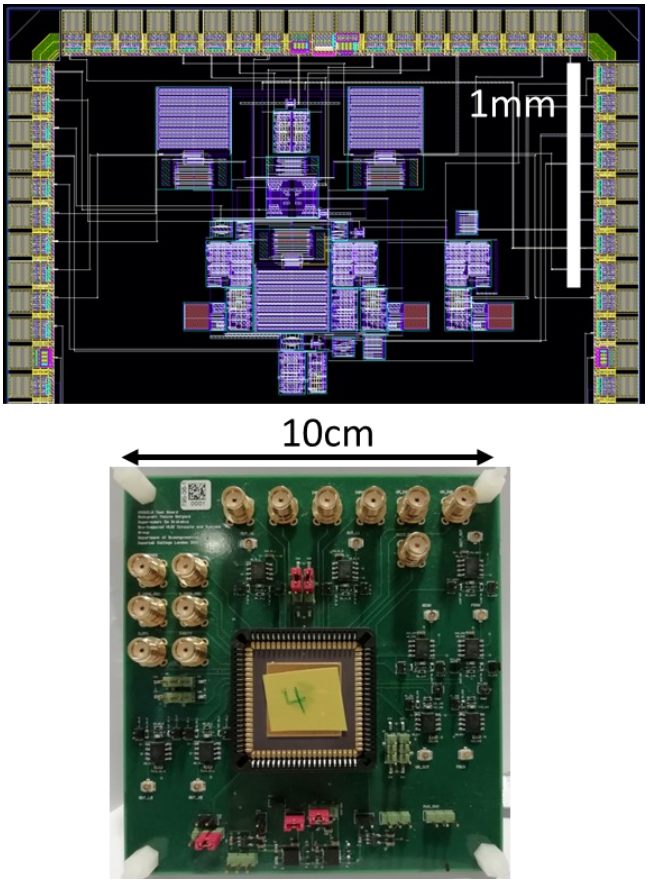


Figure 43: (Top) The layout of the entire design, which includes the whole proposed system and individual blocks to test the Seevinck integrator, the vector magnitude block and the MAV system. (Bottom) The PCB platform designed to test the various systems and subsystems inside

the designed chip. The inputs, outputs, and current biasing are connected via standard SMA connectors.

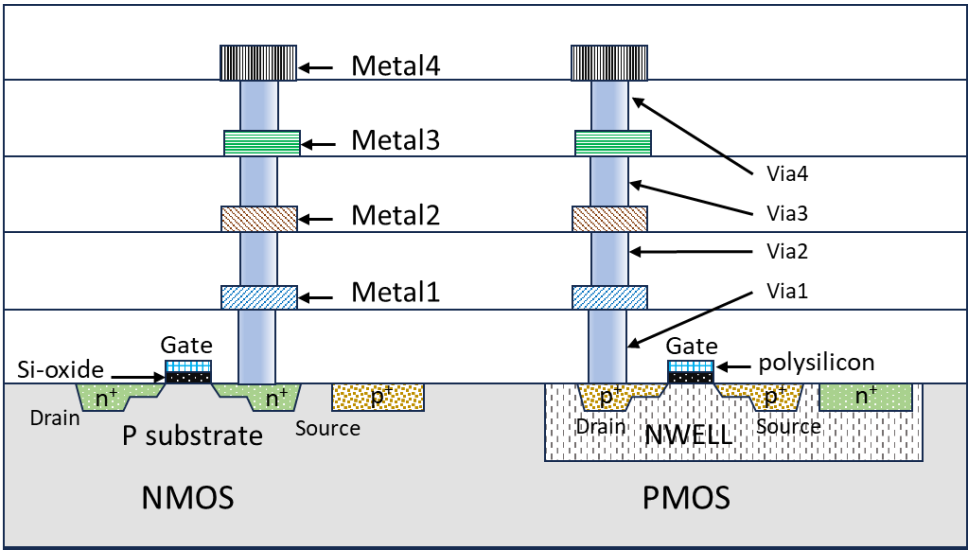


Figure 44: Cross section of the layers in a typical 4 metal 0.35µm AMS process node.

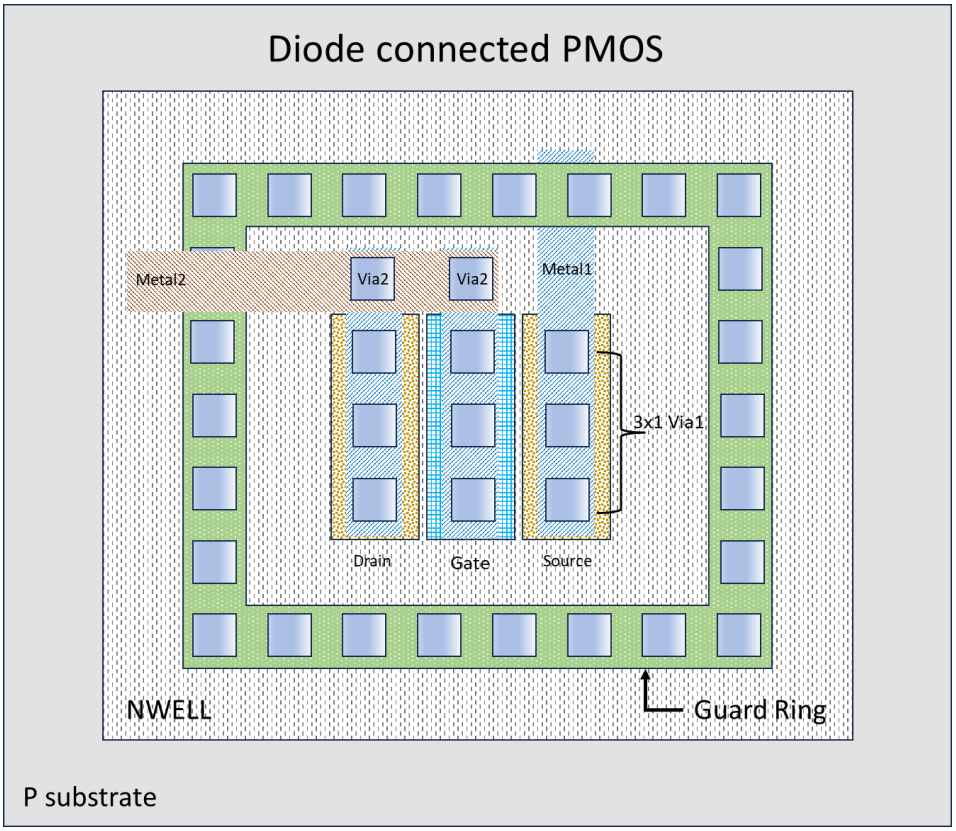


Figure 45: Top view of a diode connected pmos surrounded by a guard ring to establish a bulk connection.

Lastly, since most of the system relies on differential pairs, extra care was taken to ensure that differential current routes are kept as identical as possible to minimise the delay errors between differential current paths. Once the DRC (Design Rule Check) and LVS (Layout Vs Schematic) passed, the chip was sent to a foundry for fabrication using the 0.35 µm AMS technology node.

5.2 Measured Results from the Fabricated Chip

A PCB platform was designed, manufactured, validated, and tested to ensure the functionality of the chip was as expected. The produced PCB is a 4-layer board featuring accessibility to all pinouts of the chip as shown in Figure 46 and Figure 47. The PCB was designed to enable flexibility during testing of the different blocks, systems, and subsystems. This was achieved by having a variable gain stage at the output stages to accommodate for the range of possible input values.

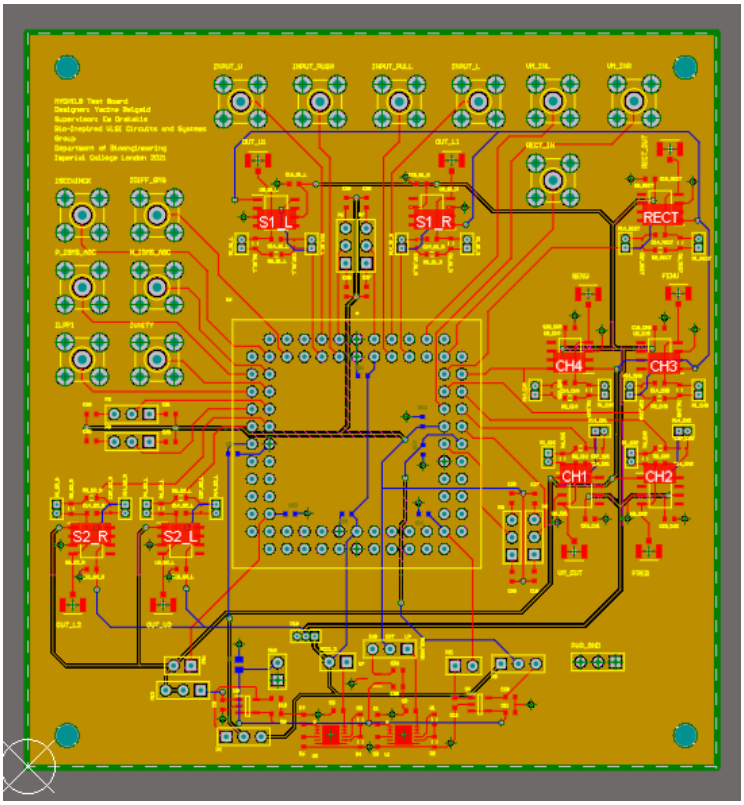


Figure 46: PCB testing platform for the chip.

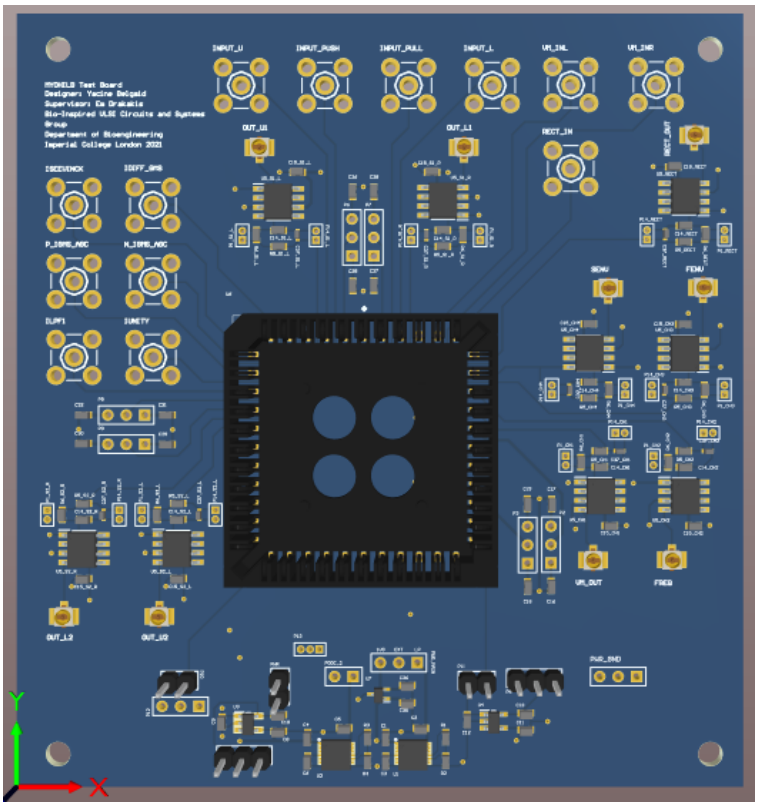


Figure 47: 3D rendered picture of the PCB testing platform for the chip.

Each current output was passed through a transimpedance amplifier that offered two gain settings, which were accessible through a set of 2-pin headers, a gain of 50 M for low currents in the range of single digit nanoamps and a gain of 750 k for larger currents in the range of hundreds of nanoamps.

All voltage sources and references for the transimpedance amplifier were created using low drop out voltage regulators. Each current input to the chip was connected to a Keithley 6221 precision AC/DC current source via an SMA cable. Lastly, outputs from the chip were accessed using a UFL to SMA cable which was then connected to voltage acquisition device (PowerLab). The results were then reviewed and recorded using data visualisation software (LabChart), which is a data logging software. Figure 48 shows the experimental setup for the results presented in this chapter.

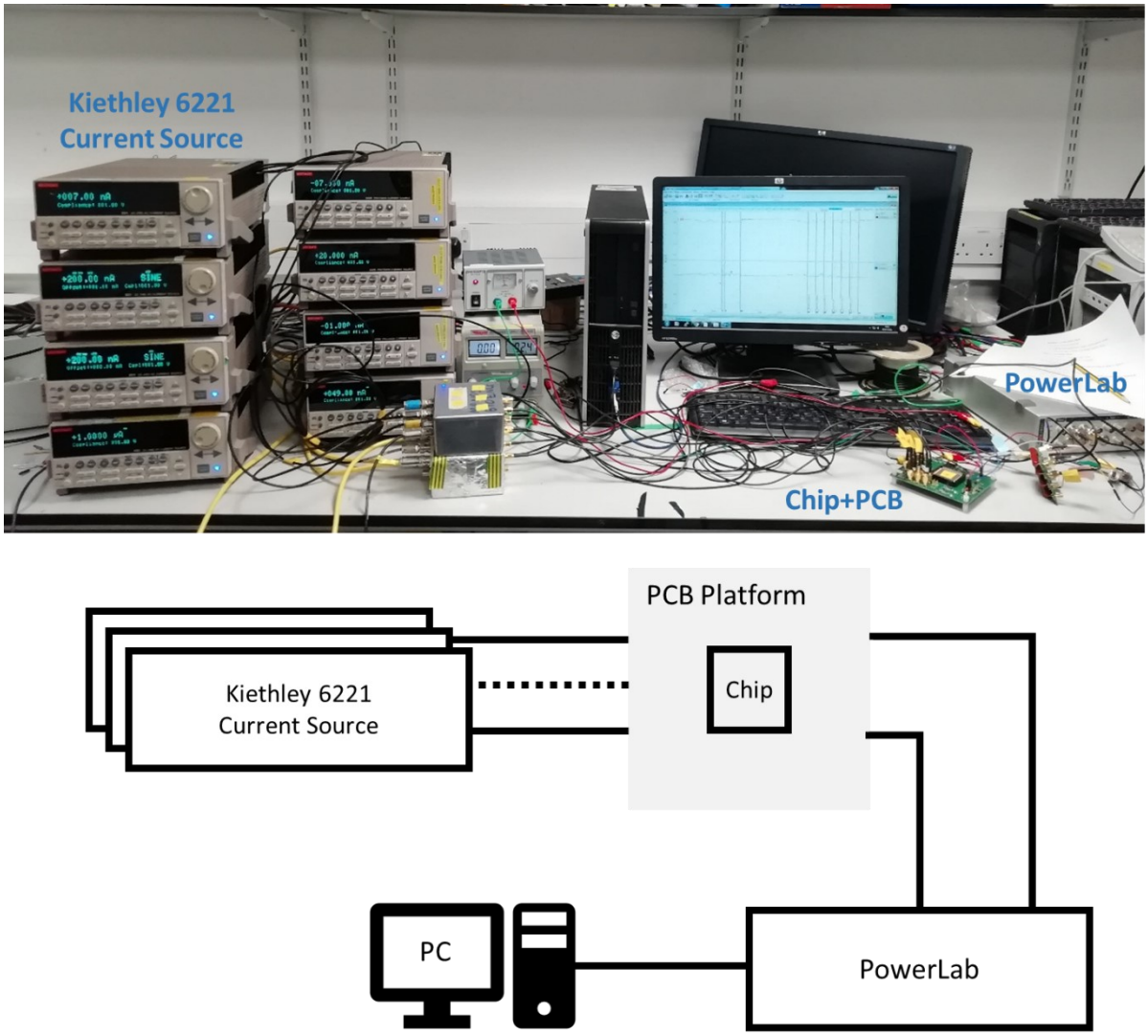


Figure 48: Full Experimental setup for the chip measurements.

All inputs and bias currents in the testing setup were sourced from multiple Keithley 6221 precision AC/DC current sources. This was done to externally control the biasing values and characterise the device. Additionally, the input current sources were connected to a PC using ethernet and GPIB to USB cables. Then custom test scripts were written by using the PyVISA and PyMeasure Python libraries to adjust the Keithley's parameter values automatically.

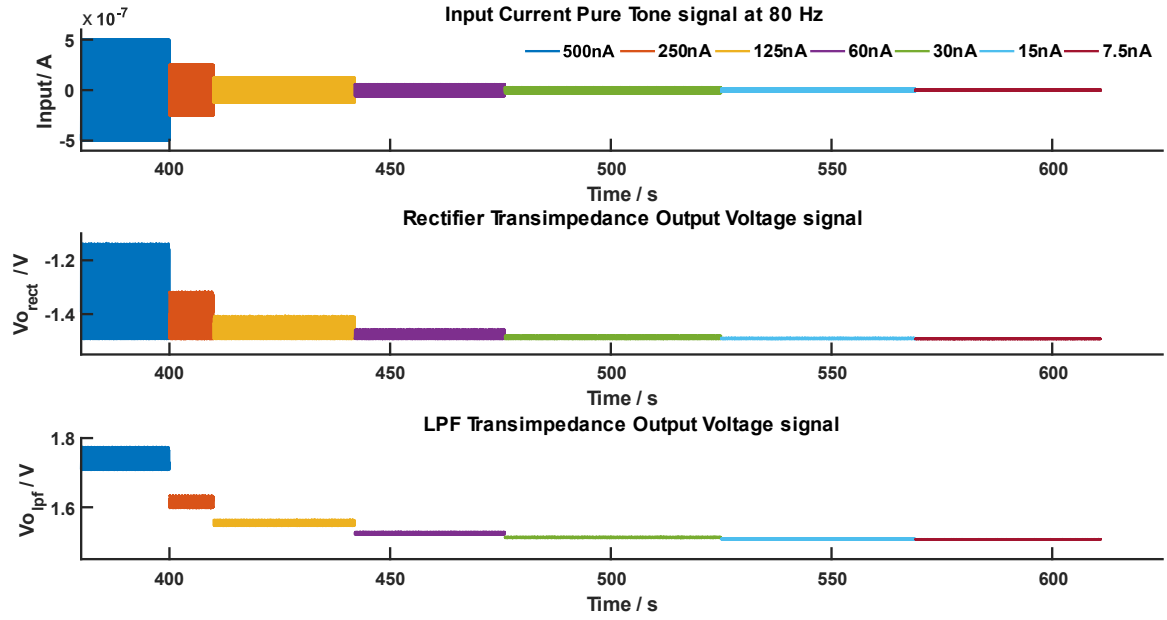


Figure 49: Single ended GMS rectifier and LPF output when an amplitude sweep is run starting from 200 nA and halving the amplitude with every step at a frequency of 80 Hz. The top trace is the input sine wave as a current signal. The middle trace is the output of the single ended GMS based rectifier. The bottom trace is the output of the long-time constant LPF circuit.

Figure 49 shows the results obtained from testing the MAV system, The input was a pure tone fixed at a frequency of 80 Hz and the amplitude was swept in seven stages starting at 500 nA and halving the amplitude with every step, finally ending at 7.5 nA. The trace at the top is the input sine wave as a current signal. The middle trace is the output of the single ended GMS based rectifier, which was converted into a voltage signal using an external transimpedance amplifier. Finally, the bottom trace is the output of the long-time constant LPF circuit whose output is also converted into a voltage signal using an external transimpedance amplifier. The results in Figure 50 shows that the MAV block has a proportional response to amplitude with a R^2 value of 0.9984, which is desired to ensure that the amplitude strength mapping is linear.

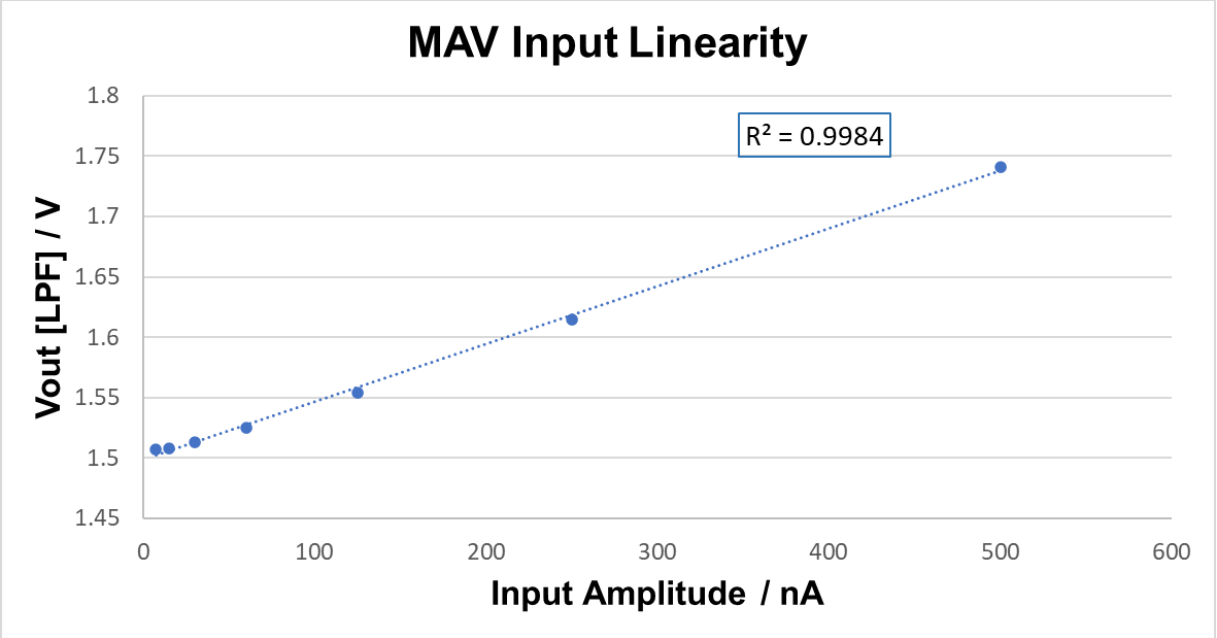


Figure 50: MAV output linearity plot versus a range of input amplitudes ranging from 7.5 nA to 500 nA with a R^2 value of 0.9984.

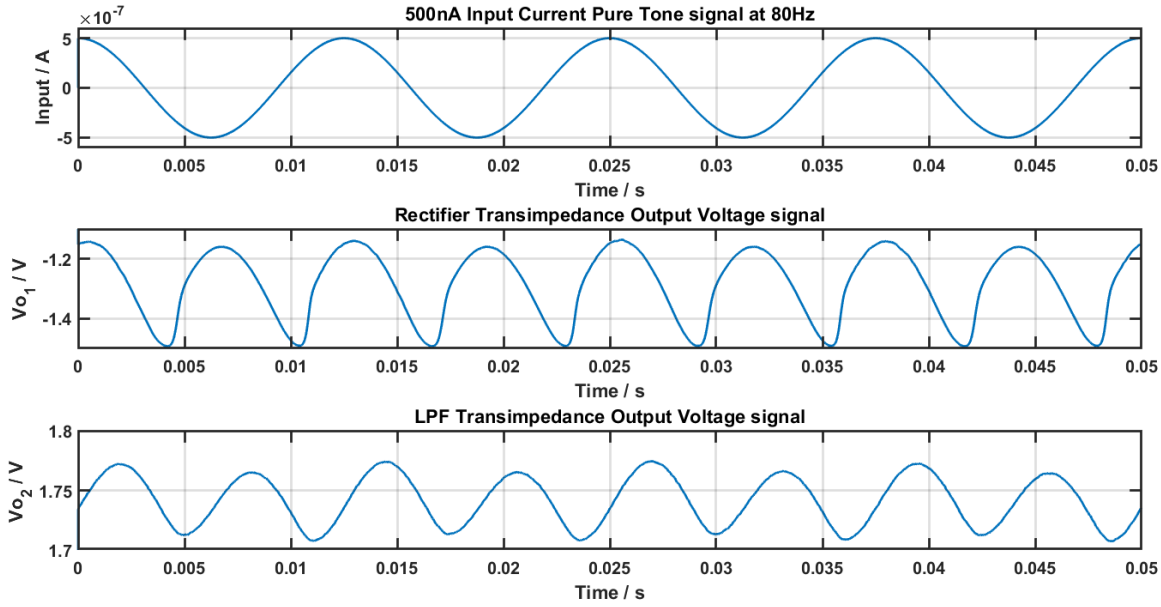


Figure 51: The GMS rectifier output with an amplitude of 500 nA and frequency of 80 Hz. Note that due to rectification the output frequency doubles. Hence, the time difference between two consecutive peaks is half the time of a single period at 80Hz.

Figure 51 depicts the output traces of the MAV block at 500 nA with a frequency of 80 Hz. Note that the output of the rectifier is a wave with double the frequency because of the rectification operation and by extension the output of the LPF is also a signal with double the frequency at 160 Hz.

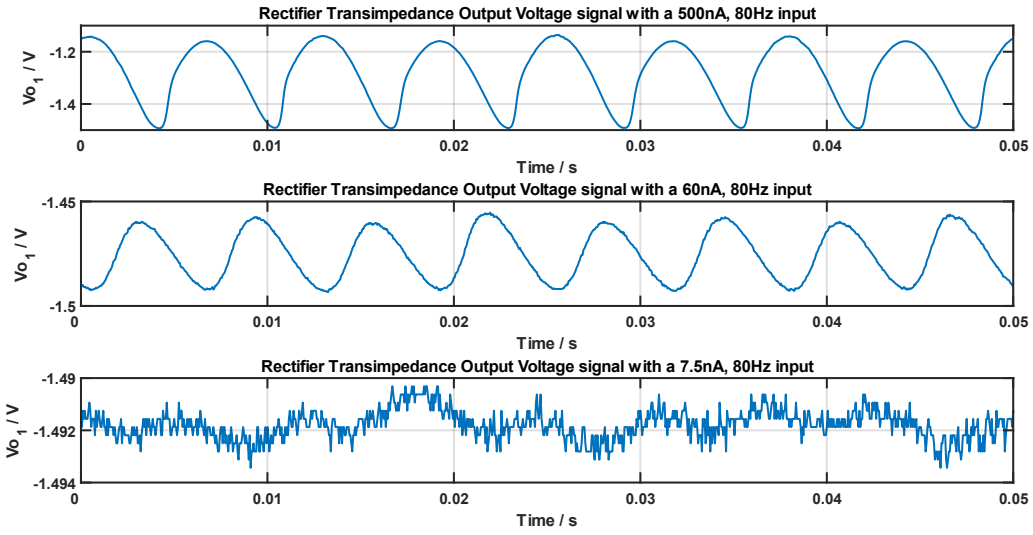


Figure 52: Rectified signal using a single ended GMS at various amplitude strength levels ranging from 7 nA to 200 nA inputs.

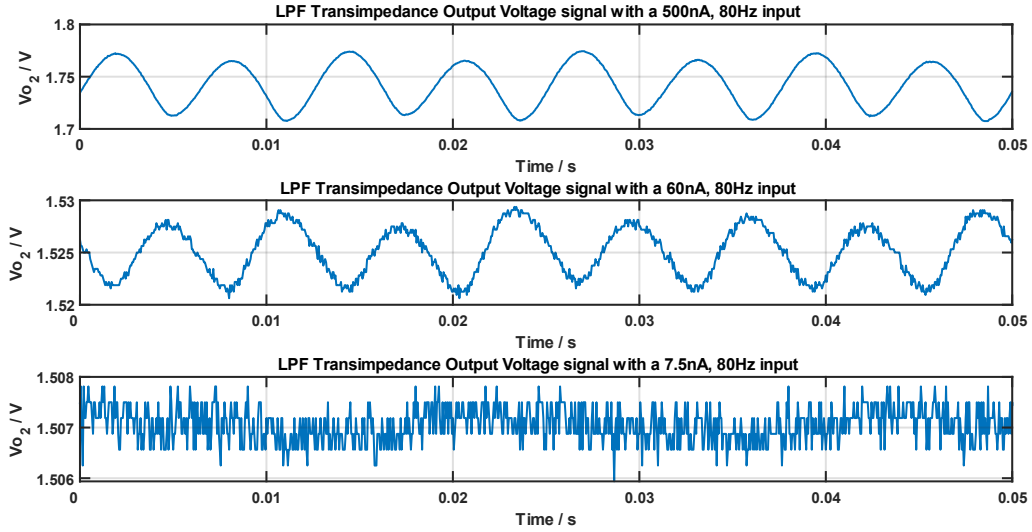


Figure 53: LPF output at several amplitude strength levels ranging from 7 nA to 200 nA inputs.

Figure 52 and Figure 52 show the outputs of the rectifier and low-pass filter at different amplitude levels respectively. In the case of the GMS based rectifier, as the input amplitude decreases the circuit shifts more into class A operation since the GMS is biased at 7 nA. The GMS rectifier serves two purposes, the first of which is to provide a rectified input for the vector magnitude block and the second function is to provide a unidirectional current to the inputs of the LPF block. Rectification for the purpose of the LPF, does not necessitate a perfectly rectified signal. This is because the MAV signal strength output, is a heavily filtered version of the input. However, the signal required for the vector magnitude block is affected by the accuracy of the rectification.

In the case of the LPF, it can be seen that as the input amplitude decreases so does the output of the LPF. The LPF circuit is biased at 20 nA. To ensure that a quasi-DC signal is generated, the purpose of the LPF block is to obtain a signal which represents the input amplitude strength therefore, the quality of the output of the previous block is not as critical compared to the linearity of the ratiometric expression from the MAV block.

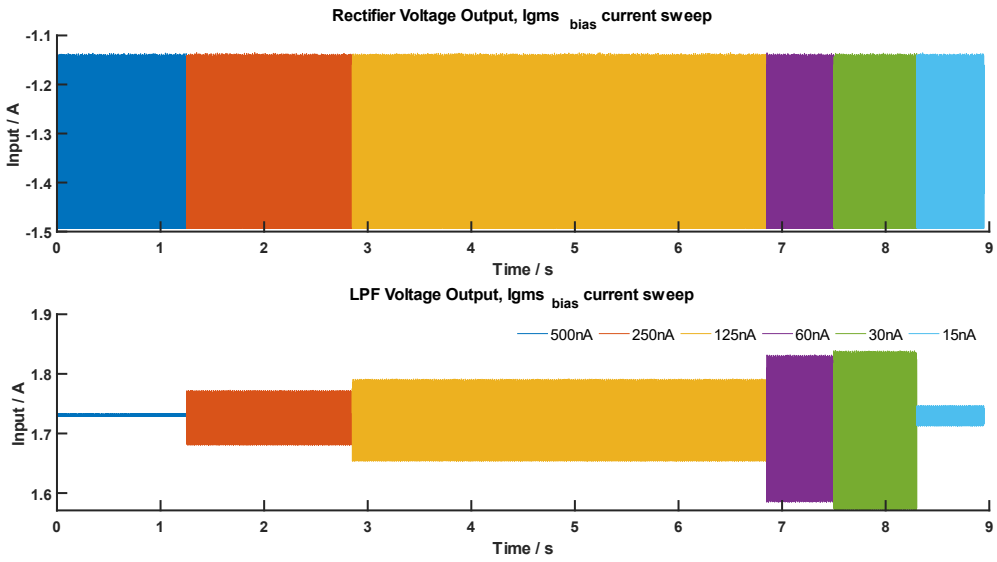


Figure 54: Outputs of the envelope detection stage which is achieved by a signal rectification stage followed by an LPF stage. The envelope output is affected by the LPF time constant which is tuneable using $Igms_{bias}$.

Figure 54 depicts a test case where the input amplitude is kept constant at a value of 200 nA and the value of the biasing current of the LPF block I_{LPF} is varied. The result shows how the time constant of the LPF, and as a result, the cut-off of the LPF is varied or tuned by shifting the value of I_{LPF}. This means that for individual channels the system can be specifically tuned to respond to signals within the bandpass of the channel.

A Python script was written which selects various amplitudes and frequencies for running tests on the chip automatically. After measuring the outputs on LabChart, the results were collected from numerous chips. The rectifier block performs as predicted when the signal is linear with increasing amplitude. That is, for every half decimation of the amplitude, the peak-to-peak signal also halves. It also is worth noting that as the frequency of the rectified signal doubles, the f_0 frequency of the input signal is doubled. The filter block was also evaluated against the rectified signal, and the findings indicate that the cut-off frequency can be altered by adjusting the $Igms_{bias}$ signal.

Note that the LPF's goal is to ensure that the majority of the signal is filtered out and that only the signal's amplitude strength representation is captured. The rectifier and LPF blocks comprise the envelope detection mechanism for slow envelopes. The output signal may be seen here and demonstrates good results. Similarly, due to the inability to generate custom sine

waves because sine waves with 0 DC are not class A signals, instead sine waves were employed as class A signals with a DC of 200 nA. The output of the vector magnitude is thus a sine wave, as the addition of two out of phase DC signals results in an AC signal, not an envelope, as would be predicted initially. The Seevinck integrator results indicate that the integrator block was frequency swept with a class A signal and the differential inputs and outputs were plotted to ensure appropriate operation. The phase was then computed using a MATLAB script that determined the phase delays of two synchronised waves.

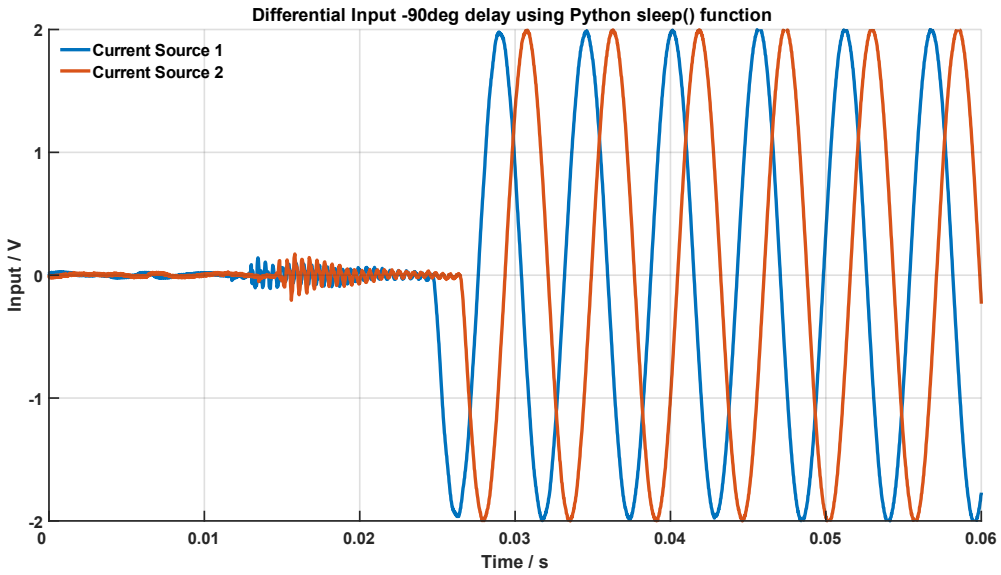


Figure 55: The effect of using the Python sleep() function to achieve a 90 degrees please shift on test start up.

Figure 55 shows the output of a Python script test to validate the time delays between a set of two Keithley 6221 precision AC/DC current sources by using the "sleep()" function in Python. The frequency was set at 180 Hz and the sleep function was set to cause a delay of -90° in the second Keithley current source. The following test was conducted: the first Keithley current source was turned on and then the script was paused to create a 90° delay. The second Keithley current source was turned on once both Keithley current sources were on they were kept on for 100 cycles and then both were turned off at the same time and this was repeated 100 times to verify that the delay between the two waves was indeed 90°. However, it was found that this method produced inconsistent results due to the inherent errors in the sleep() function as well

as the time required to communicate between in the online Python code and the Keithley machines. Another approach used to create the required 90° delay and 180° delay was to use a hardware link connecting a trigger cable between the two machines to set a hardware-based interrupt to generate the required phase delays for testing purposes. This is the method used to create all phase delays in the upcoming results.

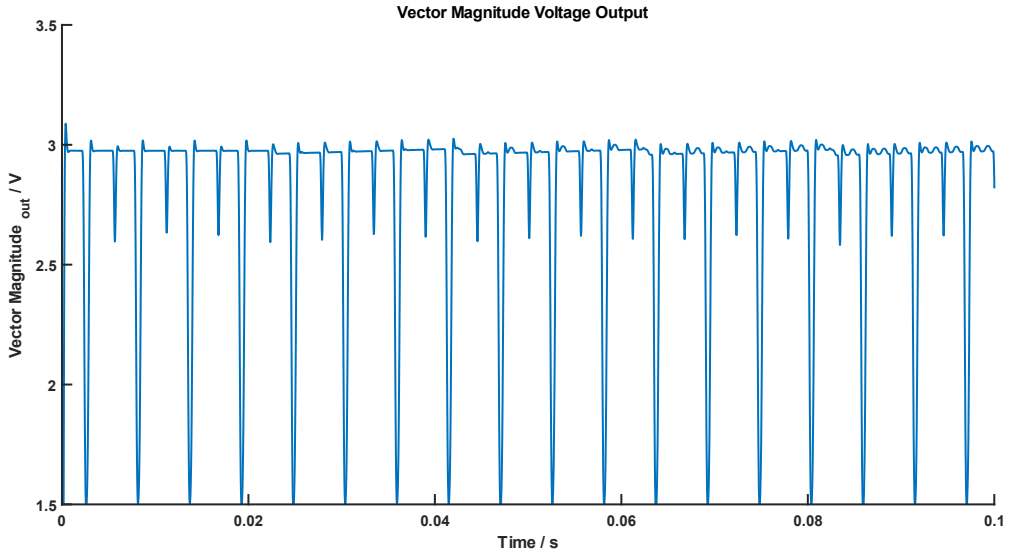


Figure 56: The output of the vector magnitude circuit is used to calculate the envelope of the signal. It should be noted that since one of the inputs is bidirectional while the other is not, the output does not reach zero due to the second input's inability to accept bidirectional currents.

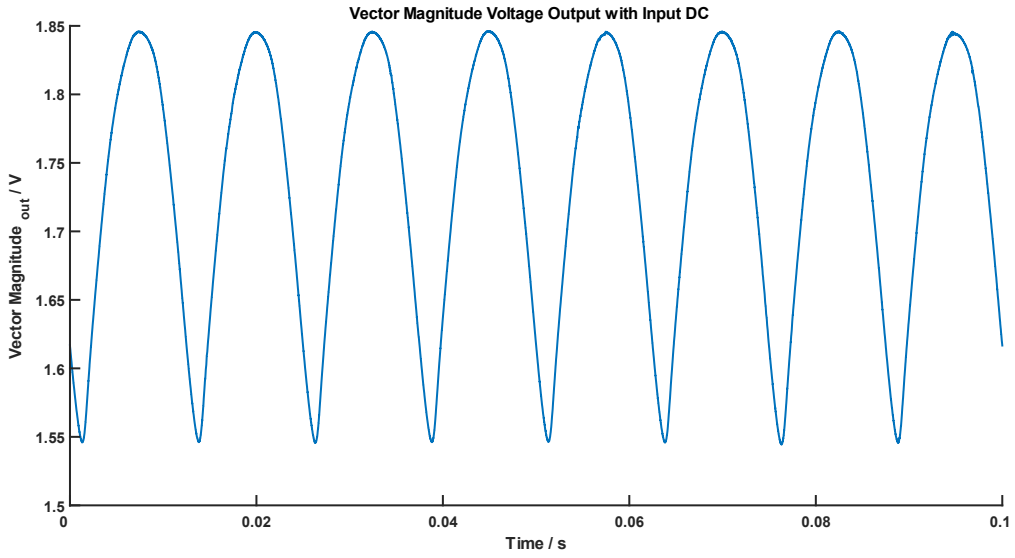


Figure 57: Effect of adding a constant DC to the inputs of the vector magnitude block result in an output which can be compared to the MATLAB simulation. The error is due to the limitation of the pin to accept bi-directional currents.

Figure 56 and Figure 57 show the output of the vector magnitude block. As a reminder, the vector magnitude of a sine and a cosine wave at the same frequency is equal to one in Figure 53, the left and right inputs to the vector magnitude block were set at 200 nA amplitude, at 180 Hz frequency, with 0 DC bias. Due to the limitation of the vector magnitude block to accept bi-directional currents in only one input pin, the generated output signal contains spikes which reach 0 A because no current is flowing in the input when the current flow direction is reversed. Hence, for Figure 54 both currents were now input into the chip with a DC bias equal to 200 nA. The resulting output is now mathematically the square root of the sum of squares of a DC biased sine and cosine wave. The resulting output is a shifted sine wave with the same peak to peak as the input signal. However, the peaks of the wave are broad, and the troughs of the wave are narrow.

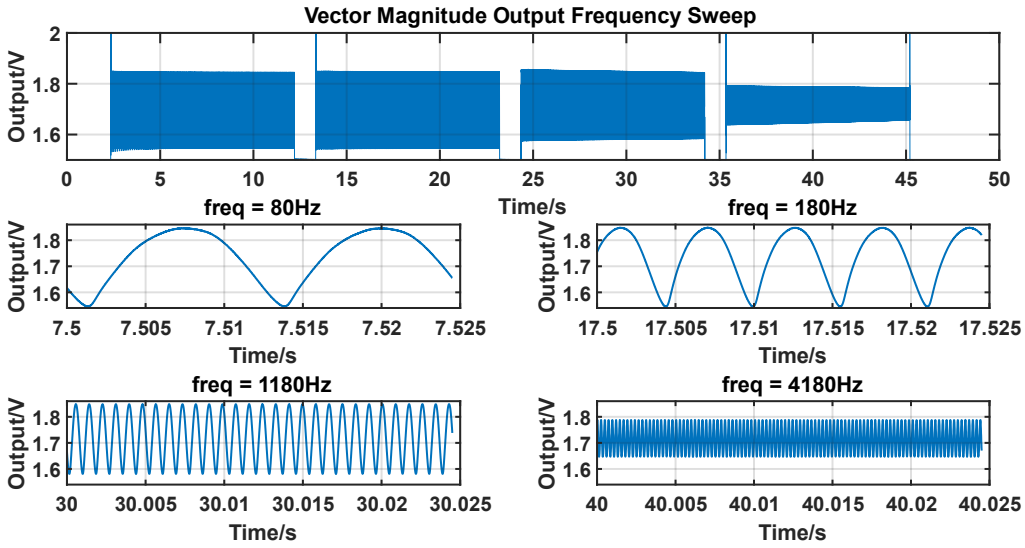


Figure 58: Vector magnitude frequency sweep to show that the output attenuation was due to the parasitic capacitance and not due to the transimpedance amplifier circuit.

In the next test, the frequency response of the vector magnitude block was investigated. Both inputs were set at 200 nA with a DC of 200 nA and a frequency sweep was performed in four steps, starting at 80 Hz and ending 4.2 kHz. The shape of the output shown in Figure 58 matches the expected form shown in *Figure 57*. However, the amplitude of the output drops at higher frequencies. Since the vector magnitude block consists of only five transistors and no capacitors the amplitude of the output should stay constant. However, due to the input capacitance parasitic present in the vector magnitude block, which could potentially explain the drop at high frequencies this phenomenon seems to be present not only in the vector magnitude block but in all the other blocks including the Seevinck integrator the GMS and the entire system.

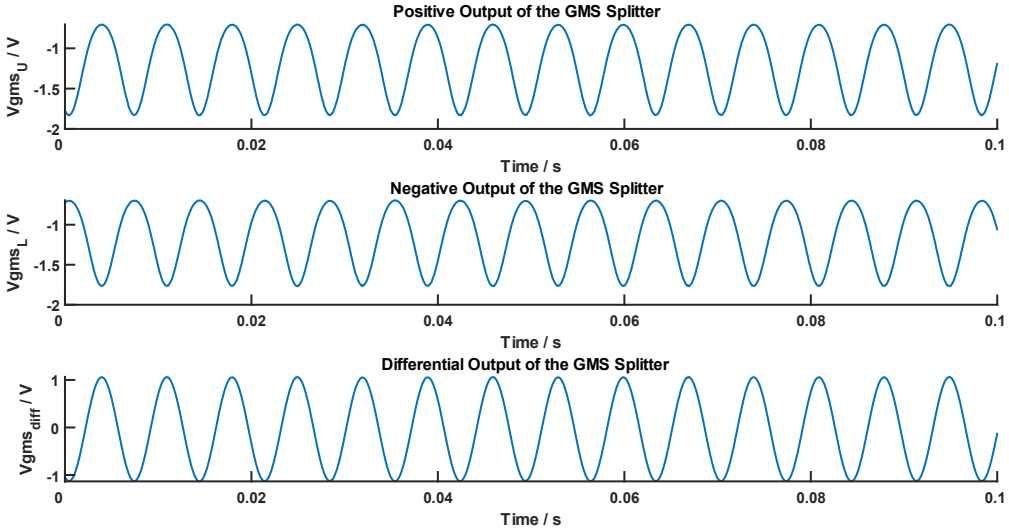


Figure 59: Output of the balanced GMS block in class -A operation.

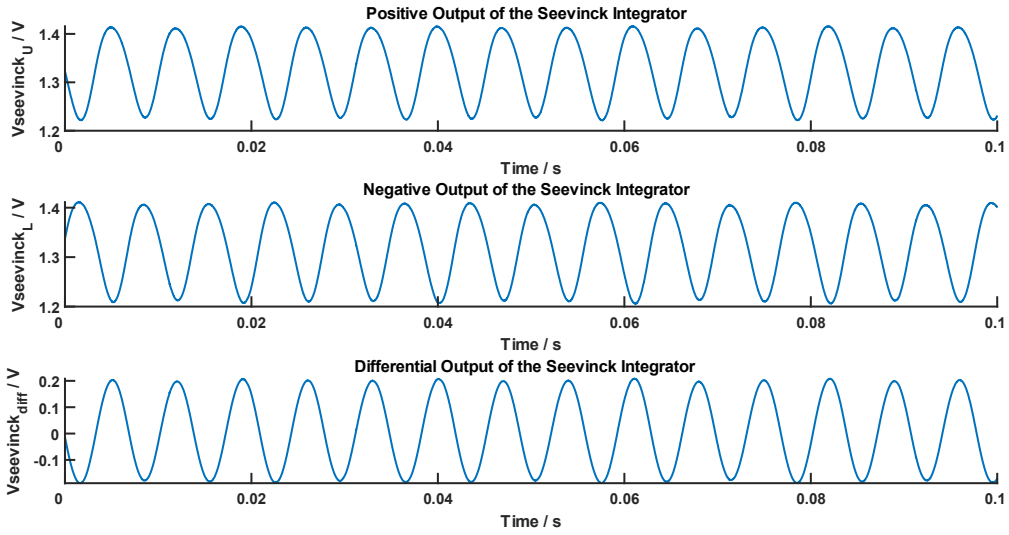


Figure 60: Output off the fully differential Seevinck integrator with a class -A input from the GMS.

Figure 59 and Figure 60 showcase the outputs of the GMS block and Seevinck integrator respectively. In this test the blocks are operating in their Class A mode, the top two traces are the upper and lower outputs respectively, and the third trace is the differential output obtained by subtracting the upper and lower signals. This test was done to ensure that the current differential pathways are consistent to minimise distortion at the outputs.

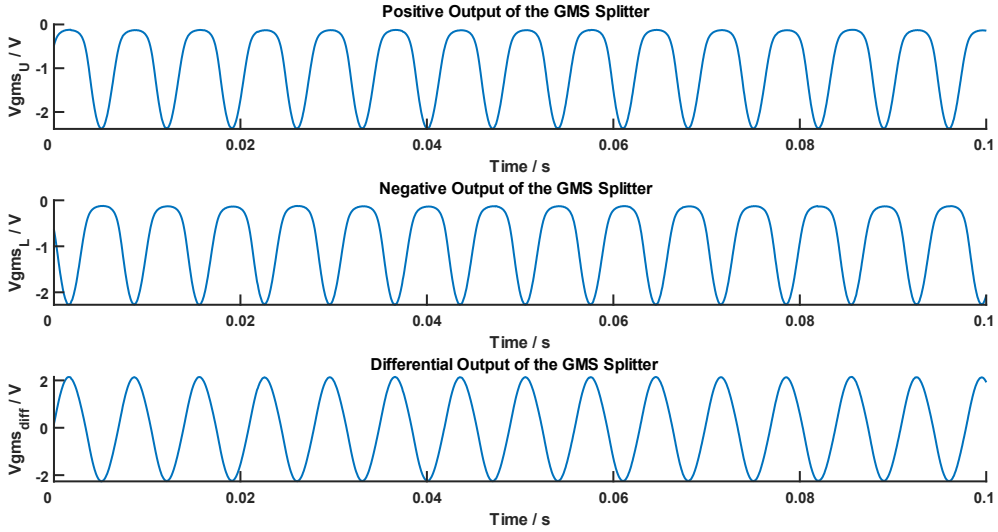


Figure 61: Output of the balanced GMS block in class AB operation.

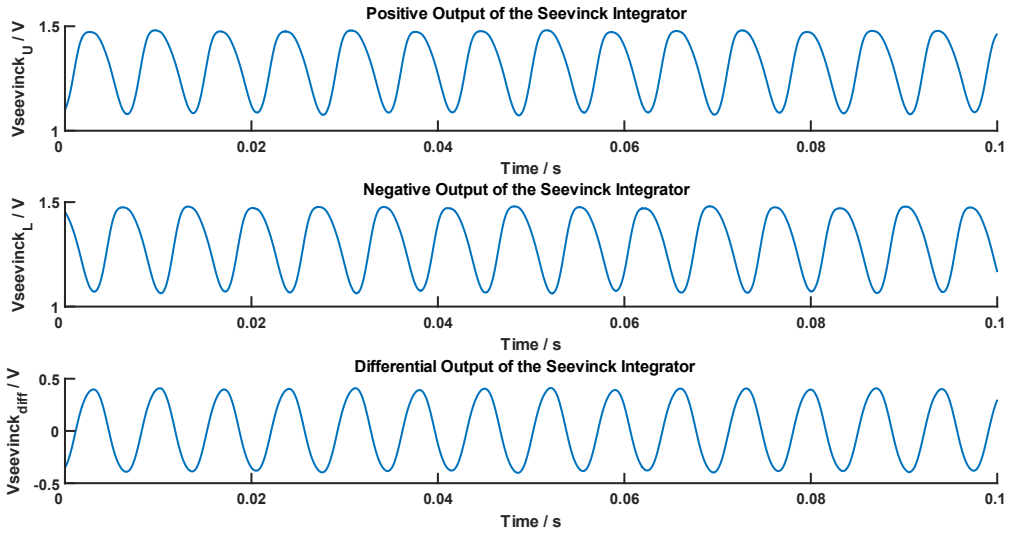


Figure 62: Output off the fully differential Seevinck integrator with a class -AB input from the GMS.

Figure 61 and Figure 62 depict the outputs of the GMS and the Seevinck integrator respectively. In the next test the blocks were biased such that they are operating in Class AB. This is achieved by using an input amplitude of 200 nA and 0 DC bias. Note that although the single outputs (the top two traces) are distorted that is to be expected because of the relationships described in Chapter 4. The signal pathways through the system remain differential until the rectification step before which the current signal difference is used.

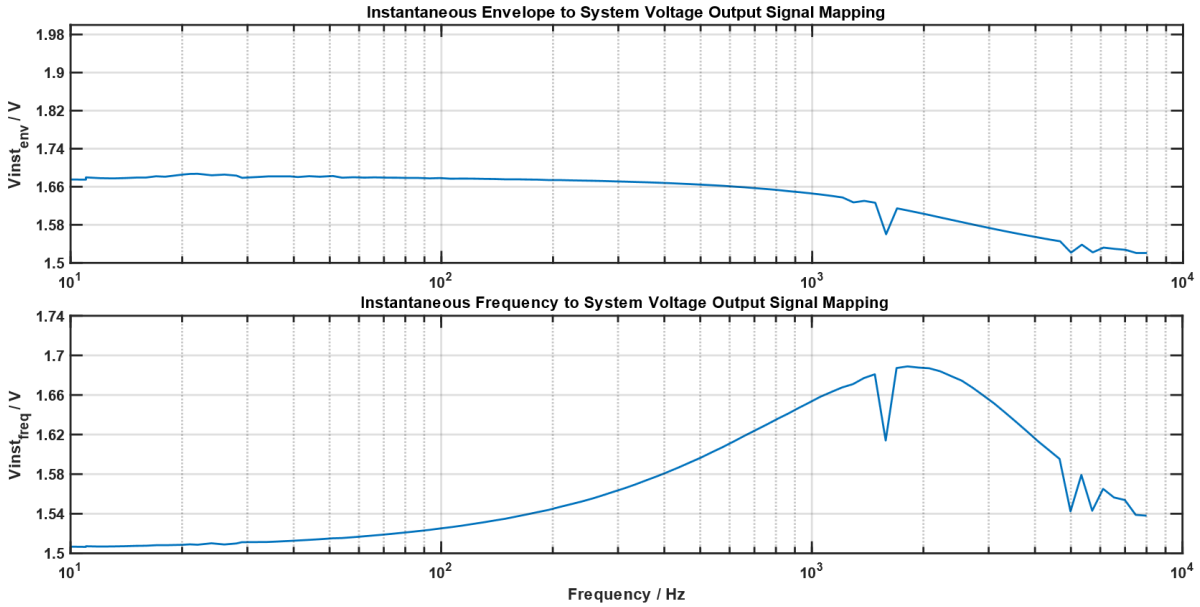


Figure 63: The analytic envelope and instantaneous frequency for a frequency sweep test ranging from 10 Hz to 4 kHz. Note that after around 1.5 kHz frequency the signal starts decreasing and this is due to the parasitic capacitance present at the input node which can be seen in the vector magnitude output decay.

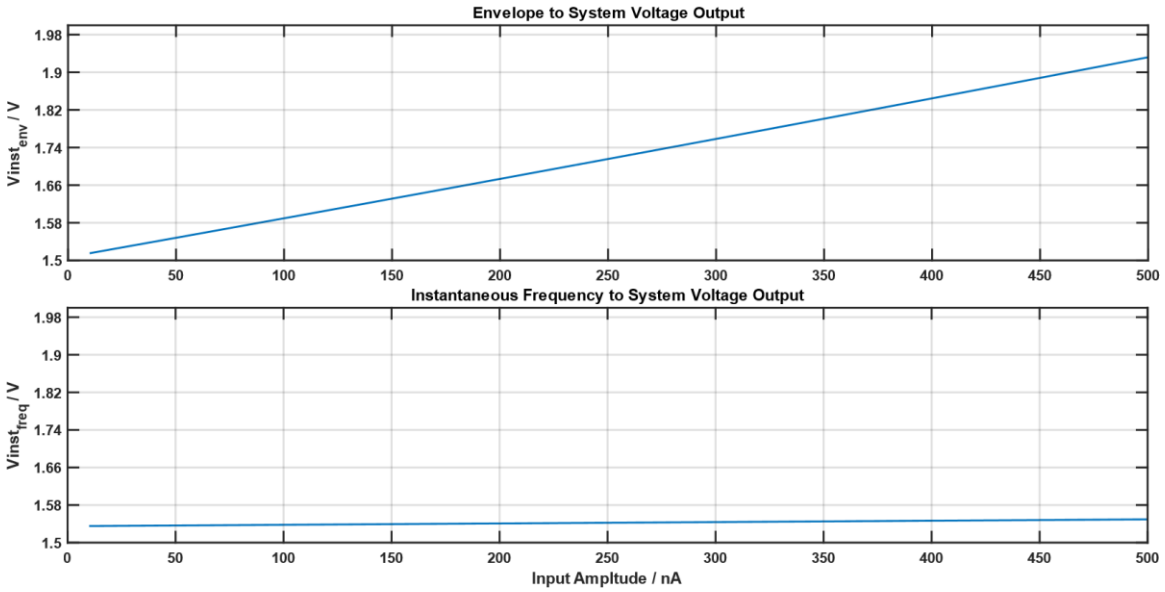


Figure 64: The outputs of the analytic envelope and instantaneous frequency. In this test, an amplitude is set as an input at a fixed frequency of 1 kHz. The top trace shows the analytic envelope signal, and the bottom trace shows the instantaneous frequency measurement.

Figure 63 and Figure 64 depict the output results of the entire system when tested. In Figure 63 the input amplitude was kept constant at 200 nA with no 0 DC. The two Keithley current sources were set at 180° phase apart to source and sink an input current into the chip. The frequency, was then logarithmically swept from 10 Hz up to 4 kHz by using a custom Python script. This was carried over several steps. For the input amplitude, the 750 k gain setting was used and for the instantaneous frequency signal the 50 M gain setting was used. This was because the instantaneous frequency signal is in the single digit nA range. The resulting output in the case of the envelope starts off at a quasi-constant value. However, at around 1 kHz the amplitude begins to drop off. The most significant contributor for this observed effect would be the vector magnitude block, which was shown to have a similar drop off also at higher frequencies. In the case of the instantaneous frequency signal increases logarithmically up to a certain point, such as 1.5 kHz. However, it also begins to drop off. This is caused by the log domain blocks, which have deviations from the expected gain at values beyond 10.

In the second test for Figure 64, the frequency was kept constant, and the amplitude was instead swept logarithmically starting at 7 nA and ending at 500 nA. In 100 steps, the output of the envelope does increase logarithmically with input amplitude. However, in the instantaneous frequency signal, it can be seen that it does increase slightly, whereas the expected outcome should have been a flat signal. This could be explained in terms of errors caused by a combination of the vector magnitude block in combination with the log domain multiplier. However, this was a test that spans the entirety of a cochlear implant frequency range, whereas in reality the system would have a limited frequency scope and would be tuned to each channel individually to obtain the optimum result within that frequency channel. In contrast, this test was conducted without changing or optimising the current bias and current values as the frequency increased. This is to show the relatively wide bandwidth operation of this method in contrast to other approaches, which were described in the previous chapter.

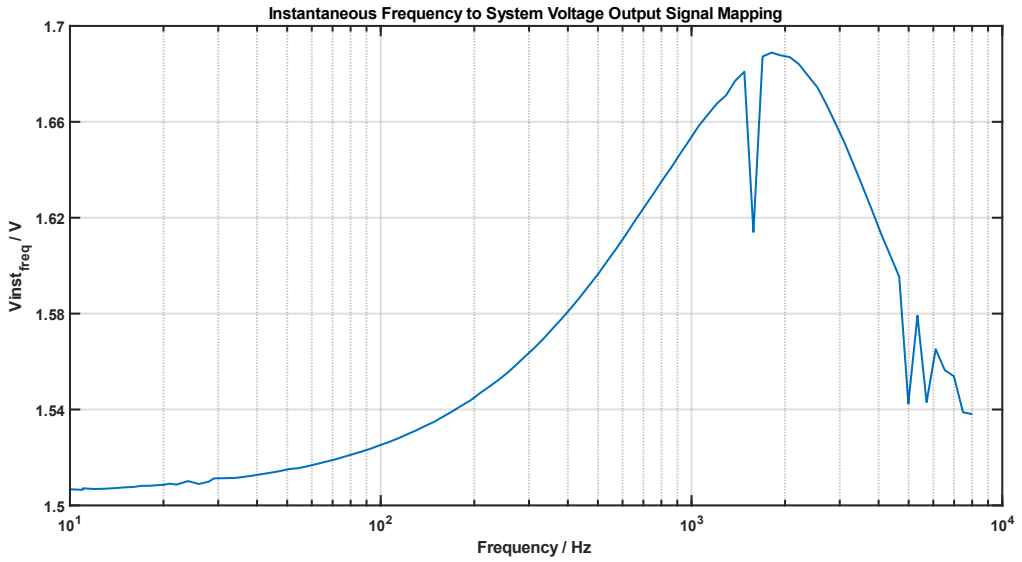


Figure 65: Frequency response output for the instantaneous frequency.

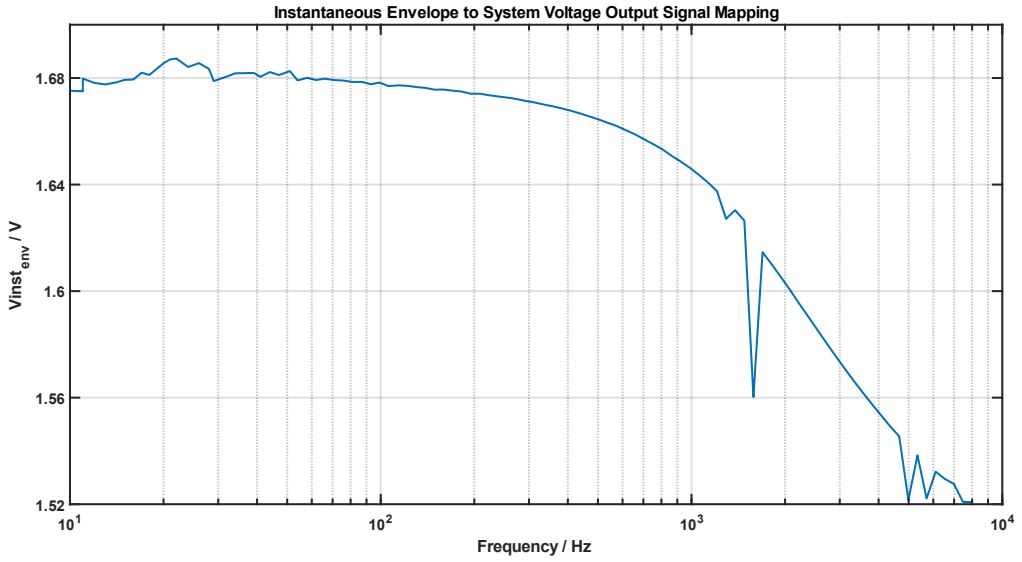


Figure 66: Frequency response output for the analytic envelope.

Figure 65 and Figure 66 are the frequency response outputs of the instantaneous frequency and envelope respectively over a functional operating range in frequency ranges from 100 Hz to 4 kHz. There is a sharp dip at around 1.5 kHz which is due to an internal destructive interference causing the sharp decrease in the signal strength.

Table 8: Power consumption for each block in the system

System Power Consumption Breakdown		
Block	**Power / µW**	**% of the System**
Seevinck Integrator	3.8	56.7
Single-ended GMS	0.7	10.4
LPF	0.6	9.0
Log-Multiplier	0.4	6.0
Vector Magnitude	1.2	17.9

Table 8 summarises the power consumption for each block in the system. As expected, most of the power is consumed by the integrator block which is responsible for creating the -90° phase shift, followed by the vector magnitude block which performs a squaring operation. Further improvements on the blocks need to be made before any consideration for implantability can be made.

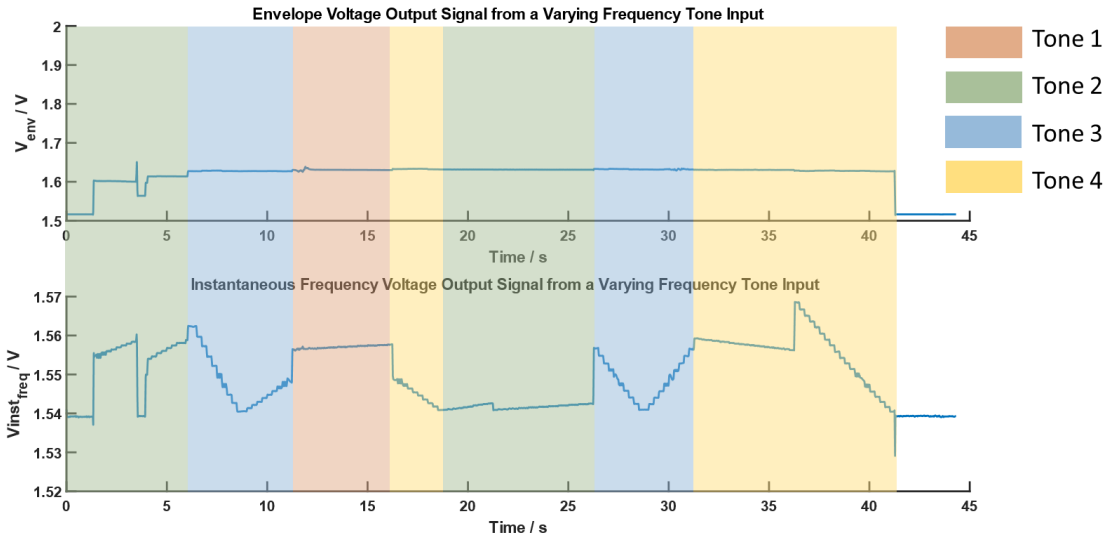


Figure 67: System output of the analytic envelope and instantaneous frequency. In this test a collection of characteristic tones present in tonal speech was used as input to show the tracking capability of the instantaneous frequency estimation. The input amplitude of these tones was kept at a constant value.

Figure 67 showcases a test whereby the input amplitude was kept constant at 200 nA and a consecutive series of frequency tones were used as inputs into the system. This was done to observe the tracking capability of the system for tonal-based languages, which utilises the 4-tone system. The shape of the tones was based on [40]. However, due to the limitation of the Keithley sources for generating custom waveforms, which prevented the possibility of the frequency to change at a very high rate, the synthesized tones had to be elongated to 45 seconds as shown in Figure 65 to ensure that there is no ambiguity in the frequency value from the Keithley. The results overall show consistency with the instantaneous frequency changes and the errors in the signals are due to primarily cumulative errors in each of the blocks. One potential way to reduce these errors would be to reduce the number of blocks which serve multiple purposes, such as allowing the vector magnitude to operate for unidirectional currents. If the rectification block could be eliminated or a new vector magnitude block designed which accepts differential currents, then such an approach could potentially minimise the accumulation of errors and its outputs.

Chapter 6

Transistor Level Design of an Efficient Log-domain N-of-M Selector Block

6.1 The Multimode Strategy

Research in stimulation strategies has been ongoing since the conception of the cochlear implant. Over the past few decades, and even more so recently, there has been a growing interest in finding efficient methods of incorporating temporal fine structure and instantaneous frequency, in addition to envelope information during stimulation [164], [165].

Fine structure and instantaneous frequency have been shown to play an important role in speech intelligibility, especially in noisy environments, as was demonstrated with the audio chimera experiments by [37] supporting the earlier findings by [166]. As a result, most modern cochlear implants employ some form of frequency-based stimulation in addition to place coding strategies. The most successful of which are the N-of-M type strategies [167], these types of

strategies provide multi-rate stimulation by varying the number of selected channels per stimulation cycle. However, due to the global trends of miniaturising implantable electronics [151] especially in wearables, implementing such strategies in hardware provides an additional engineering challenge in order to maintain a similar level of flexibility to software based solutions.

Hence, with the end goal of realising a fully implantable cochlear implant, there is a need to develop optimised hardware to realise such strategies. This also contributes to reducing the overall footprint as well as the cost since it is designed as a complete integrated system. Typically, the N-of-M strategy is realised through a digital processor, by programming in the stimulation protocol alongside the patient specific values. The algorithm for implementing the N-of-M is also done programmatically by selecting the largest N channels from a total of M channels with every new stimulation cycle.

Currently, there exists no practical method of a fully hardware-based solution, which implements the N-of-M type strategies that can also provide enough flexibility with regards to selecting a variable number of channels, robustness as well as efficiency. This limitation makes competing with existing software-based solutions impractical.

There exists a class of analogue circuits known as the Winner Takes All (WTA). These classes of circuits are used in modelling neurons and building custom neural networks for machine learning applications [168]. Presented in this chapter, is a modified hierarchical WTA architecture which implements the N-of-M selection block for 16 channels with O(n) order circuit complexity, where n is the number of input channels. The proposed design possesses the ability to implement both the basic form of the CIS (when N == M) or the 'N-of-M like' strategies (when N < M), the implementation also has the additional capability of either selecting the N largest or N smallest channels, as well as the ability to change N dynamically between stimulation cycles by changing a single biasing current as well as sorting channels based on amplitude without using memory.

The criteria for choosing N can also be based on individual channel's amplitude strength or based on percentage energy spectral contribution of the incoming signal, these design criteria constitute the two major types of N-of-M implementations [169]. The utility of the proposed architecture is not only bound to cochlear implant applications, it can also be used in analogue-based neural net circuits where the selection of weights is to be carried out efficiently [170], [171]. Attention has been paid to make sure that the proposed architecture is general and

flexible enough. This would help ensure that any further improvements and developments can conceivably occur on the same platform.

In this chapter a novel, fully hardware implementation of the N-of-M selection block is proposed. Based on a modified hierarchical WTA architecture. the simulation outputs obtained show promising results using this approach, allowing for increased flexibility and with O(n) circuit scalability.

6.1.1 Fixed Rate Stimulation

As mentioned in Chapter 2, stimulation was first delivered as a continuous time signal [72]. In other words, channels were stimulated over time with a continuously varying current signal. However, it has been found that such an approach to stimulation results in increased levels of cross talk.

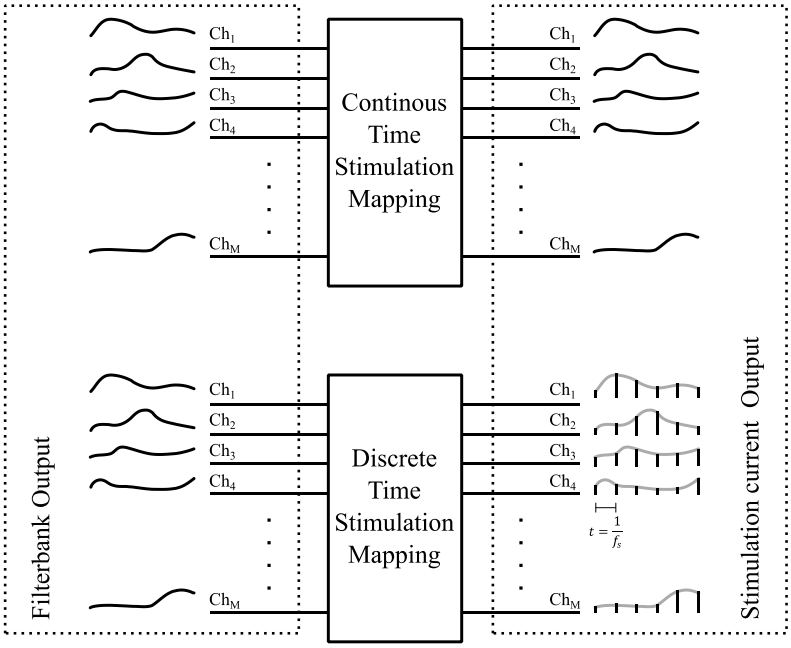


Figure 68: Diagram depicting the output signal differences between continuous and discrete time stimulation. Discrete time stimulation delivers stimulation at regular timed intervals which is called the stimulation rate.

An alternative approach to continuous time stimulation is to stimulate channels in discrete time such as the diagram in Figure 68, each channel would have a specific window in which stimulation would take place and outside this window no stimulation would occur [172]. The amplitude of the stimulation would be the result of a compression mapping to the amplitude corresponding to the relevant channel.

Hence, stimulation rate in the context of cochlear implants corresponds to the rate at which stimulation occurs for a specific channel, that is how many times a channel is stimulated per unit of time which is usually measured as a pulses per second (pps). Stimulation rate is important because it has been shown that a higher stimulation rate provides more information than a lower stimulation rate. However, beyond a 1000-3000 pps rate of stimulation the user experiences diminishing returns in speech comprehension in both quiet and noisy environments [169], [173].

Stimulation rate is therefore critical because determining a particular stimulation rate for a particular strategy, for a specific patient, means that information delivery to the cochlea can be maximised, whilst minimising the negative outcomes.

Stimulation rate has been typically implemented in a method similar to multiplexing that is to say stimulations occur all at once or by employing a method called interleaved sampling. It was quickly observed that by stimulating all channels at once and increasing the number of channels beyond a certain limit introduced very little information and users were shown to not have increased intelligibility to speech even when higher stimulation rates were used [74]. Therefore, this introduces the concept of a stimulation rate upper limit. This upper limit depends on the particular frequency channel, which in essence is the section of the basilar membrane that is being stimulated and is also dependant on the individual**.**

The concept of a stimulation rate upper limit introduces a bottle neck in cochlear stimulation strategy research which is mitigated with interleaved stimulation and variable rate stimulation. However, a stimulation rate upper limit still existed with interleaved sampling due to it being a limitation of biology when interfacing with high-speed electronic systems, which can be understood as a form of information density bandwidth.

There are various examples of strategies which use fixed rate stimulation, the most common of which includes the CIS, which is the continuous interleaved sampling at around 800 pulses per second. There are variants of the CIS including high-rate CIS also called HiRes [174], a strategy which uses a higher stimulation rate between 3000 to 5000 pulses per second for this strategy. However, fixed rate stimulation is rarely used nowadays because it is widely accepted that fine structure in speech must be encoded during stimulation to increase its performance, which means that the rate at which an electrode is stimulated also provides information as opposed to the previous understanding in which it was thought that only the amplitude of the stimulation is sufficient during stimulation.

6.1.2 Variable Rate Stimulation

As discussed in the previous section, fixed rate stimulation is limited in the amount of information it can convey. This can be visualised as a map in which one axis of delivering information is via the amplitude of stimulation, with an additional axis of information delivery being performed in the time domain which encompasses the rate at which an individual electrode is stimulated.

Variable rate stimulation aims to achieve greater information density delivery to the cochlea by varying the rate of stimulation per electrode. There are two approaches to this, in the first approach, stimulation can be delivered all together at once. For example, in a system with eight electrodes, all electrodes would have the same stimulation rate per cycle but the stimulation rate across cycles can vary. Another variant of variable rate stimulation is to vary each and every electrode individually. In this case the rate of stimulation per cycle across electrodes is no longer the same but different, this helps to deliver richer information to electrodes. This is because it has been shown that a low stimulation rate or changes in stimulation rate contribute to convey more information to slower or lower frequencies. whereas it is not as effective for high frequency channels [175]. Although it still beneficial to provide variable rate stimulation to high frequency channels.

Variable stimulation rates add additional benefits by determining how an electrode is stimulated it is possible to control the type of information that is being conveyed. For instance, in environments where the signal to noise ratio is very high, such as in the case of a clean

signal, one can still use a fixed stimulation rate strategy which couples all electrodes together. However, in an environment which is more common such as music, noisy environments or tonal speech introducing variable rate stimulation can help enrich the sounds the listener experiences [176]–[178].

By switching dynamically between different types of stimulation rates it is possible to optimise the platform the patient is using as well as help with power saving costs of the system. Some of the examples of the strategies which use variable rates of stimulation include but are not limited to ACE,SPEAK, and 'N-of-M like' strategies [179]. In particular, the N-of-M strategy will be discussed in detail in a later sub-section.

6.2 N-of-M Stimulation Strategy

In this section, the N-of-M strategy will be explained and discussed. In addition, the reason for opting for such a strategy will be described, exploring the basis for why it is the most efficient when it comes to building a complete system on chip cochlear implant.

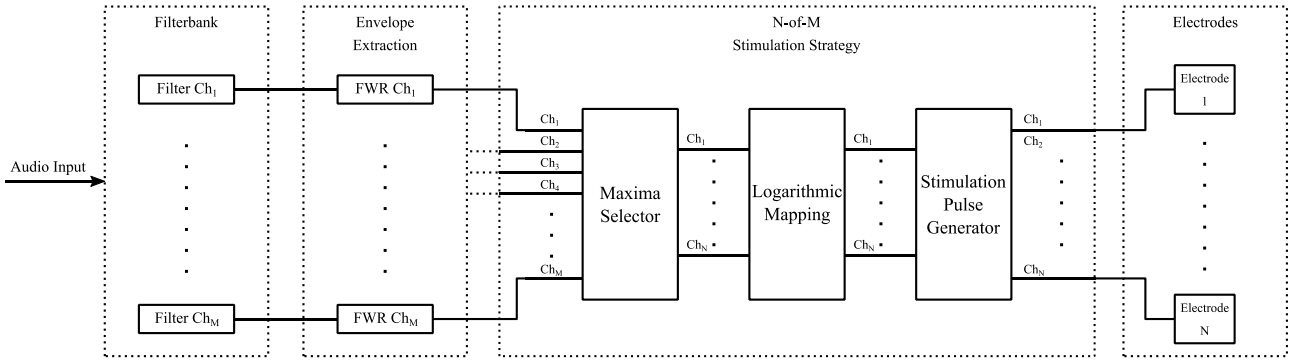


Figure 69: Top level block diagram of the N-of-M strategy. The filter bank stage usually consists of logarithmically spaced analogue bandpass filters or digital symmetric bandpass filters. The envelope extraction stage utilises full wave rectification to obtain the signal envelope. The N-of-M maxima selector selects channels based on amplitude strength or power spectral contribution, the selected channels are then mapped for electrode stimulation. The stimulation pulse generator then generates electrical pulses for stimulation.

The N-of-M stimulation strategy, shown in Figure 69, is a strategy whereby in a cochlear implant system of M electrodes, with every passing stimulation cycle, N electrodes are chosen. The criteria by which these N electrodes are chosen varies from strategy to strategy, a class of stimulation strategies are described as N-of-M like because they include an algorithmic block which selects based on a predefined criteria a subset of N electrodes out of the total M. Examples of such strategies include ACE (Advanced Combinational Encoder) and SPEAK (Spectral PEAKs).

ACE has also been shown to be the highest performing stimulation strategy [180], the reason for this is that by stimulating only the electrodes which convey the most information helps with efficiency because one can see that instead of stimulating all electrodes only a subset which can convey the most information is stimulated instead then more time can be given to said electrodes.

Within the N-of-M type strategies, there exists two sub variants the first criteria by which N electrodes is based on the amplitude. In other words, within each stimulation cycle the highest N electrodes in terms of amplitude are chosen out of the total of M. Note that this criterion can change across stimulation cycles. The other variation of N-of-M is not based on amplitude alone, but it is based on the total power contribution. Furthermore, if one hundred percent of the power of the audio is present across all channels, then N is the percentage highest power content of all channels. For instance, in a set of M channels where M is equal to eight and it is said that the power criteria for choosing electrodes is 30% then the highest contributing channels which add up to 30% of the total power of electrodes is selected. It is important to consider that there is a slight variation between these two types of N-of-M strategies and there are applications in which one is preferred over the other. The reason for choosing the N-of-M family of strategies was due to its robustness. It is critical when choosing electrodes to stimulate, to opt for ones that have a dynamic system which can respond to external criteria dynamically and is adaptable. This would be considered very beneficial when it comes to utilizing a fully hardware implementation, because a fully hardware-based implementation lacks the flexibility that software provides. Hence, it was decided that the N-of-M strategy will be the strategy of choice to realise.

The proposed implementation contains specific aims and objectives that need to be achieved by the architecture being presented.

Firstly, the N-of-M must be able to behave as the classical N-of-M. This means it would be capable of selecting the largest N out of a subset of M channels. An additional benefit would be to implement both variants of N-of-M, which is based on the number of channels with highest N channels out of a total of M or based on power content which is the highest N which form the percent power content out of the total 100% power content of all channels.

Additionally, the proposed architecture also has the additional flexibility in which the smallest N can be chosen, and additional care has been taken such that the system can interface with the OZGF filter bank [91] as well as with the proposed envelope and instantaneous frequency estimator in the previous chapter. Finally, the suggested architecture is not only is applicable to cochlear implant applications, but it is potentially useful that such an architecture can be used in machine learning applications, whereby a set of weights which change dynamically can be chosen based on a selection criterion, the highest vs lowest per cycle.

6.2.1 Problem Formulation

In order to implement the N-of-M strategy, it is necessary to formalise the problem that needs to be solved. In this section, the problem will be formalised in a way that is both intuitive while also being logical.

The problem is to select from a total of M channels a subset N. This subset forms the largest N amplitudes out of the total M. A potential approach is to use a combinatoric approach, which is to say, the number N is tracked and counted over time. This approach alone is not sufficient and would require it to be paired with a direct comparison method. The largest channels will be tracked and counted using a digital logic-based system. Finally, when the number N is reached, the selected electrodes will be chosen for stimulation.

If we were to present this idea for when M is equal to two, then such an approach might be straightforward because we are simply comparing two channels with each other, and if N is set to 1, then we simply select the highest channel. This can be implemented in various ways such as using log domain circuits, or by using Schmitt trigger type blocks. However, it is important to note that if M were to increase beyond two then the scalability of such a system will quickly increase as $N\frac{(N-1)}{2}$ number of comparisons. For instance, consider the case where M is equal

to four, N can range from one to four, whereby the largest amplitude electrodes per cycle can be selected. Nevertheless, to ensure that the correct number of channels are being chosen in each cycle, each channel needs to be compared with every other channel. It is not enough to simply compare the immediately neighbouring channels because it is not correct to assume that the channel amplitude strengths are correlated in all cases and all times. This is because even though there might be more than one region in frequency where the amplitudes are high, the subregions in nearby electrodes might be higher than another group of electrodes. Hence, using a combination of direct comparison and digital logic tracking, poses a squared block scaling complexity.

Electrodes carry continuous time signals and if electrodes are chosen then there is a non-zero chance that the relative levels of electrodes would change with respect to each other. Hence, strategies use a window-based approach. In other words, the selection phase happens within a specific time window and once the choice of electrodes is completed then no further alterations to the choices are allowed.

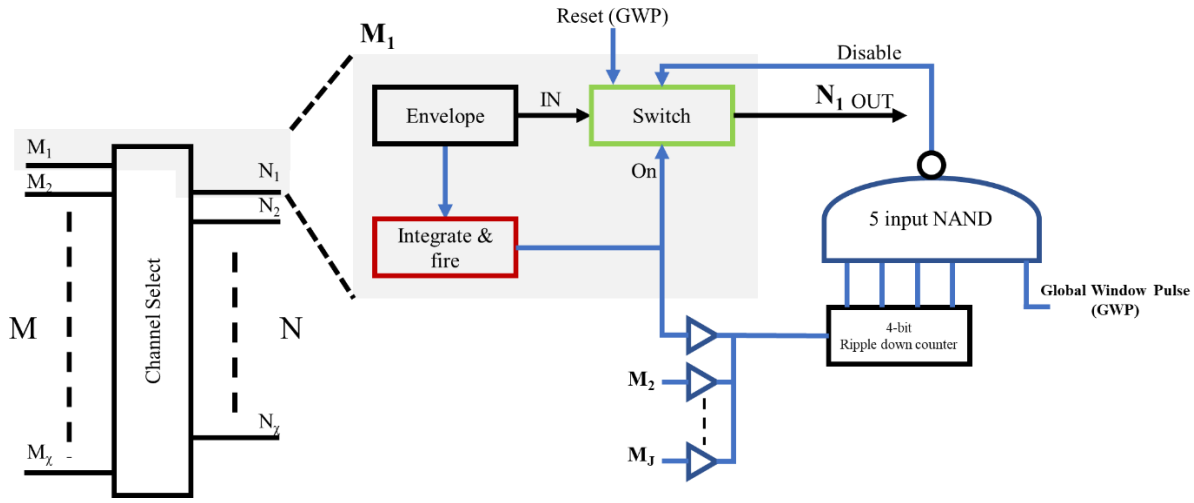


Figure 70: A block level diagram representation for implementing an N-of-M style channel selection block using an integrate and fire core, to determine the signal strength of each channel by investigating the frequency output of the integrating fire block.

An alternative to using direct comparison is to instead use a sigma delta-based approach such as the schematic shown in Figure 70. Sigma delta ADC (Analogue to Digital Converter), or a one-bit ADC sigma delta, converts amplitude information into a pulse train [58]. An input

signal will result in a spike train of a defined frequency and if the amplitude is doubled, then the spike train frequency is also doubled. This provides a solution to direct comparison because now the problem has been reformulated from comparing amplitudes to comparing frequencies of spikes. By re-formalising the problem from a direct amplitude comparison into a time-based, race type problem, the solution is to then identify which channel is the first to fire a pulse.

The problem is therefore described as from a set of M channels in a spike race what are the largest N channels that have won first as illustrated above. However, the sigma delta approach is still error prone. One of the largest limitations of using a spike time-based approach is that there is a significant chance of miscounting pulses. For instance, as in the case where twice the amplitude results in twice the frequency of a pulse train, a slower pulse train is detected first, since the integrate and fire outputs a pulse train continuously. Hence, the system would wrongfully conclude that the smaller amplitude is larger, which is not the case. Additionally, the other limitation is due to miscounting spikes when they overlap. That is because overlapping spikes will still be detected as one spike when using a digital ripple down counter. Therefore, using a Sigma Delta based architecture alone with a logic circuit which counts the number of spikes until N is reached is susceptible to errors. In the upcoming subsections, the proposed alternative approach using the time-based race problem reformulation will be introduced, which aims to solve the previously mentioned limitations.

6.3 Proposed Architecture

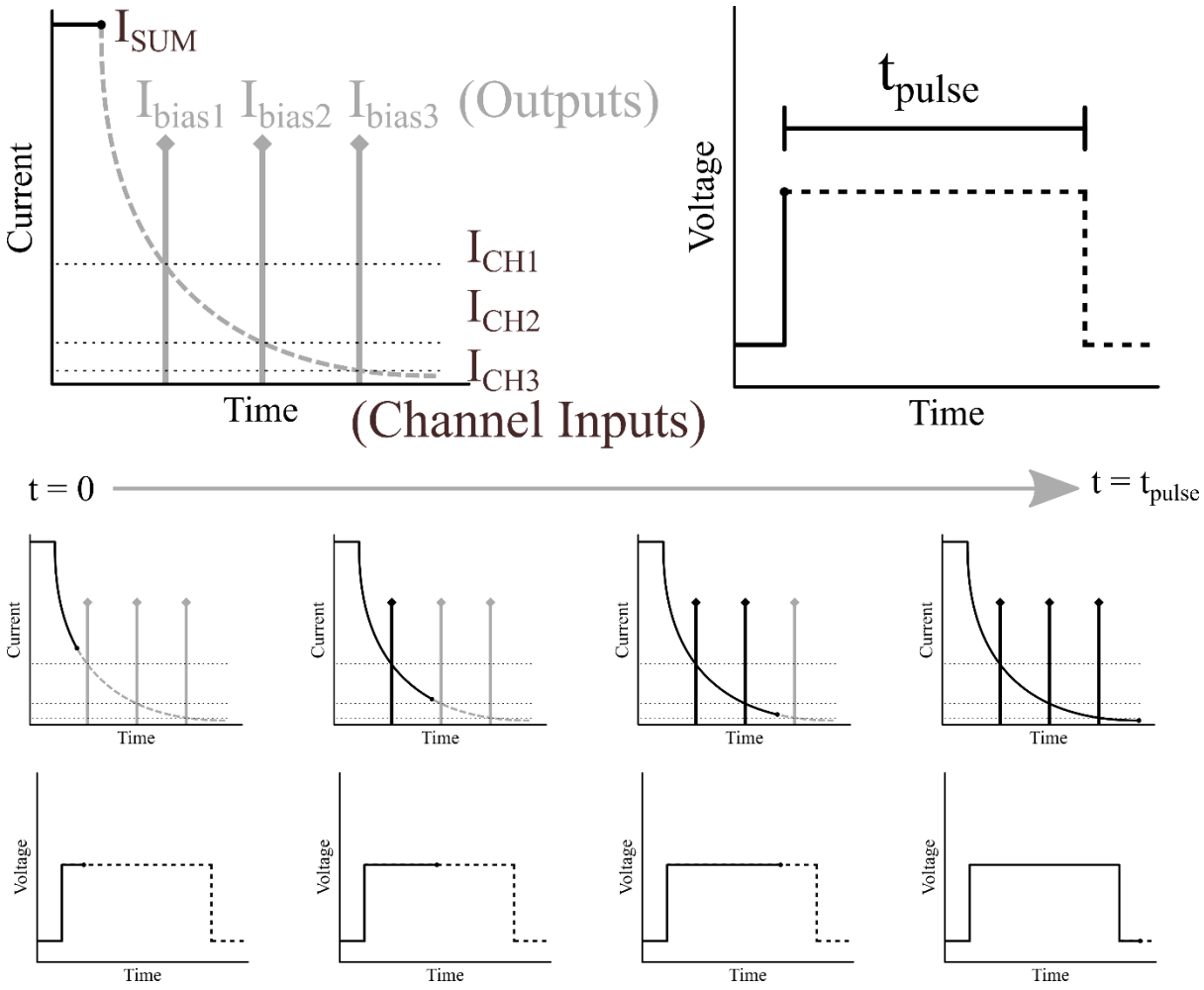


Figure 71: The principle of operation by which the proposed WTA architecture operates is illustrated from left to right as follows. Firstly, at time t=0 the threshold current is equal to I_{sum} which is the continuous real-time sum of all channels. As time moves forward I_{sum} decays over time and when the corresponding thresholds are reached, the channels in their respective WTA comparisons fire in order of strength. Finally, when the selection criteria N is reached then all switches are disabled until the next clock cycle where the whole process is repeated.

In this section, the proposed architecture will be introduced, described and results from Cadence Virtuoso (Cadence LLC) transistor level simulations will be shown to verify its efficacy. The proposed architecture is a hierarchical 'Winner Takes All' (WTA) design as shown in Figure 71 and it achieves the desired selection by summing all the WTA positive

output bias current values from each channel block. The initial state of the architecture can be visualized as the start of a race, whereby each channel is compared with a decaying threshold current. This decaying current is equal to the current sum (I_{sum}) of all channels at time zero. This is because I_{sum} is the only possible current which is larger than any channel output that can be determined *a priori* without any knowledge of the signal strength of the individual channels. It is crucial to ensure that the starting threshold current value must be greater than any other channel current value I_{chi} in order for all channels to be off at time $t = 0$.

As the current decays, larger amplitude channels will win first, and as channels win their individual WTA blocks will send their output bias currents Io_i to a summing node. Note that this process is reversible. In other words, if the condition of I_{sum} being less than I_{chi} is no longer true, then the output I_{o1} shown in Figure 72, which represents a selection signal, will change back from I_{bias} to zero.

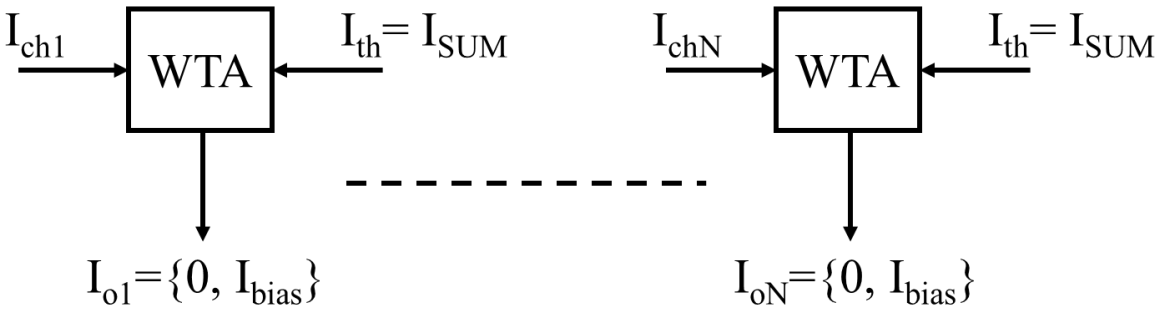


Figure 72: A top-level block diagram to illustrate the concept of several WTA blocks operating in parallel to realise a linearly scaling channel selector design.

As individual blocks win their own isolated races, the output bias currents are continuously summed up, they can be compared with an integer multiple of I_{bias} corresponding to N. Once that is achieved, all channel selections will be frozen, which means the selected channel switches stay selected and the remaining channel switches are disabled in this current clock cycle, once the clock cycle resets the entire process is repeated.

Some advantages of this approach are that on top of correctly selecting all largest N channels it is also possible to sort them in descending order in continuous time with no explicit direct comparison across channels or memory modules. This is because when a particular channel selection is performed it occurs sequentially in order of strength due to the time decaying threshold signal approach.

Additionally, this approach avoids the overlapping spike problem highlighted earlier. This is because even though channels can potentially fire a winning signal at the exact same time, the sum of the WTA output bias currents I_{biasi} will be an integer multiple of I_{bias}. Hence, it will be correctly counted as multiple channels instead of only one.

Some of the tradeoffs includes requiring a decaying current threshold which in this case is equal to I_{sum} resulting in an ($M \times I_{sum}$) current consumption for all channels. However, the minimum threshold signal $I_{th}(t)$ required is a current signal of value: $max(\{I_{ch1}(t), \ldots, I_{chM}(t)\})$. Therefore, since $I_{th}(t)$ cannot be known a priori due to it being a dynamic signal, the maximum operator would need to be continuously computed to reduce the total power consumption. Therefore, I_{sum} is a simpler signal to create which achieves the same purpose at the cost of higher current draw. Additionally, there exists a scalability upper limit, which unless a companding technique is used to supplement the approach. This can be potentially achieved by grouping groups of cells together following a 4:1 ratio to reduce the threshold currents required by a factor of four when scaling up the design. Since the proposed design relies on individual blocks per channel the overall circuit complexity would be of order O(n).

6.3.1 Winner Takes All

In this section a log domain implementation of the Winner Takes All (WTA) block, will be described. A WTA circuit is a block with two inputs and two outputs as shown in Figure 73. The positive output I_{o1} is zero when the positive input I_{in1} is smaller than the negative input I_{in2}. However, when I_{in1} is larger than I_{in2} then the positive output I_{o1} becomes I_{bias}. This can be described in the following piecewise functions:

$$I_{o1} = \begin{cases} 0, & I_{in1} < I_{in2} \\ I_{bias}, & I_{in1} > I_{in2} \end{cases} \quad (6.4.1.1)$$

$$I_{o2} = \begin{cases} I_{bias}, & I_{in1} < I_{in2} \\ 0, & I_{in1} > I_{in2} \end{cases} \quad (6.4.1.2)$$

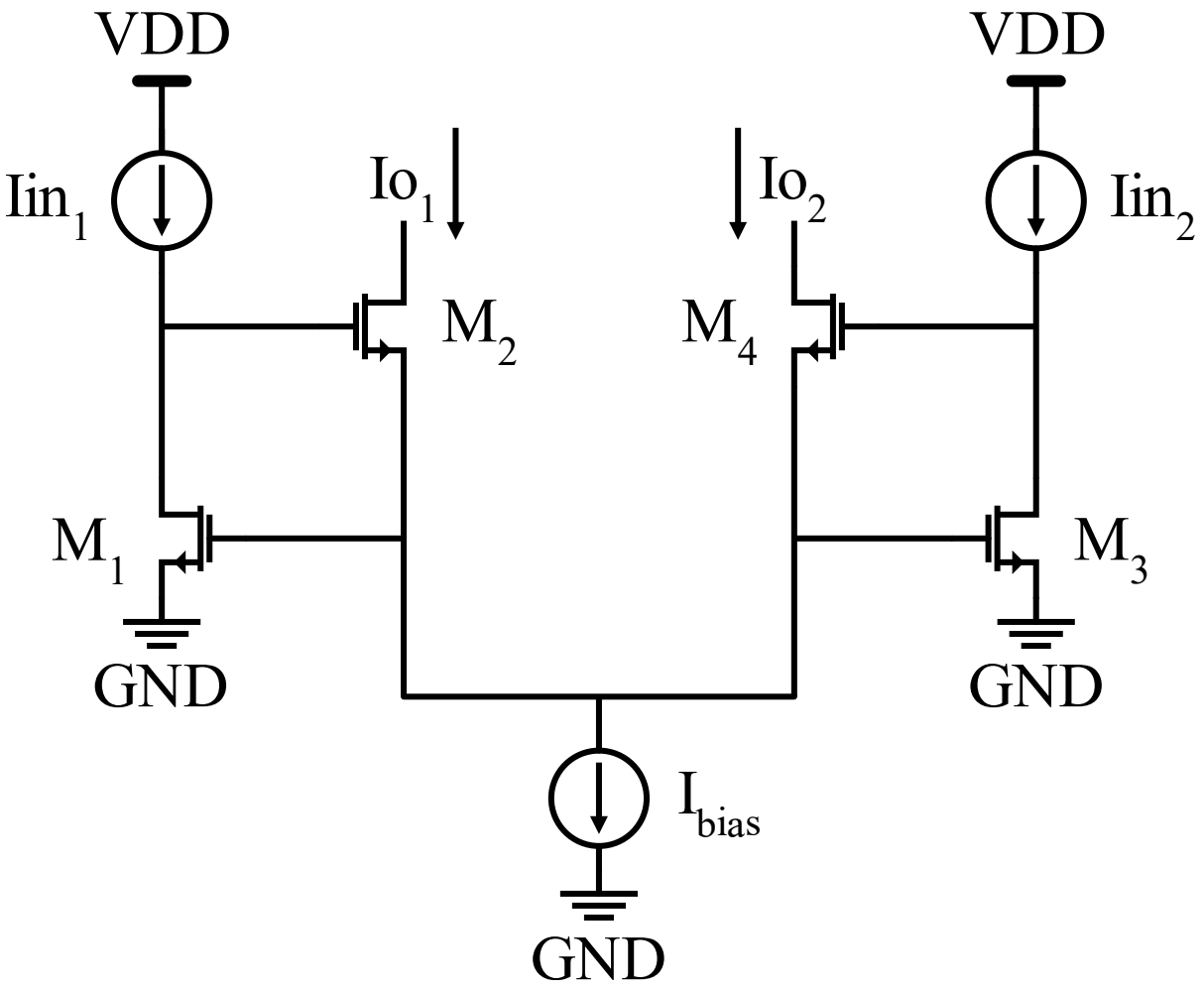


Figure 73: Circuit schematic of the WTA circuit.

The WTA operates as follows, considering the case when I_{in1} is equal to I_{in2} then the circuit is perfectly balanced and I_{o1} is equal to I_{o2} by Kirchhoff's current law. When I_{in1} is greater than I_{in2} the V_{gs} of M_1 also increases. As a result, the V_{gs} of M_3 also increases due to the gates being shorted. However, this forces the V_{ds} across M_3 to decrease to support the current flow of I_{in2} which decreases the V_g of M_4, this is a positive feedback loop which results in M_2 being switched on and M_4 being switched off and having I_{o1} equal I_{bias}. This can be shown visually with a DC sweep as in Figure 74.

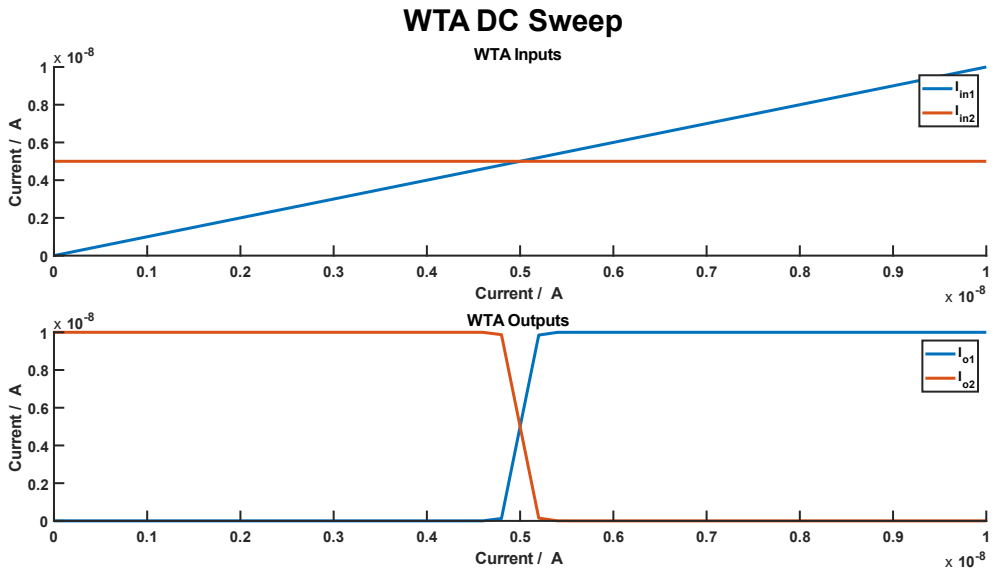


Figure 74: DC sweep of the WTA block shown in Figure 73 with a biasing current equal to 10 nA, the output I_{o1} is equal to I_{bias} (high) when the input I_{in1} is larger than I_{in2}.

Winner takes all circuits are commonly used in machine learning applications [181]–[184], when the largest weights or biases needs to be selected. The selection of the simple winner takes all (WTA) block was based on its simplicity and low transistor count. Additionally, the current based approach meshes incredibly well with the previous subsystems. As a result, this offers excellent scalability when additional channels are included. The WTA circuit that was implemented is a slightly modified version of the simple winner takes all as shown in Figure 75 alongside device and bias current values. This modification includes additional current mirrors to interface with 16 envelope channels and decaying current inputs.

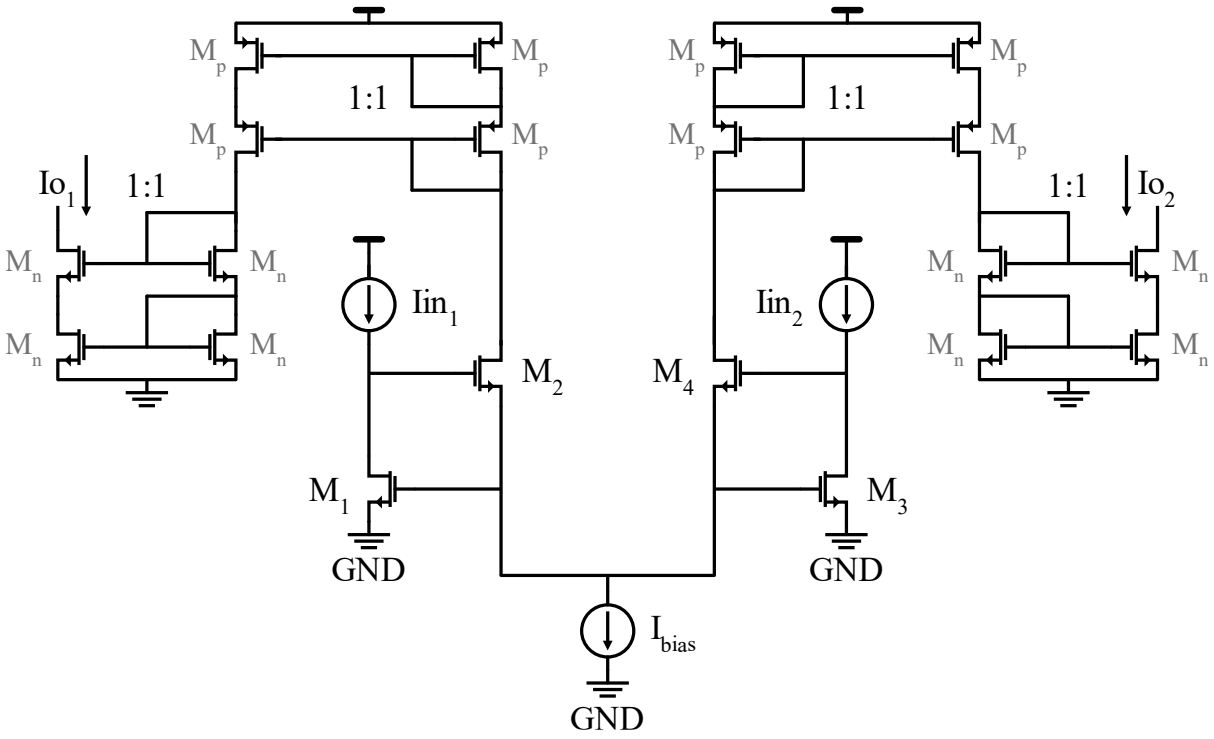


Figure 75: Circuit schematic of the modified WTA circuit to allow for parallel computation with 16 other channels.

The device parameters for the above circuit design of the balanced WTA design are summarised in the Table 9.

Table 9: Summary of the WTA circuit device dimensions and biasing current values used during all simulations.

Balanced Winner Takes ALL	
Parameter	**Value**
Vdd	3.3 V
$(W/L)_{1,2,3,4}$	0.35 µm / 0.35 µm
$(W/L)_{p,n}$	0.35 µm / 0.35 µm
I_{bias}	50 nA

A variation of the common WTA circuit is the K-winner takes all. The K-WTA topology is a modified WTA circuit with K inputs and one output, which is the largest input signal. However,

it is not enough to simply use a K-WTA circuit to implement an N-of-M maxima selector block, that is because the 'winner' of a K-WTA is still a single output [185]–[191], these implementations in literature propose voltage-mode based blocks, which lack the operational flexibility that would be required. In addition, for cochlear stimulation the ability to select a varying number of channels is required.

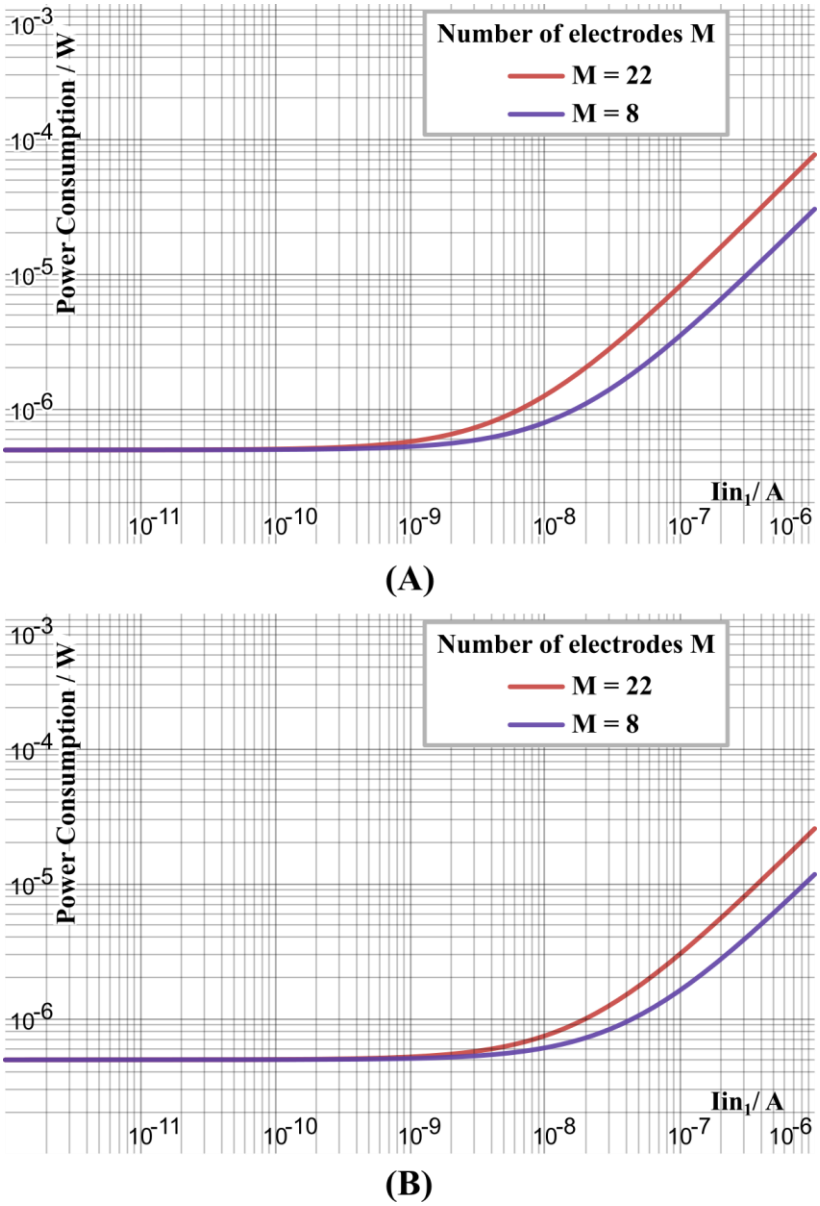


Figure 76: The total power consumption of the modified WTA circuit as a function of input signal strength and number of electrodes.(Top) The maximum theoretical power consumption if the signals in all of the channels are equal (Bottom) The typical power consumption when 30% of the channels constitute over half of the total power across all channels.

The total number of channels implemented will also have an effect on the power consumption of the WTA block, in Figure 76-(A) the absolute upper limit of the power consumption is shown in the case of 22 channels and 8 channels. This is the case when all channels are of equal value which is not a realistic scenario as that is the definition of white noise. Therefore, Figure 76-(B) is a more realistic scenario in which 30% of the channels constitute over 50% of the total power across all channels.

6.3.2 Hardware Implementation

Figure 77 shows a top-level block diagram of the proposed architecture with M total inputs and N total outputs. Such a system is required to select a subset of channels with a maximum of N, in addition the channels are sorted sequentially in order of strength during operation.

A 16-channel selector block was implemented as it is a typical number of channels for a cochlear implant. The '16-channel WTA core' consists of 16 WTA blocks, each WTA block is continuously compared with a decaying $I_{sum}(t)$ current. With this approach, the modified WTA can be used providing O(n) circuit complexity scalability with the number of channels.

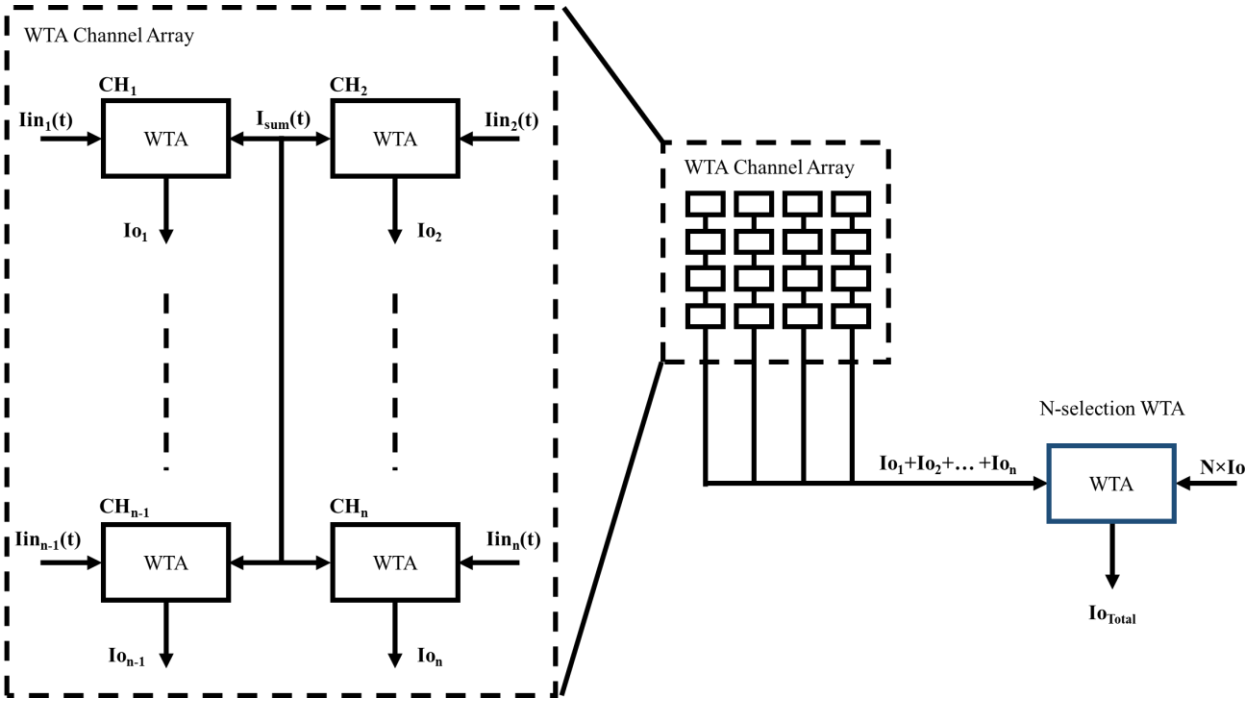


Figure 77: *Top level block diagram of the 16 channel WTA core selector block.*

The sum of the output currents Io_i from all the blocks is fed into a final N-selection WTA block which continuously compares the Io_{sum} with $N \times Io$ once this criterion is reached the output Io_{Total} changes from low to high. This output signal is then converted into a voltage signal (CTRL) which is used to disable all the channel switches since the selection criteria is met.

Furthermore, the same individual WTA output currents (Io_i) are copied and converted into a voltage and used to control the SET pin of a gated SR-latch as shown in the schematic shown in Figure 75. Each output from the 16-channel WTA core represents a voltage signal, which when high means that the corresponding channel has 'won' its individual race against the decaying I_{sum}(t). When this is the case and as long as the RESET pin is high and the ENABLE pin is low then the output of the gated SR-latch Q is set to high.

The Q signal is converted back into a current (I_{ctrl}) and is set to the positive input (I_{in1}) of a WTA based current switch, whose negative input is set to I_{th} which is equal to half of I_{ctrl} when high. Therefore, when I_{ctrl} becomes high the positive output of the WTA becomes I_{bias} which in the WTA switch case is equal to I_{chi}. On the next rising clock cycle all the gated SR-latches are reset and I_{th}(t) is reset to I_{sum} which resets the system's dynamics. The block diagram is shown in Figure 78.

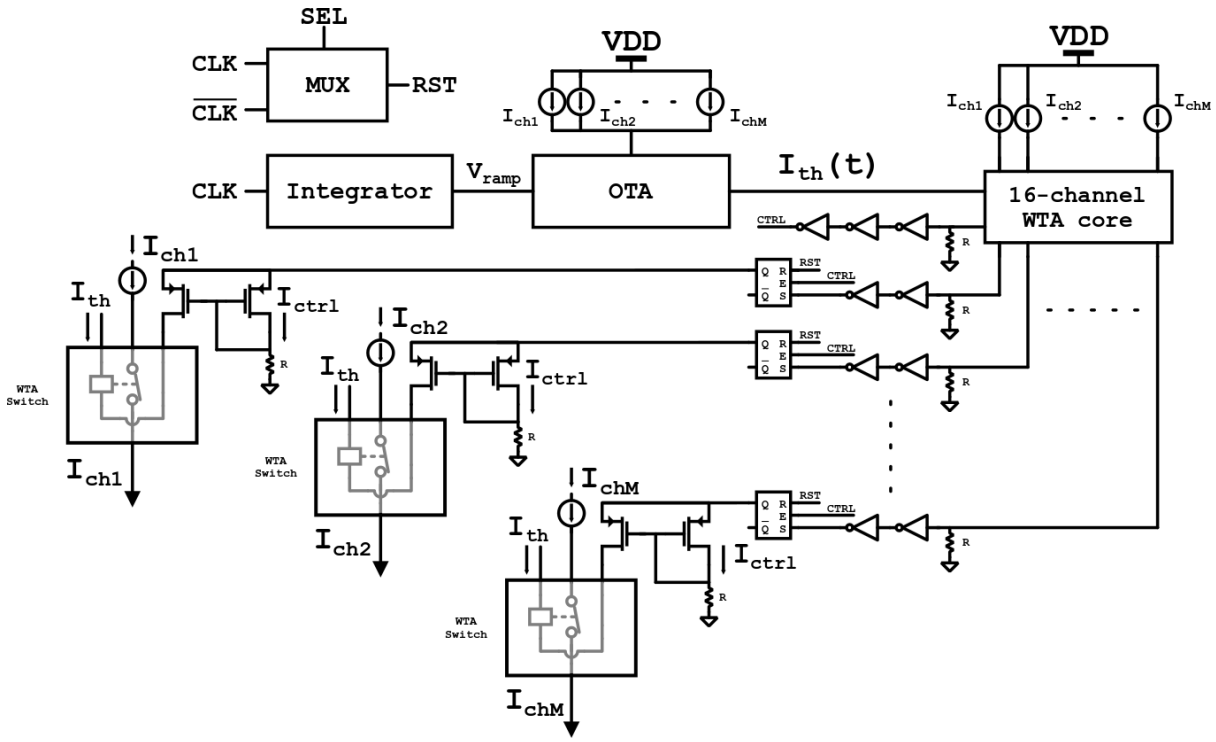


Figure 78: Top level diagram of the fully hierarchical WTA based design.

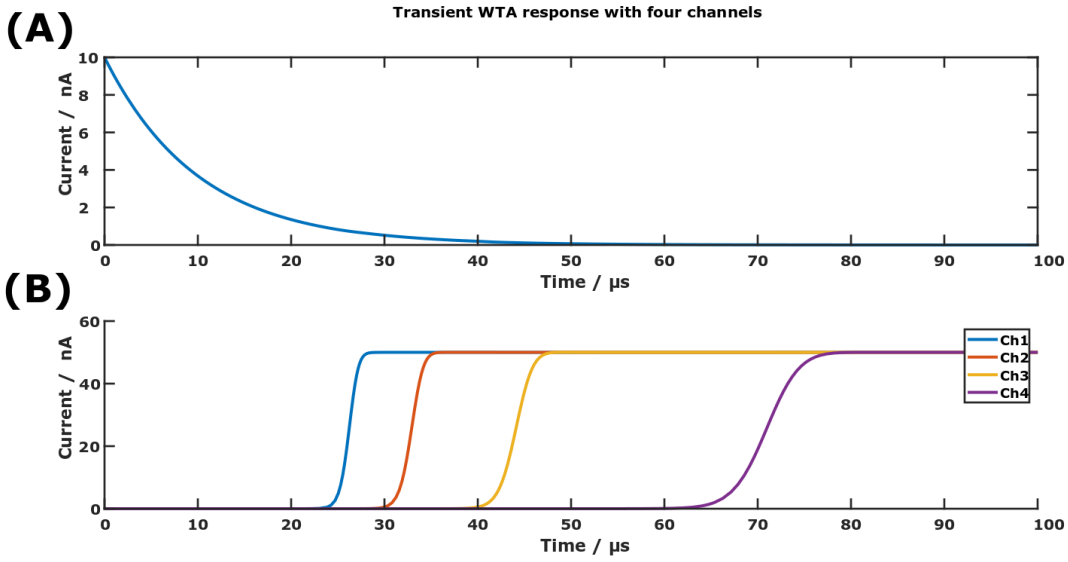


Figure 79: Cadence simulation of a transient output of four channels each with their own WTA circuit. The order in which the channels switch on is dependent on their relative strength meaning that the strongest channel fires first followed by the second strongest and as follows. (A) Shows the decaying I_{SUM} current which is used as a dynamic threshold. (B) The output currents from the individual WTA blocks.

Figure 79 illustrates a transient simulation for 4 channels of stimulation. In this example, the DC current channel values for channels 1-4 were 4 nA, 3 nA, 2 nA, and 1 nA respectively. The I_{sum} value at time zero is equal to 10 nA, as time progresses and I_{sum} decays the outputs of channels 1-4 fire sequentially in order of strength. Since the decay is exponential, the time difference between later channels is larger than earlier channels, this effect is by design and desirable because a selection error made when N approaches M is more detrimental to the system's overall reliability. As long as the decaying current is able to approach zero then all channels will eventually fire.

The subsystem to generate a decaying I_{sum} requires several stages. The decaying current is required to follow a global CLK signal, where on each rising edge, representing $t = 0$, the output current is the continuous sum of all the channel currents, doing so resets the dynamics of the entire system. Additionally, the I_{sum} decay must occur fast enough to ensure the correct number of channel selection within the determined clock cycle.

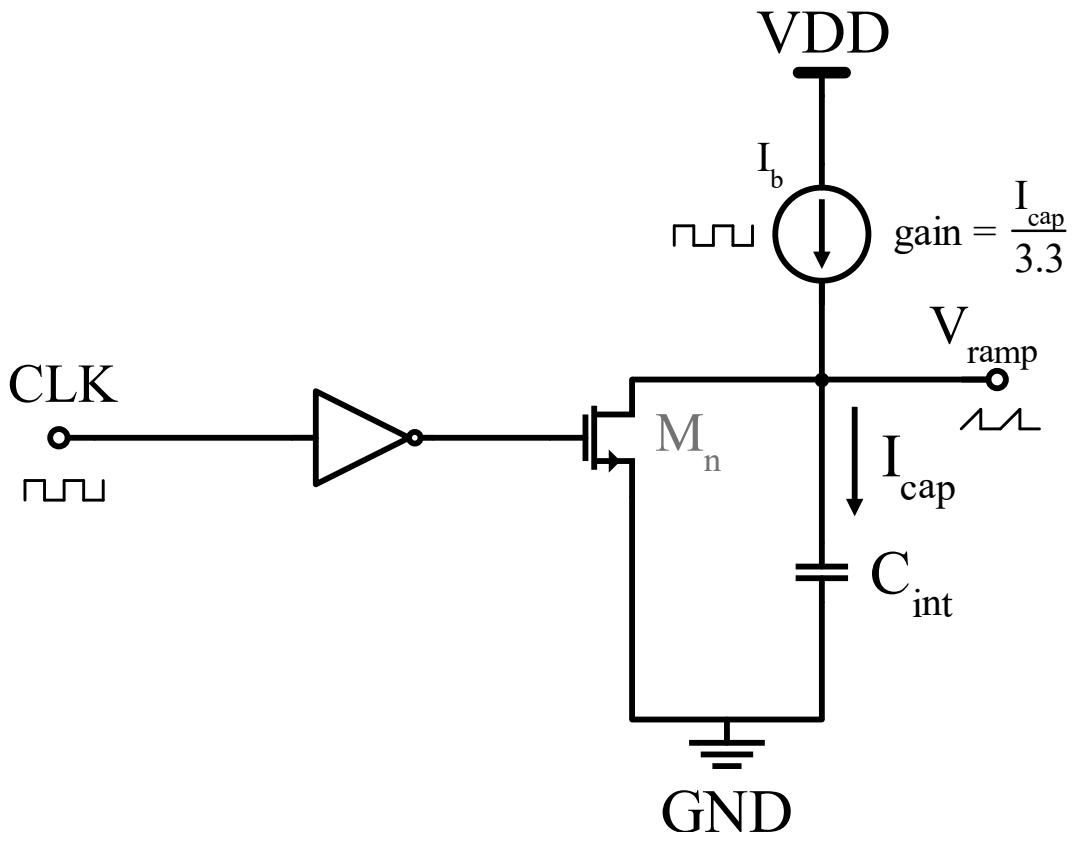


Figure 80: Clock driven integrator circuit sub block used for the N-of-M selector block.

The first block is a switch-controlled integrator shown in Figure 80. When the CLK signal is low the gate input V_g to M_n is high, in this case the biasing current I_b flows through the drain of M_n shorting the output to ground. However, when CLK is high the gate voltage V_g of M_n is low therefore:

$$I_b \approx I_{cap} \tag{6.3.2.1}$$

Hence all of I_b flows through C_{int}:

$$I_b = \mathrm{C}_{int}\frac{dV}{dt} \tag{6.3.2.2}$$

$$\int \frac{I_b}{C_{int}}dt = \int dV \tag{6.3.2.3}$$

$$\mathrm{V} = \frac{I_b \cdot t}{C} + \mathrm{k} \tag{6.3.2.4}$$

The integrating capacitor C_{int} integrates the current flowing through it into a voltage following the above relationship. Since the next stage is an OTA (Operational Transconductance Amplifier) the output V_{ramp} signal connects to a high impedance node which means that the relationship still holds. Below in Table 10 are the device parameters used during Cadence Virtuoso simulations.

Table 10: Summary of the device dimensions and biasing currents for the switch-controlled integrator block.

Switch-controlled Integrator	
Parameter	**Value**
VDD	3.3 V
$(W/L)_n$	10 µm / 0.35 µm
I_{cap}	250 nA
C_{int}	56.6 pF

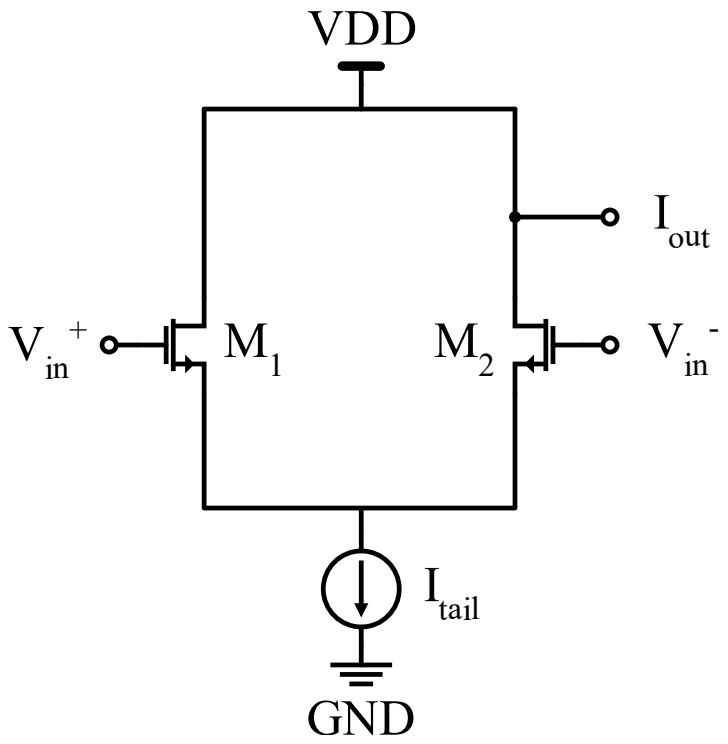


Figure 81: Circuit of an OTA block, the tail current I_{tail} defines the maximum value the OTA block can generate. A decaying I_{out} is possible to produce by sweeping the positive input voltage pin V_{in}^{+}, which is a signal that was obtained in the previous switch-controlled integrator block shown in Figure 80.

The single-ended OTA circuit shown in Figure 81 utilizes a mismatched differential pair, with their sources sinking a current I_{tail}. The OTA obeys the following relationship:

$$I_{out} = I_{D,M1} - I_{D,M2} \tag{6.3.2.5}$$

$$I_{tail} = I_{D,M1} + I_{D,M2} \tag{6.3.2.6}$$

$$I_{D,M1} = I_S \cdot e^{\left(\frac{V_{in}^+}{2nV_T}\right)}, \qquad I_{D,M2} = I_S \cdot e^{\left(\frac{V_{in}^-}{2nV_T}\right)} \tag{6.3.2.7}$$

$$tanh\left(\frac{V_{in}^+ - V_{in}^-}{2nV_T}\right) = \frac{I_{D,M1} - I_{D,M2}}{I_{D,M1} + I_{D,M2}} \tag{6.3.2.8}$$

$$I_{out} = I_{tail} tanh\left(\frac{V_{in}^+ - V_{in}^-}{2nV_T}\right) \tag{6.3.2.9}$$

Where n is a unitless number with a value of around 1.2 and V_T is the thermal voltage and is around 26 mV. Setting V_{in}^- to $\frac{Vdd}{2}$ and setting M_1 to be ten times wider than M_2 it is possible for I_{out} to span the entire range from I_{tail} to zero. The exact values and parameters used during simulation are summarized in Table 11.

Table 11: Summary of the device parameters and bias current for the single-ended OTA.

Single-ended OTA	
Parameter	**Value**
VDD	3.3 V
$(W/L)_1$	7 µm / 0.35 µm
$(W/L)_2$	0.35 µm / 0.35 µm
I_{tail}	I_{sum}*
V_{in}^-	$\frac{Vdd}{2}$

* The value I_{sum} is the continuous current sum of all channels.

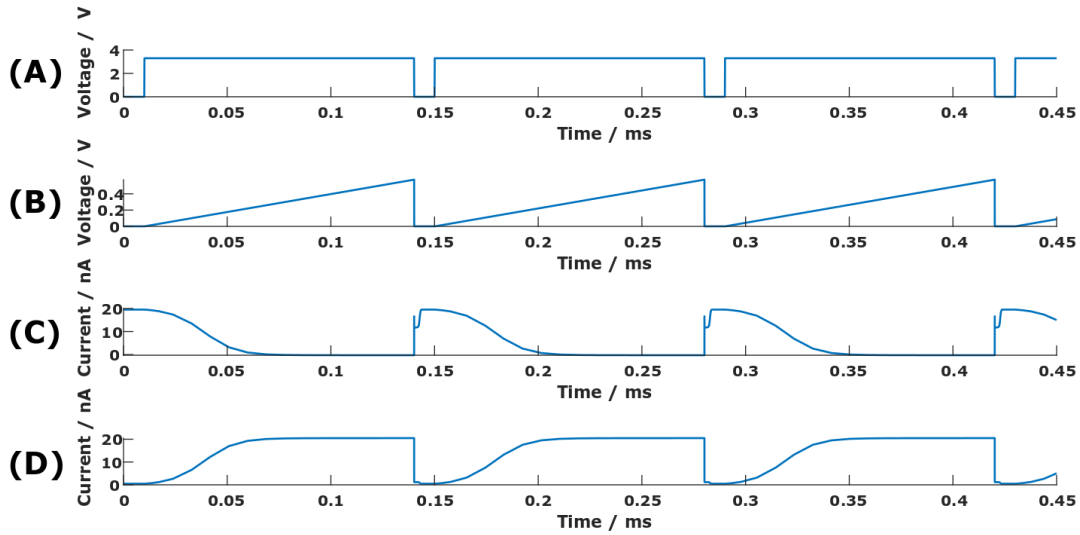


Figure 82: Transient simulation showing the outputs of the switch-controlled integrator with a clock duty cycle of 90%, the positive output current with an I_{tail} value of 20 nA when the integrated ramp is used as an input. The bottom trace is the negative OTA output current.

The integrator-OTA subsystem was simulated in Cadence, Figure 82 depicts a transient simulation when a 90% duty cycle is used as input for the integrator. The second trace shows the voltage output of the switch-controlled integrator, which converts the square wave into a linear voltage ramp. This ramp signal is then fed in as input to the single ended OTA with a tail current (I_{tail}) equal to 20 nA, the third trace shows the positive output of the OTA with the output current starting at 20 nA and decaying towards zero. The final trace is the negative output current of the OTA which is equal to I_{tail} minus the positive output current, which starts at zero and increases to 20 nA.

6.3.3 Modes of Operation

This subsection will further explore the potential modes of operation that are possible with the proposed system as well as demonstrate the flexibility using this implementation. In the previous section, we have shown that the proposed system is able to choose a subset N largest channels from a total of M.

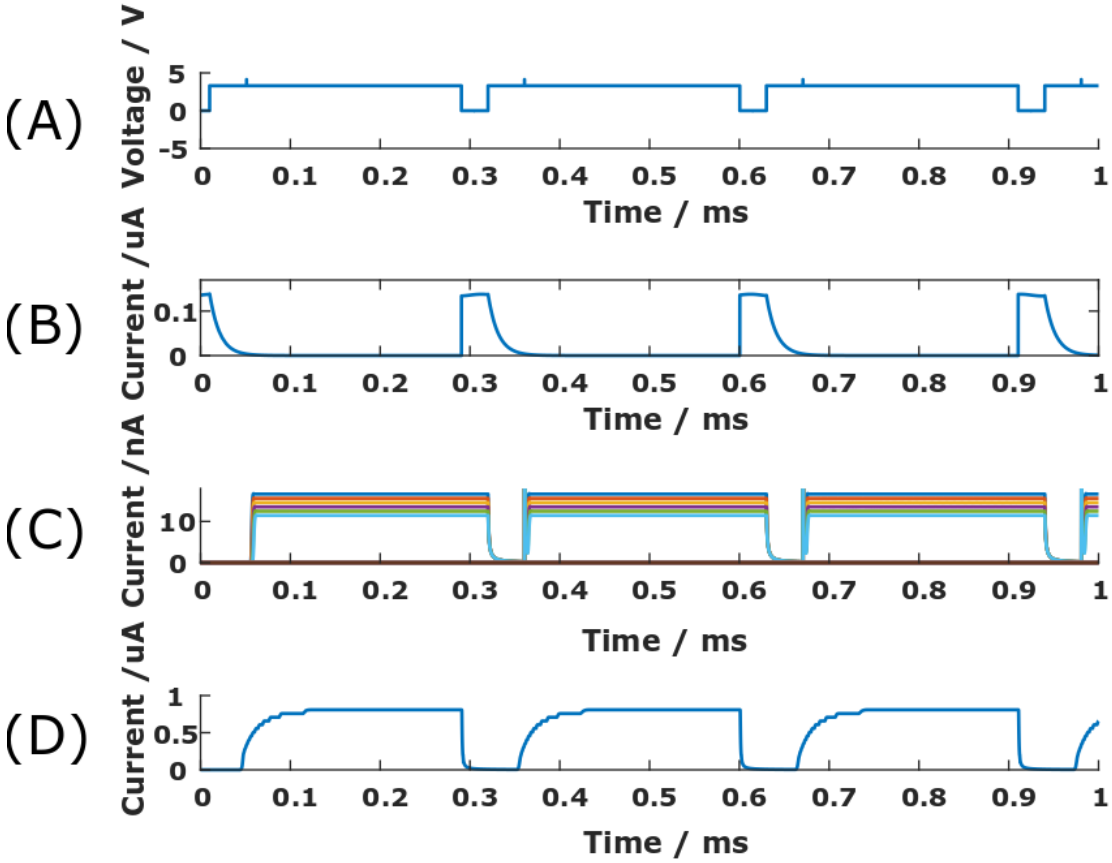


Figure 83: Transient simulation of the whole system with 16 total input channels. N is set to 6 (select 6 largest channels) with a clock frequency of 3.2 kHz. The second trace depicts the decaying I_{sum} current which is used as a threshold for the individual WTA blocks. The third trace depicts the output currents that are allowed to pass through, channels 1-16 each carry a DC current of 16 nA-1 nA respectively, only the first 6 channels are allowed to flow. The final trace depicts the continuous time value of the cumulative sum of the positive output currents Io from all 16 channels.

Figure 83 depicts the first mode of operation with 16 input channels, selecting the largest N channels, which is set to 6 in the above simulation. The rising edge of the clock initializes the system and sets the decaying threshold current to I_{sum}. As time progresses I_{sum} decays and individual channels win their respective races. The final trace shows how this continuous time cumulative current increases in integer step values of Io. When the sum of output currents is equal to 6*Io* then a signal is sent to disable all the gated SR-latches. On the next rising edge of

the clock the whole system is reset, and the process begins anew. If the value of N is changed across clock cycles, then the number of channel selections can be obtained dynamically.

The continuous nature of the decaying I_{sum}(t) current is used to achieve the second mode of operation, which is to choose channels based on power spectral contribution instead of simply amplitude strength. At time zero, all of the signal's power is distributed across the M channels. This same decaying I_{sum}(t) current will again pass through a similar N selector WTA block. However, the decaying I_{sum}(t) is now compared with αI_{sum} where α is an electronically tunable signal using a log domain multiplier shown in Chapter 4. This means if α is set to 0.5, the decaying current I_{sum}(t) is being compared against half of I_{sum}(t=0). Therefore, as individual WTA channels win their respective races the stopping condition is now no longer an integer multiple but instead it is a percentage value of the total power content as long as α<1. With this approach we are now no longer choosing channels based simply on their amplitude ranking, but we are picking the larger signals based on their power content, since the power of a signal is I^2V, which is proportional to the square of the current value.

Within the selection subset N, the final mode of operation is in the timing of channel selection. By using a $\overline{CLK}$ signal two modes of operation are obtainable; firstly, is the 'Sync' mode where all channels switch on together in synchronous fashion once the final chosen criteria are achieved, for example if N is equal to 3 then channels are only turned on when three channels are selected, this is achieved by using a $\overline{CLK}$ signal as the reset for the gated SR-Latch. signal as the reset for the gated SR-Latch, hence the inclusion of a multiplexer to achieve both modes of selection.

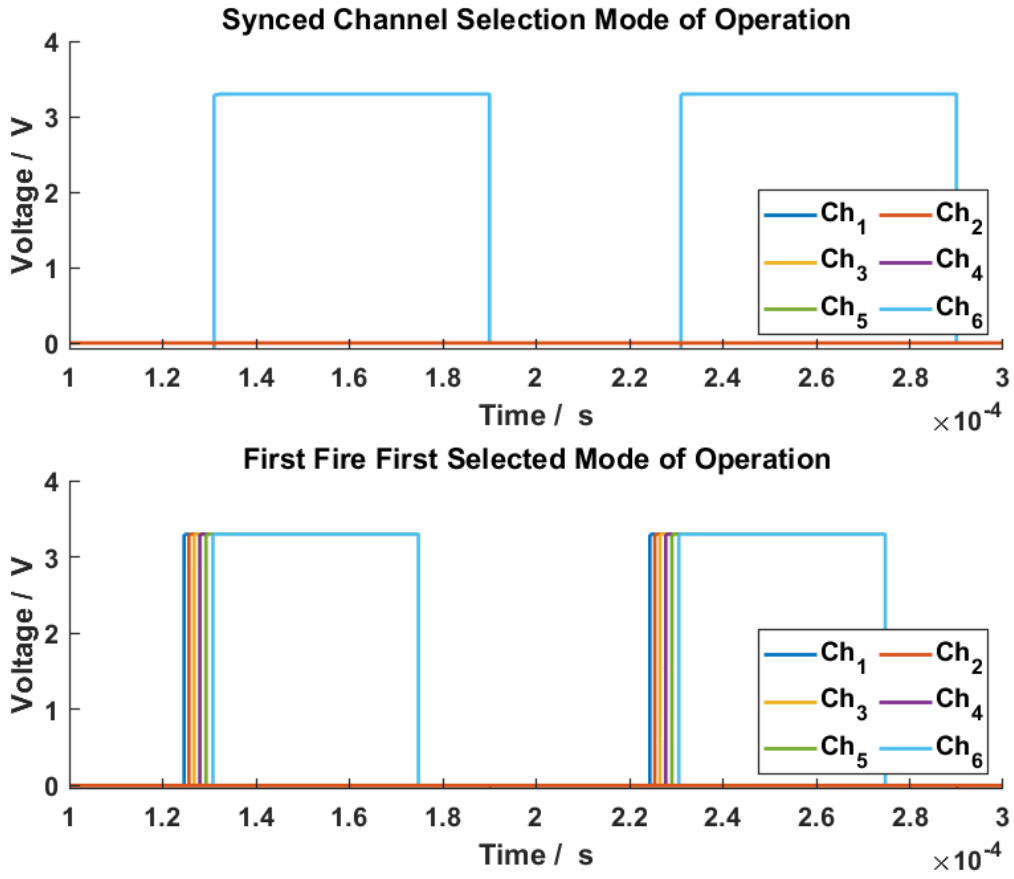


Figure 84: Channel output timing diagrams comparing both methods of channel selection with a frequency of 10 kHz. In this case N is set to 6, the top trace only switches on all selected channels when the criteria of N is achieved (Synchronous channel selection). In the bottom trace channel selection is performed sequentially in order of signal strength, this form of channel selection also performs memoryless sorting operation on the channels due to the selection method.

The second mode of channel selection is the 'FFFS' (First Fire First Selected) approach shown in Figure 84, where channel switches turn on as soon as they win their individual race. This is achieved by using CLK as the gated SR-latch reset trigger. In addition, the FFFS mode performs a memoryless channel sorting operation for all channels if N is set to equal M. These are slight variations in the mode of operation that provides novel variability to the overall system.

In conclusion, we have shown that the proposed system, although simple and scalable, is flexible enough to implement several modes of operation. Moreover, usually providing flexibility in a complete system on chip design leads to compromise in the attempt to optimize

for size, which leads to sacrificing more flexibility. This is all primarily achieved within the log domain paradigm, which meshes and behaves as expected when interacting with previous blocks, as well as operation in a low power scheme.

Chapter 7

Conclusion

7.1 Summary of Thesis Achievements

In this thesis, two major research contributions have been outlined. The first is a novel integrator-based approach to estimate the Hilbert transform by applying a -90° phase shift to the incoming signal wave using a log-domain integrator core. The input and output signals are then used to compute the slow envelope, the analytic envelope and to approximate the instantaneous frequency. This approach is performed using analogue-only log domain circuits, providing a continuous time and continuous value computation in the weak inversion regime resulting in an ultra-low power solution.

Additionally, another contribution is the development of a custom ASIC solution which implements the above signal processing approach, fabricated using 0.35µm AMS technology.

The second research contribution is in a novel flexible N-of-M selector block with multiple modes of operation, which selects the largest N signals from a set of M channels within a specified pulsed time window up to 10 kHz. This approach is realised with a hierarchical based winner-takes-all architecture with the input and output signals being quasi-DC current based

signals. The number of channels is dynamically chosen by starting a race to fire, by comparing with a decaying I_{sum} threshold current. As individual channels win the race, each of the channels are subsequently selected.

Once the criteria N is reached the choice is locked until the next selection cycle. This approach provides additional flexibility, by allowing N to change dynamically across clock cycles and to also change the selection method from an integer multiple of channels or based on channel energy content. Additionally, channel switch selection can be performed synchronously or by selecting channels in time according to their strength, which also performs a memoryless channel selection operation with O(n) circuit complexity.

7.2 Applications

The proposed blocks have several applications in various fields as mentioned previously. The most prominent ones are cochlear implants and neuro stimulators. In both, applications signal processing plays a critical role in the quality of signals produced. In addition, the approach to the stimulation strategy is important when conveying meaningful information to the nerve fibres. Other applications to the proposed systems include biosensors, where continuous data in the form of a current is read from specialised sensors. Such signals require to be processed in a continuous-time continuous value manner. Hence, the proposed system provides a framework for implementing signal processing in real time. For example in computing the various characteristics of the signals being measured by the sensors [192] such as the rate of reaction of an ion species [193]. Another example, of a potential application, is in the field of analogue based computation in which models are utilised to accelerate certain processes. These models contain parameters which contribute to the weights for specific applications. These weights need to be continually updated and selected for. Hence, the N-of-M selector might fulfil a potential gap in the field of analogue computation to provide a solution for such dynamic computation.

7.3 Future Work

For future work there are several key aspects of the proposed designs that can be improved on in future iterations. Starting with the analytic signal approximation, the Seevinck integrator can be improved by replacing the capacitors with MOSCAPS to decrease the footprint of the block as well as strengthening the feedback. This would aid in reducing the sizes of the integrating capacitors, which are present at the capacitive nodes. Furthermore, it is important to consider that this design proposal using the feed-forward approach to test simplicity and time responsiveness would warrant consideration to investigate a negative feedback approach. This would aim to offer self-rectification properties, such that the integrator's frequency response would self-correct around the centre frequency.

The second optimisation would be done on the log-domain vector magnitude calculating block, which in its current iteration only supports positive currents in one input. This would cause a limitation as additional rectifying blocks would be required. However, an alternative design to this would be to calculate the vector magnitude which supports bi-directional current. This could be beneficial in eliminating some of the blocks, as well as improving the accuracy by reducing the errors introduced in the rectification step. This is done by maintaining the differential signal flow path.

The third set of optimisations is to introduce an alternate mode of operation to select for the smallest N instead of the largest. Generally, this is not an approach that is used practically in the context of cochlear implant stimulation. However, it is important to explore all features of an architecture to identify potential implementations that may become feasible in the future. For instance, in scenarios where the time required for channel selection is critical and if N is larger than half of M, then it is faster to select for (M -N) smallest channels first and then eliminate those channels instead of picking for the largest N channels. This mode of operation is obtained by summing the negative Io currents from the OTA outputs and by using the alternate branch of the OTA in which I_{sum} exponentially increases from zero to Is_{um} from zero as channels lose, a negative output the winner takes all goes from zero to one, and when these are summed together a similar approach to the previous section can be employed, where it is compared to N times I_{bias} which is still a subset of real positive integers. However, it now represents the smallest N channels. Note that coupled with the FFFS selection approach it is

also a memoryless method of sorting signals in ascending order, whereby channels fire sequentially by ranking from smallest to largest.
It is evident from the discussion above that the N-of-M selector architecture can provide an effective means of selecting the optimal stimulation channel for a cochlear implant system. By exploring various optimization techniques, such as selecting the optimal N and M values, minimizing cross-channel interactions, and incorporating a temporal mechanism, the architecture can be tailored to meet the specific needs of individual patients. Furthermore, future advancements in electrode technology may allow for the use of companding techniques to scale up the architecture and support more than 16 channels. Specifically, grouping together groups of four channels in a hierarchical manner, such that the winner of each quarter race is then passed onto the next race, could help maintain the order of strength. Overall, the N-of-M selector developed presents a promising solution for improving the performance of cochlear implant systems and enhancing the quality of life for individuals with hearing impairments.

Lastly, once the two circuits are optimised it will be possible to design for the first time, a full cochlea on chip in the log-domain in combination with the work by Guang.Y(2014) shown in Figure 85. Such efforts would require an interdisciplinary team to ensure progress towards a totally implantable cochlear implant can be realised.

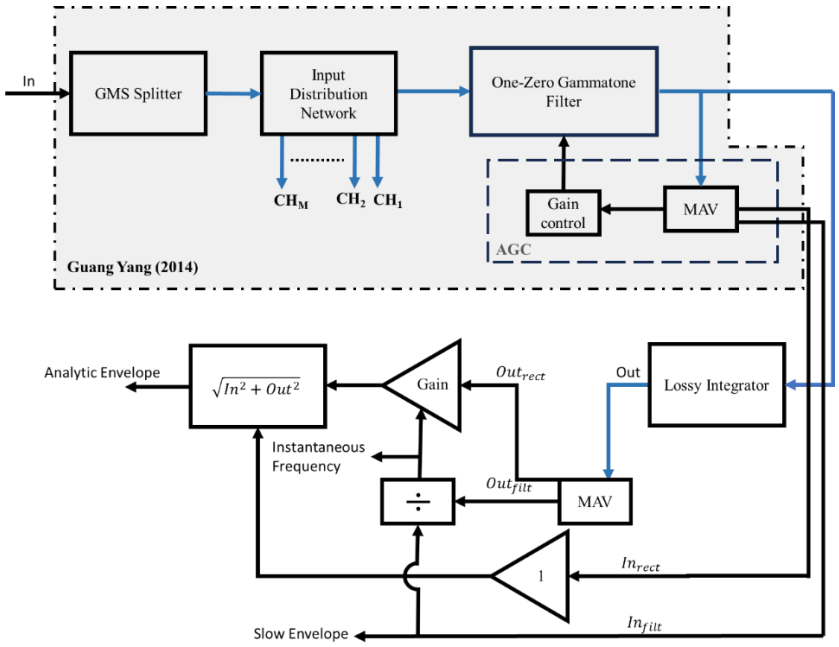


Figure 85: Top level system design of a single channel which would constitute the all-in-one CI processor by incorporating this work.

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