High Linearity Millimeter Wave Power Amplifiers with Novel Linearizer Techniques

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Abstract

Millimeter-wave communications have experienced phenomenal growth in recent years when limited frequency spectrum is occupied by the ever-developing communication services. The power amplifier, as the key component in the transmitter/receiver module of communication systems, affects performance of the whole system directly and receives much attention.

For minimized distortion and optimum system performance, the non-constant envelope modulation schemes used in communication systems have challenging requirements on linearity. As linearity is related to communication quality directly, several linearization techniques, such as predistortion and feedforward, are applied to power amplifier design. Predistortion method has the advantages over other techniques in relatively simple structure and reasonable linearity improvement. But current predistortion circuits have quite limited performance improvement and relatively large insertion loss, which indicate the need for further research. In most of millimeter-wave amplifier design, great effort has been spent on output power or gain, while linearity is often ignored. As almost all the predistortion circuits operate at the RF frequencies, the linearized millimeter-wave communication circuit is still relatively immature and very challenging.

This project is dedicated to solve the linearity problem faced by millimeter-wave power amplifier in communication systems, which lacks of effective techniques in this field. Linearity improvement with the predistortion method will be the key issue in this project and some original ideas for predistortion circuit design will be applied to millimeter-wave amplifiers.

In this thesis, several predistortion circuits with novel structure were proposed, which provide a new approach for linearity improvement for millimeter-wave power amplifier. A millimeter-wave power amplifier for LMDS applications built on GaAs pHEMT technology was developed to a high engineering standard, which works as the test bench for linearization. Actual operation and parasitic elements at tens of gigahertz have been taken into consideration during the design.

Firstly, two novel predistorter structures based on the amplifier were proposed, one is based on an amplifier with a fixed bias circuit and the other is based on an amplifier with a nonlinear signal dependant bias circuit. These novel structures can improve the linearity while improving other metrics simultaneously, which can effectively solve the problem of insertion loss faced by the conventional structures. Besides this, an original predistortion circuit design methodology derived from frequency to signal amplitude transformation was proposed. Based on this methodology, several transfer functions were proposed and related predistortion circuits were built to linearize the power amplifier. As this methodology is quite different from the traditional approach, it can improve the linearity significantly while other metrics are affected slightly and has a broad prospect for application.

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List of Terms and Abbreviations

ACPR	Adjacent Channel Power Ratio
ADS	Advanced Design System
ATM	Asynchronous Transfer Mode
CPE	Customer Premises Equipment
CPW	Coplanar Waveguide
DC	Direct Current
DOE	Design of Experiments
DUT	Device Under Test
EDA	Electronic Design Automation
EMI	Electromagnetic Interference
EDA	Electronic Design Automation
FBP	Fixed Bias Predistortion circuit
FCC	Federal Communications Commission
FET	Field Effect Transistor
FFT	Fast Fourier transform
FSK	Frequency Shift Keying
GaAs	Gallium Arsenide
GMSK	Gaussian Minimum Shift Keying
HBT	Heterojunction Bipolar Transistor
HEMT	High Electron Mobility Transistor
HJFET	HeteroJunction Field Effect Transistor
IDU	In-Door Unit
IF	Intermediate Frequency
IMD3	the Intermodulation Distortion from the 3rd harmonic
InP	Indium Phosphide

IP3	The third-order Inter-concept Point
ISM	Industry Science and Medicine
LMDS	Local Multi-point Data Service
LNA	Low Noise Amplifier
LUP	Look-Up Table
MBE	Molecular Beam Epitaxy
MIM	Metal Insulator Metal
MMIC	Monolithic Microwave Integrated Circuit
NBP	Nonlinear Bias Predistortion circuit
ODU	Out-Door Unit
OIP3	Output Third-Order Intercept Point
OQPSK	Offset QPSK
PA	Power Amplifier
PAE	Power Added Efficiency
PD:	PreDistortion circuit
pHEMT	pseudomorphic HEMT
PRC	Passive RC predistortion circuit
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RFC	RF Choke
SiGe	Silicon Germanium
TEM	Transverse Electro Magnetic
T/R	Transmitter/Receiver
V Band	50 to 75 GHz
W Band	75 to 110 GHz
W-CDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network
X Band	8.0 to 12.0 GHz

Chapter 1

INTRODUCTION

1.1 Millimeter-wave System

The term millimeter-wave system is generally applied to circuits and systems that operate in the frequency range between 30 and 300 GHz where the wavelength is of the order of a millimeter [1]. There is a massive amount of spectrum available in these high frequencies and this makes the millimeter-wave frequency range quite attractive. This naturally lends itself to systems demanding wide bandwidths which cannot be simply fulfilled by modifying the lower frequency techniques. On the other hand, some parts of the millimeter-wave range have specific propagation characteristics. A case in point is the frequency band around 60 GHz which is the frequency of interest for the fourth-generation communication. The inherent high atmospheric attenuation makes this region of the spectrum very useful for short-hop communications links, which are naturally secure and suitable for extensive use with a low likelihood of interference with frequency re-use [2–12].

Due to the excess in demand and limited amount of available frequency spectrum, band of interest has extended to millimeter-wave frequencies as communication channels are becoming crowded rapidly. This push towards increased bandwidth usage presents a need for increased bandwidth efficiency in order to increase system capacities [13].

1.2 The Problem Caused by the Distortion

The purpose of the power amplifier is to boost the radio signal to a sufficient power level for transmission through the air interface from the transmitter to the receiver. As the final functional block in the transmit path, the power amplifier is one of the key components in the transmitter/receiver module of communication system and affects performance of the whole system directly. Power amplifier can be categorized either as bias point dependent, such as Class A, B, AB and C, or depending on the passive elements in the output matching network that shape the drain voltage and current, provided that the transistor in this case operates as a switch such as Class D, E and F [14]. The power added efficiency(PAE) of switched amplifier can reach up to 100% in theory while traditional Class AB amplifier can only reach 78.5% and Class A amplifier can obtain 50% at most though Class A amplifier has the best linearity. The selection of the class depends primarily on the particular application and in this project Class AB is preferred because of its compromise between linearity and efficiency and its wide acceptation.

When a signal with a varying envelope passes through a nonlinear amplifier, the performance of the communication system will be deteriorated. As a result of the distortion generated by the amplifier, the spectrum of the signal will expand into adjacent channels causing interference for other users. The distortion will make it difficult or even impossible for the receiver to detect the information correctly. For minimized distortion and optimum system performance, the non-constant envelope modulation schemes used in communication systems have challenging requirements on linearity. This, together with the high efficiency requirement for mobile applications, has been the goals people pursue both in the industrial and academic fields. One of the solutions is to employ more bandwidth efficient modulation schemes, which in turn require highly linear amplification throughout communication architectures. Constant envelope modulation schemes such as Frequency Shift Keying (FSK) or Gaussian Minimum Shift Keying (GMSK) may be used, but a major drawback with them is an inefficient use of the spectrum [15]. To utilize the frequency spectrum better, higher order modulation schemes such as Quadrature Phase Shift Keying (QPSK), Offset QPSK (OQPSK) are generally favored for their efficient use

of bandwidth [15]. Such spectrally efficient modulation techniques have a varying phase, which are susceptible to nonlinearities in the radio.

For most applications linear amplification is necessary throughout the transmit and receive portions of the system to decode modulated signals accurately. Linear amplification is associated with low power efficiency making it unsuitable for battery-operated mobile equipments. Power efficiency is especially important for mobile equipments as the power amplifier is one of the most power consuming components. Typically a high efficiency, saturating amplifier is simply backed-off from the compression point to an input power point that exhibits the required linearity. However, the cost associated with this is very high as a higher power amplifier has to be employed. The higher power amplifier must be operated at a lower power output, which may require additional amplifier stages, driving up the overall system cost.

The nonlinear operation of high efficiency amplifiers is detrimental to a signal containing any envelope information. Any amplitude or phase distortions on the signal may reduce the ability to decode these signals properly. If some form of linearization technique could be applied to a nonlinear amplifier to realize a high linearity, significant cost could be saved while maintaining a decent efficiency.

Several linearization techniques exist such as feedback technique, feedforward technique and one of them, predistortion technique will be investigated in this thesis. Predistortion is the method where the gain compression and phase expansion of the nonlinear amplifier are compensated by the inverse characteristics of a predistorter before the signal enters the amplifier. Among the available linearization techniques, predistortion, compared with other techniques, has the advantages of low complexity and low cost. The architecture gives the technique some competitive properties: 1) the correction is applied before the power amplifier where insertion loss is not as critical; 2) the correction architecture is less bandwidth limited than other approaches, such as feedforward [16]. Due to these virtues, the predistortion technique is applied in high performance power amplifier design at RF frequencies [16–25] and is expected to be a good solution for the millimeter-wave applications.

1.3 Motivation

The phenomenal development of millimeter-wave communications such as the fourth-generation communication, Local Multi-point Data Service (LMDS) stimulates an increasing demand for high performance circuits such as millimeter-wave power amplifier, which in turn promotes intensive research in related research areas.

Although millimeter-wave communication systems have challenging requirements on linearity, people up to now, have not paid much attention to this as the subject is still relatively immature and very challenging. There is therefore a need to investigate new design methods to improve linearity with predistortion technique for millimeter-wave power amplifiers.

1.4 Objectives

The predistortion circuit research for millimeter-wave power amplifier is still relatively new in the field of millimeter-wave circuit research. Although many obstacles need to be circumvented, recent publications [16–25] have demonstrated the possibility to implement the predistortion circuit for millimeter-wave power amplifiers. As a result, it is worthwhile to devote effort to explore the area.

This project is dedicated to solve the linearity problem for millimeter-wave power amplifiers in communication systems, which is lack of effective techniques in this field. Linearity improvement with the novel predistortion circuit will be the key issue in this project and some original ideas for predistortion circuit design will be applied to millimeter-wave amplifiers.

1.5 Overview of the Thesis

In this thesis, predistortion technique was investigated in depth and a series of design methodologies were proposed, which provide a new approach for linearity improvement for millimeter-wave power amplifiers.

Firstly a millimeter-wave power amplifier for LMDS applications built on OMMIC GaAs pHEMT technology was developed to a high engineering standard, which works as the test bench for the predistortion circuit research.

With this test bench, two novel predistorter structures based on amplifier were proposed, one is based on an amplifier with a fixed bias circuit and the other is based on an amplifier with a nonlinear signal dependant bias circuit. Besides these two novel structures, an original predistortion circuit design methodology derived by applying frequency to signal amplitude transformation to a passive network was proposed. Based on this methodology, several predistortion circuits were designed to linearize the test bench. Excellent performance improvements have been achieved by simulation using ADS, which demonstrates that the predistortion circuit design methodologies proposed in this thesis are a promising solution for linearity improvement for millimeter-wave power amplifiers.

This thesis is organized as follows: Chapter 2 presents an overview of LMDS system and millimeter-wave power amplifier design methods, which are necessary for further work. Chapter 3 gives an overview of MMIC enabling device technologies including active devices and passive devices. Suitable technologies are selected for the future research. In Chapter 4, a millimeter-wave power amplifier for LMDS applications was developed as the test bench for predistortion circuit research and a detailed design process is explained. In Chapter 5 some linearization techniques, especially the principle of predistortion technique are introduced and some existing linearizers are reviewed and evaluated. The novel predistortion circuit structure based on an amplifier with a fixed bias circuit is proposed in Chapter 6 and the novel predistortion circuit structure based on an amplifier with a nonlinear signal dependant bias circuit is proposed in Chapter 7. The predistortion circuit design methodology derived from frequency to signal amplitude transformation is discussed in detail in Chapter 8. The conclusions of this project and the plan for the future work is given in Chapter 9.

1.6 Statement of Originality

The main original contributions of the project presented in this thesis fall into several categories summarized below. More detailed contributions are given in the introduction section of each chapter.

- A novel predistortion circuit structure based on an amplifier with a fixed bias circuit in Chapter 6.
- A novel predistortion circuit structure based on an amplifier with a nonlinear signal dependant bias circuit in Chapter 7.
- The predistortion circuit design methodology derived from frequency to signal amplitude transformation applied to a passive network in Chapter 8.
- Several novel predistortion circuits based on the design methodology derived from frequency to signal amplitude transformation in Chapter 8.
- Part of the work on the design methodology derived from frequency to signal amplitude transformation has been published at European Conference on Circuit Theory and Design 2007 [26].

Chapter 2

OVERVIEW OF MILLIMETER-WAVE POWER AMPLIFIER DESIGN

2.1 Introduction

In this chapter, a review of LMDS system and the general background on millimeter-wave power amplifier design will be introduced. Related design methods including wide-band amplifier design methods, load-pull and source-pull design methods, network analyzer and spectrum analyzer measurement, and the metrics of millimeter-wave power amplifier will be presented briefly.

2.2 Review of LMDS System

The Local Multi-point Data Service (LMDS) system is a broadband wireless point-to-multipoint communication system that operates typically in the 24∼31GHz range, providing two-way voice, data, internet and video services. In the US, a total of 3.8 GHz of spectrum between 27.5 GHz and 31.3 GHz was auctioned out. Other bands are also allocated for point-to-multipoint systems at 24 GHz and 39 GHz. For instance, the 24 GHz

band is allocated for LMDS services in Germany, while Korea and Japan use frequencies from 22 GHz to 28 GHz [28–31].

LMDS systems employ a cellular-like network architecture similar to mobile networks, which consists of low-power transmitters and provides transmission to the subscribers as shown in Figure 2.1. Current LMDS systems are able to offer data rates of up to 622 Mbps at the expense of dedicating a large chunk of allocated spectrum (100-112 MHz) to a single subscriber [31]. However, in general, service providers will offer data rates of around 10 Mbps because of the need to maximize the number of subscribers given a finite band of spectrum [31].

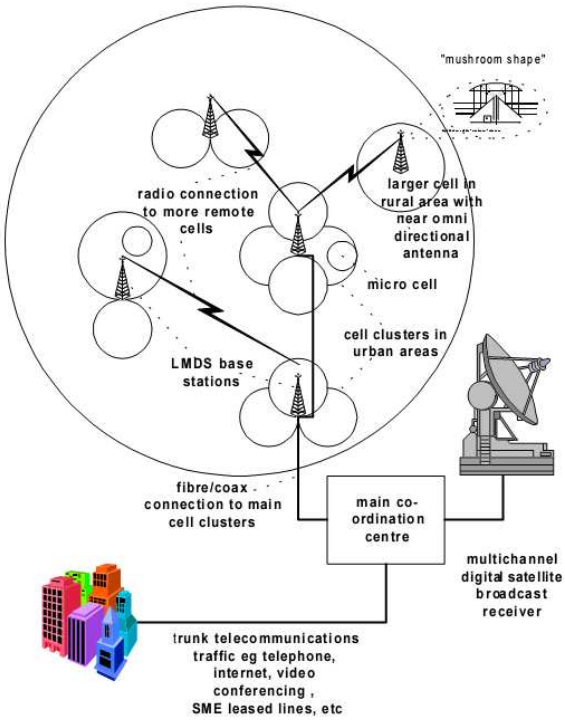


Figure 2.1: LMDS system architecture [32]

The modulation schemes available differ primarily in how efficient they are at using available spectrum. Quadrature Phase Shift Keying (QPSK) and Quadrature Amplitude Modulation (QAM) are the common modulation schemes used in the LMDS systems, and determine the capacity and distance of the link. QPSK provides 1.5 bits per second per Hz, whereas 64-QAM pumps out 5 bits per second per Hz. The radius of an LMDS cell can range from 2.5km to 10km depending on the modulation scheme used and the climate of the

region where it is deployed [29]. These modulation schemes require extremely linear power amplification while existing linearization techniques are laid behind the requirements. Existing millimeter-wave power amplifiers can provide excellent output power but the linearity still needs to be further improved, which is the subject of the project.

LMDS needs up-link (from the subscriber to the base station) and down-link (from the base station to the subscriber) wireless connections with separate frequency bands if it is used as a two-way communications system. There needs to be some spacing between these two bands in order to avoid frequency interference. In a typical analog FM system operating in 27.5∼29.5 GHz, 20-MHz-wide channels are used to broadcast video. Digital QPSK systems typically use 40-MHz channels to provide high-capacity data transfer [35]. The up-link radio frequency power is much smaller than that of the down-link. There are two ways of separating the up-link connection from the down-link connection. With Time Division Duplexing (TDD), the subscriber and the base station take turns talking to each other. At any time, both parties will use the entire spectrum allocated for that link. On the other hand, with Frequency Division Duplexing (FDD), the up-link and the down-link use different frequency bands separated by a large guard band to avoid interference. Most research work has been focused on maximum output power handling capacity for the Ka-band LMDS down-link communications [28].

There are four main elements in the LMDS network architecture, namely the base station equipment, RF equipment, Customer Premises Equipment (CPE) and network management system [31]. The base station equipment typically consists of a network interface and a modem unit. The base station is the gateway between the wireless and wireline networks, and an Asynchronous Transfer Mode (ATM) switch typically provides the connectivity. The functions of modem include multiplexing, randomization, encoding and modulation for downstream data, and the inverse operations for upstream data. It is connected to the RF equipment through the IF interface. The RF equipment is constituted by up/down conversion chains, high power amplifier, low noise amplifier and filters. The high frequency band leads to significant line attenuation, so the RF elements are located close to the antenna. The CPE contains an out-door unit (ODU) and an in-door unit

(IDU). The ODU includes a 10 to 12 inch antenna and the RF unit. The CPE IF interface connects the ODU to the IDU. The network management system monitors the health and performance of the LMDS system by means of the agent applications and management application. It covers the operations, administration, maintenance and provisioning of the network.

For LMDS applications, Siddiqui *et al.* [32] presented a high power and high efficiency monolithic power amplifier, which produced small-signal gain of 16 dB, PAE of 35%, and P_{1dB} of 32 dBm from 27.5 GHz to 29.5 GHz using 0.15 μm GaAs pHEMT. Satoh *et al.* [38] presented a K-band high-power MMIC amplifier module using GaAs pHEMT technology. This power amplifier delivered a total gain of 30 dB and a P_{1dB} of 33.5 dBm with PAE of 16% between 23 GHz and 26 GHz. Some already published power amplifiers for LMDS applications are listed in Table 2.1.

Table 2.1: Some published PA for LMDS applications

Frequency Band	Process Technology	Small Signal Gain	P_{1dB}	PAE	Ref
27.5∼29.5 GHz	0.15 μm GaAs pHEMT	16 dB	32 dBm	35%	[28]
24∼28 GHz	0.15 μm GaAs pHEMT	16.7∼18.6 dB	17.5 dBm	19.8%	[34]
27.5∼28.4 GHz	0.15 μm GaAs pHEMT	23 dB	33 dBm	N/A	[36]
25.7∼31.15 GHz	Packaged components	9 dB	27 dBm	15.3%	[37]
23∼26 GHz	0.25 μm GaAs pHEMT	29 dB	33 dBm	16%	[38]

2.3 Review of Power Amplifier Design

2.3.1 Wide-band Amplifier Design

In communication systems, wide-band is a term used to describe a relatively wide range of frequencies in a spectrum. A system is typically described as wide-band if the range of frequencies used for transmission is greater than 0.1 % of the midband frequency [33]. In the LMDS wide-band system, the frequency band covering 27 to 30 GHz, will be

used in this project. In wide-band amplifier design the following architectures and design methods are widely used.

2.3.1.1 Reactively Matched Amplifier

Reactive matching is a design method in wide-band amplifier design and its basic architecture is shown in Figure 2.2. Lossless matching networks, with either lumped or distributed elements are employed in this structure [39]. By selectively creating reflections between the matching network and the active device, gain compensation can be realized to flatten the FET's gain roll off [40]. In practice, the input matching network can be optimized for maximum gain, and the output matching circuit can be optimized for maximum output power or power-added efficiency.

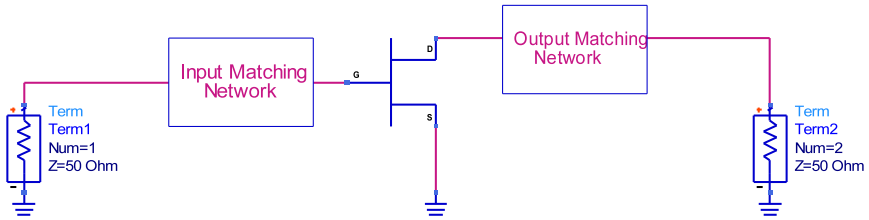


Figure 2.2: Reactively matched amplifier

The lossless matching circuits provide the desired match over a narrow band of frequencies. The main disadvantage is its relatively poor impedance match over a wide frequency band, though the lossless matching circuits can provide the desired match over a narrow band of frequencies [40].

Tserng, *et al.*[26], reported the first reactively matched 2 to 18 GHz power amplifier employing GaAs MESFET devices. The amplifier was designed using wide-band impedance transformers realized in MMIC, and it achieved average power-added efficiency in the range of 8% to 15% with an output power of 23 dBm. Palmer, *et al.* [40], produced the first reactively matched MMIC multi-octave power amplifier operating over the frequency range of 6 to 18 GHz. The amplifier achieved an output power of 27 dBm with an average power-added efficiency of 19%.

2.3.1.2 Feedback Amplifier

Feedback amplifier is a conventional amplifier topology, which can increase the bandwidth with a simple configuration. The feedback path may be comprised of resistor, capacitor and inductor as shown in Figure 2.3, in which the resistor controls the gain and bandwidth of the amplifier, the inductor can be adjusted to compensate for a fall in device gain at higher frequencies and extend the bandwidth, the capacitor is used to isolate the gate from the drain bias supply. In practical applications, not all these elements are required simultaneously according to the requirements. This structure allows wide-band amplification and can be designed for a measure of robustness against process variations, but these merits come at cost of higher noise and reduced gain [10, 12, 44].

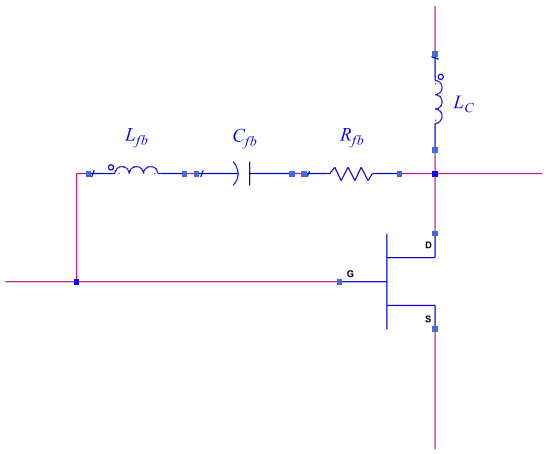


Figure 2.3: Feedback amplifier structure

Negative feedback amplifier has the following merits [44, 45]:

- It can offer gain equalization over a fairly wide bandwidth.
- It can improve the $|S_{21}|$ at the highest frequencies, compared with the bare FET.
- The matching can be improved concurrently with above, thus simplifying the task of matching network design.
- It reduces the sensitivity of the overall circuit to process deviations.

However, the loss associated with the feedback resistor can lead to the erosion of the output power and noise figure over the lower end of the frequency band. The characteristic of low gain in a millimeter-wave power amplifier makes this technique difficult to apply effectively.

2.3.1.3 Balanced Topology

The balanced architecture is one of the most popular topologies for wide-band amplifier design. It consists of two nominally identical amplifiers between a pair of quadature couplers as shown in Figure 2.4. This architecture can achieve an excellent match over about an octave bandwidth with reasonable gain [39, 44]. As any reflections of an incident signal at the input due to the poor match will be channeled back through the input Lange coupler to the 50 Ohm source where they will be absorbed, the result is that the balanced amplifier has excellent input and output matches, and the designer is free to optimize the amplifier for stability, flat gain and noise figure.

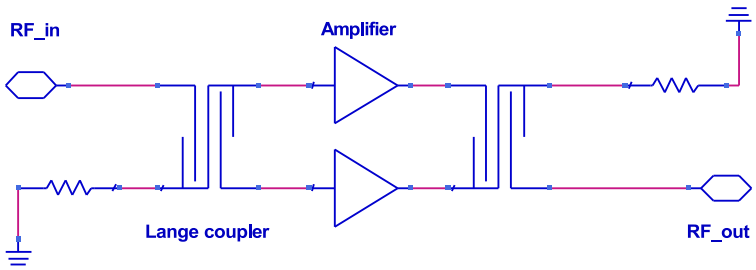


Figure 2.4: Balanced amplifier structure

Many benefits can be achieved from this topology with respect to an unbalanced amplifier [39, 40, 44–47]:

1. More freedom: The individual amplifier stage can be optimized for gain flatness or noise figure, without concern for input and output matching.

2. Better matching and stability: Reflections are absorbed in the coupler terminations, improving input/output matching as well as the stability of the individual amplifiers.

3. Higher gain: Maximum output power is 3dB higher and 1dB compression is

improved by approximately 3dB.

4. Improved robustness: The circuit provides a graceful degradation of a 6 dB loss in gain if a single amplifier section fails.

5. Wider bandwidth: Bandwidth can be an octave or more, primarily limited by the bandwidth of the coupler.

Some shortcomings come along with these benefits [39, 40, 44]:

1. More power consumption, more area and higher cost. Compared with the single amplifier, two amplifiers in a balanced structure will consume more power, occupy more chip area, and cost will increase correspondingly.

2. Degraded noise performance. Noise figure is higher because of the coupler loss.

2.3.1.4 Distributed Topology

In principle, the distributed amplifier is based on the idea of separating the capacitances of the active devices while adding their tranconductance by means of adding additional inductance formed by artificial transmission lines [39, 40, 46]. Thus the distributed amplifier in structure consists of an input line, incorporating the input capacitances of the transistors, and an output line incorporating the output capacitances as shown in Figure 2.5. The combination of FET capacitance with the high-impedance lines resembles a lumped-element version of a 50 Ohm line, which is used to provide an impedance match at the input and output ports.

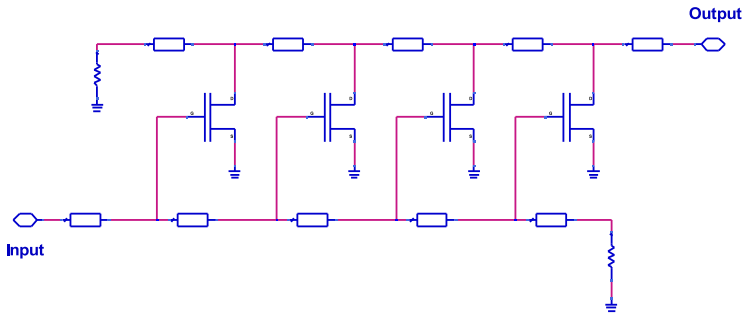


Figure 2.5: Distributed amplifier structure

In the distributed amplifier, the transmission line has shunt capacitance as well as series inductance. As the total shunt capacitance of the artificial transmission line increases, the bandwidth becomes lower than that based on ideal inductors. To minimize the reduction of the bandwidth, the transmission line should be highly inductive with small shunt capacitance [40].

In order to achieve a wide-band matching, the input and output capacitances of a number of transistors have to be incorporated into the artificial transmission line structures. The result of this arrangement is that the amplifier can operate over a very broad frequency range, from very low frequencies up to the cut-off frequency of the artificial transmission line. Generally speaking, this architecture can achieve a bandwidth more than one decade [40].

Distributed amplifiers can offer moderate gain, but the noise figure is poor. A large amount of DC power per decibel of power gain is another drawback. The load that each FET sees is not even close to optimum, and the signal distribution is such that some FETs get much greater voltage stress than others. On the other hand, its advantages include high maximum available gain, wide bandwidth, improved input-output isolation, and variable gain control capability [40, 46].

2.3.2 Review of Network Analyzer and Spectrum Analyzer Measurement

Network analyzer and spectrum analyzer are the most frequently used instruments in RFIC/MMIC measurements. In this section, the principle of these instruments will be introduced.

2.3.2.1 Network Analyzer Measurement

Network analysis is the process by which designers measure many electrical performance parameters for the components and circuits used in the complex systems.

There are two categories of network analyzers, namely scalar network analyzer

(SNA) and vector network analyzer (VNA). Scalar analyzers can only measure magnitude while vector analyzers are capable of measuring complex(magnitude and phase) reflection and transmission [49]. VNA is the most used type of network analyzer.

Figure 2.6 is the general block diagram of network analyzer, showing the major signal-processing sections [50]. In order to measure the incident, reflected and transmitted signal, four sections are required: Source for stimulus; Signal-separation devices; Receivers that downconvert and detect the signals; Processor/display for calculating and reviewing the results. They function by comparing the incident signal that leaves the analyzer with either the signal that is transmitted through the test device or the signal that is reflected from its input.

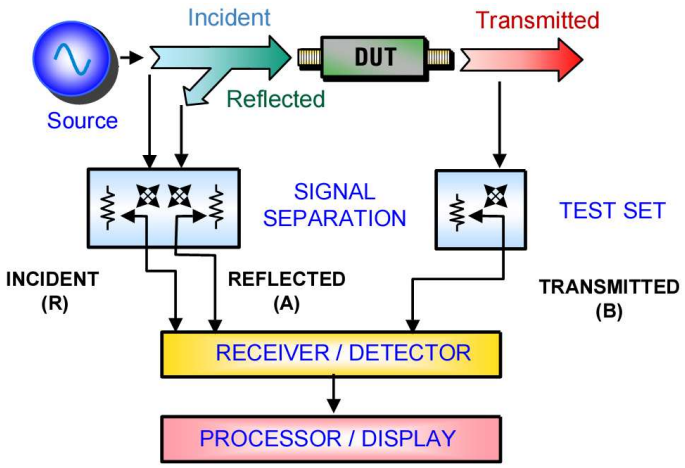


Figure 2.6: General block diagram of network analyzer [50]

Network analyzers are used to measure components, devices, circuits, and sub-assemblies. They contain both a source and multiple receivers, and generally display ratioed amplitude and phase information. A network analyzer always looks at a known signal (in terms of frequency), since it is a stimulus response system. With vector-error correction, network analyzers provide very high measurement accuracy.

A modern vector network analyzer can measure a component's magnitude, phase and group delay responses, show port impedances on a Smith chart, and with time-domain capability, show the distance from a test port to an impedance mismatch or circuit fault [50]. The metrics that can be measured by vector network analyzers include insertion loss,

return loss, and so on.

2.3.2.2 Spectrum Analyzer Measurement

Spectrum analysis primarily measures power, frequency and noise. It is concerned with signal characteristics such as carrier level, sidebands, intermodulation distortion, and phase noise [51].

Figure 2.7 is the general block diagram of spectrum analyzer, showing the major signal-processing sections [51]. Spectrum analyzers are usually configured as a single-channel receiver without a source. Spectrum analyzers generally have a wider range of IF bandwidths than most network analyzers in order to analyze diverse types of signals and are often used with external sources for nonlinear stimulus/response testing. When combined with a tracking generator, spectrum analyzers can be used for scalar component testing to show magnitude versus frequency information but not phase information [51].

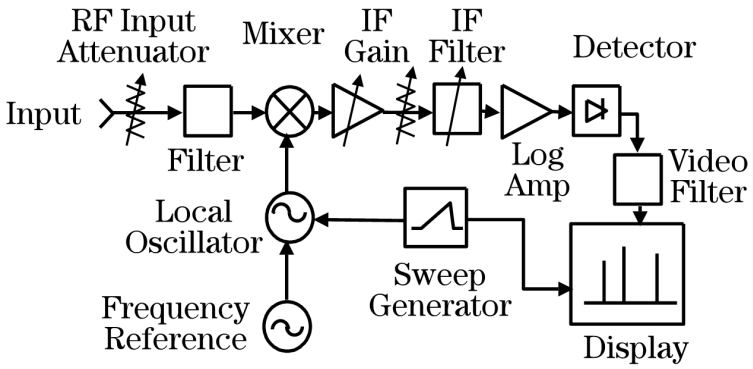


Figure 2.7: General block diagram of spectrum analyzer [51]

There are two categories of spectrum analyzers, analogue spectrum analyzer and digital spectrum analyzer. An analogue spectrum analyzer uses either a variable bandpass filter whose mid-frequency is automatically tuned through the range of frequencies for which the spectrum is to be measured or a superheterodyne receiver where the local oscillator is swept through a range of frequencies. A digital spectrum analyzer uses the Fast Fourier transform (FFT), a mathematical process that transforms a waveform into the components of its frequency spectrum [52].

Spectrum analyzers can make distortion measurement, modulation measurement, pulsed RF measurement, noise measurement, and electromagnetic interference (EMI) measurement [51]. The metrics that can be measured by spectrum analyzers include P_{sat}, P_{1dB}, $IP3$, $IMD3$ and so on [52].

Spectrum analyzers measure unknown external signals. This contrasts with network analyzers which utilize synthesized-frequency sources to provide a known test stimulus that can sweep across a range of frequencies or power levels [51].

2.3.3 Review of Load-Pull and Source-Pull Methods

Power amplifier design requires device models to be as accurate as possible and large-signal measurements are needed to characterize the large signal performance of devices. Load-pull is one of the most convenient methods to determine large-signal parameters. Designers can use the results of load-pull measurements directly to design matching networks, or confirm existing large-signal models.

Load-pull and source-pull measurements are primarily used to determinate experimentally the performance of a device under large-signal conditions and identify the conditions that yield the optimum results. With CAD software, load-pull and source-pull can also be computed with the advantage of fast tuning. But this requires that accurate large-signal device models be available.

In load-pull measurements as shown in Figure 2.8, the impedance seen by the output port of an active device is varied and one or more performance parameters are measured. Typical performance parameters of interest for power amplifier are large-signal output match, output power, power gain, efficiency and distortion. These performance parameters are evaluated as functions of input and output complex loads, bias point and input power.

On a Smith chart the contours of the load impedances that result in the maximum and other prescribed values of gain and output power are plotted. This can be used to select a load impedance that represents the best trade-off of parameters such as between gain and output power [53]. Unlike network analyzer measurement, load pull measure-

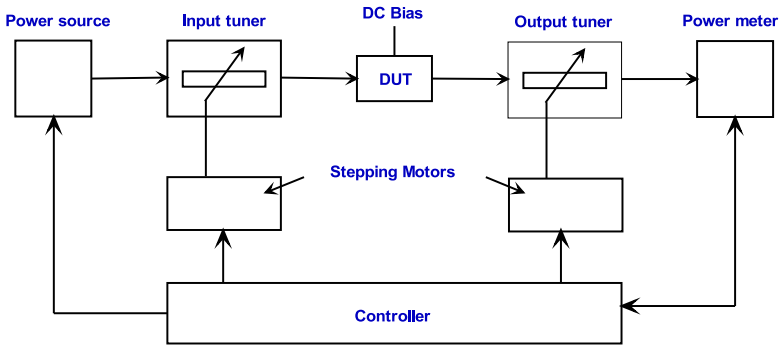


Figure 2.8: Typical load pull configuration [55]

ments can make a lot of measurements at a single frequency and then move on to another frequency [54].

In the source-pull method, the impedance seen by the input of an active device is varied and performance parameters are measured. Noise figure and gain are among the performance parameters of interest [53].

In power measurements, the input impedance is tuned to a single location that provides good power gain, while the output is swept all over the Smith chart. In noise parameter extraction, the output is load-pulled to an impedance that provides good gain, then the input is swept over all the Smith chart [54]. Examples of the use of load-pull, source-pull and the other measurement techniques discussed in this chapter will be given in Chapter 4.

2.4 Review of Millimeter-wave Power Amplifier Metrics

Several metrics are used to describe the performance of millimeter-wave power amplifier including P_{1dB}, $Gain$, power-added efficiency (PAE), K factor, the third-order interconcept point ($IP3$) and $IMD3$. In this section, the concepts of these metrics will be introduced.

- *Gain.* Two kinds of gain are commonly employed, namely small signal gain and large signal gain. Small signal can be expressed as

$$Small\ Signal\ Gain = |S_{21}|^2, \tag{2.1}$$

where S_{21} is the forward S-parameter.

Large signal gain, or power gain can be expressed as

$$Power\ Gain = \frac{P_{out}}{P_{in}}, \tag{2.2}$$

where P_{out} is the output RF power, P_{in} is the input RF power.

- Saturated output power, P_{Sat}. When the output power reaches to a certain level, it will not increase with input power any more. The corresponding output power is called saturated output power, P_{Sat} as shown in Figure 2.9.

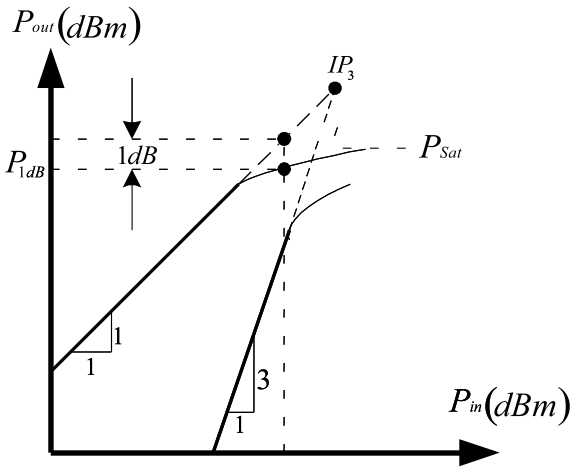


Figure 2.9: Input-output relationship for nonlinear power amplifier

- P_{1dB}. P_{1dB} is the output power level at which the amplifier's gain is compressed by 1 dB relative to the small signal gain as shown in Figure 2.9.

- PAE. Power-added efficiency, PAE is an important metric to describe a power amplifier's efficiency. It includes not only the capability of converting DC power to microwave power, but also the capability of amplification of microwave power. It is defined as

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}}, \tag{2.3}$$

where P_{out} is the output RF power, P_{in} is the input RF power, P_{DC} is the DC power.

- K factor. K factor, also known as Rollet's stability factor, is defined as

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 - \Delta^2}{2|S_{12}S_{21}|}, \tag{2.4}$$

where $\Delta = S_{11}S_{22} - S_{12}S_{21}$ [87].

When $K > 1$ and $|\Delta| < 1$ are met simultaneously, the amplifier is deemed to be unconditionally stable. That is, the amplifier is stable for terminations at both ports within the whole Smith chart at the given frequency and bias condition.

- MAG. Maximum available gain, MAG, is the maximum gain that can be obtained when Rollet's stability factor is greater than unity. MAG is defined as

$$MAG = \left|\frac{S_{21}}{S_{12}}\right| (K - \sqrt{K^2 - 1}), \text{ when } K > 1, \tag{2.5}$$

where K is Rollet's stability factor. It is shown in Figure 2.10.

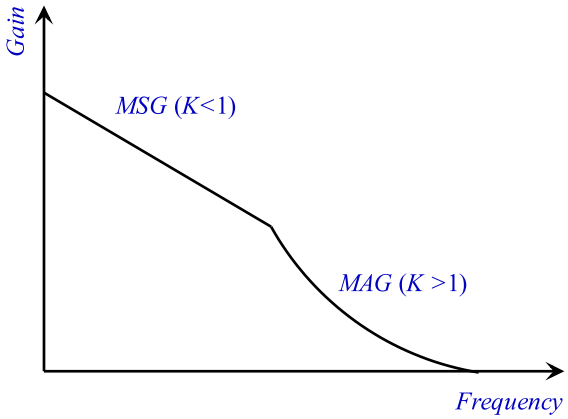


Figure 2.10: MAG/MSG **illustration**

- MSG. Maximum stable gain, MSG, is the maximum gain that can be obtained when Rollet's stability factor is less than unity. MSG is defined as

$$MSG = \left|\frac{S_{21}}{S_{12}}\right|, \text{ when } K < 1. \tag{2.6}$$

It is shown in Figure 2.10.

- $VSWR$. Voltage standing wave ratio, $VSWR$, can be expressed as below,

$$VSWR_{in} = \frac{1 + |S_{11}|}{1 - |S_{11}|}, \tag{2.7}$$

$$VSWR_{out} = \frac{1 + |S_{22}|}{1 - |S_{22}|}. \tag{2.8}$$

Under the fully matched conditions, $VSWR$ is equal to one; Under the extreme conditions such as the open-circuit and short-circuit, $VSWR$ approaches infinite.

- $IP3$. The third-order inter-concept point, $IP3$, is the point at which the fundamental output power and third-order distortion output lines intercept as shown in Figure 2.9. $IP3$ is commonly used as a figure-of-merit for linearity for small signal amplifier such as LNA.

- $IMD3$. $IMD3$ is the intermodulation distortion from the third-order nonlinearity as shown in Figure 2.11. $IMD3$ can be used as a figure-of-merit for linearity evaluation for most of applications.

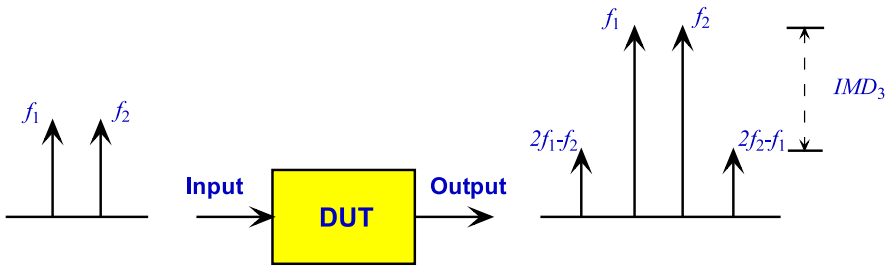


Figure 2.11: $IMD3$ **illustration**

2.5 Summary

In this chapter, the general background for millimeter-wave power amplifiers was introduced. Wide-band amplifier design methods, some measurement techniques and the metrics of millimeter-wave power amplifier were discussed briefly. In the next chapter, MMIC device technologies including active devices and passive devices will be introduced. Suitable device technologies will be selected for the research work.

Chapter 3

REVIEW OF MMIC DEVICES

3.1 Introduction

The performance that is achieved by a MMIC depends highly on its building blocks, including active devices and passive elements. In this chapter, MMIC enabling technologies will be introduced and compared. Suitable technologies will be selected for the research work.

3.2 Active Device Technologies

MMIC enabling technologies mainly include devices based on SiGe, GaAs and InP substrates. Depending on the figures of merit such as cut-off frequency, they occupy different frequency bands. For millimeter-wave circuit design, several properties are expected, such as high cut-off frequency, high power density, relatively high breakdown voltage, and low noise characteristics. Key circuit performance parameters include power gain, output power and power added efficiency (PAE), which correspondingly relate to some device parameters such as the maximum operating voltage and current handling capability [56, 57].

3.2.1 GaAs HEMT

Benefiting from mature technologies and ever-decreasing cost, the GaAs HEMT has has been the first choice for millimeter-wave circuits [40, 46]. A photo of a typical GaAs HEMT is shown in Figure 3.1 [56].

The low-noise and high frequency properties make HEMT ideal for low-noise millimeter-

wave amplifiers. HEMT devices also exhibit excellent power performance, which together with good linearity and PAE makes HEMT devices also suitable for power applications. Also a very low turn-on resistance makes HEMT attractive in switch module application.

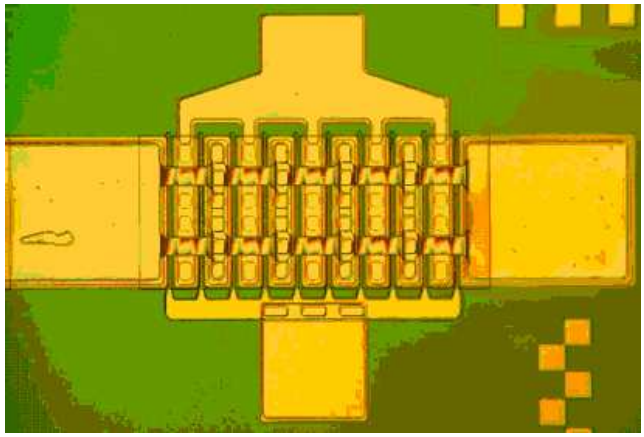


Figure 3.1: Photo of a GaAs HEMT [56]

In the micro-processing field, 0.15μm-0.1μm gate technology is widely accepted in commercial designs [28, 34–38]. Achievable f_T values with different substrates are shown in Figure 3.2.

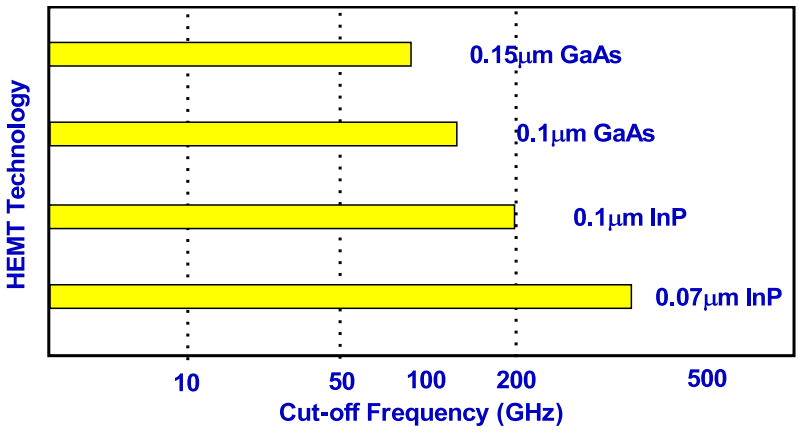


Figure 3.2: HEMT device technology [57]

The disadvantages of HEMT devices include the need for E-beam technology to realize ultra-thin gate length, which will lower the productivity and increase the cost. Another drawback is that in the practical circuit design, positive and negative voltages are required simultaneously, which will increase the complexity of the design.

3.2.2 InP HEMT

The InP-based HEMT has demonstrated top performance including very high gain, high cut-off frequency, extremely low noise figure, high maximum current density, and high substrate thermal conductivity and is therefore very attractive for the millimeter-wave applications, especially for W-band and above. But the high cost and the extremely brittle wafer have to be taken into consideration, although these are expected to improve. Low breakdown voltage also affects its use in power applications.

The InP HEMT is widely adopted in W-band or above due to its unique characteristics [58–62]. Current designs are mainly based on 0.15μm (for PA) [63–65] or 0.1μm (for LNA) T-gate technology [66,67]. High-gain InP HEMT MMICs have been realized at frequencies above 140 GHz [60] and an InP-based LNA operating at 155 GHz with 5.1dB noise figure has been reported [61]. A commercial InP HEMT design kit that can reach 180 GHz is available [71].

3.2.3 SiGe HBT

Though HEMT technology has been the first choice in the millimeter-wave circuit field, several novel technologies have challenged its position. SiGe device is a case in point and the HBT implemented using SiGe is another promising candidate for millimeter-wave circuits [57]. Advanced MBE technology and an ever-improving lithography technique have substantially improved its frequency characteristics. The extreme speed SiGe technology can offer and a low noise capability demonstrated will enable revolutionary advances in high-performance communication systems. The most obvious advantage is the substantially reduced cost which benefits from a compatibility with high-volume silicon processes. Several more merits make SiGe very attractive:

1. Many foundry providers including IHP and IBM have managed to offer SiGe HBTs above 200 GHz [72].

2. Low noise and high transconductance make SiGe very suitable for low noise and high linearity circuit design.

3. The compatibility of the process makes SiGe technology very suitable for system level integration.

In recent years, many researchers are trying to realize millimeter-wave circuits with SiGe technology. However, many inherent problems have to be solved before this technology receives wide acceptance. These problems include:

1. A relatively low breakdown voltage greatly challenges design skills. A low breakdown voltage means that more effort should be spent on trying to obtain required output power with a quite limited voltage swing.

2. Silicon substrate, which is quite different from semi-insulating substrate such as GaAs and InP, will lead to more loss especially in millimeter wave circuits. Additional steps are needed to overcome it.

Superior performance and relatively low cost make SiGe technology now familiar to designers. Many circuits based on SiGe technology have been reported and the frequency ranges cover from X band to W band [73, 74]. The use of SiGe as a replacement has been widely accepted.

3.2.4 Comparisons between Devices

Different technologies are chosen in the applications depending on the properties required. The low-noise and high frequency properties of HEMT make it ideal for low-noise and millimeter-wave amplifiers. But due to the high $1/f$ noise corner frequencies and significantly varying DC threshold voltage characteristics, the HEMT device is not a good choice for VCO application.

For HBT devices, the high linearity and low $1/f$ noise corner frequency characteristics make them ideal for high-efficiency, high linearity power amplifier and low-phase noise VCO applications. The excellent DC current gain and threshold characteristics make them suitable for analog and digital applications [57, 62].

The SiGe heterojuncton bipolar transistor, which can be combined with high-volume, low-cost silicon manufacturing, can meet the requirements of high frequency applications up to V-band or above [73, 74]. Integration with multiple functions will have impact on wireless transceiver architectures. But the performance in term of noise figure and power is not as good as the GaAs counterpart and this should be taken into consideration in the practical design [73, 74].

3.3 Passive Device Technologies

Microstrip and coplanar waveguide are the most common distributed technologies for millimeter-wave circuits [75–79]. Related characteristics will be introduced in this section.

3.3.1 Microstrip Technology

Microstrip technology is the most widely used technology in all planar circuits, regardless of the frequency range of the applied signals. Microstrip is a strip with a width W and a thickness T on the top of a dielectric substrate that has a relative dielectric constant ε_r and a thickness h, and the bottom of the substrate is a ground plane. Its structure is shown in Figure 3.3.

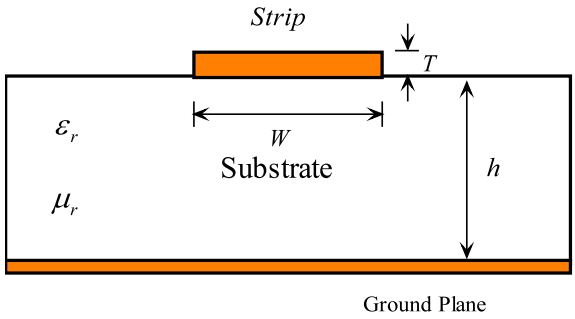


Figure 3.3: Cross-section of microstrip

As the fields in the microstrip extend within two media, the air above and the dielectric below, microstrip does not support a pure TEM wave. Propagation velocities depend not only on the material properties, but also on the physical dimensions of the microstrip. Due to the fact that the mode of propagation in microstrip is almost transverse electro-magnetic, simple approximate analysis can be performed and wide-band circuits are possible [75, 78].

The transmission characteristics of microstrip are described by two parameters, the dielectric constant and characteristic impedance. Because part of the fields from the microstrip conductor exist in air, the effective dielectric constant is less than the dielectric constant of the dielectric material separating the conductor from the ground plane.

The advantages of microstrip come from the accumulated experience which has led to a comprehensive understanding of the medium. The features of microstrip are as

follows,

1. Good layout flexibility and straightforward fabrication.

2. More EDA software support and ease of design.

The disadvantages includes:

1. Relatively large parasitic effects, especially the large parasitic inductance in the ground connection due to the viahole.

2. High radiation at millimeter-wave band. At millimeter-wave frequencies, the open stub may be regarded as an antenna which can radiate energy.

3. Characteristics are related to the thickness of the wafer, which are sensitive to process variations.

4. Low-impedance microstrip line may be impractically wide.

All these disadvantages deprive microstrip of a dominant position in V-band or higher frequency.

3.3.2 Coplanar Waveguide Technology

The conventional coplanar waveguide technology (CPW) structure consists of a center strip conductor with semi-infinite ground planes on either side as shown in Figure 3.4. CPW offers several advantages over Microstrip technology in MMIC design [77–79].

Firstly, fabrication can be simplified. Easy shunt and series surface mounting greatly improve the reliability and lowers the cost. RF grounds between tracks can make cross-talk effects between adjacent lines very weak, realizing good isolation.

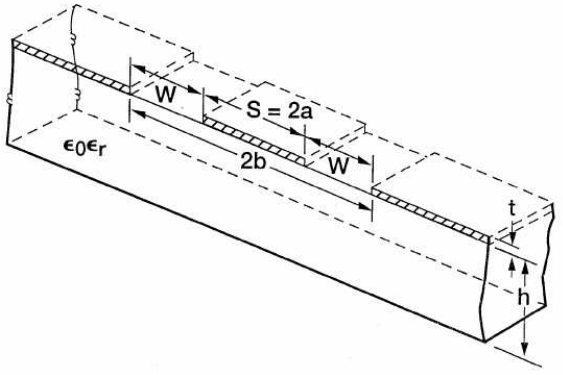


Figure 3.4: Cross-section of CPW [79]

Secondly, the need for backside processing no long exists, such as wafer thinning, via etch and backside plating. By eliminating via holes and its associated parasitic source inductance, gain can be enhanced significantly. Cost can be reduced and reliability can be improved if there is no backside processing.

Thirdly, radiation loss can be reduced. The quasi-TEM mode of propagation in CPW has low dispersion and hence offers the potential to construct wide-band circuits and components.

Furthermore as the characteristic impedance is determined by the ratio of a/b in Figure 3.4, the characteristic impedance is not sensitive to substrate thickness and considerable size reduction is possible though the penalty is higher losses.

For power amplifier design, CPW technology is highly preferred because of its low radiation loss and easy ground plane access.

There are however several disadvantages,

1. Compact circuit layout may lead to more loss, in which case CPW circuits can be lossier than comparable microstrip circuits.

2. Its effective dielectric constant is lower than that of the microstrip structure.

3. Unintended spurious transmission modes can occur. In a parallel-plate mode as shown in Figure 3.5, the substrate acts like a dielectric-filled waveguide, and EM energy propagates along unintended paths.

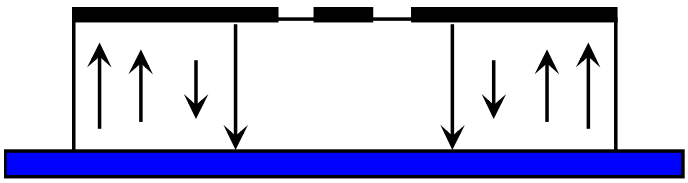


Figure 3.5: Parallel-plate mode in CPW

3.3.3 Finite Ground CPW

In most applications, a metallic plane on the substrate backside exists formed by the bottom plane of the package. This conductor backed coplanar geometry may cause undesired parasitic modes such as parallel-plate modes that cannot be suppressed by air bridges in the conventional CPW as shown in Figure 3.5. So a novel structure–finite

ground CPW (FG-CPW) was proposed to solve this problem [80, 81].

In the conventional CPW, the ground plane extends to the edge of the chip, whereas in FG-CPW, the width of the ground plain is about two to three times the width of central strip. Due to the limited size of the ground plane in FG-CPW, no parallel-plate mode is excited and consequently via-holes become unnecessary. The surface wave, which is normally induced by a large ground plane, is also eliminated. Finite ground coplanar waveguide (FG-CPW) configurations eliminate the need for backside processing (wafer thinning, via-hole) and provide ease of fabrication. Based on these properties, FG-CPW is beginning to emerge as an attractive choice for V-band circuit design [80, 81].

Unfortunately current EDA software does not give a good support for CPW, let alone FG-CPW, which greatly limits its application. In practical design, EM analysis can partly solve this problem though its very long computing time and considerable design skill needed is challenging.

3.3.4 Transmission-Line Stub

In the millimeter-wave frequency band, some lumped elements such as the inductor are no longer suitable as the working frequency approaches or exceeds the self-resonance frequency. Under such circumstance, the inductor can be replaced by a stub with proper configuration. A stub is a length of transmission line that is short- or open-circuited at one end and connected to the circuit at the opposite end. Stubs can approximate inductors, capacitors, or resonators. In most cases, stubs are used as shunt elements.

The input impedance of transmission line can be expressed as

$$Z_{in} = Z_0 \frac{Z_L \cos \beta l + j Z_0 \sin \beta l}{Z_0 \cos \beta l + j Z_L \sin \beta l}, \tag{3.1}$$

where Z_0 is the characteristic impedance, Z_L is the load impedance, β is the phase shift per unit of distance along the line, and l is the length of the transmission line [78].

For the short-circuited stub, $Z_L = 0$,

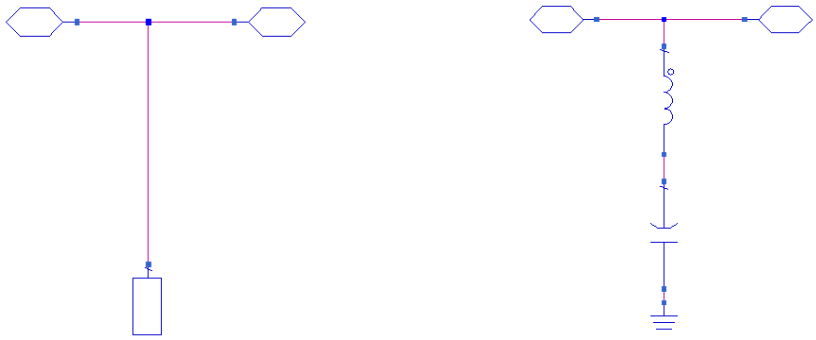
$$Z_{in} = j Z_0 \tan \beta l. \tag{3.2}$$

For the open-circuited stub, $Z_L \to \infty$,

$$Z_{in} = -jZ_0 \cot \beta l. \tag{3.3}$$

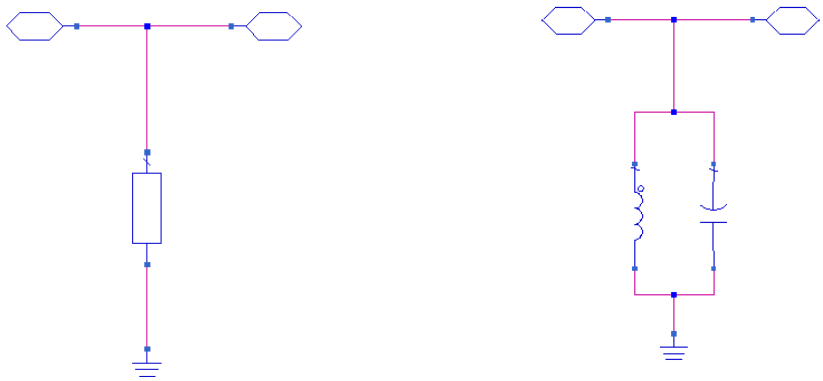
From Equation (3.2) and Equation (3.3), we can see that the short-circuited stub behaves inductively when $\beta l < \pi/2$ and the open-circuited stub behave capacitively when $\beta l < \pi/2$.

A high-impedance series line may be used as a series inductance and a low-impedance series line may be used as shunt capacitance. A quarter-wave, open-circuited stub is equivalent to a series LC resonator as shown in Figure 3.6. A quarter-wave, short-circuited stub is equivalent to a parallel LC resonator as shown in Figure 3.7 [77]. These concepts will be used to implement bias and matching networks in the Chapter 4.



(a) $\lambda/4$ open-circuited stub (b) Equivalent circuit of $\lambda/4$ open-circuited stub

Figure 3.6: $\lambda/4$ **open-circuited stub**



(a) $\lambda/4$ short-circuited stub (b) Equivalent circuit of $\lambda/4$ short-circuited stub

Figure 3.7: $\lambda/4$ **short-circuited stub**

3.4 Choice of Technology

Active devices play a key role in deciding the performance of the circuit. From the analysis of device technologies in Section 3.2.1, GaAs pHEMT technology is preferable as it can provide a balance between performance and cost for the power amplifier research. Because of its mature process technology, the transistor has a higher expansibility and the performance of the circuit can be improved with more skills correspondingly. In this project, OMMIC pHEMT 0.25 μm technology will be employed.

Passive devices are also important to the performance of the circuit, especially millimeter-wave circuit as the parasitic effects will be more prominent. As the design kit in hand does not support CPW, microstrip technology is employed in the development of millimeter-wave power amplifier for LMDS applications. The characteristics of good layout flexibility and straightforward fabrication make full use of design skills. High-impedance line and low-impedance line are widely used to realize the inductance and capacitance during the design. All the discontinuities will be verified by the EM method with the Momentum module in Agilent ADS.

3.5 Summary

In this chapter the MMIC/millimeter-wave circuit enabling device technologies and their particular advantages and disadvantages were introduced. Suitable technologies were selected for the research work. In the next chapter, a millimeter-wave power amplifier for LMDS applications will be developed and the detailed design process will be described. This amplifier will work as the test bench for the predistortion circuit research in the later chapters.

Chapter 4

MILLIMETER-WAVE POWER AMPLIFIER DEVELOPMENT

4.1 Introduction

In this chapter, a wide-band power amplifier for LMDS applications is designed as the test bench for the predistortion circuit research in the next several chapters. The power amplifier is based on cascaded structure and employs OMMIC ED02AH design kit. Practical operation and parasitic elements at tens of gigahertz have been taken into consideration to guarantee the circuit can meet stringent manufacturing requirements. Detailed design procedures will be given and key problems will be discussed in this chapter.

4.2 Amplifier Specifications

The specifications in this design were drawn up according to element limitations defined by the foundry provider [27] and the papers published [28, 34–37]. As circuit specifications are generally drawn up by the designers at system level, the specifications used in this project follow the papers [28,34–37] and are shown in Table 4.1. In Table 4.1, the bandwidth of 27∼30 GHz is defined by the LMDS standards [28]; The supply voltage of 2.0 V∼2.5V is suitable for mobile applications; The output power, power gain, linearity and PAE are consistent with the specifications [28, 34–37].

Table 4.1: The amplifier specifications

Bandwidth	27∼30 GHz
Supply Voltage	2.0 V∼2.5 V
Output Power, P_{1dB}	15∼25 dBm
Power Gain	15∼ 20 dB
Linearity($IMD3$)	Below -30 dBc@ P_{1dB}
PAE	15∼30% @ P_{1dB}
Device and Technology	GaAs pHEMT and Microstrip

4.3 Design Guidelines

According to the specifications in Table 4.1, the following guidelines will be adopted:

1. From the requirements, the circuit should have at least two stages, as a single stage cannot meet the requirement of power gain. The first stage will be designed for maximum gain and the final stage will be designed for maximum output power.

2. The input matching network will be designed for maximum gain using source-pull method, while the output matching network will be designed with load-pull method for maximum output power. The inter-stage matching network will work as an impendence transformer between stages.

3. Drain bias networks should provide a power supply with a wide low-impedance line in order to cope with the bias current, while gate bias networks can be realized with a thin high-impedance line.

4. The circuit is based on microstrip technology. All the discontinuities should be verified by the EM method. Robustness issue should be taken into consideration to guarantee the circuit can meet the stringent engineering requirements.

4.4 FET Geometry Design

As a rule of thumb, to obtain an output power of P_{1dB} mW, a maximum output power capacity of 2*P_{1dB} mW is needed. So for an output power of 20 dBm (100 mW) in Table 4.1, a maximum output power capacity of 200 mW is required. In order to determine

the total gatewidth, the maximum output power for unit gatewidth should be known. For the OMMIC pHEMT process, the maximum output power per micrometer of gate width is about 0.6 mW [27]. So the final stage in this design should have a total gate width of 200 mW $\div$ 0.6 mW/μm = 333 μm.

As non-uniformity of current distribution from cell to cell in the wide FET will reduce the output power, an extra margin should be taken into consideration during the geometry design. Hence, dependent on the margin, the gate width is expected to be between 333 μm (200 mW) and 420 μm (250 mW). According to the OMMIC design manual, the width of the gate fingers can reach up to 75 μm, and the number in parallel can reach 8 [27]. So we have two choices, 8 $\times$ 50 μm and 6 $\times$ 70 μm.

Generally speaking, longer gate width means more signal loss because of the larger gate resistance. That is why people prefer to connect several short fingers in parallel. But a wide FET structure may lead to a lower gain because of phase shift at the gate input feed point, nonuniform current distribution and nonuniform channel temperature [47]. In order to determine the optimum size of the transistor, gain-frequency analysis was carried out to compare the configurations in Agilent ADS. Several important parameters can be obtained for comparison, including S_{21}, MSG, f_T and f_{max}, in which f_T corresponds to the frequency when current gain, h_{21} reaches 0 dB, f_{max} corresponds to the frequency when MAG reaches 0 dB. The simulation results are listed in Table 4.2.

Table 4.2: Comparisons between the 1st and 2nd cases

Gate Width	8×50 μm	6×70 μm
f_T	123 GHz	108 GHz
f_{max}	133 GHz	109 GHz
MSG @ 29 GHz	12.099 dB	11.988 dB
S_{21} @ 29 GHz	4.043 dB	3.957 dB

The comparisons in Table 4.2 show that the total width of 8 $\times$ 50 μm can lead to better performance in term of frequency and gain in spite of having a smaller total gatewidth and was therefore adopted. The layout is shown in Figure 4.1.

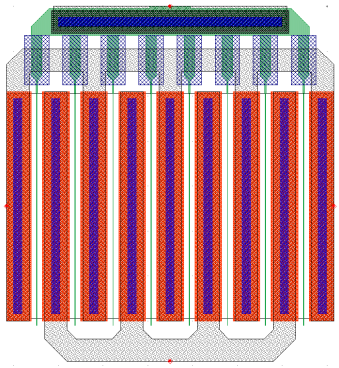


Figure 4.1: Layout of the 2nd stage transistor

In the gain allocation, the first stage is expected to have at least 10 dB of gain and the second stage is expected to have 8 dB. Thus the output power of the first stage should be at least 12∼17 dBm to drive the final stage. Using the method in the final stage design, the gate width for the the first stage should be about 54 μm, which corresponds to 4 $\times$13 μm or 6 $\times$ 9 μm. In a similar way, these two cases were analyzed with the same method in the final stage design and the comparison is shown in Table 4.3.

Table 4.3: Comparisons between the 1st and 2nd cases

Gate Width	4 $\times$13 μm	6 $\times$ 9 μm
f_T	200 GHz	84 GHz
f_{max}	150 GHz	132 GHz
MSG@29 GHz	10.361 dB	9.555 dB
S_{21}@29 GHz	5.574 dB	5.132 dB

Based on the comparison in Table 4.3, the size of 4 $\times$ 13 μm has better frequency performance and gain performance and is chosen. The layout is shown in Figure 4.2.

4.5 Bias Point Selection

For the first stage, the bias point selection was performed using the I_{DC}-V_{DC} characteristics obtained by sweeping gate voltage VGS, and drain voltage VDS, with the configuration in Figure 4.3. In this configuration, analysis is carried out under ideal conditions, in which ideal inductors work as RF chock in the bias circuit. The first stage should be designed for the maximum gain and biased near Class A. A suitable bias point

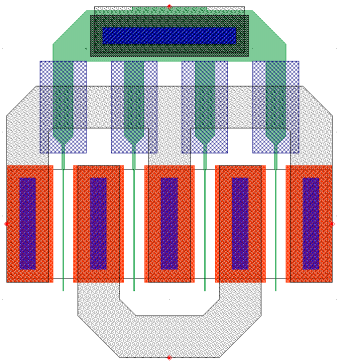


Figure 4.2: Layout of the first stage transistor

chosen is shown in Figure 4.4.

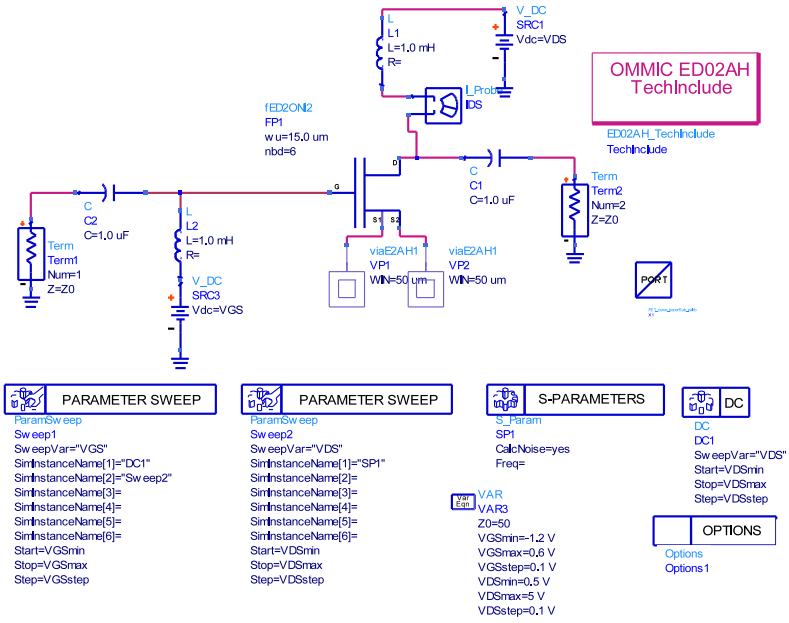


Figure 4.3: Bias point design of the first stage

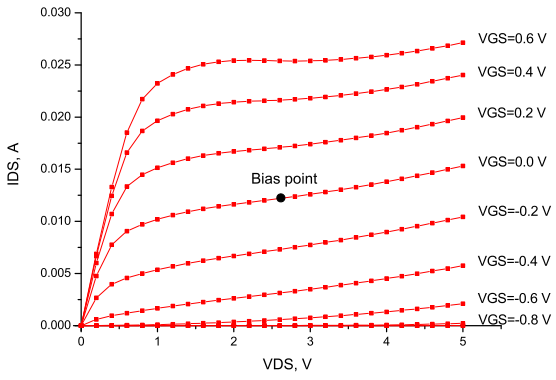
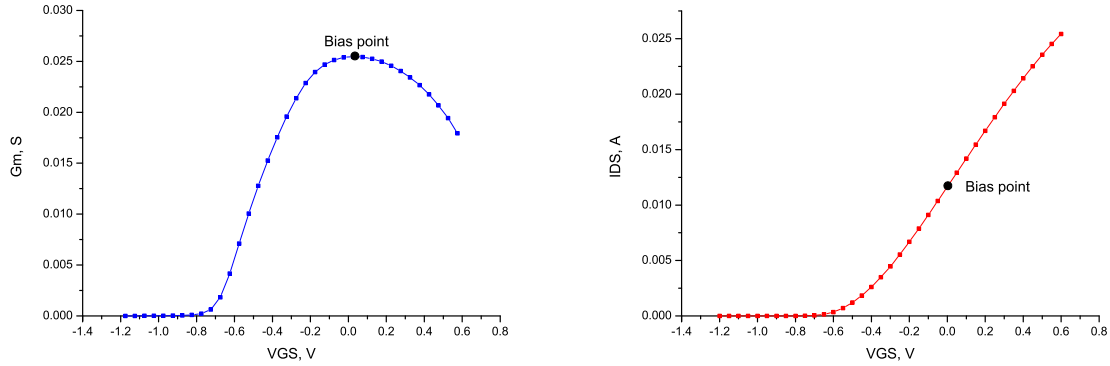


Figure 4.4: I-V curves of the 1st stage

By sweeping Gm against the bias voltage VGS, we can see that maximum gain happens to be at zero voltage gate bias as shown in Figure 4.5 (a) and the corresponding IDS is about 12 mA as shown in Figure 4.5 (b). Zero voltage is easy to implement as it does not require a separate gate bias voltage, which is referred to a self-biased design. Obviously self-biased design will ease the bias design and measurement scheme design.



(a) Bias point selection (b) Bias current at the bias point

Figure 4.5: Bias point design of the first stage

4.6 Design of Optimum Load Impedance and Source Impedance

4.6.1 Design of Optimum Load Impedance

Optimum load impedance was determined by the load-pull simulation in Agilent ADS. The set-up for simulation is configured as the practical circuit to produce reliable results. For example, the ground connection is realized by the via-holes rather than ideal ground and the high-impedance stub instead of the ideal RF chock is chosen as the drain bias network.

Figure 4.6 is the results from the load-pull analysis, in which a series of simulated load impedances are shown. By selecting the load impedance, the corresponding PAE and the delivered power are obtained. Figure 4.7 presents the output power, represented by blue contours and PAE, represented by thick red contours derived from the load-pull analysis. By tuning the load impedance, the optimum output power and PAE can be obtained and shown in Figure 4.6 and Figure 4.7.

For this case, the drain supply voltage was tuned from 1 to 5 V and the gate bias voltage was tuned from -1.2 to 0.6 V during the analysis. For the maximum output

power, the VGS should be 0.1 V when VDD is 2 V according to the analysis. Under such circumstances, the maximum output power is around 20.11 dBm and corresponding PAE can reach 34.54% as shown in Figure 4.6. Power contours and PAE contours from the load pull design are shown in Figure 4.7. In Figure 4.7, we can see that the optimum impedance for maximum output power and the optimum impedance for maximum PAE are not coincident, that is, we cannot have the maximum output power and and maximum PAE simultaneously. If VDD is increased to 2.5 V, then the maximum output power can reach 21.2 dBm and PAE is about 36.8% as shown in Figure 4.8. So VDD=2.5 V is adopted for the maximum output power.

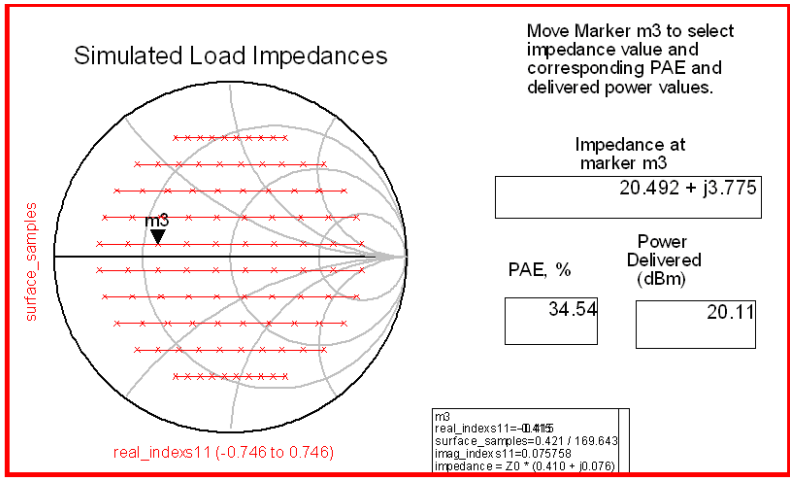


Figure 4.6: Load-pull result of the 2nd stage when VDD is 2V

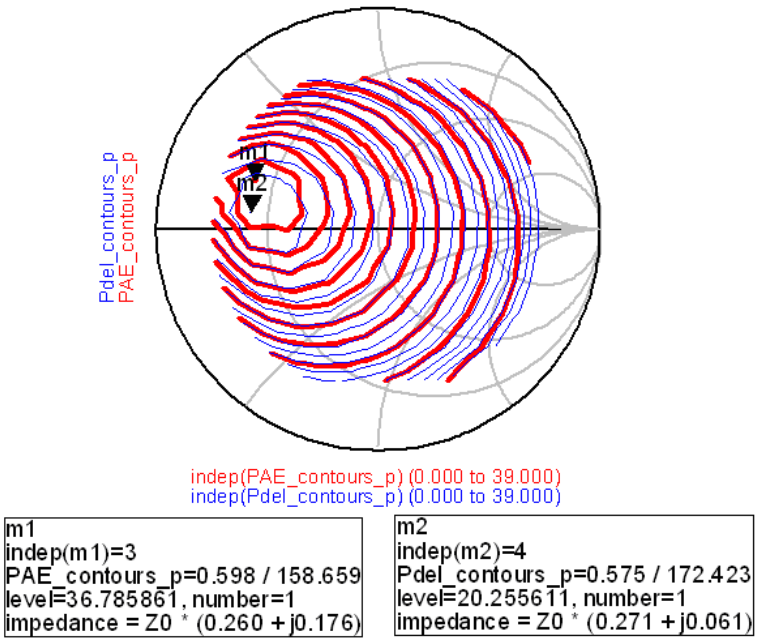


Figure 4.7: Power Contours and PAE Contours

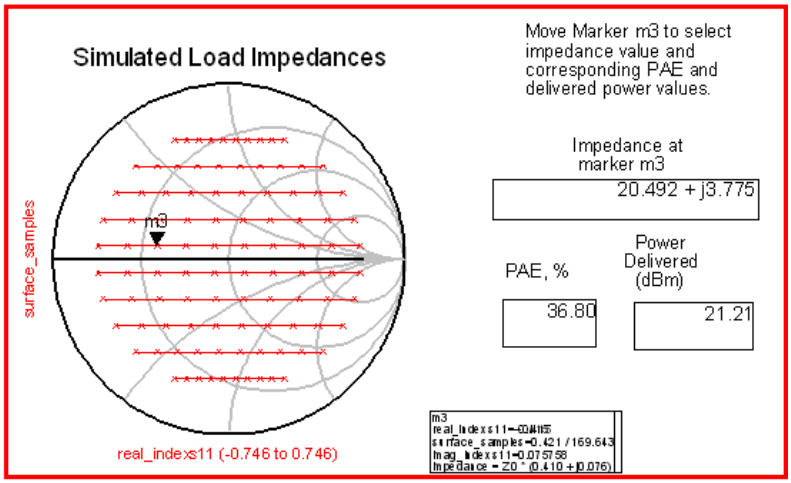


Figure 4.8: Load-pull result of the 2nd stage when VDD is 2.5V

4.6.2 Design of Optimum Source Impedance

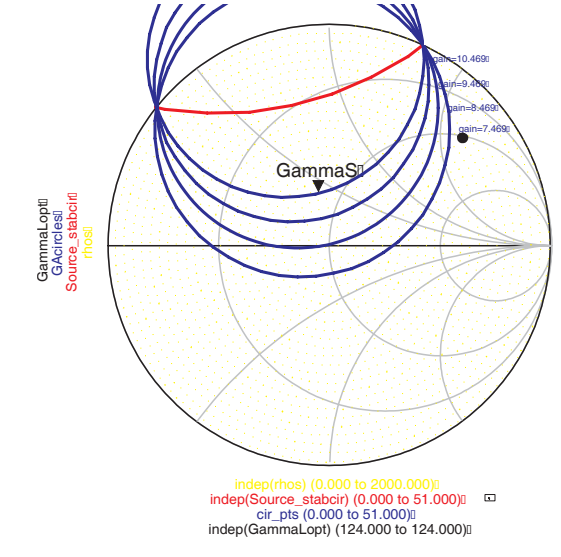
Similarly with the analysis method above, source-pull analysis was carried out to determine the optimum input impedance for the maximum gain of the first stage. In the source-pull analysis, the drain supply voltage VDD and the gate bias voltage VGS were swept and the optimum input impedance was determined at the conditions of VDD=2.5 V and VGS=0 V. Some equations were written to calculate and display the constant gain circles in Agilent ADS.

Figure 4.9 (a) is the constant gain circles from the source-pull analysis. We can see that the maximum gain that can be obtained is 10.555 dB. So the optimum source impedance for the maximum gain is (40.322+ j*20.961) Ohm as shown in Figure 4.9 (b).

4.7 Matching Network Design

In the design of matching networks, the first step is to find the optimum impedance. For the output matching network, the optimum impedance for the maximum output power can be obtained with load-pull analysis and for the input matching network, the optimum impedance can been derived by source-pull method, as discussed in Section 4.6. The interstage matching network usually works as an impedance transformer between stages.

Several topologies based on microstrip stub are available for matching network design, including single tuning stub, dual tuning stub network, quarter-wave transformer and multi-section transformer. They are illustrated in Figure 4.10.

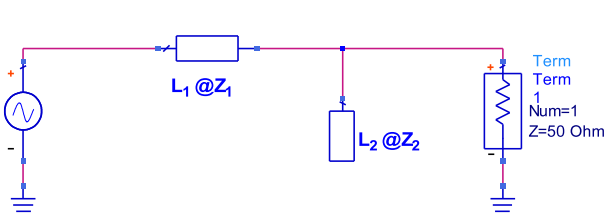


(a) Constant gain circles from source-pull analysis

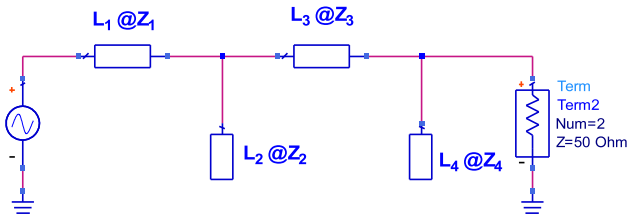
Source Impedance at marker GammaS	Optimal load impedance for power transfer when source impedance at marker GammaS is presented to input	Transducer Power Gain, dB when these source and load impedances are used
40.322 + j20.961	50.852 + j122.772	10.555

(b) Results from source-pull analysis

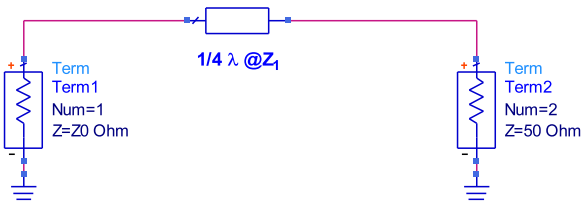
Figure 4.9: Source-pull analysis for the first stage



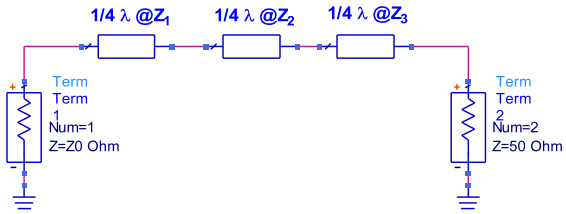
(a) Single tuning stub



(b) Dual tuning stub



(c) Quarter-wave transformer



(d) Multi-section transformer

Figure 4.10: Microstrip matching structures

The single tuning stub structure in Figure 4.10 (a) is simple and relatively easy to design. But it can only be matched at a single frequency point. When the frequency is changed, the stub has to be placed in a new position. Obviously this structure is not suitable for wide-band matching. The dual tuning stub in Figure 4.10 (b) is an improvement on the single tuning stub and it allows matching of almost all possible load

impedances. In practical applications, a limiting factor is the attenuation along the line. Another point is that wide-band matching requires the distance between the stubs be close to half of the wavelength [94], which means that this structure will occupy a large area. The quarter-wave transformer in Figure 4.10 (c) has the main problem of narrow matching bandwidth. Though a wider bandwidth can be obtained by several consecutive transformer sections shown in Figure 4.10 (d) such as the binomial transformer and the Chebyshev transformer [94], such structures would occupy a very large area.

Based on these comparisons, an idea of combining two matching methods above is introduced, that is, the single tuning stub plus the quarter-wave transformer as shown in Figure 4.11. In this topology the single tuning stub can transform the complex load impedance to a real value and the quarter-wave transformer transforms between the real value and 50 Ohm. This topology has enough flexibility to realize wide-band matching and its size is much smaller than the multi-section transformer.

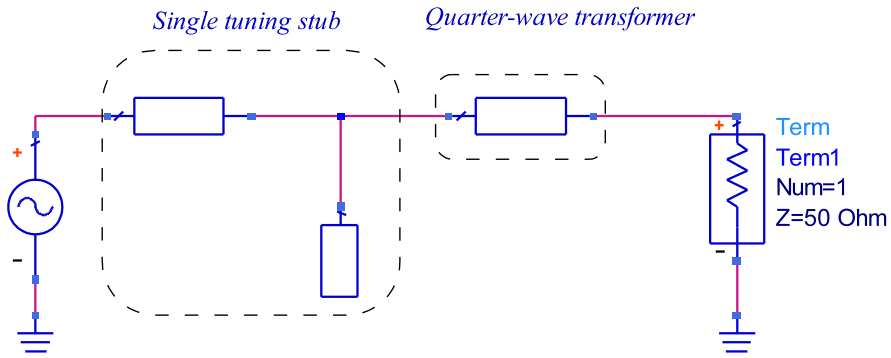
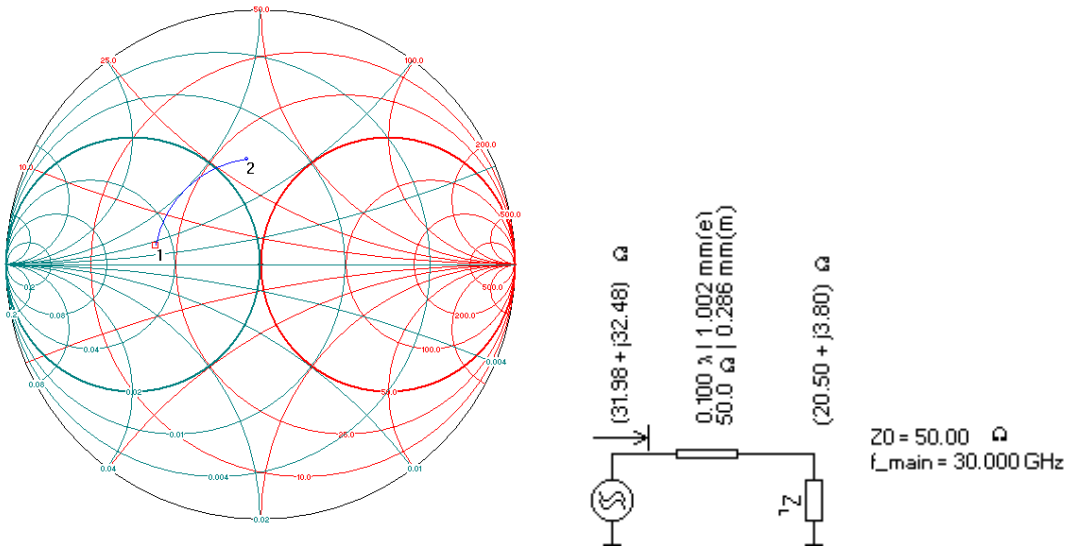


Figure 4.11: The matching structure in this design

Z-Y Smith charts are employed to design the matching networks as shown in Figure 4.12 (a) and Figure 4.13 (a). For the output matching network, the optimum impedance for the maximum output power at 30 GHz is (20.5+j*3.8) Ohm as calculated in Section 4.6. It corresponds to Point 1 in Figure 4.12 (a). In the first step, a series transmission-line stub with the length of 0.1 λ is added in order to move to Point 2, as shown in Figure 4.12 (a). Point 2 is chosen because the output impedance seen from Point 2 is (32+j*32) Ohm, which is convenient for the further quarter-wave transformer calculation. The output impedance for Point 2 in Figure 4.12 (a) is indicated in Figure 4.12 (b). In the second step, in order to cancel the susceptance part in (32+j*32) Ohm, a susceptance of -j*32 is needed. As seen in Figure 4.13 (b), the susceptance of -j*32 can be

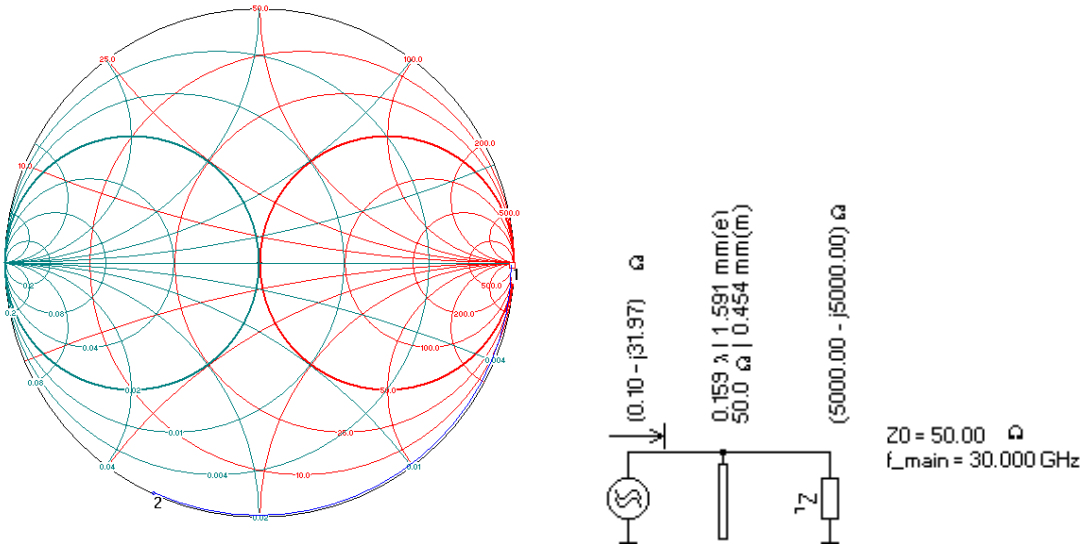
realized by an open-circuited stub with a length of 0.158λ. After this open-circuited stub is added to the matching network, the output impedance is a real value of 32 Ohm. In the third step, with a quarter-wave transformer whose characteristic impedance is $\sqrt{32 \times 50}$ = 40 Ohm, the impedance of 32 Ohm is transformed to 50 Ohm and this schematic is shown in Figure 4.14.

As the output matching network works around 30 GHz, further optimization was carried out to make it suitable for wide-band matching over 27 to 30 GHz. During the optimization, the length of open-circuited stub and transformer was adjusted according to the design rule. Figure 4.15 shows the final output network and the matching status is shown in Figure 4.16. From Figure 4.16 we can see that the return loss is less than -30 dB and $VSWR$ is only around 1, that is, this topology can realize a very good matching over the whole frequency band of interest.



(a) Illustration of the first step in Smith chart (b) The schematic in the first step

Figure 4.12: The first step in output matching network design



(a) Illustration of the second step in Smith chart (b) The schematic in the second step

Figure 4.13: The second step in output matching network design

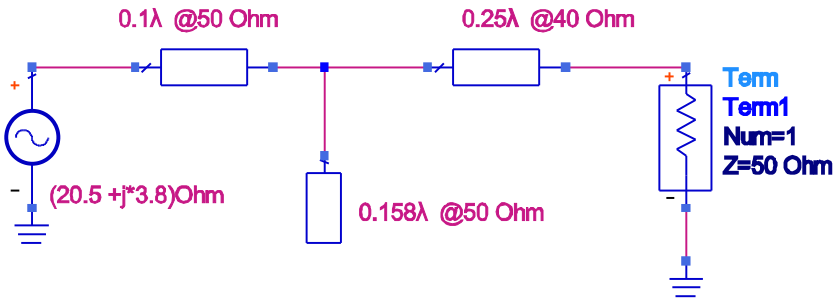


Figure 4.14: Output matching network schematic

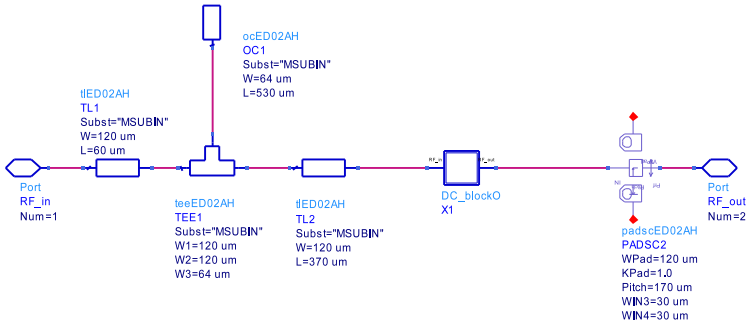
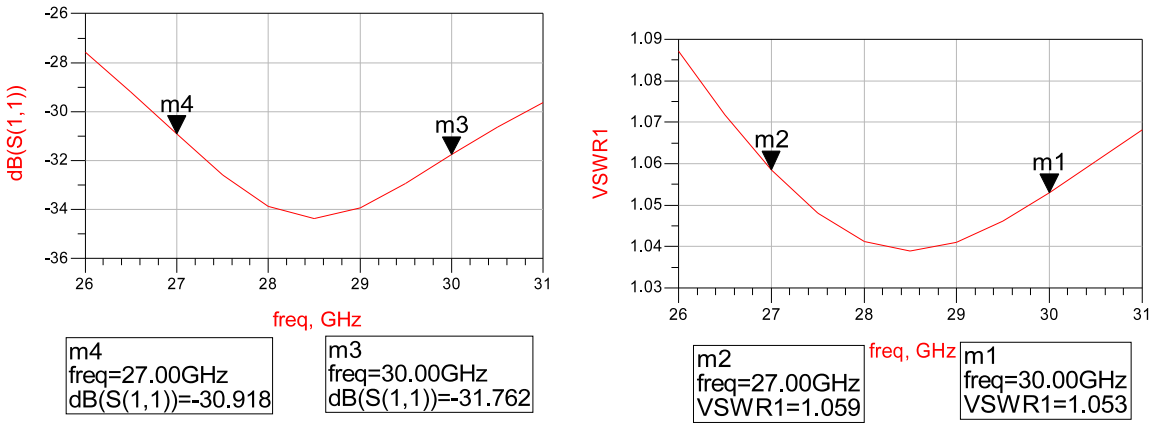


Figure 4.15: The topology of output matching network

Similarly with the method above, the input matching network and the interstage matching network were designed. Their structures are shown in Figure 4.17 and Figure 4.18 respectively.



(a) Output return loss characteristic (b) Output $VSWR$ characteristic

Figure 4.16: Matching status of output matching network

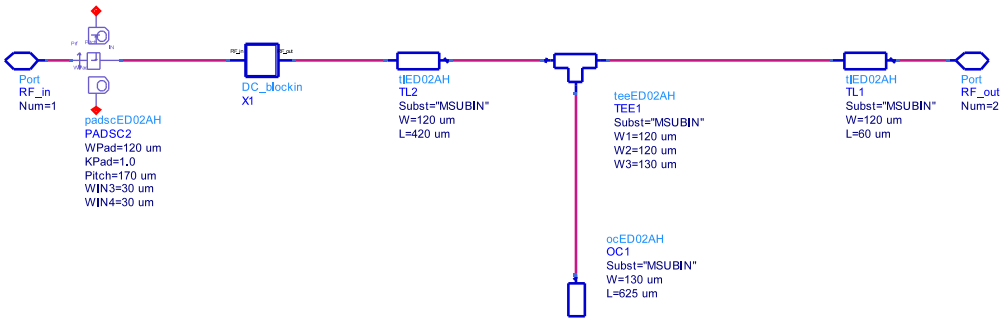


Figure 4.17: The topology of input matching network

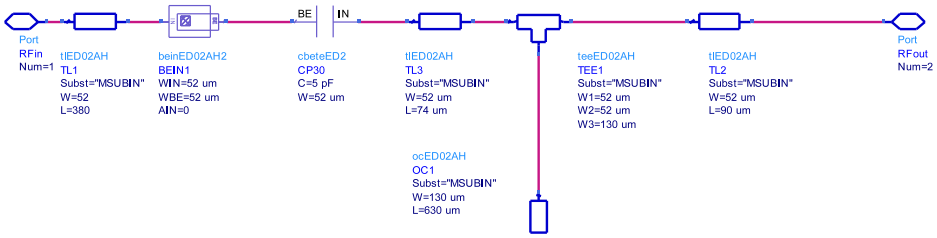


Figure 4.18: The topology of interstage matching network

4.8 Discontinuities Analysis

For millimeter-wave circuit design, accurate element models, especially accurate models for passive elements are key factors. But discontinuity schematic models in most of the design kits are not accurate as they cannot incorporate some parasitic effects such as skin effect and proximity effect. In this part of the design, a great deal of effort has been spent on the discontinuity modeling using the electromagnetic method. Full-wave analysis with the Momentum module in Agilent ADS was chosen. With the electromag-

netic method, the disparity between the standard models and practical discontinuities is expected to be resolved effectively. In this section, the design of several discontinuities with the electromagnetic method will be described.

4.8.1 High-Impedance Stub Design

The high-impedance stub is widely used in millimeter-wave circuit design. In commercial design, the discontinuities such as the short-circuited stub and the bended stub need further verification using the EM method.

4.8.1.1 Quarter-Wave Length $\lambda/4$ Calculation

The basic equation for wavelength λ is as follows:

$$\lambda = \frac{c}{\sqrt{\varepsilon_{eff}} \cdot f}, \tag{4.1}$$

where f is the working frequency, c is the light speed in free space and ε_{eff} is the effective permittivity since the field exists not only in the substrate but also in the air above.

In this design, the thickness of the microstrip is T=1.25 μm; For a GaAs substrate the relative permittivity, ε_r=12.3, the effective permittivity, ε_{eff}=8.053. According to Equation (4.1), λ_{eff}@30 GHz=3521 μm, so $\lambda_{eff}/4$= 880 μm.

4.8.1.2 High-Impedance Stub Design

In millimeter-wave amplifier design, the short-circuited high-impedance stub is always employed to replace inductor in bias networks. The equivalent circuit of the short-circuited stub is comprised of an inductor and a capacitor in parallel connection as shown in Figure 4.19.

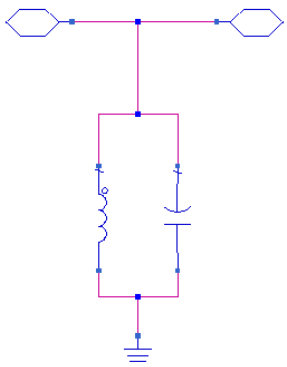


Figure 4.19: Equivalent circuit of the short-circuited stub

In the analysis, the stub is connected to ground just as the short-circuited stub in the bias network shown in Figure 4.38. The length of the stub was swept from 870 μm to 980 μm in the frequency range of 26 GHz to 31 GHz. The sweep results, including the equivalent inductance and capacitance are shown in Figure 4.20 and Figure 4.21 respectively. The results in Figure 4.20 and Figure 4.21 were used to determine the optimum width and length of the stub.

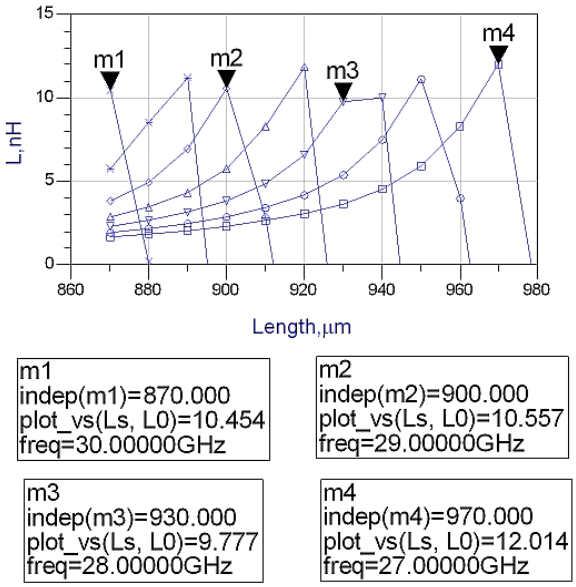
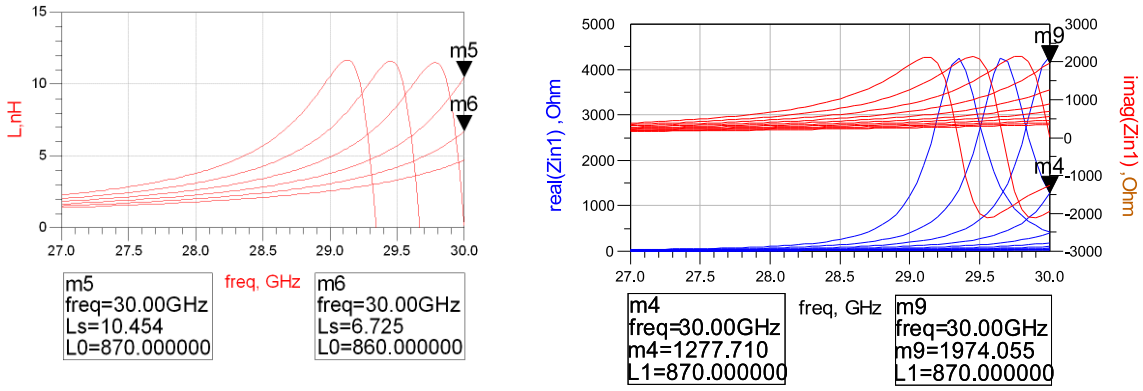


Figure 4.20: Equivalent inductance vs. strip length for the short-circuited stub

A wide-band circuit, unlike a narrow band circuit, cannot be optimized in every aspect at the whole frequency band. A case in point is the $\lambda_{eff}/4$. For 30 GHz, $\lambda_{eff}/4$= 880 μm; For 27 GHz, $\lambda_{eff}/4$= 979.3 μm. The $\lambda_{eff}/4$ that corresponds to a certain frequency



(a) Equivalent inductance sweep (b) Equivalent impedance sweep

Figure 4.21: Equivalent inductance and impedance of the stub

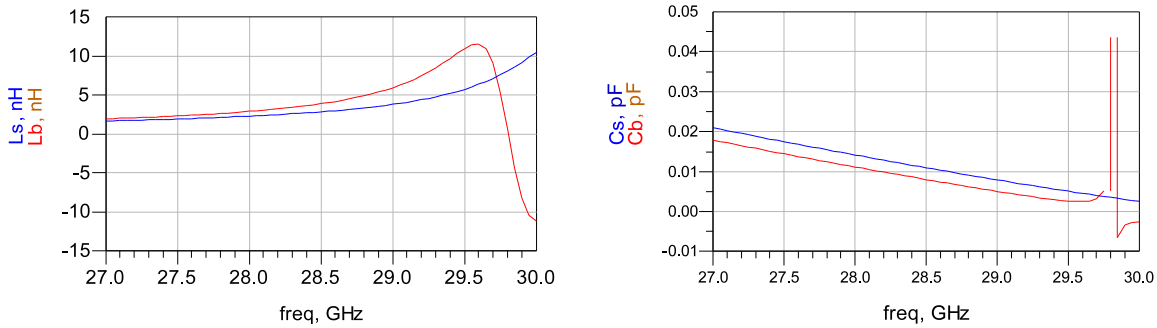
cannot give the expected performance at another frequency within the band. As distributed elements are suitable for narrow band design naturally, further analysis is needed over the whole frequency band of 27∼30 GHz.

In Figure 4.20, every curve represents the equivalent inductance at one frequency. The curves where Point m2, m10, m12, m8 are located represent 30 GHz, 29 GHz, 28 GHz and 27 GHz respectively. The X-axis represents the length of the stub and the Y-axis represents the equivalent inductance. We can see that when the length L1 is 870 μm, all the equivalent inductances are positive throughout the frequency band of interest. When the length is 880 μm, the equivalent inductance at 30 GHz is 0 and when the length is more than 880 μm, the equivalent inductances at some frequencies may be negative, that is, behave capacitively. So the length of the stub should be less than 880 μm. In Figure 4.21 (a), among 860 μm, 870 μm and 880 μm, the equivalent inductance of 870 μm is highest. In Figure 4.21 (b), the equivalent impedance of 870 μm can reach up to (1277.7 +j*1974) Ohm. So for the amplifier design, the length of 870 μm is chosen, since the short-circuited, high-impedance stub with this length has the maximum inductance and can behave inductively over the whole frequency band of interest.

4.8.1.3 Bended Line Design

Since a length of 870 μm is rather large for a real chip, a bended line is preferred in the practical design in order to save area. S-parameter simulation was carried out to evaluate the equivalent inductance and capacitance in Agilent ADS. The results of the

bended line analysis are shown in Figure 4.22, where the equivalent inductance, Lb and the equivalent capacitance, Cb, are compared with the counterparts of the straight line, Ls and Cs respectively.



(a) Equivalent inductance comparison (b) Equivalent capacitance comparison

Figure 4.22: Comparison between straight line and bended line

In Figure 4.22, we can see that Lb, is slightly bigger than Ls, while Cb is slightly smaller than Cs. The differences in Figure 4.22 mainly come from the parasitic effects, which are included in OMMIC BEND model in Figure 4.23 [27], which is used to evaluate the difference between the bended line and the straight line.

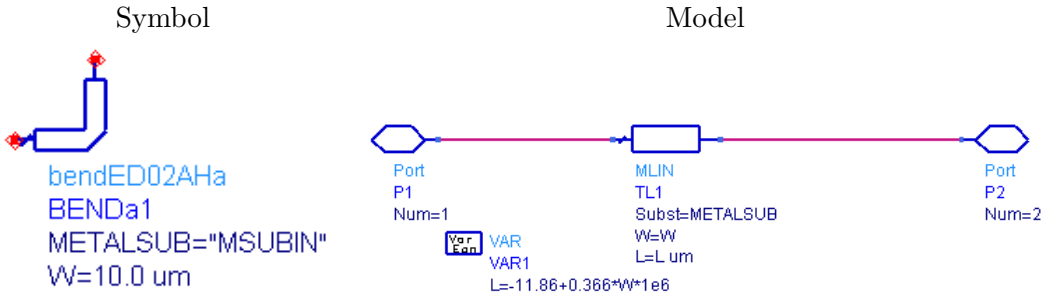
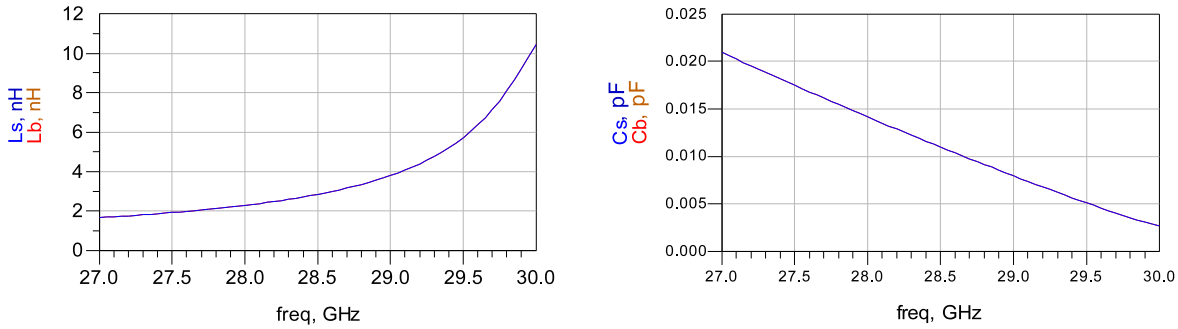


Figure 4.23: Bended line model in OMMIC design kit

The bended line in Figure 4.23 is equivalent to the straight line with the length of $L = (-11.86 + 0.366 * W * 1e6)$ μm. For this design, the increased length is about 15.8 μm. The difference between the equivalent inductance and capacitance of the straight line and the bended line after adjustment as shown in Figure 4.24. Now the difference after adjustment is negligible.

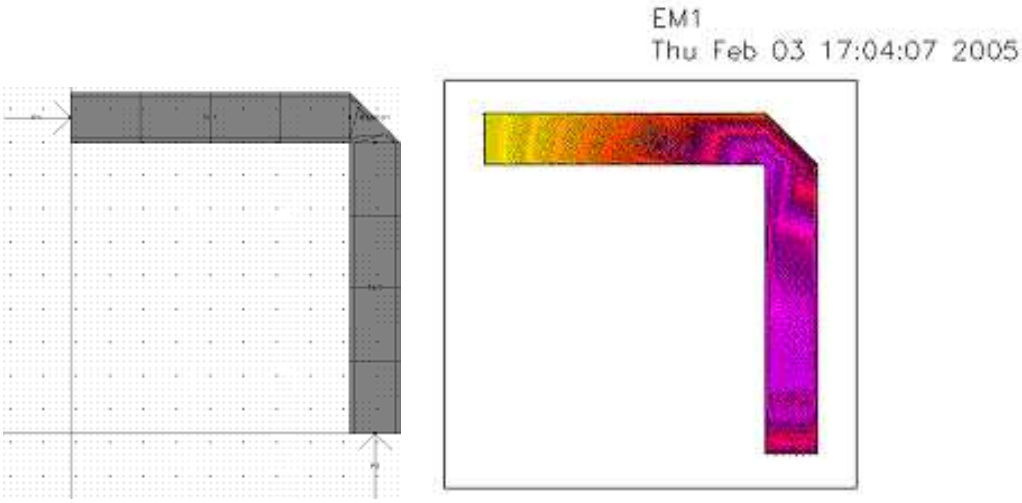
Furthermore, EM simulation is performed for accurate results. The layout and current distribution for the bended line obtained from EM analysis are shown in Figure 4.25. In Figure 4.26, 'strip..S(1,1)' and 'strip..S(2,1)' represents the results from the EM analysis and 'S(1,1)' and 'S(2,1)' represent the results from the schematic analysis.



(a) Equivalent inductance comparison (b) Equivalent capacitance comparison

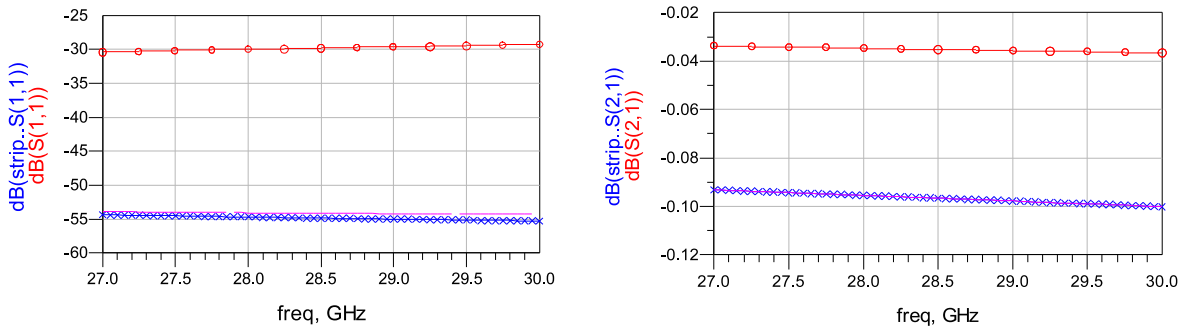
Figure 4.24: Comparison after bended line is adjusted

An obvious difference, including insertion loss and return loss between the EM analysis and schematic simulation is shown. For the return loss S(1,1) and insertion loss S(2,1), the results from the EM method are much lower than those from the schematic analysis. So further optimization is expected to minimize the gap.



(a) Bended line layout (b) Current distribution in the bended line

Figure 4.25: EM analysis of bended line



(a) Return loss comparison (b) Insertion loss comparison

Figure 4.26: Comparisons between EM analysis and schematic analysis

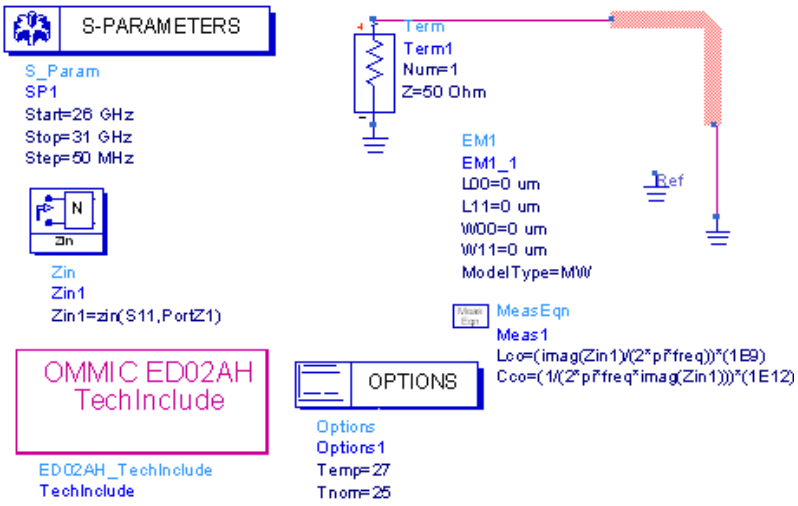
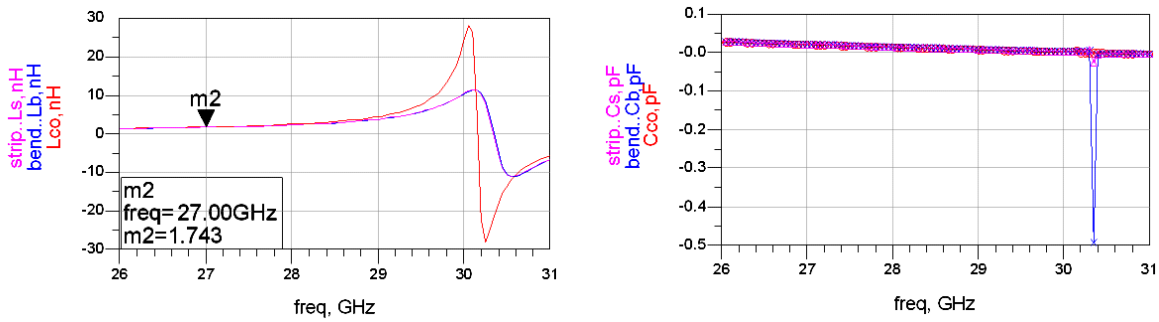


Figure 4.27: Bended line analysis with Advanced Model Composer

Advanced Model Composer(AMC) [95] is an electromagnetic method used in this design. Optimization by AMC shown in Figure 4.27 was used to adjust the length of the stub to minimize the difference between the EM analysis and schematic simulation. The bended line in Figure 4.27 was generated by AMC in Agilent ADS and the results produced are shown in Figure 4.28. In Figure 4.28, Lco represents the equivalent inductance of bended line derived from the EM method while 'bend..Lb' represents the equivalent inductance of the bended line derived from schematic analysis and 'strip..Ls' is the equivalent inductance of the straight line calculated by the schematic analysis. From the results, we can see that the equivalent inductance derived from the EM method is much bigger that that derived from the schematic analysis while the difference in the equivalent capacitance comparison is very small.



(a) Equivalent inductances comparison (b) Equivalent capacitances comparison

Figure 4.28: Comparisons between AMC analysis and schematic analysis

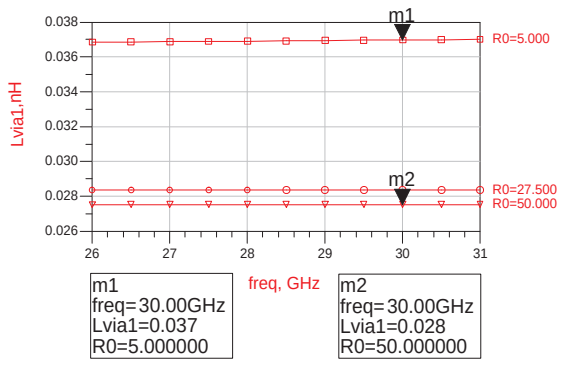
4.8.2 Via Hole Design

In this design, via holes are primarily used as FET source connection to ground. In such a configuration, the negative feedback from the parasitic inductance and resistance degrades the performance significantly. Thus the less the inductance and resistance are, the higher the performance is.

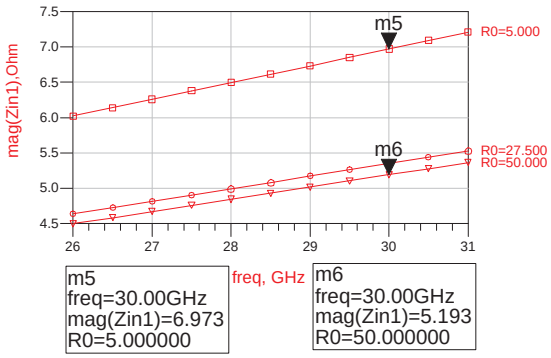
For the circuit based on the OMMIC Design Kit, the width of the access line ranges between 5 μm and 50 μm [27]. The diameter of the via-hole, R0 was swept from 5 μm to 50 μm during the analysis and the equivalent inductance and equivalent capacitance were produced. The sweep analysis results are shown in Figure 4.29, in which Lvia1 is the parasitic inductance and Zin1 is the parasitic resistance. According to the analysis, the wider the width is, the smaller the parasitic inductance and resistance are.

When the width is 50 μm, the parasitic inductance is about 0.028 nH and the equivalent resistance is about 5.193 Ohm as shown in Figure 4.29. As the parasitic inductance and resistance are the smallest when the width is 50 μm, the width of 50 μm is the optimum choice accordingly.

In the verification with the EM method, It is found that the parasitic inductance calculated by the EM method is much higher than that by the schematic method while the parasitic capacitance calculated by the EM method is much lower that by the schematic method. These comparisons are shown in Figure 4.30. Obviously, for such discontinuities, the results from the EM method should be more accurate and should be employed during the simulation.

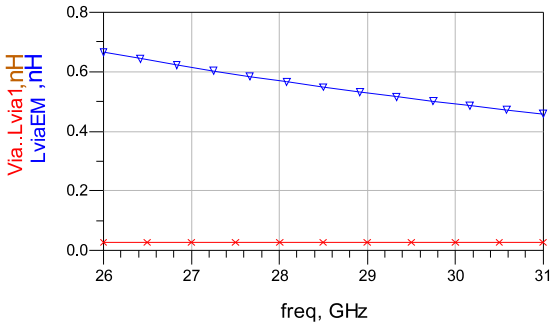


(a) Equivalent inductance sweep results

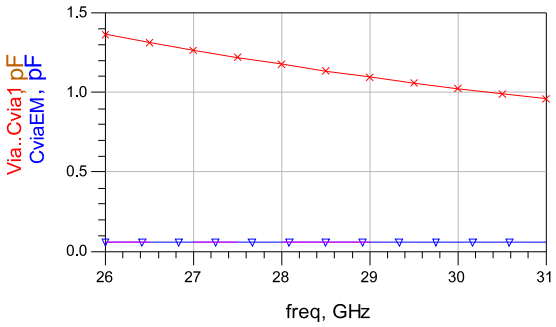


(b) Equivalent resistance sweep results

Figure 4.29: Sweep results from schematic design



(a) Equivalent inductance comparison



(b) Equivalent capacitance comparison

Figure 4.30: Comparison between the EM analysis and Schematic analysis

4.9 Design for Robustness

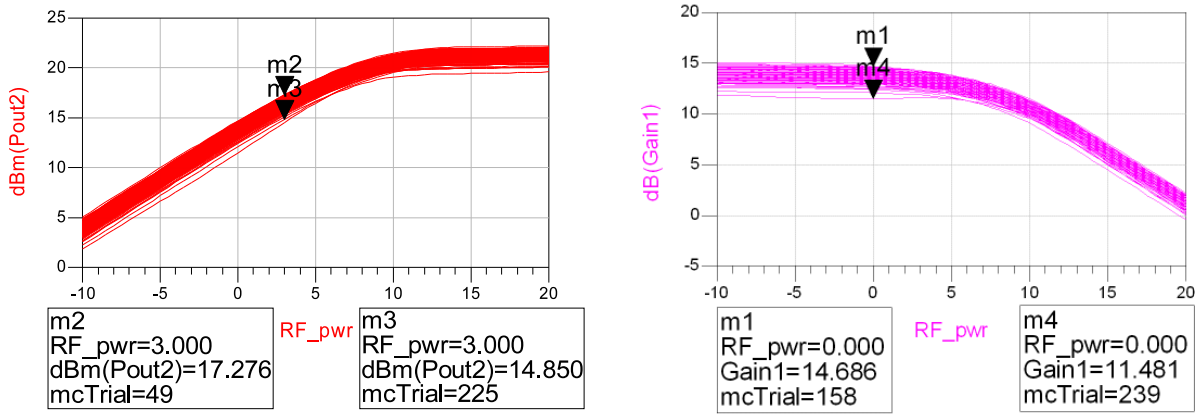
Design for robustness, as the final part of the millimeter-wave circuit design, is necessary when a paper design is converted to a practical design for manufacturing and should rightly be considered in research work. In order to expose latent problems in the design, some effort was spent on the manufacturing aspects during the millimeter-wave circuit design.

4.9.1 Monte Carlo Analysis

The Monte Carlo method has traditionally been widely used as a means to estimate yield. The method involves performing a series of trials. Each trial results from randomly generating yield variable values according to the statistical-distribution specifications, performing a simulation and evaluating the results against stated performance

specifications [95].

Figure 4.31 shows Monte Carlo analysis results for the power amplifier produced by Agilent ADS with 250 trials, including output power, Pout and Gain. In Figure 4.31, we can see that when the input power is 3 dBm, the output power ranges between 14.85 dBm and 17.28 dBm. When the input power is 0 dBm the power gain falls in the range from 11.48 dB to 14.69 dB. As some of the results in the initial Monte Carlo analysis fall below the original specifications given in Table 4.4, yield centering is needed to improve the yield and performance.



(a) Output power results (b) Power gain results

Figure 4.31: Initial Monte Carlo sweep analysis

Table 4.4: Comparison between the specifications and the Monte Carlo results

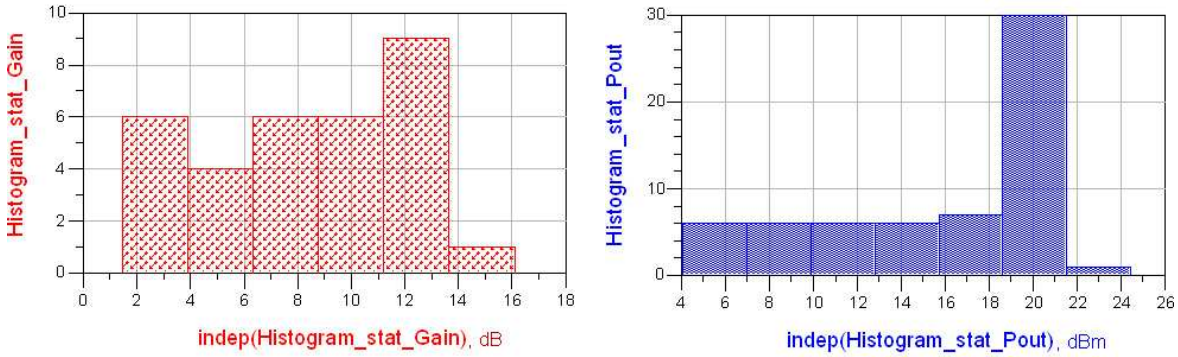
The metrics	Specifications	Monte Carlo results
Output power	15∼25 dBm	14.85∼17.28 dBm
Power gain	15∼ 20 dB	11.48∼ 14.69 dB

4.9.2 Yield Analysis

Yield analysis, based on the Monte Carlo method, enables the determination of the percentage of acceptable and unacceptable units based on the specifications. A series of trials are run in which random values are assigned to all of the design's statistical variables, a simulation is performed, and the yield specifications are checked against the simulated values. The number of passing and failing simulations is accumulated over the set of trials and used to compute the yield estimate [95].

4.9.2.1 Initial Analysis

The histogram results from the yield analysis are shown in Figure 4.32. We can see that most of power gain falls in the range of 7 $\sim$ 13 dB, while output power of 19 $\sim$ 21 dBm occupies a large percentage. In the initial analysis, 400 trials were run and the yield is only 81.75%, which is considered too low to accept for manufacturing. Yield centering needs to be performed to improve the yield.



(a) Power gain histogram results (b) Output power histogram results

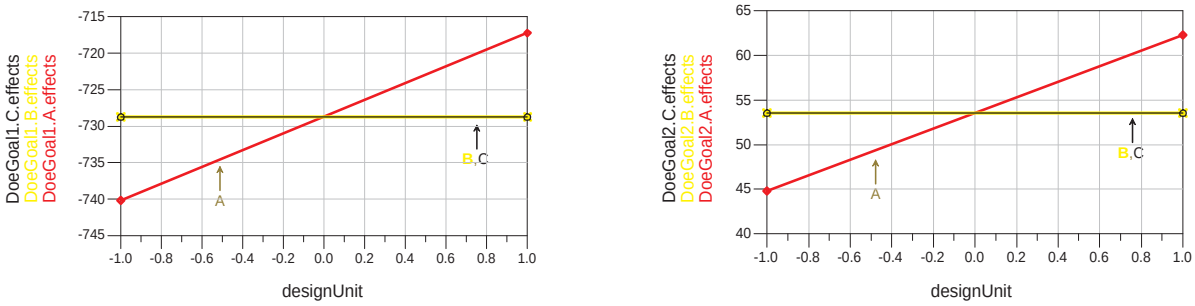
Figure 4.32: Histogram results before yield centering

4.9.2.2 Design of Experiments (DOE) Analysis

DOE was first used by agricultural engineers to improve crop yields. It is a data-driven technique that can be used for robust design. In the circuit or system simulation, DOE is used as a means to realize yield improvement, and improve the statistical performance of a circuit or system [95].

The DOE method was chosen to find the most sensitive part of the network (input, output or interstage) in the amplifier. The DOE analysis was carried out in Agilent ADS and small signal gain S(2,1) and output power Pout are set as the DOE goals. By adding steering variables to the network elements in the harmonic balance and S-parameter simulation, the sensitivity of the matching networks was analyzed and the results are shown in Figure 4.33. In Figure 4.33, A effects, B effects and C effects represent the impact of input network, the impact of interstage network and the impact of output network respectively. We can see that the input network, represented by the sloping line, is the most sensitive while the interstage network and the output network, represented by the coincidental horizontal lines, are not sensitive. So further optimization will be performed

to minimize the impact of input network on the yield.



(a) DOE result when S(2,1) is the goal (b) DOE result when Pout is the goal

Figure 4.33: DOE analysis results before yield centering

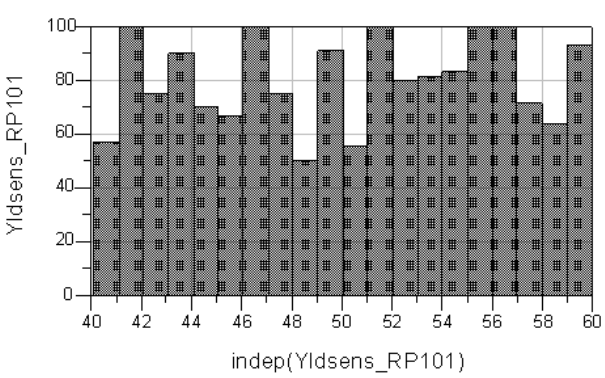
4.9.3 Yield Centering

Yield centering, or yield optimization, is a process of adjusting nominal values of selected element parameters in order to maximize yield. It is an indispensable part of the MMIC and millimeter-wave circuit design flow.

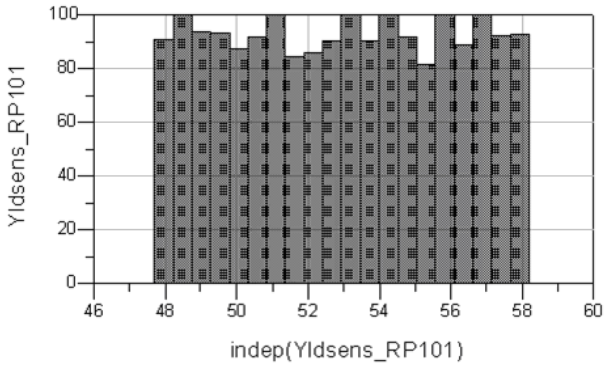
Before yield centering, there are some performance parameters with high sensitivity and the yield is strongly affected by process variations. Firstly the sensitive elements should be identified, so that the yield can be optimized with these targets. A sweep analysis was carried out to find out the sensitive elements that may lead to the latent robustness problem. A case in point is the resistor, RP10 in the gate bias network shown in Figure 4.38, whose nominal value is 50 Ohm. In the OMMIC process, the process variation of NiCr resistance is ±3.5%. That is, RP10 varies in the range between 48.25 Ohm and 51.75 Ohm. As shown in Figure 4.34 (a), when RP10 is 50.5 Ohm, the yield is only 55%, which obviously cannot be tolerated. Before yield centering, the yield is quite affected by its deviation.

After yield centering as shown in Figure 4.34 (b), it can be seen that the yield is less affected by the process variations. The new nominal value of RP10 is 48.5 Ohm. Within the deviation range of RP10, the yield is 100%. Besides RP10, all other passive elements with high sensitivity are also optimized simultaneously for the higher yield with the same method. The robustness is improved in this way.

After yield centering, a further stage of yield analysis was carried out based on



(a) Sensitivity analysis before yield centering



(b) Sensitivity analysis after yield centering

Figure 4.34: Sensitivity analysis of RP10

different criteria. Two criteria are selected to evaluate the yield after yield centering. Criterion 1: minimum output power of 17 dBm at the input power of 3 dBm and minimum 14 dB gain between 27 GHz and 30 GHz; Criterion 2: minimum output power of 16 dBm at the input power of 3 dBm and minimum 13 dB gain between 27 GHz and 30 GHz.

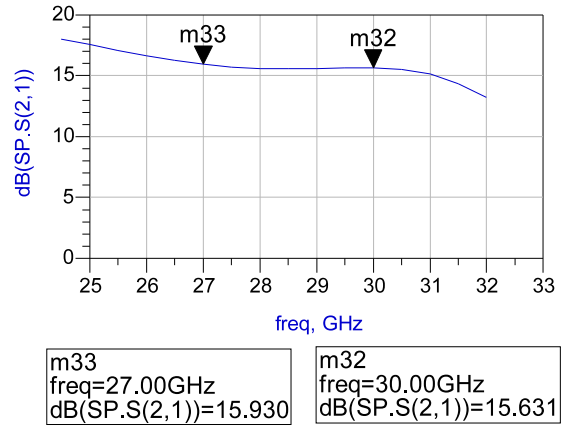
Table 4.5: Results after Yield Centering

Criterion	NumFail	NumPass	Yield
Criterion 1	35	415	92.22%
Criterion 2	0	450	100%

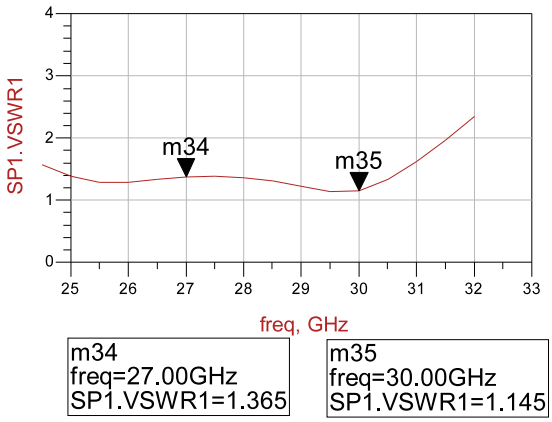
From the yield results Table 4.5, we can see that the optimization has improved the yield to the point where circuit can meet the requirements of commercial applications.

4.9.4 Simulation Results after Yield Centering

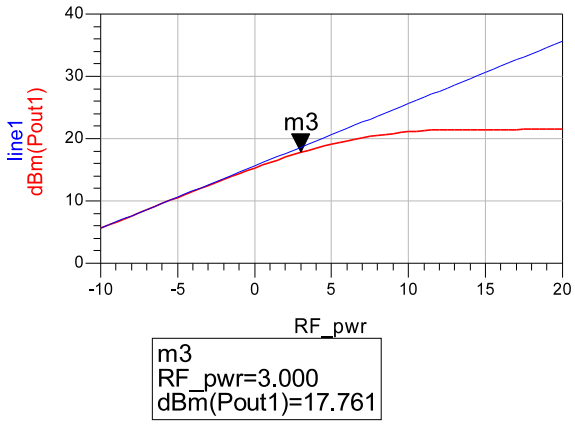
The simulation results for the millimeter-wave PA after yield centering are presented in Figure 4.35. We can see that in Figure 4.35 (a) small signal gain S(2,1) is now above 15.6 dB over the band of interest and in Figure 4.35 (c) P_{1dB} shown is above 17.7 dBm. These results are summarized and compared with the original specifications in Table 4.6. The results can meet the specifications and reach a higher yield simultaneously.



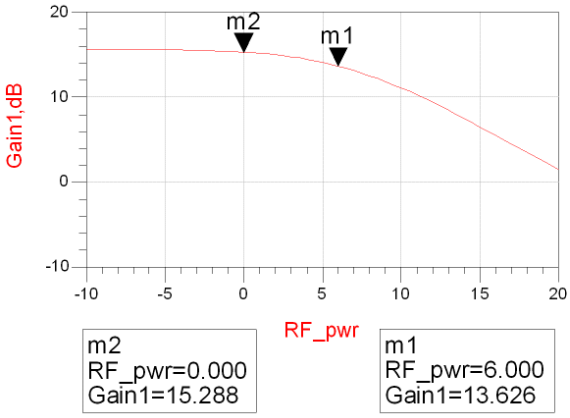
(a) Small signal gain



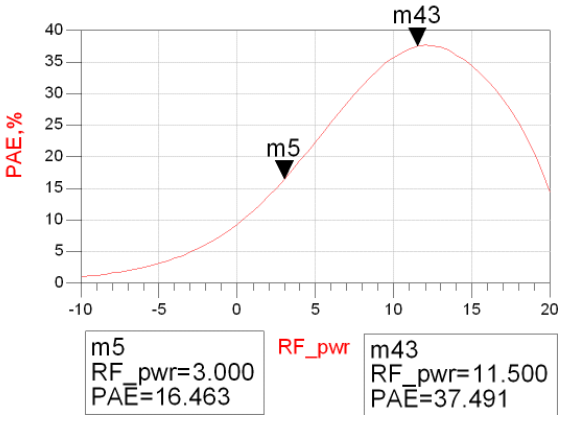
(b) Small signal input $VSWR$



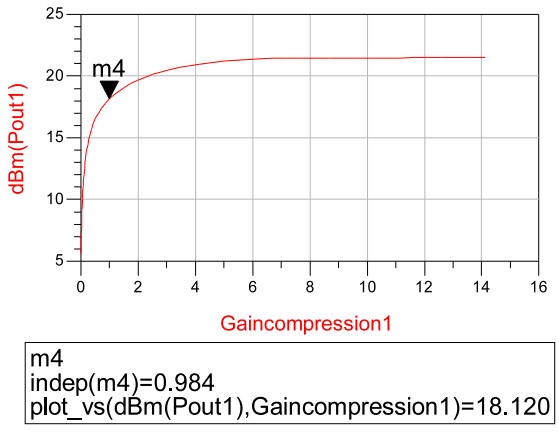
(c) Output power



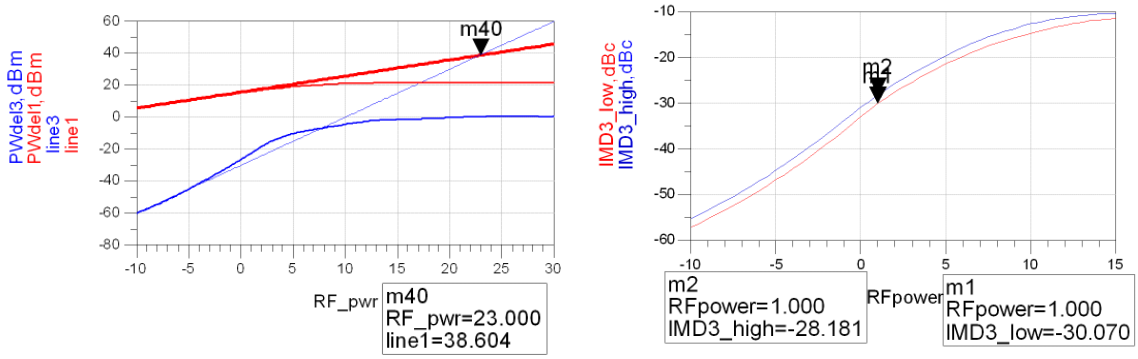
(d) power gain



(e) Power-added efficiency



(f) Output power vs. gain compression



(g) OIP3 characteristic (h) $IMD3$ characteristic

Figure 4.35: Design results after yield centering

Table 4.6: Results after Yield Centering

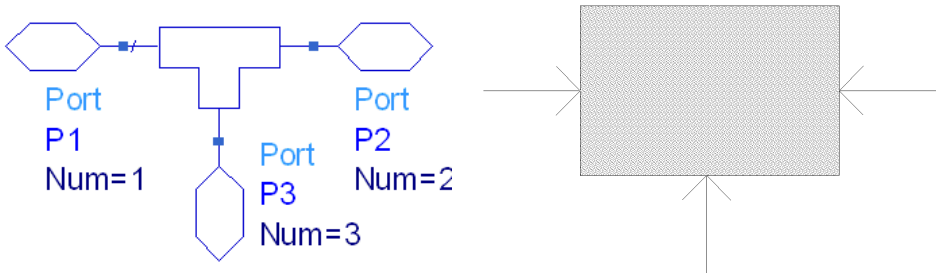
	Results after Yield Centering	Specifications
Power Gain	15.3 dB	15∼ 20 dB
Small Signal Gain	15.8 dB	
P_{1dB}	18.1 dBm	15∼25 dBm
Linearity($IMD3$)	-30 dBc	Below -30 dBc
Linearity(OIP3)	38.6 dBm	
PAE @P_{1dB}	16.5%	15∼30%
Peak Efficiency	37.5%	

4.10 Further Verification with the EM Method

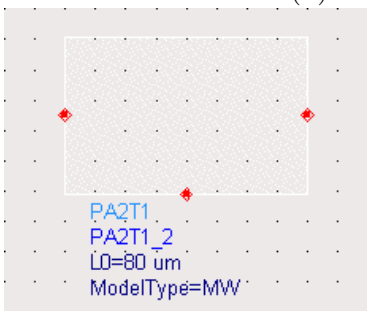
Some discontinuities need further verification with the EM method since not all parasitic effects can be incorporated in the schematic models. In this design, some effort was spent on the electromagnetic analysis using the Momentum module and Advanced Model Composer (AMC) in the Agilent ADS in order to resolve the disparity between the standard models and practical discontinuities.

The T-junction and cross junction are widely used in matching networks and bias networks, and affect the performance directly. Due to limited accuracy, people generally spend a lot of effort in verifying the accuracy. In this design, much attention is paid to the discontinuities, especially the T-junction and cross junction which are well-known for their

large dispersions at millimeter-wave frequencies, and their impacts on circuit performance will be also analyzed. In this part of the design, the component of concern is placed in the schematic window firstly as shown in Figure 4.36 (a) and Figure 4.37 (a) for the T-junction and multi-discontinuities. The corresponding layout is drawn with the Momentum module in Agilent ADS as shown in Figure 4.36 (b) and Figure 4.37 (b) respectively. With the EM analysis in AMC, a new schematic model based on the EM method is generated as shown in Figure 4.36 (c) and Figure 4.37 (c).

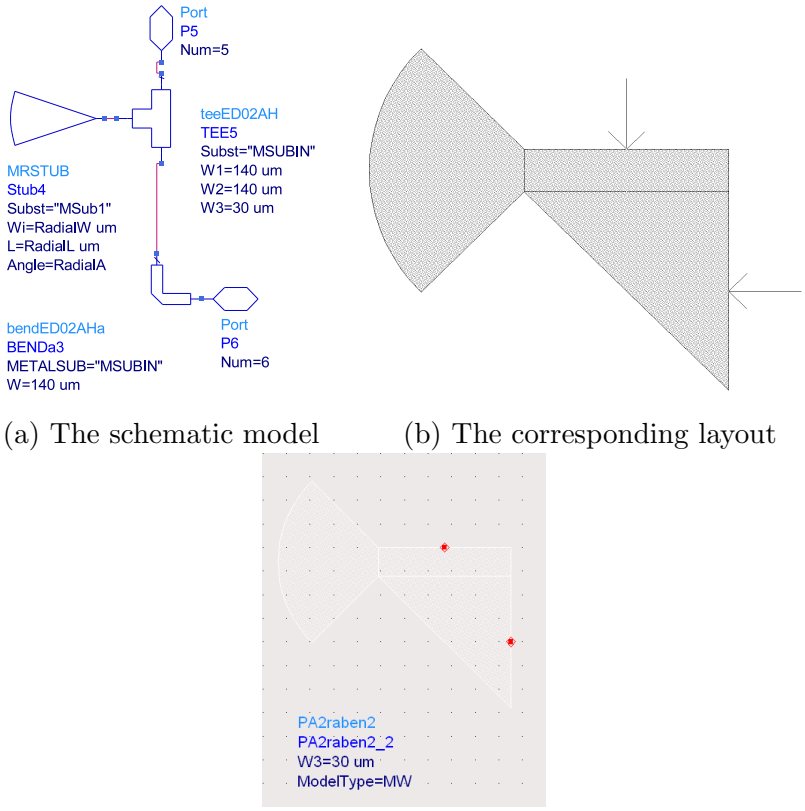


(a) T-Junction schematic model (b) T-Junction layout



(c) T-Junction EM model generated by AMC

Figure 4.36: T-Junction model in AMC design



(a) The schematic model (b) The corresponding layout

(c) The EM model generated by AMC

Figure 4.37: Multi-discontinuity model in AMC design

As these new models are produced by the EM method, they are more accurate than the schematic models. With these new models generated by AMC, the circuit will be re-analyzed as shown in Figure 4.38 to produce the final results.

4.11 Final Results

The discontinuity schematic models were replaced by the new models generated by AMC, and the whole circuit was re-analyzed with the results in Figure 4.39 and Table 4.7. The final results which represent the practical performance, differ a bit from the previous results after yield centering. Power gain is now about 15 dB when input power is 0 dBm, P_{1dB} reaches 18.3 dBm. $IMD3$ is -31 dBc when input power is 1 dBm, PAE is 15% when output power reaches P_{1dB} and peak PAE is 35%. As these results are based on EM analysis, they represent the practical circuit accurately. In Table 4.8, the final results are compared with other published designs. Though some figures are not as good as the those published, overall they are acceptable and show that the complex art of millimeter-wave

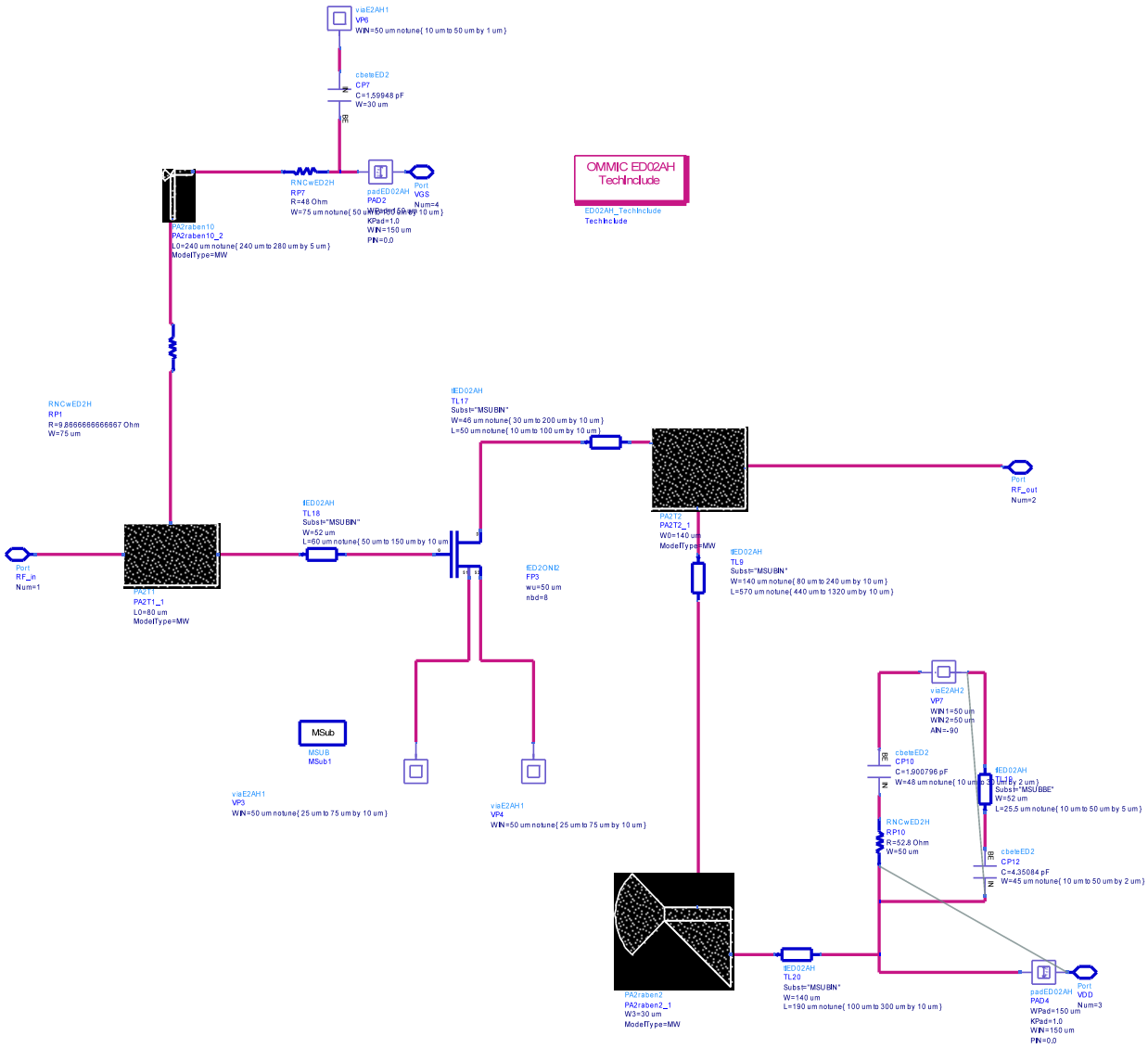
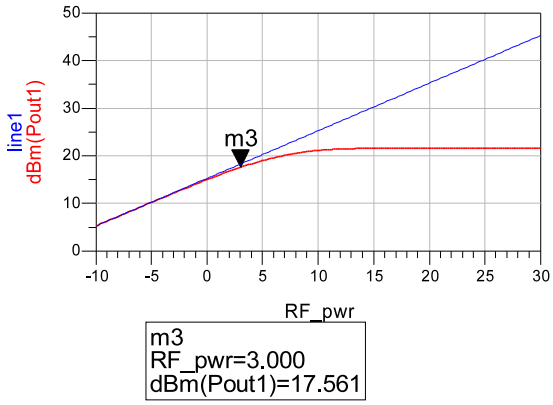
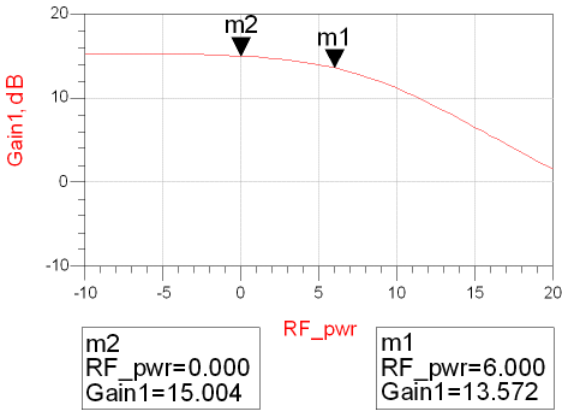


Figure 4.38: Stage level co-simulation

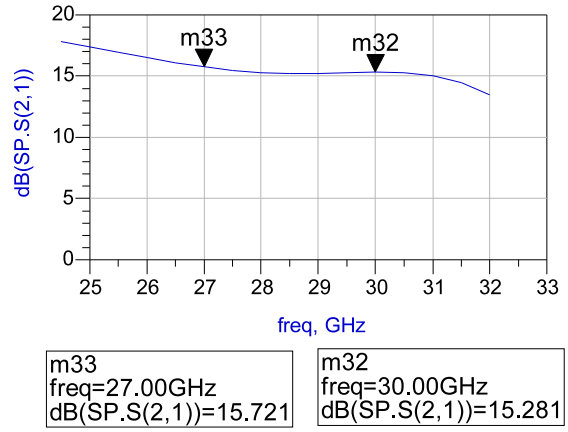
PA design has been mastered sufficiently to go on the novel predistortion circuit research.



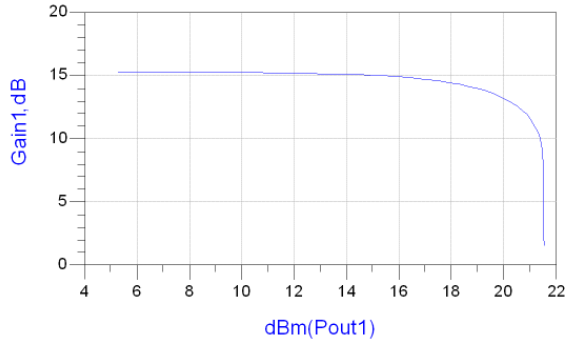
(a) Output power



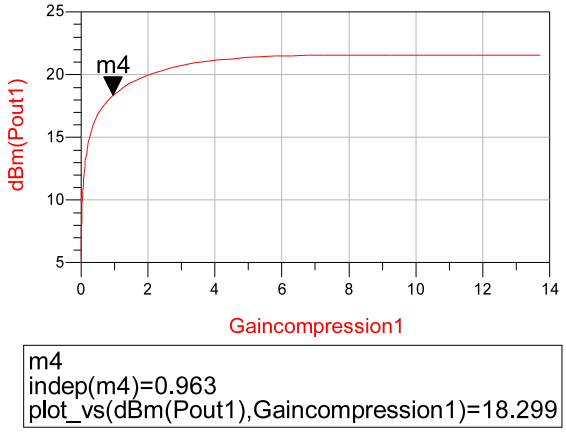
(b) Power gain



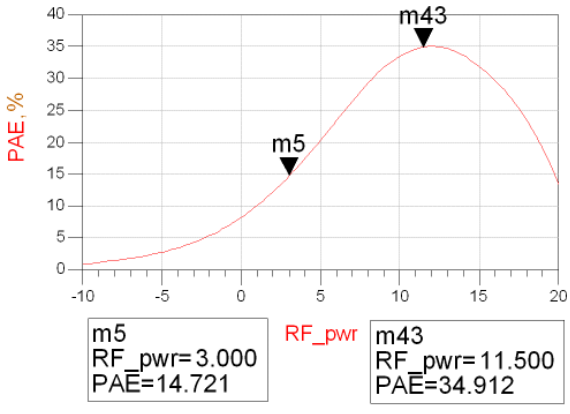
(c) Small signal gain S21



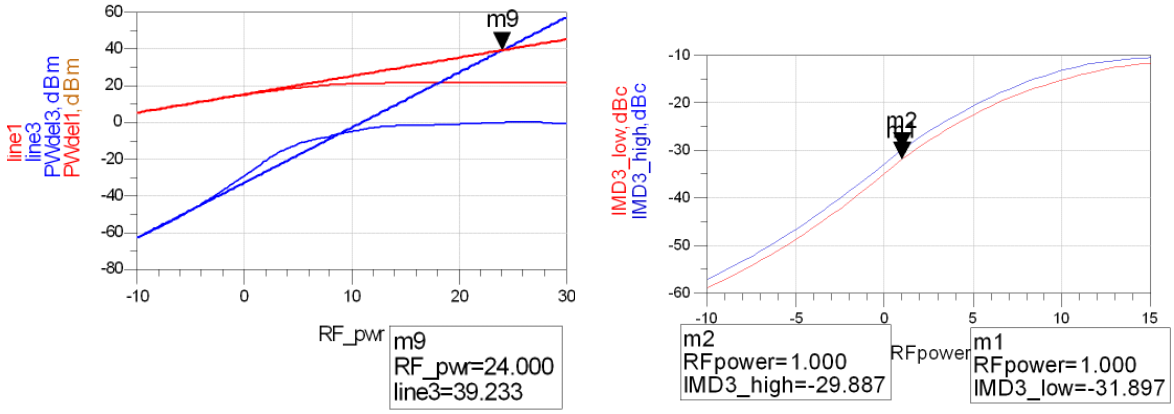
(d) Large signal gain



(e) Output power vs. gain compression



(f) Power-added efficiency



(g) OIP3 characteristic (h) $IMD3$ characteristic

Figure 4.39: Final design results

Table 4.7: Final Results

	Final Results	Specifications
Power Gain	15 dB	15∼ 20 dB
Small Signal Gain	15.5 dB	
Output Power, P_{1dB}	18.3 dBm	15∼25 dBm
$IMD3$ @ P_{1dB}	-31 dBc	Below -30 dBc
Linearity(OIP3)	39.2 dBm	
PAE @P_{1dB}	15 %	15∼30%
Peak PAE	35 %	

Table 4.8: Comparison with other designs

Circuit	Device Technology	Frequency Band	Small Signal Gain	P_{1dB}	PAE	Ref
PA	0.15 μm GaAs pHEMT	24∼28 GHz	16.7∼18.6 dB	17.5 dBm	19.8%	[34]
PA	0.15 μm GaAs pHEMT	27.5∼29.5 GHz	16 dB	32 dBm	35%	[28]
PA	0.15 μm GaAs pHEMT	27.5∼28.4 GHz	23 dB	33 dBm	N/A	[36]
PA	Packaged components	25.7∼31.15 GHz	9 dB	27 dBm	15.3%	[37]
PA	0.25 μm GaAs pHEMT	23∼26 GHz	29 dB	33 dBm	16%	[38]
Ours	0.25 μm GaAs pHEMT	27∼29 GHz	15.5 dB	18.3 dBm	15%	

4.12 Layout Design

Layout design is an important part of millimeter-wave circuit design and is quite different from layout of low frequency circuits as parasitic effects at tens of gigahertz must

be taken into consideration. The trade-off between cost and performance has been an important issue and has a great impact on the final result.

Generally speaking, to obtain high output power capacity of a FET, the total gate width has to be increased. A wide FET with a single wide gate finger could be one solution. But in that case, the gate resistance will be so high that signal loss will increase, the maximum available gain will decrease, and the noise will increase as well. Several fingers in parallel is a good solution to solve this problem. However, a wider FET structure may have a lower gain because of phase shift at the gate input feed point, nonuniform channel temperature and nonuniform operation from cell to cell [47]. So specific effort must be paid in the multi-finger FET design.

In a large cell such as the output stage power transistor, according to the design rules, the number of gate fingers should be less than or equal to eight and the unit gate width should be less than or equal to 50 μm to guarantee that the sources in the middle of the FET are correctly grounded and there is no phase shift between the gate fingers. The number of gate fingers is usually even in order to have a source pad on each side of the FET.

The parasitic elements near the FET source will degrade the gain due to negative feedback. In order to minimize these parasitic elements, the via-hole should be as large as possible and should be close to the FET source. The decoupling capacitor should be placed near the power supply and the discontinuities should be analyzed with the EM method. The issues of the FET and the layouts of passive elements have been considered in Section 4.4 and Section 4.8 where suitable decisions have been taken. Two versions of the layout for the millimeter-wave power amplifier were produced. One is shown in Figure 4.40 that is realized using straight lines. The area is 3335×2430 μm^2. Another version shown in Figure 4.41 employs bended lines. It has a smaller area of 3335×1650 μm^2, which saves about 32% of size compared with the layout using straight lines. Obviously the latter version with smaller area will be cost-saving.

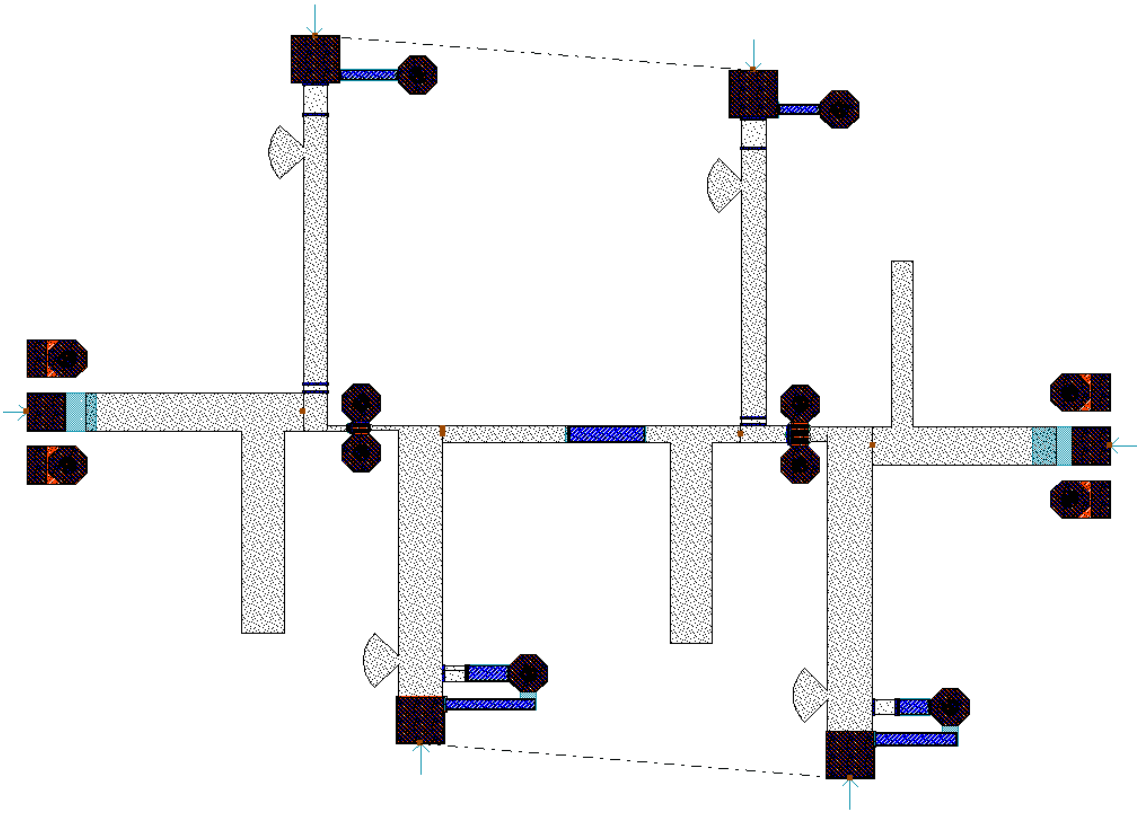


Figure 4.40: Circuit layout realized with straight line, with the area of 3335×2430 μm^2

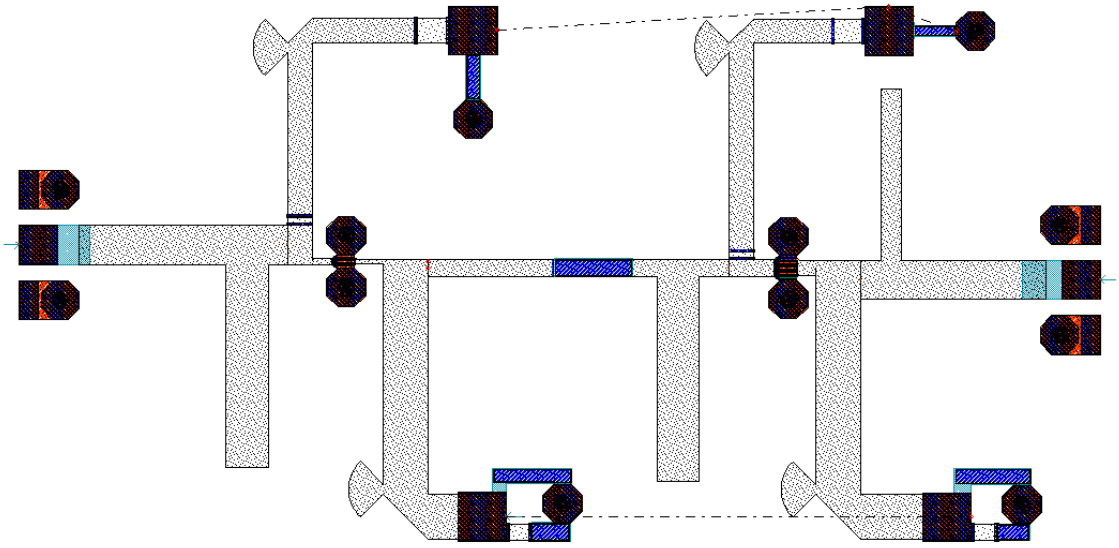


Figure 4.41: Circuit layout realized with bended line, with the area of 3335×1650 μm^2

4.13 Summary

In this chapter, a millimeter-wave power amplifier design for LMDS applications was designed as the linearization target in the next several chapters. The design flow was introduced and some key problems were discussed. Having completed this design to a high engineering and manufacturing standard, we now move on to predistortion circuit research that we can benchmark using this existing design. In the next chapter, the principle of predistortion technique will be introduced and existing predistortion circuits will be evaluated before considering innovative predistortion circuits.

Chapter 5

BACKGROUND ON AND EVALUATION OF SOME EXISTING LINEARIZERS

5.1 Background

Power efficiency and spectrum efficiency are key concerns in wireless communication systems. The pursuit of high power efficiency in communication systems generally requires that power amplifier in the transmitter operate near the saturation region while the demand on the spectral efficiency requires the system to be operated in a more linear way. When a non-constant envelope modulated signal goes through a nonlinear power amplifier, intermodulation distortion not only distorts the modulated signal, but also causes the power spectrum to overflow to the adjacent channels. As a result, both self-interference and mutual interference among neighboring channels degrade the communication quality seriously. When the frequency increases to the millimeter-wave band, as the working frequency approaches the device's maximum oscillation frequency, the role of the nonlinear elements will be greater and the distortion problem is much more serious than at lower frequencies. Just like all other communication systems which require distortion to be as low as possible, the severity of the linearity requirements for millimeter-wave communication systems are increasing [2–5]. Thus the linearization for power amplifier in millimeter-wave communication systems is a very important task.

Though many papers have been published on millimeter-wave power amplifiers from

Ku to W band, in most of the designs, great effort has been spent on output power and gain, while linearity, a key factor for the power amplifier, is often ignored [3–12, 63–67, 82]. In the rest of this thesis, linearity improvement for millimeter-wave power amplifiers will be the key issue of investigation.

5.2 Overview of Some Linearization Techniques

In order to avoid distortion and improve system performance, several linearization techniques such as feedback, feed-forward and predistortion, are applied to power amplifier design.

5.2.1 Feedback Technique

Broadly speaking, feedback technique can be broken down into four categories: RF feedback, envelope feedback, polar feedback and Cartesian feedback. Strictly speaking, the envelope feedback, polar feedback and Cartesian feedback should be referred as transmitter linearization techniques as each design is a complete transmitter rather than a simple linearized amplifier [83].

Feedback can suppress distortion as long as the feedback loop has sufficient incremental gain. To increase the loop gain, baseband error amplifiers can be used in Cartesian or polar form. The necessary up- and down-conversions inside the loop increase noise sources and loop delays, limiting the stable bandwidth of the linearizer [83].

The conventional RF feedback technique shown in Figure 5.1 is restricted to only narrow band application and suffers the drawback of gain loss of a similar degree to the distortion improvement, as well as the possibility of instability. In order to preserve stability and achieve good IMD improvement, the delay in the feedback path must be carefully taken into consideration [16]. The conventional feedback is often used to improve the broadband characteristic of a RF amplifier, rather than to improve its IMD characteristic or harmonic distortion properties.

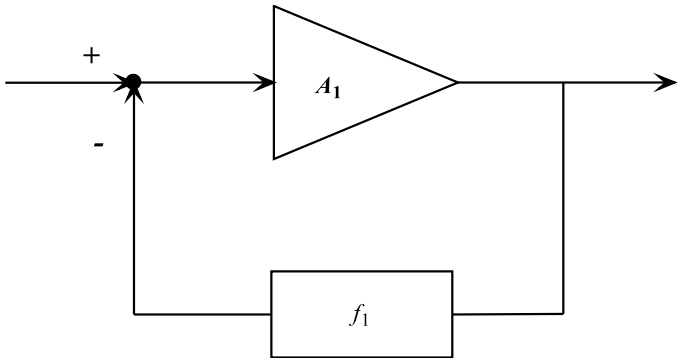


Figure 5.1: Feedback linearization technique

Details about the application of the feedback technique is given in References [88] and [83].

5.2.2 Feedforward Technique

Its popularity is largely due to the ability to linearize wide-band, multi-carrier signals. This technique is conceptually simple, but can be rather costly to implement in hardware. Rather than pre-distort the signal prior to the power amplifier, the error generated by the power amplifier is amplified, and this amplified error is subtracted from the output of the power amplifier.

Feedforward is commonly used in wide-band amplifiers. As shown in Figure 5.2 the distortion generated in the main amplifier is extracted by subtracting the linear contribution from the output of the main amplifier. This distortion signal is amplified by an auxiliary amplifier and finally subtracted from the output. As this arrangement does not contain a feedback loop, it has no stability limitations, but the bandwidth of the combiners and phase shifters limits the cancelation bandwidth. The phase shifters and attenuators needed in the feedforward loop are quite tricky to tune automatically, and the use of the linear auxiliary amplifier noticeably reduces the overall efficiency [83].

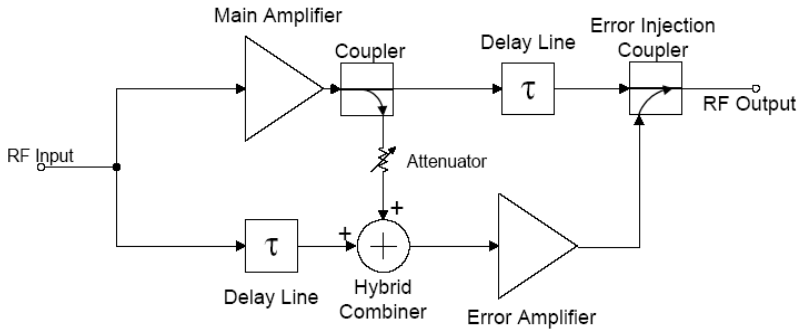


Figure 5.2: Feedforward linearization technique [16]

Feedforward technique can offer the most superior linearity improvement, but the disadvantages of requiring extra error amplifier leads to bulky size and limits it to the base station applications. Details about the application of the feedforward technique is given in References [83] and [84].

5.2.3 Envelope Elimination and Restoration

A variation of the feedforward technique is envelope elimination and restoration (EER), which is also known as the Kahn technique.

This technique splits the amplitude and phase information from each other as shown in Figure 5.3. The phase information is passed directly to the power amplifier, which operates in a completely non-linear way. The amplitude information is ideally eliminated from the carrier before carrier amplification. During carrier power amplification, the envelope is typically restored onto the carrier by driving the power amplifier's bias supply with the original envelope. To restore the envelope information, the final PA stage is amplitude modulated via the DC bias of the PA. This technique may be accomplished with analog or DSP techniques [84].

Excellent performance can be obtained due to the fact that high efficiency switching power amplifiers may be used to amplify the constant envelope signal. Ideally 100% efficiency may be attained. However, this technique is limited to modest levels of envelope variation. Large envelope variations may drive the PA transistor bias into cutoff resulting in significant distortion. EER is very sensitive to any time or phase difference between the carrier path and the supply modulating path, containing amplitude information only. Details about the application of the EER technique is given in References [83] and [84].

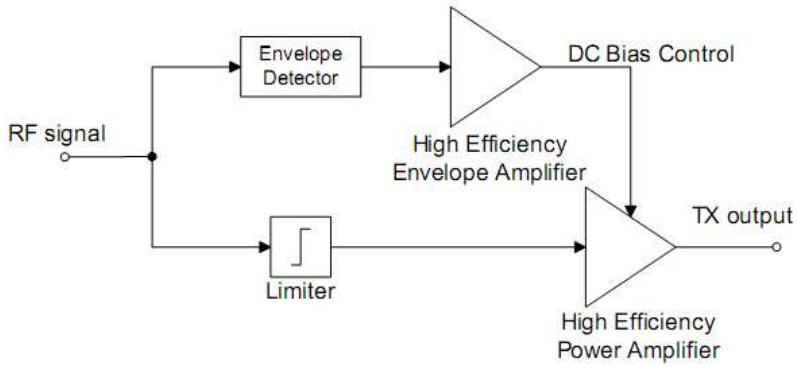


Figure 5.3: EER linearization technique [16]

5.2.4 LINC

The Linear Amplification Using Nonlinear Components, LINC technique uses a DSP to generate two constant envelope phase-modulated baseband signals, which, after up-conversion and nonlinear power amplification, will produce the required linear output signal upon final summation. Any unwanted nonlinear elements remaining in the signal before summation will be opposite in phase in each path and will cancel upon summation. This method also makes use of high efficiency switching amplifiers to achieve efficiencies theoretically approaching 100% [16].

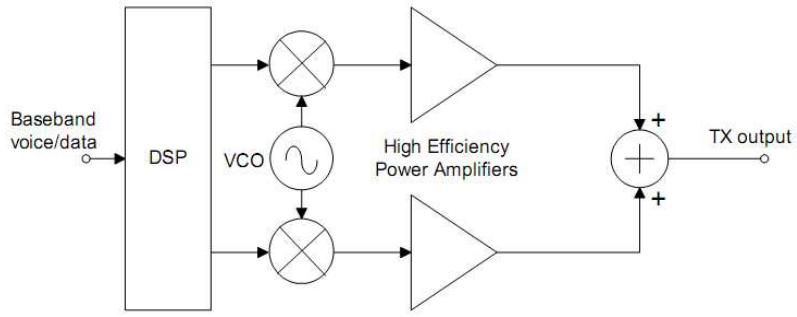


Figure 5.4: LINC linearization technique [16]

The main drawback of this technique is that gain and phase balance must be tightly controlled in the two RF paths in order to obtain the desired output waveform. Details about the applications of the LINC technique is given in References [83] and [84].

5.3 The Principle of Predistortion Technique

The predistortion approach has been proven to be one of the most effective methods that can improve linearity with minimal effect on other metrics [16–25]. Predistortion linearization can provide very useful distortion improvement at little extra cost and impact on output power. It also has the advantages over other techniques in terms of miniaturized size, low complexity and stable operation [17].

Using transfer characteristics inverse to those of the nonlinear amplifier to distort the input signals, this technique aims to introduce "inverse" nonlinearity that can compensate the AM/AM and AM/PM distortion generated by the nonlinear amplifier and generate linearized signals at the PA output. The principle of predistortion technique is illustrated in Figure 5.5.

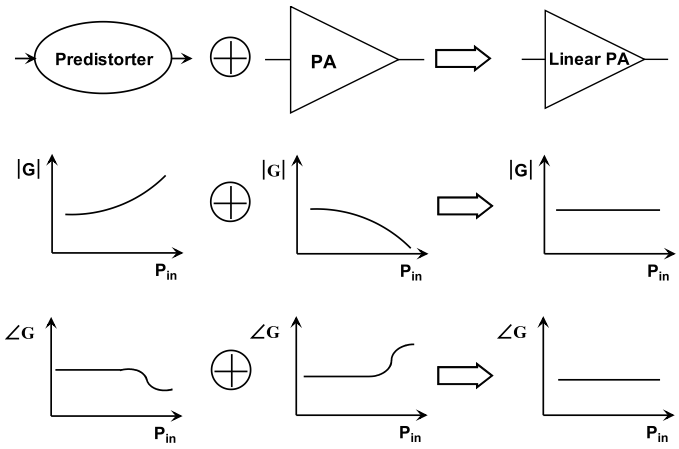


Figure 5.5: The principle of predistortion technique

Low cost, low complexity and reasonable improvement make this approach especially suitable for mobile applications. Compared with other linearization techniques, predistortion technique has the unique advantages of being situated where insertion loss is not critical and bandwidth limitation is less [16].

Predistortion linearization techniques can be roughly subdivided into digital predistortion and analog predistortion [21]. Digital predistortion technique mainly employs DSP to pre-distort the baseband information before upconversion [83]. This technique is mostly used in conjunction with the transmitter system where designers have access to the unmodulated baseband signal, and it may not be a cost effective solution for some applications. Much research on the data approach is focused on algorithm innovations [18–25].

For analog predistortion linearizers, a nonlinear generator is inserted between the input signal and the power amplifier. The nonlinear generator generally consists of active devices which are biased to produce intermodulation products that cancel out those of the nonlinear power amplifier.

5.4 Latest Developments in Predistortion Circuits

As mentioned in Section 5.3, there has been intensive research on predistortion techniques and much current predistortion research focuses on the algorithm innovations in the field of digital predistortion [18–25, 41–43].

Kyoung-Joon Cho *et al.* [41] presented a multi-order predistortion using a second harmonic based technique as shown in Figure 5.6. The operational principle was analyzed using Agilent ADS and this work achieved an $ACPR$ improvement of 11 dB for W-CDMA power amplifier at 2.1 GHz.

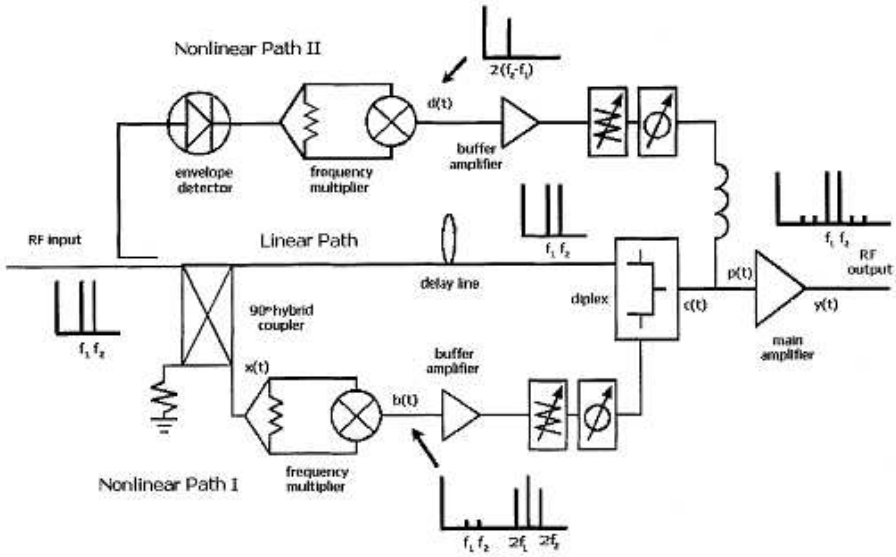


Figure 5.6: Principle of a multi-order digital predistortion [41]

Pascale Jardin and Geneviève Baudoin [42] proposed a filter lookup table(LUT) method for power amplifier linearization as shown in Figure 5.7. The predistorter device consists of a lookup table gain followed by a codebook of filters addressed by the index of the LUT. The adaptation is derived from direct learning for the LUT gains and indirect learning for the filter coefficients. Simulations showed that $ACPR$ can be improved by 19.3 dB.

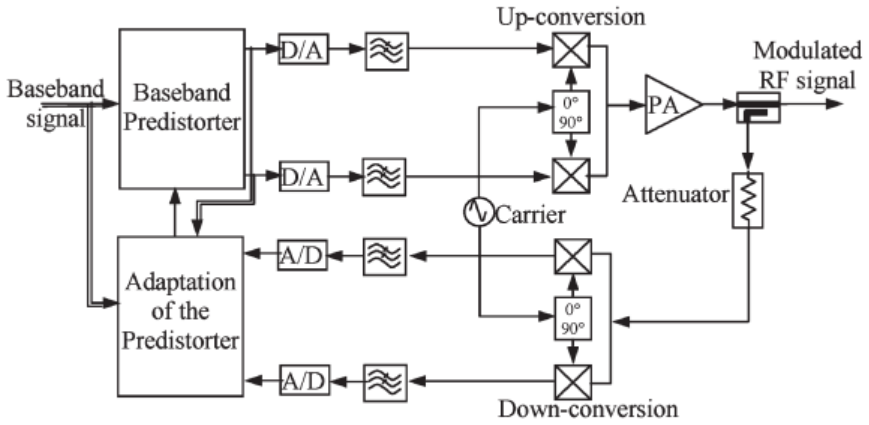


Figure 5.7: Principle of a LUT digital predistortion [42]

Young Yun Woo and Jangheon Kim [43] developed an adaptive digital predistortion linearization technique based on analog feedback predistortion as shown in Figure 5.8. The lookup-table-based feedback can overcome the bandwidth limitation of the feedback circuit due to the loop delay, and suppress feedback oscillation by accurate digital control of the feedback signal. An improvement of the $ACPR$ by 15 dB at an average output power of 43 dBm has been achieved for a 180-W power amplifier.

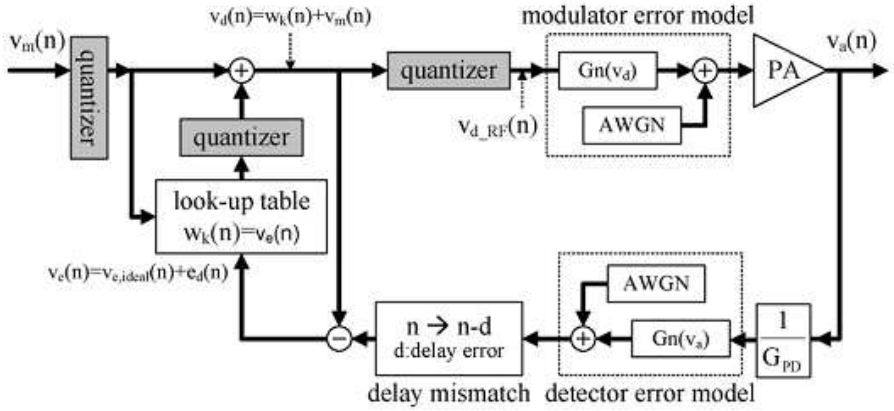


Figure 5.8: Principle of an adaptive digital predistortion [43]

Although these results seem exciting, it usually involves a complicated algorithm and is not suitable for many practical cases, especially for mobile applications.

Analog predistorters usually employ a nonlinear resistive element such as a diode or an FET channel as an RF voltage-dependent resistor. They rely fundamentally on the nonlinear characteristics of the predistortion device to compensate the distortion [84]. They can be configured to provide higher attenuation at low drive levels and lower attenuation at high drive levels. Some attenuation characteristics allow a tradeoff between

low-level insertion loss and the useful range of gain expansion. Some existing analog linearizers will be evaluated in Section 5.5. As they are simple in structure, the function and performance improvement are quite limited. They tend to suffer from some problems such as relatively large insertion loss, and the simple structures used up till now cannot produce adequate compensating gain and phase characteristics.

Up till now, almost all the predistortion circuits operate at RF frequencies [16–25, 41–43]. In this work, we will extend the predistortion technique to millimeter-wave applications and try to develop effective solutions for linearity improvement for millimeter-wave power amplifiers.

5.5 Evaluations of Some Existing Analog Linearizers

There are two kinds of analog predistorters published that may be suitable for the practical integration in mobile applications. One is the predistorter using a diode device [16] and the other is the predistorter using an HJFET device [17]. In this section, these two kinds of linearizers will be introduced and evaluated.

5.5.1 Diode Linearizer

In general, minimum insertion loss(IL), maximum return loss(RL), and AM-AM and AM-PM conversion characteristics that can compensate the PA's own characterictics are desired. In the predistorter shown in Figure 5.9, the diode may be considered equivalent to a nonlinear resistor (R_D) with a parasitic capacitance (C_P) in parallel [16]. The diode should be forward biased near the turn-on voltage to set R_D and C_P at a small-signal operating point. The I-V curve of the diode is shown in Figure 5.10. As the diode is operated under a forward bias, its nonlinear C/V characteristic can be neglected. The resistance and capacitance are used to form a nonlinear RC phase shift network. As the diode is driven beyond small signal condition, the diode rectifies the RF power and the operating point changes with increasing input power [16]. A diode in the OMMIC design kit ED02AH [27] is simulated to demonstrate the impact of the equivalent R_D and C_P and the results are shown in Figure 5.10 to Figure 5.12. R_D decreases with increasing input power since its operating point is moved up the I/V curve as shown in Figure 5.10 and Figure 5.11 respectively, resulting in a change in gain and phase shift with increasing

input power [16]. Additional capacitance may be added in parallel in order to adjust the turn-on impedance and predistortion characteristic as shown in Figure 5.12.

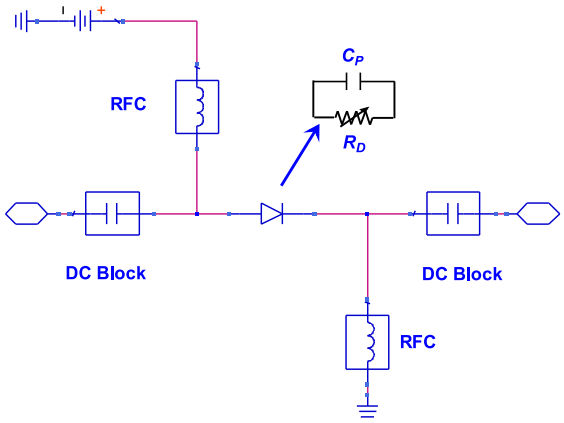


Figure 5.9: Simple predistorter in form of diode [16]

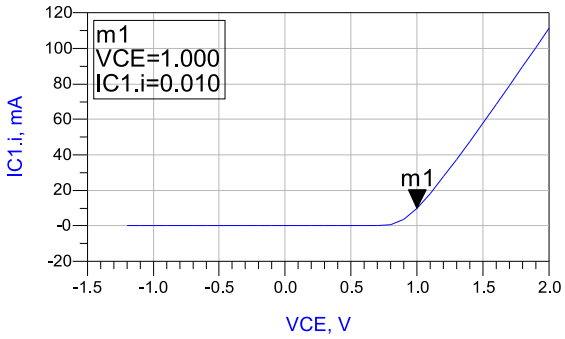


Figure 5.10: I-V curve of the diode in the OMMIC process

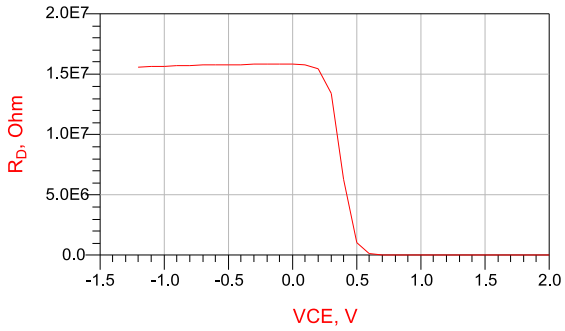
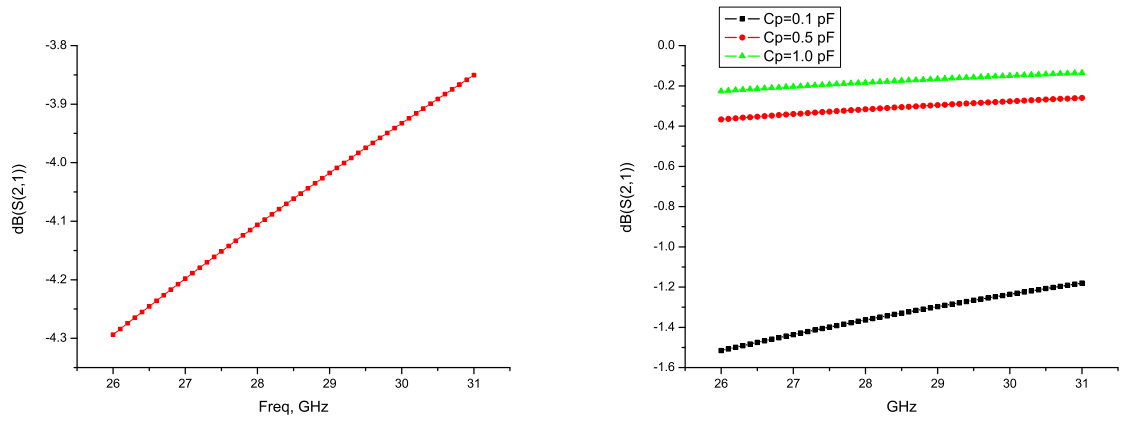


Figure 5.11: R_D of the diode in the OMMIC process

This linearizer was first used in a fully integrated 1.95 GHz power amplifier implemented by an AlGaAs/GaAs HBT device [16]. With this design, the lower channel $ACPR$ was improved by about 3 dB and the upper channel $ACPR$ was improved by about 0.1 dB at the output power of 15 dBm. The insertion loss reaches -4 dB and gain deviation



(a) The insertion loss of the diode without C_p (b) The insertion loss of the diode with C_p

Figure 5.12: Analysis results of the impact of C_p

is about 1dB when input power is swept from -20 dBm to 0 dBm [16].

In order to evaluate the diode predistorter, a two-stage power amplifier for CDMA application designed by the author previously in Reference [89] was chosen. This power amplifier works at around 2.4 GHz and is based on InGaP/GaAs HBT. As rest of the work is aimed at pHEMT technology, this evaluation is introduced briefly. Large-signal VBIC models were extracted from a cell with the emitter size of 3×15 μm^2 [89]. Part of the predistorter is shown in Figure 5.13.

The $ACPR$ specification was simulated with the IS-95 Reverse Link CDMA Signal Source (1.2288 MHz primary channel bandwidth, 30 KHz adjacent channel bandwidth and ± 885 KHz frequency offset) and the results are shown in Figure 5.14. In Figure 5.14 the $ACPR$ with the linearizer and without the linearizer are -58.6 dBc, -52.6 dBc and -43.9 dBc, -42.2 dBc at upper channel and lower channel respectively and the $ACPR$ improvement are about 9.5 dB and 10.4 dB respectively though the insertion loss is about 3.1 dB. Though the linearity improvement is satisfactory, a considerable proportion comes from the power back-off since the insertion loss is relatively large. Detailed discussions on the effect of the power back-off will be carried out in Section 8.6.1 in Chapter 8. These results confirm the basic feasibility of the diode linearizer but betray the limitation of relatively large insertion loss. The main reason why the results of this evaluation are much better than in Reference [16] is that the InGaP/GaAs HBT we chose here has much higher performance than AlGaAs/GaAs HBT in Reference [16].

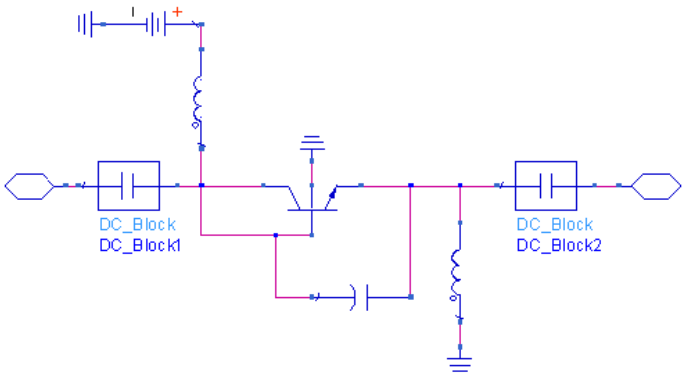


Figure 5.13: Part of the predistorter used in evaluation

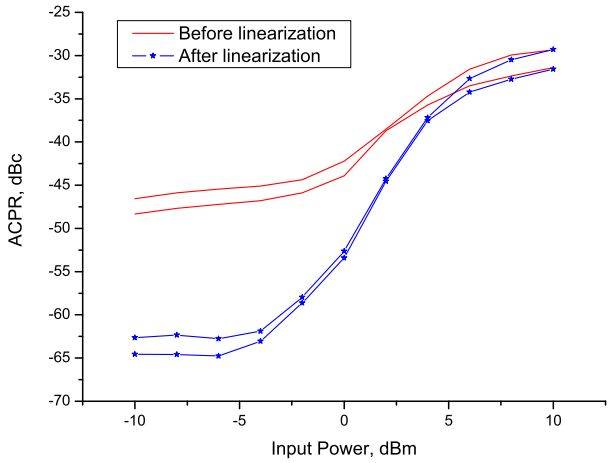


Figure 5.14: ACPR comparision

As discussed above, the main problems with this RF diode linearizer in Reference [16] are the relatively large insertion loss. In the next chapters, some effective predistorters for millimeter-wave PAs will be proposed to solve these problems.

5.5.2 Unbiased FET Linearizer

5.5.2.1 Principle of Operation

A predistortion circuit using a FET is shown in Figure 5.15 [17]. It employs an HJFET as the nonlinear element, and was designed in Reference [17] to linearize an amplifier with gain compression and phase expansion. The characteristic of the predistorter is determined by the drain-to-source resistance (r_{ds}) of the HJFET, which is a function of V_C. To obtain gain expansion, r_{ds} should decrease with increasing the input power. Such

a condition in theory can be achieved when the HJFET is biased near pinch-off [17] as shown in Figure 5.16.

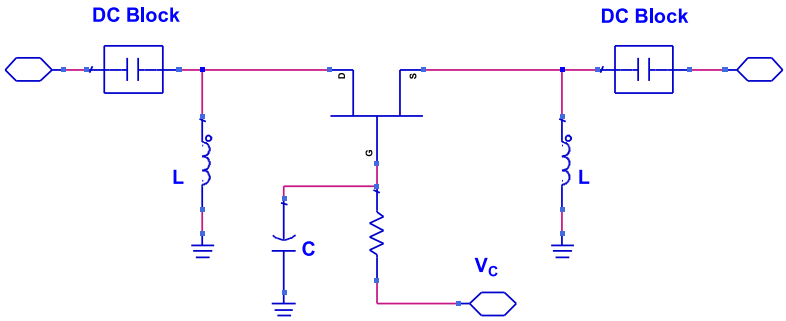


Figure 5.15: Simple predistorter in form of HJFET [17]

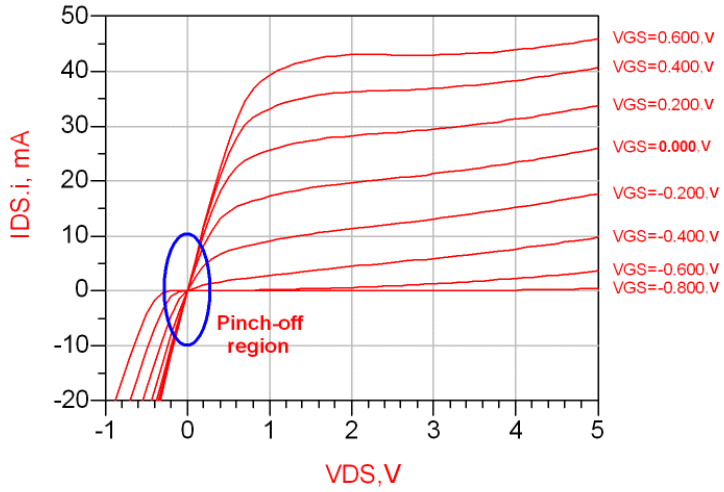


Figure 5.16: Typical FET I-V curves

The HJFET in Figure 5.15 is biased as a variable resistor, where the drain (D) and source (S) are biased through inductors to ground, and the gate (G) is connected to ground via a capacitor. Two capacitors are employed at the input and output of the predistorter for DC blocking and matching purposes. A bias control voltage (V_C) is applied to the gate of the device through a bias resistor. Inductors help produce a negative phase deviation for the predistorter. By reducing the values of L and C, the degree of negative phase deviation can increase without affecting the gain expansion level. Thus, the L and C values can be optimized to fit the phase characteristic required.

This linearizer has been used in a W-CDMA power amplifier design [17]. $ACPR$

was reported to be improved by 5 dB and the insertion loss is about -3.5 dB. Relatively high insertion loss is still one of problems of this HJFET linearizer.

5.5.2.2 Evaluation of FET Linearizer

A predistortion circuit using pHEMT technology from the OMMIC process is proposed as shown in Figure 5.17. This circuit is based on the principle discussed above and is used to evaluate the FET linearizer in Reference [17].

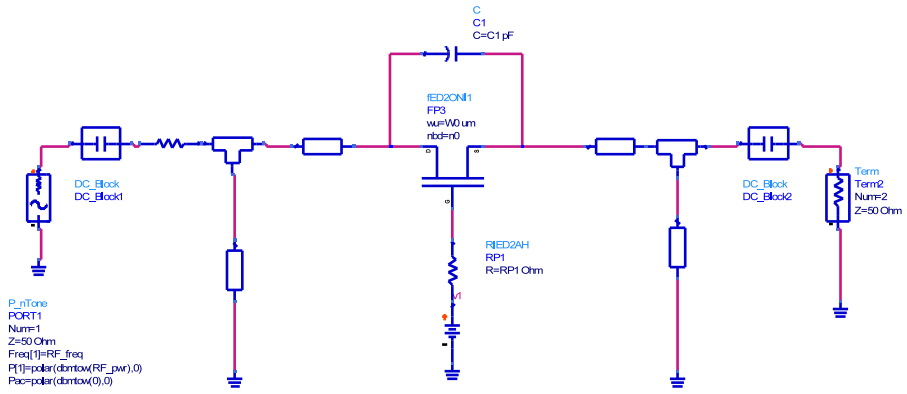
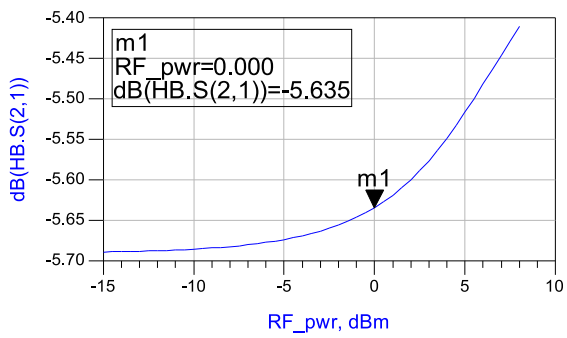


Figure 5.17: Predistorter with common gate FET

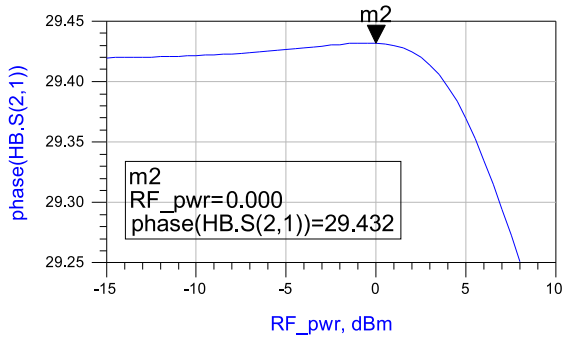
In the topology in Figure 5.17, the drain and source of the FET are biased via short-circuited stubs. By adjusting the length and width of the short-circuited stubs, their equivalent inductance will be changed. This can be used to adjust the phase characteristic. The FET realizes the nonlinear conductance function near the pinch-off region in Figure 5.16. The gate voltage is used to control the drain-to-source resistance to implement the predistortion function. The capacitor C1, in parallel with the drain-to-source resistance, provides a low resistance RF path, which lessens the impact of the channel resistance on the insertion loss.

Preliminary analysis results obtained from Agilent ADS are shown in Figure 5.18. As there is no RF power amplifier built on FET device available as the test bench, we can only analyze the nonlinear characteristics of the predistortion circuit. The gain expansion and phase compression characteristics are shown in Figure 5.18 (a) and Figure 5.18 (b). But the results in Figure 5.18 show that the insertion loss is rather large and the changes in gain and phase is small. From the results shown in Figure 5.18 (f), we can see that the input $VSWR$ is only about 1.339, so an input matching network is required to improve

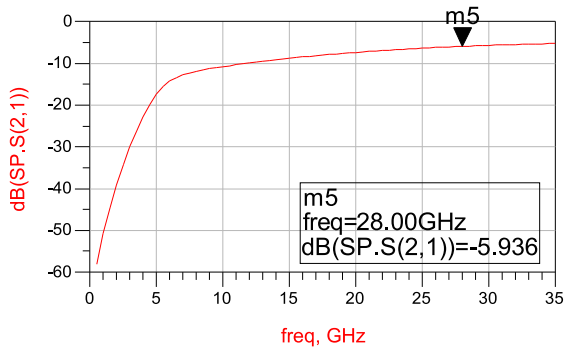
the matching status.



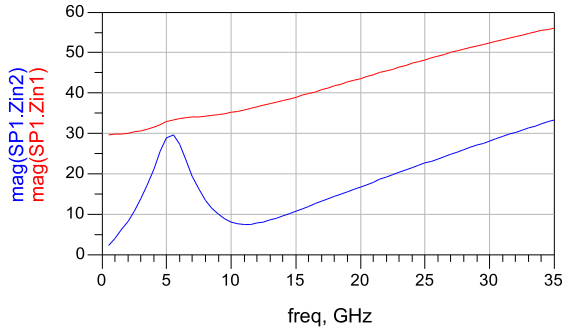
(a) Gain expansion characteristic



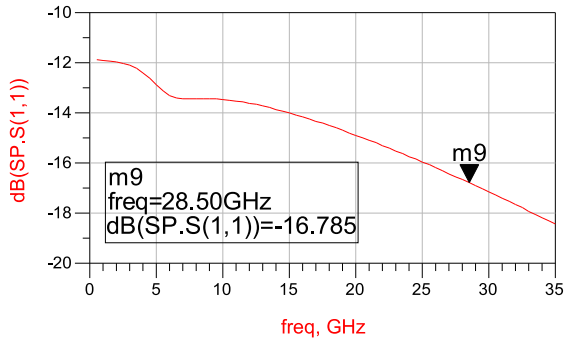
(b) Phase compression characteristic



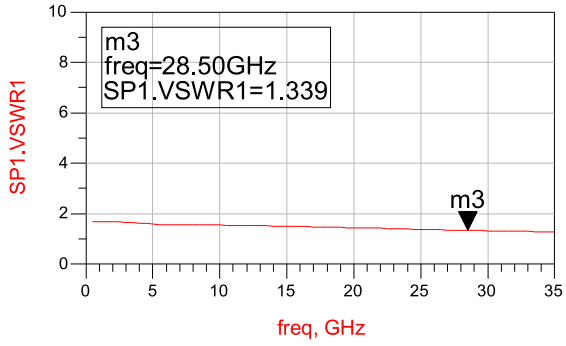
(c) Small signal S21



(d) Input and output impedance



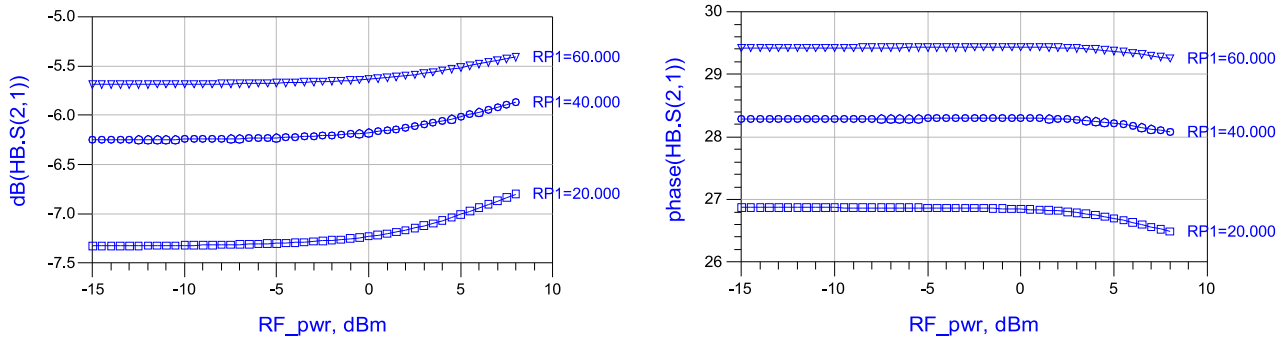
(e) S11, Input matching status



(f) $VSWR$, Input matching status

Figure 5.18: Analysis results of common gate configuration

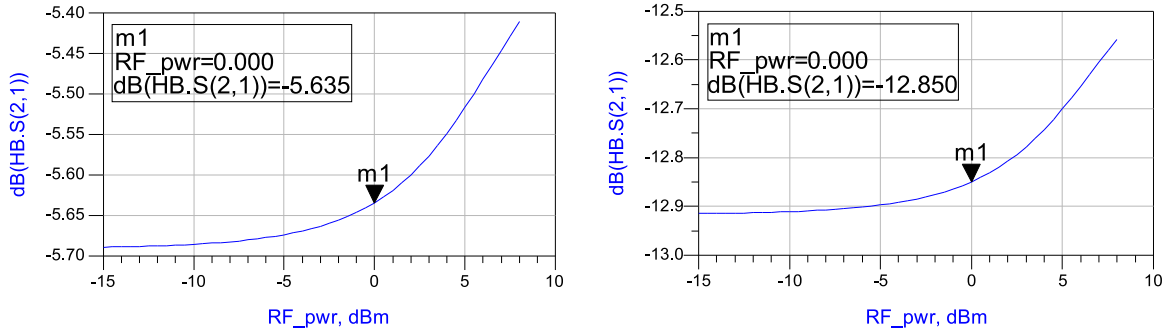
In this configuration, RP1 and C1 in Figure 5.17 affect the performance significantly. As shown in Figure 5.19, when the bias resistor RP1 increases, the insertion loss will decrease while the phase will increase.



(a) Amplitude characteristic sweep analysis (b) Phase characteristic sweep analysis

Figure 5.19: RP1 sweep analysis

As far as C1 is concerned, it significantly modifies the effect of the drain-to-source resistance, which in turn affects the insertion loss. The insertion loss increases from 5.635 dB with C1 to 12.850 dB without C1. Thus there is a big difference between the case with C1 and the case without C1, and this is shown by the comparison between them in Figure 5.20. Obviously C1 can effectively decrease the drain-to-source resistance effectively and lower the impact on the insertion loss.



(a) S(2,1) with C1 (b) S(2,1) without C1

Figure 5.20: Analysis results of the impact of C1

The main disadvantages of this predistortion circuit is relatively large insertion loss and relatively small linearity improvement, which are the common problems of simple predistortion circuits. Thus this circuit cannot meet our requirements.

5.6 Summary

In this chapter, some linearization techniques have been reviewed and the principle of predistortion technique was introduced in general terms. Some existing analog linearizers were evaluated to verify their characteristics. Generally speaking, these predistorters are quite simple and the functionality and performance improvement are very limited. Some problems such as relatively large insertion loss, and inability to produce sufficient nonlinear gain and phase characteristics indicate the need for further research. In the next several chapters, new kinds of predistortion circuits which are expected to solve these problems will be proposed and evaluated.

Chapter 6

PREDISTORTION CIRCUIT REALIZED BY AN AMPLIFIER WITH A FIXED BIAS CIRCUIT

6.1 Introduction

Relatively large insertion loss has been one of the most serious problems faced by the conventional predistortion circuits [16,17,20,22]. In this chapter, a novel predistortion circuit realized by an amplifier with a fixed bias circuit is proposed. This predistortion circuit can solve the problem of insertion loss with the benefit of improving other metrics simultaneously.

6.2 Design Principle of the Predistortion Circuit

During the research, it is found that predistortion circuit can be realized by an amplifier with a fixed bias condition with proper configuration. By choosing the bias voltage carefully in the class AB region, the circuit can realize predistortion function while providing the power gain. Figure 6.1 is a simple common source amplifier based on OMMIC pHEMT technology. Figure 6.2 shows the relationship between the power gain and input power at different bias voltages for the amplifier in Figure 6.1.

Figure 6.2 (b) is part of Figure 6.2 (a) with annotations. In Figure 6.2 (b), if we pick the peak gain point from each curve, then the left part of the peak gain point falls in

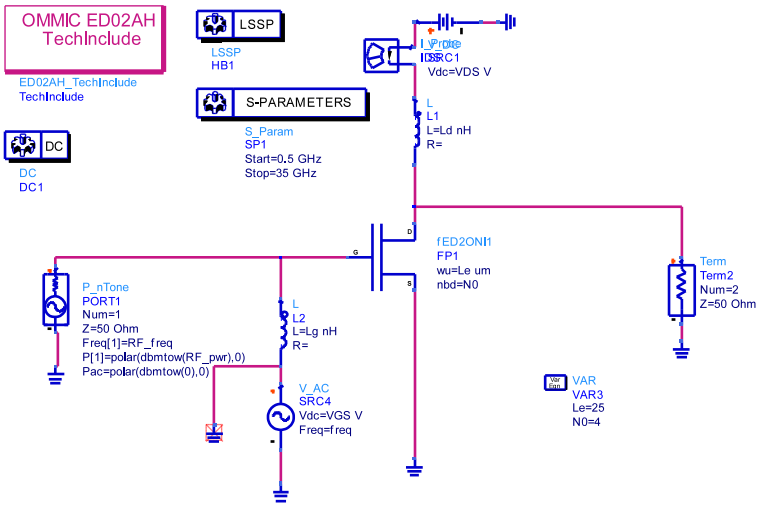
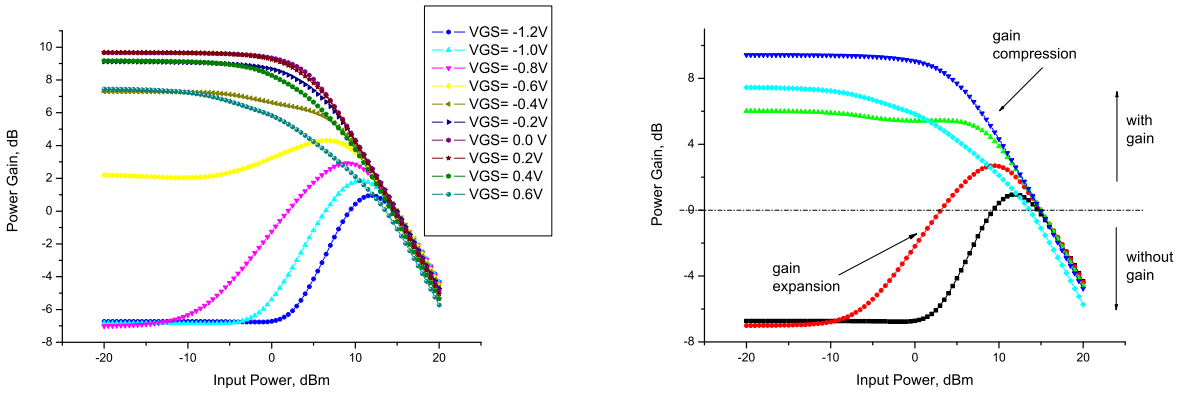


Figure 6.1: Simple common source amplifier



(a) Power gain at different bias conditions (b) Region divisions at power gain curves

Figure 6.2: Typical gain levels at different bias voltage

the gain expansion region as the gain increases with increasing input power while the right part is characterized as the gain compression as the gain decreases with increasing input power. On the other hand, the curve where the power gain is more than 0 dB can be called 'with gain' and the curve where the power gain is less than 0 dB can be called 'without gain'. Using this, the typical curves in Figure 6.2 can be divided into four regions as stated in Table 6.1. The relationship between the four regions and power gain can be expressed quantitatively and can be shown in Figure 6.3. The X axis in Figure 6.3, representing the power gain, corresponds to the Y axis in Figure 6.2. The gain expansion in Y axis can be expressed quantitatively by the power gain at different input power subtracting the minimum power gain in the gain expansion region. Similarly the gain compression can be expressed quantitatively by the power gain at the different input power subtracting

the maximum power gain in the gain compression region. With Figure 6.3, we can see clearly that there is a small region where there is the gain expansion while gain is still positive. That is, with proper bias configuration, the amplifier can have the predistortion characteristic with positive gain.

Table 6.1: Four regions of PA operation

Region 1	Gain expansion with gain
Region 2	Gain expansion without gain
Region 3	Gain compression without gain
Region 4	Gain compression with gain

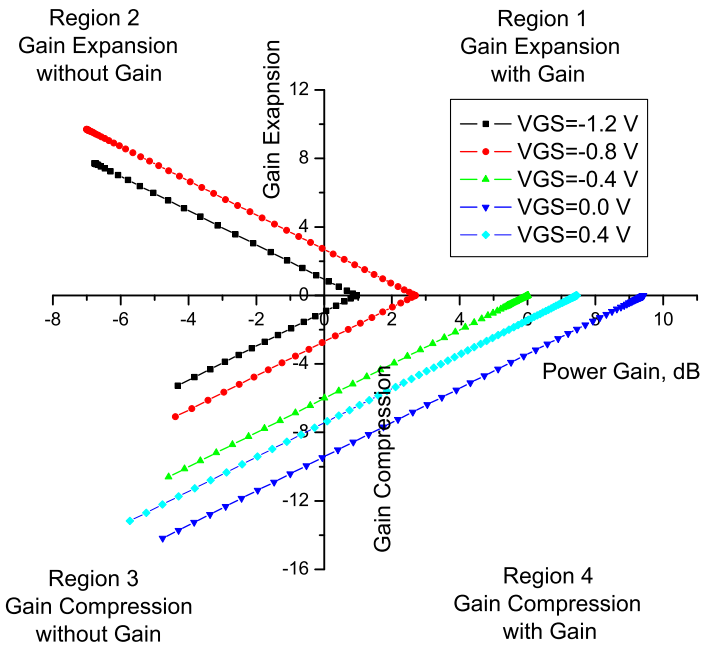
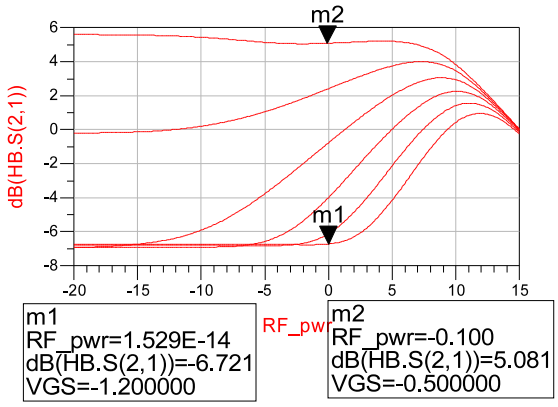


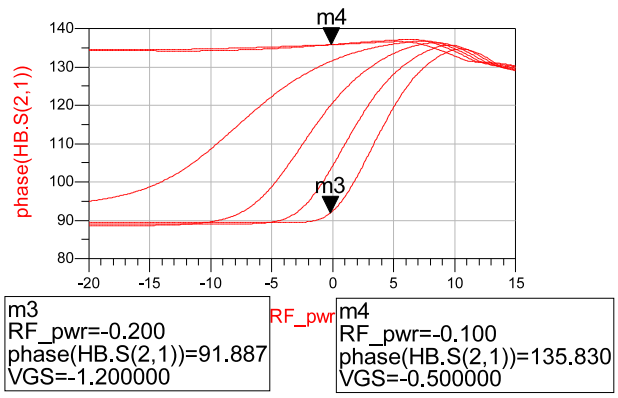
Figure 6.3: Four regions corresponds to the FET curves

In order to locate the suitable bias condition, the insertion loss is plotted verse input power at different bias voltages and the results are shown in Figure 6.4. From Figure 6.4 (a) we can see that when the bias voltage is in the range of -1.2 V and -0.5 V, the circuit can exhibit gain expansion, corresponding to Region 1 and Region 2 in Figure 6.3. That is, the amplifier alone can realize the predistortion function without extra circuit. More

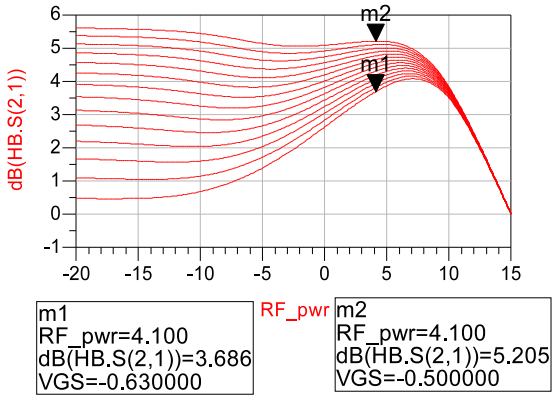
details at different bias conditions are shown in Figure 6.4 (c). From Figure 6.4 (c) when the bias voltage is in the range of -0.63 V and -0.5 V, corresponding to the power gain of 3.67 dB and 5.21 dB, the circuit can have gain expansion while the gain is still positive, corresponding to Region 1 in Figure 6.3. So if the amplifier is biased in the Region 1 with proper configuration, then it can linearize the power amplifier in the main stage without the burden of insertion loss. As the predistortion circuit is primarily comprised of an amplifier, it can bring extra benefits besides improved linearity, such as increased power gain and output power, improved PAE and so on.



(a) Gain characteristics



(b) Phase characteristics



(c) Detailed positive gain expansion characteristic

Figure 6.4: The bias voltages that can lead to predistortion function

6.3 Designing of the PD from PA characteristics

As this predistortion circuit is targeted to linearize millimeter-wave power amplifier, the millimeter-wave power amplifier designed in Chapter 4 is used for evaluation and comparison. During the design, it is very important to highlight its advantage, that is,

the predistortion circuit with a fixed bias circuit can not only linearize the nonlinear power amplifier but also improve other metrics such as power gain and output power, which is quite different from the conventional predistortion circuits.

In order to realize the expected improvement, it is very necessary to adjust the size of the transistor to provide the necessary power gain and select the bias voltage to realize the predistortion function. According to the gain and phase characteristics of the millimeter-wave PA designed, in order to have the gain expansion and positive gain simultaneously, the bias voltage should be chosen between -0.63 V and -0.5 V as stated in Section 6.2. In Figure 6.5, several $IMD3$ at different biases are shown and compared. As the bias voltage of -0.62 V can bring a relatively large linearization range, which can cover the most used power range, thus this voltage is the optimum choice. The size of the transistor was chosen to be 8×15 μm as this size can provide necessary gain with this bias condition.

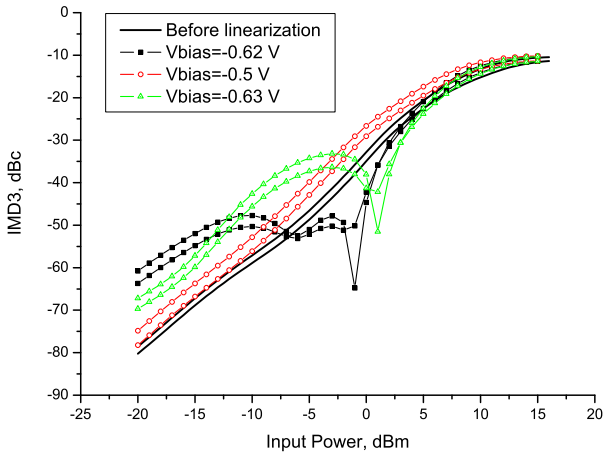


Figure 6.5: Linearization range at different biases

An input matching network and an output matching network with microstrip components were designed to translate the impedances to 50 Ohm. With such a design, the predistortion circuit can be connected with the nonlinear PA easily and linearize the amplifier without adding difficulty to the PA design. Figure 6.6 is the predistortion circuit with matching networks.

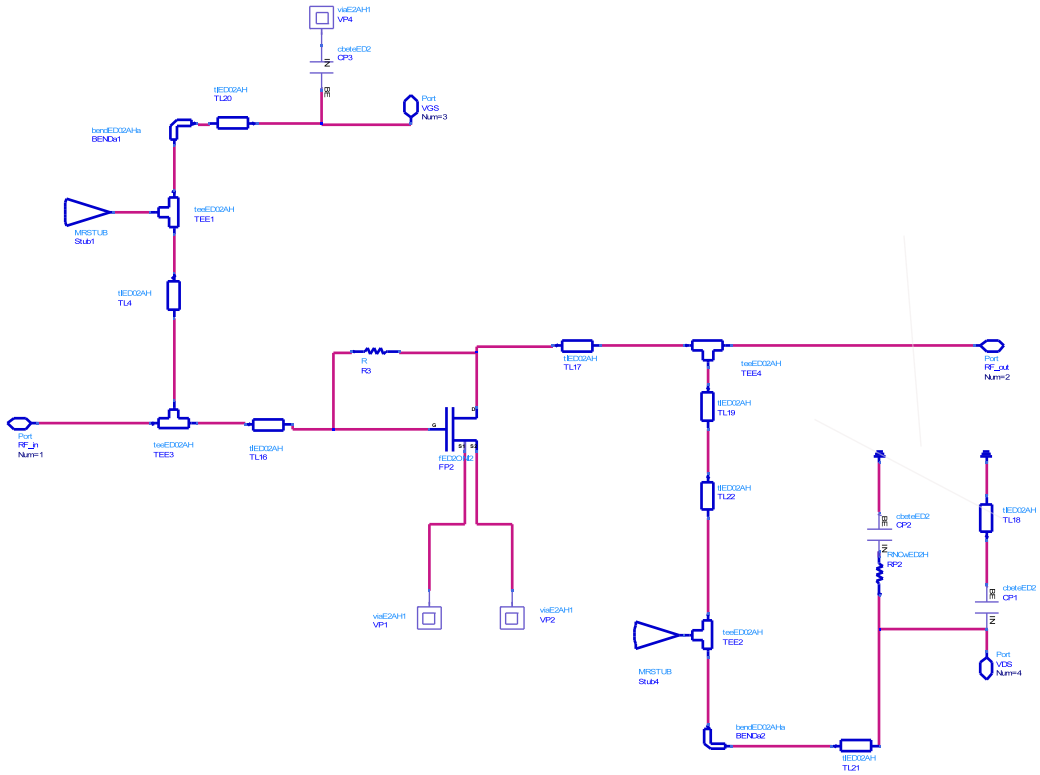
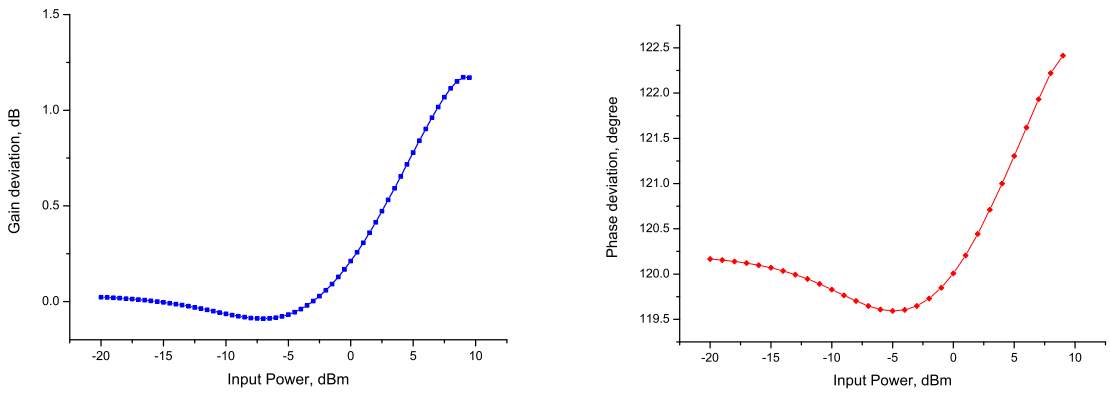


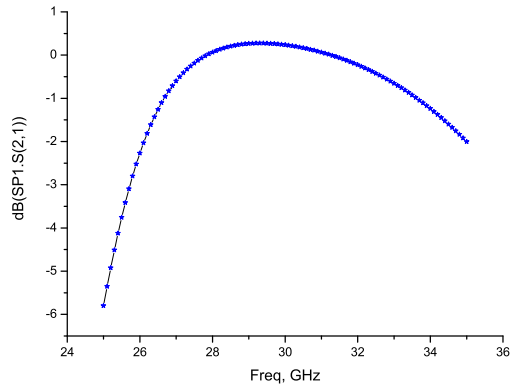
Figure 6.6: Predistortion circuit with the fixed bias circuit

With this configuration, the predistortion circuit can provide extra power gain of about 0.2 dB while improving the linearity. These results are shown in Figure 6.7 and comparisons are shown in Figure 6.8. For the circuit with matching networks biased at -0.62 V used in this case, its performance is shown in Figure 6.7. During the design, extra attention was paid to the stability issue to make sure that the predistortion circuit will not affect the stability of the PA in the main stage.

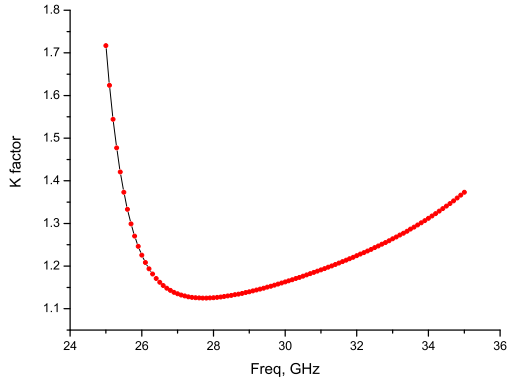


(a) Gain deviation characteristic

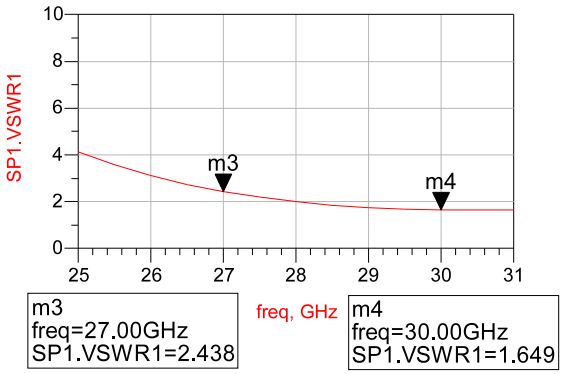
(b) Phase deviation characteristic



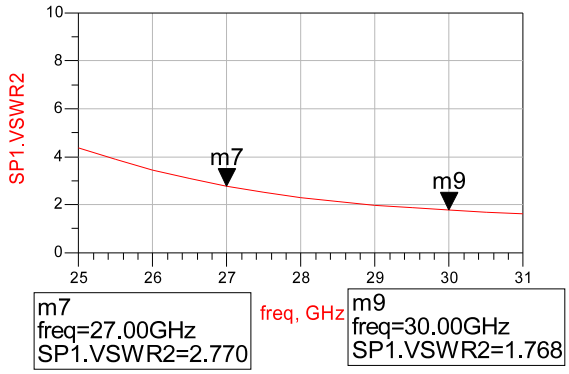
(c) Small signal gain characteristic



(d) Stability characteristic



(e) Input $VSWR$ characteristic

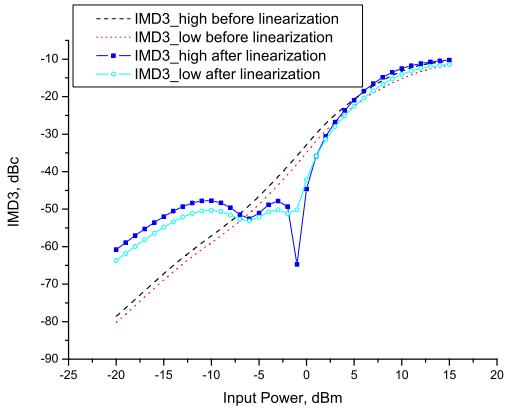


(f) Output $VSWR$ characteristic

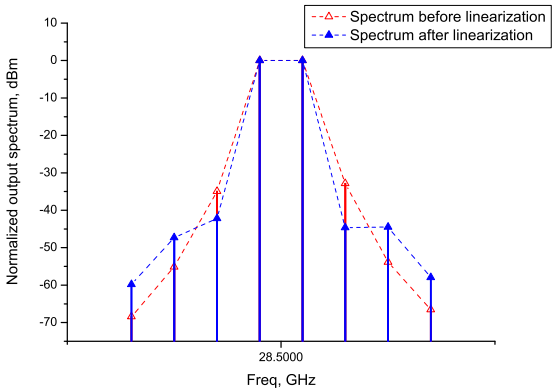
Figure 6.7: Characteristics of the predistortion circuit

6.4 Performance of PD plus PA

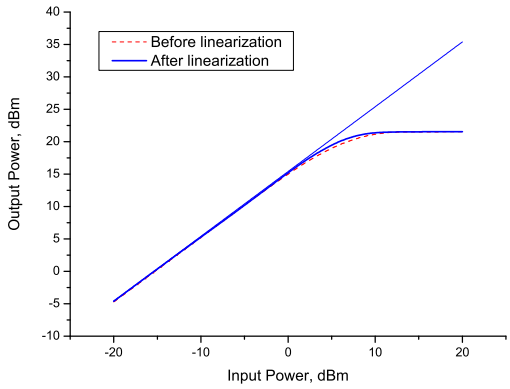
Detailed analysis was carried out and corresponding results and comparisons are shown in Figure 6.8. As the amplifier in the PD is biased at a fixed voltage, it can only linearize a certain power range. For this case, the linearized range is from -7.5 dBm to 6.5 dBm of the input power as shown in Figure 6.8 (a), which covers the power range that is most commonly used. IMD characteristics and spectrum were simulated at the fundamental frequency of 28.5GHz and frequency spacing of 50 KHz. After linearization, the $IMD3$ at input power of 0 dBm is improved by about 10 dB. Because the predistortion circuit is comprised of an amplifier, other metrics are also improved to some degree. For example, the power gain increases from 15.00 dB before linearization to 15.20 dB after linearization as shown in Figure 6.8 (d); PAE at Pin_{1dB} is improved from 17.73% to 23.91% and peak PAE increases from 35.01% to 36.86% as shown in Figure 6.8 (f). Detailed comparisons are shown in Table 6.2.



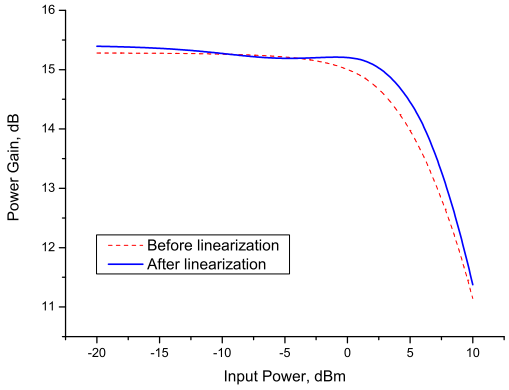
(a) $IMD3$ comparison



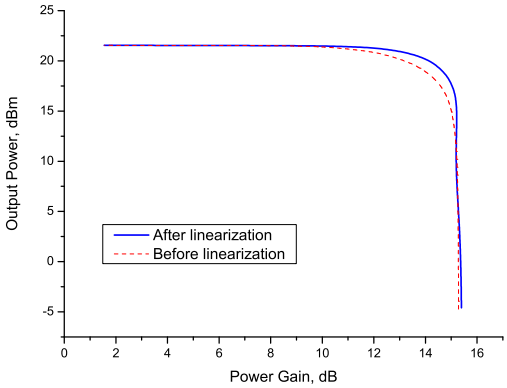
(b) Spectrum comparison



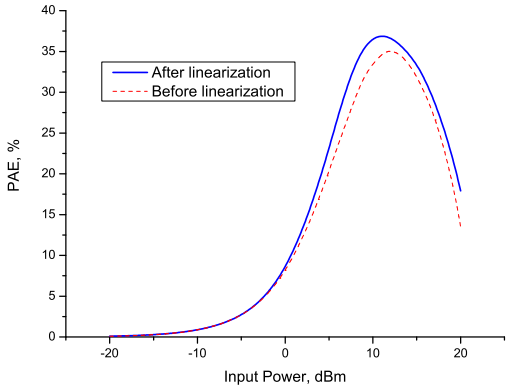
(c) Output power comparison



(d) Power gain comparison



(e) Output power and power gain comparison



(f) PAE comparison

Figure 6.8: Comparisons of the specifications before and after linearization

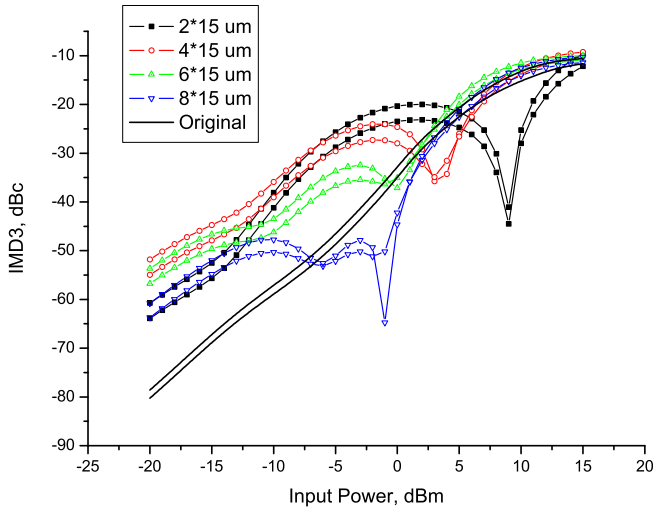
Table 6.2: Comparisons of the performances before and after linearization

Metrics	Before linearization	After linearization
$P_{in,1dB}$	4.1 dBm	5.2 dBm
$P_{out,1dB}$	18.37 dBm	19.59 dBm
Power Gain@P_{in}=0 dBm	15.00 dB	15.20 dB
PAE_{1dB}	17.73%	23.91%
PAE_{peak}	35.01%	36.86%
$IMD3$@P_{in}=0 dBm	$IMD3$_high: -32.82 dBc $IMD3$_low: -34.94 dBc	$IMD3$_high: -44.63 dBc $IMD3$_low: -42.20 dBc

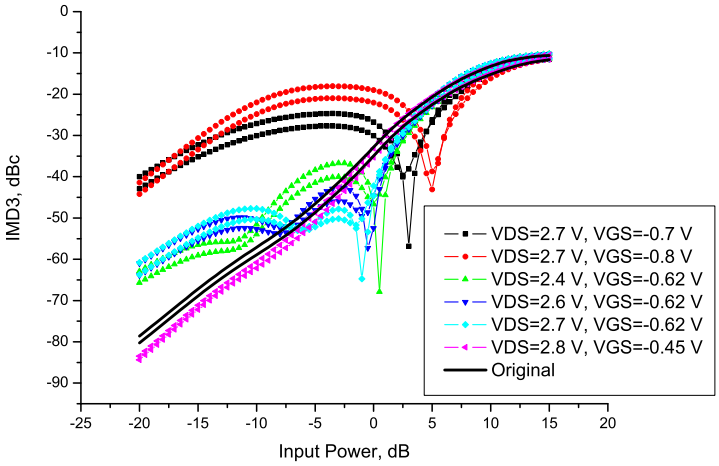
6.5 Consideration in the Practical Design

As the predistortion circuit is biased at a fixed voltage, thus the circuit can only linearize a certain range of input power. In practical applications, the required linearized power range may differ from the initial design and this problem can be solved by adjusting related parameters. By adjust the internal conditions such as the size of the transistors and the external conditions such as the supply and bias voltage, position of distortion reduction can be controlled and the gain and phase deviaton characteristics will change correspondingly, which can be used to adjust the linearized power range and linearity improvement.

As shown in Figure 6.9, by adjusting the size of the transistors, the supply and bias voltage, the predistortion circuit can linearize almost all the power range according to the requirement. In Figure 6.9 (a), the smaller the size of the transistor is, the higher linearized power level is. For the external bias conditions, the lower VDS and higher VGS, the higher linearized power level. These characteristics are shown in Figure 6.9 (b). Obviously the circuit has a practical application in the field of engineering.



(a) Linearity improvements at different transistor sizes



(b) Linearity improvements at the different bias voltages

Figure 6.9: Linearity improvements at different conditions

6.6 Summary

In this chapter, a predistortion circuit based on an amplifier with a fixed bias circuit was proposed. With this configuration, the predistortion circuit can not only improve the linearity, but also improve other metrics. Simulations show that a relatively large improvement, $IMD3$ improvement of 11.81 dB and 7.26 dB at upper and lower channels respectively was achieved and linearized power range can be adjusted according to the requirement. In the next chapter, another novel predistortion circuit realized by an

amplifier with a nonlinear signal dependant bias circuit will be proposed.

Chapter 7

PREDISTORTION CIRCUIT REALIZED BY AN AMPLIFIER WITH A NONLINEAR BIAS CIRCUIT

7.1 Introduction

Though the predistortion circuit proposed in Chapter 6 can improve the linearity significantly, the limitation of only linearizing a certain power range greatly restricts itself in the practical applications. Further to the predistortion circuit in Chapter 6, a novel predistortion circuit structure that can bring positive gain realized by an amplifier with a nonlinear signal dependant bias circuit is proposed in this chapter. This structure is based on a Class AB amplifier with a nonlinear signal dependant bias circuit. By adjusting the bias voltage with increasing input power, the amplifier shifts from Class AB operation to near Class A operation. Predistortion function can be realized and linearity is improved in this way. This approach can solve the problem of large insertion loss faced by the conventional predistortion circuit while improving other metrics considerably.

7.2 Design Principle of the Predistortion Circuit

The general principle of the novel design method is shown in Figure 7.1. The predistortion circuit in structure is primarily comprised of an amplifier with variable gain. If the gain of the amplifier increases with increasing input power, the predistortion circuit realized by the amplifier can exhibit gain expansion characteristic and realize the predistortion function. Such predistortion circuit can be realized by an amplifier with a nonlinear signal dependant bias circuit.

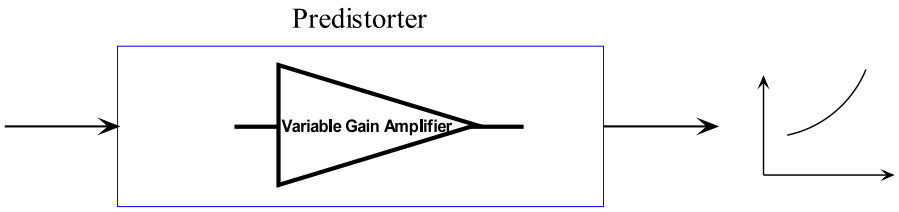


Figure 7.1: The general structure of the novel predistortion circuit

Figure 7.2 is the further illustration of the variable gain amplifier structure. The bias circuit of the amplifier employs a nonlinear bias resistor. The resistance is adaptable according to increasing input power, leading to an adjusted DC bias point. By adjusting the DC bias point, the circuit can change from class AB operation to near Class A operation, and exhibit the expected gain expansion characteristic.

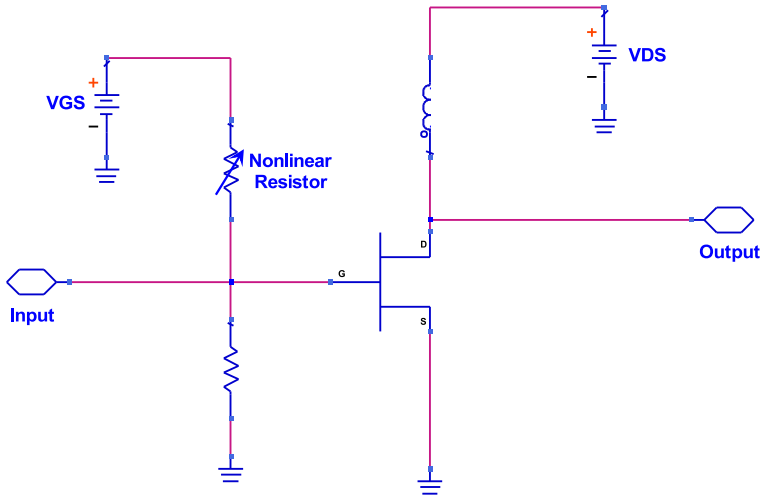
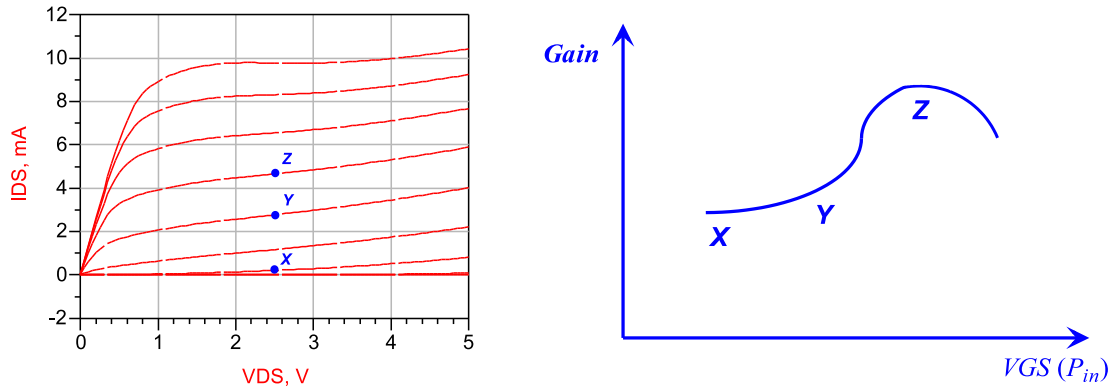


Figure 7.2: Further illustration of the predistortion design principle

Three DC bias points on the typical FET I-V curves are shown in Figure 7.3. Point X is located near the bottom of the I-V curves, corresponding to the operation in Class

AB. Point Z is located in the middle of the I-V curves, corresponding to Class A. The amplifier exhibits different gain levels at different DC bias points. For these three bias points, the FET exhibits maximum gain at point Z, next the point Y, then point X.

By adjusting the DC bias points carefully, the amplifier is biased from point X to point Z as the signal amplitude increases, corresponding to the transition from class AB to Class A. As the gain at the bias point Z is higher than that at bias point X, the circuit can exhibit the expected gain expansion characteristic. The gain trend at the different DC bias points is shown in Figure 7.3 (b).



(a) The bias points in the FET I-V curves (b) The gain trend at the three bias points

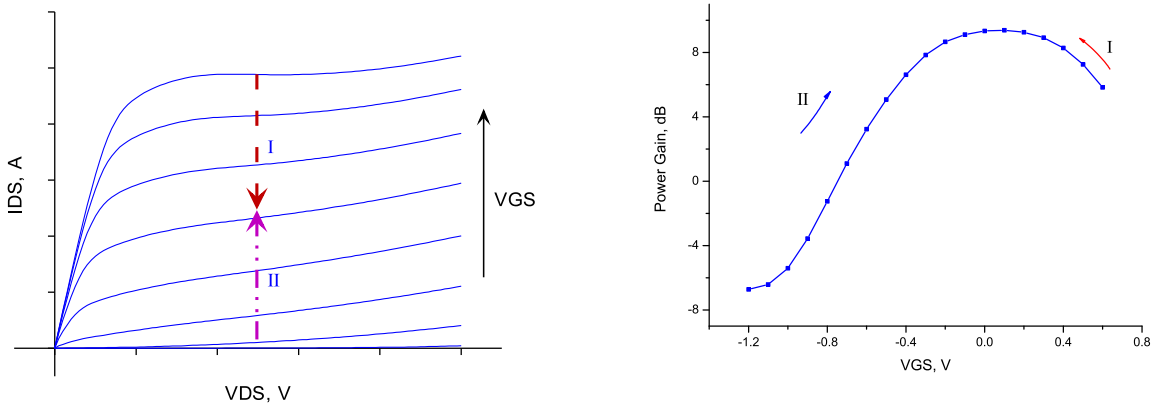
Figure 7.3: The bias points and corresponding gain trend

As the predistortion circuit is realized by an amplifier, the power gain can be positive. That is, this structure can effectively solve the problem of relatively high insertion loss, which is a severe problem faced by the conventional predistortion circuit. By adjusting the bias point, it is relatively easy to adjust the predistortion characteristic as required. Because of its positive gain, it can be placed between stages to realize a much stronger predistortion characteristic, or even replace an existing gain stage. In the next section, the detailed circuit realization of the nonlinear signal dependant bias circuit will be introduced and its principle of operation will be discussed.

7.3 Implementation of the Nonlinear Bias Circuit

In order to realize the gain expansion characteristic with an amplifier, two implementation approaches are available that can be applied in the circuit realization and they are shown in Figure 7.4. For the approach I, when the gate bias voltage VGS is positive,

the gain expansion can be realized by decreasing the VGS. For the approach II, when the gate bias voltage is negative, the gain can be increased by increasing the VGS. This trend can be verified by simulation with the practical circuit built on OMMIC pHEMT technology and the result is shown in Figure 7.4 (b). From Figure 7.4 (b), we can see that when VGS falls in the range of -1.2 V and 0 V, the higher VGS is, the higher the gain is. That is, the circuit exhibits gain expansion characteristic with increasing the bias voltage in this range. When VGS falls in the range of 0 V to 0.6 V, the smaller the VGS is, the higher the gain is. Gain expansion can be realized by decreasing the bias voltage. The changes in VGS can be realized by changing the effective bias resistance with increasing the input power.

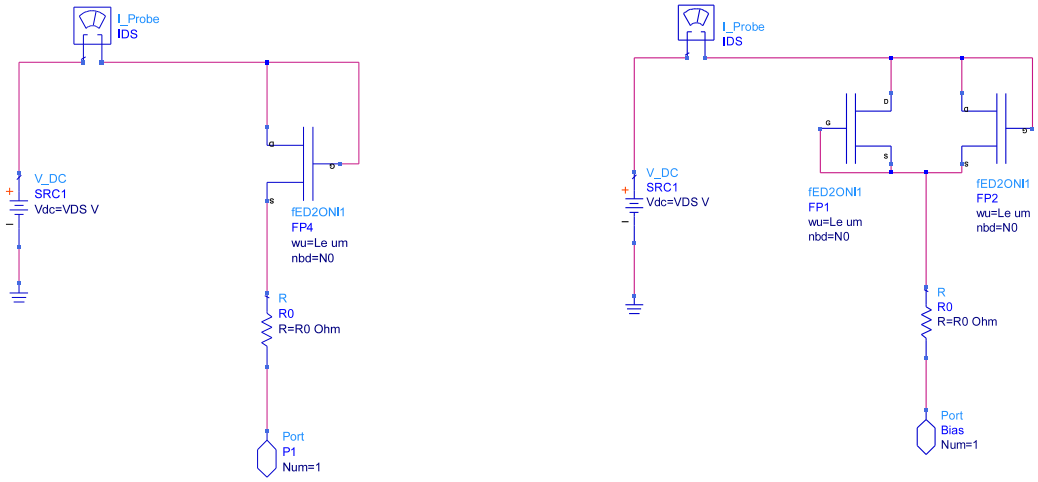


(a) Two approaches to realizing gain expansion (b) Gain verse gate bias voltage

Figure 7.4: Two approaches to realizing gain expansion

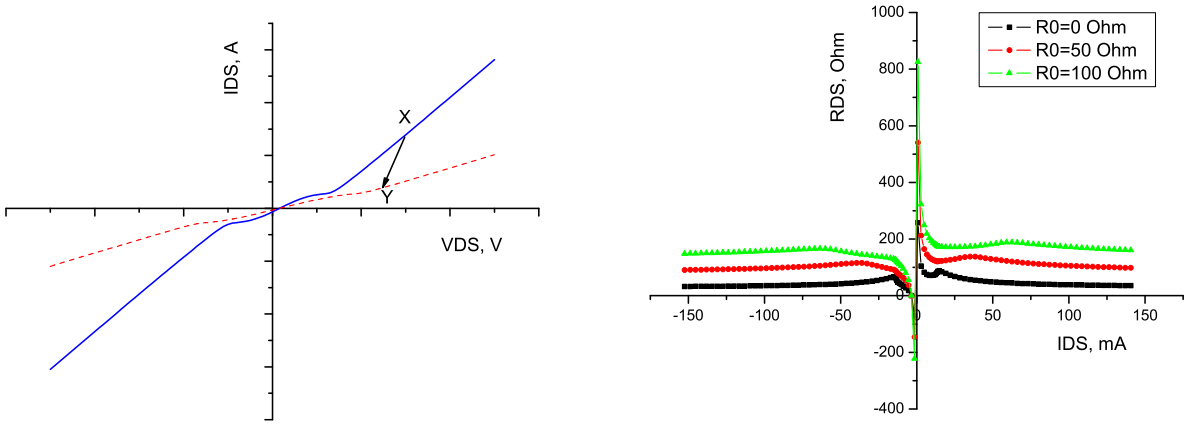
In order to demonstrate this new structure, a novel bias circuit shown in Figure 7.5 (b) is proposed to implement the predistortion characteristic and the circuit with single transistor in Figure 7.5 (a) is the basic structure from which it is derived. The novel bias circuit is comprised of two pHEMT transistors in parallel connection and a resistor R0 is connected in series with them. Its corresponding characteristics are shown in Figure 7.6. For the basic bias circuit with single transistor, it can only be connected to positive supply. With increasing input power, the current that flows through R0 will decrease. The bias point correspondingly moves from X to Y in the I-V curves in Figure 7.6 (a). The effective drain source resistance RDS increases and the gate bias voltage will decrease. Compared with the basic structure with single transistor, this bias circuit with two transistors in parallel connection can be connected to either positive supply or negative supply. When the supply voltage is positive, the right side of the transistor plays the key role. Similarly

the left side of the transistor plays the key role when the supply voltage is negative. For the negative case, with increasing input power, the current that flows through R0 will increase. The effective drain source resistance RDS increases and the gate bias voltage will increase. The resistor R0 here is employed to adjust the effective bias resistance and the bias current further. With this nonlinear signal dependant bias circuit, the gain of the amplifier can increase with increasing input power.



(a) Novel bias circuit with single transistor (b) Novel bias circuit with two transistors in parallel

Figure 7.5: Novel bias circuit

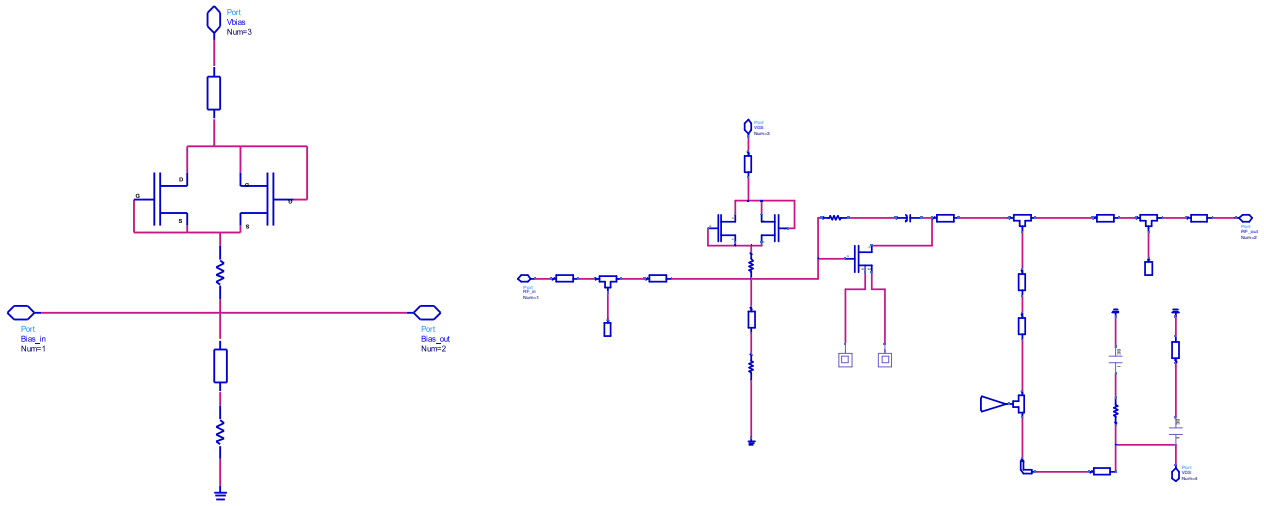


(a) Movement of bias points in the I-V curves (b) The effective drain-source resistance RDS

Figure 7.6: Operation analysis of the bias Circuit

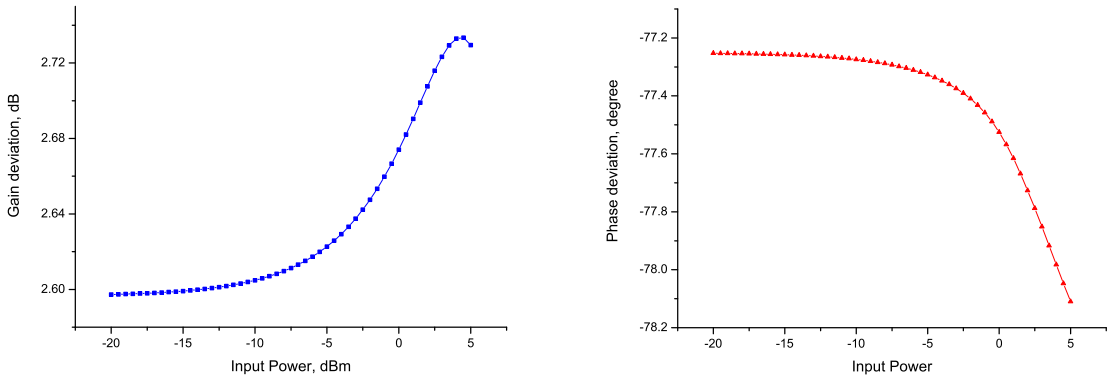
7.4 Designing of the PD from PA characteristics

Figure 7.7 (a) is the structure of the nonlinear bias circuit and the full predistortion circuit with matching networks is shown in Figure 7.7 (b). For this case, as the bias voltage is chosen to be positive, the gate bias voltage decreases with increasing input power. Just like the design in Chapter 6, in order to match the response of the amplifier and improve the linearity, circuit parameters were optimized and bias voltage was selected carefully. In this case, the size of the transistor in the predistortion stage is $6 \times 30\mu m$ and the bias voltage is 1 V. Figure 7.8 shows the gain expansion characteristic and phase compression characteristic respectively.



(a) Full structure of the bias circuit (b) The predistortion circuit with novel structure

Figure 7.7: Novel predistortion circuit with full structure



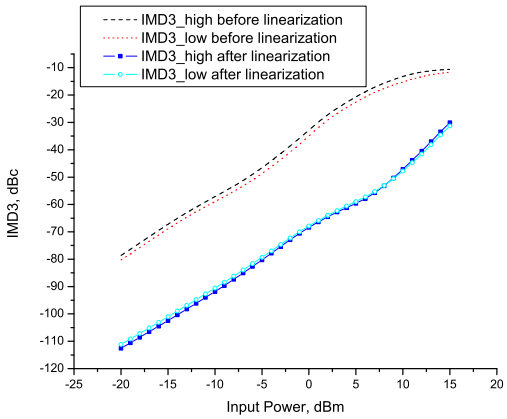
(a) Gain deviation characteristic (b) Phase deviation characteristic

Figure 7.8: Characteristics of the predistortion circuit

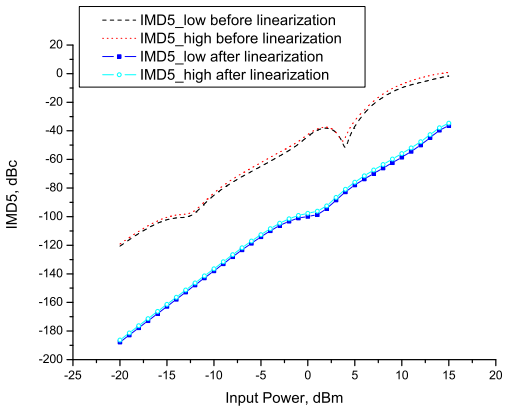
7.5 Performance of PD plus PA

As the predistortion circuit has matching networks at both ports, it is very convenient to connect to the PA, measure the performance and compare with the PA without the predistortion circuit. In order to demonstrate the performance improvement, the millimeter-wave power amplifier for LMDS applications designed in Chapter 4 is employed as the test bench for linearization and comparison.

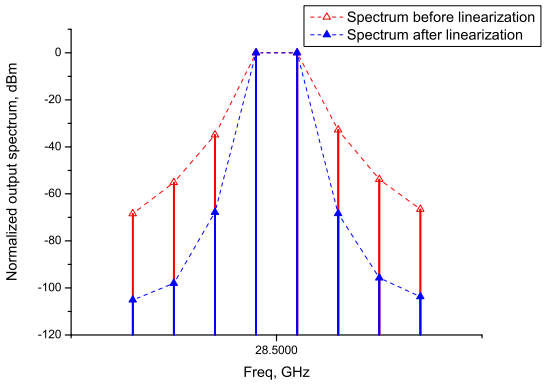
Several important metrics are shown and compared with those before linearization in Figure 7.9. The metrics related to linearity including $IMD3$, $IMD5$ and spectrum comparisons are shown in Figure 7.9 (a), (b) and (c) respectively. The output power and power gain are shown in Figure 7.9 (d) and (e) and PAE is shown in Figure 7.9 (f). IMD characteristics and spectrum were simulated at the fundamental frequency of 28.5GHz and frequency spacing of 50 KHz. $IMD3$ after linearization reaches up to -68.37 dBc and -67.88 dBc at upper channel and lower channel respectively. From the comparisons, we can see that the linearity has improved significantly while other specifications such as power gain and PAE are also improved as shown in Figure 7.9 (c) and Figure 7.9 (d) respectively.



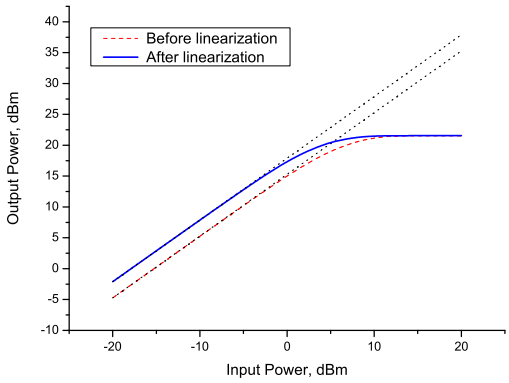
(a) $IMD3$ comparison



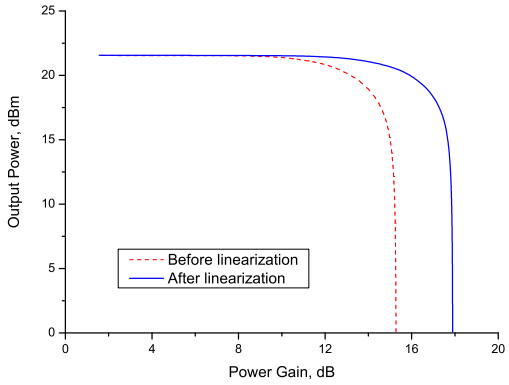
(b) $IMD5$ comparison



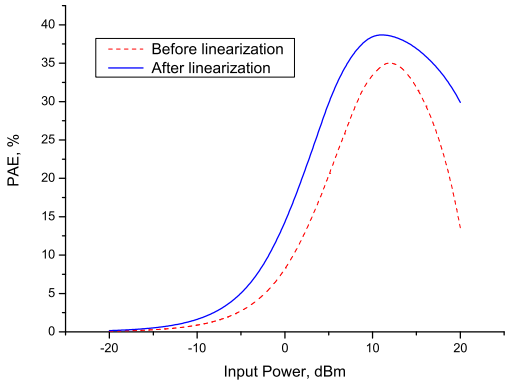
(c) Spectrum comparison



(d) Output power comparison



(e) Output power vs. power gain



(f) PAE comparison

Figure 7.9: Main Metrics Comparisons with the PA without linearization

The results before and after linearization are listed in the Table 7.1. From the comparison, we can see that after linearization, almost all the specifications are improved, including linearity, power gain, and PAE.

Table 7.1: Comparisons of main metrics before and after linearization

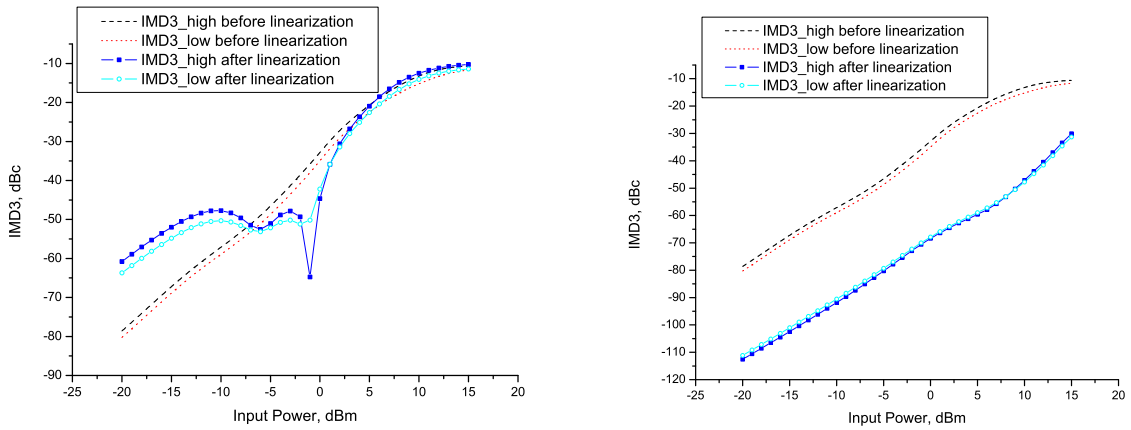
Specifications	Before linearization	After linearization
$P_{out,1dB}$	18.37 dBm	18.59 dBm
Power Gain@P_{in}=0 dBm	15.00 dB	17.32 dB
PAE_{1dB}	17.73%	19.20%
PAE_{peak}	35.01%	38.68%
$IMD3$@P_{in}=0 dBm	$IMD3$_high: -32.82 dBc $IMD3$_low: -34.94 dBc	$IMD3$_high: -68.37 dBc $IMD3$_low: -67.88 dBc
$IMD5$@P_{in}=0 dBm	$IMD5$_high: -42.52 dBc $IMD5$_low: -43.84 dBc	IMD5_high: -97.61 dBc $IMD5$_low: -99.85 dBc

7.6 Comparison with the Predistorter with a Fixed Bias Circuit

$IMD3$ comparisons for the predistorter with a fixed bias circuit (FBP) and the predistorter with a nonlinear signal dependant bias circuit (NBP) are shown in Figure 7.10. Compared with the linearity improvement brought by the FBP circuit in Chapter 6, the linearity improvement brought by the NBP circuit, is much higher and linearized power range is also much wider. On the other hand, the FBP circuit has a steep $IMD3$ curve while the NBP circuit has a relatively smooth $IMD3$ curve.

For the predistortion circuit with a fixed bias circuit, FBP, its bias voltage is fixed at a certain voltage, so it can only linearize a certain power range though the linearized power range can be adjusted externally according to the requirement. For the predistortion circuit with a nonlinear signal dependant bias circuit, NBP, as its bias voltage is adjusted automatically according to increasing input power, it can linearize a relatively wider power range.

The much larger linearity improvement by the predistortion circuit with a nonlinear signal dependant bias circuit, compared with the predistortion circuit with a fixed bias circuit can be explained through the effect of phase on $IMD3$ and the steep $IMD3$ curve of the FBP circuit can be explained through the impact of $IMD5$ factor. A brief discussion



(a) $IMD3$ illustration of the FBP circuit (b) $IMD3$ illustration of the NBP circuit

Figure 7.10: Linearity Comparison of two predistortion circuits

will be carried out in Section 7.6.1 and the analysis also applies to the predistortion circuit built on the passive RC network proposed in Chapter 8.

7.6.1 Theoretical Analysis for the Comparison

The IMD analysis in this section is primarily concerned with the conventional cascaded predistortion structure, in which predistortion circuit is placed in front of the nonlinear power amplifier as shown in Figure 7.11.

For the cascaded PD and PA modules in this case, the final $IMD3$ is comprised of two components, one from the power amplifier, PA, with voltage gain of G_1 and another from the predistortion circuit, PD, with voltage gain of G_2 as shown in Figure 7.11. For the PD module, the outputs in the main channels are S_1, S_2 with the amplitude of V_1 and V_2 for the frequency of f_1 and f_2 respectively. The third order components of the output signal are M_{30} and M_{31} for the upper channel and lower channel respectively and the amplitude of M_{30} is K_{30}.

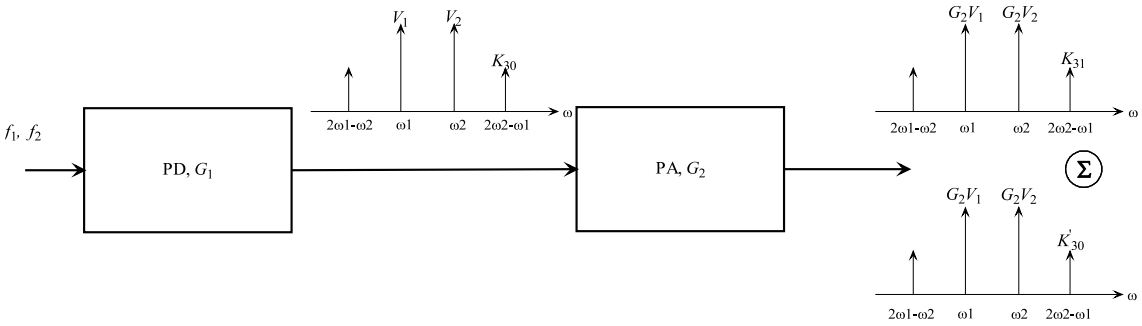


Figure 7.11: The predistortion system in IMD analysis

Assuming that the phase of the signals before entering the PD component is 0°, then we define $S_1 = V_1 \times \cos(\omega_1 t)$, $S_2 = V_2 \times \cos(\omega_2 t)$ as the signals in the upper and lower channels respectively.

The output of a nonlinear system can be expressed as

$$\begin{aligned} f(S_1 + S_2) = C_0 + C_1 \times (S_1 + S_2) + C_2 \times (S_1 + S_2)^2 + C_3 \times (S_1 + S_2)^3 \\ + C_4 \times (S_1 + S_2)^4 + C_5 \times (S_1 + S_2)^5 ..., \end{aligned} \tag{7.1}$$

in which the coefficient $C_0 \sim C_5$ are decided by the inherent characteristics of the system.

Most of works on linearity related to $IMD3$ are concerned with the term, $C_3 \times (S_1 + S_2)^3$ in Equation (7.1). In this analysis, we will take $C_5 \times (S_1 + S_2)^5$ in Equation (7.1) into consideration besides the conventional $IMD3$ factor during the linearity improvement estimate. The rest of analysis is based on these two terms. Even-degree RF domain terms have been discarded due to the assumed band-limited nature of system and cannot therefore cause in-band distortion [19].

For the PD component in the system, the fourth term in Equation (7.1) can be expressed as

$$(S_1 + S_2)^3 = S_1^3 + 3 \times S_1^2 \times S_2 + 3 \times S_1 \times S_2^2 + S_2^3, \tag{7.2}$$

where $3 \times S_1^2 \times S_2$ corresponds to M_{31}, $3 \times S_1 \times S_2^2$ corresponds to M_{30}.

$$\begin{aligned} \text{As} \quad S_1^2 \times S_2 &= V_1^2 \times V_2 \times \cos^2(\omega_1 t) \times \cos(\omega_2 t) \\ &= \frac{1}{2} \times V_1^2 \times V_2 \times \cos(\omega_2 t) + \frac{1}{4} \times V_1^2 \times V_2 \times \cos(2\omega_1 t + \omega_2 t) \\ &\quad - \frac{1}{4} \times V_1^2 \times V_2 \times \sin(2\omega_1 t - \omega_2 t), \end{aligned} \tag{7.3}$$

the third order intermodulation product in the output of PD module can be expressed as

$$M_{31} = -\frac{3}{4} \times V_1^2 \times V_2 \times C_3 \times \sin(2\omega_1 t - \omega_2 t). \tag{7.4}$$

Similarly the third order intermodulation product in the other channel can be expressed as

$$M_{30} = -\frac{3}{4} \times V_1 \times V_2^2 \times C_3 \times \sin(2\omega_2 t - \omega_1 t). \tag{7.5}$$

For convenience, the following analysis is based on a single channel signal. If we define $\theta_3 = 2\omega_2 t - \omega_1 t$, $K_{30} = -\frac{3}{4} \times V_1 \times V_2^2 \times C_3$ then

$$IMD3_{PD} = K_{30} \times \sin(\theta_3), \tag{7.6}$$

where $IMD3_{PD}$ is the $IMD3$ from the PD component without considering the phase deviation.

When the output signal of the PD component passes through the nonlinear PA, the output $IMD3$ is mainly comprised of two components. One is the third order intermodulation product generated by the nonlinear PA and the other is the third order intermodulation product from the PD component, which will be amplified by the PA.

Similarly to the analysis above, the third order intermodulation product generated by the nonlinear PA can be expressed as

$$\begin{aligned} IMD3_{PA} &= -\frac{3}{4} \times (G_2 \times V_1) \times (G_2 \times V_2)^2 \times C_3^{'} \times \sin(2\omega_2 t - \omega_1 t) \\ &= K_{31} \times \sin(\theta_3), \end{aligned} \tag{7.7}$$

where $IMD3_{PA}$ is the $IMD3$ from the PA, $K_{31} = -\frac{3}{4} \times G_2^3 \times V_1 \times V_2^2 \times C_3^{'}$.

The third order intermodulation product from the PD module when passing through the PA, will be amplified by the amplifier. Meanwhile a phase deviation φ defined in Figure 7.12 will be introduced during this process.

Thus

$$IMD3_{PD}^{'} = K_{30}^{'} \times \sin(\theta_3^{'}), \tag{7.8}$$

where $IMD3_{PD}^{'}$ is the $IMD3$ from the PD component considering the phase deviation, $K_{30}^{'} = G_2^3 \times K_{30}, \theta_3^{'} = \theta_3 + \varphi$.

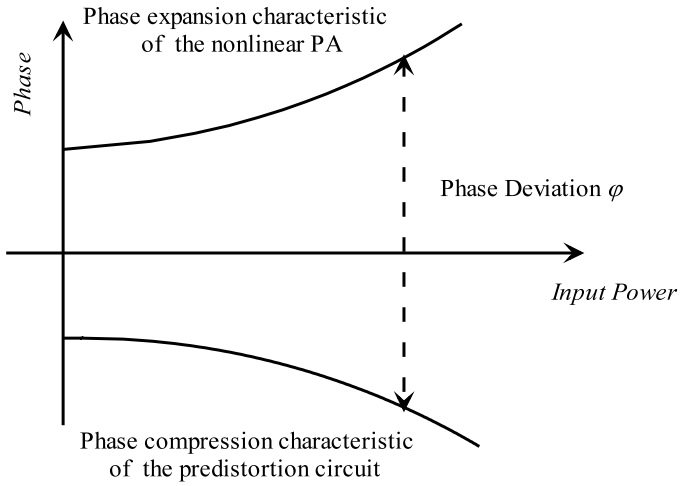


Figure 7.12: Phase deviation definition

On the other hand, the $IMD3$ intermodulation product also is related to $(S_1+S_2)^5$ in Equation (7.1), which can be expressed as

$$(S_1+S_2)^5 = S_1^5 + 5\times S_1^4\times S_2 + 10\times S_1^3\times S_2^2 + 10\times S_1^2\times S_2^3 + 5\times S_1\times S_2^4 + S_2^5. \tag{7.9}$$

$$\text{As}\quad S_1^3\times S_2^2 = V_1^3\times V_2^2\times\cos^3(\omega_1 t)\times\cos^2(\omega_2 t)$$
$$= \frac{V_1^3\times V_2^2}{4}\left[\begin{array}{l}\cos(\omega_1 t)+\frac{1}{2}\cos(2\omega_2 t+\omega_1 t)-\frac{1}{4}\sin(2\omega_2 t-\omega_1 t)+\frac{1}{2}\cos(3\omega_1 t)+\\ \frac{1}{2}\sin(\omega_1 t)+\frac{1}{4}\cos(2\omega_2 t+3\omega_1 t)-\frac{1}{4}\sin(3\omega_1 t-2\omega_2 t)+\frac{1}{2}\sin(2\omega_2 t+\omega_1 t)\end{array}\right], \tag{7.10}$$

so the $IMD5$ derivative from Equation (7.10) can be expressed as

$$IMD5 = -C_5\times 10\times\frac{V_1^3\times V_2^2}{16}\times\sin(3\omega_1 t-2\omega_2 t) = -C_5\times\frac{5}{8}\times V_1^3\times V_2^2\times\sin(3\omega_1 t-2\omega_2 t)$$
$$= K_{50}\times\sin(\theta_5), \tag{7.11}$$

where $K_{50} = -C_5\times\frac{5}{8}\times V_1^3\times V_2^2$, $\theta_5 = 3\omega_1 t - 2\omega_2 t$.

For this case, $IMD5$ is also comprised of two components. One is from the PD component and the other is from the PA component. Similarly to $IMD3$ analysis above, the $IMD5$ from the PD will be amplified by the PA and a phase deviation φ will be

introduced. Thus

$$IMD5_{total} = K_{50}^{'} \times \sin(\theta_5^{'}) + K_{50} \times \sin(\theta_5), \tag{7.12}$$

where $K_{50}^{'} = G_2^5 \times K_{50}, \theta_5^{'} = \theta_5 + \varphi$.

Thus the third derivative component related to Equation (7.10) can be expressed as

$$\begin{aligned} IMD3 &= -C_5 \times 10 \times \frac{V_1^3 \times V_2^2}{16} \times \sin(2\omega_2 t - \omega_1 t) = -C_5 \times \frac{5}{8} \times V_1^3 \times V_2^2 \times \sin(2\omega_2 t - \omega_1 t) \\ &= K_{50} \times \sin(\theta_3). \end{aligned} \tag{7.13}$$

As the $IMD3$ will be amplified by the PA and a phase deviation φ be introduced, so $IMD3$ will be modified to

$$IMD3^{'} = G_2^5 \times K_{50} \times \sin(\theta_3 + \varphi) = K_{50}^{'} \times \sin(\theta_3^{'}). \tag{7.14}$$

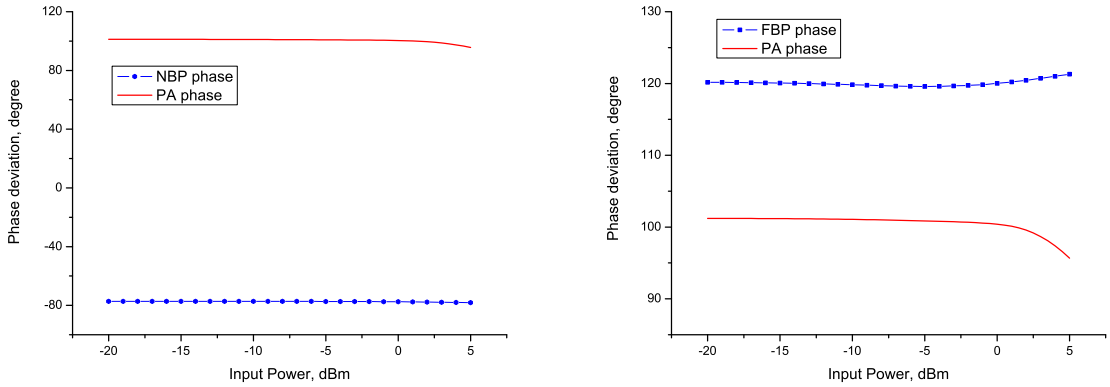
Thus the total $IMD3$ can be expressed as

$$\begin{aligned} IMD3_{total} &= IMD3_{PD}^{'} + IMD3_{PA} + IMD3^{'} \\ &= K_{30}^{'} \times \sin(\theta_3^{'}) + K_{31} \times \sin(\theta_3) + K_{50}^{'} \times \sin(\theta_3^{'}), \end{aligned} \tag{7.15}$$

where θ_3 and $\theta_3^{'}$ are the phase characteristics of PD and PA components respectively.

The fact that the relatively larger $IMD3$ improvement brought by the predistortion circuit with a nonlinear signal dependant bias circuit, NBP, compared with the PD with a fixed bias circuit, FBP, can be explained through the $IMD3_{total}$ expression in Equation (7.15). The relatively larger $IMD3$ improvement brought by the NBP circuit mainly comes from the opposite polarity of phase deviation characteristic of PA and PD as shown in Figure 7.13. As for the NBP predistortion circuit, its phase component can compensate PA's phase component more closely than the FBP circuit, the final $IMD3$ in Equation (7.15) is greatly reduced as result and linearity is improved considerably in this way.

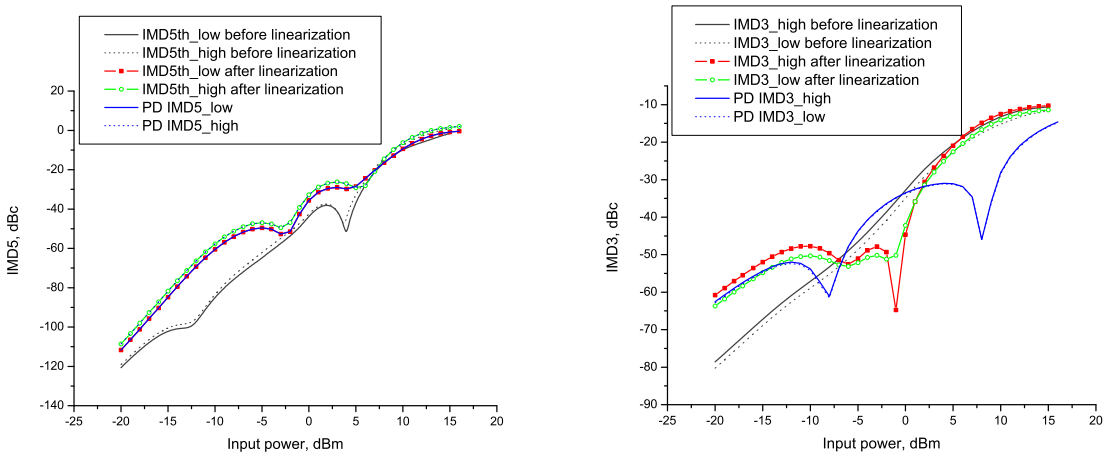
As the third term in Equation (7.15) comes from Equation (7.14) and it has the same amplitude of the first term of $IMD5$ expression in Equation (7.12), thus $IMD3_{total}$



(a) Phase characteristic of the NBP circuit (b) Phase characteristic of the FBP circuit

Figure 7.13: Phase Comparison of two predistortion circuits

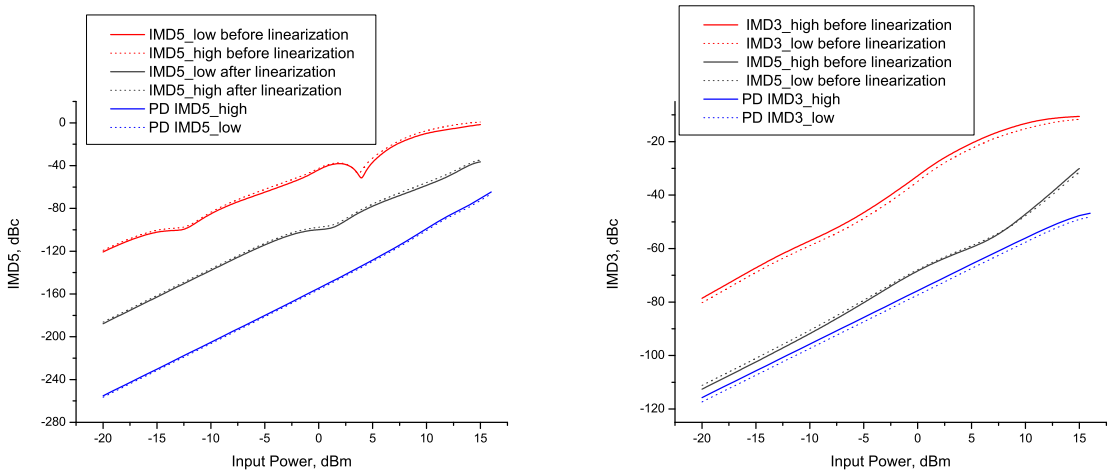
is also affected by $IMD5$ in the case when the magnitude of $IMD5$ is relatively large. When $IMD5$ from the PD is relatively large, such as the case in the FBP circuit, the third term in Equation (7.15) is relatively large, it will affect $IMD3_{total}$ correspondingly. That is why the FBP circuit has a very steep in $IMD3$ curve after linearization, which is similar to $IMD5$ curve from the PD component as shown in Figure 7.14.



(a) $IMD5$ relationship for the FBP circuit (b) $IMD3$ relationship for the FBP circuit

Figure 7.14: IMD relationship for the FBP circuit

For the NBP circuit in Figure 7.15, as the $IMD5$ from the PD is much lower, thus its impact on the $IMD3$ is correspondingly much less and that is why this circuit has a relatively smooth $IMD3$ curve.



(a) $IMD5$ relationship for the NBP circuit (b) $IMD3$ relationship for the NBP circuit

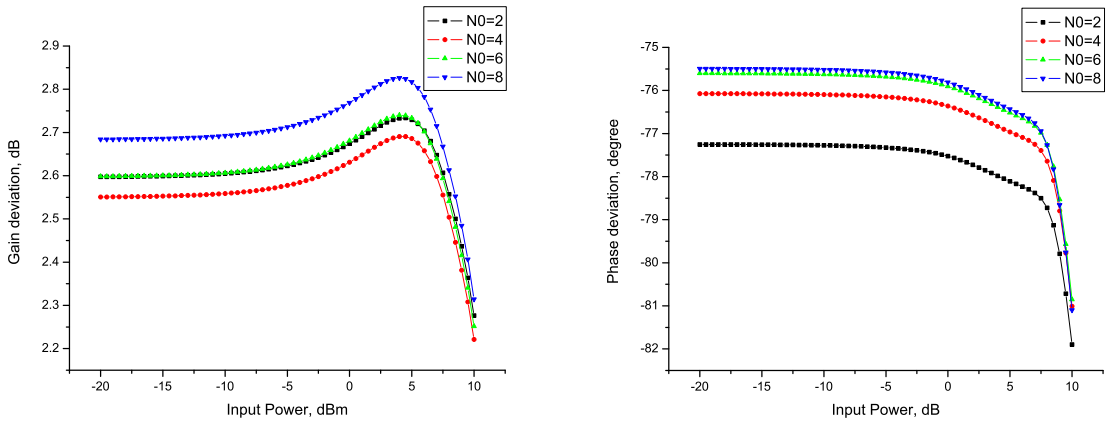
Figure 7.15: IMD relationship for the NBP circuit

7.7 Consideration in the Practical Design

Aberrant operation in a practical design must be taken into consideration and robustness analysis was carried out by considering the influence from internal factors and external factors that might exist in practical operation.

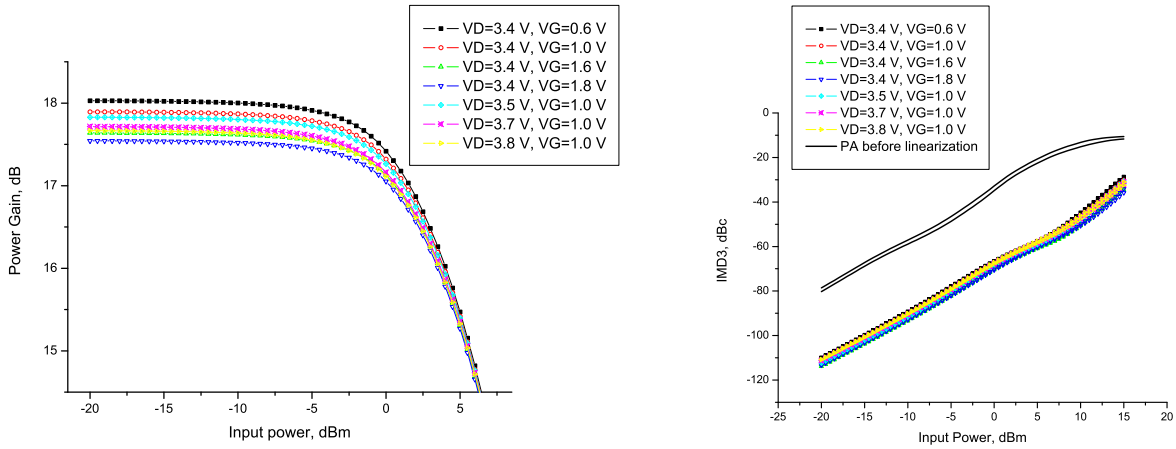
Firstly, internal factors that may affect the performance such as the impact of the size of transistor in the PD were evaluated by sweeping the numbers of the FET fingers. From the simulation results in Figure 7.16 it is found that the power gain variation is less than 0.2 dB with different sizes of transistor over the range from 2 to 8 FET fingers. Obviously the predistortion circuit is affected slightly by the size of transistor.

The influence from external factors include the supply and bias conditions were also taken into consideration. Simulation was carried out by adjusting the different bias conditions and the results in Figure 7.17 show that the power gain varies within a small range with different bias conditions and the predistortion circuit can still linearize the power amplifier at a relatively wide power range.



(a) Gain characteristic of NBP circuit (b) Phase characteristic of NBP circuit

Figure 7.16: Gain and Phase characteristic at different transistor sizes



(a) Power gain at different bias points (b) $IMD3$ at different bias points

Figure 7.17: Characteristics at different bias conditions

From the evaluation on the affection from the internal and external factors above, the predistortion circuit realized by an amplifier with a nonlinear signal dependant bias circuit has a good robustness against aberrant operation and have a broad prospect for applications.

7.8 Summary

In this chapter, a novel predistortion circuit realized by an amplifier with a nonlinear signal dependant bias circuit was proposed. With this method, large insertion loss problem normally faced by the conventional predistortion circuit can be solved and all

other specifications can be improved as well. Compared with the FBP predistortion circuit proposed in Chapter 6, this circuit can bring much higher performance improvement in terms of linearity, power gain and PAE besides a good robustness. In the next chapter, a novel predistortion circuit deign methodology derived from frequency to signal amplitude transformation will be proposed.

Chapter 8

DERIVATION OF POWER AMPLIFIER PREDISTORTION CIRCUITS BY FREQUENCY TO SIGNAL AMPLITUDE TRANSFORMATION

8.1 Introduction

In this chapter, an original approach for predistortion circuit design for millimeter-wave power amplifier linearization based on the passive RC network is proposed. The methodology employs FET devices as the nonlinear resistor to realize the required predistortion function, which is used to linearize millimeter-wave power amplifier. This methodology can effectively improve the linearity while affecting other metrics only slightly. Based on this theory, three transfer functions are proposed and related predistortion circuits are designed, compared and discussed. The millimeter-wave power amplifier designed in Chapter 4 will be used as the target for evaluation. Part of the work has been published at European Conference on Circuit Theory and Design 2007 [26].

8.2 Principle of Passive RC Network Design Methodology

The methodology is derived from the transfer characteristics of passive RC network. A network with some configuration such as the case in Figure 8.1 may have the characteristics of amplitude and phase with respect to frequency as shown in Figure 8.2.

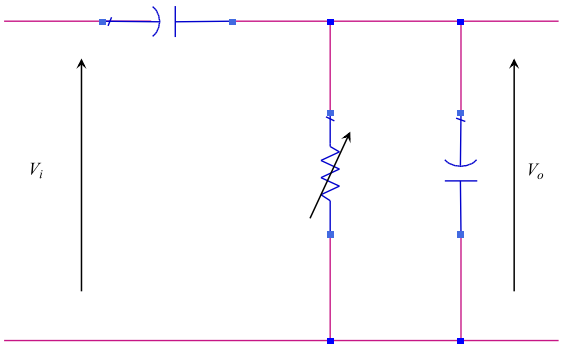
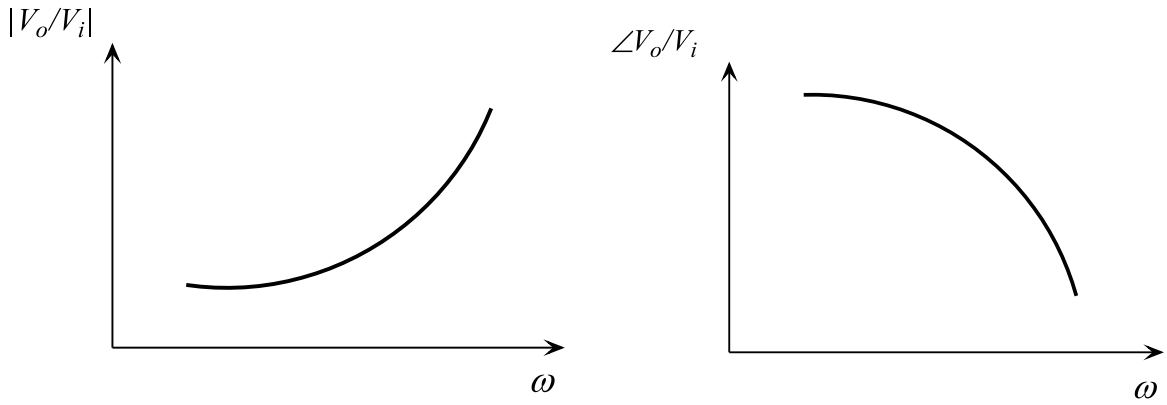


Figure 8.1: Diagram of passive RC network



(a) Magnitude response of H, $H = V_o/V_i$ (b) Phase response of H, $H = V_o/V_i$

Figure 8.2: The expected transfer characteristics

The idea is to convert this characteristic from the change in gain and phase with respect to frequencies to the change in gain and phase with respect to the input signal amplitude. In order to reach the goal, a nonlinear element needs to be introduced. Under such conditions, the value of the nonlinear element can be regarded as signal amplitude dependant. Part of this process involves introducing an impedance scaling factor s or $1/s$, such that the original RC circuit can be converted to an equivalent circuit with a nonlinear element and the required gain and phase characteristics. Then the nonlinear element will be replaced be a semiconductor device such as FET device with a suitable I-V characteristic, so that the original circuit can be converted to a predistortion circuit.

We now consider this approach in detail.

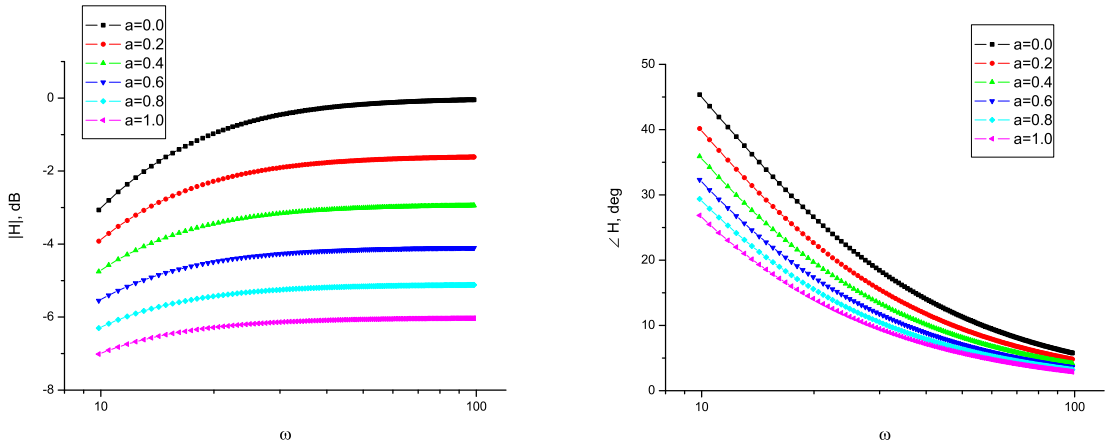
8.3 Transfer Functions

Equation (8.1) is Transfer Function 1 and is the basis for the first predistortion circuit based on the passive RC network approach.

$$H(j\omega) = \frac{j\omega}{j\omega(a+1)+b}\,, \tag{8.1}$$

where $\omega = 2\pi f$ and a and b are real quantities.

The magnitude and phase of $H(j\omega)$ in Equation (8.1) are shown in Figure 8.3 for a between 0 and 1 when b is equal to 10 and Figure 8.4 for b between 1 an 10 when a is equal to 0 respectively. In the curves, the magnitude of $H(j\omega)$ increases with increasing the frequency while phase of $H(j\omega)$ decreases with increasing the frequency. These characteristics may be employed in the predistortion circuit design.



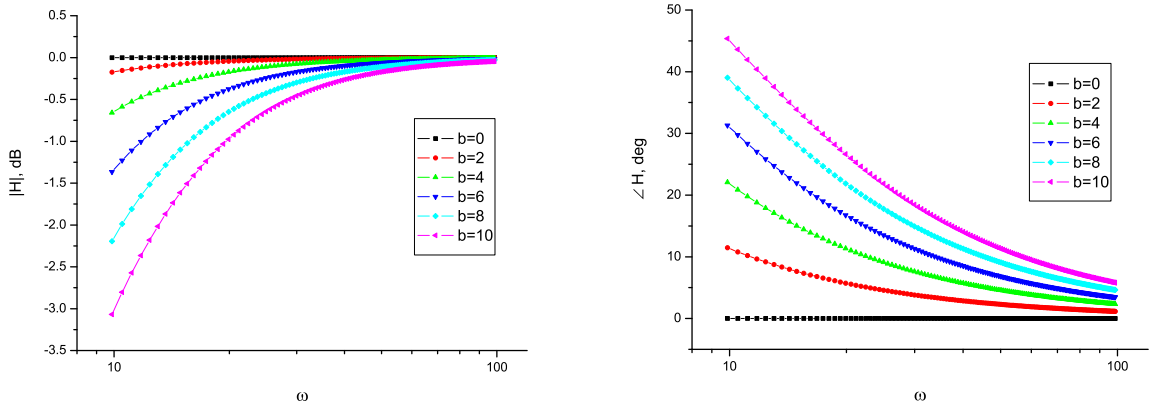
(a) Magnitude response of H (b) Phase response of H

Figure 8.3: Variation of H with a as parameter

Transfer function 2 is another transfer function for predistortion circuit design based on the passive RC network and is given in Equation (8.2).

$$H(j\omega) = \frac{1+j\omega}{1+a+j\omega}, \tag{8.2}$$

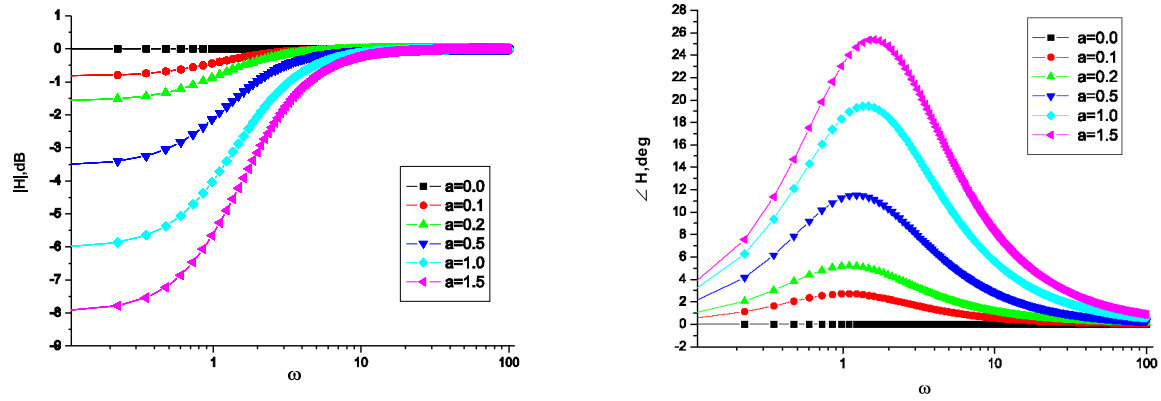
where $\omega = 2\pi f$ and a is a real quantity.



(a) Magnitude response of H (b) Phase response of H

Figure 8.4: Variation of H with b as parameter

Similarly Transfer Function 2 has the magnitude and phase of $H(j\omega)$ that may be employed in the predistortion circuit design as shown in Figure 8.5 for values of a between 0 and 1.5. In the curves, the magnitude of $H(j\omega)$ increases with increasing the frequency while phase of $H(j\omega)$ increases first and decreases after a certain frequency.



(a) Magnitude response of H (b) Phase response of H

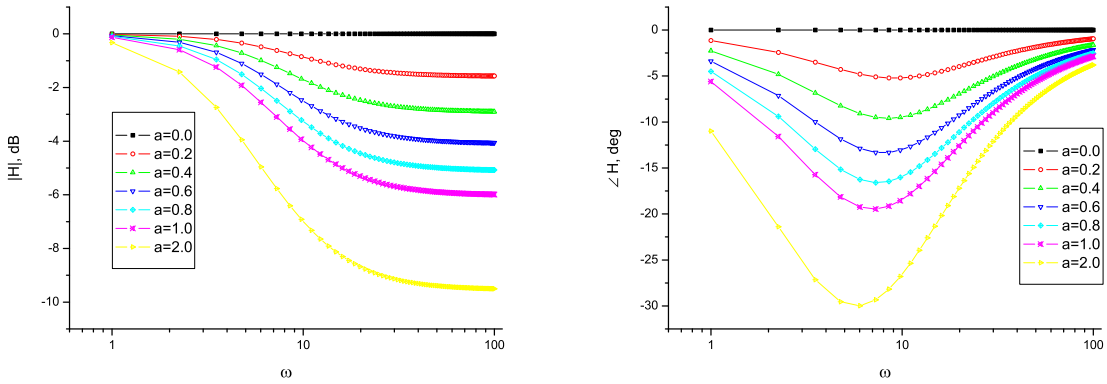
Figure 8.5: Variation of H with a as parameter

Equation (8.3) is Transfer Function 3 proposed for predistortion circuit design based on passive RC network.

$$H(j\omega) = \frac{j\omega + b}{j\omega(a+1) + b}, \tag{8.3}$$

where $\omega = 2\pi f$ and a and b are real quantities.

The magnitude and phase of $H(j\omega)$ in Equation (8.3) are shown in Figure 8.6 for a between 0 and 2 when $b = 10$, in which horizontal axis is frequency and vertical axis is magnitude and phase respectively. Different from Transfer Function 1 and Transfer Function 2, the magnitude of $H(j\omega)$ in Transfer Function 3 decreases with increasing the frequency while phase of $H(j\omega)$ decreases first and increases after a certain frequency. The characteristics of Transfer Function 3 can be employed in predistortion circuit design with a proper approach as we will show.



(a) Magnitude response of H (b) Phase response of H

Figure 8.6: Variation of H with a as parameter

8.3.1 Comparison between Transfer Functions

The comparison between the transfer functions is shown in Table 8.1, in which related data are listed.

Table 8.1: Transfer Function Comparisons

Transfer Function	Variable	Scaling factor	Transfer curves	Preferred frequency range
Equation (8.1)	a and b	$1/s$	Figure 8.3 and 8.4	Upper end
Equation (8.2)	a	$1/s$	Figure 8.5	Upper end
Equation (8.3)	a and b	s	Figure 8.6	Lower end

For the transfer characteristics of Transfer Function 1 shown in Figure 8.3 and Figure 8.4, the magnitude of H increases while the phase of H decreases with increasing the frequency. While for the transfer characteristics of Transfer Function 2 shown in

Figure 8.5, the magnitude of H increases with increasing the frequency while the phase of H increases first and decreases after a certain frequency. For transfer characteristics of these two transfer functions, if the horizontal axis was the input signal amplitude rather than frequency and the frequency was constant, then the gain and phase characteristics shown would be ideal for a predistorter as there is gain expansion and phase compression, and the effects are substantial. The value of the parameters such as a and b can be chosen according to the optimum amount of gain and phase compensation required.

Transfer Function 3 differs from Transfer Function 1 and Transfer Function 2 in the magnitude characteristic. Unlike the curves in Figure 8.3 and Figure 8.5, in Figure 8.6 the magnitude of H decreases while the phase of H decreases first and increases after a certain frequency. For the transfer characteristics of Transfer Function 1 and Transfer Function 2, it was envisioned that the horizontal axis would be transformed to input signal amplitude. However, if the horizontal axis could be regarded as the inverse of input signal amplitude rather than the input signal amplitude, then the characteristics shown would be suitable for a predistortion circuit as gain expansion and phase compression can be acquired in this way. The value of factor a and factor b can be chosen according to the optimum amount of gain and phase compensation required.

For the transfer characteristics of Transfer Function 1, at lower frequency range, the amplitude change and the phase change are much greater than those at higher frequency band. That is, the useful range lies in the higher end of the axis, as the amplitude change and the phase change at lower end of the axis are actually larger than needed. For Transfer Function 2, though the phase change is relatively small at the lower frequency range, the amplitude change is quite large in this range. That is, the lower range is not suitable for this application. As the phase change decreases after a certain frequency, in the upper range, there will be a suitable operation point as the amplitude change and phase change are reasonable to compensate the distortion of the nonlinear amplifier. The upper range is preferable for the design. Transfer Function 3 differs from Transfer Function 1 and Transfer Function 2 in the distortion trend. For Transfer Function 3, the amplitude change at higher frequency band is much larger than that at lower frequency. As the phase change decreases firstly and increases after a certain frequency, the phase change at lower frequency is reasonable. That is, the lower end of the axis is suitable for this application. Though phase characteristic is very important to linearity improvement,

the intermodulation distortion arising from the phase nonlinearity is in quadrature to the amplitude nonlinearity [30], that is, it is impossible to improve the linearity simply via the approach of phase correction. In the rest of work, more effort will be spent on the linearity improvement by compensation with the reverse amplitude change.

8.4 RC Network Implementation and Circuit Transformation

In this section, we consider implementing the transfer functions, Equation (8.1), Equation (8.2) and Equation (8.3) by simple passive circuits. Consider the circuit in Figure 8.7, in which there are two components Z_1 and Z_2.

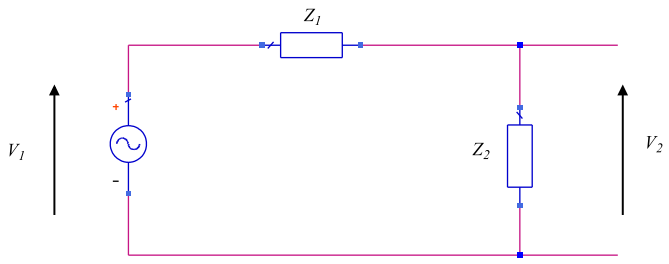


Figure 8.7: Simple circuit implementing transfer functions

From the circuit in Figure 8.7, we have

$$\frac{V_2}{V_1} = \frac{Z_2}{Z_1 + Z_2}. \tag{8.4}$$

If we let

$$Z_1 = \frac{1}{Y_1} \quad \text{and} \quad Z_2 = \frac{1}{Y_2},$$

then Equation (8.4) will be converted to

$$\frac{V_2}{V_1} = \frac{Y_1}{Y_1 + Y_2}. \tag{8.5}$$

8.4.1 Circuit Transformation for Transfer Function 1

Equation (8.1) and Equation (8.4) lead to the detailed circuit implementation in Figure 8.8, in which Z_2 is replaced by an inductor and a resistor in parallel connection. Circuit transformation will be carried out based on the circuit in Figure 8.8.

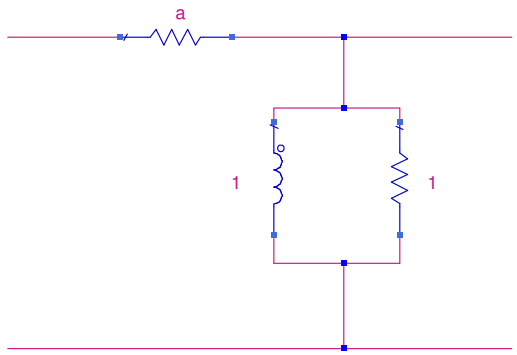


Figure 8.8: Circuit transformation of Equation (8.1) and Equation (8.4)

In order to create a predistorter, we need to translate changes in gain and phase with respect to frequency to changes in gain and phase with respect to the input signal amplitude at a fixed frequency. That means we have to introduce a nonlinear element. In the circuit in Figure 8.8 the frequency-dependant element is the inductor. In order to create the required behavior, it would be necessary that the inductor value is signal amplitude dependent and the frequency is held relatively constant. That is, the inductor would need to be nonlinear. In order to avoid this problem, we carry out circuit transformation. The circuit in Figure 8.8 can be converted, without change in transfer function, to the equivalent circuit in Figure 8.9 by scaling its three impedances by a factor proportional to $1/s$. In this circuit, the nonlinear element is a grounded resistor and the capacitors may be linear.

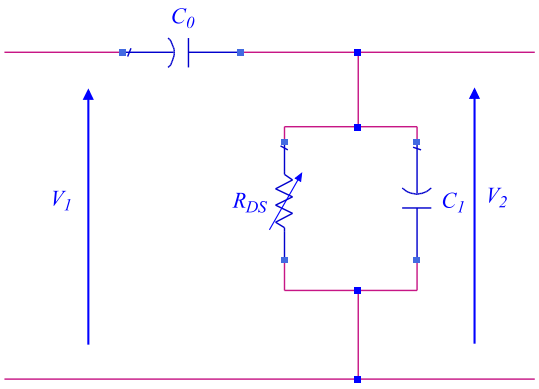


Figure 8.9: Equivalent circuit of the circuit in Figure 8.8

For the circuit in Figure 8.9, we have

$$\frac{V_2}{V_1} = \frac{Z_2}{Z_1 + Z_2} = \frac{\frac{R_{DS}}{sR_{DS}C_1+1}}{\frac{R_{DS}}{sR_{DS}C_1+1} + \frac{1}{sC_0}} = \frac{sR_{DS}}{sR_{DS} * (\frac{C_1}{C_0} + 1) + \frac{1}{C_0}}. \tag{8.6}$$

Comparison with Equation (8.1) shows that if we define $a = \frac{C_1}{C_0}$, $b = \frac{1}{C_0}$ and set the frequency ω_0 constant, then Equation (8.6) becomes

$$H(R_{DS}) = \frac{V_2}{V_1} = \frac{j\omega_0 R_{DS}}{j\omega_0 R_{DS} * (a+1) + b}, \tag{8.7}$$

which is equivalent to Equation (8.1). Now changes in the value of R_{DS} will trace similar changes in gain and phase as occur with changes in frequency ω in Equation (8.1).

An analysis setup for the circuit in Figure 8.9 is shown in Figure 8.10. The magnitude of the voltage source is set to 1 V. The value of resistor R_{DS} is swept from 8 Ohm to 210 Ohm in AC analysis and the frequency is set to a constant value of 30 GHz as the power amplifier chosen as the target works at around 30 GHz.

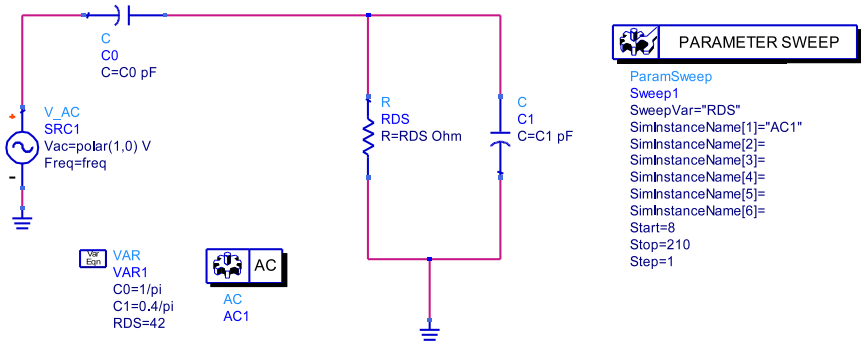
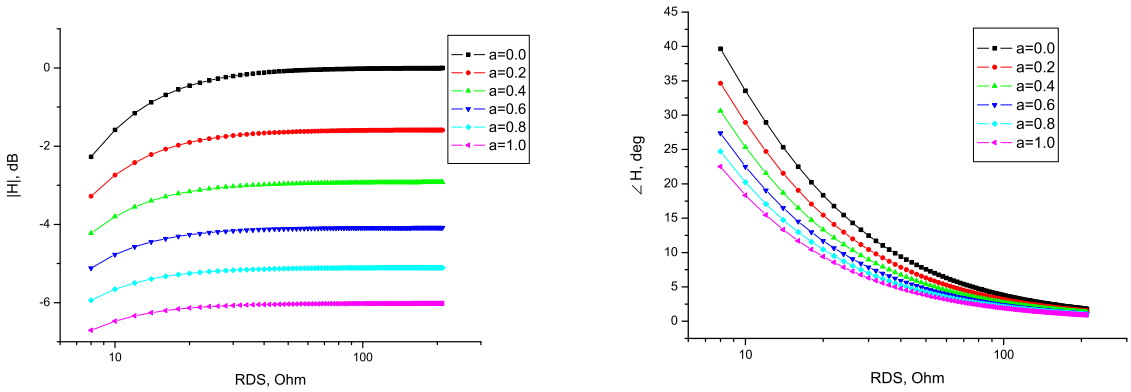


Figure 8.10: The sample circuit of the predistorter

The simulated relationship between $|H|$ and R_{DS}, $\angle H$ and R_{DS} where H is the transfer function V_2/V_1 for the circuit is shown in Figure 8.11. In Figure 8.11, the magnitude of H exhibits expansion and the phase of H exhibits compression with increasing R_{DS} as required.



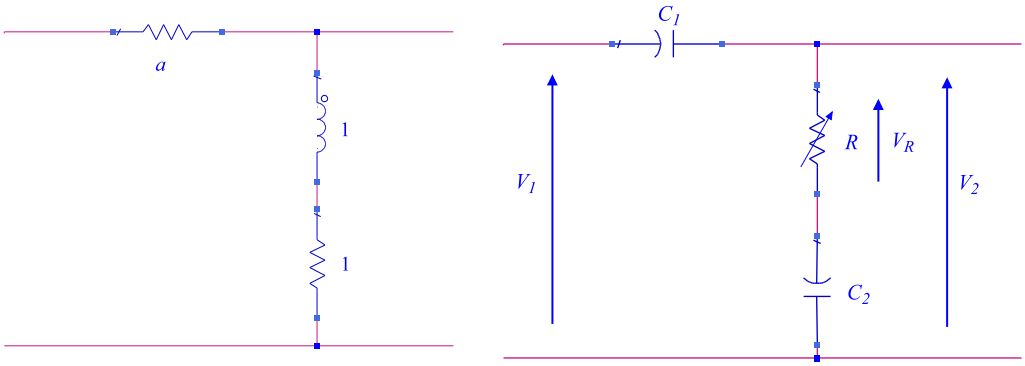
(a) The relationship between $|H|$ and R_{DS} (b) The relationship between $\angle H$ and R_{DS}

Figure 8.11: The relationship between H and R_{DS}

8.4.2 Circuit Transformation for Transfer Function 2

8.4.2.1 Circuit Transformation 1

Like the work done in Section 8.4.1, circuit transformation will be carried out for Transfer Function 2 in this section. Equation (8.2) and Equation (8.4) can lead to the circuit implementation in Figure 8.12 (a), a simple passive network in which a resistor is connected in series with an inductor replacing Z_2 in Figure 8.7.



(a) Simple circuit implementing Equation (8.7)

(b) Equivalent circuit of the circuit in Figure 8.12 (a)

Figure 8.12: Equivalent circuit implementation

Similarly a nonlinear element needs to be introduced to translate changes in gain and phase with respect to frequency to changes in gain and phase with respect to input signal level at a fixed frequency. With this guideline, the circuit in Figure 8.12 (a) can be converted, without change in transfer function, to its equivalent circuit in Figure 8.12 (b) by scaling its three impedances by the factor $1/s$. In the circuit in Figure 8.12 (b), the

nonlinear element is a resistor and the capacitor may be linear.

For the circuit in Figure 8.12 (b), we can have

$$\frac{V_2}{V_1} = \frac{Z_2}{Z_1 + Z_2} = \frac{R + \frac{1}{sC_2}}{R + \frac{1}{sC_1} + \frac{1}{sC_2}} = \frac{1 + sC_2R}{1 + \frac{C_2}{C_1} + sC_2R}. \tag{8.8}$$

Comparison with Equation (8.2) shows that C_2/C_1 corresponds with parameter a. If frequency is held constant, then changes in the value of R will trace at the same changes in gain and phase as occur with changes in frequency. An analysis setup for the circuit in Figure 8.12 (b) is shown in Figure 8.13. The magnitude of voltage source is set to 1 V. The value of resistor R_0 is swept from 8 Ohm to 210 Ohm in AC analysis. The frequency is set to a constant value of 30 GHz.

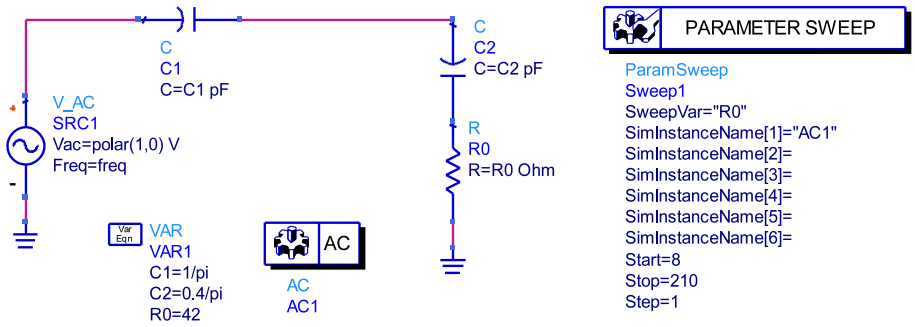


Figure 8.13: The sample circuit of the predistorter

The output voltage across the R_0 and C_2 can be expressed as below,

$$H(R) = \frac{R + \frac{1}{j\omega_0 C_2}}{R + \frac{1}{j\omega_0 C_2} + \frac{1}{j\omega_0 C1}} = \frac{1 + j\omega_0 C_2 R}{1 + \frac{C_2}{C_1} + j\omega_0 C_2 R}. \tag{8.9}$$

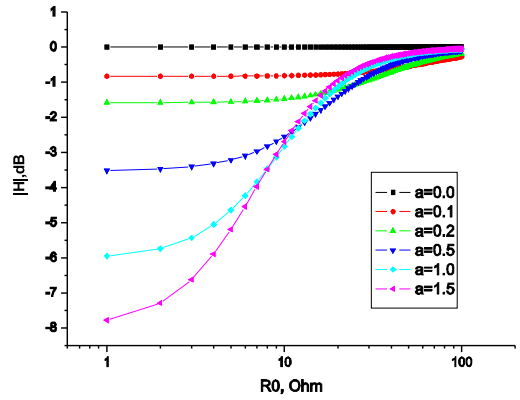
If we define $a = \frac{C_2}{C_1}$, then

$$H(R) = \frac{1 + j\omega_0 C_2 R}{1 + a + j\omega_0 C_2 R}, \tag{8.10}$$

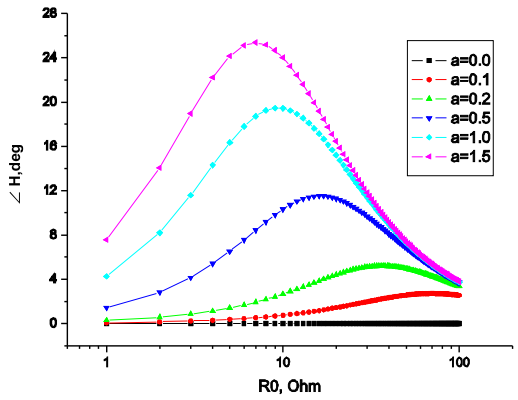
which is equivalent to Equation (8.2). Now changes in the value of R will produce similar changes in gain and phase as occur with changes in frequency ω in Equation (8.2).

Further to the initial analysis, the H verification is carried out under small signal operation. The simulated relationship between $|H|$ and R_0, $\angle H$ and R_0 where H is the transfer function for the circuit is shown in Figure 8.14. In Figure 8.14, the magnitude

of H exhibits expansion and the phase of H exhibits compression with R_0 increasing as required.



(a) The relationship between $|H|$ and R_0



(b) The relationship between $\angle H$ and R_0

Figure 8.14: The relationship between H and R_0

8.4.2.2 Circuit Transformation 2

On the other hand, Equation (8.2) and Equation (8.5) can lead to the circuit implementation in Figure 8.15, where there are three passive components, including two resistors and one capacitor.

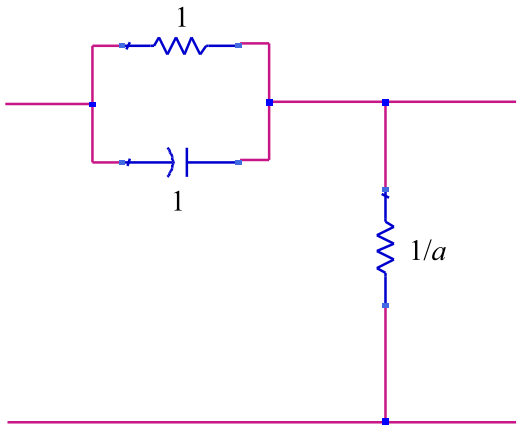


Figure 8.15: Circuit transformation of Equation (8.2) and Equation (8.5)

Similarly to the previous design, a nonlinear element will be introduced so that the changes in gain and phase with respect to frequency can be transferred to the changes in gain and phase with respect to the input signal amplitude. In the circuit in Figure 8.15 the frequency-dependant element is a capacitor. The capacitor need to be converted to a

nonlinear device by circuit transformation in order to behave signal amplitude dependent. Unlike previous designs in which the scaling factor is $1/s$, the circuit in Figure 8.15 can be converted to the equivalent circuit in Figure 8.16 by scaling its three impedances by a factor proportional to s without change in transfer function. In this circuit, the nonlinear element is a resistor and the inductor may be linear.

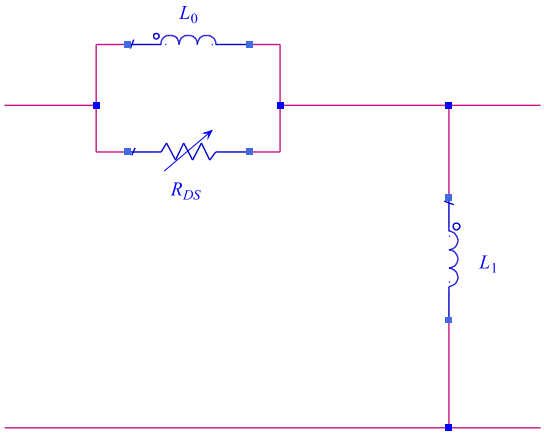


Figure 8.16: Equivalent circuit of the circuit in Figure 8.15

For the circuit in Figure 8.16, we can have

$$\frac{V_2}{V_1} = \frac{Y_1}{Y_1 + Y_2} = \frac{\frac{1}{sL_0} + \frac{1}{R_{DS}}}{\frac{1}{sL_0} + \frac{1}{R_{DS}} + \frac{1}{sL_1}} = \frac{1 + s\frac{L_0}{R_{DS}}}{1 + \frac{L_0}{L_1} + s\frac{L_0}{R_{DS}}}. \tag{8.11}$$

Comparison with Equation (8.2) shows that if we define $a = \frac{L_0}{L_1}$ and set the frequency ω_0 constant, then

$$H(R_{DS}) = \frac{V_2}{V_1} = \frac{1 + j\omega_0 L_0 \frac{1}{R_{DS}}}{1 + a + j\omega_0 L_0 \frac{1}{R_{DS}}}, \tag{8.12}$$

which is equivalent to Equation (8.2). Now changes in the value of $\frac{1}{R_{DS}}$ will trace similar changes in gain and phase as occur with changes in frequency ω in Equation (8.2). Similar analysis has been carried out in Section 8.4.1, so repeated work is ignored here.

8.4.3 Circuit Transformation for Transfer Function 3

The circuit in Figure 8.7 will be still employed for the RC network implementation here. From Equation (8.3) and Equation (8.4), we can derive the circuit implementation in Figure 8.17.

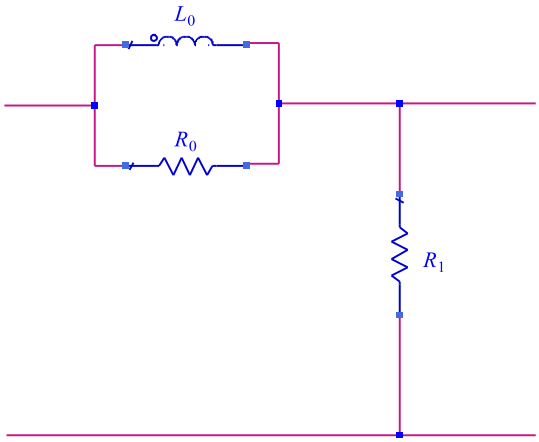


Figure 8.17: Circuit transformation of Equation (8.3) and Equation (8.4)

The predistortion circuit can be obtained by circuit transformation. The frequency-dependant element, inductor L_0 in Figure 8.17, would need to be translated to be nonlinear signal amplitude dependent at a fixed frequency. Similarly to previous designs, the circuit in Figure 8.17 can be converted, without change in transfer function, to the equivalent circuit in Figure 8.18 by scaling its three impedances by a factor proportional to $1/s$. In this circuit, the nonlinear element is a resistor and the capacitors may be linear.

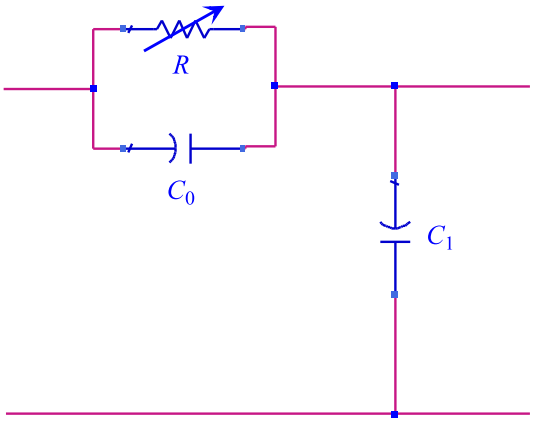


Figure 8.18: Equivalent circuit of the circuit in Figure 8.15

For the circuit in Figure 8.18, we can have

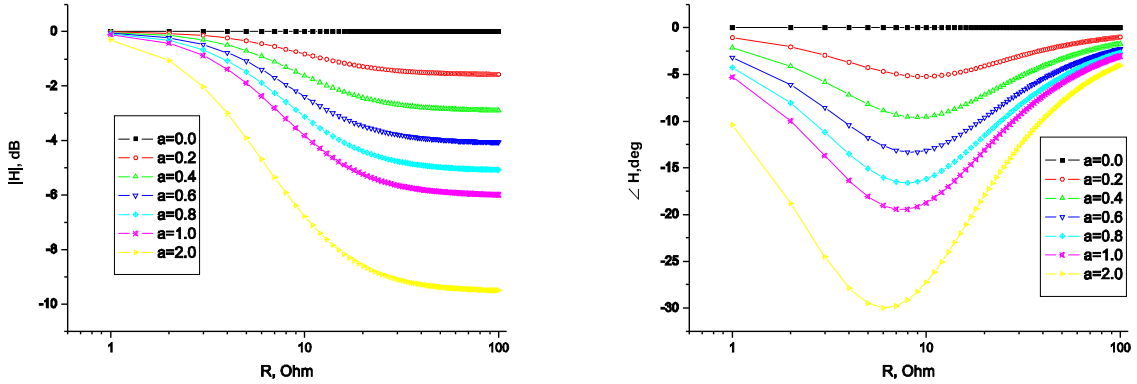
$$\frac{V_2}{V_1} = \frac{Z_1}{Z_1 + Z_2} = \frac{\frac{1}{sC_1}}{\frac{1}{sC_1} + \frac{R}{1+sC_0R}} = \frac{sR + \frac{1}{C_0}}{sR(1 + \frac{C_1}{C_0}) + \frac{1}{C_0}}. \tag{8.13}$$

Comparison with Equation (8.3) shows that if we define $a = \frac{C_1}{C_0}$, $b = \frac{1}{C_0}$ and set the frequency ω_0 constant, then

$$H(R) = \frac{j\omega_0 R + b}{j\omega_0 R(1+a) + b}, \tag{8.14}$$

which is equivalent to Equation (8.3). Now changes in the value of R will trace out similar changes in gain and phase as occur with changes in frequency ω in Equation (8.3).

The simulated relationship between $|H|$ and R, $\angle H$ and R where H is the transfer function V_2/V_1 for the circuit is shown in Figure 8.19. In Figure 8.19, the magnitude of H exhibits compression and the phase of H exhibits compression first and expansion then with R increasing. If R would decrease with the input signal amplitude, the magnitude of H can exhibit expansion and the phase of H can exhibit compression as required. We next need to realize R as a nonlinear resistor with an effective value varying with the input signal amplitude in the required way.



(a) The relationship between $|H|$ and R (b) The relationship between $\angle H$ and R

Figure 8.19: The relationship between H and R

8.4.4 Comparison between the Circuit Transformations

Up to now, the three transfer functions have been transformed to equivalent circuits with nonlinear elements via circuit transformation. These equivalent circuits have been proven to have suitable characteristics for the predistortion function in the sections above. The comparisons between the transformations are shown in Table 8.2.

From Table 8.2, we can see that the main difference lies in the transfer characteristics. The gain decreases for Transfer Function 3 while the gain increases for other two transfer functions with increasing the nonlinear resistor value. As the preferred operation

Table 8.2: Circuit Transformation Comparisons

Comparison	Transfer Function 1	Transfer Function 2	Transfer Function 3
Circuit Transformation	Figure 8.9	Figure 8.12 (b); Figure 8.16	Figure 8.18
Equivalent Equation	Equations (8.7)	Equations (8.9); Equations (8.12)	Equations (8.14)
Variable Definition	$a = \frac{C_1}{C_0}$, $b = \frac{1}{C_0}$	$a = \frac{C_2}{C_1}$; $a = \frac{L_0}{L_1}$	$a = \frac{C_1}{C_0}$, $b = \frac{1}{C_0}$
Transfer Curves	Figure 8.11	Figure 8.14	Figure 8.19
Transfer Characteristics	Gain Expands; Phase Compresses	Gain Expands; Phase Expands firstly, then Compresses	Gain Compress; Phase Compresses firstly, then Expands
Preferred operation range	Upper end	Upper end	Lower end

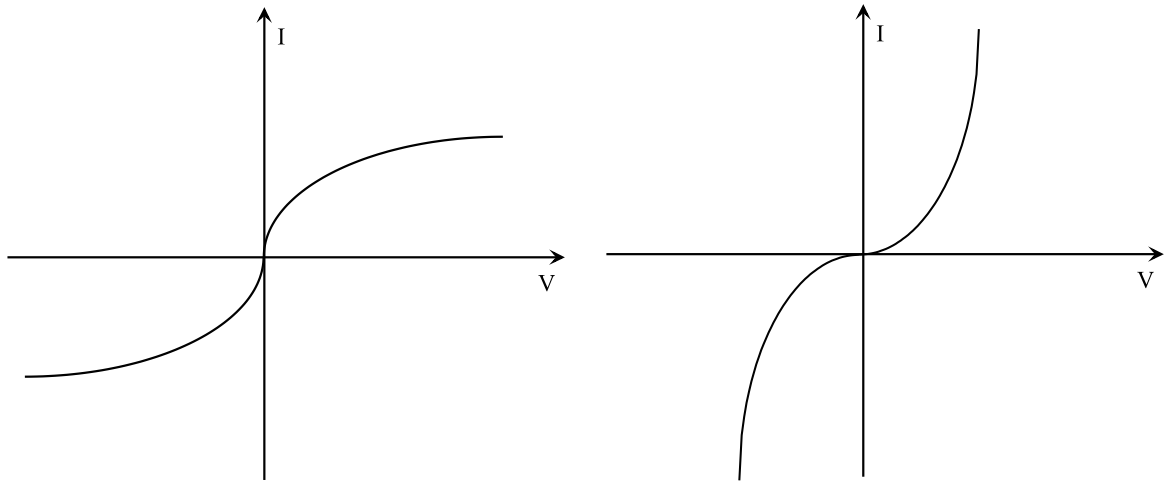
range for Transfer Function 3 lies in the lower end while upper end is preferred for the other two functions, the insertion loss of the circuit based on Transfer Function 3 will be much lower than the other two correspondingly. As the insertion loss is lower, the effect on other metrics will be lighter.

8.5 Nonlinear Conductance Element Implementation

If resistor R in the circuits shown in Figure 8.9, Figure 8.12 (b), Figure 8.16 and Figure 8.18 is nonlinear, its effective value will depend on its voltage V_R. Then the relationship between H and R can be converted to the relationship between H and the resistor voltage V_R. Since the gain and phase of the circuit are expected to depend on the amplitude of the input signal V_1, we must take into account the relationship between V_1 and V_R, which depends on V_1.

Two general kinds of symmetrical nonlinear I-V characteristics that may be considered are shown in Figure 8.20. For the nonlinear curve 1 in Figure 8.20 (a), the larger the input signal amplitude is, the larger the resistance (smaller the conductance) is. The

increase in $\hat{V}_1$ initially increases V_R but this effect will reach a limit. While for the nonlinear curve 2 in Figure 8.20 (b), the opposite applies. Because of this, when the nonlinear curve 2 in Figure 8.20 (b) is applied, the I-V curve tends to reduce V_R towards zero when $\hat{V}_1$ increases, thus counteracting the nonlinear effect.



(a) Nonlinear I-V curve 1 (b) Nonlinear I-V curve 2

Figure 8.20: Two general kinds of nonlinear I-V curves

For the circuit implementation for Transfer Function 1 in Figure 8.9, the circuit implementation for Transfer Function 2 in Figure 8.12 (b), according to Equation (8.7) and Equation (8.10), the effective resistance R_{eff} is required to increase with increasing the signal amplitude and hence the I-V nonlinear curve 1 in Figure 8.20 (a) is preferable. While for the circuit implementation for Transfer Function 2 in Figure 8.16 and the circuit implementation for Transfer Function 3 in Figure 8.18, according to Equation (8.12) and Equation (8.14), $\frac{1}{R}$ is required to increase with increasing the signal amplitude, that is, R should decrease with increasing the signal amplitude and hence the I-V nonlinear curve 2 in Figure 8.20 (b) is suitable for these applications.

The nonlinear characteristic corresponding to the nonlinear I-V curves in Figure 8.20 may be realized by FET devices with proper configuration, which can replace the nonlinear resistor and realize the predistortion function.

8.5.1 Circuit Implementation for the Nonlinear I-V Curve 1

8.5.1.1 Circuit Implementation 1

The nonlinear characteristic shown in Figure 8.20 (a) can be realized by two depletion-mode FETs connected back-to-back in series as in Figure 8.21. The I-V characteristic of this circuit was analyzed using OMMIC pHEMTs and the simulation results are shown in Figure 8.22. We can see that the I-V curve in Figure 8.22 (a) has a similar form to the nonlinear curve 1 in Figure 8.20 (a). So this configuration can realize the nonlinear resistance characteristic required. In Figure 8.22 (b), the effective resistance R_{eff}, defined as the peak value of the voltage of the voltage source V_{DS} divided by the peak current, increases with increasing I_{DS}. So if we replace R_{DS} in Figure 8.9 with the FETs in Figure 8.21, the circuit in Figure 8.9 will be transformed to a predistortion circuit with the features we have discussed.

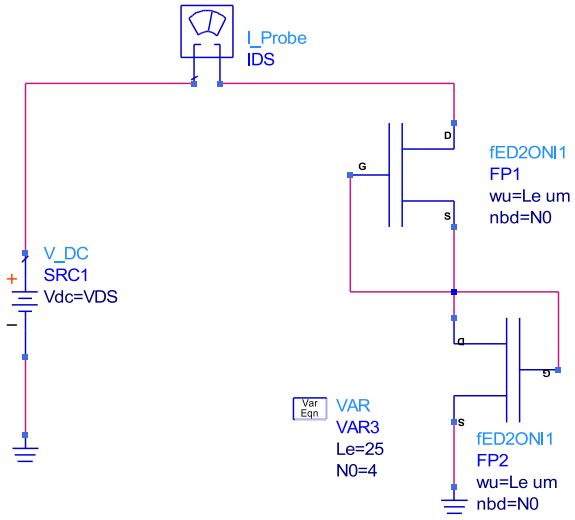
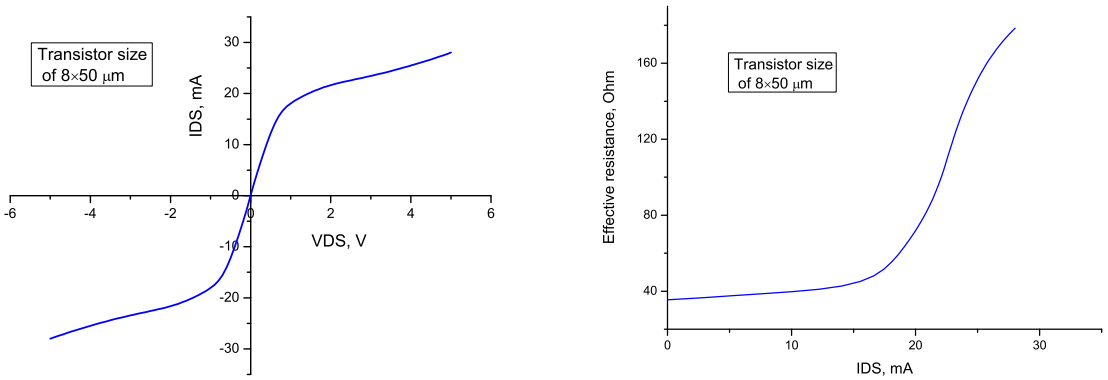


Figure 8.21: FET device used to replace R_0



(a) I-V curve of the FET (b) The equivalent resistance of the FET

Figure 8.22: The characteristic of the FET configuration

8.5.1.2 Circuit Implementation 2

Figure 8.23 shows another circuit topology which is a more general form of the circuit in Figure 8.21 and can potentially replace the nonlinear R in Figure 8.9 and Figure 8.12 (b).

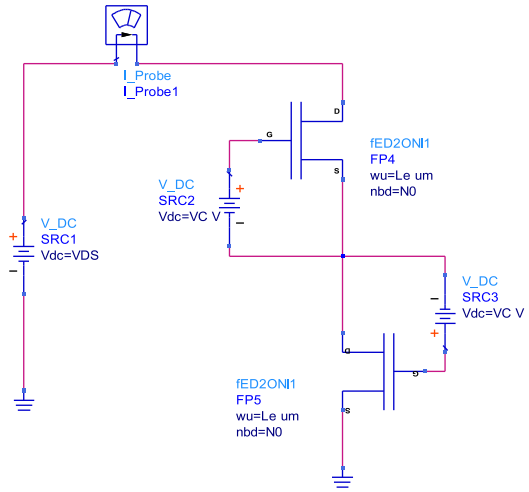
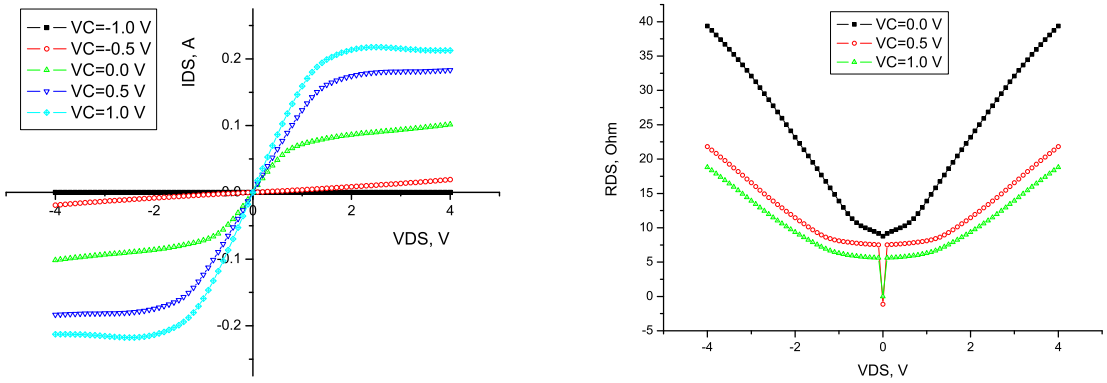


Figure 8.23: Another FET configuration used to replace the nonlinear resistor

Compared with the topology in Figure 8.21, the new topology has non-zero gate bias for both transistors. Thus this topology has more freedom to adjust its characteristics. Its related characteristics are shown in Figure 8.24. We can see that the I-V curves in Figure 8.24 (a) are similar to the I-V curve proposed in Figure 8.20 (a) and when the bias voltage is zero, it will be the same as the I-V curve in Figure 8.22 (a).

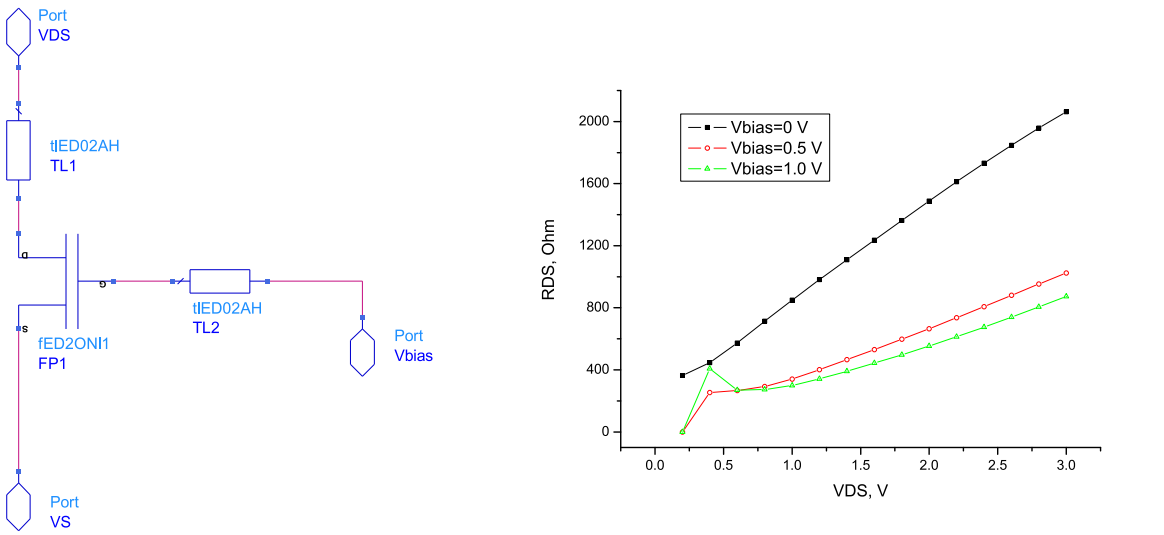


(a) I-V characteristic at different bias (b) R_{DS} at different biases

Figure 8.24: Characteristics at different biases

8.5.1.3 Circuit Implementation 3 and Circuit Implementation 4

The designs above are primarily built on the configuration with two FET transistors. Further analysis reveals that such nonlinear characteristic can be realized by a single transistor with proper configuration. Circuit implementation 3 and 4 are realized by the single transistor structure. The third circuit implementation is the circuit in Figure 8.25 (a). In Figure 8.25 (a), the circuit used to replace the nonlinear resistor is comprised of a single FET transistor with a separate bias gate voltage. Preliminary analysis in Figure 8.25 (b) shows that its effective resistance can increase with the signal amplitude.



(a) The third circuit implementation (b) The effective resistance under different operations

Figure 8.25: The third circuit implementation and its characteristics

Further to the design in Figure 8.25, another single FET design with simplified

configuration is proposed in Figure 8.26 as the fourth circuit implementation. Compared with the FET configuration in Figure 8.25 (a), the gate and the drain have the same voltage in the new configuration.

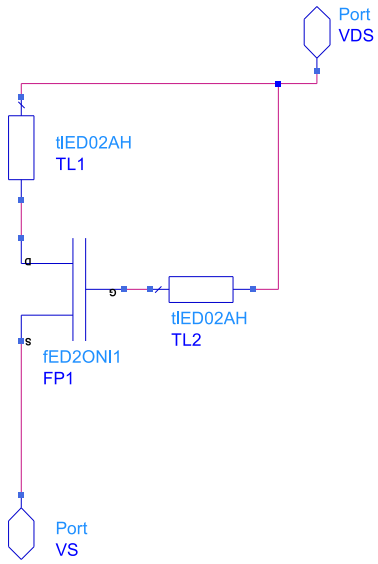
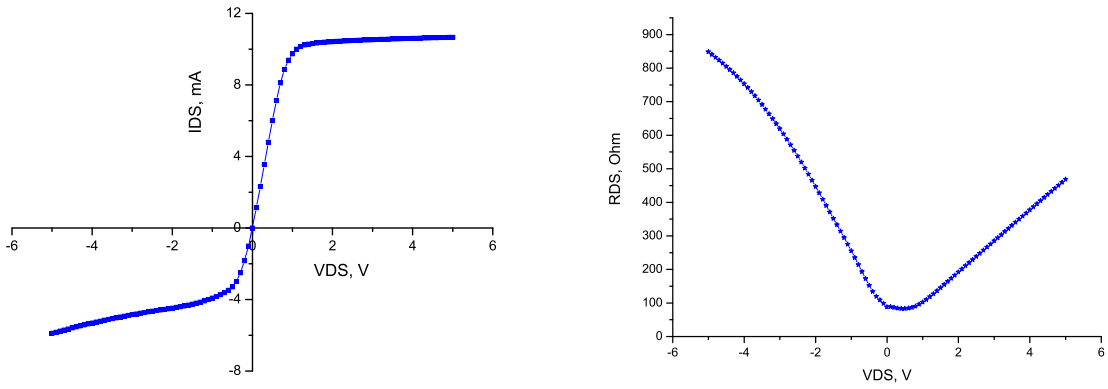


Figure 8.26: The fourth circuit implementation

Its characteristics were analyzed and results are shown in Figure 8.27. The I-V curve shown in Figure 8.27 (a) is roughly similar to the I-V curve in Figure 8.22 and its effective resistance in Figure 8.27 (b) increases with increasing VDS, that is, increases with the signal amplitude.



(a) I-V curve of the single FET configuration (b) R_{DS} under small signal operation

Figure 8.27: Characteristics under small signal operation

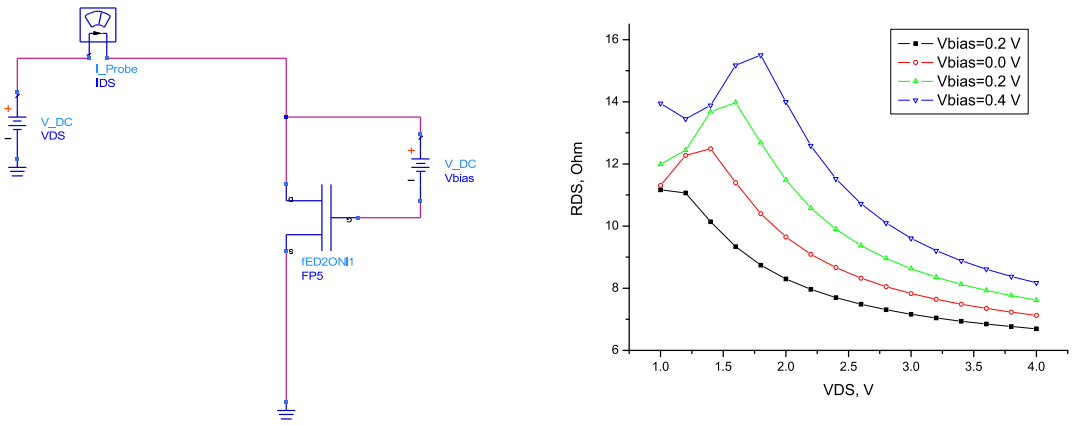
8.5.2 Circuit Implementation for the Nonlinear I-V Curve 2

According to Equation (8.12) and Equation (8.14), $1/R$ is required to increase with increasing the signal amplitude. That is, R should decrease with increasing the signal amplitude and hence the nonlinear I-V curve 2 in Figure 8.20 (b) is suitable for this application.

For the nonlinear I-V curve 2 in Figure 8.20 (b), the larger the input signal amplitude is, the smaller the resistance is. Because of this, the I-V curve tends to reduce V_R towards zero when $\hat{V}_1$ increases, thus counteracting the nonlinear effect, which is just required in this application. Just like the nonlinear characteristic corresponding to the nonlinear I-V curve 1, the nonlinear I-V curve 2 in Figure 8.20 (b) can also be realized FET devices with proper configuration where the resistance decreases with increasing the input signal amplitude.

8.5.2.1 Circuit Implementation for Transfer Function 2 and Transfer Function 3

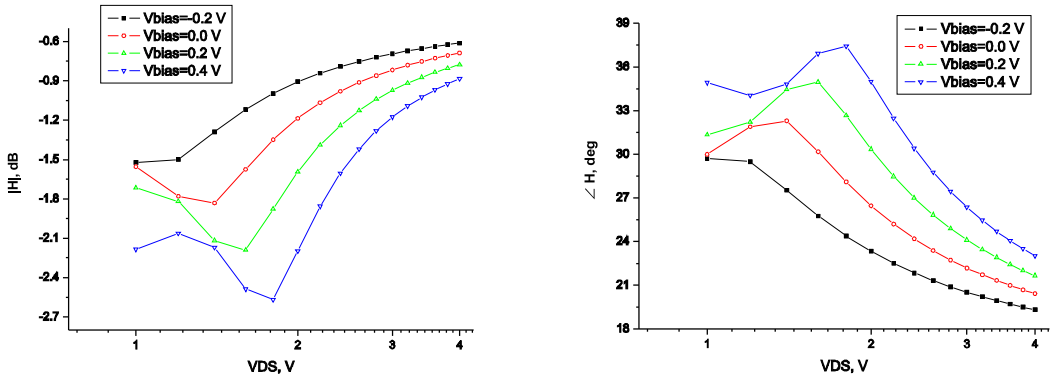
The nonlinear characteristic corresponding to nonlinear I-V curve 2 in Figure 8.20 (b) can be realized by a single FET transistor with proper configuration. A case in point is the circuit in Figure 8.28 (a), where there is a single FET with bias and Figure 8.28 (b) is its effective resistance at different biases. In Figure 8.28 (b), we can see that with this configuration, the resistance decreases with increasing VDS, or the signal amplitude, which is similar to the characteristic shown in Figure 8.20 (b).



(a) FET device used to replace R_{DS} (b) Effective resistance at different biases

Figure 8.28: The single FET configuration and its characteristic

So this configuration can realize the nonlinear characteristic required. So if we replace the R in Figure 8.16 and Figure 8.18 with the FET in Figure 8.28 (a), the circuits in Figure 8.16 and Figure 8.18 will be transformed to a predistortion circuit with the features we have discussed. With the resistance in Figure 8.28 (b), the transfer function can be plotted in Figure 8.29, where the amplitude of H expands with increasing VDS while the phase of H compresses with increasing VDS.

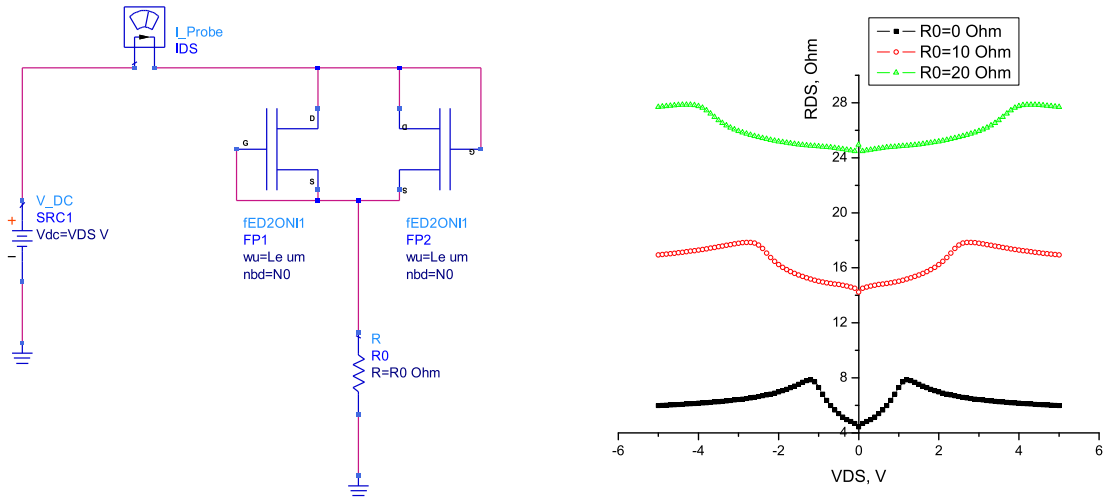


(a) Magnitude response of H (b) Phase response of H

Figure 8.29: H expression at different biases

8.5.2.2 Circuit Implementation for Transfer Function 3

Further to the circuit proposed in Section 8.5.2.1, another implementation that can be potentially suitable for the passive RC network design approach proposed in Chapter 7 can be employed. The topology which is symmetrical is shown in Figure 8.30 (a) and its characteristics are shown in Figure 8.30 (b). In Figure 8.30 (a), two FET transistors are connected in parallel and a resistor R0 is connected in series with them to adjust the effective resistance. From Figure 8.30 (b), we can see the $R0$ can effectively adjust the effective resistance and with proper bias, the resistance of the circuit can decrease with increasing the input signal amplitude. Thus this circuit can be suitable for this application. As the resistance is required to decrease with increasing the input power, $R0$ in this application is chosen to be 0 Ohm, which can bring a minimum resistance and maximize the decreasing range shown in Figure 8.30 (b).



(a) The circuit used to replace the nonlinear R (b) Effective resistance at different biases

Figure 8.30: The FET configuration and its characteristics

Having presented and validated a number of nonlinear resistor circuits, we are ready to investigate predistortion circuits using them.

8.6 Overview of Performance Comparison for PD

8.6.1 General Concepts

In order to evaluate the predistortion circuits conveniently, several concepts such as, $IMD3$ improvement, normalized $IMD3$ improvement and net $IMD3$ improvement are introduced before evaluation.

$IMD3$ improvement is defined as the difference between $IMD3$ after linearization and $IMD3$ before linearization and can be expressed as

$$IMD3_{improvement} = |IMD3_{after} - IMD3_{before}|, \tag{8.15}$$

where $IMD3_{after}$ is the $IMD3$ after linearization and $IMD3_{before}$ is the $IMD3$ before linearization.

Normalized $IMD3$ improvement is defined as $IMD3$ improvement at cost of 1 dB of insertion loss. It can be expressed as

$$IMD3_{normalized} = \frac{IMD3_{improvement}}{Insertion\,loss}, \tag{8.16}$$

where insertion loss is the gain degeneration brought by the predistortion circuit.

Unlike the predistortion circuit built on amplifier, the predistortion circuit built on passive RC network will inevitably introduce some insertion loss. Thus part of the linearity improvement comes from power back-off. Thus the net $IMD3$ improvement is the $IMD3$ improvement benefiting from predistortion without contribution from power back-off. It can be expressed as

$$IMD3_{net} = IMD3_{normalized} - IMD3_{backoff}, \tag{8.17}$$

where $IMD3_{backoff}$ is the normalized $IMD3$ improvement brought by power back-off.

According to the principle of power back-off, the $IMD3$ will improve by about 3 dB when the input power is 1 dB lower. As the linearity is compared at an input power of 0 dBm, the normalized $IMD3$ improvement brought by power back-off can be calculated from Equation (8.18).

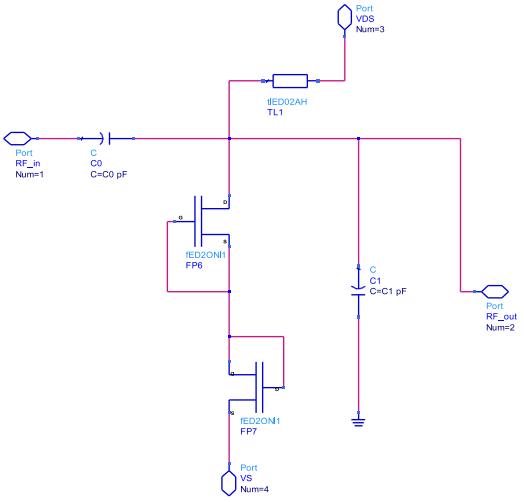
$$IMD3_{backoff} = 3 \times (Pout_{diff} - 1), \tag{8.18}$$

where $Pout_{diff}$ is the output power difference between before and after linearization and '1' represents 1 dB, the normalized gain.

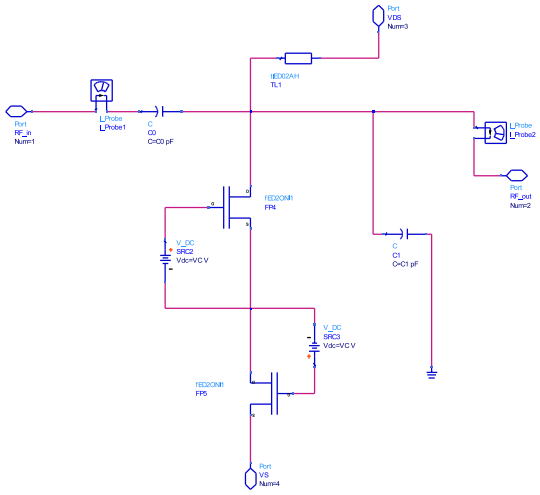
Just as the previous designs, the millimeter-wave power amplifier for LMDS application designed in Chapter 4 will be used as the test bench for linearization and comparison.

8.6.2 Overview of Performance Comparison

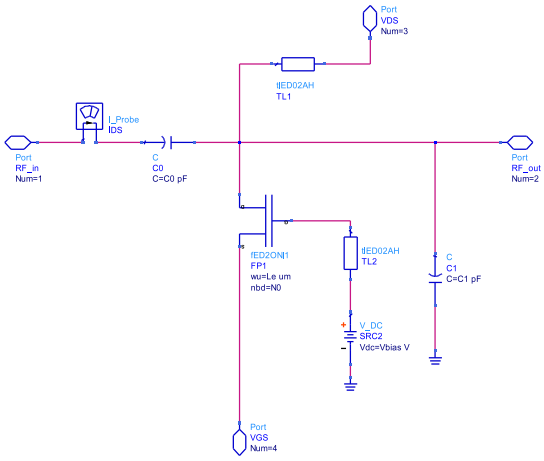
In Section 8.5, four circuit implementations were proposed in Section 8.5.1 for Transfer Function 1, five circuit implementations were proposed in Section 8.5.1 and Section 8.5.2 for on Transfer Function 2 and two circuit implementations were proposed in Section 8.5.2 for on Transfer Function 3. These predistortion circuits are shown in Figure 8.31, Figure 8.32 and Figure 8.33 respectively.



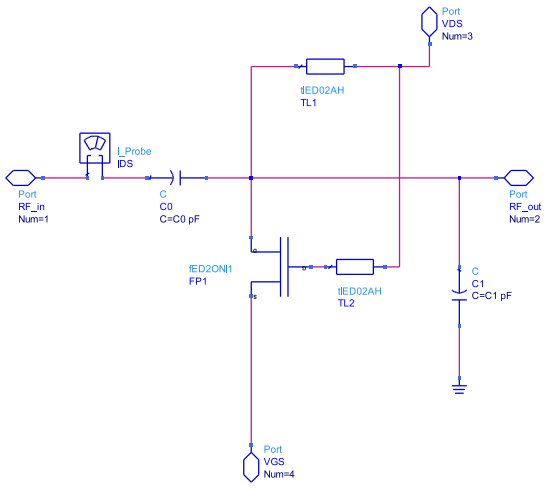
(a) Circuit A



(b) Circuit B

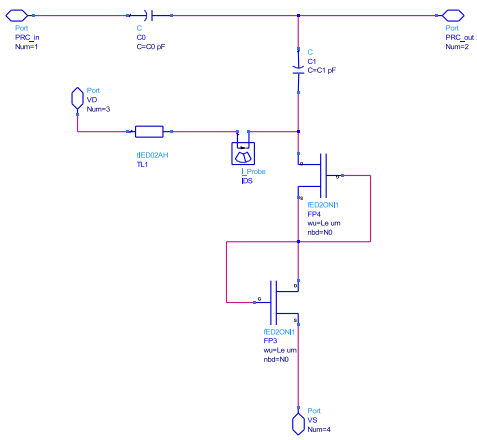


(c) Circuit C

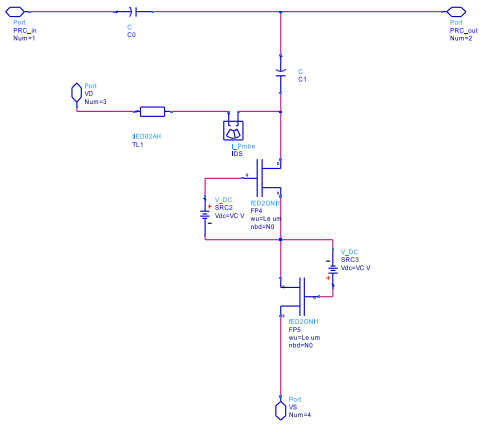


(d) Circuit D

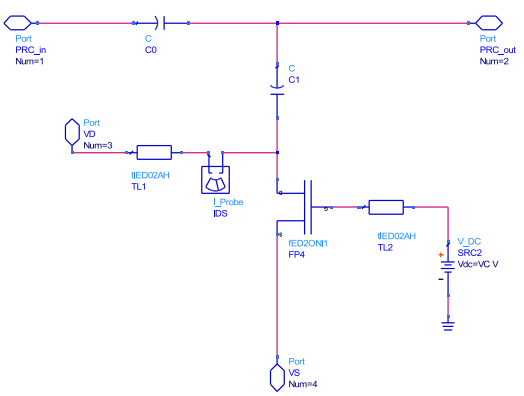
Figure 8.31: The predistortion circuits based on Transfer Function 1



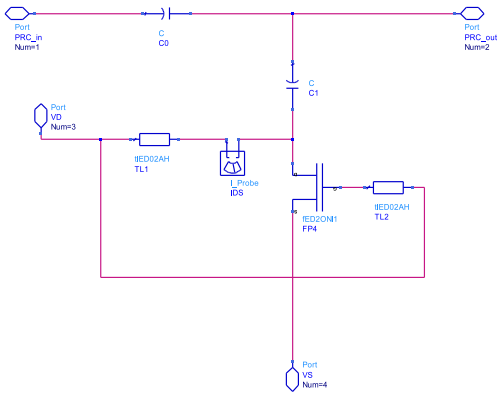
(a) Circuit A



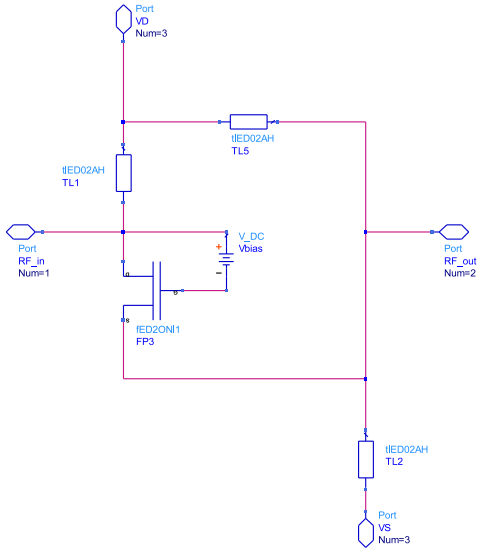
(b) Circuit B



(c) Circuit C

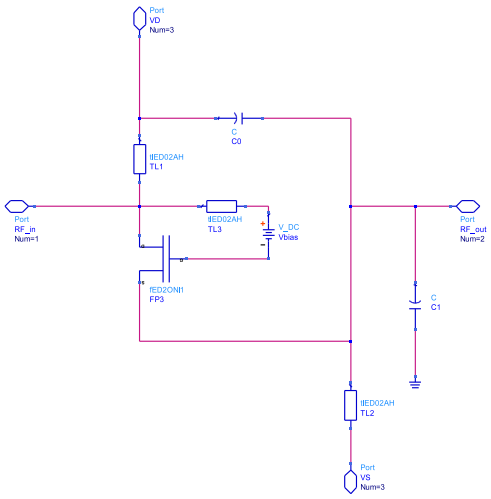


(d) Circuit D

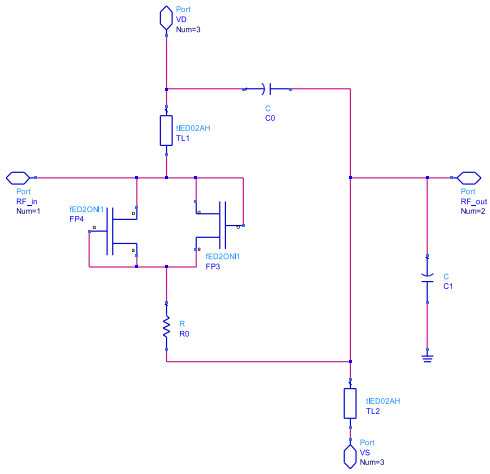


(e) Circuit E

Figure 8.32: The predistortion circuits based on Transfer Function 2



(a) Circuit E



(b) Circuit F

Figure 8.33: The predistortion circuits based on Transfer Function 3

Among these circuits, the circuits in Figure 8.31 (a), (b), Figure 8.32 (a), (b) and Figure 8.33 (b) are based on two transistors configuration while the circuits in Figure 8.31 (c), (d), Figure 8.32 (c), (d) (e) and Figure 8.33 (a) are based on single transistor configuration. The circuits in Figure 8.31 and Figure 8.32 (a) $\sim$ (d) employ the type of nonlinear characteristic in Figure 8.20 (a) while the circuits in Figure 8.32 (e) and Figure 8.33 employs the type of nonlinear characteristic in Figure 8.20 (b).

With these predistortion circuits, different levels of linearity improvements were achieved for the millimeter-wave power amplifier and they are shown in Table 8.3 and Table 8.4, in which the data in Table 8.3 is based on the type of nonlinear characteristic in Figure 8.20 (a) while the data in Table 8.4 is based on the type of nonlinear characteristic in Figure 8.20 (b). All the comparisons are in term of net $IMD3$ improvement. The net $IMD3$ improvement ranges from 3.78 dB to 19.91 dB, which demonstrates that the predistortion circuits based on the passive RC network approach can substantially improve the linearity. From the comparisons, we can see that the linearity improvements brought by the circuits based on the transfer characteristic in Figure 8.20 (b) are much higher than the circuits based on the transfer characteristic in Figure 8.20 (a). Full performance data for selected predistortion circuits will be introduced in Section 8.6.3 and full discussion of the results will be given in Section 8.7.

Table 8.3: Overview 1 of linearity improvements in term of net $IMD3$ improvement

	Circuit A	Circuit B	Circuit C	Circuit D
Transfer Function 1	Figure 8.31 (a)	Figure 8.31 (b)	Figure 8.31 (c)	Figure 8.31 (d)
	$IMD3$_high: 5.34 dB	$IMD3$_high: 7.87 dB	$IMD3$_high: 3.83 dB	$IMD3$_high: 4.74 dB
	$IMD3$_low: 5.27 dB	$IMD3$_low: 8.82 dB	$IMD3$_low: 3.78 dB	$IMD3$_low: 4.71 dB
Transfer Function 2	Figure 8.32 (a)	Figure 8.32 (b)	Figure 8.32 (c)	Figure 8.32 (d)
	$IMD3$_high: 4.20 dB	$IMD3$_high: 5.25 dB	$IMD3$_high: 4.90 dB	$IMD3$_high: 4.68 dB
	$IMD3$_low: 4.20 dB	$IMD3$_low: 6.06 dB	$IMD3$_low: 4.52 dB	$IMD3$_low: 4.64 dB

Table 8.4: Overview 2 of linearity improvements in term of net $IMD3$ improvement

	Circuit E	Circuit F
Transfer Function 2	Figure 8.32 (e)	
	$IMD3$_high: 9.94 dB $IMD3$_low: 11.46 dB	
Transfer Function 3	Figure 8.33 (a)	Figure 8.33 (b)
	$IMD3$_high: 19.91 dB $IMD3$_low: 15.06 dB	$IMD3$_high: 13.20 dB $IMD3$_low: 12.26 dB

8.6.3 Full Performance Data for Selected Predistortion Circuits

Further to the performance overview in Section 8.6.2, full performance data for selected predistortion circuits will be introduced in this section.

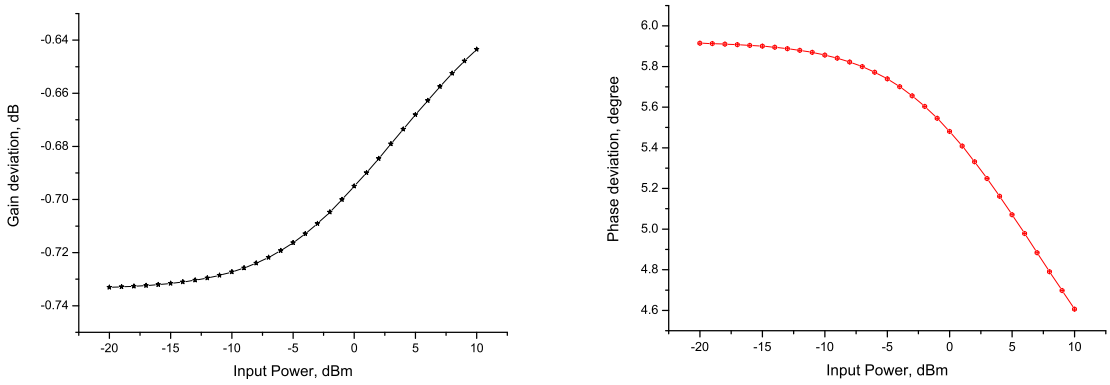
8.6.3.1 Performance Comparison for the Circuit 2 in Figure 8.31 (b)

The Circuit 2 in Figure 8.31 (b) was selected because the exploration to the structure based on two transistor in a general form can help to understand other circuits. The predistortion circuit in Figure 8.31 (b) is the circuit implementation based on the type of nonlinear characteristic in Figure 8.20 (a). The RF_in port is the input port, the RF_out port is the output port used to connect to main stage PA, and the VD port connects to the power supply via a high impedance line. If furthermore the C_1 in Figure 8.31 (b) can be regarded as part of the input capacitance of the power amplifier stage, then the rest of the circuit can work as the predistortion circuit for the power amplifier. This idea would be quite different from the conventional predistortion circuit design where PA and PD tend to be treated as separate blocks.

As the predistortion circuit is a passive circuit in nature, it is inevitable that this circuit will introduce some insertion loss and one of the goals in the overall circuit design is to alleviate the burden of insertion loss. In order to minimize the impact of insertion loss, the size of the transistors in the PD was chosen to be 2×5 μm. With this size, the insertion loss is low and linearity improvement is affected only slightly. FET size could be further adjusted at the cost of increased loss which might still be acceptable. Predistortion

characteristic can also be optimized by factors a and factor b through adjusting C_0 and C_1 as described in Equation (8.7) in Section 8.4.1.

For the PD, an input matching network with MMIC microstrip components is designed to translate the impedance to 50 Ohm and the output is connected to the PA directly since the input capacitance of the PA is part of the PD. The gain and phase deviation characteristics for the PD circuit without considering the PA are shown in Figure 8.34. As in this design, the PA will play a role in the predistortion function, the situation without considering the PA will be a bit different from the conventional PD, which needs a relatively large gain and phase deviation.

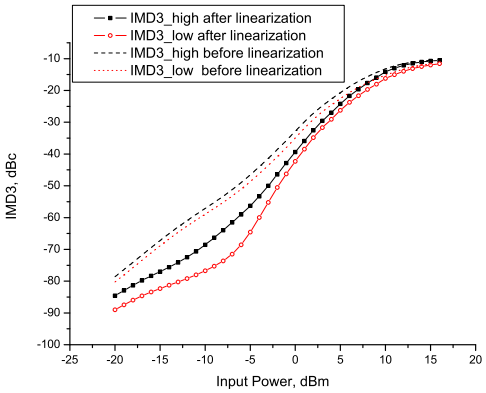


(a) Gain deviation characteristic (b) Phase deviation characteristic

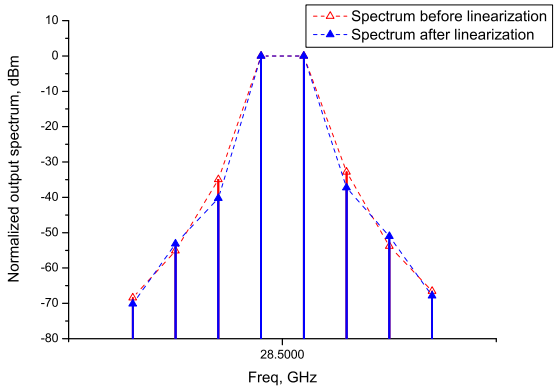
Figure 8.34: Transfer characteristics of the PD

With the predistortion circuits, the performance, especially linearity, was improved significantly. Figure 8.35 (a) and Figure 8.35 (d) show the $IMD3$ characteristic and the normalized $IMD3$ improvement respectively. In this case, IMD characteristics and spectrum were simulated at the fundamental frequency of 28.5GHz and frequency spacing of 50 KHz. $IMD3$ after linearization reaches -39.35 dBc and -42.30 dBc at upper channel and lower channel respectively. The net $IMD3$ improvement without the contribution of power back-off is about 7.87 dB and 8.82 dB respectively when the input power is 0 dBm. As the gain degenerates as the denominator in Equation (8.16) becomes smaller with increasing input power, the net $IMD3$ improvement increases dramatically when the input power is very high. Thus the linearity has improved greatly while other specifications are affected only slightly as stated in Table 8.5.

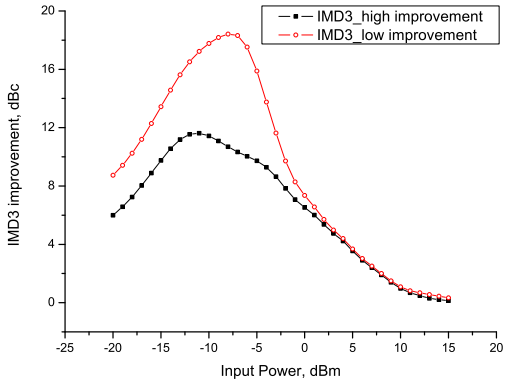
The results before and after linearization are listed in Table 8.5 and Table 8.6.



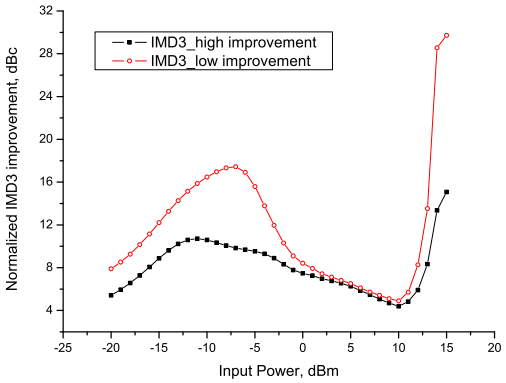
(a) $IMD3$ comparison



(b) Spectrum comparison



(c) $IMD3$ improvement comparison



(d) Normalized $IMD3$ improvement comparison

Figure 8.35: Major linearly metrics Comparisons

Table 8.5: Comparisons of performance for Circuit 2

Specifications	Before linearization	After linearization
$P_{out,1dB}$	18.37 dBm	19.08 dBm
Power Gain@P_{in}=0 dBm	15.00 dB	14.13 dB
PAE_{1dB}	17.73%	20.70%
PAE_{peak}	35.01%	34.21%
$IMD3$@P_{in}=0 dBm	$IMD3$_high: -32.82 dBc $IMD3$_low: -34.94 dBc	$IMD3$_high: -39.35 dBc $IMD3$_low: -42.30 dBc

Table 8.6: Linearity improvement for Circuit 2

$IMD3$ improvement @P_{in}=0 dBm	$IMD3$_high: 6.53 dB $IMD3$_low: 7.36 dB
Normalized $IMD3$ improvement @P_{in}=0 dBm	$IMD3$_high: 7.48 dB $IMD3$_low: 8.43 dB
Net $IMD3$ improvement @P_{in}=0 dBm	$IMD3$_high: 7.87 dB $IMD3$_low: 8.82 dB

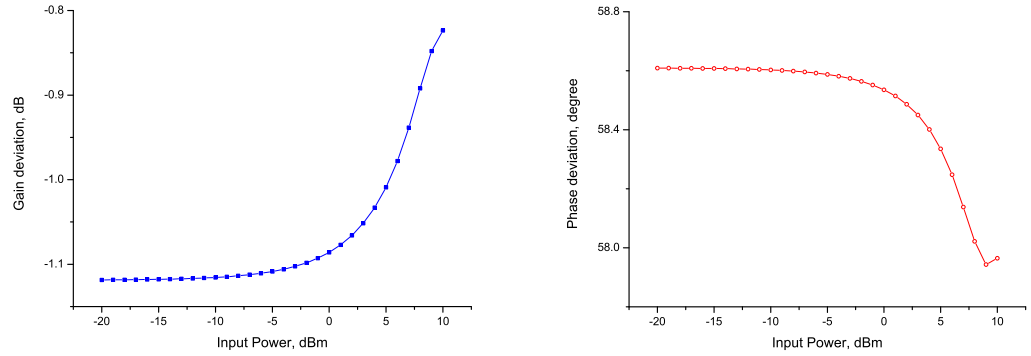
Compared with the predistortion circuit based on the circuit in Figure 8.21, the predistortion circuit in Figure 8.31 (b) has a much higher normalized $IMD3$ improvement and net $IMD3$ improvement. Thus the predistortion circuit with new proposed circuit has a much higher linearization capability.

8.6.3.2 Performance Comparison for the Circuit 5 in Figure 8.32 (e)

Having explored the structure with two transistors, the structure with single transistor based on the type of nonlinear characteristic in Figure 8.20 (b) is discussed in this section. For the predistortion circuit in Figure 8.32 (e), in order to achieve a balance between the insertion loss and linearity improvement, the size of transistor is chosen to be 4×50 μm. Similarly predistortion function can also be optimized by factor a through adjusting L_0 and L_1 as described in Equation (8.11) in Section 8.4.2 and in this application, the inductance can be adjusted by changing the width and length of the microstrip line.

The gain and phase deviation characteristics are shown in Figure 8.36. In Figure 8.36, the insertion loss is less than 1.1 dB, which is lower than other designs based on Transfer Function 2.

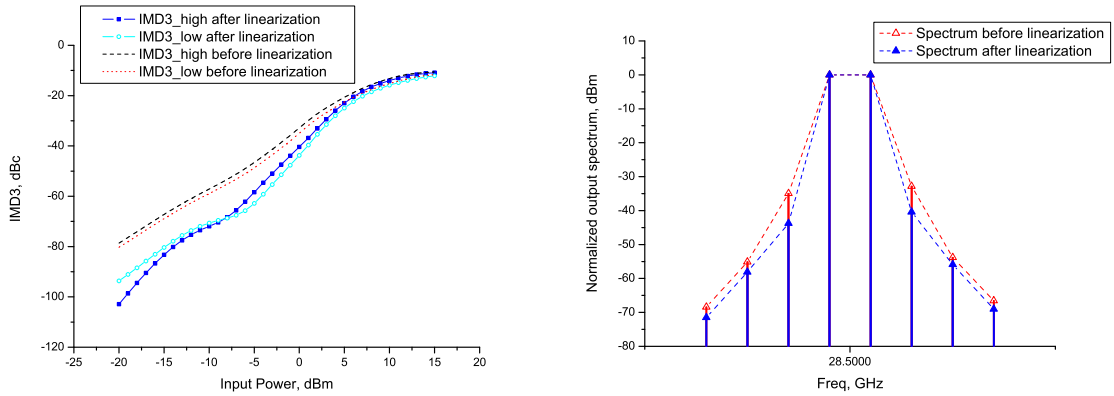
As in this case, the resistance decreases with increasing signal amplitude as in Figure 8.20 (b), the burden of insertion loss is not that heavy, and this will increase the normalized linearity improvement. Some major metrics are shown in Figure 8.37. Figure 8.37 (a) and Figure 8.37 (d) show the $IMD3$ and the normalized $IMD3$ improvement respectively. IMD characteristics and spectrum were simulated at the fundamental frequency of 28.5GHz and frequency spacing of 50 KHz. $IMD3$ after linearization reaches -40.41 dBc and -43.76 dBc at upper channel and lower channel respectively. And the



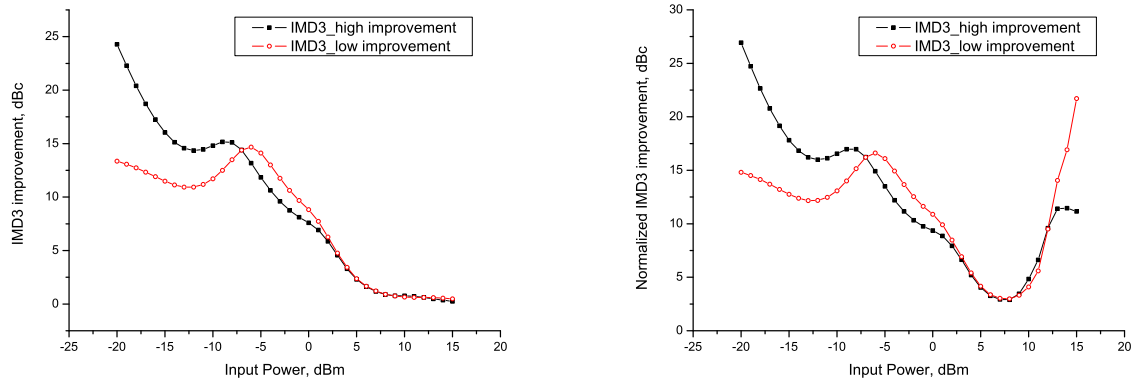
(a) Gain deviation characteristic (b) Phase deviation characteristic

Figure 8.36: Characteristics of the predistortion circuit

net $IMD3$ improvement without the contribution of power back-off is about 9.94 dB and 11.46 dB respectively when the input power is 0 dBm, which are much higher than other designs based on Transfer Function 2 in Figure 8.32.



(a) $IMD3$ comparison (b) Spectrum comparison



(c) $IMD3$ improvement comparison (d) Normalized $IMD3$ improvement comparison

Figure 8.37: Major linearity metrics comparisons

The results before and after linearization are listed in Table 8.7 and Table 8.8.

Table 8.7: Comparisons of performance for Circuit 5

Specifications	Before linearization	After linearization
$P_{out,1dB}$	18.37 dBm	18.75 dBm
Power Gain@P_{in}=0 dBm	15.00 dB	14.19 dB
PAE_{1dB}	17.73%	19.31%
PAE_{peak}	35.01%	34.85%
$IMD3$@P_{in}=0 dBm	$IMD3$_high: -32.82 dBc $IMD3$_low: -34.94 dBc	$IMD3$_high: -40.41 dBc $IMD3$_low: -43.76 dBc

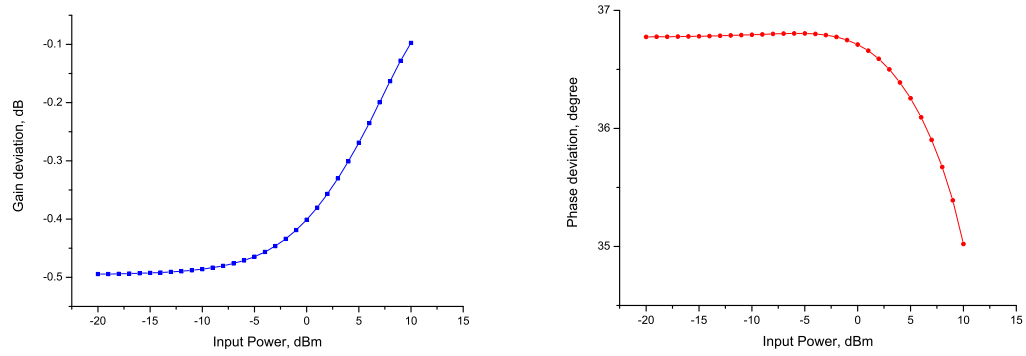
Table 8.8: Linearity improvement for Circuit 5

$IMD3$ improvement @P_{in}=0 dBm	$IMD3$_high: 7.60 dB $IMD3$_low: 8.83 dB
Normalized $IMD3$ improvement @P_{in}=0 dBm	$IMD3$_high: 9.37 dB $IMD3$_low: 10.89 dB
Net $IMD3$ improvement @P_{in}=0 dBm	$IMD3$_high: 9.94 dB $IMD3$_low: 11.46 dB

8.6.3.3 Performance Comparison for the Circuit 1 in Figure 8.33 (a)

Figure 8.33 (a) shows the first predistortion circuit based on Transfer Function 3. Similarly input capacitance of the power amplifier stage will be part of the predistortion circuit and play a role in the predistortion function. Because of resistance decreasing with increasing signal amplitude, the insertion loss is much lower than the circuits with the characteristic of resistance increasing with increasing signal amplitude. For this case, the insertion loss is less than -0.5 dB. Its characteristics can be adjusted by factor a and factor b through adjusting C_0 and C_1 as described in Equation (8.13) in Section 8.4.3. The gain and phase deviation characteristics are shown below in Figure 8.38.

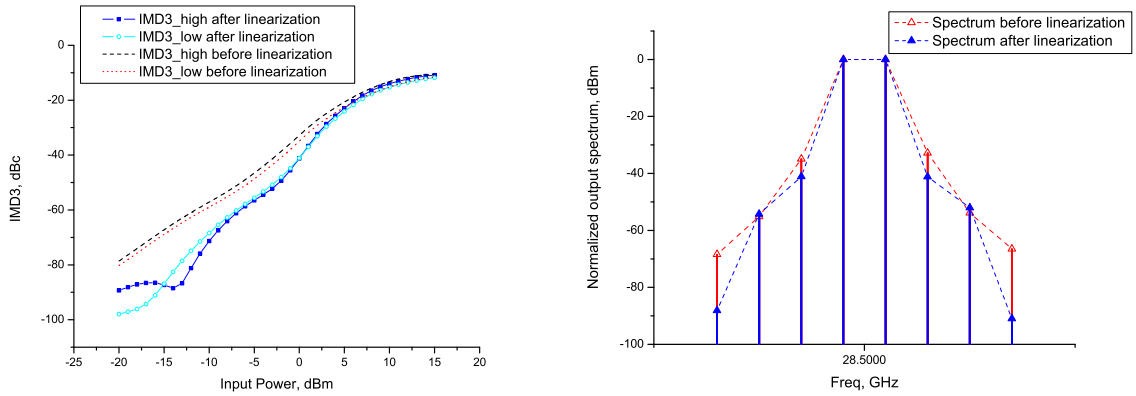
Some important linearity metrics are shown in Figure 8.39. Figure 8.39 (a) and Figure 8.39 (d) show the $IMD3$ and the normalized $IMD3$ improvement comparison char-



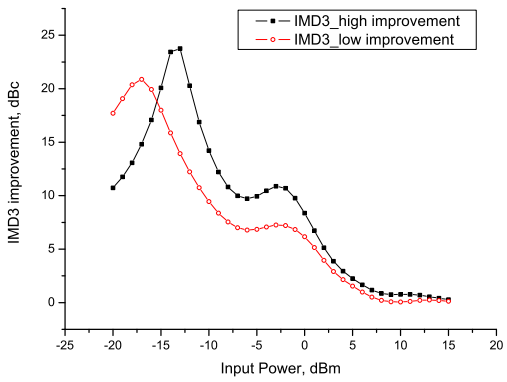
(a) Gain deviation characteristic (b) Phase deviation characteristic

Figure 8.38: Characteristics of the predistortion circuit

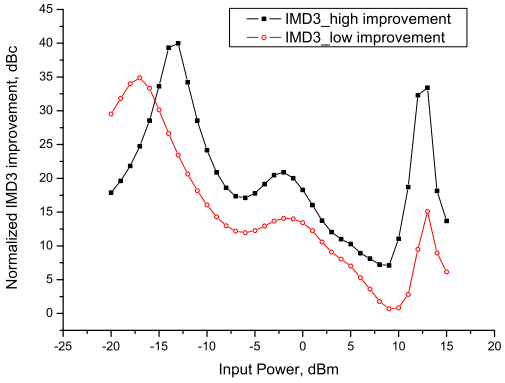
acteristics respectively. IMD characteristics and spectrum were simulated at the fundamental frequency of 28.5GHz and frequency spacing of 50 KHz. $IMD3$ after linearization reaches -41.19 dBc and -41.09 dBc at upper channel and lower channel respectively. The net $IMD3$ improvement without the contribution of power back-off is up to 19.91 dB and 15.06 dB respectively when the input power is 0 dBm, which are much higher than all other circuits designed.



(a) $IMD3$ comparison (b) Spectrum comparison



(c) $IMD3$ improvement comparison



(d) Normalized $IMD3$ improvement comparison

Figure 8.39: Major linearity metrics comparisons

The results before and after linearization are listed in Table 8.9 and Table 8.10.

Table 8.9: Comparisons of performance for Circuit 1

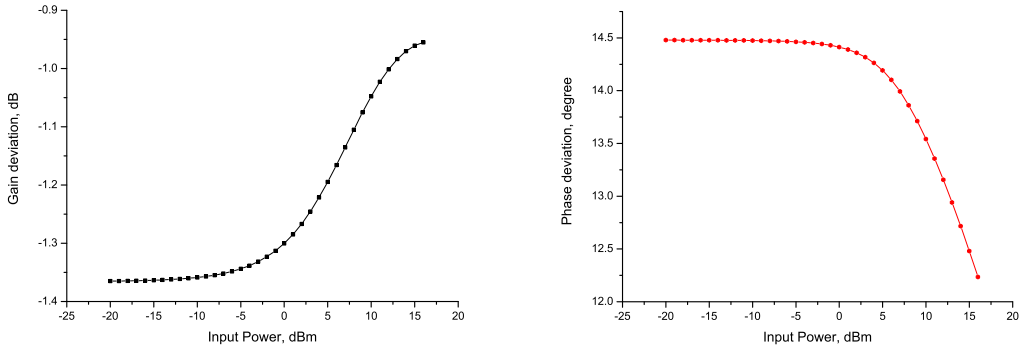
Specifications	Before linearization	After linearization
$P_{out,1dB}$	18.37 dBm	19.08 dBm
Power Gain@P_{in}=0 dBm	15.00 dB	14.55 dB
PAE_{1dB}	17.73%	20.92%
PAE_{peak}	35.01%	35.12%
$IMD3$@P_{in}=0 dBm	$IMD3$_high: -32.82 dBc $IMD3$_low: -34.94 dBc	$IMD3$_high: -41.19 dBc $IMD3$_low: -41.09 dBc

Table 8.10: Linearity improvement for Circuit 1

$IMD3$ improvement @P_{in}=0 dBm	$IMD3$_high: 8.38 dB $IMD3$_low: 6.16 dB
Normalized $IMD3$ improvement @P_{in}=0 dBm	$IMD3$_high: 18.29 dB $IMD3$_low: 13.44 dB
Net $IMD3$ improvement @P_{in}=0 dBm	$IMD3$_high: 19.91 dB $IMD3$_low: 15.06 dB

8.6.3.4 Performance Comparison for the Circuit 2 in Figure 8.33 (b)

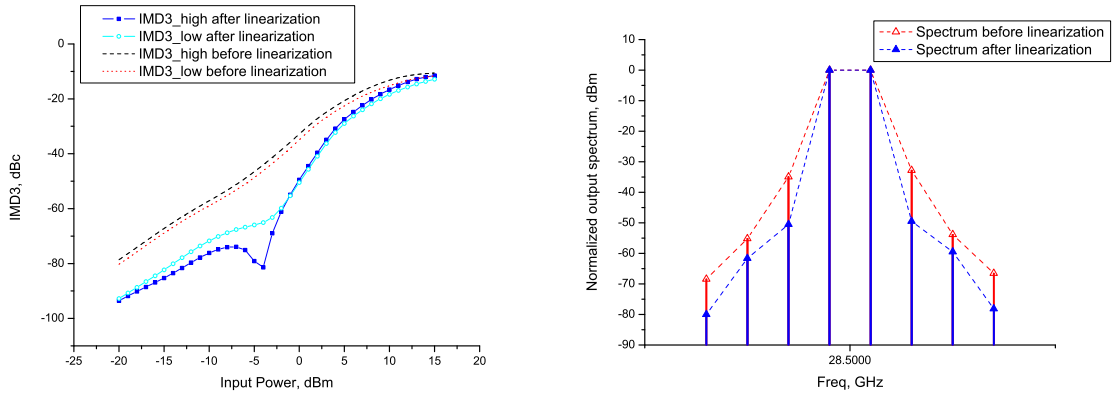
The predistortion circuit in Figure 8.33 (b) is another implementation for Transfer Function 3. Because this circuit has the characteristic of resistance decreasing with increasing signal amplitude, the insertion loss is low. Its characteristics can be adjusted by factor a and factor b through adjusting C_0 and C_1 as described in Equation (8.13) in Section 8.13. The gain and phase deviation characteristics are shown in Figure 8.40.



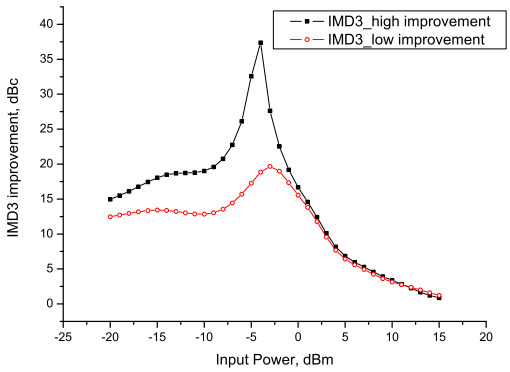
(a) Gain deviation characteristic (b) Phase deviation characteristic

Figure 8.40: Characteristics of the predistortion circuit

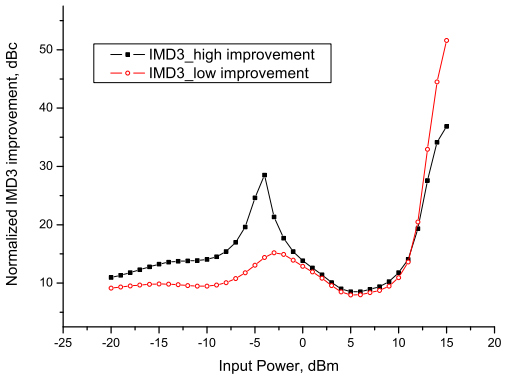
The major linearity metrics are shown in Figure 8.41. Figure 8.41 (a) and Figure 8.41 (d) show the $IMD3$ and the normalized $IMD3$ improvement respectively. IMD characteristics and spectrum were simulated at the fundamental frequency of 28.5GHz and frequency spacing of 50 KHz. $IMD3$ after linearization reaches -49.51 dBc and -50.49 dBc at upper channel and lower channel respectively. The net $IMD3$ improvement without the contribution of power back-off is up to 13.20 dB and 12.26 dB respectively when the input power is 0 dBm.



(a) $IMD3$ comparison (b) Spectrum comparison



(c) $IMD3$ improvement comparison



(d) Normalized $IMD3$ improvement comparison

Figure 8.41: Major linearity metrics comparisons

The results before and after linearization are listed in Table 8.11 and Table 8.12.

Table 8.11: Comparisons of performance for Circuit 2

Specifications	Before linearization	After linearization
$P_{out,1dB}$	18.37 dBm	18.87 dBm
Power Gain@P_{in}=0 dBm	15.00 dB	13.80 dB
PAE_{1dB}	17.73%	19.68%
PAE_{peak}	35.01%	33.87%
$IMD3$@P_{in}=0 dBm	$IMD3$_high: -32.82 dBc $IMD3$_low: -34.94 dBc	$IMD3$_high: -49.51 dBc $IMD3$_low: -50.49 dBc

Table 8.12: Linearity improvement for Circuit 2

$IMD3$ improvement @P_{in}=0 dBm	$IMD3$_high: 16.70 dB $IMD3$_low: 15.56 dB
Normalized $IMD3$ improvement @P_{in}=0 dBm	$IMD3$_high: 13.83 dB $IMD3$_low: 12.89 dB
Net $IMD3$ improvement @P_{in}=0 dBm	$IMD3$_high: 13.20 dB $IMD3$_low: 12.26 dB

8.7 Comparisons and Discussions

In the sections above, three transfer functions, two general non-linear resistor I-V curves with different nonlinear characteristics and several predistortion circuits were proposed. With different configurations, different levels of linearity improvement were achieved. In order to obtain optimum linearity improvement, it is necessary to compare the related circuits to find the latent rule in the circuit configuration design, which can be used as a guideline for circuit selection and for future work.

8.7.1 Further Analysis for Transfer Function 1

In this chapter, four circuit implementations have been proposed to replace the nonlinear resistor in Figure 8.9 in Section 8.4.1 and different levels of linearity improvement were achieved. The detailed circuit configurations have been shown in Figure 8.31.

As the predistortion circuits are based on the same transfer function, it is necessary to compare these circuits with different configurations to serve as a guideline for predistortion circuit design. The performance and related $IMD3$ improvement metrics are listed in Table 8.13 in detail.

Table 8.13: Comparisons of performance for Transfer Function 1

Specifications	Circuit A	Circuit B	Circuit C	Circuit D
Factor a	0.15	0.12	0.11	0.11
Factor b	0.5	0.5	0.5	0.5
R_{DS}	296 Ohm	48.6 Ohm	47.5 Ohm	33.8 Ohm
$IMD3$	$IMD3$_high: -39.86 dBc	$IMD3$_high: -39.35 dBc	$IMD3$_high: -40.26 dBc	$IMD3$_high: -40.63 dBc
@P_{in}=0 dBm	$IMD3$_low: -41.90 dBc	$IMD3$_low: -42.30 dBc	$IMD3$_low: -42.33 dBc	$IMD3$_low: -42.71 dBc
$IMD3$ improvement	$IMD3$_high: 7.04 dB	$IMD3$_high: 6.53 dB	$IMD3$_high: 7.45 dB	$IMD3$_high: 7.81 dB
@P_{in}=0 dBm	$IMD3$_low: 6.96 dB	$IMD3$_low: 7.36 dB	$IMD3$_low: 7.39 dB	$IMD3$_low: 7.78 dB
Normalized $IMD3$	$IMD3$_high: 5.91 dB	$IMD3$_high: 7.48 dB	$IMD3$_high: 5.15 dB	$IMD3$_high: 5.79 dB
improvement@P_{in}=0 dBm	$IMD3$_low: 5.84 dB	$IMD3$_low: 8.43 dB	$IMD3$_low: 5.10 dB	$IMD3$_low: 5.76 dB
Net $IMD3$ improvement	$IMD3$_high: 5.34 dB	$IMD3$_high: 7.87 dB	$IMD3$_high: 3.83 dB	$IMD3$_high: 4.74 dB
@P_{in}=0 dBm	$IMD3$_low: 5.27 dB	$IMD3$_low: 8.82 dB	$IMD3$_low: 3.78 dB	$IMD3$_low: 4.71 dB

Among the circuits, Circuit 2 has the highest net linearity improvement, and next comes Circuit 1. Circuit 4 ranks the third and Circuit 3 has the lowest linearity improvement. According to Transfer Function 1, predistortion characteristic is decided by factor a and factor b through adjusting C_0 and C_1 as shown in Equation (8.7) in Section 8.4.1 and R_{DS}, as the X axis shown in Figure 8.11 also plays a role in predistortion function.

As shown in Table 8.13, since all the factor b are the same, the different levels of predistortion improvement can be explained through the effect of factor a and R_{DS} as shown in Figure 8.11 in Section 8.4.1. Among the circuits, Circuit 1 and Circuit 2 has the highest factor a, which means these circuits can provide relatively larger inverse compensation, thus Circuit 1 and Circuit 2 have the highest linearity improvement. As the R_{DS} of Circuit 2 is much smaller than that of Circuit 1 while the two a are quite close, the predistortion bias decides that Circuit 2 has a higher linearity improvement as shown in Figure 8.11. For Circuit 3 and Circuit 4, since their factor a and factor b are same, thus R_{DS} will decide which is more effective. As the R_{DS} of Circuit 4 is smaller than that of Circuit 3, the linearity improvement brought by Circuit 4 is higher than that of Circuit 3.

From the analysis above, we can see how factor a and factor b, together with R_{DS} affect the linearity improvement, which can serve as a guideline for the predistorter design.

8.7.2 Further Analysis for Transfer Function 2

Five circuit configurations were applied to Transfer Function 2 in Section 8.5 as shown in Figure 8.32, among which Circuit A $\sim$ Circuit D are based on the nonlinear I-V characteristic in Figure 8.20 (a). In this section, we primarily analyze these four circuits which are based on the nonlinear characteristic in Figure 8.20 (a). From Transfer Function 2, we can see that the predistortion function is mainly affected by factor a in Equation (8.9) and in the practical application, the nonlinear resistance characteristic in Figure 8.14 also affects the linearity improvement. For the four circuits, their comparisons are shown in Table 8.14. From net $IMD3$ improvement, Circuit 2 has the highest improvement, and next comes Circuit 3. Circuit 1 has the lowest improvement and Circuit 4 is the next to the last.

Table 8.14: Comparisons of performance for Transfer Function 2

Specifications	Circuit A	Circuit B	Circuit C	Circuit D
Factor a	10	10	10	10
R_0 at the bias point	353 Ohm	0 Ohm	260 Ohm	1615 Ohm
$IMD3$	$IMD3$_high: -40.46 dBc	$IMD3$_high: -40.83 dBc	$IMD3$_high: -42.50 dBc	$IMD3$_high: -40.39 dBc
@P_{in}=0 dBm	$IMD3$_low: -42.58 dBc	$IMD3$_low: -43.84 dBc	$IMD3$_low: -42.33 dBc	$IMD3$_low: -42.45 dBc
$IMD3$ improvement	$IMD3$_high: 7.65 dB	$IMD3$_high: 8.02 dB	$IMD3$_high: 9.68 dB	$IMD3$_high: 7.57 dB
@P_{in}=0 dBm	$IMD3$_low: 7.65 dB	$IMD3$_low: 8.91 dB	$IMD3$_low: 9.14 dB	$IMD3$_low: 7.51 dB
Normalized $IMD3$	$IMD3$_high: 5.43 dB	$IMD3$_high: 7.25 dB	$IMD3$_high: 6.90 dB	$IMD3$_high: 5.67 dB
improvement@P_{in}=0 dBm	$IMD3$_low: 5.43 dB	$IMD3$_low: 8.06 dB	$IMD3$_low: 6.52 dB	$IMD3$_low: 5.63 dB
Net $IMD3$ improvement	$IMD3$_high: 4.20 dB	$IMD3$_high: 6.92 dB	$IMD3$_high: 5.70 dB	$IMD3$_high: 4.68 dB
@P_{in}=0 dBm	$IMD3$_low: 4.20 dB	$IMD3$_low: 7.73 dB	$IMD3$_low: 5.32 dB	$IMD3$_low: 4.64 dB

As all the factor a happen to be same for this application, the predistortion performance is primarily decided by the resistance R_0. From Figure 8.14 (a), we can see that the smaller the resistance is, the larger the predistortion amplitude is. While in Figure 8.14 (b), the phase change increases first with increasing the resistance and decreases after it reaches the peak. Thus the impact of the phase change is not as consistent with increasing the resistance as the gain change.

For this case, as Circuit 2 has the smallest resistance, which means it predistortion effect is biased at the position with relatively large inverse compensation as shown in Figure 8.14, thus it has the highest linearity improvement. Circuit 3 ranks the second also because of this reason. As the resistance of Circuit 4 is much larger than rest of all, its phase distortion will fall in the right side of the peak in Figure 8.14 (b), thus its linearity improvement is higher than that of Circuit 1.

On the other hand, according to Figure 8.5, the larger factor a is, the higher the predistortion effect is while the insertion loss may be larger. That is, a trade-off must be taken into consideration if we adjust the predistortion function via factor a.

From the analysis, we can see how factor a and R_0 affect the linearity improvement, which can be a guideline for predistortion circuit design in the future work.

8.7.3 Further Analysis for Transfer Function 3

In Section 8.5.2, two topologies were proposed to implement Transfer Function 3. One is with single FET configuration, named Circuit E, the other is with two FET in parallel configuration, named Circuit F, which are shown in Figure 8.33. The comparisons in this section will be carried out between these two circuits.

According to Transfer Function 3 in Section 8.5.2, the predistortion magnitude is mainly decided by factor a and factor b and partly affected by nonlinear R as shown in Figure 8.19. For Transfer Function 3, the higher factor a and factor b are, the larger the linearity improvement is. And the higher the resistance R is, the larger the linearity improvement is, As in this application, factor a and factor b are the same for the two configurations, the performance improvement is primarily affected by the resistance R. The performance comparison is listed in Table 8.15.

Table 8.15: Comparisons of performance for Transfer Function 3

Specifications	Circuit E	Circuit F
R	13.5 Ohm	6.4 Ohm
Gain Degeneration@P_{in}=0 dBm	-0.46 dB	-1.21 dB
$IMD3$ improvement @P_{in}=0 dBm	$IMD3$_high: 8.38 dB $IMD3$_low: 6.16 dB	$IMD3$_high: 16.70 dB $IMD3$_low: 15.56 dB
Normalized $IMD3$ improvement @P_{in}=0 dBm	$IMD3$_high: 18.29 dB $IMD3$_low: 13.44 dB	$IMD3$_high: 13.83 dB $IMD3$_low: 12.89 dB
Net $IMD3$ improvement @P_{in}=0 dBm	$IMD3$_high: 19.91 dB $IMD3$_low: 15.06 dB	$IMD3$_high: 13.20 dB $IMD3$_low: 12.26 dB

From the comparison in Table 8.15, we can see that

1. The net linearity improvement is related to the gain degeneration. The smaller gain degeneration, the less effect from power back-off, and the higher the normalized $IMD3$ improvement.

2. The linearity improvement is related to the effective R, which corresponds to X axis in the transfer curves in Figure 8.19. As dB(H) decreases with increasing R, so the higher the R is, the higher the linearity improvement is. As the R of Circuit 1 is larger than that of Circuit 2, thus the linearity improvement of Circuit 1 is correspondingly higher.

8.7.4 Comparison Between the Transfer Functions

In this chapter, three transfer functions were proposed for passive RC network predistortion circuit design and different levels of performance improvement were achieved.

For the the nonlinear characteristic 2 in Figure 8.20 (b), the I-V curve tends to reduce V_R towards zero when $\hat{V}_1$ increases, thus counteracting the nonlinear effect and correspondingly the effective resistance decreases with the signal amplitude increasing. According to normalized $IMD3$ improvement and net $IMD3$ improvement definitions in Equation (8.16) and Equation (8.17), smaller insertion loss with the same gross improvement will bring higher normalized improvement. As normalized $IMD3$ improvement and

net $IMD3$ improvement as the main metrics were employed in evaluation, the circuits derived from the nonlinear characteristic 2 in Figure 8.20 (b) have a much higher net linearity improvement than those derived from the nonlinear characteristic 1 in Figure 8.20 (a). As the circuits derived from the nonlinear characteristic 2 in Figure 8.20 (b) have a smaller insertion loss than their counterparts derived from the nonlinear characteristic 1 in Figure 8.20 (a), their contributions to linearity improvement are more effective. At the same time, as the insertion loss is lighter, other metrics are affected less.

Among the performance improvements from Transfer Function 1, Transfer Function 2 and Transfer Function 3, we can see from Table 8.15 that Transfer Function 3 has the highest performance improvement, which benefits from the nonlinear characteristic employed as discussed. As when factor a is zero, Transfer Function 2 cannot provide necessary distortion to realize predistortion function while the distortion in Transfer Function 1 can still play a role, Transfer Function 1 can be more effective than Transfer Function 2 under the same conditions.

8.8 Summary

In this chapter, an original predistortion circuit design methodology based on frequency to signal amplitude transformation was demonstrated. Three transfer functions were proposed and discussed systemically. Related circuit implementations were designed to realize the predistortion circuits and further linearize the millimeter-wave power amplifier designed. The performance improvements show that this methodology can effectively improve the linearity while other metrics are affected only slightly. With the comparison, the factors that affect the predistortion were clarified, which will be a guideline for the predistortion circuit design in the future. Part of the work concerning with Transfer Function 1 has been published at European Conference on Circuit Theory and Design 2007 [26].

Chapter 9

CONCLUSIONS AND FURTHER WORK

9.1 Conclusions

In this thesis, the predistortion technique has been proven to be an effective and cost-saving solution for linearity improvement for millimeter-wave power amplifier. The advantages of low complexity and low cost make it very attractive among the available linearization techniques.

After the literature review of wide-band amplifier design techniques and MMIC enabling technologies, a wide-band millimeter-wave power amplifier for LMDS applications was designed to a high engineering standard with OMMIC 0.25 μm pHEMT technology as the test bench for predistortion circuit research. Through this part of work, essential design data and experience required for the following stage of research were accumulated.

After reviewing and evaluating some existing predistortion circuits, their limitations, such as relatively large insertion loss and ineffective linearity improvement were revealed. The solutions of these problems were the key issue during the research. Several novel predistortion circuit structures were proposed and evaluated using the test bench PA.

Firstly a predistortion circuit based on an amplifier with a fixed constant bias circuit was proposed. The linearity improvement for the predistortion circuit based on an amplifier with a fixed bias circuit is about 11.83 dB and 7.26 dB in term of $IMD3$ in the

upper and lower channel respectively.

Another predistortion circuit based on an amplifier with a nonlinear signal dependent bias circuit was then proposed. As its bias can be adjusted automatically according to the input power, its linearized range is much wider. The $IMD3$ improvement brought by the predistortion circuit based on an amplifier with the nonlinear signal dependent bias circuit can reach 35.55 dB and 32.94 dB in the upper and lower channel respectively. As these structures are based on an amplifier, they can improve other metrics at the same time that they improve the linearity significantly.

A novel predistortion circuit design methodology derived from frequency to signal amplitude transformation on a passive circuit was then proposed. Three transfer functions were proposed based on this approach and related transformations and circuit implementations were designed to realize the predistortion function and further linearize the millimeter-wave power amplifier test bench. The highest linearity improvement can reach 19.91 dB and 15.06 dB in term of net $IMD3$ improvement and other metrics are affected only slightly.

These design methodologies provide a new approach for linearity improvement for millimeter-wave power amplifier and have a broad prospect for application.

9.2 Further Work

Research on linearity improvement by means of predistortion technique for millimeter-wave power amplifiers is an ever-evolving area of research and as a result the work in this thesis could be continued and extended in a variety of directions.

Firstly, improvement on the existing structures such as the predistortion circuit built on amplifier, especially on amplifier with a nonlinear signal dependent bias circuit can be further investigated. With exploration of novel forms of bias circuit, this approach may improve the linearity more effectively.

Secondly, as the gain of the predistortion circuit built on amplifier can be positive, it may be placed between stages to realize a much stronger predistortion characteristic, or even replace an existing gain stage, which would be quite different from the conventional predistortion structure. The exploration of this configuration will provide a new approach

to adjust the predistortion characteristic and the results can be used as a guideline for the future predistortion circuit design.

Thirdly, further exploration of the existing design approach such as the predistortion circuit design methodology by frequency to signal amplitude transformation can be carried out for further improved performance. The same principle in alternative circuits may be embodied. The knowledge about RC circuit synthesis can be used to tailor the gain and phase characteristics of the RC circuit more precisely. Also the design of the nonlinear conductance can be optimized to yield the most effective characteristic.

Last but not least, chip fabrication and measurement can be carried out after theoretical research. After a series of research work, engineering work including chip fabrication and measurement can be carried out to verify the simulation results. Through the verification from the measurement, defect during the design can be revealed and the design can be improved.

In conclusion, linearity improvement by means of the predistortion technique for millimeter-wave power amplifiers is an active area of research providing many opportunities for novel research. Whilst this thesis has examined many issues related to predistortion circuit built on amplifier and predistortion circuit design methodology by frequency to signal amplitude transformation of a passive network, we have shown that there are still many interesting issues that necessitate further research.

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