A 5s-Time-Constant Temperature-Stable Integrator for a Tuneable PID Controller in LOC Applications

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***Abstract*—In this paper, we present a novel, ultra-long-time-constant analogue integrator for a PID controller in Lab-on-Chip (LOC) applications. A time constant of up to 5 seconds is achievable using a capacitance of only 18pF by exploiting transconductance reduction techniques involving current splitting and gm-attenuated OTA. Additionally, this architecture provides the ability to digitally tune the time constant from 200ms to 5s with 4-bit programmability. The design achieves a temperature dependance of 1.2% over the range from 0°C to 100°C with micropower consumption.**

I. Introduction

Emerging Lab-on-Chip (LOC) platforms targeting biomedical applications [1], [2], leverage on the semiconductor economies of scale to achieve large scale integration. In such systems, it is highly desirable to monolithically integrate sensors, actuators and electronics to achieve low power, robust operation over an extended (often variable) temperature range. In the majority of such applications, for example in Polymerase Chain Reaction (PCR), it is essential to regulate the temperature with precision. This is typically achieved using a PID controller, which is most commonly implemented in software (i.e. on a microprocessor) or using dedicated digital logic. Such techniques however are often power hungry, require a relatively large silicon area and also suffer from noise injection due to clock signals [3]. On the other hand, implementing PID controllers using analogue circuits achieve limited time constants, due to prohibitively large area requirements for passive components (i.e. capacitors).

To overcome these limitations in discrete component values, Gm-C based integrators are typically used to realise large time constant integrators [4], [5]. Since the capacitance is limited by the available silicon area, a number of different techniques have been proposed to achieve a small transconductance. These include, using floating gate structures [6], scaled (low ratio) current mirrors [7], G_m-G_m^{-1} chains [8] and current division [9]. Although transconductances of under 10nA/V have been successfully achieved, no emphasis has been given to the temperature stability of such circuits. Specifically, if a LOC system is to be fully-integrated, the controller will be at the same temperature as the test solution and therefore will vary. Furthermore, the performance of such topologies is often constrained by device mismatch, limiting the dynamic range; which is essential for any temperature control system. In such systems, instead of directly tuning the transconductances, the output currents can be substantially attenuated by using current splitting techniques [9]. By sub-dividing the output current through a tree of well-matched current splitters, very small transconductances can be achieved, crucially being immune to temperature variation.

In this paper, we present a novel transconductor architecture by applying current division at the output to achieve a large time constant. By incorporating a current splitting technique together with temperature compensation, a tuneable time constant of up to 5s is achievable. This paper is organised as follows: Section II describes the top level architecture, Section III details the circuit implementation, Section IV presents the simulated results and finally Section V summarises the work presented.

II. System Design

The top level architecture of the proposed integrator is shown in Figure 1. In order to realise a small G_m with large tuneable range, we propose a two stage transconductance reduction structure by combining a low-G_m OTA with tuneable current splitting. In the first stage, a very low transconductance OTA with large linear region is required incorporating a master-slave configuration to compensate for temperature variation [10]. This feeds the second stage which consists of a current splitting network to further reduce the transconductance. Since the MOSFETs used to split the current operate as resistors, they can be controlled digitally via their gates inputs [9] and furthermore the configuration is intrinsically immune

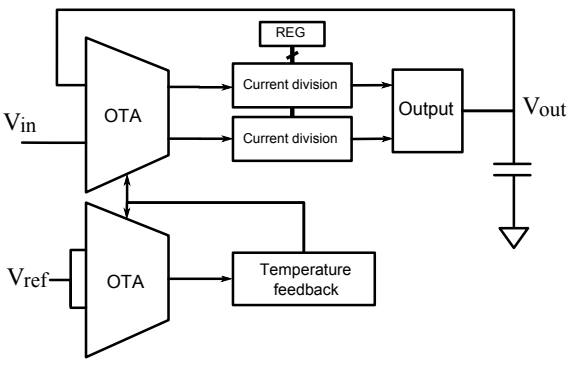


Fig. 1. Block diagram of the Proposed integrator

to temperature variation. Finally, the output stage needs to have a large output impedance to avoid degrading the achieved transconductance.

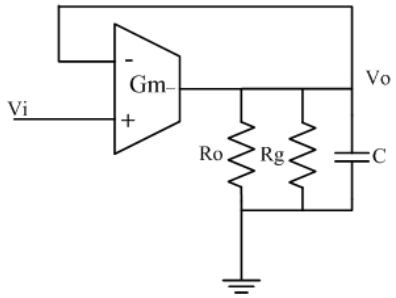


Fig. 2. Skeleton diagram of Gm-C integrator with a negative feedback

The simplified structure of the G_m-C-based integrator is shown in Figure 2, where R_o represents the output impedance and R_g the gate resistance of the OTA. A low time constant can be achieve using an open-loop configuration, however, with a limited dynamic range. Therefore this design applies negative feedback to boost the dynamic range. The transfer function of this system is given by:

$$H(s) = \frac{V_o}{V_i} = \frac{g_m/c}{s + (g_g + g_o + g_m)/c} \tag{1}$$

with the time constant of the integrator being:

$$\tau = \frac{c}{g_g + g_o + g_m} \tag{2}$$

Rather than increasing the output impedance in conventional open loop configuration, the time constant can be enhanced by g_m. To achieve a 1% error, the output and input impedances of the OTA must be at least two orders of magnitude higher than G_m^{-1}. By using regulated current mirrors, a R_o of $10^{18}\Omega$ can be achieved with the R_g being $10^{13}\Omega$ or above for a normal MOSFET [11]. Therefore, an effective transconductance of 5pA/V would achieve a good overall trade-off. In order to achieve this considering implementation issues, we've set a target transconductance of 5nA/V for the OTA and by using subsequent current splitting, the target value can be achieved whilst also providing programmability.

III. Circuit Implementation

A. 1st Stage: OTA

In order to realise a low G_m whilst maintaining temperature stability, we have combined several transconductance reduction techniques including: (1) Using a bulk input, (2) source degeneration, (3) gate degeneration and (4) bump linearisation for the OTA [12]. The circuit schematic for the OTA is shown in Figure 3. In order to limit the transconductance distortion induced by DC mismatch at high temperatures, a cross-coupled bump structure is adopted. A voltage level shifter has also been included in the design to balance the input DC level for this OTA and thus achieve a good dynamic range for a 3.3V supply [12]. The target specification of this OTA is given in Table I. Finally, a master-slave configuration is used to compensate for temperature variation over the range of 0° C to 100° C, by using a second, identical OTA to provide a common mode feedback to V_{ctrl}.

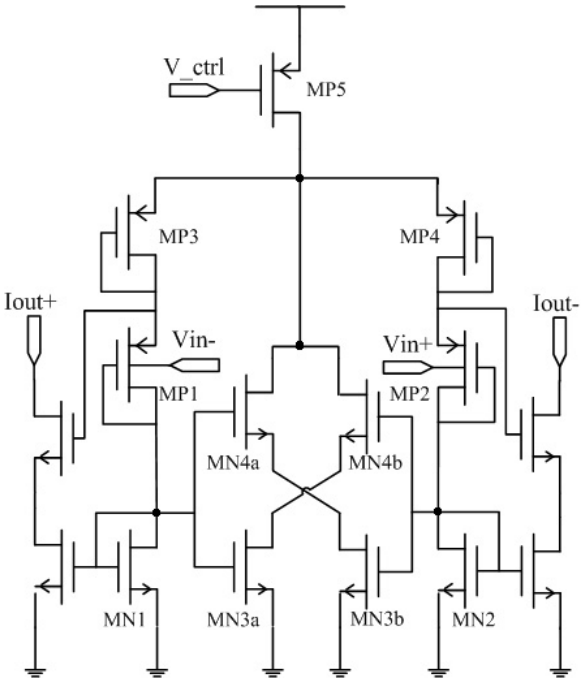


Fig. 3. Circuit schematic of the OTA

TABLE I
Specification of OTA

Parameter	0^oC	100^oC
Linear region	1.32V(V_{pp})	1.42V(V_{pp})
Power Consumption	1.44μW	2.73μW
Max. Temp. deviation	0.83% (at $\pm 300mV$)	
Bandwidth (3dB)	470kHz	430kHz
Integrated Noise	0.25mV	3.2mV

B. 2nd Stage: Current Division

The output current of the 1st stage (OTA) is fed into the 2nd stage (current splitter) via current mirrors, shown in Figure 4. Within each branch, transistors T_1 to T_6 compose a R-2R ladder that split the current by a certain ratio. These current splitters are cascaded to prove up to 60dB attenuation (from 5nA/V to 5pA/V) required to achieve the effective transconductance. However, in order to provide large attenuation, in addition to tuneability, two types of attenuation blocks have been designed: (1) 3dB attenuaters for large current ranges and (2) 2dB attenueters to provide tuneability with a 4-bit range. Moreover, the current that is discarded during the splitting can be recycled by being rewired such that to achieve custom attenuation factors or to bypass a division stage for block termination.

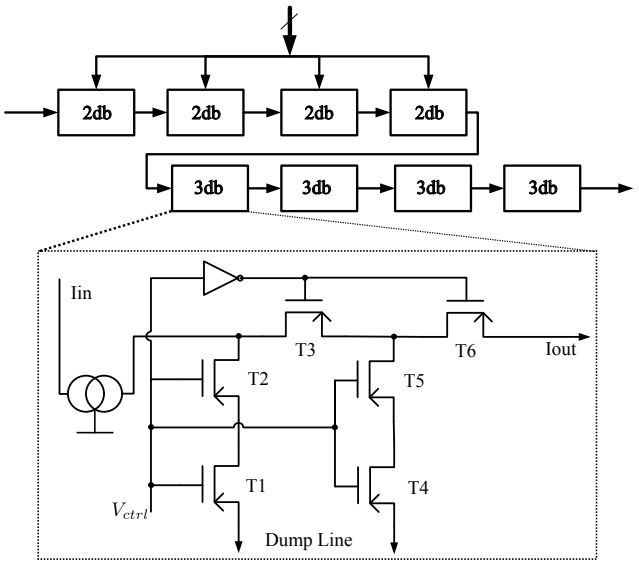


Fig. 4. Circuit schematic of the 2dB division block

A second reason to having separate division and attenuation blocks is to minimise any current offset caused by source voltage mismatch in the discarded or output branches. However, this mismatch is limited by the systematic DC offset observed in CMOS op-amps, which for conventional OTA is around 20mV. Therefore, in order to achieve a 1% attenuation distortion, the total number of R-2R branches in the stage are limited to 8. To further reduce this current offset into the sub-nano region, the bias voltage V_{gs} for each R-2R network has to be reduced providing a minimal drain source resistance.

In the high temperature region (larger than 70^{o}C), the bulk leakage current dominates the offset, significantly increasing the offset. A bulk current compensation circuit is therefore required to counterbalance this leakage. Differential current splitting structures are also implemented to further reduce the common mode offset in the differential output of the OTA. The entire current division block contains 4 stages of the 2dB blocks with 15 tuneable levels from 1 to 22.5, and 4 stages of the 3dB block achieving a fixed attenuation of 64, equivalent to 36dB. The design parameters are given in Table II for an input current of 14.55nA. The errors stated are the differences between the realistic (based on simulation) and ideal division values. The *Temp. Deviation* gives the change in value for the region from 0^{o}C to 100^{o}C, which can be found lower than 1.2%.

C. Output stage

The output stage is needed to boost the output impedance such as to minimise any pole distortion, since this impedance appears in parallel with the transconductance. To achieve this a regulated-cascode-based current mirror is adopted to provide an output impedance of over $10^{12}\Omega$. Simulation results indicate that an output impedance of approximately $10^{18}\Omega$ is achievable for a sub-nA bias current.

TABLE III
TARGET DESIGN SPECIFICATIONS FOR THE INTEGRATOR

Technology	Austriamicrosystems 0.35μm 2P3M CMOS
Load capacitor	18pF
Linear region	1.32V(V_{pp}@0^oC)
Core Power Consumption	5.7μW @100^oC
Temp. deviation	1.2%
Tuneable Bandwidth	31.8mHz - 724.1mHz

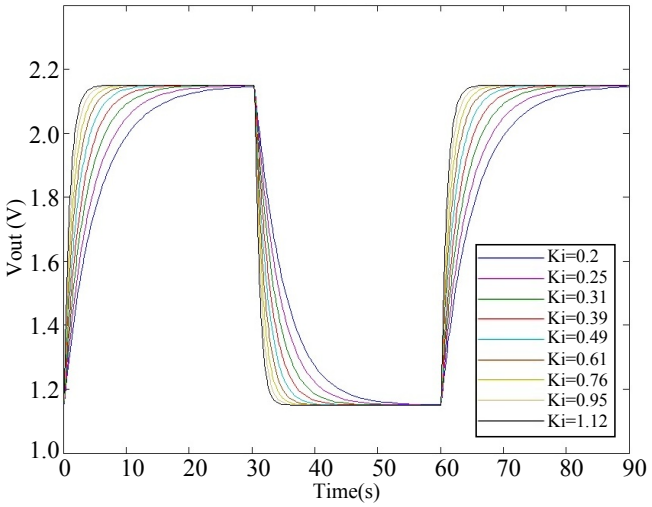


Fig. 5. Step response with integration parameters ranging from $0.2s^{-1}$ to $1.2s^{-1}$

IV. Simulated Results

This system has been implemented in Austriamicrosystems 0.35μm CMOS technology. The target specifications are given in Table III. The core power consumption includes the OTA, current division network and output stage.

1) Tuneble dynamic range: Figure 5 shows transient simulation results for a step response with 9 different integration parameters from $0.2s^{-1}$ to $1.2s^{-1}$, equivalent to time constants of $5s$ and $0.83s$ respectively. Comparing the results of the circuit simulation to the expected, i.e. ideal integrator (see Figure 6), illustrates that the distortion is below 1.2% even at the maximum time constant of $5s$.

2) Varying temperature: The step responses at different temperatures (between 0°C and 100°C) are shown in Figure 7. It can be observed that the response is consistent within this temperature range, with a deviation of under 1% for the entire tuning range.

3) Device mismatch: The sensitivity to device mismatch is illustrated in Figure 8 showing a Monte-Carlo analysis for a preset time constant of five seconds (at 300K).

V. Conclusion

In this paper, we have reported the design of a novel analogue integrator that achieves a long time constant based on splitting the output current of an OTA. Using an OTA with

TABLE II
PARAMETERS OF DIVISION BLOCK

Division figure	**64**	**100**	**125**	**195.31**	**244.14**	**305.18**	**381.47**	**476.84**	**596.05**	**745.06**	**931.32**	**1164.15**	**1455.19**
attenuated current	113.8p	72.9p	58.9p	37.42p	29.94p	23.94p	19.16p	15.34p	12.28p	9.83p	7.86p	6.29p	5.03p
Error	0.13%	0.27%	0.43%	0.47%	0.20%	0.40%	0.47%	0.51%	0.66%	0.67%	0.70%	0.64%	0.60%
Temp. Deviation	0.86%	0.49%	0.52%	0.60%	0.50%	0.53%	0.23%	0.28%	0.32%	0.36%	0.39%	0.55%	0.63%

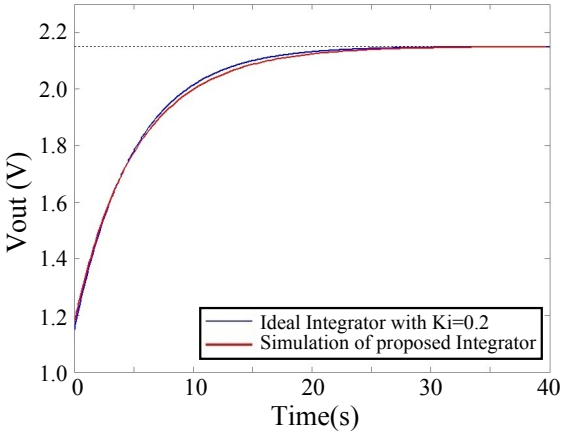


Fig. 6. Comparison of ideal and simulated responses for an integration parameter of K_i=0.2s^{-1}

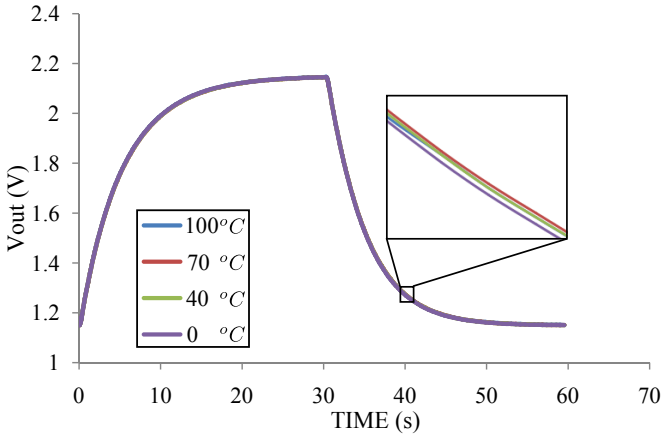


Fig. 7. Step response at 11 different temperatures

transconductance of 5nA/V, this is further attenuated by using a current division technique, down to 5pA/V. Thus, a long time constant can be achieved without the need for additional silicon area, by using this highly attenuated transconductance. A variety of different compensation techniques have been applied to minimise the offset of both the OTA and current splitting. Moreover, errors introduced by temperature variation have been reduced by use of master-slave configurations and differential structures. This makes the circuit ideal for application in Lab-on-Chip systems with integrated heating or cooling. Although, tuning parameters are digitally programmed, the signal path is fully analogue and can therefore be directly applied to front-end low pass filters requiring extremely low cut-off frequency and high noise performance.

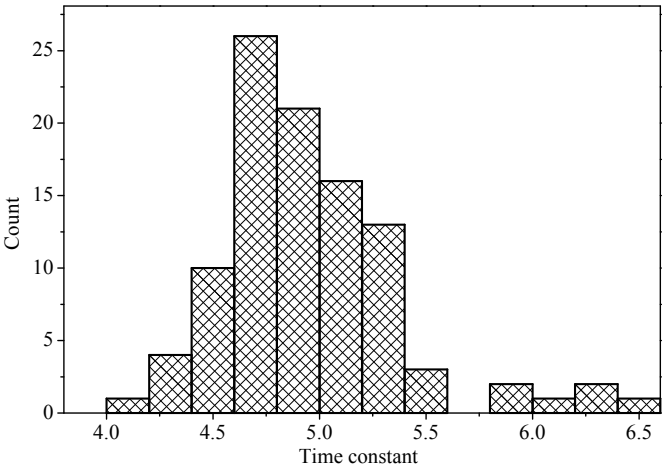


Fig. 8. Monte-Carlo Analysis

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