Floating Gate ISFET Chemical Inverters: for Semiconductor Based Biomedical Applications

by

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Abstract

Ion sensitive field effect transistors (ISFETs) have long been used as analogue chemical sensors particularly for biomedical applications. However, there are some applications where a "yes"/"no" type answer regarding pH change is sufficient. For example, in DNA sequencing the question is whether a chain extension reaction took place or not. Detecting this at the sensing point reduces the sensing process to pH change threshold detection. It eliminates the need for analogue to digital conversion and facilitates an all digital sensory system.

This thesis presents Novel Floating Gate ISFET based Chemical Inverters that were created with semiconductor based biomedical applications in mind. It starts by allowing two ISFETs to share the same ion sensing membrane and a common floating gate. Arranging them in a simple FG inverter configuration, their switching may be triggered by either the reference voltage or chemical pH change. In order to enhance its input noise immunity, a chemical Schmitt Trigger is presented.

Using ISFETs for the detection of minute pH changes have been a challenge. A simple method to locally scale input referred chemical signal at the ISFET's floating gate is presented. It is based on using the ratio of capacitive coupling to the floating gate. The chemical signal is coupled via the passivation capacitance (C_{pass}) while an electrical input (V_2) is coupled via a poly capacitance (C_2). V_2 sees the chemical signal with a scaling of C_{pass}/C_2, which can be designed.

Finally, ISFETs suffer from initial trapped charges that cause mismatch between devices in the same die. A fast matching method is presented here, that can be used to hugely reduce mismatch of arrays of FG devices. It is based on using indirect bidirectional tunnelling. Two tunnelling structures are added to each ISFET's FG, one adds electrons to it while the other removes them. It is possible to match all ISFETs' initial FG voltages to a point where both tunnelling currents reach equilibrium.

Dedication

To my parents,

family,

and great teachers

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Table of Abbreviations

ADC	Analogue to digital conversion
AFGA	auto zeroing floating gate amplifier
CTD	charge Transfer device
DOC	depletion operation condition
DNA	Deoxyribonucleic acid
ECB	electron tunnelling from the conduction band
FG-MOS	Floating gate metal oxide semiconductor
FG-MOSFET	Floating gate metal oxide semiconductor field effect transistor
EIS	electrolyte-insulator-semiconductor
HVB	holes tunnelling from the valence band
ISFET	ion sensitive field effect transistor
LPECVD	Low pressure chemical vapour deposition
MIS structure	metal-insulator-semiconductor structure
MITE	Multiple input translinear element
NM	Noise margin
PCR	Polymerase chain reaction
PG-ISFET	programmable gate ISFET
PLL	Phase Locked Loop
PWM	pulse width modulation
SAM	self applied mono-layer
SNPs	Single-nucleotide polymorphism
SNR	signal to noise ratio
STD	Standard deviation

List of Symbols

ϵ_0	Permittivity of free space
$\epsilon_{r_{ox}}$	Relative permittivity of silicon oxide
μ	Majority carrier mobility
C_{ox}	The gate oxide capacitance
λ	Channel length modulation parameter
I_{inj}	Hot electron injection current
J_{tun}	Tunnelling current density
q	The electronic charge
$\hbar$	Reduced Planck's constant, $= h/2\pi$
m^*	Effective electron mass in oxide insulator
ϕ_{ox}	The oxide barrier hight
ϕ_{ox}	Silicon-Silicon dioxide barrier hight $3.15eV$
k	Boltzmann constant
T	Absolute temperature in Kelvin
g_m	The intrinsic MOSFET's transconductance
U_T	Thermal voltage
e	Electron charge
α	Dimensionless sensitivity parameter
γ	A grouping of all pH independent terms of V_{chem}
V_{fg}	Floating gate voltage
Q_TC	Instantaneous trapped charges in a floating gate
V_{fg_0}	Initial floating gate voltage
Q_{TC_0}	Initial trapped charges in a floating gate
V_D	Transistor's drain voltage.
V_G	Transistor's gate voltage.
V_S	Transistor's source voltage.
V_B	Transistor's body (bulk) voltage.
V_{gs}	Gate-source voltage of a transistor.
V_{ds}	Drain-source voltage of a transistor.
V_{in}	Input voltage
A_i	Overlap area of two poly silicon plates
C_T	Total capacitance seen by the floating gate
C_{GS}	Gate-source capacitance of a MOS transistor
C_{GD}	Gate-drain capacitance of a MOS transistor
C_{GB}	Gate-body capacitance of a MOS transistor
$C_{MOS}V_{MOS}$	MOSFET contribution to the floating gate voltage

List of Symbols

V_{dd}	Supply voltage of MOS circuit
V_t	Threshold voltage of a MOSFET
V_{tp}	Threshold voltage of a p-type MOSFET
V_{tn}	Threshold voltage of a n-type MOSFET
V_{fg-s}	$V_{fg} - V_s$ of a floating gate transistor
d_{ox}	Oxide layer thickness
K_f	A technology dependant flicker noise constant
WL	Width $\times$ length of a transistor's gate
$\bar{V}^2$	Noise spectral density
νMOS	Floating gate MOSFET with more than one input
H^+	Proton, an ionised Hydrogen atom
V_{ref}	Reference electrode voltage
V_{chem}	The chemical voltage
ψ_0	Potential at solid insulator surface in contact with electrolyte
K	Dissociation constant
V_p	Net voltage at interface of electrolyte and ion sensing insulator
xPyM	MOS process with (x) poly layers and (y) metal layers
C_{pass}	Passivation capacitance
C_{ox}	Gate oxide capacitance of a MOSFET
f	frequency
C_1	Input coupling capacitance number 1
C_2	Input coupling capacitance number 2
C_n	Input coupling capacitance number n
C_i	The coupling capacitance of the ith input
C_{t+}	Coupling capacitance of positive tunnelling voltage
C_{t-}	Coupling capacitance of negative tunnelling voltage
C_{in}	Input coupling capacitance

List of Symbols

V_{sth}	Switching threshold voltage of an inverter
V_i	Input voltage
V_0	Output voltage
I_s	Source current of MOSFET
I_{sn}	Source current of n-type and n-type MOSFET
I_{sp}	Source current of n-type and p-type MOSFET
I_{ds}	Drain-source current of a MOSFET
V_{tn}	Threshold voltage of n-type and p-type MOSFETs, respectively
k_n	Process transconductance parameter of p-type MOSFET
k_p	Process transconductance parameter of p-type MOSFET
μ_n & μ_p	Electron and hole mobilities, respectively
V_{fg_s}	Floating gate voltage at the switching point
V_{in_s}	Input voltage of FG-MOS inverter at the switching point
V_{chem_s}	V_{chem} of ISFET inverter at switching point
V_{sL}	Lower threshold voltage of a Schmitt trigger circuit
V_{sH}	Higher threshold voltage of a Schmitt trigger circuit
V_{tun}	Tunnelling voltage
V_{t+}	Positive tunnelling voltage coupled via C_{t+}
V_{t-}	Negative tunnelling voltage coupled via C_{t-}
$V_{DS_{satn}}$	Saturation drain-source voltage difference for nMOSFET
(V_{in2})	An electrical input capacitively coupled via (C_2) to the floating gate of an ISFET
p	Mismatch of a MOS parameter
NM_l	Lower noise margin, between $0V$ and first point of $gain = -1$
NM_h	High noise margin, between second point of $gain = -1$ and V_{dd}

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Chapter 1

Introduction

1.1 Motivation

This decade is witnessing the convergence of advanced semiconductor based technologies with the healthcare industry. Biomedical equipments have been used for the diagnoses, monitoring, and treatment of diseases. Semiconductor biomedical devices have been shrinking in size, getting cheaper and consume less power while improving performance to provide real time monitoring and more intelligent information processing. Thanks to better analogue and digital circuit designs in conjunction with advances in semiconductor manufacturing processes this has been possible, Moore's law [1].

Nature is analogue, so does electronic ion sensors, like an ion sensitive field effect transistor (ISFET). However, compared to a continuum of analogue levels, the digital world is much simpler, it has only two levels: "0" and "1". Its simplicity is the key to its power that made it characteristic of this digital era. Digital circuits and systems are present in every day life, from simple house hold equipment to the most sophisticated machines. In order to maintain analogue accuracy and leverage simplicity and power of

digital representation, analogue to digital conversion (ADC) is the solution. It has been used in all practical sensory systems including biomedical and chemical applications.

Deoxyribonucleic acid (DNA) sequencing is one example of rapidly advancing biomedical applications. It attracted huge attention with the start of the human genome project [2]. Traditionally, it used expensive and hazardous methods based on electrophoresis and optical sequencing [3]. Different techniques were used to improve its methods while reducing cost in a similar fashion to Moore's low [4]. Ultimately, a semiconductor based label free method was invented about ten years ago based on ion sensitive field effect transistors (ISFETs) [5]. It was based on the fact that incorporating a nucleotide into a growing DNA strand releases a hydrogen ion which reduces the solution's pH that is detectable by chemical transducers as an ISFET. This marked the convergence of DNA sequencing with complementary-metal-oxide-semiconductors (CMOS) technology enabling the production of cheaper, robust, and scalable sequencing devices in a lab on a chip environment [6]. In 2011, Ion Torrent commercially announced the integration of more than 1.0×10^9 ISFET sensor elements in one disposable chip for their small commercial lab machine that can sequence the DNA of a bacteria in one run within few hours [7]. Few years ago, such a job needed weeks [4]. That machine uses high accuracy analogue techniques where analogue to digital conversion is done as an off chip processing step in order to digitally perform all data analysis and processing.

1.1.1 Towards fully digital biomedical sensory systems

Chemical and biomedical sensors naturally measure data in analogue form. It is a standard step to convert their output signal into digital, which is much more convenient for data handling, processing, and system integration. Considering noise and parasitics, analogue signals are much more susceptible to noise than their digital counterpart. This is very important for weak chemical signals. Moreover, for mixed analogue and digital

circuits, the analogue part is sensitive to noise and spikes coming from the digital side.

It is a well known fact that lab on a chip devices that use large arrays of analogue sensors must be designed for mixed analogue and digital operation [8] [9]. Address decoders and multiplexers as well as column and raw selectors have to be digitally driven while sensing elements and their output amplifiers are analogue blocks. A sample and hold circuit is a standard block that facilitates the interface between the two worlds through analogue to digital conversion which can be done on chip or off chip. Noise and spike coupling become a standard problem of such a mixed signal design that adds to its complexity. The problem is that, the digital part is essential and the sensing, which is analogue by nature, is the target. It would be highly desirable to reduce the analogue part as much as possible and bring the digital part as close as possible to the sensing point. This implies analogue to digital conversion (ADC) should be brought closer to the sensing element ultimately localised for each sensing point. In its simplest form, a one bit ADC is a threshold detector. The question would be is it possible to bring ADC, in its simplest form, to the ISFET sensing point? That is the sensor becomes a threshold detector instead of measuring a continuum of levels that has to be digitized. This question is to be answered in this thesis.

Thresholding applications

A valid question would be how useful is it to use a chemical sensor as a threshold detector. Well, threshold detection is the effectively analogue to digital conversion in its simplest form that outputs one bit. Its accuracy may be extended by adding more thresholds and hence more bits. Moreover, there exists applications where exact and detailed information of the chemical ion concentration is not the aim. For other applications, the interest is in pH change and whether it is larger than a certain threshold or not. For example in DNA application, the question of interest is: did hybridization

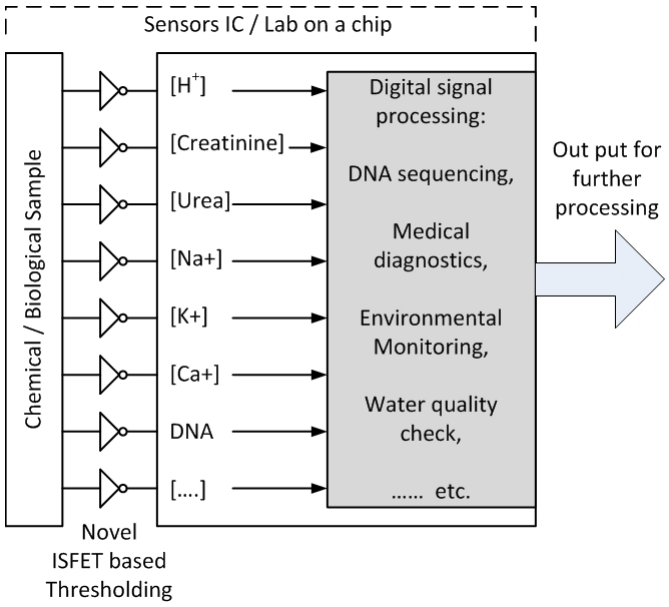

Figure 1.1: The concept of fully digital biochemical sensory and signal processing lab on a chip. No analogue signal processing is used.

take place or not [10]. Rephrasing the question would be did pH drop indicate nucleotide incorporation or not [11]. For other applications, all needed information is to find whether a chemical concentration, or pH , is above/below a certain threshold or not. For instance, water quality agencies require $10mg/l$ maximum nitrate content in drinking water [12]. All that is needed here is to know if its concentration is higher or lower than this threshold. Other application, have more than one threshold of interest. For example, water agencies specify drinking water to have pH between 6.5 and 8.5 [12]. Its exact pH value is not important; all what matters is being in this range or within these two thresholds. Similarly, it is possible to find similar thresholds of interest for effectively most clinical, environmental and chemical applications.

Therefore, building a digital sensor element that changes state when a threshold is crossed will have a great impact on sensor systems. Successful implementation of pH driven inverters opens the door for fast solid state threshold detection. It also makes it possible to build fully digital sensor arrays that include localized digital signal process-

ing. Thus, instead of fabricating mere bio-sensor chips that measure and convey large high accuracy raw data, the target is biomedical signal processing chips that locally measure and process data. Only analysis results are conveyed, which is much less data needing limited bandwidth, figure 1.1.

1.2 Research Objectives

This research aims at paving the path for fully digital biomedical sensory systems by bringing digitization to the sensing point. The most basic digital building block is an inverter or a switch. The aim is to reduce chemical sensing to threshold detection of ionic concentration where thresholds can be selected using electrical inputs. It is to give answers to the following questions:

1. Is it possible to use standard commercial CMOS process to fabricate a silicon based chemical sensor, that changes the state of its output due to predefined pH change, in a compact way that can be used in large arrays?
2. Fabricating such a chemical switch or inverter, what problems does it suffer from and how to make it better? Particularly, how to increase its sensitivity and noise immunity?
3. Building such an inverter in arrays, what is its main problem? What can be done to solve it?.

1.3 Overview

Generally, all ISFET related publications viewed its chemical signal as part of its threshold voltage [13]. This is basically how it was first introduced and analysed by Bergveld

around forty years ago [14]. The same view persisted with CMOS ISFETs, though researchers understood that ISFETs in CMOS are floating gate transistors [15]. That is the starting point of this thesis.

Chapter 2 is to review floating gate (FG) MOS transistors because of the analogy of CMOS ISFETs with them. After introducing FG-MOS operation, its inherent problem of trapped charges is to be discussed along with reported ways to deal with it. Methods that are more relevant to this research will be presented in more details. To complete its presentation, a word about FG-MOS applications is due.

Having presented FG-MOS, ISFET devices are reviewed in Chapter 3. It starts with basic ISFETs as introduced by Bergveld. Then CMOS ISFETs are presented. Solid - electrolyte interaction is presented next where the chemical voltage is derived. The ISFET modelling is presented using this chemical voltage and standard MOS device models. A word about its noise and non-ideal behaviour is due before closing the chapter with interfacing circuits and applications.

The floating gate CMOS inverter is to be reviewed in Chapter 4. Using CMOS ISFETs analogy to FG-MOS, its circuit is to be extended to the ISFET based chemical switch. Its simulations, and measurements will be presented followed by some challenges. In order to increase its input noise immunity, a chemical Schmitt trigger circuit is to be presented along with its measurements.

In floating gate MOS and ISFETs, the floating gate voltage is the weighted sum of its inputs. Exploiting this feature with the aim to amplify the chemical signal at the point of measurement will be the subject of Chapter 5. It starts by reviewing reported semiconductor ion sensitive devices with high sensitivities. A very simple and straight forward method based on sizing the capacitive coupling of inputs is to be presented along with simulations and measurement for both a single transistor ISFET and a chemical

switch.

Aiming to choose a method of matching an array of ISFETs, a review of reported ISFET's matching techniques is to be presented in Chapter 6. It is followed by testing the use of electron tunnelling to program CMOS ISFETs floating gates. After evaluating FG-MOS matching techniques, indirect bidirectional electron tunnelling was chosen for ISFET floating gate programming. It is to be presented along with its simulation and experiments for a single device. Finally, this method is extended to arrays of chemical switches. The chapter closes with a discussion and evaluation of this technique.

Finally, the conclusion summarises the research carried out towards this thesis and lists its publications. Future work describes two example methods of extending this research with large arrays in mind.

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Chapter 2

Floating Gate MOS review

2.1 Introduction

Floating gate metal oxide semiconductor transistors (FG-MOSFETs) are normal MOSFETs with their gates floating. There are no solid contacts to set the voltage of such a floating gate. Inputs can only be capacitively coupled to it, figure 2.1. This is basically the only difference between the standard MOSFET and this class of devices [1]. This brings great features and challenges to its use. Analogy of ion sensitive field effect transistors (ISFETs) built in CMOS technology with floating gate transistors (FG-MOS) will be established in the next chapter. Therefore, it makes sense to investigate FG-MOS transistors and their use to inspire ISFETs circuits.

Generally, a FG-MOS transistor can have a number of inputs that are capacitively coupled to its floating gate. The resultant floating gate voltage (V_{fg}) is their weighted sum [2]. This is one of the FG-MOS features that was exploited in due course of this thesis, as will be depicted later. Another feature of these devices is the gate's capability to store charges and to be programmed. This feature was exploited in different memory

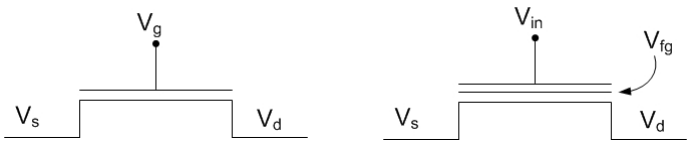

Figure 2.1: Schematic representation of a MOSFET and a FG-MOSFET transistors.

technologies. It was also used for auto-zeroing amplifiers and to set precise voltage references [1].

The main problem with FG-MOS is variable initial floating gate voltage (V_{fg0}). It is attributed to random trapped charges in the floating gate and its insulations during the manufacturing process [3]. These trapped charges constitute a shift in the initial floating gate voltage (V_{fg0}), as will be detailed in the next section. Well, this means exact V_{fg0} is simply unpredictable. It can not be dealt with using normal circuit techniques because the floating gate is surrounded by the excellent oxide insulator. Nevertheless, a number of techniques were proposed to tackle this problem. It would be interesting to investigate these methods.

This chapter starts by introducing the FG-MOS operation. Then, how trapped charges are formulated and techniques to deal with it are discussed. Finally, some floating gate MOS applications in both digital and analogue circuits are presented.

2.2 FG-MOS Operation

A floating gate MOS is fabricated by making the MOS transistor's gate electrically floating, that is isolated from its inputs and surroundings. The oxide standard CMOS isolation is normally used to wrap it. Figure 2.1 shows a schematic representation of a FG-MOS transistor, where the input is capacitively coupled to the floating gate, compared to a MOS transistor.

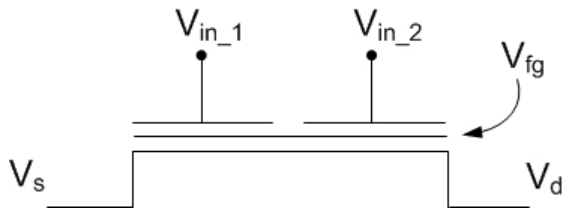

Figure 2.2: Symbolic representation of a two input FG-MOS transistor

The easiest way to model a FG-MOS transistor is to compare it with an identical MOS built using the same technology. The latter's behaviour is well modelled using its terminal voltages V_D, V_G, V_S and V_B in all its regions of operation. The only difference between the two transistors is the way the gate voltage is set. In the MOS case, a well defined V_G is externally applied. While, for FG-MOS, the floating gate voltage V_{fg} can not be set in the same way. However, because the gate is literally floating with extremely high impedance isolation around it, no current flows into it. Thus, its preserved and only capacitive coupling can be used as its input [1].

A FG device can have one or more inputs capacitively coupled to its floating gate [4]. In order to make the analysis general, "n" inputs are assumed for the FG-MOS. $n = 1$ for a single input and $n = 2$ for two inputs and so on. Figure 2.2 shows a schematic representation of a two input FG-MOS transistor while figure 2.3 shows a possible cross section for an n-type device.

Assuming planar monolithic geometry composed of two poly layers with oxide isolation sandwiched between them, the capacitance of the ith input may be found by:

$$C_i = \left(\frac{\epsilon_0 \epsilon_{r_{ox}}}{t_{ox}} \right) A_i \tag{2.1}$$

Where, C_i stands for the coupling capacitance of the ith input, ϵ_0 is permittivity of free space, $\epsilon_{r_{ox}}$ is relative permittivity of silicon oxide, t_{ox} stands for oxide thickness; and A_i is the overlap area of the two poly silicon plates [1]. Of course, this is an approximation

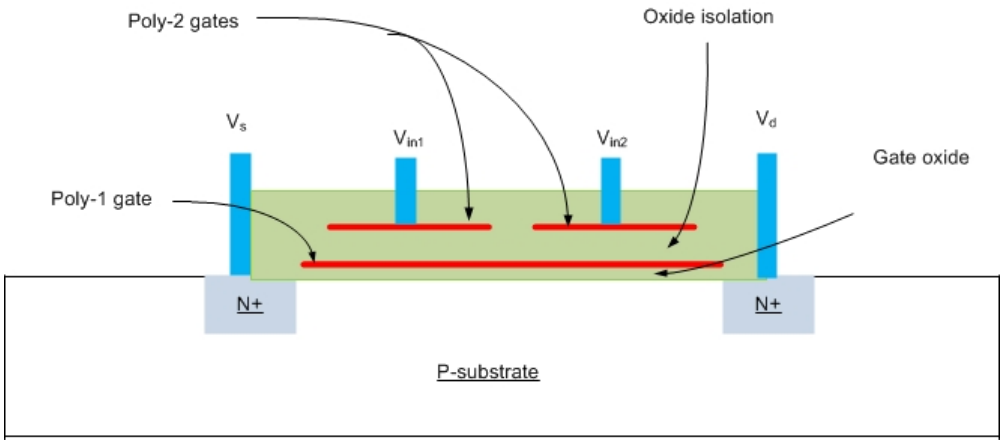

Figure 2.3: Cross sections of a two input FG-MOS transistor

as fringing capacitance and coupling capacitances to other structures around them, including ground, are not included. Nevertheless, it is a reasonably good approximation especially if care was taken during layout to reduce other effects.

Because the floating gate is surrounded by SiO_2, which is an excellent insulator, no charges can be added or removed from it after the end of the manufacturing process. Of course, this is the case under normal operating conditions where no movement of charges across the insulator take place. In this situation, the floating gate has only the random charges it is left with from the manufacturing process (Q_{TC_0}) [3]. When all nodes of the transistor and its inputs are grounded, the floating gate potential is dictated only by this charge. That is:

$$V_{FG_0} = \frac{Q_{TC_0}}{C_T} \tag{2.2}$$

where C_T is the total capacitance seen by the floating gate. That is,

$$C_T = C_{GS} + C_{GD} + C_{GB} + \sum C_i \tag{2.3}$$

where, $\sum C_i$ is the sum of all inputs' capacitances, C_{GS}, C_{GD}, and C_{GB} are the gate-source, gate-drain, and gate-body capacitances of the underlying MOS structure. With all inputs, source, and drain grounded; the total charge in the floating gate system Q_{TC} is the initial trapped charges Q_{TC_0}. This remains the case except if current flows to/from the gate across the insulating oxide. Instantaneous trapped charges (Q_{TC}) will be used hereafter as it is more general.

When, the transistor nodes or its inputs are non-zero, the net floating gate charge remains unchanged Q_{TC}. However, V_{fg} as seen by the transistor may change due to charge redistribution within the floating gate according to induced effects of its inputs. This may be calculated using charge conservation. Thus, the net charge at any time is the resultant of all charges induced by its coupled inputs. This includes charges induced by coupling capacitances of all inputs ($\sum Q_i$), gate-drain (Q_{gd}), gate-source (Q_{gs}), and gate-body (Q_{gb}). Thus,

$$Q_{TC} = Q_{gs} + Q_{gd} + Q_{gb} + \sum Q_i \tag{2.4}$$

Each input is treated as a simple capacitor. Thus, the charges induced by each input is equal to its capacitance times the voltage across it. Keeping in mind that actual net space charge in the floating gate is just the trapped charges, this gives:

$$Q_{TC} = Q_{TC} = C_{gs}(V_{fg} - V_s) + C_{gd}(V_{fg} - V_d) + C_{gb}(V_{fg} - V_b) + \sum C_i(V_{fg} - V_i) \tag{2.5}$$

Therefore, the floating gate voltage is:

$$V_{fg} = \frac{C_{gs}}{C_T}V_s + \frac{C_{gd}}{C_T}V_d + \frac{C_{gb}}{C_T}V_b + \frac{Q_{TC}}{C_T} + \sum \frac{C_i}{C_T}V_i \tag{2.6}$$

Where C_T is the total capacitance seen by the floating gate, as defined by equation 2.3. Equation 2.6 suggests that the floating gate voltage at any time is the weighted

sum of its inputs on top of the shift caused by trapped charges. The contribution of each input is simply its voltage scaled down by its coupling capacitance ratio to the total capacitance. No power is dissipated in this voltage signal addition, as no current flows. This "zero power" voltage summation directly at the transistor's gate is the most attractive feature of FG-MOS as compared to the well known wired current summation technique [4].

The contribution of MOS terminals may be summed to one term: $C_{MOS}V_{MOS} = C_{gs}V_s + C_{gd}V_d + C_{gb}V_b$. This notation is more handy as these capacitances depend on the biasing and region of operation. Thus, equation 2.6 may be rewritten as:

$$V_{fg} = \frac{C_{MOS}}{C_T}V_{MOS} + \frac{Q_{TC}}{C_T} + \sum \frac{C_i}{C_T}V_i \tag{2.7}$$

Here, all input capacitors are constants and the only variable capacitor is C_{MOS}, which is a function of the underlying MOS bias. Nevertheless, if the transistor is strongly inverted and its channel is formed, then its C_{MOS} does not change much and can safely be assumed constant equal to the gate oxide capacitance [2].

It was stated that the basic difference between a MOS and an identical FG-MOS is the gate of the latter being floating. This implies that, for MOS $V_{in} = V_g$, whereas for a single input FG-MOS, V_{in} relation to V_{fg} is more complicated. The input scaling and other terms of equation 2.7 has to be accounted for [5]. This includes a constant shift, $\frac{Q_{TC}}{C_T}$ and a variable biasing part $\frac{C_{MOS}}{C_T}V_{MOS}$, that constitutes some feedback.

The threshold voltage of a standard MOS (V_t) is constant. The same is true for the intrinsic transistor of the FG-MOS. Therefore, all equations that describe MOS operation may be used for FG-MOS after making the needed correction of using V_{fg} in place of V_g. MOS $I_{ds} - V_{gs}$ relations may be rewritten for FG-MOS, using $V_{fg-s} = V_{fg} - V_s$, as

follows,

$$I_{ds} = \begin{cases} I_{d0}\frac{W}{L}\exp\frac{V_{fg-s}-V_t}{nU_T} & \text{Weak inversion} \\ \mu C_{ox}\frac{W}{L}\left((V_{fg-s}-V_t)V_{ds}-\frac{V_{ds}^2}{2}\right) & \text{Triode Region} \\ \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{fg-s}-V_t)^2(1+\lambda V_{ds}) & \text{Saturation} \end{cases} \tag{2.8}$$

Here, I_{d0} is the specific current of the MOS transistor while V_t is its threshold voltage. U_T is the thermal voltage, n is the sub-threshold slope, and W/L is the transistor's aspect ratio given by the ratio of its channel width to its length. μ is majority carrier mobility and C_{ox} is the gate oxide capacitance while V_{ds} is the drain source voltage difference. Finally, λ is the channel length modulation parameter [6].

The most important problem with floating gate transistors is initial trapped charges in their gates. These are random in nature and unpredictable because they are introduced during the processing phase [7]. Each foundry has its own process, which results in different amount of trapped charges [8]. It is important to deal with these charges in order to build useful floating gate circuits and systems. This is the subject of the following section.

2.3 Dealing with floating gate trapped charges

Floating gate charges cause unpredictable shifts in V_{fg} of FG-MOS devices. Because they are introduced during the manufacturing process, it might be possible to limit their effect there using layout techniques. There was one reported layout technique to reduce the effects of trapped charges.

After fabrication, there are four techniques to alter trapped charges in a floating gate. They can be removed using UV exposure or set to a predefined value by means of electron tunnelling, or hot electron injection or a combination of the last two methods.

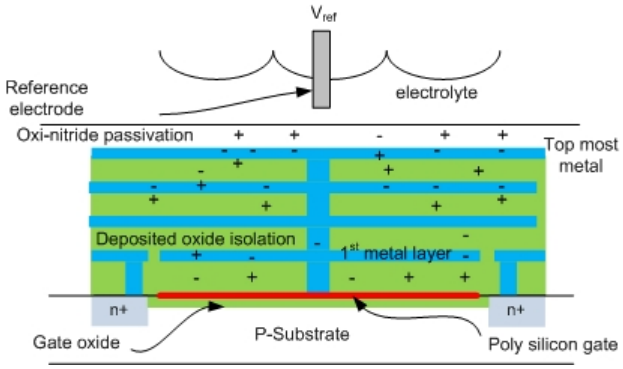

Figure 2.4: Representation of trapped charges in the stack of insulators, floating gate, and passivation layer.

2.3.1 Origin of trapped charges

In order to properly deal with floating gate trapped charges. It is vital to understand how they are generated in the first place.

The necessary doping profiles in the substrate and the growth of a clean thin layer of thermal gate oxide are common process steps for both FG-MOS and normal MOS. Afterwards, the whole wafer is covered by the poly-silicon layer used to build the transistors' gates. Its unwanted parts have to be removed. This is normally done by advanced types of reactive ion etching bombarding the undesirable areas with ions that will knock-off silicon atoms until the complete mask of this layer is formed. This process has the advantage of producing precise dimensions and vertical side walls for the gates. However, it randomly charges the remaining poly-silicon gates. This is not a problem for normal MOS devices as all gates will have a low resistance path to set their operating voltages. However, floating gate devices are left floating thereafter with these random charges causing unpredictable V_t or V_{FG_0} variations. Self aligned source and drain doping processes that follow may result in even more variations in these charges [7].

Before depositing the first metal layer, a thick oxide layer is either thermally grown

or deposited using chemical vapour deposition. Contact openings (holes) are made before the first metal layer is deposited. Once again opening these contact holes is done by bombarding the insulating layer by ions in order to make conformal openings with vertical side walls. When the openings reach ploy-silicon surfaces, this process becomes another source of random gate charges if the poly gates are contacted. Once metal layers are introduced, all gates with contacts are shorted together in the new metal layer that covers the whole wafer. This provides a means to uniformly distribute the trapped charges between contacted gates. However, floating gates without contacts are not affected. Moreover, this process affects only gates in the same wafer making them equipotential as long as they are connected by a metal layer [9].

After that comes metal etch, which is generally done by a physical process where ions bombard the unwanted metal areas to remove them. This leaves remaining metal areas with some floating charges. After the first metal deposition, no high temperature processes are allowed. Thus all oxide or nitride layers are added by chemical vapour deposition, which are not as clean, from ion generation point of view. Therefore, random charges may be trapped in the deposited metal isolation oxides. The same process repeats with every deposited metal and isolations layer. The last isolation layer to be deposited on top of the topmost metal layer is the protective oxi-nitride passivation which is not an exception, from trapped ions point of view [7].

Therefore, major sources of trapped charges are deposition and etch process steps [1]. Charges may, randomly, be trapped in the floating gate or isolation layers in the stack including the passivation layer, figure 2.4. It is very difficult to quantize the impact of each of these sources as identical circuits may end up with very different trapped charges after fabrication [10]. Examples of this for both FG-MOS and ISFET circuits are shown in chapter 6.

2.3.2 Layout Technique to reduce FG-MOS mismatch

Rodriguez et al, considering only floating gates that were formed by the poly-silicon alone with no metal contacts, suggested a method to deal with trapped charges in floating gate MOS transistors [3]. They proposed connecting these floating gates with the metal layers on top of them all the way to the topmost metal. During processing, each metal layer will first cover the whole wafer, before it is etched. During this time each layer provides a path connecting all floating gates together. If a path to ground is provided, all previous trapped charges could be removed. This way all floating gates will end up with no initial charges.

They reported the test of this technique using a three metal $0.5\mu m$ process from AMIS-C5FN [3]. However, the conclusion was that, this procedure reduced offset variations within the same wafer or die but did not affect the large variations between wafers or between dies manufactured in different processes. This indicates that, no grounding path was provided by the metal layer before its etch. All was provided is a shorting of all connected gates that will become floating after metal etch. This may explain the reduction of trapped charge variations between FG-MOS in the same die while not affecting wafer to wafer variations.

To test the above proposed method, Hasler et al fabricated large arrays of matched floating gate transistors in a $0.5\mu m$ process from MOSIS [8]. The first array had floating gate devices with one contact each to the first metal layer. The second array had ten contacts for each floating gate to the first metal. In the third array, the poly-silicon gates were floating with no metal contacts. Trapped charges offset were compared between the three arrays in four dies. This study concluded that contacts to the lowest metal layer reduced mismatch between devices in the same die but did not completely normalize it. This may lead to the conclusion that first metal layer was not grounded during

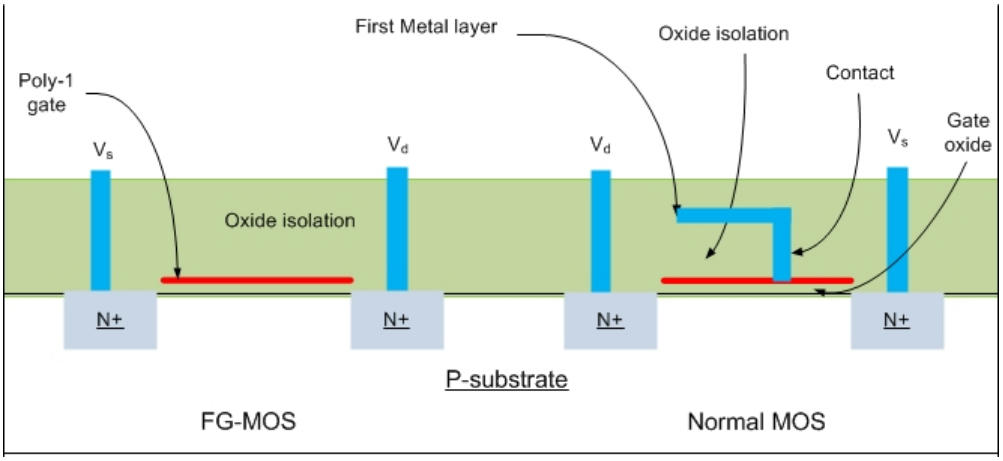

Figure 2.5: Cross section of two transistors, the first has a floating gate without a metal contact, the second is a normal MOS with a metal contact to its gate.

processing before its etch. This matching technique is highly dependant on layout.

2.3.3 UV light

Photon electron interaction is a quantum mechanical phenomenon. Basically, if a photon has comparable energy to that needed by an electron to move from valence band to conduction band, it may, with finite probability, be absorbed. This way the electron gains the photon energy and uses it to get into the conduction band. UV light, with wave lengths in the range of $254nm$, has sufficient energy to surmount the oxide barrier hight of $3.1eV$ [11]. This is the process normally used in EPROM and EEPROM erasers to remove the programmed charges from floating gate storage cells. The same method can also remove trapped charges from oxide layer.

UV illumination is not an efficient process that is why strong sources and prolonged exposure times are needed [12]. Moreover, light has to reach the poly-silicon gates in order to excite trapped charges. Thus, the layout and process have to allow path for this. From layout point of view, metal layers should leave open spaces for light to go

through and reach the floating gates [13]. A good and considerate layout technique is needed. Moreover, from processing point of view, a standard CMOS processes uses oxy-nitride passivation layers which are nearly opaque to UV light [7]. That is one reason for EPROM manufacturers to develop their own processes that use special passivation layers that allow more UV light through [14]. Another approach used for EPROM is to etch special openings in the passivation layer in order for UV light to pass to where it is needed [15] [16]. The other choice to overcome its very low efficiency is prolonged exposure with strong sources. Exposure times in the range of 10 hours are not abnormal [13].

McNulty et al demonstrated the us of UV light to remove trapped charges from floating gates in digital circuits [17]. Irradiation was done in both passive and quiescent modes. It was shown that radiation had two effects on floating gate devices. Firstly, negatively trapped charges are removed from floating gates. Secondly, positive charges are trapped in the gate oxide. Both mechanisms complement each other in reducing exposure time.

It has been widely known that UV light can be used to erase floating gate charges by removing electrons from them. That is why K. Nandhasri and J.Ngarmnil used UV illumination as a justification for assuming zero initial charges in the floating gates of their comparators [18]. They did not need to show that practically.

2.3.4 Using a Switch

The floating gate may be connected to a voltage source via a switch. Where, it may be connected to set V_{fg} then disconnected for normal operation. An ideal switch would be a great solution. However, such switches are normally realised using transistors which imply the presence of leakage current when in the off state. Therefore, the gate is no longer floating though it may be considered as pseudo floating. The set voltage level

needs to be refreshed similar to those used in dynamic memory. The needed refresh frequency depends on the floating gate total capacitance, amount of leakage current, and tolerance dictated by the application.

Kotani et al. proposed a clocked νMOS logic XOR gate where the floating gate voltage was dynamically set using a switch [19]. This logic gate was realised using two stage multiple input floating inverters. A transistor switch was used in the feedback loop of each stage. The aim was not only to reset the floating gate voltages but also to put them in the most sensitive switching region. Large floating gate capacitances were used to minimize the effect of leakage current through the switches.

2.3.5 Hot Electron Injection

The only known non-light based mechanisms to move charges across silicon oxide insulator are hot electron injection and electron tunnelling. Both are based on allowing an electron to surmount the silicon/silicon-dioxide $3.1eV$ energy barrier [11]. The first method is the subject here while the second is the subject of the next subsection.

Hot electron injection is the process whereby carriers (electrons or holes) near the surface of the semiconductor are accelerated in a high lateral electric field. Some carriers acquire sufficient kinetic energy to overcome the silicon - oxide energy barrier, these are called hot carriers. They may, under the gate to drain electric field, inject to the gate. This lateral filed does not have to be large.

Because the silicon to oxide energy barrier for electrons, $3.15eV$, is lower than that of holes, $4.8eV$, and because the electron mobility in both silicon and oxide is higher than that for holes, electrons are more likely to inject to the gate [20]. This process results in carriers moving from substrate to gate but not the other way around simply because they are generated in the channel.

Higher substrate doping makes it easier to generate hot electrons [7]. Injected hot electrons may reach the gate making gate current. Or they may get trapped in the $Si - Si0_2$ interface states contributing to the oxide's space charge. That is why this process is normally seen as a source of MOS degradation as it shifts the threshold voltage, and affects the transconductance and drain current [21].

Gate current due to hot electron injection (I_{inj}) may be modelled by:

$$I_{inj} = \beta I_s e^{\frac{V_{dc}}{V_{inj}}} \tag{2.9}$$

Where I_s is the device's source current, V_{dc} is the drain channel voltage, and V_{inj} and β are fitting constants. This means that the hot electron injection current is directly proportional to the source current of the transistor. Normally, large source currents are needed to invoke reasonable gate injection current, which may be considered a draw back for low power operation.

2.3.6 Electron tunnelling

Underneath the floating gates are very thin, clean, and uniform silicon oxide (SiO_2) layer: gate oxide. It is normally grown by dry thermal oxidation of clean uniformly crystallized silicon substrate or epitaxial layer. This gate-oxide layer may have very small number of trapping cites in its interface with silicon [22]. These are lattice disorders that may trap charges. There is also other oxide layers on the sides and on top of the gate. This is normally grown by dry or wet oxidation of the poly-silicon gate or deposited using chemical vapour deposition, depending on the process used. These oxide layers normally have much more trapping sites than the clean gate oxide [7].

Tunnelling is normally avoided in CMOS devices because electrons may get trapped within silicon oxide insulator trapping sites, which causes degradation. Charges trapped

in such sites may cause mismatch when released in the stress induced leakage current phenomena [23] [24]. However, these problem decrease with reduced trapping sites and reduced tunnelling currents to the point that devices with continuous tunnelling were proposed [22] and flash memories may be programmed millions of times before failure [26]. Thus, it is more appropriate to use the high quality thermal gate oxide, which has far less trapping sites than the inter-poly or inter-metal oxide insulator [27]. High tunnelling currents cause degradation of the oxide insulator making it leaky which is a reliability problem. It reduces charge retention capability, lifetime, and robustness of FG-MOS circuits. [25].

Tunnelling may take place in all capacitive structures if strong enough fields are present, for these reasons, poly-poly capacitors or metal-metal capacitors are not to be used for this purpose in this thesis. Therefore, the tunnelling discussion here is focused on the system composed of the poly-silicon gate, gate oxide, and the substrate [28]. This is a metal-insulator-semiconductor (MIS) structure.

For (MIS) structures, the tunnelling current depends not only on the applied voltage but it, also, critically depends on the insulator thickness. For a thick oxide layer ($d_{ox} > 5nm$), carrier transport through the insulator is negligible and such a structure represents a standard MIS capacitor [11]. In this case, Fowler-Nordheim tunnelling is the only practical tunnelling mechanism. However, if the insulator layer is very thin ($d_{ox} < 1nm$), the system behaves like a Schottky-barrier diode where carriers may flow between the metal and the semiconductor with little resistance just like a tunnelling diode[11]. Direct tunnelling becomes important for oxide thickness between these two limits.

Because the gate oxide of the devices manufactured and tested in the work of this thesis had gate-oxide thickness in the range of $7.6 \pm 0.5nm$ [29], Fowler-Nordheim tunnelling model is more relevant. It will be the focus of attention while other tunnelling

mechanisms will be briefly presented.

Fowler-Nordheim tunnelling

The application of an electric field across the insulating gate oxide bends energy levels of the MIS system. If high enough electric field is applied, the probability of electrons tunnelling through the insulating oxide increases. Fields in the range of $0.75V/nm$ to $1.0V/nm$ are sufficient to provoke Fowler-Nordheim electron tunnelling [22]. It is characterised by a triangular shape barrier where electrons tunnel through only part of the insulator area, figure 2.6 [11].

For metal-insulator-semiconductor (MIS) devices with silicon oxide thickness's greater than $5nm$, Fowler-Nordheim tunnelling dominates other tunnelling mechanisms [30]. It is modelled by:

$$J_{tun} = A_0 E_{ox}^2 e^{\left(\frac{E_0}{E_{ox}}\right)} \tag{2.10}$$

Where:

$$A_0 = \frac{q^2}{16\pi^2 \hbar \phi_{ox}} \qquad and \qquad E_0 = \frac{-4\sqrt{2m^*}(q\phi_{ox})^{3/2}}{2\hbar q}$$

Here, J_{tun} is the tunnelling current density, q is the electronic charge, $\hbar = h/2\pi$ is the reduced Planck constant, m^* is the effective electron mass in the insulator, and ϕ_{ox} is the oxide barrier hight at the oxide-semiconductor interface, equal to $3.1V$, for thermal oxide insulation. E_{ox} is the electric field across the oxide insulator given by the difference between tunnelling voltage V_{tun} and floating gate voltage (V_{fg}) divided by oxide thickness (d_{ox}).

A_0 represents a pre-exponential constant approximated by $9.63 \times 10^{-7}\ A/V^2$, and E_0 is a constant representing the starting point of analysis, nearly equals to $2.77 \times 10^8\ V/cm$

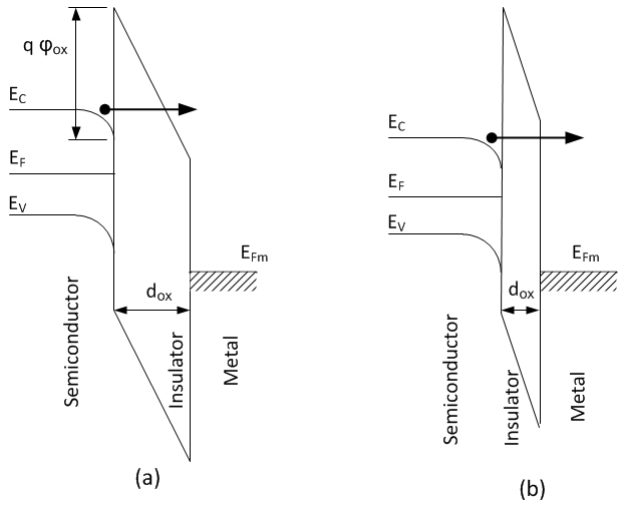

Figure 2.6: Tunnelling mechanisms(a) Fowler-Nordheim tunnelling through a triangular barrier and only part of the insulator layer (dominates for $d_{ox} > 5nm$); (b) Direct tunnelling through whole insulator layer (dominates for $5nm > t_{ox} > 1nm$).

[11, 22]. Thus, tunnelling depends only on $E_{ox} = (V_{tun} - V_{fg})/d_{ox}$ and current flows in the direction to reduce it. Electrons may move in both directions to/from the floating gate depending on the polarity of applied tunnelling voltage.

This model is based on several assumptions . These include [31]:

1. Constant d_{ox}; which does not extend by substrate or gate depletion.
2. Metal gate material, or doped poly-silicon that can be treated as metal. Thus, gate depletion and inversion are ignored.
3. Abandant carrier concentration. Hence, tunnelling dependence on carrier availability is ignored.

Fowler-Nordheim model explains tunnelling for thick oxides. In that region quantum mechanical effects associated with reduced oxide thickness can be neglected. However, it fails to explain electron tunnelling when the potential across the oxide is lower than the potential barrier of the $Si - Si0_2$ interface of $\phi_{ox} = 3.1eV$. Gate current in this region

may be modelled by direct tunnelling. The transition from Fowler-Nordheim tunnelling to direct tunnelling may be approximated by the point where: $E_{ox} = \frac{\phi_{ox}}{d_{ox}}$. The electric field ($E_{ox}$) for a medium tunnelling current is in the range $6MV/cm = 0.6V/nm$. This gives oxide thickness of $t_{ox} \approx 5nm$ [11]. For nominal oxide thickness of $7.6nm$, this field strength needs voltage difference of about $4.6V$. All tunnelling voltages used in the experimental work here had higher magnitude than this value.

Direct tunnelling

Fowler-Nordheim model fails to model tunnelling for oxide thickness less than $5nm$ or when the voltage difference across the oxide of less than ϕ_{ox} [31]. In this case, direct tunnelling dominants other mechanisms as long as the oxide is not very thin that the device behaves as a Schottky diode [11].

The direct tunnelling gate current density is given by [32]

$$J = A_0 E_{ox}^2 e^{\frac{-E_0\left(1-\left(1-\frac{V_{ox}}{\phi_{ox}}\right)^{3/2}\right)}{E_{ox}}} \tag{2.11}$$

This is a modified version of the gate current as predicted by Fowler Nordhiem in equation 2.10. It uses the same terms apart from V_{ox} which stands for voltage across the oxide and ϕ_{ox} which is the potential barrier of the $Si - Si0_2$ interface. If $V_{ox} = \phi_{ox}$ then it reduces to equation 2.10. If $V_{ox} < \phi_{ox}$ then, it predicts a higher current than that of equation 2.10.

In conclusion, tunnelling is an exponential function of voltage difference between applied tunnelling voltages and floating gate voltage. Moreover, the oxide becomes leaky with repeated tunnelling especially with high currents. That is why this process has to be treated with extra care making sure that tunnelling current remains at very low density.

2.4 Noise in FG-MOS

Being transistor based devices, FG-MOS have similar noise sources as their intrinsic transistors. Its inputs are coupled via capacitors which are effectively noiseless elements. The most important noise sources in MOS transistors are thermal noise and flicker noise. The former is due to thermal excitation of charge carriers. It is proportional to absolute temperature. With no frequency dependence, it is uniform across frequency spectrum. This type of noise appears in all types of physical devices that exhibit resistive behaviour including transistor's channel, source, and drain regions. The MOSFET's thermal noise may be expressed as the summation of their thermal noises. In saturation, it is [6]:

$$\bar{i}_d^2 = 4kT\frac{2}{3}g_m + \frac{4kT}{R_s} + \frac{4kT}{R_d} \tag{2.12}$$

While, is sub-threshold, the first term changes to [33],

$$\bar{i}_{d_c}^2 = 2qI_{ds}$$

where, k is Boltzmann constant, T is absolute temperature, and g_m is the intrinsic MOSFET's transconductance.

By contrary, flicker noise is inversely proportional to frequency. Hence, it is also named $1/f$ noise. It is mainly caused by channel energy band traps that randomly capture carriers and release them after sometime. This causes a disturbance in the current flow that reduces with frequency increase [11]. It is known to be higher in n type devices than in p type transistors. Flicker noise may be represented by [6]:

$$\bar{V}_g^2(f) = \frac{K_f}{WLC_{ox}f} \tag{2.13}$$

where, K_f is a technology dependant flicker noise constant, W and L are the width and

length of the device's gate, C_{ox} is the gate capacitance, and f is the frequency. The above equation suggests maximising the devices dimensions in order to reduce its flicker noise.

Other noise mechanisms do exist but they are not as important. For instance, shot noise is related to leakage currents of drain and source junctions. Additional thermal noises come from contact resistances and substrate and gate currents. These are generally small and may safely be ignored [34].

The difference between FG-MOS and MOS devices appears when the noise is referred to the input. The latter's input is its gate voltage but that is not the case for the former. Floating gate transistors may have multiple inputs and its floating gate is determined by their weighted sum. This shows up when referring noise to one of its inputs. Ignoring the transistor's term in equation 2.7, and assuming no trapped charges, the gate noise spectral density ($\bar{V}_g^2$) as referred to an input voltage will be [1]:

$$\frac{\bar{V}_i^2}{\Delta f} = \frac{C_T}{C_i}\frac{\bar{V}_g^2}{\Delta f} \tag{2.14}$$

Therefore, the input will see an amplified version of the MOSFET noise. However, this may have a limited impact on the dynamic range, because the floating gate already sees the input with an equivalent scaling. Thus, as seen by the floating gate, their is no increase in noise.

2.5 Applications for FG-MOS

The floating gate is effectively a node that does not have a direct path to a fixed voltage source and yet controls current between the source and drain of a transistor. It may have one or more inputs. If charged, it retain charges for very long time periods. The only

way to alter its charge is through special techniques. This made a FG-MOS device an excellent candidate that may be used to achieve flexibility, controllability, and tunability [1].

Thanks to FG-MOS flexibility, simple linear and complex non-linear functions may be realizes using FG-MOS circuits in a compact way. Effective floating gate voltage may be decided by a number of inputs. This provides for its controllability. Finally, tunability is brought by programming its floating gate charges.

2.5.1 Digital applications

Floating gate devices were first used in digital memories including EPROMs, EEPROMS, and Flash memories [35]. Digital floating gate technology have been present in nearly every electronic equipment all the way from main frame computers, PC's and laptops to mobile phones and pads.

A memory floating gate transistor is programmed or erased by modifying its floating gate charges using Fowler-Nordheim electron tunnelling. This programming for digital applications does not need the high precision required by analogue use. All that is needed is to result in V_{fg} higher/lower than a certain threshold. The exact value is not important. This is the reason behind its simplicity and power [25].

Shibata and Ohmi introduced the threshold gate [4]. It is composed of a multiple input floating gate inverter followed by CMOS inverter buffer. For example, a two input threshold gate has one main input that causes switching and a second input that controls its switching point. It was used in [36] in a feedback loop to build a Muller-C element.

This idea was extended by Shibata et al to floating gate logic [37]. It was named νMOS

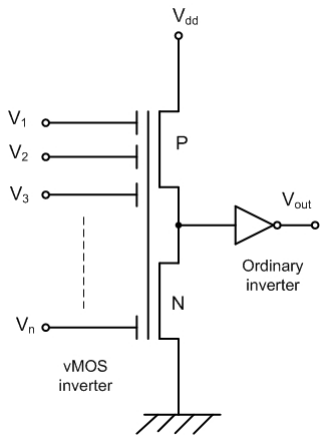

Figure 2.7: Schematic representation of the complementary νMOS inverter presented in [37].

logic because it performs a weighted sum at the input in a similar way to neurons [38]. Figure 2.7 shows an n input νMOS inverter followed by an ordinary inverter. They explained how it is possible to use this technique to realise complex logic functions using minimal circuit components [2]. This technique was used to build a number of digital blocks. For example, floating gate logic was used to build an adder and a sorting network that were used in arithmetic blocks [1].

νMOS logic techniques were not widely used because they lead to circuit configurations that use multiple threshold levels that increase in number with inputs. This placed constrains on process tolerances that were enjoyed with only two level logic [1]. Therefore, its use was not fully exploited.

2.5.2 FG-MOS analogue applications

Analogue use of FG transistors have been attracting researchers attention since the 1980's [39]. This was more encouraged by their fabrication in standard CMOS, unlike the special processes traditionally needed to manufacture digital memories [35]. Nevertheless, two poly layers are still desirable for floating gate circuits [25].

Analogue applications for floating gate transistors may be categorised into three groups: analogue memory elements, capacitor based circuits, and adaptive circuit elements [39].

Capacitor based circuits

Floating gate circuits can be used as counter parts to traditional resistor based circuits, used for discrete devices. Coupling capacitors to floating gates act as weighted inputs depending on their sizes and the total capacitance of the floating nodes. A number of tunable circuits were proposed where a floating gate has a number of inputs. One represents the main input to be processed, while other inputs provide the circuit tuning [39].

In reference to equation 2.8 where only V_{fg-S}, V_t difference appears in all regions of operation. It is possible to view selected terms of V_{fg}, as defined in equation 2.7, as part of V_t while other terms are viewed as part of V_{fg}. Thus if two inputs are used for a FG-MOS. One may be used as the normal input while the other is used to tune the devices threshold voltage. This method was used in [40] to build a charge correcting cell for FG devices.

In his PhD thesis, Minch, studied the use of multiple input floating gate transistors in translinear circuits [20]. He investigated the use of FG circuits operated in weak inversion in order to utilise their exponential current voltage relationship. The term "Multiple input translinear element" (MITE) was proposed and used to build Log domain filters as an application example [41].

Floating gate devices were used to build low voltage amplifiers. For example, an ultra-low voltage transconductance amplifier that uses these devices was proposed in [42]. It had the advantage of being highly linear with rail to rail voltage as low as $1V$. A similar target of low supply voltage and rail to rail operation was also proposed in [43].

Another low voltage tansconductance amplifier was proposed in [44]. It is different from the preceding designs in its high frequency response.

Analogue memory elements

In FG-MOS, the poly-silicon gate is surrounded by silicon oxide. Thus, its charges are stored effectively permanently forming a long - term memory. The basic charge unit, electron, is so tiny that huge amounts are needed to charge floating gate capacitors. Thus, it is possible to use them in order to provide storage for a continuum of voltage levels. Fabricating floating gate circuits with tunable threshold voltages, it is possible to adjust their V_t to optimal values for their applications.

In this type of circuits, floating gate charges are programmed in order to match or control their V_t through changing the term $\frac{Q_{TC}}{C_T}$ of equation 2.7 only once, either during manufacturing or first time use. This may be done by allowing current to flow through the isolation silicon dioxide; hence, permanently changing trapped charges in the floating gate. This technique may be used in a similar way to trimming in order to match circuit elements [1].

In [45], a CMOS programmable analogue memory array was presented using floating gate devices as the basic on chip memory cell elements. A digital off chip module was used to program on chip biasing voltages using these memory cells. The aim was to achieve high precision biasing with reduced pin count.

FG-MOS threshold voltage tuning using Ultra Violet light in order to achieve optimal performance was presented in [46]. This may enable ultra-low supply voltage for ultra low power applications [12]. However, using only UV light for tuning floating gate voltages is restricted in the sense that it can only remove electrons from floating gate and can not add them except under special biasing conditions [12]. Nevertheless, UV

light was used to tune the center frequency of a floating gate Phase Locked Loop (PLL)in [47]. This circuit used the UV light feature of moving electrons to/from the floating gate. It uses long exposures of short wave length UV light, $254nm$. Exposure times as long as 25 hours may restrict the use of such a technique.

Fowler-Nordheim electron tunnelling was used in [48] to build a very high precision voltage reference cell using floating gate devices. This floating gate analogue voltage reference had an accuracy of $200\mu V$ with negligible long term drift. It used a poly-poly capacitance in a differential dual floating gate architecture in order to achieve extremely low temperature coefficients and improved power supply rejection. Tunnelling devices were built in such a way to allow electron tunnelling in both directions to/from the flouting gate. The voltage reference buffer amplifier was biased in the sub-threshold with current as low as $500nA$. This guarantees low power operation. However, it was built in E2PROM CMOS process which facilitates for tunnelling structures that are not readily available in standard CMOS. It, also, needed high voltages in a special programming protocol that dictated the use of a special circuit for factory programming.

Adaptive floating gate circuits

This is a class of floating gate circuits where V_{FG} is continuously modified by changing the term $\frac{Q_{TC}}{C_T}$ of equation 2.7. This is achieved through allowing current to flow through the isolation silicon dioxide using simultaneous tunnelling and hot electron injection.

The auto zeroing floating gate amplifier (AFGA) presented in [27] is one of the fine floating gate device's applications that received much attention. It uses a balanced combination of Fowler-Nordheim electron tunnelling and pFET hot electron injection to adaptively set the dc operating point of the amplifier. The beauty of this circuit is the continuous adaptation being inherent, no additional circuitry is needed [49] [50]. Some of

the computational and adaptive properties of biological synaptic elements were emulated by the single transistor synapses introduced by Hasler [51]. Here, a complementary combination of electron tunnelling and hot electron injection to continuously modulate current without altering the circuit's behaviour was indirectly achieved.

2.6 Conclusion

Floating gate transistors were reviewed in this chapter. They were introduced and compared with a standard MOS device. Their theory of operation was presented where the problem of trapped charges was faced. Methods of dealing with it were discussed. A word about noise in this class of devices was due before mentioning some of its digital and analogue applications. The introduction of this class of devices was needed as they are inherent in CMOS ion sensitive field effect transistors which are the subject of next chapter.

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Chapter 3

The Ion-Sensitive Field Effect Transistor

3.1 Introduction

The ion sensitive field effect transistor (ISFET) was first introduced by Piet Bergveld in the late 1970s [1]. It was built for the purpose of miniaturised electro-physiological measurements [2]. Since then, it has been used for diverse biological, environmental, and industrial applications [3]. It has been attracting attention for its robustness, accuracy, and miniaturized size. It is superior to glass electrodes traditionally used to measure pH [4].

The ISFET is basically a metal-oxide-semiconductor field effect transistor (MOSFET) where its metal gate is replaced by an electrolyte that comes into contact with the gate insulator. A reference electrode is immersed in the electrolyte to set its potential. Its ion sensitivity arises from the interaction between the electrolyte and both the reference electrode and gate insulator which acts as the ion sensing membrane [4].

The first ion sensing membrane to be used was Silicon dioxide. Simply because it is a standard gate insulator and, at the same time, it is a similar material to glass electrodes, traditionally used for pH measurement. It was found to be sensitive to proton (H^+) concentration of a solution, that is its pH [2]. Different insulator materials were shown to give different pH sensitivities [5]. Adding an ion selective membrane on top of the oxide gate insulator, the ISFET gains ion selectivity [6].

Early ISFETs were manufactured using special MOS processes because they had no poly-silicon gates and had special layout requirements that facilitate encapsulation. Attracted by cheap mass production of standard CMOS processing, it has been used to manufacture ISFETs since 1999 [7]. This brought more advantages as driving circuitry and pre-processing blocks can be integrated in the same IC with the sensor. Moreover, arrays of ISFETs could be built allowing a wide range of applications including lab on a chip.

There are a number of non-idealities with ISFETs. Devices sharing the same die generally have different threshold voltages that suffer from temporal drift. Moreover, ISFETs exhibit light and temperature sensitivities. These contribute to its hysteresis and limit its lifetime. Well, these problems are not as bad as they may sound. There are ways to deal with them.

A review of early ISFETs and their theory of operation is to be presented in section 2. Next, ISFETs in standard CMOS process and its analogy to floating gate transistors are discussed in section 3. The chemical voltage is presented in section 4 in order to present models in section 5. After that, non ideal behaviour of these devices is reviewed in section 6. Finally, a word about ISFET applications and biasing circuits is due in sections 7 and 8.

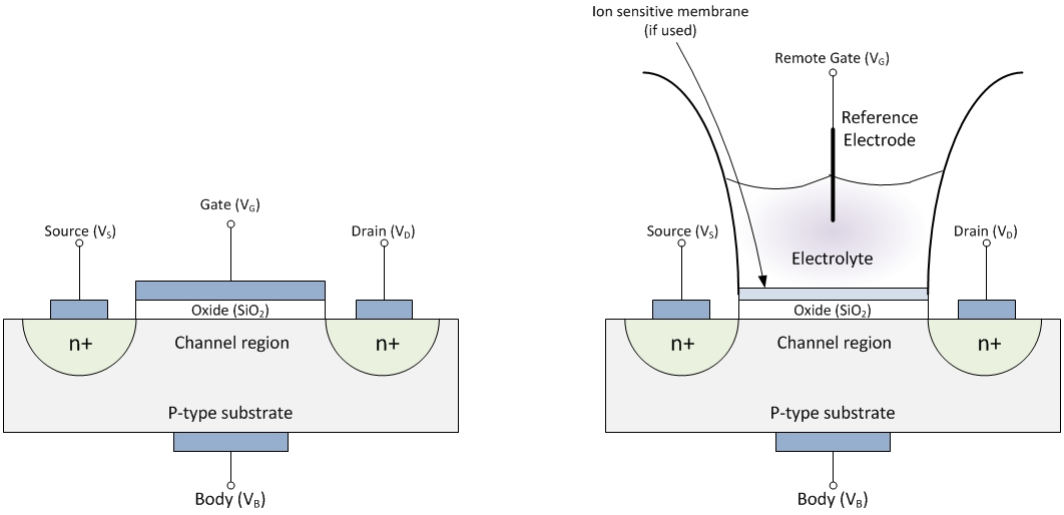

Figure 3.1: A representation of ISFET and analogy to MOSFET

3.2 Basic ISFET and MOS Analogy

A basic ISFET, as first invented, is composed of a Field Effect Transistor (FET) that has no metal (or poly-silicon) gate [2]. It is replaced by a reference electrode that is immersed in an electrolyte solution which comes into contact with the gate oxide of the transistor. Figure 3.1 presents a cross section of both an ISFET and a MOSFET of the same type. It shows how the gate oxide becomes the ions sensitive membrane. Other materials may be used or added on top of it in order to add ion selectivity [2]. This is basically how this structure is different from the standard MOSFET. Therefore, the MOSFET model is a natural starting point to model ISFETs.

The voltage drops arising from interactions of the reference electrode, the electrolyte and the ion sensitive membrane can be viewed as part of either the gate-source voltage (V_{gs}) or the threshold voltage (V_t). This is supported by the fact that it is their difference

that appears in the MOSFET $I_D - V_{GS}$ relations in all regions of operation, eq. 3.1.

$$I_{DS} = \begin{cases} I_{D0}\frac{W}{L}\exp\frac{V_{GS}-V_t}{nU_T} & \text{Weak inversion} \\ \mu C_{ox}\frac{W}{L}\left((V_{GS}-V_t)V_{DS} - \frac{V_{DS}^2}{2}\right) & \text{Triode Region} \\ \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS}-V_t)^2(1+\lambda V_{DS}) & \text{Saturation} \end{cases} \tag{3.1}$$

Because the reference voltage (V_{ref}) is externally applied to the device, which is the case for the MOSFET gate voltage (V_g). It was debated that V_{ref} remotely plays the role of V_g [1]. From this point of view, the electrolyte plays the role of the gate metal which comes into contact with the gate-oxide. Therefore, chemical dependant potentials have been seen as related to V_t.

In MOSFET, V_t is decided by the gate material, substrate doping, their insulator and the charges in this system. It is a constant for each device. Because the manufacturing process is very well controlled, its variation across devices is well controlled [8]. However, in the ISFET, according to this analogy, the electrolyte becomes part of this system making its V_t dependant on electrolyte's properties [2]. Therefore, its threshold voltage reflects this by exhibiting ion concentration dependence.

The basic ISFET as introduced by Bergveld [4] required exposing the gate isolation to the electrolyte under test while in the same time encapsulating other areas from it [9]. The aim was to protect other areas and bonding wires from reacting with the solution under test which causes undesirable effects. It had no poly-silicon gate. Thus, CMOS self alignment was not possible and the separation of the source and drain implants had to be done using photo-lithographic techniques. Moreover, the insulating pH sensitive membrane was deposited directly on the substrate. This brought even more process changes as compared with standard CMOS process. Low pressure chemical vapour deposition (LPECVD) was used to produce thin silicon dioxide layers on

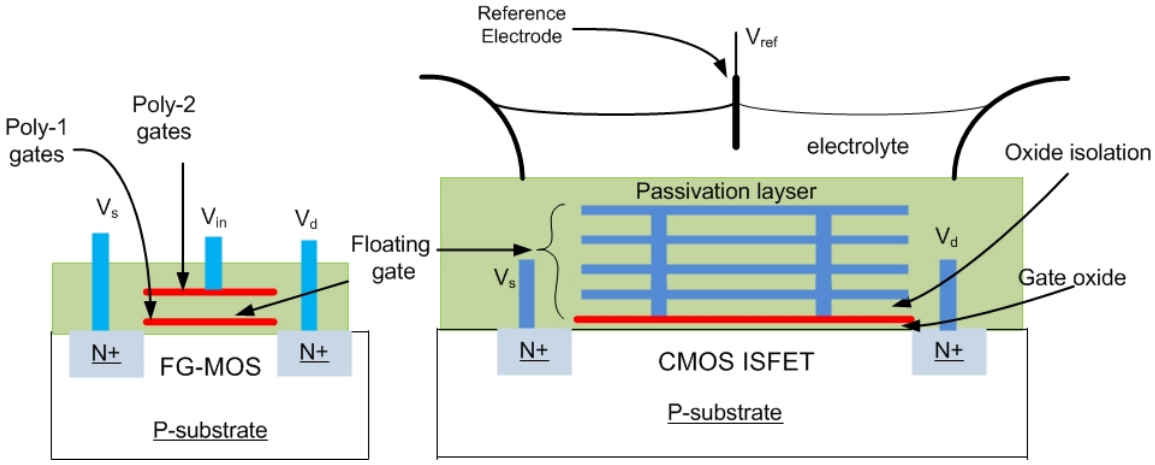

Figure 3.2: Cross section representation of a FG-MOS and an ISFET built in a standard CMOS process, indicating its parts and the chemical and electrical gates.

the substrate. This process needs higher temperatures than Aluminium metal can withstand. Therefore, modifications of the metal and contact materials were needed in order to be compatible to such high temperatures [10]. This meant basic ISFETs have to be built using dedicated processes that are not CMOS compatible.

The advantage of special processing steps was the production of reliable ISFET devices that have high sensitivities around $59mV/pH$, known as the Nernstian limit. This was attainable using Ta_2O_5/SiO_2 as the gate insulator [10]. However, this was not without the price of added complexity and extra cost. Thus, producing ISFETs in such processes is less attractive than making them in standard unmodified CMOS processes.

3.3 ISFET in Standard CMOS Process and floating gate MOS Analogy

Building ISFETs using commercial CMOS processes not only realized cheaper mass production, but also brought more advantages. Namely: driving circuitry and pre-

Table 3.1: Examples of ISFETs built in commercial CMOS technologies [11].

year	Type	Passivation thickness (μm)	Passivation material	Threshold voltage (V)	Sensitivity (mV/pH)	Technology
1996	n-type	1.5	-	3.5	41	Atmel 1μm 1P2M
1999	n-type	1.5	-	-7 to 6.5	47	Atmel 1μm 1P2M
2000	n-type	0.75	SiO_2/Si_3N_4	8.5	25	AMS 0.6μm 2P3M
2002	p-type	0.4/0.6	Si_3N_4/SiO_xN_y	-8 to -33	42	AMS 0.6μm 1P2M
2004	n-type	1	Al_2O_3	< 0.4	0.22	AMS 1.6μm 1P2M
2004	p-type	0.4/0.6	Si_3N_4/SiO_xN_y	-5	42	AMS 0.6μm 2P3M
2005	n-type	-	-	-	31-51	AMS 1.5μm 1P2M
2008	p-type	1.03	SiO_2/Si_3N_4	-4 to -1	46	AMS 0.35μm 2P3M
2008	n-type	0.5/0.7	SiO_2/Si_3N_4	-1.03 to 4.7	33.2	UMC 0.18μm 1P6M
2008	n-type	0.6/0.7	SiO_2/Si_3N_4	-10 to -0.03	33.6	UMC 0.25μm 1P6M
2008	n-type	1.03	SiO_2/Si_3N_4	0.97 to 1.73	31.7	AMS 0.35μm 2P4M
2010	p-type	0.5/0.7	SiO_2/Si_3N_4	0.8	37	UMC 0.18μm 1P6M

processing blocks could be integrated in the same IC with the sensors. Moreover, arrays of ISFETs have been built allowing a wide range of applications including lab on a chip [4].

In 1999, Bausells et al integrated an ISFET using the 1μm single poly-silicon, double metal standard CMOS process of Atmel-ES2 [7]. They integrated a standard CMOS amplifier in the same die. Basically, the ISFET was given, for the first time, a poly-silicon gate that was floating and connected to the metal stack on top of it all the way up to the topmost metal layer where the ions were sensed through the oxi-nitride passivation layer, figure 3.3. This basic idea was carried out by others and ISFETs were built in different commercial CMOS processes with multiple metal layers [3]. Table 3.1 lists a number of built and measured CMOS ISFETs.

It is interesting to note that the transistor part here is effectively a floating gate (FG-MOSFET), figure 3.2. The sensitive part looks like an ion sensitive capacitor where the topmost metal is one plate and second plate is formed by the electrolyte with passivation as the insulation layer. This is very similar to the traditional capacitive ion sensor. The reference electrode is there in order to set the electrolyte's potential [12].

The splitting of this passivation capacitance from the transistor gate insulator makes them two different structures. They may have different sizes. Hence, the ISFET's transistor gate may be called "electrical gate" and the topmost metal under the ion sensitive membrane may be called "chemical gate" [13]. This splitting allows for the difference in gate sizes to be reflected simply through their coupling weight to the floating gate. This is particularly important as ISFET's pH sensitivity was first calculated for basic devices where the electrical gate is, in the same time, the chemical gate; figure 3.1 [2].

In order to model the ISFET behaviour,the electrolyte related potentials have to be found first. The chemical voltage (V_{chem}) represents all these interactions. It stands for the resultant voltage change from the input of the reference electrode to the outer surface of the ion sensing membrane. It is the subject of the section to come.

3.4 The chemical voltage

Ion sensitive field effect transistors have been widely used as pH sensors. Their pH sensitivity is explained by the double layer model and site-bonding theory [1].

The first derivation of its pH dependence was done for the early ISFETs where the chemical gate is at the same time the electrical gate. Thus, the chemical dependent voltage was seen as part of V_t. Simply because its analysis stared with the analogy of the standard MOS device, where, the reference electrode played the role of a remote gate. In that analogy, all interactions that appear between the remote gate node and the semiconductor channel, spanning between source and drain, were related to the device's V_t. This was supported by the actual physical structure of the device which had a combined chemical electrical gate with the same insulation layer, figure 3.1. Lots of the studies were concentrated on electrolyte-insulator-semiconductor (EIS) structures

seeing it as part of ISFET's V_t [14] [2].

Most of the publications about ISFETs continued to consider V_t as the pH dependant parameter even for devices built in CMOS [2] [5] [6]. However, it is believed here that there is a more general way to present ISFETs and their chemical dependence especially those built in CMOS process.

For CMOS ISFETs, the topmost metal layer is covered by an insulating oxi-nitride passivation which may be further covered by an ion selective layer. This passivation, and any layers on top of it if exists, become the ion sensitive membrane. The chemical signal is capacitively coupled to the topmost metal, the chemical gate, via this ion sensing membrane. The chemical gate is connected to the floating gate of the intrinsic transistor. Thus, the electrolyte and its ions interact with the ion sensing membrane, that capacitively conveys the signal to the chemical gate which is part of the transistor's floating gate figure 3.3. There is no direct interaction between the intrinsic transistor and electrolyte. Therefore, it is proposed here to assume constant V_t for the intrinsic transistor part and see it no more than a floating gate MOSFET. The chemical signal is capacitively coupled through the passivation layer to the ion sensitive topmost metal layer. This is the input to the underlying floating gate transistor.

Thus, The CMOS ISFET analysis is divided here into two parts. The chemical voltage and the floating gate transistor 3.3. The first is related to all potentials between the reference electrode input and the outer surface of the ion sensing layer. It includes all electrolyte related potentials, to be presented next. The second part is just a normal floating gate transistor that was presented in chapter 2. The resultant of the first part is capacitively coupled to the floating gate of the second part. It forms its main input, other inputs are possible [15] [16] [17].

This separation has the advantage of generalising ISFET's analysis in the sense that it

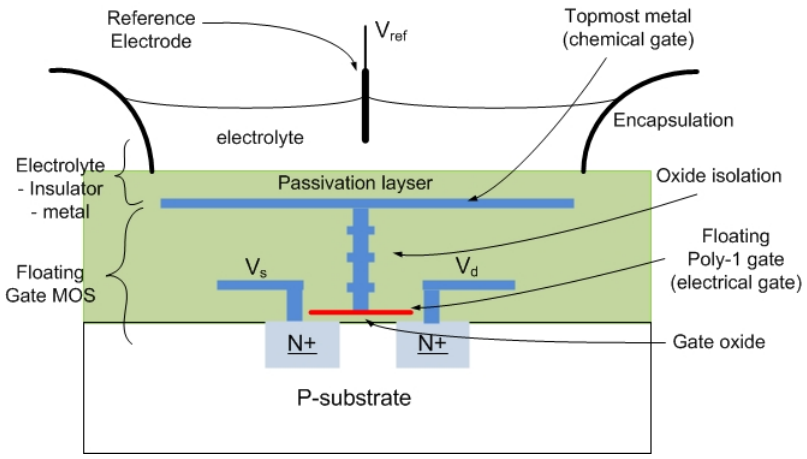

Figure 3.3: Cross section representation of an ISFET built in a standard CMOS process, not to scale.

makes a separation between the transistor part and the ion sensing part. Thus, more than one transistor may share the same chemical gate and more than one chemical gate may provide the input to the transistor part. It holds for a mixture of chemical and electrical inputs to the same floating gate. This way, ISFET circuits become more versatile. There in no more the attachment between one ion sensitive membrane and one transistor; which was physically the case of early devices. It remained as so for CMOS ISFETs only for historical reasons. This facilitates the explanation of the ISFET based chemical inverters to be presented in chapter 4.

The following presentation starts from the reference electrode followed by the electrolyte's impedance. Finally, electrolyte's interaction with the ion sensing membrane is depicted.

3.4.1 Reference electrode - electrolyte interface

One of the very important factors influencing ISFET sensor operation is the reference electrode. It was thought possible to operate ISFETs without reference electrodes re-

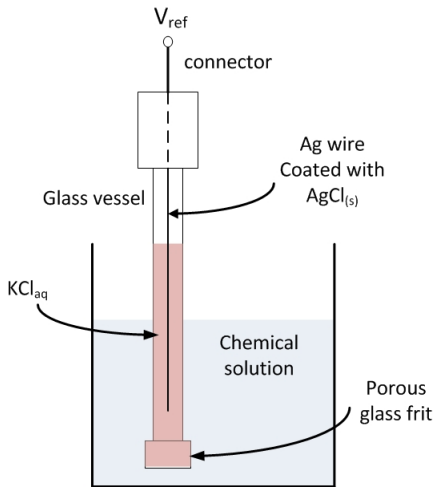

Figure 3.4: A representation of a Ag/AgCl reference electrode

lying on work function changes only [1]. However, that was experimentally proven insufficient for ISFETs accurate operation [5]. A well-defined electrical potential is needed in the chemical solution for accurate measurement of ion concentration changes [2]. The standard method to apply such potential is through a reference electrode.

Traditionally, Silver/Silver Chloride reference electrodes have been used, figure 3.4. It consists of three parts. First, a silver wire coated with silver chloride provides the input contact to receive the applied reference voltage. Second, a saturated chloride solution, normally potassium chloride (KCl), is the electrolyte that makes contact with the wire facilitating electron transfer according to the reaction:

$$AgCl_{(s)} \; + \; e^{-} \leftrightarrow Ag_{(s)} \; + \; Cl^{-}_{(aq)}$$

$AgCl$ will not be consumed in this reaction because the solution is saturated in Cl^{-} ions. This solution is confined within a glass tube. The third part is a porous glass frit. It provides electrical conduction between the confined chloride solution and the electrolyte under test without mixing the two solutions [18].

This is effectively, a silver chloride coated metal electrode in contact with a saturated solution of a soluble salt of its own cation. Thus, electron transfer between them provides a stable voltage reference with a very small potential drop that does not depend on ion concentration of the electrolyte under test. For the standard $Ag/AgCl$ reference electrode with $3.5M\ KCl$ filling solution, this potential drop is about $0.205V$ at $25°C$ [6]. This resulting potential is then conveyed through the porous glass frit to the solution to be tested with a small liquid junction potential of $3mV$ [5]. The most important advantage of this type of reference electrode is its stable potential drop that is independent of pH of the electrolyte under test.

In order to take full advantage of the integrated ISFETs systems, it would be desirable to build miniaturized reference electrodes. Two methods to realize this were reported. Suzuki et al. micro-machined a replica of the standard Ag/AgCl electrode in a silicon substrate [19]. They aimed at keeping the same advantages of the macro electrode while in the same time incorporating it in an IC. It would fit lab on a chip applications. However, even after improving it by Huang et al. in [20], the fabrication process was very complicated. It required the incorporation of KCL sample solution in a micro-chamber with a junction membrane. Of course, the resulting process was not CMOS compatible.

The second proposed method was based on using a noble metal as a pseudo-reference electrode. Platinum was proposed in [21] and a gold electrode in [22]. Such a noble metal was needed to make sure it does not react with the electrolyte under test. However, they had an interface potential that is pH dependant and had to be accounted for [23]. A solid state reference electrode made of iridium oxide was reported in [24]. It is particularly stable over a wide pH range and provides fast response. This layer may be deposited by electroplating. However, it is not standard CMOS processing step.

3.4.2 Electrolyte Impedance

The potential applied by the reference electrode appears in its vicinity at the electrolyte bulk with the small shift mentioned above. It sets this bulk potential. The model of electrolyte impedance is a parallel resistance and capacitance with their values highly dependant on its composition, used electrodes, and frequency domain [25]. However, because the flow of current needs two terminals to close the circuit, which does not exist for ISFETs. Only, negligible leakage current exists. Therefore, electrolyte's impedance contribution in the chemical voltage is ignored for the purposes this thesis [26] [27].

3.4.3 Insulator - Electrolyte Interface

The structure composed of the electrolyte - insulator - semiconductor (EIS) was extensively studied as it is responsible for the pH sensitivity in ISFETs and capacitive sensors [28] [14] [29] [30]. It is the subject here to lay the theory of EIS structures. Silicon oxide is used as an insulator example. The same analysis holds for other insulating material [31].

On the surface of oxides, like SiO_2, TiO_2 and Al_2O_3; there are groups that can dissociate [32]. That is, also, the case for silicon nitride, proteins, and many soluble polymers. For silicon oxide (SiO_2), these are $SiOH$ sites while they are $SiNH_2$ for silicon nitride. These groups are neutral when dry. But, when they interact with a water based electrolyte, they may accept or donate protons (H^+) depending on solution's pH. This produces either positively charged $SiOH_2^+$ and $SiNH_3^+$, or negatively charged (SiO^-) sites; figure 3.5 and equations 3.2 to 3.4 [2]. $SiNH_2$ may accept hydrogen ions bot may not donate them, which is different from the case of $SiOH$. Thus, it is possible for the originally neutral hydroxyl group site to become either positively or negatively charged. That is why it is called Amphoteric site. The following chemical reactions show this

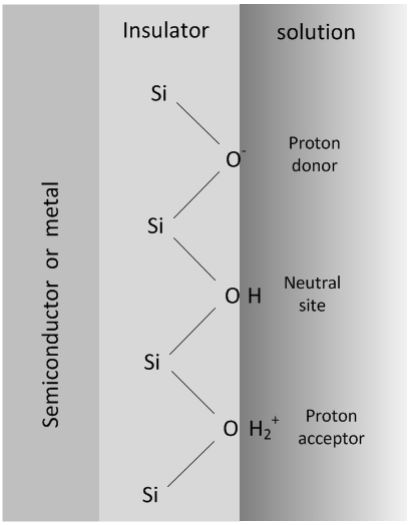

Figure 3.5: Surface sites at silicon oxide interface with electrolyte

process:

$$SiOH \iff SiO^- + H_B^+ \tag{3.2}$$

$$SiOH + H_B^+ \iff SiOH_2^+ \tag{3.3}$$

$$SiNH_3^+ \iff H_B^+ + SiNH_2 \tag{3.4}$$

The net result is a charged solid surface. This generates an electric field that attracts counter ions that forms a layer. These two layers of charged solid and oppositely charged ions are called“ electrical double layer“ [32]. It may be modelled at different levels of sophistication. Its simplest model is an ionic layer bound directly to the solid's surface to neutralize its charged layer, just like a two plate capacitor. The distance between the two plates being the molecular thickness. This is called Helmholtz double layer capacitance [31]. The solution's bulk after this double layer may be assumed neutral. This model looks to ions and molecules as point charges. However, alone, it fails to explain the capacitance of the electric double layer.

Seeking a better fit, Gouy and Chapman came with another model that treats the

solution as a continuous medium with a certain dielectric constant [18]. They considered the ions thermal motion as predicted by Poisson-Boltzmann theory. Dislike the simple theory above, they postulated thermal fluctuations to drive the counter ions away from the solid surface while electrically attracted to the charged solid surface. This forms a diffuse layer that further extends inside the solution. The molecular nature of the liquid was ignored and it was assumed a continuum of charges [25]. Thus, instead of the two plate capacitor case above, it suggested a capacitor that has one fixed plate at the solid surface. The second plate is at the first point where the electrolyte becomes neutral, the Debye length, which depends on the solution's pH [32]. The capacitance of this tow layer capacitor depends on the solution's ion concentration. This model had its own limitations, too.

Stern combined both models where the double layer is divided into two parts. An inner Helmholtz layer of immobile ions that are directly attracted to the surface. This neutralizes only part of the surface charge and has a constant capacitance. And a diffuse outer part consisting of the mobile ions according to the Gouy-Chapman model, figure 3.6. This neutralizes the rest of the solid surface charge. The transition point between the two models has a certain potential that is called the zeta potential [25]. Though, other models may better describe certain aspects of the double layer, this model generally explains most experimental observations and is widely accepted. It was adopted to explain pH related potentials in ISFETs [14].

The potential at the electrolyte bulk is zero as it is assumed neutral, for the moment. In order to find the potential at the solid insulator surface (ψ_0), the simplest case of one dissociable (hydroxyl) group is assumed. The dissociation constant (K) of a reaction in equilibrium is defined as the concentrations of its products divided by those of its

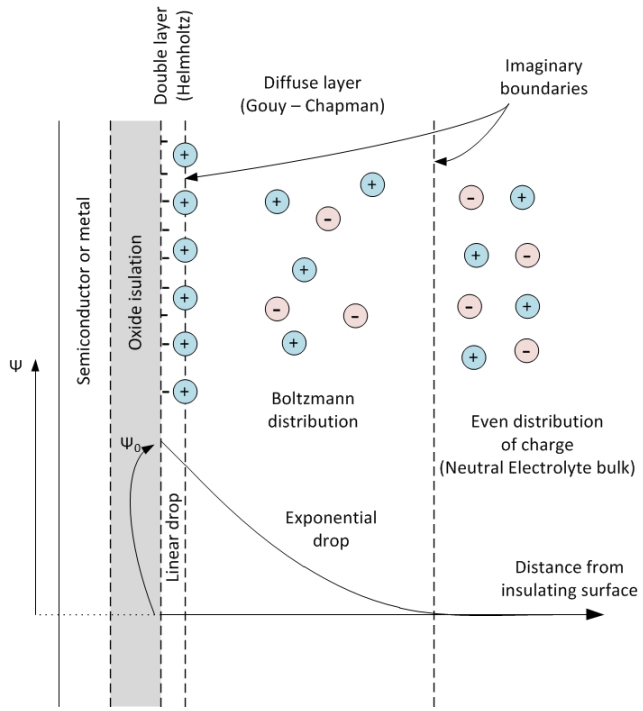

Figure 3.6: Potential distribution of insulator-electrolyte interface

reactants. According to the first reaction of equation 3.2, it will be:

$$K_{SiO} = \frac{[SiO^-][H^+]_S}{[SiOH]} \tag{3.5}$$

Where $[SiO^-]$ and $[SiOH]$ denote the concentration of the charged SiO^- and the neutral $SiOH$ in mol per unit surface area. $[H^+]_S$ stands for the proton concentration just in vicinity of the insulator surface. It is given in mol per unit volume. It can be different from the concentration in the bulk of the solution $[H^+]_B$. This is because the charged surface may attract or repel protons according to its polarity. They are related by Boltzmann distribution [32]:

$$[H^+]_S = [H^+]_B \; e^{-\frac{e\psi_0}{kT}} \tag{3.6}$$

where k is Boltzmann constant and T is absolute temperature. Using this in equation

Table 3.2: Sensing characteristics of some ISFETs' pH sensing membranes [6].

Characteristics	SiO_2	Si_3N_3	Al_2O_3	ZrO_2	Ta_2N_5
Range of pH measurement	4-10	1-13	1-13	0-8	2.5-13
Sensitivity (mV/pH)	25-46	46-563	53-56	50-56	55-57
Long term drift (mV/h, pH7)	unstable	1.0	0.8	0.2	0.5

3.5 and taking the logarithm of both sides gives:

$$\log K_{SiO} = \log\left(\frac{[SiO^-]}{[SiOH]}\right) + \log[H^+]_B - \frac{e\psi_0 \times \log e}{kT} \tag{3.7}$$

Since $pK_{SiO} = -\log[SiO^-]$ and $pH = -\log[H^+]$, the above equation becomes:

$$-pK_{SiO} = \log\left(\frac{[SiO^-]}{[SiOH]}\right) - pH - \frac{e\psi_0 \times \log e}{kT}$$

rearranging,

$$\psi_0 = \frac{1}{\log e}\,\frac{kT}{e}(pK_{SiO} - pH) + \frac{1}{\log e}\,\frac{kT}{e}\log\left(\frac{[SiO^-]}{[SiOH]}\right)$$

But, $kT/e = U_T$ is the thermal voltage. Using it and knowing that $1/\log e \approx 2.3$ give after re-ranging :

$$\psi_0 = 2.3U_T\ pK_{SiO} + 2.3U_T \log\left(\frac{[SiO^-]}{[SiOH]}\right) - 2.3U_T\ pH \tag{3.8}$$

Now, the pH sensitivity of the potential at the insulating surface may be found as:

$$\frac{\partial\psi_0}{\partial pH} = -2.3\ U_T\ pH \tag{3.9}$$

This derivation is a good first approximation but it is not thorough. The model needs to be extended to adopt more ions partially competing for binding cites. For example

H^+ and OH^- always exist in water based solutions. The basic idea remains the same. Moreover, the effect of ions' concentration on the double layer capacitance was ignored.

A more rigorous derivation in [33] and [2] showed that equation 3.8 may be corrected by the introduction of a dimensionless sensitivity parameter α, to be:

$$\psi_0 = 2.3U_T\ pK_{SiO} + 2.3U_T \log\left(\frac{[SiO^-]}{[SiOH]}\right) - 2.3\alpha U_T\ pH \tag{3.10}$$

The first two terms are not pH dependant. They are related to insulator material properties. Thus, the corrected pH sensitivity is given by:

$$\frac{\partial\psi_0}{\partial pH} = -2.3\ U_T\ \alpha\ pH \tag{3.11}$$

where

$$\alpha = \frac{1}{\frac{2.3U_TC_{diff}}{e\ \beta_{int}} + 1}$$

If $\alpha = 1$, equation 3.11 reduces to equation 3.9 and the sensitivity becomes the maximum possible sensitivity of $-59.2mV/pH$ at room temperature, $25\deg C$. It is known as the Nerstian sensitivity [2].

Different sensing membranes have different sensitivities. That is attributed to number of binding sites per square micron and the nature of reaction at these sites [1]. Table 3.2 lists measured sensitivities and measurement characteristics of a number of ion sensitive membranes.

Equation 3.10 suggests that zero potential at the solid surface (ψ_0) may be reached depending on the reaction and species concentration. For example, this occurs for pH in the range between 7.1 and 7.6 for silicon nitride in weak $NaNO_3$ solution, less than 0.1 M [25].

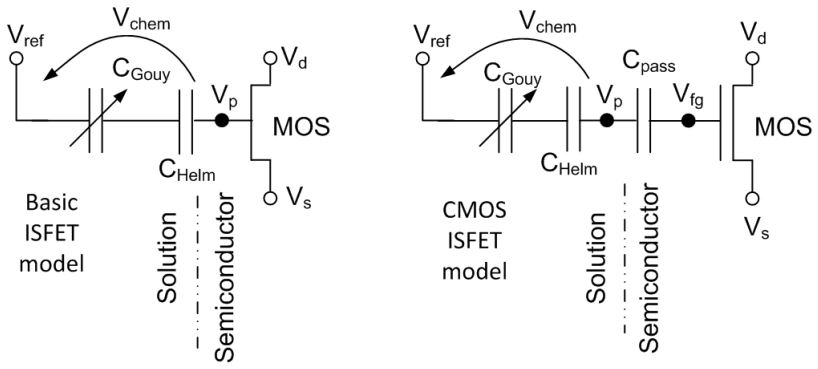

Figure 3.7: Model representation of a basic ISFET and an ISFET built in a standard CMOS process. $V_p = V_g$ in the former but not the latter.

Equation 3.10 gives the potential at the outer surface of the insulator in contact with the electrolyte when the potential at the solution's bulk is zero. The potential difference between the reference electrode input and the insulator outer surface is defined as the chemical voltage (V_{chem}) as seen by the passivation layer. It may be given by [1]:

$$V_{chem} = \gamma + 2.3U_T\alpha\ pH \tag{3.12}$$

Where, γ is a grouping of all pH independent terms including the small contact potential change between the reference electrode input and the solution's bulk. V_{chem} models the total voltage difference between the reference electrode input and the outer plate of the ion sensing membrane, which is the gate oxide in basic ISFET while it is the passivation insulator for the CMOS ISFET. Having found the chemical potential, it is time to model ISFETs.

3.5 ISFET model

The modelling of ISFETs generally starts with its analogy to MOS devices and its threshold dependence on pH [4]. A macro-model plug in for spice was proposed by

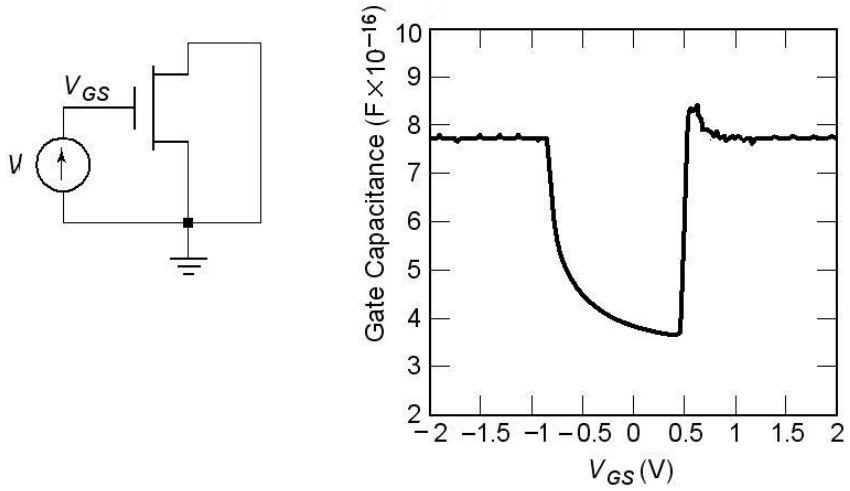

Figure 3.8: MOSFET gate-channel capacitance change with biasing, [36].

Massobrio et al [34]. It was later modified to fit general Spice based simulators without the need for a plug in software [35].

After the analysis presented above, ISEFTs may be modelled as shown in figure 3.7 for both the basic and CMOS cases. Here, the net voltage at the interface of the electrolyte and the ion sensing insulator (V_p) is the superposition of V_{ref} and V_{chem}.

$$V_p = V_{ref} + V_{chem}$$

As seen by the intrinsic transistor, this is the gate voltage in a basic ISFET

$$V_g = V_p$$

, while it is an input to the floating gate in a CMOS ISFET:

$$V_{fg} = \frac{C_{pass}}{C_T} V_p + \frac{C_{MOS}}{C_T} V_{MOS} + \frac{Q_{TC}}{C_T} \tag{3.13}$$

Where, all other terms have the same meanings as in chapter 2. $C_{MOS}V_{MOS} = C_{gs}V_s +$

$C_{gd}V_d + C_{gb}V_b$ is the contribution of MOS terminals to the floating gate voltage. It is important to note that C_{gb} depends on the region of operation with its maximum in cut-off and strong inversion [37] [36]. Its value reduces in weak inversion to about half that of strong inversion, figure3.8. Thus, the MOS contribution is not constant which may considered as a non-ideal behaviour. Moreover, C_{gb} variations, especially in weak inversion, may be a source of error in pH measurements.

C_T is the total capacitance seen by the floating gate:

$$C_T = C_{pass} + C_{gs} + C_{gd} + C_{gb}$$

A number of factors make it non-linear. First, C_{gb} is bias dependant. Second, process variations and mismatch affect all capacitances, particularly C_{pass}. Finally, there are coupling capacitances with the substrate and surrounding layers that are ignored here. However, if C_{pass} is made much larger than, for example 10 times, all other capacitances, C_T changes due to all other capacitors' variations is reduced. However, to do this C_{pass} area has to be very large simply because the passivation layer is very thick, around $2\mu m$ in total [38]. An area of $10,000\mu m^2$ is not abnormal [39]. The other way around such a high area is to exploit CMOS process to reduce passivation thickness on top of chemical gates by introducing a bond pad opening as was suggested in [40]. However, that technique has its limitation. The authors reported their devices to have higher $1/f$ noise and more drift which was explained by the sensitive area being the IMDs oxide. Moreover, normally, pad openings are over etched. In this case, they are not intended to stop on a metal layer, as is the case with normal pads. Thus, the chemical gate metal should be in a lower metal in the stack. In the above mentioned paper, it was in metal 1. This leaves very limited routing options for other circuit elements under the chemical gate.

3.6 Non ideal ISFET properties

ISFETs, as chemical sensors, have been reported to have a number of non-ideal properties. Namely: drift, hysteresis, light sensitivity, temperature dependence, and limited lifetime [41]. The good news is that there has been increasingly better understanding and modelling of these problems in order to deal with them. In the following is a presentation of these problems.

Drift

Drift is temporal change in the output of an ISFET under constant conditions of biasing, V_{ref}, pH, and environment. It is one of the most important problems with ISFETs. It is generally unidirectional, but may reverse direction [26]. That is why its origin and mechanism has been controversial.

Generally, if the ion exchange current density at the interface where the analytical signal is generated is low ($< 1nA/cm^2$), then it is assumed high impedance. Thus, the interface potential would drift due to adsorption of ionic species and electrolyte motion [42]. This is the case with ISFETs. Drift was explained by several phenomena including ion migration within the gate insulator, slow surface effects and hydration of the insulator surface [43]. It was also understood to be due to mobile ionic charges in the ion sensitive membrane [44] and [27]. This was supported by a recent study by Kwon et al in [45]. They studied the high V_{ref} effect on ISFET's threshold voltage. They found that applying a large positive V_{ref} shifts V_t in one direction and applying a similarly large negative value shifts it in the opposite direction. While doing the same thing on an identical MOS does not much change its V_t.

ISFET's transient response due to a step change in pH was shown experimentally to

be composed of three phases: fast, slow and baseline drift [46]. The largest part is the fast response, which is a result of the interface reaction at the surface cites. It accounts for about 90% of the expected response and is very fast. It was, lately shown to take less than a milli second [47]. It constitutes the chemical signal of interest. The slow response is much smaller in magnitude and takes few hours to finalize. It is correlated to the insulator's surface binding sites reducing its sensitivity [48]. Thus, etching away few nano meters of the passivation may restore the original sensitivity of ISFET [49]. Finally, a base line drift is a temporal shift of the output under constant conditions of temperature, pH value, and biasing. This drift has a very long time constant that spans the device's life time [50]. Practically, a "burn in" period of a number of hours while exposing the ISFET to solution usually minimises the shorter time constant effects. Thus, only baseline drift remains in effect.

There have been different ways to deal with drift. A straight forward way would be just to calibrate the ISFET before measurement. For continuous measurements, frequent calibration would be needed [2]. But this can be tediously difficult especially if two point calibration is used [1].

In [51], Jamasb et al. proposed an analytical technique based on modelling drift and then numerically compensating for it [52]. He modelled it by a relation of the form A/f^n, where A and n are fitting constants. For the devices he measured, these were $A = 8.665 \times 10^{-13}$ and $n = 1.154$ [53]. He experimentally showed how this method can reduce the effect of drift on pH measurements.

Liu, in [17], proposed an ingenious method based on auto-zeroing amplifier. Two nodes were capacitively coupled to the ISFET's floating gate. One reads its level and stores it in a capacitor and the other is used for sensing. The difference between the sense node and the stored level is amplified to give the output. At low frequencies, this circuit suffered from storage capacitor leakage. Moreover, during the reference reading, it is not

possible to simultaneously get an output. He further improved this method in [16], where two auto-zeroing circuits continuously output the pH value using a pin-pong method. That is one gives valid output while the other reads its reference. Another method was described in [26], where a chemical sigma delta modulation was proposed. The chemical solution was incorporated in the feedback loop between the titrating and the counter electrodes. The reference electrode was foxed at a constant voltage. Grounding was chosen. This way it was possible to actively compensate for drift.

Hysteresis

The slow response and baseline drift of ISFETs, mentioned above, cause hysteresis [50]. This transient response, both in terms of drift and hysteresis was shown to depend on the material of the ion sensing membrane and its deposition method, table 3.2. Bousse et al compared them for different materials. They found Al_2O_3 and Ta_2O_5 membranes to exhibit lower drift and hysteresis than Si_3N_4 [54].

Temperature Sensitivity

The temperature sensitivity of ISFETs is the superposition of three temperature dependencies. Namely, reference electrode potential drop, the intrinsic MOS threshold voltage temperature coefficient, and the electrolyte-insulator potential temperature dependence [2]. The reference electrode temperature dependence was estimated to be about $150\mu V/^{\circ}C$ [55]. The electrolyte/insulator potential temperature dependence is evident from equation 3.10. It is expressed by the thermal potential which is much higher than the reference electrode case. Thus, the latter can safely be ignored.

The intrinsic transistor term is not part of the chemical voltage. It is included in the floating gate model adopted here. Its temperature dependence stems from MOS

standard parameters, namely carrier mobility μ, intrinsic carrier concentration, and band-gap energy [8].

Trapped Charges

In CMOS ISFETs, trapped charges during fabrication process may exist in the passivation layer, floating gate, or its insulation layers. Because, the poly-silicon gate becomes floating once it is formed, any charges in it will remain trapped. Bausells et al reported a threshold variation between $-7V$ to $+6V$ in their n-channel ISFETS [28]. Similarly, Hammond et al measured a threshold variation between $-33V$ to $-8V$ for their p-channel ISFETs [23]. A number of methods to tackle this problem were reported. They will be reviewed in chapter 6 where yet another method is proposed.

Lifetime

Generally, lifetime of ISFETs is limited by encapsulation breakdown which leads to corrosion of bond wires. Another mechanism is degradation of the insulating membrane which can cause loss of sensitivity [6]. Due to ageing effects, the time response of ISFETs have been shown to slow down from few seconds to several tens of seconds [5]. This is of major importance for devices to be used for in-vivo systems. However, it is not an issue for disposable devices.

Light Sensitivity

ISFETs are sensitive to optical light radiations, just the same way MOSFETs are. A threshold shift of about $50mV$ was reported in n-channel devices due to switching ambient light on and off [56]. This can easily be understood as photo-diode behaviour

of the source and drain n-doped regions [5]. Generally, visible light energy is of similar range to the band gab energy on n-doped regions. Thus, it may excite electrons to the conduction band. Moreover, the passivation layer is transparent ot these wave lengths. This problem may be solved by taking preventive measures to stop light from reaching these regions. For example, in layout, metal stack may be used to shield light from reaching the substrate. Another method may use system packaging to stop light from reaching ISFETs.

Process variation and mismatch

Being MOS devices, ISFETs are subject to process and lithography variations along side device mismatch. Generally, the former is long distance while the latter is short distance within a wafer. They are process dependant but design may be used to reduce their affect [57]. Pelgrom et studied this problem and modelled mismatch of a MOS parameter "p" by [58]:

$$\sigma_p = \frac{A_p}{\sqrt{WL}}$$

where σ_p is the standard deviation of the parameter, A_p is a fitting constant and WL is the transistor's gate area.

As part of the process characterisation, fabrication foundries measure mismatch between their devices and report these fitting constants for different parameters [38]. Mismatch and process variations can be simulated using Monte Carlo analysis option available in Spice based simulators like Cadence [36].

3.7 Noise in ISFETs

The physical limit of sensitivity and resolution of any sensor is imposed by its noise and sensitivity [6]. ISFETs are not an exception. Being floating gate transistor based devices, ISFETs have similar noise sources as their intrinsic transistors. At the same time their is noise originating from its chemical interaction nature. The first was extensively studied and it is well modelled. However, the second is still in the formulation stage, though it received a lot of effort.

The most important noise sources in MOS transistors are thermal noise and flicker noise. The former is due to thermal excitation of charge carriers. It depends on resistance and temperature but not frequency. By contrary, flicker noise is inversely proportional to frequency. Hence, it is also named $1/f$ noise. It is mainly caused by channel energy band traps that randomly capture carriers and release them. This disturbs the current flow and reduces as frequency increases [8]. There is an additional noise source in ISFETs, the chemical noise that arises from electrolyte interactions with both the reference electrode and the ion sensing membrane. Thus, ISFET's noise referred to its floating gate may be found as the sum of thermal noise, flicker noise, and chemical noise [5]:

$$\overline{V_n}^2_{ISFET} = \overline{V_n}^2_{MOSFET} + \overline{V_n}^2_{Chem} \tag{3.14}$$

In saturation, thermal noise of the channel is given by [59]:

$$\bar{i}_d^2 = 4kT\frac{2}{3}g_m \tag{3.15}$$

While, in sub-threshold, it is given by [59],

$$\bar{i}_d^2 = 2qI_{ds} \tag{3.16}$$

where, k is Boltzmann constant, T is absolute temperature, and g_m is the intrinsic MOSFET's transconductance. MOS flicker noise is modelled by:

$$\overline{V}_g^2(f) = \frac{K_f}{WLC_{ox}f} \tag{3.17}$$

K_f is a technology dependant flicker noise constant, W and L are the width and length of the device's gate, C_{ox} is the gate capacitance, and f is the frequency.

From chemical side; noise sources are understood to include inter-facial ion transport at the reference electrode, and partial ionic currents due to different charged species contributing to the total current [42]. Also, dispersive transport at the electrolyte-insulator interface resulting from non-uniform spatial distribution of traps and their associated energy levels cause chemical noise [49]. This type of noise is manifested as drift, which is one of the ISFET non ideal behaviours mentioned above.

First experimental data on chemical noise of ISFETs were reported by Haimerli et al in [60]. They proposed an empirical model consisting of low pass filters with a number of break points. Barabash et al proposed a theoretical model based on ion transfer and electrolyte/oxide interaction [55]. It made use of site binding theory, electrochemical equilibrium equations, and reaction rate relations. Their model was in the form of network of resistors and capacitors but it was not backed up with experimental results.

More than a decade later, Jakobson et al, conducted experimental measurements of noise in commercially available ISFETs from Sentron [59]. These devices were manufactured with a special process with aspect ration of $W/L = 600\mu m/20\mu m$. They were basic ISFETs with no poly-silicon gates. Al_2O_3 was used as the gate insulator. Noise was measured for frequencies between $1Hz$ and $100KHz$. It was found that MOSFET 1/f noise was the dominant noise source especially at lower frequencies. It was proportional to I_d in saturation while it increases as a function of I_d^2 in the sub-threshold region.

No pH dependence of noise was observed. Though Jakobson reported drift, he did not mention how it was dealt with.

Jamasb et al modelled drift in ISFETs with Al_2O_3 and LPECVD Si_3N_4 insulators [43]. It was found to be uni-directional. Later, he measured noise in ISFETs. It was experimentally shown that drift masks all other sources of noise in an ISFET with Si_3N_4 ion sensing membrane, including electrical noise [52]. In order to measure the effect of other noise sources, he used drift analytical model to numerically compensate for drift in order to measure $1/f$ noise of his ISFETs [51]. He found that, after compensating for drift; $1/f$ noise dominates other sources of noise except for frequencies less than $10Hz$ where drift prevailed [61].

Palan, in his PhD thesis, tested commercial ISFETs, similar to those measured by Jakobson [5]. He produced similar results which confirms Jacobson's findings. He also measured $1/f$ noise in nMOS transistors and identical ISFETs built in CMOS process with chemical gates of the same size as the electrical gates. Some devices had Si_xN_y passivation as their ion sensitive membrane while others had SiO_2. He used MOS simulated $1/f$ noise as a reference. He found that, measured $1/f$ noise of MOSFETs were one order of magnitude larger than their simulations for the range from $1Hz$ to $100KHz$. However, identical ISFETs were around 1.5 times higher than simulations. $1/f$ noise dominated ISFET behaviour at low frequencies while thermal noise took over at higher frequencies. The corner frequency, where both noises were equal, ranged between $200Hz$ and $8KHz$ [5]. Interestingly, Palan noticed that noise was proportional to $1/f^2$ in some devices for frequencies lower than $10Hz$. He attributed that to drift and not chemical noise. This makes sense especially if compared with results of [61].

This is in agreement with Mr. Liu, who studied $1/f$ noise in CMOS ISFETs with different chemical and electrical gate area combinations in [26]. Focusing on frequencies lower than $1Hz$, he modelled chemical noise, referred to V_{ref}, in a similar fashion to

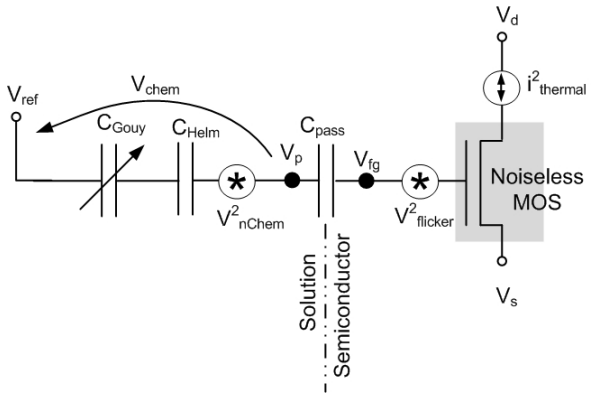

Figure 3.9: A macro-model of an ISFET showing its noise sources.

flicker noise as [26]:

$$\overline{V_{nChem}}^2 = \frac{K_{chem}}{f} \tag{3.18}$$

Thus, Liu included drift as part of ISFET noise and gave it $1/f$ dependence. He remarked that generally chemical noise dominates in this range of frequencies. Moreover, based on an empirical observation of minimum noise of $1nV/Hz$, he concluded that overall drift of less than $5mV/h$ is very challenging for oxi-nitride passivation ion sensitive membrane ISFETs.

To sum-up, generally, researchers agreed on $1/f$ chemical noise model. Thus, noise in ISFETs may be modelled as [6]:

$$\overline{V_{nISFET}}^2 = \frac{8kT}{3g_m} + \frac{K_f}{WLC_{ox}f} + \frac{K_{chem}}{f} \tag{3.19}$$

That is for basic ISFET's, where V_p is in the same time V_g, figure 3.7. However, for ISFETs built in CMOS, like the FG-MOS case, capacitive coupling should be taken into account. Ignoring the transistor's term in equation 3.13, and assuming no trapped charges, the intrinsic gate's noise spectral density ($\bar{V}_g^2$) as referred to the reference

voltage will be scaled [62] as:

$$\frac{\overline{V}_{ref}^2}{\Delta f} = \frac{C_T}{C_{pass}} \frac{\overline{V}_{fg}^2}{\Delta f} \tag{3.20}$$

Thus, CMOS ISFET's noise referred to V_{ref} may be written as:

$$\overline{V_{nISFET}}^2 = \frac{C_T}{C_{pass}} \frac{8kT}{3g_m} + \frac{C_T}{C_{pass}} \frac{K_f}{WLC_{ox}f} + \frac{K_{chem}}{f} \tag{3.21}$$

Therefore, V_{ref} will see a scaled version of the MOSFET noise. This was the reason of Liu observation that total noise increases with decreasing chemical gate area for the same electrical gate area [26]. A macro model of an ISFET showing these noise sources is depicted in figure 3.9.

Rewriting equation 3.21 with all noise terms referred to the floating gate, it becomes:

$$\overline{V_{nISFET}}^2 = \frac{8kT}{3g_m} + \frac{K_f}{WLC_{ox}f} + \frac{C_{pass}}{C_T} \frac{K_{chem}}{f} \tag{3.22}$$

Noise is the fundamental limit for signal detection. Thus, it is important to maximise the signal to noise ratio (SNR). Equation 3.21 depicts noise as seen where the chemical signal is generated. Clearly, using frequencies higher than an ISFET corner frequency would reduce the total noise [5]. Also, design may be used to reduce flicker noise. Increasing chemical gate may exhibit similar behaviour with respect to chemical $1/f$ noise, but this needs further investigation as it was not established by researchers, yet. Operating the ISFET in the low power sub-threshold mode would reduce its thermal noise. Optimally, a combination of these factors may be used. One way to maximise signal to noise ratio is by amplifying the ISFET's output early in the signal processing chain, at the point of detection, in order to reduce further noise sources effects. This is one target of this work that will be depicted in the chapters to come.

3.8 ISFET Interfacing circuits

Nature is analogue. Electronics in general and ISFETs in particular are no exception. Almost all previous work on ISFETs used them in the analogue form apart from [63] and [64] which will be discussed in details in chapter 4.

As a transistor based device, it may be biased in saturation, triode, or sub-threshold/weak inversion. Its floating gate voltage relation to its drain current is given by equation 3.1. Basically, ISFETs are used with the aim to measure pH or ion concentration changes. This may be done by one of two methods: constant charge or constant potential [4].

In the first method, a constant interfacing charge at the ion sensitive membrane is maintained. That may be done by fixing the drain current and drain source voltage. V_{chem} will cause a change in I_d, which is opposed by a feedback circuit to keep it constant. Thus, V_{ref} has to change to compensate for V_{chem} in order to keep constant I_d [6]. This is a linear relation with a unity slope.

By the second method, the interface circuit maintains both V_{ref} and V_{ds} constant. V_{chem} change is monitored through I_d, which provides an amplification by g_m. In this case, I_d is linearly related to V_{chem} and pH when the transistor is biased in strong inversion [65]. It is linearly proportional to concentration (not pH) if biased in weak inversion [66]. I_d may be used in current mode circuits or converted to voltage for normal voltage mode processing.

3.9 ISFET Applications

ISFETs were basically introduced with the intention to use them in biomedical applications [3]. They found use in other industries and fields. Here is a look at some of these

uses.

First ISFETs were developed for *in vivo* sensing for the heart pace maker [3]. The first commercial application was a catheter for in *vivo* continuous measurement of blood pH [2]. It showed how blood pH is affected by breathing, which was otherwise not measurable. A diagnostic capsule using ISFETs to continuously measure pH and wirelessly report its value was proposed in [67]. An electronic tongue system using ISFETs was proposed in [68].

Applying an enzyme-entrapping membrane on top of the ISFET's chemical gate insulator makes it sensitive to the particular enzyme targeted by the applied membrane. For example protamine was deposited to make the ISFET sensitive to heparin [2]. By this method, suitable enzymes were used to make ISFETs sensitive to glucose [69], Urea and creatinine [70] concentrations. Using ISFETs as glucose sensors, a system was proposed that mimics the operation of beta cells of the Pancreas [65]. This may be used in a closed loop system to control insulin injection to type I diabetic patients [71]. This is a nice example of using silicon based electronic systems to mimic the behavioural dynamics of biological systems using transducers as part of the control loop.

One of the hot uses of ISFETs is in the label free Deoxyribonucleic acid (DNA) sequencing [3]. Basically, during primer extension reaction, base pairs are incorporated in a chemical process that releases H^+ ions, which reduces pH of the reaction solution. This is detectable using ISFETs. This idea was first introduced in [72]. Then, it was adopted by a number of researchers around the world. Fabricating ISFETs in CMOS facilitates making arrays with preprocessing in the same chip. A number of lab on a chip examples were reported that use arrays of ISFETs for the purpose of DNA sequencing [73]. A desk top laboratory machine that uses this idea to sequence human genome, in the shortest possible time yet, was reported in [74]. A combined magnetic, optical and pH techniques were used for lab on chip applications in [75] and [76].

Single-nucleotide polymorphism (SNPs) are certain short DNA sequences that have a single nucleic acid difference from the norm. They may be associated with certain diseases or drug metabolism [71]. Thus, the detection of certain SNPs in patients may help detect susceptibility to some diseases and/or their reaction to certain medications. SNPs detection is basically sequencing of very short fragments of DNA. The output may be expressed in the form of a yes/no answer for the sought sequence. This may represent a basis for a form of logic that tells if a SNPs is present or not. DNA logic was proposed in [63] and [64]. These two proposed circuits will be further discussed later.

ISFET sensors have been commercially used to measure pH of cheese and meat [1]. These solid state sensors were safer than glass based electrodes as they do not break [3]. Similarly, water quality may be measured using ISFETs to measure its pH and ion concentrations [77]. It helps decide whether water is suitable for drinking or not [78]. ISFETs may be incorporated in wireless systems for on-line monitoring of pH and certain ion concentrations in water processing plants [79].

Paint industries were one of the fields were ISFETs were used to monitor pH of used materials [3]. In order to control irrigation and fertilizer usage in agriculture, pH and concentration of some ions, like Ca^{2+}, K^{+} and NO_3^{-}; need to be measured. Traditionally, after sample extraction, the concentration of these ions was measured in the lab using expensive techniques like absorption spectrometry, molecular emission spectrometry, and chromatographic analysis [80]. ISFETs may be used for, in the field, real time continuous monitoring of these ions concentration. It has the advantage of being solid state. Thus it may just stick in the soil and measure [81].

3.10 Conclusion

This chapter reviewed early ISFETs and those built in a standard CMOS along with their models. The former was a normal transistor with its poly-silicon gate replaced by an electrolyte and a reference electrode. The latter was presented as a floating gate transistor with its input being the superposition of the reference voltage and chemical voltage. Both coupled to its floating gate via the passivation capacitance. Both have the same mechanism for the chemical potential. It was presented. ISFET's noise and non-ideal behaviours were briefed along with examples of its applications.

It may be noticed that an ISFET, both with and without a poly-silicon gate, always had its own ion sensitive membrane. It would be interesting to investigate their behaviour if two devices are allowed to share the same ion sensing membrane. A simple example would be an inverter. This will be the subject of the next chapter.

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Chapter 4

The ISFET based chemical switch

4.1 Introduction

Generally, ISFETs were built for continuous time (analogue) measurements with analogue pre-processing circuits around them. This enables continuous real time monitoring of pH or chemical concentrations. Analogue to digital conversion (ADC) are normally one processing block in most practical systems. All signal processing and decision making circuitry is normally done in digital building blocks that use the output of the analogue to digital converters.

However, for some applications analogue detailed information is not needed. What is relevant is whether pH change is larger than a certain threshold or not. For example in DNA application, the question of interest is: did hybridization take place or not. For other applications, all needed information is to find whether a chemical concentration, or pH , is above or below a certain threshold or not. More examples were presented in chapter 1.

The earlier the digital conversion of the sensed chemical signal is done, the less degra-

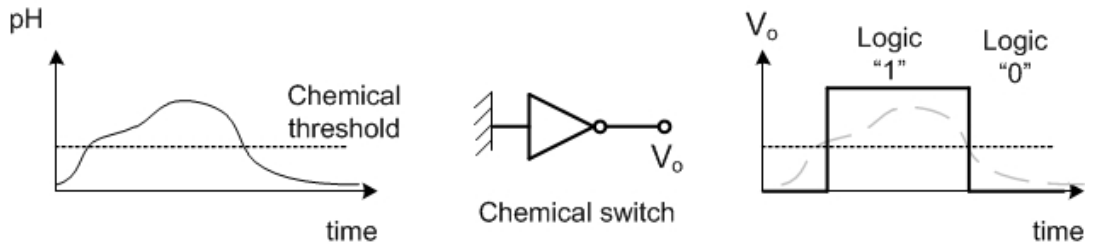


Figure 4.1: Chemical switch inputs a chemical analogue signal and outputs a digital electrical signal.

dation and interference it may be subjected to. Simply because analogue data is more susceptible to all types of electrical noise and interference, while digital signals enjoy better noise immunity and, hence, less affected by interference. Using fully digital CMOS integrated ISFET circuits makes it possible to harvest all the advantages of digital CMOS processing and operation to the full extent. This brings with it cheap mass production, scalability, and complete system integration.

In order to exploit ISFETs in the digital domain, one should start with the most basic building block that is an inverter. Building a digital chemical switch that changes state when a pH threshold is crossed will have a great impact on ISFET based sensory systems, figure 4.1. Successful implementation of a pH driven inverter opens the door for fast solid state threshold detection. It also makes it possible to build fully digital sensor arrays that include localized digital signal processing. It facilitates fully digital lab on a chip applications.

It is the subject of this chapter to draw on the analogy of ISFETs with floating gate MOS transistors extending the FG inverter to an ISFET based chemical switch. The fundamental motivation here is to produce discrete output from an analogue chemical signal. Proving the concept, it is possible to extend it to reduced transistor sizes. Previous attempts of other researchers towards a chemical inverter is discussed in the next section. In section 3, the operation of the FG inverter is presented. It is extended

to its ISFET counter part in section 4. Both normal strong inversion and low power sub-threshold operations are presented. Measurements and observations are discussed within relevant sections.

4.2 Previously reported chemical inverters

DNA sequencing prompted the research into first ISFET based chemical inverters [1]. Simply because, the process of DNA hybridisation generates protons in the reaction solution which lowers its pH. This was proven detectable using ISFET circuits [2]. Such amount of pH change depends on the ISFET sensitivity, buffer capacity, and the number of released protons; which in turn depends on the available DNA sample and its amplification. The last two are non electrical variables that are chosen as part of the whole sequencing operation. One example of sequencing system was published in [3]. It did not disclose the used buffer capacity, however it mentioned that $800K$ copies of the sequenced DNA is used. They produce a pH change of 0.02 units per nucleotide incorporation. This was reported to give a very poor SNR ratio that had to be signal processed, averaged, and fitted to a physical model in order to reach their acceptable SNR limit of 10.

This value of pH change was an example for that particular case. The pH change may be increased by decreasing the reaction buffer capacity. Another way is to increase the DNA sample size. However, both are beyond the purposes of this work. The bottom line for the aim of this work is to aim at measuring small pH changes where 0.02 units may be used as a guideline but not a limit.

Considering Drift and trapped charges, the above reported paper dealt with them in an elegant way. For each pixel, two measurements are taken per reading within $4ms$ time window. Which is the time needed to flush the sensor with a reference buffer, apply

new nucleotide, and incorporation taking place making solution ready for measurement. Therefore, due to such frequent calibration, both drift and trapped charges may be accounted for.

However, all what matters in these reactions is to detect whether hybridisation took place or not. Equivalently, it is desirable to detect whether pH of the reaction solution reduced or not. It would be of interest to build a simple, small, and robust circuit to detect this. There is no need to go through all the hassle of exact analogue measurements, A/D conversion, then using digital data for yes/no type decision making. Here, researchers thought about a simple circuit, a chemical inverter.

The first attempt to use an ISFET to build an inverter was by Dr. Shepherd and her colleagues who used the notion of ISFET based DNA logic [4] [1]. The aim was to use an ISFET to build basic digital circuit units that output a truth-table from DNA sensing operations [1].

With discrete devices in hand, they gave an n-type ISFET the role of the nMOS in a standard class AB inverting amplifier with the pMOS role taken by a normal transistor, figure 4.2. In their simulations, the input was connected to both: the gate of the pMOS (M2) and the reference electrode of the nISFET (X1). They explained how the electrolyte concentration affected V_t of the nISFET while the pMOS had constant threshold voltage. Therefore, the switching threshold of the circuit shifted in proportion to the solution‘s pH. It was reported that, according to simulations, it is possible to detect switching threshold changes due to a pH shift as little as 0.3 units.

Using similar terminology a DNA logic NOR gate was also simulated. Two reaction chambers were assumed to represent two chemical inputs to that gate. Two pull down n-type ISFETs and two pull up p-type MOS transistors completed the standard CMOS NOR gate.

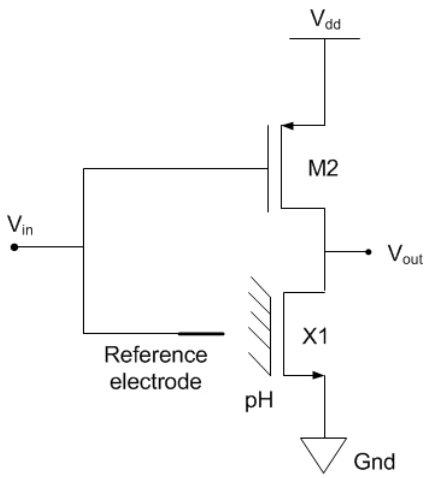


Figure 4.2: Schematic of the DNA logic inverter from [1]

As it is possible to operate the circuit in both low power weak inversion or normal strong inversion mode. The former was assumed in the analysis part of that paper, while simulation results showed strong inversion case. V_{dd} of the plots was either $2.5V$ or $2.0V$ and switching threshold voltages were in the range of $1.14 - 1.34V$. ISFET's non idealities were ignored.

The adopted terminology in this thesis is that V_t of the intrinsic MOS is fixed while the combination of V_{ref} and V_{chem} modulates V_{fg} of the ISFET. Consequently, pH changes modulated the gate voltage of the nMOS but not the pMOS of the above proposed inverter. That is only half of the complementary pair being pH sensitive. Thus, that circuit is not balanced in the sense that pull up transistor sees a different input than pull down transistor, the difference being V_{chem} plus the shift due to trapped charges. Nevertheless, it works in simulation. Results show how this is enough to detect the signals of interest.

However, that simulation did not account for the ISFET's drift nor its floating gate trapped charges. The major drawback of that circuit is ignoring these two factors, which can be large in ISFETs built with standard CMOS processes. They can render

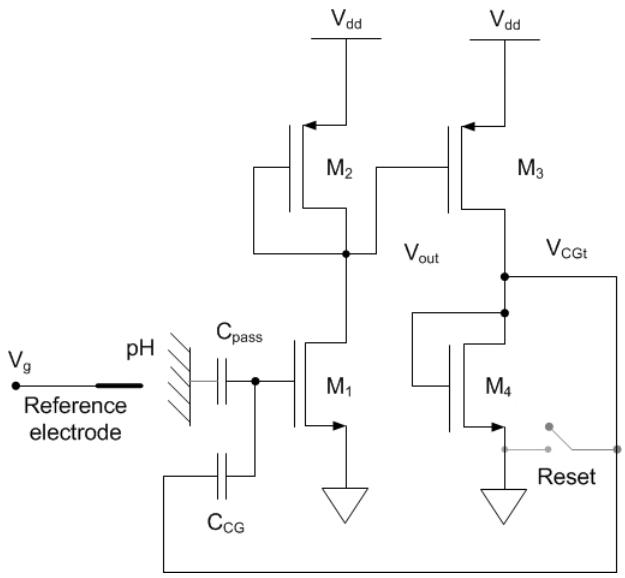


Figure 4.3: Schematic of the PG-ISFET DNA logic inverter from [5]

its switching functionality un-operational. Especially if the nISFET, due to trapped charges, had a negative or a large positive V_{fg} shift, that causes both transistors to be "on" or "off" in the same time.

Another circuit was proposed by W. Wong et al [5]. They used a programmable gate ISFET in an inverting single stage amplifier with its output fed to a second stage that is used to form a local feedback loop, figure 4.3. With this feed back action, and with proper transistor sizing, the first stage output switched when ramping the reference voltage. That paper reported minimum detectable pH change of 0.1 units.

However, that circuit did not have full inverter functionality. As it did not switch back if the reference voltage was reduced lower than the circuit's switching threshold. A reset is needed.

Both realizations of the chemical inverter used large transistor sizes. In the circuit of figure 4.2 the used aspect ratios were $50\mu m/50\mu m$ for the ISFET and $50\mu m/10\mu m$ for the pMOS [1]. The second circuit used aspect ratios of $10\mu m/10\mu m$ for M2 and M4

while it was $200\mu m/0.5\mu m$ for M1 and M3 [5]. These transistor sizes are not the only possibility for these circuits. However, as presented, these are large transistors consuming large silicon area and may drive relatively large currents compared to similarly biased smaller devices.

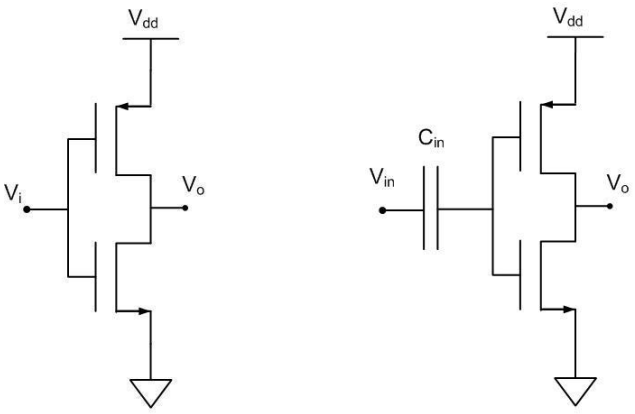
In the coarse of this thesis, the idea of chemical switching was adopted with ISFETs being the chemical to electrical signal transducers. According to the view of ISFETs as floating gate devices, it is possible to use concepts from the well established floating gate transistor technology. Following is a presentation of the floating gate inverter followed by extending the idea to ISFETs.

4.3 The Floating Gate Inverter

The starting point here is the well known CMOS inverter, figure 4.4a. The FG inverter is a simple extension of it where the input is capacitively coupled via an input capacitance to the two connected gates that are kept floating. Thus, it is composed of floating gate nMOS and pMOS transistors in an open loop class AB inverting amplifier as shown schematically in figure 4.4b. The single input (V_{in}) is capacitively coupled to their common floating gate by the input capacitance (C_{in}).

4.3.1 CMOS inverter review

Being the basic building block of digital circuits, the CMOS inverter is generally presented in this context. However, its transient analogue behaviour cannot be ignored especially when dealing with analogue signals input.



(a) MOS inverter (b) FG inverter

Figure 4.4: Schematic of MOS and a single input floating gate inverters.

The Switching Point

The switching threshold voltage (V_{sth}) of the CMOS inverter is the point where the input voltage (V_i) equals the output voltage, $V_i = V_o$. Thus $V_{gs} = V_{ds}$ for both transistors. This means, during switching, both, when in the normal strong inversion region, are in saturation. Assuming no load current, both transistors have equal currents. By solving for this point, it may be found, for strong inversion [6] or weak inversion [1] to be:

$$V_{sth} = \begin{cases} \frac{r(V_{dd}-|V_{tp}|)+V_{tn}}{1+r} & \text{Normal strong inversion} \\ \\ \frac{V_{dd}-|V_{tp}|+ln\left(\frac{I_{sn}}{I_{sp}}\right)V_{tn}}{1+ln\left(\frac{I_{sn}}{I_{sp}}\right)} & \text{Weak inversion} \end{cases} \tag{4.1}$$

Where

$$r = \sqrt{\frac{k_p}{k_n}} \quad , \quad k_n = \mu_n \times C_{ox} \quad and \quad k_p = \mu_p \times C_{ox}$$

Here, I_{sn} and I_{sp} are the specific currents of the nMOS and pMOS transistors respectively. V_{tn} and V_{tp} are threshold voltages while k_n and k_p are the process transconduc-

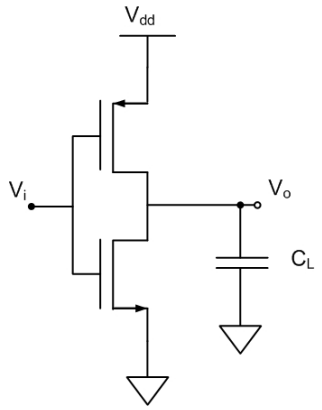


Figure 4.5: Schematic of MOS inverters with load capacitance.

tance parameters of the nMOS and pMOS transistors. μ_n and μ_p are the electron and hole mobilities while C_{ox} is the gate oxide capacitance [6].

This switching threshold voltages for both strong and weak inversion depend only on MOS parameters and the rail voltage. Switching occurs when V_{in} changes across V_{sth} going higher or lower than it.

During switching, the transistor's region of operation is dictated by its gate voltage V_g, for a grounded source, in relation to its V_t. The transistor is in moderate inversion around the point $V_g \approx V_t + 70mV$ [7]. It is assumed in weak inversion for lower V_g and assumed in strong inversion for higher V_g. The manufactured devices used in this thesis were in the $0.35\mu m$ technology of Austriamicrosystems. In this process, nMOS has $V_{tn} = 0.59 \pm 0.1V$ and for the pMOS it is $V_{tp} = -0.72 \pm 0.1V$. Therefore, the nMOS transistor would be in weak inversion if $V_i \leq V_{tn} + 0.07 = 0.66 \pm 0.1$ V. Otherwise, it would be in a different region of operation. Similarly, for the circuit in hand, the pMOS would be in weak inversion if $(V_{dd} - V_i) \leq |V_{tp}| + 0.07 = 0.79 \pm 0.1$ V.

Thus, because only two transistors, an nMOS and a pMOS, span the rails for the inverter, the region of operation during switching is decided by V_{dd} and their properties. Current flows in the circuit only during switching otherwise at least one of them is in off

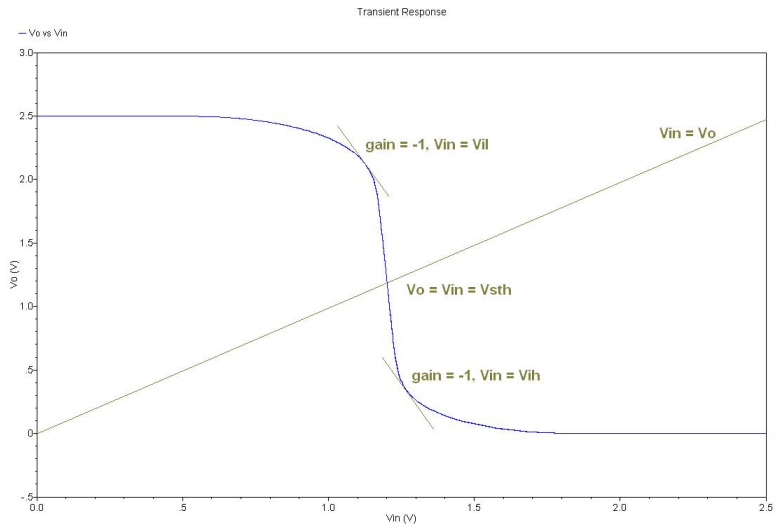


Figure 4.6: Simulated voltage characteristics of the used CMOS inverter.

state. Therefore, the only V_{fg} values that matter are those around the switching point (V_{fg_s}). In view of the above figures, and assuming switching takes place for $V_i \approx V_{dd}/2$, then the circuit operates in weak inversion if $V_{dd} \leq 1.2V$. Throughout experimental tests, $V_{dd} \leq 1.0V$ was used for weak inversion and $_{dd} \geq 1.8V$ was used for strong inversion.

Noise Margin

The simulated voltage transfer characteristics of the used CMOS inverter is plotted in figure 4.6. V_{sth} is shown as the intersection between V_o curve and the line $V_0 = V_{in}$. There are two points where the output slope equals -1, namely V_{il} and V_{ih}. They define the inverters noise margin. Their analytical solution is tedious and adds no insight into the circuit [8]. Nevertheless, they may easily be approximated using piece wise linearisation where the slope in the transition region is assumed constant and equal

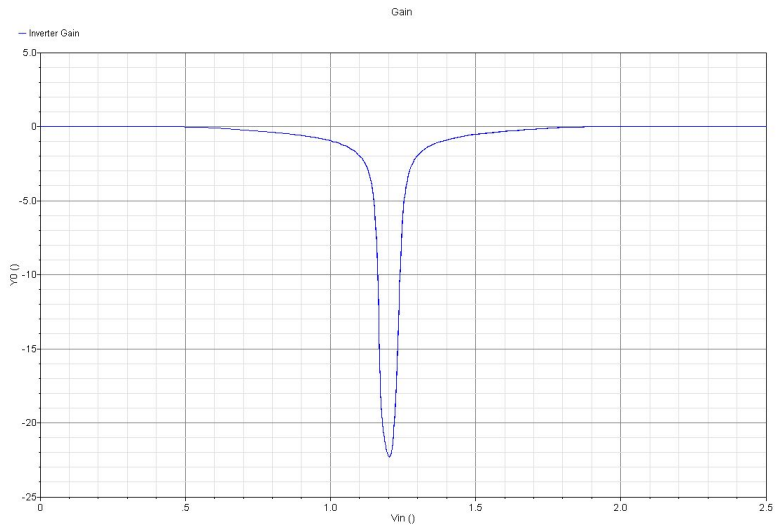


Figure 4.7: Simulated gain of the used CMOS inverter.

to the gain at the switching point (G). Thus [9]:

$$V_{ih} - V_{il} = -\frac{V_{oh} - V_{ol}}{G} = \frac{-V_{dd}}{G}$$

This gives:

$$V_{il} = V_{sth} + \frac{V_{dd} - V_{sth}}{G}$$

and

$$V_{ih} = V_{sth} - \frac{V_{sth}}{G}$$

Therefore, the noise margins NM_h and NM_l are given be:

$$NM_l = V_{il} \qquad and \qquad NM_h = V_{dd} - V_{ih}$$

The gain may be found by equating the current of both transistors and solving for

dV_0/dV_{in}. Sitting $V_{in} = V_{sth}$ and ignoring second order terms gives [9]:

$$G \approx \frac{1+r}{(V_{sth} - V_{tn} - 0.5V_{DS_{satn}})(\lambda_n - \lambda_p)} \tag{4.2}$$

Where $V_{DS_{satn}}$ is the saturation drain-source voltage difference for the n-MOS transistor. Figure 4.7 depicts the gain of used inverters. Equation 4.2 predicts the inverter's gain to be solely determined by the technology parameters particularly channel length modulation (λ). The designer has only little room choosing the gain by designing V_{sth} through transistor sizing and deciding the region of operation.

Gain

The gain of an inverter may be found using its small signal model to be [8]:

$$\frac{V_o}{V_{in}} = -\sqrt{2/I_d}\Big(\frac{\sqrt{k_n(W_n/L_n)} + \sqrt{k_p(W_p/L_p}}{\lambda_1 + \lambda_2}\Big) \tag{4.3}$$

and its corner frequency is given by :

$$\omega_{3dB} = \frac{g_{dsn} + g_{dsp}}{C_{gdn} + C_{gdp} + C_{bdn} + C_{bdp} + C_L}$$

This shows that larger load capacitances tend to limit the frequency response of the inverter.

Noise

This circuit is composed of two transistors. Its noise model would be as depicted in figure 4.8 where e_n^2 and e_p^2 stand for the pMOS and nMOS noise spectral densities.

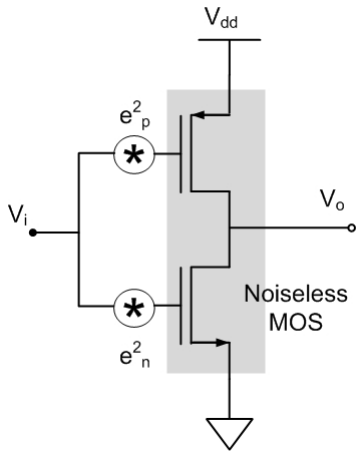


Figure 4.8: Noise model of CMOS inverter.

This is an interesting situation, since both transistors can act as input or load, none of them dominates noise generation. The only way to reduce noise is to reduce noise contribution of each device. Moreover, the equivalent input noise spectral density is not their simple addition. It was found to be [8]:

$$e_{eq}^2 = \left(\frac{g_{m_n} e_n}{g_{m_n} g_{m_p}}\right)^2 + \left(\frac{g_{m_p} e_n}{g_{m_n} g_{m_p}}\right)^2 \tag{4.4}$$

If both transistors are balanced to give $g_{m_n} = g_{m_p}$, then the net noise will be the sum of half of each transistor. This is better than the noise performance of an active load current source inverter stage where the noise is given by [10]

$$e_{eq}^2 = e_p + e_n \left(\frac{g_{m_n}}{g_{m_p}}\right)^2$$

Here, if transistors are are balanced, then the net noise will be the sum of their noises which is about twice that of the inverter [8]. The load capacitance is charged or discharged during switching. Therefore, the larger it is, the more current flows in the switch dissipating more power and increasing its noise.

4.3.2 FG-MOS inverter review

The FG-MOS inverter is basically a CMOS inverter with its gate floating. Its input is the floating gate voltage (V_{fg}) instead of the externally applied V_i. Because the gate is floating and no current may flow into or out of it, its value as seen by the inverter circuit is found using charge conservation.

Thus, in a similar way to floating gate transistors, presented in chapter 2, V_{fg} is given by:

$$V_{fg} = \frac{C_{nMOS}}{C_T} V_{nMOS} + \frac{C_{pMOS}}{C_T} V_{pMOS} + \frac{Q_{TC}}{C_T} + \frac{C_{in}}{C_T} V_{in} \tag{4.5}$$

Where,

$$C_{MOS} V_{MOS} = C_{GS} V_S + C_{GD} V_D + C_{GB} V_B \qquad \text{and}$$

$$C_T \approx C_{GS_n} + C_{GD_n} + C_{GB_n} + C_{GS_p} + C_{GD_p} + C_{GB_p} + C_{in}$$

The first and second terms of 4.5 refer to the nMOS and pMOS contributions respectively. For each, it is composed of its drain, source and body voltages, referred to ground, multiplied by their respective gate capacitances. The suffix 'n' stands for n-type device and 'p' means p-type transistor. The third term represents a constant shift due to trapped charges (Q_{TC}). The last term is the input (V_{in}) contribution.

The total capacitance seen by the floating gate C_{tot} is the resultant of all capacitances it sees. It is expressed as an approximation because fringing and some coupling capacitances including substrate coupling are ignored as they are generally very small compared to others. C_T is layout dependant and transistor related capacitances depend on biasing and the region of operation.

Extending the CMOS inverter discussion to the floating gate inverter, V_{fg_s} is used for the floating gate voltage at switching point. Thus, for identical transistor part:

$$V_{fg_s} = V_{sth}$$

Since, the floating gate voltage is a function of its coupled voltages as in equation 4.5, they collectively decide V_{fg} and switching occurs when it crosses the the switching point (V_{fg_s}), which is decided by intrinsic transistors' properties and V_{dd} in all regions of operation. Therefore, the following discussion of V_{fg} and its relation to the switching point holds for both weak and strong inversion. The only difference is the way switching point is calculated.

Therefore, switching takes place when V_{fg} crosses the value of V_{fg_s} going higher or lower that it. Using this and V_{in_s} to stand for the input level at the point of switching in equation 4.5 yields:

$$V_{fg_s} = \frac{C_{nMOS}}{C_T}V_{nMOS} + \frac{C_{pMOS}}{C_T}V_{pMOS} + \frac{Q_{TC}}{C_T} + \frac{C_{in}}{C_T}V_{in_s} \tag{4.6}$$

In order to get some insight and feeling into this circuit let us solve the above equation for V_{in_s}. This gives:

$$V_{in_s} = \frac{C_T}{C_{in}}V_{fg_s} - \frac{C_{nMOS}}{C_{in}}V_{nMOS} - \frac{C_{pMOS}}{C_{in}}V_{pMOS} - \frac{Q_{TC}}{C_{in}} \tag{4.7}$$

Assuming, balanced transistors so that switching occurs when $V_{fg_s} = V_o = V_{dd}/2$, gives:

$$V_{in_s} = \frac{C_T}{C_{in}}\frac{V_{dd}}{2} - \frac{C_{nMOS}}{C_{in}}V_{nMOS} - \frac{C_{pMOS}}{C_{in}}V_{pMOS} - \frac{Q_{TC}}{C_{in}} \tag{4.8}$$

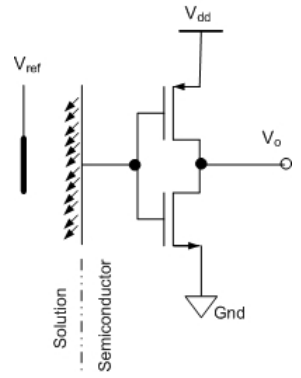


Figure 4.9: A schematic representation of an ISFET based chemical inverter.

This is the needed input voltage (V_{in_s}) that will cause switching of the the floating gate inverter. An equivalent standard MOS inverter would simply switch for an input of $V_{dd}/2$ for properly sized devices. But it is not the case here. First there is an up scaling of $V_{dd}/2$ by $\frac{C_T}{C_{in}}$. Second there is the contribution of the nMOS and pMOS transistors which tend to reduce the needed V_{in_s}. Finally there is the random trapped charges shift that has to be accounted for.

Therefore, finding the switching point of a floating gate inverter is more complicated than the CMOS case. It depends on the operating point and layout as both affect the MOS capacitances that dictate their contribution. Moreover, the input coupling capacitance plays an important role. Finally random trapped charges add their own shift.

4.4 ISFET based chemical inverter

It is the idea here to build on the floating gate inverter presented in the last section and use it as a basis for an ISFET chemical inverter. Its transistor part is just the above standard FG-MOS inverter while its input is not provided via an electrical connection (V_{in}) to a poly-poly capacitor. It is rather supplied via the CMOS ISFET's input: a

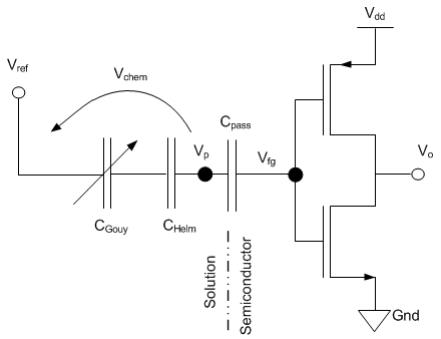


Figure 4.10: Model of the ISFET based chemical inverter.

reference electrode immersed in an electrolyte that is in contact with the passivation layer. In this configuration, two ISFETs, an nMOS and a pMOS, share the same ion sensing membrane and floating gate, in a FG inverter configuration, figure 4.9. In [11], it was the first time to suggest that more than one ISFET may share the same floating gate and use the same ion sensing membrane.

It is modelled as in figure 4.10. Here, the transistor part is just as before, the CMOS inverter. The chemical input model of chapter 3 is used. C_{in} of the FG-MOS inverter is replaced by the passivation capacitance (C_{pass}). The input voltage V_{in} is replaced by the potential at the outer surface of the passivation layer, V_p.

The set-up composed of the reference electrode, electrolyte, and sensing membrane collectively form the input to this floating gate inverter. Thus, the input is the super position of V_{ref} and the ISFET's V_{chem}. It is there combination that play the role of V_{in} of the underlying FG inverter. Therefore, V_{ref} may be used to place the inverter in its most sensitive region very close to switching in order for V_{chem} to trigger it. This is particularly useful because V_{chem} is normally small especially for small pH changes while V_{ref} can be chosen as it is externally supplied.

The switching threshold voltage of the inverter of figure 4.9 is found the same way as that of the FG case. The circuit is split into two parts: the input part that is used

to find V_{fg}, which is the input to the second part: the standard inverter. By charge conservation in a similar way to equation 4.5, V_{fg} is given by:

$$V_{fg} = \frac{C_{nMOS}}{C_T} V_{nMOS} + \frac{C_{pMOS}}{C_T} V_{pMOS} + \frac{Q_{TC}}{C_T} + \frac{C_{pass}}{C_{tot}} (V_{chem} + V_{ref}) \tag{4.9}$$

Here, all terms, apart from the last one, are exactly the same as their counterparts in equation 4.5 above. The last term represents the input part as an ISFET coupled via passivation capacitance (C_{pass}).

Switching is triggered by the sum of V_{chem} and V_{ref}. The first term is pH dependent, as in equation 4.10. The second is decided by the user and may be considered analogous to V_{in} of the FG inverter. V_{chem} has the effect of shifting the switching threshold voltage as seen by V_{ref} if it is the input. By the same taken, if V_{chem} is the input V_{ref} will shift the switching point it sees.

V_{chem} was presented in chapter 3. It is reproduced here for convenience:

$$V_{chem} = \gamma + 2.3 \alpha U_T pH \quad V \tag{4.10}$$

The pH sensitivity of this circuit is defined as the change of V_{fg} due to pH change. This may be found from equation 4.9 and 4.10 as:

$$pH sensitivity = \frac{dV_{fg}}{dpH} \approx \frac{C_{pass}}{C_{tot}} \frac{dV_{chem}}{dpH} = \frac{C_{pass}}{C_{tot}} \; 2.3 \; \alpha \; U_T \quad V/pH \tag{4.11}$$

The approximation is used to indicate that, if this change causes switching, then nMOS and pMOS contribution, assumed constant here, may change according to their operating points. This is very similar to a single transistor's pH sensitivity. Thus, similar

values are expected.

For a constant V_{ref}, the chemical voltage at the switching point (V_{chem_s}) is:

$$V_{chem_s} = \frac{C_T}{C_{pass}} V_{sth} - \frac{C_{nMOS}}{C_{pass}} V_{nMOS} - \frac{C_{pMOS}}{C_{pass}} V_{pMOS} - \frac{Q_{TC}}{C_{pass}} - V_{ref} \tag{4.12}$$

and for the reference voltage at the switching point V_{ref_s} assuming a constant V_{chem}:

$$V_{ref_s} = \frac{C_T}{C_{pass}} V_{sth} - \frac{C_{nMOS}}{C_{pass}} V_{nMOS} - \frac{C_{pMOS}}{C_{pass}} V_{pMOS} - \frac{Q_{TC}}{C_{pass}} - V_{chem} \tag{4.13}$$

It may worth noting that

$$\frac{Q_{TC}}{C_{pass}} = \frac{C_T}{C_{pass}} \times \frac{Q_{TC}}{C_T} = \frac{C_T}{C_{pass}} \times V_{fg} \textit{ induced by trapped charges} \tag{4.14}$$

This means that initial trapped charges shift V_{fg_0} is seen by the chemical input scaled by C_T/C_{pass} while it scaled up by C_T/C_{in} in the FG-MOS case.

It is interesting to note that V_{ref} and V_{chem} have a one to one relation. That is a $1mV$ change in one of them corresponds to the same change in the other. This is handy especially in lab measurements as it is much easier to electrically change V_{ref} instead of chemically modify pH. Then, It is used as an indication for an equivalent change in V_{chem}. Measured sensitivity may be used to find the corresponding pH change.

4.4.1 Simulation

The circuit of figure 4.9 was simulated using a Verilog-A model according to equation 4.10. The simulation was based on the kit of a commercial AMS $0.35\mu m$ 2P4M CMOS

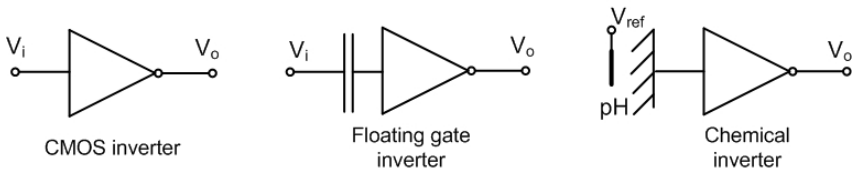


Figure 4.11: Symbols of three different inverters: CMOS, floating gate, and chemical inverters.

process that was used later to manufacture the devices. The supplied factory kit based on the BSIM3.32 model parameters was used [12].

In order to have a fair basis of comparison, the same basic CMOS inverter was simulated, fabricated and tested in three different configurations. First version was the standard CMOS inverter. Then its common gate was made floating and the input was capacitively coupled to it in a FG inverter version. Finally, the floating gate was connected using metal vias through the stack to the topmost metal layer where a large metal area formed the chemical gate as an ISFET inverter, figure 4.11. The output of each was buffered by two CMOS inverters increasing in size in order to provide enough current to drive the load of a bond pad and the measurement PCB. This implies that the simulated, and later measured, output is not that produced by the input inverter. It is rather a modified version of it. Since the aim is to produce digital output not analogue amplification, this is acceptable. However, it will have an impact on the total circuit performance. Which is depicted in appendix D.

The width of the pMOS transistor was $12\mu m$ and that of the nMOS was $4\mu m$. In the CMOS inverter case, the input was externally supplied. While for the FG-MOS inverter, the input was coupled via a $7 \times 3\mu m^2$ poly1-poly2 capacitor. According to process parameters, this makes $C_{in} \approx 20.14fF$ including fringing capacitance [12]. In the ISFET case, C_{pass} was given the value of $152fF$ which is the nominal value for a chemical gate area of $7000\mu m^2$[20]. This value is based on the information released by

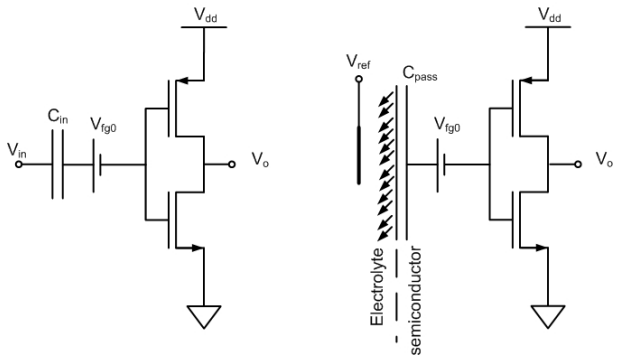


Figure 4.12: Schematics of FG-MOS inverter and ISEFT based chemical inverter indicating the initial floating gate voltage.

the factory in an email where it was indicated that the passivation material is: PECVD silicon-nitride on top of HDP Oxide. Their nominal thickness's are $1050nm$ and $950nm$ respectively. The relative permittivity of each is: $\epsilon_{r_{ox}} = 3.9$ for SiO_2 and $\epsilon_{r_{nit}} = 7$ for Si_3N_4. The used transistor sizes were not minimum size because the aim is to demonstrate the concept of pH driven inversion. Optimising silicon area would be a next step that is beyond the scope of this thesis. Moreover, the chemical gate was very large compared to inverter silicon area because it was the aim to make C_{pass} the largest capacitance in the circuit though it has,due to thick passivation, the smallest capacitance per unit area. It was made at lease 10 times all other capacitances coupled to the ISFET's floating gate. This is has two aims. First, it maximises the effect of V_{chem} on V_{fg} by making its coupling capacitance dominant. Secondly, it reduces the effect of the non linear C_{GB} of both transistors on V_{fg} by making their coupling weight small compared to C_{tot}. The area underneath the chemical gate may be used for processing circuitry. For example, it was used here for the buffering stages.

In simulations, the ISFET's pH sensitivity is an input parameter. Nerstian sensitivity of $59mV/pH$ could be used. However, it is known that ISFETs built in CMOS generally have less sensitivity [13] [14] [15]. Thus, it was assumed $45mV/pH$ which is reasonable according to the measured values reported in these references. Though, it would be

Table 4.1: Simulated switching points of a floating gate inverter and an ISFET based chemical switch, with variable initial floating gate voltage V_{fg_0} and constant pH.

V_{fg_0} (V)	-3.0	-2.0	-1.0	0.0	1.0	2.0	3.0
FG-MOS V_{in_s} (V)	7.36	5.29	3.11	0.936	-0.984	-2.76	-4.59
ISFET V_{ref_s} (V) (pH7)	4.02	2.84	1.66	0.496	-0.634	-1.77	-2.94

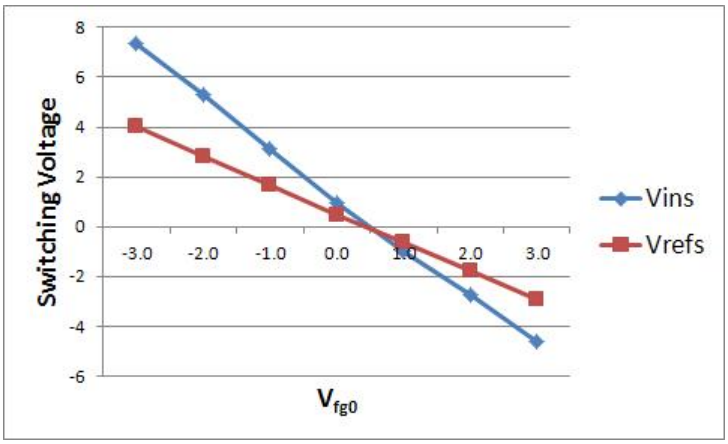


Figure 4.13: Plot of the data in table 4.1.

appealing to first measure the sensitivity of the manufactured devices and then use similar value in simulations. However, this would look like tailoring simulations to measurements, which is not the aim.

The above three circuits were simulated to find their switching points. The CMOS inverter had a constant switching point of $0.51V$ for $V_{dd} = 1.0V$. It may worth reporting that, transient simulations for the floating gate and ISFET cases did not converge without specifying an initial floating gate voltage V_{fg_0} in the convergence aid section of Cadence. This was predicted in [16]. For, the floating gate and ISFET cases, the input was swept while using V_{fg_0} as a parameter in order to find the effect of different trapped charges. Table 4.1 summarizes the results and figure 4.12 shows the schematics.

Simulations showed that, for zero trapped charges, the switching point of the floating gate inverter is higher than that expected for an identical standard CMOS. The ISFET

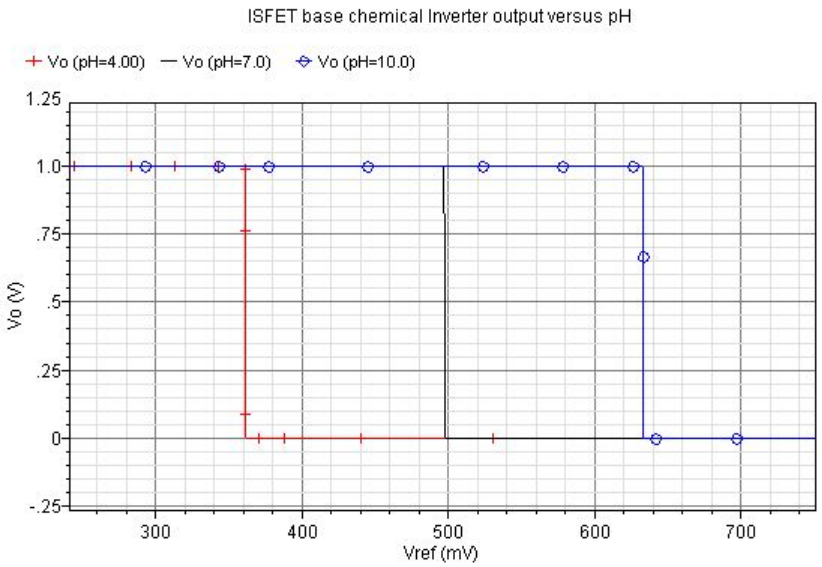


Figure 4.14: pH sensitivity of ISFET based chemical inverter.

based switch has a similar case but it is shifted down by the chemical voltage due to the pH 7 buffer solution, which gives about $-0.315V$.

The other point to get is that positive trapped charges shift the switching point to the left and negative trapped charges shifts it to the right, as shown in figure 4.13. Moreover, The switching point change is linear with respect to trapped charges voltage with a slope of $-C_T/C_{pass}$ for the ISFET inverter and $-C_T/C_{in}$ for the FG-MOS inverter. This is in agreement with equation 4.14. C_{in} was about $20fF$ for the FG case and C_{pass} was about $152fF$ for the ISFET inverter. This was the primary reason for their different trapped charges switching points difference. This becomes clearer if the shift due to pH contribution is removed.

In order to find the pH sensitivity of the ISFET based chemical inverter it was simulated for pH values of 4, 7, and 10. Figure 4.14 shows the result. Overall simulated sensitivity was $44.61mV/pH$. This is well expected with the assumed value of $45.0mV/pH$.

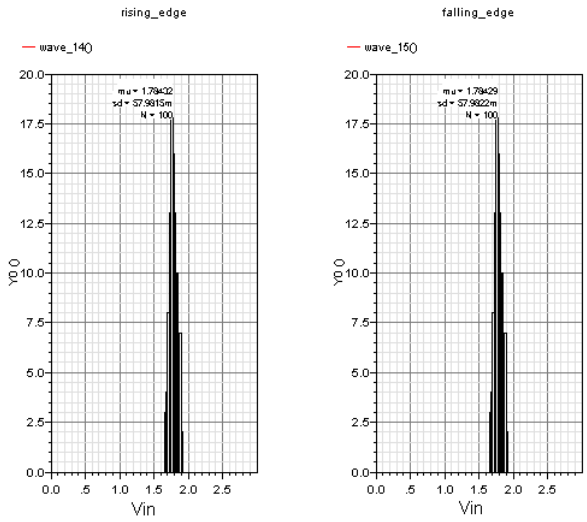


Figure 4.15: Monte Carlo Analysis of the ISFET inverter, strong inversion.

Monte Carlo Analysis

Considering mismatch and process variation, Monte Carlo analysis for both considering the falling edge and the rising edge is depicted in figure 4.15. The mean of hundred runs was $1.78V$ for $V_{dd} = 3V$ and the standard deviation was $57.9mV$. Which indicate a very stable switching points with more than 95% within the range $1.78 \pm 0.17V$ or less than 10% variations.

However, for sub-threshold operation the mean was $0.509V$ for $V_{dd} = 1V$ and the standard deviation was $49mV$, figure 4.16. This indicates that more than 95% of the switching points are within about 28.8% of the mean.

4.4.2 Measurements

The circuit described in the simulation section was manufactured using a commercial AMS 2P4M $0.35\mu m$ technology through Euro-practice. The die size was, minimum acceptable, $3mm^2$. The dies were fixed and bonded on test PCB dip-sticks. Then they

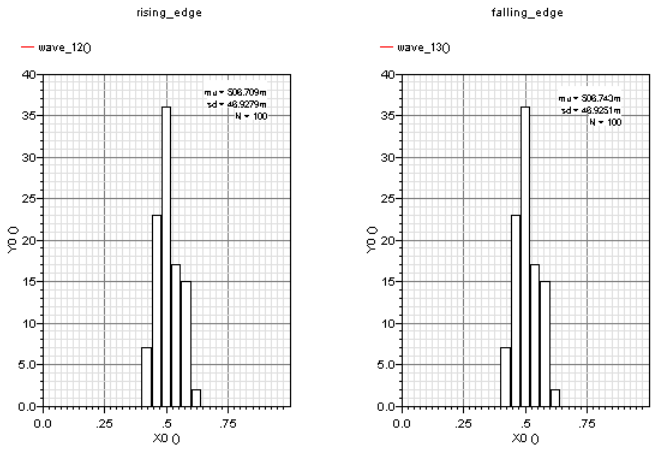


Figure 4.16: Monte Carlo Analysis of the ISFET inverter, weak inversion.

Table 4.2: Measured switching points of identical floating gate and ISFET based inverters from different dies of the same batch ($pH = 7$ for the latter)

Die number	1	2	3	4	5	6
FG-MOS V_{in_s} (V)	-8.296	6.31	12.01	> 13	4.174	3.088
ISFET V_{ref_s} (V) (pH7)	-3.04	-2.65	3.34	6.07	-3.65	1.95

.

were carefully encapsulated using EPO-TEK T7139 epoxy with only the chemically sensitive areas exposed. A single junction $Ag/AgCl$ glass reference electrode was immersed in the electrolyte under test in order to apply V_{ref}. It was chosen because of its stable junction voltage. Keithley Semiconductor Characterization System Model 4200-SCS was used in the measurements. And 3 different pH buffer solutions (4.0, 7.0, and 10.0) from Hanna chemicals were used as different pH buffer mediums.

In order to find the switching point, for the CMOS inverter, its input was swept between rails. However, for the FG and ISFET inverters this is not enough. Trapped charges may, according to equation 4.5, shift the floating gate voltage by an unpredictable amount. Thus, the input for FG case was swept as needed within a maximum range of $\pm 13V$. This value was chosen not only because it is already very high, but also to stay away from the minimum poly-poly capacitance break down voltage specified as $15V$

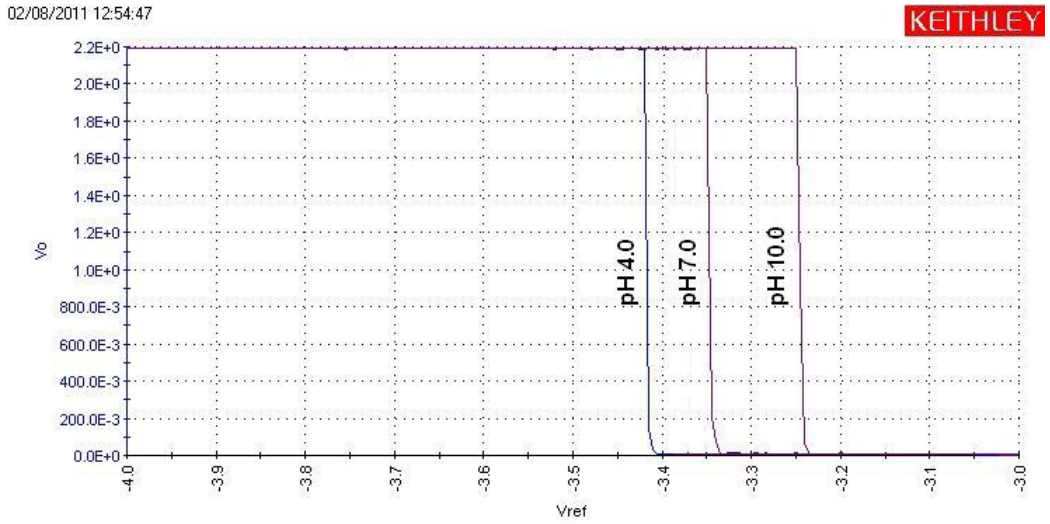


Figure 4.17: pH sensitivity of an ISFET based chemical switch operated in strong inversion.

[12]. Basically, poly-1 of the input capacitance was used for V_{in}. While, poly-2 was part of the floating gate. This reduces floating gate coupling with grounded substrate. Both devices were measured on dry PCB's.

For measuring the ISFET based inverters, the dies were immersed in pH 7 buffer solution from Hanna Chemicals. V_{ref} was swept quickly from $-5V$ to $+5V$ with large step size of $0.1V$. This gave the region of interest where switching occurs. Then a fine sweep is done with $5mV$ step size in the region of interest in order to find V_{ref_s} of the circuit under test. Care was taken not to subject the devices for high V_{ref} except if necessary. As it is understood that such large voltages shorten the life time of ISFETs [15].

Six dies were measured with one device of each type. The measured switching point of all CMOS devices was $0.52V$ for $V_{dd} = 1V$. However, the measured switching points of the floating gate and ISFET based chemical inverters are shown in table 4.2. It is clear from this table how large the effect of trapped charges can be. Device number 4 did not switch from logic "1" to "0" even after sweeping V_{in} from $0V$ to $13V$. This can only be explained by large negative trapped charges in its floating gate.

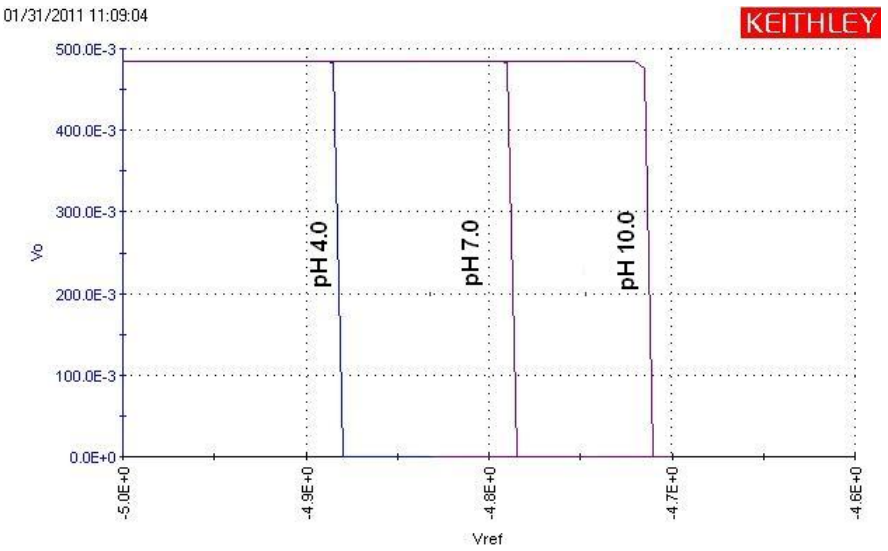


Figure 4.18: pH sensitivity of an ISFET based chemical switch operated in weak inversion.

It is interesting to note that none of the measured FG and ISFET inverters had a switching point within rails. Moreover, non of them coincided with zero trapped charges. They were either lower than it, indicating positive trapped charges, or higher than it, indicating negative trapped charges.

In order to measure pH sensitivity of an ISFET inverter, the device was inserted in buffer solutions starting with buffer 10.0 then 7.0 then 4.0. It was rinsed by DI water between buffer solutions to prevent cross contamination. The reference voltage was swept for each case in order to find the value that caused switching for each pH value. Figure 4.17 shows the outputs for a strong inversion case where $V_{dd} = 2.2V$. The switching points were: $V_{ref} = -3.415V$, $-3.345V$, and $-3.245V$ for pH $4.0, 7.0$,and 10.0 respectively. pH sensitivity, measured as the switching voltage shift due to pH change, was found to be $28.33mV/pH$ for this particular device.

As the low power sub-threshold operation is also of interest, the same was repeated for $V_{dd} = 0.5V$. Figure 4.18 shows the outputs for this case. The switching points

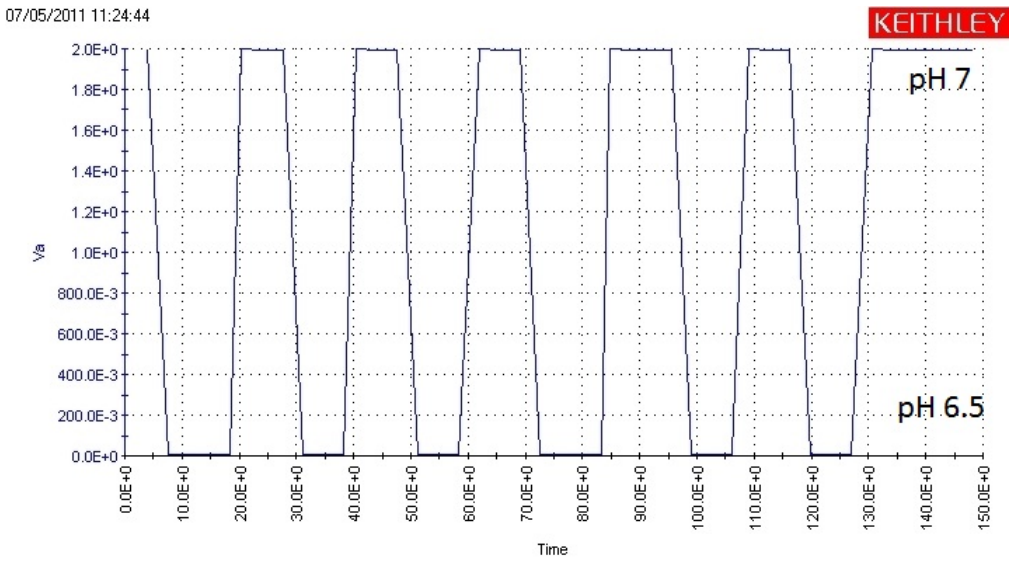


Figure 4.19: Switching triggered by changing electrolyte's pH.

were: $V_{ref} = -4.885V$, $-4.785V$, and $-4.710V$ for pH $4.0, 7.0, and 10.0$ respectively. pH sensitivity was $29.17mV/pH$.

In order to verify the switching operation driven by pH change alone, the following experiment was conducted. V_{ref} was fixed close to switching point of a pH 7.0, in a $20ml$ buffer solution. This was the initial condition of logic "1". The solution's pH was changed by pipetting $0.1M\ HCl$ that lowered the pH to 6.5 ± 0.1. This gave logic "0". Then, $0.1M\ NaOH$ was pipetted in order to bring the pH back to 7.0 ± 0.1 and hence switching the output back to logic "1". This process was repeated to cause switching sequence of ("1" $\rightarrow$ "0" $\rightarrow$ "1") a number of times. pipetting steps were manually done and were about 10 seconds apart. The resulting curve is shown in figure 4.19.

This experiment was planned without pauses. It was not possible to use a glass electrode to verify the actual pH of the solution between pipetting steps. Therefore, before conducting this experiment, a number of titration experiments were done with the same amount of starting buffer solution, $20ml$; and the pH meter alone. This was needed as

the author of this thesis was not familiar with precise chemical experiments based on exact calculations. Moreover, it is the aim to verify this circuit's operation for a pH change. Thus, it is the change that is important here, not exact pH values.

A Seven-Eleven temperature compensated glass pH meter from Mettler Toledo was used. The magnetic stirrer speed was kept constant throughout all experiments. The amount of pipetted HCl acid to change the solution's pH from 7.0 to 6.5 was recorded. Then the amount of $NaOH$ needed to bring it back to pH 7.0 was recorded. This was one pipetting cycle. A number of similar cycles were tabulated. As the solution's volume increase with each cycle, the amount of needed acid and base slightly changed. This made one experiment run. The whole procedure was repeated three times with a fresh solution for each. The amount of pipetted acid and base for each cycle of the three experiments were tabulated and verified to be consistent; which gave confidence. Afterwards, the above switching experiment was performed using these recorded volumes for each step. The aim here is not to show minimum detectable pH change. The emphasis was rather to show that the circuit does work and within a short time frame as the whole process was done in about 3 minutes. This is much faster than the glass electrode pH meter.

4.4.3 Discussion

The purpose of this work was to test the feasibility of detecting chemical thresholds using a simple and scalable switch. The sharing of the passivation ion sensitive membrane by more than one ISFET is a novel idea. It enabled the realization of a true chemical switch that works regardless of drift or trapped charges. Both can be compensated for by choosing V_{ref} at the verge of switching. That gives pH change in the form of V_{chem} change, the chance to cause switching. A number of points to note here:

Trapped charges

The switching threshold voltages in figure 4.17 were negative while positive in figure 4.18. Yet, both were different from those values predicted by simulations. Moreover, table 4.2 shows how diverse switching voltages can be for the same circuit in different dies. This adverse random shifts in ISFET inverters' floating gate voltages may only be explained by trapped charges in the system. Suitable values may be assumed for simulation purposes. However, measurements give the truth,which might be different.

It is possible for simulations to reproduce similar results as measurements by assuming initial floating gate charges that produce V_{fg} shift equal to the difference between the measured and simulated switching voltages. For the example in figure 4.17, if the trapped charge shift of V_{fg} (Q_{TC}/C_{pass}) in equation 4.13 was set to $4.975V$ in simulations. Its results will agree exactly with measured value for pH 7. Physically, this shift is due to the random charges in floating gate and passivation layer. It is interesting to note that similar charges in the circuit of figures 4.2 and 4.3 will cause them to fail, while the inverter presented here is still operational.

This large variations of switching threshold voltages of ISFET based chemical inverters shows how big a problem this can be especially for arrays in the same die with a common reference electrode. It is quite possible to get switching voltages scattered all around the place without any useful use of them. However, it would be great if it was possible to match such switches in order for all inverters in an array to detect a common threshold, of course within tolerance limits. Then a common V_{ref} can be used to bring the array on the verge of switching allowing the detection of a chemical threshold. It would be even better if it was possible to choose the point of switching, which relaxes the conditions on the choice of V_{ref}. This will be addressed in chapter 6.

Sensitivity

The second point is the reduced sensitivity. It is known that ISFETs built by CMOS technology suffer from reduced sensitivity [17] [15] [13]. The sensitivity parameter (α) in equation 4.10 reflects this. For the tested circuit: $\alpha \approx 0.51$. Having two transistors reduces the coupling effect of C_{pass} by increasing C_T, which further reduces ISFET's sensitivity. Nevertheless, this is within the range of values reported for ISFETs built in standard CMOS technologies [14] [15] [13].

However, the reported sensitivity above is limited by the Nerstian value of $59.2mV/pH$, which is the physical upper limit. One might ask: is it possible to fabricate an ISFET with a higher physical sensitivity? The answer is NO, but it is possible to scale it. A differential amplifier can be used to amplify V_{chem} which is basically the difference between an ISFET and a reference insensitive ISFET (REFET) or between V_{fg} and V_{ref} [17]. Alternatively, a correlated double sampling technique may be used to amplify the change in V_{chem} [18] or a similar technique using analogue capacitive storage [19]. It is also possible to address this problem easily and simply using floating gate techniques to design an ISFET with a higher sensitivity than the Nerstian limit. This point will be addressed in chapter 5.

Drift

Drift is a known problem in ISFETs. It was reported by a number of researchers [17]. A number of ways of dealing with it were proposed [20] [18]. This work suffered from it but it was not attempted to deal with it here.

In a similar way to single ISFETs, drift manifested itself here as temporal switching threshold voltage shift while pH remains a constant. It was postulated to be caused by mobile ionic charges in the passivation layer [21] [22]. It was observed here to start

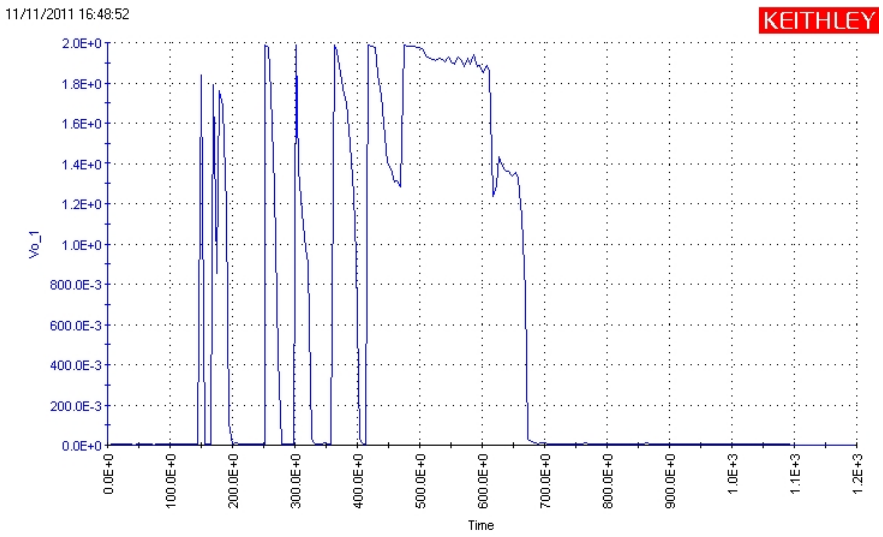


Figure 4.20: Switching triggered by 0.1 pH change in electrolyte concentration, time is in seconds.

large, then reduces with time as long as experiments are running. If experiments stop for some time, overnight for example; drift starts again with the start of V_{ref} sweep. Again, it starts large then reduces but generally with less magnitudes. This implied that in order to insure low drift, the devices had to be soaked, while repeatedly sweeping V_{ref}, for long enough time. This was the case in all reported experiments. The only exception is when the dipstick was moved from one pH buffer solution to another, after being DI water rinsed in the way.

The average drift, that was observed here, was $10mV/h$. This is quite reasonable compared to values reported elsewhere [18]. However, for a sensitivity of about $30mV/pH$ this corresponds to pH change of around 0.33 units per hour. This is well below chosen pH change to trigger switching in figure 4.19. However, in figure 4.20, the sample pH was increased by 0.1 units in order to cause switching from logic “0“ to logic “1“. This was enough to cause switching. however, it was not enough to keep it stable with time, drift counter acted it and took over after about 5 minutes. Therefore, drift was a

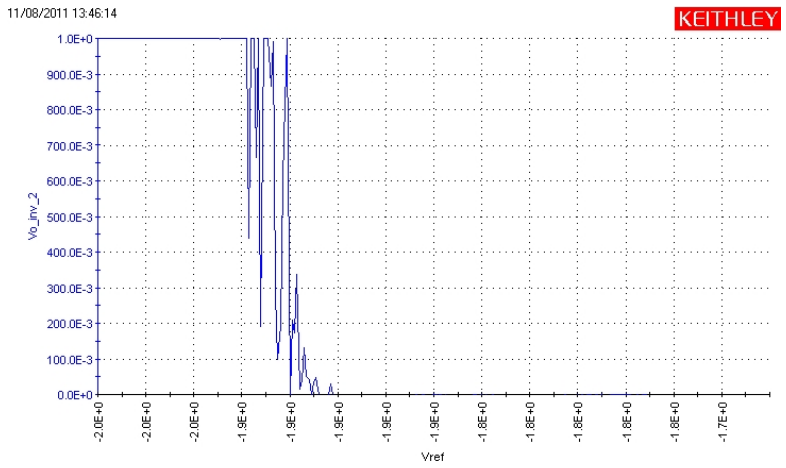


Figure 4.21: Measured response of ISFET based Chemical inverter for small changes in V_{ref}

limiting factor to measure very small pH changes that can trigger switching. It simply masks them.

Output stability

The reported results in figures 4.17 - 4.20 show nice and smooth curves simply because trouble was avoided. Large enough V_{ref} or pH change was used to cause stable switching. For example, 0.5 pH was chosen to prompt switching in the curve of figure 4.19. Though, smaller pH changes can do the job, results may not be as stable.

Similarly a large enough V_{ref} step size had to be used in its sweeps. No less than $2mV$ steps, mostly $5mV$; were used in the above presented results. This corresponds to about about 0.125 pH units assuming $40mV/pH$ sensitivity. Using smaller step sizes, result in curves like that in figure 4.21. Here, V_{ref} was swept with a step size of $1mV$.

This raised the question: will introducing hysteresis by using a Schmitt Trigger help stabilize the output in this case? The answer is YES. That was tested and will be

presented in the next section.

The nature of a switching circuit

The measured circuit is basically three cascaded open loop push pull amplifiers. They produce a huge gain, appendix, D, resulting in the sought after digital output that changes state only at the switching point. Therefore, it is difficult to know how far is the applied V_{ref} from this point. For a single ISFET case, a continuum of values is measured. Thus, the output gives a clear indication of how far is the applied V_{ref} from the needed value for a meaningful measurement. However, in the case of a switch a solid high or solid low is the output, which is not very helpful. Plus it does not make sense to span the whole possible input range with the same high resolution, as it will take a long time. This will inhibit exact measurements because drift will have a good chance to mask the sought results.

4.5 Chemical Schmitt Trigger

There are certain applications that require the detection of small pH changes. For example, for DNA detections, the target strand needs to be amplified in order to generate big enough pH signal for label free detection [2] [23]. Polymerase chain reaction (PCR) cycles are used for this process. Each cycle doubles the target DNA strand. Thus, the smaller pH change that can trigger switching, the less the number of PCR cycles that are needed and hence less time and power are needed for this process. In other applications a very small range of pH variations needs to be detected. For example, blood pH has to be measured to an accuracy of 0.001 pH units [24].

Aiming to detect smaller pH changes, V_{fg} needs to be very close to V_{sth}. In this case,

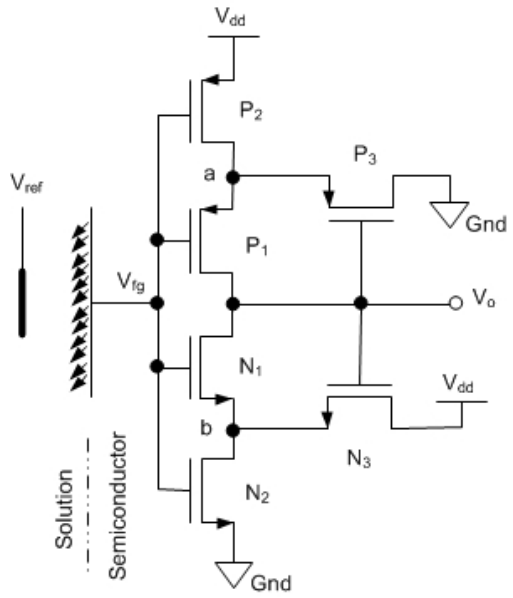


Figure 4.22: Circuit diagram of the built ISFET based Chemical Schmitt trigger

the inverter's output undergoes fast switching and suffers from instability, figure 4.21. Moreover, noise becomes a more important issue. A more stable output with better noise immunity is needed. The simple inverter is not sufficient for such a situation as it suffers from ripple and distorted output. The first circuit that may come to mind is the famous Schmitt trigger. It provides a more stable output with better input noise immunity. It can be used in applications where the digital detection of small pH changes is required. An ISFET based chemical Schmitt trigger was built and tested, figure 4.22.

The Schmitt trigger is a well known thresholding circuit with hysteresis. It is widely used in both analogue and digital applications. Generally, its closed loop applications include function generation while it is used in open loop configuration to increase input noise immunity [25]. This last application is of interest here.

Positive feedback is used in Schmitt trigger circuits to provide two distinct threshold voltages. It produces a digital output high when its input goes lower than its lower threshold voltage (V_{sL}). The output switches to low only if the input increases higher

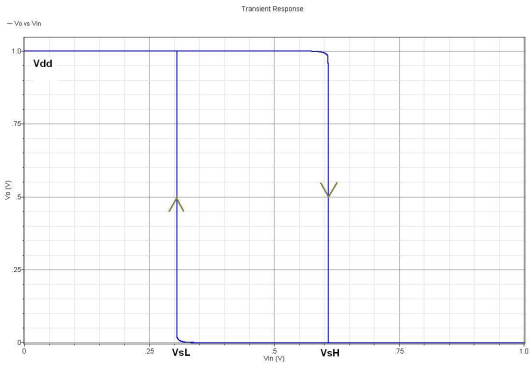


Figure 4.23: Simulated output of the built Schmitt trigger circuit showing its two distinct non overlapping switching thresholds.

than the higher threshold voltage (V_{sH}), figure 4.23 [26]. This prevents small input fluctuations from triggering fast output switching. This way the input noise margin is increased and a stable output is produced, figure 4.25.

A standard Schmitt trigger circuit [6] was adopted. An ISFET based chemical Schmitt trigger was built by allowing its four transistors to share the same floating gate connected to the ion sensitive membrane, figure 4.22. Its floating gate (V_{fg_s}) is determined by the weighted sum of its inputs [27].

$$V_{fg_s} = \frac{C_{pass}}{C_{tot}}\left(V_{chem} + V_{ref}\right) + \frac{C_{nMOS_{1,2}}}{C_{tot}}V_{nMOS_{1,2}} + \frac{C_{pMOS_{1,2}}}{C_{tot}}V_{pMOS_{1,2}} + \frac{Q_{TC}}{C_T} \quad (4.15)$$

Where C_{tot} is the total capacitance seen by the input floating gate. $C_{nMOS_{1,2}}V_{nMOS_{1,2}}$ are the contributions of the two nMOS input transistors to V_{fg}. It is found by the product of each source, drain, and body voltage by its respective gate capacitance. $C_{pMOS_{1,2}}V_{pMOS_{1,2}}$ are defined in the same way. This is similar to the inverter case but with more devices.

According to the circuit of figure 4.22, the transistors P_3 and N_3 form a feedback path

controlled by the output (V_0). If the floating gate voltage represents an input of logic (0), that is ground and the output is logic (1) that is V_{dd}; then P_1 and P_2 are in saturation while N_1 and N_2 are cut-off. P_3 is in cut-off and N_3 is in saturation. Points (a) and (b) are V_{dd}. As the floating gate voltage increases slowly towards an input logic (1), transistors P_1 and P_2, which are pulling the output up to V_{dd} move towards triode region in their way to cut-off. In the same time N_2 moves from cut-off to triode region in its way to saturation. N_1 will not move because its source is pulled high by N_3. Thus, N_3 will be competing with N_2. The former pulls point (b) high to V_{dd} while the latter tries to pull it down to ground. N_1 will not turn on to bring the output to state (0) except if N_2 wins and brings point (b) to ground at V_{sH}. If that happens, switching will be very fast due to the positive feedback action of P_3 which inters saturation and pulls down point (a) to ground turning P_1 off. Thus, V_{sH} can be designed by properly sizing N_2 and N_3 in order to increase the point where N_2 wins and the output switches to logic (0) for an input higher than a high threshold V_{sH}. The output will stay high regardless of the input value as long as it is higher than the other lower threshold, V_{sL}. At this state, N_3, P_1, and P_2 are cut-off while N_1, N_2, and P_3 are in saturation. Points (a) and (b) are pulled to ground.

When the floating gate voltage moves down towards logic (0), the opposite happens and P_2 will now compete with P_3 in pulling point (a) to V_{dd} or ground. When P_2 wins, P_1 will quickly shift the output towards V_{dd} when the input goes below the lower threshold V_{tL}. The circuit will stay in this state regardless of the input as long as it does not go higher than the V_{tH}. This way the circuit will not change state if the input undergoes small variations that do not cross one of these distinct thresholds.

Considering process variations and mismatch, Monte Carlo simulation's output is shown in figure 4.24.

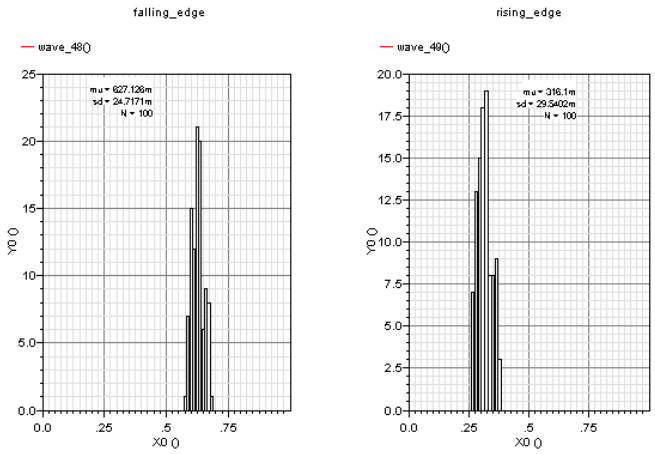


Figure 4.24: Mismatch and process variations Monte Carlo analysis for the used Schmitt trigger circuit.

4.5.1 Experimental results

The chemical Schmitt trigger circuit of figure 4.22 was manufactured in the same die with a standard chemical inverter using AMS $0.35\mu m$ 2P4M CMOS process commercially available via Europractice [12]. P_1 and P_2 transistors had a width of $1.6\mu m$ while N_1 and N_1 had a width of $1.0\mu m$. The width P_3 was $1.0\mu m$ wile N_3 was $5.7\mu m$. According to simulations V_{sL} is $306mV$ and V_{sH} is $608mV$. For a sensitivity of $45mV/pH$ their difference corresponds to a pH difference of 6.7 units. For the ISFET based chemical inverter, the transistor widths were $2.0\mu m$ for the nMOS and $3.0\mu m$ for the pMOS. Both had identical ion sensitive membrane areas of $50.0 \times 30.0\mu m^2$ and were equally buffered by two CMOS inverters increasing in size. They were tested in a pH 7.0 buffer solution from Hanna chemicals. Keithley 4200 semiconductor characterisation system was used to drive the reference electrode and measure the outputs.

V_{ref} was sept at the high resolution of $0.1V$ per step, this corresponds to about 0.03 pH units change per measurement step, for an overall sensitivity of $30mV/pH$. Measuring both circuits in the same time, the inverter's output is depicted in figure 4.21 while the

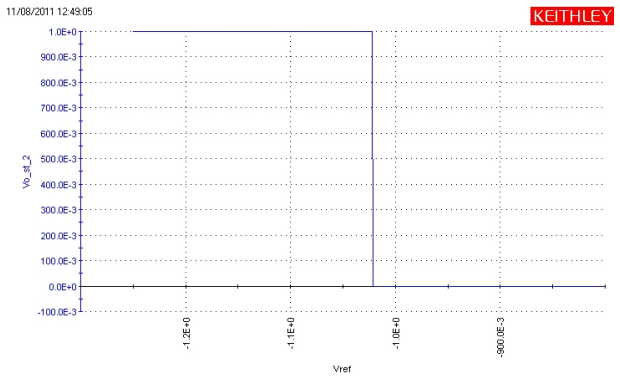


Figure 4.25: Measured response of ISFET based Chemical Schmitt trigger for small changes in V_{ref}

Schmitt trigger out put is shown in figure 4.25. This circuit was built and tested after all other circuits in this thesis were tested. Thus, it was not used in the rest of the thesis, though it would be appropriate to use it. It is left as a further work to apply the ideas to be presented in next chapters to the ISFET Schmitt trigger circuit.

It is clear that the ripples of the inverter's output were removed in the Schmitt trigger output thanks to its hysteresis. It can be seen that the two circuits had different switching points. This is attributed to different trapped charges in their floating gates.

4.6 Conclusion

This chapter presented the simplest digital block of ISFETs, an inverter. It started with reviewing the floating gate inverter. Then it was extended to the ISFET based chemical switch. Simulations and measurements were presented. Discussing the results and findings, there was a need to increase the input noise immunity. Thus, a Schmitt trigger circuit was fabricated and tested. Other points that were discussed, namely the need for increased sensitivity and better matching will be presented in the next two chapters.

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Chapter 5

ISFETs with scalable input-referred sensitivity

5.1 Introduction

The maximum theoretical potential change at the electrolyte side of the ion sensitive membrane with pH change is $59.2mV/pH$ at 25 °C. It is the well known Nerstian sensitivity. It sets the maximum sensitivity of an ISFET before considering noise. Devices built using standard CMOS processes generally have less sensitivity [1]. However, it would be desirable to realise higher values especially for applications where a small pH change is to be measured. Doing that enhances measurement resolution and relaxes constraints on sample volumes and concentrations. The ultimate aim is to increase the signal to noise ratio (SNR).

Several researchers addressed this point using different techniques. Different physical structures, both CMOS compatible and devices built by special processes, were proposed.

ISFETs in CMOS are floating gate devices. It is the subject of this chapter to present the use of floating gate transistors (FG-MOS) and νMOS concepts to scale the CMOS ISFET's sensitivity without using additional circuitry or processing steps. That is by using a second electrical input that is capacitively coupled to the ISFETs floating gate via a small capacitance. The ratio between the chemical sensitive passivation capacitance and this small capacitance becomes the scaling ratio of pH sensitivity referred to this input. The effect of this on the overall SNR of the chemical signal is to be presented.

It was possible for more than one device to share the same ion sensitive membrane (passivation layer). Using floating gate MOS concepts, a complementary pair of ISFETs (n and p devices) shared the same ion sensitive membrane forming an ISFET based chemical switch, as was presented in chapter 4. Extending the above idea to ISFET based chemical switches, a second electrical input may be capacitively coupled to its floating gate. Through properly sizing this coupling capacitor, it is possible to enhance pH sensitivity referred to its input more than a hundredfold. This forms an ISFET based νMOS chemical inverter with enhanced input referred sensitivity.

The focus here is in a building blocks for sensing pH change and can be used in large arrays. The change of interest is likely to be in one direction, as is the case with DNA sequencing. Thus, single slope sweeps are considered. Generally, bidirectional pH change may be monitored. But in such a case different strategies should be used, like the pulse width modulation (PWM) technique in [2].

The second section reviews semiconductor ion transducer structures that demonstrated sensitivities higher than the Nirstian limit. Then, the ISFET with scaled input referred sensitivity is presented in section three. It is followed by extending the same idea to high sensitivity chemical switches in section four. Both simulations and experimental results are presented. Finally a concluding word is due.

5.2 Reported High sensitivity Semiconductor Ion Sensors

This section briefly reviews previously reported semiconductor ion sensors that demonstrated high pH sensitivity. These are three devices, that are not CMOS compatible. Plus, a suggestion to put an ISFET in a very specific region of operation. Finally, a system using ISFETs in feedback loop that includes switched capacitors.

Hizawa et al in [3] used a metal insulator semiconductor (MIS) structure as the input of a charge transfer device. The concentration of the electrolyte under test was used to control the charge transfer from an input diode well, that supplied electrons, to an output diode well, that accumulates them. An input and an output transfer gates were used to switch the charge flow on and off. They control integration cycles. Charge flow from the input well to the deeper output well is controlled by the chemical potential. A reset gate was used to remove accumulated charges and start a new measurement, figure 5.1.

The output well is connected to the input of an inverting amplifier so that accumulated charges modulate its output. The charge transfer can be repeated a number of times for further charge accumulation, hence amplification of the chemical signal. A sensitivity of $1130mV/pH$ was reported after five accumulation cycles. This was an amplification of about 19 times of pH sensitivity compared with the Nerstian limit.

The same group reported an improved version of this charge transfer type pH sensor in [4]. Here, they added another input control gate in order to provide better control of the input. Charges were accumulated in the gate capacitance of an output amplifier transistor biased in a source follower configuration. A sensitivity of 60 mV/pH was reported after one accumulation cycle, which is already amplified. The authors reported sensitivities of 667 mV/pH after 10 cycles, and 5048 mV/pH after 100 cycles.

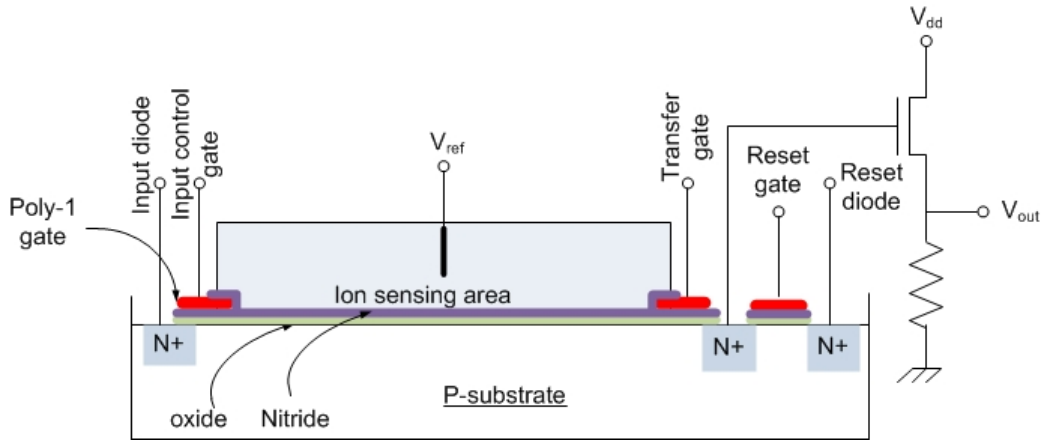


Figure 5.1: Schematic of the charge transfer type pH sensor presented in [3].

This is a beautiful technique featuring high amplification in CMOS. It demonstrated sensing chemical signals as small as 0.08 pH units. However, in this configuration the MIS was not used in a standard ISFET structure. Its operation is rather based on a complete different terminology. It was used as a control gate to modulate the underlying potential well that in-turn controls the amount of charges that move between the input and output deeper potential wells. This is effectively a charge Transfer device (CTD) structure [5].

This method is very similar to CCD light sensor output amplification techniques [6]. Thus, it needs a whole system built around the MIS that is composed of an input and output transfer gates, a reset gate, an amplifier, plus the clocking and control circuits around them. Moreover, this technique is normally power hungry because the output amplifier is biased in such a way to draw current at all times, though nothing was mentioned about power in both papers. The value of V_{ref} was not mentioned in both papers, however, according to CTD operation, it should provide large enough potential to allow V_{chem} to modulate the potential well in the channel underneath the ion sensitive area. Finally, drift was ignored, especially for the measurement of the 0.08 pH signal.

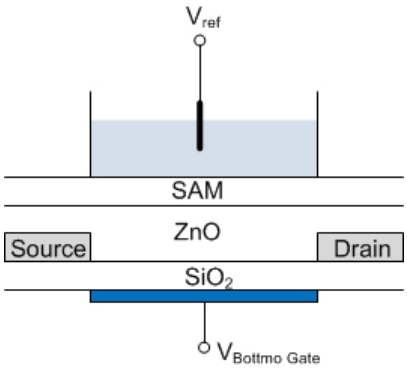


Figure 5.2: Dual gate ZnO ISFET proposed in [7].

Another idea was presented in [7] and [8]. A special process was used to build a dual gate ion sensitive structure using ZnO semiconductor on SiO_2 insulator across which an electrical bottom gate was coupled, figure 5.2. The top ion sensitive gate was made by self applied mono-layer (SAM) of "octadecylphosphnic" acid that passivated the ZnO forming a large area of the ion sensitive membrane. That article reported a sensitivity, referred to the back gate, of $2.25V/pH$. It was explained that realized amplification was due to the ratio of the electrolyte's coupling capacitance, across the ions sensing membrane; to the back gate capacitance though correlation was not shown by example. That device was fabricated using a special process and material. It is not CMOS compatible and it may not suitable for mass production.

Another device was reported by Zehfroosh et al in [9]. A 300 mV/pH ISFET was fabricated using Nano-porous silicon as the insulator and ion sensitive membrane directly on top of the poly-silicon gate. This hugely increased the ion sensitive area which resulted in higher sensitivity , the authors explained. It was observed that, pH sensitivity largely depended on biasing and drain current value. Therefore, in order to fit experimental data, the authors, proposed a charge insertion factor as a function of porosity level and electrolyte's pH. However, This device is not compatible to standard CMOS processing. Moreover, its pH sensitivity depends on its biasing point and porosity degree of the

nano-porous silicon.

In [10], Liu and Zhou suggested to operate the ISFET in the so called depletion operation condition (DOC). This was justified by the gate oxide having its minimum capacitance, and thus its maximum sensitivity, in this point. The proposal was to dope the gate oxide in order to enhance the slope of the gate voltage relation with gate charge. It was explained that: proper gate oxide doping and operation in this region may result in a sensor sensitivity that corresponds to about $1mV$ gate voltage change due to 1 electron per μm^2. This is a huge sensitivity that is not backed by experimental results. However, this device is not CMOS compatible. Moreover, it is wondered how it will behave under drift.

An ultra sensitive charge sensor based on field effect transistor was proposed by Shao and Wang in [11]. It was proposed to use a nMOS structure where the gate is replaced by a poly-silicon grid isolated by two oxide layers: one on top of it and the second under it, as a gate oxide, figure 5.3. Each of these three layers were $5nm$ thick. This proposed device was $0.22\mu m$ wide and the length was not mentioned, as it was a two dimensional simulation. $0.1\mu m$ of the top oxide was covered by a control gate while $0.12\mu m$ was open for ion detection. The control gate was used to place the transistor in DOC, that was proposed in [10]. The advantage of this device over the previous is using DOC operation without doping the gate oxide. However, source and drain were assumed highly doped. That paper reported a drain current change of $0.4\mu A$ for every electron per μm^2, in the most sensitive part. Simulations were done using COMSOL Muliphysics 3.4. No experimental results were presented.

However, in the opinion of the author of this thesis, that simulation has an issue. The gate voltage was assumed $0V$ and the control gate voltage was assumed $5V$ with a silicon oxide isolation of $5nm$ thickness. This results in an electrical filed of $1 \times 10^9\ V/m = 1\ V/nm$ in the top oxide. This is well within the range for electron tunnelling [12].

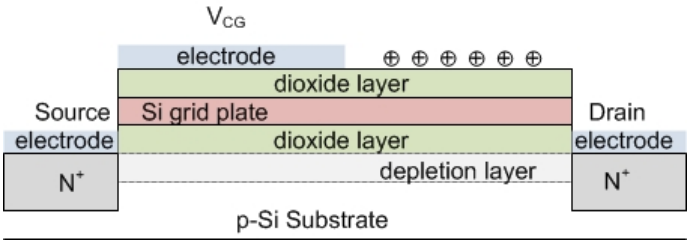


Figure 5.3: Ultra-sensitive filed effect charge sensor proposed in [11].

Therefore, the assumption of the gate being floating, no longer holds. Simulations need to account for that. That is believed to be one of those simulations that produce nice results but will not work in real life because important factors were ignored.

Exploiting ISFETs floating gate nature; more inputs can be coupled to its floating gate. In [13] and [14], Liu et al used an ISFET in a feedback loop of an auto-zeroing amplifier. It had two capacitively coupled inputs to its floating gate, namely: evaluation and sense nodes. In this ingenious method, the evaluation node was used to read the initial state of the ISFET, where it is stored in a capacitor in order to use it as a reference to compensate for trapped charges and drift. Then, the sensing node was used for reading the chemical signal. A differential amplifier read the change in the ISFET signal. This looks like correlated double sampling where the analogue sampled level is stored in a capacitor. After successive readings and corrections, sensitivities of 200 mV/pH in [14] and 100 mV/pH in [13] were reported.

That circuit was built in standard CMOS process without additional steps. However, it needed a large storage capacitor, an amplifier, and a number of switches along with their clocking circuits. It had the additional advantage of drift and trapped charges compensation. Amplification was attributed to capacitance coupling ratio without giving any details or explaining why the two circuits differ in their amplification.

Another method of programmable gate (PG-ISFET) sensitivity amplification (scaling) in CMOS is presented here. Simply, a second electrical input to the ISFETs floating

Table 5.1: Summery of reported high sensitivity semiconductor ion sensors.

reference	method	sensitivity
[3]	CTD single input gate	$1.13V/pH$ after 5 cycles
[4]	CTD two input gates	$5.048V/ph$ after 100 cycles
[7]	back and front capacitances ratio	$2.25V/pH$
[9]	nano porous Si for capacitance ratio	$300mV/pH$
[10]	DOC (special device)	$1mV$ for each electron/μm^2
[11]	monolithic DOC (special device)	$0.4\mu A$ for each electron/μm^2
[13], [14]	switching capacitances ratio	$200mV/pH$ and $300mV/pH$

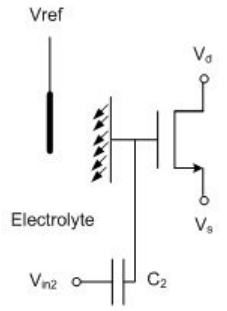


Figure 5.4: ISFET model in CMOS.

gate aiming to enhance its pH sensitivity referred to this input was successfully designed, built, and tested.

5.3 High gain νMOS ISFET

In chapter 3, it was shown that ISFETs in standard CMOS process are floating gate devices. Their chemical chemical model is reproduced here for convenience:

$$V_{chem} = \gamma + 2.3\alpha U_T pH \tag{5.1}$$

where, γ is a grouping of all pH independent terms. U_T is the thermal voltage, and α is a sensitivity parameter ranging between 0 and 1. Its maximum results in the above mentioned Nerstian limit. Devices built in CMOS generally have sub-Nerstian

sensitivity which is accounted for by the introduction of α in this equation [1]. A typical value of α is about 0.5 for SiO_2 ion sensing membrane [15].

In the ISFET of figure 5.4, a second input (V_{in2}) is capacitively coupled to the floating gate via a poly1-poly2 capacitor (C_2). It is modelled as in figure 5.5. According to floating gate and νMOS concepts [16], the floating gate voltage may be found by charge conservation to be:

$$V_{fg} = \frac{C_{pass}}{C_T}(V_{chem} + V_{ref}) + \frac{C_2}{C_T}V_{in2} + \frac{V_d C_{gd} + V_s C_{gs} + V_b C_{gb}}{C_T} + \frac{Q_{TC}}{C_T} \qquad (5.2)$$

Where ($V_d C_{gd},\ V_s C_{gs},\ and\ V_b C_{gb}$) are the transistor's drain, source and body voltages, referred to ground, multiplied by their respective gate capacitances. C_T is the total capacitance seen by the floating gate. It includes all parasitics that are ignored in equation 5.2. It is clear that C_{pass} should be maximized in order for C_{pass}/C_T to approach unity.

ISFET's sensitivity is normally defined as the chemical voltage change per unit pH. That was the case for the usual ISFETs where the gate voltage was solely defined by ($V_{chem} + V_{ref}$) since there was no floating gate. However, it is more practical to define it here as the floating gate voltage change per unit pH. Using equations 5.1 and 5.2 gives:

$$V_{fg}\ sensitivity\ to\ pH = \frac{dV_{fg}}{dpH} = \frac{C_{pass}}{C_T} 2.3\alpha U_T \quad V/pH \qquad (5.3)$$

As V_{chem} is not the only input to the floating gate, it makes sense to find its sensitivities to other inputs. Namely,

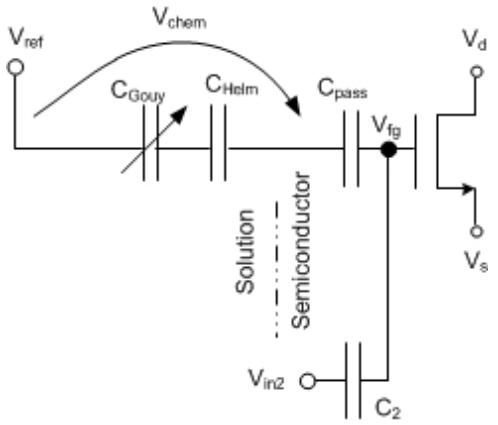


Figure 5.5: High gain minimum component ISFET model.

$$V_{fg}\ sensitivity\ to\ V_{ref} = \frac{dV_{fg}}{dV_{ref}} = \frac{C_{pass}}{C_T}$$
$$V_{fg}\ sensitivity\ to\ V_{in2} = \frac{dV_{fg}}{dV_{in2}} = \frac{C_2}{C_T} \tag{5.4}$$

It is not possible to directly measure the floating gate voltage by probing it. Nevertheless, what matters is its pH sensitivity. One way to measure this is to refer V_{fg} to one of the electrical inputs and use I_d as a marker [17]. That is, for fixed drain-source voltage (V_{ds}) and the same drain current (I_d), the transistor has the same floating gate voltage regardless of its region of operation. Thus, fixing V_{ds} and sweeping one of the inputs, V_{ref} for example while keeping V_{in2} constant, an arbitrary drain current can be chosen as a fixed point indication of V_{fg} for the value of pH in use. Then, for another pH value, the same process is repeated and a new V_{ref} value is found that will result in the same I_d chosen before. This gives how much change in V_{ref} will compensate for that pH change and corresponds to it. This is effectively pH sensitivity as seen by V_{ref}, in other words it is pH sensitivity referred to V_{ref}. That is:

$$pH\ sensitivity\ referred\ to\ V_{ref} = \frac{dV_{fg}}{dpH} \times \frac{dV_{ref}}{dV_{fg}} = 2.3\alpha U_T \quad V/pH \tag{5.5}$$

From equation 5.3, it is clear that V_{fg} sensitivity to pH is scaled down by C_{pass}/C_T compared to a standard ISFET. However, as in equation 5.5 when referring it to V_{ref}, the scaling cancels. This is expected as both are coupled via the ame cpacitance and have the same scaling. Thus, V_{ref} is a one to one measure of the chemical voltage change as they are scaled by the same factor. This is how ISFET's pH sensitivity is generally measured and reported in literature, where usually V_{ref} is the only electrical input to the ISFET's floating gate.

The point of the device reported here, figure 5.4, is providing a second input that can be used in a similar way as V_{ref} with the added advantage of having a different weight on the floating gate. Defining pH sensitivity referred to V_{in2}, in the same way it is defined when referred to V_{ref}, is the key of pH sensitivity scaling. This circuit is very similar to the programmable gate PG-ISFET proposed in [18]. Though, in that device, the electrical second input was used to shift the ISFET's threshold voltage (V_t) in order to compensate for its variations due to trapped charges. That is why its coupling capacitance was large to maximised its V_t control effect. V_{ref} was the main input.

However, in the proposed device here, V_{in2} is used as the main input that has scaled sensitivity and V_{ref} can be used to set the suitable point of operation.

Therefore, referring pH sensitivity to V_{in2}, by using equations 5.3 and 5.4 gives:

$$pH \;\; sensitivity \;\; referred \;\; to \;\; V_{in2} = \frac{dV_{fg}}{dpH} \times \frac{dV_{in2}}{dV_{fg}} = \frac{C_{pass}}{C_2} 2.3\alpha U_T \;\; V/pH \qquad (5.6)$$

Here, the capacitance ratio C_{pass}/C_2 works as a scaling that can be designed.

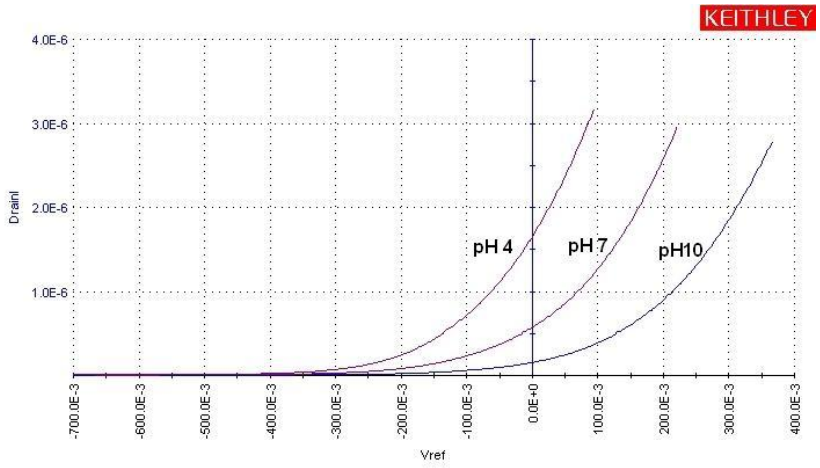


Figure 5.6: Measured $I_d - V_{ref}$ curves for high gain minimum component ISFET for pH 4,7, and 10

5.3.1 Measured results

The device of figure 5.4 was built using a commercial AMS $0.35\mu m$ process. The nMOS-ISFET's gate had a width of $3\mu m$ and length of $0.35\mu m$. The chemical sensitive area was $32 \times 62.5\mu m^2$. According to process parameters, C_{pass} was found to be $\approx 35.8fF$ [19]. And C_2 was designed to have poly1-poly2 overlap area of $2.6\mu m^2$ which results in a capacitance of $\approx 3fF$. Poly-poly capacitor was chosen because it gives finer capacitance resolution and tighter processing tolerance compared to metal capacitors provided by the same process [19]. In the design phase, a scaling of 10.75 was expected for this C_{pass}/C_2 ratio. Which was the design objective here. C_{pass} was chosen about ten times the total of all other capacitances coupled to the floating gate. This makes it dominant in order to maximise the coupling weight of V_{chem}.

The device was measured using pH 4.0, 7.0, and 10.0 buffer solutions from Hanna chemicals. A silver/silver chloride reference electrode was used to supply V_{ref}. Keithley Semiconductor Characterization System Model 4200-SCS was used for the measurements. The ISFET was biased with $V_{ds} = 0.5V$, source and body were grounded to

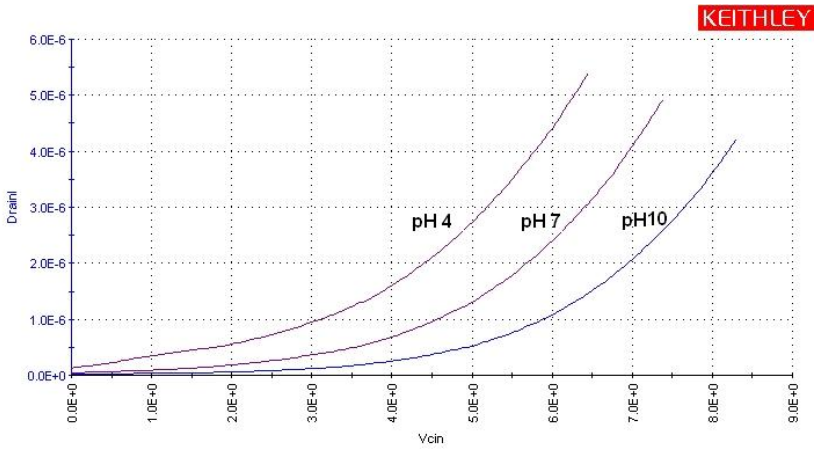


Figure 5.7: Measured $I_d - V_{in2}$ curves for high gain minimum component ISFET for pH 4,7, and 10

Table 5.2: Measured V_{ref}, and V_{in2} that gave $I_d = 1\mu A$ for different buffer solutions.

Input variable	pH 4.0	pH 7.0	pH 10.0	Sensitivity
$V_{ref}, V_{in2} = 0.0V$	-63 mV	69 mV	214 mV	46.17
$V_{in2}, V_{ref} = 300mV$	3.12 V	4.575 V	5.875 V	459.17

nullify their effects on V_{fg}. The drain current of $1\mu A$ was chosen as the fixed I_d point of reference it ensures the transistors are in the low power weak inversion region of operation [20]. However, choosing a higher current would give similar results because current is used as an indication of V_{fg} with fixed V_{ds}.

Fixing V_{in2} to ground and sweeping V_{ref} for the three buffer solutions, the set of curves in figure 5.6 were the result. Overall sensitivity was 46.17 mV/pH. Then, V_{ref} was set to 300 mV and V_{in2} was swept in a similar way giving the curves of figure 5.7. The measured sensitivity was 459.17 mV/pH. Table 5.2 summarizes the numbers. The sensitivity was scaled by 9.95 times, which is within 7.5% of designed value.

5.3.2 Noise

In chapter 3, it was shown that an ISFET noise referred to its floating gate is given by:

$$\overline{V_{nISFET}}^2 = \frac{8kT}{3g_m} + \frac{K_f}{WLC_{ox}f} + \frac{C_{pass}}{C_T}\frac{K_{chem}}{f} \tag{5.7}$$

The noise model of a capacitor is a parallel RC circuit with the thermal noise given by

$$\bar{V}_C^2 = kT/C$$

. Here k is Boltzman constant, T absolute temperature. It is normally negligible compared to other noise sources in the circuit [21]. This is particularly evident for limited frequency range, like the case here [20]. Thus, assuming capacitors are effectively noiseless passive components, equation 5.7 also represents noise in the structure discussed here. Referring it to the electrical input V_{in2} by accounting for capacitive coupling, it becomes:

$$\overline{V_{nISFET}}^2 = \frac{C_T}{C_2}\frac{8kT}{3g_m} + \frac{C_T}{C_2}\frac{K_f}{WLC_{ox}f} + \frac{C_{pass}}{C_2}\frac{K_{chem}}{f} \tag{5.8}$$

This may look very bad as V_{in2} sees a scaled version of the total ISFET noise. It is true that noise is scaled by the capacitor ratios but the floating gate sees no increase in noise. Therefore, there is no noise improvement or degradation in using V_{in2}. However, being an electrical input completely within silicon, it has an additional degree of freedom in the choice of its value adding more features to the ISFET. Moreover, frequency can be chosen to reduce total $1/f$ noise. Both the chemical input signal and chemical noise are scaled by C_{pass}/C_2 as seen by $Vin2$, equations 5.6 and 5.8. However, the transistor noise is scaled up by C_T/C_2, equation 5.8, which is higher as generally $C_T > C_{pass}$. This indicates a reduced dynamic range. But, this reduction is minimised if C_{pass} is made the largest in the circuit.

5.4 High gain ISFET based νMOS chemical inverter

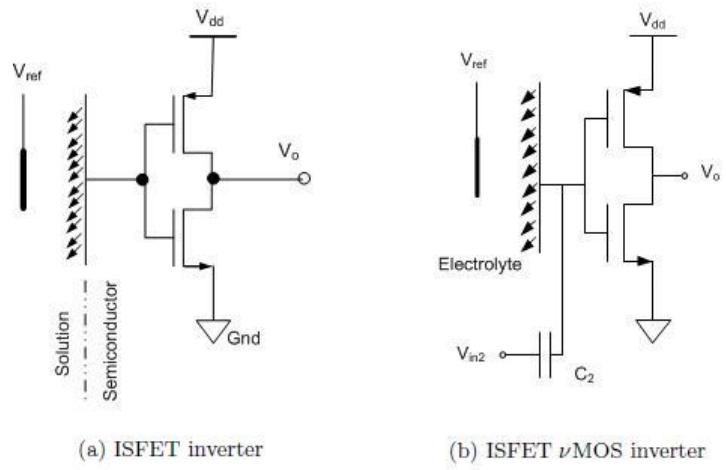
Exploiting FG-MOS nature of ISFETs a chemical inverter was reported in [22] and presented in chapter 4. The sensitivity of that particular example was about 30mV/pH. Using such a circuit for applications that need yes/no answer is faster, needs small silicon area, and low power than a similarly biased analogue systems. However, pH changes of about 0.1 units were needed to cause ripple free switching, which is more than the target of 0.02 units as mentioned in chapter 4. Therefore, it is desirable to build high sensitivity chemical switches that will change state due to small pH changes. This enhances measurement sensitivities and relaxes constraints on sample volumes and concentrations.

It is proposed in this work to further exploit FG-MOS and νMOS techniques by adding an electrical second input to that inverter. The ratio of passivation capacitance; that couples chemical signal to the inverter's floating gate, and the second input's coupling capacitance can serve as a scaling ratio. Such a slight modification of the circuit may scale its pH sensitivity by orders of magnitudes.

In the configuration of the ISFET based chemical switch presented in chapter 4, two ISFETs: an nMOS and a pMOS, shared the same floating gate, in a standard floating gate inverter configuration; figure 5.8-a, reprinted here to compare it with the proposed circuit.

The circuit presented here expands on that idea by introducing a second input that is capacitively coupled to the floating gate of the inverter of figure 5.8a resulting in the circuit of figure 5.8b.

This is effectively a floating gate MOS inverter with two inputs. Namely the ion sensitive input coupled through passivation capacitance (C_{pass}) and the second input (V_{in2})



(a) ISFET inverter (b) ISFET νMOS inverter

Figure 5.8: (a)ISFET based chemical inverter, and (b) high gain νMOS chemical inverter.

coupled through a poly1 - poly2 capacitance (C_2). The resultant floating gate voltage is the weighted sum of these two inputs, which is in agreement with the νMOS concept [16] [23] [24].

By choosing to make the second input's capacitance (C_2) very small compared to passivation capacitance (C_{pass}), it is possible to use this input (V_{in2}) as the inverter's electrical input while the chemical signal is used as a control gate. Thus, the switching point referred to V_{in2} becomes very sensitive to pH changes. In fact, it is a scaled version of the pH sensitivity referred to V_{ref}. As in the single transistor case, the ratio C_{pass}/C_2 is the scaling of pH sensitivity referred to V_{in2}. Choosing the value of C_2 should be dictated by application requirements.

5.4.1 Analysis

The circuit of figure 5.8b can be operated in both strong and weak inversion. The latter is more suited for low power operation which is a requirement for biomedical implantable

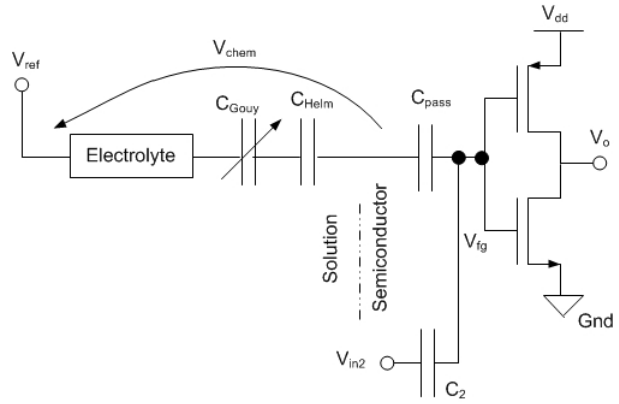


Figure 5.9: Model of high gain ISFET based νMOS chemical inverter

devices and a plus for hand held equipment. The discussion presented here holds for both modes of operation. The difference is only in the switching point that depends on the transistors' region of operation during switching.

Figure 5.9 is the model of the proposed high gain ISFET based νMOS chemical switch. Since a number of nodes are capacitively coupled to the floating gate, its potential is defined by the weighted sum of all inputs [16]. The floating gate voltage (V_{fg}) is given by:

$$V_{fg} = \frac{C_{pass}}{C_T}(V_{chem} + V_{ref}) + \frac{C_2}{C_T}V_{in2} + \frac{(VC_{MOS_n} + VC_{MOS_p})}{C_T} \tag{5.9}$$

Where:

$$VC_{MOS_n} = V_{D_n}C_{GD_n} + V_{S_n}C_{GS_n} + V_{B_n}C_{GB_n} \qquad \text{and}$$

$$VC_{MOS_p} = V_{D_p}C_{GD_p} + V_{S_p}C_{GS_p} + V_{B_p}C_{GB_p}$$

The suffix "n" stands for nMOS and the suffix "p" stands for pMOS. C_{pass} is the passivation capacitance, V_{chem} is the pH dependent chemical voltage modelled by equation 5.1. C_T is the total capacitance seen by the floating gate. It includes all other parasitic capacitances that are ignored here. The floating gate is assumed to have no trapped charges.

From equation 5.9, the factor C_{pass}/C_T scales down the effect of V_{chem} and hence pH sensitivity. This is one reason for sub-Nernstian sensitivity of ISFETs built with standard CMOS processes. It can be made close to unity by maximizing C_{pass}/C_T ratio. That is by designing the passivation capacitance much larger than the sum of all other capacitances in the circuit.

The second term of equation 5.9 is the second input (V_{in2}) scaled down by C_2/C_T. Thus minimizing C_2 allows more room for chemical sensitivity. In the same time increasing it gives V_{in2} more effect in the floating gate voltage. Thus, the ratios of these capacitances and the total floating gate capacitance are design decisions that should be addressed as appropriate.

The intrinsic inverter, operating in either strong or weak inversion, has its switching threshold voltage (V_{sth}) when both transistors have the same current and the output equals the input [25]. This was shown in the chapter 4. It is reproduced here for convenience:

$$V_{sth} = \begin{cases} \frac{r(V_{dd}-|V_{tp}|)+V_{tn}}{1+r} & \text{strong inversion} \\ \\ \frac{V_{dd}-|V_{tp}|+ln\left(\frac{I_{sn}}{I_{sp}}\right)V_{tn}}{1+ln\left(\frac{I_{sn}}{I_{sp}}\right)} & \text{weak inversion} \end{cases} \tag{5.10}$$

Where

$$r = \sqrt{\frac{k_p}{k_n}} \quad , \quad k_n = \mu_n \times C_{ox} \quad and \quad k_p = \mu_p \times C_{ox}$$

Where, V_{tn} and V_{tp} are threshold voltages, I_{sn} and I_{sp} are the specific currents of the nMOS and pMOS transistors respectively. This switching threshold voltage in equation 5.10 depends only on MOS parameters and the rail voltage, for all regions of operation. Switching occurs when V_{fg} changes across V_{sth} going higher or lower than it.

Since, the floating gate voltage is a function of its coupled voltages as in equation 5.9, they collectively decide the switching point. But, V_{chem} is only one of these inputs.

Thus, defining the inverter's pH sensitivity is not as straight forward as the single transistor case.

pH sensitivity can be defined as the pH induced shift in V_{fg}. But, this is difficult to measure as there is no direct access to it. Moreover, measuring the circuit's output does not help much since it quickly hits one of the rails. The single transistor case is easier in the sense that there is a continuum of output values, so shifts can easily be found. However, it is possible here to associate it with switching point change. Simply because switching occurs when $V_{fg} = V_{sth}$ which is a constant. Thus shifts in V_{fg} are manifested as switching point shifts as seen by the inputs. Thus, V_{fg} shift due to pH change may be referred to one of the electrical inputs; namely: V_{ref} or V_{in2}. Therefore, pH sensitivity is manifested as the shift in the switching voltage, due to pH change, as seen by sweeping either one of V_{ref} or V_{in2} while keeping the other constant.

Referring to equations 5.1 and 5.9, the floating gate voltage pH sensitivity of this inverter for pH referred to V_{ref}, while V_{in2} is kept constant; is found by:

$$V_{fg}\ sensitivity\ to\ pH\ =\ \frac{dV_{fg}}{dpH} = \frac{C_{pass}}{C_T} 2.3U_T\ \ V/pH \tag{5.11}$$

But, for constant pH and V_{in2}

$$V_{fg}\ sensitivity\ to\ V_{ref}\ =\ \frac{dV_{fg}}{dV_{ref}}\ =\ \frac{C_{pass}}{C_T}$$

Thus,

$$V_{fg}\ \ sensitivity\ to\ pH\ referred\ to\ V_{ref} = \frac{dV_{fg}}{dpH} \times \frac{dV_{ref}}{dV_{fg}}\ = 2.3\alpha U_T \quad V/pH \tag{5.12}$$

Therefore, despite the fact that the effect of V_{ref} on V_{fg} is scaled down by the ratio C_{pass}/C_T; the pH sensitivity when referred to V_{ref} is not. That is because V_{chem} itself

is scaled down by the same ratio. The scaling cancels out. It is worth noting that V_{ref} change has equivalent effect on V_{fg} as V_{chem} change. It is a one to one relation that is linear with respect to pH.

However, if V_{in2} is used to shift V_{fg} while V_{ref} is fixed, then:

$$V_{fg}\ sensitivity\ to\ V_{in2} \ = \ \frac{dV_{fg}}{dV_{in2}} \ = \ \frac{C_2}{C_T}$$

Thus,

$$V_{fg}\ \ sensitivity\ to\ pH\ referred\ to\ V_{in2} = \ \frac{dV_{fg}}{dpH} \times \frac{dV_{in2}}{dV_{fg}} \ = \ \frac{C_{pass}}{C_2} 2.3U_T \quad V/pH \quad (5.13)$$

Therefore, if V_{in2} is used as the input where V_{ref} is kept constant and the chemical input plays the role of a control gate that shifts the switching point, then the circuit's pH sensitivity referred to V_{in2} is scaled up by C_{pass}/C_2. It is still a linear relation to pH change, but with a different slope.

It is possible to set the ratio C_{pass}/C_2 at design time. Then, using V_{in2} as the inverter's electrical input, the coupling weight is used to enhance pH sensitivity by this ratio compared to the case of V_{ref}. Without using amplifiers or additional circuitry, pH sensitivity is scaled up.

5.4.2 Simulation results

Using a Verilog-A model based on equation 5.1, the circuit of figure 5.8b was simulated in cadence according to the design kit of the standard AMS $0.35\mu m$ process that was used to manufacture the devices. The high sensitivity νMOS inverter dimensions used in simulations were used to build the circuit. The output was buffered by two MOS inverters increasing in size in order to provide enough current to drive the load introduced

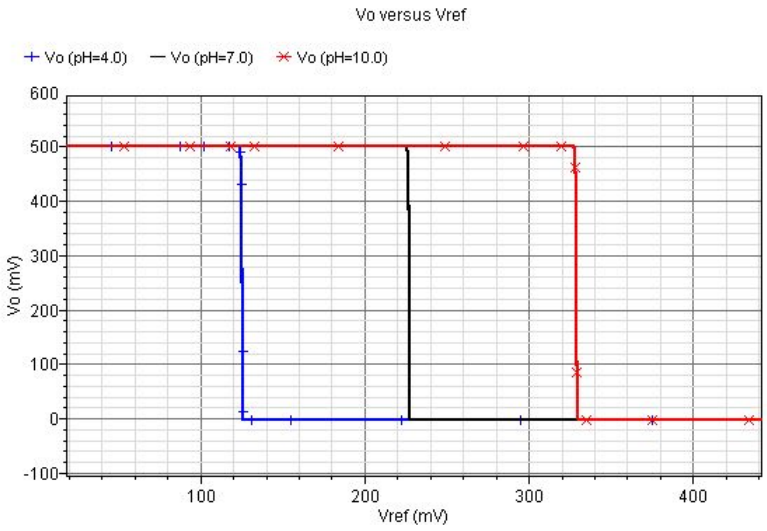


Figure 5.10: Simulated output for the high gain ISFET based MOS chemical inverter, V_{ref} sweeps with constant V_{in2}, and pH = 4, 7, 10.

by the bond-pad and test PCB. For simulations, 35 mV/pH single ISFET sensitivity was assumed. This is reasonable according to measured data for devices built with this technology [26] [27] and reported in chapter 4.

According to the manufacturing process parameters, the threshold voltage of the nMOS device is $0.59V$. And for the pMOS device it is $-0.72V$ [19]. Therefore, using V_{dd} of $0.5V$ insures sub-threshold operation during switching by capping the rail to rail voltage to less than transistors' threshold voltages.

V_{ref} was swept to find its value that causes switching ($V_{ref_{sth}}$). The pH of the electrolyte was stepped through 4.0, 7.0, and 10.0. V_{in2} was kept at zero volts. The output is shown in figure 5.10. The simulated sensitivity was:

$$\frac{dV_{ref_{sth}}}{dpH} = 33.9 \quad mV/pH$$

Therefore, from equations 5.1 and 5.9, shifting V_{ref} by 33.9 mV corresponds to elec-

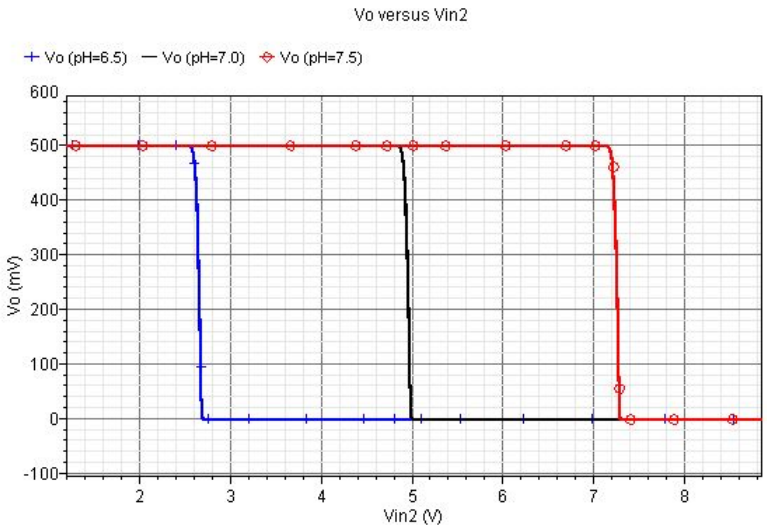


Figure 5.11: Simulated output for the high gain ISFET based νMOS chemical inverter, V_{in2} sweeps with constant V_{ref}, and pH = 6.5, 7, 7.5.

trolytes pH change of one unit.

For the traces in figure 5.11, V_{ref} was kept constant at the verge of switching while V_{in2} was swept to find the switching point ($V_{in2_{sth}}$) for pH values of 6.5, 7.0, and 7.5. The resultant sensitivity was

$$\frac{dV_{in2_{sth}}}{dpH} = 4.6 \quad V/pH$$

This is a high and promising input referred sensitivity provided noise is not a limitation. This is within 3% of expected value; as $C_{pass} \approx 420fF$ and $C_2 \approx 3fF$ which gives a scaling factor of $C_{pass}/C_2 \approx 140$ [19]. Thus, using dV_{ref}/dpH, the expected pH sensitivity referred to V_{in2} is $(C_{pass}/C_2) \times 33.9 \times 10^{-3} = 4.7\ V/pH$. The small difference is attributed to parasitics that are included in simulations but excluded in hand calculation. An interesting point to note here is $V_{dd} = 0.5V$ which means that about $0.1pH$ corresponds to V_{in2} going from ground to V_{dd}.

Finally, the graph of figure 5.12 shows the switching point change due to sweeping V_{in2}

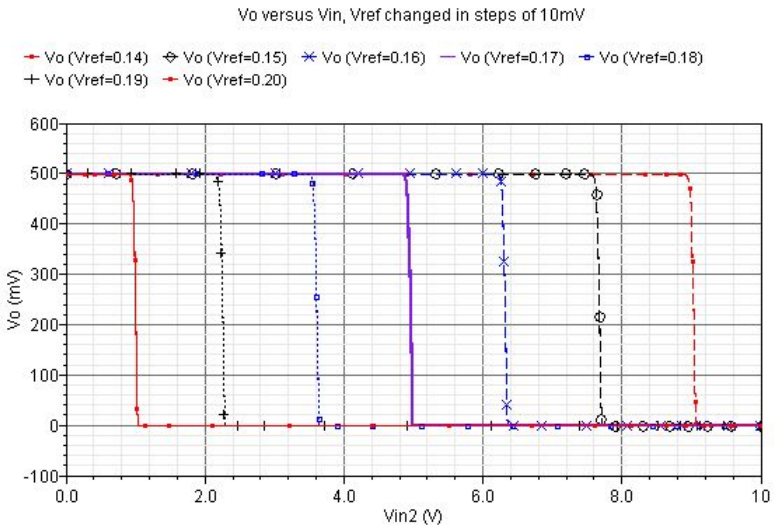


Figure 5.12: Simulated output for the high gain ISFET based νMOS chemical inverter, V_{in2} sweeps, V_{ref} stepped at 10 mV, and pH=7.

while pH is fixed. V_{ref} is changed in $10mV$ steps. The relation between their changes is:

$$\frac{dV_{in2}}{dV_{ref}} = -141.5$$

There is no need to talk about the minimum pH change that can trigger switching. This circuit sensitivity is very high when referred to V_{in2}. According to simulations, 0.01 pH change can trigger switching. However, it is very difficult to measure such a value in lab environment; especially when V_{ref} has to put the circuit in its most sensitive region, at the verge of switching. Therefore, the question is: what range of pH change is of interest.

5.4.3 Experimental results

The high gain ISFET based νMOS chemical inverter was designed and built using a commercial AMS $0.35\mu m$ process through Euro-practice. The nMOS had a width of $4\mu m$ and the pMOSs width was $12\mu m$. The output was buffered by two MOS inverters.

The chemical sensitive area was $95 \times 200\mu m^2$. According to process parameters, C_{pass} was found to be $\approx 420fF$. And C_2 was designed to have ply1 - poly2 overlap area of $2.8\mu m^2$ which results in a capacitance of $\approx 3.0fF$ [19]. Poly capacitor was chosen because it gives finer capacitance resolution and tighter processing tolerance compared to metal capacitors provided by the same process.

A single junction Ag/AgCl glass reference electrode was immersed in the electrolyte under test in order to apply V_{ref}. It was chosen because of its stable junction voltage. During titration experiments, the solution was placed on a magnetic stirrer and the pH of the buffer solution was modified by pipetting either HCl or $NaOH$ solutions of $0.1M$ each. After titration, the pH was measured using a Seven-Eleven temperature compensated glass pH meter from Mettler-Toledo. Keithley Semiconductor Characterization System Model 4200-SCS was used for the measurements. The die was bonded on a PCB and carefully encapsulated using EPO-TEK T7139 epoxy with only the chemically sensitive areas exposed.

pH sensitivity referred to V_{ref}

The reference voltage was swept in order to find the value that caused switching for different pH values. V_{in2} was grounded during these measurements. Three inverters were built in the same die and measured together. The die was soaked in a pH buffer for 12 hours. Then, it was measured every 20 minutes, for 3 hours to confirm drift is less than $7mV/h$, the last measurement was reported. The solution's pH was measured to be 8.2. Then, using titration, HCl was pipetted and pH was brought down to 3.7. After that, V_{ref} was swept, the new switching point was found. Then, $NaOH$ was pipetted in a similar procedure until the pH became 10.95. Finally, another sweep of V_{ref} was done. The output of circuit-A is depicted in figure 5.13. Table 5.3 summarizes the findings for these three circuits.

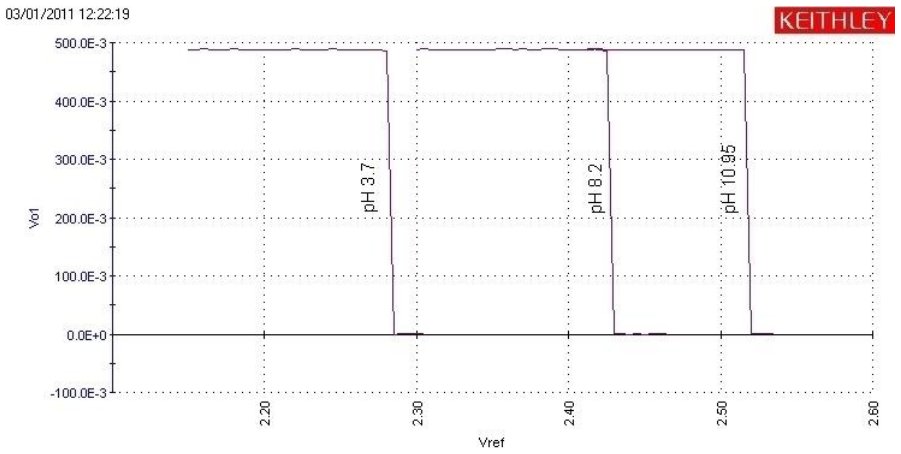


Figure 5.13: Measured V_{ref} referred pH sensitivity of the high gain ISFET based νMOS chemical inverter.

Table 5.3: Switching thresholds; by sweeping V_{ref}, for three circuits using three different pH values, $V_{in2} = 0$ V.

	$V_{ref_s}(V)$			overall pH
circuit	pH = 3.7	pH = 8.2	pH = 10.95	sensitivity (mV/pH)
A	2.285	2.430	2.505	30.34
B	2.17	2.340	2.395	31.03
C	2.255	2.400	2.490	32.41

Average measured sensitivity by sweeping V_{ref} was: $\Delta V_{ref}/\Delta pH = 31.26\ mV/pH$, which is slightly less than the simulated value reported earlier. This can be explained by less measured sensitivity or fabrication process variations. Nominal values were assumed in the simulations while actual measurements are reported here. Another point to notice is that V_{ref} is higher than V_{dd} and V_t of nMOS and pMOS. The circuit still operates in weak inversion regardless of this. That is because all that matters is the value of V_{fg} compared to V_{sth}, which is well below V_t of both transistors. The output will switch state only when V_{fg} crosses V_{sth} going higher or lower. More increase or decrease will not change the output state. The only reason such a high values were needed is to compensate for trapped charges.

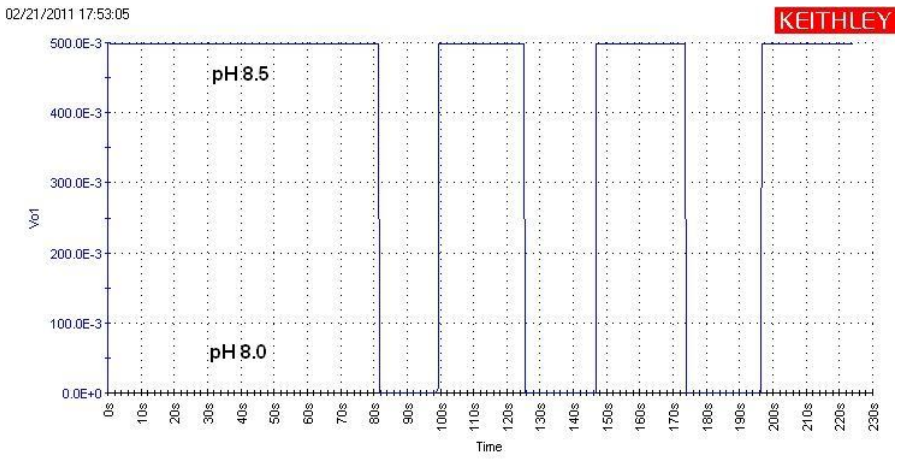


Figure 5.14: Switching by changing electrolyte's pH.

Switching due to pH change

In order to verify the switching operation driven by pH change alone, the following experiment was conducted. V_{ref} was fixed very close to switching threshold at pH of 8.5 with output logic high (H). V_{in2} was grounded. The solution's pH was changed by titrating $0.1M\ HCl$ that lowered the pH to 8.0 ± 0.1. Then it was raised again by titrating $0.1M\ NaOH$ in order to bring it back to pH 8.5 ± 0.1. The same process was repeated to cause switching sequence of ("H" $\rightarrow$ "L" $\rightarrow$ "H") three times. Titrations were 20 - 25 seconds apart as they were manually done using two different pipettes. The resulting curve is shown in figure 5.14.

This experiment was planned without pauses. It was not possible to use a pH probe to verify the actual pH of the solution between titration steps. Therefore, before conducting this experiment, a number of titration experiments were done with the same amount of starting buffer solution, $20ml$; and the pH meter alone. It is the aim to verify this circuit's operation for a pH change. Thus, it is the change that is important here, not exact pH values. The chosen pH range was large to insure that switching was solely due to it.

A Seven-Eleven temperature compensated glass pH meter from Mettler Toledo was used. The magnetic stirrer speed was kept constant throughout all experiments. The amount of pipetted HCl acid to change the solution's pH from 8.5 to 8.0 was recorded. Then the amount of $NaOH$ needed to bring it back to pH 8.5 was recorded. This was one titration cycle. A number of similar cycles were tabulated. As the solution's volume changed with each cycle, the amount of needed acid and base slightly changed. This made one experiment run. The whole procedure was repeated three times with a fresh solution for each. The amount of titrated acid and base for each cycle of the three experiments were tabulated and verified to be consistent; which gave confidence. Afterwards, the above switching experiment was performed using these recorded volumes for each step. The aim here is not to show minimum detectable pH change. The emphasis was rather to show that the circuit does work and within a short time frame as the whole process was done in less than 3 minutes. This is much faster than the glass electrode pH meter.

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pH sensitivity referred to V_{in2}

In order to test the use of the second input, pH was fixed and V_{ref} was set at the verge of switching in a new pH 7.0 buffer solution. V_{in2} was swept from $-5V$ to $+5V$ to find the value that causes switching. The chosen range was large because the coupling weight of this input is very small compared to the chemical input. The bond-pads had no ESD protection in order to allow for such high voltages. Though, the break down voltage for poly1-poly2 capacitor is $20V$, the normal maximum operating voltage for each terminal is $5.5V$ [19]. Therefore, the value 5V was chosen to be within normal operating range. Then V_{ref} was raised by $10mV$ and V_{in2} was swept again, and the process was repeated

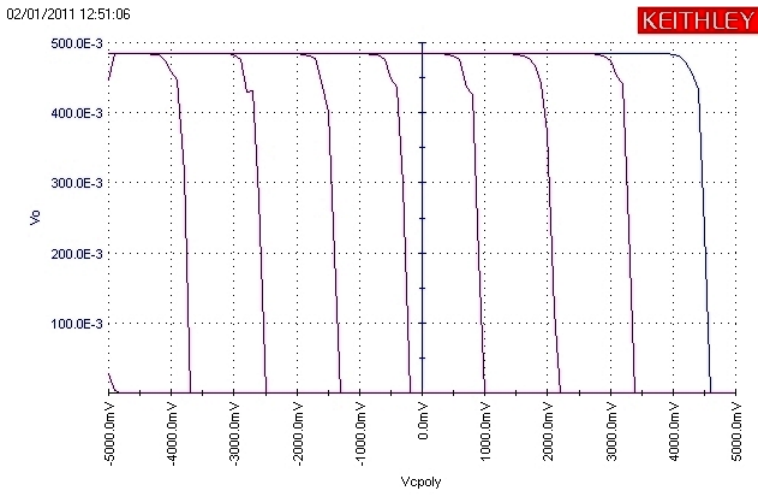

Figure 5.15: Sweeping V_{in2} for constant pH and V_{ref} increased in $10mV$ steps.

seven times. The group of curves of figure 5.15 was the result. The rightmost curve is for the lowest value of V_{ref} and the leftmost is for the highest value.

The relative change of $V_{in2_{sth}}$ due to V_{ref} change was found to be:

$$\Delta V_{in2_{sth}}/\Delta V_{ref} = (4.6 - (-3.7))/(-4.38 - (-4.31)) = -118.6$$

Reflecting this back to the change in pH yields:

$$-\Delta V_{in2_{sth}}/\Delta V_{ref} \times \Delta V_{ref}/\Delta pH = \Delta V_{in2_{sth}}/\Delta pH = 3.79V/pH$$

This is about 82.5% of the simulated value. However, it is within possible process variations and is consistent with the above measured sensitivities.

Dicussion

Though simulation and measurements presented here were for the weak inversion operation of the proposed circuit, strong inversion operation is possible. It was previously

presented for the ISFET based chemical switch in [22] and chapter 4. The choice of weak inversion is driven by its low power consumption which makes it suited for low power medical applications. It is clear that measured results agree with simulations within the limits of process variations.

Trapped floating gate charge was assumed zero during simulations. Clearly that was not the case in measurements. This is apparent from Table 5.3 as different switching points were measured for each inverter. However, this shows that the proposed circuit is immune to trapped charge variations and drift in the sense that it works regardless of their effects, which is manifested as shifting the switching point. Nevertheless, this can be a problem if an array of these devices is to have matched switching threshold voltages. This is a challenge for researchers. It would be beneficial to tackle it without additional manufacturing processing steps.

It is worth noting that the main source of uncertainty is passivation thickness that directly affects C_{pass}. Passivation, for this process, is composed of silicon nitride on top of silicon oxide. The former is $1000 \pm 200nm$ thick while the latter is $1030 \pm 100nm$ thick. This is already about 13% tolerance in the resulting capacitance. For standard CMOS circuits, passivations exact thickness is not important as long as it is enough to do its job of circuit protection. However, for ISFETs, it is one of the most important layers, the ion sensing membrane. By contrary, C_2 can be designed with higher accuracy using known capacitor matching layout techniques.

This device has similar operation principle as that proposed in [8]. However, that device used a back gate in a special non commercial process. While, the solution presented here is a simple monolithic device that can be built in a standard commercial CMOS process.

Though this work presents a promising highest measured input referred pH sensitivity,

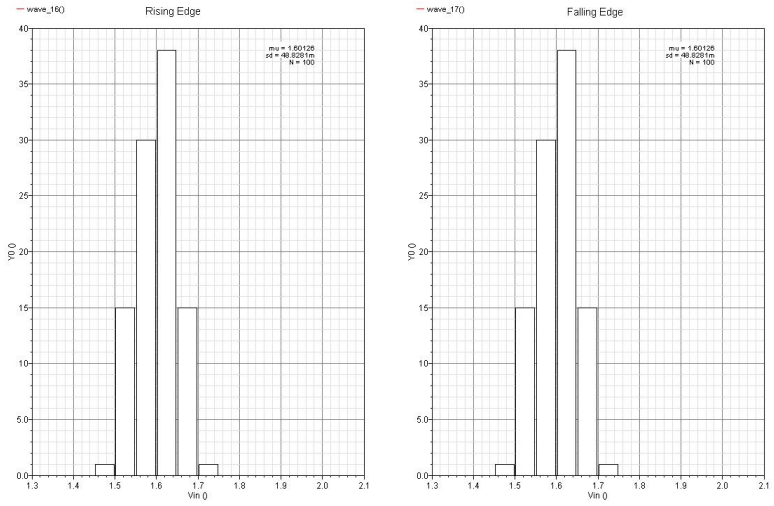

Figure 5.16: Mismatch and process variation Monte Carlo analysis for the νMOS inverter, V_{ref} sweeps.

it is clear this was not attained by improving ISFET's physical properties. It is rather reached by exploiting the floating gate nature of the ISFET built in unmodified CMOS process and the νMOS concept with different coupling capacitances. Noise is scaled the same way the chemical signal is, giving no increase SNR. It could be argued that using a amplifiers, similar or better results are attainable. However, that is not without extra price of area, power and complexity. The advantage here is the high gain without these associated costs.

The ISFET based chemical switch had no mismatch problems, so does its νMOS version when referred to V_{ref}, figure 5.16. However, when referred to V_{in2} it becomes very sensitive 5.17.

Accuracy here is process limited especially because it depends on capacitance values which are affected by area and both insulation thickness and physical properties. Particularly for C_{pass}, the second factor is very important. Exact C_2 sizing might place some constraints on array performance as it is the smallest capacitor in the circuit. Hav-

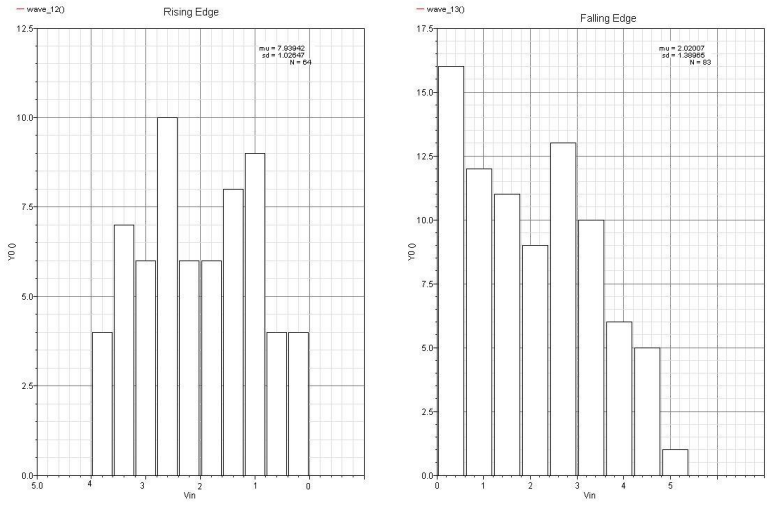

Figure 5.17: Mismatch and process variation Monte Carlo analysis for the νMOS inverter, V_{in2} sweeps.

ing exact areas is not easy especially for small capacitors. However, layout techniques can be used to reach reasonable accuracy.

By allowing two transistors to share the same ion sensitive area, it was possible to build the first complimentary all ISFET inverter. Exploiting the weighted sum of coupled inputs to the floating gate of this ISFET inverter, it was possible to increase its sensitivity more than a hundred fold. Simulations and experiments carried out here were only to demonstrate this technique. Capacitor sizes used here were only examples. Of course, circuit elements should be designed to suite the particular application they are intended for.

5.5 Conclusion

It was demonstrated in this chapter that by coupling a second input to an ISFET's floating gate, the ratio of passivation capacitance to its coupling capacitance works as

a scaling ratio for pH sensitivity referred to this input. No post processing steps are needed. For the single ISFET circuit built here, pH sensitivity was scaled by 10 times from 46.17 mV/pH, when referred to V_{ref}; to 459.17 mV/pH, when referred to V_{in2}.

This method provides basis for high sensitivity ISFET circuits. It is particularly useful in applications where it is desirable to fix the voltage applied to the chemical sample (V_{ref}). for example, it may be grounded to avoid any effect applied voltage may have on the chemical reaction of interest.

Applying this idea to ISFET based chemical switches, a second electrical input (V_{in2}) was capacitively coupled to the floating gate. Through properly sizing the coupling capacitances, it was possible to enhance pH sensitivity referred to this input about a hundredfold. This forms a high gain ISFET based νMOS chemical inverter with enhanced input referred sensitivity.

This circuit was simulated, built, and tested. The switching threshold voltage; referred to reference electrode, shifted by 31.26 mV per pH. This was increased to 3.7 V/pH when referred to V_{in2}. This is a very high chemical signal scaling for such a minimum component ISFET circuit.

This was attainable through properly sizing the capacitors ratio. There was no need to use amplifiers or additional circuit elements that may increase noise, power dissipation, and circuit area. This circuit can be used in vast applications for pH thresholding. It provides basis for high sensitivity ISFET circuits that are entirely digital.

This circuit can be the basis for other FG logic circuits that use mixed types of signals as input: electrical and chemical or biological signals. For example a two input logical gate (AND, NAND, OR, NOR, XOR, or XNOR) may have one chemical input capacitively coupled through passivation layer. The second input is just a normal electronic logical signal that is capacitively coupled through a properly sized C_{in2}. Both pH sensitivity

and capacitance sizing define the pH change that corresponds to used logic levels.

For example, if $V_{dd} = 0.5V$, C_{pass}/C_2 can be chosen in such a way that a change of 0.5 pH unit corresponds to $0.5V$ when referred to V_{in2}. This way, a chemical change of 0.5 pH has the same weight on the logic gate as a change of the electrical input from rail to rail. Thus, both chemical and electrical inputs have similar weights for the FG-logic gate. Of course, mentioned V_{dd} value and pH change are only examples. Other combinations are possible. For the circuits tested above, 0.1 ph corresponded to a rail to rail change of 0.5 V on V_{in2}.

This circuit can be used to perform reaction monitoring and pH-thresholding operations for a reaction chamber with chemical or biological inputs. Its digital output can be used to build standard digital circuits with inputs being either electrical or coming from different reaction champers. This facilitates the construction of completely digital ISFET based lab on chip applications.

With feedback to the reference electrode, it is possible to change the switching threshold voltage to reflect the needed pH region of interest.

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Chapter 6

Bidirectional Tunnelling ISFET V_t Control and Matching

6.1 Introduction

FG-MOS and ISFETs, alike, suffer from floating gate trapped charges which can be seen as either V_{fg} shifts or threshold voltage (V_t) variations. This is a problem since it is difficult to design circuits without knowing V_t of its main sensing transistors. It is even more serious a problem for an array having a common reference. That problem is understood to be due to trapped charges in the floating gate and insulations around them [1]. Measurements from the previous two chapters clearly show this effect. In ISFETs, this problem has similar origins as that of floating gate transistors. In addition, passivation layer buried sites further complicate it [2]. These are caused by positively or negatively charged silicon centres that may bond with carriers in the silicon nitride or oxide [3].

Charges trapped in insulation layers introduce more polarisation to the ISFET's FG-

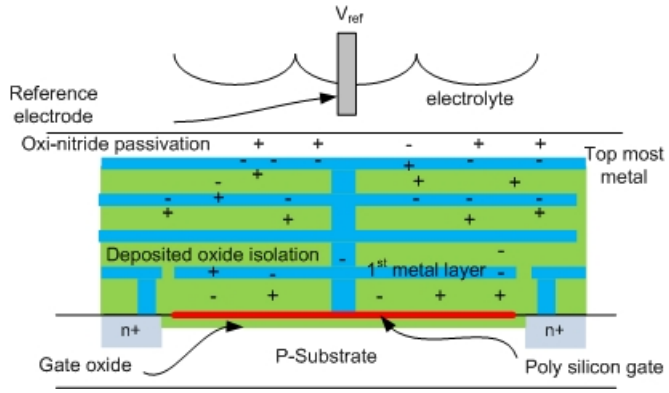

Figure 6.1: Cross section of ISFET built in CMOS technology.

MOS system which has to maintain charge neutrality [4]. Thus, they are opposed, within the system space charge, by an equal but opposite bound charges in either metal or semiconductor surfaces or both [3], figure 6.1. Therefore, the net effect is seen as an initial V_{fg} or V_t variation. From this point of view, it is possible to match an array of ISFETs by altering each device's initial V_{fg} using known FG-MOS techniques discussed in chapter 2. These basically are:

- Removing trapped charges using UV light to excite them into conduction band where they are neutralized.
- Using layout methods to minimise trapped charge variations within a die.
- Moving electrons across the insulator potential barrier using hot electron injection and/or electron tunnelling to program the floating gate voltage to a desired level.
- Using a switch to dynamically connect to the gate in order to set its voltage then disconnect it to restore its floating state.

Exploiting floating gate nature of ISFETs in CMOS, these techniques can basically be used. This is encouraged by the demonstration of hot electron injection use to alter ISFET's V_t through adding electrons to its floating gate under constant pH and

appropriate biasing conditions [5]. The opposite was demonstrated in the course of this thesis where electrons were removed from ISFET's floating gate using Fowler-Nordheim electron tunnelling.

This chapter describes one way to program a CMOS ISFET's floating gate charges in order to bring its threshold voltage to a desirable value using only circuit techniques, without post processing steps. This method can be used to match large arrays of ISFETs. It is proposed to use indirect bidirectional electron tunnelling for this purpose. Two indirect tunnelling inputs are capacitively coupled to its floating gate in such a way that one adds and the other removes electrons from the floating gate.

Section two reviews methods reported to match ISFETs. Then, section three introduces the use of electron tunnelling to alter trapped charges of an ISFET. The proposed method of matching ISFET arrays is depicted in section 4. The application of this method to match chemical switches is depicted in section 5. Simulations and experimental measurements are described and discussed in due course.

6.2 Reported ISFET matching techniques

The problem of random trapped charges in CMOS ISFETs has been known since their invention [6] [7] [2]. It is important to match threshold voltages/trans-conductances of devices in order to have comparable responses for similar chemical stimuli. Knowing the threshold voltage of an ISFET greatly simplifies the design of its circuit. Better than that is the ability to program it to the value of interest, for example similar to the intrinsic MOSFET transistor's V_t. A couple of techniques were reported by researchers.

UV light is known to excite trapped charges into conduction band. It has traditionally been used to erase non-volatile memories [8]. In [9], it was successfully used to remove

trapped charges with the aim of matching transconductance of ISFETs. Initial mismatch of an array of four ISFETs was reduced from about 1V to 10 mV after 10 hours of UV light exposure while suitably biasing the devices. This method required a post processing step with long use of external calibration sources.

Another method of addressing this problem is simply to leave trapped charges in place and look at them from a different point of view. Since an ISFET in CMOS is a floating gate device and assuming constant V_t for the intrinsic MOS transistor, then its floating gate voltage (V_{fg}) is the affected variable by these trapped charges.

FG-MOS can have a number of capacitively coupled inputs where V_{fg} is determined by their weighted sum [10]. This idea was first exploited for an ISFET by Georgiou et. al., in [11]. A second electrical input was capacitively coupled to its floating gate. It was used as a control gate to program V_t. However, the coupling capacitance of this control gate was large in order to increase its effective weight so that its input may be within rails and yet have significant effect. This was at the cost of reducing the coupling weight of the chemical signal and hence reducing that ISFET's sensitivity.

A similar idea was used in [12] and [13] to build an auto-zeroing amplifier with a feedback loop incorporating two capacitively coupled nodes to the ISFET's floating gate, namely: evaluation and sense nodes. The evaluation node was used to read and store a reference level. The sensing node was used for reading the signal change after the chemical stimuli. A comparator amplified the difference between the two levels in order to compensate for trapped charges and drift. This ingenious method is similar to correlated double sampling. It needed a large storage capacitor, an amplifier, a number of switches, and their control circuit to run the system.

In [5], hot electron injection was demonstrated to program an ISFET's threshold voltage by adding electrons to its floating gate which increased its V_t. That method cannot

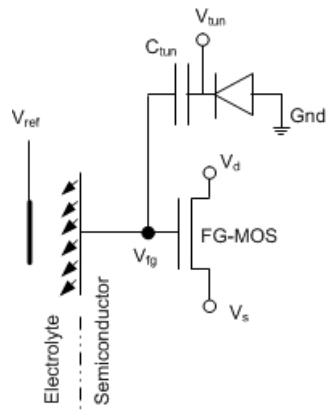

Figure 6.2: ISFET model with an added tunnelling structure.

reduce V_t by removing electrons from ISFETs' floating gates. However, in order to achieve complete controllability of V_t, it should be possible to increase and decrease it by adding or removing charges to the floating gate. With, only half of this job possible using hot electron injection, the second half is still to be done. Electron tunnelling is one solution.

6.3 Electron removal from ISFETs' floating gates using electron Tunnelling

This section describes experiments to demonstrate the use of electron tunnelling to remove electrons from the floating gate of an ISFET built in standard CMOS technology.

6.3.1 Device description

Figure 6.2 is a representation of an ISFET with an additional tunnelling structure. The P-region of the isolation diode is grounded and its N-region is connected to the tunnelling voltage source (V_{tun}), planned to be positive. It is capacitively coupled to

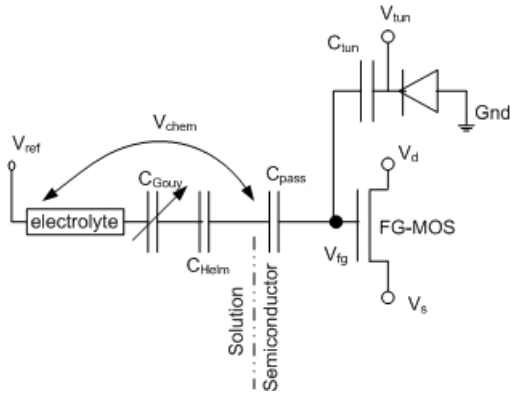

Figure 6.3: ISFET model with an added tunnelling structure.

the ISFET's floating gate by C_{tun}. C_{pass} , V_{ref}, and V_{chem} have their usual meanings.

The floating gate voltage, here, is given by:

$$V_{fg} = \frac{C_{pass}}{C_T}(V_{ref} + V_{chem}) + \frac{C_{MOS}V_{MOS}}{C_T} + \frac{C_{tun}V_{tun}}{C_T} \tag{6.1}$$

Where ($C_{MOS}V_{MOS} = V_D C_{GD} + V_S C_{GS} + V_B C_{GB}$) is the MOS contribution into V_{fg}. This equation shows the floating gate voltage as predicted by charge conservation. C_T is the total capacitance seen by the floating gate.

For programming, V_{tun} is raised to a positive tunnelling voltage as planned by respective experiment, otherwise, it is grounded. Hence, its contribution to V_{fg} is nullified during V_t measurement.

In order to measure changes in ISFETs V_t after tunnelling sessions, it was biased in weak inversion where the drain current is given by:

$$I_d = I_{d0}\frac{W}{L}e^{\frac{V_{fg}-V_t}{nU_T}} \tag{6.2}$$

yealding:

$$V_{fg} - V_t = nU_T ln\left(\frac{I_{ds}}{I_{d0}\frac{W}{L}}\right) \tag{6.3}$$

From equations 6.1, if I_d (thus $C_{MOS}V_{MOS}$), and pH (thus V_{chem}) are constants, while $V_s = 0$ V, $V_d = 0.5$ V, and $V_{tun} = 0$ V (When measuring I_d); then:

$$V_{fg} = V_{ref}\frac{C_{pass}}{C_T} + const. \approx V_{ref} + const. \quad for \;\; C_{pass} \approx C_T$$

This is valid if C_{pass} is designed much larger than all other capacitances in the model. Using this in equation 6.3 gives:

$$V_{ref} - V_t \approx const.$$

Therefore, a measured shift of V_{ref} that gives an arbitrary fixed value of I_d is equivalent to shifts in V_t. The same relation can be shown to hold in all regions of operation. Thus, shifts in V_t may be measured by finding shifts in V_{ref} that produce the same predefined I_d under constant biasing conditions. 0 The probability of electrons tunnelling through the insulating gate oxide barrier increases with the increasing electric field across it. The tunnelling current is calculated using Fowler-Nordheim model presented in equation 6.4 [14] [8]. Where, t_{ox} is the oxide thickness, E_0 is a device parameter that marks the onset of tunnelling, V_{tun} is the tunnelling voltage, and E_{ox} is the electric field across gate oxide.

$$I_{tun} = I_0 e^{\frac{E_0}{E_{ox}}} = I_0 e^{\left(\frac{t_{ox}E_0}{V_{tun}-V_{fg}}\right)} \tag{6.4}$$

Tunnelling occurs for oxide electric fields in the range of $0.75 - 1V/nm$ [15]. This is normally avoided for normal MOS operation because gates become leaky. Nominal operating voltages are chosen to leave enough margin away from this region. Higher voltages than normal CMOS operating range are required to produce fields in favour of

Table 6.1: V_{ref} for $I_d = 2\mu A$, initially and after each tunnelling experiment.

Experiment #	V_{tun}	Measured V_{ref} for $I_d = 2\mu A$	
1	initial	Vref-0	2.446
2	6.9	Vref-1	2.198
3	7.1	Vref-2	1.713
4	7.3	Vref-3	1.4075
5	7.5	Vref-4	1.233
6	7.7	Vref-5	0.911
7	7.9	Vref-6	0.489
8	8.1	Vref-7	0.34
9	8.3	Vref-8	-0.21
10	8.5	Vref-9	-1.01

tunnelling. However, as CMOS devices shrink in size, their gate oxide thickness shrinks which reduces tunnelling voltages to ranges that can be supplied by batteries for hand held devices. For example, $6 - 8V$ is enough to cause low density of electron tunnelling in the used $0.35\mu m$ process where nominal gate oxide thickness is $7.6nm$.

6.3.2 Experiments description

A p-type ISFET device was fabricated in AMS $0.35\mu m$ technology with aspect ratio of $W/L = 3\mu m/0.35\mu m$. Its gate was connected to top metal layer of area $35\mu m \times 200\mu m$. And C_{tun} area of $0.5 \times 0.35\mu m^2$. These areas show that C_{pass} is much larger than all other floating gates' coupling capacitors. The die was bonded on a PCB and the bonding wires were encapsulated by epoxy to protect them from electrolytes. It was immersed in pH 7.0 buffer solution throughout all experiments and V_{ref} was applied via $Ag/AgCl$ reference electrode. Keithley 4200S CS was used for both measurement and tunnel programming the floating gate.

For programming, while $V_d = V_s = V_{ref} = 0V$; V_{tun} was swept from 0 V to the desired level, fixed for about 80 seconds, and then swept back to 0 V. A number of tunnelling experiments were done with increasing tunnelling voltage as listed in table 6.1. V_t shift

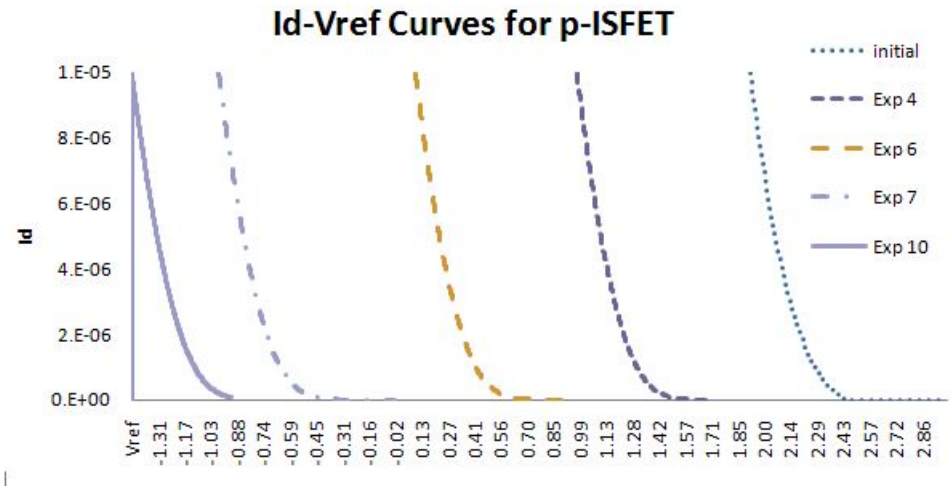

Figure 6.4: P-type ISFET's $I_d - V_{gs}$ curves after five tunnelling experiments.

after each experiment is listed in the same table.

For measurement of V_t shift, V_{ref} was swept while measuring I_d; $V_s = 0.5V$ and $V_{tun} = V_d = 0.0V$. $I_d = 2\mu A$ was chosen as the fixed I_d point. Thus, values of V_{ref} that produced this I_d value were recorded and used to indicate V_t shifts. The transistor was first measured to find the initial V_{ref_0}, that produced $I_d = 2\mu A$ before any tunnelling session. Next, the first programming phase was done with $V_{tun} = 6.9V$. Afterwards, the new V_{ref_1}, that produced the same I_d, was measured. After applying $V_{tun} = 7.1V$, V_{ref_2} was found. This procedure was repeated nine times where V_{tun} was increased in steps of 0.2 V as shown in table 6.1.

It was found that V_t shifted with each tunnelling step reflecting removal of electrons from its floating gate. A total V_t shift of -3.45 V was recorded. Figure 6.4 shows $I_d - V_{ref}$ curves for five of these experiments.

The shift here was solely due to removing electrons from the floating gate by tunnelling. Due to biasing, no hot electron injection took place. The current levels where not enough for it, μA range. Moreover, V_t shifts here were in the opposite direction of that

reported in [5], where hot electron injection was used to add electrons to the floating gate. The current levels used in [5] were three orders of magnitude larger, that is in mA range.

6.4 CMOS ISFET V_t Programming Options

In principle, all floating gate programming and matching techniques may be applicable for ISFETs. This is supported by the demonstration of hot electron injection use to program an ISFET floating gate [5]. Similarly, Fowler-Nordheim electron tunnelling was demonstrated in the last section to alter floating gate charges of an ISFET [16]. It make sense to look for methods that provide full V_t controllability.

The intention in this section is to evaluate the use of FG-MOS V_{fg} programming techniques for ISFETs use. The aim is to choose a method to program floating gate charges in order to match an array of ISFETs that satisfies the following criteria:

- Uses the minimum substrate area. Thus, it can be used for large arrays with small pixel sizes without being the size limiting factor.
- Can be used in digital circuits in order to use the same method with the chemical switches presented in chapter 4.
- Does not require large C_{pass} as chemical areas may shrink in size to increase the number of sensing elements.
- Low power, does not need the flow of large currents. This keeps large arrays low power.
- Fast, can match a large array within minutes. Therefore, does not put a constraint on measurement operations.

- Uses standard CMOS process without post processing steps. So, cost is kept low.
- V_{fg} may not be subjected to large potential variations which may appear across C_{pass}. This aims to avoid possible adverse effects on passivation's mobile ionic charges, which may cause unpredictable drift effects.
- Needs minimum control circuitry.
- It is a plus if the method is indirect, as this will allow its use with diverse circuits, like inverters, without much altering their properties.

In the following, known FG-MOS techniques for floating gate programming are evaluated for ISFET use according to the above criteria.

UV light

Milgrew used this method in [17] and used it to build a proton arrays for different applications in [6], [9] and [18]. The quantum mechanical interaction between light and matter is used to excite trapped electrons into conduction band where they are drained away. However, this process is slow and not efficient. Long exposure hours and strong light sources are needed. Moreover, it needs post processing steps. Thus, this method is not suitable here.

Layout techniques

The layout technique described in chapter 2 relies on extending the floating gate of FG-MOS devices to the topmost metal layer [1]. But, this is not useful for ISFETs. Simply because their floating gates are already extended to the topmost metal layer and the mismatch still exists. It is understood that if the area in the topmost metal is

minimal, as is the case with reported FG-MOS in that paper, this method works because of negligible passivation capacitance. However, that is not the case for ISFETS.

Using a switch

The use of a switch to set floating gate voltage of FG-MOS devices was illustrated in [19]. However, large capacitors and dynamic refreshing is needed. This method might be applicable to monitor very fast chemical reactions. However, for reactions that need more than few Milli seconds, switch leakage current will inhibit any useful chemical signal sensing. Reactions of interest here, may need even longer time [20]. This method is not suitable.

Hot electron injection and electron tunnelling

This technique was elegantly used for a number FG-MOS applications and circuits [21]. Basically, a pMOS transistor is biased in such away that hot electron injection adds electrons to its floating gate while Fowler-Nordhiem electron tunnelling removes them [15] [22]. At the desired point of operation, both currents are equal. It is a delicate balance, if V_{fg} deviates from this equilibrium point, currents will change in order to restore balance. This transistor may be part of the circuit [23] or auxiliary to it [24]. In this case large currents that trigger hot electron injection are needed. This consumes appreciable power especially for large arrays. Moreover, applied tunnelling voltage may induce charge redistribution in the floating gate which results in large electrical fields in the passivation layer for small C_{pass}. This is undesirable as it may cause adverse effects on mobile ionic charges that are understood to cause drift [3]. This method needs special biasing, that may need special design procedures [25].

Bidirectional electron tunnelling

This technique was used to build precise floating gate voltage reference [26]. Basically, a tunnelling diode was used in a differential dual floating gate arrangement. It had an oxide thickness of $400A^{\circ}$ indicating the use of an EPROM manufacturing process. That device was factory programmed using a special circuit. It used a special protocol where each programming voltage was separately applied via poly-2 while the floating gate is in poly-1 layer[27]. This method as used in this example is not of much interest for ISFETs. Because, programming was done only once in the factory and large electrical fields result on the floating gate because strong tunnelling voltages were applied in turns.

Evaluating the above techniques, the first three methods are doomed not suitable and are out of question. Last two may be possible. The use of hot electron injection requires higher currents and voltages similar to those needed for tunnelling [5]. This facilitates the use of a combination of these two techniques. It has the advantage of using only positive voltages. However, this method dictates the use of special biasing that allows for simultaneous hot electron injection and tunnelling. The penalty here is the possibility of inducing large electrical fields across the passivation capacitance, which may cause drift problems. Moreover its special biasing requirements deem it incompatible with digital circuits except if it was done in an indirect way. Another point to consider is the power requirement of applying high voltages suitable for tunnelling that, at the same time, produce high drain currents suitable for hot electron injection. Therefore, this method may not be the first choice, though it is promising.

A method is sought where small, transistor sizes could be used in matching that depends only on applied voltages and can be done in a short time without affecting the circuit mechanism of a simple inverter. Moreover, strong electrical fields across C_{pass} are avoided during V_{fg} programming. The bidirectional tunnelling method presented above

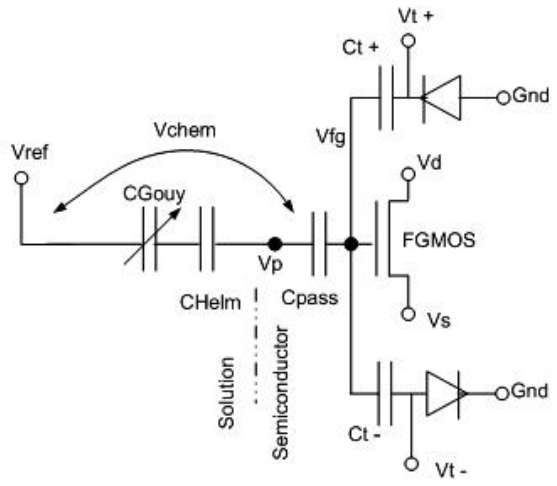

Figure 6.5: Model of ISFET in CMOS with indirect electron tunnelling structures

is preferred. However, it is not suitable as presented in [26]. It has to be modified in order to be fully CMOS compatible and replace factory programming by field matching that can be repeated. Its drawback is the need for both positive and negative tunnelling voltages. These can be externally supplied for experimental purposes. Once, their use and protocol are fully stable and understood, they may be internally generated using charge pumps.

6.5 CMOS ISFET V_t Programming Using Indirect Bidirectional Electron Tunnelling

It was decided, in this work, to use only electron tunnelling to program V_{fg} of ISFETs by adding and removing electrons from it. Two inputs are capacitively coupled to the ISFET's floating gate via matched capacitors. They are used to indirectly tunnel electrons across their oxide isolation to/from the floating gate in a controlled way. The floating gate charges will be programmed in such a way to result in a desirable V_t using

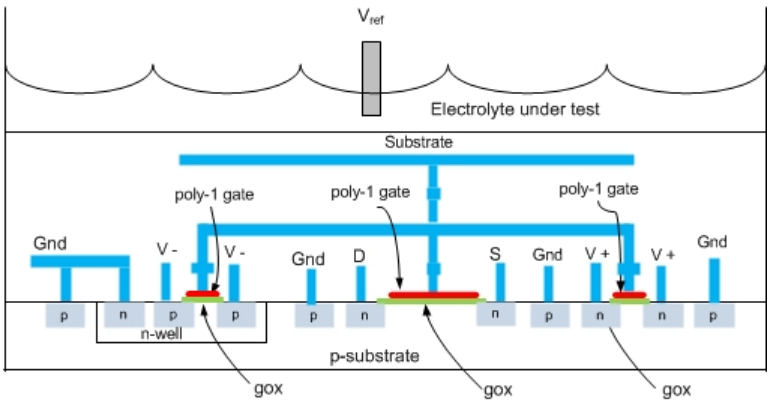

Figure 6.6: Cross section of n-ISFET with the indirect tunnelling structures featuring V_{t+} and V_{t-}

a balanced combination of these two tunnelling voltages.

By the same method, floating gate charges can be programmed to be different from zero. It is experimentally shown here, that using tunnelling voltages with appropriate magnitude combinations, V_t of ISFET's can be made comparable to that of similar MOS devices within few minutes. This method can be used to match arrays of ISFETs with a common reference to a desired V_t in a short time using only circuit techniques.

Figure 6.5 shows an ISFET model in CMOS with two inputs coupled to its floating gate: a positive tunnelling voltage (V_{t+}), coupled via C_{t+}; and a negative tunnelling voltage (V_{t-}), coupled through C_{t-}. They are used for the bidirectional indirect tunnelling.

Because, tunnelling is carried out between a poly-1 gate, that is part of the ISFET's floating gate, and a substrate diffusion area, current must be prevented from flowing to other substrate areas. Diode isolation is used to make sure this diffusion area always has a reverse biased junction with the surroundings. Therefore, the two tunnelling voltages are applied via the substrate in such a way to prevent these junctions from being forward biased at all times. Figure 6.5 shows a model of this arrangement while figure 6.6 is the nMOS cross section representation, not to scale. And figure figure 6.7 shows the pMOS

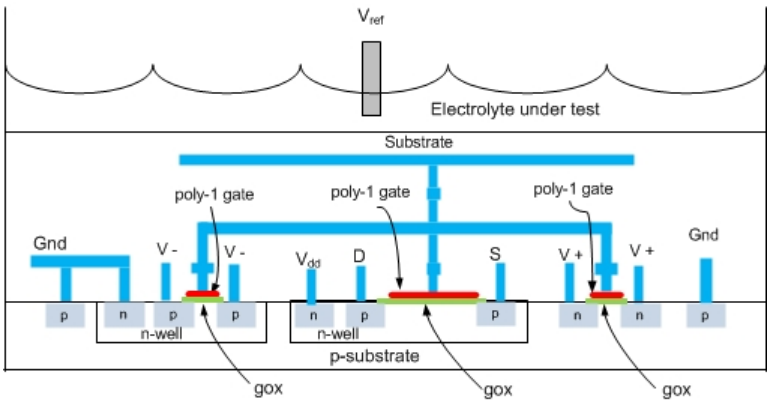

Figure 6.7: Cross section of p-ISFET: with the indirect tunnelling structures featuring V_{t+} and V_{t-}

case for the AMS single well process.

By charge conservation, V_{fg} is given by:

$$V_{fg} = \frac{C_{pass}}{C_T}(V_{chem} + V_{ref}) + \frac{C_{t+}}{C_T}V_{t+} + \frac{C_{t-}}{C_T}V_{t-} + \frac{V_{MOS}C_{MOS}}{C_T} + \frac{Q_{TC}}{C_T} \tag{6.5}$$

Here, C_T is the total capacitance seen by the floating gate and ($V_{MOS}C_{MOS} = V_dC_{gd} + V_sC_{gs} + V_bC_{gb}$) is the MOS transistor contribution to V_{fg}. V_{TC} represents trapped charges.

For normal ISFET sensing operation, all voltages are used in their usual sense, which means V_{t+} and V_{t-} are grounded. Therefore, equation 6.5 reduces to:

$$V_{fg_{sense}} = \frac{C_{pass}}{C_T}(V_{ref} + V_{chem}) + \frac{V_{MOS}C_{MOS}}{C_T} + \frac{Q_{TC}}{C_T} \tag{6.6}$$

This is exactly the case for a single ISFET without tunnelling structures, apart from slightly larger C_T here. During floating gate tunnel programming, only V_{t+} and V_{t-} are non-zero while all other voltages are set to ground, including V_{dd} and V_{ref}. Thus,

equation 6.5 becomes:

$$V_{fg_{tun}} = \frac{C_{pass}}{C_T} V_{chem} + \frac{Q_{TC}}{C_T} + \frac{C_{t+}}{C_T} V_{t+} + \frac{C_{t-}}{C_T} V_{t-} \tag{6.7}$$

Therefore, during tunnelling, V_{fg} is dictated by the tunnelling inputs, the constant V_{chem}, and floating gate trapped charges, which is to change. From equation 6.4, after the onset of tunnelling, J_{tun} depends only on E_{ox} which, in turn, is a function of the voltage difference between V_{fg} and V_{t+} or V_{t-}. Their coupling weight depends on their coupling capacitances. Tunnelling current depends on actual area exhibiting tunnelling, assumed to be full capacitor area, and current densities, magnitudes given by:

$$J_{tun+} = A_0 E_{ox+}^2 e^{\left(\frac{E_0}{E_{ox+}}\right)}, where\ E_{ox+} = \frac{V_{t+} - V_{fg}}{t_{ox}} \tag{6.8}$$

$$J_{tun-} = A_0 E_{ox-}^2 e^{\left(\frac{E_0}{E_{ox-}}\right)}, where\ E_{ox-} = \frac{V_{fg} - V_{t-}}{t_{ox}} \tag{6.9}$$

The positive tunnelling voltage V_{t+} is used to remove electrons form the floating gate, whereas, the negative voltage V_{t-} is used to counteract it.

V_{t+} and V_{t-} are chosen in such a way to result in the flow of tiny and opposite currents from/to the ISFET's floating gate. These currents will be constant and equal at the desired point of operation, midway between them. Any deviation from it, causes imbalance that will bring V_{fg} back to its equilibrium operating point within a limited time frame. Thus, one way to bring V_{fg} to zero regardless of its initial charge is by choosing $V_{t+} = -V_{t-}$. Though this combination is advantages , different magnitudes may have other advantages. For example, according to equations 6.7, it is possible to use them in order to choose an appropriate equilibrium value of V_{fg} that is different from zero [27].

The time needed to match an ISFET array is collectively determined by the amount of trapped charges; the magnitudes of tunnelling currents, each floating node total

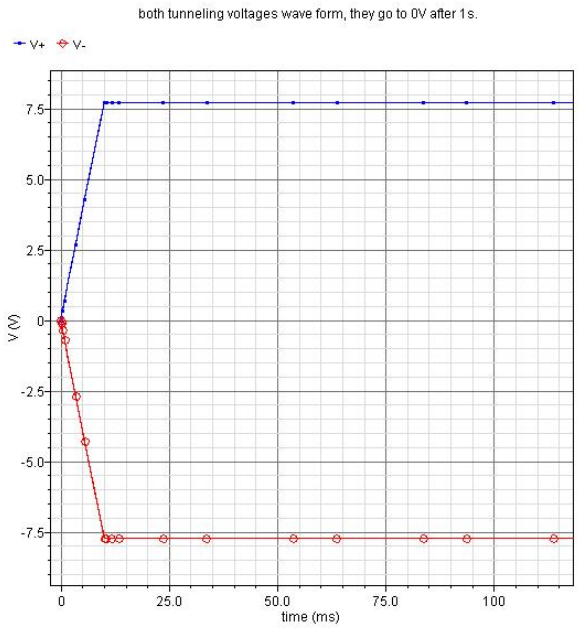

Figure 6.8: Wave-form of ±7.6 V tunnelling voltages.

capacitance (C_T). Higher tunnelling currents provide faster matching but need higher voltages.

Finally, because the initial V_{fg} of each ISFET in an array is not known, V_{t+} and V_{t-} are swept from 0.0 V to their respective tunnelling values with equal but opposite slopes. Then, they are kept steady for long enough time to match all devices in the array, figure 6.8. Afterwards, they are brought down to zero in a similar way. This insures that E_{ox} does not reach undesirable values that can cause oxide breakdown. Moreover, this results in nearly zero net coupling weight on V_{fg} through out the matching process. This insures minimum field across C_{pass}. Thus, reduced effect on mobile ionic charges that are postulated to cause drift [28] [2] [3].

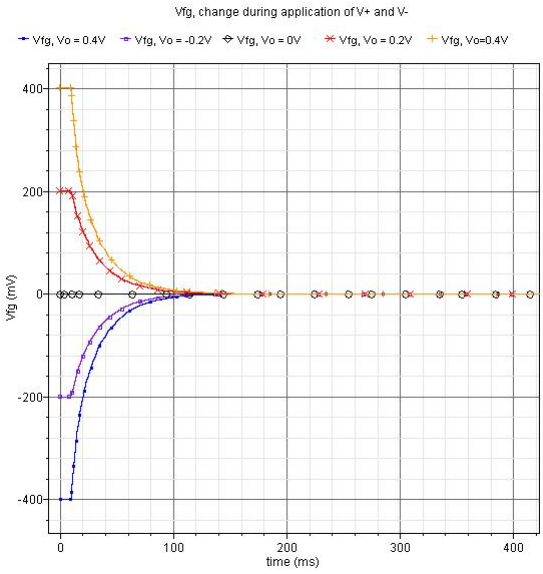

Figure 6.9: V_{fg} change starting from different initial values

6.5.1 Simulation results

The proposed circuit was designed in an AMS 0.35μm commercially available CMOS process. The nISFET had a width of $3\mu m$ and length of $0.35\mu m$. The passivation capacitance was assumed $C_{pass} = 45fF$. Both tunnelling coupling capacitors were designed with poly1 - diffusion capacitance $C_{t+} = C_{t-} = 1fF$. For minimum size, this was realised by transistors where drain and source are shorted and act as the tunnelling input. The circuit of figure 6.5 was simulated in Cadence using BSIM3V3.2 MOS model and a verilog-A ISFET model based on V_{chem} and a verilog-A tunnelling models according to equations 6.8 and 6.9.

The nominal gate oxide thickness in this process is 7.6 nm and the minimum diode break down voltage is 9.0 V [29]. Therefore, there is a small range where electron tunnelling can take place before the reverse biased isolation diodes break down, that is in the range 6.0V - 9.0V. Interestingly, this can be handled using high voltage modules of the same process [29]. Moreover, it is within the supply range of batteries for hand held devices.

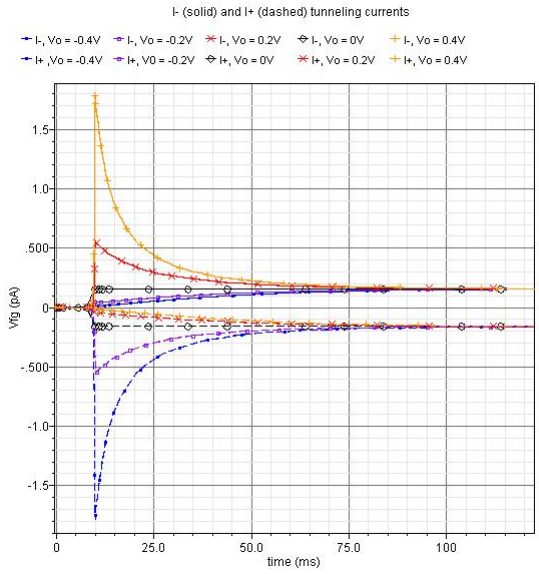

Figure 6.10: Tunnelling current change starting from different initial V_{fg}

It was chosen to apply $V_{t+} = -V_{t-} = 7.6V$ according to the wave form of figure 6.8. They were first swept from 0 V to ±7.6V in 10 ms in order to avoid breaking down the gate oxide since initial V_{fg} is not known. Then, they were kept their for a time that is more than enough to bring V_{fg} to zero. Finally, they were swept back to 0.0 V. This part is not shown in figure 6.8.

Figure 6.9 shows the change of V_{fg} in response to these applied tunnelling voltages. A number of parametric sweeps were done where initial V_{fg} was used as a parameter with values (-0.4, -0.2, 0.0, 0.2, and 0.4)V. Each time, V_{fg} was brought to its steady state value of 0 V within about two minutes. Figure 6.10 depicts both tunnelling currents during this process. They drop very fast with the change of V_{fg} and reach a steady state value of about $\pm 0.1pA$.

Table 6.2: Simulated V_{ref} for $I_d = 2\mu A$, for the circuit of figure 6.5 for both ISFETs, different initial V_{fg} (V_{fg0}) voltages are assumed. All values are in Volts

V_{fg0}	-1.0	-0.5	0.0	0.5	1.0
n-ISFET	1.954	1.398	0.86	0.323	-0.241
p-ISFET	1.023	0.460	-0.085	-0.623	-1.173

Table 6.3: Measured V_{ref} for $I_d = 2\mu A$, initially and after two tunnelling sessions with tunnelling voltages (V_{t+}, V_{t-})

	Measured V_{ref} for $I_d = 2\mu A$		
	Initial	After (+7.6,-7.6)V	After (+8.7,-6.5)V
nMOS ISFET	-1.62 V	1.894 V	0.603 V
pMOS ISFET	2.238 V	1.45 V	-0.362 V

6.5.2 Measurements

The standard $0.35\mu m$ CMOS process, that was used in simulations, was used to fabricate two ISFFETs in the same die, an nMOS and a pMOS. Both had an aspect ratio (W/L) of $3.0\mu m/0.35\mu m$. All tunnelling capacitors were matched to about $0.98fF$. Both had equal chemical sensitive areas of $2000\mu m^2$ corresponding to about $45\pm6fF$ [29]. The die was bonded and water tight encapsulated. The devices were tested and V_t programmed using Keithely 4200-SCS semiconductor characterization system. The reference voltage was applied via a standard Ag/AgCl reference electrode that was immersed in pH 7 buffer solution from Hanna chemicals.

For ISFETs' characterization, a similar protocol as the last section was used. $I_{ds} - V_{ref}$ curves of the two ISFETs were measured by sweeping V_{ref} in pH 7 while grounding the tunnelling nodes, to nullify their contribution. Both devices were biased with $V_{dsn} = V_{sdp} = 0.5V$, where the suffix "n" stands for the nISFET and "p" for p type device. V_{ref} that resulted in $2\mu A$ drain current were reported for each case, table 6.3.

During the use of V_{t+} and V_{t-} in tunnelling sessions, all other nodes (V_d, V_s, V_{dd}, and substrate) were grounded. The n-Well, that housed the p-diffusion used for V_{t-}, was

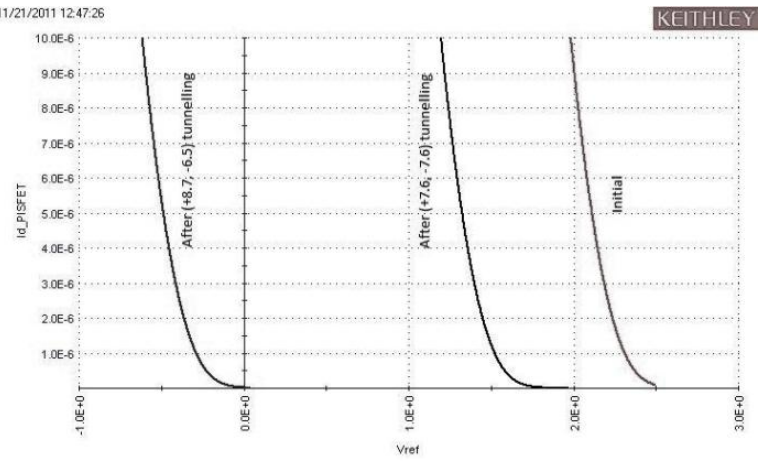

Figure 6.11: $I_{ds} - V_{gs}$ curves of the pMOS ISFET: initially, after tunnelling session with (+7.6,-7.6)V, and then (+8.7, -6.5)V

also grounded. This prevents it from biasing the lateral pnp BJT where it plays the base role, figure 6.7. The used process is single well. Thus, the n-diffusion that was used for V_{t+} was surrounded by ground in the p-type substrate. The wells were seperated in this layout only for experimental purposes. For this protocol,V_{t-} can share the same n-well as the pISFET, which greatly reduces silicon area.

Table 6.2 lists the simulated V_{ref} for drain currents of $2\mu A$ for both devices under different initial floating gate charges. It is used as a reference to indicate the polarity of floating gate charges that resulted from tunnelling experiments. It, also, gives an idea of how close the charges are from the targeted results.

The curves labelled "initial" in figures 6.11 and 6.12 show the initial $I_d - V_{ref}$ traces measured for both ISFETs before starting tunnelling experiments. For the nISFET, $I_{dn} = 2\mu A$ resulted for $V_{ref} = -1.62V$. Comparing this with table 6.2, a positive initial floating gate charge is indicated. For the pISFET, $I_{dp} = 2\mu A$ resulted when $V_{ref} = 2.38V$, which indicate negative initial floating gate charge; as table 6.2 reveals. This shows how much variation trapped charges may cause, though both devices were in the same die.

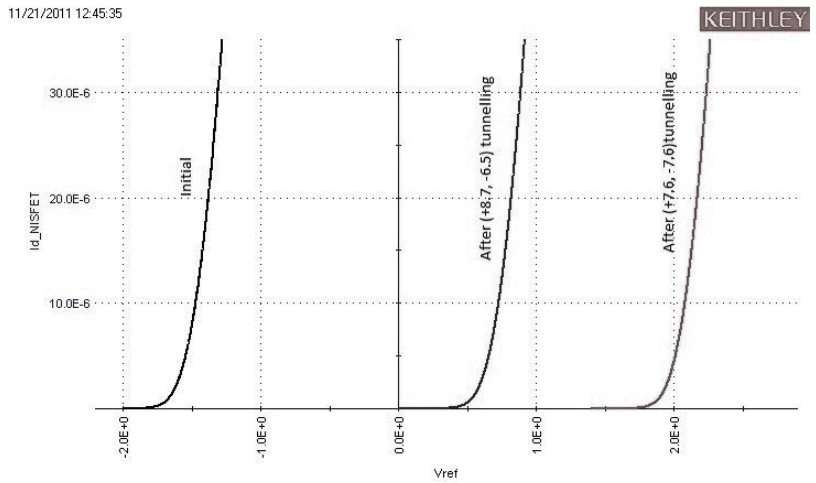

Figure 6.12: $I_{ds} - V_{gs}$ curves of the nMOS ISFET: initially, after tunnelling session with (+7.6,-7.6)V, and then (+8.7, -6.5)V

Afterwards, both ISFETs were subjected to a tunnelling session where V_{t+} and V_{t-} were swept from $0V$ to $\pm 7.6V$, stayed constant for about five minutes then swept back to zero volts. The results were the curves labelled accordingly. Here, for $I_d = 2\mu A$ V_{ref} was 1.894 V for the nISFET and 1.45 V for the pISFET. However, comparing these values with table 6.2, it is evident that the ISFETs floating gates are negatively charged while zero charge is expected.

It would be desirable to bring the ISFETs' V_t closer to the intrinsic devices' threshold voltage. This way V_{ref} values higher than rails, as reported in [17] [30], will no longer be needed. This will, also, make it easier to use V_{ref} in feedback loops, just the same way V_g of a normal MOS device is used. In order to accomplish this, the devices were subjected to a number of tunnelling experiments with different V_{t+} and $V_{t}-$ combinations. The combination $V_{t+} = +8.7V$ and $V_{t-} = -6.5V$ resulted in the curves labelled accordingly. V_{ref} that produced $I_d = 2\mu A$ for the n-ISFET and p-ISFET were $0.603V$ and $-0.362V$ respectively. These are close the intrinsic MOS V_t and their difference is 0.965 V which is nearly equal to the intrinsic devices threshold voltages difference.

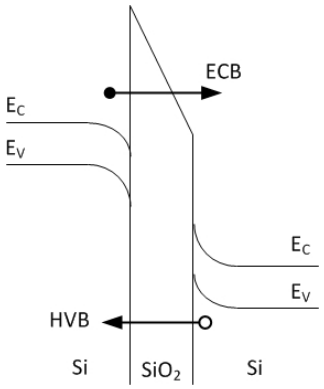

Figure 6.13: Band diagram of two tunnelling current components in a $Si - SiO_2 - Si$ structure [31].

The above measurements for both ISFETs are listed in table 6.3. Comparing both tables, it is clear that for this combination, the floating gates of both ISFETs are slightly negatively charged.

6.5.3 An observation related to V_{t+} and V_{t-}

Above experimental results show that applying equal magnitudes but opposite polarities to V_{t+} and V_{t-} do not result in zero trapped charges in ISFETs' floating gates. V_{t+} needs to be higher than V_{t-} in order to reach this point. This is clear from tables 6.1 and 6.3. Fowler-Nordheim tunnelling, used for simulations, does not fully explain this observation. Assumptions made for its modelling, like metal gate and ignoring carrier availability, may explain this observation [31].

One may think of different possible reasons for this difference. For example, it may be explained by different tunnelling mechanisms between the two structures. For the n-diffusion case tunnelling may be dominated by electrons from the conduction band (ECB) while hole tunnelling from the valence band (HVB) dominates the current mechanism for the p-diffusion case [31]. This may explain higher tunnelling current for V_{t-}

than that of V_{t+} [32].

Another, more likely, possibility to explain this is poly-silicon gate depletion. As the tunnelling voltage is supplied via the substrate, it may play a role here [33] [34]. For equal magnitudes of tunnelling voltages, poly-1 gate depletion may explain the resulted negative floating gate charge [32] [35]. For n-doped poly-1 gate, V_{t-} will attract holes and repel electrons. This results in a depletion capacitance in series with C_{t-}. The result is reduced net coupling capacitance for V_{t-}. This is not the case with C_{t+} as V_{t+} attracts electrons in the highly n-doped poly-silicon. Equation 6.7 helps understand the excess negative charge bound to C_{t+} compared to the positive charges bound to C_{t-} during tunnelling due to their different capacitances. These charges are freed when the tunnelling voltages are removed and a net negatively charged floating gate results. In order to compensate for this, the floating gate should be deliberately positively charged during the tunnelling session by applying higher V_{t+}. This should be done in such away to result in the desired V_{TC} when the tunnelling voltages are removed and the bound charges in C_{t+} and C_{t-} are freed. Similar observation was reported without explanation in [26], though a different structure was used. Though, diffusion profiles of the process are not disclosed, the authors could have estimated them using available information; such as device models, sheet resistances, and junction capacitances. However, this is beyond the scope of this thesis, though it deserves investigation in future work.

6.6 Matching Arrays of ISFET Based Chemical Inverters Using Indirect Bidirectional Electron Tunnelling

The above method was extended to an ISFET based chemical switch giving the circuit of figure 6.14. It works the same way as the single ISFET case detailed above. It is

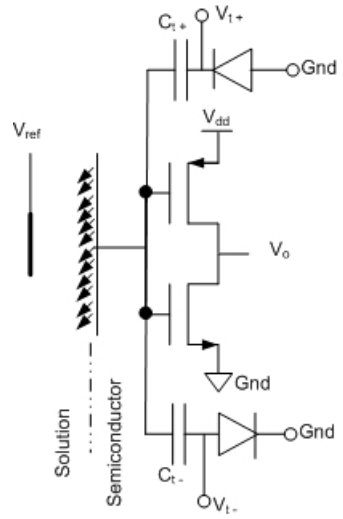

Figure 6.14: Schematic of ISFET based chemical switch with indirect bidirectional tunnelling structures.

modelled as in figure 6.15. The floating gate voltage is given by:

$$V_{fg} = \frac{C_{pass}}{C_T}(V_{ref}+V_{chem})+\frac{C_{nMOS}}{C_T}V_{nMOS}+\frac{C_{pMOS}}{C_T}V_{pMOS}+\frac{C_{t+}}{C_T}V_{t+}+\frac{C_{t-}}{C_T}V_{t-}+\frac{Q_{TC}}{C_T} \quad (6.10)$$

For normal operation when the tunnelling voltages are zero, this reduces to the normal inverter case, apart from larger C_T:

$$V_{fg} = \frac{C_{pass}}{C_T}(V_{ref} + V_{chem}) + \frac{C_{nMOS}}{C_T}V_{nMOS} + \frac{C_{pMOS}}{C_T}V_{pMOS} + \frac{Q_{TC}}{C_T} \quad (6.11)$$

However, during tunnel programming, when all terminal voltages are set to zero apart from tunnelling nodes, it becomes similar to the single transistor case:

$$V_{fg} = \frac{C_{pass}}{C_T}V_{chem} + \frac{C_{t+}}{C_T}V_{t+} + \frac{C_{t-}}{C_T}V_{t-} + \frac{Q_{TC}}{C_T} \quad (6.12)$$

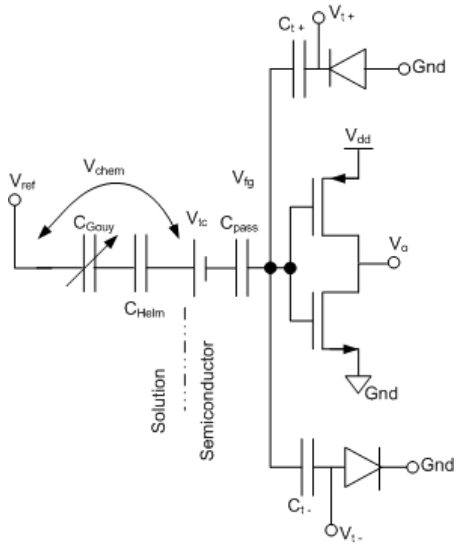

Figure 6.15: Modle of the ISFET based chemical switch with indirect bidirectional tunnelling structures.

6.6.1 Experimental measurements

The circuit of figure 6.14 was built using a commercial AMS $0.35\mu m$ technology. An array of four inverters in the same die were subjected to the same indirect bidirectional tunnel programming sessions. They were tested in pH 7 buffer solution. Keithely 4200-SCS semiconductor characterization system was used to measure their switching points and to tunnel program them.

The tunnelling voltages V_{t+} and V_{t-} were supplied via two source measurement units of the Keithley 4200 system. Figure 6.16 shows an example of tunnelling voltage sweeps along with their currents. The voltages start from a low level, that may not cause tunnelling, and increase with equal but opposite slopes to the desired level. They stay high for about 4 - 5 minutes and then are brought down with equal slopes to the low level.

It may be noted that I_{t+} is generally higher than I_{t-}. Well, both are a measurement

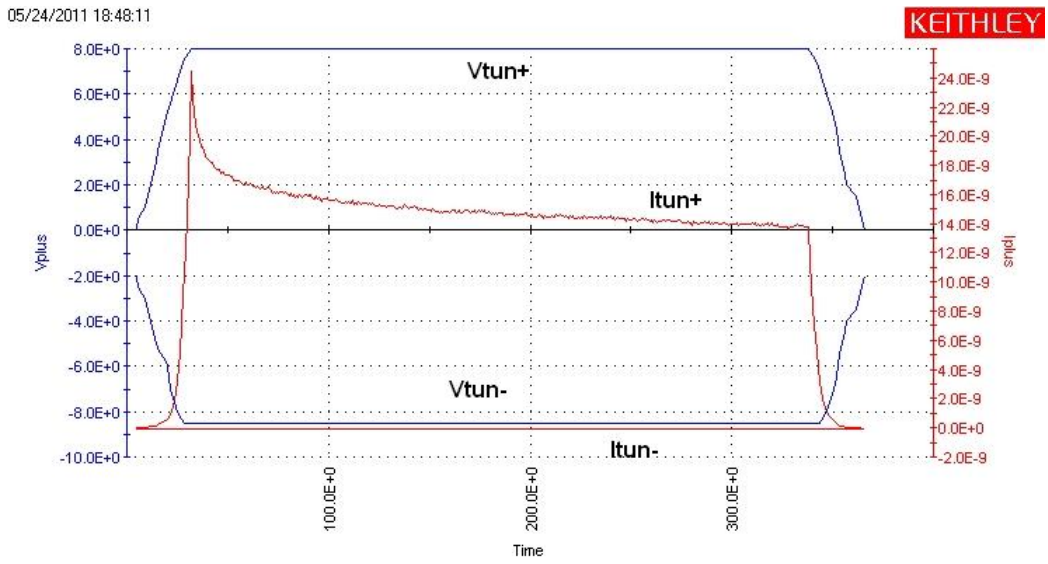

Figure 6.16: An example of applied tunnelling voltages and resulting currents.

of the supplied current by the voltage sources of V_{t+} and V_{t-} respectively. This current includes isolation diodes' leakage currents. For the V_{t+} case, this is a single diode with a large area that happens to draw more leakage current, in the range of few nano amperes. While two diodes in a row with much smaller area are formed for the V_{t-}, this draws much less current, in the range of few pico amperes. Nearly no current is drained by the lateral BJT transistors formed between the tunnelling regions, ground, and V_{dd} because V_{dd} is grounded at this time. Tunnelling current in this example can be seen around the 40th second of figure 6.16. It increases exponentially and then drops very quickly due to the change of V_{fg}.

Figure 6.17 and table 6.4 show the measured switching points of the array after each programming cycle. The x-axis is the tunnelling voltage combinations after which V_{ref} sweeps were done. V_{dd} was $1.8V$. A fifth identical ISFET based chemical switch was in the same die but not subjected to tunnel programming. It is used as a reference to demonstrate that floating gate charges were changed solely due to programming. The figure demonstrates that it is possible to use different tunnelling voltage combinations

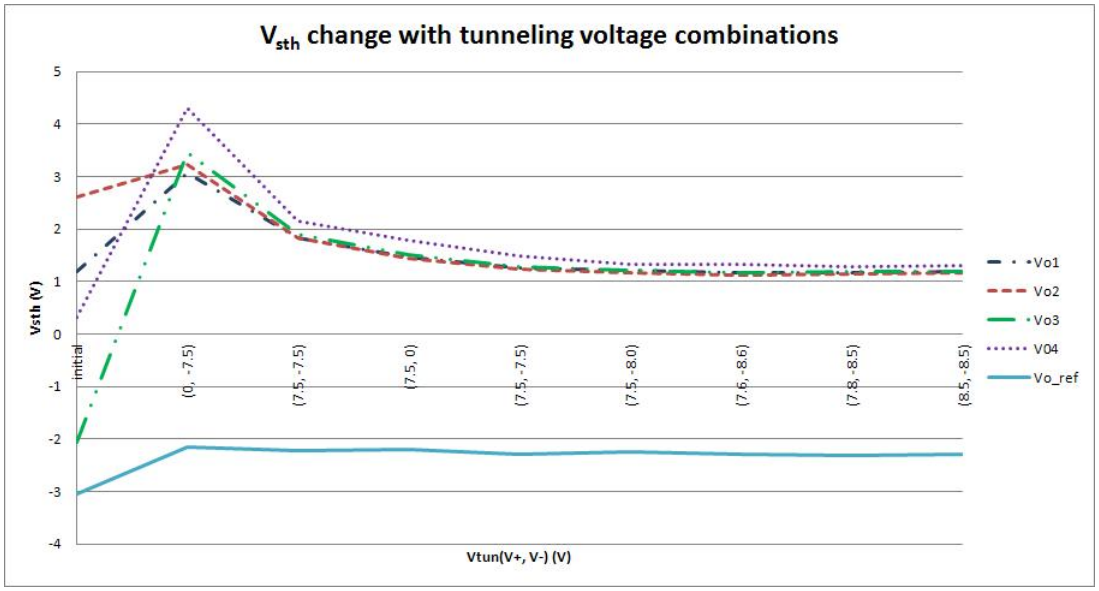

Figure 6.17: Output of an array of four chemical switches after a number of bidirectional indirect tunnelling experiments with different combinations.

in order to choose the switching point region of interest. The tunnelling sessions were short and use only small current magnitudes. The switches were matched to within $\pm 70mV$, table 6.4.

For verification and comparison purposes, an identical floating gate inverter was fabricated in the same die. It was subjected to a number of tunnelling experiments. The same was repeated for similar devices in a total of five dies. Figure 6.18 shows the switching point change of this FG-MOS inverters.

6.7 Discussion

Because of high V_{t+} and negative V_{t-}, their bond pads can not use standard static discharge protection. However, a suitably modified version can be designed for them. Alternatively, these voltages may be generated internally using appropriate circuits.

Table 6.4: Measured switching points for an array of four chemical witches after a series of tunnelling sessions with different combinations of tunnelling voltages, and one identical switch that was used as a reference not subjected to tunnelling.

V_{t+}	V_{t-}	inv-1	inv-2	inv-3	inv-4	mean	STD	range	Tol.	ref-inv
Initial	initial	1.19	2.62	-2.065	0.315	0.515	1.96	4.69	2.34	-3.04
0	-7.5	3.075	3.22	3.45	4.295	3.51	0.546	1.22	0.61	-2.16
7.5	-7.5	1.825	1.83	1.89	2.15	1.92	0.151	0.32	0.16	-2.23
7.5	0.0	1.46	1.445	1.5	1.795	1.55	0.165	0.35	0.175	-2.195
7.5	-7.5	1.265	1.245	1.29	1.485	1.32	0.111	0.24	0.12	-2.285
7.5	-8.0	1.205	1.175	1.205	1.33	1.23	0.069	0.155	0.078	-2.245
7.6	-8.5	1.155	1.13	1.165	1.315	1.19	0.084	0.185	0.093	-2.295
7.8	-8.5	1.17	1.15	1.18	1.29	1.198	0.0629	0.14	0.07	-2.31
8.5	-8.5	1.185	1.165	1.2	1.305	1.21	0.0625	0.14	0.07	-2.3

This method is fast compared to UV light, few minutes compared to 10 hours [17]. It can be used in standard CMOS without post processing steps. Moreover, it can be applied without feedback as it relies on homing V_{fg} to a value dictated by both V_{t+} and V_{t-}. Though a grounded electrolyte provides a reference level, dry ISFETs may be used as these trapped charges are inherent in the devices before they come into contact with an electrolyte. However, this needs to be experimentally tested. Finally, this method can be adapted to existing ISFET circuits because the tunnelling structures are external to the circuit and play no role in it.

The passivation layer is a protection layer in CMOS. Its thickness or properties are not of high importance. However, it is the sensing membrane for an ISFET in standard CMOS. Its properties and thickness are of vital importance. It is the main source of uncertainty in this work, for example, its thickness range results in about 13.6% tolerance in C_{pass}.

Clearly, this matching method is highly sensitive to processing and its variations. Even though, gate oxide is the best oxide quality in CMOS process, it may undergo slight thickness variation which may greatly affect tunnelling. Moreover, its surface may not be smooth enough, resulting in most of the tunnelling current going through roughness

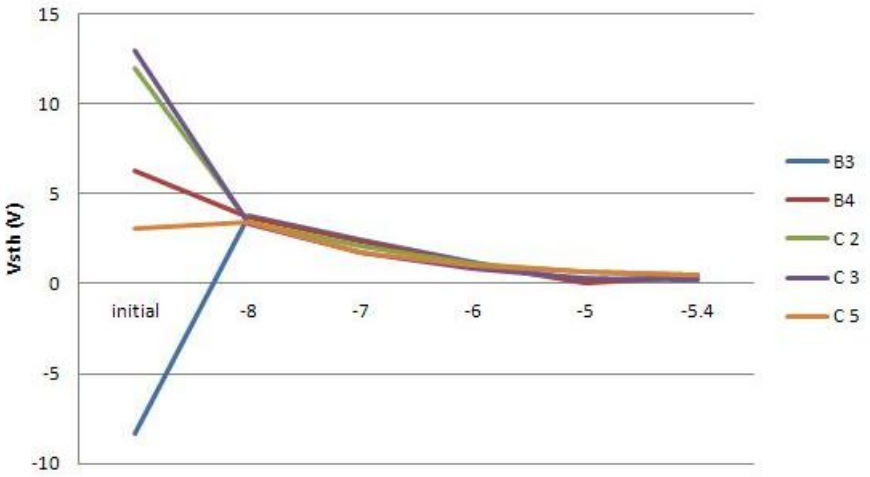

Figure 6.18: V_{sth} change of five FG-inverters in different dies after a number of bidirectional indirect tunnelling experiments with different tunnelling voltage combinations, constant $V_+ = 8V$ and V_- is the x-axis.

points if they exist [25]. However, it remains the best candidate for this operation because it is the best available in terms of thickness variations and quality. Its reduced trap cites reduce post stress charge leakage [36]. Due to its excellent thickness control, its thickness variations within a die is very small and affects both C_{t+} and C_{t-} in the same way. This reduces its effect.

The results show that an array of ISFET based chemical switches may be matched using this method. Some switching threshold variations may still exist. According to table 6.4, this was within $\mp 70mV$. A similar value was reported in [27] to be caused by a number of factors. That includes non linear capacitance changes and de-trapping of tunnel devices under dielectric relaxation [31]. The former being the release of charges trapped in oxide isolation after removal of tunnelling voltages [37]. As a safe value that is larger than reported values and larger than measured tolerances, $\mp 100mV$ may be chosen. Well, this is not good enough especially if compared with $200\mu V$ reported in [26]. The difference is that, in that paper a special EEPROM CMOS technology was used with special factory programming mechanism. It uses one tunnelling voltage at a

time. It uses an external high voltage circuit in a feedback loop that stops programming when the floating gate reaches its desired level.

It is possible to use a similar idea here by incorporating high voltage circuits and/or special EEPROM structures, especially as they are supported in some CMOS commercial processes. Thus may be applied in the field which is very important. However, the proposed mechanism is much simpler and faster. Plus, the purpose here is to prove the concept. Moreover, an evaluation of needed accuracy is needed in view of drift and total noise, which is beyond the scope this thesis.

This method is good enough to be used in conjunction with the pulse width modulation method depicted in [38] and [3]. In that circuit, a triangular control signal is coupled to the floating gate, of the ISFET based chemical inverter, via a control input . The output is pulse width modulated by the pH of the chemical under test. It can easily be converted to a digital form. That is an excellent circuit that operates under constant V_{ref}, and works even under some trapped charges mismatch. The coupling capacitance values along with control signal amplitude, frequency, and the circuit biasing are chosen to trade-off pH range and sensitivity with trapped charges cancellation capability. The circuit reported in [38] can cancel the effect of trapped charges within $2V$. But, mismatch due to trapped charges in ISFET arrays may be much more than that. An example is presented in table 6.4 where in an array of four devices the range of mismatch was more than $4.5V$. The method presented here, will reduce such mismatch to within $\pm 0.1V$, table 6.4. This enables the use of the pulse width technique with arrays of sensor pixels with relaxed trapped charges cancellation requirements. It leaves more room for pH sensitivity and range. An added advantage is programming trapped charges in ISFET's floating gates, which relaxes the choice of V_{ref} and DC bias of the control signal.

6.8 Conclusion

Exploiting the floating gate nature of ISFETs in CMOS, it is possible to use indirect bidirectional electron tunnelling to control its V_t. The same method can match an array of ISFETs. Basically, two tunnelling inputs are coupled through matched poly1 - diffusion capacitors to the floating gate. Applying high enough tunnelling voltages V_{t+} and V_{t-}, tunnelling takes place in two opposite directions across the high quality gate oxide. V_{fg} reaches steady state when both tunnelling currents are equal and in opposite directions. It was demonstrated by simulation that this technique brings V_{fg} to 0 V from initial values between -0.4V to +0.4 V within 2 minutes. Measured results showed that V_t of an n-ISFET and a p-ISFET can be controlled using appropriate combination of tunnelling voltages V_{t+} and V_{t-}. They can be brought close the intrinsic MOS threshold voltages.

This method provides for V_t programming of ISFETs in standard CMOS without additional processing steps. It can be used for fast matching of ISFET arrays. This method is particularly useful for disposable lab on chip applications where devices are used only once.

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Chapter 7

Conclusion

7.1 Contribution

This thesis focused on novel floating gate ISFET chemical inverters for semiconductor based biomedical applications. It presented the ISFET based chemical switch and a Schmitt trigger circuit aimed to enhance its input noise immunity. In order to make it more sensitive, a simple way was presented to amplify its input referred sensitivity. Finally, a fast matching method was presented that can be used to hugely reduce mismatch of arrays of chemical switches without adversely affecting mobile ionic charges in the passivation layer.

Generally, all previous ISFET related work viewed it as a MOS device with the reference voltage being its remote gate. The chemical signal affects its threshold voltage. This is basically how it was first introduced by Bergveld around forty years ago [1]. Even in CMOS, the same view persisted, though researchers understood that ISFETs in CMOS are floating gate transistors [2] with the superposition of the reference voltage and the chemical voltage as its input.

The floating gate voltage of FG-MOS is the weighted sum of its inputs [3]. This inspired bright researchers to exploit this feature in order to overcome known non-ideal behaviours of ISFETs. For example, Dr. Georgiou invented the notion "programmable gate ISFET (PG-ISFET)" where an electrical input was coupled to the ISFETs floating gate in order to compensate for trapped charges and drift [4] and [2]. This was extended by Dr. Liu who reported a dynamic system with two coupled nodes to the ISFET floating gate [5] and [6]. A general ISFET model that reflects the ISFETs floating gate nature and accounts for the coupling weight of the chemical input via the passivation capacitance and other inputs while considering the actual MOS electrical input was reported in [7].

Because of the analogy of ISFETs with floating gate transistors, this thesis started with reviewing the FG-MOS transistors in chapter 2. After introducing their operation, their main problem of trapped charges was reviewed. Different ways of addressing it were listed while the more relevant method for this thesis, electron tunnelling, was presented with more details. A word about FG-MOS digital and analogue applications followed.

The ISFET was reviewed in chapter 3. After introducing basic devices and those built in CMOS, the chemical sensitivity was reviewed in order to present ISFET models. Non ideal behaviour of ISFETs was presented next. It was followed by a presentation of noise in ISFETs. Finally, the chapter was concluded after a word about interfacing circuits and applications.

In chapter 4, the floating gate CMOS inverter was reviewed. It was extended to the ISFET based chemical switch, which was the first contribution in this thesis. It was the first reported circuit that allowed two transistors to share the same ion sensitive membrane of an ISFET. It basically drew a line between the transistor part and the ion sensing part of the ISFET. The link between them being the floating gate. The transistor part may be composed of one or more transistors sharing the same floating gate; which,

in turn, may have a number of capacitively coupled inputs that can be electrical or chemical via ion sensing membranes. Simulations, and measurements of the chemical switch were presented. In order to increase its input noise immunity, it was extended to the chemical ISFET based Schmitt trigger. Measurements were presented. The work of this chapter was reported in [8], [9] and [10]. Dr. Liu was inspired by this work and used it to build an ISFET read out scheme based on pulse width modulation; which was reported in [11].

In floating gate MOS and ISFETs, the floating gate voltage is the weighted sum of its inputs. Exploiting this feature with the aim to scale the chemical signal at the point of measurement was the subject of chapter 5. It started by reviewing reported semiconductor ion sensitive devices with sensitivities higher than the Nerstian limit; which is the maximum theoretical limit for solid state devices including ISFETs. A very simple and straight forward method based on sizing the capacitive coupling of inputs was presented. It was simulated and measured for both a single transistor ISFET and a chemical switch. This chapter resulted in the paper [12].

In chapter 6, a method to match an array of ISFETs or ISFET based chemical switches was proposed. It began with a review of ISFET's matching techniques reported in literature. Then, according to ISFET analogy to floating gate MOS, it reviews the results of hot electron injection in ISFETs. As electron tunnelling was not tested on ISFETs before this work, the use of this method to alter ISFET's floating gates was found here. After evaluating these techniques, the indirect bidirectional electron tunnelling was chosen for ISFET floating gate programming. The same method was used to match an array of ISFET based chemical switches. experimental results were presented. First part of the work of this chapter was published in [13] while the second part was sent to IEEE sensors journal and is still under review.

The work, curried here, focused on addressing some of the problems biomedical systems

are faced with. Particularly, pH change detection for the purpose of DNA sequencing. Solutions were proposed, studied, and tested in order to lay the foundation for point of sensing threshold detection aiming to gain an understanding of the proposed structures, their related challenges, and limitations. This lays the path for designing new systems that make use of the presented building blocks.

7.2 Future Work: Towards fully digital biomedical sensory systems

ISFET blocks in biomedical circuits have traditionally been analogue [8]. Digital signal processing has generally been a need [14] [15]. Having analogue and digital circuits in the same die has its own pitfalls and noise constraints. The aim of this thesis was to bring the digital circuits as it can be to the sensing point. Having introduced the switch as a sensing element alleviate the need for analogue blocks. The sensing operation was reduced to threshold detection. However, what was presented is just the detection of one threshold, or just one bit operation. This is already very useful for applications where the interest is in a single threshold. An example, in DNA sequencing, is whether base pair extension took place or not.

However, in a number of applications, the detection of one threshold is not enough. An example, still with DNA sequencing, would be if a base pair extension took place, was the detected signal for one insertion or multiple insertions for the same base pair. Here, it becomes useful to detect a number of threshold levels. Still analogue blocks are to be avoided. There must be a number of ways to achieve this. Two methods are to be presented here as future work after proposing a possible system concept for indirect bidirectional tunnel programming of ISFETs.

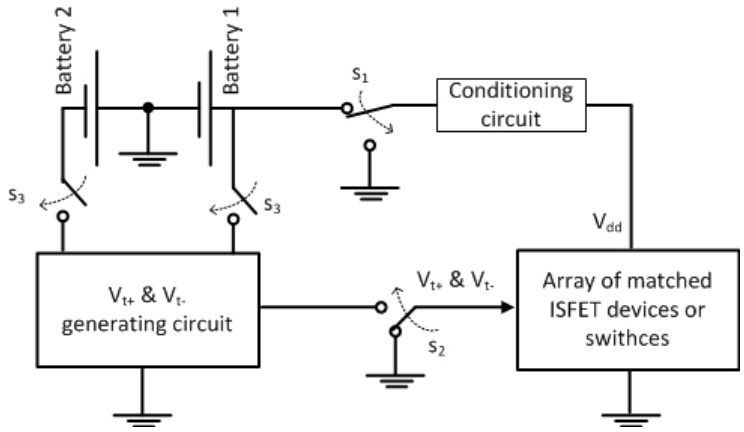

Figure 7.1: Measured output of a 2 bit ISFET based pH flash thermometer code analogue to digital converter.

7.2.1 Self programmable array of ISFETs with Indirect bidirectional tunnelling

The bidirectional indirect tunnelling method may be used to match arrays of ISEFT transistors or switches in lab on a chip applications for hand held devices. This is particularly useful for point of care applications and portable pH measuring equipment. These devices require the use of batteries to provide for all its power requirements. In order to provide for the tunnelling voltage in both positive and negative polarities, two batteries may be used with their middle point being the ground. Normal measuring operation is carried when the connections are as in figure 7.1. All switches are used simultaneously at the beginning of measurement or when a reset button is pushed. In this case, the system goes into matching mode where prearranged tunnelling voltages are applied to the ISFET array in order to program floating gates' charges. The circuit goes back to normal measurement mode after matching. V_{dd} is generated by a bias conditioning circuit while V_{t+} and V_{t-} are outputted by their generating circuit.

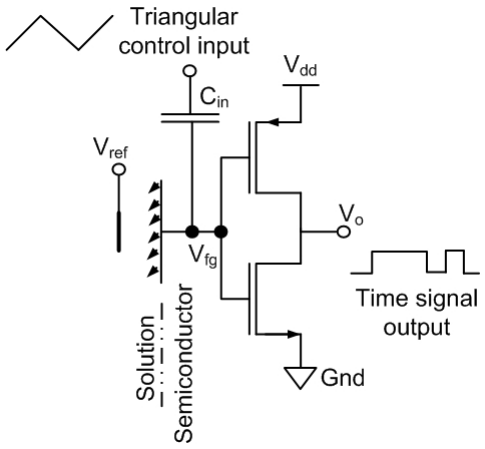

Figure 7.2: Structure of pH to time sensor proposed in [11].

7.2.2 Matched Chemical Switches Based Pulse Width Modulation Readout

In [11], Liu et al presented a pulse width modulation readout that uses the chemical inverter, presented in chapter 4, as the basic building block. It has a capacitively coupled control input to the ISFET based inverter floating gate, figure 7.2. It inputs a traingular control signal that is converted in the inverter to a pulse width modulated signal, which was called time signal. Its pulse width is altered by the solution's pH. Its output can easily be converted to a digital signal using a pulse width to digital conversion. In that paper, it was stated that this circuit may compensate for floating gate trapped charges up to about $1V$ according to the chosen signal levels and coupling capacitances.

That circuit addressed both the electrical $1/f$ noise and the chemical noise, which was also modelled with $1/f$ behaviour, by using an AC input. Thus, if operated above its corner frequency, where total $1/f$ noise equals thermal noise, would have the advantage of reduced noise. However, the chemical noise is scaled by the same ratio as the chemical signal, C_{pass}/C_{in}. This would be improved if the triangular signal was provided via V_{ref} where scaling of both chemical signal and noise is removed. This maximises the

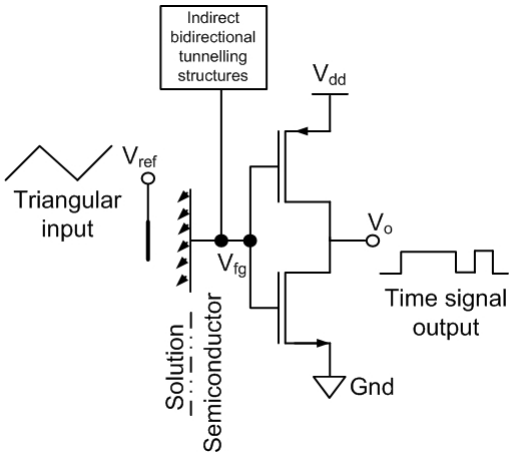

Figure 7.3: Structure of pH to time sensor proposed here.

chemical coupling capacitance at the price of losing the advantage of amplifying the chemical signal.

Here, the indirect bidirectional tunnelling structures presented in chapter 6 would provide a means to bringing the trapped charges in the array of inverters to a point closest to the middle point of the planned triangular input. This would preferably be $V_{dd}/2$. Thus, the floating gates of the inverter arrays may be planned to have the correct amount of trapped charges in order to bring the average switching voltage very close to this point, $V_{dd}/2$. This matching process is not perfect as it allows for small but limited variations that can be compensated for by the reading scheme.

Thus, the basic block would be as depicted in figure 7.3. Here, the amplitude and frequency of the triangular signal input may be chosen in such a way to compensate for trapped charge variations that remain after matching. This is expected to be within $\pm 100mV$ of the average chosen switching point. In the same time the input frequency should be chosen in such away to minimise flicker noise.

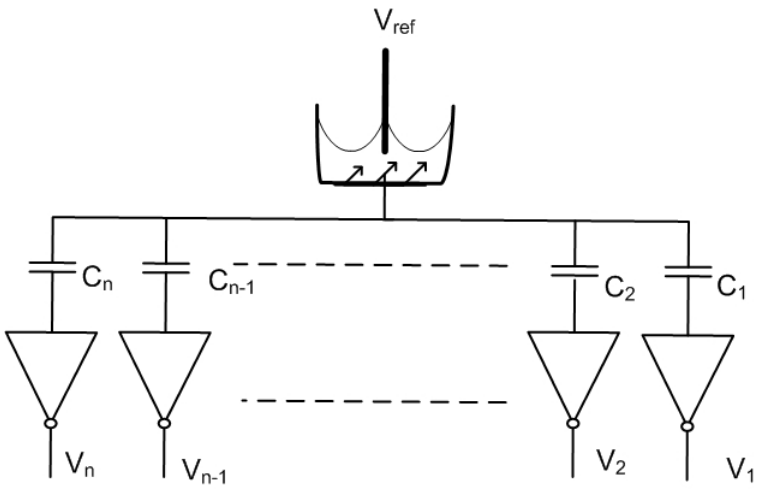

Figure 7.4: Structure of an ISFET based pH flash thermometer code analogue to digital converter.

7.2.3 Chemical Switches with Multiple Thresholds

Another method to realise multiple thresholds for a chemical switch is to use the weighted coupling nature of floating gates. That is to connect to the same flaoting gate of a chemical switch, presented in chapter 4, to more than one electrical inverter with different coupling weights. Figure 7.4 depicts a flash analogue to digital converter that converts the pH signal into an n bit thermometer code output. The capacitors, C_1 to C_n are to be increasing in size while the inverters are identical circuits. This way, each device will see a different pH threshold than the rest. And these thresholds can be chosen by properly sizing these coupling capacitors.

This circuit was simulated in cadence using the AMS $0.35\mu m$ process kit. The switching threshold voltages for a 24 bit output is shown in figure 7.5. To demonstrate the idea, a circuit was built with $n = 2$. Its measured output is depicted in figure 7.6.

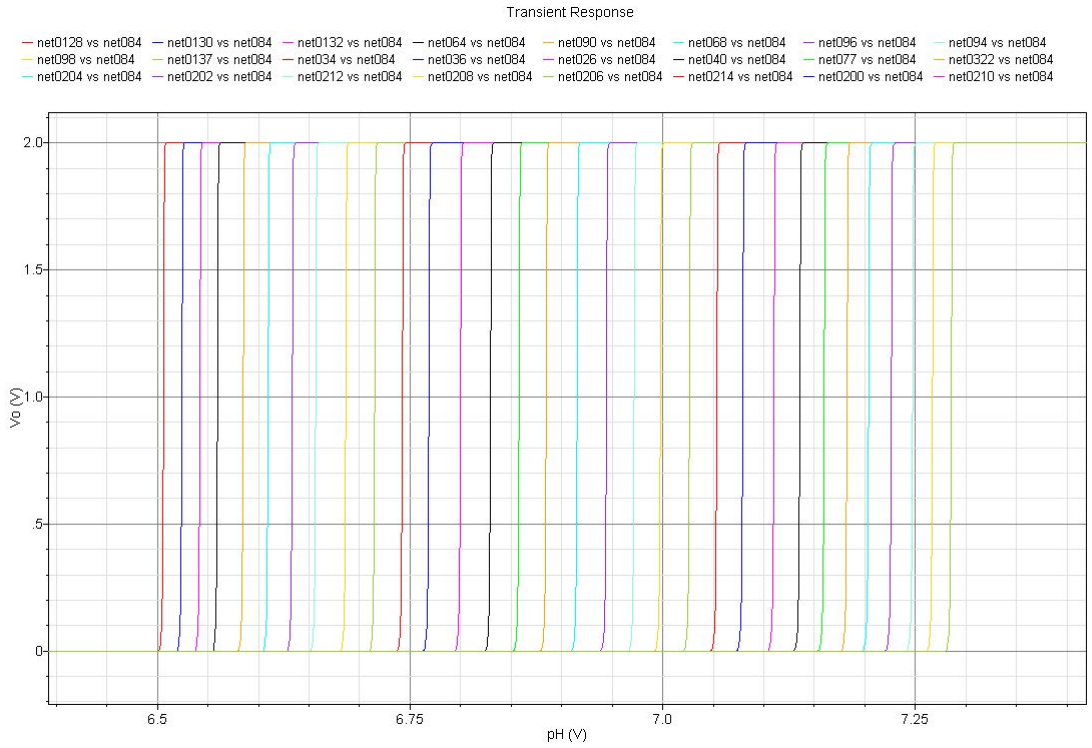

Figure 7.5: A simulated example of switching points of a 24 bit ISFET based pH flash thermometer code analogue to digital converter.

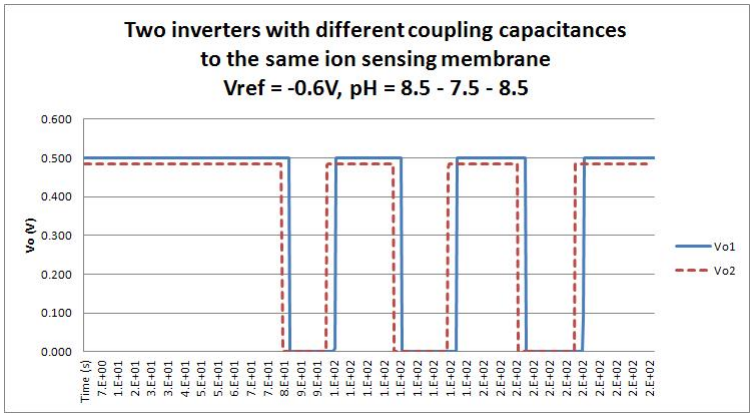

Figure 7.6: Measured output of a 2 bit ISFET based pH flash thermometer code analogue to digital converter.

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Appendix A

Publications

A.1 Publications arising from this work

1. Abdulrahman Al-Ahdal, and C. Toumazou, "ISFET based Chemical switch", IEEE Sensors Journal, Vol. 12, No. 5, May 2012, pp. 1140 -1146.

2. Abdulrahman Al-Ahdal, and C. Toumazou, "High gain ISFET Based νMOS Chemical Inverter", Sensors and Actuators journal: B chemical, In Press, vol: 171, no. 1, pg. 110-117, 2012.

3. Abdulrahman Al-Ahdal, and C. Toumazou, ISFET threshold voltage programming in CMOS using electron tunnelling, Electronics letters [0013-5194], vol: 47, No:25 pg:1398, 2011.

4. Abdulrahman Al-Ahdal, and C. Toumazou, A Digital CHEMFET basic block, the MELECON 2012 conference, March 2012.

5. Abdulrahman Al-Ahdal, and C. Toumazou, ISFET based Chemical Schmitt trigger, electronics letters, vol: 48, No:10 pg:549 -550.

6. Y. Liu, A. Al-Ahdal, P. Georgiou, C. Toumazou, A Minimal Readout Scheme For ISFETSensing Arrays based on Pulse Width Modulation, electronics letters, vol: 48, No:10 pg:548 -549.

7. Abdulrahman Al-Ahdal, and C. Toumazou, CMOS ISFETs Threshold voltage programming using indirect bidirectional Electron Tunnelling, IEEE sensors journal, under review.

A.2 Patent applications

1. C. Toumazou and Abdulrahman Al-Ahdal, ISFET Device,International Publication number WO 2012/046137 A1.

2. C. Toumazou, Abdulrahman Al-Ahdal, Method and Apparatus for matching Arrays of ISFET Devices and Switches, not granted yet.

3. C. Toumazou, Abdulrahman Al-Ahdal, Chemical Schmitt trigger, not granted yet.

Appendix B

Fabricated Chips

Two dies were fabricated in the course of this thesis. The first was code named: Tom and Jerry chip B.1 and the second was code named Asterix B.2. The former contains, among other test structures, all circuits used here apart from the Schmitt trigger circuit which was in the second die.

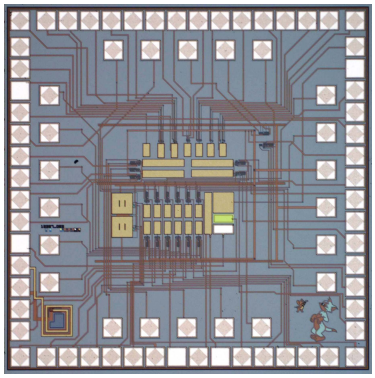

Figure B.1: AMS 0.35 μm, Tom and Jerry chip.

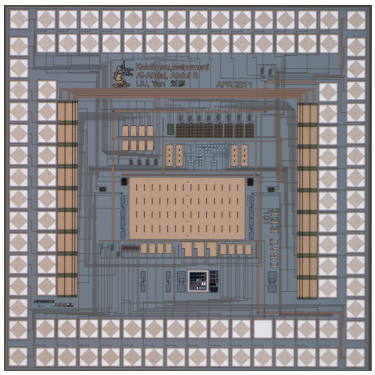

Figure B.2: AMS 0.35 μm, Asterix chip.

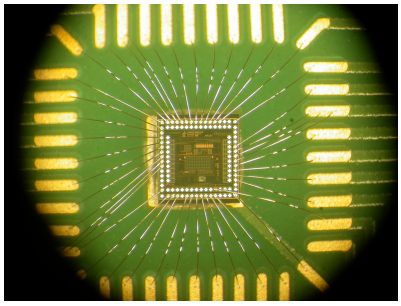

Figure B.3: Bonded Asterix chip before encapsulation.

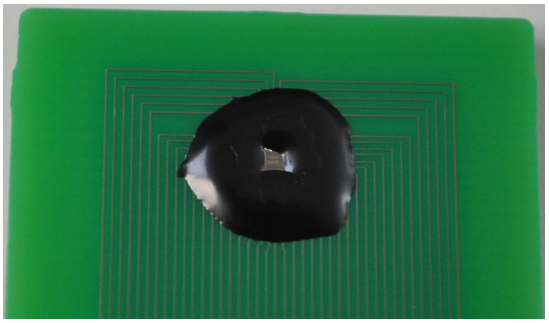

Figure B.4: Tom and Jerry die after encapsulation.

Appendix C

Experimental Setup

The measurement experimental set up is composed of the the equipment shown in figure C.1. Experiments where pH was changed by titration, were first calibrated using the set-up of figure C.2 where Mettler Tolido Seven easy temperature compensated pH meter was used to measure pH changes. Then, the first set-up was used with the addition of pipettes to introduce acid and base as needed.

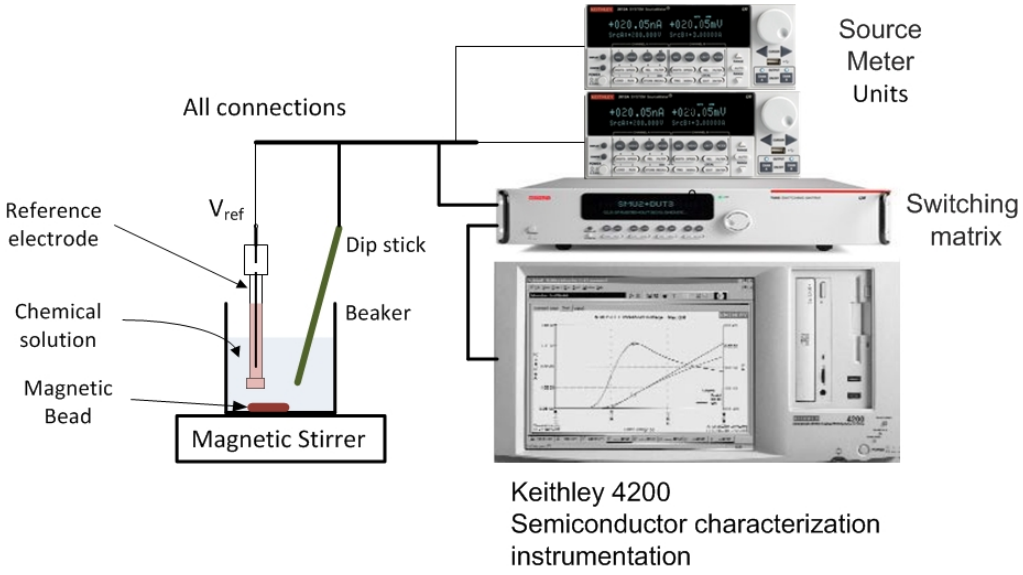

Figure C.1: Test instrumentation for sensor circuits.

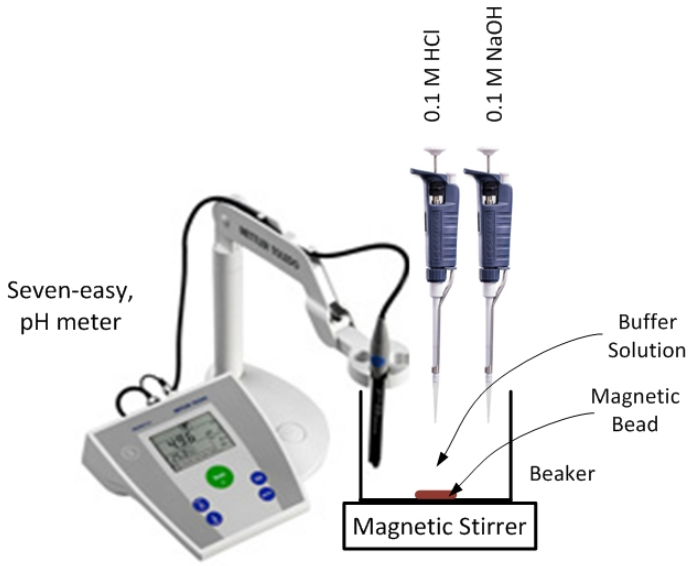

Figure C.2: pH measurement set-up.

Appendix D

Buffered Inverter Analysis

The general aim has been to produce a digital output from the analogue chemical signal. The input stage is an open loop push pull inverting amplifier built by two complementary CMOS transistors. The output of that stage (V_1) was further amplified by an identical second stage, figure D.1. Its output (V_2), is basically digital and may be used as an input for in chip circuits. However, for the aim of measurements, a larger third stage was used as a digital block in order to provide the needed fan out. Following is a presentation of their analysis.

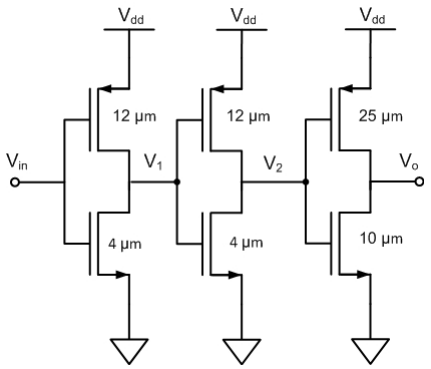

Figure D.1: Schematic of used inverter buffering stages with transistor sizes.

Table D.1: Simulated V_{in} range for the transition from 10% to 90% of V_{dd} for the output of each stage of the cascaded inverter, along with the corresponding pH range assuming $45mV/pH$ sensitivity.

V_{dd} (V)	V_1 (mV)	V_2 (mV)	V_o (mV)	V_1 (pH)	V_2 (pH)	V_o (pH)
1	16.8	1.38	0.17	0.373	0.031	0.003
2	112	4	0.13	2.49	0.089	0.004
3	403	21.6	1.2	8.96	0.480	0.027

The Switching Point

The switching threshold voltage (V_{sth}) of the CMOS inverter is the point where the input voltage (V_{in}) equals the output voltage, $V_{in} = V_o$. Thus $V_{gs} = V_{ds}$ for both transistors. This means, during switching, both, when in the normal strong inversion region, are in saturation. Equating both transistors' currents and solving for $V_{in} = V_{sth}$ gives [1]:

$$V_{sth} = \frac{r(V_{dd} - |V_{tp}|) + V_{tn}}{1 + r} \tag{D.1}$$

Where

$$r = \sqrt{\frac{k_p}{k_n}} \quad , \quad k_n = \mu_n \times C_{ox} \quad and \quad k_p = \mu_p \times C_{ox}$$

Here, V_{tn} and V_{tp} are threshold voltages while k_n and k_p are the process transconductance parameters of the nMOS and pMOS transistors. μ_n and μ_p are the electron and hole mobilities while C_{ox} is the gate oxide capacitance [1].

This switching threshold voltage depends only on MOS parameters and the rail voltage. Switching occurs when V_{in} changes across V_{sth} going higher or lower than it.

The switching point of the cascaded inverters does not change from one stage to another as the first stage decides it. The second stage see steeper version of the input. The third

Table D.2: Simulated noise margin of cascaded inverters, $V_{dd} = 3V$.

NM	stage 1	stage2	stage 3
NM_l (V)	1.22	1.422	1.473
NM_h (V)	1.29	1.477	1.535

stage will just see a digital signal. This was verified by simulation. For example, for $V_{dd} = 2.0V$, $V_{sth} = 0.936V$ for the output of each stage. That is not the case with the dynamic range, which is the range of the input signal that causes the output to move between 10% and 90% of its maximum. Table D.1 lists the simulated dynamic range for this circuit as seen at after each stage. Assuming $45mV/pH$ sensitivity, it shows the corresponding pH dynamic range.

Noise Margin

The simulated out put voltage V_1 of the first stage of figure D.1 is shown in figure 4.6. V_{sth} is shown as the intersection between V_o curve and the line $V_0 = V_{in}$. There are two points where the output slope equals -1, namely V_{il} and V_{ih}. They define the inverters noise margin. Their analytical solution is tedious and adds no insight into the circuit [2]. Nevertheless, they may easily be approximated using piece wise linearisation where the slope in the transition region is assumed constant and equal to the gain at the switching point (G_1). Thus [3]:

$$V_{ih} - V_{il} = -\frac{V_{oh} - V_{ol}}{G_1} \;=\; \frac{-V_{dd}}{G_1}$$

This gives:

$$V_{il} = V_{sth} + \frac{V_{dd} - V_{sth}}{G_1}$$

and

$$V_{ih} = V_{sth} - \frac{V_{sth}}{G_1}$$

Therefore, the noise margins NM_h and NM_l are given be:

$$NM_l = V_{il} \qquad and \qquad NM_h = V_{dd} - V_{ih}$$

Now this output becomes the input to the second stage whose output in turn becomes the input to the third stage. The noise margin increase after each stage D.2.

Gain

The gain may be found by equating the current of both transistors and solving for dV_0/dV_{in} [2]:

$$\frac{V_0}{V_{in}} = -\sqrt{2/I_d}\Big(\frac{\sqrt{k_n(W_n/L_n)} + \sqrt{k_p(W_p/L_p}}{\lambda_1 + \lambda_2}\Big) \tag{D.2}$$

Sitting $V_{in} = V_{sth}$ and ignoring second order terms gives [3]:

$$G \approx \frac{1+r}{(V_{sth} - V_{tn} - 0.5V_{DS_{satn}})(\lambda_n - \lambda_p)} \tag{D.3}$$

Where $V_{DS_{satn}}$ is the saturation drain-source voltage difference for the n-MOS transistor. Figure 4.7 depicts the gain of one stage of the used inverters. Equation D.3 predicts the inverter's gain to be solely determined by the technology parameters particularly channel length modulation (λ). The designer may choose gain by designing V_{sth}, by transistor sizing, and their region of operation. The gain after the second and third stages will simply multiply,

Table D.3: Simulated gain of each stage of the cascaded inverters, $V_{dd} = 3V$.

V_{dd}	stage 1	stage2	stage 3
3 V	-18.57	350	-6,354
2 V	-28.8	1313	-22,450
1 V	-51	2311	113,000

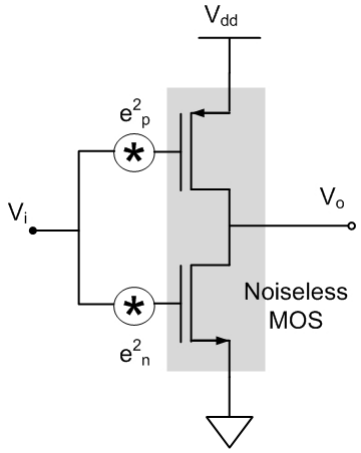

Figure D.2: Noise model of CMOS inverter.

Noise

This circuit is composed of two transistors. Its noise model would be as depicted in figure D.2 where e_n^2 and e_p^2 stand for the pMOS and nMOS noise spectral densities. This is an interesting situation, since both transistors can act as input or load, none of them dominates noise generation. The only way to reduce noise is to reduce noise contribution of each device. Moreover, the equivalent input noise spectral density is not their simple addition. It was found to be [2]:

$$e_{eq}^2 = \left(\frac{g_{m_n} e_n}{g_{m_n} g_{m_p}}\right)^2 + \left(\frac{g_{m_p} e_n}{g_{m_n} g_{m_p}}\right)^2 \tag{D.4}$$

Appendix E

Fowler-Nordheim tunnelling verilogA model

The model encoding of Fowler-Nordheim tunnelling is based on equations,

$$I_{tun} = I_0 E_{ox}^2 e^{\left(\frac{V_0}{V_{ox}}\right)} \tag{E.1}$$

Where:

$$I_0 = \frac{q^2 A}{16\pi^2 \hbar \phi_{ox}} \qquad and \quad V_0 = \frac{-4t_{ox}\sqrt{2m^*}(q\phi_{ox})^{3/2}}{2\hbar q}$$

A_0 and V_0 are process and design dependant. For the purposes of this thesis, they are as shown in the code below. However, they need to be recalculated for the process in hand. Here comes the verilogA code for the case of tunnelling from n-diffusion to floating gate. For the tunnelling from floating gate to p-diffusion, the same code may be used where the current flows in the opposite direction.

```
// VerilogA for FN tunnelling, veriloga

`include ``constants.vams``
`include ``disciplines.vams``

// module name and its terminals: diffusion and floating gate.
module FNT(ndiff,fgate);

//terminal usage declaration
inout ndiff, fgate;

// electrical nodes declaration
electrical ndiff, fgate;

// parameter types and values declaration
parameter real V0 = 386.04;
parameter real I0 = 9.35e8;

// actual equations
analog begin
Vtun = abs(V(ndiff,fgate));
I(n_{diff},fgate)<+ I0*exp(-V0/Vtun);
end
endmodule
```

Appendix F

V_{chem} verilogA model

V_{chem} models the total voltage difference between the reference electrode input and the outer plate of the ion sensing membrane, which is the gate oxide in basic ISFET while it is the passivation insulator for the CMOS ISFET. Its VerilogA encoding is based on the equation:

$$V_{chem} = \gamma + 2.3U_T\alpha\ pH$$

Where, γ is a grouping of all pH independent terms including the small contact potential change between the reference electrode input and the solution's bulk. Following is the code [4].

```
// VerilogA for ISFET, Vchem, veriloga

`include "constants.vams"
`include "disciplines.vams"

// module name and its terminals
```

```
module Vchem(ref,pH,gate);

// terminal usage declaration
input ref,pH;
inout gate;

// electrical nodes declaration
electrical n10,ref,pH,gate;

// alpha type and value declaration
parameter real alpha=0.75;

// gamma component parameter types and values declaration
real Eabs = 4.7;
real Phim = 4.7;
real Erel = 0.2;
real Chieo = 3e-3;
real Philj = 1e-3;;

// actual equations

analog begin
V(ref,n10) <+ Eabs-Phim-Erel+Chieo+Philj;
V(gate,n10) <+ -1*2.3*alpha*\vt*(V(pH)-3);
end
endmodule
```

References

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