Hermetic packaging for implantable microsystems: Effectiveness of sequentially electroplated AuSn alloy

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***Abstract*— With modern microtechnology, there is an aggressive miniaturization of smart devices, despite an increasing level of integration and overall complexity. It is therefore becoming increasingly important to be achieve reliable, compact packaging. For implantable medical devices (IMDs), the package must additionally provide a high quality hermetic environment to protect the device from the human body. For chip-scale devices, AuSn eutectic bonding offers the possibility of forming compact seals that achieve ultra-low permeability. A key feature is this can be achieved at process temperatures of below 350°C, therefore allowing for the integration of sensors and microsystems with CMOS electronics within a single package. Issues however such as solder wetting, void formation and controlling composition make formation of high-quality repeatable seals highly challenging. Towards this aim, this paper presents our experimental work characterizing the eutectic stack deposition. We detail our design methods and process flow, share our experiences in controlling electrochemical deposition of AuSn alloy and finally discuss usability of sequential electroplating process for the formation of hermetic eutectic bonds.**

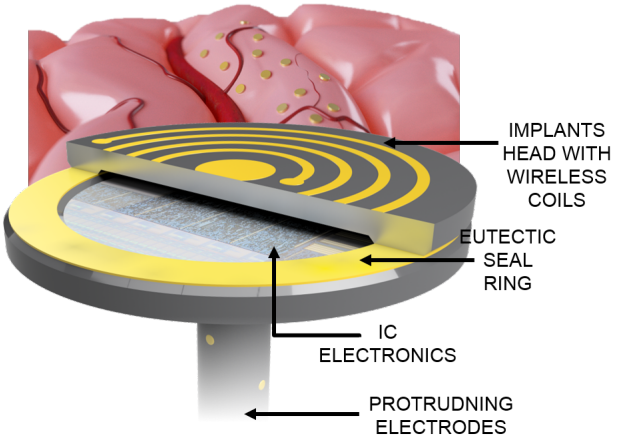

Fig. 1. Concept for packaging future implantable neural microsystems for intracortical recording [6], [7] based on eutectic bonding.

I. Introduction

Reliable packaging of next generation of implantable medical devices is one of the most challenging aspects of their design, as it largely influences their size and performance. Over recent years, thanks to significant advancements in integrated circuit design and wireless communications there is a growing need of integrating these capabilities within medical devices to create fully independent, distributed systems [1]. For the package it means that apart from of a small footprint, reliability and biocompatibility, it must conform to constraints imposed by CMOS compatibility and also transparency to the communication signal, e.g. electromagnetic wave. Moreover, the packaging must support often complex geometries of sensing elements and protruding electrodes by providing them with stable mechanical and electrical interconnects. Because implants operate in delicate and moist biological environment, standard CMOS insulation layers are not sufficient enough to provide protection from corrosion that could result in electronics failure [2].

Thus far, the vast majority of implants packages are in form of cans made of metals or glasses which are welded together or of thick polymer coatings, mainly medical-grade silicones [3]. Despite a high level of hermeticity and maturity of technology, metal housings are rather large and prevent possibility of wireless communication. Glass and quartz packages require singular processing, thus increasing overall fabrication time [4]. On the other hand, polymers provide only limited level of barrier against moisture penetration and can suffer delamination problems, unless they are several hundred microns thick [5].

Despite this, the possibility of hermetically enclosing implant electronics at wafer scale using only narrow seal rings with addition of in silicon feedthroughs is highly desirable. Taking into account how delicate the electronics are, and that these need to be implanted and operate within the body, only a few bonding methods exist that do not involve high temperatures or toxic materials. Among these, eutectic bonding is well established and can be performed using relatively relaxed environmental parameters, allowing for wafer-scale processing.

The concept of using eutectic bonding for medical device packaging relies on a single seal ring in between faces of two planar substrates containing electronic circuitry and wireless communication elements. Both the thickness and width of the joint are in the range of microns, thus allowing for overall size reduction and more design freedom. Such an approach allows for the significant miniaturization of the package. This could be used both in already established implantable medical devices, such as cochlear and cardiac implants, as well as in future electroceuticals [8]. As an example, in intracortical neural interfaces, eutectic bonding

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is compatible with currently used fabrication techniques and could be placed around the rim of the implant head that is floating at the surface of the brain. This concept is shown in Fig. 1.

Of several eutectic stacks, we have selected gold-tin because of the high joint strength, fluxless process, reliability in harsh condition and low eutectic temperature of 278°C. This allows for post-processing of CMOS devices (i.e. CMOS-compatibility). Au-Sn eutectic bonding is already used commercially in the packaging of MEMS timing devices, thus demonstrating the viability [9]. Regardless of the mechanical properties, gold-tin solder alloys are biocompatible, and have been widely used in dental applications [10]. To provide a good joint, the eutectic must be exactly at 80Au20Sn (wt.%) composition. Physical vapor deposition methods allow for only thin layers, and where thick stacks are needed electroplating or solder preforms are used. Electrochemical deposition allows for wafer-scale, fully semiconductor technology-based processing. Alloy-plating solutions are few and unstable over time while sequential plating is troublesome because of different acidity of solutions and necessity of accurate control of plating characteristics for each bath.

In this paper, we explore the challenges in wafer-level sequentially electroplated eutectic layers for bonding purposes. The remainder of the paper is organized as follows: Section II describes the design methods and process flow; Section III detail the fabrication results; Section IV discusses issues encountered; and Section V concludes this work.

II. Methods and materials

A. Seal design

To identify the effect of electroplating on different seal ring geometries the mask set containing 36 different designs was implemented. Overall, three sizes (4 mm^2, 9 mm^2, 16 mm^2), with four widths (30 μm, 60 μm, 90 μm, 150 μm) and three different shapes (circular, rectangular and chamfered) of seal rings have been tested. Eutectic stacks heights were either of 3 μm or 11 μm corresponding to Au(1.8 μm)-Sn(1.2 μm) and Au(6.6 μm)-Sn(4.4 μm) tin-rich compositions. Additionally, some of the geometries contained gold-only rectangular standoffs, placed either inside or outside of the seal rings. These are aimed to act as a spillage stoppers preventing liquid solder squeeze-out during bonding phase.

B. Lid and eutectic wafers fabrication

The process flow is shown in Fig. 2. Electroplated gold-tin eutectic seal rings were fabricated on double-side polished, standard thickness (525 μm) 4-inch (100) silicon wafers. To ensure substrate properties did not influence our tests, a total thickness variation of wafers was less than 2.3 μm. Wafers were first oxidized, either by means of dry thermal oxidation or by plasma enhanced CVD, to the oxide thickness of respectively 130 and 200 nm.

Substrates were evaporated with thin adhesion layer-30 nm of chromium or titanium, followed by 60 nm of gold seed layer for electroplating. Spill-preventing rectangular structures were patterned in AZ15nxt (150 cps) negative photoresist and subsequently electroplated with gold to the thickness of either 70% or 30% of corresponding eutectic stack height- that is 2.1 μm for 3 μm stack height and 3.5 μm for 11 μm stack height. Lid wafers were cleaned and again patterned to cover gold standoffs. The outlines of seal rings were formed by differential etching of surrounding layers of chromium and gold. Membranes for the purpose of deflection test indicating hermeticity of bonds were patterned and etched to the depth of approximately 250 μm in the center of each chip by selective oxide removal in buffered hydrofluoric acid followed by deep reactive ion etching.

Eutectic wafers were twice patterned in thick AZ15nxt (450 cps) photoresist. First, for the sole purpose of gold electroplating, and then after photoresist was stripped, for the tin electroplating cycle. After photoresist removal in heated NI555 remover, wafers underwent differential wet etching of adhesion and seed layers and were solvent-cleaned.

C. Eutectic stack electroplating

Thick gold layers were electroplated from commercial, ready-made ECF60 sulfite-based gold electroplating solution, without addition of brighteners or grain refiners. Throughout the experiment, the solution was monitored and kept within 9.4 – 9.5 pH value and constant temperature of 58°C with 550 rpm magnetic stirring. Deposition was performed in pulsed chronopotentiometry mode in 15 s deposition: 30 s break cycles at current density of 3.5 mA/cm^2, which produces layers of low stress [11]. As a reference and counter electrodes, Ag/AgCl electrode and 100 cm^2 platinized titanium mesh were used. During deposition the distance between electrodes was in the range of 3 cm to 5 cm.

Tin plating was done at room temperature in ready-made methanesulphonic acid-based NB Semiplate Sn100 solution, without stirring. As a reference and counter electrodes, Ag/AgCl electrode and 100 cm^2 pure tin sheet were used. Similarly to gold processing, deposition was done in pulsed chronopotentiometry mode in 15 s deposition: 30 s break cycles at current density of 25 mA/cm^2, as suggested by the manufacturer. After reaching desired thickness of eutectic stack, superficial layer of deposited tin was once again flash-plated with thin gold layer to prevent oxidation.

D. Bonding

In order to test the usability of the layers in joining process, corresponding wafers were cleaned in oxygen plasma and transferred to AML AWB05 wafer bonder for the eutectic bonding process. Wafers were aligned in situ and kept in vacuum atmosphere to prevent any oxidation. Substrates were held together by constant low force of 50 N while heating from room temperature to 315°C (at the rate of 10°C/min) at which they were kept for 10 minutes. Subsequently, the pairs were left under vacuum for controlled cool down back to room temperature.

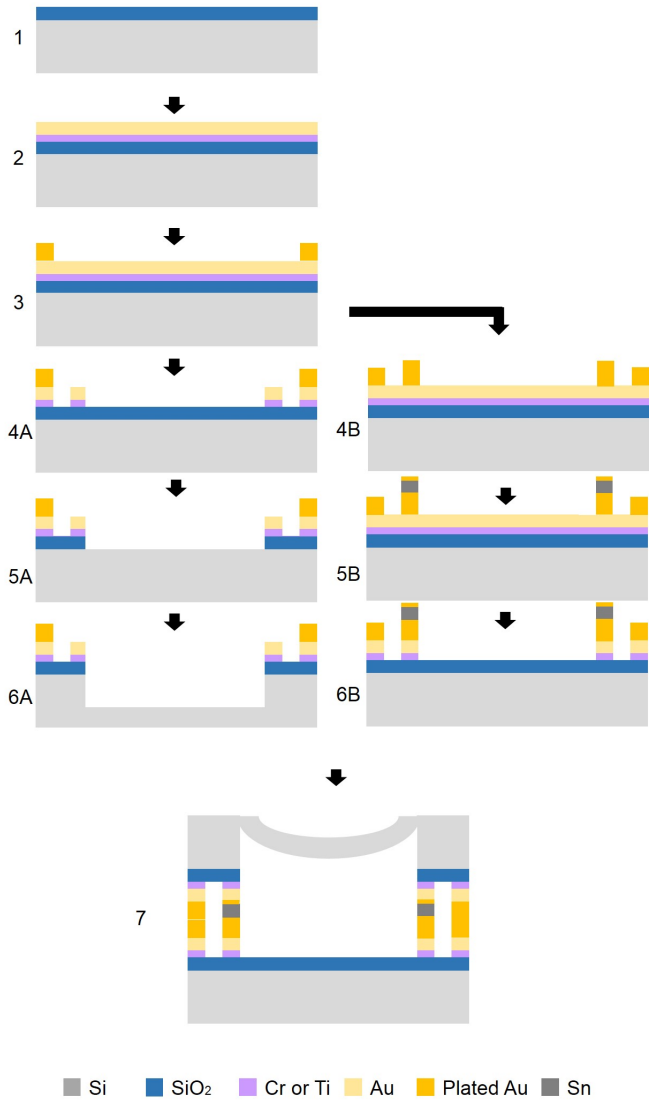

Fig. 2. Process flow for the fabrication of lid and eutectic wafers: (1) oxidation; (2) adhesion and seed layer deposition; (3) spill stopper electroplating; (4A) eutectic frame definition on lid wafer; (4B) gold electrodeposition for frames on base wafer; (5A) oxide removal; (5B) tin and flash gold electrodeposition; (7) bonding.

III. Experimental Results

A. Electroplating

Prior to bonding the height of deposited stacks was measured by contact profilometry, to estimate deposit thickness deviation across the wafer and to evaluate resulting plating rate.

Between feature widths of 30 μm and 150 μm the rate of resulting deposition was different by 50 nm/min for gold deposition and by 87 μm for tin deposition. The area of the largest deviation in comparison to entire wafer was located the closest to the magnetic stirrer pellet during plating, where the solution's mixing rate was the fastest. Overall the most significant thickness deviations were found around the edges of the wafer.

Across various wafers, under same conditions, electroplating rate was varying by 2% – 11% for gold plating and by more than 15% during tin plating. Because of intense frothing, tin layers locally exhibited spherical over-deposits of poor anchorage to the substrate. The size of the tin over-deposits and resulting non planarity of layer could hinder bonding phase, hence they were removed by the means of ultrasonication in water.

Overall deposited tin layers are characterized by much more developed morphology and grain size than those of gold. Because of that, accurate control of thin layers is compromised by the grain size, which for tested deposition parameters was in the range of 0.5 – 1 μm. Moreover, tin deposits did not form continuous uniform layers and formed dense, spherical islands of material instead.

It was found out that despite being dedicated for use in electroplating, photoresist AZ15nxt after long cycles of subsequent plating was exhibiting local cracking and lifting off around the wafer edges. This lead to underplating of material near the cracks (see Fig. 2-F). That is why it was decided to run two separate patterning steps both before gold and tin, which solved the photoresist stability problem. On account of lack of substrate's backside cover, significant metallic deposits of poor adhesion were forming there during electrodeposition cycle, which then needed to be removed by ultrasonication.

B. Influence of adhesion layer

After photoresist removal and differential etching of sputtered gold and chromium, 11 μm high stacks of plated eutectic composition were lifted of the surface of wafer during pre-bonding cleaning steps, due to the poor adhesion to chromium layer underneath (Fig. 3-E). This was not observed in wafers deposited with titanium adhesion layer.

C. Bond stability

Bonded pairs were initially inspected via observing the extent of membrane deflection. Pair with plated 11 μm stack height pair exhibited clearly concave membranes over 70% of chips on the wafer, suggesting good hermeticity level of formed joints. However, during subsequent dicing step to release singular chips for testing, wafers peeled off each other, most likely because of internal stresses within rigid seal being enhanced by poor adhesion to underlying thin chromium film. Pair with 3 μm high stack failed bonding attempt, with wafers remaining in separation despite temperature cycling. Later performed scanning electron microscopy inspection revealed non-uniform and cracked surface of the seal ring (see Fig. 3-F).

IV. Discussion

Sequential electroplating despite being seemingly straightforward, has proven challenging for deposition of layers of accurate stoichiometry. Different characteristics of plating baths cause problems in choosing the right masking material. Positive photoresists do not withstand prolonged exposure to alkaline character of gold plating solution, whereas negative

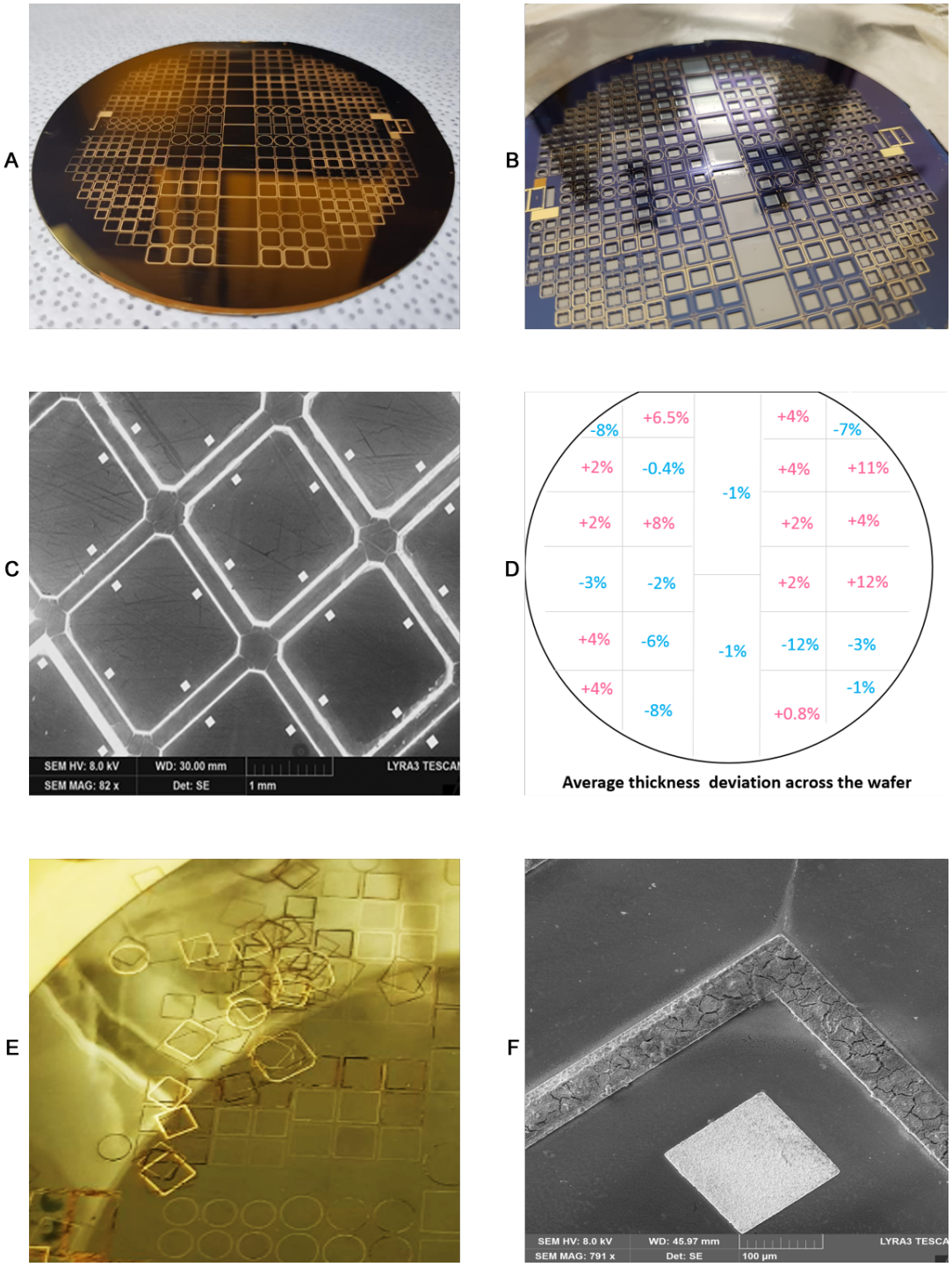

Fig. 3. Photos of our engineering samples. Shown are: (A) patterned bottom eutectic wafer before differential etching of seed and adhesion layers; (B) lid wafer with deep-etched membranes; (C) SEM picture of AuSn stacks before bonding with spillage stopping structures around; (D) average thickness deviation of deposited eutectic stacks across the wafer; (E) adhesion problems on chromium resulting in lifting off eutectic structures after differential etching of seed and adhesion layers; (F) cracked, oxidized surface of gold-tin deposit after attempted bonding

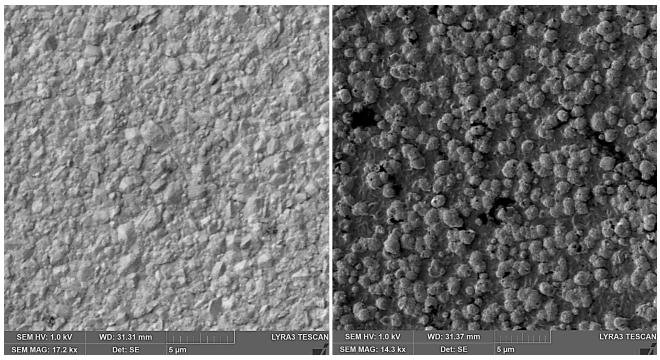

Fig. 4. SEM photographs of morphology of deposited layers left: gold layer, right: tin layer.

resists, such as dedicated AZ15nxt show significant impairment upon exposure to chemicals of varying temperature and acidity. The need of sequential patterning before each cycle can then compromise accuracy of seal geometry and prolongs overall fabrication time.

Gold and tin formed during sequential deposition differ significantly form each other from morphology perspective (see Fig. 4). Gold forms uniform layers the thickness of which can be well controlled, despite moderately large grain size. Tin creates non-continuous layers of large grains, hence when thin eutectic stacks are required, developed morphology makes it difficult to ensure thickness accuracy of deposited material with contact profilometry.

Chromium as an adhesion layer for gold, as well as for gold-tin layers, despite easy processing and availability of selective removal was found unfit for adhesion purposes as compared to other materials. We suggest to avoid using evaporated chromium for the eutectic bonding purposes, and instead use titanium, or titanium-tungsten layers, which despite being difficult to remove are known to provide good anchoring for gold.

Bonding, which was supposed to be the benchmark for successful sequential deposition of eutectic stack of right stoichiometric composition failed. This can be explained by the different character of the plating non-uniformities across wafer between tin and gold deposits. Where gold thickness was rather uniform in the middle regions of deposited substrates and differed in the areas close to the edge of wafers, tin thickness was varying randomly across wafer sublease of intense foaming of the bath. As a result, composition of deposited stacks was shifted towards high-temperature eutectic, thus hindering bonding possibility.

Additional factors compromising successful bonding is intermixing between gold and tin, which occurs already at room temperature. Especially for low-height stacks, it may effect in quicker consumption of excess tin and formation of high-temperature intermetallics, resulting in shifting composition towards higher-temperature, more brittle joints. Any additional process steps, especially involving elevated-temperatures processing, which occur after tin deposition should be kept to minimum to avoid premature interdiffusion and layer oxidation.

V. Conclusion

This study has demonstrated some of the key challenges in the use of sequential approach to electroplating for the deposition of AuSn eutectic stacks in form of frames. Unless thick-electroplated directly in the form of alloy or co-sputtered, gold-tin eutectic formed by two-stage sequential plating is found to be difficult to control. Different characteristics of solutions and need of changing plating tanks leads to layer non-uniformities and problems in subsequent bonding steps, especially for the stacks of lower height. As an alternative, solid-liquid interdiffusion bonding of gold and indium could be used, as it does not require as strict control over stack composition. Nonetheless, it remains promising technique for providing biocompatible, small footprint hermetic encapsulations for future implants.

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