

Low Power, Low Emission Open Loop Periodic and Chaotic Modulator Topologies

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Dedicated to all my teachers for enlightening my path.

गुरुर्ब्रह्मा गुरुर्विष्णुर्गुरुर्देवो महेश्वरः ।
गुरुरेव परं ब्रह्म तस्मै श्रीगुरवे नमः ॥१॥

Translation

Gurur-Brahmaa Gurur-Vissnnur-Gururdevo Maheshvarah |

Gurure[-I]va Param Brahma Tasmai Shrii-Gurave Namah ||1||

Meaning

1.1: The Guru is Brahma, the Guru is Vishnu, the Guru Deva is Maheswara
(Shiva),

1.2: The Guru is Verily the Para-Brahman (Supreme Brahman); Salutations to
that Guru.

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Abstract

Electromagnetic interference has become an important topic of research as more and more radios are getting integrated around us. One of the well-known techniques to lower the EMI from integrated circuits is to use spread spectrum techniques [1]. Traditionally, phase locked loops (PLL) have been utilized to generate SSC clocks. The PLL's consist of a high power voltage controlled oscillator. This is undesirable in scenarios wherein the low power operation is required such as medical implants. In addition, the PLL loop band width impacts the intentional jitter. The current work introduces a non-PLL (Phase Locked Loops) modulator to enable low power operation. A chaotic modulation profile has been proposed to efficiently spread the frequency spectrum. Since there is no feedback loop, the input deterministic jitter is passed to the output.

One of the proposed applications is biomedical telemetry. With the advent of more and more implantable and non-implantable devices for monitoring various physiological parameters, the operating frequency band will become more and more clouded. Hence, there is a need to lower the EM signature of the transmitter. In addition, the transmitters need to be able to shift the operating frequency as per the MAC protocols [2] [3] to be able to operate in a channel with least interference. Also, the transmitter needs to be low power to conserve power. The interference path from the transmitter lies within the body and outside the body. The in body path to the

adjacent transmitter depends upon the operating frequency and the distance from source [4]. The proposed architecture is able to integrate within DOSS (dynamic open spectrum sharing) protocol and is able to adjust the frequency of operation based on the communication from the MAC controller [5]. A system level model has been built to simulate an implanted transmitter and tested with a 10s sleep signal obtained through Physionet [6].

Another proposed application is generation of on die clocks. The ever increasing speed of clocks and higher data rates leads to increased radiated coupling. Traditionally PLL's have been utilized for generating the dithered clock on die [7]. Multi clock domains from the same PLL clock source [8] require different amount of spreading. The proposed frequency modulator could be used in such scenarios to allow the clock domains to be independently controlled from the source PLL.

The frequency modulator and a chaotic generator have been fabricated on AMS 6 metal layer $0.18\mu m$ technology. The frequency modulator was fabricated, characterized and measurements have been presented.

The current work achieves a low power through circuit techniques by proposing a non-PLL based topology thus excluding the use of high power consuming VCO. Low emission is achieved using a variety of modulation profiles (periodic and chaotic) for spreading the bandwidth of the modulated spectrum.

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Declaration

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Declaration of Originality

I declare that work carried out in the thesis is my own and that all else is appropriately referenced.

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List of Abbreviations

AC	Alternating current
AMS	Austria micro systems
ANSI	American national standards institute
AWMA	Alternative wireless medium access
BER	Bit error rate
CMOS	Complementary metal oxide semiconductor field effect transistor
dB	Decibel
DBS	Deep brain stimulation
DC	Direct current
DFS	Dynamic frequency selection
DLL	Delay locked loop
DOSS	Dynamic open spectrum sharing
EEC	European economic community
EMBC	Engineering in medicine and biology society
EMI	Electromagnetic interference
ERC	European research council

ETSI	European telecommunications standards institute
EU	European union
FCC	Federal communications commission
FDA	Food and drug administration
FM	Frequency modulation
FSK	Frequency shift keying
IEEE	Institution of electrical and electronics engineers
IPG	Implantable pulse generator
Loop BW	Loop bandwidth
MAC	Media access control
MBAN	Medical body area network
MedRadio	Medical device radio communication service
MHz	Mega hertz
MOST	Metal oxide semiconductor transistor
PCB	Printed circuit board
PI	Phase interpolator
PM	Phase modulation
PSD	Power spectral density

PTA	Packet traffic arbitration
RFI	Radio frequency interference
SBPLL	Self bias phase locked loop
SNR	Signal to noise ratio
SSC	Spread spectrum clocking
TPC	Transmission power control
TS	Time sharing
TX	Transmitter
WBAN	Wireless body area network
WMTS	Wireless medical telemetry services
WWAN	Wireless wide area network

List of Symbols

Symbol	Description
f_c	Base band frequency of the carrier
$x_c(t)$	Carrier Signal
π	Ratio of circumference of circle to diameter of circle
A_c	Amplitude of the carrier
$y(t)$	Modulated signal with a single tone
f_{Δ}	Frequency deviation due to modulation
$f(\tau)$	Instantaneous frequency of the modulated signal
$x_m(\tau)$	Modulation profile
A_m	Amplitude of modulating signal
f_m	Frequency of modulating signal
β	Modulation index for a single tone modulation
Δf	Peak frequency-deviation, the maximum deviation of the instantaneous frequency from the carrier frequency
J_n	Bessel function of the first kind
f_{m1}	Frequency of modulating signal 1

Symbol	Description
f_{m2}	Frequency of modulating signal 2
a	Amplitude of modulating signal with frequency f_{m1}
b	Amplitude of modulating signal with frequency f_{m2}
f_{i2}	Instantaneous frequency of modulating signal with two tones
f_{i2}	Instantaneous frequency of modulating signal with two tones
$x_{m3}(t)$	A third sinusoid modulating signal
ω_{m3}	Frequency (radians) of third modulating signal
f_{i3}	Instantaneous frequency of a modulated signal using a three tone modulating signal
$f_{\Delta 3}$	Desired maximum frequency deviation from the centre frequency of the modulated signal with triple tones
f_{m3}	Frequency (hertz) of third modulating signal
θ_{i3}	Phase of modulated signal modulated with a three tone modulating signal
β_3	Modulation index with respect to the third tone
$y_{3tone}(t)$	Modulated signal with three tones
$F_{y(3tone)}(t)$	Fourier transform of modulated signal with three tones
$y_{Ntone}(t)$	Modulated signal modulated with a three tone modulation profile
$F_{y(Ntone)}(t)$	Fourier transform of modulated signal modulated with a three tone modulation profile
β_N	Modulation index with respect to the third tone

Symbol	Description
$m_{overlap}$	Harmonic at which the spectrum of the modulated signal overlaps
f_o	Baseband frequency
B_m	Bandwidth of m^{th} harmonic
x_{n+1}	Next sampled value of the chaotic system implementing a tent map
x_n	Current value of the chaotic system implementing a tent map
θ_{output}	Output phase of charge pump phase locked loop
θ_{input}	Input (reference) phase of the charge pump phase locked loop
N	Phase locked loop divider ratio
i_{cp}	Charge pump current in the phase locked loop
r	Loop filter resistor in charge pump phase locked loop
C_1	Loop filter capacitance of charge pump PLL
K_{VCO}	Gain of voltage controlled oscillator in PLL
ζ	Damping ratio of charge pump PLL
ω_n	Loop bandwidth of the charge pump PLL
ω_{REF}	Input reference frequency to the charge pump PLL
$f_{VCO_{out}}$	Output frequency of the voltage controlled oscillator
$f_{VCO_{FR}}$	Free running oscillator frequency of the voltage controlled oscillator
$y_{VCO}(t)$	Output modulated signal of the voltage control oscillator
$\theta_{i_{VCO}}$	Instantaneous phase of the VCO
β_{VCO}	Modulation index of the VCO
f_{VCO_m}	Frequency of modulation signal to the VCO

Symbol	Description
$V_{ctrl_{VCO_{mod}}}$	Modified control voltage generated by the loop filter in figure 3.3
I_0	Current feeding through the resistor R_2 in modified filter depicted in 3.3
I_2	Modulation current added intentionally to generate a triangular profile as depicted in 3.3
I_Y	Current flowing though resistor R_3 as depicted in figure 3.4
I_4	Modulation current added intentionally to generate a triangular profile as depicted in 3.4
ω_{z1}	Frequency domain zero for the filter depicted in figure 3.3 (a)
ω_{z2}	Frequency domain zero for the filter depicted in figure 3.5
$V_{ctrl_{cc}}$	Control voltage generated by the modified phase locked loop proposed by [15] and depicted in figure 3.6
$I_{CP_{cc}}$	Charge pump current generated by charge pump 1 depicted in 3.6
R_{1Cc}	Loop filter resistance depicted in figure 3.6
C_{1cc}, C_{2cc}	Loop filter capacitance depicted in figure 3.6

Publications

- Ruchir Saraswat, Esther Rodriguez-Villegas, “A low emission, low power non-linear frequency modulation based transmitter for implanted devices” 35th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC), 2013, Pages 826 - 829
- Ruchir Saraswat, Esther Rodriguez-Villegas, “Chaotic inductively coupled non-PLL low emission transmitter for implanted devices” IEEE 5th Latin American Symposium on Circuits and Systems (LASCAS), 2014, Pages 1-4
- Ruchir Saraswat, Esther Rodriguez-Villegas, “Low power EMI mitigation strategies utilizing non-PLL based periodic and chaotic SSC profiles for implanted devices”, IEEE International Symposium on Medical Information and Communication Technology (ISMICT), 2014
- Saraswat, Ruchir ; Abbasi, Mohammad Usaid ; Rodriguez-Villegas, Esther, “Ultra-Low Power, Low Noise MAC Protocol Compliant Non-PLL based Wearable Transmitter for Dynamic Open Spectrum Sharing” IEEE Neural Engineering Research Conference (IEEE-NER), 2015
- Abbasi, Mohammad Usaid ; Raikos, George ; Saraswat, Ruchir ; Rodriguez-Villegas, Esther, “A high PSRR, ultra-low power 1.2V curvature corrected Bandgap reference for wearable EEG application”, IEEE New Circuits and Systems Conference (NEWCAS), 2015

- Ruchir Saraswat, Esther Rodriguez-Villegas, “Low Emission, Open Loop MAC Protocol Compliant Implantable FSK Modulator”, IEEE New Circuits and Systems Conference (NEWCAS), 2016

Invited Talk

- Organizer: Hermes Partnership in cooperation with The intervention Centre of Oslo University Hospital and COST Action IC0905 - TERRA

Sponsor : European Union Commission

Title of workshop: Workshop on Sensor Communications & Technologies, Body Area Networks, e-health Services and Standardization. Sponsor

URL for talk and slides: <http://www.hermes-europe.net/workshops/workshop-ismict-2014/>

Title of talk: Low Power EMI Mitigation Strategies for Implanted Devices.

1 Introduction

OVER the past few years, there has been a push to remotely monitor patients both for clinical and non-clinical purposes, e.g. cardiac patients [19], insulin pumps [20] and EEG based physiological monitoring systems [21]. Commercial acute or chronic patient monitoring solutions continue to be developed and are starting to be deployed commercially [22]. During the 90's, with the advent of mobile communication, medical devices, such as pacemakers, apnoea monitors, electrically powered wheelchairs [23], [24], [25], [26] were seen failing because of radio frequency interference [23]. Radio frequency interference (RFI) is the radiation or conduction of radio frequency energy at levels that interfere with the operation of adjacent equipment. The consequence of the failures ranged from inconvenience to serious injuries and even death.

There has been a significant rise in the use of electronically controlled medical devices outside the clinical environment. These devices are often used in homes, attached to patients, or implanted in their bodies [24]. To an ever increasing extent, wireless communications equipment (e.g. cellular phones) is likely to be used in close proximity to medical devices without the knowledge of the patient or attending medical personnel [27]. With an explosion of devices, both implantable and non-implantable, it is vital that mechanisms are developed for ensuring the correct functionality of the impacted devices in an increasingly noisy environment.

In past decades, interference to medical equipment has led to severe casualties including death [28]. In the mid-1980s, the US Food and Drug Administration (FDA) had become aware that approximately 60 infants died in the United States while being monitored for breathing cessation by one model of apnoea monitor. Subsequent tests showed that this particular monitor was extremely susceptible to low level RF fields [29], including those from mobile communication base stations several hundred meters away and FM radio broadcast stations more than one kilometre away. This resulted in voluntary recall of more than 16,000 apnoea monitors.

Problems were reported especially in implanted cardiac pacemakers and defibrillators due to RFI. Teams of engineers and cardiologists in several countries have independently studied these devices, either in patients or tissue simulating models, demonstrating that nearby digital cellular phones sometimes induce undesirable effects. The dominant effect observed has been loss of pacemaker adaptive control, causing the device to deliver stimuli either irregularly or at a pre-programmed fixed rate [30].

Warnings have been published concerning the use of wireless communications equipment in the clinical environment. Hospitals worldwide have recommended cellular phones should not be used in intensive care units, operating theatres, and patient rooms where critical care medical equipment is in use [31], [32]. Extensive measurements have been made to determine the field strengths produced by common RF sources in actual or simulated non-clinical environments to study the impact of electromagnetic interference (EMI) on critical medical devices [33].

Patric Blomsted et al. [34] did a study to evaluate the impact of electromagnetic environment on the implanted deep brain stimulator. A review of 172 patients for around 40 months found that the magnetic control circuit in the IPG (implantable pulse generator) was susceptible to inadvertent deactivation by other electromag-

netic forces. Since DBS patients gain increased mobility from the treatment and there are high chances that they will be surrounded by devices emitting electromagnetic radiation.

Stringent requirements have been put into place by various agencies, such as the American National Standard Institute (ANSI) [35], Federal Communications Commission (FCC) [36], European Telecommunications Standards Institute (ETSI) [37] et al. around the world to regulate the amount of EMI radiated by electronic devices. With more and more devices being implanted or worn, the devices need to lower the amount of EMI radiated and also have a mechanisms to be able to functionally operate within a clouded spectrum [38], [39]. There are several approaches that are being looked into by designers to contain the EMI radiated from their designs or allow the devices to work within a clouded spectrum [40], [41]. Some of these techniques are covered in next few sections.

1.1 Factors impacting occurrence of RFI

To address the challenges of RFI, the problem must be broken into manageable pieces. Figure 1.1 (a) shows the problem in simple interference and electromagnetic compatibility terms [42].

The sources depicted in the system in figure 1.1 (a) are the aggressors and its subsystems. There could be multiple sources impacting a single victim. The source could be a supply line transient caused by load switching, radios (something that transmits such as mobile phones), electro static discharge (ESD) et al. A simplified model to study the interference is depicted in figure 1.1 (b). As illustrated, the platform noise is added into the channel at a number of possible locations and can be considered as the summation of individual sources resulting in a complex signal.

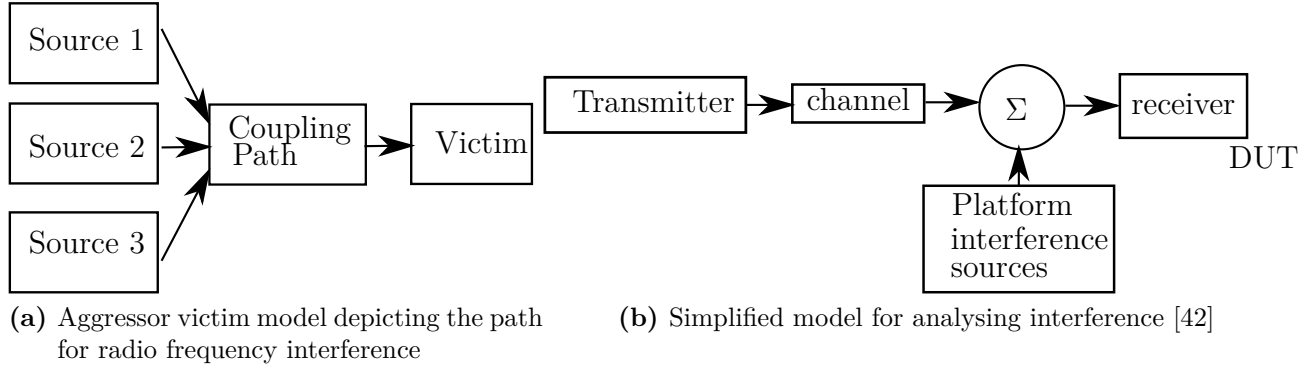


Figure 1.1: Aggressor victim interference model

The coupling path typically represents the loss path that reduces the amount of energy the victim radio will see. The coupling could either be the radiated (e.g. through the air) and/or conducted (e.g. shared power) paths. A time varying field generates a time varying magnetic field and vice-versa. Effects of coupling occur primarily when the susceptible device is in the near field of the source [43]. The ratio of E-field (electrical field) to H-field (magnetic field) in the coupling path determines the nature of coupling. If the ratio is greater than 377Ω , the source can be treated as a E-field generator. Capacitive coupling occurs in a region near the source where the electric field is dominant (e.g. the tip of a dipole antenna). In contrast, if the ratio is smaller than 377Ω , the source can be treated as a H-field generator. An example is loop antenna such as formed by a current loop. Interference in such a case would be by H field coupling (magnetic), which is basically inductive coupling. Locating the antenna away from the noisy electronics or shielding the noisy electronics will increase the loss path, thereby reducing the level of noise seen by the radio.

The victim is the wireless radio, including both the antenna subsystem and RF components.

Figure 1.2 depicts an example of an interference noise lying within a radio's operating band. In this case, a 133.33 MHz noise source and its harmonics are depicted. As can be seen, the 7th harmonic sits in the 925-960 MHz WWAN band. Thus,

in such a configuration, there is a possibility that the noise at the 933 MHz may interfere with the radio operating in the same range.

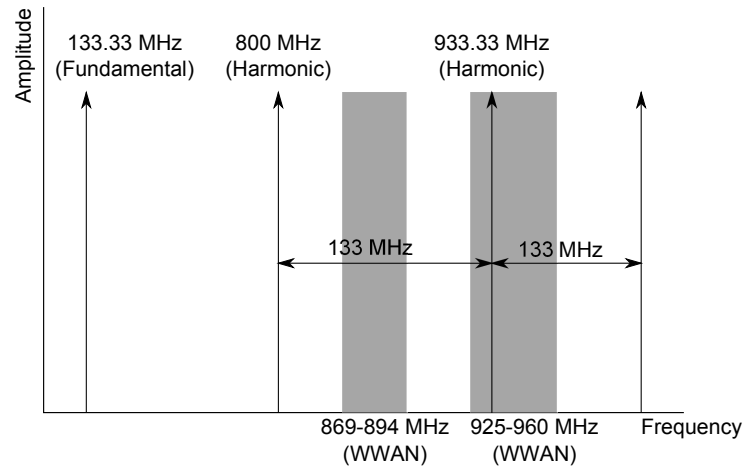


Figure 1.2: Interfering channel and DUT power spectrum

One possible solution to the problem at hand would be to move the operating band of interest out of the interfering noise harmonic, e.g. through MAC (media access protocol) algorithms [5]. A brief discussion of MAC protocols is included later in the chapter.

1.2 Regulatory and Compliance Standards

1.2.1 Operating Standards for Medical Devices

Medical electronic devices can be classified into various categories depending on the frequency range and standards they use [44]:

- Inductive implants: Inductive implantable medical devices have been used to control or monitor cardio activity. Most devices operate in the bands below 200 kHz and communicate at distances of less than one foot from the patient's body [45].

- Medical device radio communications service (MedRadio) [46]: The Medical Device Radio communications Service (MedRadio) is split into different bands, namely, 401–401.85 MHz, 401.85–402 MHz, 402–405 MHz, 405–406 MHz, 413–457 MHz. MedRadio spectrum is used for diagnostic and therapeutic purposes in implanted medical devices as well as devices worn on a body. For example, MedRadio devices include implanted cardiac pacemakers and defibrillators as well as neuro-muscular stimulator that help restore sensation, mobility, and other functions to limbs and organs. In May 2012, the Commission modified the MedRadio rules to enable the deployment of Medical Body Area Network (MBAN) devices in the 2360–2400 MHz band. A MBAN is a low power network of sensors worn on the body controlled by a hub device that is located either on the body or in close proximity to it.
- Wireless medical telemetry services (WMTS) [47]: This service is for the remote monitoring of a patient’s health where the RF communication occurs between a patient worn transmitter and a central nursing station. WMTS devices are pre-programmed to transmit at periodic intervals with short transmission duration and a long waiting period. This leads to low power consumption and less probability of interference occurring to receivers in other services. FCC allocated interference-protected spectrum for the use by licensed physicians, healthcare facilities and certain trained and supervised technicians. The frequencies currently allocated for WMTS are divided into three blocks:
 - 608 – 614 MHz: This spectrum band corresponds to television channel 37, but it is not used by any TV station because it is used for radio astronomy.
 - 1395 – 1400 MHz.
 - 1427 – 1432 MHz: The channels in this spectrum band are shared by

WMTS devices and non-WMTS devices such as utility telemetry devices. Generally, WMTS operations are accorded primary status over non-medical telemetry operations in the 1427-1429.5 MHz band, but are treated as secondary to non-medical telemetry operations in the 1429.5-1432 MHz band.

- Wi-Fi, Bluetooth and Zigbee: These unlicensed technologies are commonly used with cell phones, hand held devices and personal computers, but can also be used for implanted or body-worn medical devices. These devices operate in the 902-928, 2400-2483.5 and 5725-5850 MHz bands at distances up to a few hundred feet.

1.2.2 EMC Regulatory Standards

There are a number of regulatory bodies dealing with EMI [48]. Most of the regulations are based on preventing the specific problems in a given environment. Furthermore the nature of the rules and regulations vary in different parts of the world according to local requirements [49].

The general electromagnetic compliance (EMC) requirements in the US are set by the Federal Communications Commission (FCC), while the Food and Drug Administration (FDA) regulates medical products [36]. The FCC has different sets of regulations for different types of digital devices. Devices that are marketed for use in commercial, industrial or business environments are classified as Class A digital devices. Devices that are marketed for use in residential environments, notwithstanding their use in commercial, industrial, or business environments are classified as Class B digital devices. In general, the regulations for Class B devices are more stringent than those for Class A devices. This is because in general digital devices

are in closer proximity in residential environments, and the owners of the devices are less likely to have the abilities and or resources to correct potential problems.

The European EMC Directive, 89/336/EEC [50], sets out the legal requirements on EMC for all electronic devices operating within the European Economic Zone. While the focus for the commercial EMI regulation in the US is on emissions, in Europe these include both emissions and immunity.

Table 1.1 lists the voltage levels allowed under FCC Rules and Regulations, Part 15, for both Class A and Class B within 10 meter (Class A) and 3 meter (Class B) [51], [52].

Table 1.1: FCC Class A and Class B Limits

	Class “A” (10 meters)	Class “B” (3 meters)
Frequency of emission (MHz)	Field Strength	Field Strength
	$\frac{\mu V}{m} dB$	$\frac{\mu V}{m} dB$
30-88	90 49.5	100 40
88-216	150 54	150 43.5
216-960	210 56.5	200 46
>960	300 60	500 54

If the equipment under test exceeds these limits, as measured by a calibrated receiver in a special chamber, the excess energy must be reduced to within agency limits before the equipment can pass agency regulations.

1.3 Mitigating Radio Frequency Interference

Standard RF immunization techniques include the use of shielding, grounding, and filtering as illustrated in figure 1.3.

Shielding includes enclosing the device in a metal box or in a plastic box coated with metallic paint. Use of RF shielded cables is a standard practice in commercial

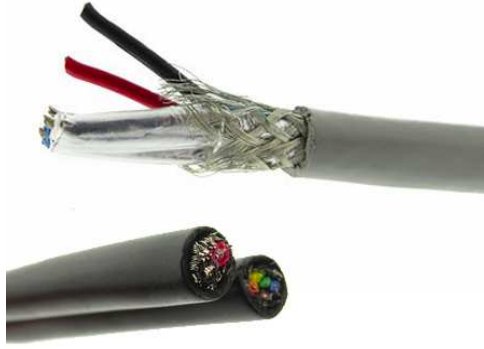


Figure 1.3: Traditional Methods of protecting against EMI. Redrawn from [9]

audio and video devices. Grounding of electronic circuitry and cable shields is an expensive but necessary step toward ensuring RFI immunity. RF filtering of signal carrying conductors, especially in sensitive patient monitoring equipment, should be performed carefully. The potential for the success of these techniques has been demonstrated in implanted cardiac pacemakers, which commonly achieve immunity of up to 200 V/m even though these devices monitor weak electro-physiological voltages [53].

Another method to deal with interference is to use a frequency selective filter as illustrated in figure 1.4. The selection and the type of filter depends on the design case. A low pass filter is preferable if the frequency of the interfering signal is higher than the desired band, and a high pass filter if the frequency of the interfering signal is lower. For cases, where there is a maze of frequencies, a band pass filter is preferable. Examples of two basic filter tanks are a parallel tank and a series tank as shown in figure 1.4 (b) and figure 1.4 (c) respectively. Stevenson et al. [54] have used capacitive feed through RF filters for reducing interference in case of cardiac pacemakers.

It has been shown that different wireless telemetry technologies impact the medical equipment differently [55]. The establishment of wireless techniques into medical or

healthcare environment depends on the wireless frequency band, the wireless transmitter output power, the distance between wireless devices and medical equipment, and the surrounding environment of the hospital. The selected technology needs to be chosen such that the data can be transmitted reliability with least amount of low data loss rate, be immune to the disturbance by other wireless devices, be secure, easy to be reconfigured and be cost effective.

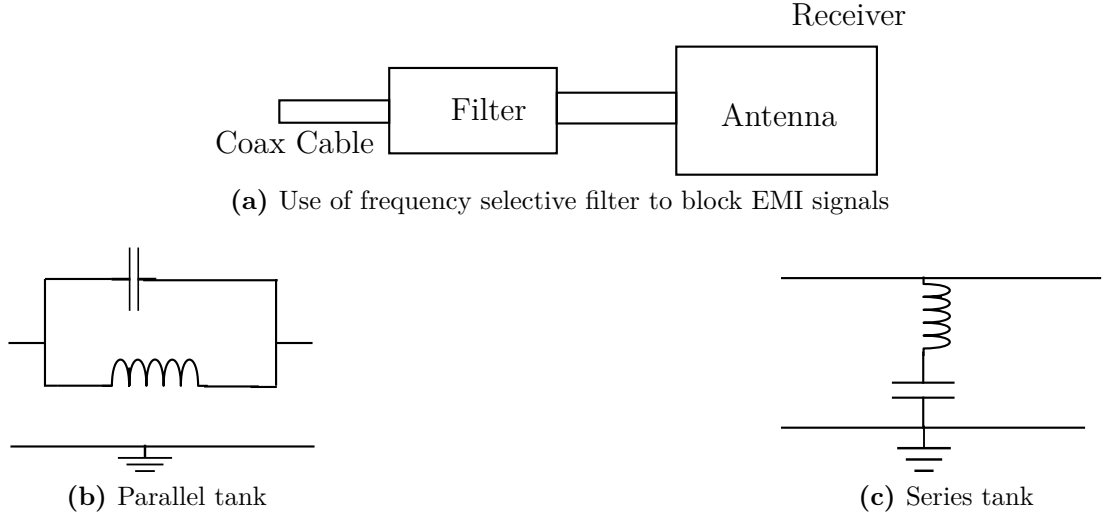


Figure 1.4: Frequency selective filter to block EMI signals

In an event of an interference, designers can add interference recognition and fail-safe circuitry to their medical devices. For example, many cardiac pacemakers are protected from erratic operation by being programmed to revert to a fixed rate when RFI is detected.

The various techniques discussed are based on filtering out noise creeping into the receiver. With the advent of more and more sensors for monitoring bodily physiological parameters, protocols such as Wireless Body Area Network (WBAN) have been proposed [2]. A WBAN consists of in-body and on-body nodes that continuously monitor patient's vital information for diagnosis and assessment of diseases. Some on-body nodes can also be used for multimedia and gaming applications. A WBAN

uses Wireless Medical Telemetry Services (WMTS), unlicensed Industrial, Scientific, and Medical (ISM), Ultra-wideband (UWB), and Medical Implant Communications Service (MICS) bands for data transmission. The brain of the WBAN infrastructure is the coordinator. With more and more sensor devices being integrated within the WBANs, there is a need for the sensors to choose the frequency channel with least interference. This poses a challenge for the coordinator to efficiently allocate spectrum to various devices for optimal band utilization [38]. In addition, various sensors that collect the information need to utilize the spectrum efficiently while communicating to the central WBAN co-coordinator so as to reduce power dissipation due to collision of packets, overheating of nodes, idle listening and control packet overhead.

One of the proposed protocols to effectively utilize the available spectrum is Media Access Protocol (MAC) [5]. A MAC approach is reactive, and provides protection only when it is necessary. The most common methods in this category are dynamic frequency selection (DFS), transmission power control (TPC) [56], and time sharing (TS). The basic idea is to detect and then avoid interferences by adjusting frequency, transmit power [57], [58] or timing. DFS allows a radio to dynamically select a channel with the least interference. TPC forces a radio to operate at its lowest transmit power subject to link budget measurement or calculation. As a result, when a client is closer to access point or base station, it will transmit less power, and cause less interference to other coexisting radios. Moreover, a receiver that is suffering from coexistence interference can notify its peer transmitter to increase transmit power. But TPC cannot help if client is at cell edge or transmit power is already at its maximum. TS (time sharing) is also used by the industry to support coexistence, particularly for Bluetooth and Wi-Fi. The basic idea is to schedule multiple radios in time domain so that they do not overlap with each other, e.g.

alternative wireless medium access (AWMA) and packet traffic arbitration (PTA).

One example of a DFS scheme is dynamic open spectrum sharing (DOSS) protocol [3]. The principle of dynamic open spectrum sharing (DOSS) has been depicted in figure 1.5.

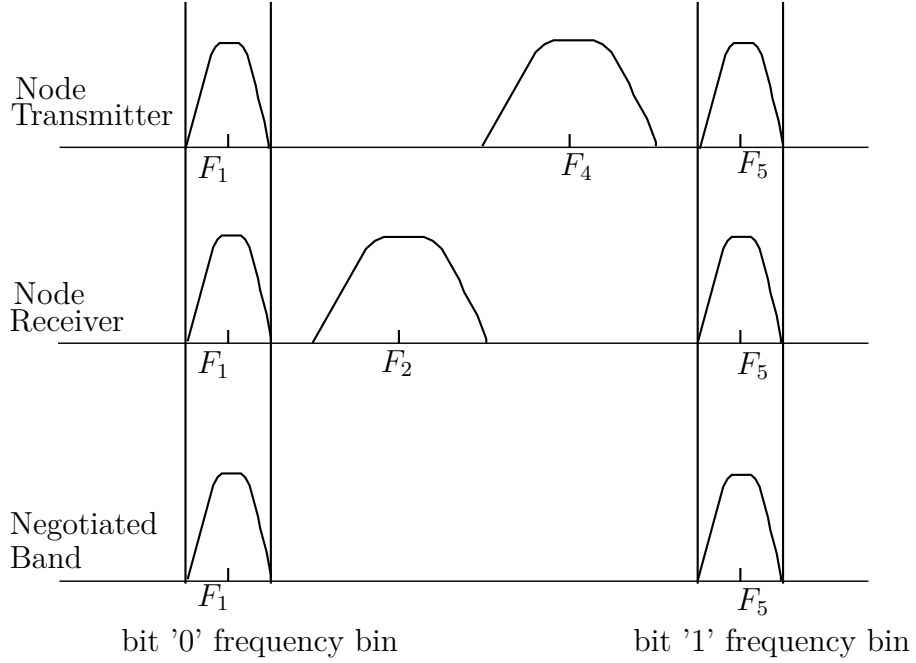


Figure 1.5: Spectrum Negotiation is Dynamic Open Spectrum Sharing Protocol [3]

$Node_{Transmitter}$ (transmitter) has F_1 , F_4 and F_5 as the available frequency bands while $Node_{Receiver}$ (receiver) has F_1 , F_2 and F_5 frequency bands available. The MAC coordinator recognizes that there two available shared bands and sends a negotiated signal to align the transmitter and receiver band of operation allowing the transmitter and the receiver to work in the band of least interference.

1.4 Concluding Remarks

The current chapter has made an attempt to give a brief overview of the various aspects of RFI in medical devices. The focus of the discussion was to provide an

overview of the methods for mitigating RFI through various means. It is important to be aligned to various regulations and emit as little radiation from a device as possible. A desirable solution for an implantable transmitter would be to lower the amount of radiations and also have the capability to alter its band of operation to be compatible with various MAC protocols. The current work proposes a frequency shift keying (FSK) [59] modulator capable of adjusting the carrier frequency of the transmit bit's (EEG Signals) dynamically.

1.5 Thesis Structure

This thesis is structured as follows:

Chapter 2

The theory behind the spread spectrum modulation technique is discussed in this chapter. The chapter explores the impact of adding various tones to the modulation profile modulating the incoming clock signal. It has been shown that as the number of tones are added, the peak in the output spectrum of the modulated clock comes down. The work has been proven both analytically and numerically with MATLAB simulations. The chapter introduces the concept of chaos briefly and the idea behind chaotic modulation is explored. Specific contributions are listed below

1. Previous work reported the impact of a single and a double tone modulation profile on the spectra of modulated signal. The current thesis has extended the study to three tones, N-tones modulation profiles both analytically and through MATLAB simulations.
2. Extensive papers have been published detailing techniques of generated spread spectrum clocks (SSC) signals using periodic modulation profiles. The chapter

proposes exploiting chaotic systems towards achieving a further improvement in the spectrum of the modulated signals.

Chapter 3

A literature survey of published techniques for generating spread spectrum clocks is discussed. SSC generators can be broadly classified into phase locked loop (PLL) based systems and all digital (non-PLL) systems. Approaches for both types have been discussed. A self-bias PLL in a 65nm process was simulated to study the impact of the loop bandwidth on the type of modulation and the results were discussed. A non-PLL open loop architecture for generating a modulated clock using a delay locked loop and a phase interpolator is described using verilogA modelling techniques. Specific contributions are listed below

1. The interaction between the loop bandwidth of a self-bias PLL (SBPLL) and a modulating signal has been discussed.
2. An open loop non-PLL architecture is explored using a delay locked loop (DLL) and a phase interpolator (PI).

Chapter 4

Chapter 4 proposes an open loop frequency modulator capable of handling both periodic and chaotic modulation profiles. The transmitter path from the implanted sensor until the coiled inductor was been modelled in verilogA and simulations were carried out to validate the proposal. An open loop frequency modulator and a tent map based chaotic generator are designed and discussed. All the simulations were done on an extracted netlists in a $0.18\mu m$ technology. Specific contributions were:

1. A transmission link is proposed and modelled in verilogA to test the proposal.

2. A tent map chaos generator was implemented and fabricated.
3. An open loop frequency modulator was proposed, simulated and fabricated.
4. The chaotic map generator signal was fed to the frequency modulator and a reduction in the peak of the output spectrum was shown.

Chapter 5

The proposed design was fabricated in a $0.18\mu m$ IBM technology through Europractice. A two layer printed circuit board (PCB) was designed using Altium designer. Detailed measurements were carried out to characterize the circuit and measured results discussed.

Chapter 6

Chapter 6 summarizes the main contributions of the research, detailing the publications which have arisen from this work. Some specific conclusions are drawn and intended future research directions are explored.

2 Spread Spectrum Clocking Schemes

SPREAD spectrum clock generation is analogous to spread spectrum techniques used in communications in the sense that the energy of the intended signal is spread over a wider bandwidth [60]. The spreading of the energy is accomplished by frequency modulating (FM) the clock signal with a unique waveform. A spread spectrum clock (SSC) is a special type of digital clock that provides lower EMI output clocks when compared with conventional clock generator outputs [61]. In figure 2.1 (a) the spectrum of an unmodulated clock is compared with the spectrum of a modulated clock 2.1 (b). Both clocks feature the same amount of energy but as the spectrum of the modulated clock is widened its energy is spread over a bigger frequency band leading to a lower amplitude of the spectrum.

Modern day compute platforms utilize SSC clocking extensively for lowering the EMI radiations [62], [63]. The present chapter details the mathematics behind the spread spectrum signalling. The work has been drawn mainly drawn from Schwartz et al.[10], Peterson et al.[64] and Proakis et al.[65]. However, the concept has been extended to study the impact of adding multiple tones into the modulating signal. The chapter concludes by introducing chaotic modulation as a better contender for efficient spreading power in the modulated signal.

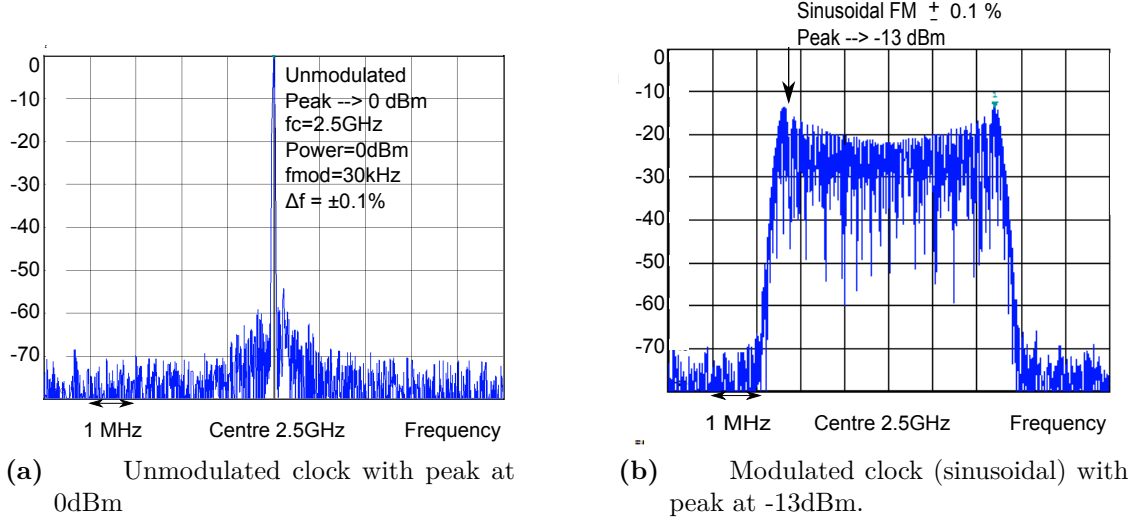


Figure 2.1: PSD of unmodulated and modulated clock with centre frequency: 2.5GHz , modulation frequency: 30kHz , peak frequency deviation: $\pm 0.1\%$, resolution bandwidth: 30kHz

2.1 Single Tone Modulation Profile

Spreading of the spectrum is achieved by frequency modulating the carrier signal.

A sinusoidal carrier $x_c(t)$ can be represented as [66]:

$$x_c(t) = A_c \cos(2\pi f_c(t)) \quad (2.1)$$

where A_c is the amplitude of the carrier and f_c is the base band frequency of the carrier. The instantaneous frequency of the modulated clock can be expressed as:

$$f(t) = f_c + f_\Delta x_m(t) \quad (2.2)$$

where f_Δ is frequency deviation and $x_m(t)$ is the modulating signal.

The combined modulated signal is then given by [66]:

$$y(t) = A_c \cos \left(2\pi \int_0^t f(\tau) d\tau \right) \quad (2.3)$$

Substituting equation 2.2 in equation 2.3:

$$y(t) = A_c \cos \left(2\pi \int_0^t [f_c + f_\Delta x_m(t)] dt \right) \quad (2.4)$$

$$y(t) = A_c \cos \left(2\pi f_c t + 2\pi f_\Delta \int_0^t x_m(t) dt \right) \quad (2.5)$$

Letting the modulating signal to be sinusoidal and comprising of a single tone:

$$x_m(t) = A_m \cos(2\pi f_m t) \quad (2.6)$$

The phase variation of the modulated signal is given by:

$$\int_0^t x_m(\tau) d\tau = \frac{A_m \sin(2\pi f_m t)}{2\pi f_m} \quad (2.7)$$

Substituting equation 2.7 in equation 2.5, the modulated signal is given by:

$$y(t) = A_c \cos \left(2\pi f_c t + \frac{f_\Delta}{f_m} \sin(2\pi f_m t) \right) \quad (2.8)$$

where the amplitude A_m of the modulating sinusoidal is represented by the peak deviation f_Δ . β is called the modulation index defined as the ratio of the frequency

deviation to unmodulated level, given as [66]:

$$\beta = \frac{\Delta f}{f_m} = \frac{f_{\Delta} A_m}{f_m} \quad (2.9)$$

where f_m is the highest frequency component present in the modulating signal and Δf is the peak frequency-deviation i.e. the maximum deviation of the instantaneous frequency from the carrier frequency. Thus, equation 2.8 can be written as:

$$y(t) = A_c \cos(2\pi f_c t + \beta \sin(2\pi f_m t)) \quad (2.10)$$

Frequency modulation can be divided into narrow band modulation and wide band modulation. Small β corresponds to narrow bandwidths, and FM systems with $\beta \ll \pi/2$ are called narrow band systems. For the cases where $\beta > \pi/2$ the modulation is called a wide band modulation [10]. The current analysis has been done for wide band FM.

Utilizing the trigonometric identity [67]:

$$\cos(u \pm v) = \cos(u)\cos(v) \mp \sin(u)\sin(v) \quad (2.11)$$

Equation 2.10 can be expanded to:

$$y(t) = A_c (\cos(\omega_c t) \cos(\beta \sin \omega_m t) - \sin(\omega_c t) \sin(\beta \sin \omega_m t)) \quad (2.12)$$

where $\omega_c = 2\pi f_c$, $\omega_m = 2\pi f_m$. From Maclaurin series [67] series:

$$\cos(x) = \sum_{l=0}^{\infty} \frac{(-1)^l x^{2l}}{2l!} = 1 - \frac{x^2}{2!} + \frac{x^4}{4!} - \dots \quad (2.13)$$

Thus:

$$\cos(\beta \sin(\omega_m t)) = 1 - \frac{\beta^2}{2} \sin^2 \omega_m t + \frac{\beta^4}{24} \sin^4 \omega_m t - \dots \quad (2.14)$$

Considering $\beta^2 \ll 6$ only the first two terms of the expansion are retained [10]. Again from Maclaurin series [67] expanding $\sin(\beta \sin(\omega_m t))$:

$$\sin(\beta \sin(\omega_m t)) = \beta \sin(\omega_m t) - \frac{\beta^3}{6} \sin^3(\omega_m t) \quad (2.15)$$

Here again, if $\beta^2 \ll 6$ only the first term is significant. Substituting equation 2.14 and equation 2.15 in equation 2.12 for the case where $\beta^2 \ll 6$, the modulated carrier can be expressed as:

$$y(t) = (1 - \frac{\beta^2}{4}) A_c \cos(\omega_c t) - \frac{\beta}{2} A_c [\cos(\omega_m - \omega_c) t - \cos(\omega_m + \omega_c) t] + \frac{\beta^2}{8} A_c [\cos(\omega_c + 2\omega_m) t + \cos(\omega_c - 2\omega_m) t] \quad (2.16)$$

The following observations can be made from equation 2.16

- The first term is the carrier term. As the modulation index increases the amplitude of the carrier term decreases.
- The first order side bands increase with β .
- A new set of sidebands appear at $\omega_c \pm \omega_m$. The appearance of new sidebands with increasing modulation index corresponds to the widening of the spectrum. For a fixed modulating frequency, the modulation index (β) is proportional to the amplitude of the modulating signal, so that increases in the signal amplitude generates new sidebands.

Since the average power in the modulated wave is independent of the frequency of the modulating wave, increasing power in the sideband frequencies corresponds to a

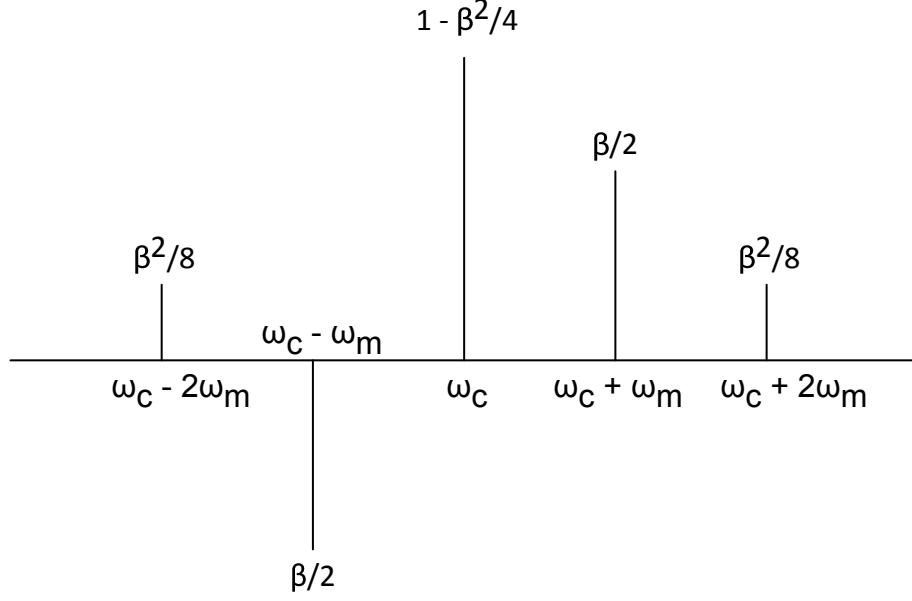


Figure 2.2: Effect of increasing β on FM spectrum ($\beta^2 \ll 6$) of sine-wave modulation [10].

decrease in the power associated with the carrier. This is accounted for the decrease in carrier amplitude as noted above. As β increases further, more terms from the power-series (Maclaurin series) expansion are required for both $\cos(\beta \sin(\omega_{mod})t)$ and $\sin(\beta \sin(\omega_{mod})t)$. Correspondingly, sideband components increase and the bandwidth begins to increase with β or with the increase in the amplitude of the original modulating signal. The effect of increasing β on the spectrum of the modulated clock has been depicted in figure 2.2.

For the case of a carrier modulated by a single sine wave, the resulting frequency spectrum can be calculated using Bessel functions of the first kind, as a function of the sideband number and the modulation index.

For a periodic complex exponential given as [10]:

$$v(t) = e^{j\beta \sin(\omega_m t)} \quad -\frac{T}{2} < t < \frac{T}{2} \quad (2.17)$$

the spectrum of equation 2.17 can be given as [10]:

$$e^{j\beta \sin \omega_m t} = \sum_{n=-\infty}^{\infty} J_n(\beta) e^{jn\omega_m t} \quad (2.18)$$

where $J_n(\beta)$ is the Bessel function of the first kind. Multiplying equation 2.18 with $e^{j\omega_c t}$ and taking the real part:

$$\text{Re} \left(e^{j\beta \sin \omega_m t} e^{j\omega_c t} \right) = \cos(\omega_c t + \beta \sin \omega_m t) \quad (2.19)$$

Referring to equation 2.10, the modulated clock can be written as:

$$y(t) = \text{Re} \left(\tilde{f}(t) e^{(j\omega_c t)} \right) \quad (2.20)$$

where $\tilde{f}(t)$ is given by:

$$\tilde{f}(t) = \sum_{n=-\infty}^{\infty} \left(J_n(\beta) e^{jn\omega_m t} \right) \quad (2.21)$$

Thus, by using:

$$y(t) = \sum_{n=-\infty}^{\infty} \text{Re} \left[J_n(\beta) e^{jn\omega_m t} e^{j\omega_c t} \right] \quad (2.22)$$

$$y(t) = \sum_{n=-\infty}^{\infty} [J_n(\beta) \cos(2\pi(f_c + nf_m)t)] \quad (2.23)$$

Fourier Transform of $\cos(2\pi k_0 x)$ is given by [68]

$$\mathcal{F}[\cos(2\pi k_0 x)] = \frac{1}{2} [\delta(k - k_0) + \delta(k + k_0)] \quad (2.24)$$

Thus, the Fourier transform of 2.23 given as

$$\mathcal{F}[y(t)] = \frac{1}{2} \sum_{n=-\infty}^{\infty} J_n(\beta) [\delta(f - f_c - n f_{mod}) + \delta(f + f_c + n f_m)] \quad (2.25)$$

As expected it can be seen that additional harmonics have been added into the spectrum.

2.2 Multi Tone Modulation Signals

Kim et al. [68] explored and suggested a two tone modulation approach for modifying the voltage controlled oscillator (VCO) of a charge pump phase locked loop (PLL) to further lower the peak in the frequency spectrum with respect to a single tone modulation. Considering the modulation wave to be composed of two sinusoidal modulating signals with frequencies f_{m1} and f_{m2} and amplitude a and b , the modulating wave can be written as:

$$x_{m2}(t) = a \cos(2\pi f_{m1}t) + b \cos(2\pi f_{m2}t) \quad (2.26)$$

The instantaneous frequency is thus given by:

$$f_{i2} = f_c + f_{\Delta 2} (a \cos(2\pi f_{m1}t) + b \cos(2\pi f_{m2}t)) \quad (2.27)$$

where $f_{\Delta 2}$ is the desired maximum frequency deviation from the centre frequency.

The phase of the modulated signal is represented by integrating f_{i2} :

$$\theta_{i2} = \int 2\pi f_{i2} dt = 2\pi f_c t + \beta_1 \sin(2\pi f_{m1}t) + \beta_2 \sin(2\pi f_{m2}t) \quad (2.28)$$

where $\beta_1 = \frac{f_{\Delta 2}}{f_{m1}}$ and $\beta_2 = \frac{f_{\Delta 2}}{f_{m2}}$. The modulated carrier is then given by:

$$y_{2tone}(t) = \cos(\omega_c t + \beta_1 \sin(\omega_{m1} t) + \beta_2 \sin(\omega_{m2} t)) \quad (2.29)$$

where $\omega_c = 2\pi f_c$, $\omega_{m1} = 2\pi f_{m1}$ and $\omega_{m2} = 2\pi f_{m2}$.

Similar to equation 2.23, the modulated wave is given as:

$$y_{2tone}(t) = \text{Re}(\tilde{f}_{2tone}(t) \exp(j\omega_c t)) \quad (2.30)$$

where

$$\tilde{f}_{2tone}(t) = \sum_{n=-\infty}^{\infty} J_n(\beta_1) e^{jn\omega_{m1} t} \sum_{m=-\infty}^{\infty} J_m(\beta_2) e^{jm\omega_{m2} t} \quad (2.31)$$

Thus, the modulated signal is given as [68]

$$y_{2tone}(t) = \sum_{n=-\infty}^{\infty} \sum_{m=-\infty}^{\infty} \text{Re}[J_n(\beta_1) J_m(\beta_2) e^{jn\omega_{m1} t} e^{jm\omega_{m2} t} e^{j\omega_c t}] \quad (2.32)$$

$$y_{2tone}(t) = \sum_{n=-\infty}^{\infty} \sum_{m=-\infty}^{\infty} J_n(\beta_1) J_m(\beta_2) \cos(2\pi(f_c + nf_{m1} + mf_{m2})t) \quad (2.33)$$

The Fourier transform of 2.33 is given by [68]

$$F_{2tone}(f) = \frac{1}{2} \sum_{n=-\infty}^{\infty} \sum_{m=-\infty}^{\infty} J_n(\beta_1) J_m(\beta_2) [\delta(f - f_c - nf_{m1} - mf_{m2}) + \delta(f + f_c + nf_{m1} + mf_{m2})] \quad (2.34)$$

Comparing equation 2.25 to equation 2.34 it is observe that more harmonics have been created. According to the combination of n and m, the place that power

spectrum appears is determined. Due to the additional harmonics the difference between the trough and the peaks in the spectrum of the modulated clock gets reduced further.

The same analysis is now extended to a three tone modulation profile. Adding another tone to the modulation profile, the modulation wave is now composed of three sinusoidal modulating signals with frequencies f_{m1} , f_{m2} , f_{m3} and amplitude a, b, c. The modulating wave can now be written as:

$$x_{m3}(t) = a\cos(\omega_{m1}t) + b\cos(\omega_{m2}t) + c\cos(\omega_{m3}t) \quad (2.35)$$

The instantaneous frequency is thus given as:

$$f_{i3} = f_c + f_{\Delta 3} (a\cos(2\pi f_{m1}t) + b\cos(2\pi f_{m2}t) + c\cos(2\pi f_{m3}t)) \quad (2.36)$$

where $f_{\Delta 3}$ is the desired maximum frequency deviation from the centre frequency.

The phase of the modulated signal is represented by integrating f_{i3}

$$\theta_{i3} = \int 2\pi f_{i3} dt = 2\pi f_c t + \beta_1 \sin(2\pi f_{m1}t) + \beta_2 \sin(2\pi f_{m2}t) + \beta_3 \sin(2\pi f_{m3}t) \quad (2.37)$$

where $\beta_1 = \frac{f_{\Delta 1}}{f_{m1}}$, $\beta_2 = \frac{f_{\Delta 2}}{f_{m2}}$, $\beta_3 = \frac{f_{\Delta 3}}{f_{m3}}$

The modulated carrier is then given as:

$$y_{3tone}(t) = \cos(\omega_c t + \beta_1 \sin(\omega_{m1}t) + \beta_2 \sin(\omega_{m2}t) + \beta_3 \sin(\omega_{m3}t)) \quad (2.38)$$

where $\omega_c = 2\pi f_c$, $\omega_{m1} = 2\pi f_{m1}$, $\omega_{m2} = 2\pi f_{m2}$, $\omega_{m3} = 2\pi f_{m3}$.

Referring to equation 2.32, the modulated signal can be written as

$$y_{3tone}(t) = \sum_{n=-\infty}^{\infty} \sum_{m=-\infty}^{\infty} \sum_{o=-\infty}^{\infty} J_n(\beta_1) J_m(\beta_2) J_o(\beta_3) \cos(2\pi(f_c + nf_{m1} + mf_{m2} + of_{m3})) \quad (2.39)$$

The Fourier transform of equation 2.39 is given by [68]:

$$\begin{aligned} \mathcal{F}_{y(3tone)}(t) = \frac{1}{2} \sum_{n=-\infty}^{\infty} \sum_{m=-\infty}^{\infty} \sum_{o=-\infty}^{\infty} J_n(\beta_1) J_m(\beta_2) J_o(\beta_3) [\delta(f - f_c - nf_{m1} \\ - mf_{m2} - of_{m3}) + \delta(f + f_c + nf_{m1} + mf_{m2} + of_{m3})] \end{aligned} \quad (2.40)$$

Comparing equation 2.34 to equation 2.40, another harmonic has been created leading to a further reduction in peak power spectrum.

It can be inferred that as the number of tones increase in the modulating signal more harmonics would be added to the output spectra. For a N tone modulation signal (similar to three tone and two tone derivation) the modulated signal can be written as:

$$y_{Ntone}(t) = \cos(\omega_c t + \beta_1 \sin \omega_{m1} t + \beta_2 \sin \omega_{m2} t + \beta_3 \sin \omega_{m3} t + \dots + \beta_N \sin \omega_{mN} t) \quad (2.41)$$

The Fourier transform of equation 2.41 can be derived as:

$$\begin{aligned} \mathcal{F}_{y(Ntone)}(t) = \frac{1}{2} \sum_{n=-\infty}^{\infty} \sum_{m=-\infty}^{\infty} \sum_{o=-\infty}^{\infty} \dots \sum_{z=-\infty}^{\infty} J_n(\beta_1) J_m(\beta_2) J_o(\beta_3) \dots J_z(\beta_N) \\ [\delta(f - f_c - nf_{m1} - mf_{m2} - of_{m3} - \dots - zf_{mN}) + \delta(f - f_c \\ + nf_{m1} + mf_{m2} + of_{m3} + \dots + zf_{mN})] \end{aligned} \quad (2.42)$$

An increase in number of tones leads to a spreading bandwidth which brings down

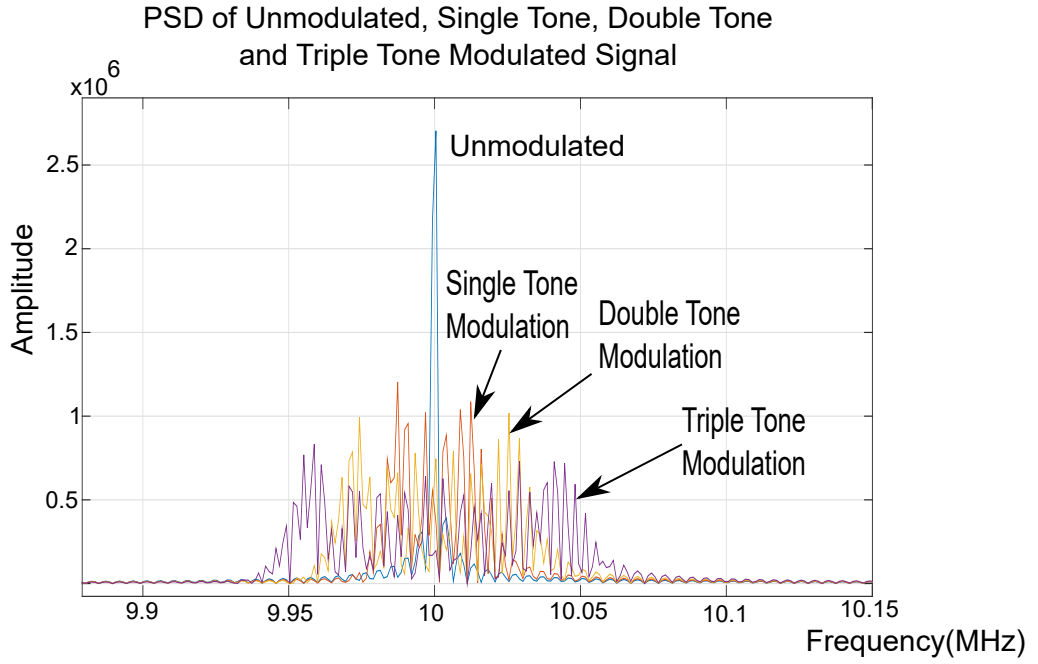


Figure 2.3: PSD for a single tone, double tone and triple tone modulated signal. Carrier frequency: 100MHz, Modulation Frequency: 32 kHz; Modulation Index: 5

the peak energy of the spectrum. Thus the higher the number of tones, the better will be the spread of the spectrum. However, the reduction in the peak power may not be of gain as the circuit becomes very big and complex leading to higher power et al. Matlab simulations were carried out to study the impact of increasing the number of tones in the modulating signal on the spectrum of the modulated clock. It can be seen in figure 2.3 that as the number of tones are increased in the modulating signal, the peak of the frequency spectrum gets lowered.

A white noise is composed of an infinite number of sinusoidal tones. Thus, it should be possible to get a very optimal spectrum of the modulated signal. This result was used to propose a new circuit architecture utilizing a chaotic signal (deterministic noise) in order to achieve an optimized level of the PSD for the modulated signal.

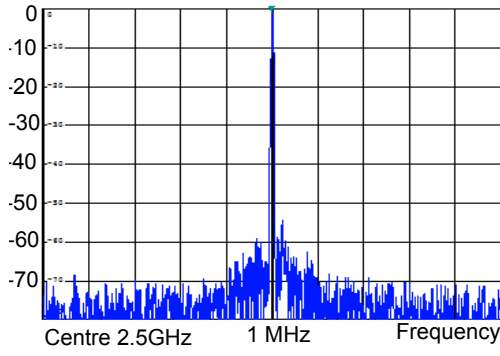
2.3 Impact of various parameters on the frequency spectra of the modulated signal

A sinusoidal modulating waveform does not provide optimum attenuation of the clock harmonics. The energy in the spectrum of the modulated waveform (x_m) will tend to concentrate at those frequencies corresponding to points in the modulating waveform where $\frac{dx_m}{dt}$ is small. This can be observed in figure 2.1 where a sinusoidal signal was used to frequency modulate a clock signal. The spectrum exhibits a peaking of the amplitude at the minima and maxima of the sine wave where the time derivative is equal to zero. Also, since $\frac{dx_m}{dt}$ is maximum at the zero crossing, the amplitude of the spectrum is low at the corresponding frequencies. Thus higher attenuation of the peak energy can be obtained by additional reduction of the amplitude of the spectrum lines. The peaks of the amplitude are reduced when the triangular wave is used to modulate the clock signal as shown in figure 2.4. Since $\frac{dx_m}{dt}(\text{sinusoid}) > \frac{dx_m}{dt}(\text{triangular})$ at the zero crossing, the amplitudes at the centre of the spectrum are slightly increased in case of triangular modulation. However, this is offset by a reduction in the amplitudes at the edges of the spectrum. Further flattening of the spectrum can be achieved by increasing the time derivative at the peaks and decreasing the time derivative at the zero crossing point of the modulating profile. Hardin et al. [61], [69] proposed a parametric family of cubic polynomials to describe the profile [1]:

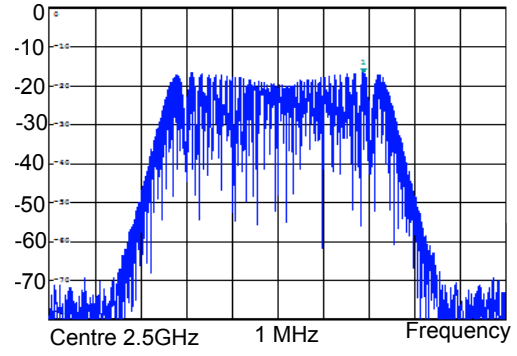
$$c(x) = 16(4 - p)x^3 + px \quad (2.43)$$

where

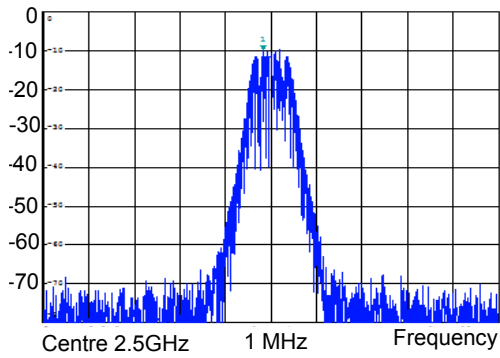
$$x \in \left[-\frac{1}{4}, \frac{1}{4}\right] \quad (2.44)$$



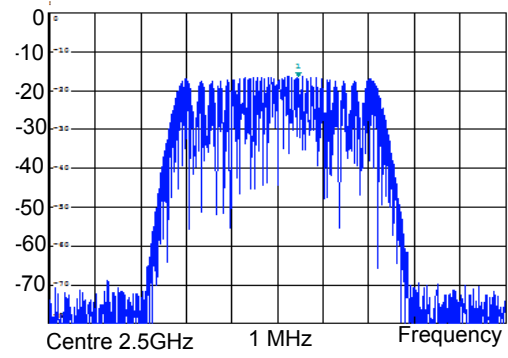
(a) Unmodulated peak: 0dBm



(b) Triangular FM $\pm 0.1\%$ Peak: $-16.7dBm$



(c) Triangular FM $\pm 0.02\%$ Peak: $-9dBm$



(d) Hershey Kiss FM $\pm 0.1\%$ Peak: $-16.8dBm$

Figure 2.4: Impact of various modulation profiles on the frequency spectrum of the modulated signals

By setting $p = 4$, a triangular modulation profile is achieved, while $p = 4.12$ results in the slightly curved profile [70] (known as Hershey kiss modulation profile). Matlab simulations were carried to study the impact of various modulation profiles. Referring to figure 2.4, it can be observed that a wider bandwidth, figure 2.4(b) (large β) leads to lowering of the power compared to a smaller bandwidth (smaller β), figure 2.4(c). Figure 2.4 (d) shows that the Hershey kiss profile leads to an almost flat spectrum.

The modulation index (β) can be varied by either changing the frequency deviation or the frequency of the modulating signal. For a fixed modulating frequency (f_m),

the modulation index is proportional to the amplitude of the modulating signal. An increase in the amplitude of the signal generates new sidebands. The modulation index can also be changed by keeping the amplitude of the modulating signal constant and varying the modulation frequency. The impact of varying β by changing the frequency spread can be seen in figure 2.5. More number of harmonics are added with an increase of the modulation index β . The designer needs to keep in mind the impact of changing f_{Δ} or f_m to make an optimal choice for deciding which parameter to change for obtaining the target β .

The value of maximum frequency deviation Δf is limited by the timing constraints in the system. For example, in case of the high speed IO's there is an upper limit on the maximum amount of variation or jitter that a clock must have. The SSC clock specification must include this budget so that the FM clock variation does not increase this specification.

As the main harmonic order increases, the side-band bandwidth also increases (linearly with the harmonic order for higher harmonics) while the amplitude decreases as depicted in figure 2.6. Referring to figure 2.6, it can be formulated that the overlap occurs when

$$m_{overlap}f_o + \frac{B_m f_o}{2} = (m_{overlap} + 1)f_o + \frac{B_{m+1} f_o}{2} \quad (2.45)$$

where $m_{overlap}$ is the harmonic at which overlap occurs, B_m depicts the bandwidth of the m^{th} harmonic and f_o is the centre frequency. As Δf increases $m_{overlap}$ decreases. Thus, larger value of Δf produces an overlap at lower main harmonics leading to an undesired increase in the displayed spectral amplitude. The amplitude of the harmonic spectrum decreases in proportion to $\Delta f^{\frac{1}{2}}$ [71].

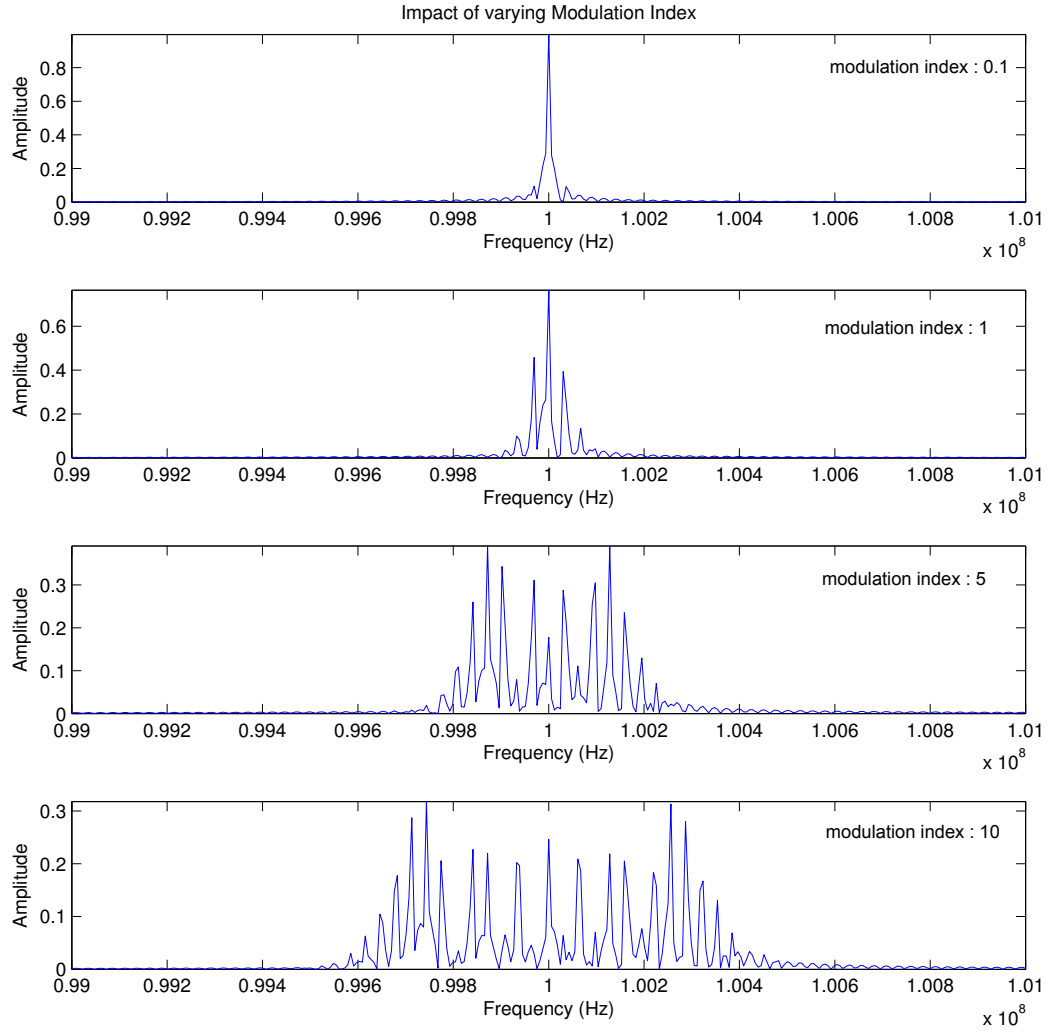


Figure 2.5: Effects of changing β on the spectral content of the modulated signal with fixed f_m and varying the frequency deviation, f_Δ for modulation frequency $f_{mod} = 32kHz$, centre frequency $f_c = 100MHz$.

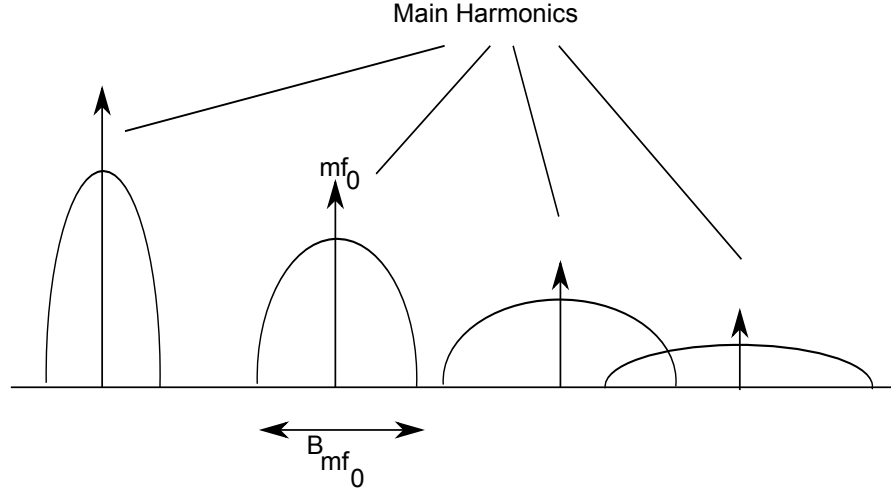


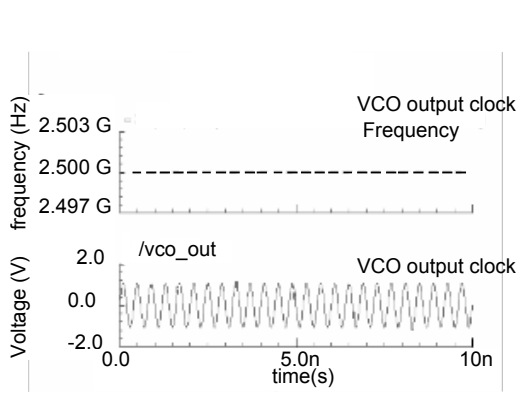
Figure 2.6: Impact of increasing Δf

2.3.1 Behavioural Modelling to study the impact of various parameters

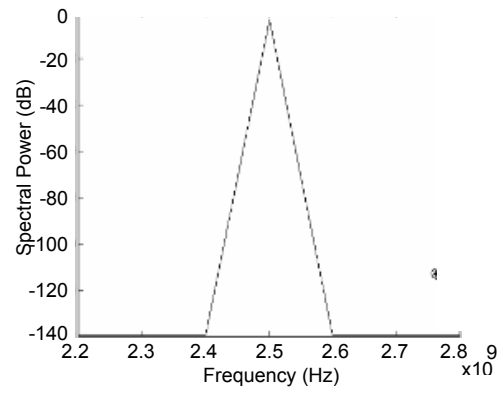
A verilogA model of a voltage controlled oscillator (VCO), appendix 7.3.1, was developed to study the impact of various modulation profiles on the frequency spectrum of the modulated signal. A sinusoidal carrier was utilized for various studies. The spectrum of the unmodulated clock, figure 2.7 (a), is shown in figure 2.7 (b). Figure 2.7 (c) plots the change in the frequency of the sine wave with time. Figure 2.7 (d) shows a log plot of the frequency spectrum of the sinusoidal modulated waveform. Comparing with figure 2.7 (b) a reduction of approximately 12 dB in the spectrum is observed. Two peaks also arise symmetrically placed above and below the fundamental frequency by 0.2 GHz. This is same as the maximum and minimum value of the frequency after modulation. This proves the statement made earlier that the energy is concentrated at the point where the time derivative is minimum, i.e. the peak and maximum points. The peaks in the spectrum are not desirable as they are the measure of EMI radiation. It can also be observed that the number of peaks is equal to the number of points where the time derivative is

zero. A triangular modulation is now applied as shown in figure 2.7 (e). It can be seen in figure 2.7 (f) that the spectrum power is flat and there are no distinct peaks seen. It can also be observed comparing figure 2.7 (b) and figure 2.7 (f) that using a triangular modulation profile a reduction of approximately 20 db has been achieved for a clock frequency of 2.5 GHz with a modulation frequency of 32 kHz (voltage waveform which results in a symmetrical frequency spread of ± 0.2 GHz around centre frequency).

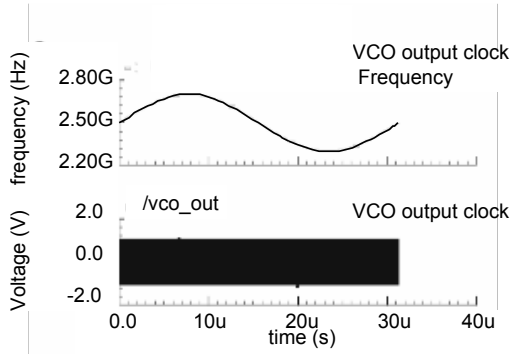
To study the impact of stable points in the modulation profile, trapezoidal modulation was applied to the VCO. As illustrated in figure 2.8 (a), since the VCO output frequency is proportional to the control voltage, the frequency also follows a trapezoidal pattern. Figure 2.8 (b) plots the frequency spectrum of the modulated waveform. It can be observed that there are two peak harmonics present in the spectrum. To study the effect of the flat band on the frequency spectrum, the modulation profile was changed to have a less flat region or a lesser region with zero time derivative. Figure 2.8 (c) depicts the frequency plot vs the time showing the modulation profile. It can be seen in figure 2.8 (d) that there are still two peak harmonics present in the spectrum as expected. Comparing figure 2.8 (d) with figure 2.8 (b) it can be observed that the difference between the trough and the peak has decreased. A decrease in the flat region of the modulation profile leads to the lowering of the difference between the peak and the trough will keep. To achieve a flat frequency spectrum for a zero or a minimal flat region modulation profile i.e. a flat spectral plot for a triangulation modulation profile as can be observed in figure 2.7 (f). Another interesting periodic profile is a stair case waveform. As illustrated in figure 2.8 (e) the frequency modulation has a stair case waveform. The frequency of the modulation wave is 32 kHz with 5 steps on each side of the fundamental. Since there are 5 steps on both sides of the fundamental frequency, from earlier



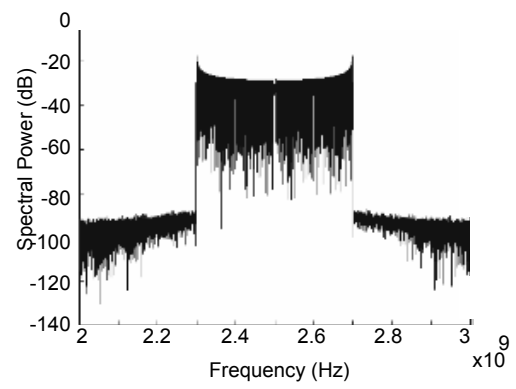
(a) Transient response of unmodulated clock



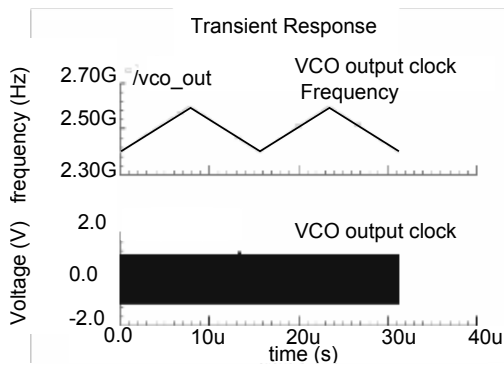
(b) Frequency response of unmodulated clock



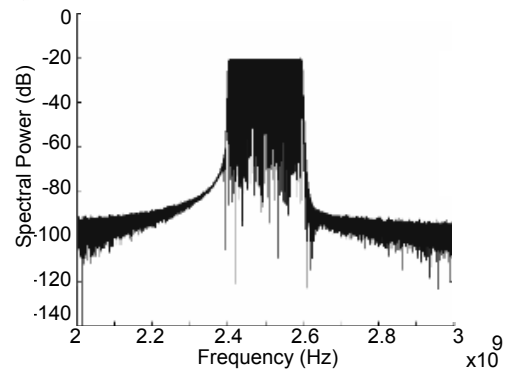
(c) Transient response of sinusoidal modulated clock



(d) Frequency spectrum of sinusoidal modulated clock



(e) Transient response of triangular modulated profile



(f) Frequency spectrum of triangular modulated clock

Figure 2.7: Frequency spectrum of various modulation profiles as applied to the VCO model

observations five peak harmonics should be expected in the frequency spectrum, on both sides of the fundamental tone as illustrated in figure 2.8 (f). A reduction of the peak power by around 10 dB with respect to the fundamental non modulated sinusoidal sine wave was seen.

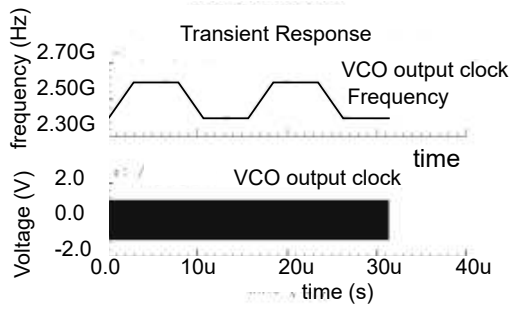
2.4 Chaotic Modulation

As the number of tones are increased in the modulating signal, a higher number of tones are added to the output signal spectrum. Furthering the logic, it was inferred that an infinite number of tones will lead to the most optimum spreading of the energy in a given bandwidth. Infinite tones in a signal lead to white noise. However, producing a white noise signal is quite complex. Even if it was possible to create a perfect noise source, a signal being modulated by noise would be very difficult to re-construct at the receiver. A feasible alternative is to generate a noise-like signal using chaotic transfer functions. A brief introduction to chaotic theory has been provided in appendix 7.2.

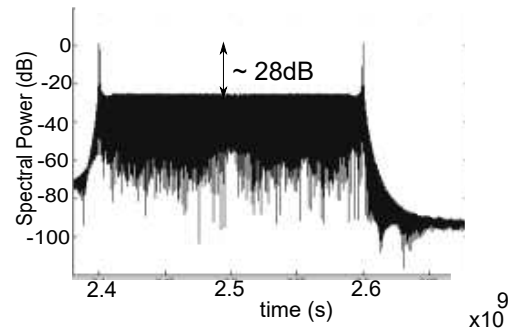
The current work aims to utilize a chaotic transfer function to introduce various tones into the modulating profile. Figure 2.9 depicts the block diagram of the proposed system. It comprises of a chaotic modulator generating the modulating signal x_{n+1} . The modulating signal is fed to the frequency modulator which varies the output frequency in proportion to the modulating signal. A tent map [72] function has been utilized for the current work.

$$\text{Case 1: } x_n \in \left[0, \frac{1}{2}\right)$$

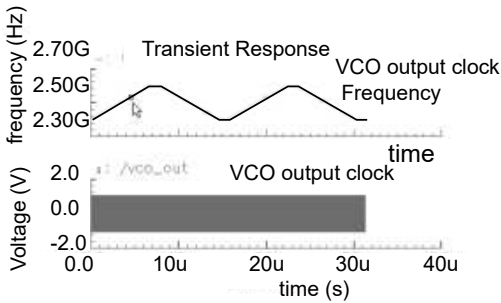
$$x_{n+1} = 2x_n \tag{2.46}$$



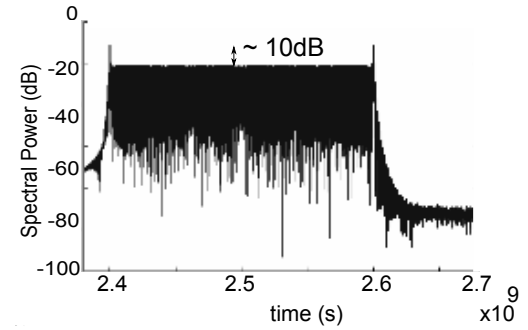
(a) Transient simulation of a 2 step stair case modulating signal



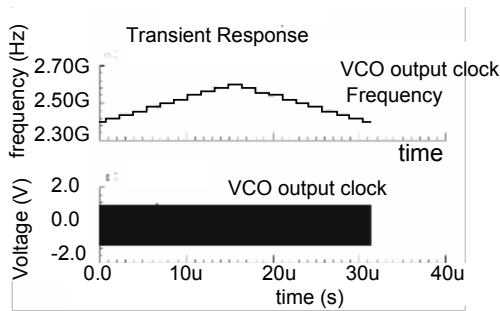
(b) Frequency spectrum of (a)



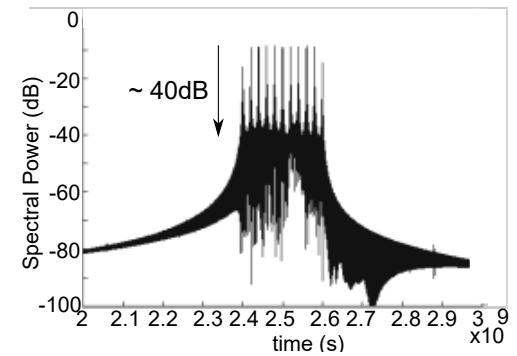
(c) Transient response PSD of a signal modulated with a 2 step stair case modulating signal (lower flat band)



(d) Frequency spectrum of (c)



(e) Transient response of a signal modulated with a 10 step stair case modulated signal



(f) Frequency response of (e)

Figure 2.8: PSD of various modulation profiles as applied to the VCO model

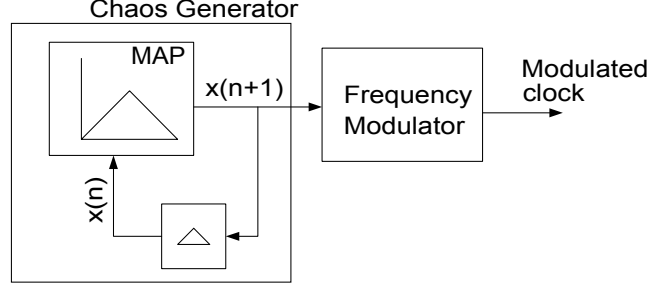


Figure 2.9: Block diagram of the chaotic spread spectrum clock modulator

Case 2: $x_n \in \left[\frac{1}{2}, 1 \right]$

$$x_{n+1} = 2(1 - x_n) \quad (2.47)$$

A non-PLL open loop modulator was developed for modulating the clock to allow a low power operation and achieve a flatter output spectrum of the modulated clock as discussed in chapter 4. Figure 2.9 depicts the block diagram of the proposed chaotic modulator. The map generates an iterate x_{n+1} according to the chaotic transfer function (MAP). The generated iterate x_{n+1} is sampled and utilized for the next computation. The generated sequence is fed to the frequency modulator. The frequency modulator modulate the frequency proportional to the generated sequence. Van et al. [72] have shown that the chaotic maps such as tent maps generate statistically uniform PDF's for the output sequence. Since, the modulated clock varies as per the generated sequence, the clock will be modulated containing various tones leading to lowering of the spectrum. Chapter 4 describes in detail the circuit architecture for implementing a chaotic modulator.

2.5 Concluding Remarks

This chapter discussed the basics of the theory behind the spread spectrum signals. This thesis has extended the previously reported work to three tone, N tone modulation profiles. The equations developed for three tone and N tone were developed by inference and a formal proof is pending. Chapter 3 will look into architectures utilizing periodic modulation profiles for generating SSC signals; while Chapter 4 will propose a non-PLL based topology for modulating a signal using a chaotic signal.

3 Circuit Architectures for realizing Periodic Spread Spectrum Clocks

The spread spectrum clock generators can be broadly classified as phase locked loop (PLL) based implementations and non-PLL based implementations. Most of the reported work done has utilized PLLs for modulating the incoming clock with a variety of modulating profiles. Recently, a new class of non-PLL modulators have been reported as an alternative to PLL based schemes. Both kinds of implementation have their respective advantages and disadvantages. Spread spectrum clock generators (SSCG) implementations can be broadly classified into various categories:

- The first kind modulates the Voltage Controlled Oscillator (VCO). The control voltage could either be varied by modifying the loop filter to generate the modulating profile [13] or by adding a summing junction through some scheme resulting in a modulated VCO control voltage [15], [12], [7], [73].
- The second type modulates the divider in the phase locked loop utilizing fractional N PLL [74], [75], [76].
- The third type combines digital signal processing circuits and the multiphase outputs of the clock source to modulate the incoming clock signal and outputting a modulated clock [77], [78], [79], [80].

The current chapter covers in brief the PLL based topologies reported earlier. Studies were done on a self-biased PLL (SBPLL) to study the impact of the PLL loop bandwidth on the modulation profiles. Subsequently, a new class of non-PLL based SSC generator is proposed and simulated. The current chapter deals with periodic SSC profiles.

3.1 Phase Locked Loop Based SSC Generators

Figure 3.1 depicts a generic block diagram of the well known charge pump PLL [11]. It is composed of a phase comparator, charge pump, loop filter, bias generator and a VCO. The negative feedback in the loop adjusts the VCO output frequency by integrating the phase error that results between the periodic reference input and the divided VCO output. Once in lock, the VCO will generate an output with a frequency that is N times larger than that for the reference input such that there is no detected phase error between the reference and the divided output. Since the loop filter integrates the charge representing the phase error and the VCO integrates the output frequency to form the output phase, the PLL has a 2^{nd} order closed loop response. The output phase of the PLL is given as:

$$\theta_{output}(s) = \left(\theta_{input}(s) - \frac{\theta_{output}(s)}{N} \right) \times i_{cp} \times \left(r + \frac{1}{sC_1} \right) \times K_{VCO} \times \frac{1}{s} \quad (3.1)$$

where

i_{cp} : charge pump current

r: loop filter resistor

C_1 : loop filter capacitance

K_{VCO} : VCO gain

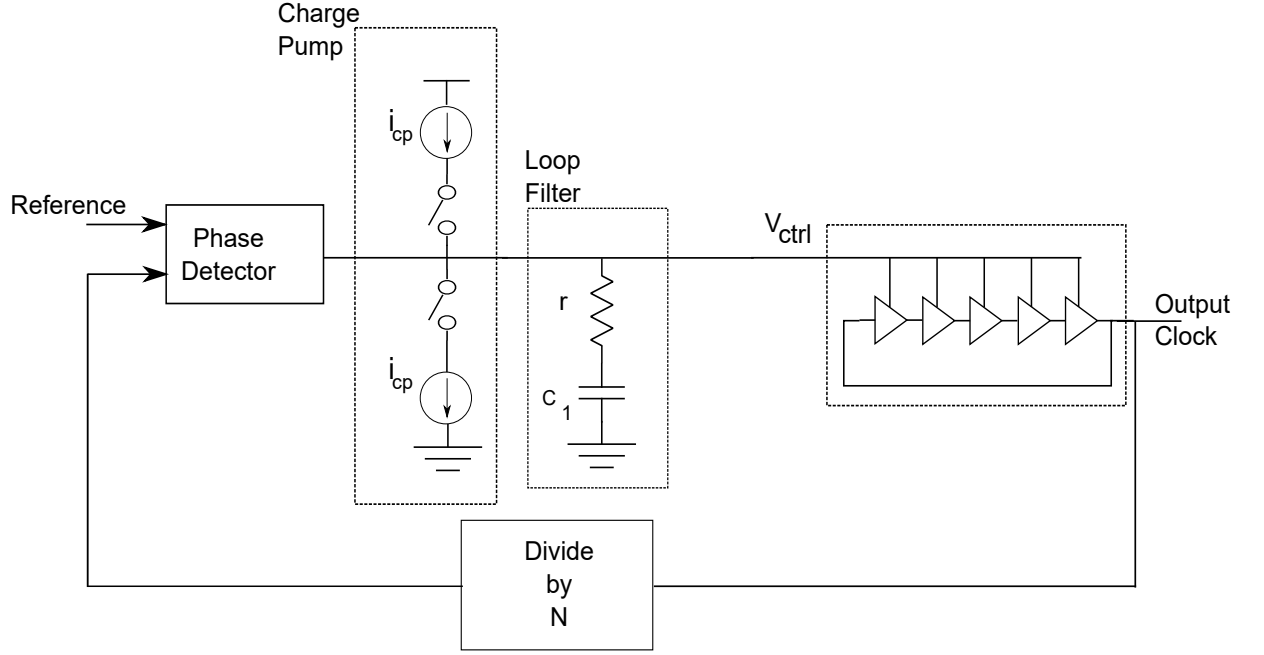


Figure 3.1: Block diagram of a charge pump PLL [11]

θ_{input} : input phase

N: PLL divider ratio

Thus:

$$\frac{\theta_{output}(s)}{\theta_{input}(s)} = \left(\frac{1}{N} + \frac{s}{i_{cp} \times \left(r + \frac{1}{sC_1} \right) \times K_{VCO}} \right)^{-1} \quad (3.2)$$

Equation 3.2 can be re-written as:

$$\frac{\theta_{output}(s)}{\theta_{input}(s)} = N \times \frac{1 + 2\zeta \cdot \frac{s}{\omega_n}}{1 + 2\zeta \cdot \left(\frac{s}{\omega_n} \right) \cdot \left(\frac{s}{\omega_n} \right)^2} \quad (3.3)$$

where ζ is the damping factor and is given by[11]:

$$\zeta = \frac{r}{2} \times \sqrt{\frac{1}{N} \times i_{cp} \times K_{VCO} \times C_1} \quad (3.4)$$

and ω_n is defined as the loop bandwidth (rad/s) and is given by[11]:

$$\omega_n = \frac{2 \times \zeta}{r \times C_1} \quad (3.5)$$

The close loop response of the PLL is characterized by the loop bandwidth and the damping factor. The PLL is critically damped with a damping factor of one and over-damped with a damping factor greater than 1. Referring to equation 3.4 and equation 3.5 we can thus see that for a constant i_{cp} , K_{VCO} and r , we get a constant damping factor and a constant loop bandwidth. A constant bandwidth is a constraint to achieving a wide operating frequency range and low input tracking jitter. The ω_n should be positioned as close as possible to ω_{REF} to minimize the total phase error. Also, as seen ω_n depends on i_{ch} , K_{VCO} , r and C_1 and not on ω_{REF} . However, ω_n must be kept at least a decade below than the lowest operating frequency for stability. Thus, ω_n must be conservatively set for stability at the lowest operating frequency with the worst case process variations, rather than set for optimized jitter performance.

In order for the phase locked loop to accurately reproduce the spread spectrum clock generator clock at the output, the closed loop bandwidth must pass a sufficient number of harmonics of the modulating signal [69]. The more the number of harmonics within the bandwidth of the phase locked loop the higher will be the accuracy of the modulating waveform at the output of the PLL.

The closed-loop bandwidth has an effect on the time required by the PLL to obtain lock after an abrupt frequency change. In general, increasing the bandwidth reduces the time required to obtain the lock, although it may introduce additional effects such as overshoots resulting in a dramatic increase in the VCO operating frequency leading to lock failure. Thus, while optimizing the phase locked loop to pass a spread

spectrum clock, careful analysis of all the parameters should be done so as to get the desired profile. If the PLL is not optimized properly the reduction in the EMI will be less than required and thus the profile obtained at the output will not be the required one. To study the impact of the loop bandwidth on the SSC profile, a self biased PLL was simulated while varying the modulation frequency with respect to loop bandwidth. The results have been presented in 3.1.2.

The output clock of the PLL can be modulated by either changing the control voltage of the voltage control oscillator [15] or by modulating the divider ratio [75]. Numerous papers have been published using one of the two types to module the PLL clock. The following sections look at the basic theory behind the two approaches.

3.1.0.1 Direct Modulation of VCO

An ideal voltage-controlled oscillator generates a periodic output wave whose frequency is a linear function of the control voltage V_{ctrl} . The instantaneous frequency of the VCO can be given as [81] (the variables have been changed with respect to [81] to avoid conflict with previously defined variables).

$$f_{VCO_{out}} = f_{VCO_{FR}} + K_{VCO}V_{VCO_{ctrl}} \quad (3.6)$$

where $\omega_{VCO_{out}}$ is the output frequency of the voltage controlled oscillator, K_{VCO} is the VCO gain , V_{ctrl} is the control voltage of the VCO generated by the loop filter. The instantaneous phase of the VCO is given as

$$\theta_{i_{VCO}} = 2\pi f_{VCO_{FR}}t + 2\pi K_{VCO} \cdot \int_0^t V_{ctrl} dt$$

Thus, the output of the VCO can be given as

$$y_{VCO}(t) = A_{VCO} \cdot \cos \left(2\pi f_{VCO_{FR}} t + K_{VCO} \cdot \int_0^t V_{ctrl} dt \right) \quad (3.7)$$

Taking case where the control voltage is composed of a single tone and given as $V_{ctrl}(t) = A_{VCO_m} \cos(2\pi f_{VCO_m} t)$, then [81]

$$y_{VCO}(t) = A_{VCO} \cdot \cos \left(2\pi f_{VCO_{FR}} t + \frac{K_{VCO} A_{VCO_m}}{f_{VCO_m}} \sin(\omega_{VCO_m} t) \right) \quad (3.8)$$

Equation 3.8 is similiar to 2.10 with

$$\beta_{VCO} = \frac{K_{VCO} V_{VCO_m}}{f_{VCO_m}} = \frac{\Delta f_{VCO}}{f_{VCO_m}} \quad (3.9)$$

The quantity $K_{VCO} V_{VCO_m}$ represents the peak frequency deviation of the FM signal from the center frequency and is directly proportional to the amplitude of the modulating signal and the gain of the VCO.

The VCO modulation can be accomplished by introducing an adder before the VCO as depicted in the linear model of the CPLL in figure 3.2.

Multiple approaches have been published to modify the control voltage of the VCO according to the modulation profile required. The basic principle is same as discussed i.e. of modulating the control voltage of the VCO. Chang et. al. [12] modified the loop filter to generate a triangular profile by inserting a second loop. Figure 3.3 (b) depicts the implementation of the loop filter as proposed in [12]. As can be seen a modulating current source has been added to the traditional filter 3.3(a). By utilizing the superposition theorem, we can analyze the output waveform at V_{ctrl} .

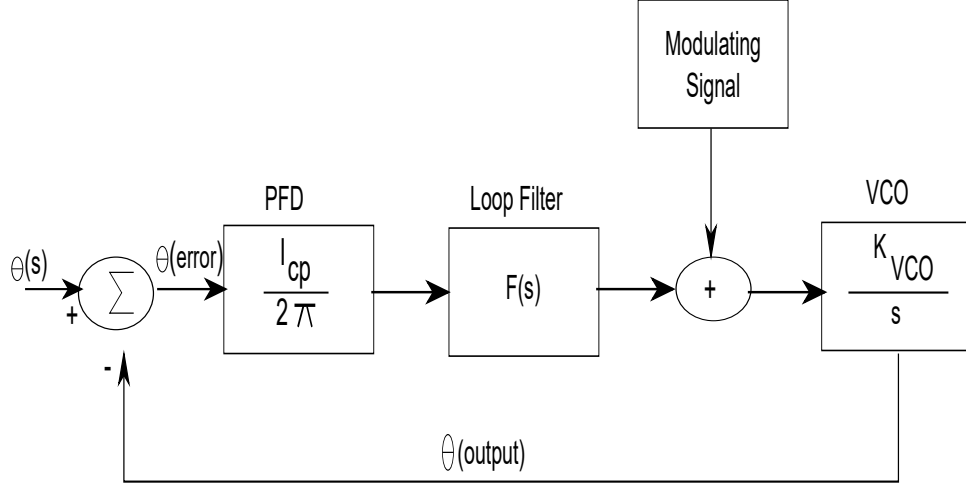


Figure 3.2: Forward Path Modification for generation of modulated clock

It can be observed from 3.3 (c) that

$$V_{ctrl_{VCO_{mod}}} = \frac{1}{sC_2} \cdot I_0 \quad (3.10)$$

$$= \frac{\frac{1}{sC_2} \cdot \left(R_1 + \frac{1}{sC_1}\right)}{\left(R_2 + \frac{1}{sC_2}\right) + \left(R_1 + \frac{1}{sC_1}\right)} \cdot I_2 \quad (3.11)$$

Thus,

$$\frac{V_{ctrl_{VCO_{mod}}}}{I_2} = \frac{\frac{1}{sC_2} \cdot \left(R_1 + \frac{1}{sC_1}\right)}{\left(R_2 + \frac{1}{sC_2}\right) + \left(R_1 + \frac{1}{sC_1}\right)} \quad (3.12)$$

If $R_1C_1=R_2C_2=RC$ [12], then

$$\frac{V_{ctrl_{VCO_{mod}}}}{I_2} = \frac{1 + sR_1C_1}{s^2R_2C_2C_1 + s^2R_1C_1C_2 + s(C_1 + C_2)} \quad (3.13)$$

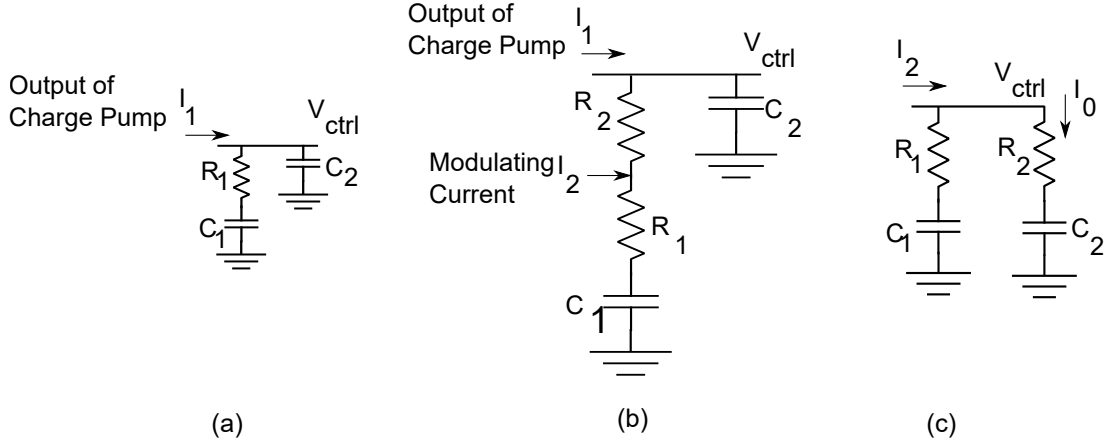


Figure 3.3: Modified Filter for creating the triangular waveform [12] (a) Traditional filter (b) modified filter with a current source I_2 (c) Filter re-drawn to enable mathematical analysis for determining the impact of modulating current (I_2) on the control voltage.

$$\frac{V_{ctrlVCO_{mod}}}{I_2} = \frac{1 + sRC}{s^2RCC_1 + s^2RCC_2 + s(C_1 + C_2)} \quad (3.14)$$

$$\frac{V_{ctrlVCO_{mod}}}{I_2} = \frac{1}{s(C_1 + C_2)} \quad (3.15)$$

Thus, by creating a programmable current I_2 , a triangular ramp can be created at the V_{ctrl} , thereby modulating the frequency of the VCO. A problem with the approach is that $R_1C_1 = R_2C_2$.

Huang et. al. [13] resolved the stringent requirement by modifying the proposed loop filter as depicted in figure 3.4 (a). Open circuiting the current source I_1 , the circuit can be redrawn as depicted in figure 3.4(b).

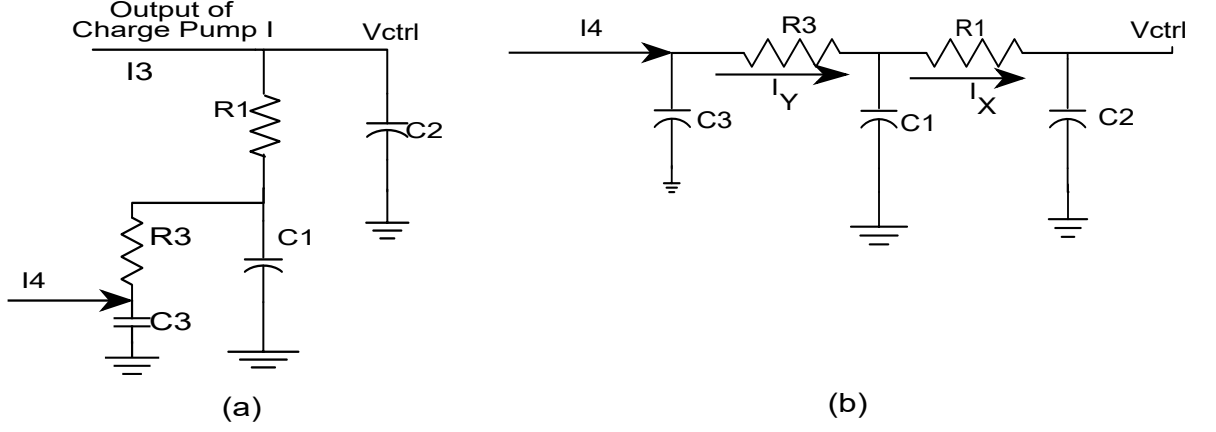


Figure 3.4: (a) New filter proposed for creating the triangular wave proposed by huang et. al. [13] (b) Filter re-drawn to enable mathematical analysis for determining the impact of modulating current (I_5) on the control voltage.

Referring to 3.4 (b)

$$I_Y = \frac{\frac{1}{sC_3}}{\frac{1}{sC_3} + R_3 + \frac{\left(\frac{1}{sC_1}\right) \times \left(R_1 + \frac{1}{sC_2}\right)}{\frac{1}{sC_1} + R_1 + \frac{1}{sC_2}}} \times I_4 \quad (3.16)$$

$$I_Y = \frac{1}{1 + sC_3R_3 + \frac{(sC_3)\left(\frac{1}{sC_1}\right) \times \left(R_1 + \frac{1}{sC_2}\right)}{\frac{1}{sC_1} + R_1 + \frac{1}{sC_2}}} \times I_4 \quad (3.17)$$

$$I_X = \frac{1}{\frac{1}{sC_1} + R_1 + \frac{1}{sC_2}} \times I_Y \quad (3.18)$$

Since,

$$V_{ctrl_{VCO_{mod2}}} = I_X \times \frac{1}{sC_2} \quad (3.19)$$

Thus,

$$\frac{V_{ctrlVCO_{mod2}}}{I_4} = \frac{1}{s(C_2 + C_1) + s^2 C_1 C_2 R_1} \times \frac{1}{1 + sC_3 R_3 + \frac{\frac{C_3}{C_1} \times (sC_2 + 1)}{\frac{C_2}{C_1} + sC_2 R_1 + 1}} \quad (3.20)$$

For $C_1 \gg C_3, C_1$, equation 3.20 reduces to [13]

$$\frac{V_{ctrlVCO_{mod2}}}{I_2} = \frac{1}{s(C_1 + C_3)} \quad (3.21)$$

Thus the circuit now reduces to the desired second order low pass filter. An advantage of this approach is that now the constraint is less stringent than required in [12].

The advantage of direct modulation of VCO is a simple circuit structure. However the loop bandwidth of a PLL has to be much less than the modulation frequency to allow the frequency variation of the VCO (as discussed in 3.1 and shown through simulations in 3.1.2). In general, the required loop bandwidth is about one of ten times that in the modulation [69]. If modulation frequency is around 30 to 50 kHz then the loop bandwidth should be kept a decade lower at around 3 to 5 kHz. Referring to equation 3.5, it can be seen that the loop bandwidth is inversely proportional to the loop filter capacitance. Thus, one disadvantage of the discussed schemes is the requirement of a large capacitance to achieve a low loopbandwidth to allow sufficient harmonics of the modulated clock through. [12].

To reduce the capacitance required, capacitance multiplication has been proposed by chen et. al. [14]. The principle of capacitance multiplication is depicted in figure 3.5 . For the conventional filter depicted in figure 3.3(a), the zero of the filter is given by $\omega_{z1} = \frac{1}{R_1 C_1}$ while for the modified filter (figure 3.5), the zero can be derived as $\omega_{z2} = \frac{1}{R_1(nC_1 + C_2)}$. Thus, by controlling the charge current I_{CP2} , the zero can be

effectively lowered without the need to increase the cap. However, the issue with the approach is that an extra charge pump is required. Also, it is interesting to notice that the capacitance C_1 is a floating cap. Floating cap in CMOS is usually achieved with Metal Insulator Metal Caps (MIM). MIM caps are expensive as they require extra masks. The floating capacitor in a standard CMOS process can be poly-insulator-poly (PIP) or metal-insulator-metal (MIM) cap and needs extra masks and process steps.

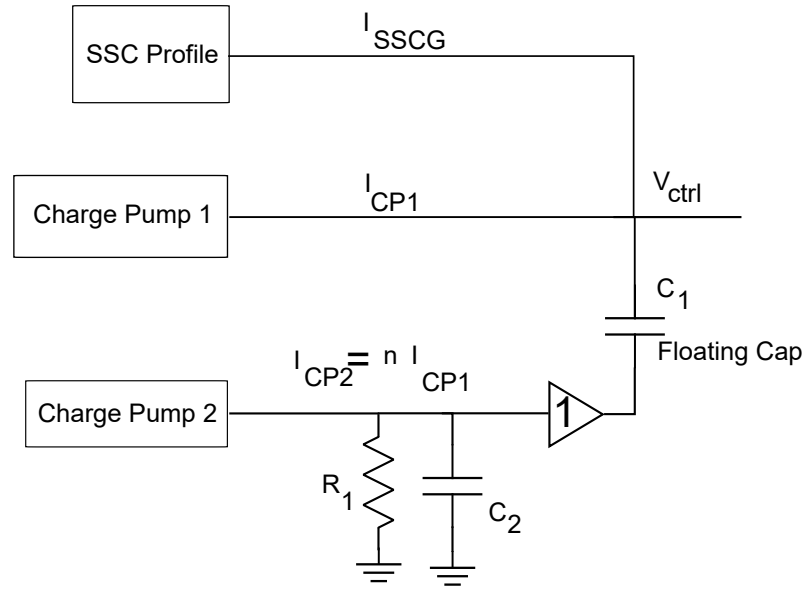


Figure 3.5: Capacitance Multiplication Principle [14]

Razavi et.al. [82] Hsieh et.al. [15] proposed an alternative capacitance multiplication method utilizing grounded caps as shown in 3.6. I_{SSCG} provides current profile for the VCO modulation.

The first path composed of R_1 and C_2 and is a low-pass filter. The second path composed of C_1 and unity gain buffer acts as an integrator. The voltages from these two paths are combined together so that a zero is created in transfer function. Ignoring the modulation current, I_{SSCG} , referring to figure 3.6(a), the transfer function can

be derived as

$$\frac{V_{ctrl_{cc}}}{I_{CP1_{cc}}} = \frac{R_{1_{cc}} \left(s + \frac{1}{R_{1_{cc}} n C_{1_{cc}}} \right)}{s (1 + s R_{1_{cc}} C_{2_{cc}})} \quad (3.22)$$

Referring to figure 3.6(b), the transfer function can be derived as

$$\frac{V_{ctrl_{cc}}}{I_{CP_{cc}}} = \frac{R_{1_{Cc}} \left(s + \frac{1}{R_{1_{cc}} n C_{1_{cc}}} \right)}{s \frac{n C_1 + C_2}{n C_2} \left(1 + s R_{1_{cc}} \frac{n C_{1_{cc}} C_{2_{cc}}}{n C_{1_{cc}} + C_{2_{cc}}} \right)} \quad (3.23)$$

Comparing equation 3.22 with equation 3.23, it can be seen that both exhibit same zero response. An effective capacitance multiplication has been achieved. By choosing a high value of n, the size of capacitance can be reduced. In addition, the filter is less noisy as there is only one active device and requires a smaller area since there is no floating capacitor. The two capacitance can now be implemented as MOS caps connected to a low noise supply.

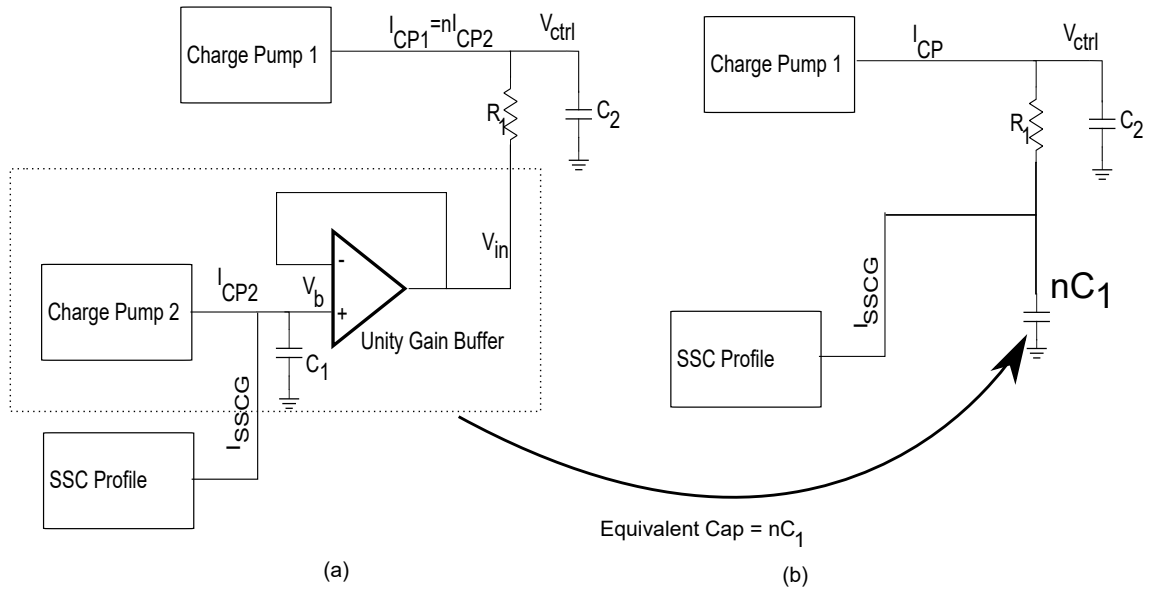


Figure 3.6: Modified dual loop filter not requiring floating caps [15]

Lee et. al. [7] added another block to the PLL to take care of process mismatches by generating mismatch codes at a particular control voltage and generating com-

pensating codes before enabling the frequency modulation path.

3.1.1 Modulating the divider

From the PLL block diagram (figure 3.1), it can be observed that the output frequency is a multiple of the input frequency. A fractional N PLL [16] operates in an almost similar way. In a fractional-N PLL, the N-divider is broken up into the integer divider (N) and a modulus-M interpolator (M), which acts as the fraction function by toggling the N-divider. The interpolator is programmed with some value

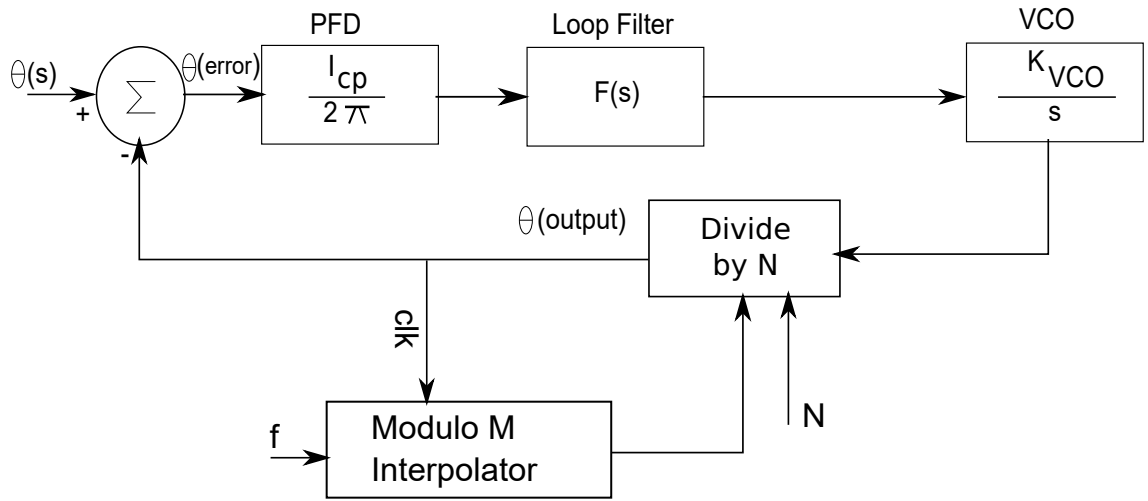


Figure 3.7: Fractional PLL Synthesis [16]

(f). The average division factor is now $N + \frac{f}{M}$ where f is the output frequency $f(out)$ and the Phase Frequency Detector frequency ($f(PFD)$)

$$0 < f < M \quad (3.24)$$

$$N_{fracN} + \frac{f}{M} = \frac{f(out)}{f(PFD)} \quad (3.25)$$

Traditionally, the major drawback of fractional-N PLL is the generation of fraction spurs. A well established solution is to utilize a $\Delta\Sigma$ modulator as depicted in figure 3.8. A $\Delta\Sigma$ delta modulator pushes the quantization noise to the end of higher frequency. Utilizing the $\Delta\Sigma$ modulator in the feedback eliminates spurs by means of randomization and noise shaping [83].

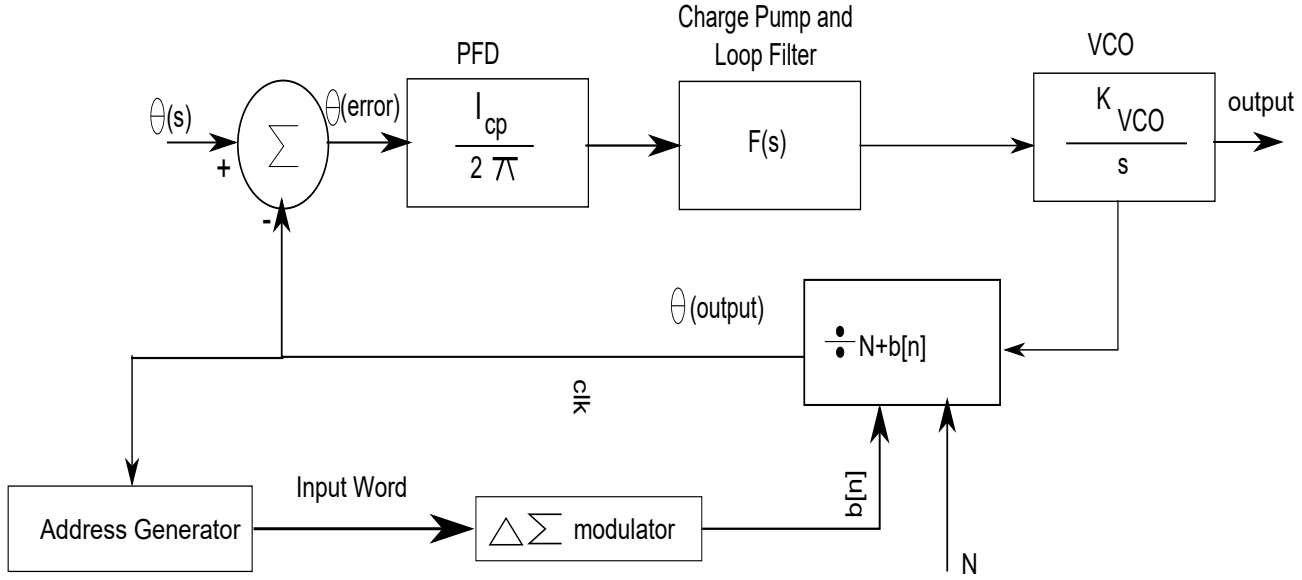


Figure 3.8: Fractional N PLL with $\Delta\Sigma$ modulator

3.1.2 Loop Bandwidth studies for PLL based approaches

To simulate the interaction between the PLL loop bandwidth and the modulating frequency, a self biased phase locked loop was simulated. Figure 3.9 depicts the block diagram of the sbpll. The focus of the work is to study the impact of loop bandwidth on the modulation characteristics [84]. The SBPLL was designed based on [85]. The details of the SBPLL implementation can be found in [86] and was done as a part of Masters thesis.

To determine the bandwidth of the PLL, transient simulation was done. As depicted in figure 3.10 (a,b) the PLL stabilizes after about 500ns. This also gives us a hint

that the bandwidth of the PLL is of the order of 10MHz. A reference frequency of 100 MHz and a multiplier of 22 was utilized to get the 2.2 GHz output.

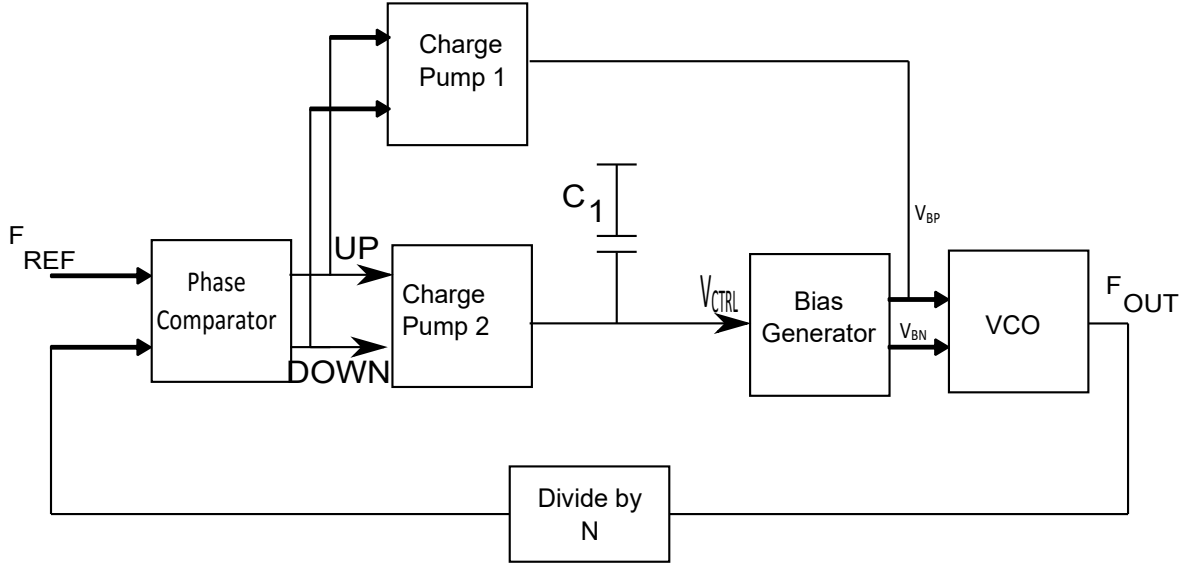
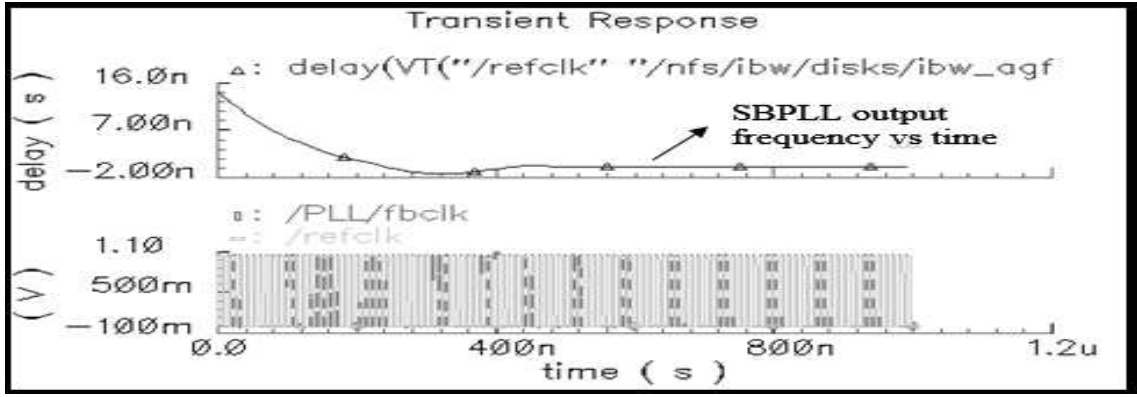


Figure 3.9: Self Bias PLL

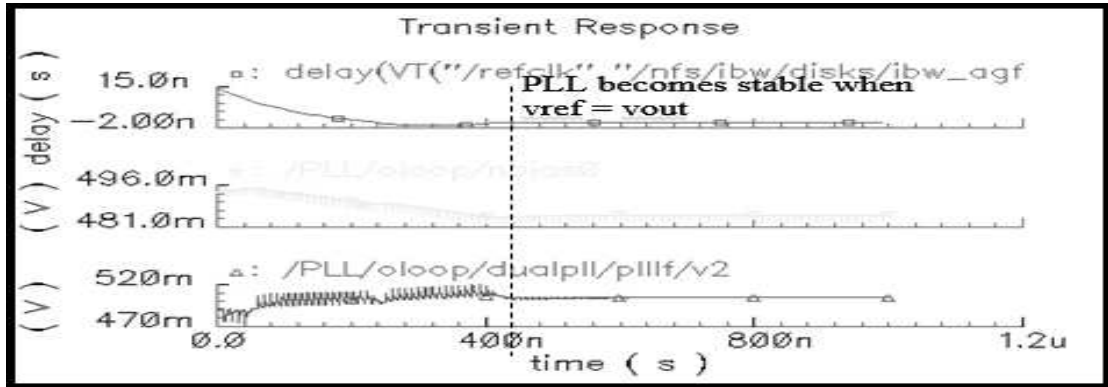
Figure 3.11 shows the frequency spectrum of the un-modulated SBPLL output clock. It can be seen that the PLL has a one peak in the output spectrum which is equal to the reference frequency 2.2 GHz with presence of two side band spurs symmetrical around the fundamental tone.

An adder was added to the output of the charge pump to modulate the V_{ctrl} as depicted in figure 3.12

To obtain the modulated signal, a summing junction was been added before the VCO to modulate the control signal feeding into the voltage control oscillator. As discussed before, the loop bandwidth of the phase locked loop is of the order of 10MHz and is being operated with a multiplier factor of 22 and a reference frequency of 2.2 GHz. The simulation was again run for a period of $1 \mu s$ as the PLL itself takes around 500 ns for settling. Figure 3.14 (a) shows the voltage profile of the signal generated by the charge pump and the loop corrected control voltage going



(a)



(b)

Figure 3.10: (a) frequency output from SBPLL (b) reference clock, nbias and control voltage in SBPLL

in the voltage control oscillator. It can be seen that the phase locked loop has regulated the modulation profile. Although a triangular modulation was inserted in the loop, due to the high loop bandwidth of the phase locked loop (10 MHz), the PLL did not follow the modulation. Due to the loop bandwidth being higher than the modulating signal (V_{mod}), control voltage generated by the PFD + charge pump is in exact opposition with a negative slope in the first half between 500ns and 2.5 μs period, thereby giving a constant bias voltage to the voltage controlled oscillator. This results in no affect on the output frequency of the PLL as can be seen in figure 3.14 (b). In addition, it can be seen that there is no affect on the bias voltage to the current source in the differential buffer stage within the VCO, which

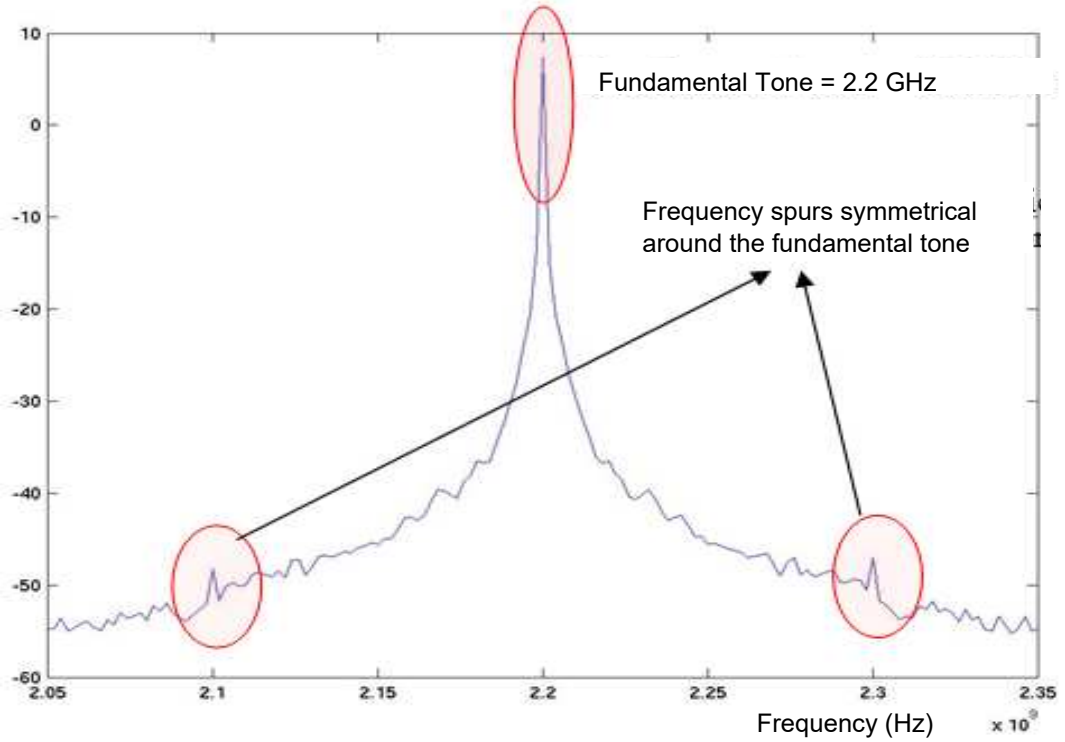


Figure 3.11: Frequency Spectrum of Self Bias PLL

means that the bias current remains the same. This is expected as the change in frequency is only because of the control voltage offset. The above hypothesis leads us to believe that for the forward path modulation to work, the modulation profile should be high enough (of the order of 100) for the phase locked loop to follow it.

Next frequency of the modulation waveform is increased to a factor of 100 with respect to the internal reference frequency. As shown in figure 3.16, we can now see the control voltage following the modulating signal.

It can also be observed in figure 3.16 (b) that due to the change in the control voltage, the output frequency also gets changed. Figure 3.17 depicts the frequency spectrum of the output clock of the SBPLL. It can be observed there has been a decrease in the magnitude of the fundamental tone by an order of 10 dB compared to figure 3.11.

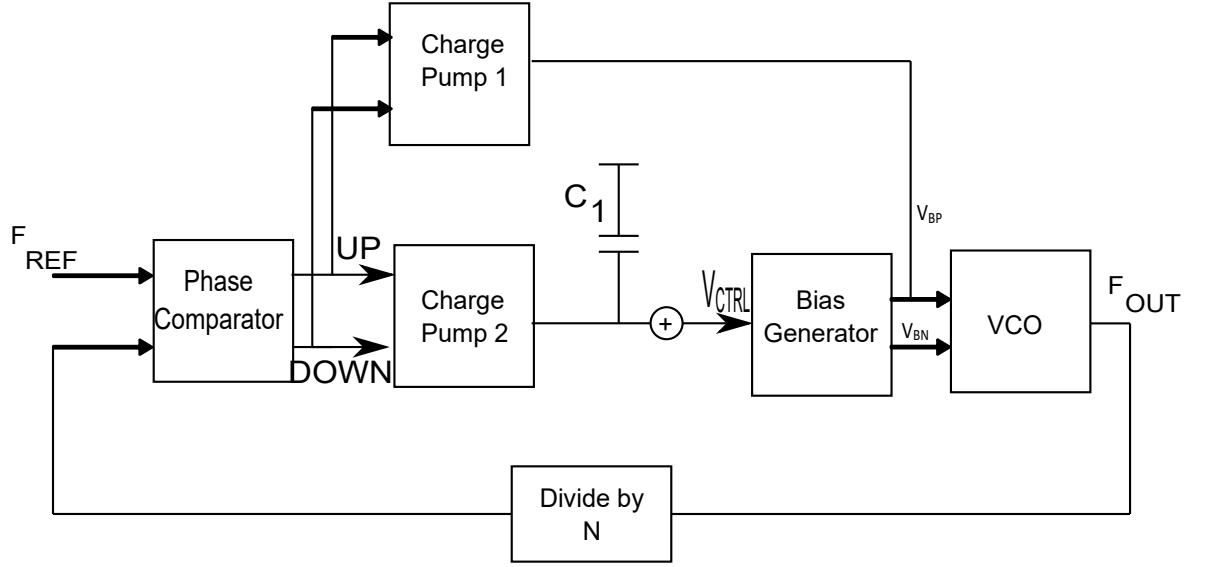


Figure 3.12: Block diagram of self bias charge pump.

Thus, we can conclude that the PLL loop bandwidth impacts the modulation profile inserted in the loop. The modified forward path topology is used when the modulating signal frequency is higher than the PLL loop bandwidth. Similarly, the feedback modified path is preferable where the modulating signal frequency is lower than the PLL loop bandwidth.

A two point modulation approach was recently published [87] utilizing both the direct VCO modulation and the divider modulation to alleviate the problems with the relation between the PLL bandwidth and the modulation frequency [88]. It has been shown that if any mismatches between the two modulation paths are removed, then the output signal can be modulated without distortion and bandwidth limitation.

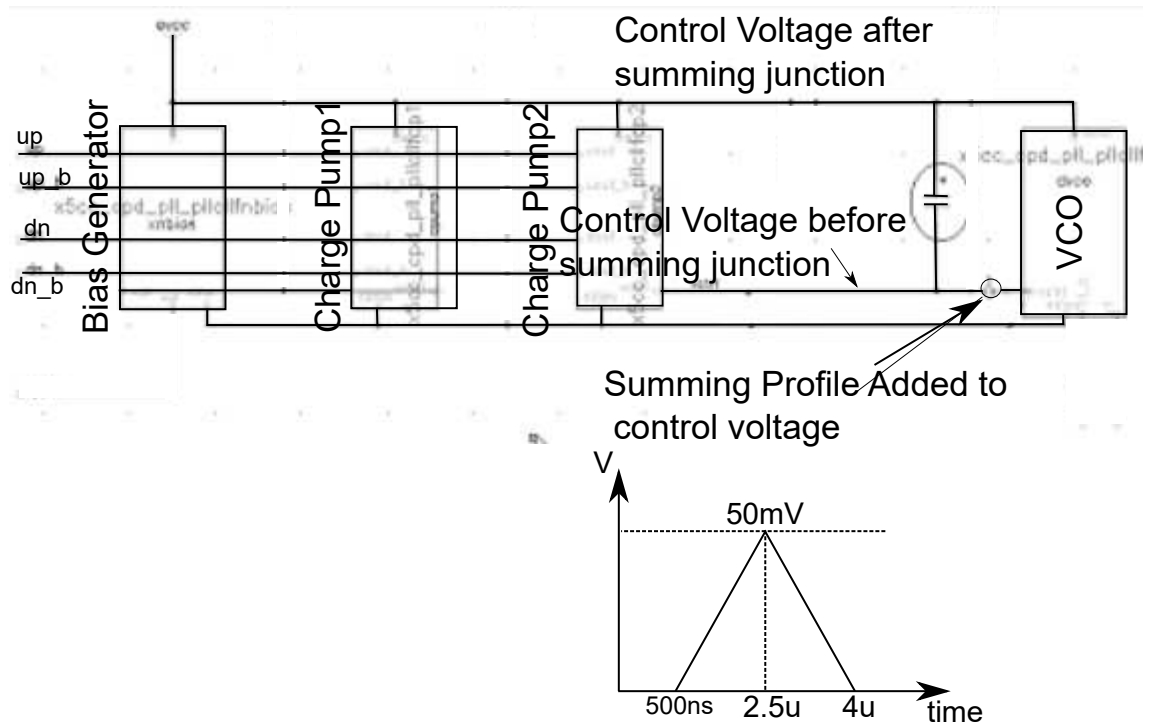
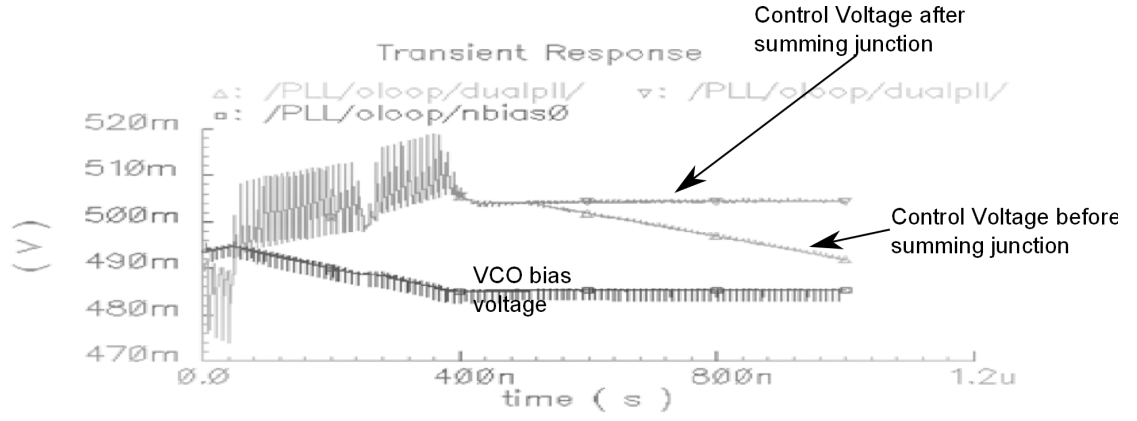


Figure 3.13: Voltage generated by the charge pump and the PFD and the control voltage going into the VCO in case of a slow triangulation modulation profile

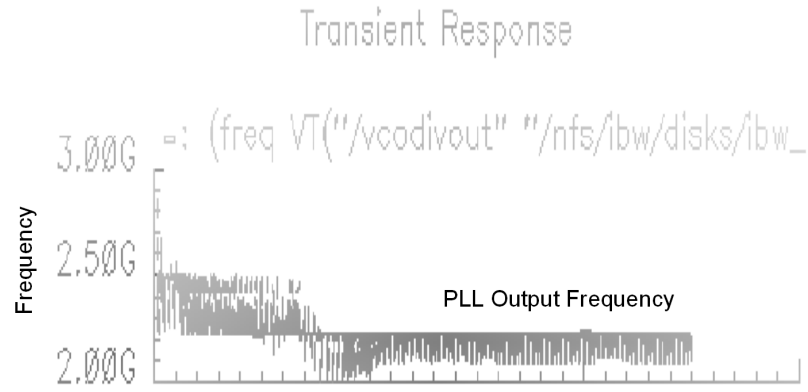
3.2 Non PLL or External Signal Processing

The above mentioned approaches implemented a spread spectrum clock generator by modifying either the forward path or the feedback path of the PLL. Though this is a widely accepted implementation, such a topology is expensive from a power perspective in cases where, the PLL is not necessarily required. There are three problems with the conventional phase locked loop based spread spectrum clock generators, namely :

- on a system level different partitions of the chip might require different spreading. Implementing a separate phase locked loop for each requirement is power and area consuming.
- phase locked loop based SSCG's are difficult to implement as many factors



(a)



(b)

Figure 3.14: Control voltage before and after the summing junction and the bias voltage (controlling the bias current) to the symmetric loads

need to be taken into account.

- decrease of the peak power amplitude (AdB) with random jitter.

A higher clock frequency requires a finer control of the SSC period jitter. If the controller SSC period jitter becomes smaller than the random period jitter, the implementation becomes difficult. In addition the peak power amplitude reduction also decreases [89]. The choice between the PLL and non-PLL based SSCG is highly dependent on the clocking and system specifications. For example, for a system clock in compute platforms, where the source is a CK-505 based chip, it would make more sense to integrate the SSC functionality within the PLL to optimize

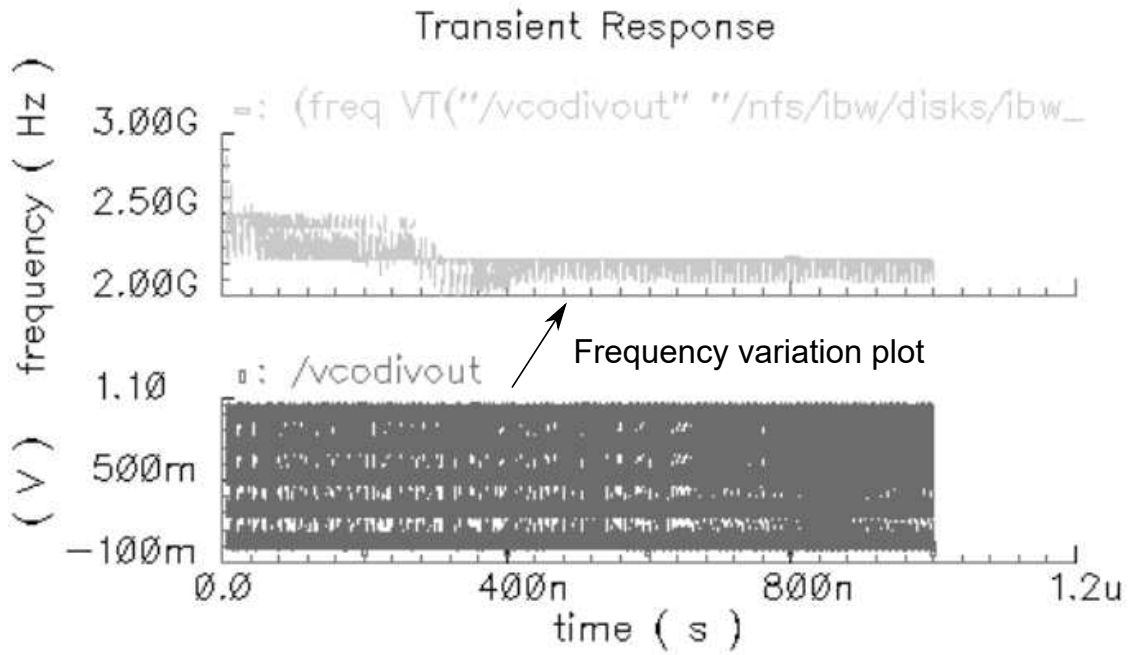


Figure 3.15: Output frequency of the slow modulated SBPLL. No modulation in frequency observed

power/area. However, for a better timing perspective, it might make more sense to have individual SSCG for a display clock (higher spreading as the timing is relaxed) and a dedicated SSCG for microprocessor clock (lower spreading as the timing is very tight).

Multiple implementations have been reported for generating the SSC signal independent of the PLL. Damphouse et.al [90] used a differential delay cell to form a long delay time for generating the delays. The problem for achieving a fine granular delay was tackled by [91] by dividing the delay chains in coarse delay and fine delays. They utilized standard cells for implementation making the implementation relatively portable. [92] proposed utilizing a digitally controlled oscillator to alleviate use of analog design components such as DLL's by controlling the delay in the invertor chain of the DCO. Other variations of the same approach were reported

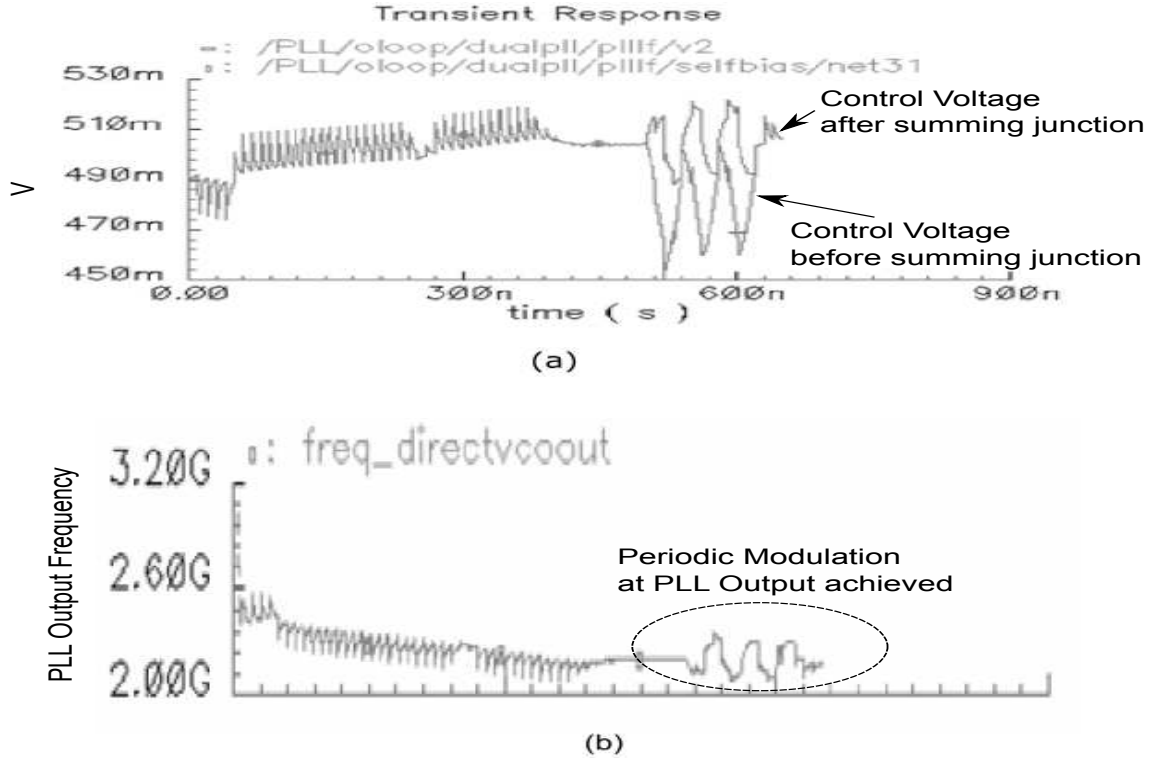
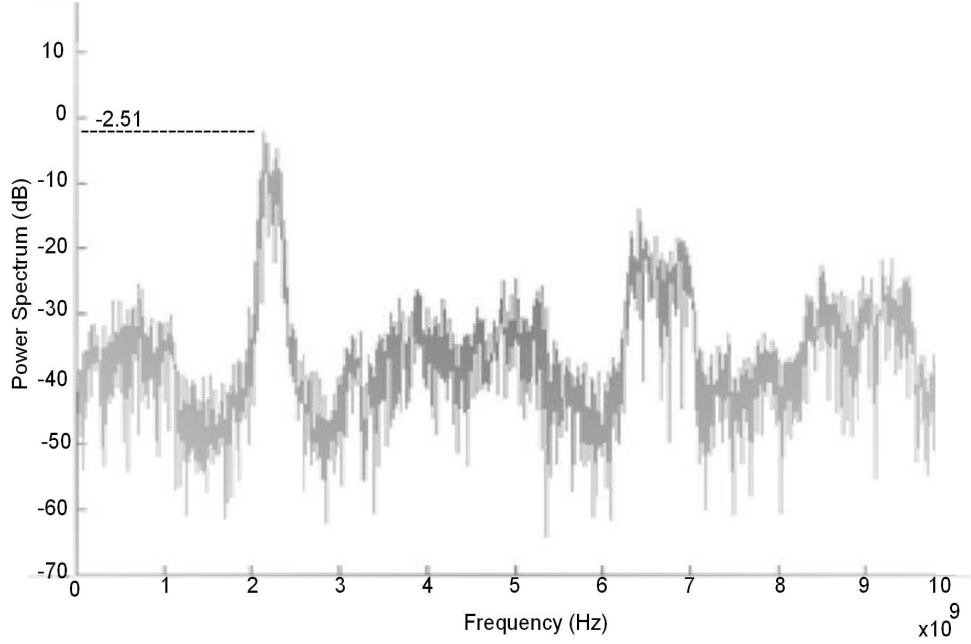


Figure 3.16: SBPLL control voltage before and after the summing junction for a fast triangular modulation profile

in [91][93]. A different approach was utilized in [94][95] called Suppressed Carrier Clock where the SSC is realized by skipping transitions of the regular clock.

We propose an alternative scheme utilizing a delay locked loop and a phase interpolator. The advantage of the scheme is that it allows to control the amount of spread and does not contain any high power VCO. The architecture was modeled using verilog A and a mixed simulation was done. Figure 3.18 depicts an architecture to generate an SSC signal by utilizing a period delay locked loop (DLL), muxes and a phase interpolator (PI) as depicted in figure 3.19. The advantage of utilizing the DLL and PI combination is that it is easier to obtain a lower resolution when compared to a single delay line approach.

The block works at a low frequency, 33 MHz to 133 MHz with a modulation frequency of 32 kHz and thus consumes lower power. Since the block does not contain a



1

Figure 3.17: Frequency Spectrum of Modulated Clock

regulation loop, the jitter profile introduced at the input is equivalent at the output. The block uses a staircase modulation profile where each step corresponds to a frequency change. Each step causes a peak in the frequency spectrum as the maximum energy will concentrate at $\frac{df}{dt} = 0$. It can be calculated that an input frequency of 133 MHz with 5 modulation steps and 0.5% spread would require a resolution of 7.5ps. The higher the number of steps, the finer the resolution required. Multiple phases of an input clock are generated such that the last phase is 360° out of phase (or in phase) with respect to the reference clock. The output clock is formed by selecting the delayed phases at every edge as shown in figure 3.18(a). If we keep on adding a delay of $\Delta 1$ at every rising edge, a new stable time period of $T + \Delta 1$ is achieved. If there is an integer number g such that $gx \Delta 1 = T$, then at g^{th} edge the input clock and the output clock edge will coincide (wrap around). This is shown pictorially in figure 3.18(b) where each dot on the circle represents the change in phase. At the

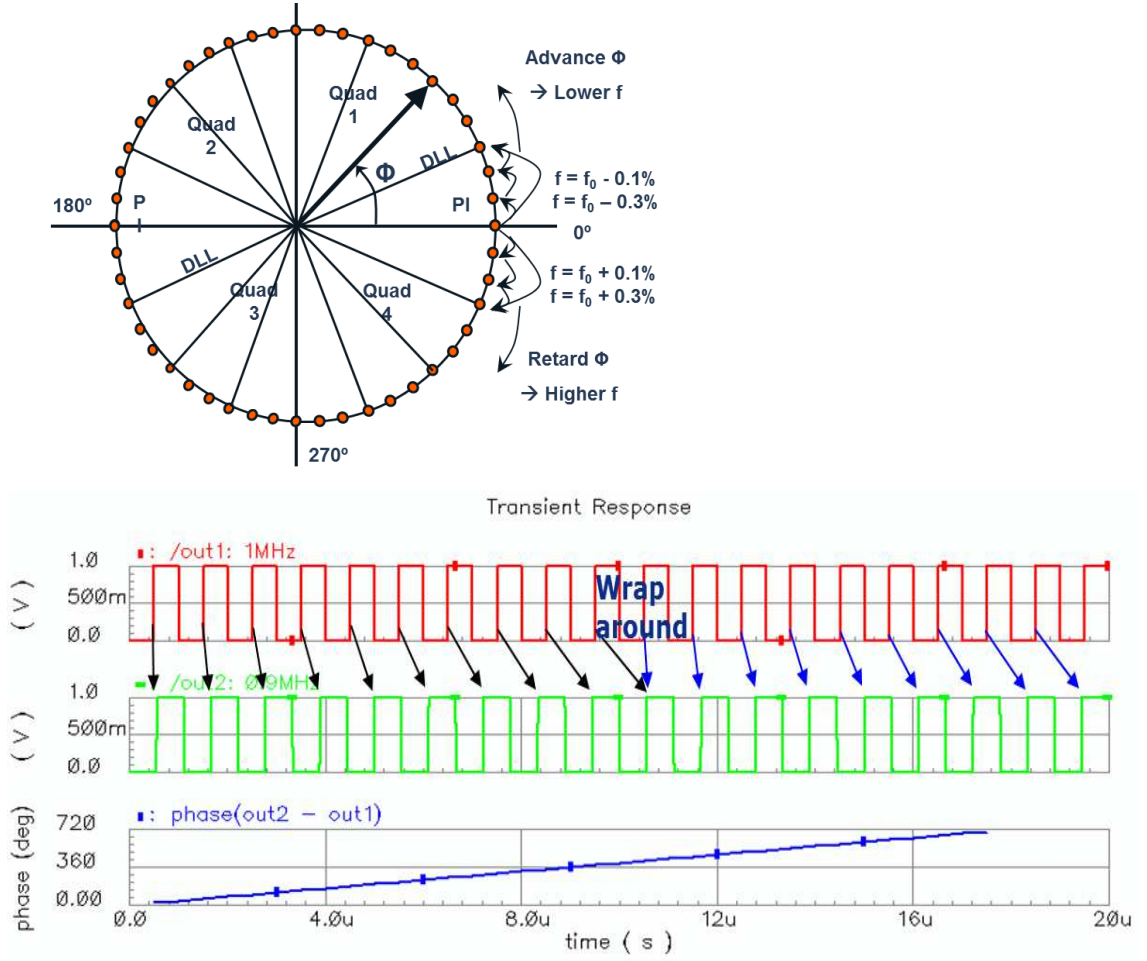


Figure 3.18: (a) Phase circle depicting different steps chosen with regards to various step sizes. (b) Upon one complete rotation, the clock wraps around in phase.

g^{th} edge we complete a full circle. Anti-clock wise rotation corresponds to $a + \Delta$ delay leading to a decrease in frequency while a clockwise rotation corresponds to a $- \Delta$ delay leading to increase in frequency. Thus, by rotating around the phase circle of figure 3.18, and controlling the Δ introduced a new stable frequency is generated.

For generating a different step, different delay steps need to be chosen as depicted in 3.18(a). As the pointer is moved around the circle, phase accumulation occurs as depicted in figure 3.18 (b) and after a 360° turn, the output clocks wrap around.

Thus, by choosing appropriate number of phase steps, a new frequency can be chosen.

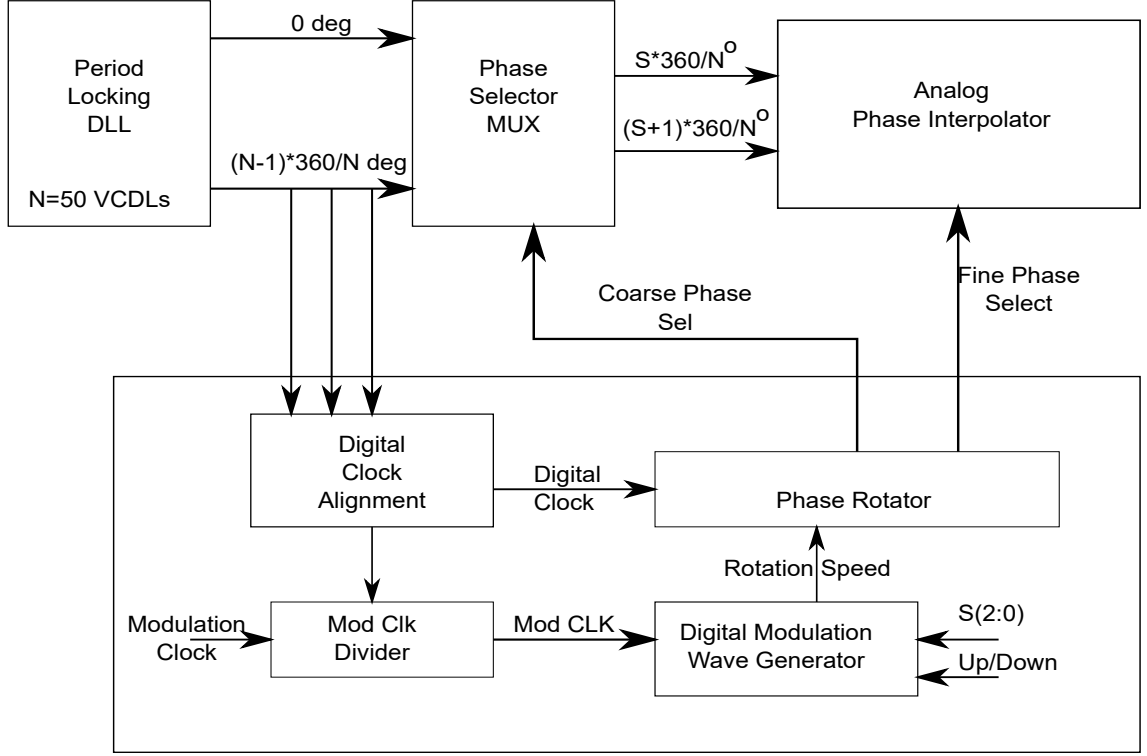


Figure 3.19: Top Level Block Diagram

Figure 3.19 depicts the block diagram of proposed system. A period DLL divides the incoming clock into multiple phases. A phase is selected by the Mux and further divided into finer phase points by the phase interpolator. A 32 KHz clock is utilized to generate the modulation profile. The digital clock alignment block aligns the high frequency clock and the modulation clock. The phase rotator generates the coarse phase select signals which select the DLL outputs and the corresponding fine phase select signals for choosing the phase steps in the phase interpolator. The phase rotator keeps rotating the phase signals according to the modulating profile.

A verilog A model (Appendix 7.3.5) was built to test the concept and simulations. To modulate the incoming clock, a step profile was created by choosing a different number of phases around the circle for different frequency steps. A larger frequency

spread would require more number of frequency steps in the modulation profile. It can be seen in figure 3.20 (a) that for a spread of 0.5% a 6 step modulation profile was utilized. As the phase is rotated, the output clock phase keeps accumulating as depicted in figure 3.20 (b). Figure 3.21 show the power spectral densities (PSD) of the output modulated clock for a 100MHz input unmodulated square pulse clock time domain. It is interesting to note that in case of lower spreads there is an increase in the difference between the peak and the trough. This is due to the decrease in number of steps. As discussed in section 2.8, the frequency spectrum will have a peak corresponding to a step in the modulation profile. Due to the fixed resolution of the delay (7.5 ps) defined by the DLL and the MUX-PI, we have a three step changes (symmetrical spread) for a 0.5% modulation while a 5% modulation has 5 steps. Thus, we have 3 distinct bigger peaks for 0.5% while 5 relatively flatter peaks for the 5% change.

The various blocks can be realised using

- DLL : A period locking DLL based on self bias techniques is proposed as the technique provide a good process matching.
- Phase Interpolator and phase selector mux: It is proposed to use a phase interpolator with a good linearity. The linearity is an important parameter as any non-linearity would cause change in the frequency step leading an incorrect frequency deviation. It is proposed to combine the phase interpolator cell and the switching mux for choosing the appropriate phase of the incoming clock.
- Digital control : It is proposed to synthesize the various digital controller blocks, namely, digital clock alignment, phase rotator, mod clock divider and digital modulation wave generator.

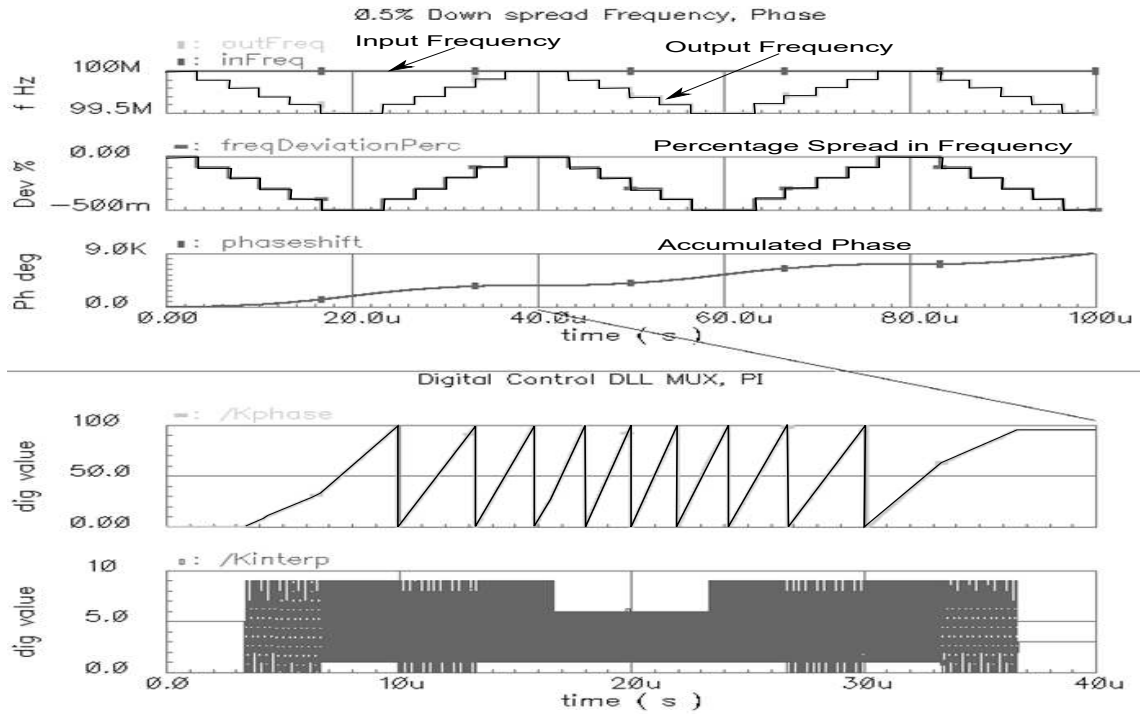


Figure 3.20: Simulation Results depicting the movement of phase as the phase rotator block moves the DLL and Phase Interpolator outputs around the phase circle.

3.3 End of chapter remarks

The current chapter described the investigations that were carried out to define the architecture for lowering the EMI signature of the modulated signal. The PLL approach discussed is power hungry due to high frequency elements. In addition, the PLL impacts the incoming intentional jitter (modulation profile). However, if a low jitter clock is required, integrating SSC generation is a preferable approach.

The non-PLL architecture proposed requires a DLL and a phase interpolator. This is seemingly a low power solution compared to PLL. However, the modulating profile is periodic in nature. It was discussed in 2.4 that the peaks in the power spectrum of the modulated signals can be lowered by utilizing a chaotic modulation profile. It will be hard to implement a chaotic scheme in the proposed DLL+PI approach

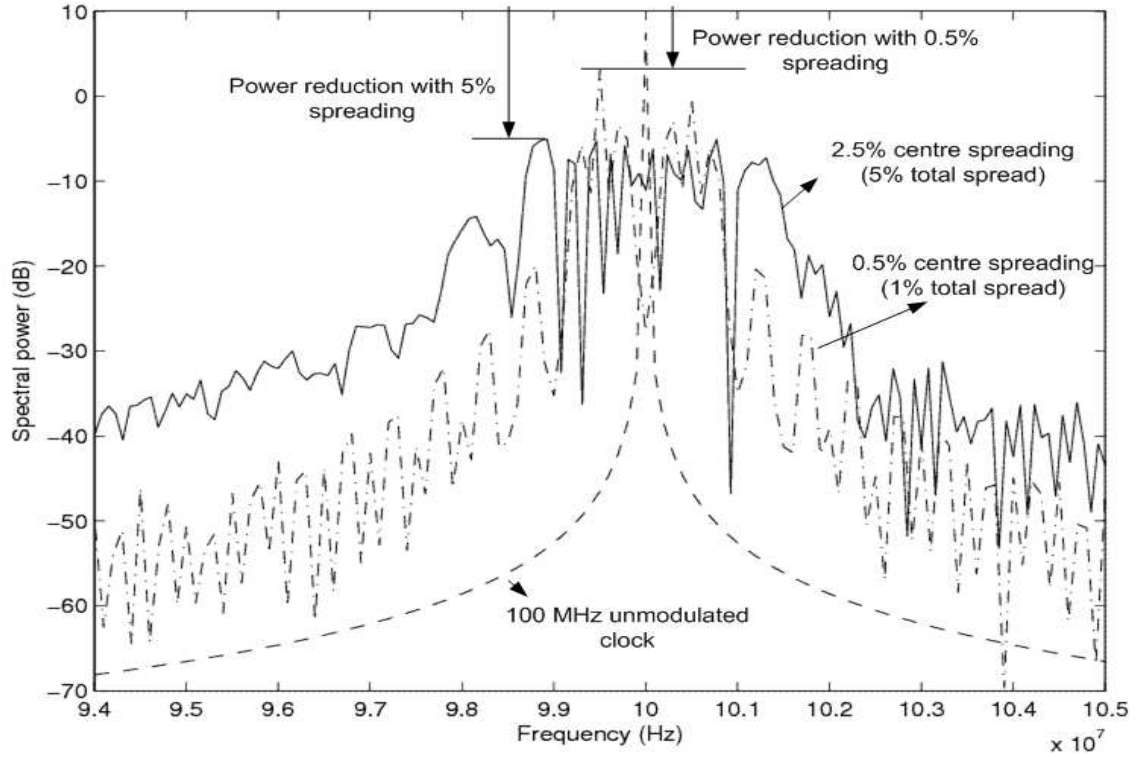


Figure 3.21: Spectral Properties of the modulated SSC clock

as high number of phase points would be required to get random phases for various frequencies. In addition, we would like to encode the data bit stream to be transmitted in the modulated signal to lower the power further (separate clock transmission is not required). A chaotic SSC modulation and a simultaneous data bit encoding would require a very high number of phase steps, requiring a low resolution of the PI.

An alternate architecture has been proposed in chapter 4 to chaotically modulate the clock and encode the bits that need to be transmitted.

4 Non Linear Chaos Based Spread Spectrum Frequency Modulator

DIFFERENT modulation technologies, such as impedance modulation [96], frequency shift keying (FSK) [97] and amplitude shift keying (ASK) [97] have been used for encoding the data stream to be transmitted through a wireless medium from an implanted device. FSK is one of the common modulation schemes in digital communications and it involves sending binary data with a sinusoidal carrier at two distinct frequencies representing logic 1 and logic 0. Consequently, in the frequency domain, the signal power is centred on these two frequencies.

The previous chapters introduced architectures utilizing periodic modulation profiles for modulating the generated clock. As discussed earlier, the non-PLL approach is advantageous in scenarios where a high power consuming VCO is not needed [98]. Signals produced by chaotic systems are typically aperiodic and broadband thereby spreading the energy more efficiently in contrast to concentrating them at multiples of periodicity as in the case of conventional periodic modulation profiles such as the Hershey Kiss profile [99]. Recently, there has been an interest in utilizing the chaotic modulation to lower the EMI. The current reported publications have utilized the fractional N approach [100], [101]. As discussed, fractional-N PLL based

architectures suffer from bandwidth limitations. This chapter proposes a novel approach based on utilizing a chaotic signal [102], [103] for modulating the encoded signal. The current chapter proposes a non-PLL modulator to efficiently transfer the encoded signal to the receiver through a FM technique.

The block proposed in this thesis provides several advantages over phase locked loop approaches using periodic modulation profiles, namely:

- Firstly, as mentioned it uses a chaotic modulation profile thereby achieving a lower peak spectral power.
- Secondly, the block does not use a regulation path in the clock generation in contrast to the conventional PLL based SSC designs [13]. Thus, the jitter profile is same as the modulating signal profile.
- Thirdly, for additional flexibility blocks can be connected after a PLL to cater to different spread requirements on the platform without the need of having multiple PLL's.

The circuit has been simulated and fabricated in $0.18\mu m$ technology. Section 4.1 discusses the algorithm utilized to encode the neural data stream. Section 4.3 describes the circuit realization of the block and the simulation results in a $0.18\mu m$ technology.

4.1 Algorithm

Figure 4.1 depicts the algorithm utilized for encoding the incoming bit stream into a frequency modulated signal. Two 180° out of phase ramps are generated. The ramp waveforms are compared against a reference signal and an edge is produced at the intersection point. The frequency of the modulated signal can be varied by

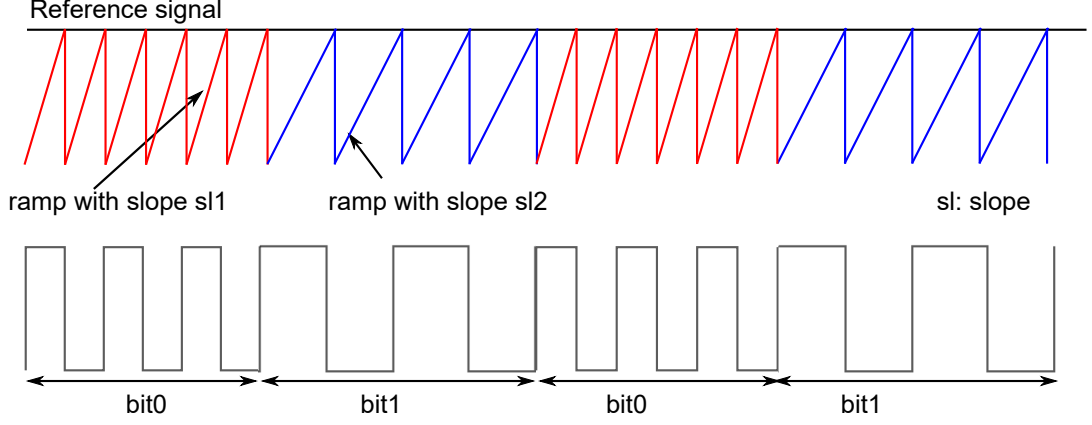


Figure 4.1: Generation of modulated signal edges by comparing a ramp with a reference signal. The slope of the ramp determine the frequency of resultant encoded signal.

varying the gradient of the ramp. Two ramps are utilized to compensate for error resulting due to the finite time it takes for the ramp to discharge. As illustrated in figure 4.1, the gradient of the ramp is chosen based on the incoming bit. Thus, two distinct frequencies are created to represent logic ‘zero’, f_{space} and logic ‘one’, f_{mark} .

To reduce the peak of the PSD’s of the two frequencies, both are modulated around the two central frequencies f_{space} and f_{mark} . Figure 4.2 depicts the algorithm for a wideband chaotic modulation of the encoded modulated signal around its base frequency. Similar to figure 4.1, an edge is produced at the intersection of the reference voltage and the ramp. However, in this case the frequency of the modulated clock is changed by changing the value of the reference voltage rather than the gradient. The reference voltage value is changed chaotically around the base value corresponding to the chosen frequency for f_{space} and f_{mark} . Other modulation profiles can also be used to modulate the encoded signal.

The chaotic noise is a continuous voltage signal with random voltage levels and is generated by the chaotic sequence generator. For the current work, a tent map

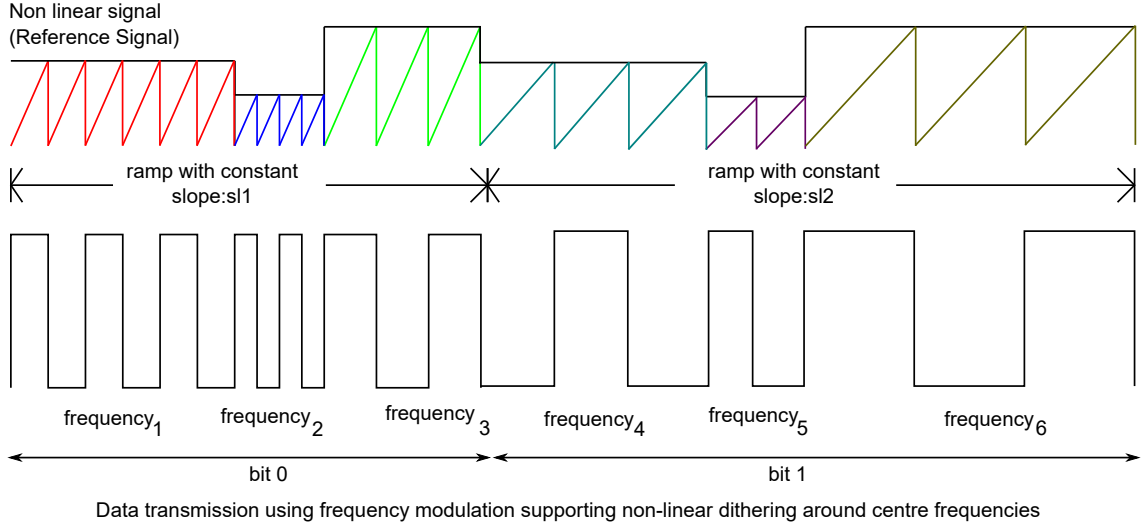


Figure 4.2: Chaotic dithering of the encoded signal by comparing the two ramps with the chaotic signal.

function (equation 4.1) has been utilized to generate the chaotic sequence:

$$\begin{aligned}
 x_{k+1} &= 2 \cdot x_k & x_k > V_b \\
 x_{k+1} &= 2 \cdot (2V_b - x_k) & x_k < V_b
 \end{aligned} \tag{4.1}$$

It is important to note that the data is encoded by changing the gradient of the ramp while the SSC dithering is done by varying the reference level. The gradient of the ramp is controlled using a charge pump (section 4.3.2.1) while the reference voltage is controlled using a chaotic generator (section 4.3.1). The same algorithm can be used for generating a periodic modulated signal as well, by varying the reference signal periodically.

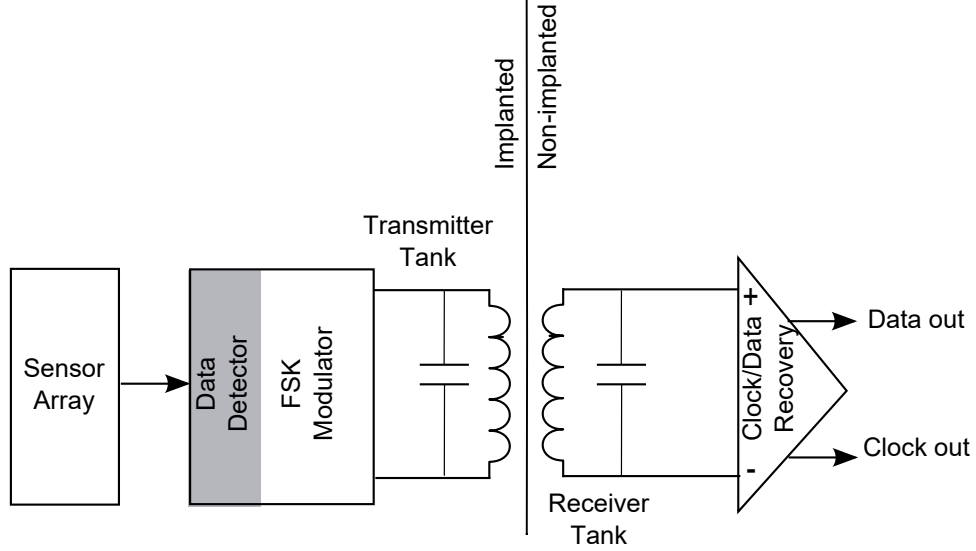


Figure 4.3: Frequency shift keying based telemetry system

4.2 System Level Description

Figure 4.3 depicts the main components of the complete system. The sensor array comprises of neural sensors [104] followed by an A/D converter and a neural amplifier [105]. The amplified signal is encoded as a pattern of one's or zeros. The encoded data stream is passed on to the FSK modulator which performs FSK modulation to transmit the information to the external receiver. The external receiver is formed by a conventional clock recovery circuit and data processing circuitry.

The current work concentrates on the FSK modulator as depicted in figure 4.4. The FSK modulator for the current work is referred to as the Non-Linear FSK Modulator (NLM) as chaos is used to further modulate the two encoded frequencies. The NLM comprises two parts, namely, the chaotic signal generator and the frequency modulator.

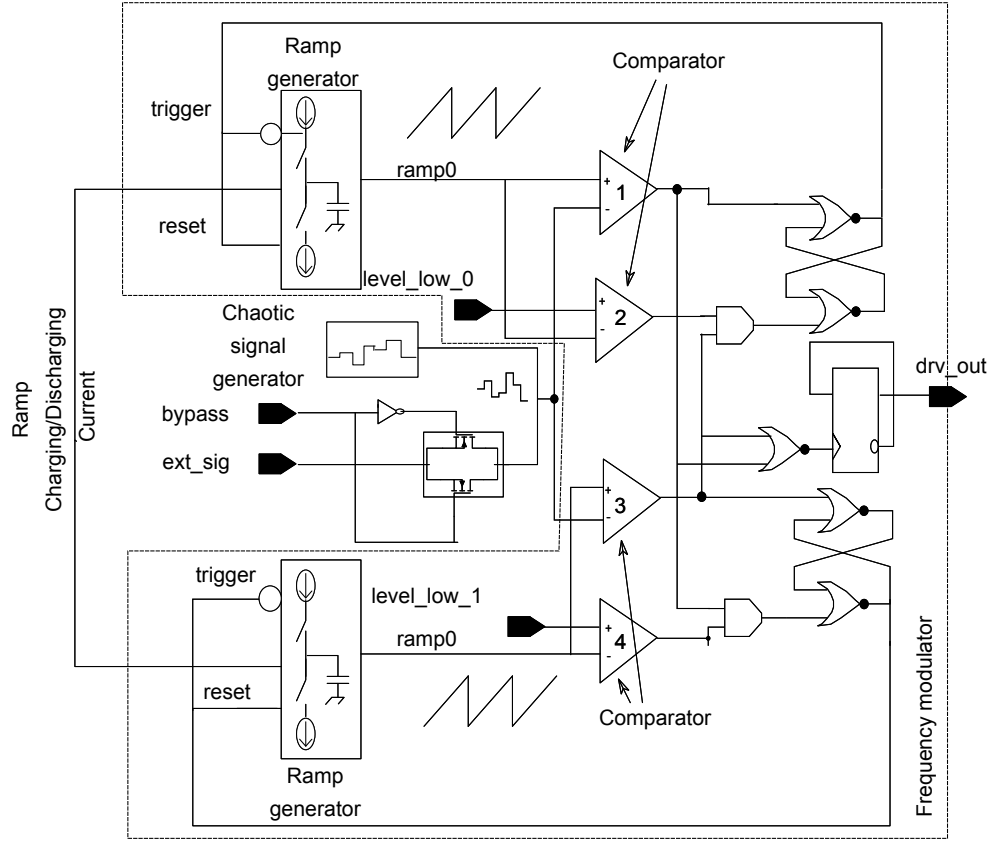


Figure 4.4: Block diagram of the chaotic spread spectrum clock generator.

4.3 Circuit Architecture

Figure 4.4 depicts the block diagram of the proposed chaotic SSC generator.

It comprises two major blocks,

1. The chaotic signal generator: The chaotic noise generator implements a tent map function described in section 4.3.1
2. The frequency modulator: The frequency modulator circuit generates the modulated signal stream depending upon the incoming bit stream (encoded using the gradient) and reference signal level (either generated using the chaotic signal generator or fed externally).
 - a) The ramp generator: The ramp generator generates two ramps, each

equal to the high and the low pulse width of the reference clock discussed in section 4.3.2.1.

- b) The comparator: The comparator compares the reference signal (chaotic noise) and the ramp to generate the modulated edge of the clock.
- c) The RS latch and edge logic: Based on the comparator output, the edge logic generates the ‘set’ and ‘reset’ signals. The RS latch generates the output clock. The ‘reset’ is tied to the lower path and generates the negative edge. The ‘set’ is tied to the upper path and generates the positive edge discussed in section 4.3.2.2.

The following sections describe the above blocks in details.

4.3.1 Chaotic Signal Generator

The current work uses a tent map transfer function (equation 4.2) [72] to model the chaotic transfer function (M). For the current thesis, $V_b = 0.5V$, $V_{high}=2V_b=1V$. The advantage of the tent map is that the transfer function has only two quadrants and therefore makes the implementation simple.

$$\begin{cases} V(x_{n+1}) = 2V(x_n) & V(x_n) < V_b \\ V(x_{n+1}) = 2(2V_b - V(x_n)) & V(x_n) \geq V_b \end{cases} \quad (4.2)$$

Even though the current work utilizes a tent map function, any other map [100] could also have been chosen provided that it was chaotic and within bounds. Figure 4.5 illustrates the block diagram of the chaotic signal generator.

- The voltage comparator compares $V(x_n)$ with V_b .
- The voltage subtractor computes $V_{high} - V(x_n)$, where V_{high} is $2V_b$.

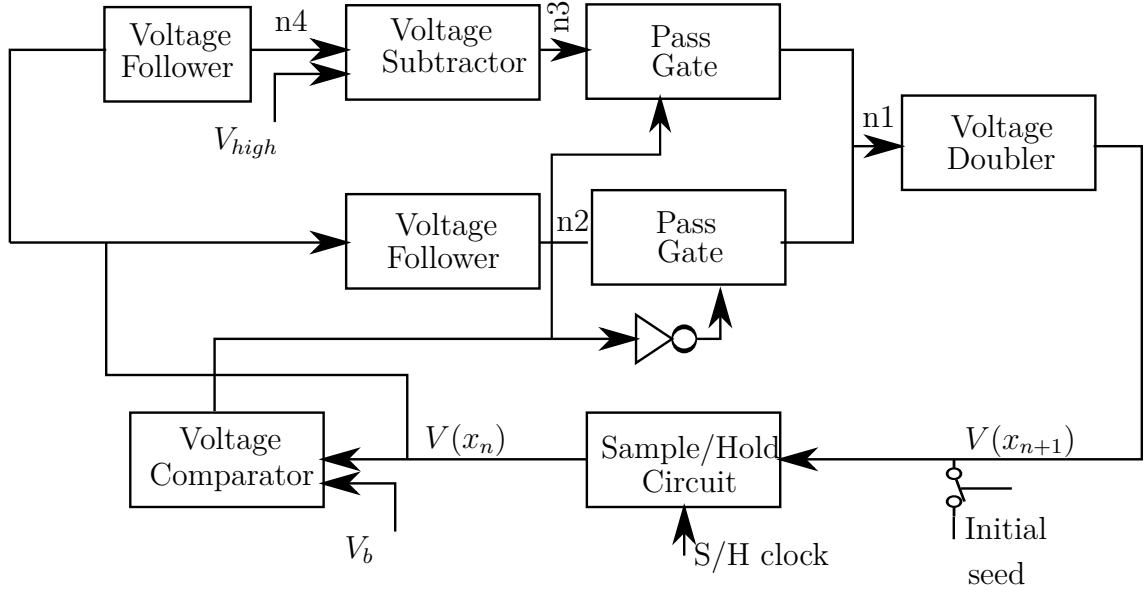


Figure 4.5: Block diagram of nonlinear (chaos-tent map) signal generator

- The voltage doubler either computes either $2V_b$ or $2(V_{high} - V(x_n))$ depending upon whether $V(x_n) < V_b$ or $V(x_n) \geq V_b$ respectively. The output of the voltage doubler circuit forms the chaotic signal, x_{n+1} .
- The sample and hold circuit samples the chaotic signal x_{n+1} and passes the sampled value x_n to the voltage comparator for the next iteration.

The analogue mathematical operators were designed utilizing standard operational amplifier topologies. Figure 4.6 depicts the op-amp [106] utilized for the current design. The operation amplifier was based on the analogue cell library available in AMS design kit. R_{bias} generates the biasing current. The biasing current is transported to the input tail current stage through a current mirror. Transistors TP_3 , TP_5 , TP_{12} , TN_{13} and TN_2 bias the various internal lines in power down mode. Table 4.1 gives the sizing of the various critical transistors.

Since a resistive biasing has been utilized, the biasing current varies across corners by around 16% due to the change in resistance as can be seen in figure 4.7. The variation in the current across corners is not an issue as it was ensured during the

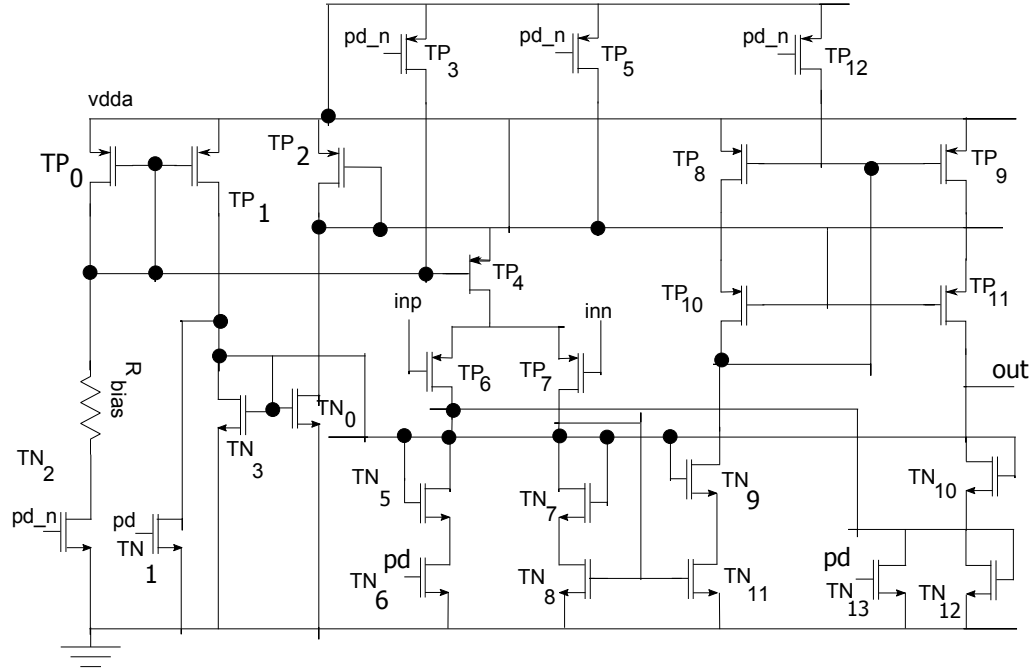


Figure 4.6: Operational amplifier

Table 4.1: Two stage operational amplifier sizing

Element	Width	Length	Number of instances
TP_0	4μ	5μ	1
TP_1	2μ	5μ	1
TN_0, TN_3	1μ	8μ	1
TN_2	1μ	1μ	1
TP_2	1μ	3.5μ	1
TP_6, TP_7	2.5μ	$180n$	9
TN_5, TN_7	2.5μ	1μ	1
TN_6, TN_8	$\frac{5\mu}{2\mu}$	2μ	1
TP_4	4μ	5μ	1
$TP_8, TP_9, TN_{11}, TN_{12}$	5μ	2μ	$TP_9 = TN_{12} = 4$
$TP_{10}, TP_{11}, TN_9, TN_{10}$	2.5μ	1μ	$TP_{11} = TN_{10} = 4$
R_{bias}	234787 ohms		

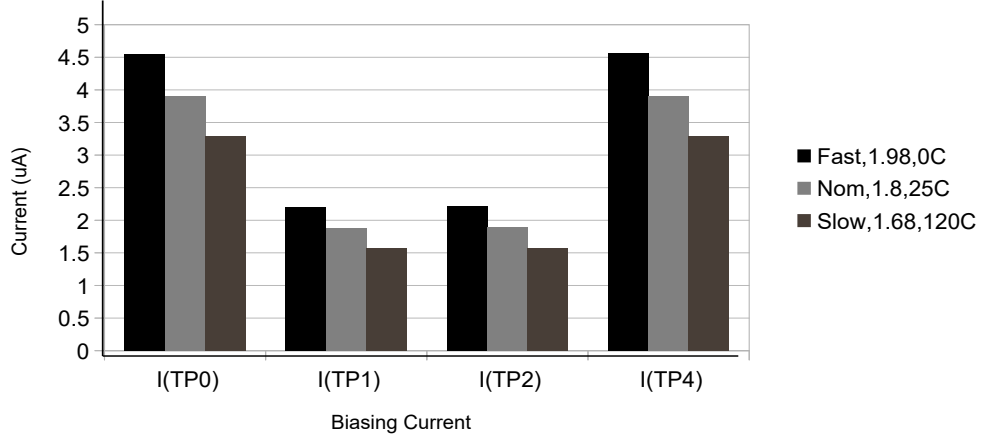


Figure 4.7: Two stage op amp biasing currents

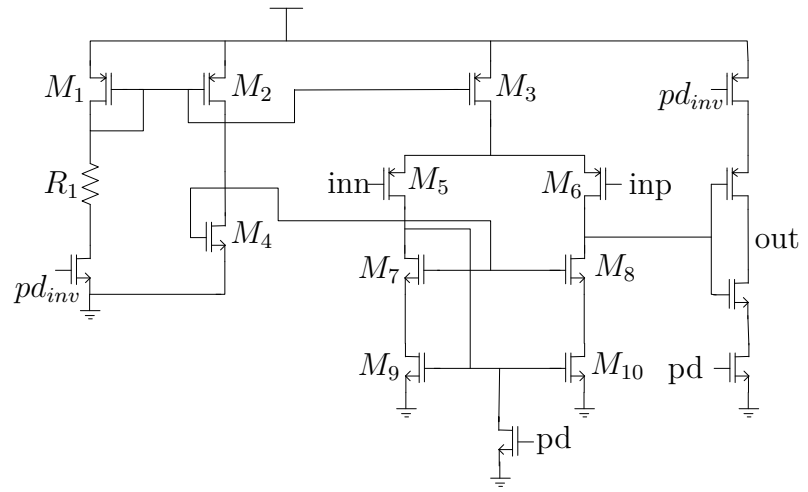
Table 4.2: DC offset across corners

	fast,1.98V,0C	nominal,1.8V,25C	slow,1.62V,100C
Offset (V)	1mV	18mV	9mV

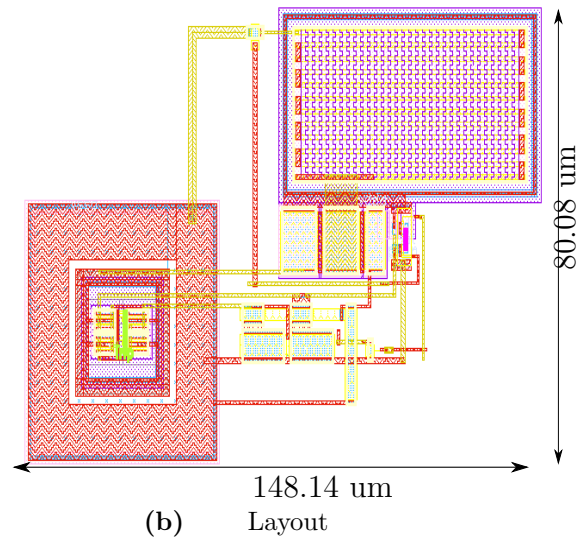
design that the transistors remain biased in saturation region.

A two stage comparator was implemented as shown in figure 4.8 (a). Figure 4.9 shows the DC simulation results for the comparator. Since the comparator is utilized to make a decision for the next iterative value, a finite offset leads to a finite delay. Any mismatch between compataor1 and comparator2 (figure 4.5) would lead to duty cycle error. Table 4.2 lists the offset in the comparator across various corners. A possible improvement to the existing circuit to calibrate for nullifying the input referred offset in the comparator and the operational amplifier before transmitting the data.

A differential amplifier was used to build the ‘subtractor’ as shown in figure 4.10 (a). For the current work, $R \approx 235K$ and a compensation capacitance of 10.22 pF were implemented on die. Thus the transfer function is given by $V_{out} = V_{pos} - V_{neg}$. The resistors were placed symmetrically as illustrated in 4.10 (b). A guard ring was



(a) Schematic



(b) Layout

Figure 4.8: Comparator

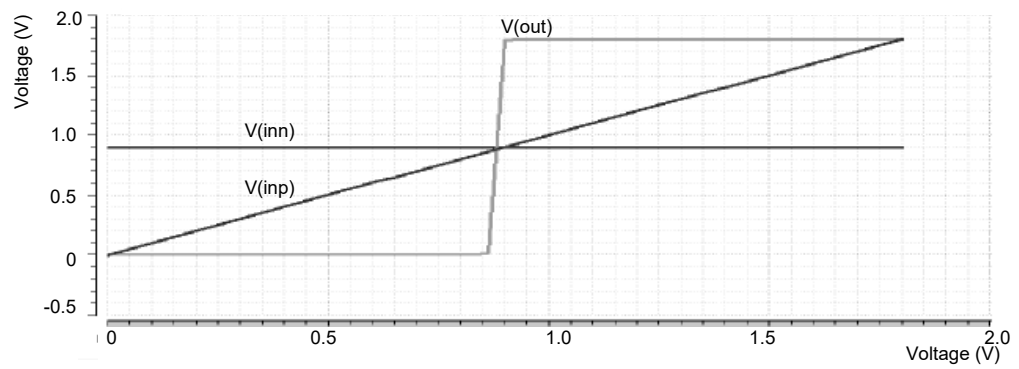


Figure 4.9: Results of dc simulation on voltage comparator

placed around the capacitance to minimise coupling cap to adjacent nets. Figure 4.10 shows a DC simulation run across corners. Since $V_b = 1V$, DC simulations were run with the positive node ($V_{pos} = 1V$). It can be seen that the subtractor works as expected.

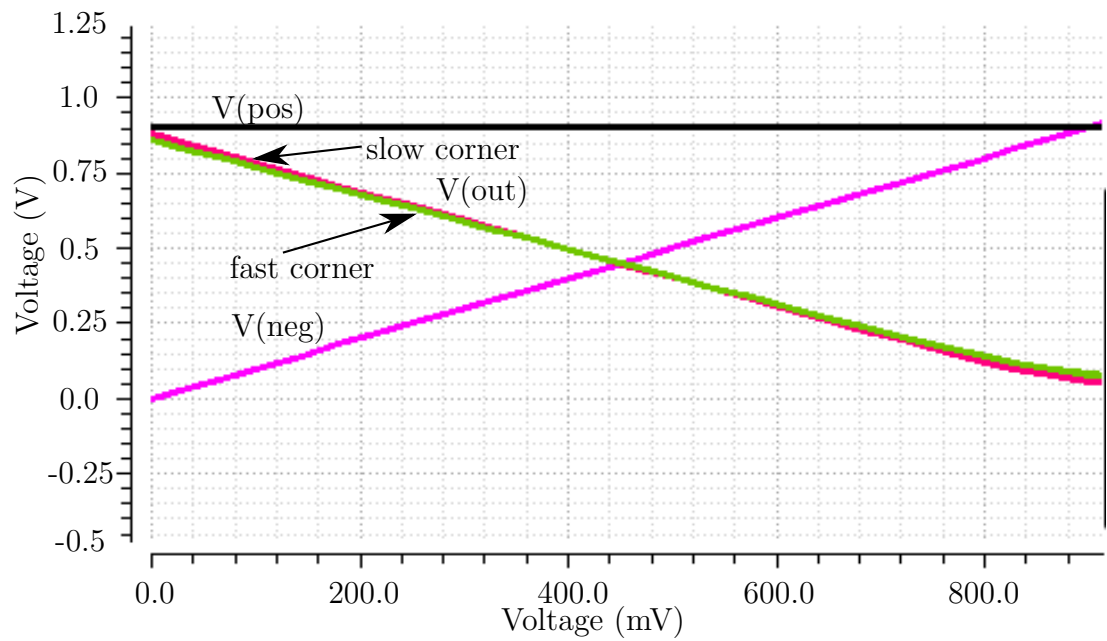
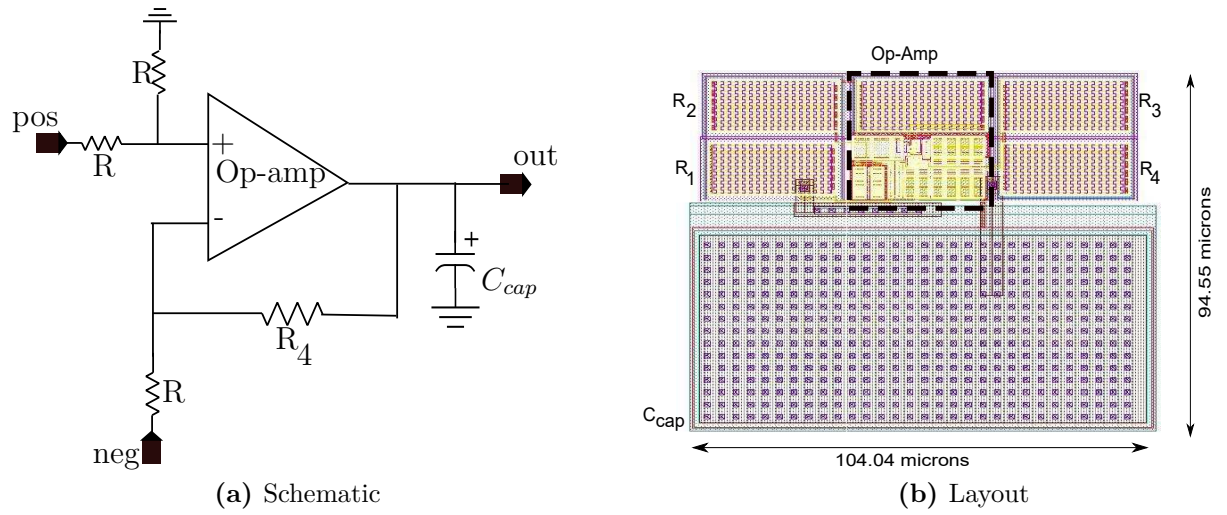
A standard op-amp based voltage doubler circuit topology was implemented as depicted in figure 4.11. The operational amplifier starts saturating around 0.9V. This is not an issue as the voltage doubler operating region is in first half of the tent map. Figure 4.12 shows the dc simulation results for the voltage doubler. The output of the voltage doubler forms the signal, $V(x_{n+1})$.

The resulting signal is then sampled using sample and hold (S/H) topology. One of the problems arising in S/H circuit as illustrated in figure 4.13, was charge sharing between sample/hold phases and the leakage path through the low impedance nodes of the sampling switches. To take care of charge sharing between sample/hold phases, the input and output nodes were isolated during the sample and hold periods as shown in figure 4.14. As shown, during one phase PG_2/PG_3 are enabled while in the next phase PG_1/PG_4 are enabled. Thus, while C_1 samples $V(x_{n+1})$, the charge sampled in the previous cycles is held and passed to $V(x_n)$.

To avoid the hold capacitors from discharging due to the low impedance node of the following stage, a high impedance node was created by inserting voltage followers (figure 4.15 (a)) at the output node of the S/H circuit (figure 4.5). The output node of the unity gain amplifier follows the input node in the region of interest as depicted in figure 4.15 (c).

Figure 4.16 shows a zoomed version of the S/H simulation. It can be seen that the output of the S/H circuit follows well the sampled value quite well.

Figure 4.17 depicts the layout of the chaotic generator. Guard rings were created around the sensitive differential pairs of the op-amps. The S/H circuit was placed



(c) DC simulations across corners.

Figure 4.10: Voltage subtractor

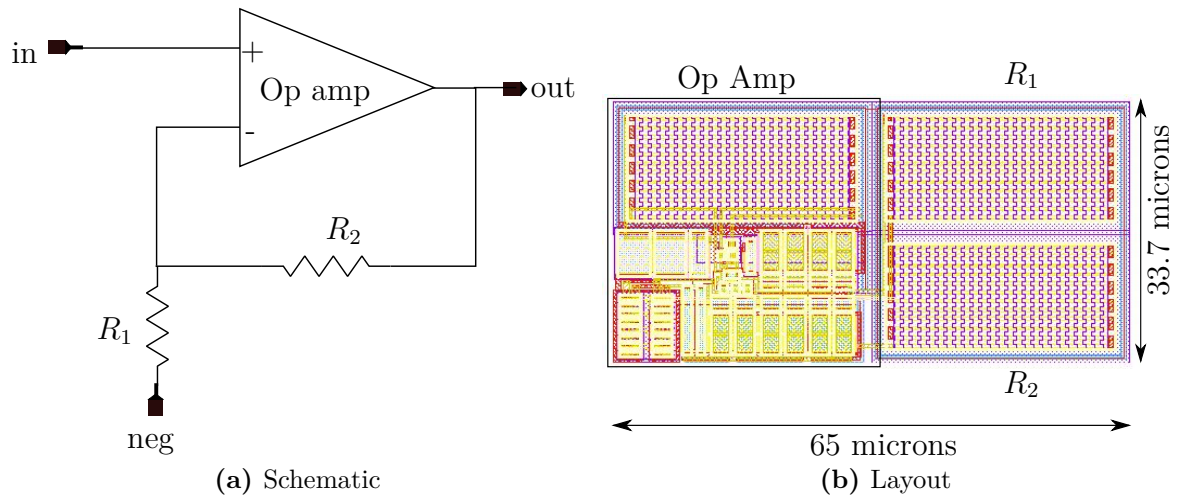


Figure 4.11: Voltage doubler schematic and layout

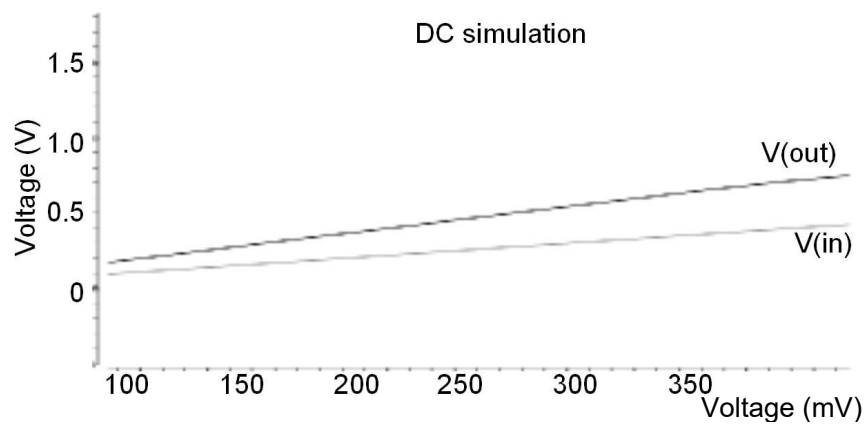


Figure 4.12: Results of dc simulation on voltage doubler

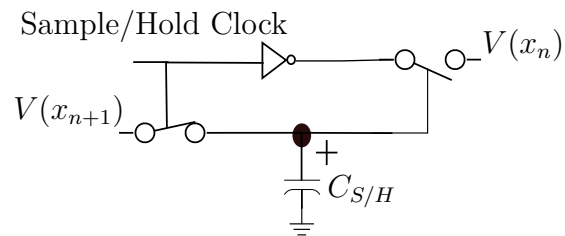
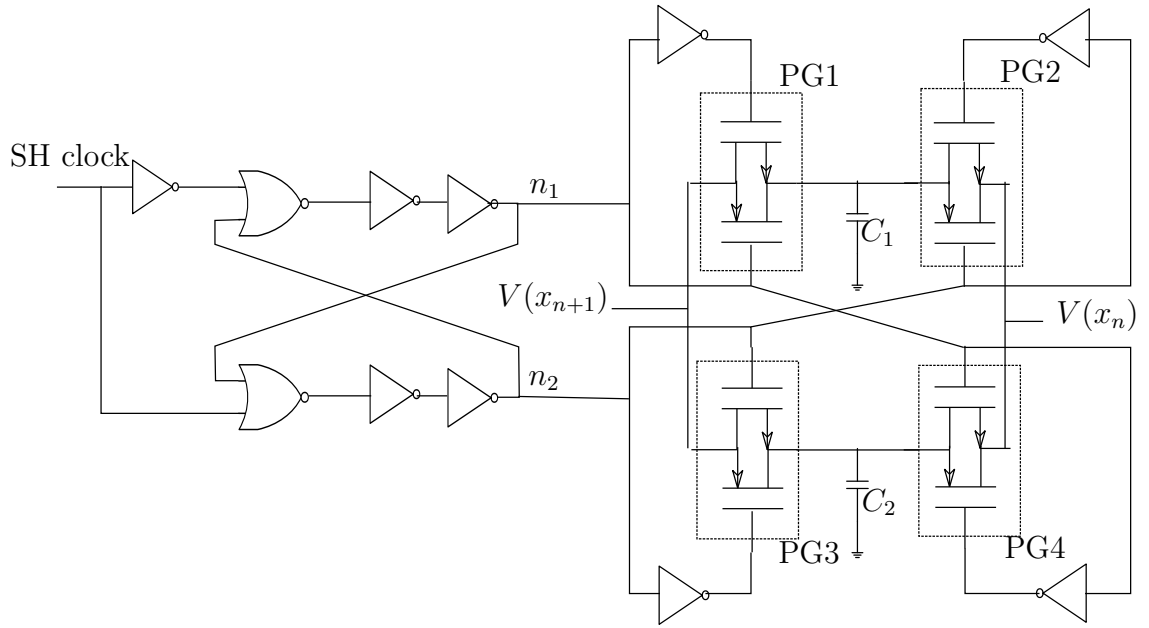
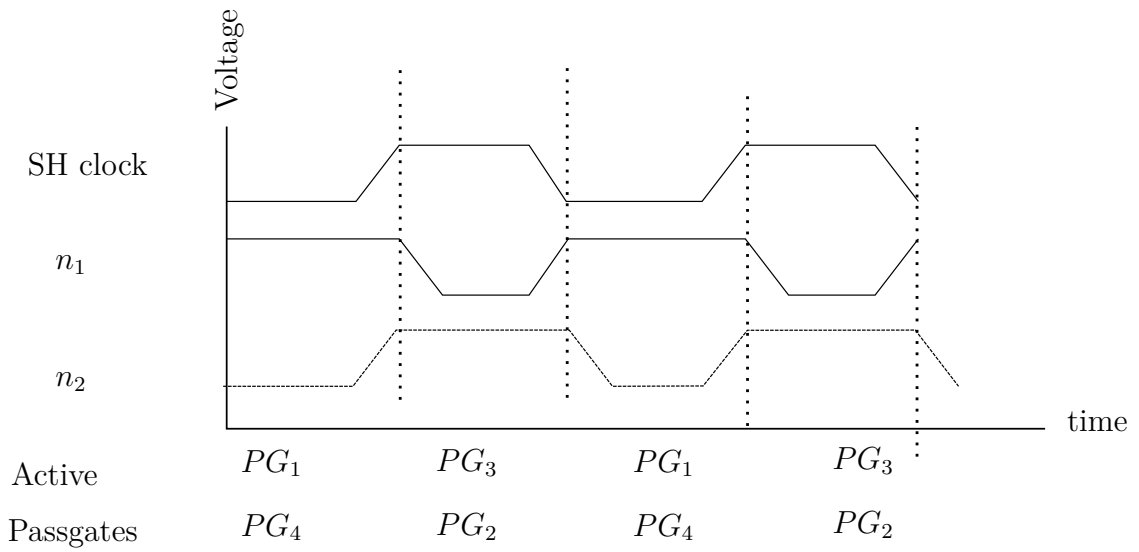


Figure 4.13: Sample and hold circuit

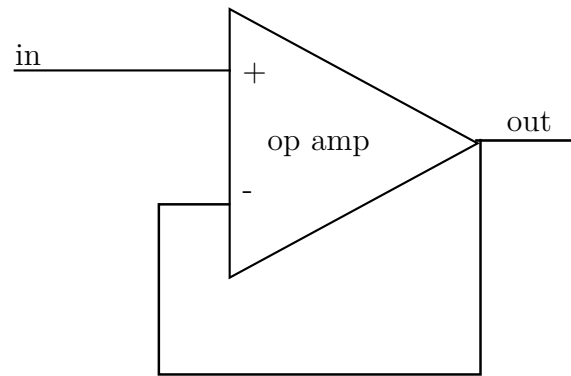


(a) Schematic of proposed SH circuit

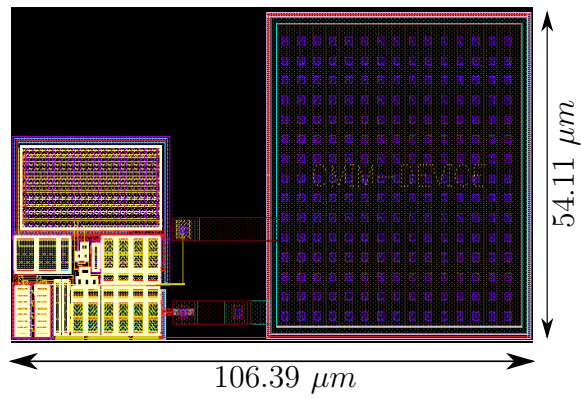


(b) Timing diagram

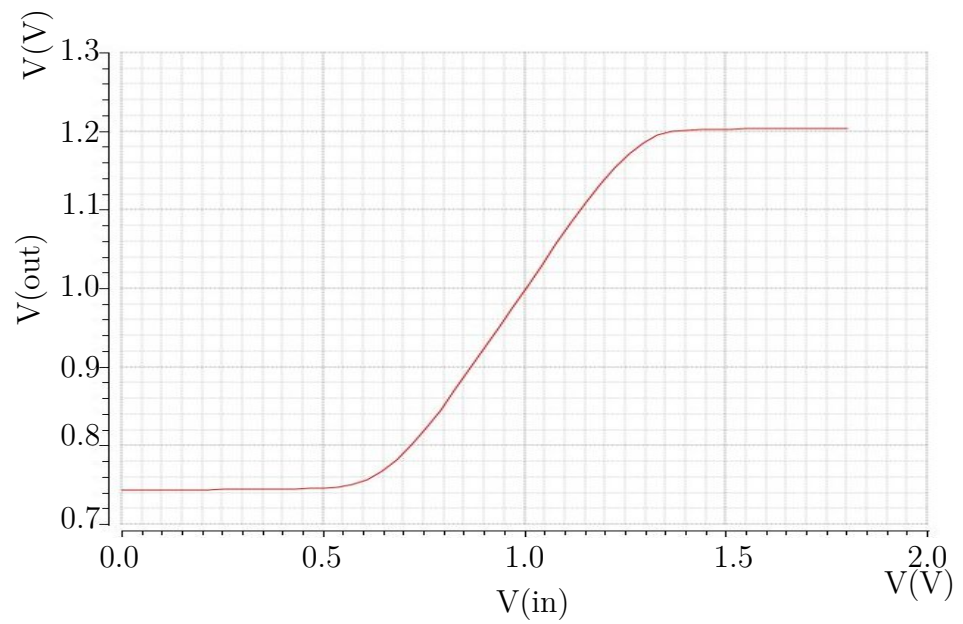
Figure 4.14: Sample and hold circuit with associated timing diagram



(a) Schematic



(b) Layout



(c) DC simulations results

Figure 4.15: Voltage follower

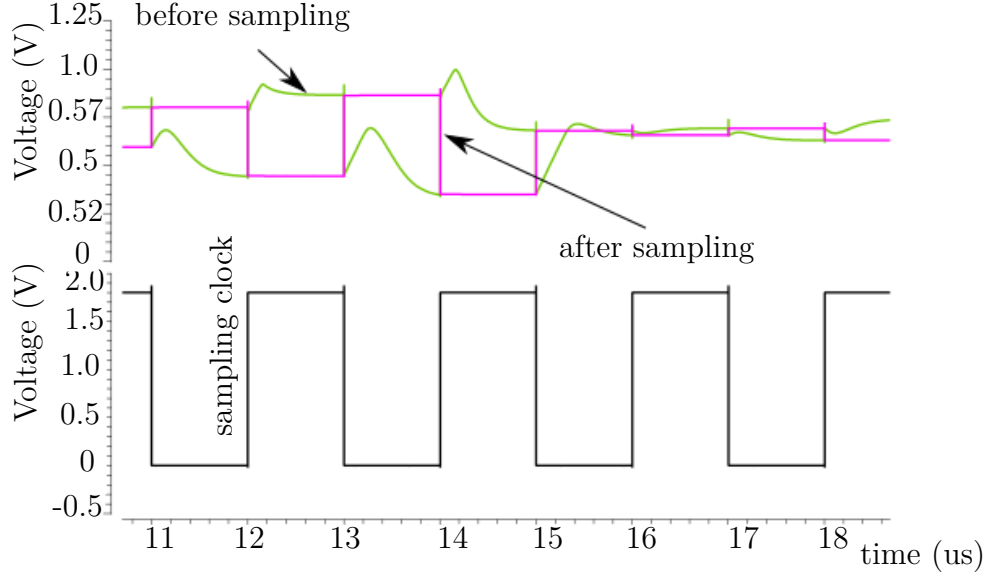


Figure 4.16: Output for sample and hold circuit

away from the switching circuit to minimize any noise coupling to the sampled signal. The unity gain amplifiers were placed close to the intended high impedance nodes.

The layout was extracted using Caliber and extracted simulations were run on the tent map circuit. The circuit was tested using $V_b = 500mV$ and multiple initial conditions. The observed output ($50.14mV \rightarrow 100.3mV \rightarrow 200.6mV \rightarrow 38.07mV$) can be seen in line with the transfer function. As can be seen in figure 4.18 (b) the PDF of the chaotic signal is uniform. The tent map was allowed to run for $600\mu s$. Due to an unstable equilibrium at $x_k = \frac{4V_b}{3}$, the PDF will contain peak at that value. Instability means that if x_k is in the vicinity of $\frac{4V_b}{3}$, the following iterations will slowly diverge from the value. Figure 4.19 (b) illustrates the chaotic signal in vicinity of the equilibrium point. It can be observed that the signal slowly diverges away from $667mV$. Figure 4.19 (a) shows the top level chaotic signal generator. Transient simulations were run and have been shown in figure 4.19 (b).

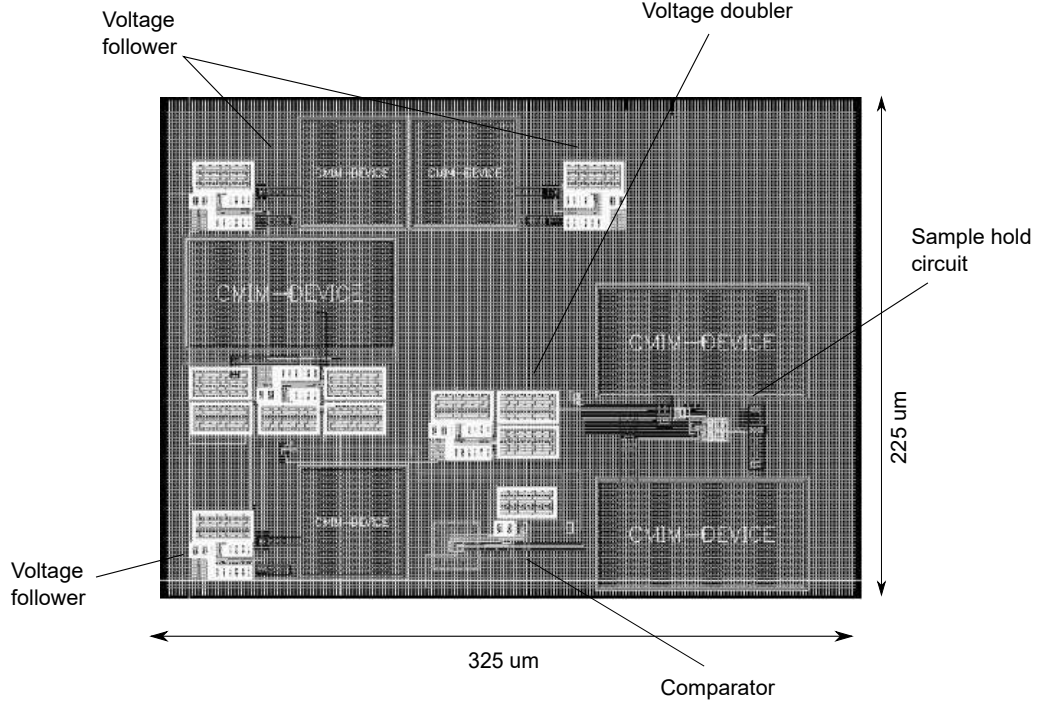


Figure 4.17: Chaos Generator Layout

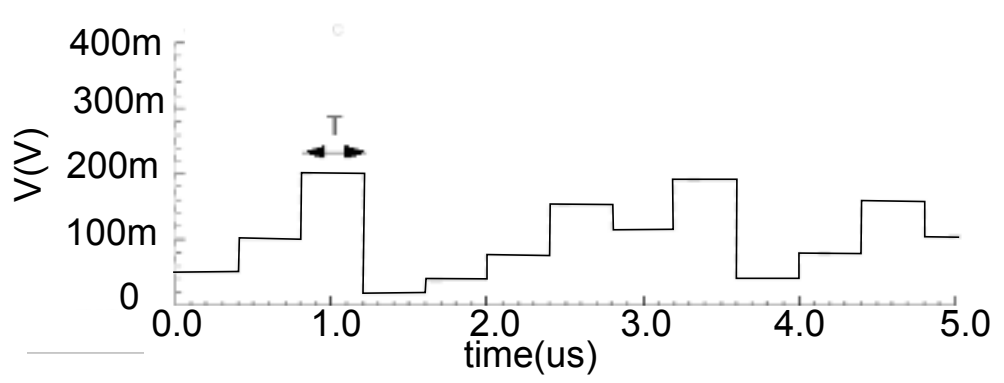
4.3.2 Frequency Modulator

The frequency modulation circuit generates the modulated signal stream depending upon the incoming bit stream (encoded using the gradient) and reference signal level (either generated using the chaotic signal generator or fed externally).

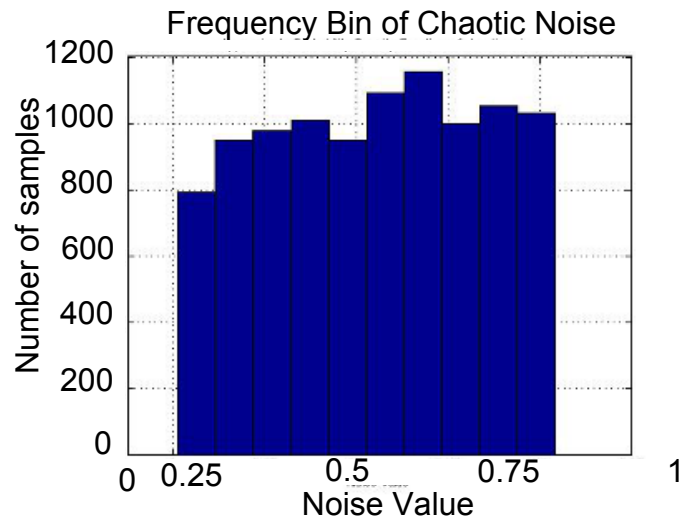
4.3.2.1 Saw Tooth Generator

A conventional single ended charge pump topology [107], [108] was utilized for generating the ramps as illustrated in figure 4.20. The ramp is created by either charging or discharging the load capacitor. The gradient of the ramp is given by

$$m_{gradient} = \frac{dV}{dt} = \frac{i_{(charging,discharging)}}{C_{cap}} \quad (4.3)$$

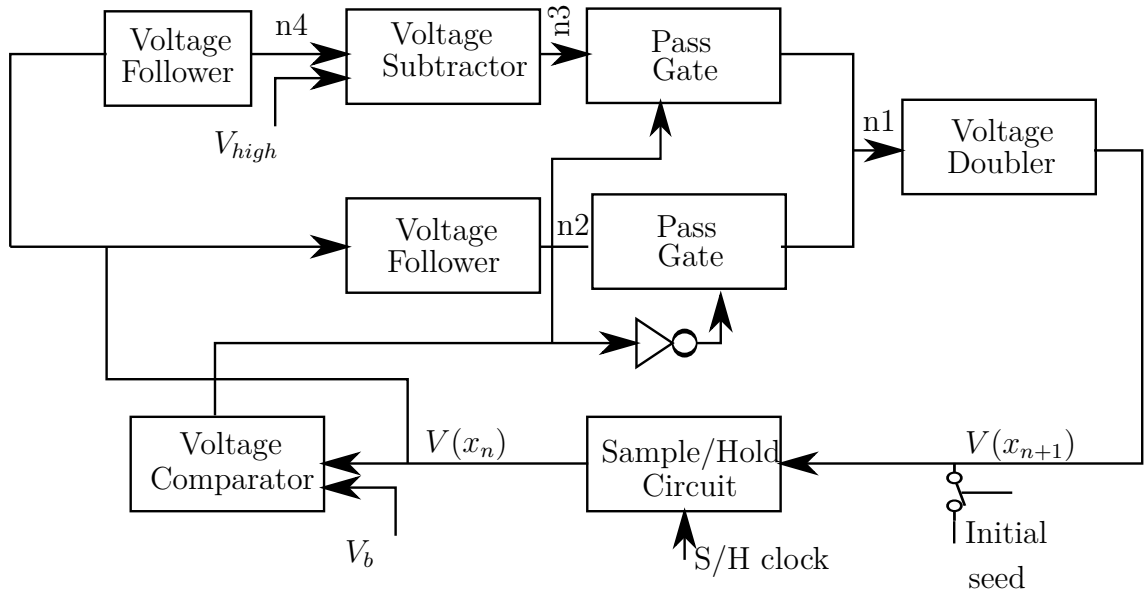


(a) Transient simulations with the chaotic signal probed

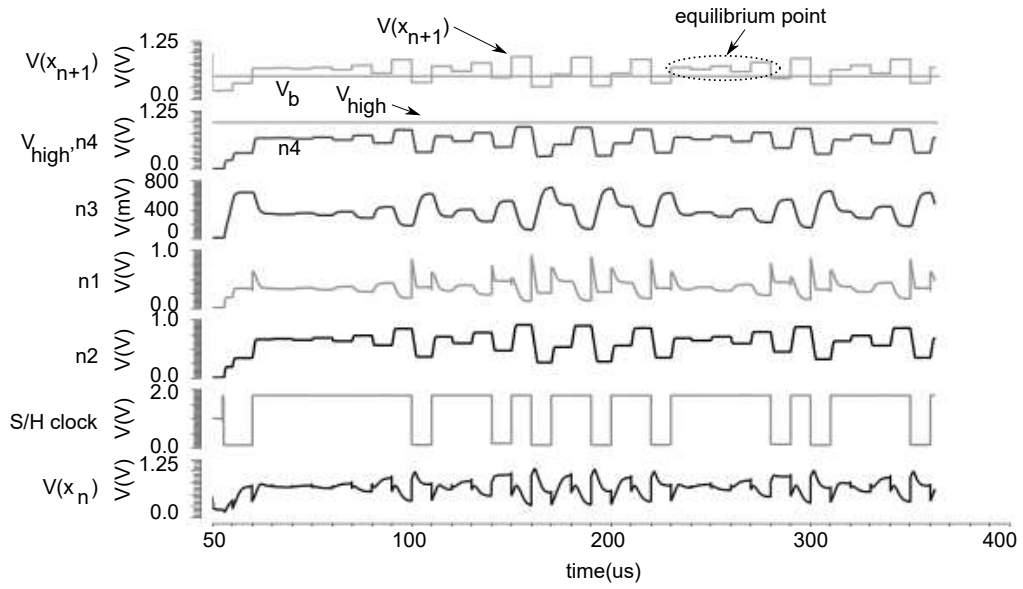


(b) PDF of the chaotic signal

Figure 4.18: Tent Map Perturbations (a) transient simulations with the chaotic signal probed (b) PDF of the chaotic signal



(a) Schematic with the various nodes labelled



(b) Transient simulation results

Figure 4.19: Chaos generator

Table 4.3: Transistor Sizing of the Saw Tooth Generator

Transistor	Transistor Type	Width(m)/Length(m)	Multiplication factor
M_1	p MOSFET	$20\mu/5\mu$	$<3:0>$
M_2	p MOSFET	$20\mu/5\mu$	$<1:0>$
M_3	p MOSFET	$10\mu/180n$	1
M_4	p MOSFET	$10\mu/180n$	1
M_5	n MOSFET	$40\mu/180n$	1
M_6	n MOSFET	$40\mu/180n$	1
M_7	n MOSFET	$20\mu/5\mu$	$<1:0>$
M_8	n MOSFET	$20\mu/5\mu$	$<3:0>$

where, C_{cap} is an array of MIM capacitance which is controlled using a 4-bit thermometer decoder. $i_{(charging,discharging)}$ is the charging or discharging current. The charging current is controlled through a biasing current, $i_{bias_charging}$ and mirrored. The discharge path is formed by transistors M_5 and M_6 . Transistors M_4 and M_5 disconnect the output node during power down state. It can be seen that the charging current ($i_{charging}$) is controlled while the discharging ($i_{discharging}$) current is not controlled. The reason is that the ramp is required to discharge as quickly as possible so as to initialize the ramp generator for the next clock cycle as depicted in figure 4.1. Table 4.3 depicts the sizing of the various transistors. For the current work, the bias charging current was provided through an off chip current source for simplicity. Referring to equation 4.3, the gradient of the ramp can be controlled by either controlling the current input (charging current) or by changing the capacitive load.

A thermometer code was implemented to configure the capacitance as shown in figure 4.21 (a). The thermometer decoder allows only one bit to change at a time. This allows the capacitance to vary approximately $30fF$ to $464.3fF$. Figure 4.21 (b) shows the simulation results as the input codes to the decoder vary from 0000 to 1111. The variations in the gradient as the capacitance values change with the input code of the thermometer decoder for a constant charging current of 500nA are

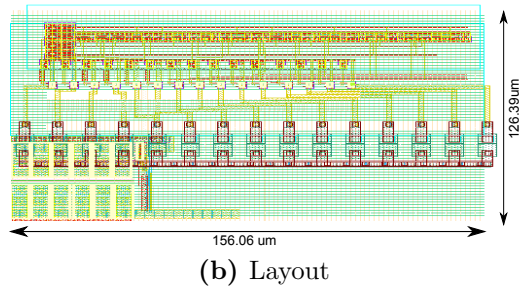
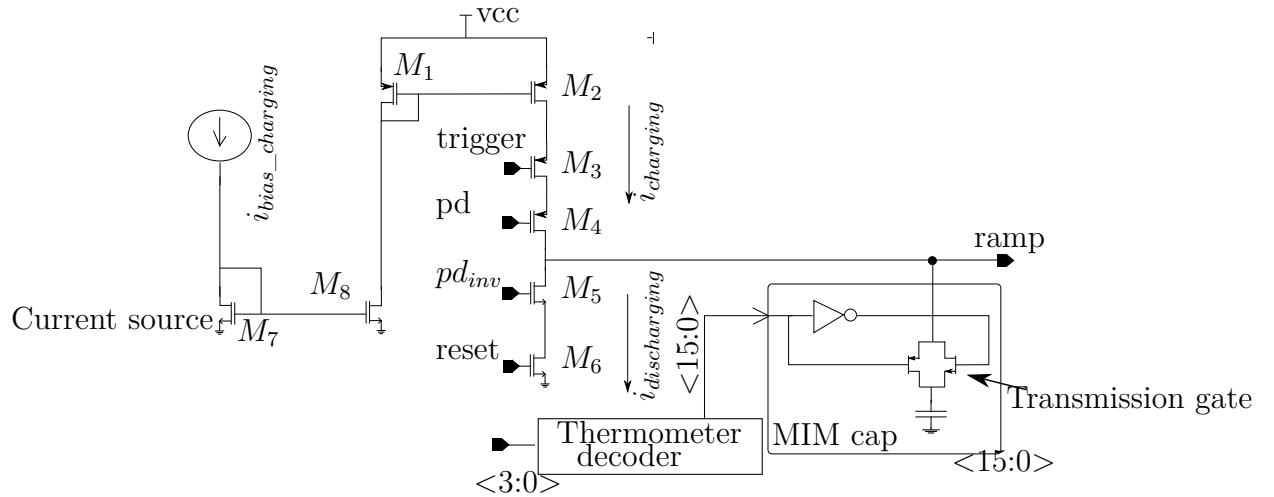


Figure 4.20: Charge Pump Based Ramp Generator

shown in figure 4.22.

Figure 4.23 depicts the change in slew rate (10% – 90%) for a constant current of $50\mu A$ while figure 4.24 characterizes the change in slew rate as the charging current is varied between $1\mu A$ and $100\mu A$ for maximum capacitance across slow, fast and nominal corners.

4.3.2.2 Edge Generation Circuitry

Referring to figure 4.4, the comparators are used to compare the ramp and the reference signals re-used from the chaotic generator. Comparator1 and comparator3 compare ramp1 and ramp2 with the reference signal. Comparator2 and comparator3 compare ramp1 and ramp2 with V_{low} . V_{low} determines the lower bound of the ramp discharge. The output of comparator1 and comparator3 is fed to a toggle flip flop. A positive pulse at comparator1 (intersection point of reference signal and ramp1) enable the discharge path thereby discharging ramp1 while simultaneously triggering or charging ramp2. Similarly, a positive pulse at comparator2 (intersection point of reference signal and ramp1) enable the discharge path thereby discharging ramp2 while simultaneously triggering or charging ramp1. Thus, the two ramps charge and discharge 180° out of phase. The toggle flip flop creates an edge at *drv_out* every time either of the ramps intersects with the reference signal. Thus, the frequency of *drv_out* is dependent on the level of the reference signal and the gradient of the ramps, ramp1 and ramp2. The duty cycle of the output signal can be varied by individually controlling the gradient of each of the ramps.

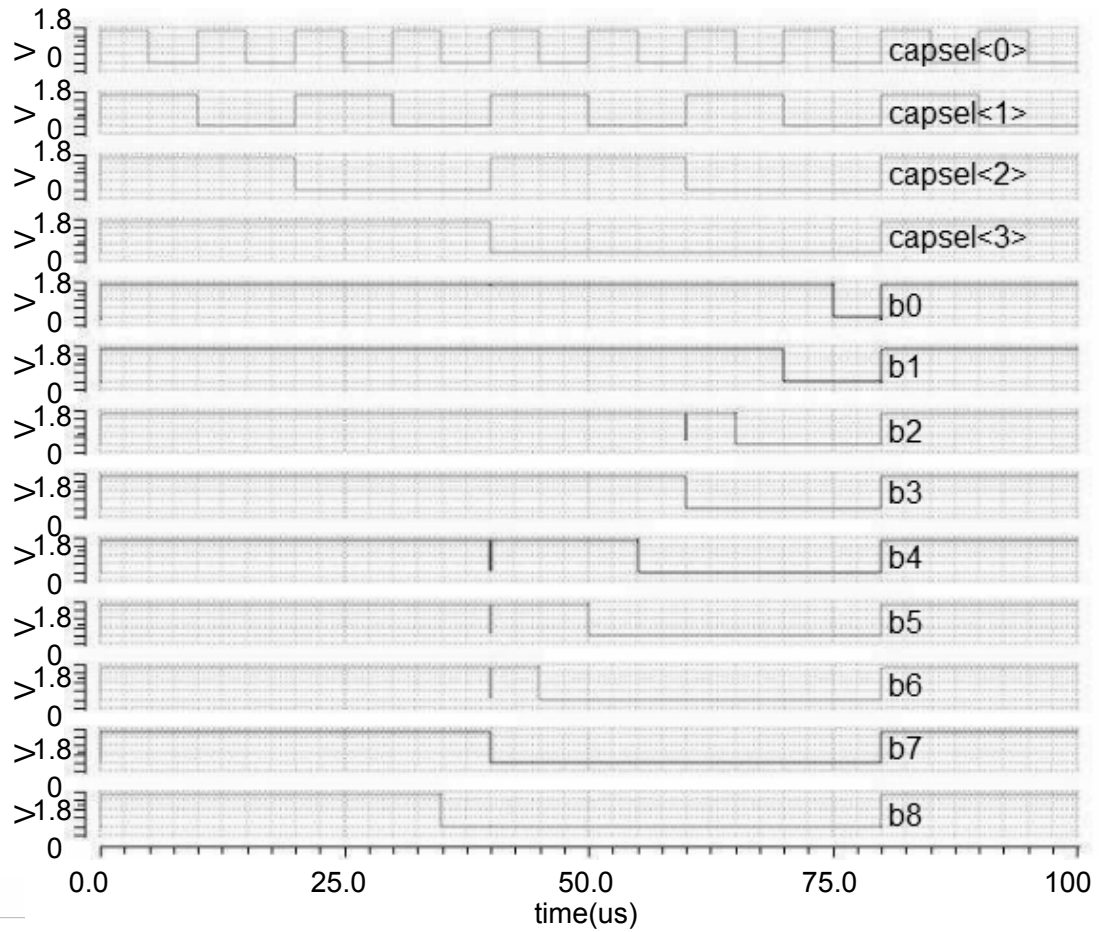
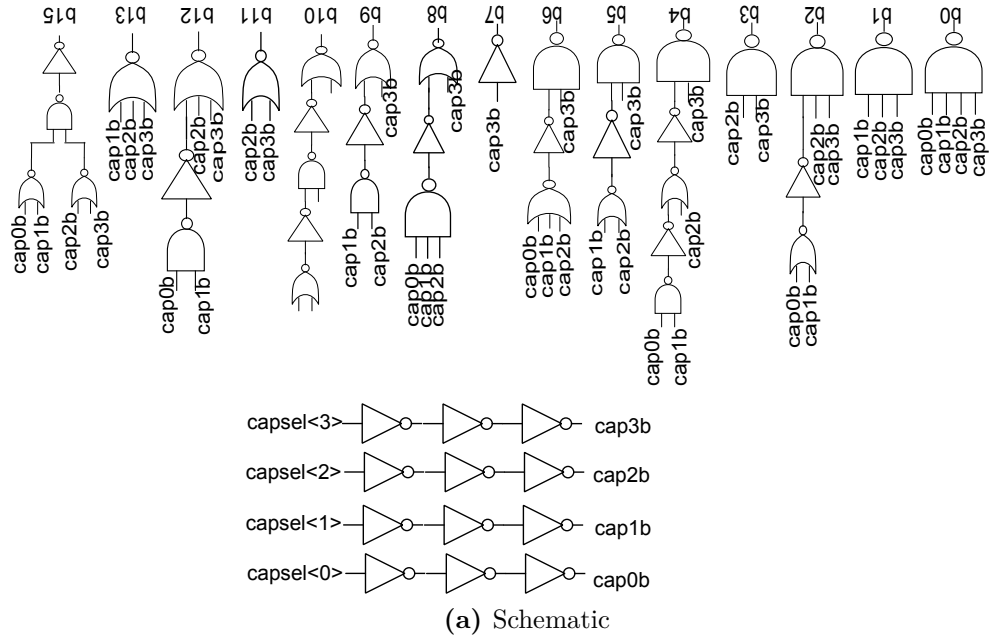


Figure 4.21: 4 bit Thermometer Decoder

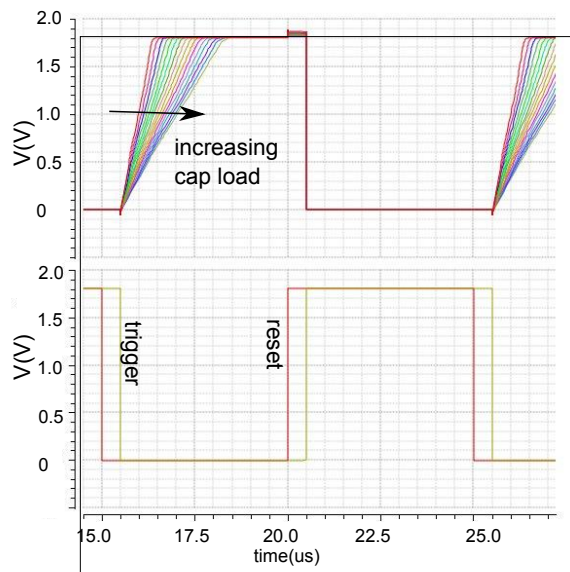


Figure 4.22: Variation of slope with varying capacitive load for $i_{charging}=500\text{nA}$

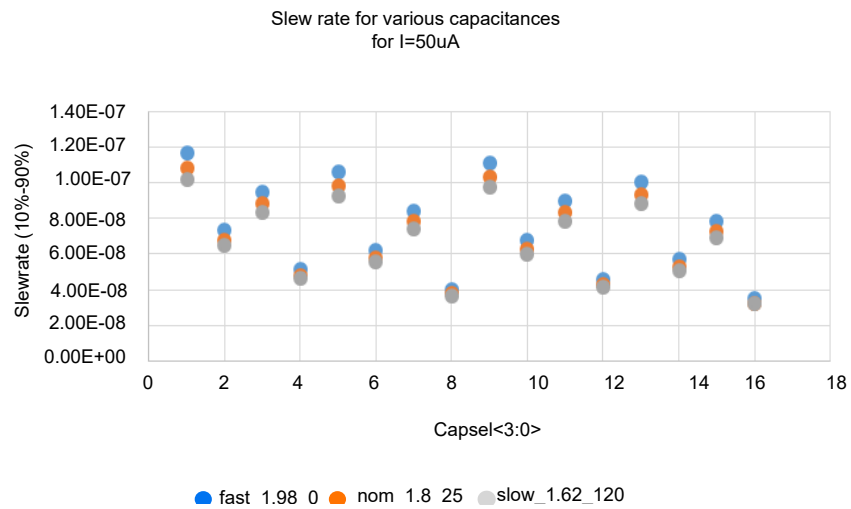


Figure 4.23: Variation in slope with varying capacitance for a constant charging current

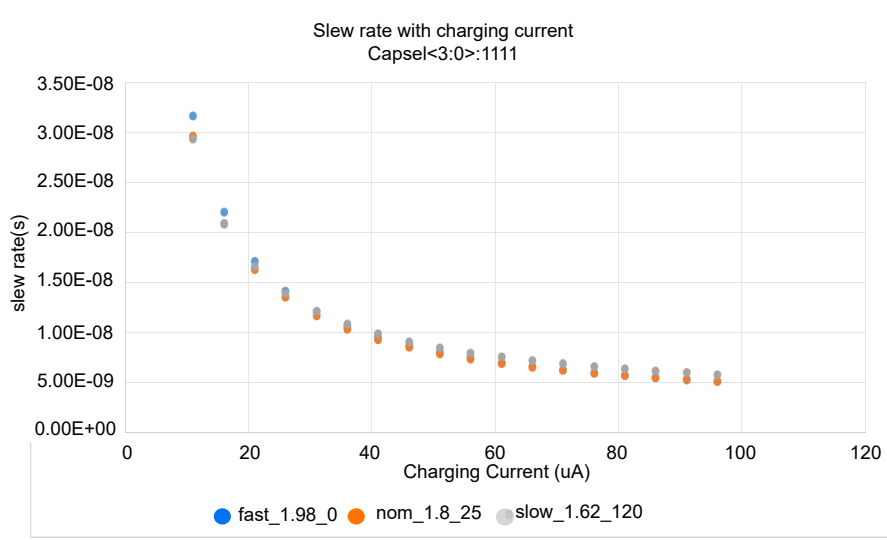


Figure 4.24: Change in gradient of the ramp generator with the change in charging current between $10\mu A$ and $100\mu A$.

4.3.3 Debugging Capabilities

In order to be able to test the internal nodes for debugging on Silicon, a monitor port was implemented. A 3 to 8 binary decoder (illustrated in figure 4.25) was implemented to map the internal node to the monitor port, table 4.4. Analog pass gates were implemented to pass the internal signals to the monitor port. To prevent the test circuitry probe and PAD cap loading the node under observation, a unity gain amplifier (voltage follower) was connected between the internal node and the PAD.

In order to test the frequency modulator independent of the chaotic generator and monitor the output of the chaotic circuit, an analogue bypass multiplexer was implemented to control the V_{high} signal off die.

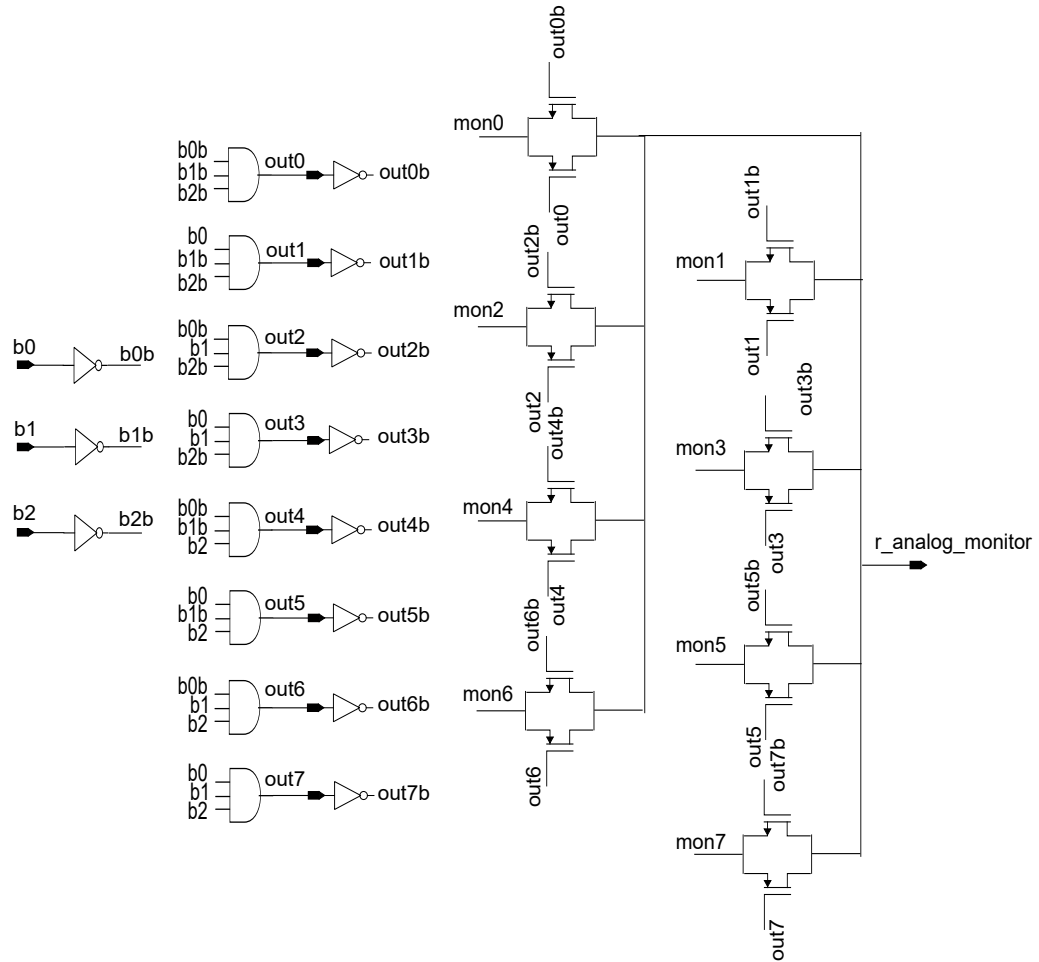


Figure 4.25: Monitor port decoder

Table 4.4: Monitor Port Connections

Monitor Port	Node Under Observation	Comments
mon0	r_level_high_rampgen0	Upper charging level for ramp 0
mon1	r_level_high_rampgen1	Upper charging level for ramp 1
mon2	ramp0	Output of ramp generator - ramp0
mon3	ramp1	Output of ramp generator - ramp1
mon4	cmp_pos_gen0	Output of comparator 0
mon5	cmp_pos_gen1	Output of comparator 1
mon6 - mon7	Unconnected	Unconnected Pins

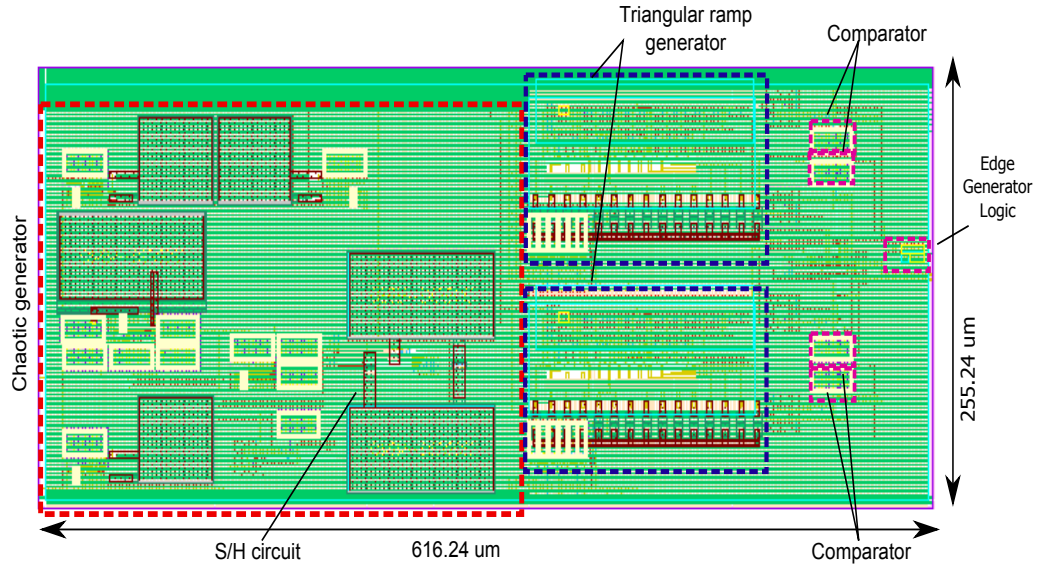


Figure 4.26: NLM top level layout in 0.18um technology

4.3.4 Top Level Layout Integration

Figure 4.26 depicts the layout of the NL modulator. Great care was taken to reduce the impedance of the power grid, to shield sensitive circuits and matching various paths. As shown, the ramp generators and the comparators were placed symmetrically around the y-axis. This was done intentionally to match the two paths to have minimal impact on the two edges due to any mismatches in ramp1 and ramp2 [109]. Any mismatches in the two paths would cause an unintentional duty cycle error in the generated clock. A guard ring was placed around all the critical circuits to shield them from any noise.

To lower the coupling between high speed nets, for example, ramp1, ramp0 and clock nets, at least two routing grid spaces were kept. In addition, a ground shield was inserted to minimize the coupling further [110]. To prevent amplifying of the coupling cap between the routing tracks, care was taken not to route any two nets with 180° phase difference. To lower the power grid resistance, a rectangular alternating power and ground grid was adopted. This is shown in figure 4.27.

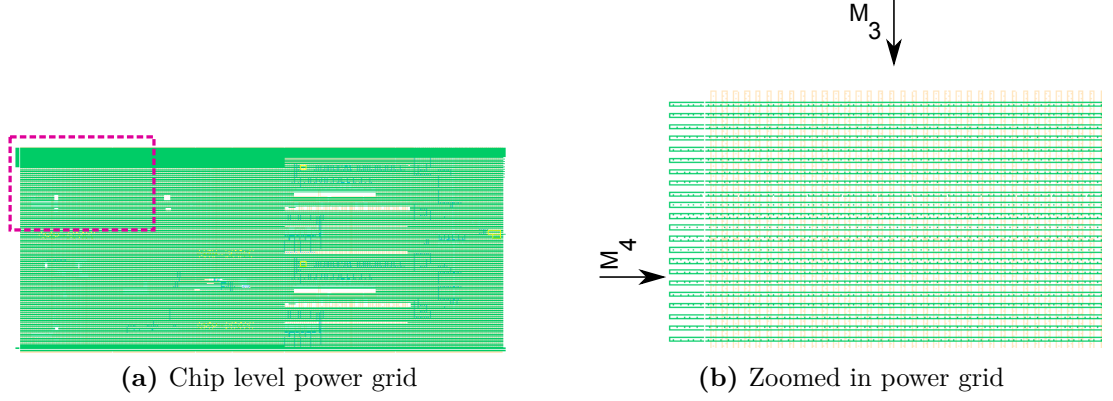


Figure 4.27: Power grid design for chip level

A pad ring was built using the 1.8V IO pads for the test chip. A $66\mu m$ wide M2 metal layer was used for power/ground connections as shown in figure 4.28.

4.3.5 System Level Simulations

A mixed mode simulation test bench was built to simulate the entire system. The system model was built using verilogA [111] and schematics. Cadence AMS tool

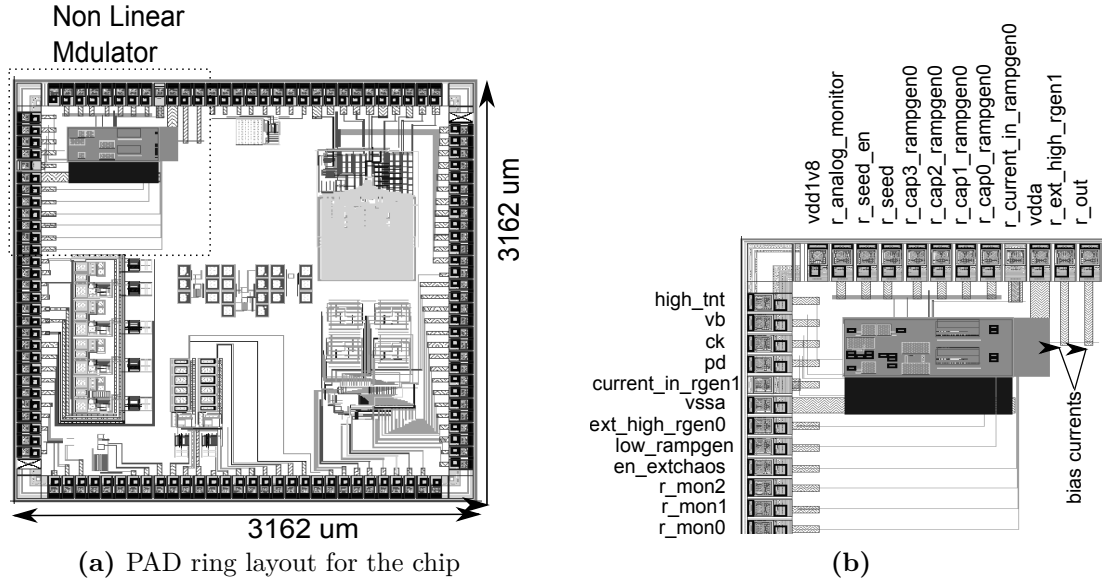


Figure 4.28: PAD ring connections for non linear modulator

[112] suite was used to perform mixed mode simulations. Figure 4.29 illustrates the proposed system level diagram for modulating and transmitting the neural signals. The system comprises of sensor array for sensing the neural signals which are amplified by the neural amplifier. A sleep signal was obtained through Physionet [6]. The amplified EEG signal was digitized using a 12 bit analog to digital converter (ADC). The converted bits were serialized using the parallel to serial (P2S) block and a current digital to analog converter (IDAC) was utilized to generate a current $I_{out_{dac}}$ comprising of two DC current values I_1 and I_0 corresponding to bit ‘1’ (mark) and bit ‘0’ (space) respectively. The currents I_1 and I_0 were used to generate a ramp in the ramp generator. By switching the current, the corresponding frequency modulation is achieved. A shift in the carrier frequency as per DOSS (Dynamic Open Spectrum Sharing) protocol [3] was achieved by changing the load capacitance of the ramp generator. The block Up/Dn converter is a look up table for selecting an appropriate capacitance for the base frequency required. A change in the base frequency also leads to a change in the encoded frequencies which might have to be re-tuned using the charging currents I_1 and I_0 . The reference signal generates the modulation profile.

To test the proposed system, a neural amplifier was designed while verilogA models were built for ADC, IDAC and P2S blocks. The amplifier is not a part of the current work and has been covered in detail in [113]. Figure 4.30 shows the simulation results from sensor output to the IDAC. The amplified EEG signal, $data_{EEG}$, is sampled by a 12bit ADC. The ADC then feeds the bits into the parallel to serial block (P2S) to generate a serialized bit stream, $p2s_{out}$. The sampling frequency of the P2S block is 12 times the frequency of the ADC to enable all the bits to serialize. It is possible to reduce the P2S operating frequency by storing the 12 ADC bits into registers before serializing them.

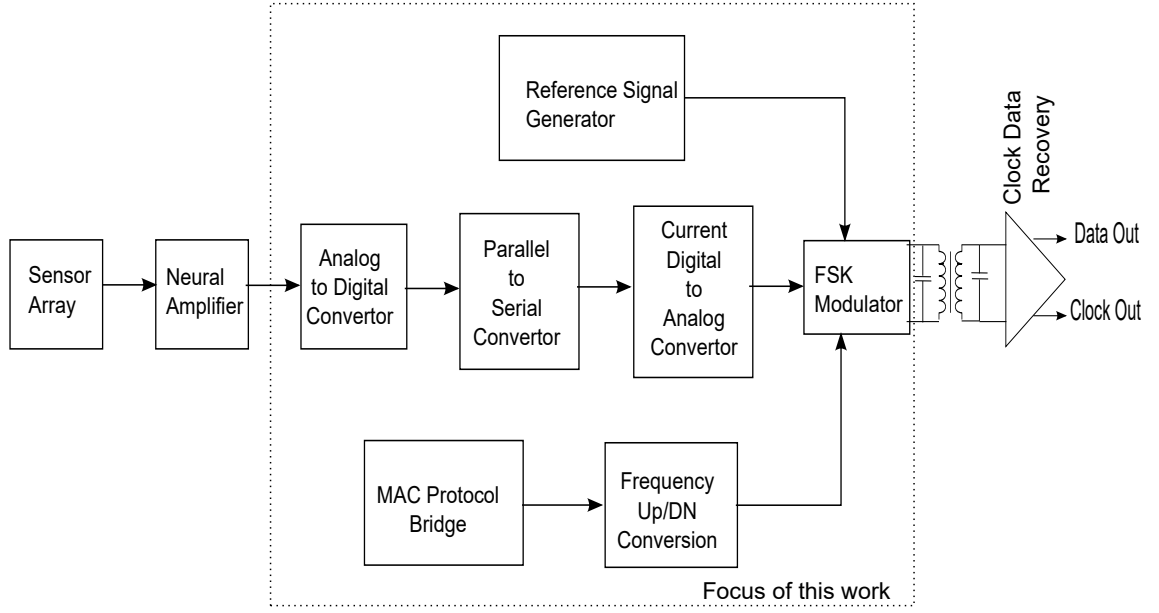


Figure 4.29: System diagram for a FSK transmitter system

The serialized bit stream is fed to an IDAC which translate the two levels of the bit stream to two corresponding current levels (figure 4.31). As discussed the charging current, $I_{out_{dac}}$, was derived from the IDAC while the charging capacitance was set by the ‘MAC protocol bridge/Frequency Up/Dn Converter reference signals.

Figure 4.32 depicts the signals as they move from P2S block to the frequency modulator. It is worth noting that in the current case, the reference signal is not varied. Thus, for a single current (bit not changing) the output frequency is not modulated. It can be seen that a change in the load capacitance leads to a change in the base frequency wherein three cases with different cap selection settings are depicted. Figure 4.32 depicts an amplified case wherein the cap setting was suddenly changed. A notch can be seen at the switch over point due to change in frequency with the change in IDAC current.

It can be observed that for all the cases, the IDAC output current follows the serial bit pattern leading to the change in outputs signals frequency as shown in figure 4.33. Even though in the current case the IDAC current is kept constant, it can be

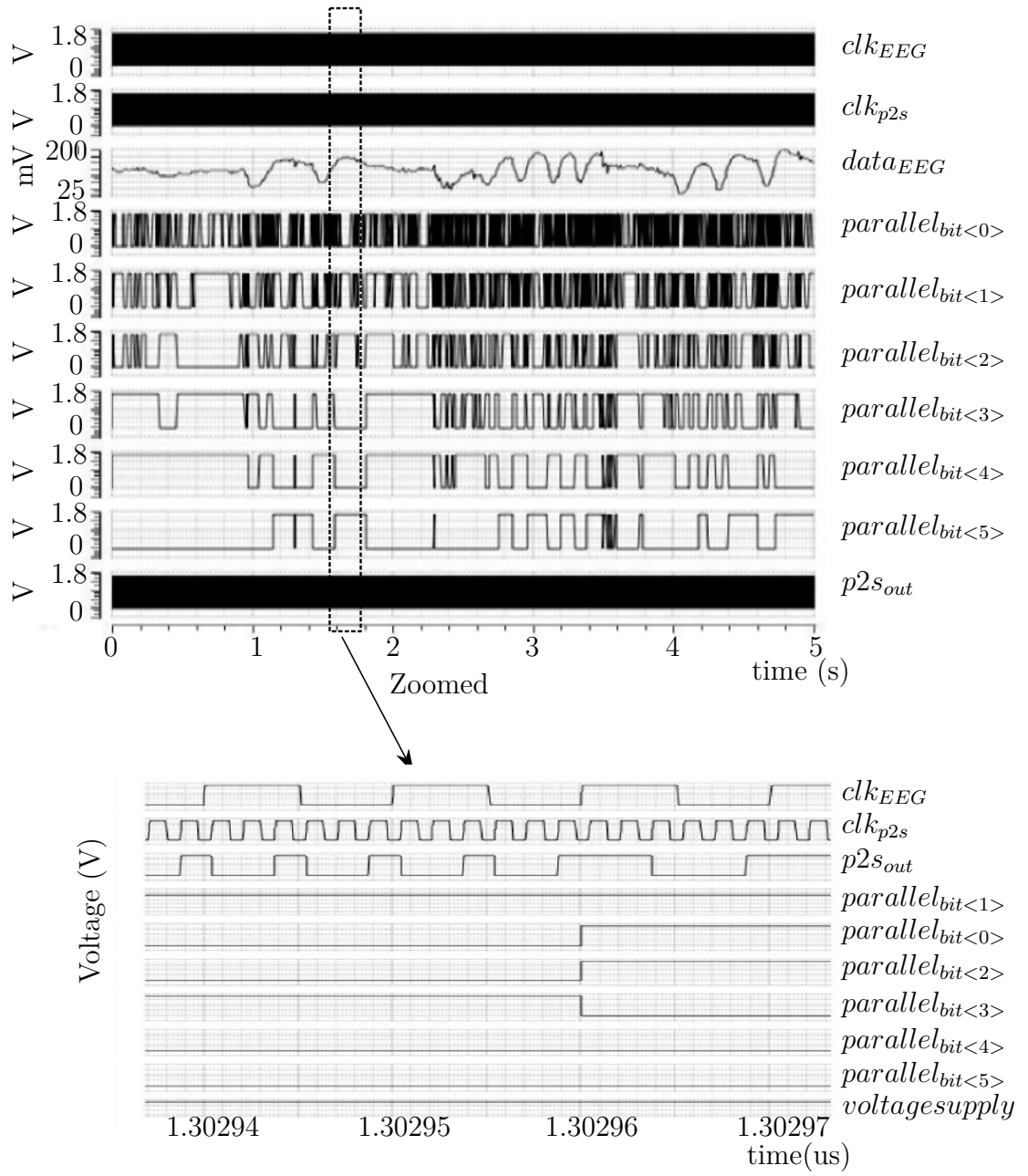


Figure 4.30: EEG data path from the sensor to the IDAC. The EEG clock samples the amplified EEG signal which is then parallelized into a `eeg_p2s_out`

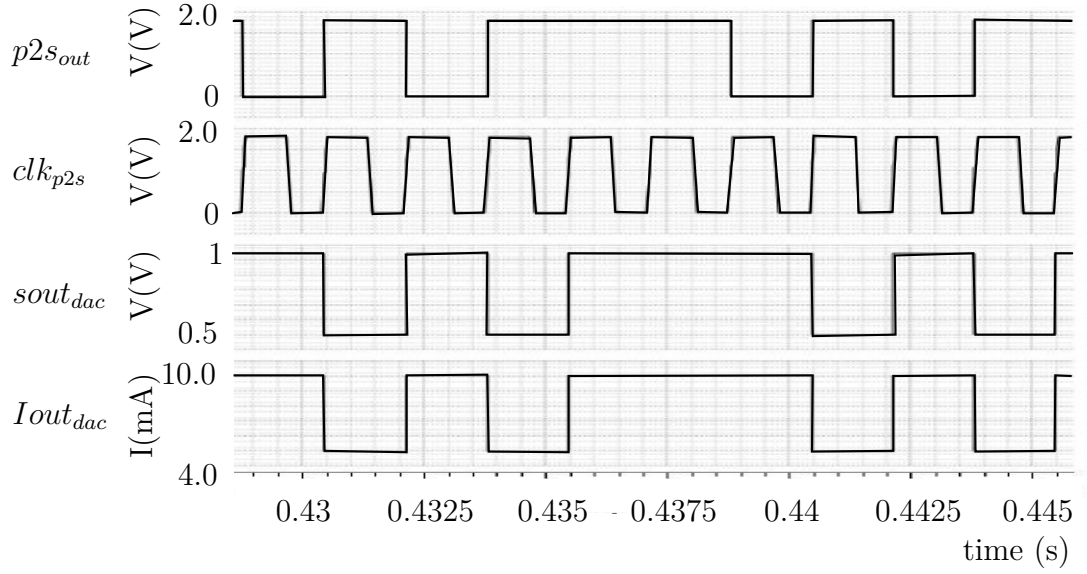
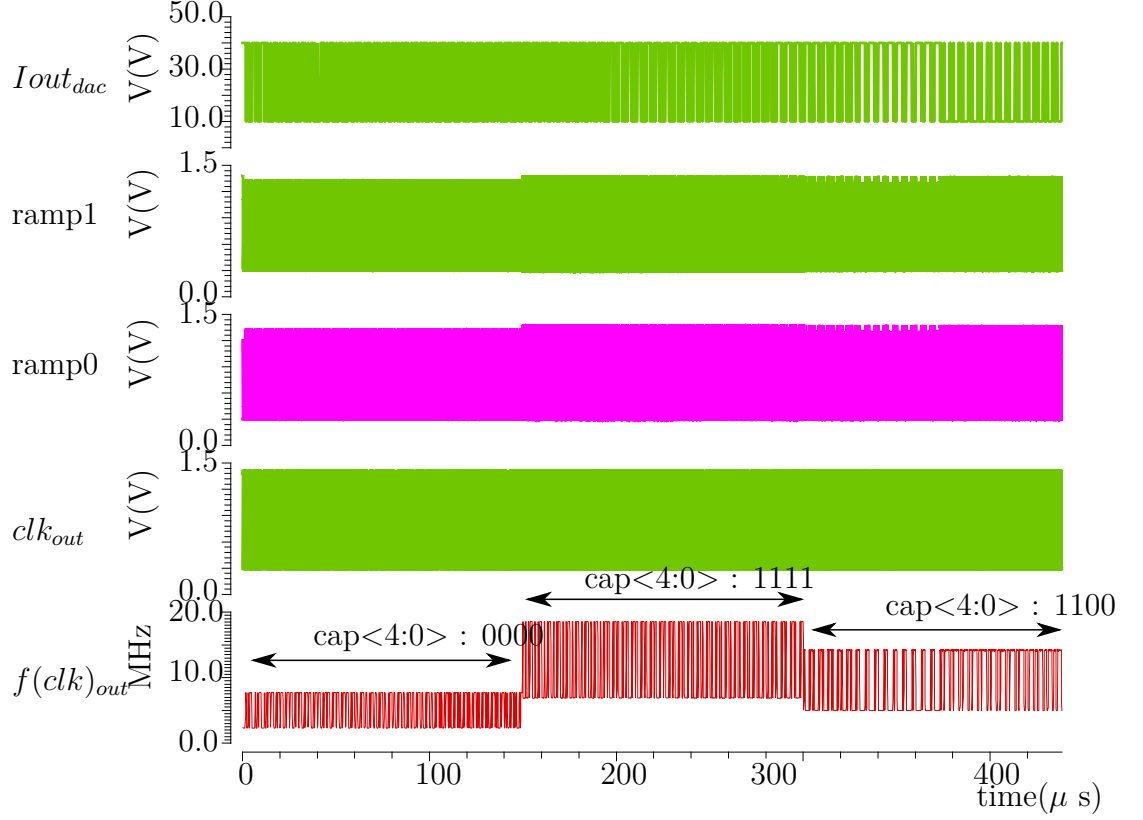


Figure 4.31: The serialized bit stream (eeg_p2s_out) is passed to a 2 bit IDAC and converted to $10\mu A$ and $40\mu A$ currents. The time stamp starts from $1.137s$

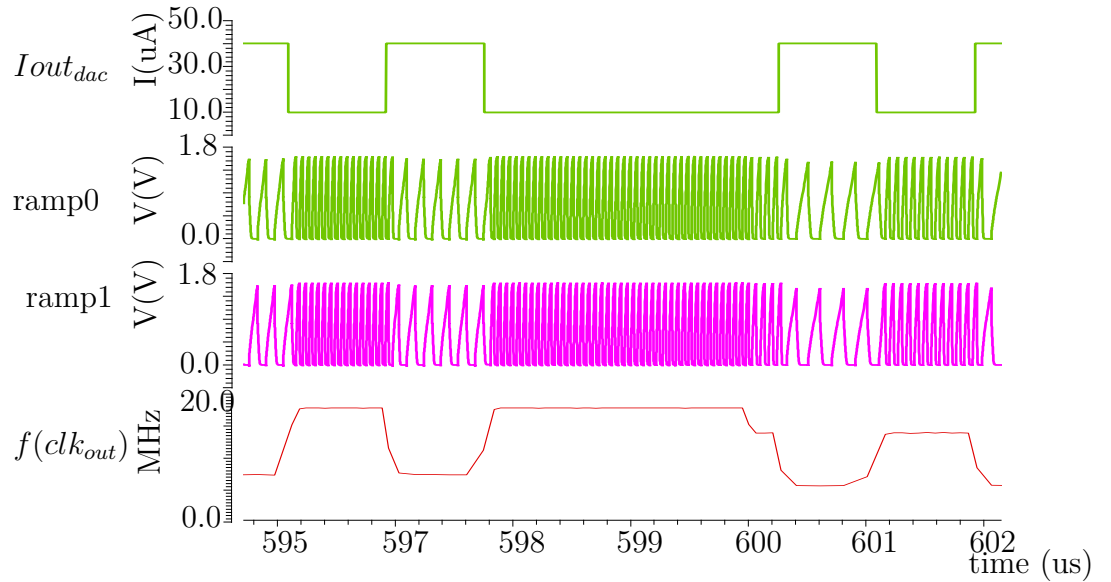
tuned for cases where better resolution is required.

Various modulation profiles were generated and fed to the frequency modulator. An analog multiplexer was built to allow bypassing the chaotic signal generator and passing the reference signal from an external pad. A sinusoidal modulation profile of 2 kHz with 300mV peak to peak amplitude around 1V reference signal was fed as the reference signal to the frequency modulator. It can be seen in figure 4.34 that the ramp charging follows the sinusoidal signal. An edge is generated at the intersection point of the ramp and the reference signal, thus modulating the output clock as can be seen in figure 4.34. Figure 4.35 depicts the spectrum of the unmodulated clock (generated with a constant reference signal of 1V) and the sinusoidal modulated signal. As expected, it can be seen from the peak of the spectrum has lowered.

To further test the circuit, a 2 kHz triangular signal was used as a reference signal with peak to peak amplitude of 300mV as depicted in figure 4.36. Again, it can be seen that the ramp charging follow the modulation profile. The frequency of the



(a) The IDAC output current is fed to charge pumps leading to movements of gradients in the ramps, thus encoding the bits into two frequencies. The frequencies move around the base frequency set by the ramp generators cap setting.



(b) Zoomed case showing the sudden change in frequency as the capacitance setting is changed

Figure 4.32: System path from IDAC to output

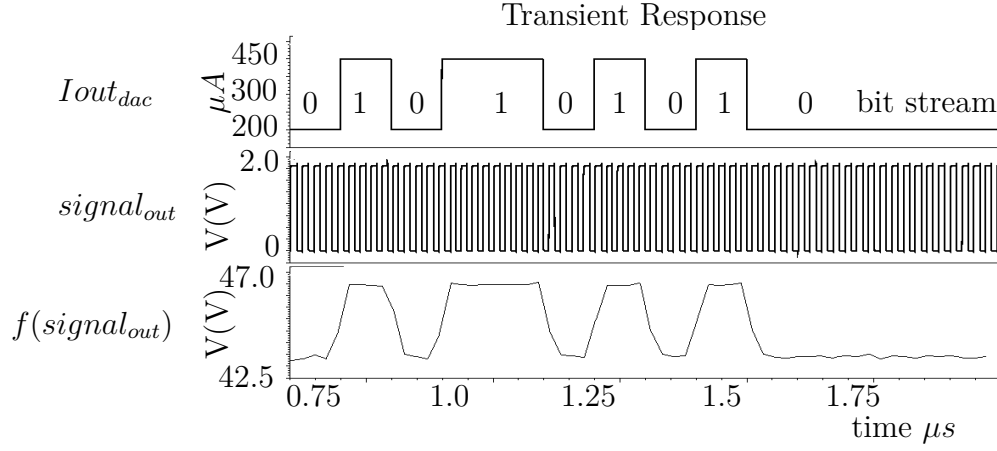


Figure 4.33: Encoded data stream into the frequency

output clock follows the modulation profile. Figure 4.37 shows the output spectrum of the output clock modulated using a triangular reference signal with a peak-peak amplitude of 600mV and 300mV around 1V. A wider peak to peak range leads to a larger frequency deviation, hence lowering the peak, and a wider bandwidth as can be seen in figure 4.37.

The chaotic generator was enabled next and fed to the frequency modulator. It can be seen in figure 4.38 that as the reference signal (chaotic signal) changes, the modulation frequency follows it. However, since the chaos generator is unbounded, meaning that the chaotic signal can lie anywhere between 0V to 1V, for low values (less than 300 mV) of the chaotic signal, the clocks did not appear. Referring to figure 4.39 it can be seen that around at low value of the chaotic signal, as expected, the ramp reaches the reference signal in a short time resulting in a very short pulse at the comparator output. As discussed previously, the comparator output acts as a trigger for the next charging cycle for the other ramp. Since, the pulse is very small, the system is unable to respond. This is further worsened if the reference

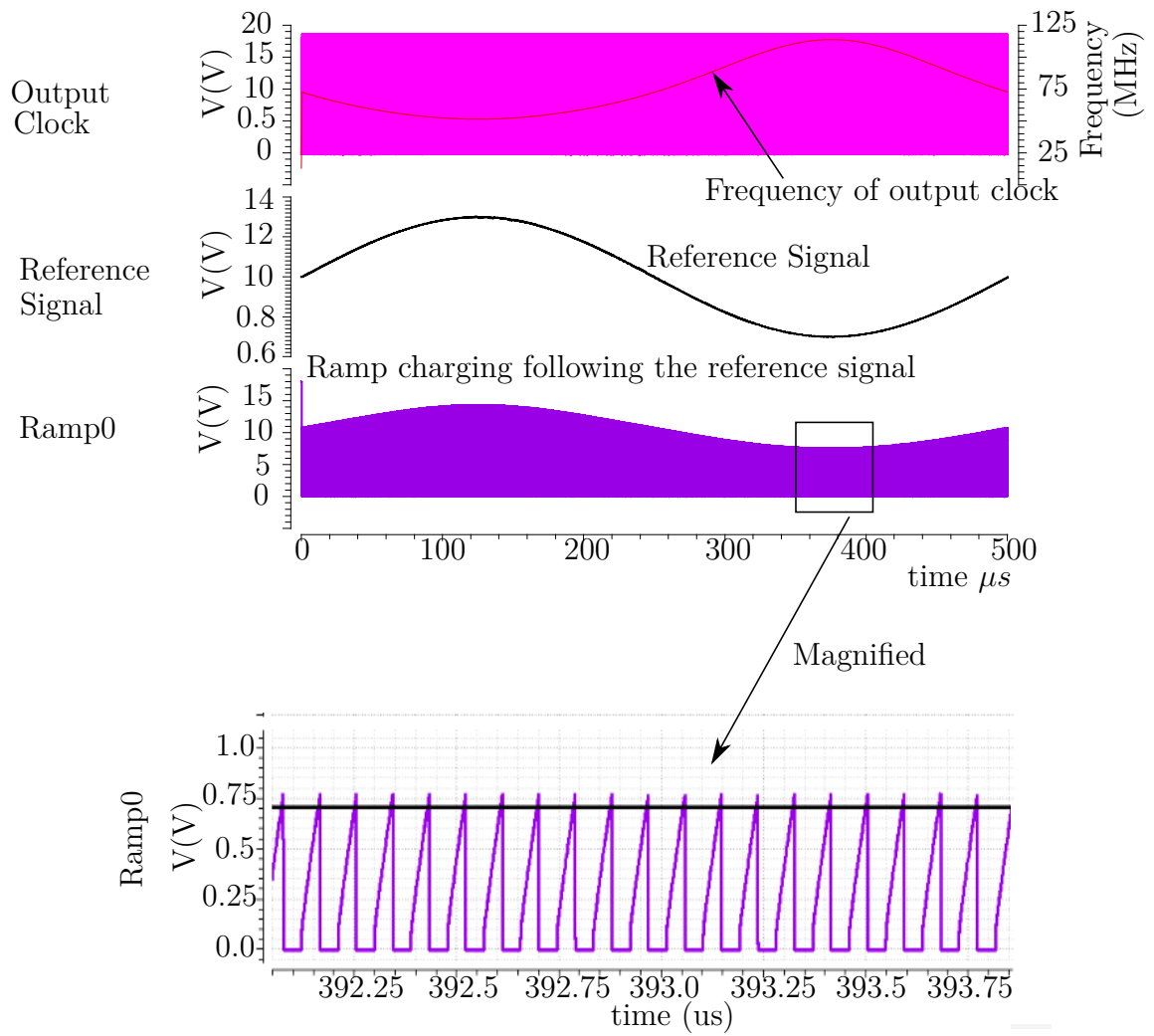


Figure 4.34: Output clock modulated using a sinusoidal reference signal

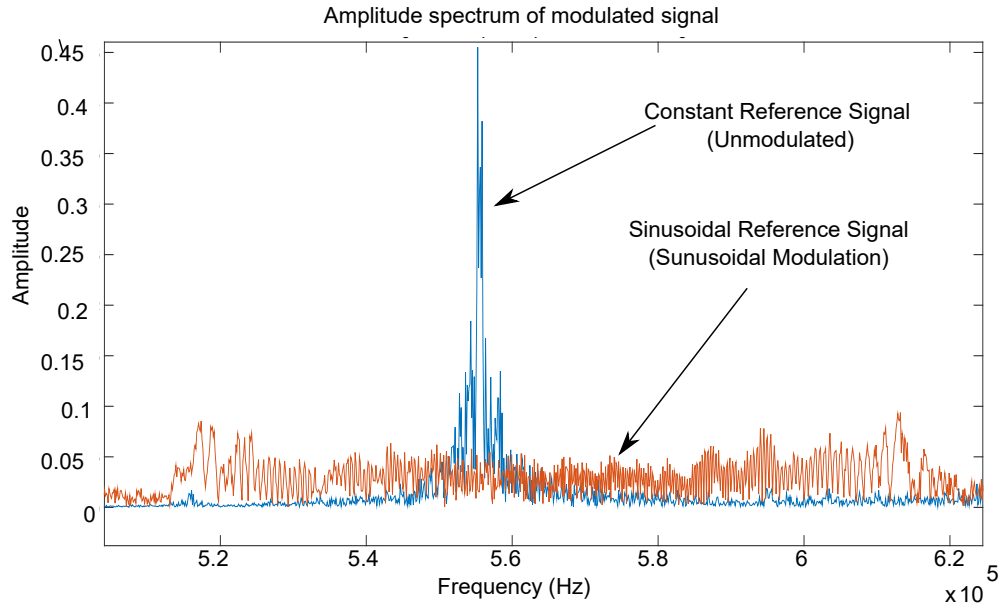


Figure 4.35: Frequency spectrum of unmodulated vs sinusoidal modulated clock signal changes at the same time as the trigger point for the charging cycle (figure 4.39).

One straightforward solution is to shift the generated chaotic signal. For the current case, 300mV was added to generate chaotic signal and fed back to the frequency modulator through the analogue bypass. It can be observed in figure 4.40 (a) that the modulated clock is generated and follows the change in chaotic signal. Figure 4.40 (b) depicts a zoomed in sample of the simulation. As discussed, the ramps follow the chaotic reference signal.

Figure 4.41 depicts the frequency spectrum of the chaotic modulated clock. It can be seen that the spectrum is not as dense and flat as expected. This is due to the fact that the simulation time was not sufficient to get all frequency ranges. Additionally, as discussed the chaotic signal was modified leading to further missing certain tones.

A model was built for the frequency generator and the chaotic signal pattern from

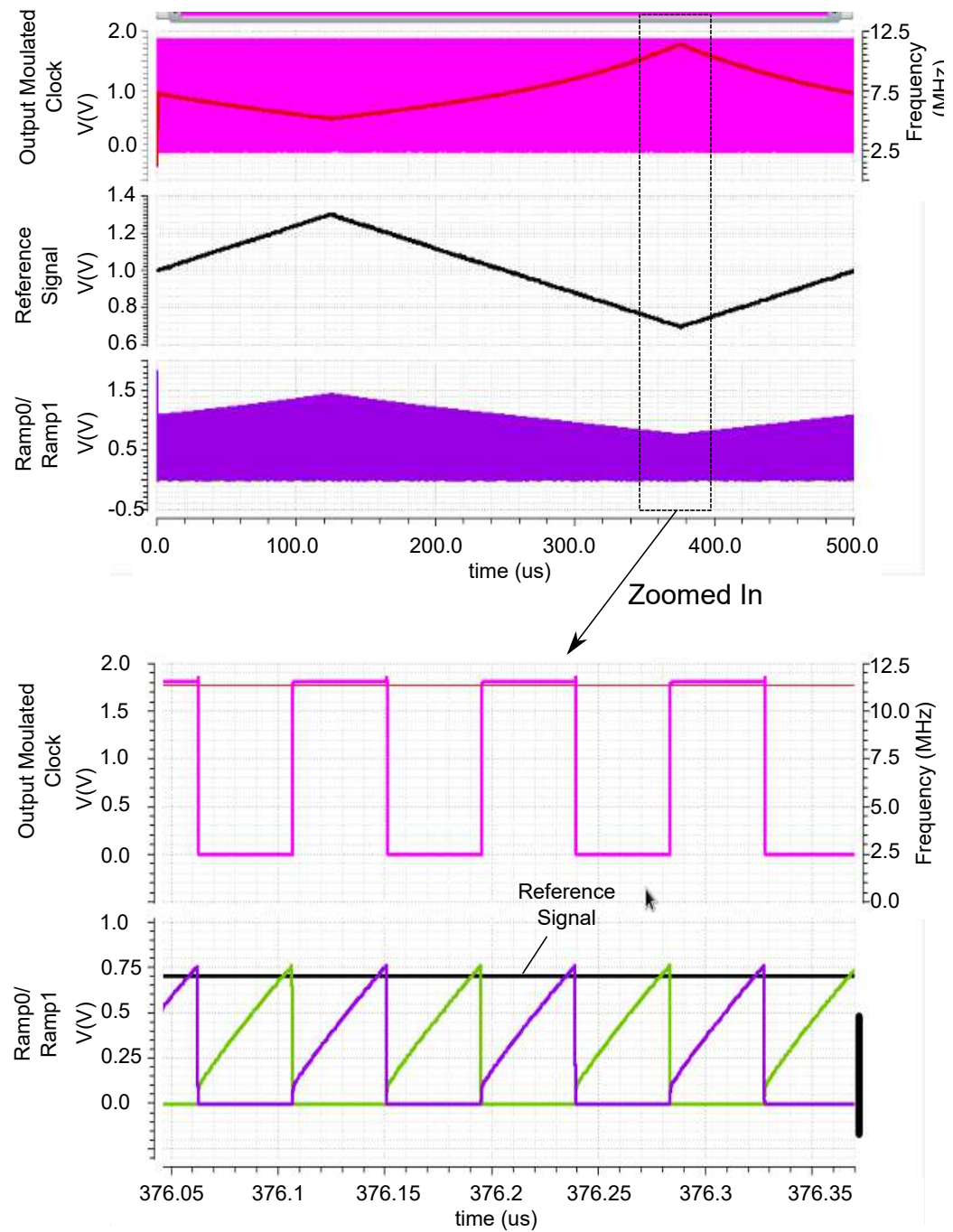


Figure 4.36: Output clock modulated using a two triangular reference signal of 300mV and 600mV amplitude around 1V

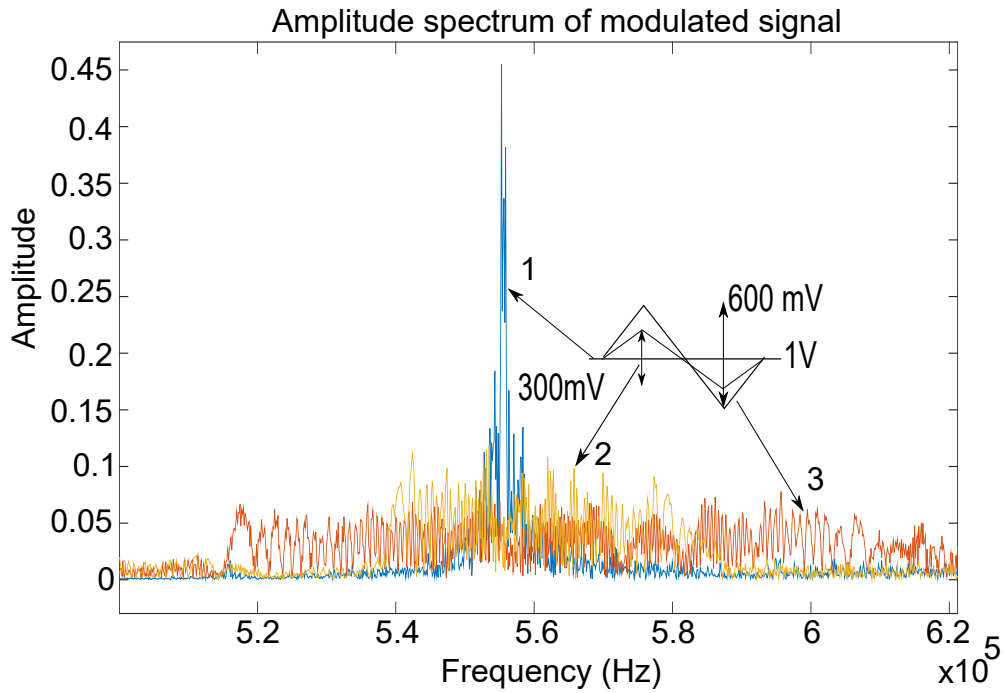


Figure 4.37: Frequency spectrum of the output clock modulated using two triangular reference signal of 300mV and 600mV amplitude around 1V vs the unmodulated clock

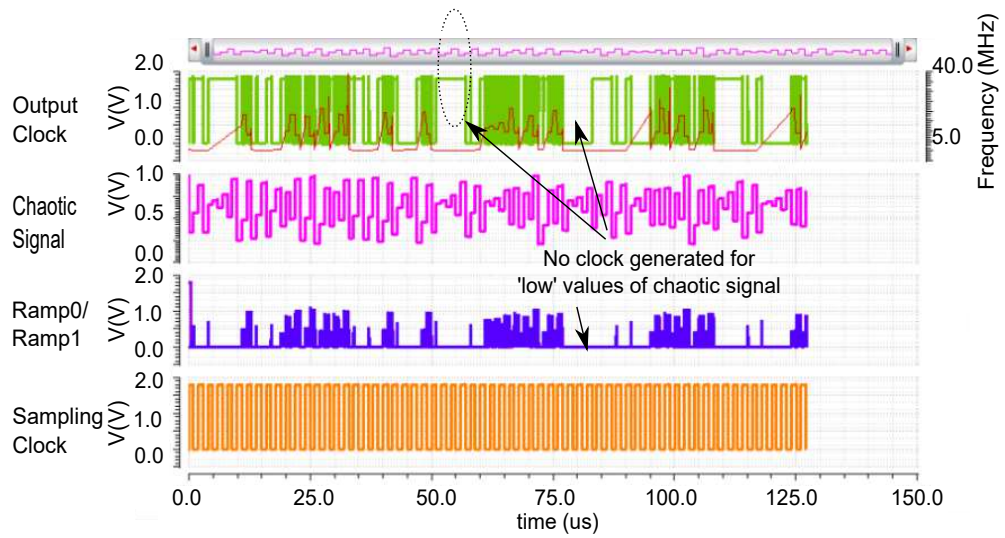


Figure 4.38: Illustration of how Lower values of the chaotic signal below 300mV lead to clock not being generated as the ramps do not charge/discharge

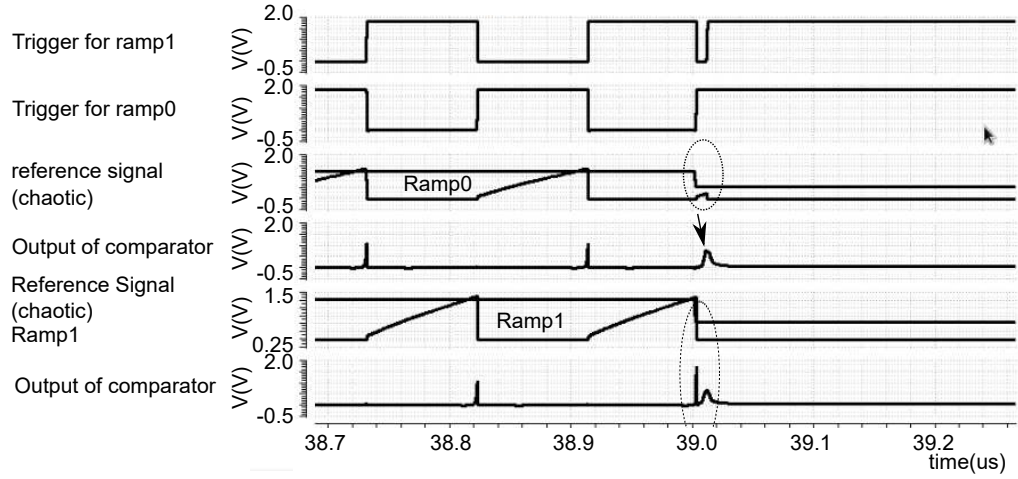
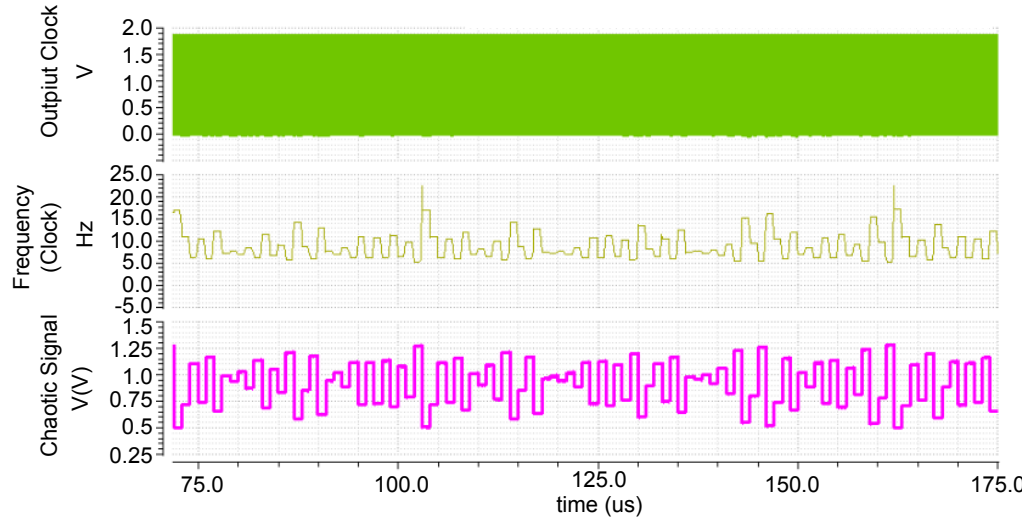


Figure 4.39: Loss of clock due to short ramp pulse leading to missed clock cycles

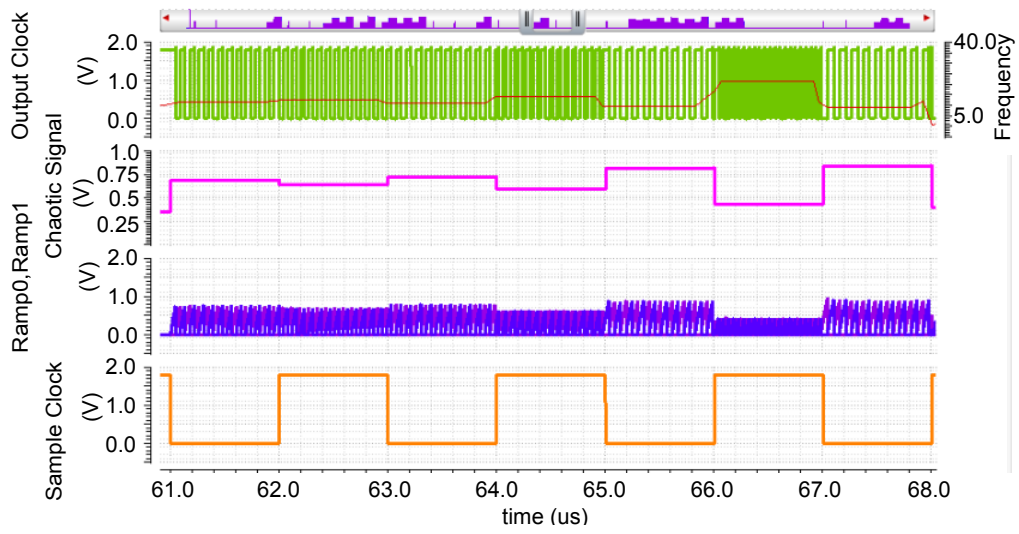
the chaotic generator was fed to the frequency modulator. Figure 4.42 depicts the PSD of the chaotic modulated signal (chaotic). It can be seen that the frequency spectrum of the chaotic modulated clock is very dense. However, it can be observed that the noise floor has increased over side-bands. The modulation has been done for a single bit stream without any bit encoding. This is reasonable as the frequency dithering has been proposed to be within the encoded symbol.

Finally, figure 4.43 depicts the photograph taken through a microscope of the fabricated chip. A wire bond package was used. chapter 5 discusses in details the test board, measurement setup and measured results.

A 8db improvement in the peak power spectrum was achieved over a periodic Hershy-Kiss modulation profile in simulations. Table 4.5 compares a PLL based SSC modulator with a stair case periodic non-PLL and chaotic SSC modulator.



(a) Frequency of output clock follows the chaotic signal



(b) Zoomed showing the movement of ramps with the chaotic signal

Figure 4.40: The chaotic signal generated by the chaos generator is applied as the reference signal to the frequency modulator with the chaotic signal shifted by 300mV

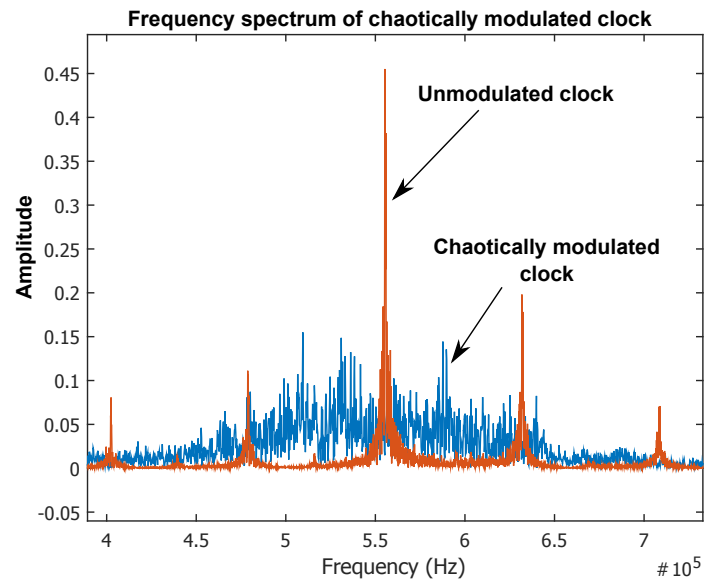


Figure 4.41: Frequency spectrum of the chaotically dithered clock vs the unmodulated clock.

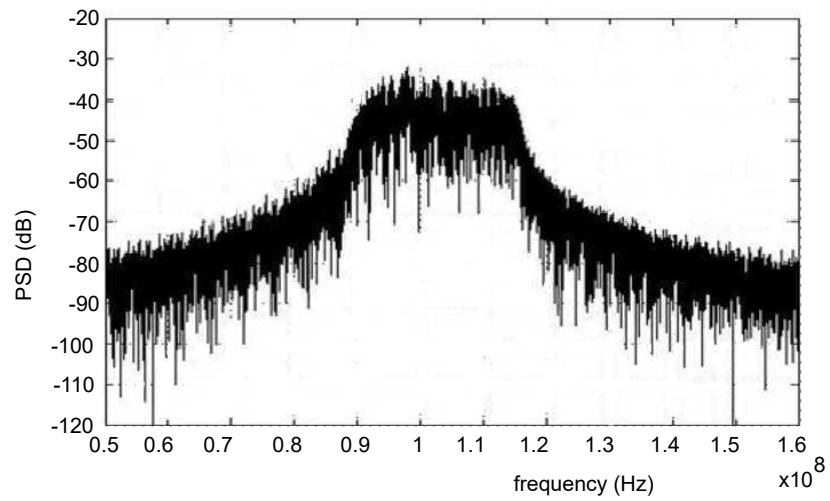


Figure 4.42: Power spectral density of the chaotic modulated clock

Table 4.5: Summary of performance comparison

SSCG Modulation profile	Triangular	Step Modulation profile	Chaotic
Process CMOS	180nm	65nm	180nm
Supply Voltage	1.8V	1.05V	1.8V
Input Frequency (MHz)	1 - 120	33 - 133	1 - 100
Modulation Frequency	30kHz-50kHz	Independent	Independent Power at 47 MHz
Power	100mW	1.15mW	1.64mW

4.4 End of chapter remarks

The current chapter proposed a chaotic modulator. All the simulations presented were carried out on 0.18 μm IBM technology on the extracted netlist. A full system was modelled using verilogA. The neural amplifier presented was borrowed from a colleague, Mr. M. Abbasi (PhD. student at Imperial College). The circuit proposed was fabricated through Europractice. chapter 5 discusses in detail the measurements carried out and development of the measurement setup.

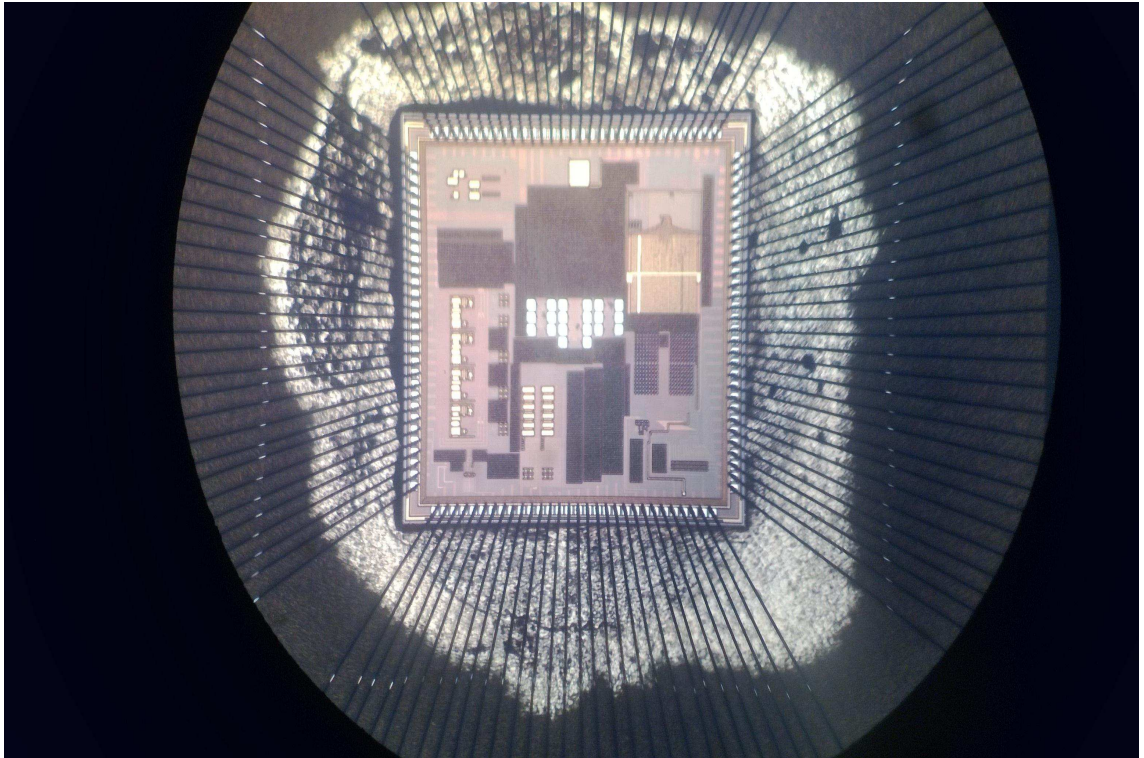


Figure 4.43: Fabricated chip die

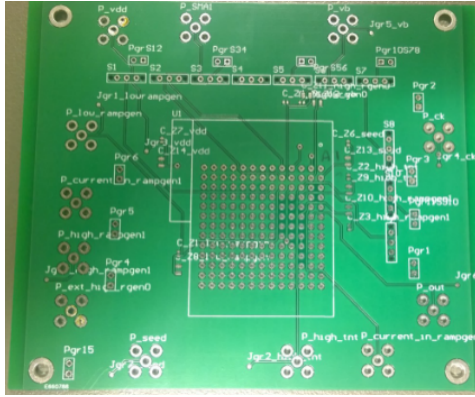
5 PCB Design, Test Setup and Silicon Measurements

THE chip was fabricated using AMS 0.18μ technology [114] through Europractice [115]. The dimension of the chip is $3162\mu m \times 3162\mu m$ with a total die of about $10mm^2$. The total utilizable area was $2794.1\mu m \times 2794.1\mu m$ resulting in $7.0807mm^2$ which was shared amongst various projects. Standard cell pads were utilized to create the pad ring. 120 standard IO analogue cells were built using a pitch of $90\mu m$. The current chapter presents the considerations put into building the test setup and the measurement results.

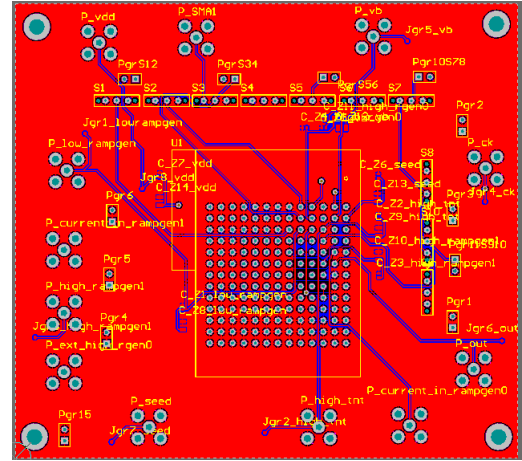
5.1 Printed Circuit Board Design and Layout Considerations

The PCB (printed circuit board) was designed and layout done using the Altium suite of software [116]. The layout of the PCB is depicted in figure 5.1(b), (d) while the final manufactured PCB is depicted in figure 5.1 (a), (c).

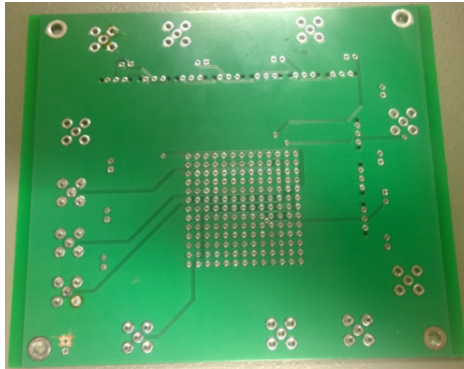
To enable re-use of the PCB for testing multiple chips, a socket was used to mount the chip. A Zero Insertion Force (ZIF) [117] (2-CUS-6313-1902) socket for Ceramic



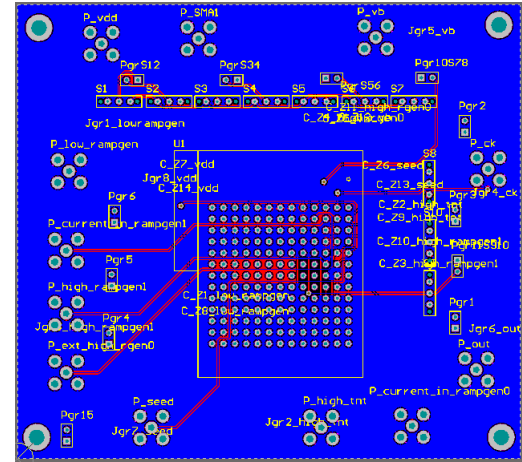
(a) Top layer of manufactured PCB



(b) Layout of top layer for the PCB



(c) Bottom layer of manufactured PCB



(d) Layout of the bottom layer

Figure 5.1: PCB board designed to test the chip

Pin Grid Array (CPGA) from BFI Optilas was utilized for housing the fabricated chip. Figure 5.2 shows the photograph of the ZIF socket.

Each of the 20 pins of the socket were connected to the bond pads of the chip as detailed in figure 5.2 (b). The current work utilizes pins 1 to 12 and pins 109 to 120. The choice of pins was done keeping in mind that the tracks are closer to the pads as depicted in figure 5.3. The current work was placed in the top left corner of the die (depicted as region Non Linear Modulator in the figure 5.3).

Table 5.1 lists the connectors used to interface signals with the test equipment. As can be noticed, the various configuration signals were connected using a switch which either sets or resets the configuration signal. Low pass filters were implemented and connected to various signals to filter out high frequency noise as depicted in figure 5.4. Additional pin connectors were used to monitor the signals. The pin connectors are denoted as $Jgr_ [Pin_Name]$ in the schematic shown in figure 5.4.

As discussed, switches were used to toggle the various configuration bits to appropriate values as shown in figure 5.5.

A two layer PCB was used for routing the various layers. To reduce the ground bounce between the topside and bottom side, ground planes of the PCB board, multiple points were shorted between the top and bottom layers. In addition, ground shielding was inserted between critical signals. Also, to reduce the mutual cap, it was ensured that the adjacent routes on board were not out of phase. The same principle was applied for on die tracks.

Figure 5.7 depicts the test setup for performing the silicon measurements. The following equipment was used

- Yokogawa Oscilloscope (D1) [118]
- Agilent spectrum analyser (D2) [119]



(a) Zero Insertion Force socket (ZIF) socket

	N	M	L	K	J	H	G	F	E	D	C	B	A	
1	30	27	26	23	21	18	17	14	11	9	6	3	120	1
2	33	32	29	25	22	19	15	13	10	7	5	2	117	2
3	36	35	31	28	24	20	16	12	8	4	1	119	116	3
4	39	37	34							N/C	118	115	113	4
5	41	40	38								114	112	111	5
6	44	43	42								110	109	108	6
7	47	45	46								106	105	107	7
8	48	49	50								102	103	104	8
9	51	52	54								98	100	101	9
10	53	55	58								94	97	99	10
11	56	59	61	64	68	72	76	80	84	88	91	95	96	11
12	57	62	65	67	70	73	75	79	82	85	89	92	93	12
13	60	63	66	69	71	74	77	78	81	83	86	87	90	13
	N	M	L	K	J	H	G	F	E	D	C	B	A	

Top view

(b) Socket to Bond Pad mapping

Figure 5.2: Zero insertion force socket and its bond pad mapping

Table 5.1: Description of connectors used to interface PCB with the test equipment

Pin Name	Direction	Socket Number	Connector Type
r_high_tnt	Input	C3	SMA
r_vb	Input	B2	SMA
r_clk	Input	B1	SMA
r_pd	Input	D3	Switch
r_current_in_rampgen1	Input	C2	SMA
r_vssa	Input/Output	C1	Shorted to the PCB ground plane
r_ext_high_rgen0	Input	D2	SMA
r_level_low_rampgen	Input	E3	SMA
r_en_extchaos	Input	D1	Switch
r_mon2	Input	E2	Switch
r_mon1	Input	E1	Switch
r_mon0	Input	F3	Switch
VSS0V_1	Output	N1	SMA
VDD1V8_1	Input	N13	SMA
VSS0V_2	Input	A13	Shorted to the PCB ground plane
r_out	Output	B6	BNC
r_ext_high_gen1	Input	C6	BNC
r_vdda	Input	A5	SMA
r_current_in_rampgen0	Input	B5	SMA
r_cap0_rampgen0	Input	A4	Switch
r_cap1_rampgen0	Input	C5	Switch
r_cap2_rampgen0	Input	B4	Switch
r_cap3_rampgen0	Input	A3	Switch
r_seed	Input	A2	BNC
r_seed_en	Input	C4	Switch
r_analog_monitor	Output	B3	BNC
VDD1V8_2	Output	A1	BNC

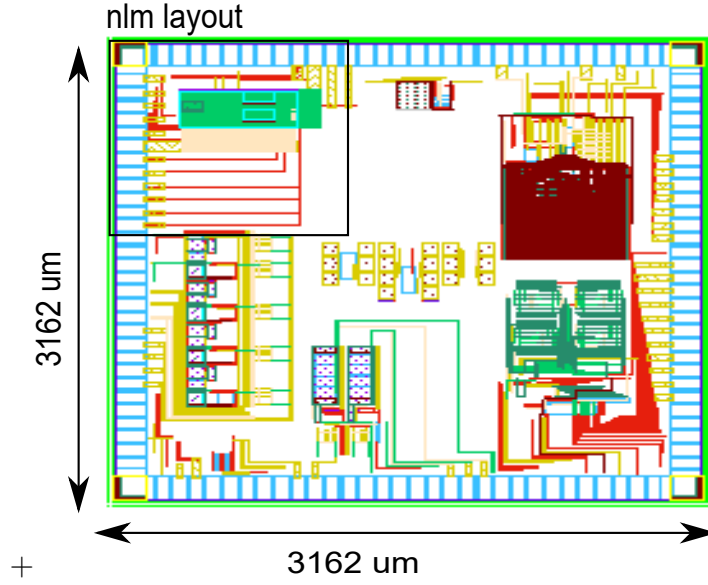


Figure 5.3: Snapshot of the final assembled die. The current work is shown as ‘nlm layout’ while the other portions of die include other unrelated circuits

- Arbitrary waveform analyser (D3) [120]
- Voltage source generator (D4 and D5) [121]
- Sony arbitrary waveform generator (D6)
- National current/voltage generator (D7).

As shown in figure 4.25, a monitor port was implemented on die to access the internal nodes. Table 5.2 depicts the various configurations to access the internal nodes. A voltage follower was implemented to isolate the internal nodes from the PAD and probe capacitance to avoid loading the internal nodes.

Table 5.2: Monitor port programmable

r_mon2	r_mon1	r_mon0	Internal Node
0	0	0	r_level_high_rampgen0
0	0	1	r_level_high_ramgen1
0	1	0	ramp0
0	1	1	ramp1
1	0	0	cmp_pos_gen0
1	0	1	cmp_pos_gen1

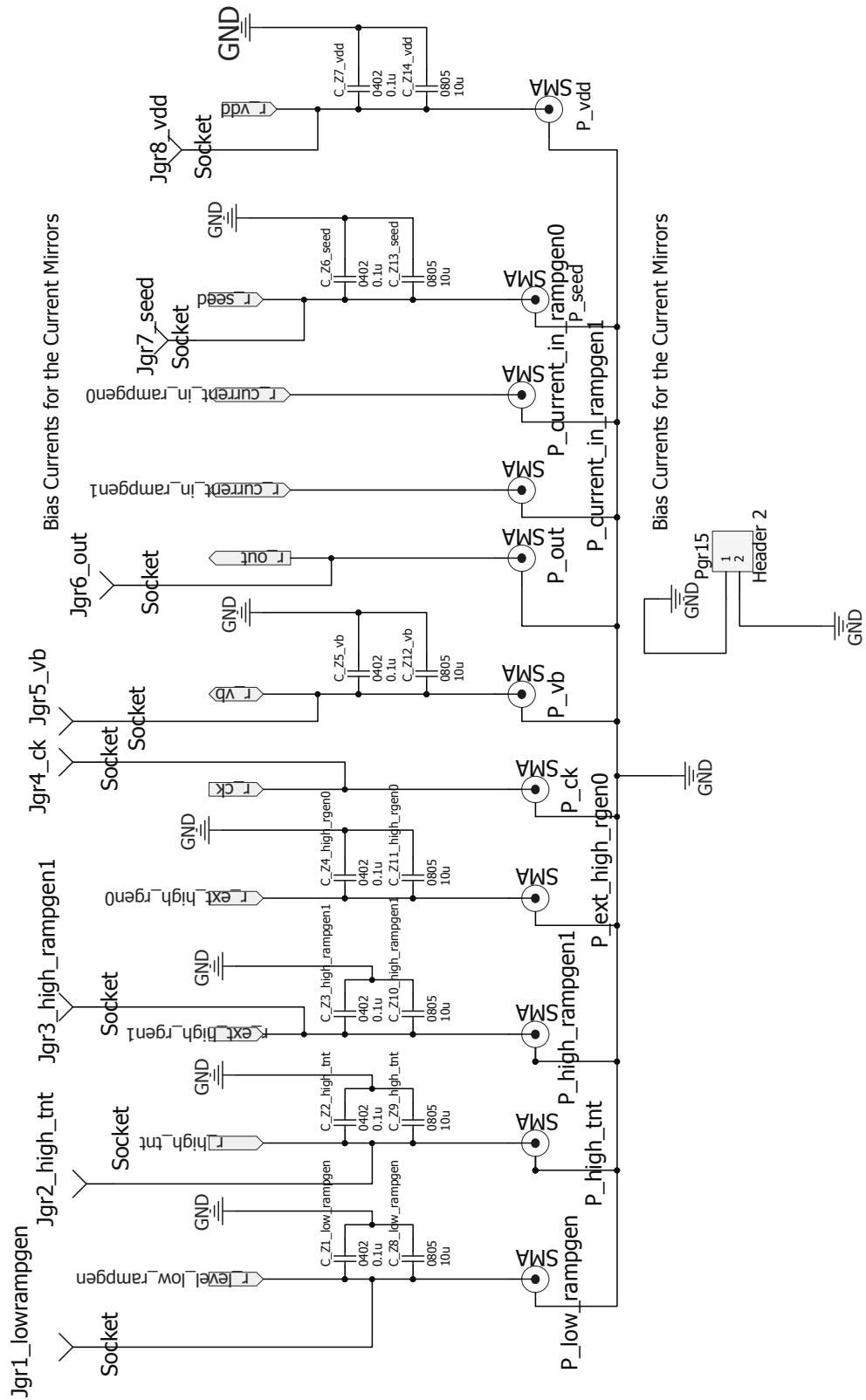


Figure 5.4: Bias Current Connections

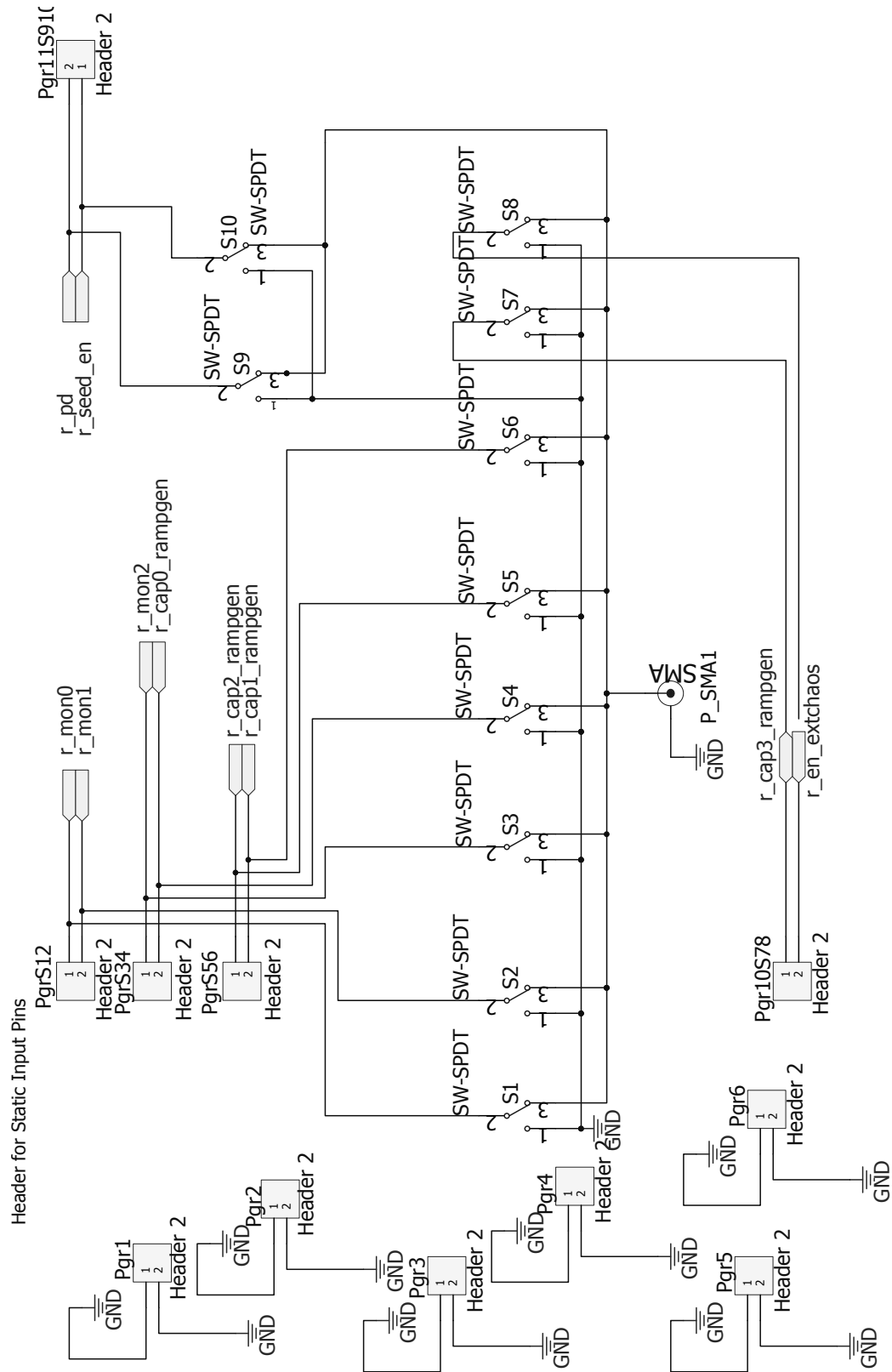


Figure 5.5: Configuration bits

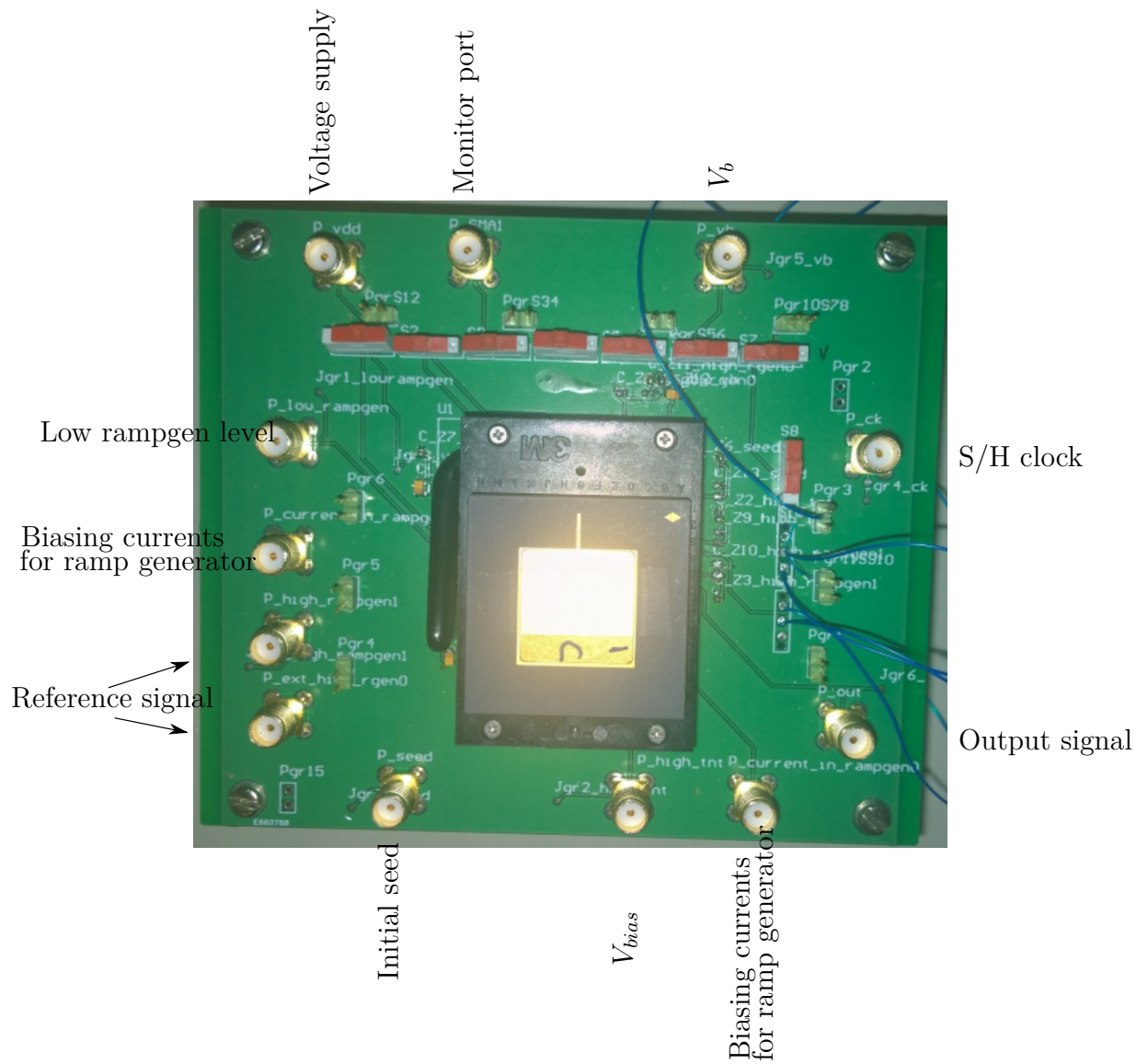


Figure 5.6: Assembled PCB with chip, filters and connectors

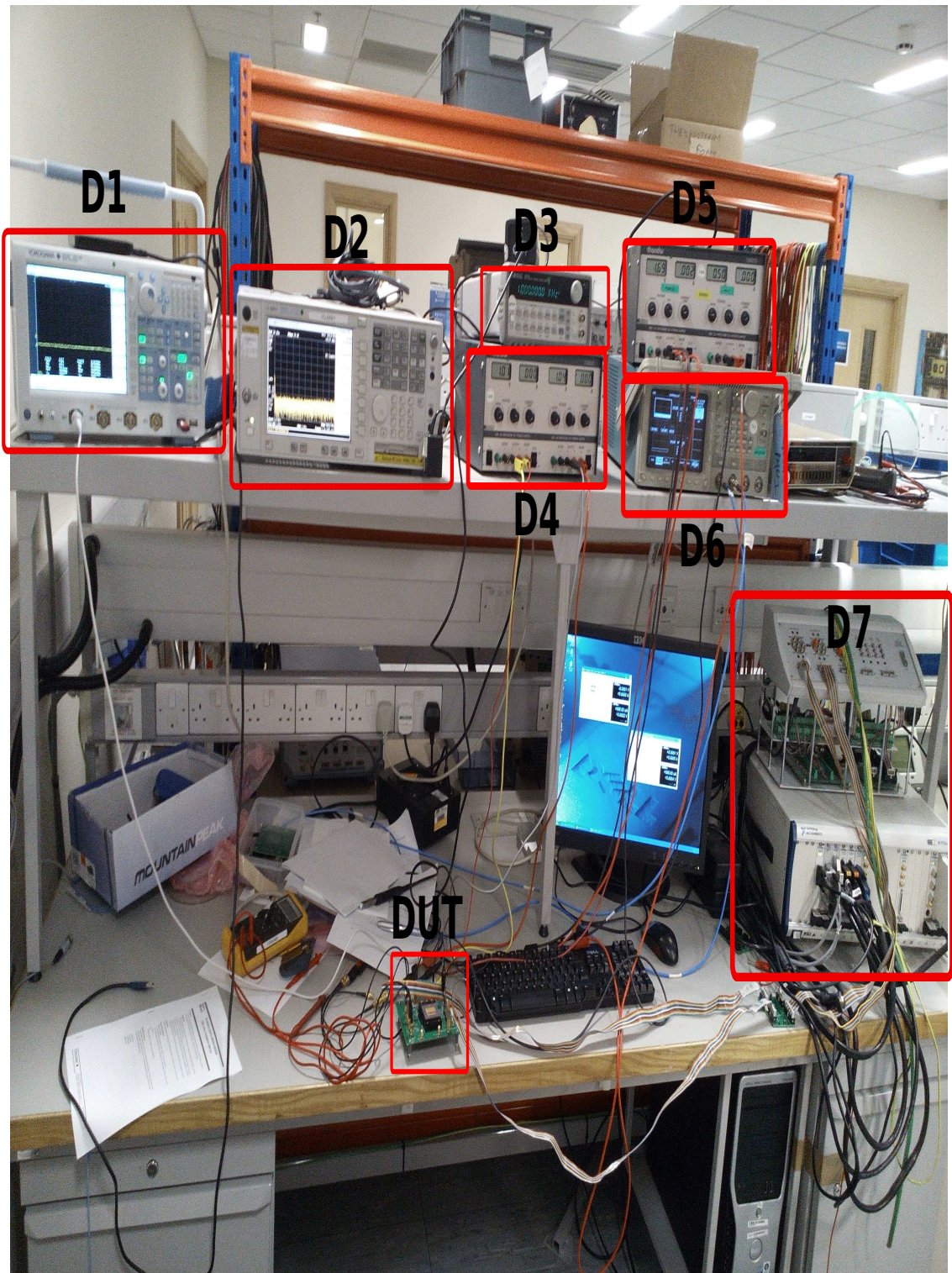


Figure 5.7: Test Setup. D1: Oscilloscope D2: Spectrum Analyzer D3: Arbitrary Waveform Generator D4: Voltage Source D5: Voltage Source D6: Arbitrary Waveform Generator DUT: Design Under Test D7: National Instruments Current Source

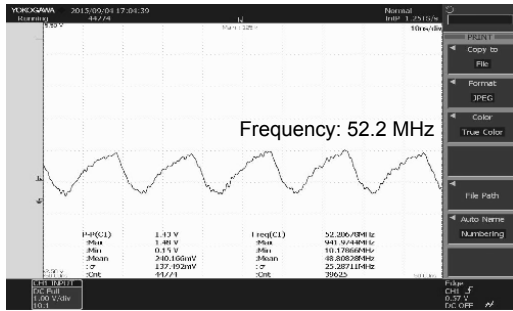
5.1.1 Silicon Measurements

5.1.1.1 Frequency Modulator Characterization

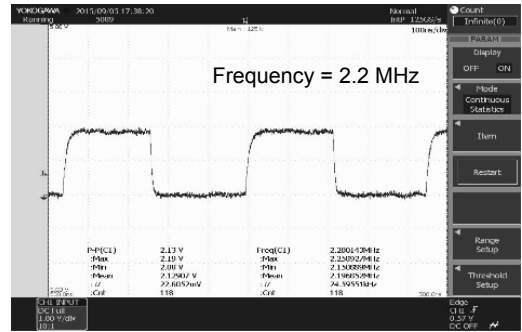
The chip was powered on by providing a ramped up power supply. The supply was ramped slowly to avoid any inrush currents. As described in section 4.3 the frequency could be varied by either changing the gradient of the ramp as shown in figure 4.1 or by changing the voltage reference as shown in figure 4.2. The incoming data stream was encoded by choosing the appropriate gradient either by changing the charging current or by choosing an appropriate capacitance or a combination of both. The capacitance could be selected by changing the decoder inputs, namely `r_cap3_rampgen0`, `r_cap2_rampgen0`, `r_cap1_rampgen0` and `r_cap0_rampgen0`.

Figure 5.8 depicts the two extreme cases: (a) highest frequency with $i_{charging}$ set to $100\mu A$, lowest capacitance (code 1110) (b) lowest frequency $i_{charging}$ set to $10\mu A$, largest capacitance (code 0000). The frequency could be lowered by choosing a lower current value. Due to limitations of the measurement equipment, a lower bound of $10\mu A$ was chosen. It can be seen that the gradient of the output signal is quite low. This is due to the high pad capacitance in $0.18\mu IBM$ technology. Figure 5.8 (c) shows the frequency information of figure 5.8 (a) captured on a spectrum analyser. As expected, it can be seen that the various harmonics lie on multiples of the base band frequency.

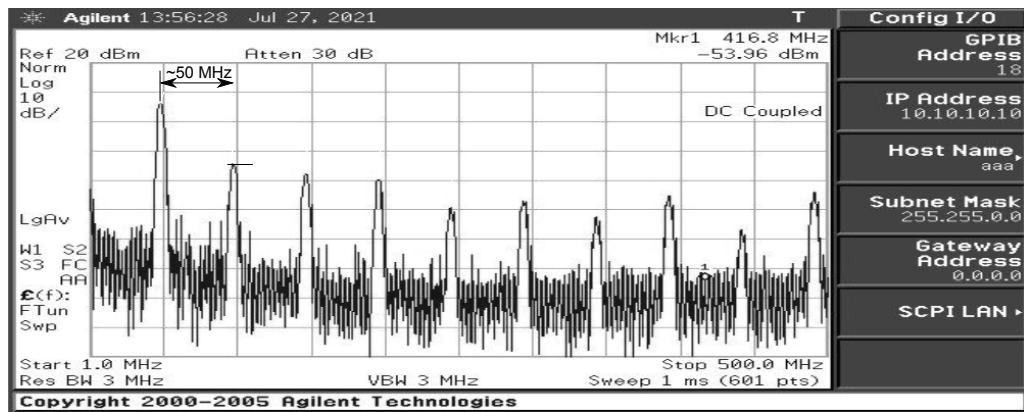
Detailed measurements were carried out for characterizing the chip across two current and capacitance bounds. Figure 5.9 shows the variation in frequency as the gradient of the ramp was changed by controlling the charging current with the current being varied in steps of $10\mu A$. It can be seen that for a low capacitance, the frequency remains more or less constant beyond a charging current of $50\mu A$. This is due to the fact that there is not a large enough change in the ramp gradient to



(a) Capacitance Setting:1110.
 $i_{charge}=100\mu m$



(b) Capacitance Setting:0000.
 $i_{charge}=10\mu m$



(c) Frequency Domain measured at spectrum analyser

Figure 5.8: Silicon measurements on unmodulated signal

cause a frequency increase.

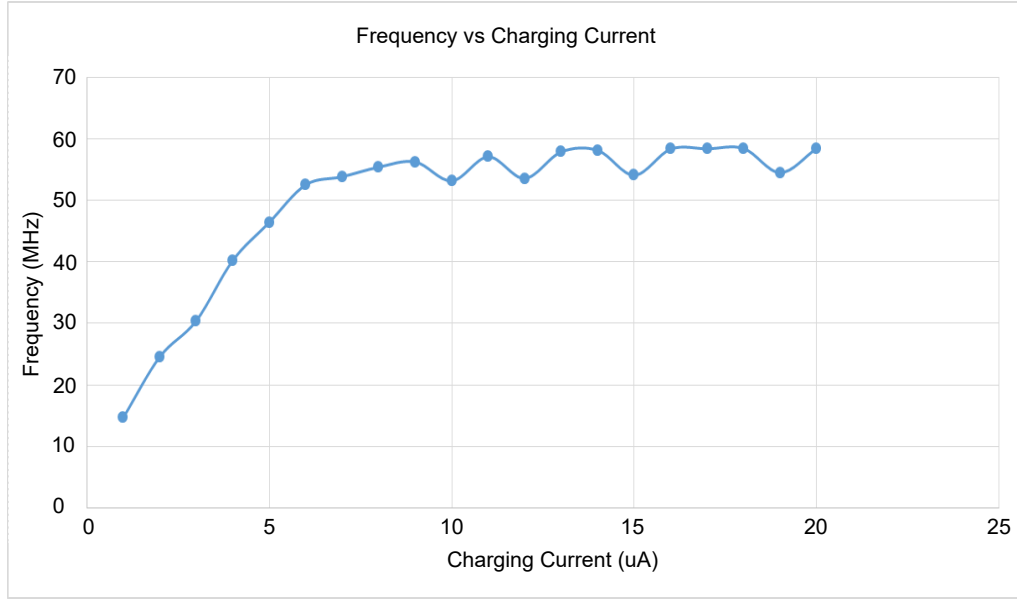


Figure 5.9: Measured Frequency vs Charging Current

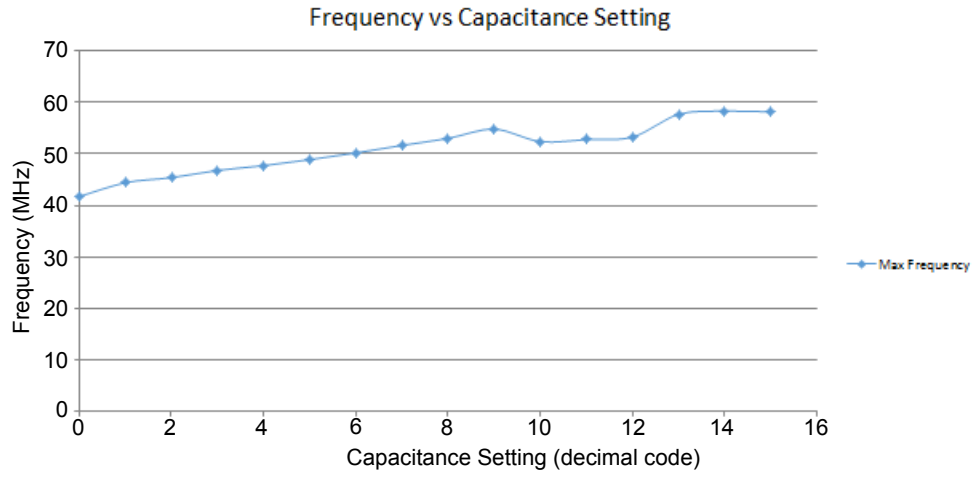
Figure 5.10 depicts the change in frequency as the gradient of the ramp is changed by controlling the capacitance setting. The capacitance can be varied by choosing an appropriate setting at the thermometer decoder. Table 5.3 lists code setting for selecting appropriate on-die MIM cap.

Two sets of data were measured, low current ($10\mu A$) and high charging current ($100\mu A$). As can be seen, for the current work, a max frequency of 60 MHz and a low frequency of approximately 4 MHz can be achieved for a reference voltage of 1V. Figure 5.10 (b) shows the simulated frequency vs silicon measurements.

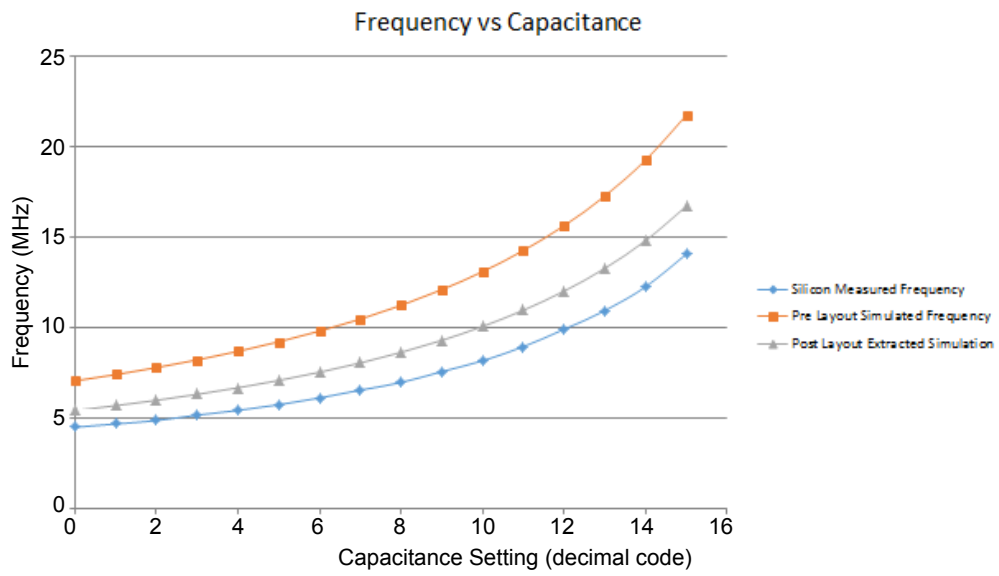
As discussed previously, the modulation of the frequency is obtained by changing the voltage level of the reference signal. Figure 5.11 shows the change in the frequency with the change in the voltage level from 0.5V to 1.5V. It can be clearly seen that by dynamically changing the reference signal for a given ramp gradient (setting the centre frequency), a frequency modulation can be achieved. It can be observed that there is a difference in the measured and the simulated frequencies.

Table 5.3: Thermometer Decoder Truth Table

capsel<3:0>	Corresponding Capacitance (fF)
0	464.3
1	433.3
2	402.4
3	371.4
4	340.5
5	309.5
6	278.6
7	247.6
8	216.7
9	185.7
10	154.8
11	123.8
12	92.85
13	61.9
14	30.95
15	No capacitance selected. Parasitic cap seen by the nodes.



(a) Charge Current:100uA, Reference Voltage Level:1V



(b) Charge Current:10uA, Reference Voltage Level:1V

Figure 5.10: Measured frequency vs capacitance load

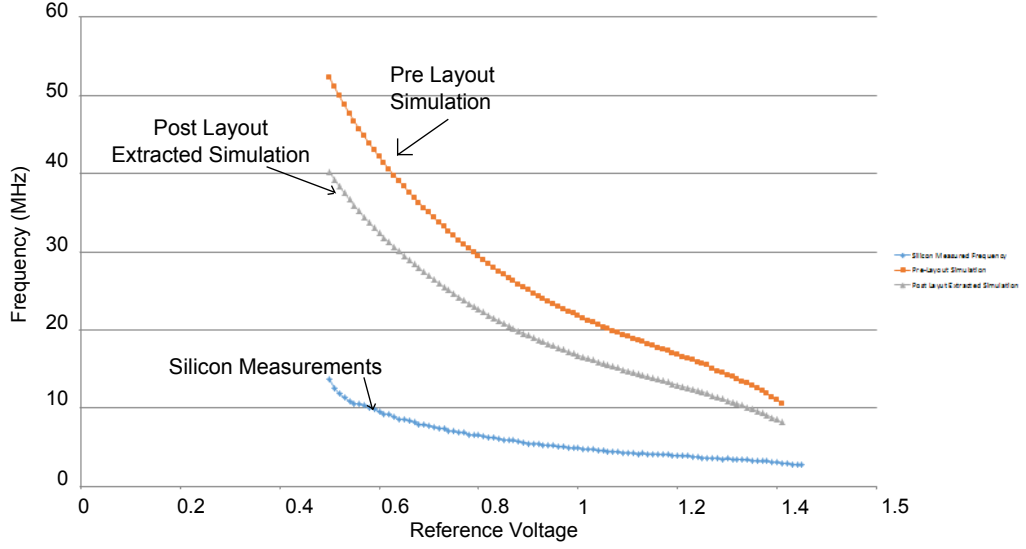


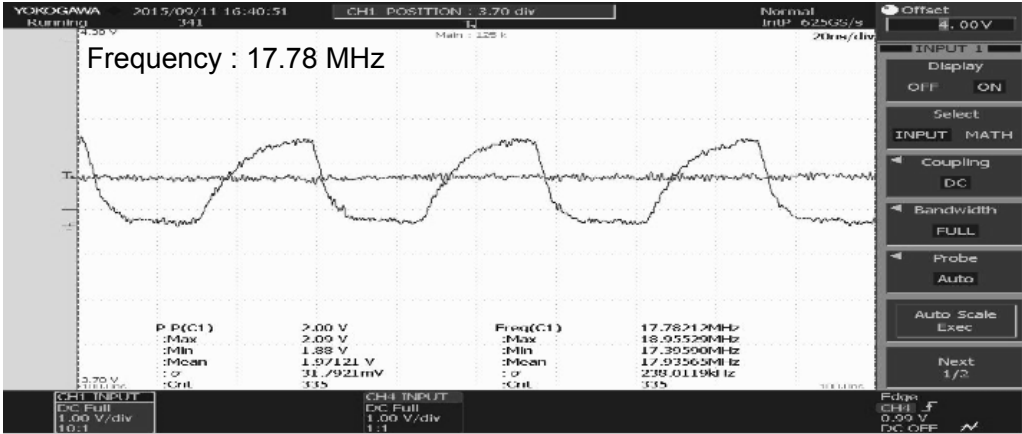
Figure 5.11: Measured frequency vs change in reference voltage for charge current of $10\mu\text{A}$, capacitance setting of 0 decimal, supply of 1.8V

It was noticed that there is around 20% difference between the post layout (extracted netlist) and the Silicon measurements. This points to the hypothesis that the interconnect models from the fab do not match well with Silicon. Another reason could be also the skew (the variability of fabrication process) over which the measurement were done. The extracted simulations were performed over a typical corner while the skew information of the silicon die was unknown.

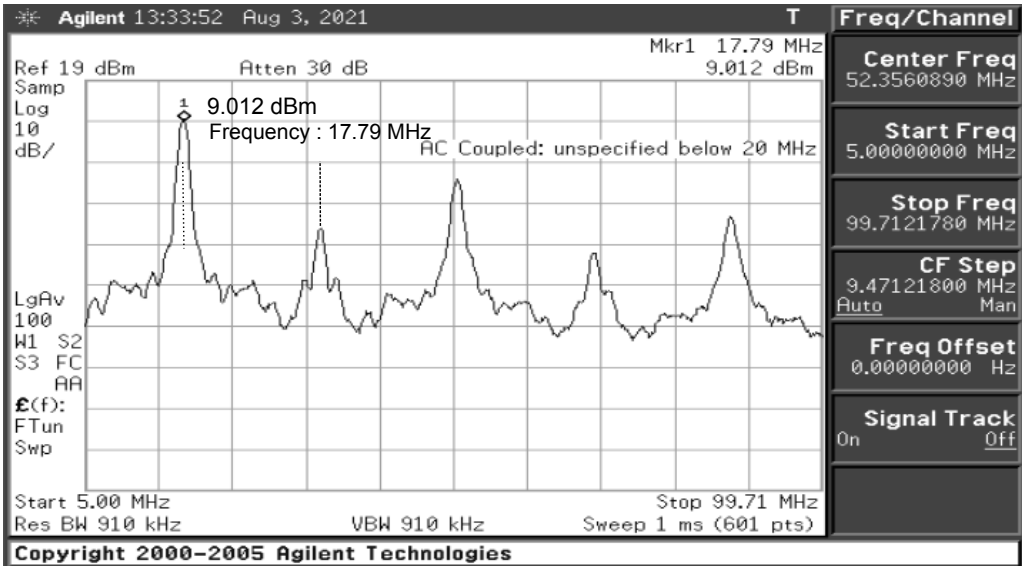
5.1.1.2 Frequency modulation measurements

A bypass circuit implemented for feeding the reference signal directly to the frequency modulator to study the impact of various modulation profiles. By configuring the pin 'r_en_extchaos' high (1.8V), the modulation pattern could be fed externally through the bypass switch. The aim of the measurements was to demonstrate that clock frequency modulation of the circuit follows the input pattern. For the various measurements, a centre frequency of 18MHz was chosen (setting: $i_{charging} = 10\mu\text{A}$, $cap_{code} = 15$) as shown in figure 5.12. A spectrum analyser was used to measure

the spectral density of the modulated signal, figure 5.12 (b). It can be noticed that sharp harmonics lie at the baseband frequency (approximately 18 MHz) and multiple of the base band.



(a) Unmodulated signal measured on Silicon

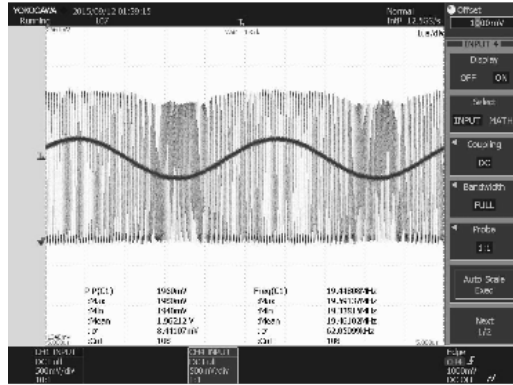


(b) Frequency spectrum of the unmodulated signal with peak power at 9.012 dBm

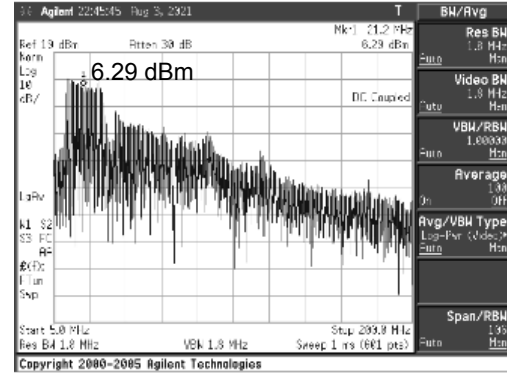
Figure 5.12: Umodulated measured clock on Silicon.

A single tone sinusoidal wave was applied as the reference signal (approximate frequency 750 kHz) as shown in figure 5.13 (a). The sine wave was applied to the reference signal (reference signal in 4.2). The reference signal is varied between 1.25V and 0.75V. Thus, the centre frequency relates to a reference signal level of

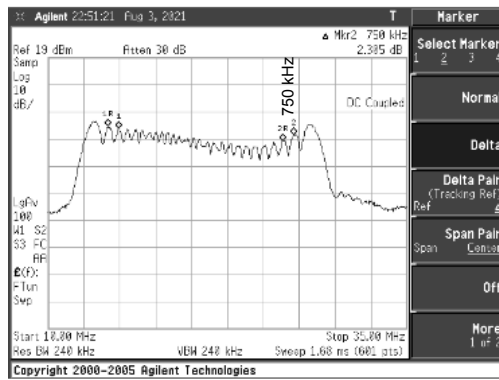
1V. It can be seen, figure 5.13 (b) that this leads to widening of the PSD around various harmonics as expected (section 2.1) with sub bands introducing additional harmonics spaced with the modulating frequency, figure 5.13 (c).



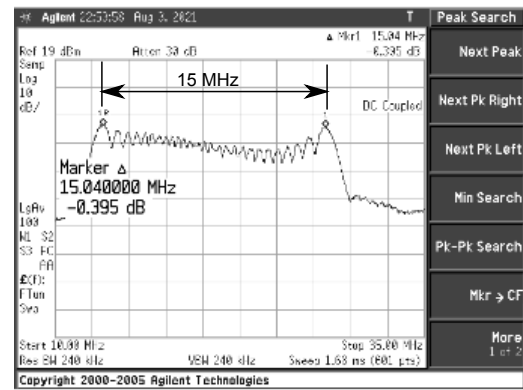
(a) Time domain measurement of the sinusoidal modulated signal



(b) Frequency spectrum with peak power at 6.29 dBm



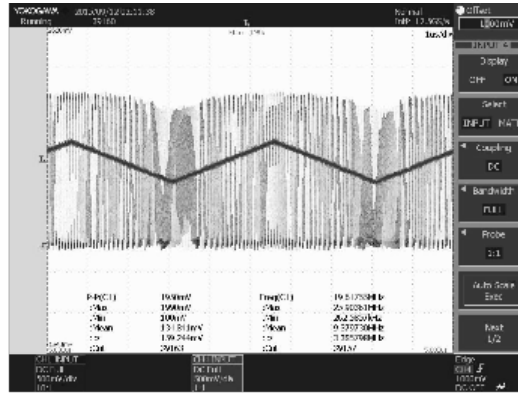
(c) Harmonics lying at modulation frequency: 750 kHz



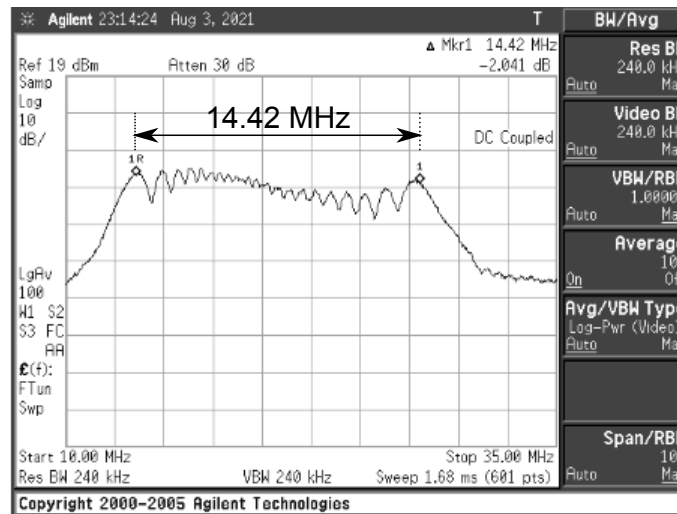
(d) Bandwidth of the modulated signal

Figure 5.13: Power spectral density for a sinusoidal modulated signal as measured on Silicon for $i_{charging} = 10\mu m$, centre frequency=18MHz, input supply=1.8V.

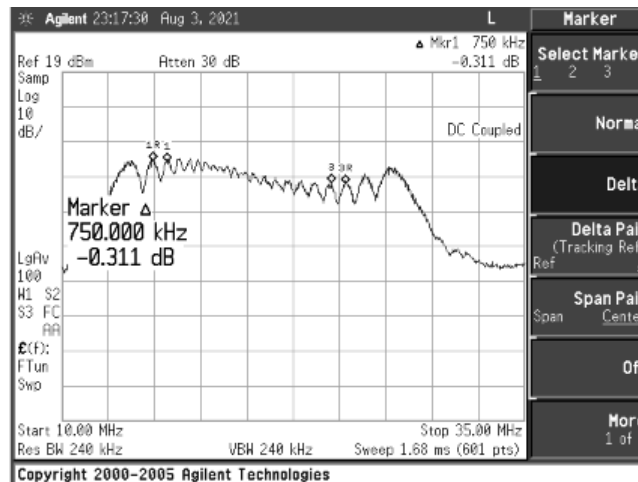
Next, a triangular modulation profile (200 kHz modulation profile) was applied in order to vary the reference signal (non-linear signal in 4.2) between 1.25V and 0.75V, figure 5.14 (a). As discussed in section 2.3, a flatter PSD is expected. It can be seen that the peak to trough, figure 5.14 (b), improved by 4dB compared to a sin wave modulation, figure 5.13 (c).



(a) Time domain measurement of the triangular modulated signal



(b) Frequency spectrum with peak power at 6.29 dBm



(c) Harmonics lying at modulation frequency: 750 kHz

Figure 5.14: Power Spectral Density for a triangular modulated signal as measured on silicon for $i_{charging} = 10\mu m$, centre frequency=18MHz, input supply=1.8V.

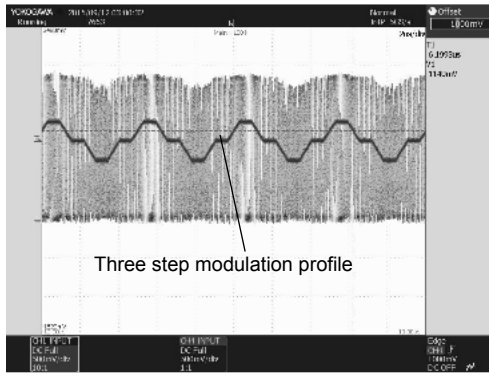
It can also be seen that in case of a step modulation, figure 5.15, energy is concentrated corresponding to the frequency steps. A 3 step reference signal, figure 5.15 (a), was applied to the test setup using the arbitrary waveform generator and bypassing the chaotic generator. As expected, unique peaks can be seen in the frequency spectrum (figure 5.15 (b)). Similarly, a 4 step reference signal leads to corresponding 4 peaks in the frequency spectrum, figure 5.15 (c), (d), while a 5 step reference signal leads to 5 peaks in the frequency of the modulated signal (figure 5.15 (d), (e)). As the number of steps are increased, the PSD becomes flatter. This is intuitive as an increasing number of steps would lead towards a triangular wave.

It can be seen, that the circuit is behaving well and the output frequency follows the change in the reference signal.

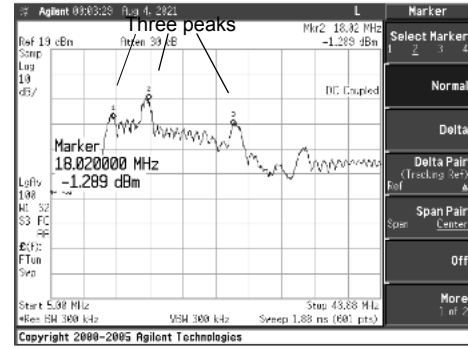
5.1.1.3 Chaotic Generator Measurements

A tent map chaos generator was also fabricated in the chip. As described in table 5.2, the output of the tent map generator could be accessed via the monitor port. It is interesting to recall that a capacitor S/H circuit was built with non overlapping S/H to avoid charge sharing issues. To avoid any charge leakage, a voltage follower was implemented on the hold side. However, parasitic MOS cap e.g. C_{gs} , C_{gd} would lead to some charge drop in the sampled value due to leakage current, both due to the self ESR (equivalent series resistance) of the sample/hold cap and also the ESR of the S/H cap of the following stage. This would determine the minimum operating frequency of the chaotic generator.

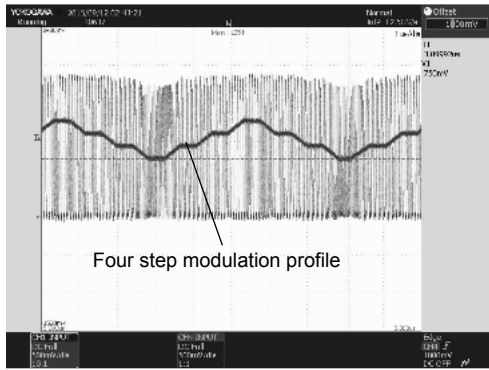
An initial seed can be programmed into the circuit through pin ' r_seed '. A transmission gate was implemented on-die to provide the initial seed. The transmission gate can be controlled using ' r_seed_en '. Table 5.4 enlists the various parameters that can be programmed.



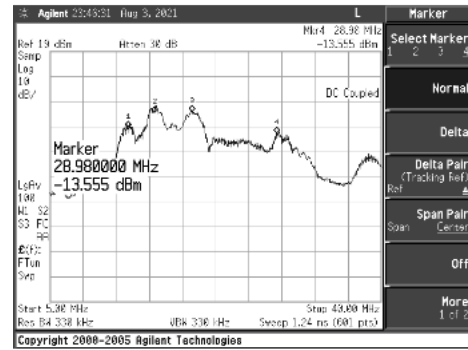
(a) Time domain measurement of the 3 steptriangular modulated signal



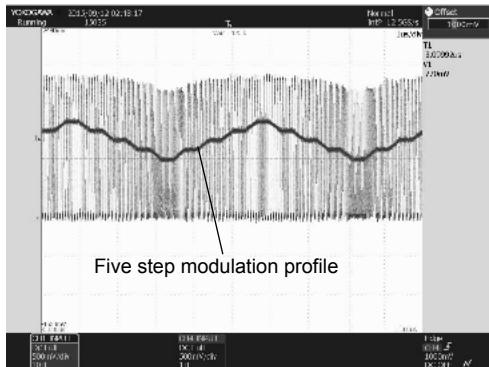
(b) Frequency spectrum of a 3 step triangular modulated signal



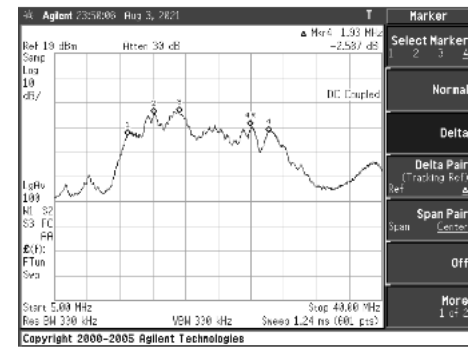
(c) Time domain measurement of the 4 step triangular modulated signal



(d) Frequency spectrum of a 4 step triangular modulated signal



(e) Time domain measurement of the 5 step triangular modulated signal



(f) Frequency spectrum of a 5 step triangular modulated signal

Figure 5.15: Power Spectral Density for a stair case modulated signal as measured on silicon for $i_{charging} = 10\mu m$, centre frequency= $18MHz$, input supply= $1.8V$.

Table 5.4: Programmable parameters for fabricated on chip tent map generator

Parameter	Pin Name	Description
V_b	r_vb	Bias voltage against which the tent map is compared for x_{n+1} .
Initial Seed	r_seed	Initial seed to the chaotic map
V_{high}	r_high_tnt	For the current implementation, chose as $2r_V_b$
ck_{sample}	r_clk	Sample and hold clock.
en_{seed}	r_seed_en	Control signal for enabling seed into the tent map

The various measurements were done for V_b : 0.5V. Thus, equation 4.2 becomes

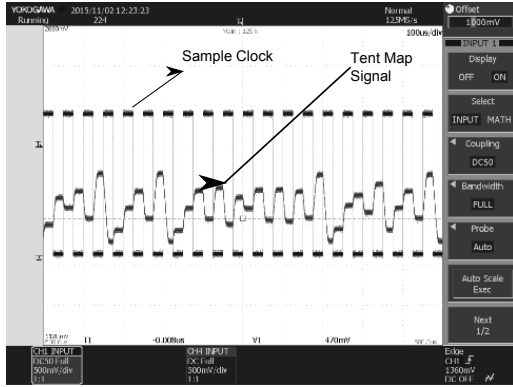
$$\begin{cases} x_{k+1} = 2.x_k & x_k < 0.5 \\ x_{k+1} = 2.(1 - x_k) & x_k \geq 0.5 \end{cases} \quad (5.1)$$

translating into the well known chaotic tent map equation.

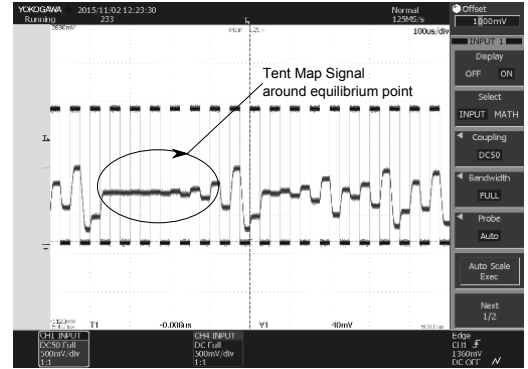
A $20kHz$ sampling clock was used for sampling and updating the next sample, x_{n+1} . A seed of 0.33 V was applied to the chaos generator and then let to free run with a sample clock of 10 kHz. Figure 5.16 (a) depicts the sample clock and the chaotic output signal. It can be seen in figure 5.16 (b) that the next iteration of the signal is either on $2x_k$ or $2(1 - x_k)$ depending on the current value of the iteration point. It can be observed, as discussed in section 4.3.1, that when the tent map hits the equilibrium point, it takes time to come out. This effect can be seen on silicon measurements in figure 5.16 (b).

Two measurements were taken over 250 ms time period for seed values of 0.33V and 0.48V. The chaotic signal was saved as a csv filed and a frequency of various sampled points was calculated as shown in figure 5.17 (a) and (b). It can be seen that the various bins occur with similar probability around the 0.39V to 0.89V bins. The frequency of bins varies with the seed value and also the sample time (figure 5.18 was taken over 500 ms).

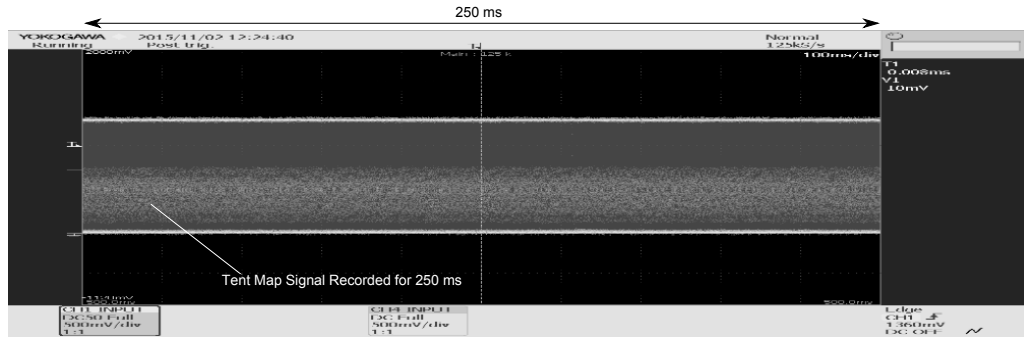
The generated on die chaotic signal is fed to the frequency modulator by disabling



(a) Silicon Measured plot for a seed value 0.33

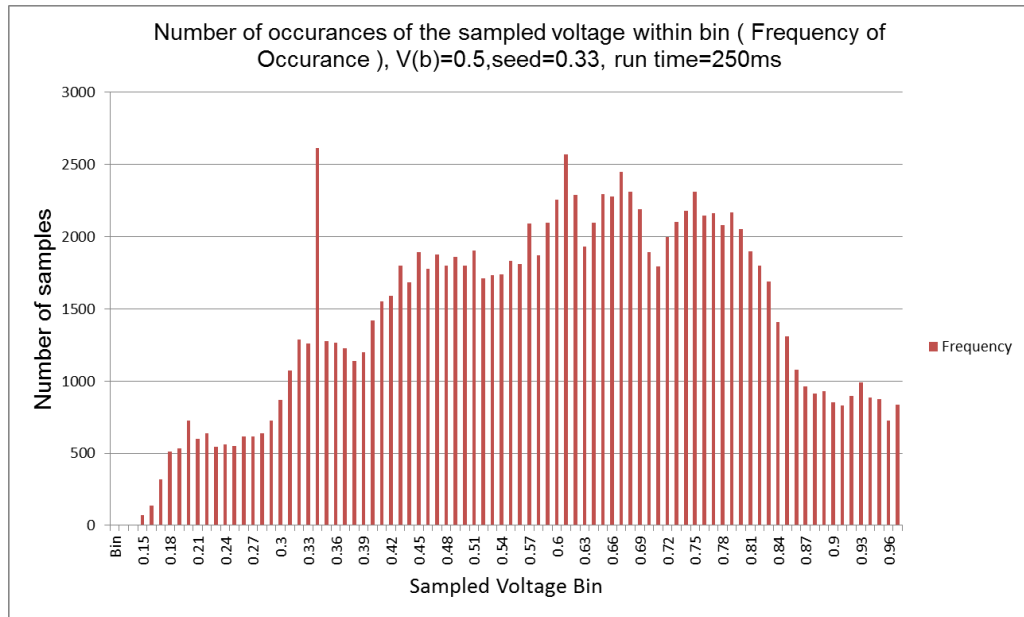


(b) Zoomed tent map signal from silicon measurement

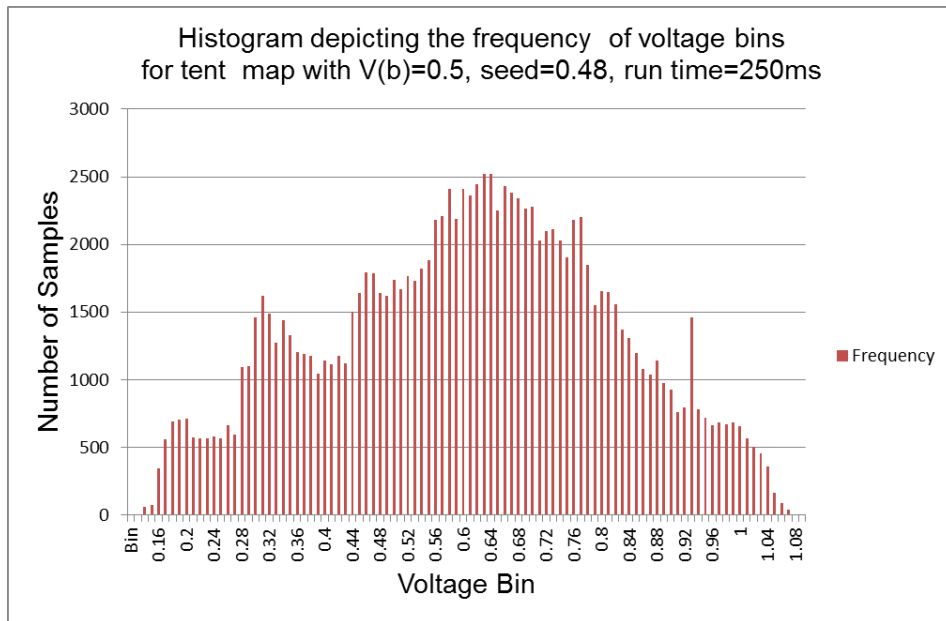


(c) A 250ms sample on silicon to generate statistical data

Figure 5.16: Measurements of the tent map circuit on silicon



(a) Histogram of sampled voltage for $V(\text{initialseed}) : 0.5$



(b) Histogram of sampled voltage for $V(\text{initialseed}) : 0.48$

Figure 5.17: Tent map sampled voltage frequency

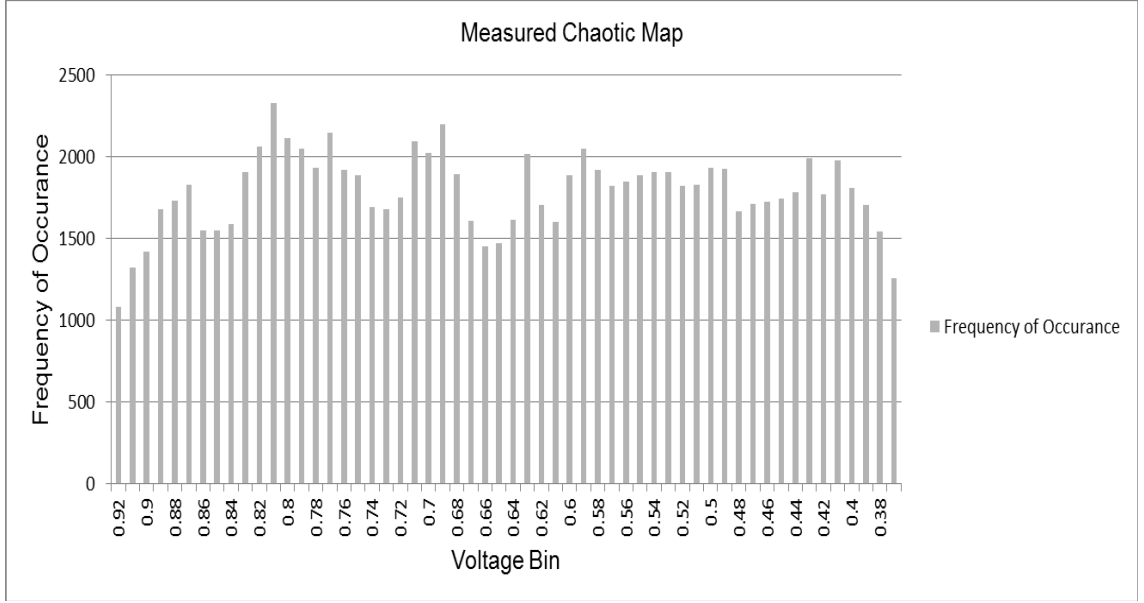


Figure 5.18: Measured plot for a seed value 0.33

the bypass switching ' $r_en_extchaos = low$ '. Referring to figure 5.17 (a), (b) it can be seen that the chaotic signal generated on die varies between 150mV to 960mV. The chaotic signal forms the reference signal for ramps to be compared against as discussed in section 4.2. For the cases where the chaotic signal is lower than the threshold of the transistor, the frequency modulator does not generate a clock edge. Figure 5.19 shows the modulation of the generated signal when the on die generated chaotic tent map signal is applied to the frequency modulator. The chaotic signal becomes the reference signal as discussed earlier. The chaotic signal was probed using the $r_analog_monitor$ port while the clock was probed using the $r_outport$. It can be seen that when the chaotic signal is below the threshold voltage of the transistor no clock edge is produced.

One of the proposed solutions around the issue is to generate bounds around the chaotic map or to operate the chaotic map at half the supply (both ground and vdd) of the frequency modulator supply, thus ensuring that the chaotic signals do not go out of bounds.

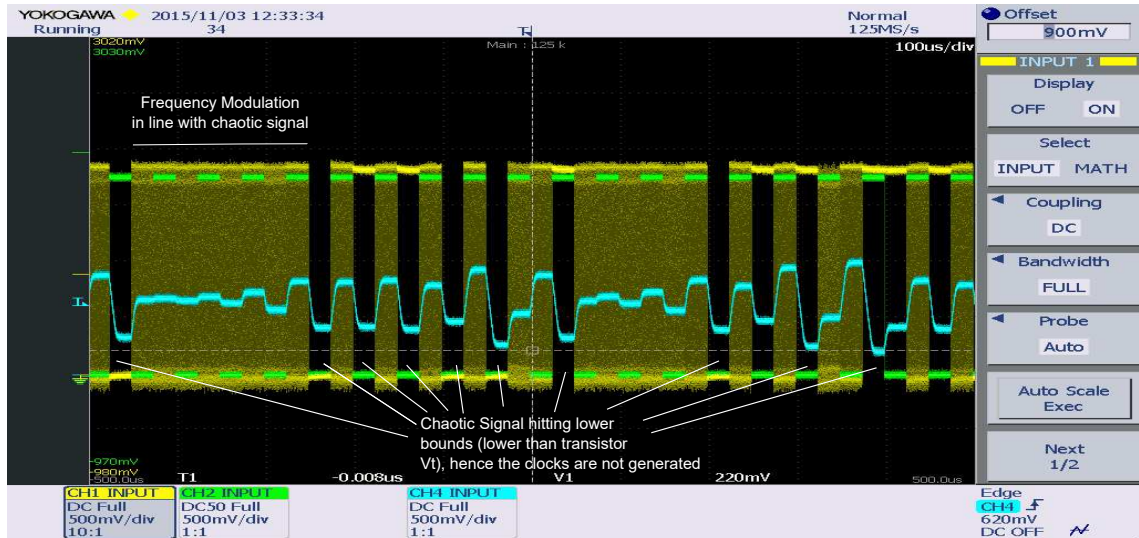


Figure 5.19: Chaotic Modulation of the frequency

To test the hypothesis, two test patterns were loaded into the chip using Textronics arbitrary waveform generator 33210A [122]. The csv file was converted into a .wvf and sent to the chip by bypassing the on die chaotic generator. The sampling frequency of the chaotic signal was kept to half of the clock generated by the frequency modulator. Figure 5.20 illustrated a case where the chaotic signal is unbounded. It can be seen that when the chaotic signal is low, the clock edge is not produced. When the chaotic signal is above approximately 400mV, the edge appears again.

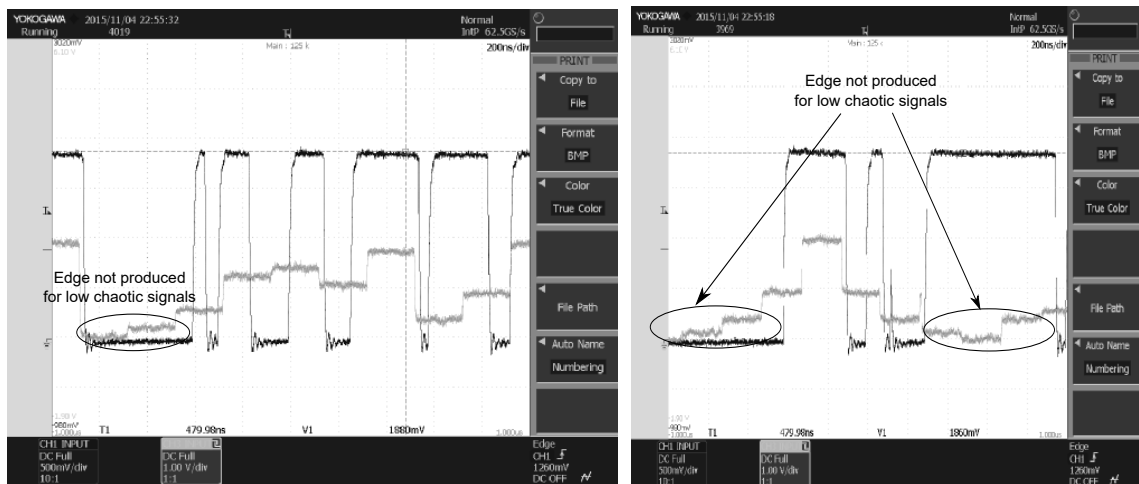


Figure 5.20: Frequency modulation with external unbounded chaotic signal.

Figure 5.21 depicts a case where the chaotic signal is bounded. In this case, whenever the chaotic signal is lower than 0.4 V, a random number is generated (using Microsoft Excel) and added to the chaotic signal. It can be observed in figure 5.21 (two samples taken) that the edge is modulated at every change in the chaotic signal.

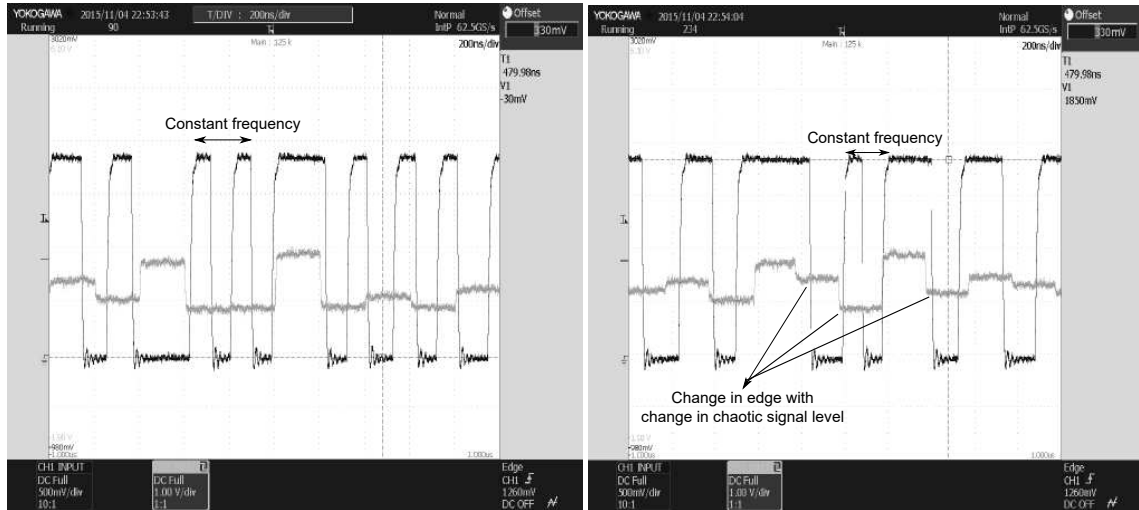


Figure 5.21: Frequency Modulation with external bounded chaotic signal. The chaotic signal is always greater than 400mV.

5.2 End of chapter remarks

The current chapter described the measurement setup and the various measurements performed on Silicon. The chip has been shown to be functional and performing as expected from simulations.

6 Conclusion

THE research work presented in this thesis proposes a low power, low emission media access control (MAC) compliant frequency shift keying transmitter to operate within wireless body area networks (WBANs). Spread spectrum techniques have been utilized to lower the peak power of the FM modulated signal. Traditionally, phase locked loops have been used to generate the modulated signals. The current research focuses on an open loop approach to lower the power and also enable the jitter function to be independent of the PLL response. An open loop topology was proposed utilizing a chaotic modulation profile. It was shown that chaotic modulation provides a better modulation technique for lowering the EMI. In addition, open loop modulators consume lower power compared to PLL based approaches.

A verilogA model was built to test the complete transmitter channel using a 10s single channel sleep related EEG recording. The EEG signal was converted into a binary bit stream by a 12 bit analog to digital converter followed by a parallel to serial converter. Frequency modulation was achieved by utilizing a ramp to encode the bit stream derived from the EEG signal into two distinct frequencies. The negotiated frequency of operation for dynamic frequency shifting and frequency encoding was achieved changing the gradient of the ramp thorough the load capacitance and the charging current in the charge pump. The work was implemented on a $0.18\mu m$ AMS

technology and the results presented.

6.1 Publications and Presentations

The following publications have arisen from this work.

- Ruchir Saraswat, Esther Rodriguez-Villegas, “A low emission, low power non-linear frequency modulation based transmitter for implanted devices” 35th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC), 2013, Pages 826 - 829
- Ruchir Saraswat, Esther Rodriguez-Villegas, “Chaotic inductively coupled non-PLL low emission transmitter for implanted devices” IEEE 5th Latin American Symposium on Circuits and Systems (LASCAS), 2014, Pages 1-4
- Ruchir Saraswat, Esther Rodriguez-Villegas, “Low power EMI mitigation strategies utilizing non-PLL based periodic and chaotic SSC profiles for implanted devices”, IEEE International Symposium on Medical Information and Communication Technology (ISMICT), 2014
- Saraswat, Ruchir ; Abbasi, Mohammad Usaid ; Rodriguez-Villegas, Esther, “Ultra-Low Power, Low Noise MAC Protocol Compliant Non-PLL based Wearable Transmitter for Dynamic Open Spectrum Sharing” IEEE Neural Engineering Research Conference (IEEE-NER), 2015
- Abbasi, Mohammad Usaid ; Raikos, George ; Saraswat, Ruchir ; Rodriguez-Villegas, Esther, “A high PSRR, ultra-low power 1.2V curvature corrected Bandgap reference for wearable EEG application”, IEEE New Circuits and Systems Conference (NEWCAS), 2015
- Ruchir Saraswat, Esther Rodriguez-Villegas, “Low Emission, Open Loop MAC

Protocol Compliant Implantable FSK Modulator”, IEEE New Circuits and Systems Conference (NEWCAS), 2016

- Invited Talk

- Organizer: Hermes Partnership in cooperation with The Intervention Centre of Oslo University Hospital and COST Action IC0905 - TERRA

- Sponsor: European Union Commission

- Title of workshop: Workshop on Sensor Communications & Technologies, Body Area Networks, e-health Services and Standardization. Sponsor

- URL for talk and slides: <http://www.hermes-europe.net/workshops/workshop-ismict-2014/>

- Title of talk: Low Power EMI Mitigation Strategies for Implanted Devices

6.2 Future Direction

The next phase of this research is to test the link with coupled inductors. As discussed, chaotic systems are very sensitive to initial conditions. For the decoding the bit stream, the modulating signal needs to be replicated at the receiver side. However, since a small amount of noise can also create a different trajectory for the chaotic transfer function, a scheme needs to be developed to correctly decode at the receiver.

The current media access control protocols propose to achieve optimal frequency utilization by shifting the operating frequency away from the noisy channel. It was shown in the current work, that the proposed circuit is capable of working with the DOSS protocol. A further improvement can be achieved by wave shaping the PSD of

the chaotically modulated signal. By performing both frequency shift and spectrum shaping, further reduction in radio interference might be achieved.

6.2.1 Specific Improvements to the proposed circuit

Supply Voltage

The circuits proposed have been designed with 1.8V power supply. However, for implantable systems, a 1.2 V operation is required. Thus, it would be desirable to optimize the circuits to enable integration within implantable systems. [21]

Calibration

As discussed in Chapter 4, any offset in the comparators would lead to frequency errors. One good solution around this would be to calibrate the various analogue blocks to remove any DC offset. One common approach is to insert an additional differential pair to the input stage of the comparator and introduce nullifying currents to remove any DC offset [123].

Although the current focus of this research was to transmit encoded bits, the current work can be used to generate on die SSC clocks for lowering the emissions on computer platforms. Similarly, the proposed circuits could also be used to generate jittered SSC PWM (pulse width modulated) clocks for DC-DC converters.

Chaotic Generator

It was shown during the silicon measurements and simulations that the current frequency modulator is unable to react to low values of the chaotic generator. One way to resolve this issue is to bound the chaotic generator around a minimum and

maximum values. One issue with this could be a loss of certain frequency bands. In addition, since the lower bound signal would be adjusted to a specific value, a peak will be produced at the corresponding frequency. Hence, extra care would be needed.

It can be observed in figure 5.20 and figure 5.21 that the duty cycle of the modulated signal varies when the chaotic signal iteration occurs. Special care needs to be taken when choosing the sampling frequency of the S/H circuit not to allow the change of the chaotic signal at same instance as the clock signal.

As was shown in Chapter 4, chaotic modulation leads to an increase in noise floor at the sidebands. This needs to be further investigated to enable the attenuation of the peak in PSD only within the desired sidebands.

Power Supply Rejection

The current work has not looked into the jitter introduced due to the power supply and this could be a critical parameter for system. Since the ramps follow the reference signal, it can be inferred that any noise in the reference signal could lead to a one on one jitter in the output clock. One potential improvement would be to supply a low noise stable voltage supply to the critical circuits such as the ramp generator and the chaotic signal (on any reference signal generator). A proposal was published to utilized a high power supply rejection ratio bandgap to generate a stable power supply [124].

Antenna Design

The current work proposes a frequency shift keying based approach to transmit data through inductive link [18]. A primary design consideration for the antenna

are in vivo losses due to tissue absorption, antenna size, and choice in operating frequency. A brief summary of signal transmission through the body is introduced in appendix 7.1. A coupled inductor need to be designed in the MICS frequency range and studies needs to be carried out to quantify the improvement in EM interference to other receivers coupled to various physiological implants.

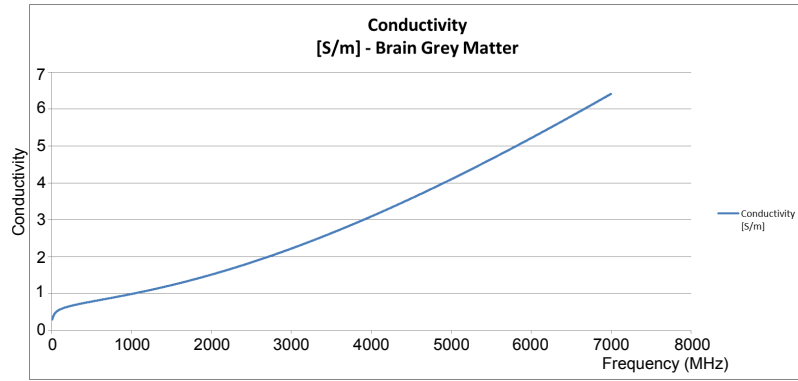
7 Appendix

7.1 Propagation of Radio Waves within Human Body - A brief review

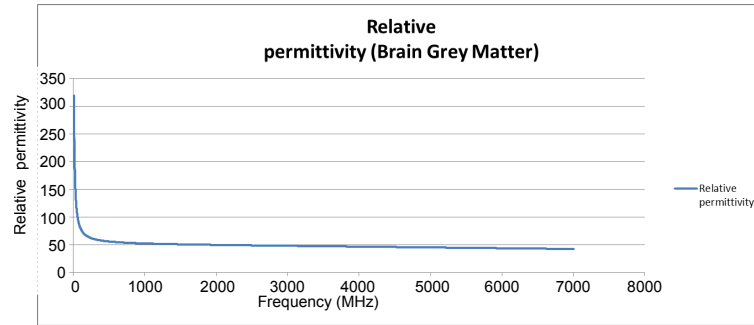
The current work proposes a frequency shift keying based approach to transmit data through inductive link [18]. A primary design consideration for the antenna are in vivo losses due to tissue absorption, antenna size, and choice in operating frequency. The operating frequency range [44] of the medical implants has been divided by FCC to lie within kHz range, MedRadio - 401 - 457 MHz [46], Wireless Medical Telemetry Services (WMTS): 608 – 614 MHz, 1395 – 1400 MHz, 1427 – 1432 MHz [47] , ISM bands 902-928MHz, 2.4-2.483 GHz, 5.725-5.875GHz.

The impact of operating frequency has been characterized in detail [4]. It was shown that the electrical properties of the biological tissue is highly dependent on the frequency of operation [125]. To assist researchers, an online data base for dielectric properties of bodily tissues has been made available by Italian National Research Council [17]. Dielectric data was generated from 10 MHz to 7GHz to cover the various operating frequencies regulated by FCC for the brain grey matter. Figure 7.1 (a) depicts the variation of the conductivity of the brain grey matter between 10 MHz and 7GHz. It can be seen that the conductivity drops significantly

from 6.42 S/m at 7GHz to 0.22 S/m for 10MHz. Similarly, the relative permittivity of the brain grey matter varies from 319.67 at 10 MHz to 0.3898 at 7GHz. The attenuation properties of a dielectric may be described by ‘penetration depth’. This is the depth at which the amplitude of a penetrating wave will be attenuated to $1/e$ of its initial value. The penetration depth for the brain grey matter is depicted in figure 7.2.



(a) Conductivity of brain grey matter vs frequency



(b) Relative permittivity of brain grey matter vs frequency

Figure 7.1: Dielectric Properties of Brain Grey Matter. The data has been generated from [17]

The data indicates at low frequencies the magnetic fields are well penetrable in biological media. Bashirullah et al. [18] used a complete electrical model of an American male to determine the radiation characteristics. As expected, as the operating frequency is lowered, the radiations penetrate deeper within the tissue as

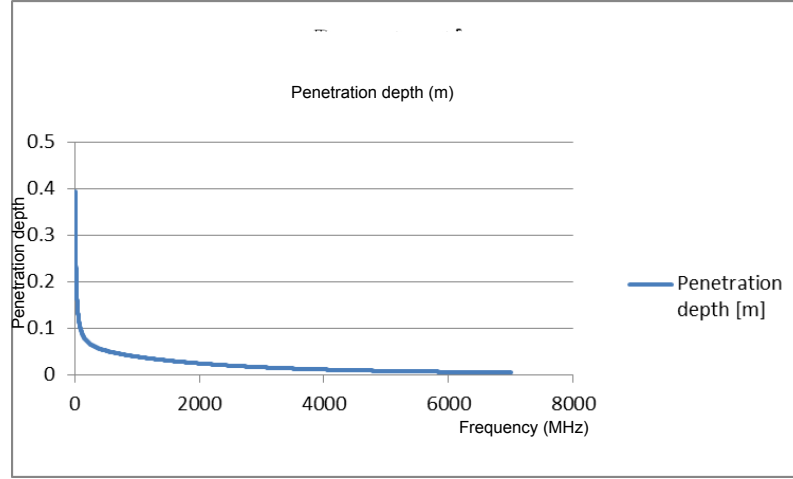


Figure 7.2: Penetration depth of brain grey matter. The data has been generated from [17]

illustrated in figure 7.3.

7.2 Chaotic Systems

The term chaos used in the current work refers to a non-linear system if it exhibits sensitive dependence on initial conditions and has an infinite number of different periodic responses. If a system's state space trajectories originating from two-closely spaced initial conditions diverge exponentially then can then be said that the system exhibits sensitive dependence on initial conditions and is known as a chaotic system. An important observation is that the chaos is not the result of noise or interference. However, in actual implementation this might add on to the deterministic chaos generated. One of the well-known examples of a map is the logistic function given by

$$x_{n+1} = rx(1 - x_n) \quad (7.1)$$

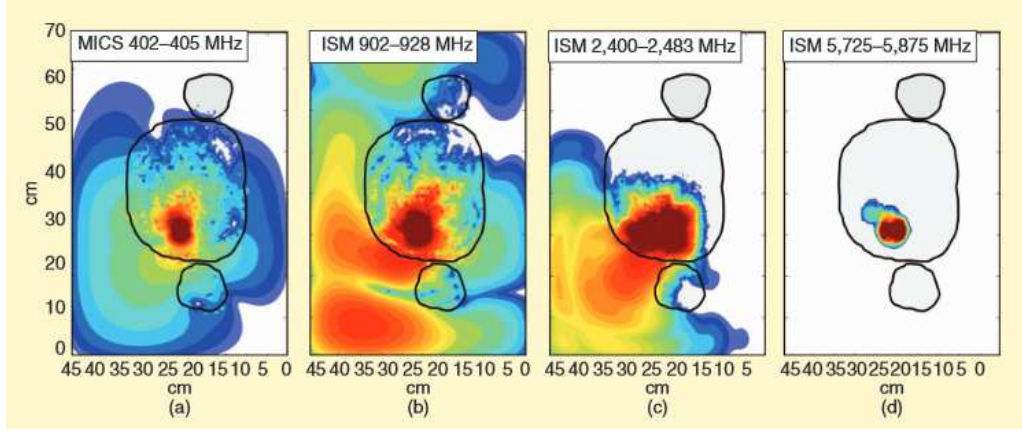


Figure 7.3: Cross section of human body model torso indicating the normalized radiation field intensity contours generated by a 14mmx3mm zig-zag dipole antenna in (a) MICS 402-405 MHz (b) ISM 902-928 MHz (c) ISM 2.4-2.483 GHz (d) 5.725-5.875 GHz FCC frequency bands. The smaller circles are the arms of the subject. Re-drawn from [18]

For certain values of parameter r , e.g $r=4$, the system exhibits chaotic behaviour.

The current work utilizes a tent map function given by

$$\text{Case 1: } x_n \in \left[0, \frac{1}{2}\right)$$

$$x_{n+1} = 2 \cdot x_n \tag{7.2}$$

$$\text{Case 2: } x_n \in \left[\frac{1}{2}, 1\right]$$

$$x_{n+1} = 2(1 - x_n) \tag{7.3}$$

The name tent map is derived from the shape of the transfer function shown in figure 7.4.

An important parameter defining the chaotic systems is called the Lyapunov exponent. A map is chaotic when its Lyapunov exponent is positive [72]. The Lyapunov

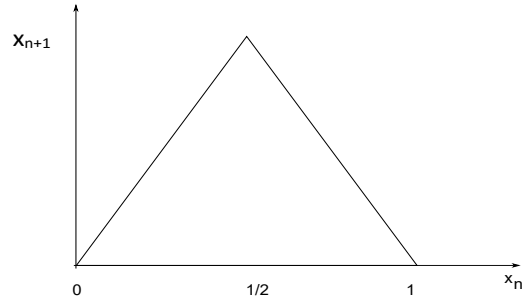


Figure 7.4: Pictorial Representation of Tent Map

exponent of the tent map is given as:

$$\lambda(x_0) = \ln 2 \quad (7.4)$$

Since λ is positive the tent map is chaotic.

One way to study the chaotic maps is to plot the cobweb diagram. The cobweb plot makes use of a plot of the mapping and a plot of the reference line $y = x$. From these two curves the iterative sequence can be constructed. Figure 7.5 depicts the cobweb plot for a $\mu = 2$ and a starting value of 0.22 generated using Matlab, appendix 7.4.5. Starting at that value on the x-axis, moving vertically upwards provides y-value of the first iterate. Next, moving horizontally until reference line $y = x$ provides the x-coordinate and is the value of the next iterate. Next, moving vertically to the intersection with graph of $\text{cobwebtent}(x)$ gives the y-coordinate which forms the second iterate. The steps can be repeated to get the third iterate and subsequent iterations.

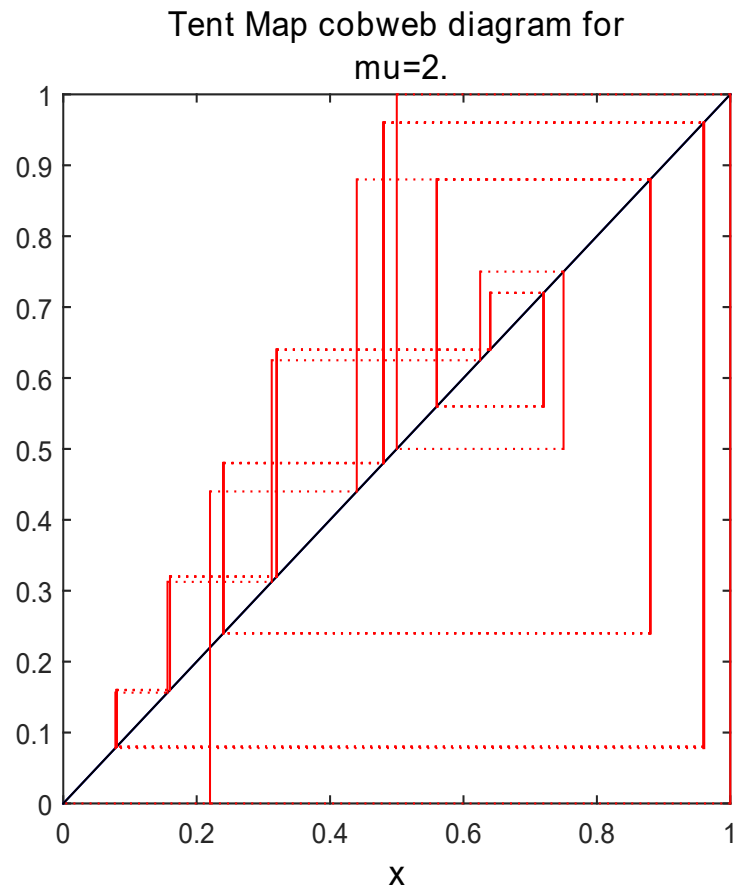


Figure 7.5: Cobwebb diagram for tent map with seed=0.22

7.3 Verilog A Model Codes

7.3.1 VCO Model

Given below is the complete behavioural model of a VCO running at 2.5 GHz and providing both a sine wave and a square wave.

```
//-----
//
```

Description: Verilog A VCO Model // Usage : Used to study the affects of various spread modulation profiles

```

`include "discipline.h"

`include "constants.h"

// vcomodel

// - VCO voltage controlled oscillator (VCO)

// in:  data inputs [V,A]

// vout:  [V,A]

// INSTANCE parameters

// vref = reference voltage that conversion is with respect to [V]

// vtrans = transition voltage between logic high and low [V]

// tdel,trise,tfall = {usual} [s]

// MODEL parameters

// {none} module vcomodel (vco_in, vco_out, vco_outdig, enableb); input
vco_in, enableb; output vco_out, vco_outdig; electrical vco_in, enableb;

// vco_vin is vco control input value.  Center freq is achieved when vco_vin
=

// iin_nominal_value.  electrical vco_out, vco_outdig;

parameter real vin_nominal_value = 0.5 from (0:inf);

parameter real center_freq = 2G;

parameter real vco_gain = (0.5*center_freq);

parameter real vlogic_high = 1.05;

parameter real vlogic_low = 0;

parameter real vtrans=(vlogic_low+vlogic_high)/2 from (vlogic_low:vlogic_high);

```

```

// logic threshold level parameter real tdel = 0 from [0:inf);

parameter real trise = 100p from (0:inf);

parameter real tfall = trise from (0:inf);

real ctrlnrm, vcoout;

// vco output real sinusoidal;

real phase_lin, phase_nonlin;

// function to get logic value at node
`define L(node) (V(node)>vtrans)

analog begin

@ ( initial_step or initial_step("dc") )

begin

vcoout = 0;

end

// --- VCO --- ctrlnrm = V(vco_in)/vin_nominal_value;

// sinusoidal wave + phase_lin = center_freq * $abstime;

phase_nonlin = idt( vco_gain*(ctrlnrm-0.5), 0 );

sinusoidal = sin(2*`M_PI*(phase_lin + phase_nonlin));

// form rectangular wave by catching transistions

// catch rising transition.

@ (cross(sinusoidal, +1)) vcoout = 0;

// catch falling transition

@ (cross(sinusoidal, -1)) vcoout = 1;

```

```

// vco is disabled?

if ('L(enableb)) vcoout = 0;

// VCO output

V(vco_out) <+ ('L(enableb)) ? vlogic_low : sinusoidal

* (vlogic_high-vlogic_low) + vlogic_low;

V(vco_outdig) <+ transition((vcoout) ? vlogic_high : vlogic_low, tdel,
trise, tfall);

end

endmodule

//-----

```

7.3.2 Analog to Digital Convertor

```

// VerilogA for r_2012_chip_c, adc_sixbit, veriloga

`include "constants.vams"

`include "disciplines.vams"

module adc_sixbit(vout,vin,vclk,s_out);

input vin,vclk;

output [11:0] vout;

output s_out;

electrical [11:0] vout;

electrical vin,vclk;

electrical s_out;

```

```

parameter real trise = 0 from (-inf:inf);

parameter real tfall = 0 from (-inf:inf);

parameter real tdel = 0 from (-inf:inf);

parameter real vinh = 0 from (-inf:inf);

parameter real vinl = 0 from (-inf:inf);

parameter real voh = 0 from (-inf:inf);

parameter real vol = 0 from (-inf:inf);

parameter real vth_clk = 0 from (-inf:inf);

parameter real vth_bit = 0 from (-inf:inf);

real vref;

real midref;

real sampledV;

real vdout[11:0];

real pow2[12:0];

real code,power_base,output_range;

integer i,j,k,m;

analog

begin

@(initial_step)

begin

vref = (vinh-vinl)/2 + vinl;

midref = vref / 2;

```

```

output_range = (voh-vol);

generate j(11,0)

begin

vdout[j] = 0;

end

pow2[0] = 1.0;

for (k=1; k<=12;k=k+1)

pow2[k]=2.0 * pow2[k-1];

end

@(cross(V(vclk) - vth_clk, 1))

begin

sampledV = V(vin);

for (i = 11; i >= 0 ; i=i - 1)

begin vdout[i] = 0;

if (sampledV > vref)

begin vdout[i] = voh;

sampledV = sampledV - vref;

end

else

begin

vdout[i] = vol;

end

end

```

```

sampledV = sampledV * 2;

end code = 0.0;

generate m (11,0)

begin

if (vdout[m] < vth_bit)

power_base = 0.0;

else

power_base = pow2[m]; #

code=code+power_base;

end

code = output_range/(pow2[12]-1) * code;

end

generate i ( 11,0)

begin

V(vout[i]) <+ transition(vdout[i], tdel, trise, tfall);

end

V(s_out) <+ transition(code,tdel,trise,tfall);

end

endmodule

```

7.3.3 Parallel to Serial Convertor

```
// VerilogA for r_2012_chip_c, p2s, veriloga
```

```

`include "constants.vams"

`include "disciplines.vams"

module p2s(a0,a1,a2,a3,a4,a5,a6,a7,a8,a9,a10,a11,clk,out);

input clk;

input a0,a1,a2,a3,a4,a5,a6,a7,a8,a9,a10,a11;

output out;

voltage a0,a1,a2,a3,a4,a5,a6,a7,a8,a9,a10,a11;

voltage clk;

voltage out;

parameter real vth_clk = 0 from (-inf:inf);

parameter real ttr = 10e-12 from (-inf:inf);

parameter real tdelay = 0 from (-inf:inf);

real vout;

integer counter;

analog

begin

@(initial_step)

begin

counter = -1;

end

@(cross(V(clk)-vth_clk,1))

begin

```

```

counter = counter + 1;

if (counter > 11) counter = 0;

if (counter == 0) vout = V(a0);

if (counter == 1) vout = V(a1);

if (counter == 2) vout = V(a2);

if (counter == 3) vout = V(a3);

if (counter == 4) vout = V(a4);

if (counter == 5) vout = V(a5);

if (counter == 6) vout = V(a6);

if (counter == 7) vout = V(a7);

if (counter == 8) vout = V(a8);

if (counter == 9) vout = V(a9);

if (counter == 10) vout = V(a10);

if (counter == 11) vout = V(a11);

end

V(out) <+ transition(vout,0,ttr);

end

endmodule

```

7.3.4 Current Digital to Analog Convertor

```

// VerilogA for r_2012_chip_c, vdac_2bit, veriloga

`include "constants.vams"

```

```

'include "disciplines.vams"

module vdac_2bit(s_in,in, dc_level, vclk,out,s_out);

input dc_level, vclk;

input [1:0] in;

input s_in;

output out,s_out;

electrical [1:0] in;

electrical s_in, s_out;

electrical dc_level, out, vclk;

parameter real vinh = 0 from (-inf:inf);

parameter real vinl = 0 from (-inf:inf);

parameter real voh = 0 from (-inf:inf);

parameter real vol = 0 from (-inf:inf);

parameter real vth_clk = 0 from (-inf:inf);

parameter real output_range = 0 from (-inf:inf);

parameter real trise = 10p from (-inf:inf);

parameter real tfall = 10p from (-inf:inf);

real code, power_base;

real pow2 [1:0];

real vth_bit;

real sampledV;

real vdout[5:0];

```

```

real vin_range, midref,vref;

real code2, power_base2;

integer i,j,k,m,n;

analog

begin

@(initial_step)

begin vin_range = (vinh-vinl);

vref = (vin_range)/2;

midref = vref/2;

generate k(1,0)

begin vdout[k] = 0;

end

vth_bit=(vinh+vinl)/2;

pow2[0] = 1.0;

for (i=1; i<=1;i=i+1) pow2[i]=2.0 * pow2[i-1];

end

@(cross(V(vclk)-vth_clk, 1))

begin

code = 0.0;

generate j (1,0)

begin

if (V(in[j]) < vth_bit)

```

```

power_base = 0.0;

else

power_base = pow2[j];

code=code+power_base;

end

code = output_range/(pow2[1]-1) * code;

sampledV = V(s_in); for (m=1; m>=0; m=m-1)

begin vdout[m] =0;

if (sampledV > vref )

begin vdout[m] = voh;

sampledV = sampledV - vref;

end

else

begin vdout[m] = vol;

end

sampledV = sampledV * 2;

end

code2 = 0;

generate n (5,0)

begin

if (vdout[n] < vth_bit)

power_base2 = 0.0;

```

```

else power_base2 = pow2[n];

code2 = code2+power_base2;

end

code2 = output_range/(pow2[1]-1) * code2;

end

V(out) <+ V(dc_level) + transition(code,0,trise,tfall);

V(s_out) <+ V(dc_level) + transition(code2,0,trise,tfall);

end

endmodule

```

7.3.5 Digital Controller for Phase Rotator Block

```

// Define perform phase rotation digital control.

// Generate mux-pi signal vectors according to desired freq. offset

//

// OPERATION:

//

// INCLUDE FILES:

#include "discipline.h"

#include "constants.h"

// Number of VCDL legs the main DLL has (phase steps)

#define NumberOfVCDLs 50

// Number of legs the phase interpolator has (fractional phase steps)

```

```

// Associated to LSB part of Phase accumulator 'Kpkase'

`define NumberOfPISteps 4

//

module drsd_MSCG_muxpi_digctl_cougar(ckin, pdir, poffs1, poffs0, mxsel,
intp, reset, quad, kph, kint);

input ckin;

electrical ckin;

output [`NumberOfVCDLs-1:0] mxsel;

electrical [`NumberOfVCDLs-1:0] mxsel;

// mux branch select (1 out of 'NumberOfVCDLs)

output [1:0] intp;

electrical [1:0] intp; //phase interpolation value (0..NumberOfPISteps-1)

input pdir, poffs1, poffs0, reset;

electrical pdir, poffs1, poffs0, reset; // phase selection digital value
[0..NumberOfVCDLs-1]

output [1:0] quad;

electrical [1:0] quad;

output kph, kint;

electrical kph, kint;

parameter real VH=1.05, VL=0; // nominal input signal swing

parameter real Vthres=0.5*(VH+VL);

parameter real Tr=0.5n from (0:inf); // output rise time

```

```

parameter real Tf=Tr; // output fall time

parameter real ttol=Tr/10; // edge detect time tolerance

parameter real vtol=(VH-VL)/10; // edge detect voltage tolerance

parameter integer Debug=0; // debug printing flag

parameter integer Edge=1 from [-1:1]; // clock edge to trigger on

parameter integer Kinit=0 from [0:'NumberOfVCDLs); // initial/reset output
level

// Print step (for debugging)

real printtime;

`define PRINTSTEP 5n

// function to get logic value at node (returns 0 or 1)

`define L(node) (V(node)>Vthres)

integer Kphase; // phase mux out value as integer (0..NumberOfVCDLs-1)

integer Kinterp; // phase interpolator value as integer (0..NumberOfPISteps-1)

integer qsel; // current quadrant of phase counter

// 0: 315-0-45deg, 1: 45-90-135deg, 2: 135-180-225deg, 3: 225-270-315deg

integer ckHi; // clock state after edge occurs (0..1)

// integer j;

genvar j;

// direction flag

`define forward 1

`define reverse 0

```

```

//-----

//-----

analog function integer ADDPH;

input Count, Inc, dir;

integer Count, Inc, dir;

begin

ADDPH = Count + ((dir=='forward')? Inc: ((dir=='reverse')? -Inc: 0));

end

endfunction

analog function integer ADDWRAPPH;

input Count, Inc, dir, Nmax;

integer Count, Inc, dir, Nmax;

begin

ADDWRAPPH = ADDPH(Count, Inc, dir);

if (ADDWRAPPH >= Nmax) ADDWRAPPH = ADDWRAPPH-Nmax; // if overflow wrap

else if (ADDWRAPPH < 0) ADDWRAPPH = ADDWRAPPH+Nmax; // if underflow wrap

end

endfunction

//-----

analog begin

@(initial_step) begin

ckHi=(Edge==1); // clock state after edge.

```

```

Kphase=Kinit; // load initial output state.

Kinterp = 0;

printtime = 0;

end

//---- Phase rotator wrapping counter

@(cross(V(ckin)-Vthres, 0, ttol, vtol)) begin // On clock edge,

if (~L(reset) && (L(ckin)==ckHi)) begin // if not reset & proper edge,

'define DAC2(b1,b0) (((b1)? 2: 0)+(b0)? 1: 0)

Kinterp = ADDPH(Kinterp, 2*L(poffs1) + L(poffs0), L(pdir));

// Kinterp = ADDPH(Kinterp, 'DAC2(L(poffs1),L(poffs0)), L(pdir));

while (Kinterp >= 'NumberOfPISteps) begin

Kinterp = Kinterp-'NumberOfPISteps; // if overflow wrap

Kphase = ADDWRAPPH(Kphase, 1, 'forward, 'NumberOfVCDLs);

end

while (Kinterp < 0) begin

Kinterp = Kinterp+'NumberOfPISteps; // if underflow wrap

Kphase = ADDWRAPPH(Kphase, 1, 'reverse, 'NumberOfVCDLs);

end

end

end

if (L(reset)) begin

Kphase = Kinit; Kinterp = 0; // asynchronous reset signal.

```

```

end

//----- Output VCDL phase multiplexer selector:  one out of 'NumberOfVCDLs

// generate j (0,'NumberOfVCDLs-1)

for (j=0; j<'NumberOfVCDLs; j=j+1)

V(mxsel[j]) <+ transition( (Kphase==j)?  VH: VL, 0, Tr, Tf);

//----- Output phase interpol value

V(intp[0]) <+ transition( (Kinterp&1)?  VH: VL, 0, Tr, Tf);

V(intp[1]) <+ transition( (Kinterp&2)?  VH: VL, 0, Tr, Tf);

V(kph) <+ transition(Kphase, 0, Tr, Tf);

V(kint) <+ transition(Kinterp, 0, Tr, Tf);

qsel = floor((8*Kphase/'NumberOfVCDLs + 1) / 2) % 4;

V(quad[0]) <+ transition((qsel&1)?  VH: VL, 0, Tr, Tf);

V(quad[1]) <+ transition((qsel&2)?  VH: VL, 0, Tr, Tf);

if (Debug>0 && $abstime >= printtime) begin

$strobe("muxpictl t=%7.3f ns, Kphase=%d, Kinterp=%d", $abstime/1n, Kphase,
Kinterp);

printtime = $abstime+'PRINTSTEP;

end

end

endmodule

```

7.3.6 Periodic Delay Locked Loop

```

// Emulate a period locking DLL

```

```

// Number of VCDL legs the main DLL has (phase steps)

#define NumberOfVCDLs 100

// A simple periode detection algorithm tracks the frequency of the input
signal

// Model includes hysteresis so that noisy signals will still find reasonable

// Result: variable 'Per' contains the measured period time

THnew = last_crossing(V(ckin)-VHthres,1); // check for VHthresh cross

TLnew = last_crossing(V(ckin)-VLthres,-1); // check for VLthresh cross

if (THnew>THold+DeltaT) begin

if (THold>0) Pmeas = THnew-THold; // update period

THold = THnew; // save cross time

end

if (TLnew>TLold+DeltaT) begin

if (TLold>0) Pmeas = TLnew-TLold; // update period

TLold = TLnew; // save cross time

end

if (Pmeas>PerOld+DeltaT || Pmeas<PerOld-DeltaT) begin // whenever period
is updated,

if (PerOld==0) Per = max(Pmin,min(Pmax,Pmeas)); // first measurement.

else if (Pmeas<1.9*PerOld) // extrapolate new unless it missed a cycle:

Per = max(Pmin,min(Pmax,Pmeas+FracEst*(Pmeas-PerOld)));

PerOld=Pmeas; // save measured for next test.

```

```

end

// Form a Delay chain with 'NumberOfVCDLs legs total delay locked to period
time

// Result: Delayed output clock signals are stored into an array 'legout'
generate j (0,'NumberOfVCDLs-1)

legout[j] = transition((Lck)? VH: VL, 'EVADELAY(Per,j), Tr, Tf);

// End of Delay chain

```

7.3.7 Phase Selector Mux

```

// Digital unit clock generation

if (ck4phb) ck4phasel = floor((8*Kphase/'NumberOfVCDLs+1)/2) % 4;

if (ck4phc) ck4phbsel = ck4phasel;

if (ck4phd) ck4phcsel = ck4phbsel;

if (ck4pha) ck4phdsel = ck4phcsel;

// .. and drive 4 4 to 1 clock MUXes

// Result: output clock to digital control unit is: 'ck4pha'

// 4 times a 4:1 Cloxk MUXes. 180deg is 0deg inv, 270deg is 90deg inv.

case (ck4phasel)

0: ck4pha = 'L(ckin90);

1: ck4pha = ¡L(ckin0);

2: ck4pha = ¡L(ckin90);

default: ck4pha = 'L(ckin0);

```

```

endcase

case (ck4phbsel)

0:  ck4phb = ꝑL(ckin0);

1:  ck4phb = ꝑL(ckin90);

2:  ck4phb = 'L(ckin0);

default:  ck4phb = 'L(ckin90);

endcase

case (ck4phcsel)

0:  ck4phc = ꝑL(ckin90);

1:  ck4phc = 'L(ckin0);

2:  ck4phc = 'L(ckin90);

default:  ck4phc = ꝑL(ckin0);

endcase

case (ck4phdsel)

0:  ck4phd = 'L(ckin0);

1:  ck4phd = 'L(ckin90);

2:  ck4phd = ꝑL(ckin0);

default:  ck4phd = ꝑL(ckin90);

endcase

// End of Digital unit clock generation

```

7.4 Matlab Scripts

7.4.1 Generating the Power Spectral Density

```
% -----  
  
% MATLAB Script to generate the Frequency spectrum  
  
% Author:  Ruchir Saraswat  
  
% CID : 00448044  
  
% Dept.   : Department of Electrical and Electronics Engineering  
  
% -----  
  
% The waveform was stored by saving the output of the  
  
% PLL in the text format. The simulator chooses the % same time step as  
specified in the Cadence.  
  
% Tool used for simulation:  Lynx  
  
%-----  
  
% Load the VCO output profile from Cadence load  
  
% Vcodivout.out  
  
%-----  
  
% -----  
  
% Define the parameters in the array  
  
% Define the First Column as the time in MATLAB time = Vcodivout_0719(:,1);  
  
%-----
```

```

% Define the Second Column as the voltage point in MATLAB vcodivout = Vcodivout_C

%-----

% Plot the waveform in the MATLAB for sanity check figure(1);

plot(time,vcodivout,'r');

%-----

% Set Labels on figure 1

% Title of the Window title('vco div out');

set(gcf,'Name','vco div out clock');

% -----

% Set X Label xlabel('time (s)'); ylabel('volt');

% -----

% Take only points for t>0.5microsecond. The figure of

% 0.5 micro second is chosen because the PLL takes

% around 500 micro seconds to settle to the final

% value. Thus, %it makes sense to take the fourier

% transform of the

%clock signal beyond 0.5 micro

% seconds i1=find(time>.5e-6);

i1=i1(1);

otime = time(i1:size(time));

ovco = vcodivout(i1:size(time));

```

```

%-----

% Try fft from matlab help example (Mathematics)

N = size(otime);

N=N(1)

%-----

% allow only even numbers for N N = fix(N/2)*2;

Y = fft(ovco,N);

%-----

% Compute the power spectral density RN = 50;

Pyy = Y.*conj(Y)/(N*N / RN);

tstep=(otime(N)-otime(1))/(N-1);

f = 1./(N*tstep)*(0:N/2-1);

figure(2);

plot(f,Pyy(1:N/2));

title('Power spectral density');

set(gcf,'Name','Power spectral density');

xlabel('Frequency (Hz)');

%-----

% rescale frequency (zoom in) to fundamental freq. xlim([2.05e9 2.35e9]);

% there is a 3rd order harmonic because of rectangular signal shape

xlim([6e9 7e9]);

```

```

ylim([0 500]);

%-----

% try to find reference spurs left and right of fundamental freq.

% re plot result power in dB

plot(f,db(Pyy(1:N/2),'power'))

xlim([2.05e9 2.35e9]);

xlabel('Frequency (Hz)');

ylabel('Spectral power (dB)');

% Yupp, they are very small at fundamental +-100MHz ylim([0 1]);

%-----

% Find the maximum amplitude of the fundamental tone.

% Limiting vector P to plot window

WindowPyy = Pyy(find((f>2.05e9) & (f<2.35e9)));

db(max(WindowPyy),'power')

%-----

```

7.4.2 Studying the impact of Modulation Index on the modulation index

```

%-----%

% Description:The code has been written to study the impact of various

% parameters on SSC % Revision History

```

```

% Author : Ruchir Saraswat

% Contact : ruchir.saraswat@imperial.ac.uk

% Parameters to Enters

% fm_tone1 : Tone 1 Modulating Frequency

% fm_tone2 : Tone 2 Modulating Frequency

% fm_tone3 : Tone 3 Modulating Frequency

% fc : Carrier Frequency % beta_tone1 : Modulation Index for tone 1

% beta_tone2 : Modulation Index for tone 2

% beta_tone2 : Modulation Index for tone 3

%-----

clc;

clear all;

close all;

choice=input('Choose 1 for constant delta_f, 2 for constant fmod =');

fm_tone1=input('Tone 1 Modulating Frequency =');

fc=input('Carrier Frequency =');

beta_tone1=input('Tone 1 Modulation Index =');

beta_tone2=input('Tone 2 Modulation Index =');

beta_tone3=input('Tone 3 Modulation Index =');

beta_tone4=input('Tone 4 Modulation Index =');

delta_f =input('frequency deviation =');

```

```

ncycles=input('Number of modulation cycles');

%t=0:0.0001:0.1;

if (choice == 1) fmod_tone1=delta_f/beta_tone1;

fmod_tone2=delta_f/beta_tone2;

fmod_tone3=delta_f/beta_tone3;

fmod_tone4=delta_f/beta_tone4;

else fmod_tone1 = fm_tone1;

fmod_tone2 = fm_tone1;

fmod_tone3 = fm_tone1;

fmod_tone4 = fm_tone1;

end

fs= 4*fc;

T=1/fs;

fl=50000;

t = (0:fl-1)*T;

Fm=sin(2*pi*fm_tone1*t);

Fc=sin(2*pi*fc*t);

%fl=length(Fc);

plot(t,Fm);

xlabel('Time');

ylabel('Amplitude');

title('Modulating Signal');

```

```

grid on;

newplot;

Fmtone1=sin(2*pi*fc*t+(beta_tone1.*sin(2*pi*fmod_tone1*t)));

%Frequency changing w.r.t Message

Fmtone2=sin(2*pi*fc*t+(beta_tone2.*sin(2*pi*fmod_tone2*t)));

%Frequency changing w.r.t Message

Fmtone3=sin(2*pi*fc*t+(beta_tone3.*sin(2*pi*fmod_tone3*t)));

%Frequency changing w.r.t Message

Fmtone4=sin(2*pi*fc*t+(beta_tone4.*sin(2*pi*fmod_tone4*t)));

%Frequency changing w.r.t Message

%Calculating the fft of the modulated and carried frequencies

NFFT = 2^nextpow2(f1);

f=fs/2*linspace(0,1,NFFT/2+1);

%f1=2^ceil(log2(f1));

%f=(-f1/2:f1/2-1)/(f1*1.e-4);

% Calculating the FFT of a Single Tone Modulated Frequency

Fm_singletone_fft1=fft(Fmtone1,NFFT)/f1;

Fm_singletone_fft2=fft(Fmtone2,NFFT)/f1;

Fm_singletone_fft3=fft(Fmtone3,NFFT)/f1;

Fm_singletone_fft4=fft(Fmtone4,NFFT)/f1;

plot1=subplot(4,1,1);

plot(plot1,f,2*abs(Fm_singletone_fft1(1:NFFT/2+1)));

```

```

xlabel('Frequency (Hz)');

ylabel('Amplitude');

title('Impact of varying Modulation Index');

plot2=subplot(4,1,2);

plot(plot2,f,2*abs(Fm_singleitone_fft2(1:NFFT/2+1)));

xlabel('Frequency (Hz)');

ylabel ('Amplitude');

plot3=subplot(4,1,3);

plot(plot3,f,2*abs(Fm_singleitone_fft3(1:NFFT/2+1)));

xlabel('Frequency (Hz)');

ylabel('Amplitude');

plot4=subplot(4,1,4);

plot(plot4,f,2*abs(Fm_singleitone_fft4(1:NFFT/2+1)));

xlabel('Frequency (Hz)');

ylabel('Amplitude');

axis([plot1 plot2 plot3 plot4],[99e6 101e6 0 inf]);

```

7.4.3 Study the impact of number of tones in modulating signal

```

%-----
%
```

% Description:The code has been written to study the impact of various

```

% parameters on SSC

% Revision History

% Author : Ruchir Saraswat

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% Parameters to Enters

% fm_tone1 : Tone 1 Modulating Frequency

% fm_tone2 : Tone 2 Modulating Frequency

% fm_tone3 : Tone 3 Modulating Frequency

% fc : Carrier Frequency

% beta_tone1 : Modulation Index for tone 1

% beta_tone2 : Modulation Index for tone 2

% beta_tone2 : Modulation Index for tone 3

%-----

clc;

clear all;

close all;

fm_tone1=input('Tone 1 Modulating Frequency=');

fm_tone2=input('Tone 2 Modulating Frequency=');

fm_tone3=input('Tone 3 Modulating Frequency=');

fc=input('Carrier Frequency=');

beta_tone1=input('Tone 1 Modulation Index=');

beta_tone2=input('Tone 2 Modulation Index=');

```

```

beta_tone3=input('Tone 3 Modulation Index=');

ncycles=input('Number of modulation cycles=');

%t=0:0.0001:0.1;

t=0:1/(1000*fc):ncycles*(1/fm_tone1);

m=sin(2*pi*fm_tone1*t); subplot(4,2,1);

plot(t,m);

xlabel('Time');

ylabel('Amplitude');

title('Modulating Signal'); grid on;

c=sin(2*pi*fc*t); subplot(4,2,2);

plot(t,c);

xlabel('Time');

ylabel('Amplitude');

title('Carrier Signal');

grid on;

Fc=sin(2*pi*fc*t);

Fsawtooth=sawtooth(2*pi*fm_tone1*t);

Fmtone1=sin(2*pi*fc*t+(beta_tone1.*sin(2*pi*fm_tone1*t)));

%Frequency changing w.r.t Message

Fmtone2=sin(2*pi*fc*t+(beta_tone1.*sin(2*pi*fm_tone1*t))

+(beta_tone2.*sin(2*pi*fm_tone2*t)));

%Frequency changing w.r.t Message

```

```

Fmtone3=sin(2*pi*fc*t+(beta_tone1.*sin(2*pi*fm_tone1*t))
+(beta_tone2.*sin(2*pi*fm_tone2*t))+
(beta_tone3.*sin(2*pi*fm_tone3*t)));

%Frequency changing w.r.t Message

Fmtone1_tr=sin(2*pi*fc*t+(beta_tone1.*sawtooth(2*pi*fm_tone1*t)));
Fmtone2_tr=sin(2*pi*fc*t+(beta_tone1.*sawtooth(2*pi*fm_tone1*t))
+(beta_tone2.*sawtooth(2*pi*fm_tone2*t)));

%Frequency changing w.r.t Message

Fmtone3_tr=sin(2*pi*fc*t+(beta_tone1.*sawtooth(2*pi*fm_tone1*t))
+(beta_tone2.*sawtooth(2*pi*fm_tone2*t))+
(beta_tone3.*sawtooth(2*pi*fm_tone3*t)));

%Frequency changing w.r.t Message

subplot(4,2,3);

plot(t,Fmtone1);

hold on;

plot(t,Fmtone2);

xlabel('Time');

ylabel('Amplitude');

title('Single Tone FM Signal');

grid on;

%Calculating the fft of the modulated and carried frequencies fl=length(Fc);

```

```

fl=2^ceil(log2(fl));

f=(-fl/2:fl/2-1)/(fl*1.e-4);

% Calculating the FFT of Carrier Signal Fc_fft=fftshift(fft(Fc,fl));

subplot(4,2,3);

plot(f,abs(Fc_fft));

xlabel('Time');

ylabel('Amplitude');

title('PSD of Carrier Signal');

grid on;

hold on;

% Calculating the FFT of a Single Tone Modulated Frequency subplot(4,2,4);

Fm_singletone_fft=fftshift(fft(Fmtone1,fl));

plot(f,abs(Fm_singletone_fft));

xlabel('Time');

ylabel('Amplitude');

title('PSD of Single Tone Modulated Signal'); hold on;

% Calculating the FFT of a Dual Tone Modulated Frequency subplot(4,2,5);

Fm_dualtone_fft=fftshift(fft(Fmtone2,fl));

plot(f,abs(Fm_dualtone_fft));

xlabel('Time');

```

```

ylabel('Amplitude');

title('PSD of Double Tone Modulated Signal');

hold on;

% Calculating the FFT of a Dual Tone Modulated Frequency subplot(4,2,6);

Fm_tripletone_fft=fftshift(fft(Fmtone3,fl));

plot(f,abs(Fm_tripletone_fft));

xlabel('Time');

ylabel('Amplitude');

title('PSD of Triple Tone Modulated Signal');

```

7.4.4 Iterate Tent Map Function

```

%-----

% Matlab function for iterating and plotting tentmap function

% The function cobwebtent(x) successively iterates a given point 'x' with
the 'tent' map as a fixed set.

% Tent Map Function

%  $\mu \cdot x_n$ , if  $0 \leq x \leq 0.5$ 

%  $\mu \cdot (1 - x_n)$ , if  $0.5 \leq x \leq 1$ 

% Parameter Description

% x(1) : Initial Condition of the iteration

% mu : positive real constant

```

```

% maxiter : maximum number of iterations

%-----

function Titerate(x,maxiter)

clc;

clf;

clear all;

close all;

x_previous(1)=input(' Initial Condition x_0: ');

mu=input(' Parameter value mu: ');

maxiter=input('Maximum number of iterations : ');

r=1;

fsize=12;

% Compute the tent map. for iter = 1:maxiter

if (x_previous(iter)<0.5)

x_next(iter)=mu*x_previous(iter);

elseif (x_previous(iter) >= 0.5)

x_next(iter)=mu*(1-x_previous(iter));

end

if ((iter+1) <= maxiter)

x_previous(iter+1)=x_next(iter);

end

end

```

```

% Plot 'tent' map

xeq = [0 1];

yeq = [0 1];

% 'xe','ye' values for plotting

plot( x_previous,x_next);

hold on;

% Plot y=x

y=x plot(xeq,yeq,r);

title(['Graphical iteration of tent map'],'FontSize',fsize,'Color','b');

xlabel('x','FontSize',fsize,'Color','b');

ylabel('T^[^n^](x), n=2','FontSize',fsize,'Color','b');

```

7.4.5 Generate cobweb plots for tent map

```

%-----

% Matlab function for displaying cobweb plots for tent maps

% The function cobwebtent(x) successively iterates a given point 'x' with
the 'tent' map as a fixed set.

% Tent Map Function

%  $\mu \cdot x_n$ , if  $0 \leq x \leq 0.5$ 

%  $\mu \cdot (1 - x_n)$ , if  $0.5 \leq x \leq 1$ 

% Parameter Description

% x(1) : Initial Condition of the iteration

```

```

% mu : positive real constant

% maxiter : maximum number of iterations

%-----

function gen_cobwebtent(x)

clear all;

clc;

clf;

global mu r fsize=12; % font size.

x(1) = input(' Initial Condition x_0: ');

maxiter=input(' Maximum number of iterations: ');

n=input('Repeat Counting for mapping : ');

mu=input(' Parameter value mu: ');

xn=0:0.0001:1;

y=xn; plot(xn,functiontent(xn),'b-')

% Plot function in file functiontent1.m hold on plot(xn,xn,'k')

% Superpose plot of y=x axis([0 1 0 1]);

% Scale picture axis('square');

% Ensure plot is square fprintf('\n n Iterate \n')

% Print table header

% Compute the tent map.

for k=1:maxiter

for l=1:n

```

```

xn=mu*(0.5-abs(x(k)-0.5));

% Mapping is  $x(n+1)=2*r*(0.5-abs(x_n-0.5))$ 

end

x(k+1) = xn;

fprintf(' %3.0f %10.10f \n', k,x(k+1))

%Print the iterated value end

% Draw the cobweb plot.

for k=1:maxiter xa(2*k-1)=x(k);

xa(2*k)=x(k);

end

xb(1)=0;

xb(2)=x(2);

for k=2:maxiter

xb(2*k-1)=x(k);

xb(2*k)=x(k+1);

end

for k=1:maxiter

if k>1 xh=[xa(k-1) xa(k)];

yh=[xb(k) xb(k)];

plot(xh,yh,'r:')

end xv=[xa(k) xa(k)];

yv=[xb(k) xb(k+1)];

```

```
plot(xv,yv,'r')
```

```
end
```

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