

A Micropower Front-end Interface for Differential-Capacitive Sensor Systems

T.G. Constandinou, J. Georgiou and C. Toumazou

Abstract: This letter presents a front-end circuit for interfacing to differential capacitive sensors, including certain microelectromechanical systems (MEMS). The system combines a self-resetting, biphasic integrator with a difference timer, producing a word parallel output representing the differential capacitance. The measurable capacitance range is tunable by means of an input current bias and system clock frequency. For an input bias of 10nA and system clock of 128KHz, the measurable capacitance range is $\pm 5\text{pF}$ (to 8 bit resolution) consuming below 26 μW total system power.

Introduction: An increasing number of medical devices including implantable prosthetics and body worn instrumentation are incorporating sense systems within and around the body. Physical constraints demand such systems to be compact and lightweight, both features that are achievable through MEMS technology. Such sensors may include inertia and position detectors, for example accelerometers and tilt sensors. In addition, the need for autonomy and therefore an acceptable battery life imposes stringent power budgets on such systems.

Capacitive microsensors are in wide use because of their many advantages. They offer low-power operation, high sensitivity, low temperature variation, simple structure and the option of applying electrostatic actuation for closed-loop control. However, these also present certain design challenges including interfacing to a high impedance readout node, susceptibility to parasitics and electromagnetic interference. Therefore, readout circuit design needs to consider sensor structure and packaging before implementation is possible. Common techniques for capacitive measurement can be grouped into four main categories: (i) AC bridge with voltage amplification [1], (ii) transimpedance amplification [2], (iii) switched capacitor charge amplification [3] and (iv) integrate & reset or oscillating [4,5] techniques.

An essential feature of a modern sensor interface employed within the personal area network (PAN), is that it incorporates a suitable data conversion technique thus to produce a digital output. Bracke et al. [6] and Kulah et al. [7] have developed switched-capacitor interfaces using sigma delta modulators to produce a bitstream; used both, to extract a digital output and provide closed-loop feedback. Kung et al. [8] have presented an interface based on a successive approximation converter, George et al. [9] have presented a triple slope capacitance to digital converter based on a dual slope converter, and Tedja et al. [10] have presented a multi-channel interface feeding a Wilkinson converter.

In this letter, we present a micropower interface circuit for a differential capacitive sensor generating a digital output. This is achieved by using current integration and thresholding for phase detection and temporal sampling for conversion. This has been implemented as part of a two chip solution (MEMS sensor/CMOS interface) and has been fabricated.

Principle of Operation: The equivalent circuit of a typical differential capacitive sensor is shown in Fig. 1. Variations in the sensor's capacitances C_N and C_P are normally equal and opposite (i.e. maintains a constant total capacitance) and linear as given by:

$$C_N = C_0(1 \pm kx), C_P = C_0(1 \mp kx) \quad (1)$$

Where k and x are the relative sensitivity and displacement respectively. Assuming a constant current flows into one branch of the sensor's "capacitor", the charge will accumulate at constant rate causing the voltage to rise also linearly. This yields the following relationship:

$$I_{bias} \cdot dt = C \cdot V_{ref} \rightarrow \tau_{total} = \frac{(C_N + C_P) \cdot V_{ref}}{I_{bias}} \quad (2)$$

Where I_{bias} is the bias current, V_{ref} is the voltage reference (for threshold detection) and τ is the total charging period (for both C_N and C_P). For a given sensor, this defines a nominal refresh rate to be: $f_{refresh} = 1/\tau_{total}$. If an N -bit output resolution is required, this imposes a minimum clock frequency as:

$$f_{clk} = \frac{2^N \cdot I_{bias}}{(C_N + C_P) \cdot V_{ref}} \quad (3)$$

This defines the minimum acceptable input-referred voltage error (for threshold detection) to achieve the desired resolution:

$$V_{LSB} = V_{ref} / 2^N \quad (4)$$

Implementation: The presented interface circuit has been developed and submitted for fabrication in a commercially available CMOS technology (AMS 0.35 μ m 2P4M). The top-level system schematic is shown above in Fig. 2. The comparator used is based on a two-stage operational amplifier topology with inverter forming a 3rd stage. The delay cells use a cascade of current starved inverters to produce an artificial propagation delay. The comparator uses a current bias I_{bias} of 2 μ A, and delay-cells current bias-limit I_{limit} of 1 μ A and 250nA, tuned such that $\tau_1=10ns$ and $\tau_2=100ns$.

The maximum allowable input-referred voltage error (Eqn. 4) incorporates the comparator input-offset in addition to contributions from device leakage (through reset switches and the inactive current steer switch). Moreover, any short-term fluctuation in bias current will affect this input-referred error. The effect is however massively reduced due to the inherent differential operation- which acts to remove any static input-referred errors (including comparator input-offset). On the other hand, the system remains susceptible to dynamic effects, in particular relating to electrostatic actuation, for example in small proof mass accelerometers. The microsensors are designed such that the stiffness in the direction of the electric field is maximised, whilst maintaining minimal out-of-plane stiffness thus maximizing sensitivity to inertia.

The complete system core measures 240 μ m x 140 μ m. This excludes the current bias circuitry (which is being generated off-chip) and I/O cells (buffers and ESD protection). In top-level layout, special care was taken in connecting to capacitance input nodes to maintain symmetry and thus match any parasitic capacitances. Furthermore, bond pad metal stack

and surface area have been reduced for input pads in order to reduce parasitics. The total on-chip parasitic load (for purposes of die-to-die bonding) excluding transducer interconnects and bondwire has been designed to remain below 250fF and be matched to be within below 5%. Although any mismatch in parasitics will manifest itself as a static differential error, this has been maintained minimal to reduce any die-to-die variations and thus the need for post-calibration.

Simulation Results: The circuit was simulated using the Cadence Spectre (5.1.41sr1) simulator with foundry supplied BSIM3v3 models. Transient simulation results for a typical capacitance variation ($C_N=2.5pF$ and $C_P=7.5pF$) are shown in Fig. 3. This uses $I_{bias}=10nA$ and $V_{ref}=2V$, and from Eqn. 3, the clock frequency used is determined to be: $F_{clk}=128KHz$. As extracted from the simulated data, the integration phases are 1.5ms and 500 μs , relating to the positive and negative differential capacitances respectively, i.e. C_P and C_N . This is in exact agreement with the theoretically expected from Eqn. 2. Furthermore, the counter output value, latches at: 128, again matching the expected, (i.e. $OUT=F_{clk} \cdot \delta t = 128K(1.5m - 0.5m)$). In this configuration, the average power consumption comes to 25.9 μW , extracted from the results shown in Fig. 3.

Conclusion: The design of a novel micropower, differential-capacitive sensor interface has been described. The front-end consisting of a current-integrating threshold detection is a commonly used technique in bio-inspired neuron circuits. Coupled with a current steering technique and up/down counter provides an easily implementable method for extracting a differential, digital reading. By using this technique, most technology-related variations and device non-idealities are eliminated.

The system designed, simulated and fabricated has considered ideal capacitance elements, valid if the transducers are designed such that the combs are made stiff in the direction of the electric field, but remaining flexible out-of-plane, thus maintaining sensitivity. For micro-sensors with the electric field incident along the sense plane, the interface can be

altered, by implementing the current integration across a feedback capacitor in a switched-capacitor configuration, thus biasing the sense nodes with fixed voltages and not applying a dynamic electrostatic force.

The interface described herein achieves at least a 45dB dynamic range with micropower operation in a compact footprint. It is envisaged, such a front-end may be applicable within capacitive sensor arrays with each element having a dedicated interface in niche applications benefiting from embedded in-sense-plane processing.

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Figure Captions:

Fig. 1 Equivalent circuit of a differential capacitive microsensor

Fig. 2 Top level circuit schematic for the sensor interface

Fig. 3 Transient simulation results (for $C_N=2.5\text{pF}$, $C_P=7.5\text{pF}$, $I_{\text{bias}}=10\text{nA}$, $F_{\text{clk}}=128\text{KHz}$, $V_{\text{ref}}=2\text{V}$, $V_{\text{dd}}=3.3\text{V}$). Shown are: (a) V_{reset} , (b) V_T , (c) V_{CN} and V_{CP} , (d) CountQ(9:0) and Q(9:0), (e) I_{Vdd} , and (f) $\text{integ}(I_{\text{Vdd}})$.

Figure 1:

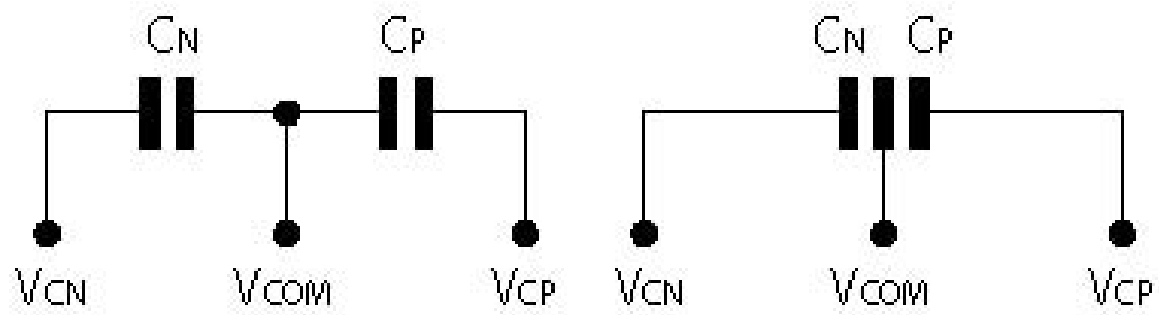


Figure 3:

