

DC-Link Capacitance Design for VSC-HVDC Systems With a Robust Small-Signal Stability Certificate Under Load Uncertainties

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Abstract—VSC-HVDC is often employed to connect generation hubs with load centers. Proper design of DC-link capacitance provides buffering against disturbances, thereby maintaining power supply stability in the presence of uncertainties. Existing studies have addressed the DC-link capacitance design problem under given loading conditions. However, it remains unclear how to determine an appropriate DC-link capacitance to maintain stability under uncertain load conditions. A key difficulty lies in ensuring that the stability condition holds across all potential scenarios, which could be computationally prohibitive. To address this challenge, we propose a computationally tractable method for designing the DC-link capacitance of a VSC-HVDC with a robust small-signal stability certificate. We first derive a sufficient condition to certify robust stability, formulated as a convex program whose number of constraints does not grow with that of the uncertainty. Then, we develop a capacitance design algorithm towards finding the smallest parameter that satisfies the condition within a desired precision. Finally, we report a capacitance-control co-design approach that further reduces the required capacitance. The effectiveness of the proposed work is demonstrated using simulations in MATLAB/Simulink.

Index Terms—HVDC transmission, uncertainty, robust stability, capacitance, state feedback.

I. INTRODUCTION

The stability of voltage-source-converter-based high-voltage direct-current (VSC-HVDC) systems is crucial for modern power systems with increasing penetration of power electronic devices. Due to their dependence on fast control loops, accurate measurements, and parameter-dependent models, VSC-HVDC systems may be sensitive to load variations, parameter uncertainties, and cyber-physical disturbances [1], [2]. Therefore, stability-oriented design is essential for secure and reliable VSC-HVDC operation.

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VSC-HVDC is usually employed to transmit power from remote energy hubs to load centers [3]–[5]. In such power transmission systems, variations in demand impact the system stability margin [6]–[8]. The DC-link capacitance is a buffer to withstand power disturbances [9]. With a proper design, for instance, if the capacitance size is beyond a certain threshold, the system could remain stable to a given range of loading conditions [10]. In addition, finding this threshold assists in determining a well-informed stability margin, potentially leading to a more economic design [11].

DC-link capacitance has a significant influence on VSC-HVDC stability [12]. Existing literature has studied small-signal stability and the oscillation problems of VSC-HVDC systems, which usually center the study around a fixed equilibrium calculated based on the nominal power [13]–[18]. Modal analysis [13] and impedance analysis [14] methods have been proposed. In [13], a state-space model of a direct-drive wind farm integrated with VSC-HVDC is established to discuss the impact of rectifier control parameters and AC circuit parameters on sub-synchronous oscillation damping performance by modal analysis. In [14], the authors use the Nyquist stability criterion to examine resonance characteristics and conclude that increasing DC-link capacitance can suppress the resonance effectively. In addition, damping torque analysis is developed to derive the analytic stable criteria and is used in VSC-HVDC stability analysis as well [15]. A stability criterion containing DC-link capacitance is developed based on damping torque analysis in [16]. Besides, DC-link capacitance has a positive effect on the large-signal stability as well. Brayton-Moser’s mixed potential method and fuzzy modeling methods have been proposed for such studies [17], [18].

Despite the rich literature on VSC-HVDC stability analysis and DC-link capacitance design, existing works have several limitations in designing the DC-link capacitance of VSC-HVDC. First, stability analysis methods for VSC-HVDC systems based on the assumption of the availability of a fixed and known operating equilibrium point have been proposed [13]–[18]. In a power system with increasing uncertainties, the actual equilibrium of a VSC-HVDC system is inherently dependent on loading conditions, which are often unknown and subject to continuous variation over time [4], [8]. Second, existing research has studied the impact of DC-link capacitance on the dynamic stability of VSC-HVDC systems [14], [17], [18]. There is currently a lack of a systematic design

method that sizes the DC-link capacitor that ensures robust stability.

Addressing the above limitations requires a systematic stability analysis framework that can explicitly account for parametric uncertainties in the system model, while remaining computationally tractable for design purposes. Linear matrix inequality (LMI)-based approaches provide such a framework and have been widely adopted in robust stability analysis [19]–[21]. Although LMI-based methods have been preliminarily applied to robust stability analysis of DC microgrids under load uncertainties [22], [23], their application to DC-link capacitance design in VSC-HVDC systems remains unclear. Further investigation and validation are therefore needed.

To close this gap, this paper proposes a DC-link capacitance design method considering bounded loading uncertainties. We formulate a semi-definite programming (SDP) problem whose solution yields a capacitance that ensures robust stability against an uncertain power condition that varies arbitrarily within a given range. First, we derive the state-space model of the VSC-HVDC system, considering uncertainties in loading conditions. Then, we show that checking robust stability of the system can be formulated as an uncertain SDP problem. A sufficient condition for robust stability can then be developed. Nonetheless, the number of stability conditions grows exponentially with that of uncertainties. To cope with the computational difficulty, we reformulate the uncertain SDP and derive a set of sufficient conditions that can be effectively checked to ensure robust stability. Finally, based on the developed conditions, we propose a method to find a suitable DC-link capacitance that ensures robust stability under bounded loading uncertainties. Moreover, we report a capacitance-control co-design problem under the same formulation paradigm, which further reduces the need for capacitance.

The contributions of this paper are summarized as follows.

- We develop a sufficient condition that certifies the robust stability of VSC-HVDC against an interval-bounded loading uncertainty. We further transform the condition, where the number of constraints is exponentially dependent on the number of uncertainties, into a tractable counterpart with only two constraints.
- We develop a capacitance design algorithm based on the stability condition to obtain a proper DC-link capacitance that satisfies the proposed robust small-signal stability criterion.
- We propose a capacitance-control co-design synthesis method that further reduces the requirement of DC-link capacitance for VSC-HVDC systems.

The rest of this paper is organized as follows. Section II reports the state space model of a VSC-HVDC system and formulates the capacitance design problem. Section III derives a sufficient stability condition and develops an algorithm for DC-link capacitance design. Section IV shows that the proposed work can be extended to a capacitance-control co-design problem. Section V demonstrates the effectiveness of the proposed work using simulation testing. Section VI concludes the paper.

Table I provides a list of acronyms used throughout.

TABLE I
Glossary of Acronyms

AC	- Alternating Current
DC	- Direct Current
VSC	- Voltage Source Converter
HVDC	- High-Voltage Direct Current
PCC	- Point of Common Coupling
PWM	- Pulse Width Modulation
PI	- Proportional-Integral
LMI	- Linear Matrix Inequality
SDP	- Semi-Definite Programming
CVX	- Convex Optimization Toolbox
MMC	- Modular Multilevel Converter
LCC	- Line-Commutated Converter
p.u.	- Per Unit

II. SYSTEM MODELING AND PROBLEM STATEMENT

In this section, we first report the system model, including the VSC-HVDC network and its control system. Then, we derive a small-signal model with an uncertainty in the system loading condition to support the DC-link capacitance design. At last, we discuss the main problem considered in this paper.

A. Preliminaries

We focus on a two-terminal two-level VSC-HVDC system, as shown in Fig. 1. The system represents an AC grid supplying power to a load center and represents a wide spectrum of applications, such as an energy hub supplying power to a remote city [4], [17], [24].

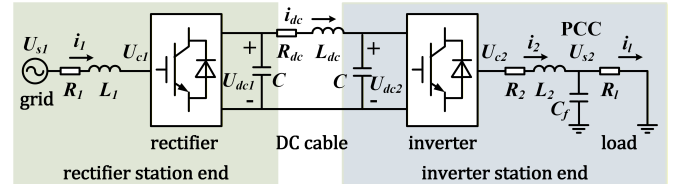


Fig. 1: Two-terminal VSC-HVDC model

Symmetric three-phase electrical variables are commonly represented as a constant-amplitude vector rotating at a fixed angular frequency. As shown in Fig. 1, to simplify our discussion, let U_{s1} , U_{c1} and i_1 be the AC grid voltage vector, the AC voltage vector and the current vector of rectifier, respectively; let U_{s2} , U_{c2} and i_2 be the voltage vector at point of common coupling (PCC) of inverter, the AC voltage vector and the current vector of inverter, respectively. Besides, on the DC side, let U_{dc1} , U_{dc2} , and i_{dc} be the DC voltage of the rectifier, the DC voltage of the inverter, and the direct current, respectively. For the circuit parameters, let L_1 , R_1 and C be the reactor inductance and equivalent loss resistance of the rectifier, and the DC-link capacitance, respectively; let L_{dc} and R_{dc} be the equivalent inductance and resistance of DC cable, respectively; let L_2 , C_f and R_2 be the inverter's reactor inductance, filter capacitance and equivalent loss resistance, respectively; let R_l be the equivalent resistance of the load.

We use subscripts d and q to represent the d-axis and q-axis components of each vector in the dq coordinates, respectively. For a real symmetric matrix L , let $L \succ 0$ and $L \prec 0$ represent that L is positive definite and negative definite, respectively, and let $L \succeq 0$ and $L \preceq 0$ represent that L is positive semidefinite and negative semidefinite, respectively. We say that a matrix is Hurwitz stable if all of its eigenvalues have negative real parts. Let $\|\cdot\|$ be the Euclidean norm of a vector.

B. Individual Component Models

The HVDC network connects to the grid and the load through a rectifier and an inverter, respectively. The electromagnetic dynamics of the system are studied in this paper, enabling the consideration of the capacitance design problem [4]. Similar to [17], [18], based on the reference directions of voltages and currents defined in Fig. 1, Kirchhoff's voltage/current law, and energy conservation law, component models are established as follows.

1) Rectifier Model

In dq coordinates, the state variables of the rectifier include i_{1d} , i_{1q} , and U_{dc1} , which represent the inductance current and capacitance voltage, respectively, and their dynamics are given by,

$$\begin{cases} L_1 \frac{di_{1d}}{dt} = -R_1 i_{1d} + \omega_1 L_1 i_{1q} + U_{s1d} - U_{c1d} \\ L_1 \frac{di_{1q}}{dt} = -R_1 i_{1q} - \omega_1 L_1 i_{1d} + U_{s1q} - U_{c1q} \\ C \frac{dU_{dc1}}{dt} = \frac{3}{2U_{dc1}} i_{1d} U_{c1d} + \frac{3}{2U_{dc1}} i_{1q} U_{c1q} - i_{dc} \end{cases}, \quad (1)$$

where ω_1 is the angular frequency of the dq coordinates of the rectifier control system. One can see that there are nonlinear terms $3i_{1d}U_{c1d}/(2U_{dc1})$ and $3i_{1q}U_{c1q}/(2U_{dc1})$ in (1).

2) DC Cable Model

The DC cable is modeled as a π -equivalent circuit. The two equivalent capacitances of this π -equivalent circuit are taken into account in the DC-link capacitances of the rectifier and the inverter. The state variable of the DC cable model is the direct current, i_{dc} , and its dynamics are given by,

$$L_{dc} \frac{di_{dc}}{dt} = U_{dc1} - U_{dc2} - R_{dc} i_{dc}, \quad (2)$$

3) Inverter Model

Similar to [25], an LC filter is applied at the AC side of the inverter to improve the power quality. The energy storage elements of the inverter station end include LC filter inductance L_2 , LC filter capacitance C_f , and DC-link capacitance C . Thus, in dq coordinates, the state variables include i_{2d} , i_{2q} ,

U_{dc2} , U_{s2d} , and U_{s2q} , and their dynamics are given by,

$$\begin{cases} L_2 \frac{di_{2d}}{dt} = -R_2 i_{2d} + \omega_2 L_2 i_{2q} - U_{s2d} + U_{c2d} \\ L_2 \frac{di_{2q}}{dt} = -R_2 i_{2q} - \omega_2 L_2 i_{2d} - U_{s2q} + U_{c2q} \\ C_f \frac{dU_{s2d}}{dt} = \omega_2 C_f U_{s2q} + i_{2d} - \frac{U_{s2d}}{R_l} \\ C_f \frac{dU_{s2q}}{dt} = -\omega_2 C_f U_{s2d} + i_{2q} - \frac{U_{s2q}}{R_l} \\ C \frac{dU_{dc2}}{dt} = -\frac{3}{2U_{dc2}} i_{2d} U_{c2d} - \frac{3}{2U_{dc2}} i_{2q} U_{c2q} + i_{dc} \end{cases}, \quad (3)$$

where ω_2 is the angular frequency of the dq coordinates of the inverter control system. One can see that there are nonlinear terms $3i_{2d}U_{c2d}/(2U_{dc2})$ and $3i_{2q}U_{c2q}/(2U_{dc2})$ in (3).

The receiving end's load is modeled as a resistance R_l [18]. The uncertain parameter R_l may take any value in an interval $[\underline{R}_l, \bar{R}_l]$ where $\bar{R}_l \geq \underline{R}_l > 0$ are known bounds.

C. VSC-HVDC Control Model

The VSC-HVDC system has two AC/DC converters on the sending and receiving ends. Their control systems are discussed in the following. The control of the rectifier is shown in Fig. 2. It can be seen that the rectifier controls the DC voltage [5]. The active power is controlled by regulating the DC voltage U_{dc1} to the reference value U_{dcr} by the outer loop and inner loop in d-axis, and the reactive power is controlled by regulating the reactive power current i_{1q} to zero by the inner loop in q-axis. k_{pv1} and k_{iv1} are the proportional gain and integral gain of the voltage loop PI regulator, and k_{pi1} and k_{ii1} are the proportional gain and integral gain of the current loop PI regulator, respectively. m_1 , m_2 , and m_3 are state variables of PI regulators. Note that the pulse width modulation (PWM) connects the control system and the physical system and has a time delay [26]. We model the PWM as an inertia link whose time constant is the switching period T_s and gain is 1 [4]. It is worth mentioning that in Section IV, we show that a state feedback control shown in the figure's purple colored block can be co-designed with the DC-link capacitance to enhance stability.

The inverter control is shown in Fig. 3. It can be seen that the voltage at PCC is controlled by double closed-loop decoupled control [7]. The PCC voltage is used as the reference phase of the AC-side of the inverter, so its q-axis component should be zero. k_{pv2} and k_{iv2} are the proportional gain and integral gain of the voltage loop PI regulator, and k_{pi2} and k_{ii2} are the proportional gain and integral gain of the current loop PI regulator, respectively. m_4 , m_5 , m_6 , and m_7 are the state variables of PI regulators.

In Fig. 2 and Fig. 3, the outer and inner loop outputs will appear as linear polynomials in the ordinary differential equations. They are i_{1dr} , U_{c1dr} , U_{c1qr} , i_{2dr} , i_{2qr} , U_{c2dr} , and

The diagram illustrates the control system for a three-phase inverter. It consists of two main control loops: the d-axis (direct) and the q-axis (quadrature).
 - **d-axis loop:** The reference voltage U_{sd}^* is compared with the feedback voltage U_{sd} at a summing junction. The error signal is processed by a PI controller (k_{pv2} and $1/s$) to produce the d-axis current reference i_{d}^* . This reference is compared with the feedback current i_{d} at another summing junction. The error is processed by a PI controller (k_{pi2} and $1/s$) to produce the d-axis voltage reference U_{sd} . The output is filtered by a low-pass filter ($1/(T_s s + 1)$) to produce the final d-axis output voltage U_{cd} .
 - **q-axis loop:** The reference voltage U_{sq}^* is compared with the feedback voltage U_{sq} at a summing junction. The error signal is processed by a PI controller (k_{pv2} and $1/s$) to produce the q-axis current reference i_{q}^* . This reference is compared with the feedback current i_{q} at another summing junction. The error is processed by a PI controller (k_{pi2} and $1/s$) to produce the q-axis voltage reference U_{sq} . The output is filtered by a low-pass filter ($1/(T_s s + 1)$) to produce the final q-axis output voltage U_{cq} .
 - **Feedback and Cross-Coupling:** The output voltages U_{cd} and U_{cq} are fed back to the input summing junctions. Additionally, the d-axis output voltage U_{cd} is fed back to the q-axis input summing junction, and the q-axis output voltage U_{cq} is fed back to the d-axis input summing junction, indicating a cross-coupling effect. The d-axis current reference i_{d}^* is also fed back to the q-axis input summing junction, and the q-axis current reference i_{q}^* is fed back to the d-axis input summing junction.

Let vector x_e be the equilibrium of system (6). Let the difference between state x and the equilibrium x_e be $\Delta x \triangleq x - x_e$. Similar to [4], the nonlinear VSC-HVDC dynamics (6) around the equilibrium x_e is approximated by its first-order Taylor expansion, that is, the small-signal model. The model

is given as follows,

$$\begin{cases} \Delta \dot{x} = J(\delta, C) \Delta x \\ J(\delta, C) = M(C)^{-1} \left(A_0 + \sum_{k=1}^{11} \delta_k D_k \right), \end{cases} \quad (7)$$

where matrix $J(\delta, C) \in \mathbb{R}^{20 \times 20}$ is the Jacobian matrix, vector $\delta \in \mathbb{R}^{11}$ represents uncertainties derived from the equivalent load resistance R_l and the portion v^e of equilibrium x_e , matrix array D that stores matrices resembling that a vector stores scalars locates uncertainties in the matrix $J(\delta, C)$ and has 11 elements that are all square matrix. Let v_k^e , δ_k be the k -th element of the vector v^e and the vector δ , respectively, and let D_k be the k -th matrix of the matrix array D , which are shown below,

$$\begin{aligned} \delta_1 &= \frac{U_{c1d}^e}{U_{dc1}^e}, \delta_2 = \frac{U_{c1q}^e}{U_{dc1}^e}, \delta_3 = \frac{i_{1d}^e U_{c1d}^e + i_{1q}^e U_{c1q}^e}{(U_{dc1}^e)^2}, \\ \delta_4 &= \frac{i_{1d}^e}{U_{dc1}^e}, \delta_5 = \frac{i_{1q}^e}{U_{dc1}^e}, \delta_6 = \frac{U_{c2d}^e}{U_{dc2}^e}, \delta_7 = \frac{U_{c2q}^e}{U_{dc2}^e}, \\ \delta_8 &= \frac{i_{2d}^e U_{c2d}^e + i_{2q}^e U_{c2q}^e}{(U_{dc2}^e)^2}, \delta_9 = \frac{i_{2d}^e}{U_{dc2}^e}, \delta_{10} = \frac{i_{2q}^e}{U_{dc2}^e}, \\ \delta_{11} &= \frac{1}{R_l}, D_1 = \frac{3}{2} E_{4,2}, D_2 = \frac{3}{2} E_{4,3}, D_3 = -\frac{3}{2} E_{4,4}, \\ D_4 &= \frac{3}{2} E_{4,8}, D_5 = \frac{3}{2} E_{4,9}, D_6 = -\frac{3}{2} E_{14,10}, \\ D_7 &= -\frac{3}{2} E_{14,11}, D_8 = \frac{3}{2} E_{14,14}, D_9 = -\frac{3}{2} E_{14,19}, \\ D_{10} &= -\frac{3}{2} E_{14,20}, D_{11} = -\frac{1}{C_f} E_{12,12} - \frac{1}{C_f} E_{13,13} + \\ &E_{16,12} + E_{18,13} + \frac{k_{pi2}}{T_s} E_{19,12} + \frac{k_{pi2}}{T_s} E_{20,13}. \end{aligned} \quad (8)$$

where $E_{i,j} \in \mathbb{R}^{20 \times 20}$ is a matrix of all zeros except for the (i, j) -element whose value is 1.

In the small-signal model (7), the load R_l and the Jacobian-related steady-state v^e are modeled as unknown parameters, and the DC-link capacitance C is a design variable to be determined. Hence, the Jacobian matrix is subject to unknown δ involving R_l , v^e , and C . Thus, while R_l and v^e might make the system matrix unstable, a properly designed C can stabilize the system given all realizations of R_l and v^e .

E. Problem Statement

The operation of VSC-HVDC is subject to varying load conditions. With improper network or control parameters, a disturbance might result in stability issues.

As mentioned earlier in the previous subsection, the load is modeled as a resistance. This modeling approach is practical, especially around a steady-state operating point [27], and in references [4], [17], [24], researchers have adopted a similar modeling approach.

Here, the equivalent load resistance R_l is assumed to be physically bounded in a polytopic set $\mathcal{R}$ defined as follows,

$$\mathcal{R} \triangleq \{R_l \in \mathbb{R}^+ : R_l \in [\underline{R}_l, \overline{R}_l]\}.$$

As R_l varies in $\mathcal{R}$, the system's operating point changes

accordingly. We study the stability of all the possible equilibria that are operationally feasible for the VSC-HVDC, and define an operational constraint set $\mathcal{V}^e$ in the following form,

$$\mathcal{V}^e \triangleq \{v^e \in \mathbb{R}^{10} : v_k^e \in [\underline{v}_k^e, \overline{v}_k^e], k = 1, \dots, 10\},$$

where $\overline{v}_k^e \geq \underline{v}_k^e$. Note that v^e collects all the state variables associated with the system's Jacobian matrix, as mentioned in Section II-D.

Since both R_l and v_k^e vary in intervals, each uncertainty δ_k varies in an interval as well. Let $\delta_k \in [\underline{\delta}_k, \overline{\delta}_k]$, where the two bounds can be easily determined from the bounds of R_l and v_k^e . Let set $\Delta \triangleq \{\delta \in \mathbb{R}^{11} : \delta_k \in [\underline{\delta}_k, \overline{\delta}_k], k = 1, \dots, 11\}$ be the set of the composite uncertainty.

With the above definitions, this paper studies system (6)'s robust stability defined as follows:

Definition 1. System (6) is said to be locally robustly stable if $J(\delta, C)$ is Hurwitz stable for all $\delta \in \Delta$.

For linear system (7) to be locally robustly stable for all $\delta \in \Delta$, a sufficient condition is that there exists $P = P^\top \succ 0$ that satisfies the following inequalities [28, Th. 4.6]:

$$J(\delta, C)^\top P + P J(\delta, C) \prec 0, \quad \forall \delta \in \Delta. \quad (9)$$

The goal of this paper is to determine a suitable DC-link capacitance C such that system (7) remains locally robustly stable. Furthermore, we synthesize a capacitance-control co-design to reduce the need for capacitance. The DC-link capacitance design problem can be formulated as the following robust optimization problem,

$$\textbf{Main Problem:} \quad \min_{C, P} C, \quad (10a)$$

$$\text{s. t.} \quad (9). \quad (10b)$$

Since the problem constitutes a semi-infinite program that consists of infinitely many constraints, directly solving it manifests a significant computational overhead.

III. ROBUST STABILITY CONDITIONS AND DC-LINK CAPACITANCE DESIGN

In this section, we develop sufficient conditions to certify robust stability and then propose computationally efficient approaches to solve the capacitance design problem (10).

A. Robust Stability Conditions

As discussed in Section II-E, directly solving (9) is impractical. The computational burden can be reduced by virtue of matrix $J(\delta, C)$ which is affine in uncertainty δ . Hence, a more computationally tractable condition can be developed for (6). Note that $\delta \in \Delta$, $J(\delta, C)$ belongs to a set $\mathcal{J}(\Delta, C)$ defined as follows,

$$\mathcal{J}(\Delta, C) = \{J(\delta, C) \in \mathbb{R}^{20 \times 20} : J(\delta, C) = M(C)^{-1} \left(A_0 + \sum_{k=1}^{11} \delta_k D_k \right), \forall \delta \in \Delta\}.$$

The set $\mathcal{J}(\Delta, C)$ is a polytopic set, and it has 2^{11} vertices. Let matrix $J_j(\delta, C)$ be the j -th vertex of set $\mathcal{J}(\Delta, C)$. It can be

written in the form: $J_j(\delta, C) = M(C)^{-1}(A_0 + \sum_{k=1}^{11} \delta_k D_k)$ with $\delta_k = \underline{\delta}_k$ or $\delta_k = \bar{\delta}_k$.

Locally exponential stability for system (6) is equivalent to all the matrices in the set $\mathcal{J}(\Delta, C)$ being Hurwitz stable. If there is a common Lyapunov function for all the matrices in the set $\mathcal{J}(\Delta, C)$, they are all Hurwitz stable. Notice that there are infinitely many elements in the set. Since the set is polytopic, any element of it can be expressed as a convex combination of its vertices. Thus, as a standard result in linear uncertain systems, to ensure stability of the matrices in the set, it suffices to have a common Lyapunov function for all the vertices of the set.

Lemma 1. System (6) is locally robustly stable for all $\delta \in \Delta$ under a given decision parameter C if $\exists P = P^\top \succ 0$ satisfying

$$J_j(\delta, C)^\top P + P J_j(\delta, C) \prec 0, \quad j = 1, \dots, 2^{11}. \quad (11)$$

If constraints (11) are all feasible for some $\exists P = P^\top \succ 0$, $U(\Delta x) = \Delta x^\top P \Delta x$ is a common Lyapunov function for the vertices in $\mathcal{J}(\Delta, C)$. Moreover, the function $U(\Delta x)$ is a common Lyapunov function for all the matrices in $\mathcal{J}(\Delta, C)$ as well, and they are all Hurwitz stable by the Lyapunov method.

The condition of Lemma 1 is more computationally tractable than (9), but the number of linear matrix inequalities (LMIs) exponentially depends on that of linear uncertainties. Specifically, the number of linear uncertainties is 11, and that of LMIs is 2^{11} , implying a considerable computational burden.

Since the uncertain LMI (9) is subject to interval-bounded uncertainty, we apply Theorem 9.1.2 of [21] to derive an equivalent condition whose number of certain LMIs is only two that are independent of the number of uncertainties. Intuitively, after the rank-1 decomposition, the uncertain terms ζ_k can be handled as structured norm-bounded uncertainties. The nonnegative multipliers λ_k are then introduced, following [21, Th. 9.1.2], to bound their worst-case effect and obtain a finite set of tractable LMIs.

To achieve this, we let each matrix D_k that determines the impact of the sole uncertainty δ_k on the Jacobian matrix $J(\delta, C)$ be expressed as a sum of rank-1 matrices generated by vector pairs, specifically as,

$$D_k = p_k q_k^\top (k = 1, \dots, 10), \quad D_{11} = \sum_{k=11}^{16} p_k q_k^\top,$$

where $q_k \in \mathbb{R}^{20}$ has the only nonzero entry, be 1, and its position and $p_k \in \mathbb{R}^{20}$ are obtained by D_k .

Theorem 1. System (6) is locally robustly stable for all $\delta \in \Delta$ under a given decision parameter C if there exists $P = P^\top \succ 0$, $N = N^\top \prec 0$, and 16 positive scalars $\lambda_1, \dots, \lambda_{16}$ satisfying

$$\begin{bmatrix} N + \sum_{k=1}^{16} \lambda_k R_k^\top R_k & L_1^\top(P) & \cdots & L_{16}^\top(P) \\ L_1(P) & -\lambda_1 & & \\ \vdots & & \ddots & \\ L_{16}(P) & & & -\lambda_{16} \end{bmatrix} \preceq 0, \quad (12a)$$

$$N \succeq A^\top P + P A, \quad (12b)$$

where $A = M(C)^{-1} \left(A_0 + \sum_{k=1}^{16} p_k q_k^\top \frac{\bar{\delta}_k + \delta_k}{2} \right)$, $L_k(P) =$

$$p_k^\top M(C)^{-1} P, \quad R_k = -\frac{\bar{\delta}_k - \delta_k}{2} q_k^\top, \quad k = 1, \dots, 16.$$

Proof. Let $\zeta_k \triangleq \left(\delta_k - \frac{\bar{\delta}_k + \delta_k}{2} \right) / \frac{\bar{\delta}_k - \delta_k}{2}$, we have $|\zeta_k| \leq 1$ and $\delta_k = \zeta_k \frac{\bar{\delta}_k - \delta_k}{2} + \frac{\bar{\delta}_k + \delta_k}{2}$. Substituting δ_k into condition (9), then it is equivalent to,

$$A^\top P + P A + \sum_{k=1}^{16} \zeta_k [L_k^\top(P) R_k + R_k^\top L_k(P)] \preceq 0, \quad (13)$$

$$\forall (\zeta \in \mathbb{R}^{16} : \|\zeta\|_\infty \leq 1).$$

We decomposed the uncertain matrices into rank-1 blocks and introduced normalized perturbation variables to transform the robust stability problem into a structured, bounded form.

According to Theorem 9.1.2 of Reference [21], the condition (13) holds if the following LMIs

$$\begin{aligned} S_k &\succeq \pm [L_k^\top(P) R_k + R_k^\top L_k(P)], \quad k = 1, \dots, 16, \\ A^\top P + P A + \sum_{k=1}^{16} S_k &\preceq 0. \end{aligned} \quad (14)$$

in matrix P and in matrices $S_1, \dots, S_{16}$ hold. As $P \succ 0$, all $L_k(P)$ are nonzero.

$$X^\top Y + Y^\top X \leq \lambda X^\top X + \frac{1}{\lambda} Y^\top Y \quad (15)$$

Invoking Exercise 9.1.2 of Reference [21], there exists $\lambda_k > 0$ such that $S_k \succeq \lambda R_k^\top R_k + \frac{1}{\lambda_k} L_k^\top(P) L_k(P)$. Since $A^\top P + P A + \sum_{k=1}^{16} S_k \preceq 0$, we have,

$$\left[A^\top P + P A + \sum_{k=1}^{16} \lambda_k R_k^\top R_k \right] + \sum_{k=1}^{16} \frac{1}{\lambda_k} L_k^\top(P) L_k(P) \preceq 0. \quad (16)$$

We applied Young's inequality to introduce slack variables, separating coupled terms and conservatively relaxing the cross-product terms for tractable LMI formulation.

The Schur Complement Lemma allows a block matrix inequality to be converted into an equivalent inequality involving only one block, simplifying the LMI for easier computation. Hence, by the Schur Complement Lemma, condition (16) is equivalent to condition (12).

Furthermore, by Exercise 9.1.1 of Reference [21], it can be proved that condition (16) is a sufficient condition for condition (14). Therefore, conditions (16) and (14) are equivalent. As a result, condition (12) is a sufficient condition for condition (9). This completes the proof. $\square$

The condition in Theorem 1 only involves two LMIs, as opposed to Lemma 1.

B. DC-Link Capacitance Design

With Theorem 1, we are equipped with a tractable condition to check the locally robust stability for system (6). To find matrices P and N that satisfy (12) with a given C , the following optimization problem is solved:

$$\begin{aligned} &\text{find } P, N, \lambda_1, \dots, \lambda_{16} \\ &\text{s. t. } (12), C = \hat{C}, P = P^\top, P \succ 0, \\ &N = N^\top, N \prec 0, \lambda_k > 0, k = 1, \dots, 16, \end{aligned} \quad (17)$$

By virtue of problem (17), a bisection method is proposed to solve problem (10) [29, Chapter 4.2.5]. We start with an interval randomly selected as long as it contains an initial guess C^0 that makes problem (17) feasible. We then solve the convex feasibility problem (17) at its midpoint $\hat{C}$. If the midpoint makes the problem feasible, then the interval's upper bound is replaced by $\hat{C}$, and vice versa. The process continues until a stopping criterion is met.

Let $\underline{C}$ and $\overline{C}$ be the lower and upper bounds, respectively, $\epsilon > 0$ be a required precision value, and C^* be the solution. The following algorithm is developed to summarize the aforementioned solution process.

Algorithm 1 Bisection Method for Capacitance Design

Input: Initial guess C^0 , bounds: $\underline{C} = 0$, $\overline{C} = C^0$, precision requirement: $\epsilon > 0$.

Output: C^* .

Step 1: $\hat{C} = \frac{\overline{C} + \underline{C}}{2}$.

Step 2: Solve the feasibility problem (17) with $\hat{C}$.

Step 3: If the problem is feasible, $\overline{C} = \hat{C}$; else, $\underline{C} = \hat{C}$.

Step 4: Repeat steps 1-3, until $\overline{C} - \underline{C} \leq \epsilon$, $C^* = \hat{C}$.

Algorithm 1 involves only computations related to convex optimization problems and algebraic calculations. Hence, it is tractable to find a design of C to make system (6) locally robustly stable.

IV. EXTENSIONS TO CAPACITANCE-CONTROL CO-DESIGN

The proposed method can be easily extended to design other parameters. In this section, we demonstrate the applicability of the proposed work by conducting capacitance-control co-design to further reduce the need for capacitance.

A. Capacitance-Control Co-Design Problem

To exemplify the co-design capability, we design a state-based feedback control strategy together with the capacitance. The structure of the control is shown in Fig. 2 of Section II-C. The control enhances the dynamic performance of the VSC-HVDC system and seeks to drive the DC voltage to converge to a reference value, U_{dcr} . The control signal w is governed by a linear control, as given in the following,

$$w = Kx' + \frac{k}{s}(U_{dcr} - U_{dc1}),$$

where the scalar k is the gain of the integral regulator, s is the differential operator, vector $x' = [x^\top, m_8]^\top$, and matrix $K \in \mathbb{R}^{1 \times 21}$ is the gain of the state-based feedback control. Notice that, in terms of dynamic stability, the upstream integral regulator generally requires slower integration compared to the downstream outer loop, i.e., $k < k_{iv1}$.

The small-signal model of the system with the proposed control can be expressed by,

$$\begin{cases} \Delta \dot{x}' = H(\delta, C) \Delta x', H(\delta, C) = J'(\delta, C) + G'K, \\ J'(\delta, C) = M'(C)^{-1} \left(A_0' + \sum_{k=1}^{11} \delta_k D_k' \right), \\ A_0' = \begin{bmatrix} A_0 & kG \\ e_c^\top & 0 \end{bmatrix}, D_k' = \begin{bmatrix} D_k & 0 \\ 0 & 0 \end{bmatrix}, G' = \begin{bmatrix} G \\ 0 \end{bmatrix}, \end{cases} \quad (18)$$

where $e_c^\top \in \mathbb{R}^{1 \times 20}$ is defined as $e_c^\top = [0, 0, 0, -1, 0, \dots, 0]$, matrices $G \in \mathbb{R}^{20 \times 1}$ is the first column of matrix B and $M'(C)$ is the direct sum of $M(C)$ and 1. The entry -1 in $e_c^\top$ is placed at the fourth position, corresponding to the state U_{dc1} in $x = [i_{dc}, x_1^\top, x_2^\top]^\top$. Thus, the augmented row $[e_c^\top \ 0] \in \mathbb{R}^{1 \times 21}$ correctly represents the small-signal equation of the new integral state, i.e., $\Delta \dot{m}_8 = -\Delta U_{dc1}$.

Similar to (9), the linearized system matrix $H(\delta, C)$ is always Hurwitz stable for all $\delta \in \Delta$ under a given decision parameter C if there exists $P = P^\top \succ 0$ and K satisfying,

$$(J'(\delta, C) + G'K)^\top P + P(J'(\delta, C) + G'K) \prec 0 \quad \forall \delta \in \Delta. \quad (19)$$

In the co-design, we aim to determine the lowest feasible value of C among those that satisfy condition (19). Therefore, the DC-link capacitance-control co-design synthesis can be formulated as the following robust optimization problem,

$$\text{Co-Design:} \quad \min C, \quad (20a)$$

$$\text{s. t.} \quad (19), \quad (20b)$$

where matrices P and K , and scalar C are decision variables.

B. Solution Approach

Lemma 1 is applied here to solve the co-design problem (20). Since δ is a bounded linear uncertainty, the matrix $J'(\delta, C)$ lies in a polytopic uncertain set. Let matrix $J_j'(C)$ be the j -th vertex of the set. Inspired by Lemma 1, constraints (20b) hold if the following conditions are satisfied,

$$(J_j'(C) + G'K)^\top P + P(J_j'(C) + G'K) \prec 0, \quad j = 1, \dots, 2^{11}. \quad (21)$$

As shown in equation (21), there is a coupling between decision variables P and K in the condition (21), which makes the condition non-convex. We can take a change of variables to obtain the equivalent tractable LMI condition. For $P \succ 0$, define $W = P^{-1}$ and $Y = KP^{-1}$, so that we have $K = YW^{-1}$. Substituting into matrix inequalities (21) and multiplying both sides of them from the left and from the right by W yields

$$WJ_j'(C)^\top + J_j'(C)W + Y^\top G'^\top + G'Y \prec 0, \quad j = 1, \dots, 2^{11}, \quad (22)$$

which are LMIs in W and Y if C is given.

In addition, similar to Section III-A, the condition of problem (20) holds if the following two LMIs in variables W , Y , N , λ_k , $k = 1, \dots, 16$ hold.

$$\begin{bmatrix} N + \sum_{k=1}^{16} \lambda_k R_k^\top R_k & L_1^\top(W) & \cdots & L_{16}^\top(W) \\ L_1(W) & -\lambda_1 & & \\ \vdots & & \ddots & \\ L_{16}(W) & & & -\lambda_{16} \end{bmatrix} \preceq 0, \quad (23a)$$

$$N \succeq WZ^\top + ZW + Y^\top G'^\top + G'Y, \quad (23b)$$

$$W = W^\top, N = N^\top, W \succ 0, N \prec 0, \lambda_k > 0, \quad (23c)$$

where $Z = M(C)^{-1} \left(A_0 + \sum_{k=1}^{16} p_k q_k^\top \frac{\bar{\delta}_k + \delta_k}{2} \right)$, $L_k(W) = q_k^\top W$, $R_k = -\frac{\bar{\delta}_k - \delta_k}{2} p_k^\top M(C)^{-1}$, $k = 1, \dots, 16$.

A large K may cause a large overshoot. Hence, additional

constraints could be imposed to improve the dynamic response performance. We define an ellipsoid set ε using W^{-1} as follows,

$$\varepsilon = \{\xi \in \mathbb{R}^{21} : \xi^\top W^{-1} \xi \leq 1\}.$$

The set ε is forward invariant, and $\|K\Delta x'\| \leq \mu$ holds, if the following LMIs are satisfied,

$$\begin{bmatrix} 1 & \Delta x'(0)^\top \\ \Delta x'(0) & W \end{bmatrix} \succeq 0, \quad \begin{bmatrix} W & Y^\top \\ Y & \mu^2 I \end{bmatrix} \succeq 0, \quad (24)$$

where matrices W and Y satisfy the LMIs (22), and I is the identify matrix.

Remark 1. There are two regulation parameters $\Delta x'(0)$ and μ in constraint (24). Since the constraint is based on a linearized model, the selection of $\Delta x'(0)$ and μ is inherently limited, implying that these parameters cannot be handled in the same manner as in a linear system. To determine appropriate values, we assume that the linearization error within $\pm 1\%$ of the equilibrium x'_{e0} calculated based on the nominal loading parameter is sufficiently small. By this assumption, we set $\Delta x'(0) = 0.01x'_{e0}$ and $\mu = 0.01U_{dcr}$ for an instance.

Let C^{**} be the solution of the co-design problem (20). If the convex feasibility problem,

$$\begin{aligned} & \text{find } W, Y, \\ & \text{s. t. } (22) \text{ or } (23), \\ & (24), C = \hat{C}, W = W^\top, W \succ 0, \end{aligned} \quad (25)$$

is feasible, then we have $C^{**} \leq \hat{C}$ and $K = YW^{-1}$ that can make the linearized system matrix $H(\delta, C)$ remain Hurwitz stable for all $\delta \in \Delta$. Conversely, if it is infeasible, then we can conclude $C^{**} \geq \hat{C}$.

Therefore, we can use the Bisection method that checks the convex feasibility problem (25) at each given value $\hat{C}$ to solve the problem (20). Implementation procedures are consistent with Algorithm 1 and are omitted to avoid redundancy.

V. CASE STUDIES

In this section, we demonstrate the effectiveness of the proposed Algorithm 1 and co-design using simulations. The algorithm is executed on MATLAB with the CVX tool. The simulations are performed on the professional power system simulation software MATLAB/Simulink. We first set up the simulation model and the relevant parameters. Then, we verify the proposed DC-link capacitance design method. Finally, we validate the proposed capacitance-control co-design method.

A. Simulation Setup

We built a two-terminal VSC-HVDC main circuit in MATLAB/Simulink in accordance with Fig. 1. In the main circuit, the switching device, namely the converter, is set up to its average-value model. In the average-value model, the AC side of the converter is represented by three controlled voltage sources, while the DC side is modeled as a controlled current source [30], [31]. Furthermore, the controllers for the sending and receiving end converters are established based on the structures shown in Fig. 2 and 3, respectively.

The parameters of the main circuit model and control are given in Table II.

TABLE II
Parameters of Model and Control

Parameters	Symbol	Value	Unit
Grid frequency	f	50	Hz
Rated AC voltage	U_{s1}	10	kV
Rated DC voltage	U_{dcr}	20	kV
Converter rated power	P_n	10	MW
Rectifier inductance	L_1	19	mH
Rectifier resistance	R_1	0.06	Ω
DC cable resistance	R_{dc}	0.1	Ω
DC cable inductance	L_{dc}	35	mH
Inverter inductance	L_2	19	mH
Inverter resistance	R_2	0.06	Ω
LC filter capacitance	C_f	14	μF
PWM frequency	f_{pwm}	2000	Hz
Inner loop gain	(k_{pi1}, k_{ii1})	(13, 40)	/
Outer loop gain	(k_{pv1}, k_{iv1})	(0.06, 8)	/
Inner loop gain	(k_{pi2}, k_{ii2})	(20, 63)	/
Outer loop gain	(k_{pv2}, k_{iv2})	(0.06, 5)	/

We determine the upper bound of the load power variation interval in a rational manner. This bound is constrained by both the allowable current and the DC voltage utilization rate. Under the allowable current constraint, the maximum output power of the VSC can be obtained based on the rated power. Under another constraint, it can be obtained via power flow calculation. Then, we chose the lower of the two results as the upper bound of load power.

We obtain the specific interval of the equivalent load resistance R_l based on the rated parameters given by Table II. Let the allowable current be 1.5 p.u., then the corresponding power is also 1.5 p.u., i.e., 15 MW. Meanwhile, the DC voltage utilization rate-constrained maximum output power of the VSC is about 11 MW. Taking the smaller one as the upper bound, the interval of the load power is [6 MW, 11 MW]. Then, we can further determine that the uncertain load resistance R_l lies in the interval [9.09 Ω , 16.67 Ω].

The operational constraint set $\mathcal{V}^e$ is constructed from the equilibrium operating points corresponding to the considered load-power range. Specifically, for each sampled load-power condition $P_L^{(j)} \in [P_L^{\min}, P_L^{\max}]$, the nonlinear steady-state equations of the VSC-HVDC system are solved using the `fsolve` function in the MATLAB Optimization Toolbox. The obtained equilibrium point $x^{e,(j)}$ satisfies

$$f(x^{e,(j)}, P_L^{(j)}) = 0. \quad (26)$$

Then, the corresponding operating-variable vector $v^{e,(j)}$ is obtained from the equilibrium solution. By sweeping the load-power interval, a set of equilibrium operating points and the associated operating-variable vectors are obtained. For each component v_i^e , its lower and upper bounds are determined as

$$\underline{v}_i^e = \min_j v_i^{e,(j)}, \quad \bar{v}_i^e = \max_j v_i^{e,(j)}. \quad (27)$$

Therefore, the operational constraint set is constructed as

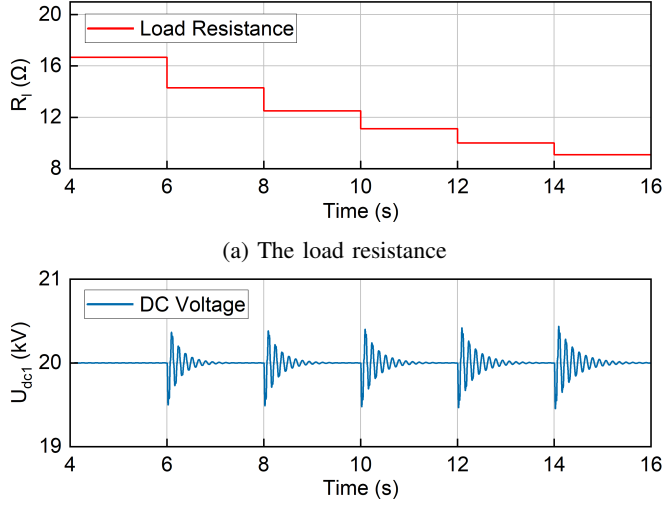
$$\mathcal{V}^e = \{v^e \mid \underline{v}_i^e \leq v_i^e \leq \bar{v}_i^e, i = 1, \dots, n_v\}. \quad (28)$$

In this way, $\mathcal{V}^e$ is obtained from the numerically computed steady-state operating points rather than being directly assigned based on heuristic interval assumptions.

B. Validation of DC-Link Capacitance Design

Based on the rated parameters given in Table II, the base value of capacitance used for normalization is $318 \mu\text{F}$. Under the prescribed uncertainty set and the adopted search precision, Algorithm 1 yields a minimum feasible DC-link capacitance of 3.41 p.u. for the proposed sufficient LMI condition.

The load resistance is inversely proportional to the steady-state power. We consider a decrease in load resistance, corresponding to a uniform increase in steady-state power at a rate of 1 MW per 2 seconds. As shown in Fig. 4(b), when the load resistance varies in the interval $[9.09 \Omega, 16.67 \Omega]$, the system remains stable if the DC-link capacitance is 3.41 p.u.. This simulation result is consistent with the proposed LMI-based capacitance design and verifies the effectiveness of the obtained feasible capacitance.



(b) The DC voltage when the DC-link capacitance is 3.41 p.u.

Fig. 4: The load resistance and DC voltage of the VSC-HVDC system.

C. Validation of Capacitance-Control Co-Design

The results in Section V-B indicate that, using only the existing control structure, the minimum feasible DC-link capacitance obtained under the proposed sufficient LMI condition is 3.41 p.u. To reduce the capacitance requirement and its associated cost, we introduce the feedback control using the method proposed in Section IV. Under the same uncertainty set and search precision, the capacitance-control co-design reduces the minimum feasible capacitance to 0.76 p.u.

However, for the convex feasibility problem (25), if the constraint (24) on the feedback control gain is omitted, the resulting gain $K = YW^{-1}$ becomes excessively large, thereby

invalidating the linearized model. To illustrate this issue, we consider the case where the problem is solved with a DC-link capacitance of 3.41 p.u. We set the integral regulator gain to $k = 6$. As shown in Fig. 5, the system remains stable until approximately 6 ms earlier, at which point the load resistance reaches 16.67Ω , corresponding to a steady-state power of 6 MW. At 6 ms, the state-based feedback control without the proposed gain constraint (24) is introduced. It can be seen that the system becomes unstable approximately 10 ms after. This demonstrates that constraining the feedback gain magnitude is essential in the linearized model-based state-feedback control design to mitigate nonlinear effects and consequently preserve the validity of the linear approximation.

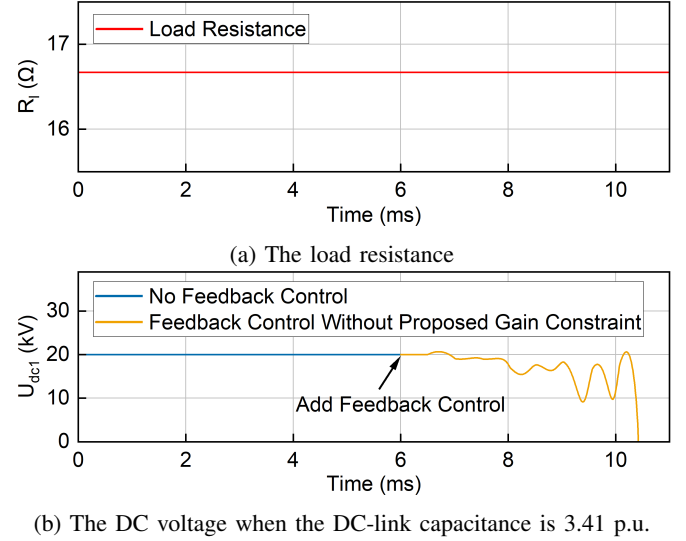


Fig. 5: The load resistance and DC voltage of the VSC-HVDC system with gain unconstrained-feedback control.

In comparison, we impose the constraint (24) in co-design. The resulting lowest DC-link capacitance among those that make the feasibility problem (25) feasible is 0.76 p.u.. With this capacitance, the feedback gain, and the integral regulator gain, the simulation results are shown in Fig. 6(b), demonstrating robust stability across the entire range of load resistance.

In Fig. 6(b), we consider step decreases in the load resistance from 16.67Ω to 11.76Ω and then to 9.09Ω , where each step corresponds to a 2.5 MW increase in the steady-state power demand. It can be observed that after each decrease in load resistance, the DC voltage initially drops and then rapidly returns to the rated value of 20 kV under the action of the state-feedback controller.

The physical mechanism can be explained as follows. When the load resistance decreases, the absorbed load power increases, which tends to discharge the DC-link capacitor and causes a temporary voltage drop. The proposed feedback controller improves the damping characteristics of the system and regulates the power balance, thereby suppressing the voltage oscillation and restoring the DC-link voltage to its steady-state value. Therefore, Fig. 6 verifies that the proposed co-design method can maintain stable DC voltage regulation under load variations even with a relatively small DC-link capacitance.

In addition, the co-design result of 0.76 p.u. is much lower than the 3.41 p.u. obtained without feedback co-design, demonstrating that the proposed co-design effectively reduces the required feasible capacitance.

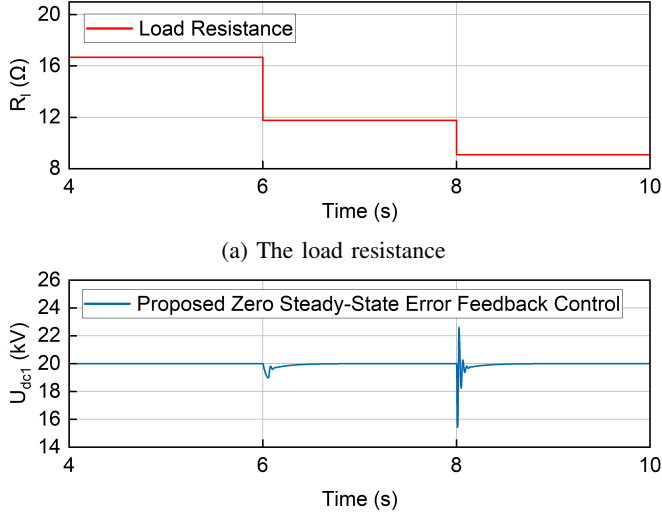


Fig. 6: The load resistance and DC voltage of the VSC-HVDC system with the proposed co-design.

D. Hardware-in-the-Loop Case Study

The OPAL-RT platform is widely applied in power system and power electronics research due to its high-performance hardware-in-the-loop (HIL) capabilities. Utilizing a multi-core CPU combined with FPGA-based parallel computation, OPAL-RT enables microsecond-level real-time simulation of complex power systems and power electronic devices. Unlike offline simulations, it allows external controllers and protection devices to interact with the simulation at real-world sampling frequencies, latencies, and trigger mechanisms. The platform reduces experimental risk and cost, allowing repeated testing under diverse fault scenarios and extreme conditions. OPAL-RT5600 integrates a powerful Intel CPU and Xilinx FPGA boards, providing up to 128 analog and 256 digital high-speed I/O channels for precise real-time control and measurement.

The RT-LAB platform complements OPAL-RT by providing a distributed computing environment that orchestrates multiple targets for real-time simulation. The software framework allows automatic code generation, compilation, and deployment onto target hardware, ensuring seamless interaction between the host computer and the real-time simulation nodes. The system supports multi-core synchronization, real-time task scheduling, and precise execution of control algorithms, making it ideal for verifying controller performance and system stability under varying operating conditions. Fig. 7 illustrates the overall setup of the OPAL-RT real-time simulation platform, including the main chassis, oscilloscope, and host computer used for HIL experiments.

Using OPAL-RT and RT-LAB, we constructed a two-terminal VSC-HVDC system to validate the proposed DC-link capacitance sizing and co-designed state-feedback control.

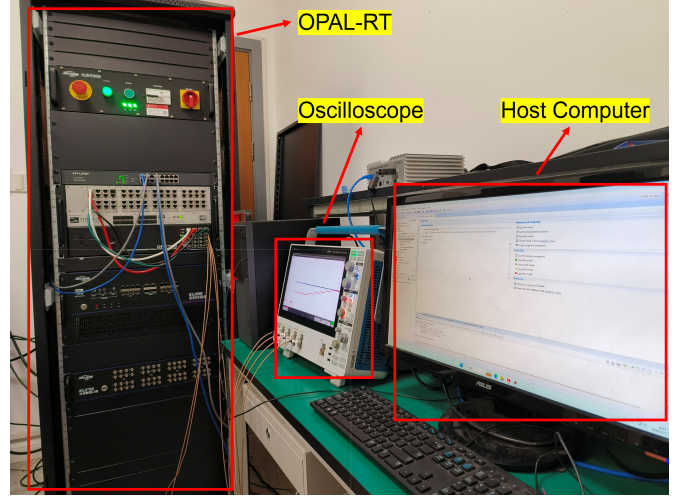


Fig. 7: Overview of the OPAL-RT Real-Time Simulation Platform

The main circuit and control algorithms were implemented according to the models described in Sections II and III. Fig. 8 and Fig. 9 show the DC voltage and load power responses of the VSC-HVDC system under different DC-link capacitances and control schemes, illustrating the effect of adding state feedback on system stability. Results demonstrate that with the baseline DC-link capacitance of 3.41 p.u., the system remains stable under load variations within [6 MW, 11 MW]. Furthermore, with the co-designed state-feedback control, the required DC-link capacitance can be reduced to 0.76 p.u. while maintaining robust stability. The DC voltage converges to its reference value across all tested scenarios, illustrating the effectiveness of the proposed methodology.

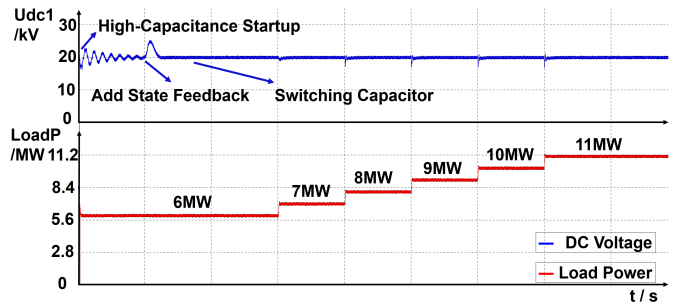


Fig. 8: Load Power and DC Voltage with DC-Link Capacitance of 3.41 p.u. under No State Feedback

E. Computational Benchmarking

To further clarify the optimization aspect and evaluate the computational efficiency of the proposed method, the conventional vertex-based method is adopted as a benchmark. The vertex-based method is selected because it is a direct and rigorous approach for robust stability verification of uncertain linear systems. Specifically, it checks the LMI stability condition at all vertices of the uncertainty polytope. Therefore, it can provide a relatively non-conservative reference result for the minimum feasible DC-link capacitance. However, its

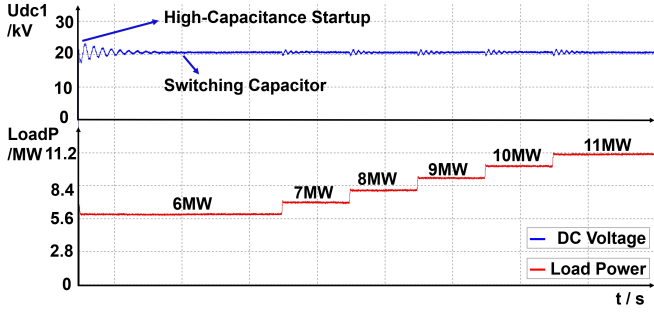


Fig. 9: Load Power and DC Voltage with DC-Link Capacitance of 0.76 p.u. under State Feedback

computational burden increases rapidly with the number of uncertain variables due to exhaustive vertex enumeration.

For a fair comparison, the initial search interval of the DC-link capacitance is set as 0–10 p.u., and the search accuracy is set as 0.001 p.u. for both methods. The benchmark results are shown in Table III.

TABLE III

Benchmark comparison of different capacitance design methods

Method	Minimum capacitance	Wall-clock time
Vertex-based method with 2^{11} vertices	3.203 p.u.	3412.9 s
Proposed 2-LMI method	3.410 p.u.	26.3 s

As shown in Table III, the vertex-based method obtains a minimum feasible capacitance of 3.203 p.u., while the proposed 2-LMI method obtains a feasible capacitance of 3.410 p.u. This indicates that the proposed method introduces about 6.5% additional conservativeness in terms of the capacitance result. However, the wall-clock time is reduced from 3412.9 s to 26.3 s, corresponding to an approximately 129.8-fold acceleration. Therefore, the proposed method significantly improves the computational efficiency at the cost of only slight additional conservativeness, which provides a practical trade-off for robust DC-link capacitance optimization.

F. Sensitivity Analysis

The co-design result reported above is affected by the regulation parameters introduced in constraint (24). To clarify this dependence, we further conduct a sensitivity analysis with respect to these parameters. Let

$$\Delta x'(0) = \rho x'_{e0}, \quad \mu = \eta U_{dcr},$$

where ρ determines the size of the initial perturbation considered in the invariant ellipsoid constraint, and η determines the allowable magnitude of the feedback action.

Table IV reports the minimum feasible DC-link capacitance under different values of ρ and η . It can be observed that increasing ρ generally leads to a larger minimum feasible capacitance, since a larger initial region needs to be certified. In contrast, increasing η reduces the required capacitance be-

TABLE IV

Minimum feasible DC-link capacitance under different regulation parameters.

$\eta \backslash \rho$	0.005	0.010	0.015	0.02
0.005	0.76	0.46	0.35	0.29
0.010	1.22	0.76	0.57	0.46
0.015	1.53	1.02	0.76	0.62
0.020	1.85	1.22	0.94	0.76

cause the feedback controller is allowed to provide a stronger stabilizing action. These results indicate that the reported capacitance reduction is not only determined by the physical system parameters, but also by the admissible feedback magnitude and the size of the certified operating region.

We also investigate the influence of the load uncertainty range. Table V shows the minimum feasible capacitance under different load power intervals. As the uncertainty range increases, the required capacitance increases accordingly. This is because the robust stability condition needs to hold for a larger set of admissible Jacobian matrices. Nevertheless, the proposed co-design method remains feasible over the tested uncertainty ranges and consistently reduces the required capacitance compared with the original control structure.

TABLE V

Minimum feasible DC-link capacitance under different load uncertainty ranges.

Load power range	Original control	Co-design
[8, 9] MW	0.75	0.22
[7.5, 9.5] MW	0.89	0.29
[7, 10] MW	1.05	0.38
[6.5, 10.5] MW	1.28	0.52
[6, 11] MW	3.41	0.76

VI. CONCLUSION

This paper addresses the problem of DC-link capacitance design in VSC-HVDC systems under uncertain loading conditions. Sufficient conditions for robust stability and capacitance-control co-design synthesis method are developed. From the theoretical derivations and numerical studies, this work verifies the engineering observation that if the load power is below a certain threshold for a given capacitance, the system may remain stable. On the other hand, regarding a given load power, the system keeps stable with a capacitance exceeding a corresponding value. In addition, the proposed method can potentially be extended to the robust stability analysis and control synthesis for other systems with multi-parameter uncertainties.

The proposed method can also be extended to other VSC-HVDC topologies because its core procedure relies on an uncertainty-dependent small-signal model and a robust LMI stability condition. For MMC-based HVDC or multi-terminal VSC-HVDC systems, similar robustness analysis can be applied by modifying the state vector, the small-signal Jacobian

matrix, the uncertainty set, and the uncertainty decomposition matrices according to the corresponding topology. In particular, MMC internal dynamics and multi-terminal DC network coupling should be incorporated into the model. These extensions of the proposed capacitance design framework will be investigated in future work.

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