

Room temperature single electron charging in single silicon nanochains

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Single-electron charging effects are observed at room temperature in single Si nanochains. The nanochains, grown by thermal evaporation of SiO solid sources, consist of a series of Si nanocrystals ~ 10 nm in diameter, separated by SiO₂ regions. Multiple step Coulomb staircase current-voltage characteristics are observed at 300 K in devices using single, selected, nanochains. The characteristics are investigated using a model where the nanochain forms a multiple tunnel junction. The single-electron charging energy for a nanocrystal within the multiple-tunnel junction is $E_C = e^2/2C_{\text{eff}} \sim 0.32$ eV, $\sim 12k_B T$ at 300 K. © 2008 American Institute of Physics.

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Grown silicon nanowires (SiNWs) and nanochains are among the most promising materials for the development of nanometer-scale electronic devices fabricated by material synthesis.^{1,2} These nanostructures can, in principle, form building blocks to assemble nano-devices in a “bottom-up” approach, removing the need for high-resolution lithography.³ SiNWs ~ 10 nm or less in diameter and ~ 1 μm in length and Si nanochains consisting of a series of ~ 10 nm diameter Si nanocrystals (SiNCs) separated by narrow SiO₂ regions, may be prepared by chemical vapour deposition⁴ or by thermal evaporation of solid sources.² At present, most research work has investigated single crystal SiNWs, aiming at realizing nanoscale field-effect transistors and devices for circuit application.^{3,5,6} In contrast, there is comparatively little work on the electrical properties of Si nanochains.

The morphology of Si nanochains suggests that they may form a one-dimensional array of nanoscale islands (the SiNCs) isolated by tunnel barriers (the SiO_x regions), raising the possibility of single-electron and quantum confinement effects⁷ in the SiNCs. Single-electron effects require that the island charging energy for one electron, $E_C = e^2/2C \gg k_B T$, where C is the island capacitance and the measurement temperature is T . The ~ 10 nm scale of the SiNC islands in Si nanochains suggests that C may be ~ 1 aF or less and T may be raised to room temperature, raising the possibility of the bottom-up fabrication of room-temperature single-electron devices.

Single-electron transistors (SETs) operating at RT have been fabricated using a “top-down” nanolithographic approach, with islands ~ 10 nm or less in size.^{8–11} Other RT SETs have used a combination of nanolithography and nanoscale material structure, e.g., a nanotextured thin film¹² or a nanocrystalline Si thin film,¹³ to define the islands. SETs have been fabricated in single crystal SiNWs formed by a chemical vapor deposition reaction,⁵ however, the maximum operating temperature was less than ~ 30 K. In these devices, the tunnel barriers were defined by the contacts to the SiNW. The ~ 100 – 400 nm SiNW section between the contacts, lithographically defined by the contacts, behaved as a single quantum dot with capacitance $C \sim 10$ aF, too large for RT single-electron charging. In measurements of large bundles of SiNWs and nanochains,¹⁴ a “Coulomb staircase”⁷ current-voltage (I - V) characteristic was observed at RT attributed to single-electron effects in SiNCs within the bundle. However, the large number of SiNWs and nanochains in the bundle complicates detailed analysis of the results.

In this paper, we characterize a *single* Si nanochain device and report the observation of strong single-electron effects at RT. Our nanochains, prepared by thermal evaporation of SiO, consist of SiNCs ~ 10 nm in diameter, separated by narrow SiO₂ regions. Ti/Al contacts are fabricated to select nanochains to create single nanochain devices. Each nanochain “naturally” defines a multiple-tunnel junction^{7,11,15,16} (MTJ) and both the islands (the SiNCs) and the tunnel barriers (the SiO₂ regions) are defined completely by the nanochain morphology. Single-electron charging in the MTJ leads to multiple step Coulomb staircase characteristics at 300 K. The single-electron charging energy for a nanocrystal within the MTJ is $E_C = e^2/2C_{\text{eff}} \sim 0.32$ eV $\sim 12k_B T$ at 300 K.

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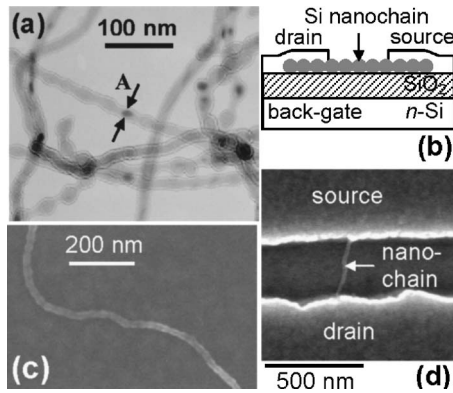


FIG. 1. (a) Transmission electron micrograph of Si nanochains, prepared by thermal evaporation of SiO. The image is slightly underfocused to emphasize diameter variations. A JEOL 200CX transmission electron microscope was used. (b) Schematic of a Si nanochain device. (c) Scanning electron micrograph (SEM) of a Si nanochain deposited on SiO₂. (d) Scanning electron micrograph of a Si nanochain device.

The Si nanochains were synthesised by thermal evaporation of a SiO powder solid source (99.99% purity) at 1400 °C in a quartz tube furnace.¹⁷ Ar gas carried the vapour through the tube. Undoped SiNWs were synthesized in a cooler part of the furnace at 900–950 °C. Depending on the growth conditions, 50%–90% of the SiNWs formed nanochains, with SiNCs separated by SiO₂ “necks.” Figure 1(a) shows a transmission electron micrograph of nanochains grown at an ambient pressure of 800 mbars, dispersed on a copper grid from isopropyl alcohol (IPA) solution. In different nanochains, the SiNC diameter varies from <10 to ~30 nm and the separation varies from ~15 to 40 nm. The SiNC marked “A” has a diameter of ≈12 nm. A thin SiO₂ layer, ~1–3 nm thick, exists on the SiNC outer surface. The width of the necks varies from approximately the diameter of the SiNCs to well below this value.

The number of SiNC in a given nanochain depends on the length of the SiO₂ necks between the SiNCs. It is possible to control this length by controlling the ambient pressure in the furnace tube during growth.^{2,17} In investigations of the nanochain formation process,¹⁷ we find that as the ambient pressure is increased from 400 to 800 mbars, SiNW and nanochains of different morphologies are deposited. At 400 mbars, in different nanochains, the length of the SiO₂ necks can vary from ~20 nm to several hundred nanometres. In contrast, at 800 mbars, the majority of the deposited material consists of uniform SiNWs and the percentage of nanochains in the material is small. In these nanochains, the SiO₂ necks are only a few nanometers in length. At intermediate pressures, intermediate values of SiO₂ neck length predominate. If the neck lengths are ~20 nm or greater; they form highly resistive tunnel barriers and the nanochains tend not to conduct. In contrast, neck lengths of ~10 nm or less lead to conducting nanochains, suitable for single-electron applications. In a particular device, the number of SiNCs (and the corresponding MTJ length) between the source and drain contacts may be controlled by selecting a nanochain with a suitable neck length and then by choosing a suitable source-drain contact separation.

The Si nanochain devices were fabricated by defining Ti/Al contacts to selected single nanochains, using electron-beam (e-beam) lithography in polymethyl methacrylate resist. Figure 1(b) shows a schematic of the device. The devices were defined on silicon-on-insulator (SOI) material with an ~50 nm thick SiO₂ capping layer, grown thermally on the top-Si layer of the SOI material. The top-Si layer, 300 nm thick and doped *n* type to a concentration of $1 \times 10^{19}/\text{cm}^3$, formed a conducting back plane for the device, with the potential to form a back gate. Initially, an array of Cr/Au alignment marks was fabricated by e-beam lithography on the SiO₂ capping layer. Next, hexamethyldisilazane vapor treatment of the surface was used as an adhesion promoter for the nanochains. Nanochain material from the furnace, dissolved in IPA (0.1 mg/3 ml IPA) using ultrasonic tip agitation, was then spun onto the sample at 5000 rpm. Figure 1(c) shows a scanning electron micrograph (SEM) of a slightly thicker ~20 nm wide nanochain where the mean separation between nanocrystal centres is ~28 nm and the standard deviation is ~4.5 nm, a variation of $\pm 16\%$. Individual nanochains were then selected with reference to the alignment marks, by scanning electron microscope inspection. Finally, 20 nm Ti/75 nm Al contacts were evaporated on to the nanochain, after wet etching of the SiO₂ layer around the nanochain in the contact regions. Ti/Al contacts can form better contacts to silicon nanowires.³ Furthermore, as our nanochains are undoped and high resistance tunnel barriers exist within the nanochains at the SiO₂ necks, the total resistance of the device is likely to be dominated by the nanochain rather than the contacts. Following device fabrication, the *I*-*V* characteristics of the devices were measured in vacuum, at $\sim 10^{-6}$ mbar. Figure 1(d) shows a scanning electron micrograph of a device with a source-drain separation of ~300 nm. The micrograph was obtained after electrical measurement of this device.

Figure 2(a) shows the drain current I_D , the source current I_S , and the back-plane current I_B versus the drain-source voltage V_{DS} , in a nanochain device (device A) at 300 K. The back-plane voltage $V_B=0$ V. The source-drain separation in this case was ~180 nm, the nanochain width was ~20 nm, and there were seven SiNCs along the nanochain. The current I_D increases in a stepwise manner with V_{DS} (steps marked with arrows), forming a Coulomb staircase.^{7,15} I_S (stepped by 10 pA) and I_D are seen to be similar. The leakage current to the back plane, I_B remains within the noise level, <0.1 pA. The values of I_D , I_S , and I_B confirm that the current flows through the nanochain and not via the back plane. I_D is low because of the small size and undoped nature of the nanochain.

Figure 2(b) shows I_D plotted on a log scale. Three current steps (arrowed) can be identified in the characteristics, at approximately 0.45, 1.5, and 3 V. A faint, fourth step may exist at ~4 V [clearer in Fig. 2(a)]. The current below the first step is within the noise level. The threshold voltage for current flow, $V_T \approx 0.45$ V, corresponds to the edge of the “Coulomb blockade” region.⁷ Using the back plane as a gate, it was difficult to measure complete I_D versus V_{DS} and V_B characteristics, as I_D was not sufficiently stable when V_B was varied.

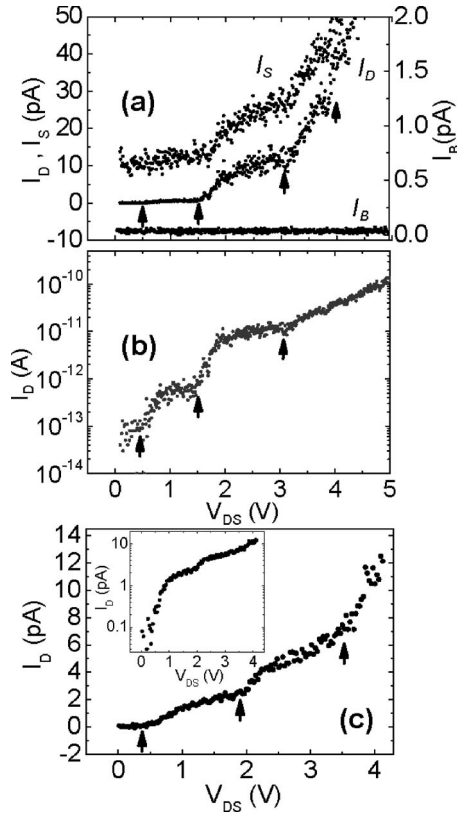


FIG. 2. (a) I - V characteristics of a Si nanochain device (device A), measured at 300 K. I_S is offset by 10 pA for clarity. (b) Log-linear plot of I_D - V_{DS} for device A. (c) I - V characteristics of a second device (device B), measured at 300 K. The inset shows a log-linear plot of I_D - V_{DS} for device B.

Figure 2(c) shows the I_D - V_{DS} Coulomb staircase at 300 K from another device [device B, shown in Fig. 1(d)], where the source-drain separation was ~ 300 nm. There were approximately 12 SiNCs in this device. Here, $V_T \approx 0.35$ V and two steps at 1.9 and 3.6 V are visible. The inset of Fig. 2(c) shows I_D plotted on a log scale.

We investigate the Coulomb staircase characteristics in our devices qualitatively, using single-electron Monte Carlo simulations.¹⁸ We use N junction MTJ circuit to model the nanochains in our devices [Fig. 3(a)], assuming equal junction capacitances C and island stray capacitances C_0 for simplicity. In our devices, C_0 corresponds mainly to the SiNC to back-plane capacitance. Our observation of a Coulomb staircase suggests a strong asymmetry in the junctions along the MTJ and we include the effect of this by means of a random variation in the tunnel junction resistances R_n . Such a variation may be caused by our observed variation in SiNC separation. We note that there is also likely to be an associated variation in C , although we neglect this in our analysis for simplicity. The variation in C would further increase the MTJ asymmetry, further improving the Coulomb staircase. It is, however, likely that R_n varies more with the SiNC separation, due to the greater sensitivity of the tunnel current to changes in the tunnel barrier width.

Figure 3(b) shows the simulation results for device B (solid line), compared to the experimental data (open circles), with I_D on a log scale. The inset shows the same data on a linear scale. In this device, the number of junctions

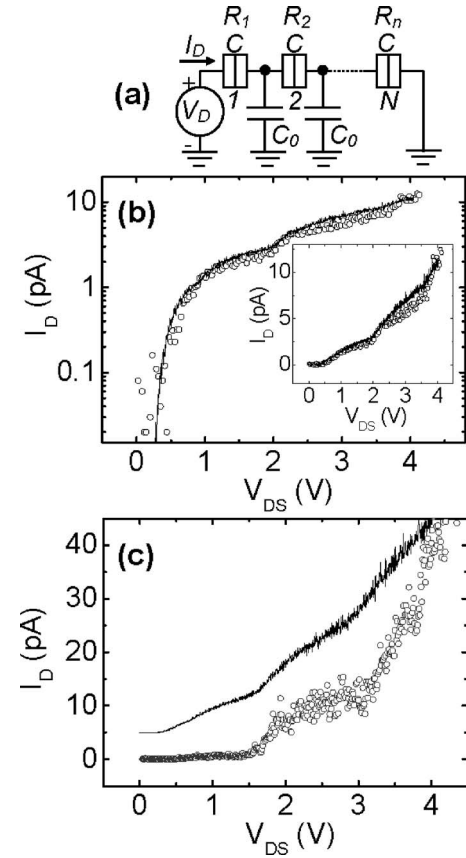


FIG. 3. (a) MTJ circuit model for a nanochain. The circuit is used for single-electron Monte Carlo simulations of our devices. (b) Simulated (solid line) and experimental (open circles) I_D - V_{DS} characteristics of device B, on log-linear scale. The inset shows these characteristics on a linear scale, with the simulation data offset by 2 pA for clarity. (c) Simulated (solid line) and experimental (open circles) I_D - V_{DS} characteristics of device A, with the simulation data offset by 5 pA for clarity.

$N=13$ is determined by the number of nanocrystals in the device observed in SEM images. The values of C and C_0 are 0.12 and 0.1 aF, respectively, determined by matching the experimental values of $V_T \approx 0.35$ V, and the step positions, $V_{DS}=1.9$ and 3.6 V. This gives $C=0.12$ aF and $C_0=0.1$ aF. R_n varies randomly within 50% of a mean tunnel resistance of $R_{av}=8.2$ G Ω (maximum value: 10 G Ω , minimum value: 4.5 G Ω), in order to reproduce the Coulomb staircase steps. Figure 3(c) shows the simulation results for device A, obtained using a similar process. Here, $N=8$ (determined from an SEM image of the device), $C=0.12$ aF, and $C_0=0.12$ aF (very similar to Device B), $R_{av}=6$ G Ω , and the random variation in R_n was within 60% of R_{av} (maximum value: 9.4 G Ω , minimum value: 2.8 G Ω). While this simulation reproduces the step positions in the data, it does not reproduce the nonlinear increase in current along the staircase, predicting a sharper increase in the current at the first step. Our simple simulation model does not include the possibility of a reduction in the tunnel resistances with V_{DS} or a Schottky barrierlike potential in series with the MTJ.¹⁹ In both cases, a higher resistance would occur at low bias, reducing at higher bias. This would lead to the increasing current observed in the data.

We can compare C and C_0 to our SiNC size. The total capacitance connected to a SiNC in device B is $C_T=2C$

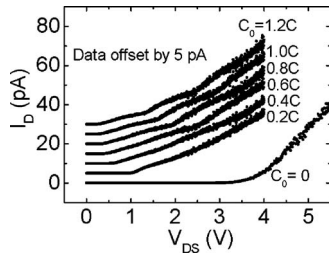


FIG. 4. Simulated I_D - V_{DS} characteristics for a nanochain, with C_0 increasing from 0 to $1.2C$. All simulation parameters except C_0 are similar to those used in Fig. 3(c), for device A. Curves offset from each other by 5 pA for clarity.

+ $C_0 \sim 0.34$ aF. We can compare this to the self-capacitance $C_S = \{4\pi\epsilon_r\epsilon_0 ab/[b+a(\epsilon_r-1)]\}$ of a sphere of radius a , surrounded by a shell of outer radius b and dielectric constant ϵ_r . For a SiO_2 shell ($\epsilon_r=3.9$) with $b=5$ nm, $C_S=C_T=0.34$ aF can be used to obtain the radius of the conducting core of the SiNC, $a=3$ nm, and a shell thickness $b-a=2$ nm. This is very similar to the SiNCs in the nanochains in Fig. 1(a). However, as the self-capacitance of the SiNC may be somewhat smaller than 0.34 aF, this implies that a may be less than 3 nm.

Our MTJ simulations require significant stray capacitance C_0 to reproduce both the low observed values of V_T and the wide step widths in the Coulomb staircase. Figure 4 models the effect of increasing C_0 from 0 to $1.2C$, with all other parameters similar to the simulation data in Fig. 3(c). As C_0 increases, V_T reduces and the clarity of the staircase improves. For $C_0=0$, a high value of $V_T \sim 4$ V is observed. This value corresponds approximately to the sum of the individual charging energies of the SiNC, i.e., $V_T \sim (N-1)e/2C = 4.6$ V.⁷ In our experiments, removing the contact to the back plane in a device leads to I_D - V_{DS} characteristics similar to the $C_0=0$ curve, supporting a model including C_0 . As C_0 increases, a greater proportion of V_{DS} drops across the first tunnel junction, due to the voltage divider formed by the first junction capacitance C , and the first stray capacitance C_0 parallel with the equivalent capacitance of the rest of the MTJ.¹⁵ The charging energy of the first junction is then overcome at lower voltages, leading to a lower onset of current and reduced V_T . At $C_0=1.2C$, V_T is reduced to only 0.25 V. Finally, we may estimate the single-electron charging energy of the SiNCs. For a SiNC in the center of the MTJ, approximating the two halves of the MTJ as semi-infinite capacitive networks, the SiNC effective capacitance is $C_{\text{eff}}=(C_0^2+4CC_0)^{1/2}$.⁷ For device B, we find that $C_{\text{eff}}=0.25$ aF and the single-electron charging $E_C=e^2/2C_{\text{eff}} \sim 0.32$ eV $\sim 12k_B T$ at 300 K. We note that C_{eff} is lower than the total capacitance attached to an island, $C_T=2C+C_0$

~ 0.34 aF. E_C is then higher for a SiNC embedded within a MTJ, as compared to a single SiNC, leading to an improvement in the Coulomb staircase.

In conclusion, we report single-electron effects at room temperature in single Si nanochain devices. The nanochains are prepared by thermal evaporation of SiO and consist of a series of SiNCs ~ 10 nm in diameter. Single-electron charging in the MTJ leads to multiple step Coulomb staircase characteristics at 300 K. The charging energy for a nanocrystal within the MTJ, $E_C=e^2/2C_{\text{eff}} \sim 0.32$ eV $\sim 12k_B T$ at 300 K.

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