A HIGH SPEED DATA ACQUISITION AND ANALYSIS SYSTEM FOR LOCATING FAULTS IN POWER LINES

by

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ABSTRACT

This thesis describes the development of a high speed data acquisition and analysis system for the investigation of fault location in electric power lines and cables. The system is intended to be used to measure and acquire data from real lines and cables for analysis. In particular it is used to investigate the practical effectiveness of a fault locating algorithm resulting from previous theoretical work, with the idea of automating the fault location operation.

The system works by injecting an interrogating pulse into the input of the suspected line or cable and recording the digitized input voltage and current via the high speed data acquisition unit. The recording modes are versatile and can be selected to cater for a wide variety of parameter values, such as, input attenuation levels, trigger level, pre and posttrigger and works up to a maximum sampling frequency of 20 MHz.

The analysis of the recorded data is performed via a travelling wave based algorithm, which takes the telegraph equations as the transmission line model. From the recorded voltage and current the algorithm generates estimated voltage and current profiles along the length of the line based on the solutions to the telegraph equations. A time average function involving the square of the estimated voltages is used to locate the point of fault.

The "sensitivity" of the method is increased by setting parameter values such as pulse generator output impedance and data window length to values found to be optimum.

The overall performance of the system has been assessed with data obtained from a physical model of a transmission line and from a real coaxial cable. Satisfactory results have been obtained for the different kinds of faults that occur in an overhead transmission line and for short circuit or low resistance faults in underground cable.

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I am particularly grateful to Lizbeth, my wife, for the moral support she offers me and for the long hours she spent typing this thesis.

To Lizbeth and my Parents,
for all the love they give me.

INDEX

FIGURES

CHAPTER 1.

CHAPTER 2.

CHAPTER 3.

TABLES

INTRODUCTION

The main function of an Electricity Supply Authority is to maintain a constant supply of electricity to its consumers at the stated voltage and frequency at a reasonable cost. In order to fulfill this obligation , an essential requirement is the fast detection, location and repair of any fault on the electric power system.

In general, for a three phase system,a fault develops from a reduction of the basic insulation strength between phase conductors, or between phase conductors and earth. This reduction is not regarded as a fault until is detectable, that is, until it results either in an excessive flow of current or in a reduction of the impedance between conductors , or between conductors and earth, to a value below that of the lowest load impedance normal to the circuit. Thus a high degree of pollution on an insulator string, although it reduces the insulation strength of the affected phase, does not become a fault until it causes a flashover across the string, which in turn produces excess current or other detectable abnormality.

Amongst the causes of faults are : on overhead lines - lightning, ice and snow loading, broken insulators, open circuit conductors ; in machines cables and transformers - failure of solid insulation because of moisture, mechanical damage, accidental contact with earth. All incidents arising from these causes are called "system" faults. There is another kind of faults known as "non system" faults which are a consequence of human error in testing or maintenance work or incorrect settings in the protection equipment.

Recent published statistics [1] , related to the system faults in the CEGB's 400 kV. and 275 kV. systems and some lower voltage circuits, are shown in Table 1.1. These statistics cover five consecutive years of a typical five-year period. From the table it can be noted that, on average, over the five year period, approximately 63% of the system faults occurred in the overhead line and cable circuits. The fast location and repair of faults in these circuits is therefore of great importance.

This thesis addresses the fault location problem in overhead lines and underground cable. Chapter 1 describes some fault location methods for overhead lines and

underground cable in present use. Its principle of operation and main advantages and drawbacks are reviewed. Additionally, some real fault locators are described in order to gain an idea of the present state of the fault location operation. The objective of this research work is established at the end of this chapter.

The main features and details of design, construction and testing of the fault locator apparatus developed during the course of this work and which forms the main thrust of this thesis are described in chapter 2.

Chapter 3 describes the tests carried out and the results obtained while assessing the overall performance of the fault locator apparatus and, in particular, of the fault location method to be introduced in section 1.1.5.

Chapter 4 includes the conclusions and suggestions for further work.

Type of Plant or Equipment concerned	Year 1	2	3	4	5
Overhead Line and Cable Circuits.	435	460	293	269	174
Transformers and Reactors	91	100	102	49	32
Generators and generator transformer	89	75	66	65	51
Busbars and Switchgear.	50	32	31	33	27
Other (motors, compensators, etc.)	7	11	13	13	11

TABLE I.1. Distribution of system faults on the CEGB system over a typical five-year period.

CHAPTER 1

FAULT LOCATION METHODS AND FAULT LOCATORS

1.0 INTRODUCTION.

This chapter gives a brief survey of fault location methods for overhead transmission lines and underground cable. First is given the description corresponding to overhead lines followed by that for underground cable. The separation is being made on the grounds that, as it will be seen later, the fault location in underground cable may be considered more demanding since greater accuracy is required than with overhead lines, and includes an additional stage for the exact location of the fault. A description of some fault locators is also included and the objective of this research work is established .

1.1 FAULT LOCATION METHODS FOR OVERHEAD LINES.

1.1.1 FAULT CLASSIFICATION.

Broadly speaking the faults that occur in an overhead line can be classified into the following types:

a) Momentary fault.- This type of fault is also called "nonpermanent" or "transient";

this kind of fault permits successful reclosure, as for example, a lightning flashover not causing major damage.

b) Sustained fault.- Also called "permanent", includes conductor or conductors grounded, short circuited or open. Successful reclosure is not possible, e.g., line conductor in direct contact with tower.

c) High breakdown faults.- These do not appear as faults when ordinary low-voltage test devices are used, however, successful reclosure is not possible, for example, impaired clearance from conductor to ground without actual contact, or heavy damage to insulators.

d) Latent fault.- Consists in a localized impairment of insulation which does not prevent successful operation under normal conditions, but reduces insulation margin provided in design for surges and dynamic overvoltages. It does not become a real fault until it is detectable.

1.1.2 FAULT LOCATION METHODS CLASSIFICATION.

Fault location methods may be classified in terms of many different criteria such as :

a) Quantity measured: intrinsic electrical quantity or travelling wave propagation time.

b) Type of fault to which it is best applied: momentary, sustained, high breakdown, or latent.

c) Mobility of equipment: fixed or portable.

d) Method of operation: automatic or manual.

e) Condition of line: energized or unenergized during measurements.

f) Type of travelling wave: fault generated surge or applied wave or pulse.

If the first classification criterion is adopted, the fault location methods based on measurements taken at one or more points on the line can be classified into two categories[2]:

a) Those based on the measurement of intrinsic electrical quantities and,

b) those whose basic operating principles rely on travelling wave time.

1.1.3 METHODS BASED ON THE MEASUREMENT OF INTRINSIC ELECTRICAL QUANTITIES.

This classification includes methods based on the measurement of current, current and voltage, reactance or impedance, and resonance frequencies of the line.

1.1.3.1 Resonance Frequency.

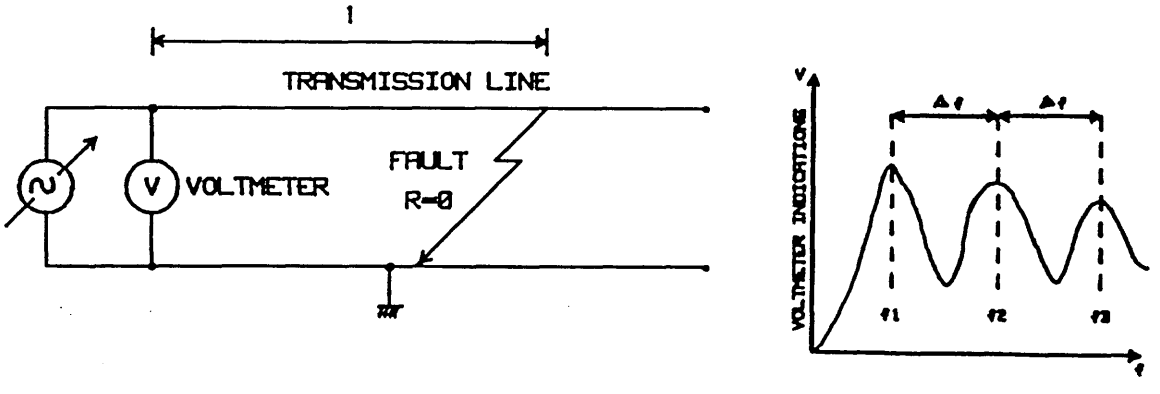
The resonance frequency method operates on the principle that standing waves are produced on a line which has a discontinuity or impedance mismatch such as a fault. A length of line l will resonate to a sinusoidal voltage signal for a frequency f_1 for which l represents one quarter of a wavelength or multiples of this. A variable frequency voltage source is connected to one end of the line. The transmitted wave and the reflected wave from the point of fault add together and produce points of maxima and minima. By varying the frequency, voltage maxima and minima can be produced in succession at the line terminal and the distance to the point of fault calculated from the frequency difference between successive maxima or minima.

The distance from the measuring end to the point of fault is given by :

$l = v/[2\ \Delta f]$,

l = length of line or length between measuring point and point of fault [meters].
v = velocity of propagation, [meters/s].
Δf = frequency interval, [Hz].

Figure (1.1) ilustrates this principle:



(a) Standing waves measurement principle. b) Voltage-frequency characteristic.

Figure 1.1. Resonance frequency method.

This method is simple since it gives quantitative indications and it does not require skilled personnel for its application. Its main drawback is that if discontinuities between the measuring point and the fault exist, (e.g., joints, specially in underground cable) they will also produce standing waves making the interpretation more difficult.

1.1.3.2 Impedance Measurement.

The main task of a power system protection engineer is concerned with limiting the effects of disturbances on the system, which, if allowed to persist, may damage plant and interrupt the supply of electric energy. To facilitate speedy removal of a disturbance from a power system, the system is divided into "protection zones", and relays monitor the system quantities (current, voltage) appearing in these zones; if, for example, a fault occurs inside a zone, the relay operates to isolate the zone from the remainder of the power system.

Several schemes exist to establish whether or not a fault is within a given zone. One of such schemes is known as distance protection. Its principle of operation derives from the fact that the impedance of a transmission line is proportional to its length, it is possible then, to use a relay capable of measuring the impedance of the line up to a given point. A relay with this capability is referred to as distance relay, and is designed to operate only for faults occurring between the relay location and the selected point, thus giving discrimination for faults that may occur between different line sections [3].

The basic principle of operation consists in the comparison between the current "seen" by the relay with the voltage at the relaying point; from this comparison it is possible to measure the impedance of the line up to the fault point. Figure (1.2) shows a simple example of how this comparison is made using a "balanced beam" relay.

The relay is connected at position R and receives a secondary current proportional to the primary fault current and a secondary voltage proportional to the product of the fault current and the impedance of the line up to the point of fault. The primary winding of the current transformer is connected in series with the power circuit; the impedance of the primary winding is negligible compared with that of the power circuit, even if the transferred effects of the secondary circuit are included, so that the impedance of the power circuit entirely controls the flow of current.

If the relay is designed so that its operating torque is proportional to the current and its restraining torque proportional to the voltage, then, according to the relative number of ampere-turns applied to each coil, there will be a definite ratio at which the torques will be

equal. This is known as the balance point of the relay.

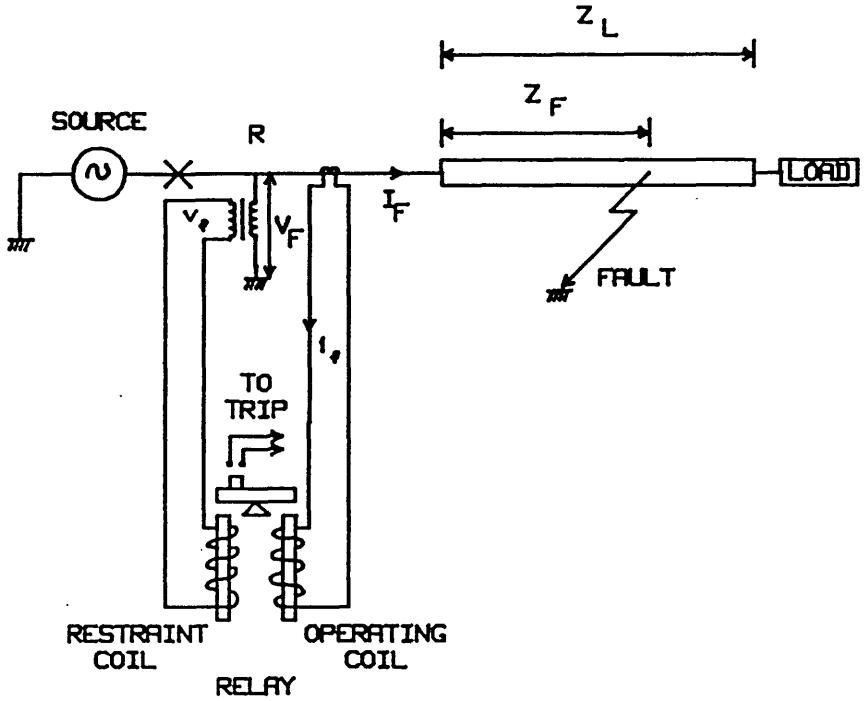


Figure 1.2. Simple impedance relay of the balanced beam type.

Below a given ratio of V/I the operating torque will become larger than the restraining torque and the relay will close its contacts. On the other hand, above a given ratio of V/I the restraining torque will be greater than the operating torque, the relay will restrain and the contacts will remain open. Such relays have been designed so that it is possible to adjust their ohmic setting by changing the relationship of the ampere-turns of the operating coil to those of the restraint coil, making it possible to select a setting suitable for the length of the line to be protected. The "balance beam" relay is an amplitude comparator, because the resultant torque is entirely dependent on the magnitude of the input quantities.

During the past decade and with the introduction of digital computers into distance protection the basic idea of impedance measurement has evolved and has been refined. The basic objective has been extended and, in addition to isolating the fault for protection purposes, new approaches make use of digital samples of line voltages and currents, which are analysed by an appropriate algorithm[4] in order to locate the fault. This algorithm calculates the series impedance of the line from the relay location to the fault

point from the available voltage and current samples and then compares this calculated impedance with that corresponding to the zone covered by the relay in order to determine whether the fault occurs within this zone or not. The calculated impedance is that related only to the power frequency voltages and currents which are extracted by using filters or Fourier analysis to remove high frequency components and in some occasions d.c. offset from the recorded fault voltage and current waves. This new type of computer based relays are referred to as digital distance relays. The calculated impedance R+jX provides an exact distance to the fault, provided that the fault resistance is zero, however, the fault resistance is not zero in many actual faults, causing the impedance R+jX to deviate from its true value, therefore, the digital distance relays would be susceptible to error in calculating the exact impedance to the fault.

Recent research work[5],[6] has found that the effect of the fault resistance is to introduce a phase shift between the current which flows through the fault resistance and that measured at the end of the line, the fault resistance is then recognized as an impedance with both resistive and reactive components, leading to the error in the fault location. In order to correct this error, Wiszniewski [5] introduced a correction equation which neutralizes the phase shift effect in a simple non iterative computation, Ziegler [6] proposed to use a fault locator at each line end, and take as distance to the fault the shorter one. This would give a measuring accuracy of 5%.

Several other researchers [7],[8], have proposed alternative solutions which eliminate the influence of the fault resistance upon the accuracy of fault location, (one of these methods will be reviewed in more detail later, since it is used as the operating principle in a real fault locator).

A common factor in the above methods is the need for removing the high frequency components from the recorded fault voltage and current waves using filters or Fourier analysis.

1.1.4. METHODS BASED ON TRAVELLING WAVES

Most travelling wave based methods rely on the same basic principle: to measure the time of propagation of travelling waves. Several approaches have been proposed[2], two of them are briefly discussed as an illustration.

1.1.4.1 Time Domain Reflectometry.

Time domain reflectometry (TDR) is well known and has found application in overhead lines as well as in underground cable fault location. Its basic principle of operation is as follows: a fast rise-time generator emits an impulse or step which is injected into the faulty line. The pulse propagates along the line and is reflected/transmitted at the points of discontinuity, i.e., a fault, joint, tee, etc. The initial injected pulse together with the reflected pulses are displayed on an oscilloscope for visual analysis. The distance between discontinuities is related to the time interval between the corresponding pulses by the velocity of propagation. Time domain reflectometry has been widely used and its development continued to the extent that all timing functions, measurements and direct readout of fault distance were digitally controlled [9]. As a result, the oscilloscope was reduced to a simple monitor, thereby removing a source of errors. A schematic diagram of a typical time domain reflectometer test system is shown in figure (1.3).

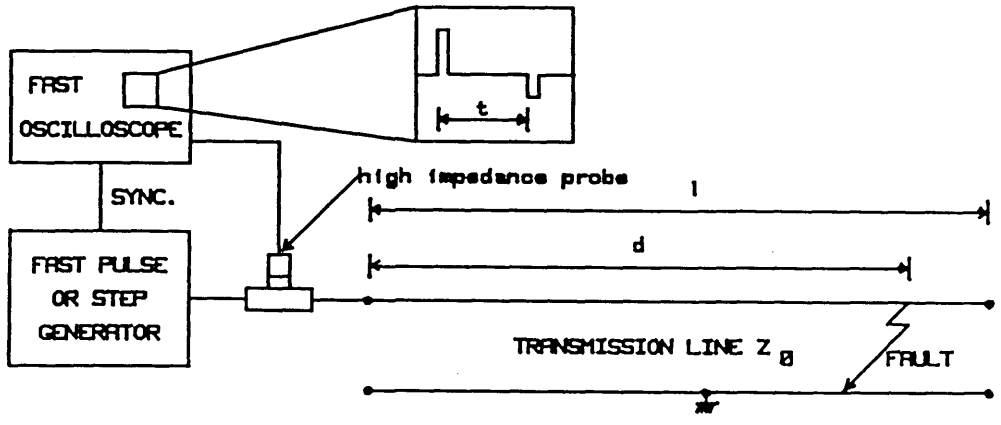


Figure 1.3. A typical time domain reflectometer.

The figure also shows a typical waveform for a fault to ground. The distance to the fault can be found by measuring the time interval, t, between the initial and reflected pulses, and from the knowledge of the velocity of propagation v; the distance is given by d = tv/2. Typical values for the velocity of propagation v are near to the velocity of light for transmission lines and to 2/3 of that for cables, i.e., 300 m/μs and 200 m/μs respectively.

Faults which can be located successfully using TDR are limited by the extent of the mismatch at the fault. The practical limit for the successful location is usually a few hundred ohms fault resistance.

TDR waveforms may be complex and difficult to interpret especially when the line network is complicated by the presence of joints or tees each giving a significant reflection or when the fault reflection coefficients are low. Additionally, dispersion degrades the rise time of pulses as they travel along the line giving problems with precise measurements.

1.1.4.2 Radio Timing Pulse.

Another travelling wave propagation time fault location method is based on the radio timing pulse technique. With reference to figure (1.4), the method works as follows: on fault inception two travelling waves are generated on either side of the line. These waves are detected when they reach the opposite ends of the line. The wave reaching the near end starts an electronic counter. The wave reaching the far end triggers a transmitter which sends a signal to the near end to stop the counter. From the accumulated count the fault distance can be deduced.

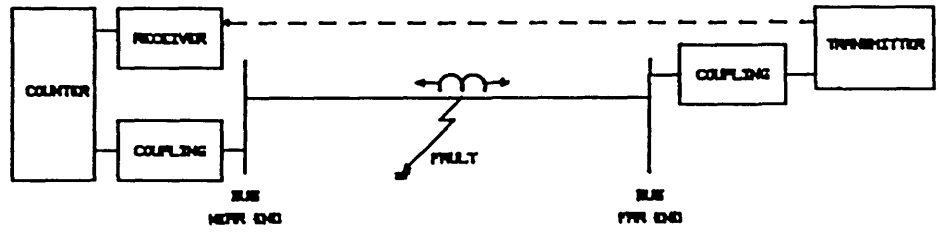


Figure 1.4 . Radio pulse fault location technique.

This type of fault locator transmits the signal over a microwave channel. The types of fault located are momentary, sustained and high breakdown and the fault location is carried out during the fault occurrence, that is, with the system energized.

These methods are considered to be accurate, reliable and fast, however they need a considerable amount of apparatus and in some cases a skilled operator is required to interpret them accurately.

1.1.5. FAULT LOCATION AS AN ESTIMATION PROBLEM.

Since the high frequency components contained in the fault waveforms are of

travelling wave nature, they should not present a problem to a travelling wave based method for fault location and no filtering would be required. Such a method was proposed initially by Kohlas [10] for single phase systems and later, it was extended by Ibe[11] to the three phase case. This method is of particular interest in the present work and is investigated further with the instrumentation described later in this thesis.

This method employs the distributed parameter line model of the line and the fault location is deduced by analysing voltage and current travelling waves recorded immediately after the fault occurrence. The theoretical basis of this method is examined in more detail since it will be used later. In the following section no proofs or derivations are included since they are given elsewhere [10],[11],[12]. The telegraph equations are taken as the model of the line as follows:

$$\frac{\partial}{\partial x} v(x,t) + L \frac{\partial}{\partial t} i(x,t) = - Ri \qquad (1)$$

$$C \frac{\partial}{\partial t} v(x,t) + \frac{\partial}{\partial x} i(x,t) = 0 \qquad (2)$$

where R, L and C are the resistance, inductance and capacitance per unit length of the line, and the conductance G is considered to be zero. The boundary conditions are given by recordings of voltage and current taken at one end of the line, i.e., x=0, immediately after the fault inception:

$$\begin{matrix} v(0,t) \\ i(0,t) \end{matrix} \quad ; \quad 0 \le t \le T \qquad (3)$$

where T is the time during which the recordings are taken. These measurements form the data of the problem. The fault sets another boundary condition at the point on the line, $x = x_f$, where it occurs:

$$v(x_f,t) = v_f \quad , \quad 0 \le t \le T \qquad (4)$$

the voltage v_f is expected to be minimum at the point of fault. Mathematically the problem is then stated as follows: determine the coordinate x_f, for which (4) holds,

using the data given by (3) and the line model stated by (1) and (2).

The method of characteristics was used to solve this problem. The basic principle is as follows: at every point in the x,t plane there are two directions in which the integration of partial differential equations reduces to integration involving total differentials only. That is, in these directions the equations are not complicated by the presence of partial derivatives in other directions. The curves along these two directions are called the "characteristics" and the method basically involves the determination of these unique directions along which solutions are then obtained[13]. A discrete version of the solutions, suitable for numerical computer calculation, was obtained. This numerical solution technique is illustrated in figure (1.5). The solutions are given in equations (5) and (6) :

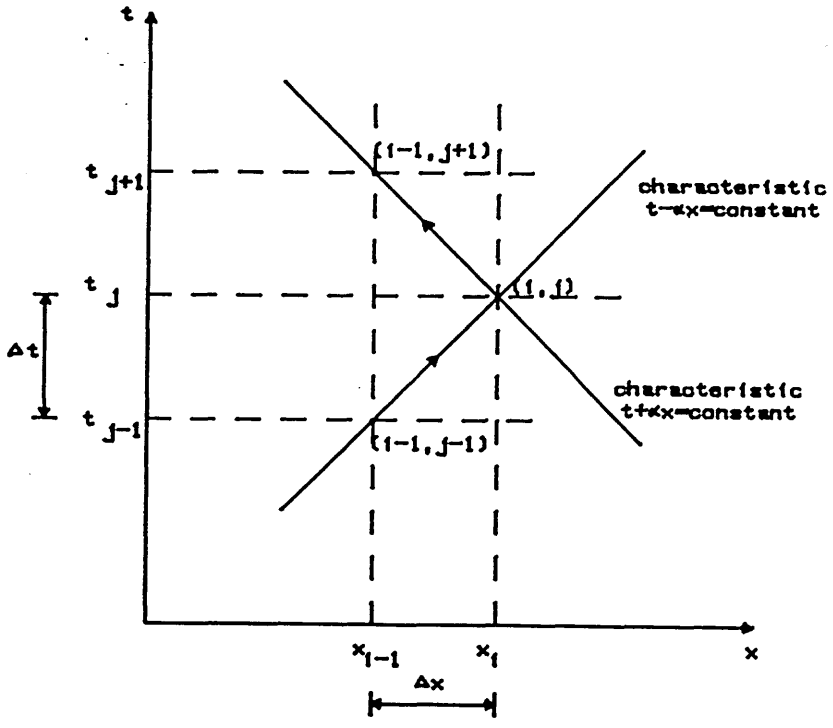


Figure 1.5. Illustration of the numerical solution technique.

$$i_{ij} = \frac{1}{2\alpha}\left(u_{i-1\,j+1} - u_{i-1\,j-1}\right) + \frac{2\alpha + \beta\Delta x}{4\alpha} i_{i-1\,j+1} + \frac{2\alpha - \beta\Delta x}{4\alpha} i_{i-1\,j-1} \qquad (5)$$

$$u_{ij} = \frac{1}{2}\left(u_{i-1\ j+1} + u_{i-1\ j-1} \right) + \frac{2\alpha + \beta\Delta x}{4} i_{i-1\ j+1} - \frac{2\alpha - \beta\Delta x}{4} i_{i-1\ j-1} + \frac{\beta\Delta x}{2} i_{ij} \qquad (6)$$

where: $u = -Cv$, $\alpha = \sqrt{[LC]}$, $\beta = RC$.

From equations (5) and (6) the values of i_{ij} and u_{ij} can be computed recursively from the initial data i_{oj} and u_{oj} at each discrete point x_i at intervals of Δx, as shown in figure (1.5). The relationship between the window length T, and the computed voltage and current along the transmission line is illustrated in figure (1.6). The v and i at sample point i,j are calculated using samples at all the intersection nodes within the pair of characteristics through i,j. So the pair of characteristics through i,j define the domain of dependence of the sample point i,j.

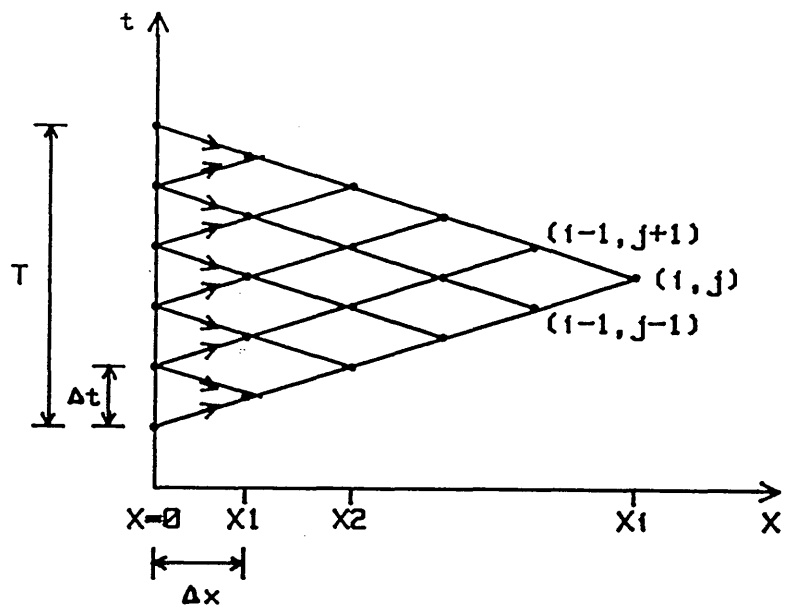


Figure 1.6 The concept of domain of dependence.

The discretization interval is given by:

$$\Delta x = \Delta t / \alpha$$

If N initial samples corresponding to a window length T at x=0 are used, N-2m samples are calculated at each succeding discrete point x on the line, where m is the number of discretization intervals from the initial point x=0.

At the point of fault x_f the voltage is expected to be a minimum, and can be found by minimizing the function:

$$F(x) = \frac{1}{T} \int_{\alpha x}^{T-\alpha x} u^2(x,t)\, dt$$

This function is computed from the voltage samples at each discrete point x_i (including x=0), and the point of fault is indicated by the minimum point in this function.

1.2 FAULT LOCATION METHODS FOR UNDERGROUND CABLE.

The problem of fault location is underground cables may be considered more demanding since greater accuracy is required than with overhead lines, if the location and repair of the fault is to be accomplished with a single excavation. Because of this the fault location problem in underground cable has been systematized and divided into four main stages[14] :

a) Diagnose.
b) Precondition.
c) Prelocate.
d) Pinpoint

The first three stages are similar to those followed in overhead line fault location, however, stage d) is not required for overhead lines since the exact location of the fault can often be accomplished by visual means.

1.2.1 FAULT CLASSIFICATION

Faults in cables can be shunt or series and can be represented by the circuit shown in figure (1.7) [15].

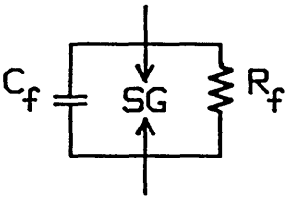


Figure 1.7. Equivalent circuit of a cable fault.

The figure shows a spark gap, S.G., for which the breakdown voltage, V_b, is determined by the separation of two conductors involved; a resistance, R_f, that depends on the degree of carbonization of the dielectric and a capacitance C_f which varies with the amount of moisture present. Cable faults are classified into the types shown in table 1.1. Since most modern methods of prelocation are based on travelling wave principles, the dividing line between low and high resistance faults is taken as a resistance equal to ten times the characteristic impedance (Z_0) of the cable under test.

Fault Type	Resistance	Spark gap
Series	-> ∞	Breakdown under impulse or dc.
Low series	< 10 Z_0	Breakdown under impulse if R_f is not too low.
High resistance	> 10 Z_0	Breakdown under impulse.
Flashing	-> ∞	Breakdown under impulse or dc.
Intermittent	∞	Breakdown under prolonged dc.

Table 1.1. Definition of cable fault types.

1.2.2. FOUR STAGES OF SYSTEMATIC CABLE FAULT LOCATION

1.2.2.1 Diagnosis.

The first indication of the possible existence of a fault is usually given by the automatic operation of the circuit protection. Occasionally protection may maloperate and it is therefore advisable to confirm whether or not a fault exists, and in the case it does exist, to measure the value of its resistance. This is usually done with a low voltage instrument such as an AVO.

1.2.2.2 Preconditioning.

Depending on the type of equipment available for fault prelocation it may be necessary to attempt to alter the fault characteristics. Typical preconditionings can change a high resistance fault to a low resistance one or a flashing fault into a stable one,this is done by passing current through the fault to carbonize the insulation. Special instruments exist for this purpose known as fault burners. A fault burner must be able to initiate breakdown of a high resistance fault but must then be able to supply increasing amounts of current as the fault resistance falls. Table 1.2 lists the various outputs available on a typical fault burner [16].

Maximum output voltage	Maximum output current
15.0 kV d.c	0.4 A
10.0 kV d.c.	0.8 A
5.0 kV d.c.	1.5 A
1.0 kV d.c.	7.5 A
240 V a.c.	15.0 A
100 V a.c.	60.0 A

Table 1.2 . Output level of a typical fault burner.

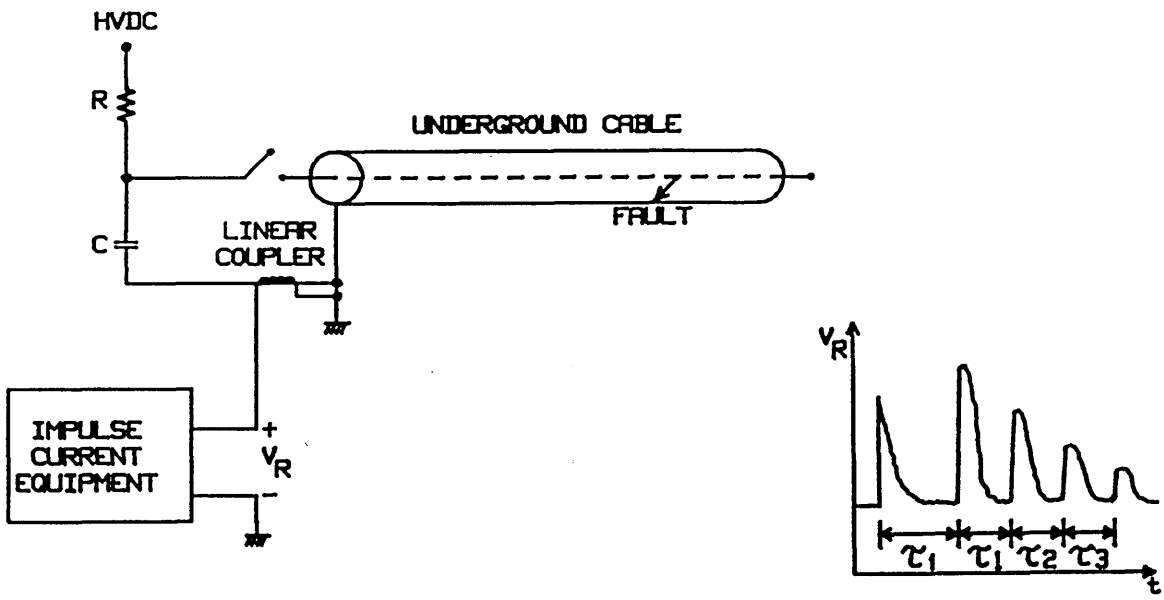
Care should be taken so as not to reduce the fault resistance to a value so low that the final accoustic pinpointing test cannot be performed (see pinpointing).

1.2.2.3 Prelocating.

The purpose of this stage is to establish an approximate area, where the pinpointing of the fault (stage d) is to be carried out.

The simplest of prelocation methods is time domain reflectometry or, as it is also known, pulse echo technique. Its principle of operation is the same as for overhead lines. The success of this method depends on the ability to recognize the reflection from the fault point amongst reflections from other discontinuities along the cable, e.g. joints, therefore, most cable faults should be preconditioned before they can be prelocated, that is, in case of a high resistance or flashing fault, they should be converted into a low and stable resistance one in order to have an appropriate reflection coefficient value at the fault point.

The most recent prelocating method was presented by Gale[15] and is known as the impulse current method. This method avoids the need to precondition the fault, i.e., fault burning. Figure (1.8 a) shows its principle of operation.



(a) Schematic arrangement for the impulse current method using a linear coupler.

(b) Output current waveform of impulse generator as seen using a linear coupler.

Figure 1.8. Impulse current method of cable fault location.

The high voltage surge generator is fired into the cable. Voltage and current waves

are initiated and travel along the cable. When the voltage reaches the fault the spark gap breaks down, this may take some time since breakdown never occurs instantaneously due to a phenomenon called "ionization delay". On breakdown two new travelling waves are generated, one on either side of the fault, which travel towards the cable terminals, where they are reflected again towards the fault. Both voltage and current waves are generated, but the current wave is considered simpler to detect with this method. This is done by using a linear coupler in the return path of the surge generator. A typical waveform so obtained is shown in figure (1.8b). The distance to the fault can be determined from the time interval, τ (μs), between successive reflections of the breakdown pulse using the following equation :

$$D = \frac{\tau v}{2} \quad (m)$$

D = Distance to the fault.
v = velocity of propagation (m/μs).
τ = time interval between successive reflections (μs).

The impulse current method can be used to prelocate all types of cable faults by appropriate interpretation of the transient waveforms but, a highly trained operator is required. Since the waveforms are of short duration it is essential to use some form of real-time recording. In impulse current equipment in present usage the waveforms are first stored in a digital memory which is then repetitively scanned, so that a reconstituted analogue waveform appears as a steady trace on the CRT. A cursor on the screen is also provided so that measurements of the time interval between any two points on the waveform can be taken.

1.2.2.4 Pinpointing.

Once an approximate distance to the fault has been obtained by one of the prelocation methods, the pinpointing stage is carried out in the near vecinity of the prelocated distance, in order to confirm the exact location of the fault.

The most used method for the exact location of the fault is to detect the acoustic signal produced by the fault when a surge generator is discharged on the cable. In some cases the acoustic signal can be detected above ground without any special equipment, but in general it is an advantage to use a ground microphone and amplifier to detect the

acoustic signal. The pinpointing stage is very important, and anything which might jeopardize the generation of the acoustic signal, for example prolonged fault burning, should be avoided. Once the fault resistance develops into a very low value, the spark gap (see figure 1.7) will effectively cease to exist, making it impossible for the acoustic signal to be generated, and several excavations may be necessary before the precise location of the fault can be identified.

1.3 FAULT LOCATORS.

This section describes some real fault locators, their principle of operation is based on methods already described or a slight variation of them.

Saut and Paithankar [17] described a digital on-line fault locator based on the reactance-ratio measurement principle. The inputs to the device are taken from existing current and voltage transformers and it locates transient as well as permanent short circuit faults. The reactance-ratio involved is that between the reactance of the line from the measuring point up to the point of fault over the reactance of the line, i.e., X_f/X_n. Because X_n is a known value, the ratio X_f/X_n determines the fault, and is given by:

$$\frac{Xf}{Xn} = \frac{\text{Sin}\,(\beta 2 - \beta 1)\ \text{Cos}\,(360 - \beta 2)}{\text{Sin}\,(\beta 1 - 180)}$$

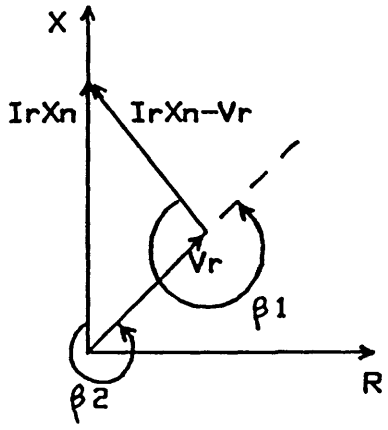
where β_1 and β_2 are shown in figure (1.9). The sinusoidal inputs fed to the fault locator are defined as :

$$S_1 = V_r$$

$$S_2 = I_r X_n - V_r$$

$$S_3 = I_r X_n$$

The circuitry is reproduced in figure (1.10). The fault locator is initiated on receiving the trip pulse from the relay; when the positive zero crossing of signals S_1, S_2, S_3 is detected, a train of pulses P_1, P_2 and P_3 respectively is started. P_1 initiates both counters. P_2 stops counter 1, recording $\beta 1$; and P_3 stops counter 2 which records $\beta 2$.



V_r, I_r = Voltage and current at the relay location.

X_n = Reactance of the line.

Figure 1.9. Phasor diagram for fault condition.

As with standard impedance measurement based fault locators, low pass filtering is needed to avoid the undesirable high frequency components, besides, a minimum time of

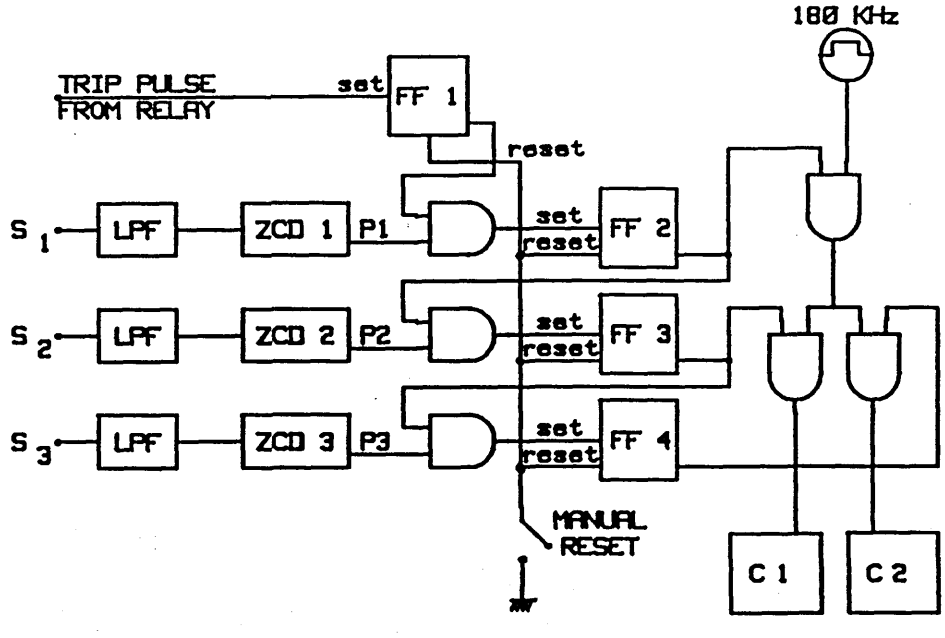


Figure 1.10. On-line digital reactance ratio fault locator.

two cycles of the power frequency of operation is required for correct operation. An accuracy of $\pm$ 2% in fault location was reported. This accuracy is not very good and implies an error of $\pm$ 500 meters for a 25 km. line length.

Gallagher and Dickerson[18] presented a transmission type cable fault locator that is suitable for a 3 phase system with a flashing fault in one of the phases. It measures the distance from the test end of the cable to the fault as a fraction of the total cable length. The system consists of a high voltage power supply, shorting relay switch, spark-gap and two voltage sensors with clamping diode and latch circuits. A reproduction of the system connection is given in figure (1.11).

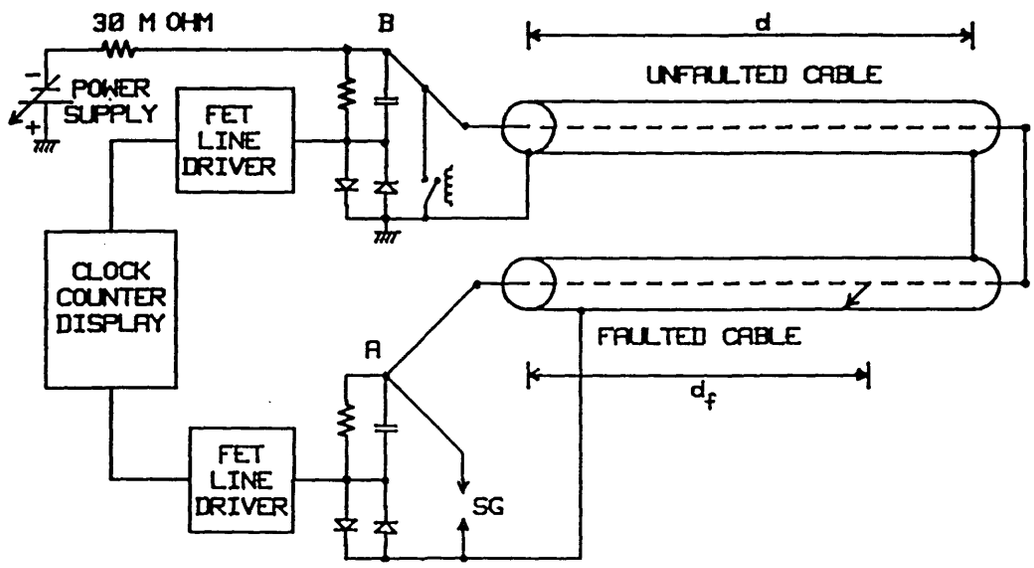


Figure 1.11. Transmission type cable fault locator.

The faulted phase is connected to one of the unfaulted phases at the far end of the cable. The fault location system is connected to the cables at the near end.

In order to locate the fault two measurements are carried out. First the sparkgap is set to arc at a voltage below the breakdown level for the faulted phase. The wavefront generated by the arcing sparkgap arrives at voltage sensor A instantaneously, and starts the counter. This same wavefront propagates along the faulted cable towards the far terminal, across the connection to the unfaulted phase conductor and back the voltage sensor B at the near terminal. The arrival of the wavefront at voltage sensor B stops the

counter. The accumulated count, t_1, represents two times the total length of the cable d. The second measurement is similar, but this time the fault, not the spark-gap, is forced to arc, and t_2 is obtained.The distance to the fault is found as :

$$\frac{df}{d} = 1 - \frac{t2}{t1}$$

Even though faults were located within the expected accuracy ($\pm$10m), during laboratory tests, it was recognized that equipment modifications were necessary when dealing with long cables (8.8 km. or greater). Such modification included an increase in signal sensitivity and noise immunity in the voltage sensors as well as the use of optical links to prevent ground loops.

Masahide et.al.[19] proposed a fault locator based on the calculation of the ratio of line voltage drop obtained from the local terminal voltage versus voltage drop per unit line length obtained from the local terminal current and line impedance per unit length. The distance to the fault point , x , is calculated by the following equation[7]:

$$x = \frac{Im (Vs * Is'')}{Im (ZIs * Is'')}$$

where:
- x = distance to the fault point.
- Vs = Local terminal voltage.
- Is = Local terminal current.
- Is" = Fault component current (difference between currents before and after fault inception.Complex conjugate)
- Z = Transmission line impedance per unit length.
- Im = Imaginary component.

Figure (1.12) shows the relation between V_L(line voltage drop between the measuring point and the fault), V_F (voltage at the point of fault), I_F (fault current), R_F (fault resistance), I_L(load current), V_S (local terminal voltage) and I_S (local terminal current).

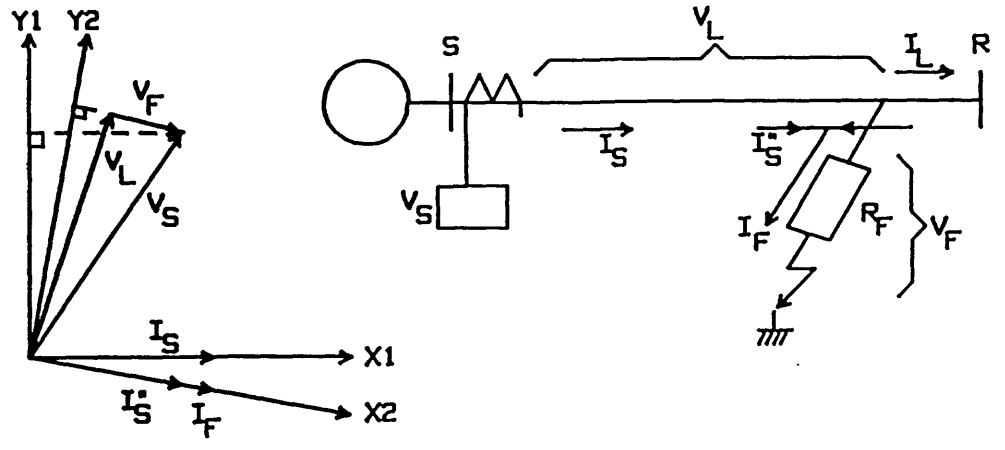


Figure 1.12. Fault location vector diagram.

Because conventional distance relays used in system protection respond to the reactive component of the impedance determined from the voltage and current, V_S and I_S, they measure the V_S component on the Y_1 axis perpendicular to I_S. Therefore, a distance measuring error will be caused by the phase difference between fault point voltage V_F and I_S.

They proposed to use the V_S component on the Y_2 axis perpendicular to I_F (fault current), instead of the component on the Y_1, axis. Considering that the fault is purely resistive, I_F and V_F must be in phase. Therefore, V_F has no effect on the V_S component on the Y_2 axis. Their fault locator calculates the distance using the V_S component on the Y_2 axis, instead of the Y_1 axis, to eliminate the V_F effect, which is the fault resistance R_F effect.

The Y_2 axis is determined by the I_F phase angle. I_F is not available at the local terminal of the fault locator. I_S" is used instead of I_F in their equation, considering that these currents are in phase. They also assume that the line is lossless and the source impedances at both ends of the line are purely inductive.

A block diagram of the fault locator is shown in figure (1.13).

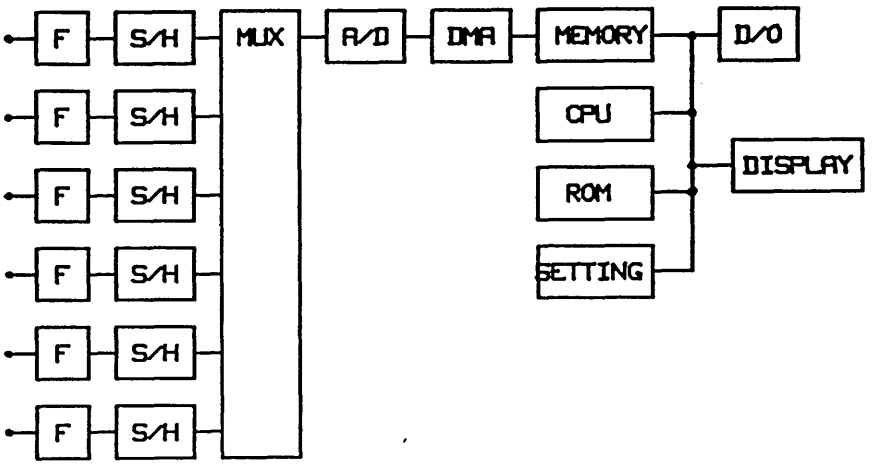


Figure 1.13. Fault resistance elimination fault locator. F= low pass filter, S/H= sample-hold, Mux= multiplexer, A/D= analogue to digital converter, DMA= direct memory access, CPU= central processing unit, ROM= read only memory, D/O= digital output.

Since the calculations are based on the line frequency voltage and current the fault locator includes low pass filters for the high frequency components; the measuring error is within $\pm$ 1 km. or 1% the line length, whichever is greater.

1.4 SUMMARY.

A brief survey of fault location methods and techniques has been given. Basic principles of operation have been discussed, and main advantages and drawbacks reviewed. Some real fault locators have been described to gain an idea of the present state of the art. The present research work was carried out against this background.

1.5 OBJECTIVES.

Most of the fault location methods and techniques are based on power frequency parameter evaluation or travelling wave principles. The high frequency components in the voltage and current fault waveforms give undesirable effects in methods based on power frequency parameter evaluation and, as a consequence, filtering of fault waveforms, to remove these high frequency components, is essential for accurate fault location. On the other hand, fault location methods which derive from travelling wave principles can cope with the high frequency components since they basically depend on travelling wave phenomena. Its main drawback is the need for skilled interpretation of recorded waveforms. The method described in section 1.1.5 is of particular interest since it avoids this need.

The objective of this work is to develop a High Speed Data Acquisition and Analysis system for the investigation of fault location in electric power lines and cables. The system is intended to be used to measure and acquire data from real lines and cables for analysis. In particular, it will be used to investigate the practical effectiveness of the fault location method described in section 1.1.5, with the idea of automating the fault location operation.

CHAPTER 2

FAULT LOCATOR APPARATUS

2.0 INTRODUCTION.

In this chapter a detailed specification for the fault locator apparatus based on the requirements imposed by the fault location method described in section 1.1.5 of the previous chapter, is established. A full description of its main features and details of design, construction and testing is given.

2.1 FAULT LOCATOR APPARATUS DESCRIPTION.

As stated in chapter 1 most of the methods for fault location currently in use are based either on power frequency parameter evaluation or travelling wave principles. They require as input data recordings of fault voltage and current waveforms which are, subsequently, processed by a suitable algorithm or analized by visual inspection.

The recording of the initial voltage and current waveforms is performed by some kind of real time recording device. The recorded fault voltage and current waveforms may be those produced within the first few milliseconds after the fault occurrence in an energized line, or those produced by the injection of an interrogating signal into the faulty line or cable, once it is unenergized.

The particular method described in section 1.1.5, can cope with the high frequency content of fault waveforms, as opposed to those based on the power frequency parameter evaluation. It treats the fault location as an estimation problem, using the telegraph

equations as the line model. From the input data, instantaneous voltage and current profiles are generated for the rest of the line. The voltage and current estimation is based on the solution of the telegraph equations obtained by the method of characteristics. A criteria function involving the square of the estimated voltage profile along the line is applied for determination of the fault position. The method is automatic, that is, it does not need skillful interpretation.

The above considerations suggest a fault locator apparatus composed basically of two main components, that is, a recording or data acquisition unit to capture voltage and current waveforms and a processing unit which would implement the proposed fault location method in the form of an algorithm. If the fault locator apparatus is intended to be used for energized or unenergized lines or cables, it should provide facilities to capture useful data, i.e., data related to the fault, and it should provide an adequate sampling frequency in order to cope with the high frequency components in fault waveforms. These and other features of the fault locator apparatus developed are further discussed in the following sections.

A block diagram of the fault locator apparatus showing its basic modules, the relation between them, and the "signal flow" is shown in figure (2.1). The intended typical sequence of operation would be as follows: assuming that the fault location is to be carried out on an unenergized line, the pulse generator injects an interrogating signal into the line; the signal conditioning module sets the amplitude of the input voltage and current waveforms to adequate levels for the analogue to digital conversion module, besides, setting the input impedance of the instrument so as not to load the line. The voltage and current waveforms are converted into digital form by the analogue to digital converter module which contains two independent analogue to digital converters. The digital codes generated by each converter are stored in corresponding memory banks within the memory module. Once the digitized fault voltage and current waveforms have been stored in memory, they can either be reconstructed into their analogue form for visual display and analysis on a general purpose oscilloscope or can be transferred to the processing unit, where the fault location algorithm is applied to them in order to locate the fault. The distance to the fault would be indicated on a VDU.

From the above description it can be recognized that the fault locator apparatus has several "modes" or "states" in its operation.

a) It can be converting the voltage and current waveforms into its digital representation and storing them into memory. This mode will be referred to as "converting and storing" mode.

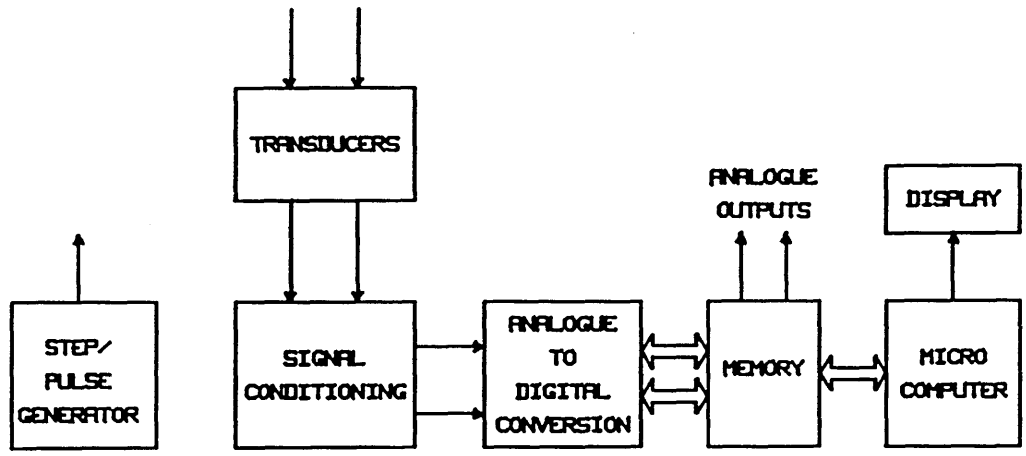


Figure 2.1. Block diagram of the fault locator apparatus.

b) It can be transferring the digitized voltage and current to the processing unit for its subsequent processing. This mode will be referred to as "sending data to microcomputer and processing".

c) It can be outputting the reconstructed analogue voltage and current waveforms to be seen in an oscilloscope. This mode is referred to as "outputting data to oscilloscope".

d) It can be in a "stand-by" state which is entered immediately after powering it up.

The mode in which the fault locator is desired to operate is selected through control switches and knobs located at the front panel.

In the case of an energized line the pulse generator would not be required, but the ability to detect a fault and record the voltage and current waveforms generated on its occurrence is a key factor. It will be seen later how this is done by taking advantage of the trigger facility of the fault locator apparatus.

2.2 STEP/PULSE GENERATOR.

The objective of this module is to provide the interrogating signal to be injected to the faulty transmission line. The following material discusses the desirable features of suitable test waveforms on the assumption that the behavior of the transmission line can be modelled by a linear constant parameter network. The validity of this assumption is tested later in this thesis.

2.2.1 WAVEFORM.

Of all possible test signals, sine waves have the unique property that their shape is unaffected by linear circuits or systems. In response to a sinusoidal excitation all voltages and currents in a linear system will be sinusoids of the same frequency, altered only in amplitude and phase. Additionally the response of a linear system to any input signal, is completely defined by the knowledge of the effect of the system on the amplitude and phase of a sinusoidal signal at all frequencies. Therefore, an array of steady state measurements or a swept frequency measurement can be made to completely and accurately characterize a linear system.

Although, these measurements may tell all about the system, they may tell it in an implicit way. For example, what is often important about a linear system, and particularly for our case, a transmission line, is its response to transient signals. While the transient response may be inferred from the steady-state measurements, or may be computed by using Fourier transform techniques, a much more direct approach is to apply a kind of standardised transient and observe the response. The "standard transients" most often used are step functions, square waves, and impulses.

The spectrum of a unit impulse :

$$x(t) = \delta(t)$$

is

$$X(\omega) = \int_{-\infty}^{+\infty} \delta(t)\, e^{-j\omega t}\, dt = 1$$

that is, the unit impulse has a Fourier transform representation consisting of equal contributions at all frequencies. The spectrum of a unit step function:

$$u(t) = 0 \ , \ t < 0$$
$$1 \ , \ t \geq 0$$

is

$$U(\omega) = \frac{1}{j\omega}$$

where 1 is the amplitude of the step. In real cases the impulse will always have finite rise time, duration and fall time, and the step a finite rise time, and both of the above expressions hold up to frequencies of the order of the reciprocal of the impulse duration or step function rise time. If the impulse duration or step rise time is short enough, then a single impulse or step will contain all frequencies that would be used in a steady-state measurement, and in known amounts. In a sense, the impulse or step performs a complete characterization by applying the whole spectrum to the system in the form of a single signal.

A square wave does not have the continuous smooth spectrum of the isolated event, but because it is periodic, contains only frequencies that are harmonics of the fundamental frequency. Such a test signal samples the response of the system at these frequencies only. Any feature lying completely between zero frequency and the fundamental or between any two harmonics will not be observed.

The step function, because of its greater energy at the low end of the spectrum, tends to display phenomena associated with low frequencies better than do impulses. This is specially true for wideband systems where the high-end cut-off frequency may be several thousand times the low-end cut-off frequency. The duration of a test impulse should be short compared with the period of the highest frequencies passed by the system. The wider the frequency response of the system, the smaller the choice of practical impulses that are suitable test signals. As the width of an impulse is shortened, its amplitude must be increased to hold the low-frequency energy content constant, but the ideal zero-rise time step can be approximated as closely as desired depending on the devices used to produce it. For these reasons a step function is preferred to an impulse or square wave, as test signal.

There exists an additional reason to prefer a step function as test function. It is derived from standard short circuit analysis in electric power systems, where it is considered that a short circuit represents a structural network change equivalent to that caused by the addition of an impedance at the place of fault. The changes in voltages and

currents that will result from this structural change are analyzed by means of Thevenin's theorem which states:

> "The changes that take place in the network voltages and currents due to the addition of an impedance between two network nodes are identical with those voltages and currents that would be caused by an emf placed in series with the impedance and having a magnitude and polarity equal to the prefault voltage that existed between the nodes in question and all other active sources being zeroed" .

In order to show the basic concept, a two bus system is depicted in figure (2.2):

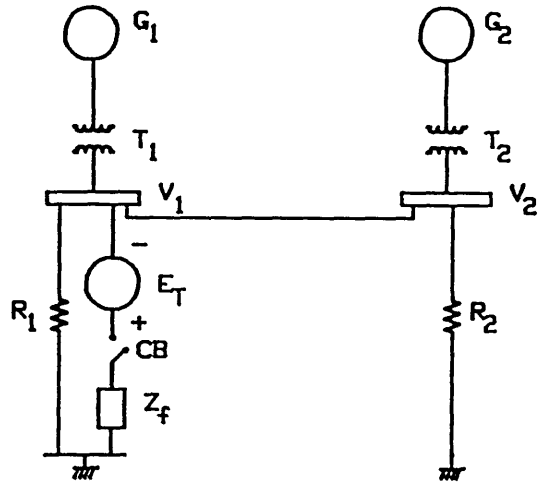


Figure 2.2. Equivalent fault circuit

It is assumed that a short circuit occurs on bus 1, which is structurally equivalent with closing the "circuit-breaker" CB in the diagram. Z_f is the fault impedance and E_T is the Thevenin's voltage which is equal to V_1 in magnitude and opposite in polarity. On fault occurrence the voltage at bus 1 will be zero if the fault impedance is zero, which corresponds to a solid fault. This mechanism is equivalent to injecting a voltage pulse (negative pulse for the case described) to the system in the point of the fault .

2.2.2 AMPLITUDE.

As a wave travels along a transmission line it suffers three different changes :

a) The wave decreases in amplitude or is attenuated.

b) The wave changes shape, that is, becomes more elongated, its irregularities are smoothed out and the rise time is increased.

c) The voltage and current waves cease to be similar. The latter two changes occur together and cause distortion. It is theoretically possible to have attenuation without distortion as in Heaviside's distortionless line, where :

$$R\,C = L\,G \quad ; \quad \begin{array}{l} R = \text{Resistance}, \\ L = \text{Inductance}, \\ C = \text{Capacitance}, \\ G = \text{Conductance}, \\ \text{all in per unit length.} \end{array}$$

In addition to the attenuation due to the line resistance, faults rarely present zero impedance, especially in underground cables. When this situation arises it is necessary to force the fault to arc, so as to have the voltage step referred to above. This breakdown voltage can vary widely, but generally it will be greater than 1 kV.

2.2.3 OUTPUT IMPEDANCE.

When a step injected to a transmission line reaches a transition point, at which there is an abrupt change of circuit constants, as an open or short circuited terminal or a junction with another line, a part of the wave is reflected back and a part may be refracted or transmitted. Assuming that the discontinuity is a solid fault to earth, the reflected wave will be of the same amplitude, but opposite sign to the incident wave for the voltage, and same magnitude and sign for the current. There will not be refracted waves. The resultant voltage at this point is the sum of the incident and reflected waves,

which is equal to zero, and the resultant current is double the value of the incident wave. When the reflected waves, travelling back now, reach the source, the same phenomena occur (assuming an ideal voltage source, $Z_{source}=0$), i.e., new reflected voltage and current waves are generated. The resultant voltage at this point will be the sum of the initial voltage plus the reflected wave travelling back from the fault (which is now considered as incident wave) plus the newly generated reflected wave. The latter two

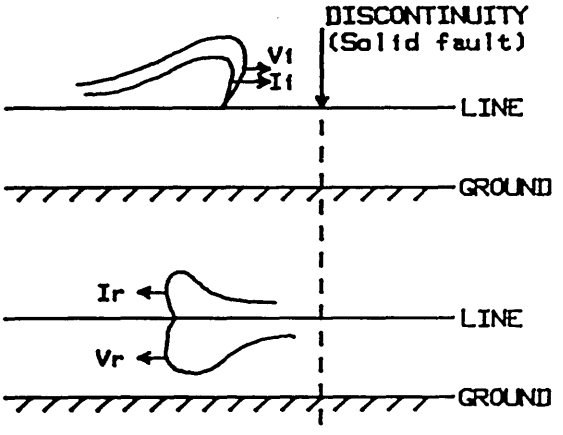


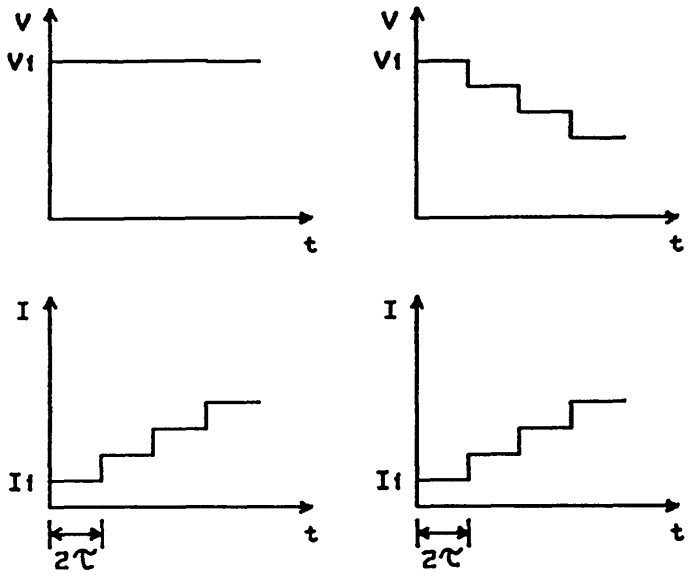
Figure 2.3. Reflection/refraction of travelling waves.

waves, being equal in magnitude but opposite in polarity cancel each other and the final voltage is equal to the initial one, i.e., there is no apparent evidence in the voltage waveform of the reflections being generated.

The current will show a "staircase" waveform clearly showing the reflections. This is shown in figure (2.4a).

If the output impedance of the source has a value different from zero the reflection will also be apparent in the voltage waveform. The 'best' output impedance for the purpose of locating faults, depends on how many apparent reflections are to be contained in the time interval of interest and on the characteristic impedance of the line.

It will be seen that by experimentation, the 'best' value was found to be equal to 10% of the characteristic impedance of the particular transmission line under test. This value was chosen to reveal voltage reflections being careful to avoid affecting the current significantly. The resultant voltage waveform is shown in figure (2.4b).



(a) *(b)*

Figure 2.4. Effect of source output impedance. Vi, Ii = Voltage and current measured at the input of the line or cable. a) Zsource= 0, b) Zsource>0.

2.3 ANALOGUE TO DIGITAL CONVERSION MODULE.

The main function of this module is to provide an accurate digital representation of the voltage and current analogue waveforms, and since it contains the time base, it also generates all the necessary timing signals for the correct operation of the fault locator apparatus in all its modes of operation.

2.3.1. ADC MODULE DESIGN CONSIDERATIONS.

Two main characteristics of an A/D converter determine its applicability to the

recording of transient signals : sampling rate and word length.

In order to specify the requirements for the sampling rate, in the general case, one has to attend to the bandwidth of the particular system under test and/or to the frequency content of the test signal.

For the particular case of fault location three considerations will be made :

a) The frequency content of the injected or fault generated step.

b) The frequency content of fault induced transients and,

c) the relation that exists between sampling frequency and accuracy in distance in the fault location.

The input signal, as already mentioned, consists of a step which can be the one injected by the step generator or that produced by the fault itself. The power spectrum of an ideal step is well known and is shown in figure (2.5).

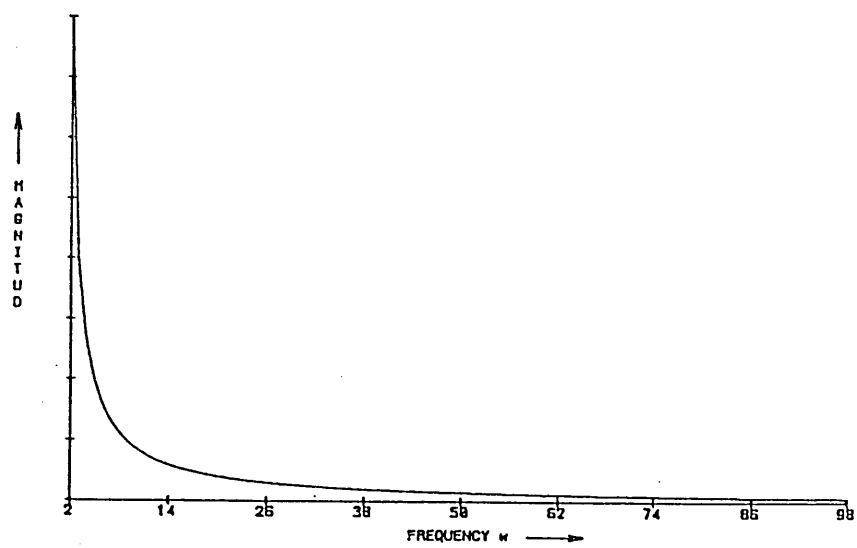


Figure 2.5 Power spectrum of an ideal step.

Consider now the situation of a single phase line with a fault on it, as shown in figure (2.6). The fault is considered to have zero resistance to ground. The impedance of the pulse generator is purely resistive and equal to one tenth the characteristic impedance of the line. If it is assumed that a pulse is applied to point A of the line, the measured voltage and current at point A would have the waveforms shown in figure (2.7).

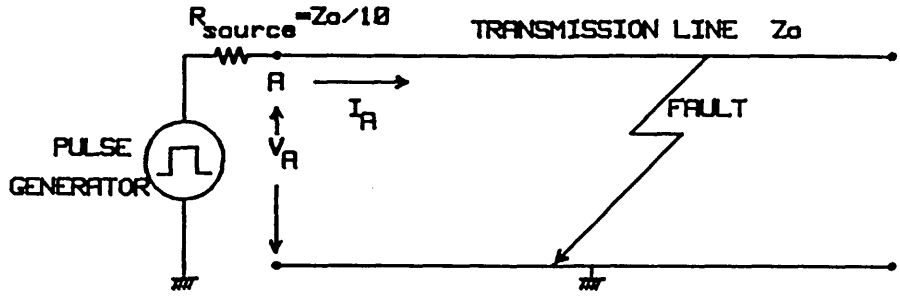


Figure 2.6 Single phase line with a solid fault.

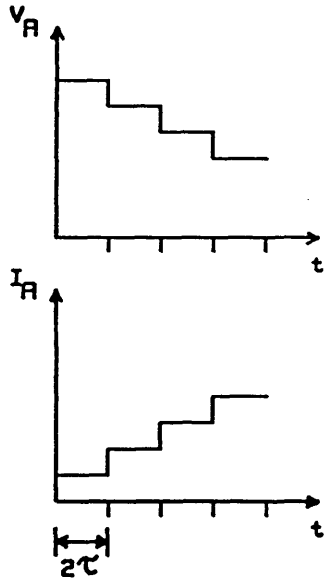


Figure 2.7 Voltage and current waveshape at point A.

The power spectrum of these waveforms will show a dominant frequency component given by [20]

$\frac{1}{2\tau}$; τ = wave transit time from measuring point to point of fault

the time τ is dependent on the fault position along the line, the longer the distance from the measuring point to the fault, the bigger this time will be and the dominant frequency will be lower, on the other hand, the nearer the fault point to the measuring end the higher this frequency will be. Assuming a distance to the fault equal to 100 meters and a wave propagation velocity near to that of light, the dominant frequency would be expected to be around 1.5 MHz.

The relation that exits between the sampling frequency and the accuracy in distance in the fault location is as follows: as was stated in chapter 1, the numerical solution of the line model equations is discretized. The discretization interval, Δx, being determined by Δt and α:

$$\Delta x = \Delta t/\alpha$$

where $1/\alpha$ is the wave propagation velocity. Since α is calculated from L and C of the line (which are considered constant in the calculations), any variation in Δx depends only on Δt. The fault distance obtained with the algorithm is a multiple of Δx, the best result being the nearest multiple of Δx to the actual distance. It is clear then that the higher sampling rate the better the accuracy achievable. Additionally, the limit given by :

$$T \geq Z \cdot 2\alpha \qquad ; \; T = \text{length of data window.}$$

Z = total length of line.

$1/\alpha$ = wave propagation velocity.

sets a minimum data window length which form the initial data of the problem. For a given distance, T has a fixed value. Increasing the sampling frequency means increasing the number of data recorded during T. This directly affects the data storage capacity of the recording device and the processing time of these data in the microcomputer.

Bearing these considerations in mind, a maximum sampling frequency equal to 20 MHz is adequate, since an accuracy of $\pm$ 10 meters would be expected for an overhead transmission line with a propagation velocity near to that of light. The magnitude of the frequency content of the injected or fault generated step at 10 MHz (Nyquist frequency)

has already decayed by nearly 80 dB from its low frequency value, and the frequency content of the fault induced transients is well below 10 MHz even considering an extremely short fault distance of 100 meters as in the example given above.

2.3.2 FAST ANALOGUE TO DIGITAL CONVERTER TYPES.

Generally what is meant by a flash converter is a converter with a conversion rate in excess of 10 MHz. A fully parallel converter is sometimes referred to as full flash.

The following techniques are generally used in faster than 10 MHz converters :

1.- Full flash
2.- Two step flash
    a) with DAC
    b) reference switching

A full flash ADC has 2^n voltage comparators for n bit conversion followed by an encoder and a latch to provide binary outputs. The basic configuration is shown in figure (2.8).

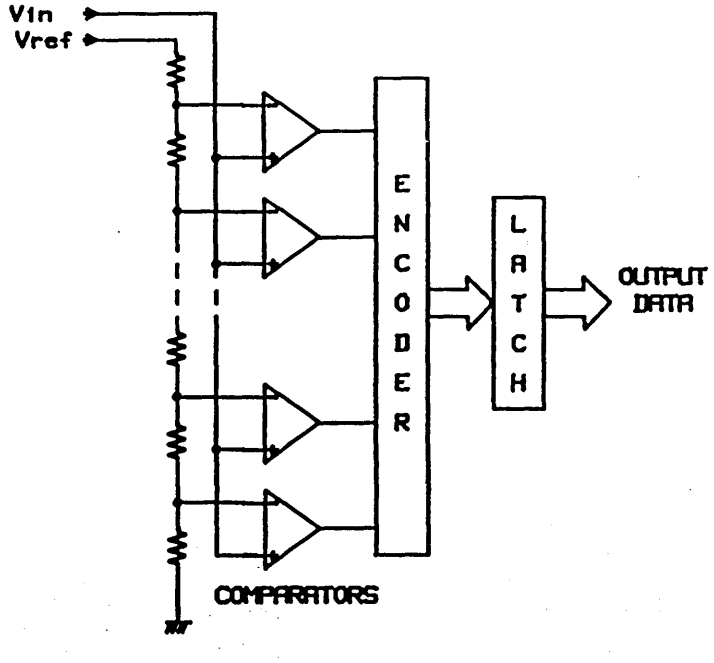


Figure 2.8. Full flash analogue to digital converter.

Another type is a two step converter in which the analogue voltage is stored in a sample-hold circuit, as shown in figure (2.9). The input is first converted by a 4 bit flash converter whose binary outputs are fed to a high speed 4 bit digital to analogue converter with 8 bit accuracy. The DAC output is subtracted from the sample and hold signal and fed to another 4 bit flash converter to provide the least significant bits (LSB). This device requires only a fraction of the components of a full flash. It has a much slower speed due to the settling time of the DAC and the subtractor.

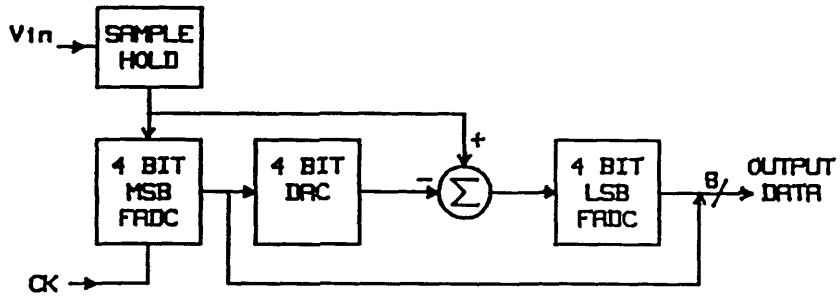


Figure 2.9. Two step analogue to digital converter.

This deficiency in the conventional two step ADC is overcome by a recent development[21] of a two step fast analogue to digital converter (FADC) with reference switching.

The principle of operation is shown in fig. (2.10a,b) for a 4 bit device. A resistor chain supplies the reference voltages to the comparators. Initially, the most significant bit (MSB) comparators look at the analogue signal V_{in}. Say V_{in} is between V_n and V_{n+1} reference levels of the MSB comparators. All the MSB comparators to V_n are latched, then, through a matrix of switches, V_n and V_{n+1} levels are applied as full scale references to LSB comparators. After an appropriate settling time the data is latched in LSB latches. If the input signal changes by more than $\pm$ 1/2 LSB between the MSB and LSB conversions it becomes necessary to use a sample hold.

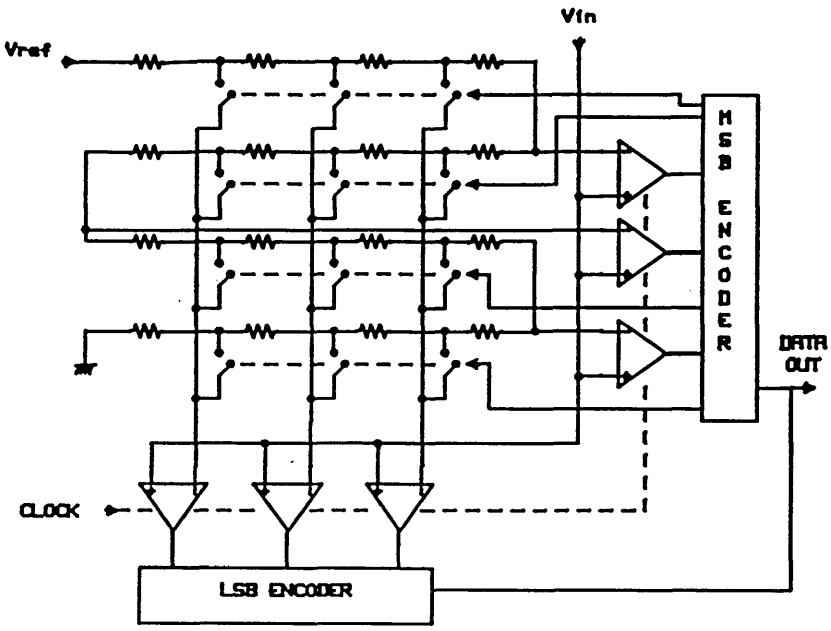


Figure 2.10 a.Two step FADC with reference switching.

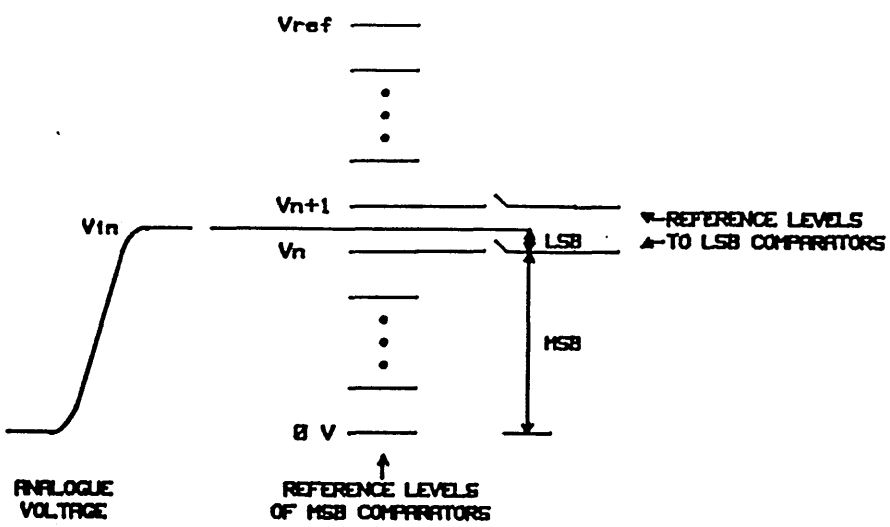


Figure 2.10b. Reference levels applied to MSB and LSB comparators.

2.3.3 SELECTION OF A/D CONVERTER.

Commercially available fast A/D converters were reviewed. Table 2.1 shows some of the more representative devices. The criteria for inclusion was number of bits, sampling frequency, availability and price.

From a review of the table the following combinations considering number of bits and sampling frequency can be found: 10 bits-20 MHz, 9 bits-18 MHz, 8 bits-20 MHz. The inherent analogue to digital conversion errors amount to 0.1%, 0.2% and 0.4% respectively. The Sony CX20052 converter was chosen because it offered better availability and price. It is an eight bit converter with an inherent A/D conversion error of 0.4% and a minimum sampling frequency equal to 20 MHz. The particular version used, BX-1200, included a sample-hold circuit, buffer driver and timing circuitry. The digital output is provided in ECL logic as 8 parallel bits from open emitters.

Manufacturer	Part No.	Process	Type	No. Bits	Samp.F [MHz.]	Logic In/Out
Fujitsu	MB40548	Bipolar	Flash	8	20 (min)	ECL
Hitachi	Flash 8AD	Bipolar	Flash	8	30	ECL
Panasonic	AN6857	Bipolar	Flash	8	35	ECL
Panasonic	AN6859	Bipolar	Flash	10	20	ECL
RCA	CA3308	CMOS	Flash	8	15 (typ)	CMOS
Sony	CX20052	Bipolar	2 Step	8	20 (min)	ECL
Toshiba	T1595	Bipolar	Flash	8	20 (min)	ECL
TRW	TDC1007	Bipolar	Flash	8	20 (min)	TTL
TRW	TDC1019	Bipolar	Flash	9	15 (min)	ECL
TRW	TDC1019-1	Bipolar	Flash	9	18 (min)	ECL
TRW	TDC1025	Bipolar	Flash	8	50 (min)	ECL
TRW	TDC1048	Bipolar	Flash	8	20 (min)	TTL

Table 2.1. Fast analogue to digital converter characteristics.

Other facilities that would add flexibility to the fault locator apparatus are the following :

a) Variable sampling frequency: The top sampling frequency will provide the best

accuracy in distance possible, while lower sampling frequencies will be found to be useful in preliminary tests as will be seen later.

b) Variable digital trigger level: Conventional analogue settings of the potentiometer type tend to be difficult to precisely adjust and change with temperature and aging. A digital one, by its own nature, is more precise and stable.

c) Posttrigger: Transient recording devices are usually started when the input signal reaches some defined value known as trigger level. A pretrigger facility enables a certain amount of the incoming signal before the trigger to be captured and stored. Posttrigger refers to the amount of memory used to store the incoming signal after the trigger. Pretrigger and posttrigger memory amounts are related by :

pretrigger memory amount	+	posttrigger memory amount	=	total storage capacity.

2.3.4. SPECIFICATION OF THE ADC MODULE.

The above discussion leads into the specification of the conversion module which is given below :

- Two independent analogue to digital converters , which will exhibit a sampling frequency up to 20 MHz. each one .
- The value of the sampling frequency is always the same for both converters and can be any of the following :

a) 20 MHz
b) 10 MHz
c) 5 MHz
d) 2.5 MHz
e) 1.25 MHz

- The trigger level can be chosen from 0% to 90% of the full scale of the converter, in 10% steps.

- It is possible to choose which of the two converters is the one to trigger.

- It is possible to choose the degree of posttrigger from 0% to 90% of the total memory amount in 10% steps.

2.3.5 ADC MODULE CIRCUIT DESCRIPTION.

Figure (2.11) shows a block diagram of the ADC module. The circuit diagram is included in appendix A and a photograph of the real module is shown in figure (2.31).

The functions performed by this module are the following :

- Receives the analogue signals and converts them into their corresponding digital form.

-Generates the necessary signals to perform the conversion (SC), latch the output data in the output latches (LE) and store the data in memory (WE/).(See block diagram).

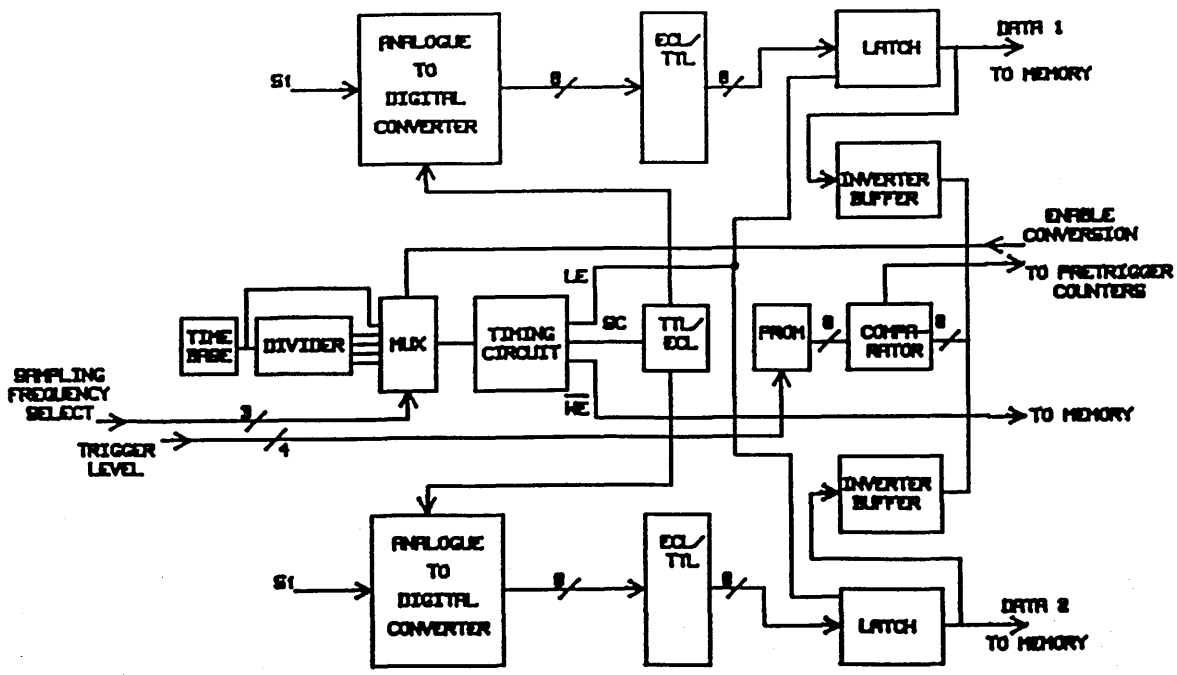


Figure 2.11. Block Diagram of the analogue to digital converter module.

- Detects if the trigger level has been reached , in which case sends a signal (trigger level reached) to initiate the posttrigger counters.

- Receives the signal to select the channel which is to trigger and enables the appropriate buffer.

- Receives the signals defining the trigger level and inputs to the comparator the appropriate word.

- Receives the signal to set the sampling frequency and selects the appropriate channel of the multiplexer.

- Starts/stops conversion upon receipt of the signal enable/disable conversion.

- Generates a signal to reset the trigger level reached flip flop when non valid data are present at the input of the comparator.

The basic operation of this module when the fault locator is operating under the "converting and storing" mode is as follows: with reference to figure (2.12) the time base generates a stable TTL signal at 40 MHz, which is passed through the divider (four cascaded flip-flops connected as toggles) to obtain 4 signals whose frequencies are a submultiple of 40 MHz. These four signals and the time base are applied to the multiplexer. The signal passed by the multiplexer is of a frequency double that corresponding to the desired sampling frequency . This signal enters the timing circuitry where the following signals are generated :

Start of conversion (SC).- Used to drive the P latch enable (PLE) of the comparator and, after passing through a TTL/ECL converter is used as the clock signal for the A/D converters. The inverted signal of SC is used to latch the valid output data from the converter. SC is also used as clock for the posttrigger counters.

Write enable (WE/).- Clock signal to drive the memory.

The digital variable trigger level is implemented as follows (see figure 2.13): the A/D converter receives the analogue signal and outputs the corresponding digital code, this code is first converted from ECL to TTL, latched, and sent to memory. The code given by the A/D is complementary binary, the buffers between the latches and the input to the comparator are inverters so the input to the comparator is natural binary. Only one of this buffers is enabled depending on the channel to trigger selection chosen through the front panel switch. The word which sets the desired trigger level is provided by a PROM which in turn is driven from a thumb wheel located at the front panel. During a conversion cycle each word given by the A/D converter is compared against the desired trigger word, when the former is bigger than the latter a signal is generated, trigger level

reached, to start the posttrigger counters. The signal SC is used to enable the comparator in such way that a comparison is performed only when valid and stable data are present at the output of the latches.

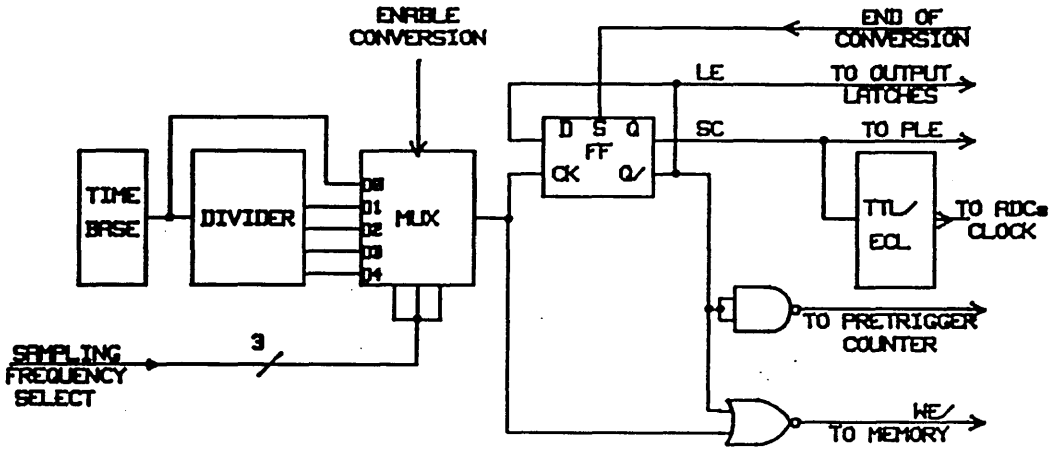


Figure 2.12 Timing and control signal generation in analogue to digital converter module.

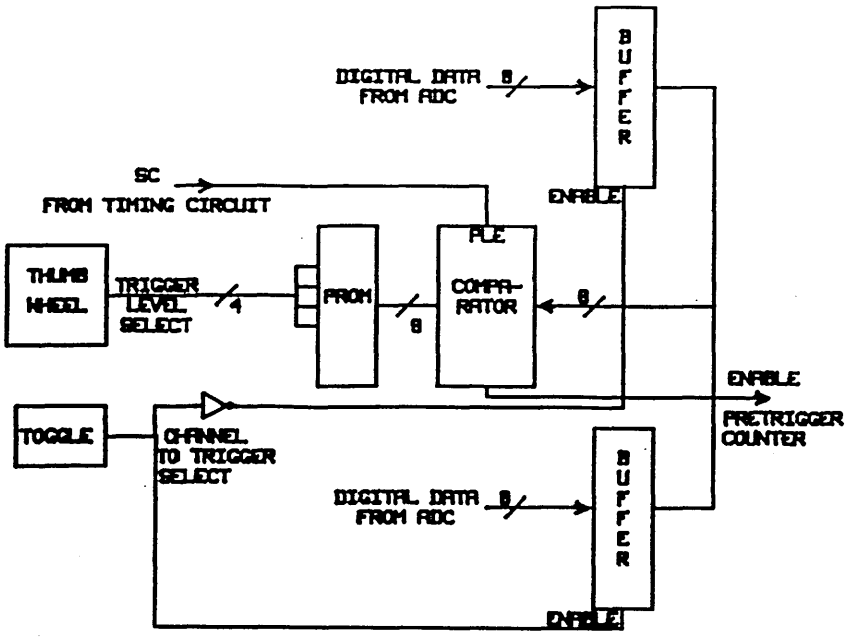


Figure 2.13. Digital trigger level implementation.

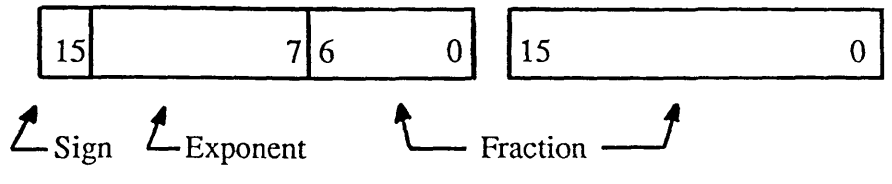
2.3 MEMORY MODULE.

The main function of this module is to store the digital representation of the analogue voltage and current. Additionally a digital output port provides the facility to transfer the digital data to the processing unit, i.e., the microcomputer, and two analogue outputs offer the possibility to display the digital data on a standard oscilloscope.

2.4.1 MEMORY MODULE DESIGN CONSIDERATIONS.

The main characteristic of the memory module to specify, is the storage capacity. The storage capacity has a close relation with the sampling frequency, data window length and addressing capability of the microcomputer.

Due to the experience and support offered within the MAG Section, it was proposed to use the LSI-11-23 microcomputer as processing unit. This particular computer has a direct addressing capability of 64K bytes (this addressing capability can be extended by appropriate usage of a memory management unit, however, this was not available at the time during which this work was carried out). Floating point numbers are represented as either 32 bits (single-precision) or 64 bits (double precision). Single precision numbers are stored within two contiguous 16 bit words as shown below :



Thus, in principle, it would be possible for this computer to address up to 16K single precision numbers. This is not totally true since some space should be provided for the operating system and the program which implements the algorithm. As a consequence it was decided to set, initially, the storage capacity of the memory module to 4K bytes per channel, and include in the design the facility to easily expand it to 8K bytes per channel. The 4K bytes per channel storage capacity implies a maximum transmission line length of 30 km., which is reasonable for the line lengths encountered in the power system distribution level.

2.4.2 SPECIFICATION OF THE MEMORY MODULE.

The specification for the memory module is given below :

- Two independent memory banks, each one with a storage capacity of 4K bytes.
- Parallel digital output port to work as interface with a processing unit or microcomputer.
- Two independent analogue outputs to be connected to an oscilloscope for display of the information contained in both memory banks.
- Easily expandable to a storage capacity of 8K bytes per bank.

Figure (2.14) shows a block diagram of the memory module. The circuit diagram is included in appendix A and a photograph of it is shown in figure (2.32).

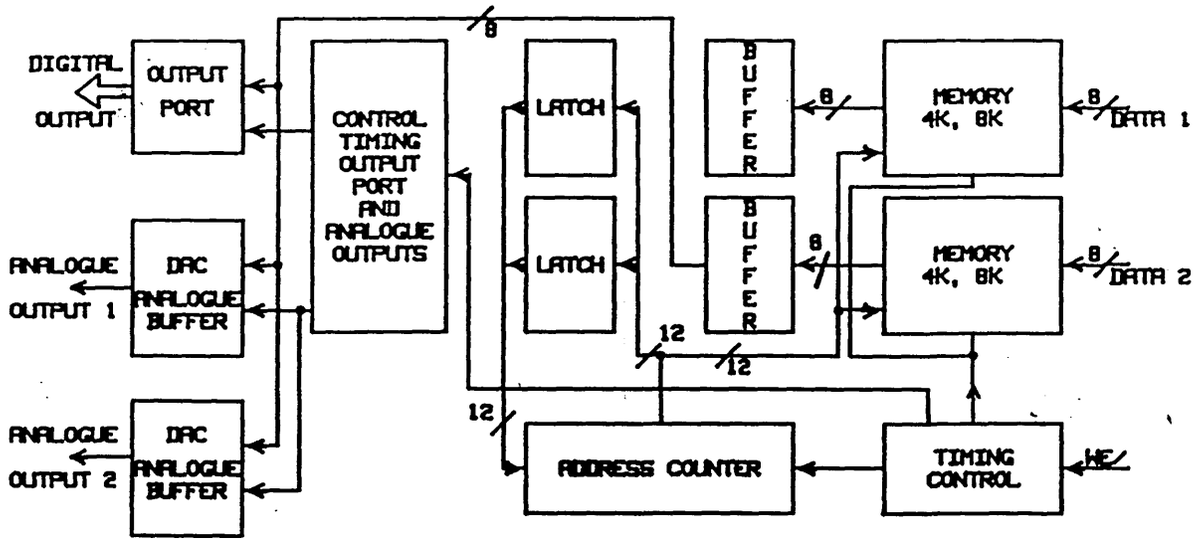


Figure 2.14. Block diagram of the memory module.

2.4.3 MEMORY MODULE CIRCUIT DESCRIPTION.

The function performed by this module are :

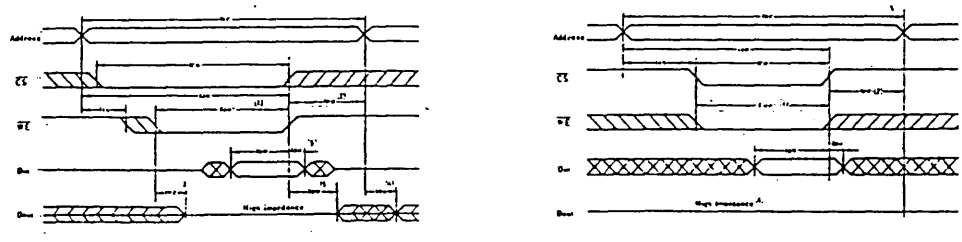
- Store the digital representation of the analogue signals at the input channels.
- Store the address of the memory location coincident with the trigger.
- Output data to computer.
- Generate the analogue version of the digital data stored in memory to display it in an oscilloscope.

This module plays an active role under three of the four possible modes of operation of the fault locator, that is to say :

a) Converting and storing mode
b) Sending data to microcomputer and processing mode, and
c) Outputting data to oscilloscope mode.

These modes of operation are mutually exclusive, i.e., only one can be active at any one time.

Converting and storing mode.- In the first mode, data entering the module are stored in consecutive memory locations in both memory banks. The memory chip chosen is a 4K x 4 bits device, with a minimum write cycle of 45 ns. It has two possible write cycles, WE/ controlled or CS/ controlled. Both are reproduced in figure (2.15).



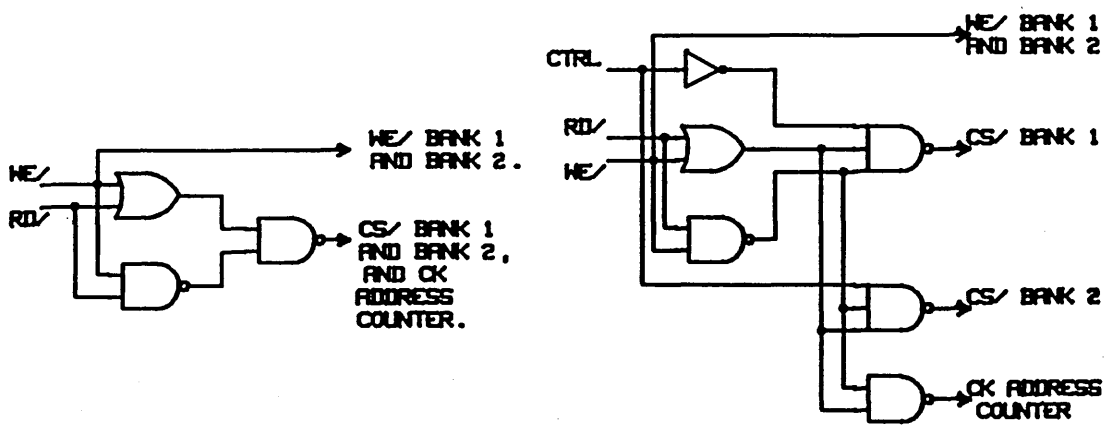
(a)WE/ controlled *(b) CS/ controlled*

Figure 2.15. Memory chip write cycles.

The difference between the two cycles at a first glance, seems to be only whether WE/ or CS/ is considered the active signal since a write occurs during the overlap of a low CS/ and a low WE/, however, a closer examination shows that under the CS/ controlled write cycle, if the CS/ low transition occurs simultaneously with the WE/ low transition or after the WE/ transition, the output buffers of the memory chips remain in a high impedance state. This is important since the data lines are being driven by the output latches of the A/D conversion module, and contention would occur if the output buffer of the memory chips were enabled in this mode of operation.

The signals controlling the write to memory cycles are WE/ and enable conversion. The timing circuitry that generates the appropriate signals for a full write cycle is shown in figure (2.16). Two cases are shown which are slightly different depending on the existing storage capacity, 4K bytes or 8K bytes. Timing analysis was done for the worst case, i.e., 20 MHz sampling frequency.

The operation in this mode is straight forward (see figure 2.17). On receiving the enable conversion signal, modes b) and c) are disabled. Each WE/ pulse enables the memory chips, valid data are written into memory and the address counters are incremented. This state is maintained until either, the trigger level reached is generated by the comparator in the analogue to digital conversion module or the stop sampling button, at the front panel, is depressed. The signal trigger level reached is used as the clock signal for the initial address registers which store the address coincident with the trigger (this address is used later as the starting address to send data to the microcomputer).



a) 4K, 20 MHz. *b) 8K, 20 MHz.*

Figure 2.16. Timing circuitry for write cycle.

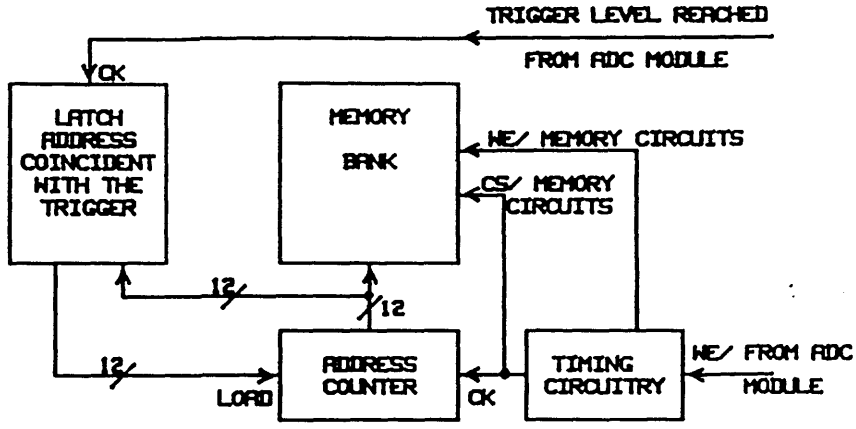


Figure 2.17 Circuitry involved in the converting and storing mode.

The timing diagram showing all the signals involved in the "converting and storing" mode of operation is shown in figure (2.18). This diagram corresponds to 20 MHz. sampling frequency operation which is the most demanding case since the point of view of speed and includes worst case delay values. The operation is described only for channel 1 since the operation for channel 2 is similar.

As explained in section 2.3.5, the time base generates a stable 40 MHz. TTL signal which is passed through the multiplexer U14 (see analogue to digital converter circuit diagram), from which the signals MC and its complement MC/ are obtained. MC is divided by two to obtain SC and SC/. The signal SC is passed through a TTL to ECL converter (U17), and is used to drive the clock inputs of both A/D converters. The negative going edge of SC digitizes the four most significant bits, while the positive going edge digitizes the four least significant bits. The output data in ECL logic are available 12 nanoseconds maximum after the rising edge of the clock. The data are converted to TTL logic by the ECL to TTL converters U3 and U4, which introduce a delay of 3 ns. The TTL data are latched in the output latch U5 by the rising edge of SC/. After a maximum propagation delay of 15 ns., introduced by the latch, valid data appear at the input of the memory circuits. Meanwhile, the signal WE/ has been generated as WE/ = (MC + SC/)/. This signal has to propagate through several gates (NOR gate in ADC module and NAND gates in memory module) before reaching the write enable input of the memory circuits. The two propagation delay extremes (minimum and maximum) for these gates were considered and a WE/ minimum and a WE/ maximum were obtained. From the diagram it

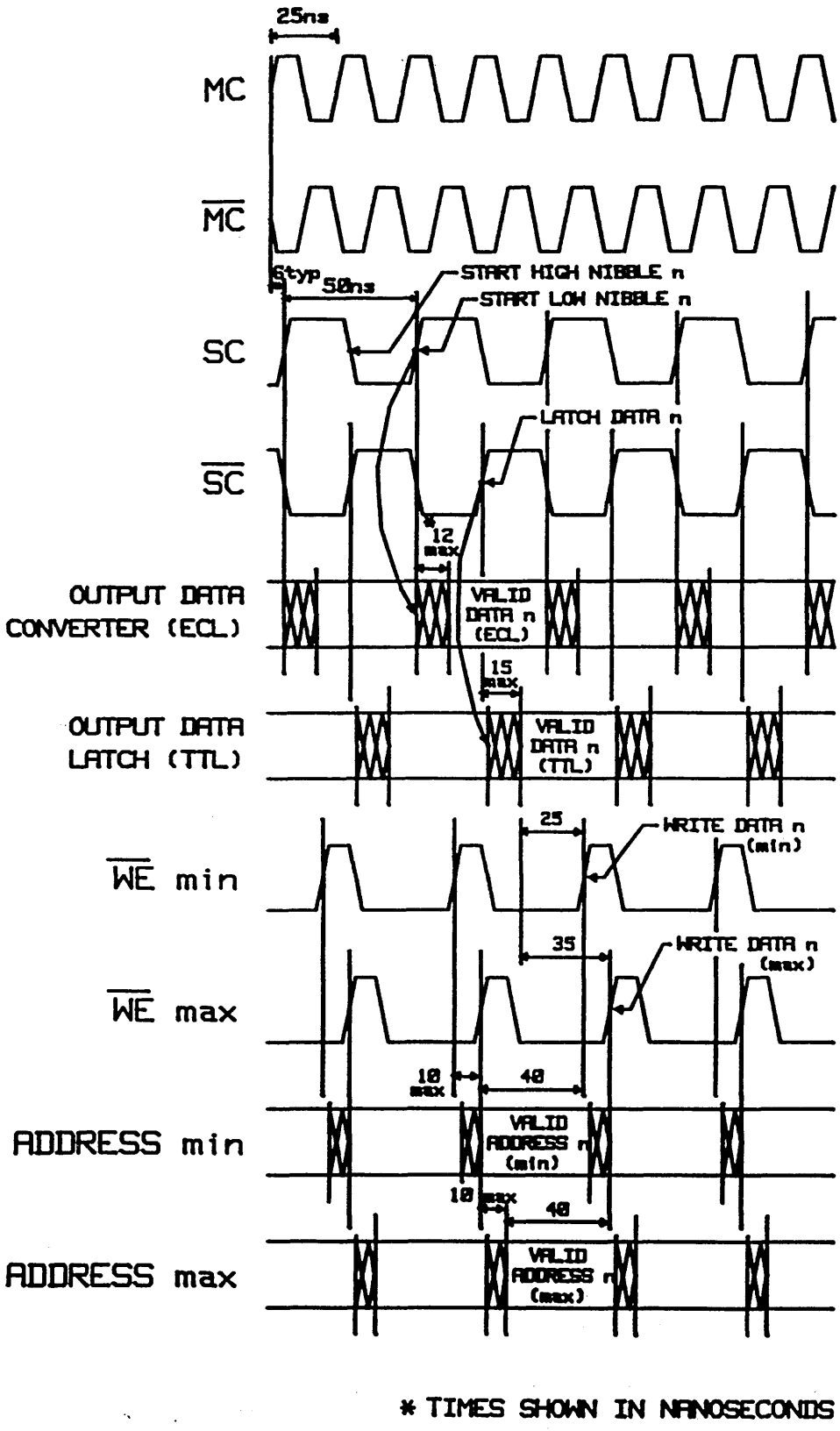


Figure 2.18. Timing diagram for "converting and storing" mode.

can be noted that the time during which valid TTL data are present before the rising edge of WE/min is 25 ns. and that for WE/max is 35 ns. Both data set-up times are above the minimum data set-up time specified by the manufacturer of the memory circuits which is 20 ns. It can also be noted that the set-up time for valid address is 40 ns. in both cases which accords with the chip specification.

Transfer data to computer.- The data transfer is done through the output port (see figure 2.19). The signal Ready/ should be low before initiating the transfer. The control under this mode is given by the microcomputer via the signals CTRL0, CTRL1 and RD/. The state table for the control lines is given below :

CTRL1	CTRL 0	State
0	0	Idle
0	1	Load Initial Address
1	0	Read Memory Enable 1
1	1	Read Memory Enable 2

Driving these signals to the appropriate state, the information contained in either memory bank 1 or memory bank 2 can be read. A typical sequence would be as follows: enter state "load initial address" and send a pulse in the RD/ line, this will load the address coincident with the trigger to the address counters. Enter state "read memory enable 1" or 2 and send pulses in RD/. During the low state of RD/ a valid data will appear in the data bus. This byte should be read with the rising edge of the RD/ pulse. As each RD/ pulse corresponds to one byte of data, 4K pulses should be sent for a complete data transfer. A similar procedure is repeated to transfer data corresponding to the other memory bank.

Output data to computer.- Once the "output to scope" button is depressed at the front panel the information contained in memory banks 1 and 2 will appear in analogue form at the analogue outputs 1 and 2 respectively. The timing diagram associated with this state is given below in figure (2.20). The signals referenced in the diagram can be found in the circuit diagram of the memory module in appendix A. The description of this timing diagram is as follows: the backplane signal Aux.Ck. is used to obtain the signals labeled as CK and CK/. These signals are divided over two to obtain CK/2 and its

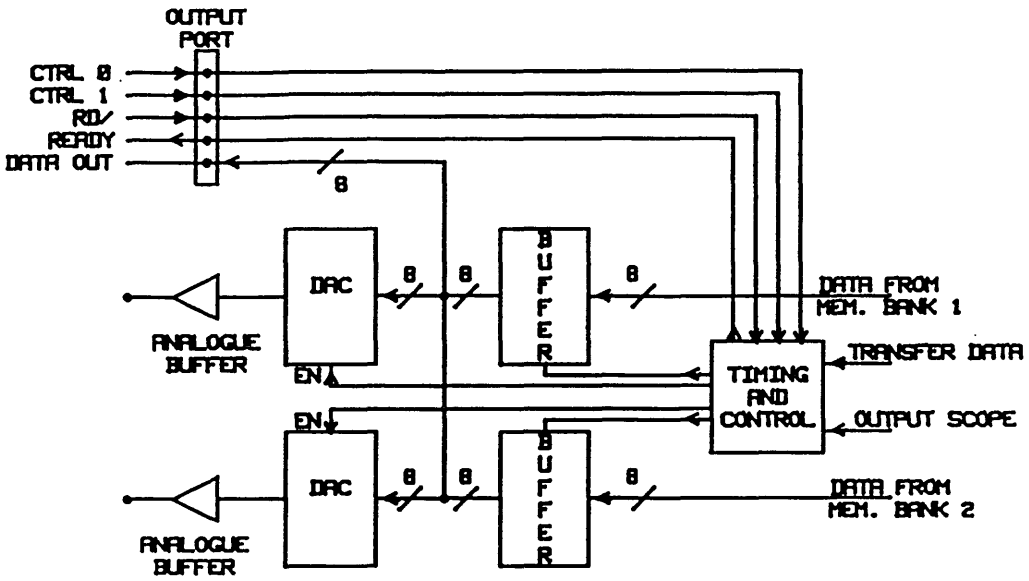


Figure 2.19. Circuitry involved in transfer data to computer and output data to scope modes.

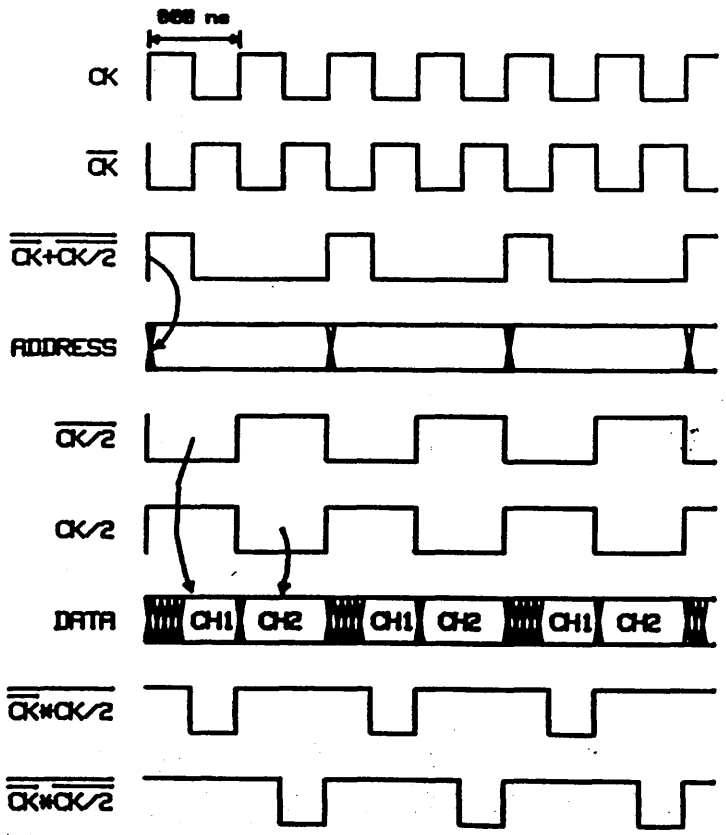


Figure 2.20. Timing diagram for output to scope mode.

complement (CK/2)/. The signal (CK/2)/ is used to drive the output enable inputs of the buffer U4, which allows valid channel 1 data to appear on the output data bus. The signal CK/2 performs a similar action for channel 2 data. The signal (CK/ + (CK/2)/)/ is used to drive the clock input of the address counters and the chip select input of the memory circuits in such a way that for each address increment both memory banks are enabled. The signals (CK/ * (CK/2)/ and (CK/ * (CK/2)/)/ are used to drive the enable inputs of the digital to analogue converters in such a way that the DAC's are enabled only when stable and valid data are present in the output data bus.

2.5 ANALOGUE INPUTS MODULE (SIGNAL CONDITIONING).

The functions performed by this module are the following :

- Reduce the amplitude of the input voltage and current injected to the line to adequate levels for the A/D module.
- Set the input impedance of the instrument.
- To drive the inputs of the analogue to digital converters.
- To filter the input signals according to the sampling frequency to avoid aliasing.

2.5.1 ANALOGUE INPUTS MODULE DESIGN CONSIDERATIONS.

The A/D converter has a low input impedance (75 Ω) limited to 1 V_{pp} signal level which is not compatible with capacitive voltage dividers nor signal levels obtained from them or from current shunts. These problems can be solved by adding a proper buffer amplifier and input attenuators.

The attenuators should be designed to change the magnitude of the input signal seen at the buffer amplifier input while presenting a constant impedance on all ranges of attenuation at the input of the attenuator, otherwise the loading to the signal source would

be variable. The resistor combination:

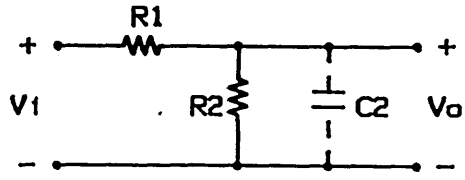


Figure 2.21. Resistor divider.

would multiply the input signal by the ratio $a = R_2 / (R_1 + R_2)$ if it were not by the inevitable capacitance C_2, which represents the addition of the input capacitance of the buffer amplifier plus stray capacitances. This attenuator is usually compensated by adding a capacitance C_1 across R_1 to obtain the circuit :

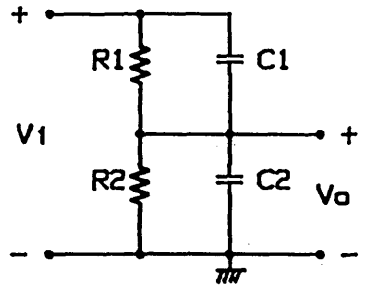


Figure 2.22. Compensated resistor divider.

The transfer function for this circuit is:

$$\frac{Vo}{Vi} = \frac{R2\,(1 + s\,R1C1)}{R2\,(1 + s\,R1C1) + R1\,(1 + s\,R2C2)}$$

making R1C1 = R2C2 gives:

$$\frac{Vo}{Vi} = \frac{R2}{R1+R2}$$

which is independent of frequency.

The designed attenuator is characterized by a high (1 MΩ) input impedance in parallel with 10 pF which eliminates the loading effect on the transducers. Each of the two attenuators has five division ratios in a 1-2-5 sequence with maximum attenuation ratio equal to 50. A typical attenuator is shown in figure (2.23), where a 5 pF capacitor has been added in parallel to keep the input impedance constant and make the individual sections cascadeable.

In order to drive the 75 Ω input of the A/D converter a fast buffer amplifier with highly stable unity gain is required. The analogue bandwidth of either channel should be as wide as possible, say, 3 to 4 times the bandwidth of the input signal referred to the maximum sampling frequency. This wide analogue bandwidth results in reduced amplitude rollof and less time delay distortion.

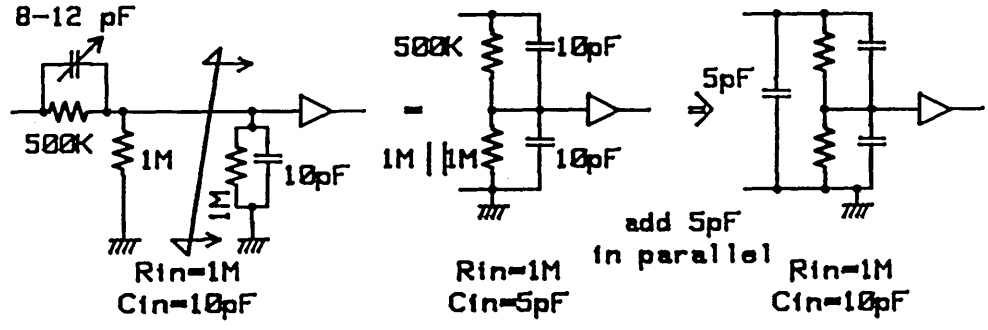


Figure 2.23. Attenuator.

The anti-aliasing function should be performed by separate anti-aliasing filters design especially for that purpose. If the sampling frequency is variable, the cutoff frequency of the anti-aliasing filter should change accordingly.

2.5.2 SPECIFICATION OF THE ANALOGUE INPUTS MODULE.

- Two identical and independent analogue input channels with attenuation ratios

equal to : 1, 2, 5, 10, 20 or 50.

- The attenuation factors are selected individually for each channel by means of two knobs at the front panel.
- Anti-aliasing filters with cutoff frequencies according to the sampling frequencies.
- The maximum input voltage to either channel is 100 V.

A block diagram of the analogue inputs module is shown in figure (2.24). The circuit diagram is included in appendix A.

The device chosen as buffer amplifier is the LH0033C. Even though it is completely specified elsewhere, its main A.C. characteristics are included in the following table:

PARAMETER	CONDITIONS	TYPICAL LIMIT	UNITS
Slew Rate	Vin = ± 10 V	1500	V/μs
Bandwidth	Vin = 1.0 Vrms	100	MHz
Phase Non-linearity	BW=1.0 to 20 MHz	2.0	degrees
Rise time	ΔVin = 0.5 V	2.9	ns
Propagation Delay	ΔVin = 0.5 V	1.2	ns
Harmonic Distortion	f > 1 KHz	< 0.1	%

Table 2.2. A.C. characteristics for fast buffer amplifier.

Overvoltage protection has been included by means of two schottky barrier diodes connected as a double-ended clipper.

The anti-aliasing filters are passive, 4th. order, low pass, Butterworth types. Since source and load impedances are equal,either T or Pi configuration could be used,

however, the Pi configuration was chosen because it requires fewer inductors.

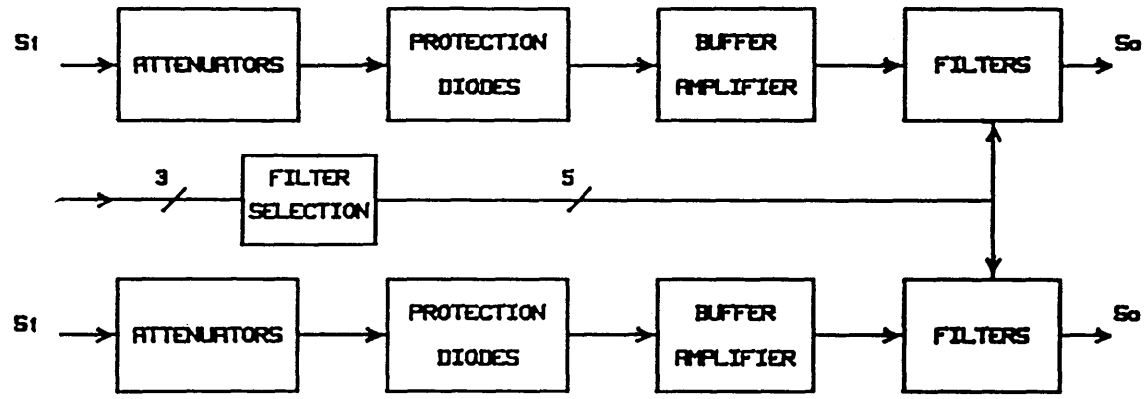


Figure 2.24. Block diagram analogue inputs module.

2.6 CONTROL MODULE.

The main function performed by this module is to generate the necessary signals to control the operation of the instrument and to select the different modes of operation. Figure (2.25) shows a block diagram of this module and the circuit diagram is included in appendix A.

The signals generated are the following:

- Initial power on reset that :
  - sets the "end of conversion steady state" signal low.
  - sets "enable conversion" high
  - clears the posttrigger counters

clears address counters

sets "trigger level reached" low

clear initial sequence counter

- Start sampling.- Prior to start sampling the posttrigger counters are loaded.

- Stop sampling .- Required if the of instrument is storing data in memory and the trigger level is not reached, i.e., the trigger level is higher than the input signal and it is desired to stop the conversion.

- Manual Reset.-It has the same effect as power-on reset.

- Output to scope.- Enables the output to scope clock.

-End of conversion.- This signal is generated by the posttrigger counter on reaching its final count and is used to disable the conversion.

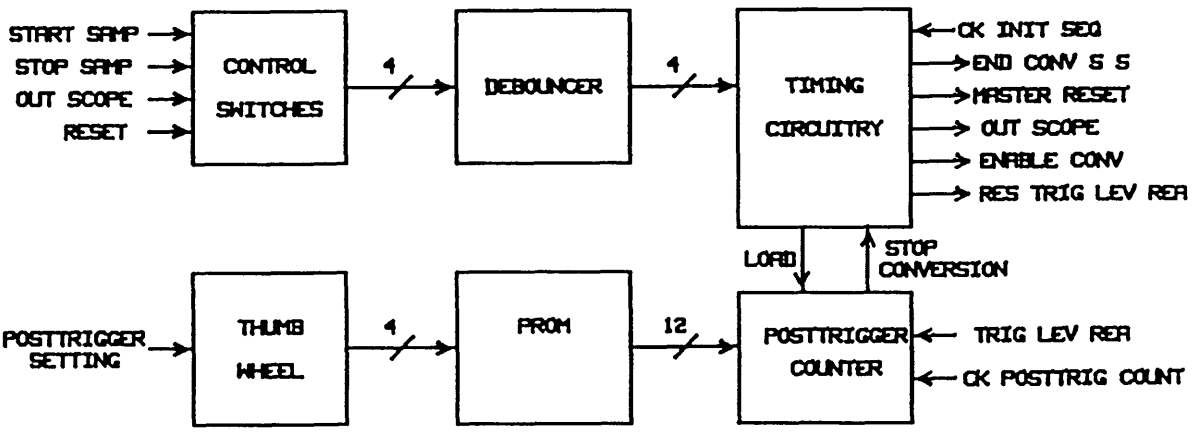


Figure 2.25. Block diagram of control module.

2.6.1 CONTROL MODULE CIRCUIT DESCRIPTION.

The operation of the control module under the different modes operation of the fault locator is as follows:

Conversion and storing.- On receiving the start sampling signal from the front panel a sequence of preparatory actions is started before the actual conversion and storing.

The first action is to reset the trigger level reached signal to low level, then the posttrigger counters are loaded with the code corresponding to the amount of desired posttrigger, and finally enable conversion is driven to its active state, initiating the conversion. This state is maintained until the signal trigger level reached is received from the ADC module, which enables the posttrigger counters. On reaching its final count the posttrigger counter generate a signal to drive the enable conversion signal to its inactive state, ending the conversion and storing of data. The count corresponding to the posttrigger memory amount is given by a PROM which in turn is driven from a thumb wheel at the front panel.

Transfer data to computer and output to scope.- The role played by this module under these modes is that of enabling or disabling them, depending on the signal received from the front panel since all the timing and control signal for these modes of operation are generated at the memory module as explained in section (2.4.3)

2.7 BACKPLANE.

The designed backplane provides the interconnection medium between the different modules which conform the fault locator apparatus.

2.7.1 BACKPLANE DESIGN CONSIDERATIONS.

Since several high frequency signals propagate along the backplane, special attention was given to electromagnetic compatibility considerations and transmission line effects during the design. A more detailed account on these considerations is given in section (2.8). The pins are numbered following the 41612 DIN standard. Table (2.3) lists the pin designation. A photograph of the real backplane is shown in figure (2.33).

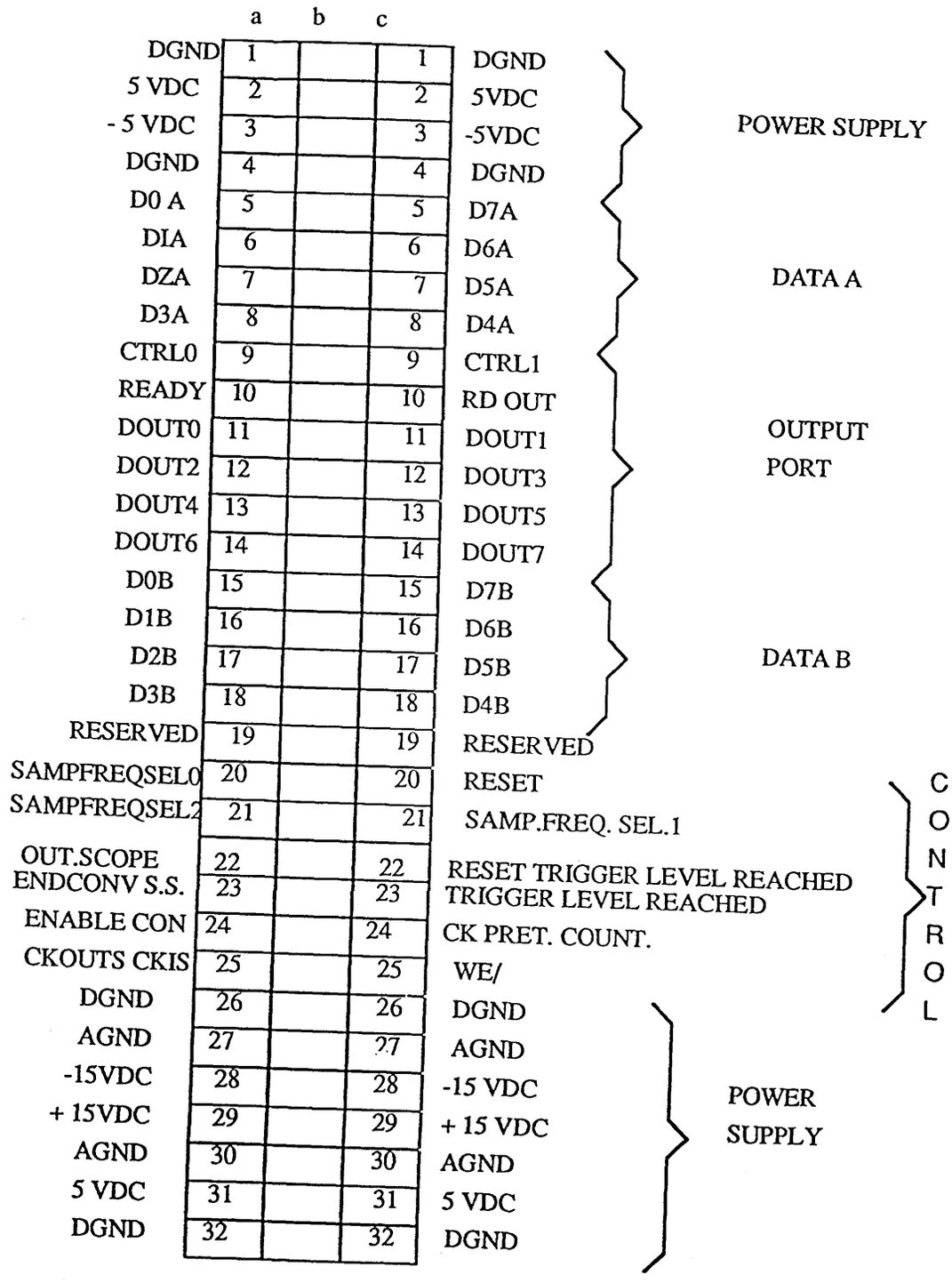


TABLE 2.3. Pin designation for backplane.

2.7.2 BACKPLANE SIGNAL DEFINITIONS.

Pin No.	Signal	Definition
a5-8, c5-8	D0A- D7A	Data bus channel A, active high , unidirectional.
a15-18, c15-18	D0B- D7B	Data bus channel B, active high, unidirectional.
c20	RESET/	Master reset, it has action on : - Reset trigger level. - Set enable/ disable conversion. - Clear posttrigger counters. - Clear address counters. - Reset initial sequence flip-flop.
a20-21, c21	SAMP. FREQ. SEL. 0,1and2	Sampling frequency selection lines.- The state of these lines selects the appropriate anti-aliasing filter depending on the chosen sampling frequency.
a22	OUT SCOPE/	Output to scope control, active low.-Generated by pressing the appropriate button in the front panel. Enables the output to scope circuitry only if there no conversion cycle in process.
c22	RESET TRIG LEV. REACHED	Reset trigger level reached, active low, used to reset the trigger level reached signal (conversion module) during the initial sequence before starting a conversion cycle.
a23	END of CONV. SS/	End of conversion steady state, active low. Disables output to scope and transfer to computer when a conversion cycle is being performed.
c23	TRIG. LEV. REACHED	Trigger level reached, active rising edge.- Generated when a valid data , coming from the channel selected for trigger, have surpassed the trigger level. It enables the posttrigger

		counters (control module) and clocks the initial address registers (memory module).
a24	EN. CONV./	Enable conversion, active low.- When low, the conversion cycle is started, all other modes of operation are disable. It goes high once the posttrigger information has been stored.
c24	CK.PRET. COUNT.	Clock posttrigger counters. Once the trigger level has been reached in a conversion cycle, each rising edge of this signal increments the posttrigger counters.
a25	AUX.CK	Auxiliary Clock.- Used to clock the initial sequence before a conversion cycle (control module) and to clock the output to scope circuitry (memory module).
c25	WE/	Write enable.- Generated by the conversion module and used to control the WE/ and CS/ inputs of the memory chips and to increment the address counters.
a9-10, c9-10	CTRL0 and 1 READY, RD/	Control lines to select channel to transfer data to computer.
a11-14, c11-14	DOUT0- DOUT7	Data lines to transfer data to computer.
a1,c1, a4, c4 a26, c26, a32,c32	DGND	Digital signal ground.
a2,c2, a31,c31	+5 VDC	+5 Vdc regulated voltage.
a3, c3	-5 VDC	-5 Vdc regulated voltage.
a27,c27, a30, c30	AGND	Analogue signal ground.
a28, c28	-15 VDC	-15 Vdc. regulated voltage.
a29, c24	+15 VDC	+15 Vdc. regulated voltage.

TABLE 2.4 Backplane signal definition.

Additional to the backplane a mechanical assembly, i.e., a card cage is needed to accomplish the following:

- Hold all modules at a prescribed distance between each other.
- Permit quick insertion and extraction for assembly and testing.
- Provide a base for holding the backplane to defined tolerances.
- Offer a degree of shielding to either radiation pickup or radiation emission.

2.8 CONSTRUCTION.

Since the memory and analogue to digital conversion modules and the backplane are involved in high frequency operation, it was decided to design a printed circuit board for each one. The main objectives during the design were to minimize : a) the internal noise sources, b) the radiated and conducted emissions and, c) the susceptibility of the modules to external fields.

2.8.1 CONSTRUCTION DESIGN CONSIDERATIONS.

Noise reduction techniques in electronic systems are well known[23], they are fairly simple and straightforward when applied in the early stages of the design. Of this techniques, the best known and most widely used in digital circuits is, perhaps, the minimization of inductance in the circuit grounding, power distribution and interconnection. Inductance depends on the physical properties of the circuit layout and on the area of the loops formed by the signal and signal return conductors.

Since the inductance is directly proportional to the length of the conductor, an initial step would be to shorten the interconnection tracks. This is usually applied to lines carrying heavy transient currents, like clock lines.

Another way of reducing inductance is to increase the width of the conductor, unfortunately this is not very effective due to the logarithmic relationship between the

geometrical properties and inductance, i.e.,

$$L \approx 0.005 \, Ln (2 \pi h / \omega) \quad [\mu H/in] , \quad h = \text{hight above ground plane.}$$

ω = width of conductor.

for a flat conductor.

Another method is to provide parallel paths, i.e., the equivalent inductance of two identical paralleled inductors is half of the original one. Taking this concept to its limit, an infinite number of parallel lines is obtained, which is equivalent to a plane.

When paralleling conductors the effect of the mutual inductance should be taken into account in calculating the total inductance, however, if the conductors are arranged in a grid pattern, the mutual inductances can be ignored if the grid size is 0.3" or more[24].

There is another important method of reducing inductance based on the role played by loop areas in magnetic behaviour. If a magnetic field crosses a loop a voltage appears in that loop, i.e.[25]:

$$V_N = j\omega \, B \, A \, Cos \, \phi \quad , \quad V_N = \text{induced noise voltage, V.}$$

ω = frequency, rad/ sec.

B = magnetic field, Weber/ m^2.

A = area of loop, m^2.

for a stationary closed loop and flux density varying sinusoidally.

Conversly, if current flows in a loop , a magnetic field is created which can induce voltages in other parts of the circuit or even in external equipment. Therefore, power and ground lines should be routed close together , as well as signal and signal return conductors, minimizing the area enclosed by them.

Assuming that a low inductance gridded ground system already exists in a PCB, ideally the power distribution system should run parallel to it, however this is not always the case, an alternative solution to the noise voltage generated in the power lines is the inclusion of decoupling capacitors, close to the logic elements requiring the switching current. The value of this capacitor is given by :

$C = \frac{\Delta I}{\Delta V / \Delta t}$, ΔV = voltage variation at capacitor output caused by the flow of a current ΔI during the time interval Δt.

ΔI = transient current demanded by the logic.

Δt = logic state switching time.

The placement of the capacitor should be as close as possible to the IC so as to minimize the inductance of the track connecting it to the IC pins and that of the capacitor leads.

Figure (2.26) shows a power supply distribution and ground system layout which includes several of the above mentioned guidelines.

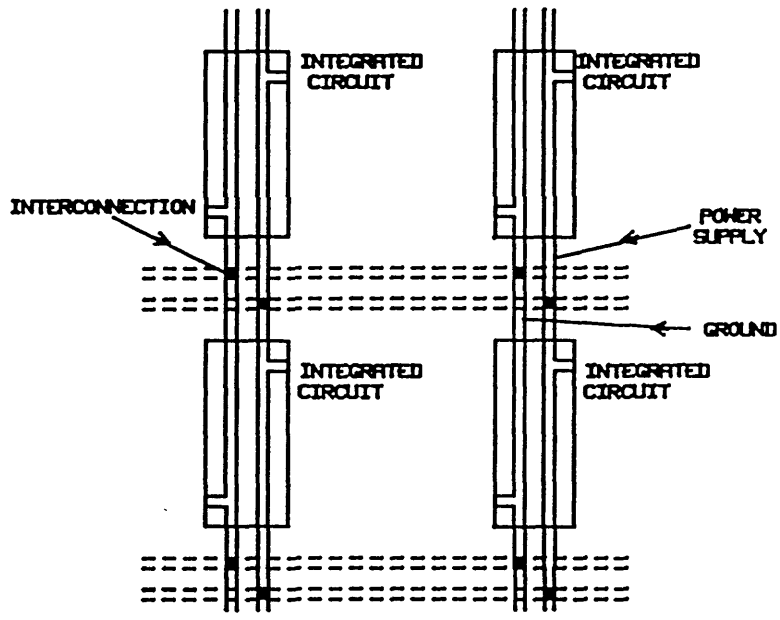
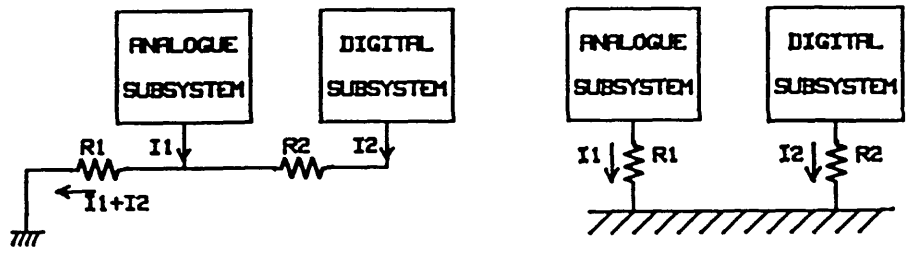


Figure 2.26. Gridded power supply distribution and ground system.

This structure served as the model to follow when the memory and ADC modules printed circuit boards were designed. A diagram of the actual PCB's is included in the appendix B.

The backplane follows the applicable guideline, for example : minimum loop area , etc. and it includes a ground plane, as well as a power plane for 5 Vdc.

From a system point of view the noise problem was considered in the following way. The acquisition system can be thought as being composed of two subsystems, i.e., analogue and digital. These subsystems work at very different power levels. If both were to share a common ground system, the high level power subsystem (digital) ground currents would affect adversely the low level subsystem (analogue). In other words, noise would be coupled through the common impedance. This situation is illustrated in figure (2.27a).



a) *b)*

Figure 2.27 Noise coupled through common impedance.

A more desirable ground system is illustrated in fig. (2.27b) where a ground connection is provided for each subsystem. The ground potential is now a function of the ground current and ground impedance of that susbsystem only.

2.9 TESTS.

Figure (2.28a) shows the ideal conversion relationship for a 3 bit A/D converter. Apart from the inherent quantization uncertainty of $\pm$ 1/2 LSB, there are other sources of error which may deviate the behaviour of the A/D converter from its ideal graph. These sources of error are shown in figure (2.28 b,c,d,e).

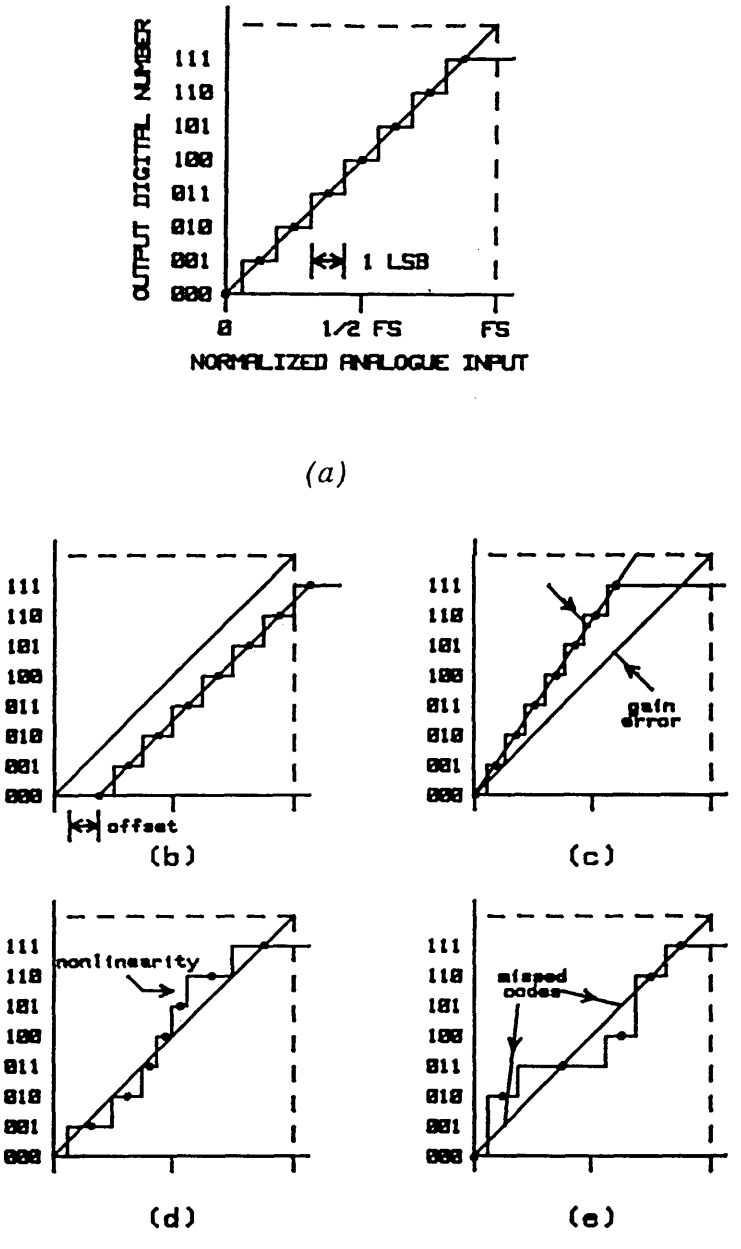


Figure 2.28. (a) Ideal 3 bit A/D conversion (b) Offset error (c) Gain error (d) Linearity error (e) Missed codes.

In order to evaluate the dynamic performance of the data aquisition system the histogram test was carried out using a sine wave as reference signal. The frequency of the sine wave (495 KHz) was selected to be non-coherent with the sample rate (20 MHz). 4K samples of the input signal were taken.

The histogram is plotted with the output codes on the X axis and its number of occurrences on the Y axis. Given a sine wave input, an ideal A/D converter would

produce the probability density function described by [22]

$$p(V) = \frac{1}{\pi \sqrt{[A^2 - V^2]}}$$

where A = peak amplitude of the sine wave.
p (V) = probability of an occurrence at a voltage V.

and plotted in figure (2.29)

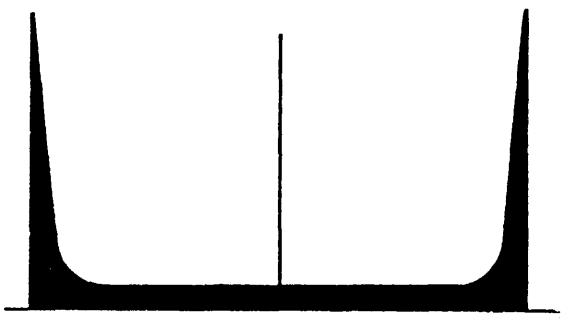
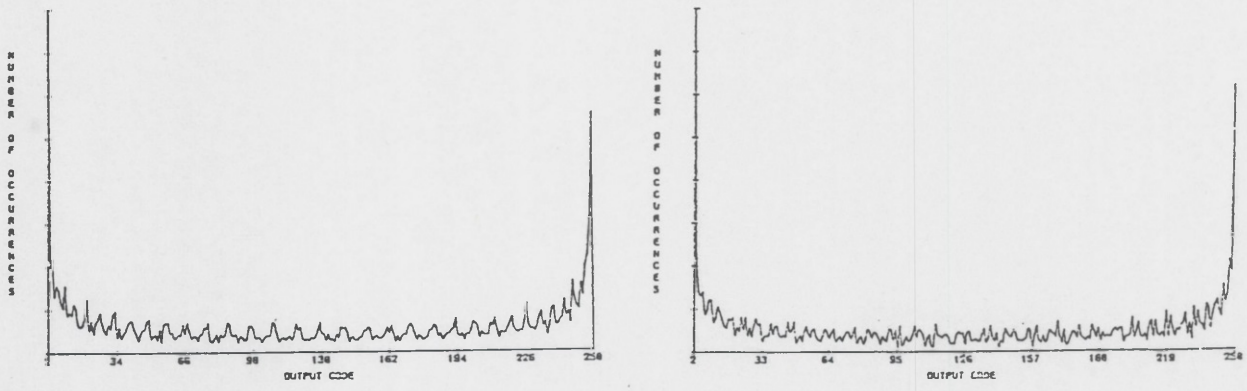


Figure 2.29. Ideal histogram.

If the A/D converter has a step wider than the ideal one, the corresponding digital code will accumulate more "counts " than the ideal one would have, similarly, if the step is narrower than the ideal one, it will accumulate fewer codes. Missing codes are easily detected since the corresponding digital code will show zero "counts".

The differential non linearity is shown up as spikes. Gain and offset errors can be detected since the histogram should be symmetrical with respect to the digital code corresponding to midscale.

The histogram for the acquisition system of the fault locator apparatus is shown in figure (2.30). It can be seen that there are no missing codes, spikes (differential non linearity) and that it is about symmetrical. A photograph of this data acquisition system is shown in figure (2.34).



(a) *(b)*

Figure 2.30. Histogram for data acquisition system .
a) Channel 1, b) Channel 2

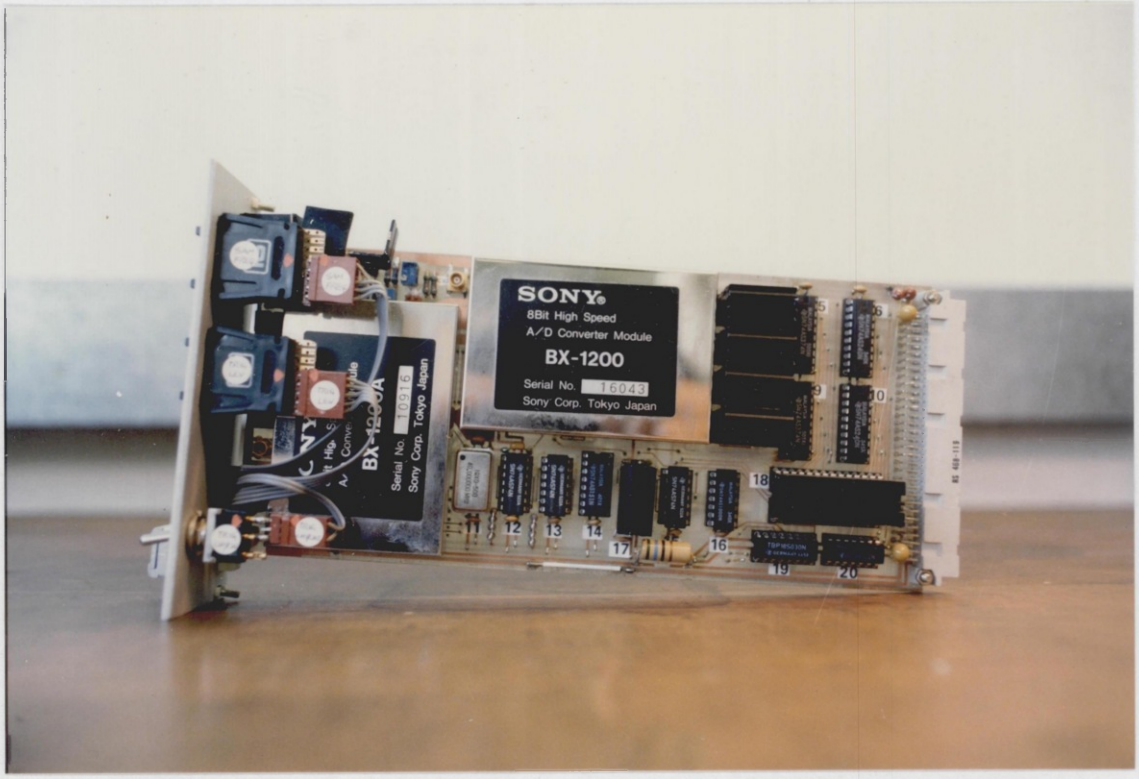


Figure 2.31. Photograph of the analogue to digital converter module.

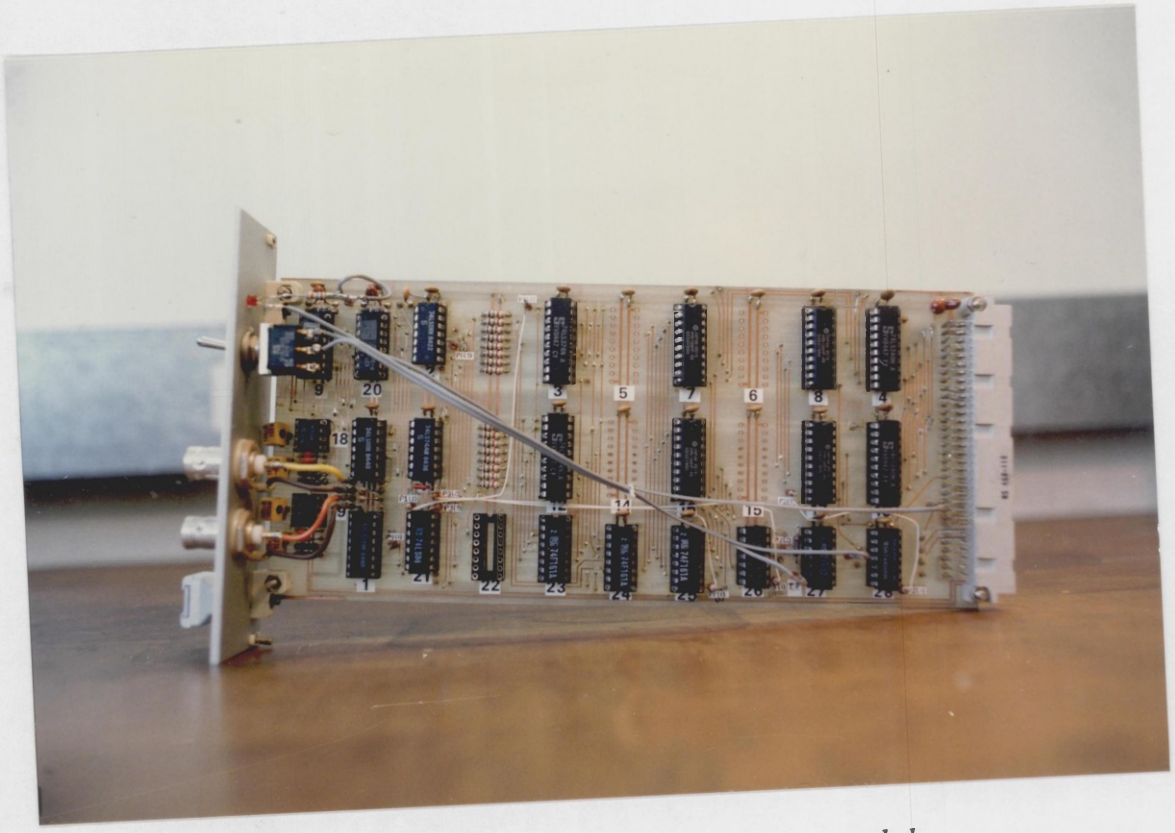


Figure 2.32. Photograph of the memory module.

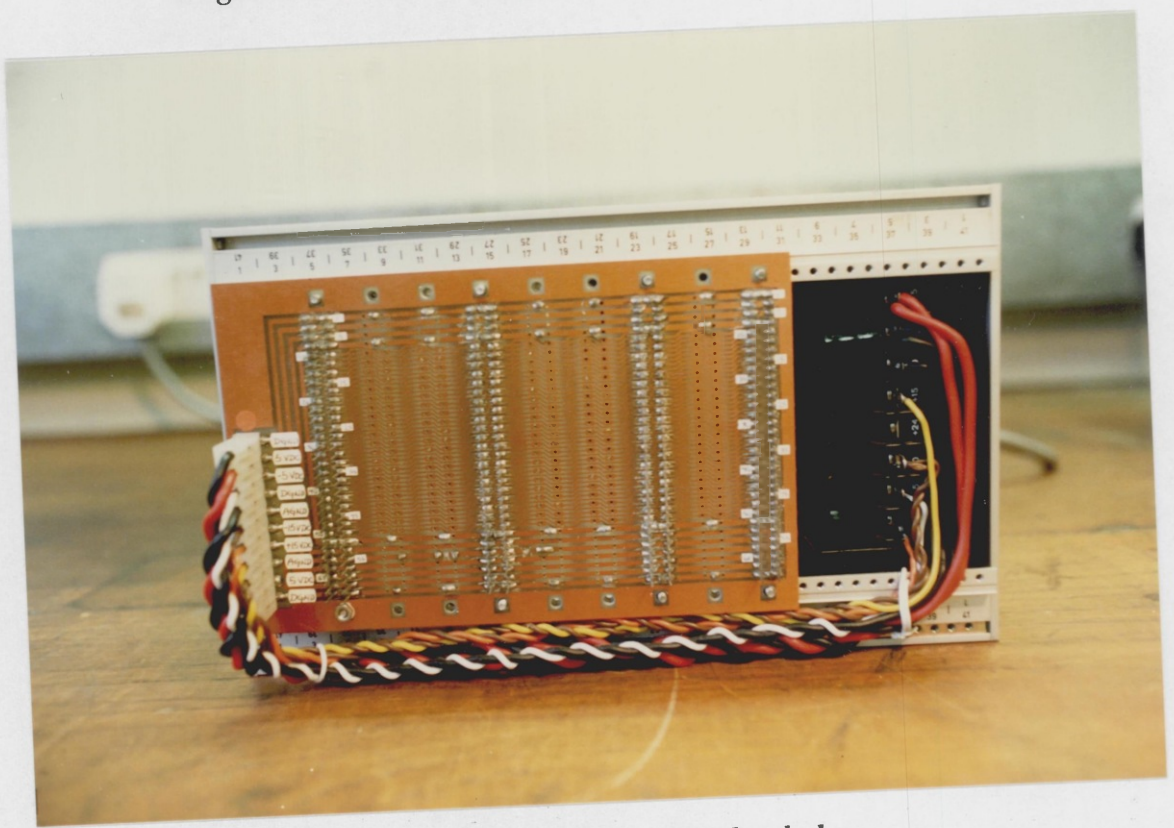


Figure 2.33. Photograph of the backplane.

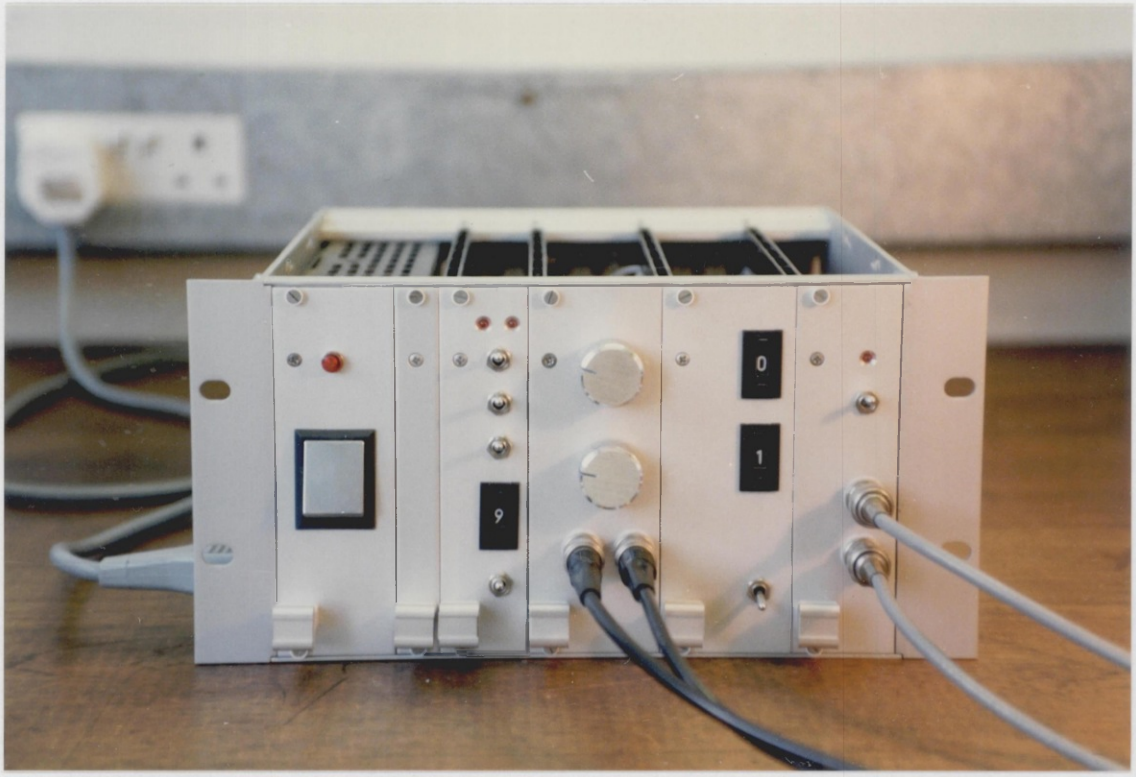


Figure 2.34. Photograph of the data acquisition system of the fault locator apparatus.

2.10 COMPUTER ALGORITHM.

As already stated, the assessment of the practical effectiveness of the fault location method described in section 1.1.5 is of particular interest in the present work. In order to realize this method a computer algorithm was implemented. A flow diagram of this algorithm is shown in figure (2.35), and a listing of the computer program is given in appendix C.

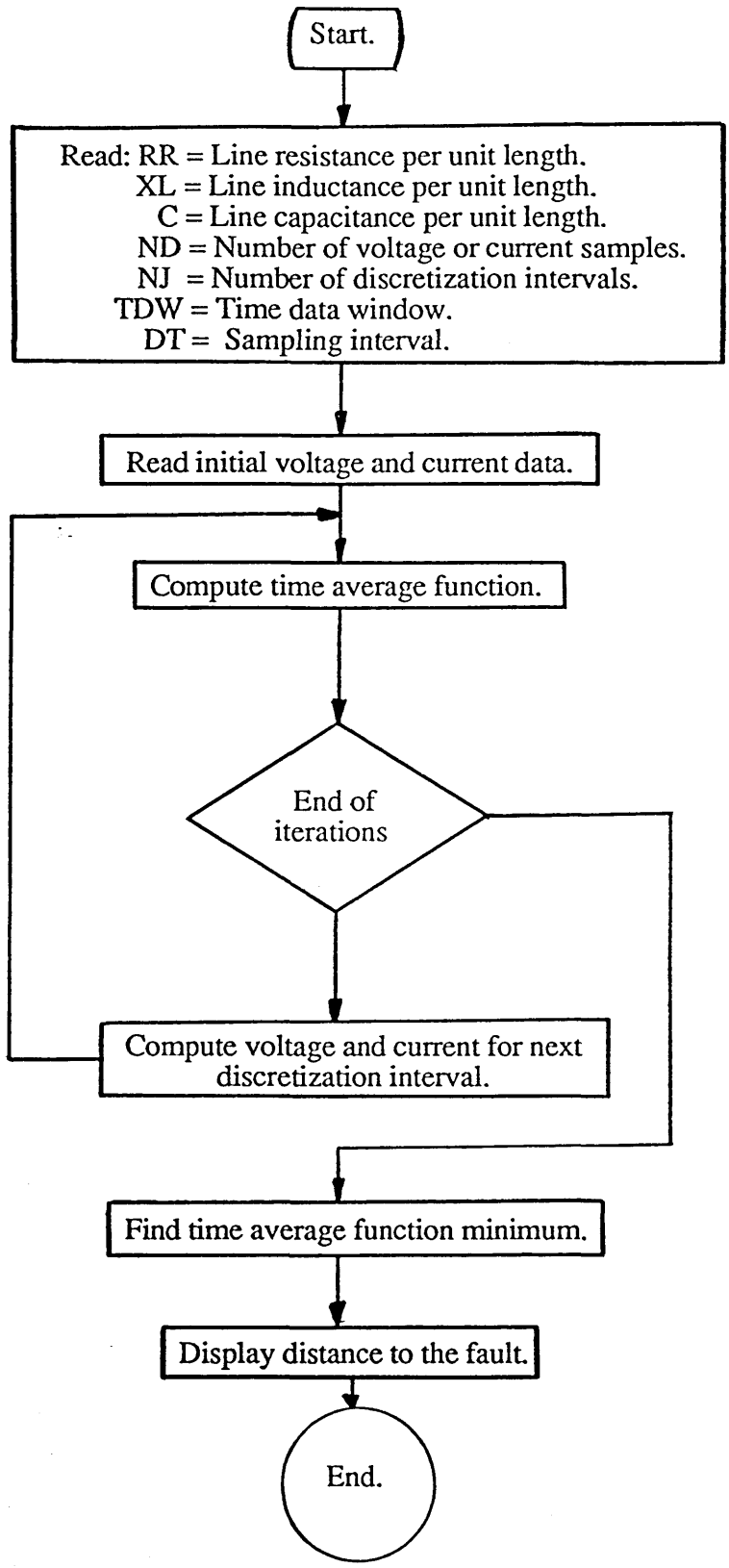


Figure 2.35. Flow diagram for fault location algorithm.

From the flow diagram it can be seen that the initial recordings of voltage and current are stored in two different vector arrays, the size of which, it can be remembered, depends on the time data window T and sampling frequency. The time average function:

$$F(x) = \frac{1}{T} \int_{\alpha x}^{T-\alpha x} u^2(x,t)\, dt$$

is computed from the square of the voltage samples.

By using equations (5) and (6), given in chapter 1, new voltage and current samples are computed for the next discretization interval. Figure (2.36) shows the dependence of the new samples on the previous ones, for the case of six initial voltage and current samples. In order to store the new data being generated and from the computational point of view, a straightforward approach would be to generate two new vector arrays, one for current and one for voltage, and store the newly computed values on them.

On the other hand, assuming that the initial number of voltage and current samples amounts to 4K bytes each one, the minimum data storage capacity required to store the four arrays would amount to nearly 16K bytes. For reasons discussed in section 2.4.1, the LSI-11-23 computer was chosen to be used as processing unit in the fault locator apparatus. This computer has restrictions in its storage capabilities and, consequently, the definition of arrays whose total storage requirements exceed 12K bytes is not possible, therefore, for the situation described above the definition of the two new arrays is not possible in this particular computer.

By introducing a very simple shift in the array indexing, the generation of the two new vector arrays is avoided. This index shift is illustrated in figure (2.37).

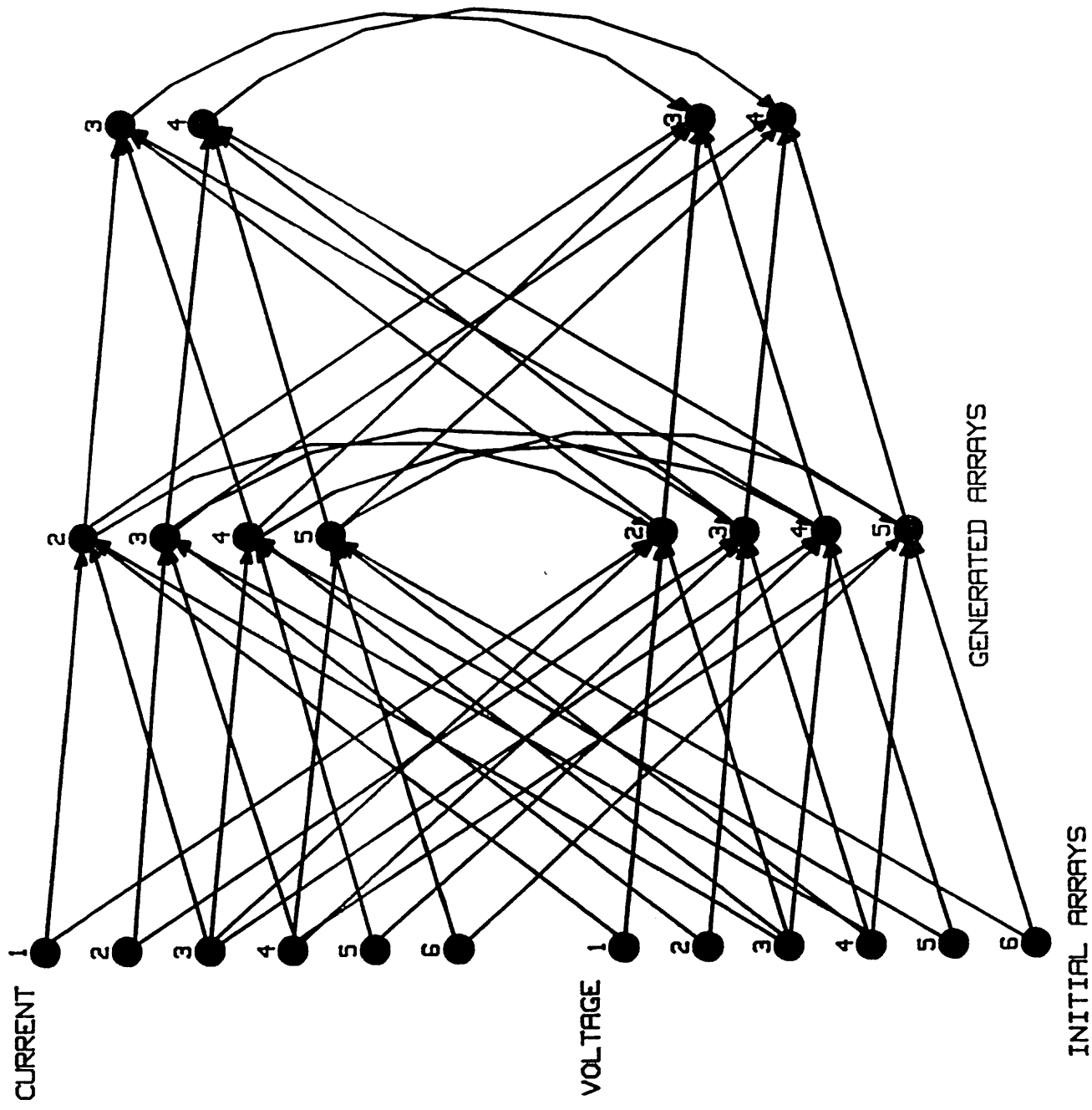


Figure 2.36. Recursive computation of voltage and current samples.

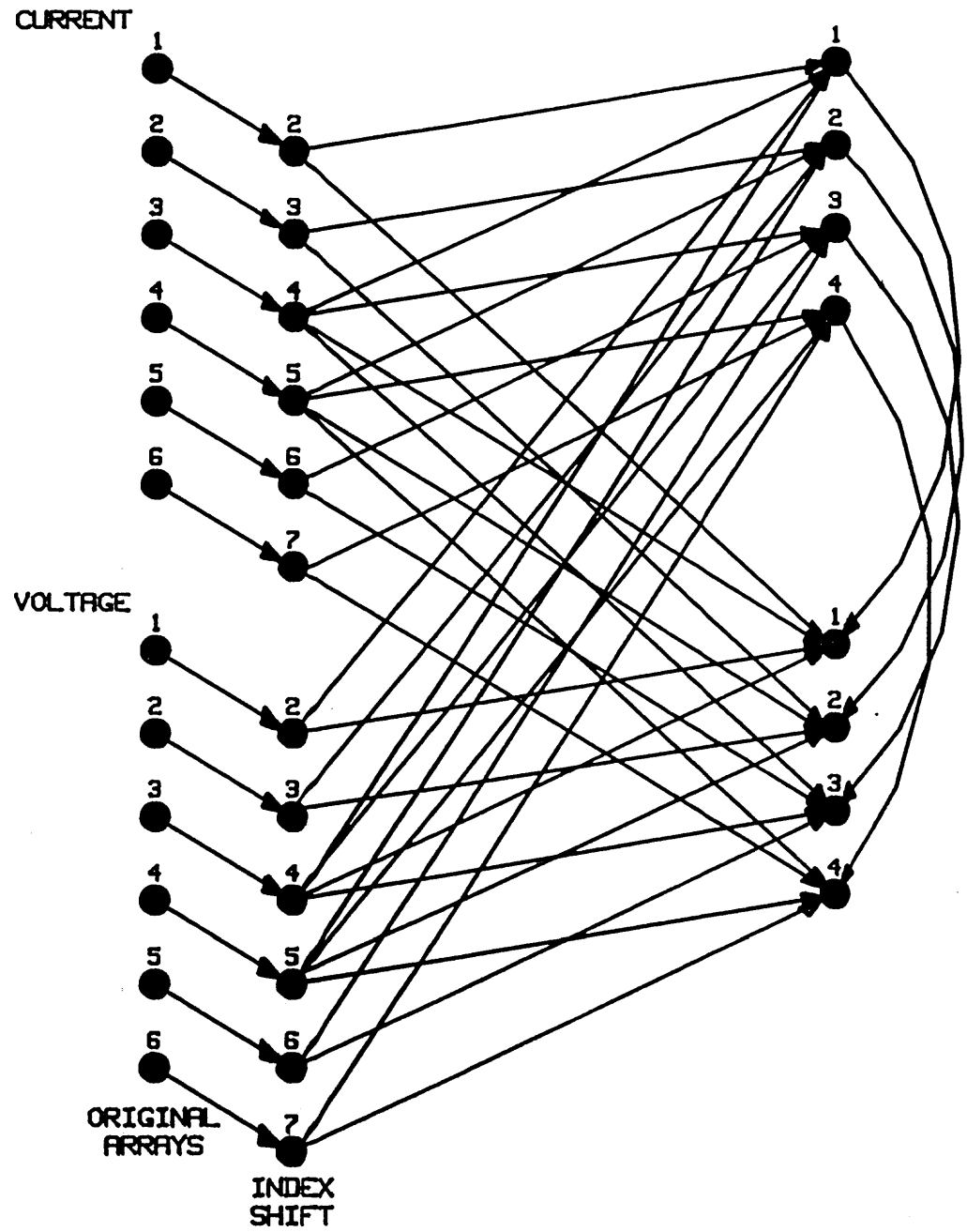
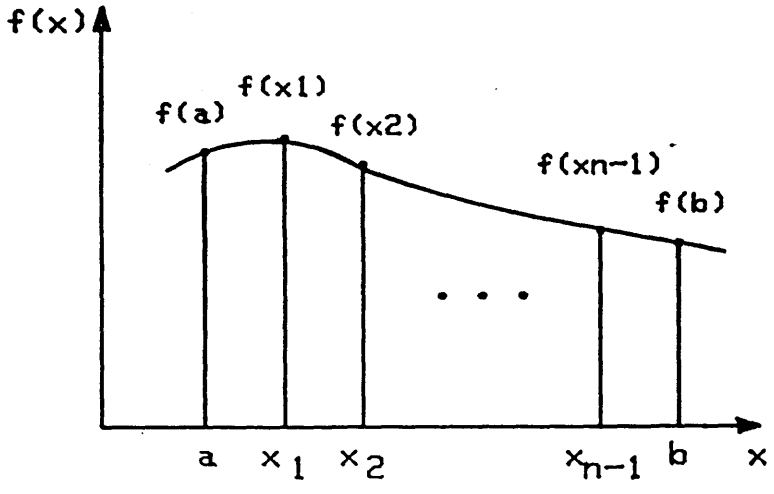


Figure 2.37. Index shift in recursive computation of voltage and current samples.

The time average function is computed by using the well known trapezoidal rule of integration as shown in figure (2.38).



$$F(x) = \int_a^b f(x)\,dx = h\,[\,0.5\,f(a) + f(x_1) + f(x_2) + \ldots + f(x_{n-1}) + 0.5\,f(b)\,]$$

where: $h = \frac{b - a}{n}$

Figure 2.38. Trapezoidal rule of integration.

As already discussed this function is computed for each discretization interval from the square of the voltage samples. In the algorithm, as each new voltage sample is computed, its square is also calculated. These squared voltages are added together in the variable called SUM which is later multiplied by the sampling interval and divided by the time data window value to obtain F(x), therefore, the generation of a new array, containing the square of the voltages, is avoided.

It should be noted that the implementation of the algorithm plays an important part in the accuracy of the fault location. It is estimated that errors due to rounding and truncation are less than one part in six decimal places[30].

CHAPTER 3

SYSTEM PERFORMANCE ASSESSMENT AND RESULTS

3.0 INTRODUCTION.

As stated in section 1.5 the object of this work is to develop a High Speed Data Acquisition and Analysis System for the investigation of the fault location problem in power system lines and cables.

As discussed in section 2.1 the method which considers the fault location problem as an estimation problem is of special interest since it can cope with the high frequency components contained in fault waveforms and does not need highly trained personnel for its interpretation. These two features accord with present trends in fault location practice since the preprocessing of the initial data, that is filtering of high frequency components or dc offset, would be avoided, and the fault location equipment could be operated by unskilled personnel.

Based on the requirements imposed by this particular method and those established by the fault location problem in general, the instrumentation described in the preceding chapter was developed. It includes added features, such as variable trigger level and posttrigger capability, which should make it flexible and enable it to record a range of useful information related to the fault waveforms. It also acts at a sampling frequency which is high enough to sample the injected interrogating signal and the fault generated transients without aliasing, and, since the distance to the fault found is a multiple of the distance discretization interval Δx, and Δx depends on the sampling interval Δt, this sampling frequency promises a distance accuracy in the order of a few meters.

The main purpose of carrying out the tests described in this chapter was to evaluate the performance of the particular method of fault location mentioned above, when applied

in practice on a real coaxial cable and a modelled transmission line.

The tests carried out may be divided into two sets depending on the kind of transmission line used. The first set applies to tests and results obtained for a physical overhead transmission line model, and the second set to a real coaxial cable.

3.1 TESTS AND RESULTS FOR A TRANSMISSION LINE MODEL.

Two different cases were considered during this stage.

a) Injecting a pulse.

b) Injecting a pulse to force the fault to "arc" with ionization delay.

3.1.1. INJECTING A PULSE.

The simplest of fault location problems is, perhaps, that of locating a short circuit or low resistance fault. For this case, the intended fault location sequence would be to inject a pulse to the line, record input voltage and current, analyse these data and obtain the distance to the fault. The circuit diagram of a suitable test circuit is shown in figure (3.1).

The transmission line model is for a 132 kV. overhead line. It consists of 18 pi-sections; each section is equivalent to 2/3 of a mile and is constructed from ferrite cored inductors and paper or ceramic capacitors. The value of the parameters is as follows:

$R = 0.307$ Ω/km (at 159 Hz.)
$L = 1.269 \times 10^{-3}$ H/km
$C = 8.761 \times 10^{-9}$ F/km

In practical tests the amplitude of the injected pulse was restricted to 5 volts to prevent saturation of the inductors occurring. The actual signal injected is a 100 ns. rise time, 1 ms. width pulse, however, only a few microseconds (130 μs. maximum) after the rising edge are used as data window.

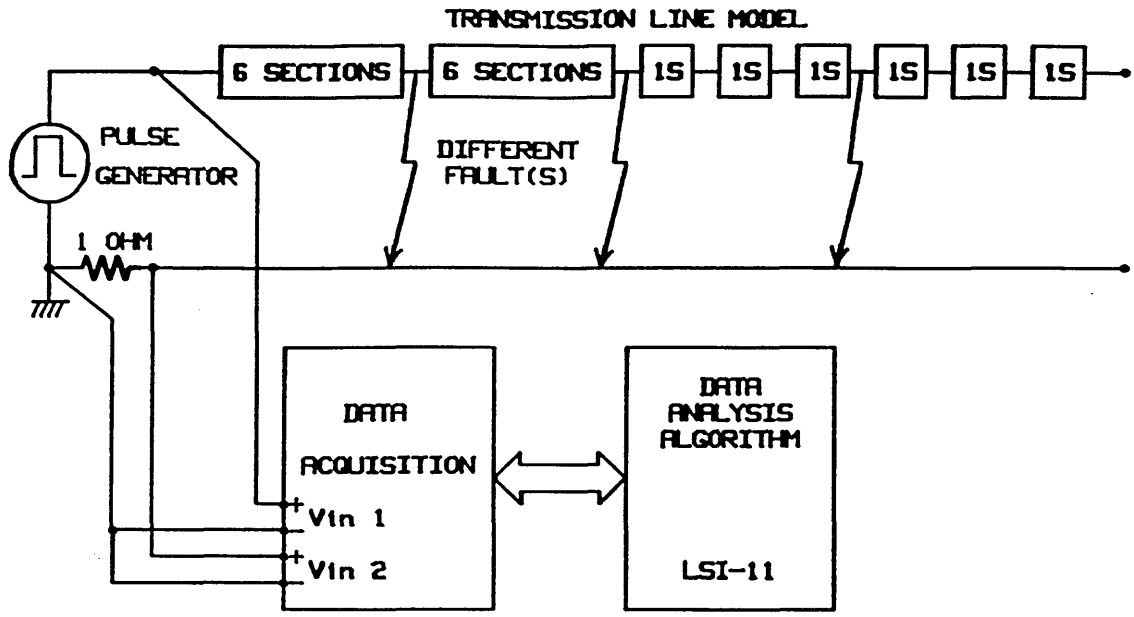


Figure 3.1. Injecting a pulse to a transmission line model , test circuit.

The voltage is measured directly across the input of the transmission line model and ground. The current is measured by means of a resistor located between the ground of the transmission line model and the ground terminal of the pulse generator. Since the resistor is of a very low value (1 Ω), it is considered that its effect on the measurements is negligible.

Three parameters were varied during the tests :

a) Position of the fault along the line.- Three points were chosen :

- 6.437 km
- 12.874 km
- 16.093 km

b) Sampling frequency.- Four different sampling frequencies were used:

- 1.25 MHz
- 2.5 MHz
- 5 MHz

- 10 MHz

c) Data window length.- The theoretical minimum recording of the fault wave corresponds to two times the wave transit time from the measuring point to the point of fault. Initially the estimates of voltage and current should be obtained for the whole length of the line which is known. Additionally, as stated in section 2.3, the accuracy in distance depends on the sampling frequency and this, in turn, affects the data storage capacity and processing time. If a first attempt to locate the fault is performed using a low sampling frequency, a rough idea of the fault location will be obtained, this can be refined by increasing the sampling frequency and restricting the calculation of the voltage and current estimates to a distance slightly longer than the one obtained by the rough approximation. This will save some computation time. Based on this, four data window lengths were considered :

- Two wave transit time for the whole line length.
- Four wave transit times of the same length.
- Two wave transit times for a line length slightly longer than the distance to the point of fault.
- Four wave transit times for the same distance.

Two of the plots of the voltage, current and the criteria function :

$$F(x) = \frac{1}{T} \int_{\alpha x}^{T - \alpha x} u^2(x, t)\, dt$$

defined in section 1.1.5 are shown in figures (3.5) and (3.6) for two of the different test conditions mentioned above. The complete results obtained are shown in Table (3.1).

3.1.2 INJECTING A PULSE TO FORCE THE FAULT TO ARC WITH IONIZATION DELAY.

As mentioned before, section 2.2.2, in the case of high resistance or intermittent faults for cables or high voltage breakdown faults for lines it is necessary to apply a voltage high enough to force the fault to arc and obtain the desired voltage and current waveforms from the transients created by this breakdown. In the present fault location practice this is accomplished by the application of an impulse, generated by an impulse generator, to the faulty line or cable.

The principle of operation of an impulse generator is to charge a number of capacitors in parallel through resistances and discharge them in series through spark gaps[26]. A typical circuit is shown in figure (3.2).

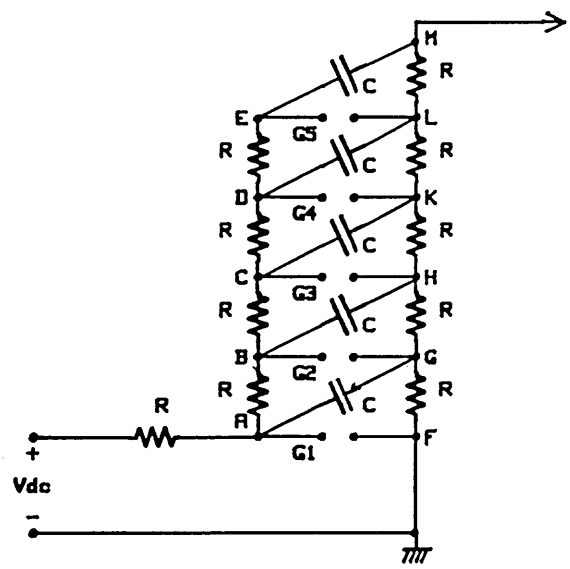


Figure 3.2. Basic circuit of a five-stage impulse generator.

The stage capacitors C are charged in parallel through high value charging resistors R. At the end of the charging period, the points A, B, C, D, E will be at the potential of the D.C. source, say $+ V_{CH}$ with respect to earth, and points F, G, H, K, L, M will remain at the earth potential. The discharge of the generator is initiated by the breakdown of the spark gap A-F which triggers the simultaneous breakdown of all the remaining gaps. The potential at point M attains a value of $- 5 V_{CH}$, i.e., the charging voltage

multiplied by the number of stages with opposite polarity.

Once the impulse generator is discharged, the fault will break down, however, this may take some time, as stated in section 1.2. If the ionization delay is such that the fault does not arc until the reflected wave from the far end has passed the fault point, the reflected wave will be "trapped" between the measuring point and the fault, where it will propagate together with the wave produce by the fault break-down. This situation may complicate the resulting waveforms, and is illustrated in the Bewley lattice diagram of figure (3.3)

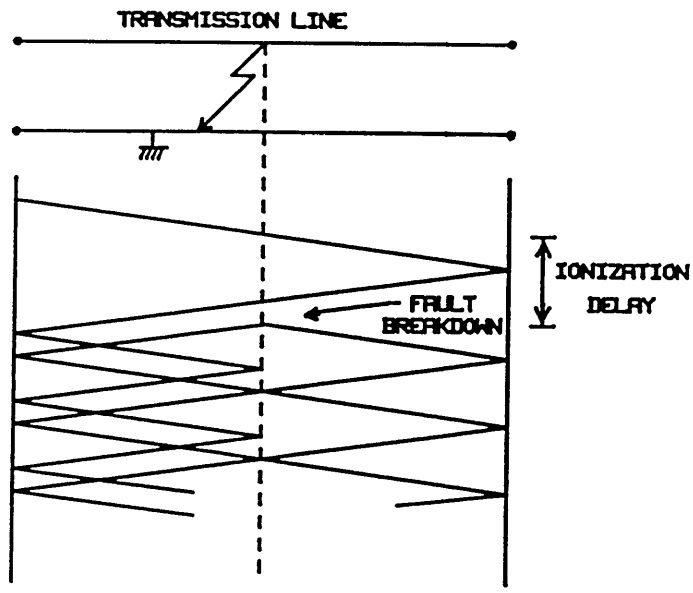


Figure 3.3 Lattice diagram of possible effect of "large" ionization delay.

The test circuit used to evaluate the system performance under this condition is shown in figure (3.4). A capacitor C_1 is charged through resistor R_1; once fully charged, it is discharged on the line by closing switch S_1 (emulating the discharge of an impulse generator). A delay is introduced (115 μs) to allow the wave to reach the far end, be reflected and pass the fault point. Switch S_2 is then closed. The recording of data is initiated by choosing the current wave as trigger signal and fixing the trigger level to an adequate value (10 % in this case). Switches S_1 and S_2 are V-MOS transistors with a maximum R_{DS} of 3Ω, $V_{GS(Th)}$ = 1.7 volts and rise and fall times of 5 ns. maximum.

They are driven by two pulse generators. Resistor R_2 is introduced to accentuate the reflections in the recorded waveforms as stated in Section 2.2.3. A large number of the plots of voltage, current and criteria function were produced. Only two of them are shown in figures (3.7) and (3.8). The results obtained are given in table (3.2).

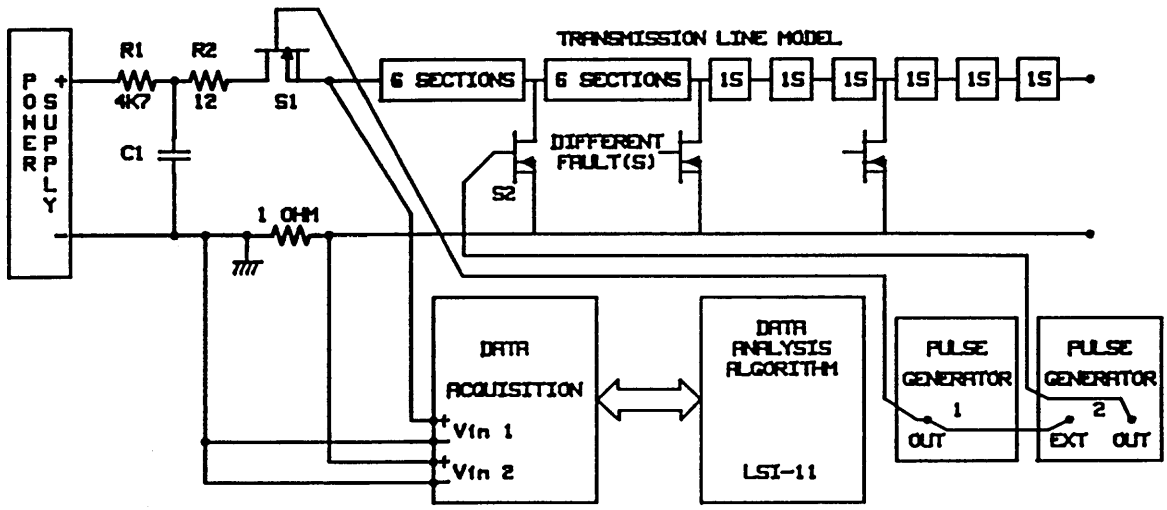
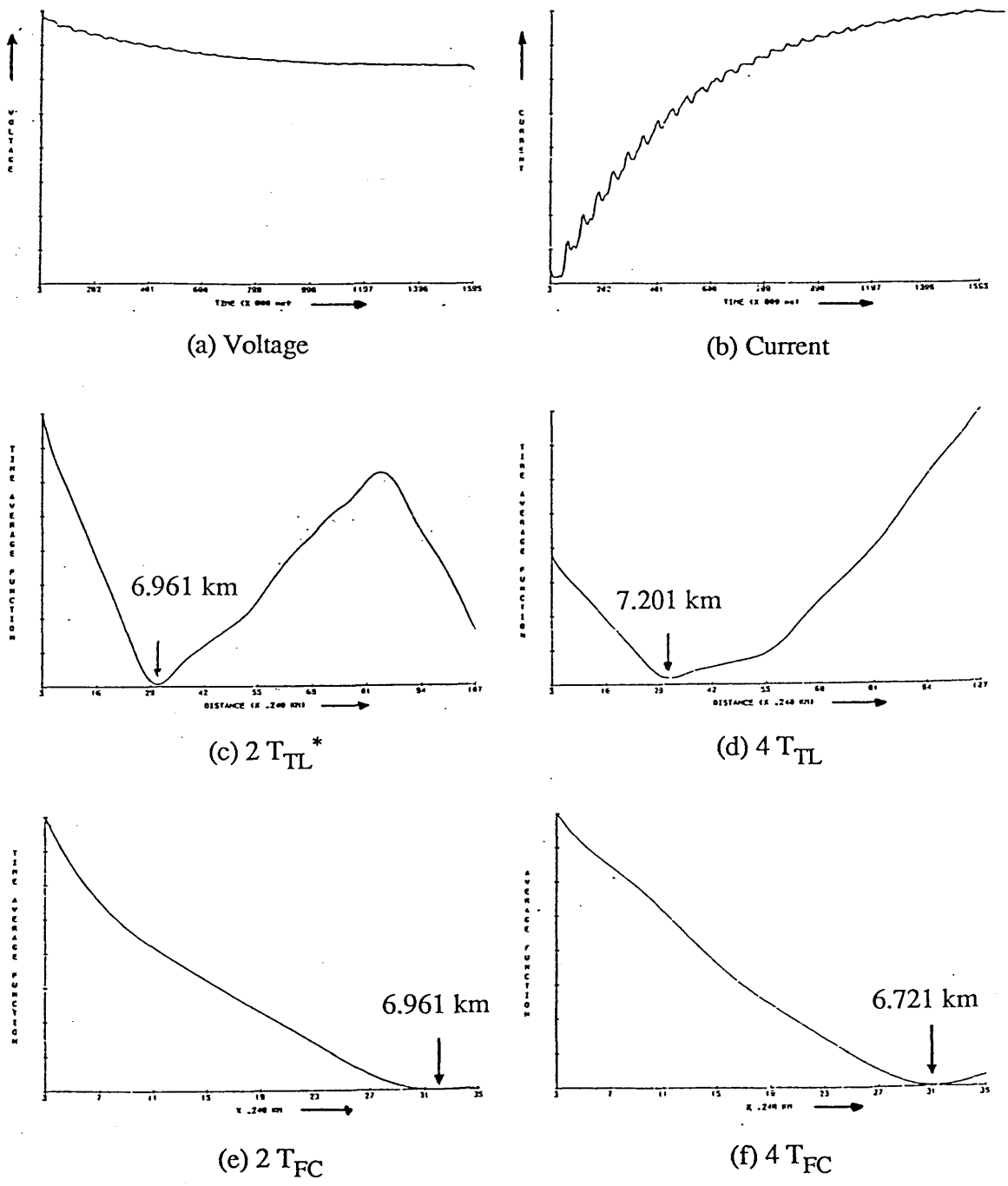


Figure 3.4. Test circuit for "large" ionization delay using the transmission line model.



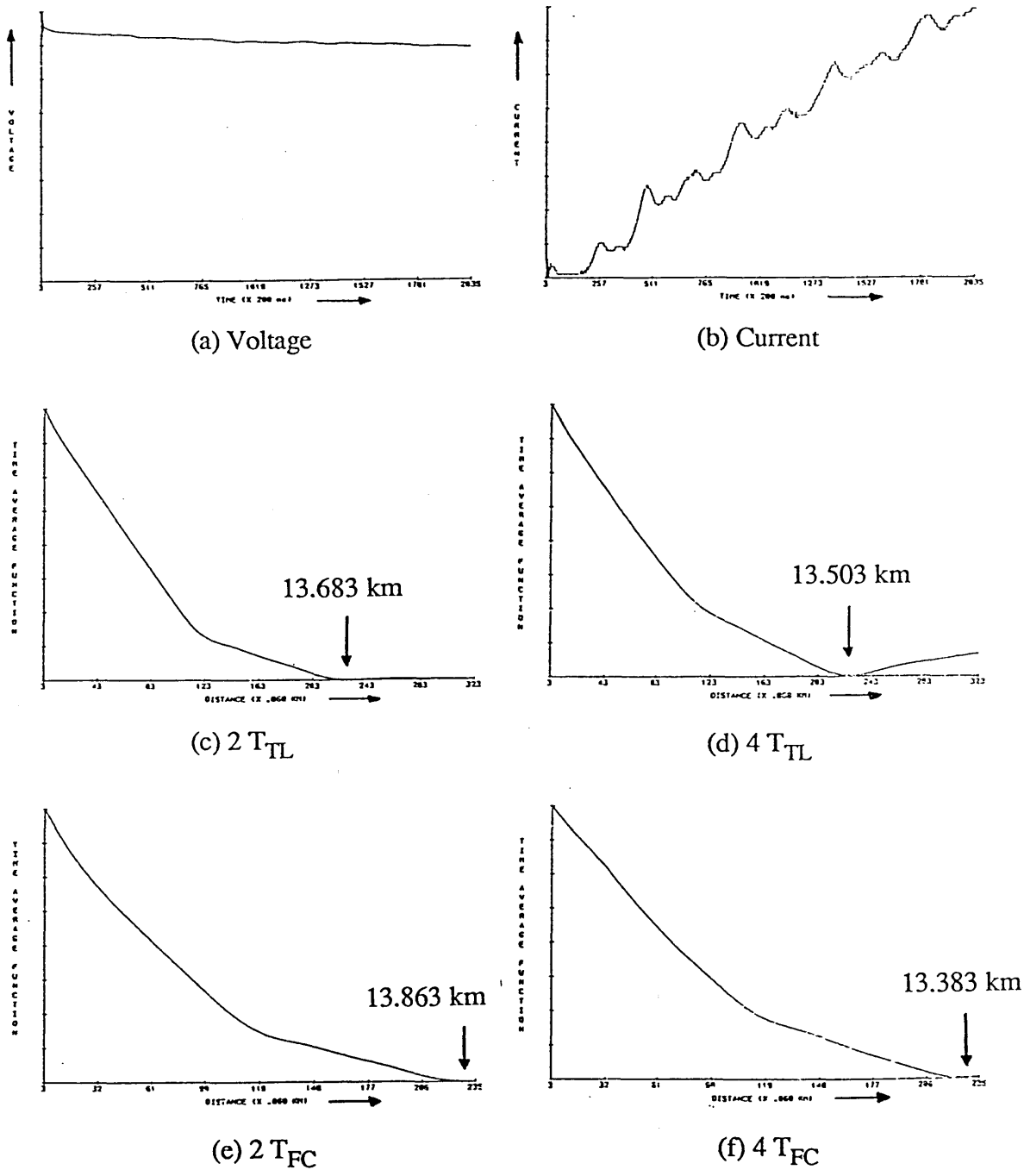
(a) Voltage (b) Current

(c) 2 T_{TL}* (d) 4 T_{TL}

(e) 2 T_{FC} (f) 4 T_{FC}

Figure 3.5. Voltage and current waveforms, and criteria function obtained by injecting a pulse to a transmission line model. Sampling frequency = 1.25 MHz. Fault at 6.437 km.

* In figures (3.5) to (3.8), T_{TL} stands for "transit time for the total length of the line" and T_{FC} stands for "transit time from the measuring point to the fault considered".

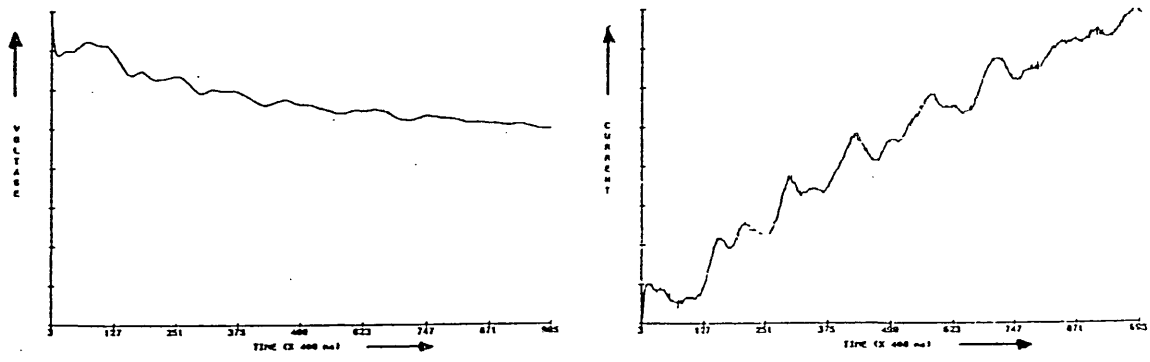


(a) Voltage (b) Current

(c) 2 T_{TL} (d) 4 T_{TL}

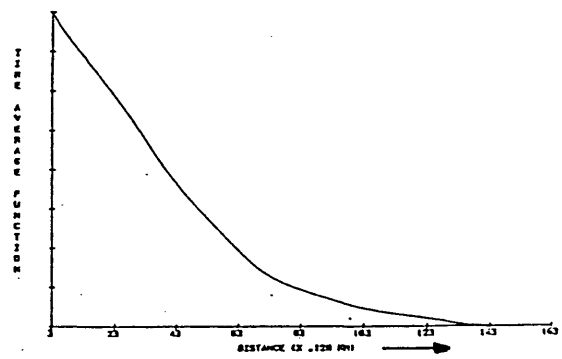
(e) 2 T_{FC} (f) 4 T_{FC}

Figure 3.6. Voltage and current waveforms, and criteria function obtained by injecting a pulse to a transmission line model. Sampling frequency = 5 MHz. Fault at 12.874 km.

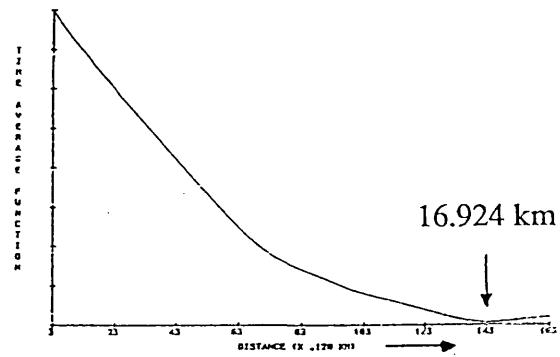


(a) Voltage

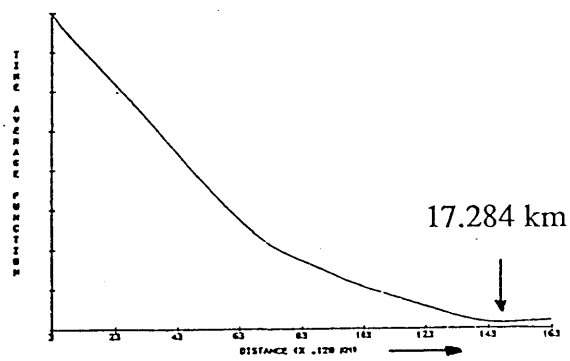
(b) Current



(c) 2 T_{TL}

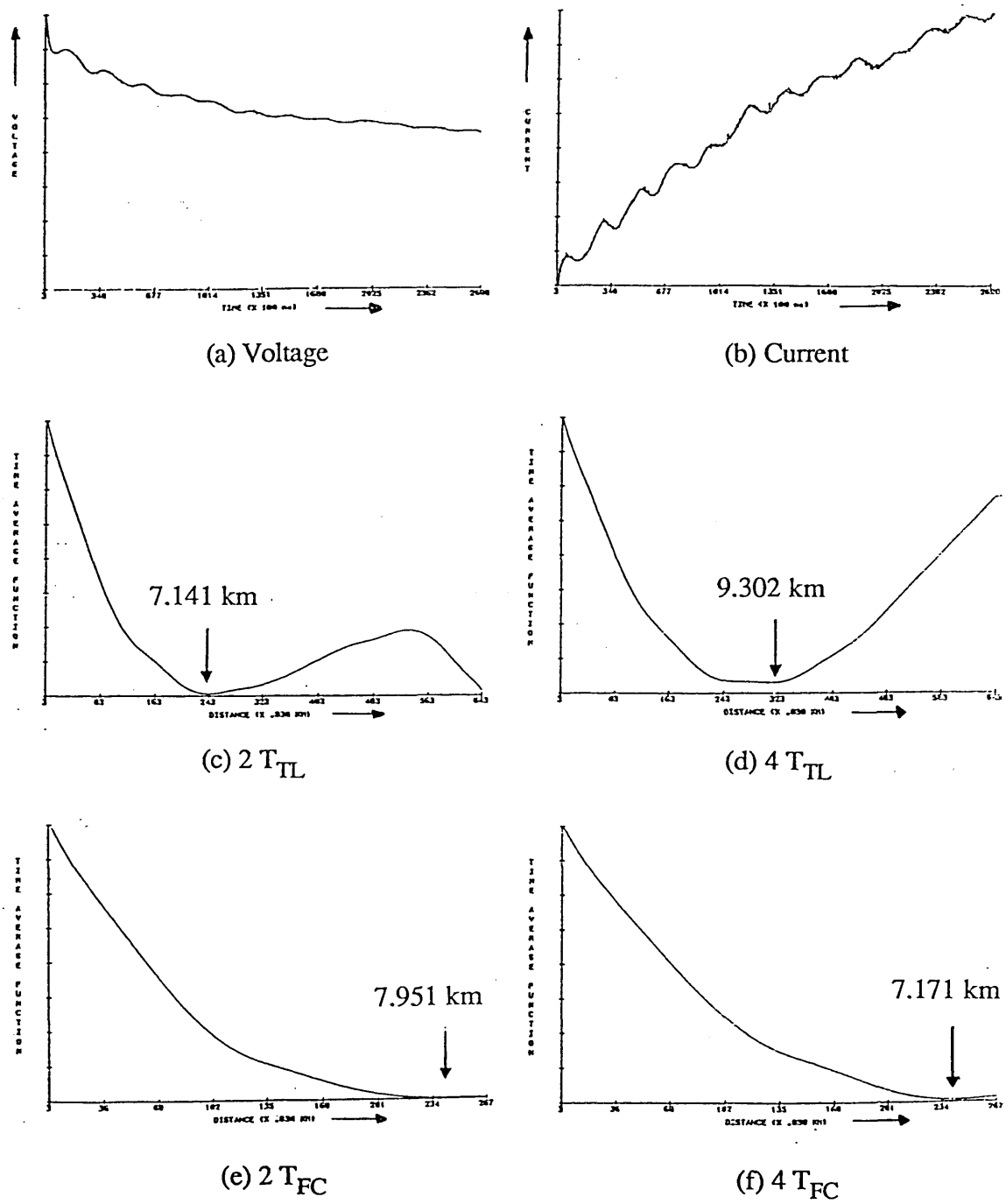


(d) 4 T_{TL}



(e) 6 T_{TL}

Figure 3.7. Voltage and current waveforms, and criteria function obtained by injecting a pulse to a transmission line model including the ionization delay and reflected wave effects. Sampling frequency = 2.5 MHz. Fault at 16.093 km.



(a) Voltage (b) Current

(c) 2 T_{TL} (d) 4 T_{TL}

(e) 2 T_{FC} (f) 4 T_{FC}

Figure 3.8. Voltage and current waveforms, and criteria function obtained by injecting a pulse to a transmission line model including the ionization delay and reflected wave effects. Sampling frequency = 10 MHz. Fault at 6.437 km.

SAMP. FREQ.	DISTANCE FOUND [Km.]			
1.25 MHz.	6.961	7.201	6.961	6.721
2.5 MHz.	6.961	7.441	7.441	7.081
5.0 MHz.	7.021	7.381	_	7.021
10.0 MHz	7.141	7.381	_	7.141
WINDOW	$2\,T_{TL}$	$4\,T_{TL}$	$2\,T_{FC}$	$4\,T_{FC}$

a) Actual point of fault 6.437 Km.

SAMP. FREQ.	DISTANCE FOUND [Km.]			
1.25 MHz.	13.203	13.443	13.443	13.203
2.5 MHz.	13.443	13.443	13.563	13.323
5.0 MHz.	13.683	13.503	13.863	13.383
10.0 MHz	13.683	13.503	13.893	13.413
WINDOW	$2\,T_{TL}$	$4\,T_{TL}$	$2\,T_{FC}$	$4\,T_{FC}$

b) Actual point of fault 12.874 Km.

SAMP. FREQ.	DISTANCE FOUND [Km.]		
1.25 MHz.	17.284	16.804	16.804
2.5 MHz.	17.404	16.804	17.044
5.0 MHz.	17.404	16.803	17.044
10.0 MHz	_	16.594	_
WINDOW	$2\,T_{TL}$	$4\,T_{TL}$	$6\,T_{TL}$

c) Actual point of fault 16.093 Km.

Table 3.1. Results obtained by injecting a pulse to a transmission line model with different points of fault along the line. The blank boxes mean that "the fault could not be located".

SAMP. FREQ.	DISTANCE FOUND [Km.]			
1.25 MHz.	7.201	9.362	_	7.201
2.5 MHz.	7.201	9.482	_	7.201
5.0 MHz.	7.201	9.362	_	7.261
10.0 MHz	7.141	9.302	7.951	7.171
WINDOW	$2\,T_{TL}$	$4\,T_{TL}$	$2\,T_{FC}$	$4\,T_{FC}$

a) Actual point of fault 6.437 Km.

SAMP. FREQ.	DISTANCE FOUND [Km.]			
1.25 MHz.	13.683	13.683	_	13.443
2.5 MHz.	13.683	13.683	13.683	13.443
5.0 MHz.	13.503	13.563	13.503	13.383
10.0 MHz	_	13.563	13.563	13.383
WINDOW	$2\,T_{TL}$	$4\,T_{TL}$	$2\,T_{FC}$	$4\,T_{FC}$

b) Actual point of fault 12.874 Km.

SAMP. FREQ.	DISTANCE FOUND [Km.]		
1.25 MHz.	_	16.804	17.284
2.5 MHz.	_	16.924	17.284
5.0 MHz.	_	16.893	17.284
10.0 MHz	17.084	16.954	_
WINDOW	$2\,T_{TL}$	$4\,T_{TL}$	$6\,T_{TL}$

c) Actual point of fault 16.093 Km.

Table 3.2. Results obtained by injecting a pulse to a transmission line model with different points of fault along the line and considering the effect of the ionization delay. The blank boxes mean that "the fault could not be located".

3.1.3 ACCURACY ANALYSIS.

As discussed in section 2.3.1 the expected fault distance obtained by the particular fault location method under consideration is a multiple of the distance discretization interval Δx, the best result being the nearest multiple of Δx to the actual distance. The discretization interval Δx depends on the wave propagation velocity along the line, $1/\alpha$, and on the sampling interval Δt. Since the propagation velocity is considered constant, Δx depends only on Δt.

$$\Delta x = \Delta t/\alpha \qquad ; \qquad \alpha = \sqrt{[LC]}$$

Considering the propagation velocity associated with the transmission line model used and the different sampling frequencies applied during the tests, the values of the discretization interval Δx, are given in table 3.3.

fs [MHz]	Δt [ns]	Δx [m]
1.25	800	240
2.5	400	120
5	200	60
10	100	30

Table 3.3 Discretization interval Δx values for different Δt values for line model.

The nearest multiples of Δx for the fault distances considered and the sampling frequencies applied during the tests are given in table 3.4.

An examination of tables 3.1 and 3.2 reveals that the accuracy of the results varies widely with both, sampling frequency and data window length. The minimum theoretical data window length corresponds to two times the wave transit time from the measuring point to the point of fault. This data window would contain information about the first reflection only, and should be, at least in principle, sufficient to locate the fault, however, the results obtained suggest that this data window length is not enough to locate the fault,

as indicated by the time average function plots obtained, where the minimum point is weakly defined, and in several of them not defined at all. This last condition corresponds to the blank boxes in tables 3.1 and 3.2 where the fault could not be located.

Actual Fault Distance [km]	Nearest Δx multiple [km]			
6.487	6.48	6.48	6.48	6.48
12.874	12.96	12.84	12.9	12.87
16.093	16.08	16.08	16.08	16.08
Sampling frequency [MHz]	1.25	2.5	5	10

Table 3.4 Nearest multiples of Δx for the fault distances considered.

As the data window is increased two facts can be observed: the point of minima in the time average function is more sharply defined, thereby, a distance to the fault is always obtained, and the accuracy of the distance tends to improve over the previous one. Such is the case for a data window of four transit times from the measuring point to the point of fault.

One would expect that increasing further the data window length would improve the accuracy further as well, however, this is not the case as can be observed from the plots and results for a data window equal to 2 and 4 times the transit time from the measuring point to the far end of the line. Even though the point of minima is well defined in most of the cases, the accuracy tends to worsen in all of them. This may be explained as follows: as stated in section 2.2.2, as a wave travels along a transmission line it is attenuated and distorted causing the new generated reflections to be less pronounced and more smoothed than the older ones. In general, the longer the data window, the more attenuation in reflections and distortion of the waveform it will contain, affecting adversely the fault related "information" contained in it and therefore, the accuracy in the distance to the fault obtained. From the above considerations it may be said that by experimentation, it was found that the "best" data window length corresponds to four times the transit time from the measuring point to the point of fault.

Restricting the discussion to those results obtained for this data window length, it

can be seen from tables 3.1 and 3.2, that the best result obtained corresponds to an accuracy of 1.7% of the total length of the line and the worst to 4.45%. None of the results falls within the theoretical accuracy which corresponds to 1.26% for a sampling frequency equal to 1.25 MHz and to 0.157% for 10 MHz (see tables 3.3 and 3.4) given the total length of line equal to 19.312 km (it should be noted that the theoretical accuracy mentioned above only includes the quantization error). Since the fault location method under consideration assumes a distributed parameter line model, that is, the telegraph equations, it seems reasonable to expect some error due to the lumped nature of the physical line model used. With 18 "π" sections intuitively one might expect errors of the order of 1 part in 18 or 5% . It may be fortuitous that actual errors are in this range, but the figures tend to suggest some correlation between the inaccuracy of the physical model and the errors in the results.

3.2 TESTS AND RESULTS FOR A COAXIAL CABLE.

The objective of carrying out tests in a coaxial cable was to assess the performance of the system when dealing with a real distributed parameter transmission line, according with the mathematical model used by the fault location method under consideration, and to investigate the effect of the variation of the cable parameter values with frequency on the fault location accuracy, since the mathematical model assumes these parameters to be constant.

3.2.1 INJECTING A PULSE.

As before the procedure was to inject a pulse, record input voltage and current and analyse these data to obtain the distance to the fault. The circuit diagram for the test circuit is shown in figure (3.9).

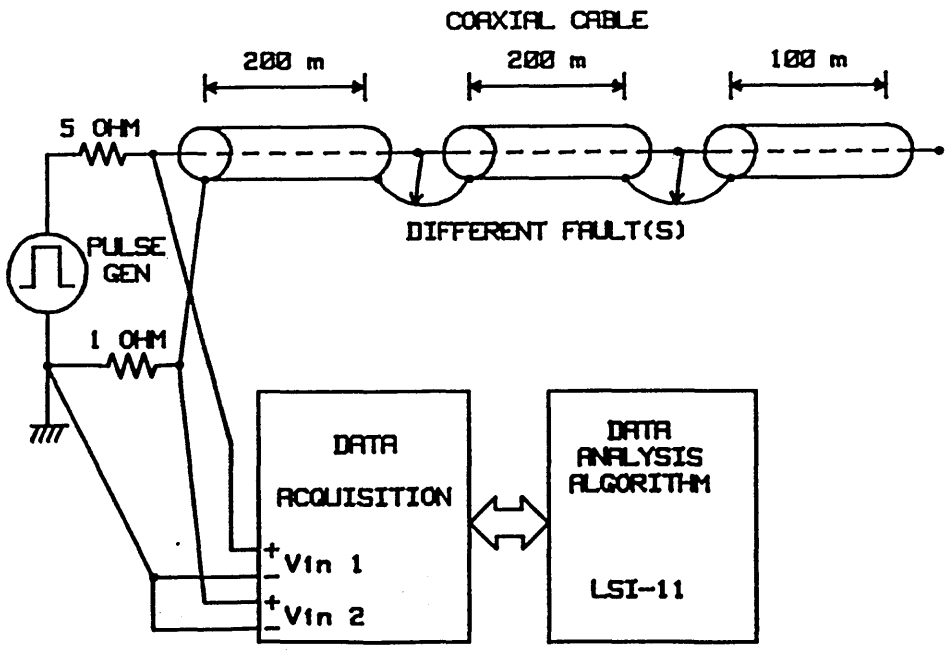


Figure 3.9. Injecting a pulse to a coaxial cable, test circuit.

The coaxial cable used was the standard uniradio number M202 with a characteristic impedance of 75Ω. It is well known that the value of distributed parameters varies with frequency [27] , however, single parameter values are needed since the fault location method used assumes constant parameter values.

The frequency involved is not a single one but the continuous spectrum of voltage and current waveforms generated by the injection of the interrogating signal into the faulty line, however, this spectrum will have a dominant frequency component with a period of approximately twice the propagation time from the source to the fault [20]. This dominant frequency is a function of the distance to the fault and it is expected to shift towards higher frequency when the distance to the fault decreases.

Two typical sets of voltage and current waveforms (for faults at 0.4 km. and 0.2 km. respectively) were Fourier transformed in order to find their power spectrum and obtain the dominant frequency. The power spectra obtained are shown in figure (3.10) . From the power spectra the dominant frequencies were found to be :

$$f_{D\,/\,0.2\ km} = 406.25\ KHz. \quad , \quad f_{D\,/\,0.4\ km} = 312.5\ KHz.$$

These frequencies were used to calculate the value of the parameters of the cable. For a coaxial cable with the following physical and geometrical properties :

$a = 0.4 \times 10^{-3}$ m (Internal conductor radius)

$b = 1.625 \times 10^{-3}$ m (Internal radius, external conductor)

$c = 1.875 \times 10^{-3}$ m (External radius, external conductor)

σ_c = copper conductivity = 5.80×10^{-7} mhos/m

$\mu = \mu_o\ \mu_R$ = copper permeability = 1.25×10^{-6} H/m

$\varepsilon = \varepsilon_o\ \varepsilon_D$ = Dielectric permitivity = 20.01×10^{-12} F/m

The values of the parameters are given by [28]

$$R = \frac{1}{\sigma_c\, 2\pi\, \delta} \left(\frac{1}{a} + \frac{1}{b} \right)$$

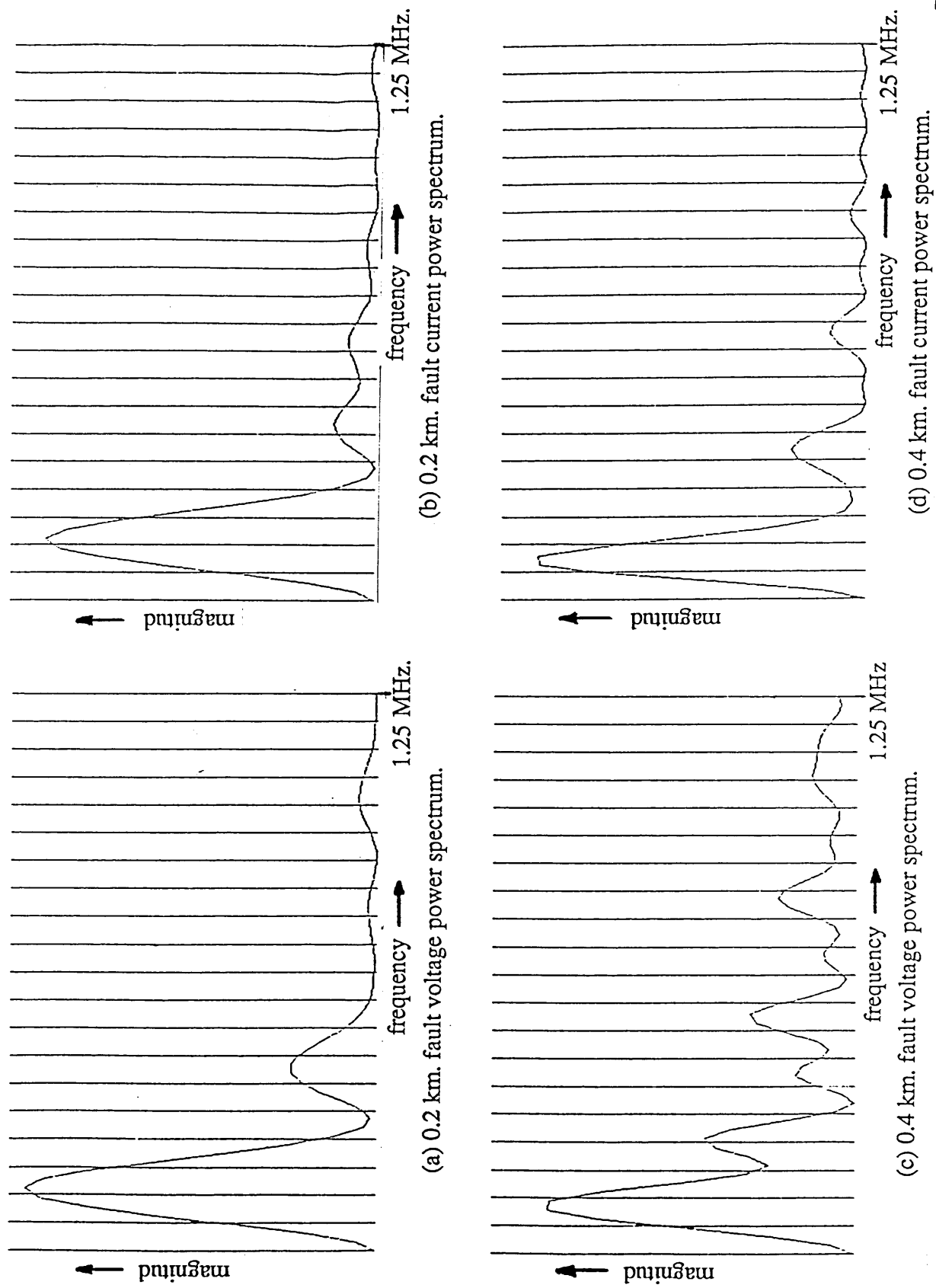


Figure 3.10. Power spectra of typical voltage and current fault waveforms.

$$L = \frac{\mu}{2\pi}\left[\ln\frac{b}{a} + \frac{\delta}{2}\left(\frac{1}{a}+\frac{1}{b}\right)\right]$$

$$C = \frac{2\pi\varepsilon}{\ln(b/a)}$$

where δ is the depth of penetration or skin depth and is given by:

$$\delta = \frac{1}{\sqrt{[\pi f \mu \sigma]}} \quad [m]$$

for copper this expression reduces to:

$$\delta = \frac{0.0661}{\sqrt{[f]}} \quad [m]$$

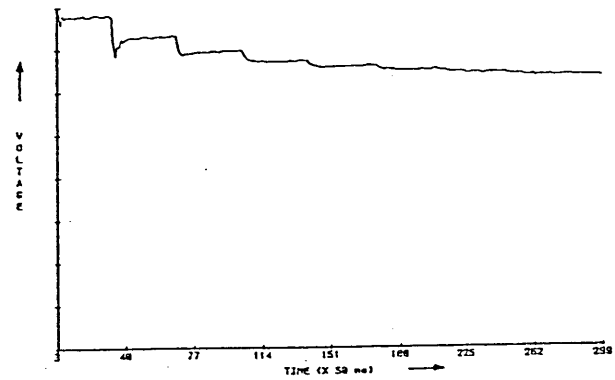
where f is given by the dominant frequency.
The parameter values calculated are as follows, for the 0.2 km fault :

$R = 82.43 \quad \Omega/km$
$L = 312.53 \times 10^{-6} \quad H/km$
$C = 89.68 \times 10^{-9} \quad F/km$

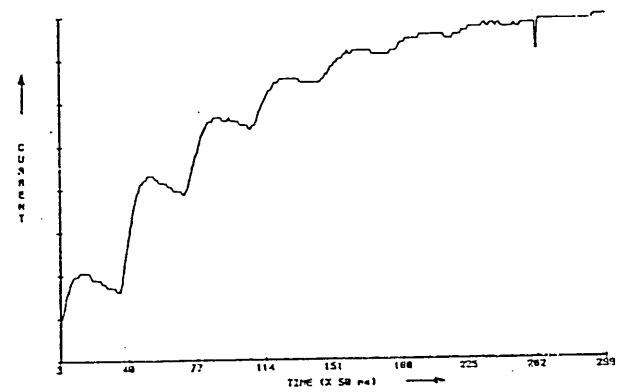
for the 0.4 km fault

$R = 72.29 \quad \Omega/km$
$L = 317.05 \times 10^{-6} \quad H/km$
$C = 89.68 \times 10^{-9} \quad F/km$

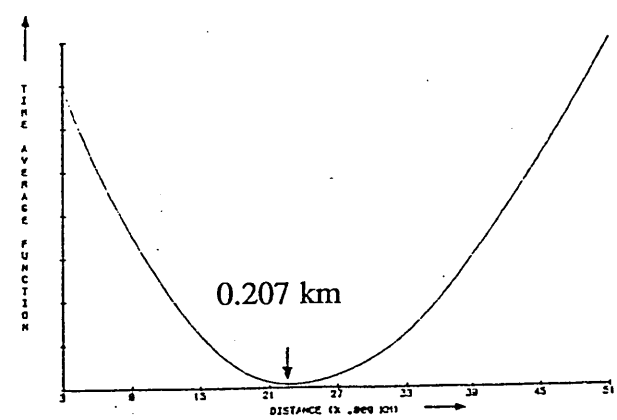
Due to the short length of the cable only one sampling frequency was used, 20MHz. Two points of fault were considered, 200 m. and 400 m. The length of data window used was slightly bigger than 4 wave transit times from the measuring point to the point of fault considered since, by experience, this data window length was found to be the more suitable (see section 3.1.3). Plots of voltage, current and criteria function are shown in figures (3.11) and (3.12) the results obtained are given in table (3.5), page 119.



(a) Voltage

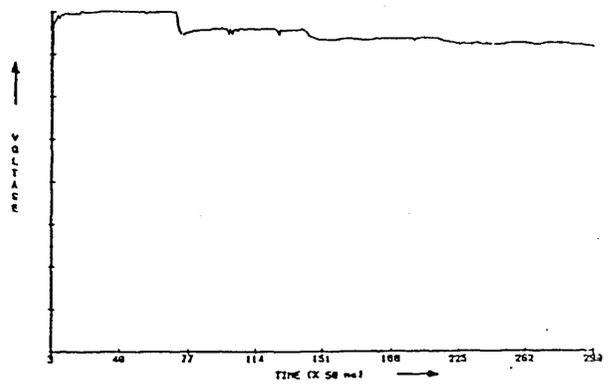


(b) Current

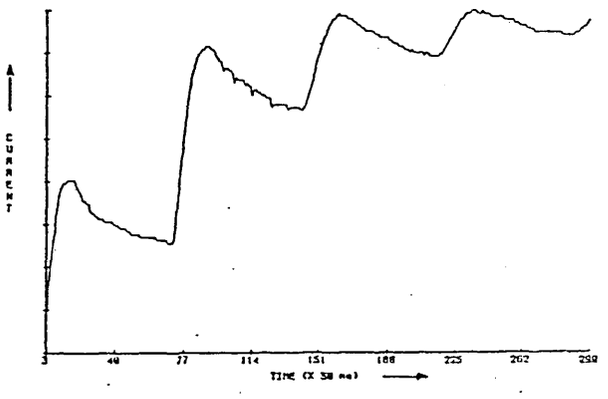


(c) Criteria function

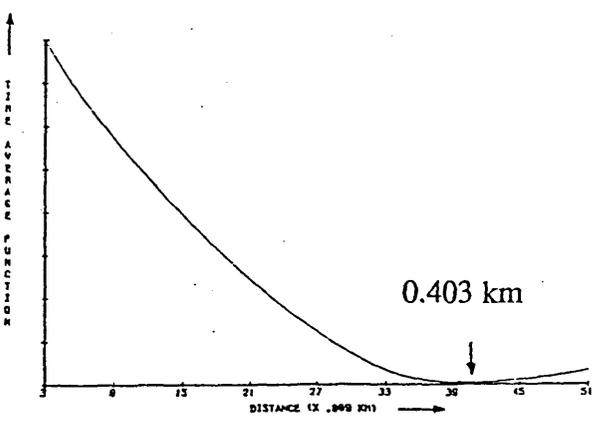
Figure 3.11. Input voltage and current, and criteria function for a 0.2 km. fault obtained by injecting a pulse to a coaxial cable.



(a) Voltage



(b) Current



(c) Criteria function

Figure 3.12. Input voltage and current, and criteria function for a 0.4 km. fault obtained by injecting a pulse to a coaxial cable.

3.2.2 INJECTING A PULSE TO FORCE THE FAULT TO ARC WITH IONIZATION DELAY.

The test described in section 3.1.2 was performed on the coaxial cable. The sampling frequency, points of fault and length of data window used were the same as in section 3.2.1. The test circuit is shown in figure (3.13).

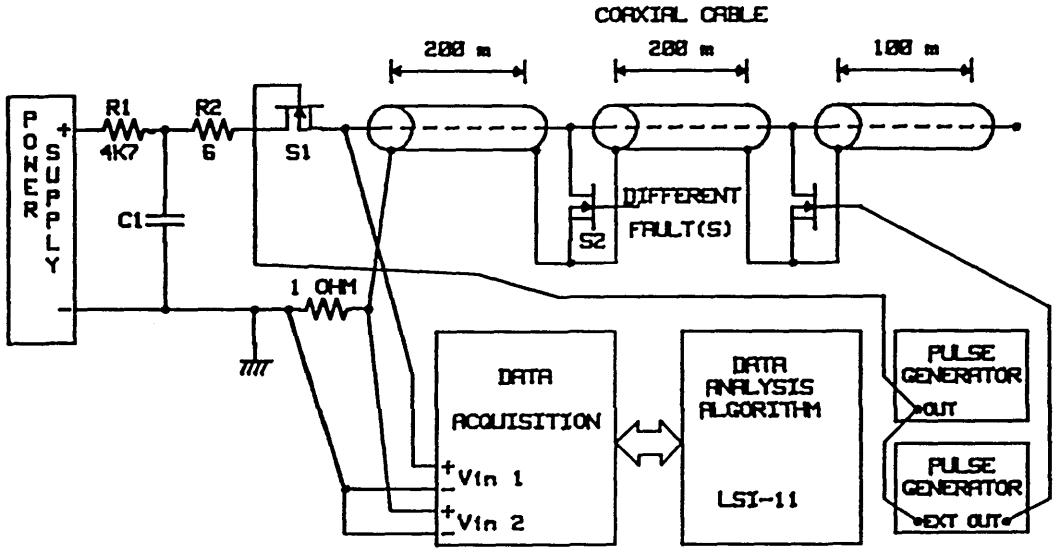


Figure 3.13. Test circuit for large ionization delay using a coaxial cable.

Under these tests, two ionization delays were considered:

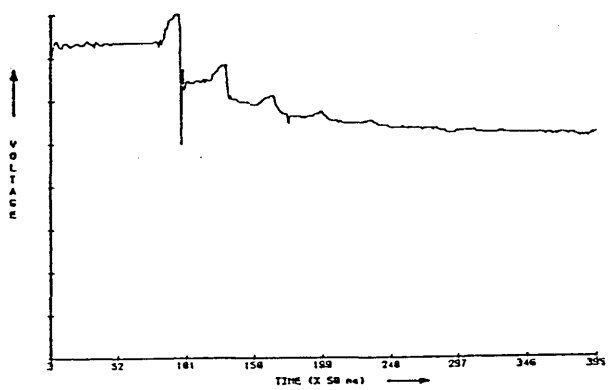
a) Ionization delay 1.- The first corresponds to a ionization delay which allows the reflected waveform from the far end to reach the measuring point and be reflected again.

b) Ionization delay 2.- The second is similar to that treated in section 3.1.2, i.e., the fault arcs when the reflected waveform from the far end is between the measuring point and the fault point.

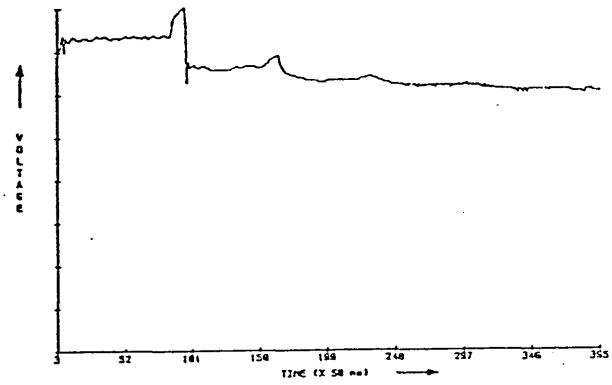
The voltage, current and criteria function plots are shown in figures (3.14) and (3.15). The results are shown in table (3.5).

It should be noted that under this conditions the voltage and current waveforms recorded include " information " which is not directly related with the fault, i.e., the initial

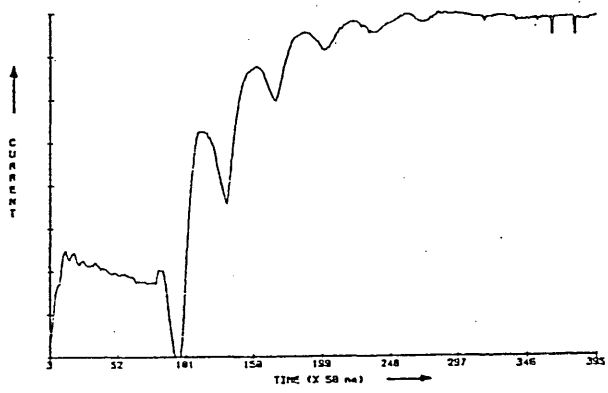
part of the waveform. By appropriately adjusting the trigger level facility in the acquisition system of the fault locator, the waveforms produced on fault breakdown only can be recorded and used as initial data. The voltage and current waveforms recorded and the criteria function plots thus obtained are shown in figures (3.16) and (3.17). The results are shown in table (3.5).



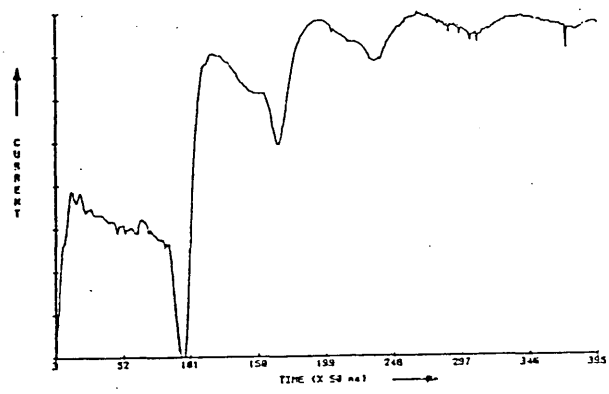
(a) Voltage



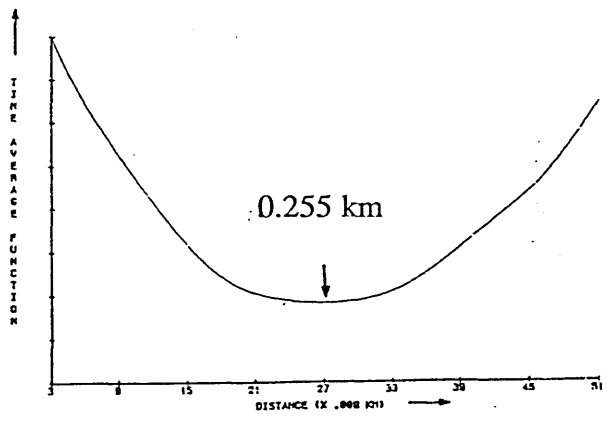
(a) Voltage



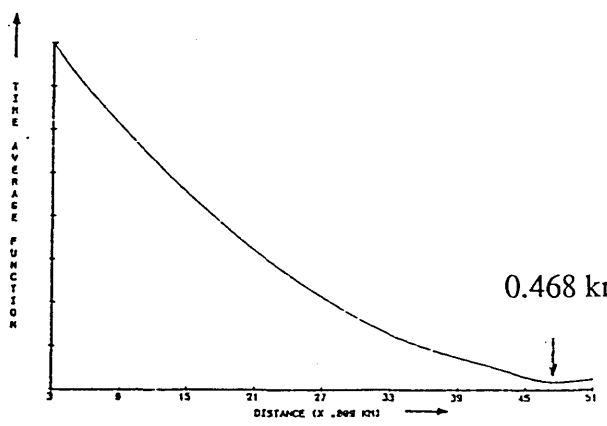
(b) Current



(b) Current



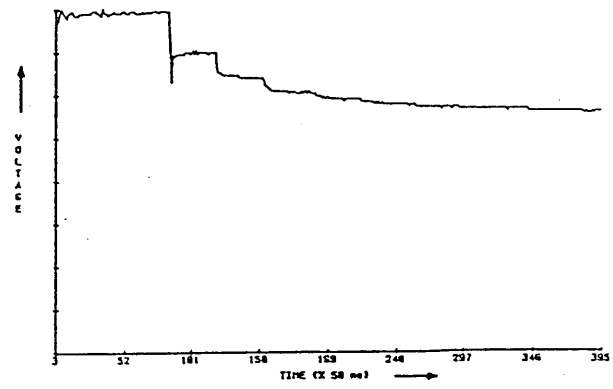
(c) Criteria function



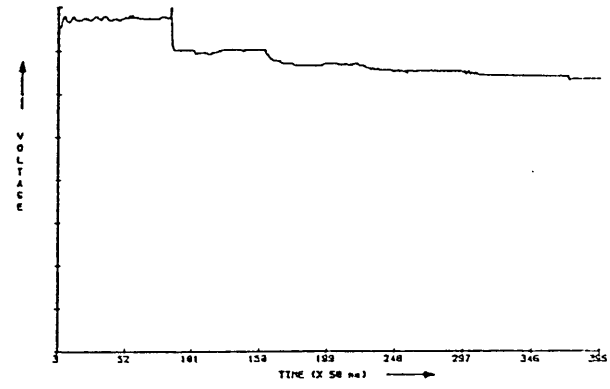
(c) Criteria function

(a) *(b)*

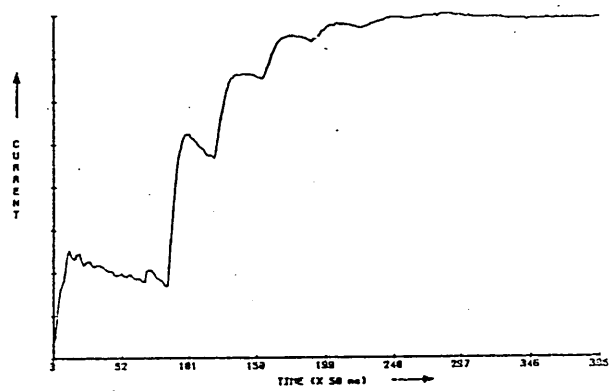
Figure 3.14. Input voltage and current, and criteria function for: a) 0.2 km. and b)0.4 km. faults considering the effect of ionization delay 1.



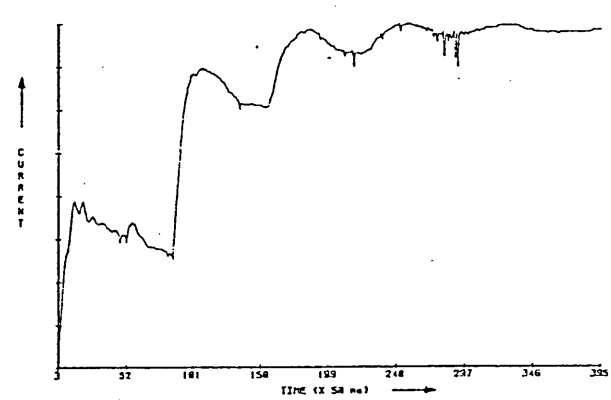
(a) Voltage



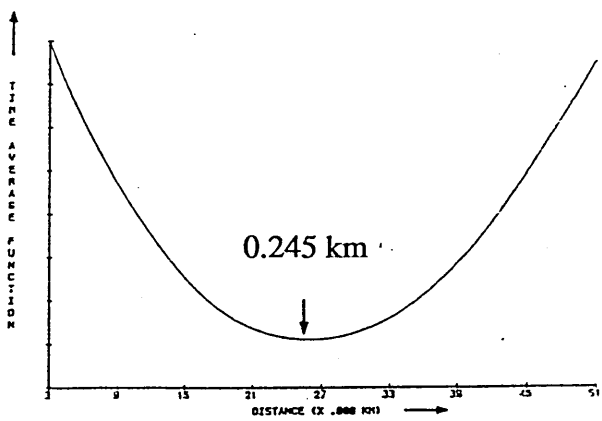
(a) Voltage



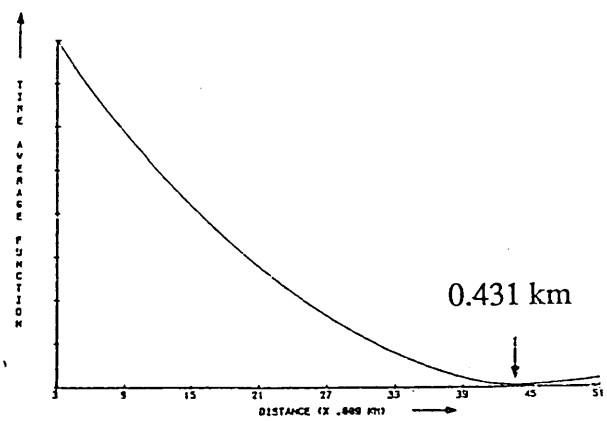
(b) Current



(b) Current



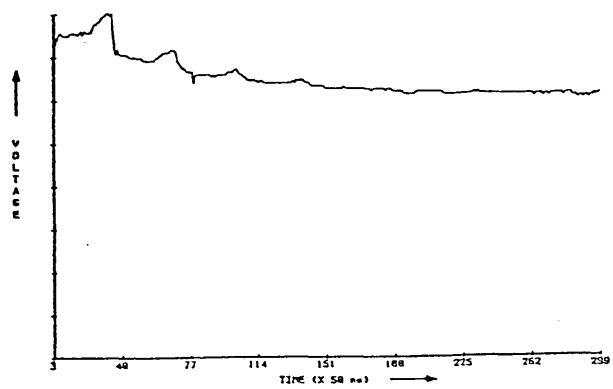
(c) Criteria function



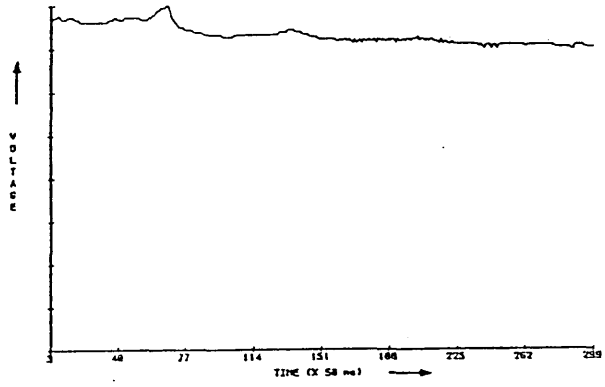
(c) Criteria function

(a) *(b)*

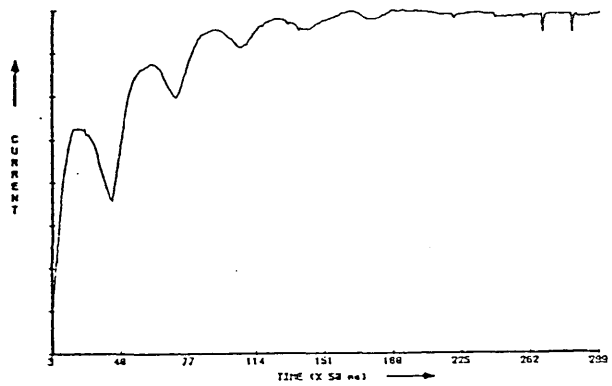
Figure 3.15. Input voltage and current, and criteria function for: a) 0.2 km. and b) 0.4 km. faults considering the effect of ionization delay 2.



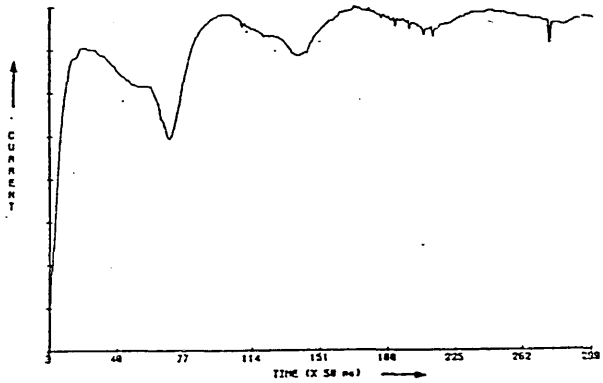
(a) Voltage



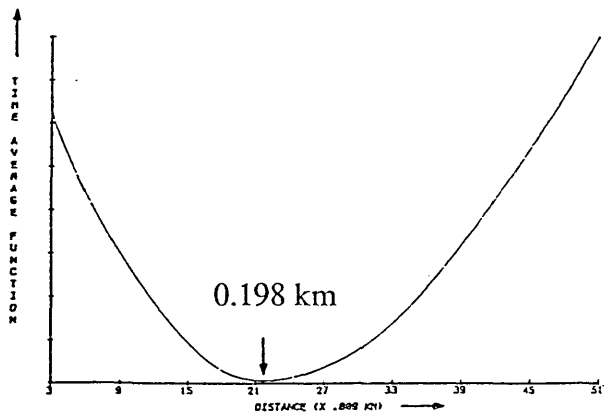
(a) Voltage



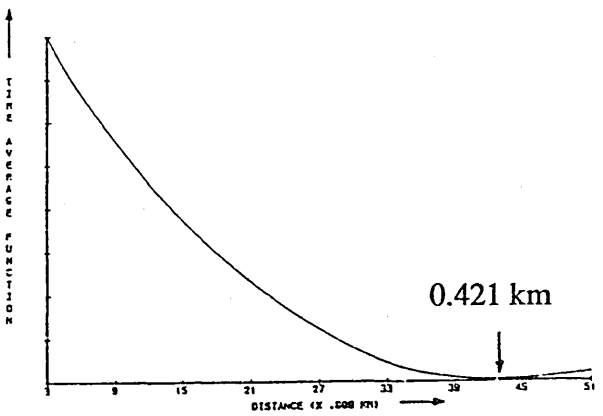
(b) Current



(b) Current



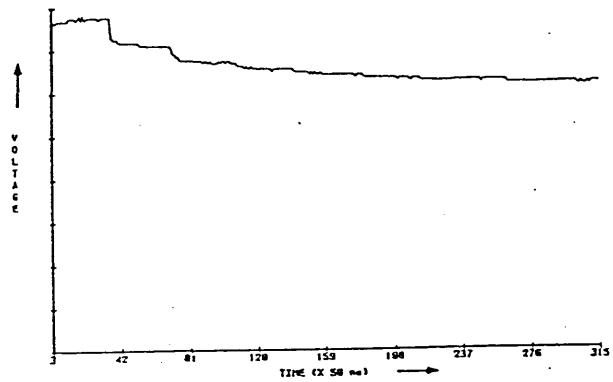
(c) Criteria function



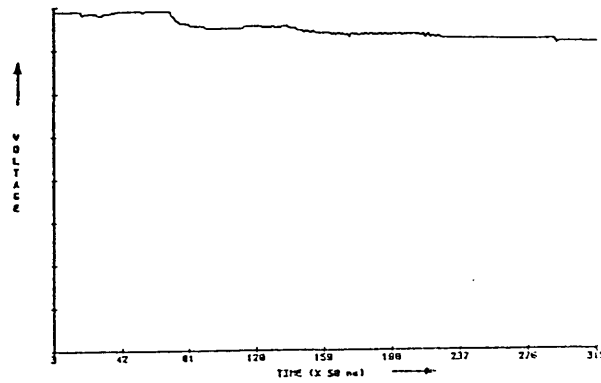
(c) Criteria function

(a) *(b)*

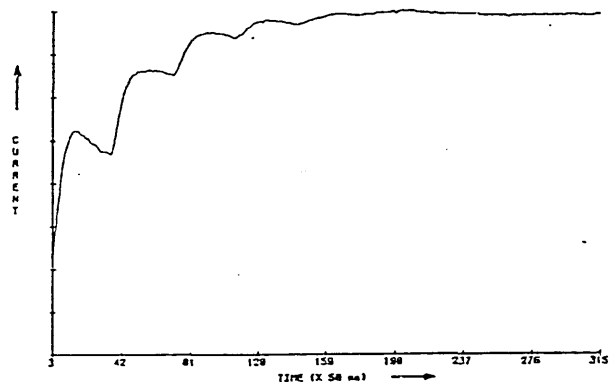
Figure 3.16. Input voltage and current, and criteria function for: a) 0.2 km. and b) 0.4 km. faults omitting the initial part of the waveforms due to ionization delay 1.



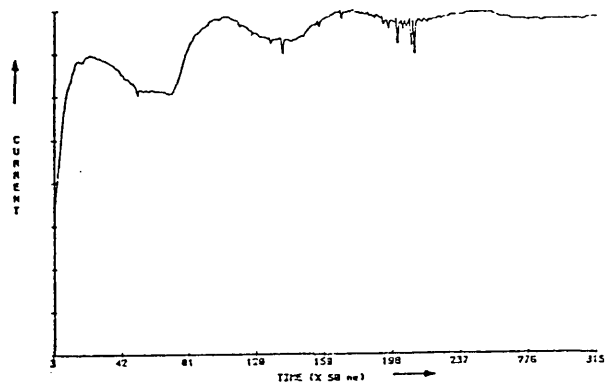
(a) Voltage



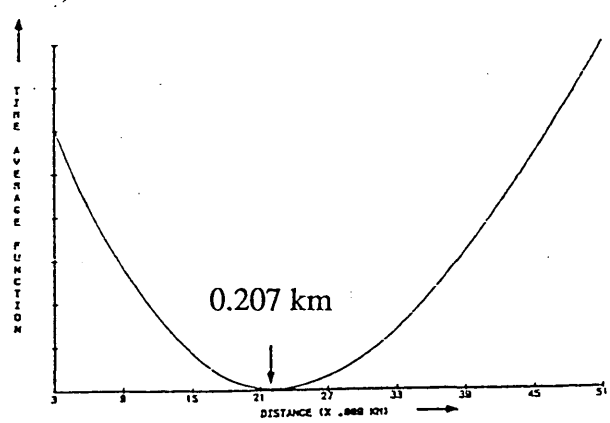
(a) Voltage



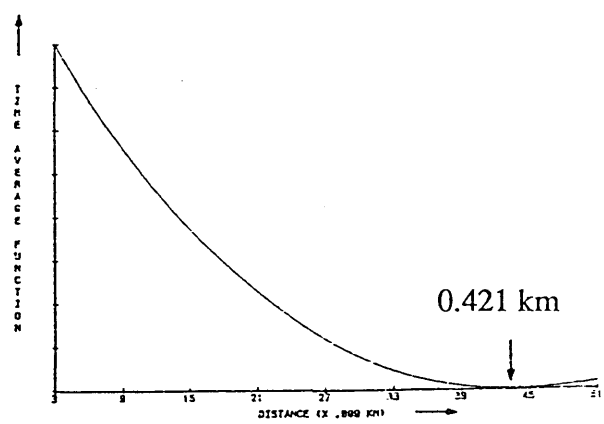
(b) Current



(b) Current



(c) Criteria function



(c) Criteria function

(a) *(b)*

Figure 3.17. Input voltage and current, and criteria function for: a) 0.2 km. and b) 0.4 km. faults omitting the initial part of the waveforms due to ionization delay 2.

	Samp. Freq.	Distance Found	Actual Fault Position
Injecting a Pulse	20 MHz	0.207	0.200
	20 MHz	0.403	0.400
Ionization Delay 1	20 MHz	0.255	0.200
	20 MHz	0.468	0.400
Ionization Delay 2	20 MHz	0.245	0.200
	20 MHz	0.431	0.400
Omitting Ionization Delay 1	20 MHz	0.198	0.200
	20 MHz	0.421	0.400
Omitting Ionization Delay 2	20 MHz	0.207	0.200
	20 MHz	0.421	0.400

Table 3.5. Results obtained by using a coaxial cable.

3.2.3. ACCURACY ANALYSIS.

Considering the wave propagation velocity obtained from the computed parameter values for the coaxial cable and the sampling frequency applied during these tests, the values for the discretization interval Δx are as shown in table 3.6.

fs [MHz]	Δt [ns]	Fault at [km]	Δx [m]
20	50	0.2	9.44
20	50	0.4	9.3

Table 3.6 Discretization interval values for faults on a coaxial cable at 0.2 km and 0.4 km.

The nearest multiples of Δx for the fault distances considered and the frequency applied are given in table 3.7.

Actual Distance [km]	Nearest Δx multiple [km]
0.2	0.198
0.4	0.403

Table 3.7. Nearest Δx multiplies to actual fault distances for 0.2 km. and 0.4 km. faults.

Table 3.5 shows the results obtained for tests using a coaxial cable. These results corresponds to three different situations, that is, those obtained by injecting a pulse, those obtained by considering the effect of ionization delays 1 and 2 and those which omit this effect.

The ionization delay effect corresponds to the initial part of the voltage and current

waveforms shown in figures (3.14) and (3.15). It strongly affects the shape of these waveforms and consequently affects the accuracy of the results obtained, as can be seen from table 3.5. Fortunately, the ionization delay effect can be easily avoided by setting the trigger level and posttrigger features to adequate levels (40% and 90% respectively in this case). The voltage and current waveforms produced on fault breakdown only can be recorded and used a initial data. It should be noted that waveforms recorded under the condition effectively do not include the ionization delay effect, but they still include the effect introduced by the reflected wave from the far end (see section 3.1.2).

For the reason given above results obtained by considering the ionization delays 1 and 2 are omitted from the accuracy discussion.

From table 3.5 it can be seen that the best result obtained corresponds to an accuracy of 0.4% of the total length of the cable and the worst to 4.2% .This last result corresponds to the test which included the effect of the reflected waveforms, for a 0.4 km fault. Even though the accuracy figures are similar to those obtained for the physical model of a transmission line, there is an important difference between them, since the results for the coaxial cable correspond more closely with theory (see tables 3.6 and 3.7).

The results obtained by injecting a pulse are encouraging since they exhibit an accuracy of 1.4% for the 0.2 km fault (7 meters error) and 0.6% for the 0.4 km fault (3 meters error). This accuracy is adequate even for the prelocation stage in underground cable fault location where, it can be remembered, an accuracy of $\pm$ 10 meters is desirable. The type of faults involved would be those with zero or low resistance values.

The accuracy obtained from the tests which included the reflected waveform is 0.4% for the 0.2 km fault (2 meters error) and 4.2% for the 0.4 km fault (21 meters error). They show a lack of consistency, reason why they are not considered as good as the previous results. It should be noted, however, that the condition under which this test was carried out, that is, considering the effect of ionization delay and that of the reflected waveform, is, perhaps, the most difficult to cope with.

CHAPTER 4

CONCLUSIONS AND SUGGESTIONS FOR FURTHER WORK

The design, construction and testing of a High Speed Data Acquisition and Analysis System for the investigation of fault location in power system transmission lines and cables have been described. The system offers versatility in its recording modes and can cater for a wide variety of fault induced waveforms. The digital trigger level feature enables it to record useful fault related voltage and current waveforms whether these are produced by injecting an interrogating signal into the line or cable, or by the fault breakdown itself. This feature avoids the need for synchronization between the pulse generator and acquisition system or the need of external signals, such as those generated by protection relays in the on-line case, to start the recording. The posttrigger feature enables information before the trigger to be captured.

The high sampling frequency can cope with the high frequency content characteristic of fault induced voltage and current waveforms and proved to be useful when dealing with very short lines or cables. The amount of memory provided is suitable for line or cable lengths found in the power system distribution level where, in general, line lengths in the order of few tens of kilometers are found.

The analysis of the recorded data is performed by a travelling wave based algorithm which can cope with the high frequency component of fault waveforms and which avoids the need for skillful interpretation of results. From the recorded voltage and current the algorithm generates voltage and current profiles for the rest of the line based on the solution to the telegraph equations. A time average function involving the square of the estimated voltages is used to locate the point of fault.

By experimentation it was found that the "sensitivity" of the algorithm is increased by setting the output impedance of the pulse generator to 10% of the characteristic impedance of the line or cable under test, and by selecting a data window length slightly

bigger than four times the wave transit time from the measuring point to the point of fault.

The overall performance of the system has been assessed with data obtained from a transmission line model and from a real coaxial cable. For the coaxial cable results with an accuracy from 0.6% to 1.4% of the total line length have been obtained for short circuit or low resistance faults. A location accuracy between 0.4% and 4.2% was achieved for the case of high resistance or flashing faults which also included the reflected wave effect.

The accuracy obtained is adequate for fault location of the different faults that occur in overhead transmission lines. It is also adequate for fault prelocation of short circuit or low resistance faults in underground cable. When dealing with high resistance or flashing cable faults the distance to the fault obtained is slightly larger than the one expected from present prelocation methods ($\pm$ 10m). This would mean that the area where the pinpointing stage is to be carried out is slightly larger. This inconvenience would be set against the advantage of the elimination of skillful interpretation of waveforms or results needed in present prelocation methods, and indeed make it possible to locate faults automatically.

The fault locator apparatus developed during the course of this work will enable other workers to gather information on real cables or lines and should provide a useful research tool.

SUGGESTIONS FOR FURTHER WORK.

Since the processing of the data involves only additions and multiplications, the whole facilities offered by a general purpose microcomputer are not needed, the design and construction of a purpose-built processing module based, perhaps, on a 16 bit microprocessor would involve benefits in size and cost. The main function assigned to this new module would be that performed by the LSI-11-23 microcomputer at the moment, i.e., processing the initial voltage and current waveforms in order to obtain the distance to the fault.

The acquisition unit of the fault locator apparatus includes a parallel output port with 8 data lines and 4 control lines, therefore, the interconnection between the acquisition unit and the proposed processing unit would be straightforward.

The computer algorithm described in section 2.10 was written in Fortran. Since the main calculation in the algorithm consists of a loop in which the new values of voltage and current are computed, and this loop only includes multiplications and additions, a saving in computation time would be expected if a version of this algorithm is written in assembly language.

In section 3.2.1 the values of the distributed parameters of the cable were computed for the dominant frequency found from the power spectrum of the voltage and current waveforms. This idea could be implemented as a subroutine and incorporated into the main algorithm in such a way that the "best" value of the line or cable parameters for a particular fault are calculated before the main computation.

The accuracy of the results obtained by injecting a pulse to the coaxial cable was fairly good, however, it would be worth exploring the posibility of improving this accuracy by using interpolation. The approximation of a second or third order polynomial to the points near the minimum of the time average function would be a good start.

The selection of recording parameter values such as attenuation level, posttrigger memory amount, sampling frequency and trigger level is performed by manual operation of the switches and/or knobs located at the front panel. This is adequate for off-line fault location where the fault location equipment is taken to the place where the faulted line is, and the necessary conections are performed by an operator. If the fault location is to be performed on-line, it would be an advantage to perform the setting of the recording parameters through the proposed microprocessor module. The added advantage consists in the possibility to remotely control the setting of these parameters from the control room of the generating plant or substation where the equipment is installed, since it is very likely for the fault locator apparatus to be installed away from the control room.

The modifications to the existing equipment would consist mainly in the inclusion of appropriate latches instead of thumb wheels for posttrigger, trigger level, sampling frequency and channel to trigger select; appropriate relays and circuitry to drive them instead of the rotary switches for the attenuation level selection.The inclusion of control lines driven by the microprocessor for selection of the different latches and data lines would also be necessary. These modifications are easy and should not present a major problem. The microprocessor module would have to include some sort of communication channel (RS-232 perhaps), in order to communicate with the control room.

APPENDIX A

CIRCUIT DIAGRAMS

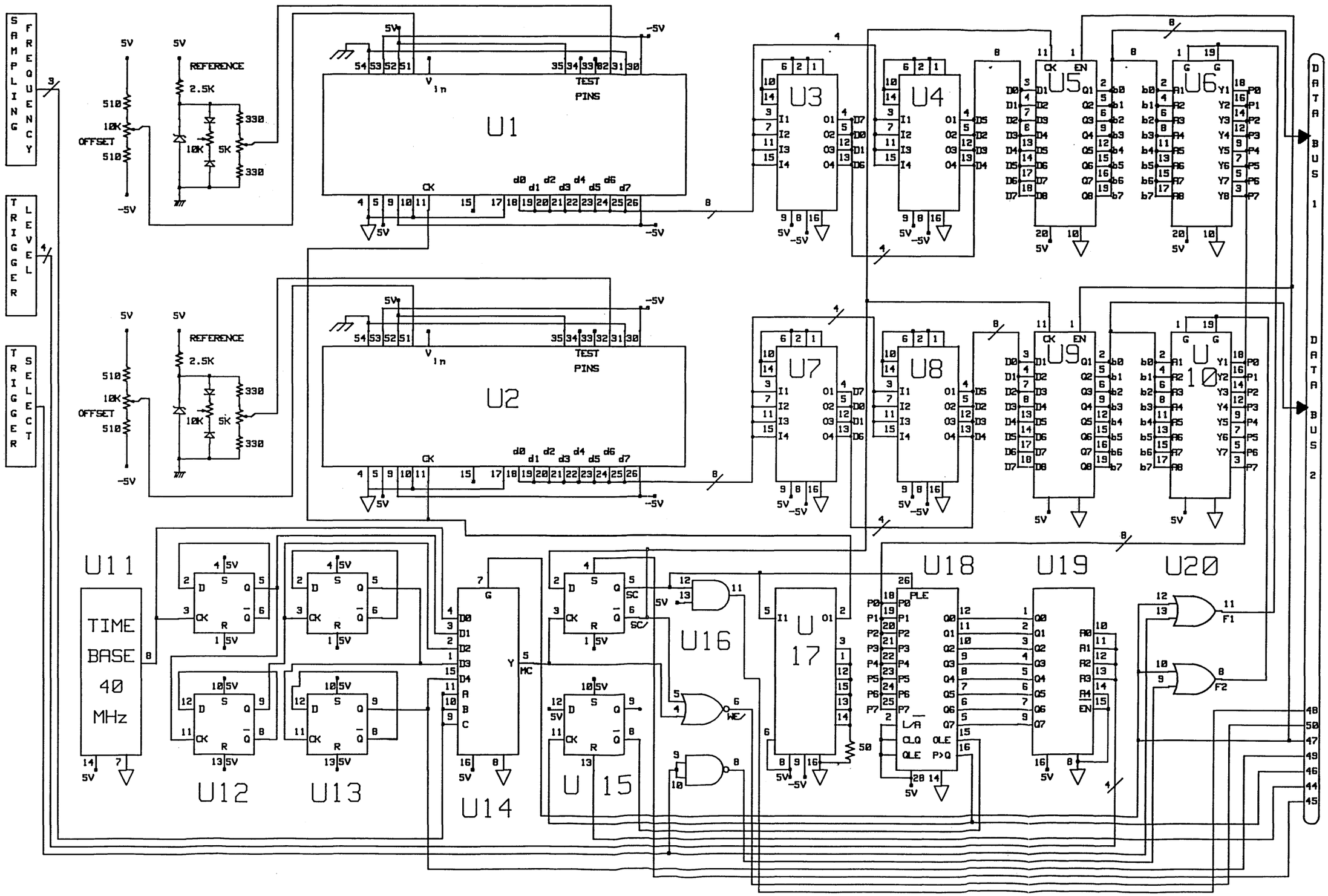


Figure A1. Analogue to digital conversion module, circuit diagram.

Analogue to digital converter module integrated circuit list.

Reference	*Part number*
U1,U2	BX-1200
U3,U4	MC10125
U5	74AS374
U6	74AS240
U7,U8	MC10125
U9	74AS374
U10	74AS240
U11	IQXO-500 (40 MHz)
U12,U13	74AS74
U14	74AS151
U15	74AS74
U16	74AS1000
U17	MC10124
U18	74AS866
U19	TBP18SA030
U20	74AS32

Figure A2. Memory module, circuit diagram.

Memory module integrated circuit list

Reference	*Part number*
U1	74LS139
U2	74LS08
U3	74LS374
U4	74LS240
U5,U6,U7,U8	HM6168HP-45
U9	ZN428
U10	74LS00
U11	74LS74
U12	74LS374
U13	74LS240
U14,U15,U16,U17	HM6168HP-45
U18,U19	531
U20	ZN428
U21	74ALS04
U22,U23,U24,U25	74F161A
U26	74LS11
U27	74ALS32
U28	74S00

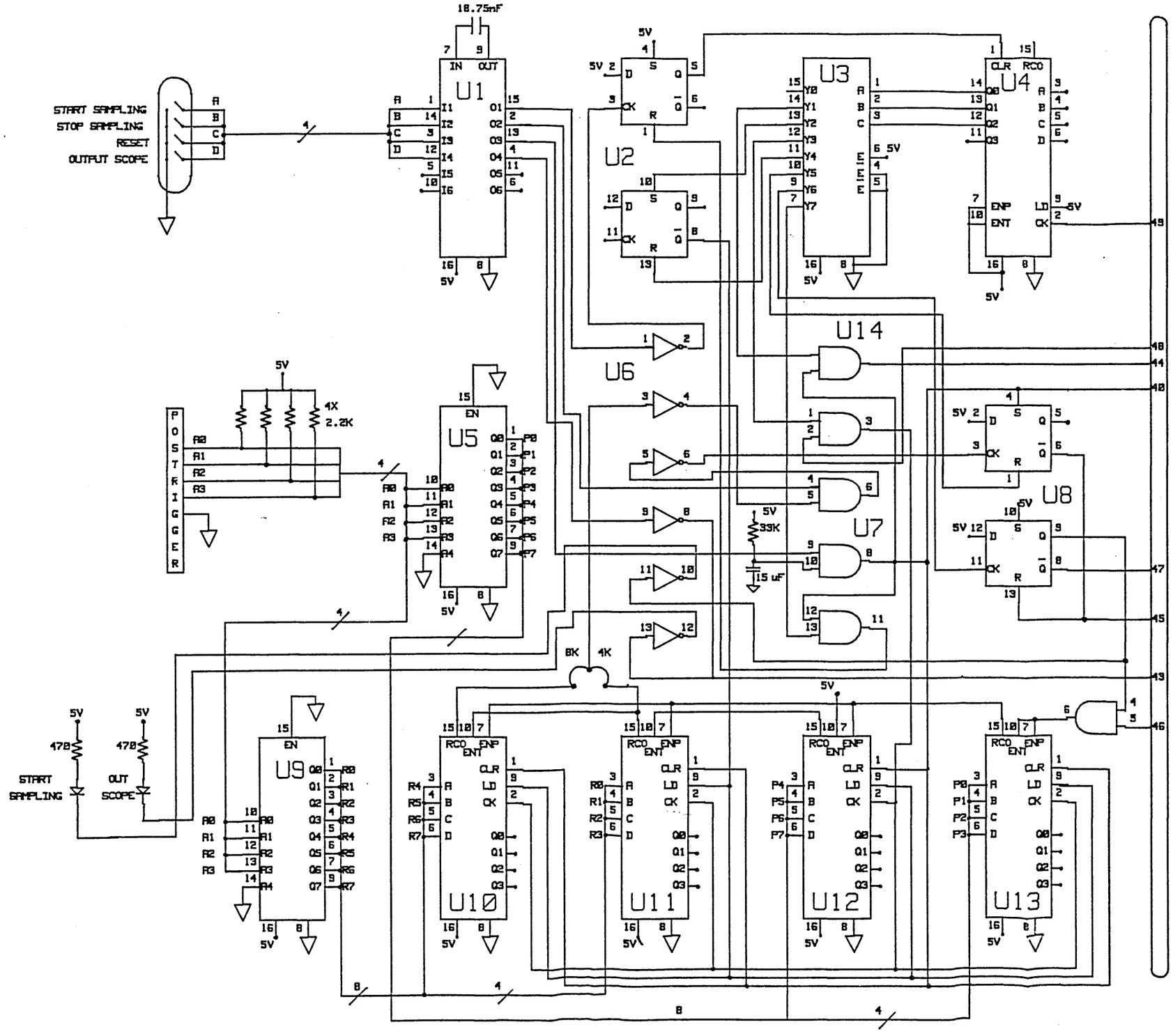


Figure A3. Control module, circuit diagram.

Control module integrated circuit part list

Reference	*Part number*
U1	MC14490
U2	74LS74
U3	74LS138
U4	74LS161
U5	TBP18SA030
U6	74AS04
U7	74AS08
U8	74AS74
U9	TBP18SA030
U10,U11,U12,U13	74F161A
U14	74LS08

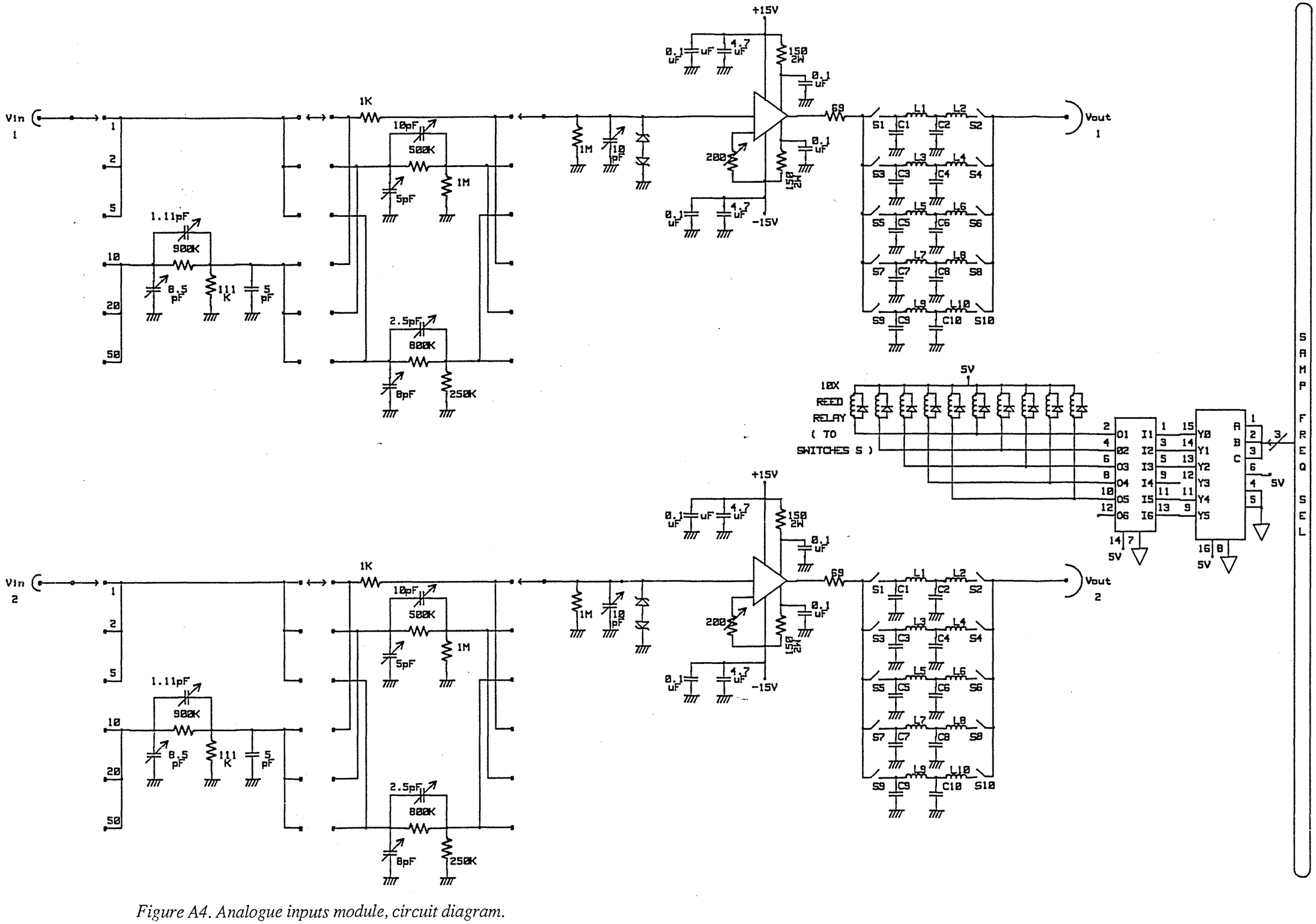


Figure A4. Analogue inputs module, circuit diagram.

Analogue inputs module integrated circuit list

Reference	*Part number*
U1,U2	LH0033
U3	7417
U4	74LS138

Filter component values

Reference	*Value*	*Cutoff frequency*
C1	162.423 X 10^{-12} F	10 MHz
L1	2.205 X 10^{-6} H	
C2	392.115 X 10^{-12} F	
L2	913.629 X 10^{-9} H	
C3	324.846 X 10^{-12} F	5 MHz
L3	4.411 X 10^{-6} H	
C4	784.231 X 10^{-12} F	
L4	1.827 X 10^{-6} H	
C5	649.692 X 10^{-12} F	2.5 MHz
L5	8.822 X 10^{-6} H	
C6	1.568 X 10^{-9} F	
L6	3.654 X 10^{-6} H	
C7	1.299 X 10^{-9} F	1.25 MHz
L7	17.640 X 10^{-6} H	
C8	3.136 X 10^{-9} F	
L8	7.309 X 10^{-6} H	
C9	2.598 X 10^{-9} F	0.625 MHz
L9	35.290 X 10^{-6} H	
C10	6.273 X 10^{-9} F	
L10	14.618 X 10^{-6} H	

The inductors were constructed by using insulated copper wire and ferrite cores. The

number of turns was obtained by using the formula given by Terman [29]:

$$N = \sqrt{[\,[\,L/\mu\,]\,/\,[\,d * F\,]\,]}$$

where: N = Number of turns.

d = Diameter of the coil [inches].

F = Variable depending upon the ratio of coil diameter to length of winding.

μ_r = relative permeability of core.

APPENDIX B

PRINTED CIRCUIT BOARDS

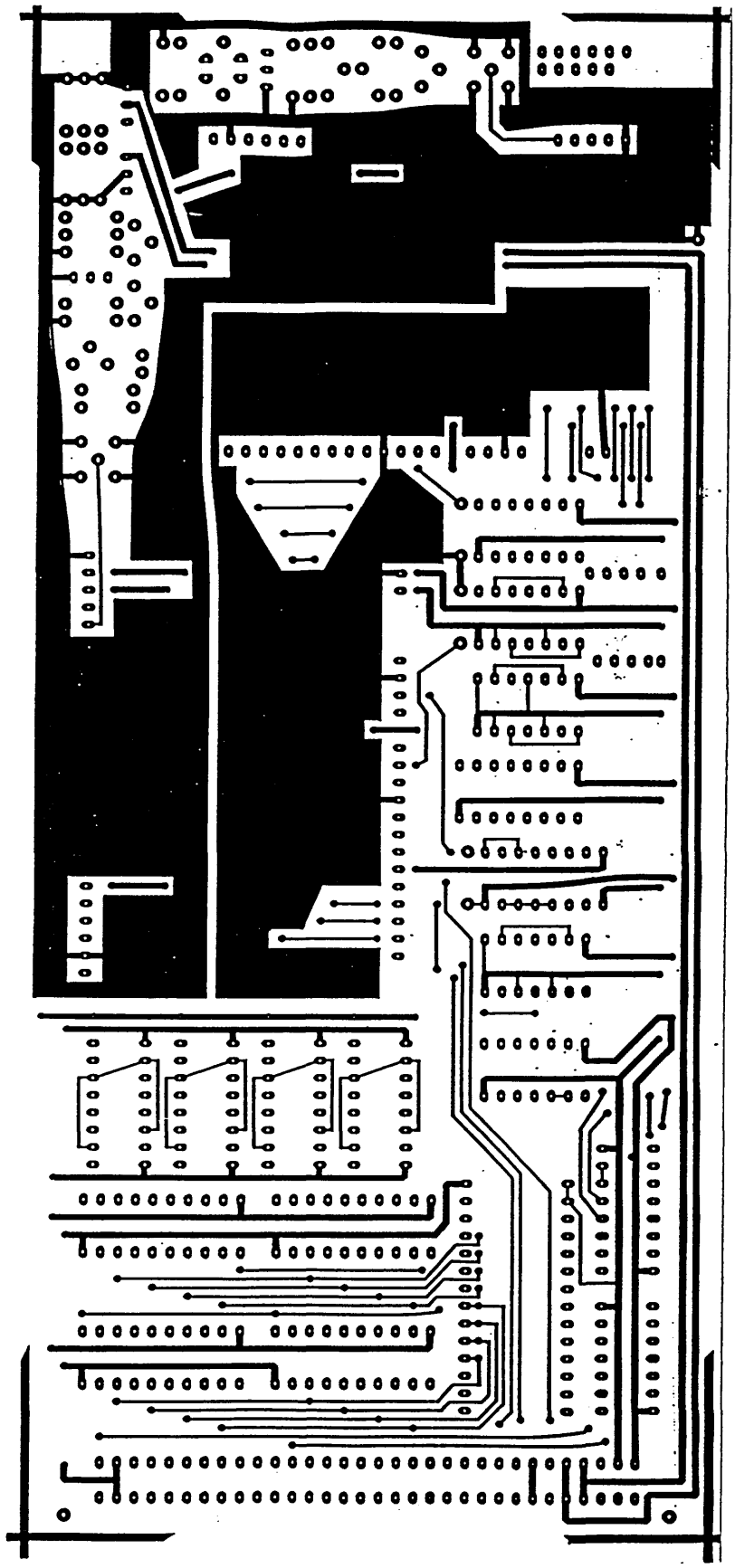


Figure B1. Printed circuit board for analogue to digital converter module, component side.

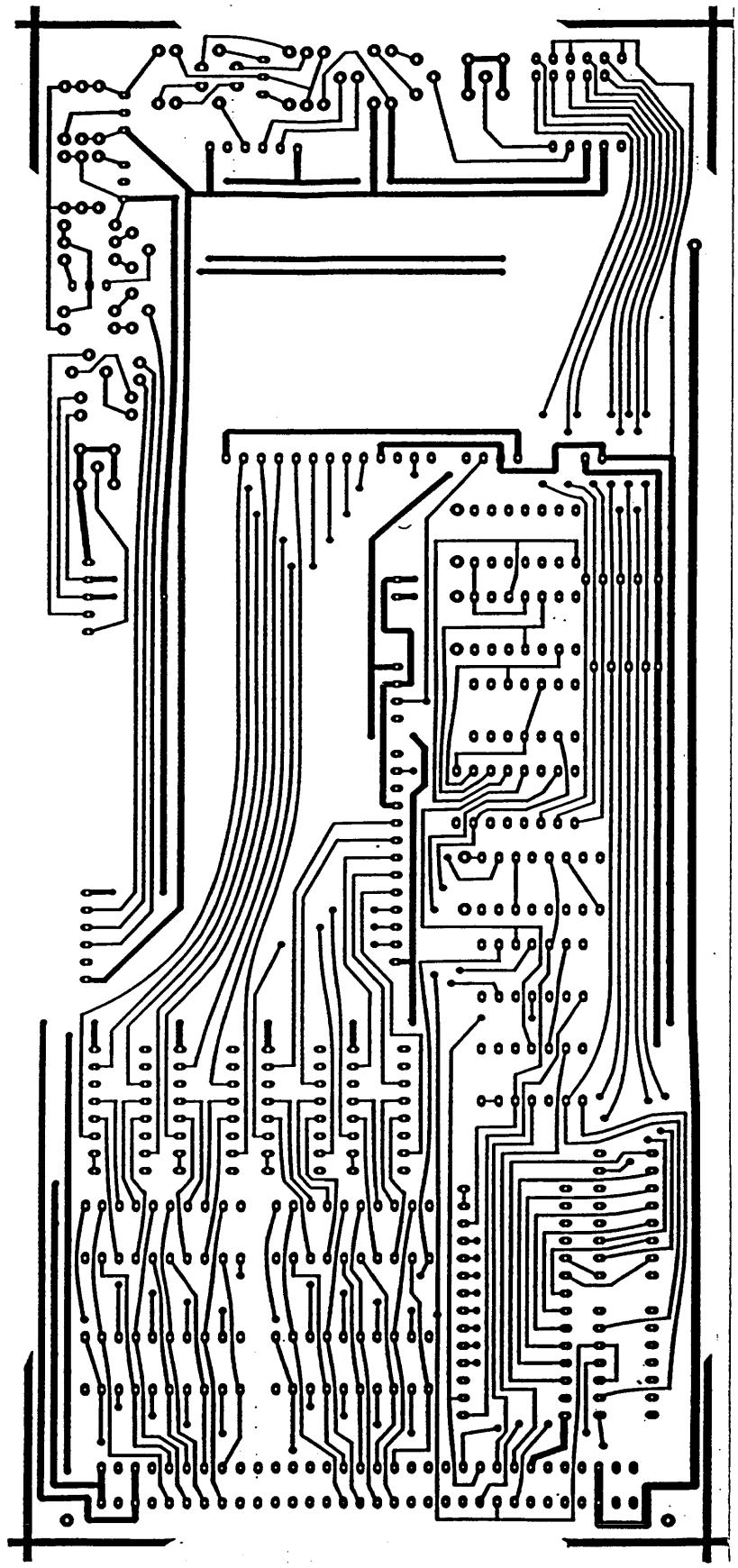


Figure B2. Printed circuit board for analogue to digital converter module, solder side.

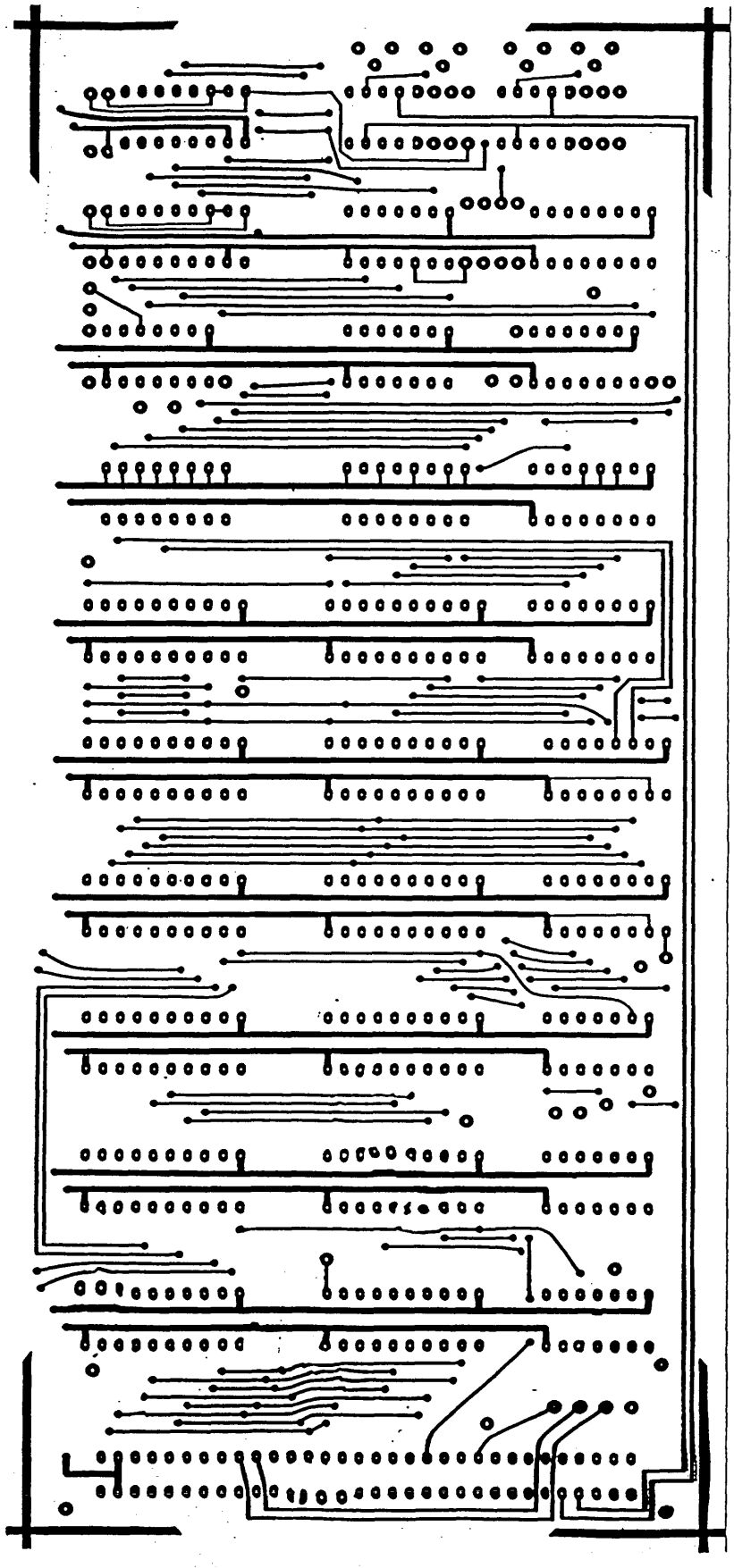


Figure B3. Printed circuit board for memory module, component side.

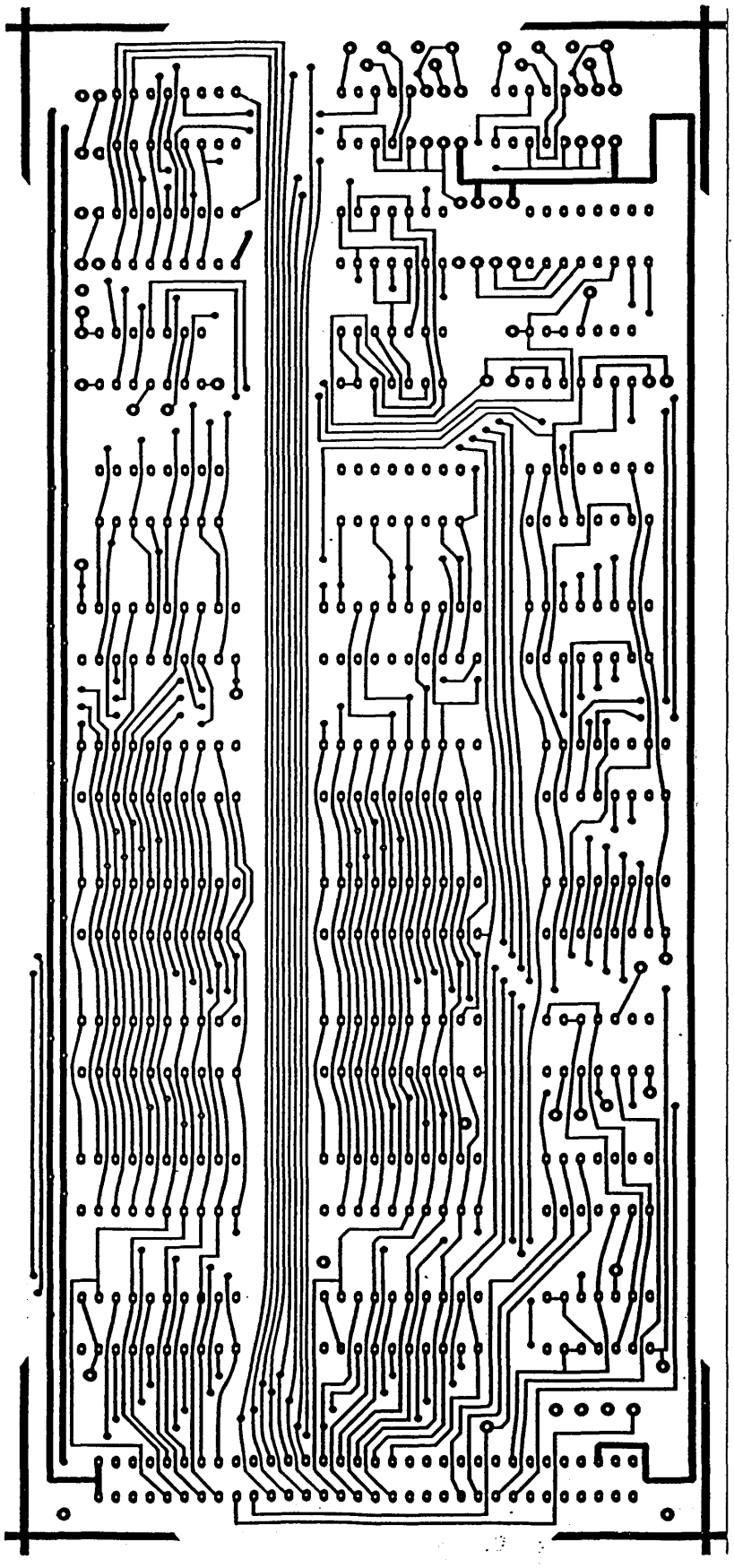


Figure B4. Printed circuit board for memory module, solder side.

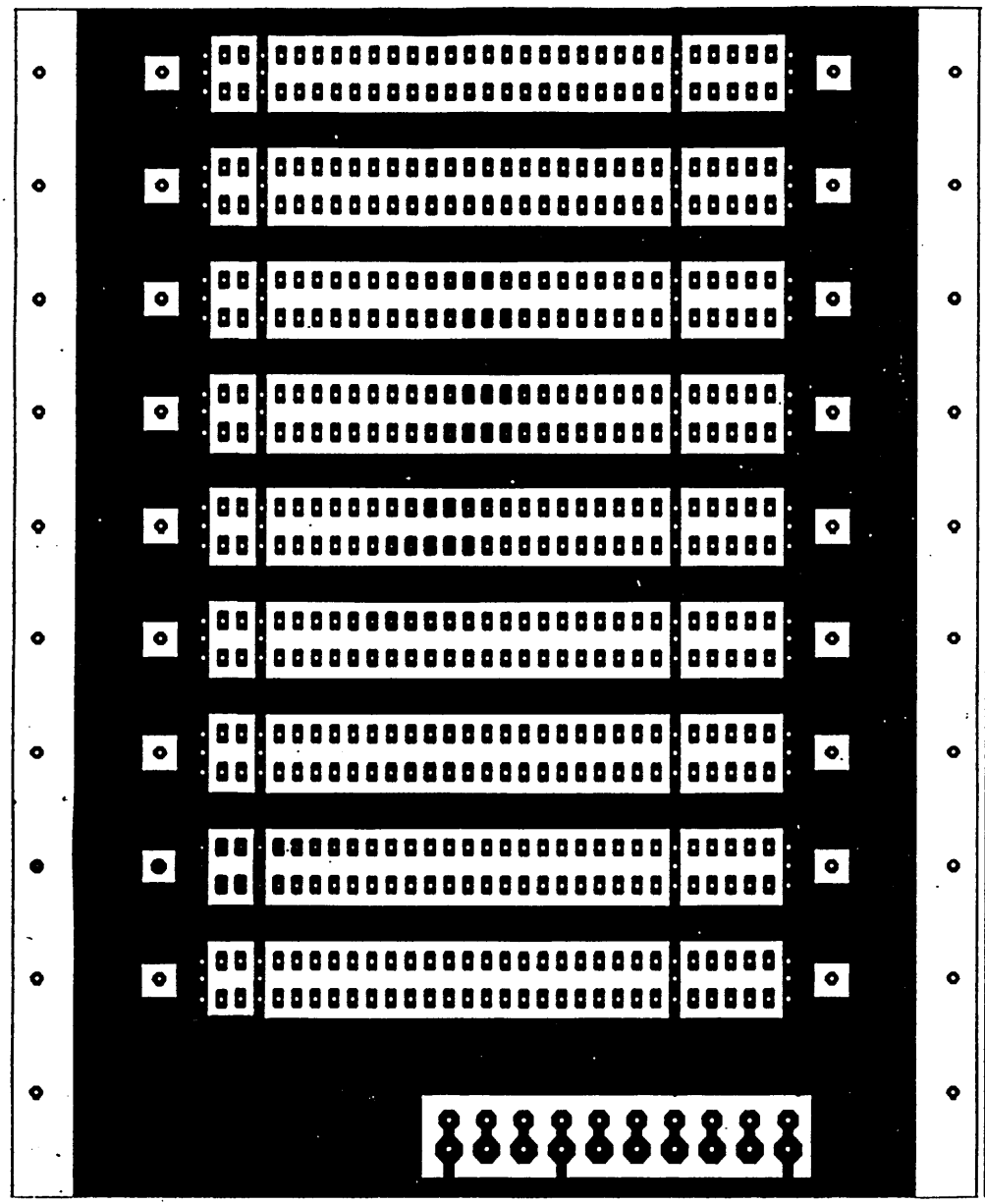


Figure B5. Printed circuit board for backplane, component side.

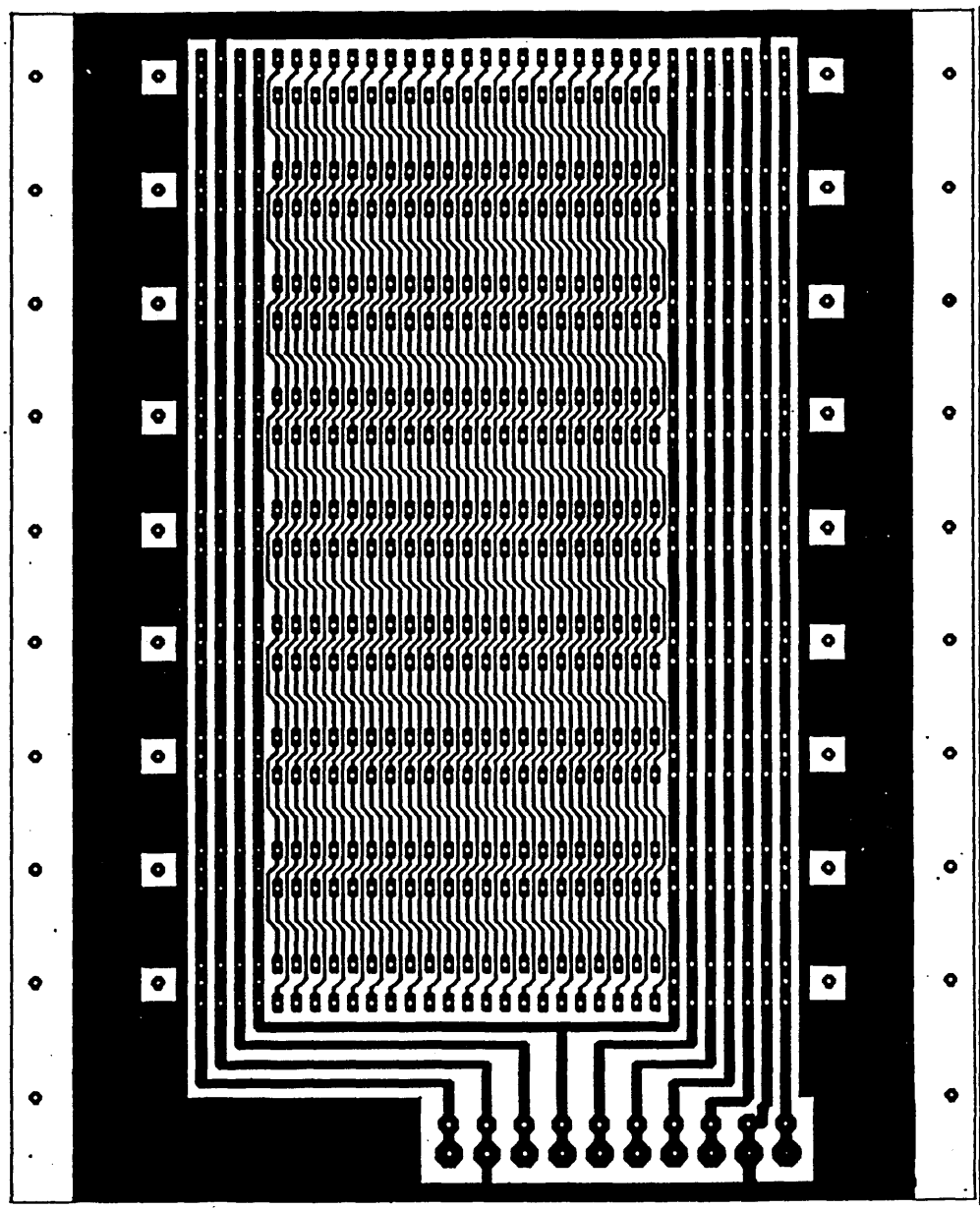


Figure B6. Printed circuit board for backplane, solder side.

APPENDIX C

COMPUTER ALGORITHM

```
FORTRAN IV      V02.5-11    Tue 21-Oct-86 00:49:09

0001          PROGRAM TWAVE
      C
      C       PROGRAM TO RUN LABORATORY TESTS
      C
0002          DIMENSION W0(3500)
0003          REAL I0(3500)
0004          COMMON/VAR1/SUM,DD,TDW,DT
0005          COMMON/VAR2/DIST(860),FX(860),NJ
      C
0006          CALL ASSIGN (3,'DATAIN.DAT')
0007          CALL ASSIGN (1,'AVER.DAT')
0008          CALL ASSIGN (2,'TANG.DAT')
0009          READ(3,*) RR,XL,C
0010          READ(3,*)  ND,NJ,TDW,DT
0011          ALPHA=SQRT(XL*C)
0012          BETA=RR*C
0013          DX=DT/ALPHA
0014          B1=(2.0*ALPHA+BETA*DX)/(4.0*ALPHA)
0015          B2=(2.0*ALPHA-BETA*DX)/(4.0*ALPHA)
0016          D1=B1*ALPHA
0017          D2=B2*ALPHA
0018          DD=0.0
      C
      C       ******************************************************
      C       THE CRITERIA FUNCTION BASICALLY INVOLVES:
      C         (1) THE SQUARE OF THE VOLTAGE, V*V
      C       ******************************************************
      C
0019          SUM=0.0
0020          DO 10 K=1,ND
0021          READ(3,*) V,I0(K)
0022          W0(K)=-C*V
0023          IF(K.NE.1.AND.K.NE.ND)GO TO 11
0025          SUM=SUM+(V*V)/2.0
0026          GO TO 10
0027       11 SUM=SUM+V*V
0028       10 CONTINUE
0029          CALL SUMA(1)
0030          DO 25 J=2,NJ
0031          K=ND
0032       17 I0(K+1)=I0(K)
0033          K=K-1
0034          IF(K.GE.1)GO TO 17
0036          K=ND
0037       18 W0(K+1)=W0(K)
0038          K=K-1
0039          IF(K.GE.1)GO TO 18
0041          DD=DD+DX
0042          ND=ND-2
0043          SUM=0.0
0044          DO 15 K=1,ND
0045          I0(K)=(W0(K+3)-W0(K+1))/(2.0*ALPHA)+B1*I0(K+3)+B2*I0(K+1)
0046          W0(K)=(W0(K+3)+W0(K+1))/2.0+D1*I0(K+3)-D2*I0(K+1)+
             *BETA*DX*I0(K)/2.0
0047          V=-W0(K)/C
0048          IF(K.NE.1.AND.K.NE.ND)GO TO 21
0050          SUM=SUM+(V*V)/2.0
0051          GO TO 15
```

```
FORTRAN IV      V02.5-11    Tue 21-Oct-86 00:49:09

0052      21 SUM=SUM+V*V
0053      15 CONTINUE
0054         CALL SUMA(J)
0055      25 CONTINUE
0056         CALL OPTIMI
0057         STOP
0058         END
```

```
FORTRAN IV      V02.5-11    Tue 21-Oct-86 00:49:19

0001         SUBROUTINE SUMA(J)
      C      AN INTEGRATION ROUTINE
0002         COMMON/VAR1/SUM,DD,TDW,DT
0003         COMMON/VAR2/DIST(860),FX(860),NJ
0004         FX(J)=SUM*DT/TDW
0005         DIST(J)=DD
0006         WRITE(1,30) FX(J)
0007      30 FORMAT(5X,E10.4)
0008         RETURN
0009         END
```

```
FORTRAN IV      V02.5-11    Tue 21-Oct-86 00:49:21

0001         SUBROUTINE OPTIMI
      C      A ROUTINE TO SEARCH FOR THE TURNING POINT OF "F(X)"
0002         COMMON/VAR2/DIST(860),FX(860),NJ,DX
0003         FXMIN=FX(1)
0004         FDIST=DIST(1)
0005         DO 40 J=2,NJ
0006         IF(FX(J).GE.FXMIN) GO TO 40
0008         FXMIN=FX(J)
0009         FDIST=DIST(J)
0010      40 CONTINUE
0011      45 IF(FDIST.GE.DIST(NJ)) GO TO 55
0013         WRITE(7,50) FDIST
0014      50 FORMAT(/2X,'THE FAULT LOCATION IS',F9.4,'TIME AVERAGE FUNCTION'
0015         GO TO 70
0016      55 WRITE(7,60)
0017      60 FORMAT(//2X,
                * 'THE FAULT CANNOT BE LOCATED BY THE TIME AVERAGE FUNCTION')
0018      70 RETURN
0019         END
```

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[2] Stringfield, T.W., Marihart, D.J., Stevens R.F. *'Fault Location Methods for Overhead Lines'*, AIEE Trans., 1955, PAS-74, pp. 1423-1428.

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