

Imperial College London

**Novel Current-Mode Sensor
Interfacing and Radio Blocks for Cell
Culture Monitoring**

by

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“The only source of knowledge is experience”

Albert Einstein

Imperial College London

Abstract

Department of Bioengineering

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Since 2004 Imperial College has been developing the world's first application-specific instrumentation aiming at the on-line, in-situ, physiochemical monitoring of adult stem cell cultures. That effort is internationally known as the 'Intelligent Stem Cell Culture Systems' (ISCCS) project. The ISCCS platform is formed by the functional integration of biosensors, interfacing electronics and bioreactors. Contrary to the PCB-level ISCCS platform the work presented in this thesis relates to the realization of a miniaturized cell culture monitoring platform. Specifically, this thesis details the synthesis and fabrication of pivotal VLSI circuit blocks suitable for the construction of a miniaturized microelectronic cell monitoring platform. The thesis is composed of two main parts.

The first part details the design and operation of a two-stage current-input current-output topology suitable for three-electrode amperometric sensor measurements. The first stage is a CMOS-dual rail-class AB-current conveyor providing a low impedance-virtual ground node for a current input. The second stage is a novel hyperbolic-sine-based externally-linear internally-non-linear current amplification stage. This stage bases its operation upon the compressive $\sinh^{-1}$ conversion of the interfaced current to an intermediate auxiliary voltage and the subsequent $\sinh$ expansion of the same voltage. The proposed novel topology has been simulated for current-gain values ranging from 10 to 1000 using the parameters of the commercially available $0.8\mu\text{m}$ AMS CMOS process. Measured results from a chip fabricated in the same technology are also reported. The proposed interfacing/amplification architecture consumes $0.88\text{--}95\mu\text{W}$.

The second part describes the design and practical evaluation of a 13.56MHz frequency shift keying (FSK) short-range (5cm) telemetry link suitable for the monitoring of incubated cultures. Prior to the design of the full FSK radio system, a pair of 13.56MHz antennae are characterized experimentally. The experimental S-parameter-value determination of the 13.56MHz wireless link is incorporated into the Cadence Design Framework allowing a high fidelity simulation of the reported FSK radio. The transmitter of the proposed system is a novel multi-tapped seven-stage ring-oscillator-based VCO whereas the core of the receiver is an appropriately modified phase locked loop (PLL). Simulated and measured results from a 0.8 μ m CMOS technology chip are reported.

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Patent

‘Current Amplifier’ H.M.D.Ip, A.Walia, A.G.Katsiamis and E.M.Drakakis, PCT filing date Dec 2007, contact: Dr. Tim Knott, Imperial Innovations

Publications

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2. 'A CMOS Current-Mode Hyperbolic-Sine-Based Three-Electrode Sensor Interfacing and Amplification Circuit' Walia, A.S.; Ip, H.M.; Katsiamis, A.; Drakakis, E.M.; Electronics, Circuits and Systems, 2007. ICECS 2007. 14th IEEE International Conference on 11-14 Dec. 2007 Page(s):1320 - 1323
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List of Contributions

1. Conception, design, analysis, layout fabrication and testing of a ‘Novel Current Mode Sinh Current Amplifier’ - The block consumes $95\mu\text{Ws}$ when offering a current gain of 1000, and has a measured bandwidth of 400Hz.
2. Conception, design, analysis, layout fabrication and testing of a ‘Novel Multi-tapped Voltage Controlled Ring Oscillator’ - Which is at the heart of both the transmitter and receiver units of the 13.56MHz radio targeted.

Contents

Abstract	ii
Acknowledgements	iv
Patent	v
Publications	v
List of Contributions	vi
List of Figures	xii
List of Tables	xviii
I Introduction	1
1 Thesis Overview	2
2 Stem Cells: What are they and what is their general significance?	7
2.1 Embryonic Stem Cells	8
2.2 Adult Stem Cells	8
2.3 Summary	9
II Sensor Interfacing Circuitry	11
3 Overview of Sensor Interfacing Circuits	12
3.1 Piezoelectric / Resistive Sensors	13
3.2 Capacitive Sensors	15
3.3 Potentiostats	17

3.3.1	Two Electrode Potentiostat	19
3.3.2	Three Electrode Potentiostat	20
3.3.3	Peripheral Circuitry	21
3.3.4	Randles Electrode Model	23
3.3.5	Literature Review	26
3.4	Summary	30
4	CMOS Current Conveyors	32
4.1	General	32
4.2	Transistor-level topology of CMOS Current Conveyors	34
4.3	Voltage Swing Analysis	38
4.4	Current Swing Analysis	39
4.5	Noise Analysis [60]	39
4.6	Summary	41
5	Sinh Current Amplifier	42
5.1	Elementary Transistor Theory	42
5.1.1	$I_d - V_{ds}$ Characteristics	43
5.1.2	Saturation Region	44
5.1.3	Linear Region	44
5.1.4	Weak Inversion	45
5.2	Sinh Amplifier	47
5.2.1	Exponential Transconductor Cells (E Cells)	47
5.2.2	I-to-Sinh(V) Block	49
5.2.3	Sinh(V)-to-I Block	50
5.3	The Proposed Sinh Current Amplifier	52
5.3.1	Impact of an offset voltage at the V_x node	53
5.4	Error analysis of the Sinh Current Amplifier	58
5.5	Conclusion	62
6	Sinh Current Amplifier Results	64
6.1	AMS $0.8\mu\text{m}$ Results	66
6.1.1	Simulation Results	66
6.1.2	Measured Results	71
6.2	AMS $0.35\mu\text{m}$ Results	80
6.3	Conclusion	86
6.3.1	General	86
6.3.2	Measured results from a practical sensor	88
7	Summary and Discussion of the Sinh Current Amplifier Approach	92
III	Wireless Unit	95
8	Introduction to Wireless Sensors	96

8.1	Literature Review	97
8.1.1	Bluetooth - Zigbee	97
8.1.2	Inductive Link Telemetry	99
8.1.3	Application Specific Radio Design	104
8.2	ISM Bands	106
8.3	Conclusion	107
9	Transmitter	108
9.1	PLL Based Radio	108
9.1.1	Types of Transmission	108
9.1.2	Proposed Radio Design	109
9.2	Oscillators	110
9.2.1	LC Oscillator	110
9.2.2	Colpitts Oscillator	112
9.3	Ring Oscillator	113
9.3.1	Ring Oscillator Analysis	113
9.3.2	The Role of the Number of Stages of a Ring Oscillator	116
9.3.3	Example	118
9.3.4	Variable MOS Capacitor	120
9.3.5	Multitapped Ring Oscillator	125
9.3.6	Multi-tapped Ring Oscillator: properties and comparison with conventional Ring Oscillator	127
9.3.7	Jitter Noise Analysis	135
9.3.8	Summary of the VCO Design	137
9.4	Antenna Interface	137
9.5	Antenna Driver	144
9.6	Conclusion	145
10	Receiver	147
10.1	Amplifier	147
10.2	Phase Locked Loop - Theory Summary	148
10.2.1	Voltage Controlled Oscillator	149
10.2.2	Phase Detector	150
10.2.3	Loop Filter	151
10.2.4	Loop Dynamics	151
10.2.5	Summary	154
10.3	Summary	154
11	Simulated and Measured Results of the proposed Radio Link Blocks	156
11.1	Simulated Results	157
11.2	Measured Results	160
11.3	Conclusion	164

IV Conclusion	166
12 Conclusion	167
12.1 Sinh Current Amplifier	168
12.2 Radio	171
12.3 Summary	172
13 Appendix A: Jitter Noise [121]	174

List of Figures

1.1	Miniaturized Biosensors	3
1.2	Model of a Typical Bioreactor	3
1.3	Bioreactor together with the Sensors	4
1.4	Bioreactor along with the biosensors placed within the incubator	4
1.5	(a) Potentiometric and (b) Amperometric modules.	5
1.6	Concentration of ammonia with Mouse 3T3 fibroblast cell cultures over a period of 7 days. Each trace represents an electrode placed in a different location in the cell culture.	6
2.1	Stem Cells can proliferate or become specialized cells. Extracted from [2]	7
2.2	Embryonic Stem Cells Pathway. Extracted from [5]	9
2.3	Bone stem cell differentiation pathways. Extracted from [6]	10
3.1	Theoretical setup of a piezoelectric sensor. Extracted from [11]	14
3.2	Wheatstone bridge-based sensor comprising of piezoresistors and polysilicon resistors. Extracted from [14]	14
3.3	Rotation sensor using a Wheatstone Bridge. Extracted from [15]	15
3.4	Capacitor in normal state (a) and when under pressure (b). Extracted from [20]	15
3.5	Capacitive Heartbeat Sensor. Extracted from [21]	16
3.6	Model of the patch electrodes placed on the chest. Extracted from [21] .	16
3.7	CSF shunt system implementation. Extracted from [22]	17
3.8	Wireless LC based pressure sensor. Extracted from [22]	18
3.9	Potentiostat from the 1940's (left) [29], and 2000's (right) [30]	18
3.10	Typical two electrode potentiostat. Extracted from [32]	19
3.11	(a) Two electrode potentiostat, (b) zero current conditions, (c) positive current conditions, (d) Three electrode potentiostat, (e) zero current conditions, (f) positive current conditions, (g) positive current conditions with V_{WE} held constant. Extracted from [32]	21
3.12	Typical Three electrode potentiostat. Extracted from [32]	22
3.13	Typical Three electrode potentiostat circuit analysis	22
3.14	Randles equivalent model of an electrode in electrolyte. Extracted from [43]	24
3.15	AC response of the Randles equivalent model, R_w corresponds to the parallel combination of R_c and C_c . Extracted from [44]	24
3.16	Electrochemical Cell. Extracted from [46]	25

3.17	Electrode / Electrolyte Interface Model. Extracted from [48]	26
3.18	Three electrode potentiostat theoretical setup. Extracted from [44]	26
3.19	Two electrode potentiostat based on charging and discharging C_d . Extracted from [49]	27
3.20	Three electrode potentiostat from Stanford.. Extracted from [50]	28
3.21	Single ended potentiostat. Extracted from [51]	28
3.22	Test circuit for the potentiostat of figure. Extracted from 3.21. [51]	29
3.23	Microprocessor-based potentiostat. Extracted from [52]	29
3.24	Potentiostat with triangular excitement. Extracted from [53]	30
3.25	Potentiostat driven with a DA converter. Extracted from [54]	30
4.1	Current Conveyor Block. Extracted from [57]	33
4.2	NMOS transistor viewed as Current Conveyor	35
4.3	NMOS current mirror	35
4.4	PMOS current mirror	35
4.5	PMOS current mirror modified	36
4.6	Voltage Follower	36
4.7	Class A-Single Rail-Current Conveyor	37
4.8	Class AB-Dual Rail-Current Conveyor . Extracted from [62] and [63]	37
4.9	Typical Cascode Current Mirror	38
4.10	Current Limiting Node	39
4.11	Class AB-Dual Rail-Current Conveyor	41
5.1	NMOS Transistor	43
5.2	Typical $I_{ds} - V_{ds}$ Curves for an NMOS Transistor. Extracted from [78]	43
5.3	Typical $I_{ds} - V_{ds}$ Curves for an NMOS Transistor. Extracted from [78]	44
5.4	Log I_d vs V_{gs} Curve	46
5.5	Plot of $\frac{dLogI_d}{dV_{gs}}$ vs V_{gs}	46
5.6	CMOS transistor configuration of an E_+ Cell; $I_{out,E+} = I_{bias}e^{\frac{(V_+-V_-)}{2nV_T}}$	47
5.7	CMOS transistor configuration of an E_- Cell; $I_{out,E-} = I_{bias}e^{\frac{-(V_+-V_-)}{2nV_T}}$	48
5.8	I-to-sinh(V) block response	49
5.9	I-to-sinh(V) block response	50
5.10	Sinh(V)-to-I Block response	51
5.11	Sinh(V)-to-I Block	51
5.12	Sinh Class AB Current Amplifier topology	53
5.13	Plotting of the terms $\cosh(x)$, $1 + \tanh(x)$ and, $\cosh(x)[1 + \tanh(x)]$ of equation 5.37	56
5.14	$I_{out-real}$ vs V_{offset} when $I_{out-ideal} = 1000(\gg I_1)$	57
5.15	$I_{out-real}$ vs $I_{out-ideal}$ when $I_1=50, 100, 200nA$'s and $V_{off}=-20, 0 +20mV$	57
5.16	E_+ error cell	58
5.17	E_- error cell	59
5.18	Sinh Class AB Current Amplifier topology	62
6.1	Traditional three electrode potentiostat theoretical measurement. Extracted from [38]	64

6.2	Proposed three electrode potentiostat theoretical measurement	64
6.3	Current Mode Sensor Interface Circuit	65
6.4	Typical Frequency responses of the topology of figure 6.3 gains of (a) 20, (b) 40 and (c) 60dB's	66
6.5	Typical Transient Waveforms of the topology of figure 6.3 for gains of (a) x10, (b) x100 and (c) x1000 and the (d) input current	67
6.6	Output THD	68
6.7	Current Input vs Current Output	68
6.8	Sinh Amplifier transistor topology in 0.8 μ m process	70
6.9	AMS 0.8 μ m mask layout of the Sinh Amplifier	71
6.10	0.8 μ m chip microphotograph	72
6.11	Test and measurement setup	72
6.12	Laboratory setup for the Sinh Current Amplifier	73
6.13	$I_{in} = 1n, 2n, 3n, 6n$ and $8n$ for the test conditions (see figure 6.12): $G = 10, R_L = 1M\Omega$	74
6.14	$I_{in} = 1n, 2n$ and $3n$ for the test conditions (see figure 6.12): $G = 100, R_L = 1M\Omega$	75
6.15	$I_{in} = 1n, 2n$ and $3n$ for the test conditions (see figure 6.12): $G = 1000, R_L = 1M\Omega$	76
6.16	20dB Gain for $I_{in} = 1n, 2n, 3n, 6n$ and $8n$	77
6.17	40dB Gain for $I_{in} = 1n, 2n$ and $3n$	78
6.18	60dB Gain for $I_{in} = 1n, 2n$ and $3n$	79
6.19	$I_{in} = 2nA$ at 80 Hz at 1000x gain	80
6.20	AMS 0.35 μ m mask layout of the Sinh Amplifier	81
6.21	0.35 μ m chip microphotograph	81
6.22	Sinh Amplifier transistor topology in 0.35 μ m process	82
6.23	$I_{in} = 10n, 15n$ and $20nA$ for the test conditions (see figure 6.12): $G = 100, R_L = 100k\Omega$	84
6.24	100x Gain for $I_{in} = 10n, 15n$ and $20nA$	85
6.25	Transient and frequency spectrum measured results for a gain of x100 when the single tone input current amplitude is set to 10nA at 80Hz	86
6.26	I_{in} vs I_{out} for 100x Gain	87
6.27	Practical sensor interfacing setup (Equipment used: Keithley 6220 Precision Current Source and 6221 DC and AC Current Source, TTI Thurlby Thandy Instruments PL320QMT, Lecroy Wavesurfer 434 350MHz Oscilloscope, Lecroy Wavepro 7300A 3GHz Oscilloscope)	89
6.28	Results from the 0.2mM solution. a) recorded current from Matlab through Kiethley, and b) recorded current from the Oscilloscope through the Sinh Current Amplifier prototype chip	90
6.29	Hysteresis curve of the results from a 0.2mM solution under a cyclic voltammetry input	91
7.1	Typical op-amp-based interfacing with three-electrode sensors	92
7.2	The Sinh current-amplifier based interfacing (compare with figure 7.1)	93

8.1	Incubator	96
8.2	Indicative Two Channel Frequency Hopping case. Extracted from [86]	98
8.3	Bluetooth Sensor Development Kit. Extracted from [90]	99
8.4	Circuit Representation of an Inductive Link. Extracted from [93]	100
8.5	Coil Alignments, (a) Ideal alignment, (b) Lateral alignment, (c) Angular misalignment, (d) General misalignment. Extracted from [95]	102
8.6	Schematic for the explanation of the Load Shift Keying Technique. Extracted from [96]	103
8.7	Capacitive Wireless Load-Shift-Keying Sensor System. Extracted from [97]	105
8.8	Laboratory-in-a-pill Device. Extracted from [98]	105
8.9	Biotelemetry Microsystem for Measuring Multiple Physiological Parameters: Extracted from [99]	106
9.1	ASK, PSK and FSK	109
9.2	The proposed simple radio: VCO transmitter, PLL receiver. Extracted from [101]	109
9.3	LC oscillator Basic diagram. Extracted from [102]	111
9.4	(a) Typical Differential LC oscillator, (b) Negative impedance $\left(-\frac{2}{g_m}\right)$ of cross coupled pairs. Extracted from [102]	111
9.5	(a) Inductor, (b) Impulse response applied to an inductor, (c) ringing response of the inductor.	112
9.6	Typical Colpitts Oscillator. Extracted from [106]	113
9.7	(A) a basic inverter, (B) an example of a seven-stage ring oscillator, (C) typical output waveform from a ring oscillator	114
9.8	A definition of t_{fall} . Extracted from [112]	114
9.9	(a) 3 stage ring oscillator, (b) ‘wave’ propagation through circuit in a, (c) 5 stage ring oscillator, (d) ‘wave’ propagation through circuit in c.	117
9.10	Inverter model, of a 5 stage ring oscillator.	118
9.11	Capacitance controlled oscillation frequency: $N = 5$, $\frac{W}{L_n} = \frac{3.2\mu}{0.8\mu}$, $\frac{W}{L_p} = \frac{3.2\mu}{0.8\mu}$, square wave ring oscillator; frequency range: 202-11MHz	119
9.12	Capacitance controlled oscillation frequency: $N = 5$, $\frac{W}{L_n} = \frac{1.6\mu}{1.6\mu}$, $\frac{W}{L_p} = \frac{1.6\mu}{1.6\mu}$, square wave ring oscillator; frequency range: 60-2MHz	119
9.13	a) PMOS varactor, b) Capacitive equivalence	120
9.14	PMOS transistor in depletion mode. Extracted from [80]	121
9.15	PMOS transistor in inversion mode. Extracted from [80]	121
9.16	Gate-Bulk Capacitance Model [119]	122
9.17	PMOS varactor C_{gb} vs V_{gb} , (dashed line for high frequencies)	124
9.18	Simulated PMOS varactor (inset): C_{gb} vs V_{gb}	124
9.19	Frequency vs DC input of the VCRO (inset)	125
9.20	Frequency vs capacitance of a ring oscillator (inset)	125
9.21	C_{gb} vs V_{gb} for the PMOS varactor (inset)	126
9.22	(a) Ring Oscillator, (b) Conventional VCO, (c) Multitapped VCO	126
9.23	Three-stage voltage controlled ring oscillator	128

9.24	Signal Analysis	128
9.25	Comparison of two 3-stage multi-tapped RO's (also consult figure 9.26) with the MOS capacitor control lines all connected together ('net67' trace) and when they are not. Superposition of signals seems to lead to amplitude reduction. All PMOS varactors are of the same size.	129
9.26	a) Three stage multi-tapped ring oscillator with individual inputs, b) Three stage multi-tapped ring oscillator with all inputs connected together. Note all PMOS varactors are of the same size.	130
9.27	(a) shows expected charging and discharging of a capacitor and (b) shows what would happen if the charging and discharging occurred at high frequency	130
9.28	The effect of superposition (relation 9.37) for a) $N=3$, b) $N=5$ and c) $N=7$, with the amplitude = 1 unit and $\omega = 10$. Observe that as N increases the amplitude of X_s decreases	132
9.29	a) Multi-tapped Oscillator, b) Single Tap Oscillator, c) reduced size varactor from (a) used in Single Tap Oscillator	133
9.30	Single output control line for the multi-tapped oscillator (9.29a)	134
9.31	Single output control line for the single tapped oscillator (9.29b)	134
9.32	The reduced size MOS transistor capacitor single tapped oscillator. Clearly multi-tapping reduces the unwanted signal on the control line (9.29c).	135
9.33	(a) Perfect sine wave in the time domain, (b) Perfect sine wave in the frequency domain, (c) 'Real' sine wave in the frequency domain	136
9.34	(a) The ideal transient oscillator signal, (b) the signal in a) with noise injected when the signal is 'low' and (c) the signal in a) with the noise on a transitional period.	136
9.35	The Copytag 13.56MHz antenna used, its dimensions are 35mm by 34mm, cost: £46.53	138
9.36	Experimental setup used for testing the antenna link. A Agilent/HP 8116A Signal generator and a Agilent DSO3062A oscilloscope were used.	139
9.37	Measured results of the antenna link	140
9.38	Experimental setup for the S-characterisation of the link	141
9.39	Measured S_{11} results of the antenna link	142
9.40	Measured S_{21} results of the antenna link	143
9.41	Smith Chart positioning of the measured S_{11} and S_{21} values for different distances between the antennae. ($A=0.5\text{cm}$, $B=1\text{cm}$, $C=1.5\text{cm}$, $D=2\text{cm}$ etc)	144
9.42	The transmitting antenna driver circuit	145
9.43	Block diagram of the transmitting unit	145
9.44	Circuit diagram of the VCRO circuit	146
9.45	Output frequency of the circuit in figure 9.44 when subjected to a logic 1 or 0 at the DATA terminal	146
9.46	Output frequency of the circuit in figure 9.44 when subjected to a variation in the Frequency tuning input terminal	146
10.1	Receiver Antenna Amplifier	148

10.2 Traditional Phase Locked Loop	148
10.3 Voltage controlled oscillator operation basics	149
10.4 Basic phase detector operation: the phase difference $\Delta\phi$ in (a) produces aa dc output voltage $K_{PD}\Delta\phi(b)$	150
10.5 Elementary Loop Filter	151
10.6 PD LPF output waveform typical examples	151
10.7 Basic PLL Model	152
10.8 (a) PLL model used for ζ analysis, (b) ζ value effects on V_c	153
10.9 PLL Concept-Based Radio	154
10.10 PLL-based Receiver	155
10.11 The proposed short range radio	155
11.1 Block-level schematic of the simulated 13.56MHz radio	156
11.2 The Transmitter's multi-tapped VCRO Circuit.	157
11.3 Antenna Driver Circuit	157
11.4 Recovery circuit	158
11.5 (a) D-Flip-Flop Circuit, (b) D-Flip-Flop Hardening Function	158
11.6 Phase Detector XOR	158
11.7 Waveforms of the LPF output with and without a Charge Pump	159
11.8 Charge Pump and RC LPF	159
11.9 Simulated (a) Input, (b) Control Voltage and (c) Output ($V_{CO_{receiver}}$ in- put) of the Full Wireless System for a Range of 2.5cm	160
11.10 Inter-chip tuning and variation of the multitapping VCRO transmitter as a function of the input voltage DC_1	161
11.11 DC_1 input voltage to needed to achieve the correct 13.56MHz frequency	161
11.12 Transmitters' (a) practical setup, (b) transient response with the antenna placed 2cm apart	162
11.13 $V_{peak-to-peak}$ vs distance, for the practical setup of the circuit illustrated in figure 11.12	163
11.14 The Transmitter's Multi-Tapped VCRO Circuit.	164
11.15 Output frequency of the circuit in figure 11.14 when subjected to a vari- ation at the data and frequency tuning input	164
12.1 Incubator	167
12.2 Traditional three electrode potentiostat theoretical measurement [38]	168
12.3 Proposed three electrode potentiostat theoretical measurement	168
12.4 Class AB-Dual Rail-Current Conveyor	169
12.5 Sinh Class AB Current Amplifier	170
12.6 Block-level schematic of the simulated 13.56MHz radio	171

List of Tables

4.1	Generic Current-Conveyor-based Operation [57] [58]	34
5.1	Dependence of % error of $I_{out,ideal}$ upon ϵ_1 , ϵ_3 and λ	62
6.1	Sinh Current Amplifier Specifications	69
6.2	Transistor sizes of Sinh Current Amplifier depicted in figure 6.8	71
6.3	Transistor sizes of Sinh Current Amplifier depicted in figure 6.22	83
6.4	Measured Sinh Current Amplifier results	87
7.1	Sinh Current Amplifier Specifications	94
8.1	Cases for table 8.2	100
8.2	Summary of the Power Supply Characteristics for Five Cases of Transmitter and Receiver Coils. Where X_{cr} receiver capacitor reactance, M = mutual inductance, P = Power of the transmitter source signal and $R_{eq} = X_{cr} * \text{Receiver's coil's } Q$. . Extracted from [93]	101
8.3	Frequency ranges used for ISM-systems	106
12.1	Sinh Current Amplifier Specifications	170

Dedicated to my parents...

Part I

Introduction

Chapter 1

Thesis Overview

At Imperial College London, since early 2005, a BBSRC / EPSRC - funded project termed ‘Intelligent Stem Cell Culture System’ (ISCCS) runs. The project aims: a) at the collection of in-situ and on-line physiochemical information from an ongoing stem cell (and in general cell) culture, and b) the biologically relevant interpretation of the collected spatiotemporal information. The ultimate and overarching scope of the project is to shed light on the physiology of stem cells from a different perspective perhaps contributing to the demystification of stem cell differentiation paths through the interpretation of the temporally evolving spatial profiles of the targeted physiochemical parameters.

The main research involved in the projects are three: a) miniaturized biocompatible biosensors capable of sensing physical or chemical parameters such as temperature, pH, oxygen, glucose and lactate. b) data acquisition electronics tailored to the specific biosensors and offering interfacing with amperometric sensors in the range of 0.1-10nAs and potentiometric sensors in the range of mVs. c) Bioreactors for bioprocessing. The specific project used two-dimensional bioreactors. Figure 1.1 shows a typical miniaturized biosensors used whereas figure 1.2 illustrates the bioreactor used. Figure 1.3 illustrates the bioreactor together with the sensors whereas figure 1.4 illustrates the bioreactor together with the biosensors inside the incubator.

The Intelligent Stem Cell Cultures Systems project aims at the concurrent in-situ and on-line monitoring of many cell cultures under the same or different conditions (parallel bioprocessing). The reason for this has to do with the hypothesis that the parallel physiochemical monitoring of many stem cell cultures should facilitate the study of differentiation paths and culture behavior in general. In practice however the need for



FIGURE 1.1: Miniaturized Biosensors

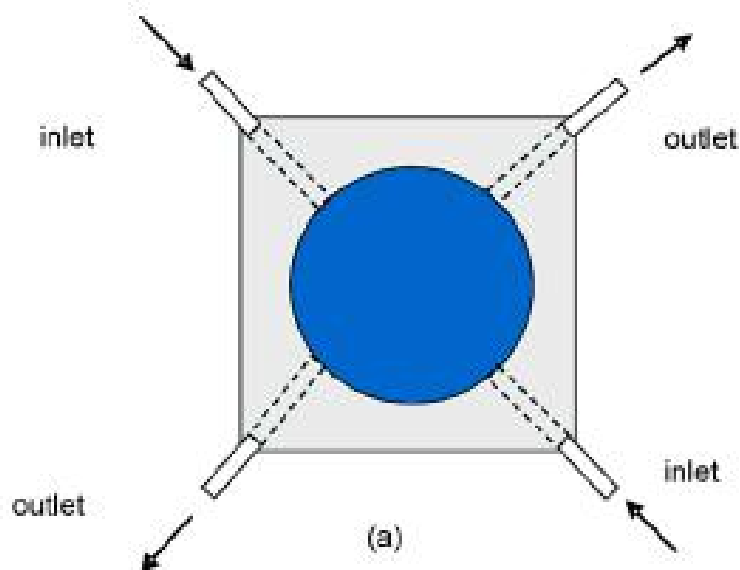


FIGURE 1.2: Model of a Typical Bioreactor

parallel bioprocessing translates into the need for a multi-channel data acquisition system.

As part of the ISCCS project, the ‘Bioinspired VLSI CAS Group’ of the Dept. of Bioengineering, under the leadership of Dr’s Xicai Yue and E. M. Drakakis has developed a new multi-channel sensor interfacing instrument tailored for cell culture monitoring purposes. The new instrument incorporates both hardware and software and its full details can be found in [1]. The platform can support up to 128 channels organized in 8 modules of 16 channels each. Each one of the modules can be either amperometric or potentiometric. Figure 1.5a and b illustrates the potentiometric and amperometric modules respectively.

As an example of the use of the new platforms Figure 1.6 illustrates the temporally evolving concentration of ammonia with a Mouse 3T3 fibroblast cell cultures over a period of 7 days.

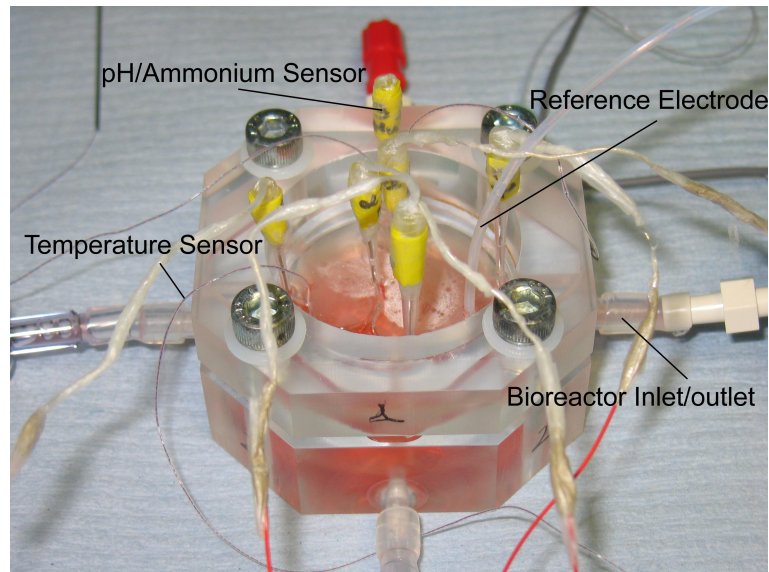


FIGURE 1.3: Bioreactor together with the Sensors

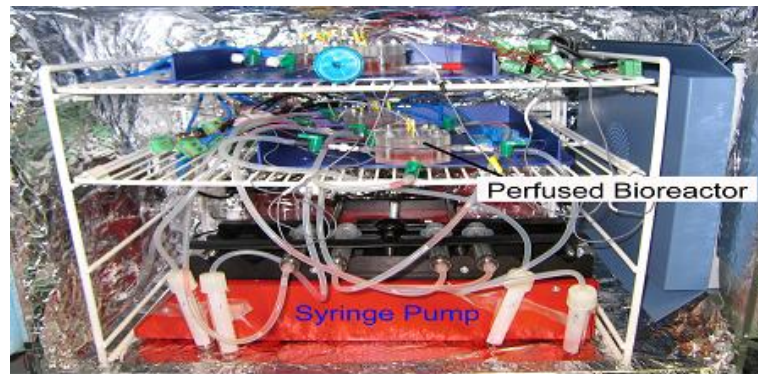


FIGURE 1.4: Bioreactor along with the biosensors placed within the incubator

The ISCCS project involved three full time post-docs one for each of the constituent areas of research involved i.e. one for biosensors, one for electronics and one for bio-processing. These three post-docs were accompanied by three PhD student, one on each of the three research areas.

The work presented in this thesis entails the research effort associated with the peripheral PhD study on the general area of electronics within the framework of the ISCCS projects.

This particular PhD thesis focuses on the design, analysis, synthesis, fabrication and testing of IC blocks suitable for current-sensors and short-range radio. The motivation behind the whole effort is to propose IC blocks that would allow, to a certain extent, the miniaturization of the sensor interfacing boards used by the ISCCS project.

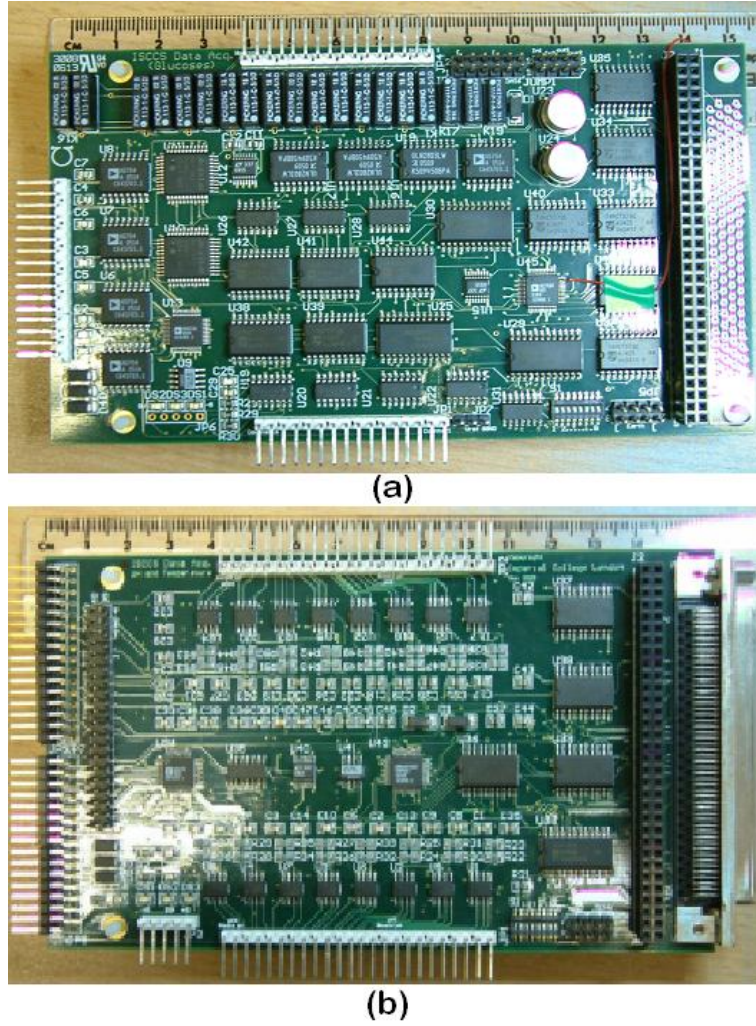


FIGURE 1.5: (a) Potentiometric and (b) Amperometric modules.

The research presented in this thesis focuses on a new current-mode hyperbolic-sine amplifier suitable for nA-range sensor current interfacing and on short-range 13.56MHz radio blocks.

The current amplifier is based upon the novel weak inversion Sinh synthesis techniques. The Sinh Current Amplifier is a novel circuit currently under patent. It utilizes MOS transistors in their weak inversion region exploiting their exponential relationship between the drain current and the gate source voltage. By doing this, an input current may be converted to a sinh intermediate voltage I_{in} -to- $\sinh(V_x)$ via a bias current I_0 . With a modification to the circuit, the reverse operation may be performed and a voltage to sinh current may be achieved ($\sinh(\sinh^{-1}(I_{in}))$ -to- I_{out}) by means of a bias current I_1 . In doing so a ‘current to sinh voltage to current’ (I to $\sinh(V_x)$ to I) conversion is performed, thereby making the amplifier circuit Externally Linear, but Internally Nonlinear (ELIN). The gain of the circuit is determined by the ratio of the current values I_1 and

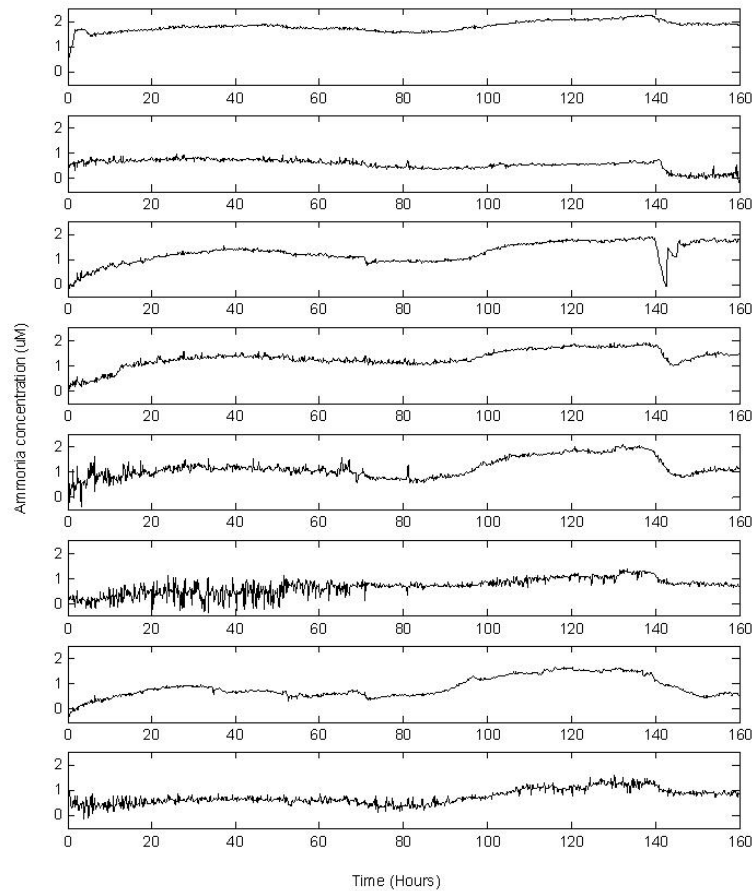


FIGURE 1.6: Concentration of ammonia with Mouse 3T3 fibroblast cell cultures over a period of 7 days. Each trace represents an electrode placed in a different location in the cell culture.

I_0 . Chapter 3 presents a literature review of present day sensor models. Chapter 4 and 5 deals with the synthesis and analysis issues of the new current amplifier. Chapter 6 presents simulated and measured results from fabricated and tested chips in the AMS $0.8\mu\text{m}$ and AMS $0.35\mu\text{m}$ technologies

The wireless unit consists of a single transmitter and receiver circuits. Both consist of a novel multi-tapped voltage controlled ring oscillator which allows the shift in frequency range of a basic VCO as well as reducing the high frequency feedback noise. The wireless unit operates within the 13.56MHz industrial-scientific-medical (ISM) band and is designed for a range of 5-10 cms. Whereas the transmitter works on the principle of Frequency Shift Keying, and is based around a VCO, the receiver consists of a Phase Locked Loop. Chapter 8 presents a literature review of present day radio system designs. Chapter 9 and Chapter 10 entails the design of a novel radio system's transmitter and receiver blocks, whereas Chapter 11 presents simulated and measured results from fabricated and tested chips in the AMS $0.8\mu\text{m}$ and AMS $0.35\mu\text{m}$ technologies

Chapter 2

Stem Cells: What are they and what is their general significance?

Many lower animals are able to regenerate amputated limbs, while mammals are unable to do this to the extent of animals such as the star fish and newt, humans are able to replace blood, skin and other tissue. The cells that allow for this regeneration and renewal of tissue are known as Stem Cells. Stem cells are the most fundamental building blocks of human life: Stem cells can replicate themselves or become specialized cells (such as skin, blood, muscle and nerve) depicted in figure 2.1. [2]

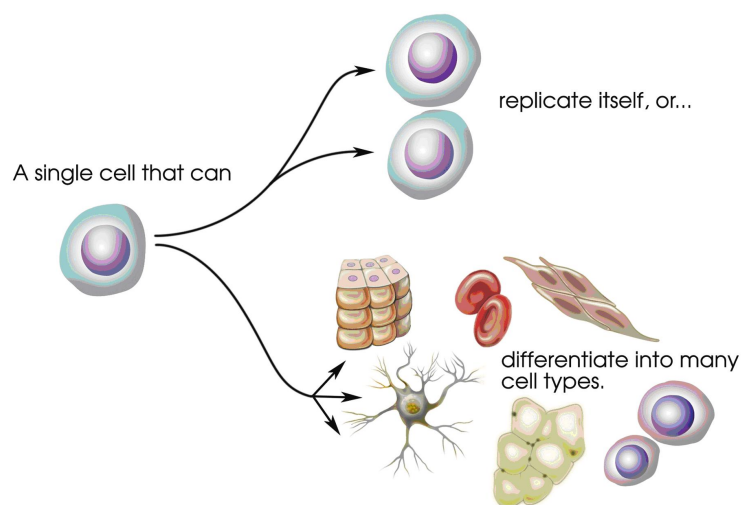


FIGURE 2.1: Stem Cells can proliferate or become specialized cells. Extracted from [2]

The fundamental difference between muscle, blood, nerve cells and stem cells is that stem cells are able to divide and renew themselves whereas muscle, blood and nerve

cells cannot. When stem cells multiply (replicate) themselves the process is termed proliferation, whereas when they transform into a specialized cell the process is termed differentiation.

2.1 Embryonic Stem Cells

The human body contains over two hundred different types of cells. These different cells are not present in a fertilized egg but are developed from a pool of stem cells that are located within the embryo. This pool will then proliferate, differentiate and finally give rise to every cell, organ and tissue of the fetus's body. There are two different classifications of stem cells - embryonic and adult ones. Embryonic stem cells are obtained by withdrawing the inner cell mass from a Blastocyst placed in a culture. The culture medium is then cultivated in the dish. Nutrients are released into the culture medium. The inner mass proliferates and outgrows the dish. At this time the medium is split up and placed into many dishes, and this process continues. [3]

A blastocyst is a 4-day-old embryo (developed 4 days after fertilization), and it contains the material for the construction of a full organism. The inner cell mass of the Blastocyst is composed of about 30-34 cells that are known as pluripotent as they have the unique ability to transform into any (and all) types of cells within the body. The outer layer of the Blastocyst goes on to form the placenta and other material required for the fetus to fully develop.

It is here that the ethical and moral debate of stem cells comes into play. Removing the inner cell mass provides scientists with the most basic building blocks of human life as we know it which have the potential to lead to cures of degenerative diseases. However, by removing the inner cell mass, the ability of the blastocyst to become a fetus is destroyed. Figure 2.2 shows the pathway of an embryonic stem cell culture. [4]

2.2 Adult Stem Cells

The second type of stem cells are adult stem cells. It was previously believed that they do not have the potential of embryonic stem cells. Adult stem cells reside deep within human organs. Blood, skin and the lining of the gut are but a few parts of the body

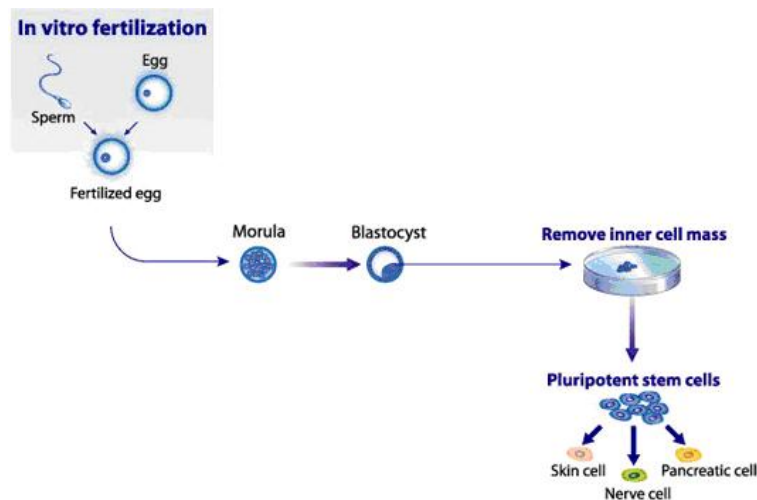


FIGURE 2.2: Embryonic Stem Cells Pathway. Extracted from [5]

which are constantly replenishing themselves. In those cases, stem cells are in constant use.

It was previously thought that haematopoietic (blood) stem cells were unable to become the cells of different tissues like nerve cells. Studies and research have allowed scientists to realize that stem cells have the potential to become cells of a completely different tissue than the one in which they reside in. This process has been termed Plasticity. The understanding of this phenomenon could lead to insulin producing liver cells, haematopoietic stem cells becoming the muscle of the heart as well as neurons. As adult stem cells are found within organs and tissue, they are surrounded by the organs and tissue and hence it is difficult to obtain them and preserve them in a lab. [7]

Figure 2.3 shows how stem cells residing within the bone are able to differentiate following a number of paths.

2.3 Summary

The ability of stem cells to replace dead or damaged tissue is why stem cells excite both medical doctors and biologists alike. Embryonic stem cells could provide a wealth of knowledge. However their use is shadowed by an ethical and moral discussion. Moreover there is a risk associated with the use of embryonic stem cells as they could lead to the creation of tumors in the subject where the undifferentiated cells have been implanted. Adult stem cells on the other hand both overcome the ethical debate and they

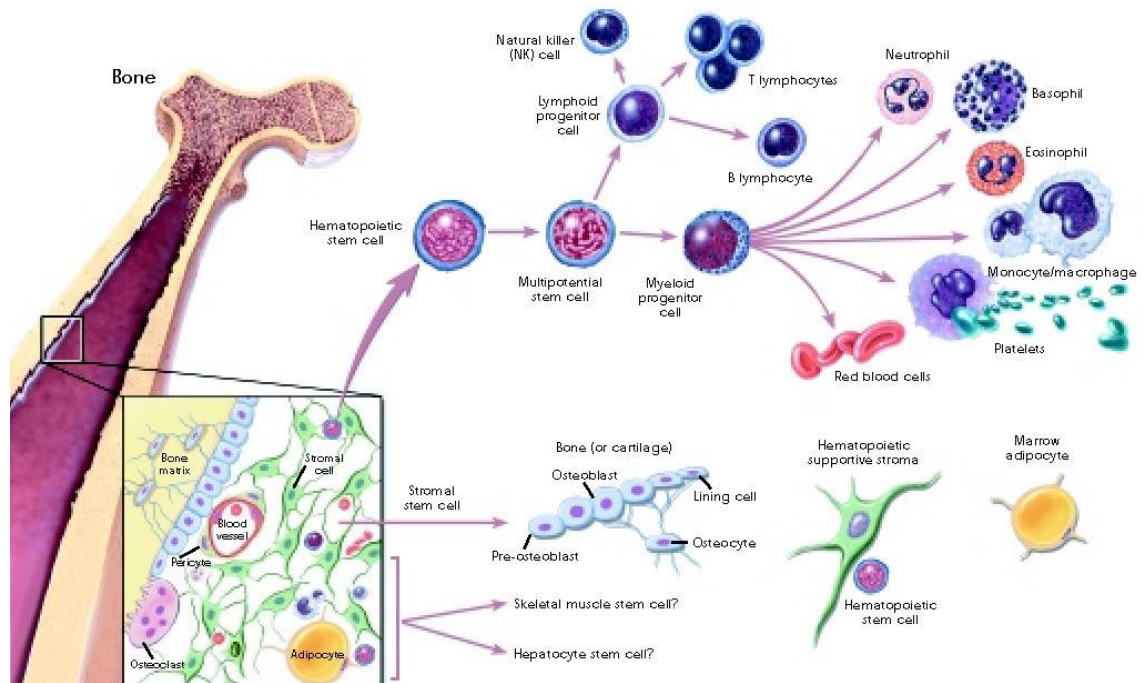


FIGURE 2.3: Bone stem cell differentiation pathways. Extracted from [6]

do not seem to cause cancer. However they are difficult to identify, maintain and grow in a lab. Today stem cells are predicted to be able to treat at some point Parkinson's disease, diabetes, heart disease, spinal cord injury, Alzheimer's and vision loss. [8] [9] [10]

As explained in Chapter 1 the circuit research presented in this Thesis is motivated by the need for miniaturizing of a multi-channel (up-to-128 channel) physiological monitoring platform which in turn aims at the acquisition of temporarily evolving spatial profiles of physiochemical parameters during the growth of stem cell cultures.

Part II

Sensor Interfacing Circuitry

Chapter 3

Overview of Sensor Interfacing Circuits

Sensors are essential for medical research. By monitoring a chemical experiment with accurate sensors, an engineer would be able to understand and further the knowledge of that reaction. It is with a greater understanding of biological reactions that makes it possible to cure and prevent diseases.

There are various and numerous types of sensors that are available on the market. A sensor is defined as a component which changes a real world signal such as temperature, pressure etc into an electrical signal. However, there are also Sensor Interface Circuits whose existence is due to the electrical signals (previously mentioned) requiring signal conditioning. This conditioning may take on the appearance of amplification, current-to-voltage conversion, digitization or a combination of the aforementioned methods.

This chapter reviews literature on present day sensor models. Initially elementary capacitive and resistive models used to sense pressure, mis-alignment, heartbeats and cerebrospinal fluid pressure within the brain were considered. However due to the limitations of the aforementioned sensors, the more sophisticated potentiostat is explored. The potentiostat allows CO_2 , glucose and electrolyte solutions to be characterized by monitoring the solution under electrical stimulation. Subsequently the three-electrode potentiostat is analytically described via its electrical model. Potentiostat-based sensor systems are finally illustrated in detail.

3.1 Piezoelectric / Resistive Sensors

In 1880 at the French Academy of Science, the Curie brothers told the audience that they had discovered the piezoelectric effect. The brothers realized that some materials had the property to transform pressure into an electrical output. When for example, quartz has pressure applied to or relieved from it, then an electric current would be induced with a positive or negative sign respectively. The Curies set up an experiment where a crystal specimen was sandwiched between two copper plates. The plates were then connected to a Thomson electrometer. Applying and relieving stress showed a charging in opposite polarities. [11]

Even though the Curies discovered the piezoelectric effect in the late 19th century, it took till the 1950's for the phenomenon to be exploited industrially. In the past sixty years, the applications of piezoelectric devices have been vast. As a piezoelectric sensor can measure pressure, acceleration strain or force, it has practical applications in the following areas:

- Aerospace Engineering: accelerometers, gyroscopes (to measure acceleration) and level sensors
- Ballistics: velocity, impact, sound sensors
- Engine Testing: dynamic stressing
- Engineering: medical ultrasound, SONAR devices, shock and vibration isolation
- Industry: strain gouges, engine management systems (sample the vibrations of the engine block), acoustic emission testing.
- Miscellaneous: Loudspeakers, ink jet printers, microscopes and quartz clocks to name just a few.

The role of the piezoelectric effect in a force sensor is shown in figure 3.1. Compressing the plates, will result in a charge proportional to the force. However if the plates had a voltage applied across them, then the electric field would cause a realignment and the material would be deformed. This is used in speakers (voltage to mechanical compression) and microphones (mechanical to electrical conversion). [13]

A common setup of using the piezoelectric effect as a sensor is in the Wheatstone bridge depicted in figure 3.2. Two polysilicon resistors are used, which are placed on the silicon

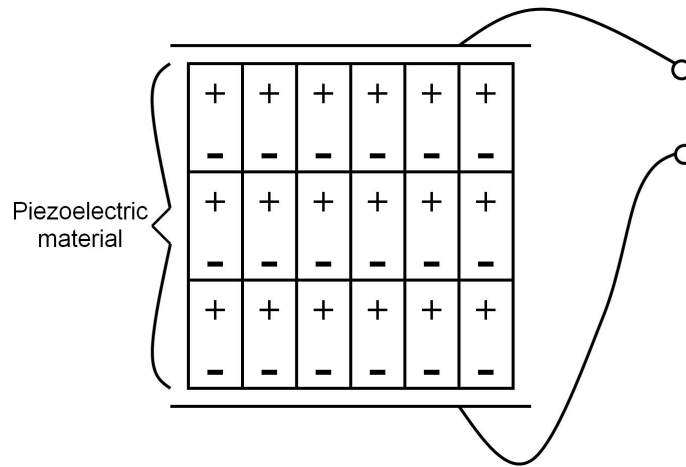


FIGURE 3.1: Theoretical setup of a piezoelectric sensor. Extracted from [11]

nitride membrane. The resistors are positioned at the edge of the membrane where they are exposed to the greatest stresses and strains.

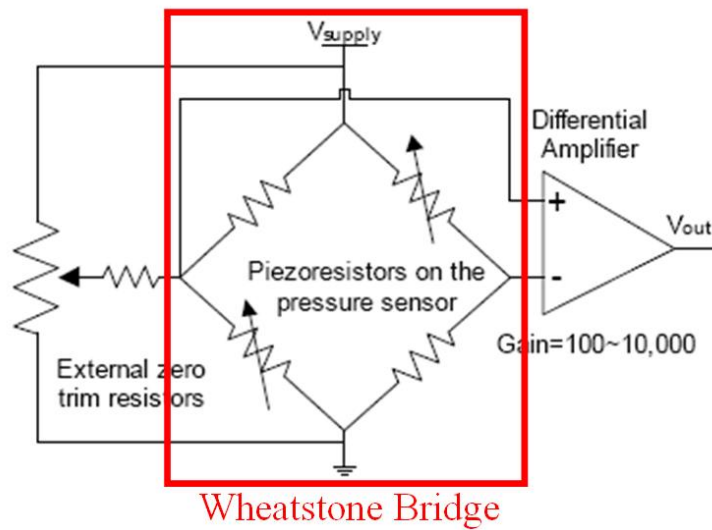


FIGURE 3.2: Wheatstone bridge-based sensor comprising of piezoresistors and polysilicon resistors. Extracted from [14]

The circuit in figure 3.3 shows a similar setup. However in this case the engineers have also incorporated a wireless unit which transmits the sensed data. Specifically, in this configuration, the piezoresistive device is used as a bending beam (R_3 acts as the beam, and R_4 is used for calibration). The applied pressure causes a varying voltage to be fed into the differential amplifier AMP04. This circuit can be used as a rotation sensor. [15]

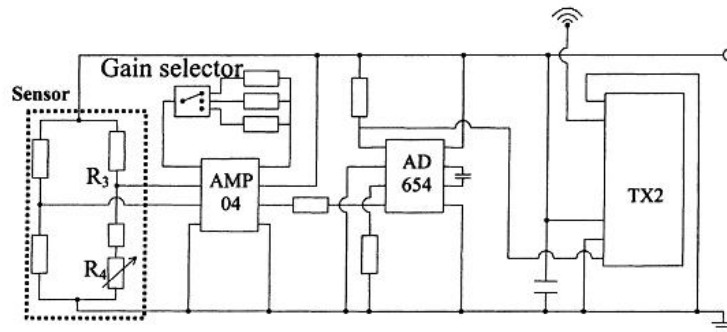


FIGURE 3.3: Rotation sensor using a Wheatstone Bridge. Extracted from [15]

3.2 Capacitive Sensors

Physically speaking, a capacitor consists of two conductive plates with a non-conducting dielectric material sandwiched in between. Due to the dielectric being non-conductive, no current will flow through it but there will be a potential difference between the plates. As the two plates are oppositely charged, an electric field will exist between them. If now, one of the plates is fixed and the second is suspended, then as the second vibrates, a changing capacitance value is induced which can be monitored. Since the capacitor value is proportional to area, then a smaller capacitor will be far more sensitive than a larger one [17]. If Δx represents the maximum possible misalignment of the two plates due to vibrations, should a small capacitor be used, then the capacitor value variation will be large in comparison to the capacitor size. If the capacitor was large, then the variation will be small in comparison to the capacitor size.

Whereas piezoelectric materials provide sensing information when they are stressed, the capacitive devices measure/sense by means of the displacement of their plates with respect to one another [18] [19]. Figure 3.4 codifies schematically the variations when the capacitor is stressed.

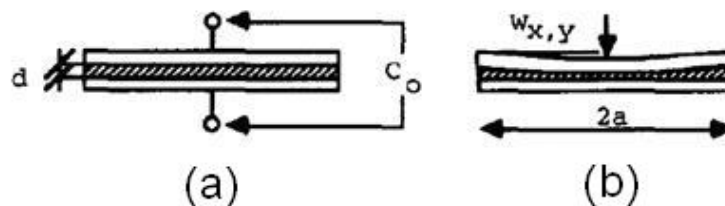


FIGURE 3.4: Capacitor in normal state (a) and when under pressure (b). Extracted from [20]

The capacitance value C is given by equation 3.1,

$$C = \epsilon \frac{\text{Area}}{d} \quad (3.1)$$

Where ϵ denotes the dielectric constant value and d denotes the distance.

The capacitive effect used as a sensor is shown in figure 3.5.

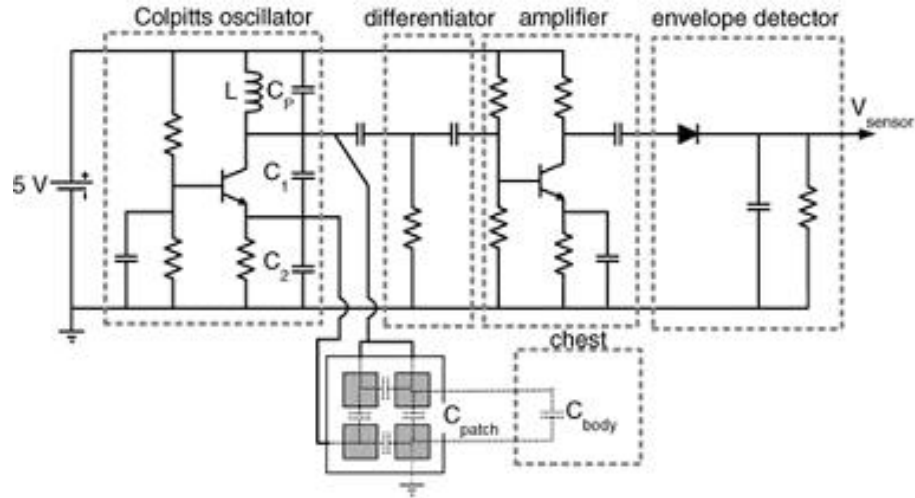


FIGURE 3.5: Capacitive Heartbeat Sensor. Extracted from [21]

The sensor is based on a Colpitts oscillator whose capacitance is varied by cardiac and respiratory activities. The frequency of oscillation provides a representation of the heartbeat and respiration. Capacitive electrodes are placed upon a piece of cloth with the electrodes arranged in a square of four patches. Figure 3.6 illustrates the model of the electrodes placed on the body.

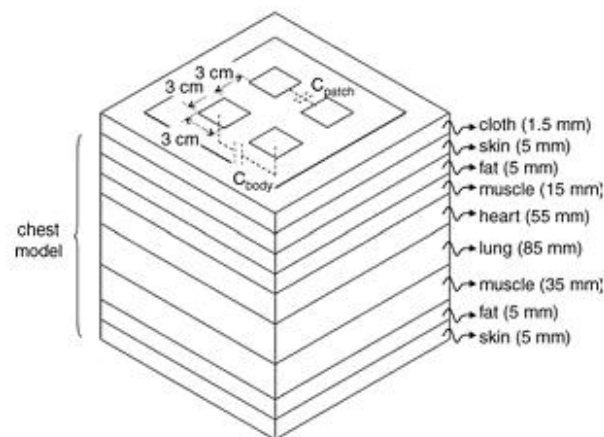


FIGURE 3.6: Model of the patch electrodes placed on the chest. Extracted from [21]

The capacitive sensor is also used in the cerebrospinal fluid (CSF) shunt system [22]. CSF is the fluid which protects the brain tissue and transfers nutrients. The CSF is

absorbed into the bloodstream after it flows to the base of the brain. Hydrocephalus is a neurological disease due to unregulated increments in intracranial pressure that arises due to CSF pooling in the brain. The CSF shunt system consists of a micro-telemetry pressure sensor, a micro-pump and a controller. The microcontroller pressure sensor is an LC Oscillator designed with a pressure sensitive capacitor and an inductor. The resonator may then be implanted within the skull and can be magnetically coupled to an external detector. Figure 3.7 illustrates the CSF shunt system. An increase in the intracranial pressure compresses the sensor shifting the phase near the resonance frequency.

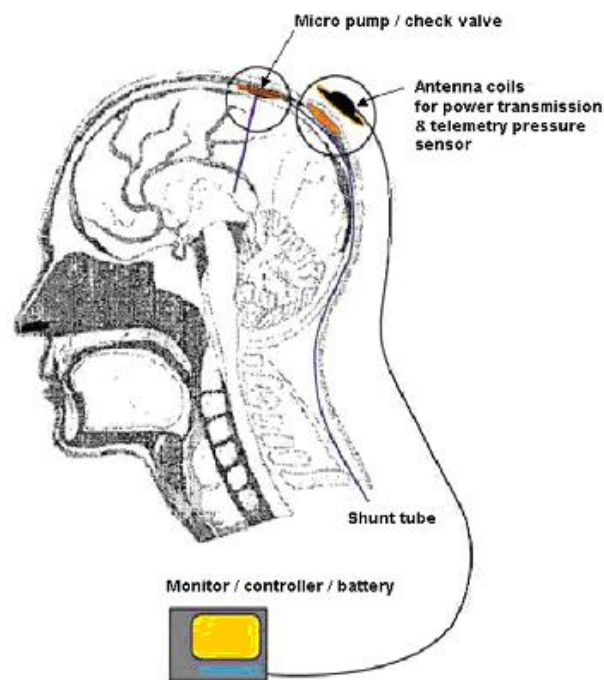


FIGURE 3.7: CSF shunt system implementation. Extracted from [22]

Figure 3.8 illustrates the pressure sensor. The Cr/Au electrode situated the p+ diaphragm and the Cr/Au electrode on the Pyrex glass creates the variable capacitance.

3.3 Potentiostats

In 1942, the term ‘potentiostat’ was coined by Hickling, who designed and produced the first three electrode version. Later he presented its ability to further knowledge in the areas of iodide oxidation and solution stripping [24]. However the true potential of the potentiostat was only realized in the 1960’s when it was used for corrosion research

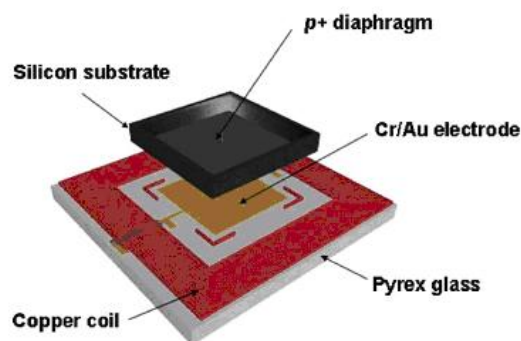


FIGURE 3.8: Wireless LC based pressure sensor. Extracted from [22]

(such as atmospheric corrosion and corrosion in structures as well as other types of steel) [25].

A potentiostat is a specific piece of (research) equipment that has allowed engineers to obtain a far greater understanding of many chemical reactions that take place in nature and in a laboratory [26]. Potentiostats essentially may be considered as an analytical tool which allows a scientist to evaluate, characterize and identify organic, inorganic and biochemical specimens. One specific use has been the measurement of the dielectric attributes of biological tissue, cells and molecules. For this application, a potential is applied to a cell culture and the output current frequency would be taken as a measure of the studied reaction. More present day applications of the potentiostat include the in-vivo detection of analytes like glucose and catechol amines [27], food control, and the of analysis blood [28].

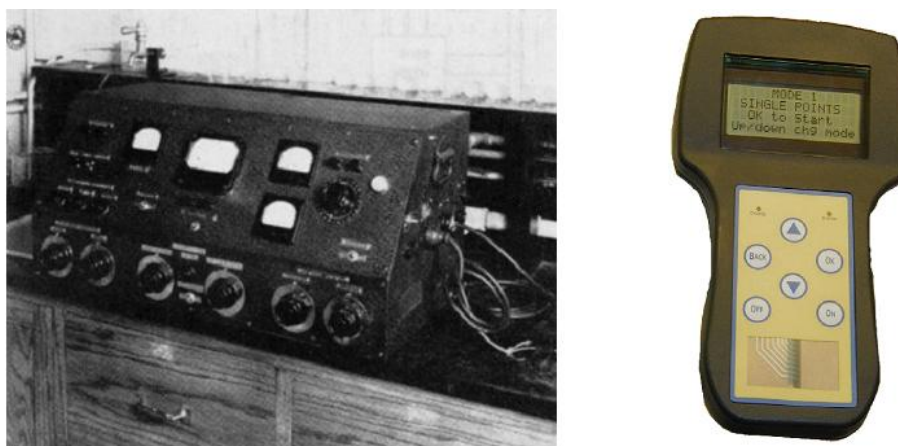


FIGURE 3.9: Potentiostat from the 1940's (left) [29], and 2000's (right) [30]

One of the first potentiostats built in the 1940's is shown in figure 3.9. Commercial providers were Caldwell, Parker and Diehl. Adjacent to it is a present day handheld model.

3.3.1 Two Electrode Potentiostat

The material covered in this section is based primarily on references [31] and [32]

The theoretical construct of the two electrode potentiostat is shown in figure 3.10. In order for a reaction to occur, the potential drop across the working electrode (called so, as it is where the reactions occur) must be above a particular value. The reaction takes place between the working electrode (WE) and the electrolyte (solution in which the working electrode is immersed). In order to complete the circuit, a counter electrode (CE) is also inserted in the solution. The potential difference across the WE and CE is set to the desired value for the specific reaction to take place, and the output (current) is taken from the grounded working electrode.

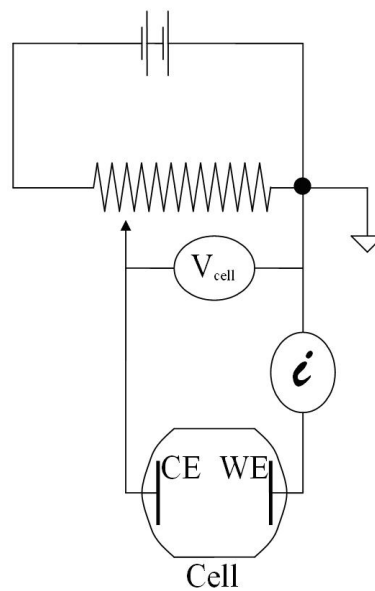


FIGURE 3.10: Typical two electrode potentiostat. Extracted from [32]

The current output from the WE gives a measure of the concentration of the electrolyte solution. Providing a variable (saw-tooth) input also allows the reaction time of the electrolyte to be recorded. The CE is chosen to have a high redox rate in order to reduce the CE's sensitivity to current variations (as long as the current is kept small). Hence the potential across the CE is kept practically constant. Therefore, the output current is directly related only to the reaction taking place at the working electrode - electrolyte interface.

The voltage V_{cell} is a combination of three separate potential drops: the potential V_{CE} across the CE, the electrolyte potential V_{elec} ($I_{electrolyte} * R_{electrolyte} = V_{elec}$) and, the WE

potential V_{WE} . In order for a reliable and descriptive current output to be obtained from the WE, V_{WE} should remain constant so that I_{WE} carries the information of the reaction.

Figure 3.11a illustrates a model of a two electrode potentiostat. Under zero current conditions (and as CE has a high redox rate), the potentials V_{CE} and V_{WE} remain constant (figure 3.11b). If a non-zero current is present (figure 3.11c), then V_{elec} would increase and as V_{cell} is fixed, V_{WE} would reduce to compensate. In this case both V_{WE} and I_{WE} are varying. With two variables, the results become unreliable. However if V_{RE-WE} (V_{CELL}) is kept constant, then only I_{WE} would vary as the reaction takes place, and I_{WE} would ‘carry’ all of the relevant information of the reaction.

3.3.2 Three Electrode Potentiostat

The material covered in this section is based primarily on references [32], [33], [34], [35], [36] and [37]

Figure 3.12 illustrates a typical three electrode potentiostat.

The Reference Electrode (RE illustrated in figure 3.12) is used to measure the working electrode’s potential. In order for it to not affect the reaction, no current should flow through it. In other words the RE should have a very high input impedance. Usually the RE is constructed from silver/silver chloride (Ag/AgCl). The counter electrode has a similar function; it must not interfere with the reaction, but it must provide the required current and ‘close the circuit’. In fact the counter electrode’s main function is to complete the circuit [32].

The reference electrode plays a vital role in ensuring reliable results may be collected from the working electrode.

For reliable results, V_{WE} should remain stable, Figure 3.11d illustrates the simple model of a three electrode potentiostat. Under the zero current conditions (figure 3.11e), V_{cell} is at the desired potential. If the current increases (figure 3.11f), then as previously V_{elec} increases and V_{WE} decreases and so V_{cell} drops. Therefore, for a constant V_{WE} (figure 3.11g), V_{C-RE} is increased returning V_{WE} (and V_{cell}) to its original value.

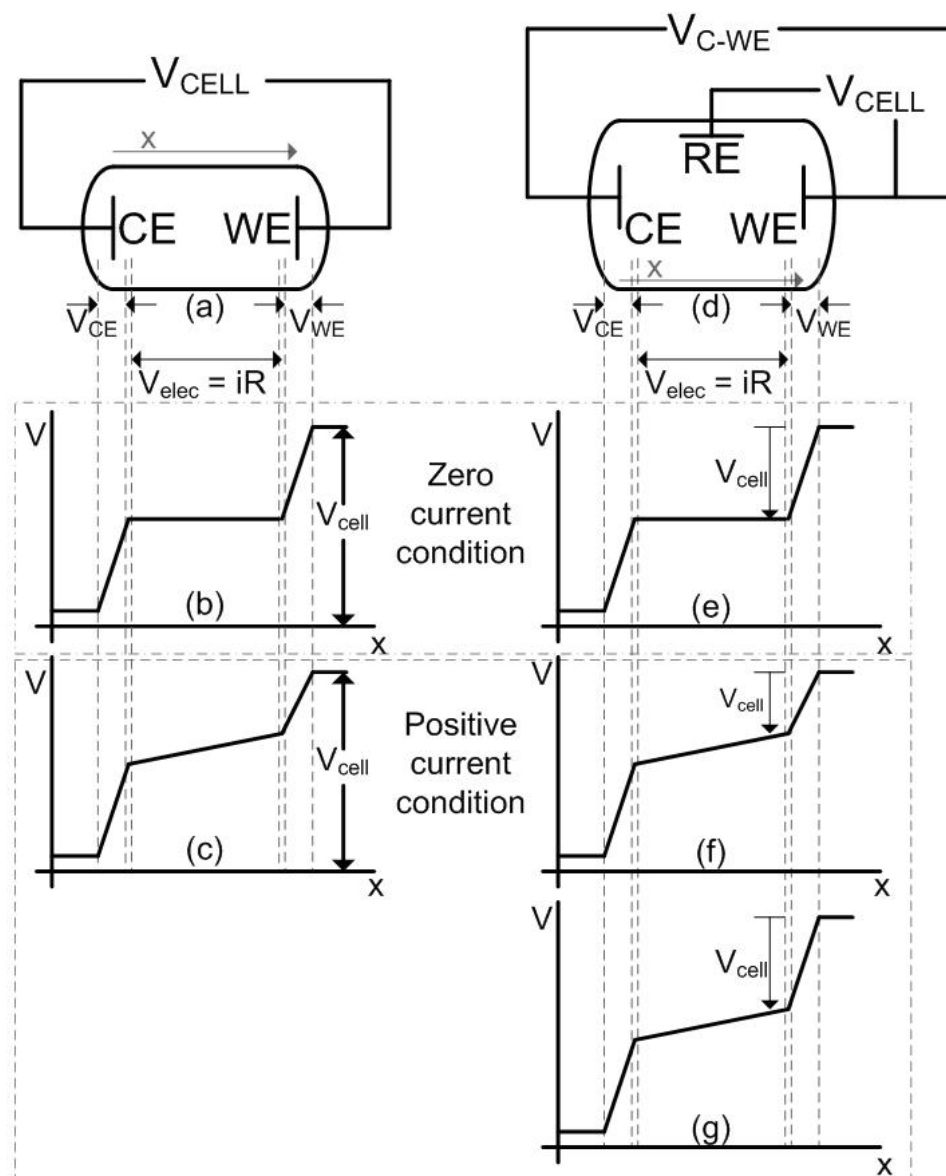


FIGURE 3.11: (a) Two electrode potentiostat, (b) zero current conditions, (c) positive current conditions, (d) Three electrode potentiostat, (e) zero current conditions, (f) positive current conditions, (g) positive current conditions with V_{WE} held constant.

Extracted from [32]

3.3.3 Peripheral Circuitry

Figure 3.13 depicts the basic three electrode potentiostat with a typical set of surrounding circuitry. The output stage consists of a standard current amplifier configuration with the current from the working electrode being fed into a virtual ground node. By creating the working electrode - virtual ground connection, a low impedance path is created for current to flow from the working electrode to the current amplifier without restriction.

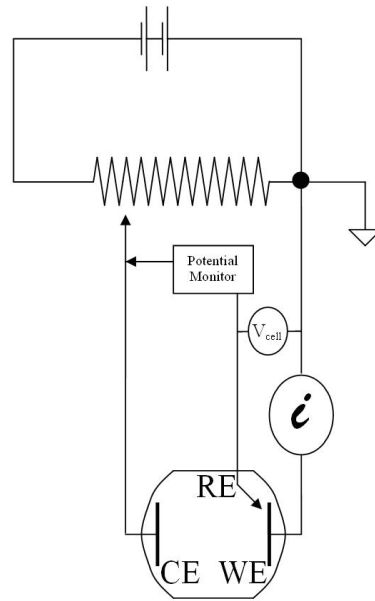


FIGURE 3.12: Typical Three electrode potentiostat. Extracted from [32]

Figure 3.13 illustrates the circuit analysis of the three-electrode potentiostat.

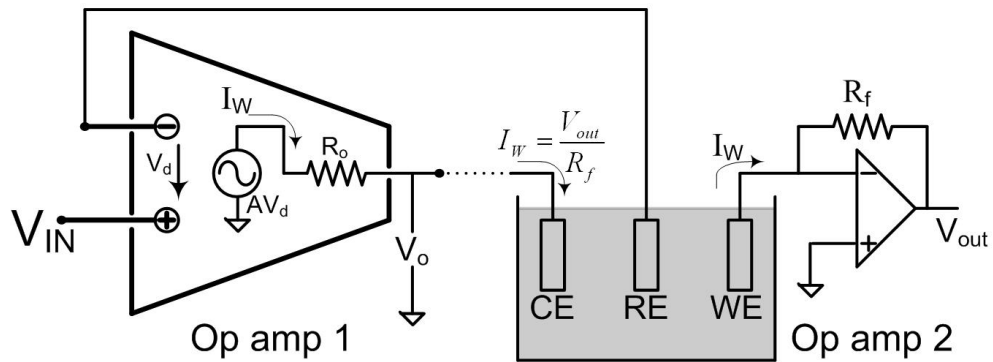


FIGURE 3.13: Typical Three electrode potentiostat circuit analysis

Clearly

$$AV_d - I_W R_o - V_o = 0 \quad (3.2)$$

Rearranging 3.2 gives 3.3

$$V_o = AV_d - I_W R_o \quad (3.3)$$

Substituting $V_d = (V_{IN} - V_{RE})$ into 3.3 yields 3.4,

$$V_o = A(V_{IN} - V_{RE}) - I_W R_o \quad (3.4)$$

As $I_W = -\frac{V_{out}}{R_f}$ then,

$$V_o = \frac{R_o}{R_f} V_{out} + A(V_{IN} - V_{RE}) \quad (3.5)$$

The requirement of op-amp2 in figure 3.13 is to amplify the low amplitude current I_W .

3.3.4 Randles Electrode Model

The material covered in this section is based primarily on references [33], [39], [40], [41] and [42]

In order to obtain a greater understanding of the internal operation of the potentiostat, the electrolyte and electrode will be replaced by electrical models. Figure 3.14 illustrates ‘Randles equivalent model’ for an electrode in a solution. Randles model represents a coated electrode that has been submerged in an electrolyte.

- R_S - impedance of the electrolyte solution between the reference electrode tip and the surface of the working electrode.
- C_C - double layer capacitance of the coating of the working electrode which is defined by the thickness and dielectric constant of the electrode.
- R_C is the impedance of the working electrode.

Randles model reveals handily the effect the parallel resistance and capacitance will have. The typical frequency response of the passive circuit equivalent depicted in figure 3.14 is given in figure 3.15,

Referring to figure 3.15, at low frequencies the total magnitude is a combination of R_S and R_W (where R_W is the parallel combination of R_C and C_C). At higher frequencies however, the capacitor C_C becomes short circuited and R_S remains as the dominant term.

An example of a practically used electrochemical cell is shown in figure 3.16. The potentiostat is used for Electrochemical Impedance Spectroscopy (EIS). The working,

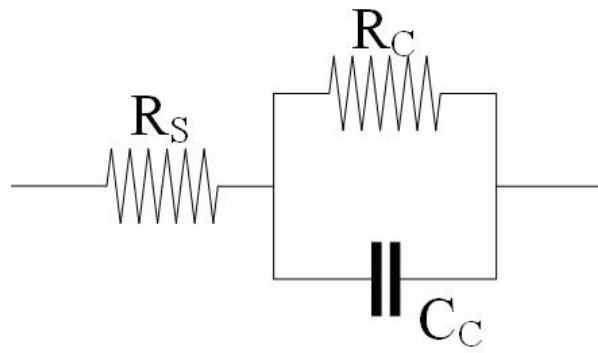


FIGURE 3.14: Randles equivalent model of an electrode in electrolyte. Extracted from [43]

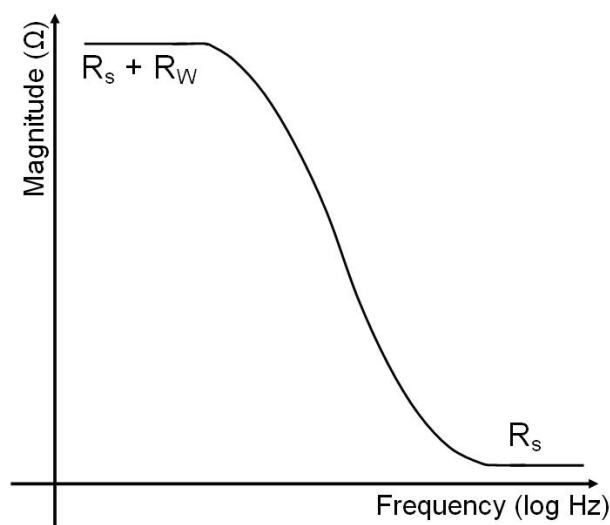


FIGURE 3.15: AC response of the Randles equivalent model, R_w corresponds to the parallel combination of R_c and C_c . Extracted from [44]

reference and counter electrodes are submerged into an electrolytic solution (5% salt water). In this case the RE is typically a saturated calomel electrode (SCE) and the CE tends to be an inert material (carbon / platinum). The potentiostat circuitry must provide both DC and AC excitation to the counter electrode, as well as recording the result from the working electrode. The recorded information can be used to calculate the impedance of the electrolyte.

In this specific case [45] “a small (5-10mV) amplitude ac signal is applied to the sample by the potentiostat and the current response is analyzed to extract the phase and amplitude relationship between the current and voltage signals”. With these data, the electrolyte solution can be fully characterized. Due to the requirement for precise results, a signal of 1mHz was applied meaning the time period of the waveform would be

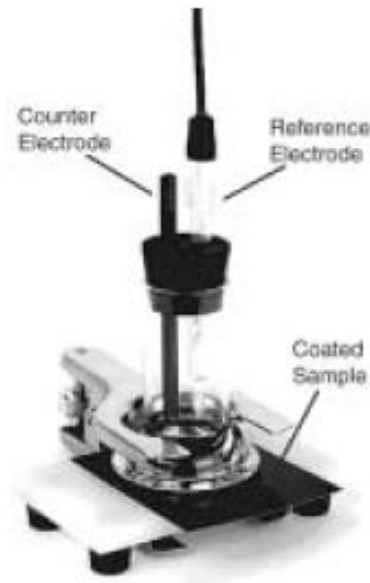


FIGURE 3.16: Electrochemical Cell. Extracted from [46]

16mins and 40seconds [46]. This time frame specifies the longevity required in order for the reaction to occur.

A more detailed version of Randles circuit is depicted in figure 3.17. Positively charged oxidants move towards the negatively charged electrode and charge transfer occurs creating reductants. Subsequently the reductants move towards the bulk of the electrolyte. IHP and OHP represent the inner and outer Helmholtz planes, respectively and exist around the electrode where charge transfer occurs.

- R_s - impedance of the electrolyte fluid
- C_d - double layer capacitance defined by the total of the combined charges in the electrode and the ions within the solution.
- R_p - charge transfer resistance created by the current flowing due to the reaction at the electrode - electrolyte interface.
- R_w - the Warburg impedance represents the limit of the diffusion process due to the ions within the solution. [47]

Utilizing Randles model of figure 3.17, allows the potentiostat figure 3.13 to be redrawn in an equivalent manner as in figure 3.18.

Note how, as the reference electrode has no current flowing through it, is considered to be a single impedance.

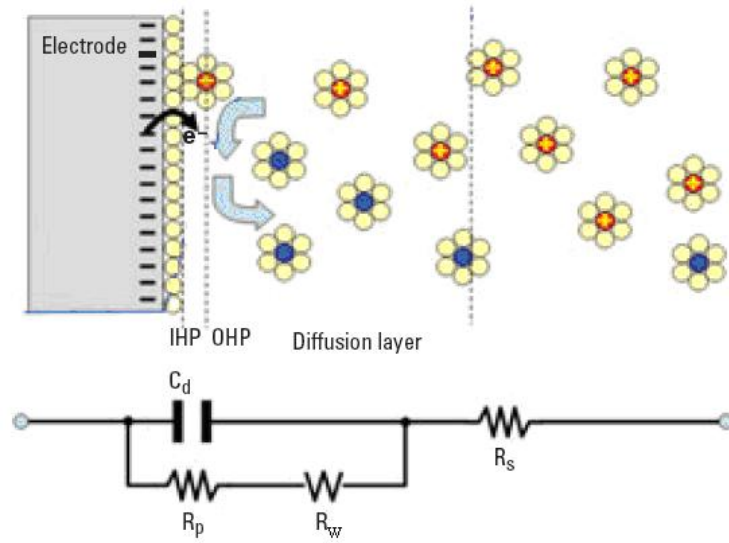


FIGURE 3.17: Electrode / Electrolyte Interface Model. Extracted from [48]

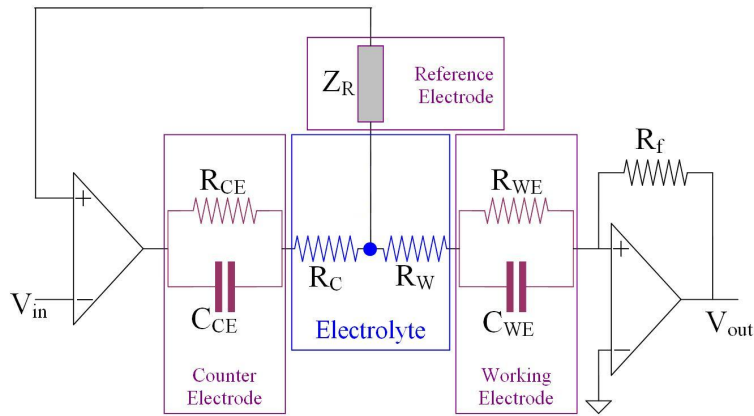


FIGURE 3.18: Three electrode potentiostat theoretical setup. Extracted from [44]

3.3.5 Literature Review

The two electrode potentiostat suffers from the disadvantage that potential across the working electrode cannot be controlled (section 3.3.1). However its simplicity makes it desirable for some applications. Figure 3.19 describes a two electrode potentiostat designed by Narula and Harris (University of Florida).

Assume that at the beginning of the experiment the RESET is initiated. The capacitor C_d will be pre-charged to V_{dd} , henceforth the capacitor will then discharge via the working electrode - that is, the charge stored on the capacitor will dissipate through the working electrode at a rate controlled by the WE / electrolyte reaction. When the potential of C_d reaches V_{ref} , an output pulse is generated, and a reset pulse is initiated.

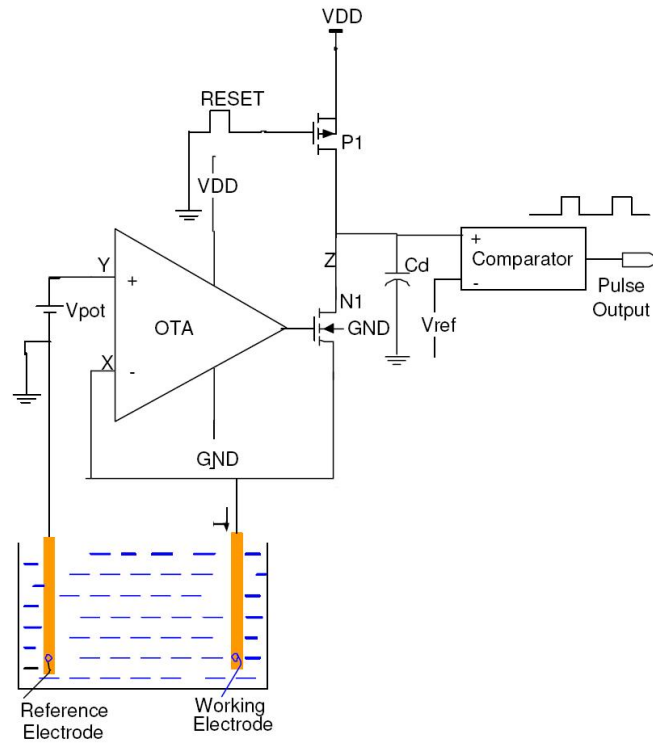


FIGURE 3.19: Two electrode potentiostat based on charging and discharging C_d . Extracted from [49]

A practical three electrode potentiostat has also been presented by scientists at Stanford University who designed a miniaturized three electrode version for electro-analytical instrumentation. In this case a DA converter (shown in figure 3.20) is used to set the potential difference between the working and reference electrodes. The control amplifier is used to analytically compare the desired counter electrode potential while taking into account the reference electrode's potential. Finally the working electrode current is sensed via a current input based AD converter [50].

Experimentally, a thin film Iridium electrode submerged in de-ionized water is connected to the chip. In order to characterize the solution, the counter electrode is driven with a triangular waveform. To interpret the response of the potentiostat, the output is measured and plotted on a current vs voltage plot.

Engineers from the University of Michigan describe the design of a single ended potentiostat shown in figure 3.21. A slight modification is presented in the reference - counter (AE) electrode loop, where the input potential is added to that of the reference electrode. OP1 in figure 3.21 is configured as a voltage follower, as such (nearly) no current will flow from the cell through the reference electrode. The function of OP3 is simply to provide a current to voltage conversion with gain and a virtual ground node.

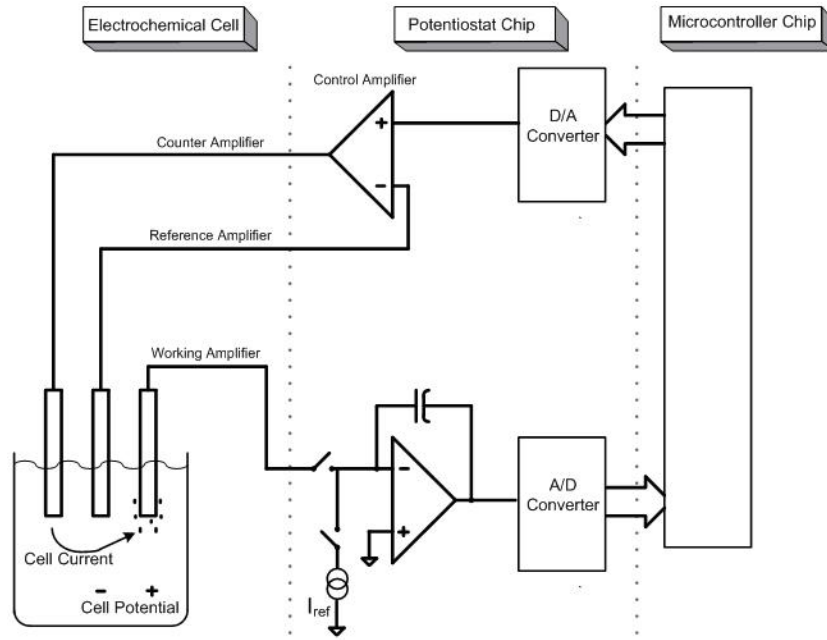


FIGURE 3.20: Three electrode potentiostat from Stanford.. Extracted from [50]

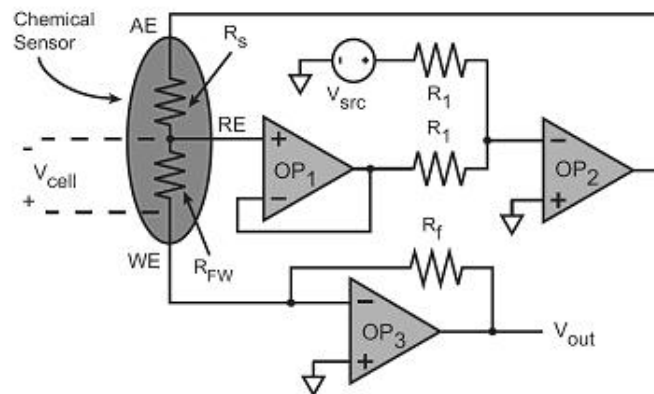


FIGURE 3.21: Single ended potentiostat. Extracted from [51]

The test circuit is described in detail in figure 3.22. The electrode-electrolyte interface is modelled by a simple series resistance. The results of the AE (auxiliary electrode also known as the counter electrode), reference and working electrode are plotted on an Agilent 54641 oscilloscope.

The potentiostat shown in figure 3.23 was designed as a collaboration of two Taiwanese universities [52]. An amplifier block is used to measure the potential difference between the reference and working electrode. The result of this provides information on whether the potential of the reference electrode reaches the desired voltage or not. ADC^{-1} dictates the operation of the microprocessor to decide and provide the signal that is required for the D/A converter to efficiently drive the potentiostats interfacing

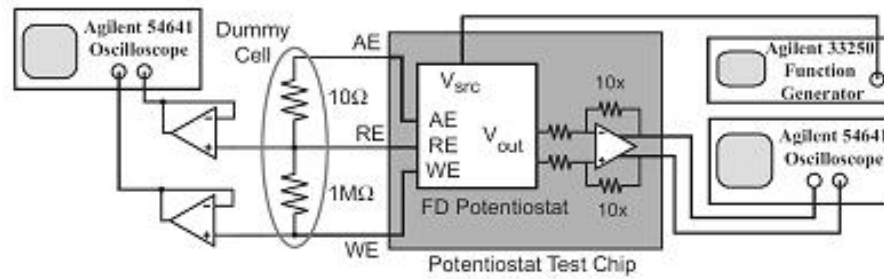


FIGURE 3.22: Test circuit for the potentiostat of figure. Extracted from 3.21. [51]

circuitry. The D/A converters function is to control the current through the cell by applying the sufficient voltage to the counter electrode. The feedback iteration process proceeds till the potential between the reference electrode and ground is at the desired level.

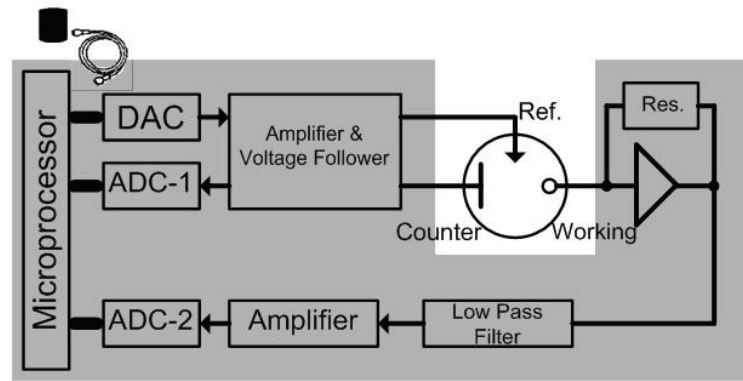


FIGURE 3.23: Microprocessor-based potentiostat. Extracted from [52]

A smart chip has been designed by an international team of engineers [53], it consists of a number of potentiostatic sensors (one of which is shown in figure 3.24), ADC's, microcontroller and other systems. The Op-Amp 1, Op-Amp 2, R_1 and R_2 loop provides a modified voltage follower circuit which is excited by the triangular wave generated by the Op-Amp 3 - C_{ext} loop. The triangular waveform provides cyclic voltammetry in order to characterize the electrolytic solution. A simple transimpedance amplifier is used for the current output (from the working electrode) to voltage conversion.

The next paper described is a collaboration of a number of South Korean universities. Their design consists of a three-stage unit. It contains an electrochemical potentiostat sensor, an ADC, a microcontroller and a wireless RF device to transmit the sensed data [54]. Figure 3.25 shows the sensing part of the circuit. The DA converter is used to set the desired value for the working electrode reaction to occur. Op-amp-1 reads the desired value from the DA converter and processes it against the potential on the reference

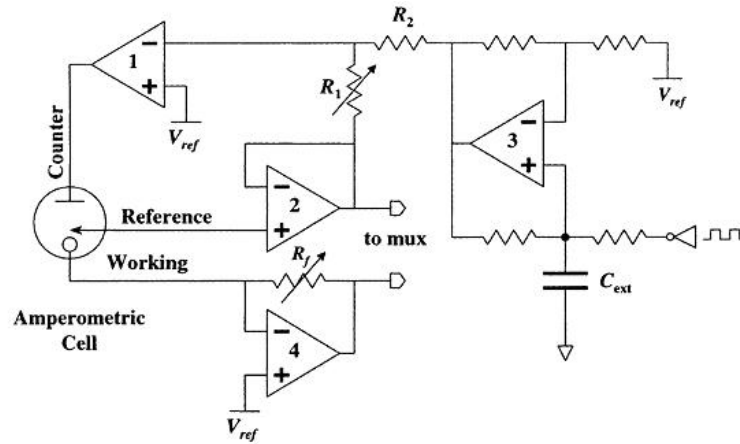


FIGURE 3.24: Potentiostat with triangular excitement. Extracted from [53]

electrode. The reference electrode is Ag/AgCl, the counter electrode is constructed from platinum, while microfabricated mercury makes up the working electrode. The output is taken from the working electrode and is connected to an op-amp in current amplifying configuration.

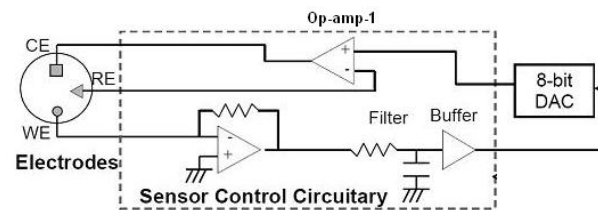


FIGURE 3.25: Potentiostat driven with a DA converter. Extracted from [54]

3.4 Summary

Over time, the methods used to sense real world signals have changed. Through advancing technologies and building upon the knowledge already known, sensors and their interfacing circuits have become more sophisticated. Presently the standard method of current amplification is the use of a potentiostat when attempting to characterize (concentration of CO_2 , glucose, etc) an electrolyte. However, the potentiostat's setup (peripheral circuitry) has not varied much in the past decade. Many present day potentiostat-based sensors all use the standard structure for the amplification of current. The output of the potentiostat consists of a simple current amplifying op-amp. This in itself is an inherently bad design for low currents. If for example, the current being sensed by the potentiostat is in the range of 100's pA - 1nA, then a resistor of $1G\Omega$ would be

required for sufficient amplification. Along with the difficulty of obtaining an accurate $1\text{G}\Omega$ resistor, there are a number of other inherent problems that would arise. The noise contribution by a resistor of this size is comparable to the size of the signal itself. Many op-amps also consume high amounts of power and require external binary and other components. These factors make the current amplifying op-amp undesirable.

Chapter 4

CMOS Current Conveyors

A Potentiostat is an electrochemical device which allows the characterization of an electrolytic solution. The potentiostat's current output is too small for direct monitoring and hence requires signal processing in order for it to be recorded. Traditionally the working electrode current is passed through an op-amp in current amplifier configuration. The op-amp performs two functions.

1. To provide a virtual ground - low impedance node for the working electrode current to be driven into, and
2. To provide amplification for the aforementioned current to be recorded.

This and subsequent chapters try to emulate this operation with current mode circuits. While the proceeding chapter dictate the design of a current mode amplifier, this chapter discusses the design of a current mode circuit which provides a low impedance virtual ground node. [\[55\]](#)

4.1 General

The current conveyor is one of the most useful blocks in current mode design. It has the ability to perform a number of various analog signal processing functions. The current conveyor was first introduced in the late 60's by Sedra and Smith. The idea was not taken up by many engineers, who saw the op-amp as the gateway to the future for advancements in technology and commerciality. Despite this, current conveyors

have had a noticeable impact on analog design in the past 20 years or so. The number of people studying and exploiting them for analog design has increased considerably. Through novel work being done in the area of current mode techniques, the versatility of the current conveyor as a block has only begun to be seen. ADC's and amplifiers are indicative examples of areas that the current conveyor has been applied to. Low noise and higher resolution are but some of the advantages being enjoyed at the expense of bandwidth. [56]

Current conveyors are represented as the block of figure 4.1, and their operation is characterized by the matrix shown below:

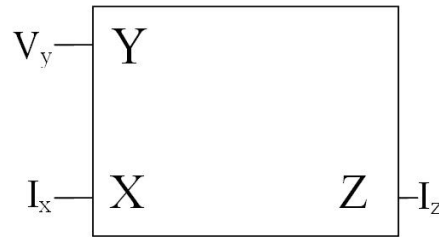


FIGURE 4.1: Current Conveyor Block. Extracted from [57]

$$\begin{pmatrix} I_y \\ V_x \\ I_z \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{pmatrix} \begin{pmatrix} V_y \\ I_x \\ V_z \end{pmatrix}$$

Or more simply, the current conveyor operation is codified by equations 4.1 and 4.2:

$$V_x = V_y \quad (4.1)$$

$$I_z = \pm I_x \quad (4.2)$$

That is, whatever voltage is applied to node Y, is buffered to node X, and whatever current is applied to node X is mirrored to node Z. Though its operation seems trivial, the current conveyor has a number of uses. The modes of operation that the current conveyor can be configured to range from current amplification, voltage-to-current conversion, current buffering, voltage amplification, current/voltage integrators and differentiators, as well as other more advanced circuits. Table 4.1 codifies the configuration of a number of different current-conveyor-based circuits.

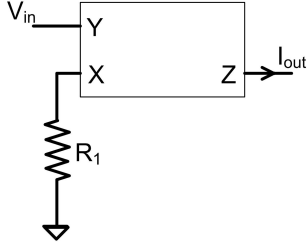
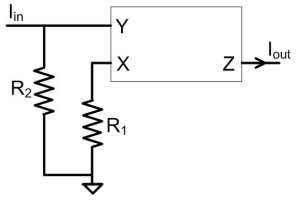
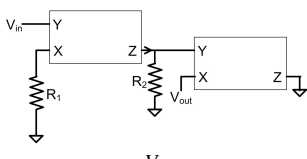
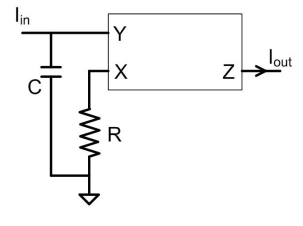
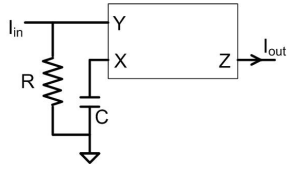
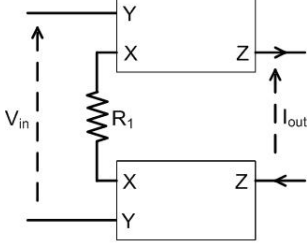
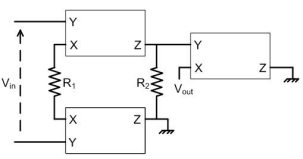
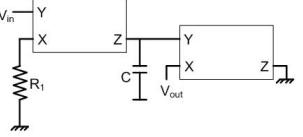
V-to-I Converter  $\frac{V_{IN}}{R_1} = I_x$ $I_{out} = V_{IN}R_1$	0V Input Current Mirror  $I_{out} = I_{in}$	Current Amplifier  $I_{IN} * R_2 = V_x$ $I_{out} = \frac{R_2}{R_1} I_{in}$
Voltage Amplifier  $I_{x1} = \frac{V_{in}}{R_1} = I_{z1}$ $V_{y1} = \frac{R_2}{R_1} V_{in} = V_{out}$	Current Integrator  $I_{out} = \frac{1}{CR} \int I_{IN} dt$	Current Differentiator  $I_{out} = CR \frac{dI_{in}}{dt}$
Differential I to V Converter  $I_{x1} = \frac{V_{in}/2}{R_1/2}$ $I_{out} = \frac{V_{in}}{R_1}$	Differential Voltage Amplifier  $V_{out} = \frac{R_2}{R_1} V_{in}$	Voltage Integrator 

TABLE 4.1: Generic Current-Conveyor-based Operation [57] [58]

4.2 Transistor-level topology of CMOS Current Conveyors

Implementing a current conveyor at transistor level can be achieved in the simplest case by means of a basic NMOS device as shown in figure 4.2. However, this configuration leaves much to be desired in terms of biasing, dynamic range, impedance levels and so on. Therefore more efficient designs needed to be conceived. [58]

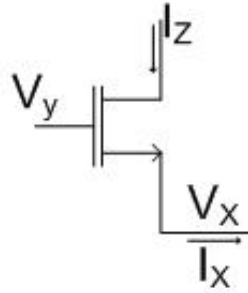


FIGURE 4.2: NMOS transistor viewed as Current Conveyor

Figure 4.3 shows an NMOS current mirror.

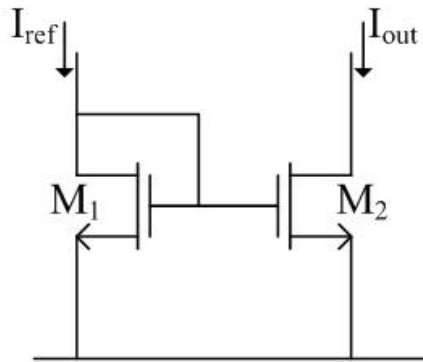


FIGURE 4.3: NMOS current mirror

Assuming that the transistors are matched: [59] [60]

$$I_{out} = \left(\frac{W_2}{L_2} \right) \left(\frac{W_1}{L_1} \right)^{-1} I_{ref} \quad (4.3)$$

Simply put, if both M_1 and M_2 of figure 4.3 are equal in dimensions, then the output current will be equivalent to the input. Equation 4.3 illustrates the relationship between I_{out} and I_{ref} (or I_{IN}), note the similarities between equation 4.3 and the current mirror in table 4.1. Figure 4.4 illustrates the typical PMOS current mirror.

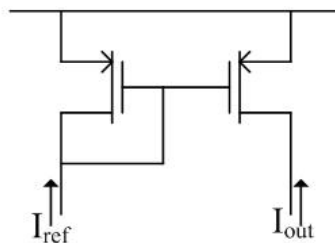


FIGURE 4.4: PMOS current mirror

Slightly modifying figure 4.4, gives figure 4.5

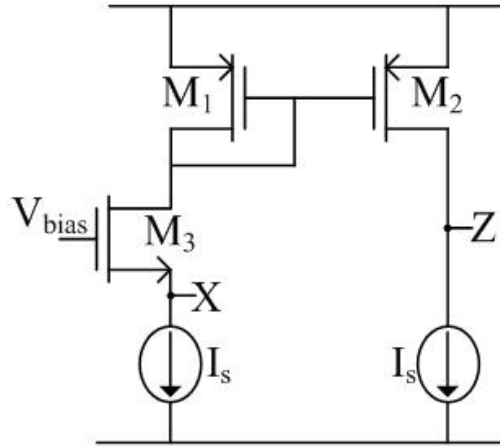


FIGURE 4.5: PMOS current mirror modified

Figure 4.5 shows that any current input on node X will be mirrored by (as I_s is fixed) the $M_1 - M_2$ mirror, to node Z.

Figure 4.6 shows a modification of the current mirror previously depicted in figure 4.3. If the voltage on node Y is changed, then the V_{gs} of M_4 is changed. Effectively the diode-connected current-driven M_4 acts as a voltage level shifter. Assuming that the transistors are matched in size and process, the current through M_3 has changed so that the biasing of M_3 matches that of M_4 . Any voltage at node Y is copied to node X.

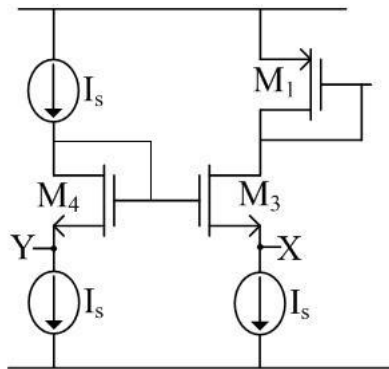


FIGURE 4.6: Voltage Follower

Combining the circuits in figures 4.5 and 4.6 allows a Class A-single rail-current conveyor to be realized (figure see 4.7).

In order for the current conveyor depicted in figure 4.7 to become more versatile, dual rail operation is required. Therefore, the circuit in figure 4.7 is complemented and a Class AB-Dual Rail-Current Conveyor is realized as shown in figure 4.8 [61].

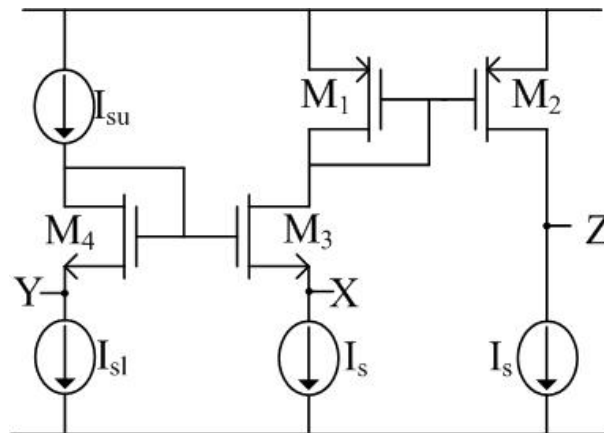


FIGURE 4.7: Class A-Single Rail-Current Conveyor

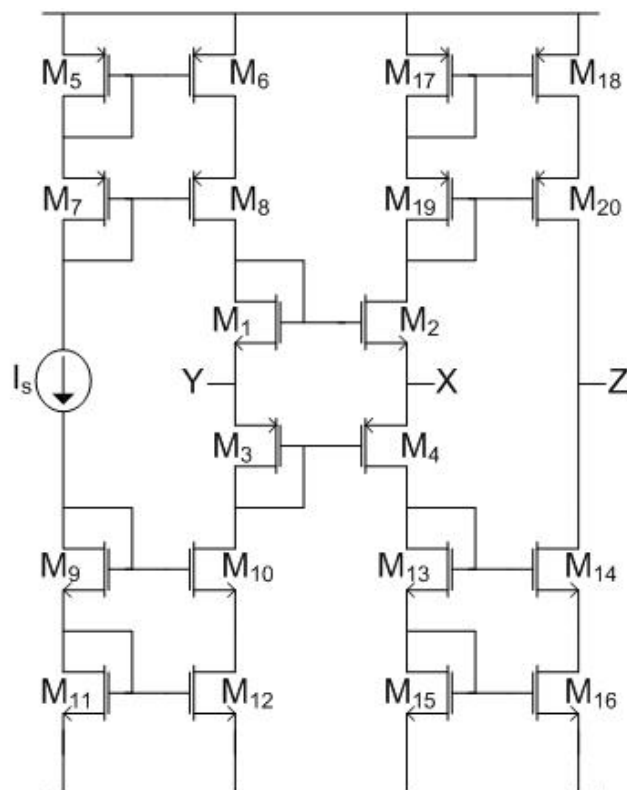


FIGURE 4.8: Class AB-Dual Rail-Current Conveyor . Extracted from [62] and [63]

Observe that a useful way of viewing the current-conveyor operation is that it is a block which accepts as input, a current signal of interest and delivers that signal at a high-impedance node.

4.3 Voltage Swing Analysis

The circuit shown in figure 4.8 consists mainly of blocks that are cascoded (stacked) current mirrors. Figure 4.9 shows the NMOS cascoded current mirror (full analysis can be found in [62] [63]). The minimum voltage between the V_{out} node and V_{ss} (assuming all transistors are in the saturation region,) is given as in equation 4.4:

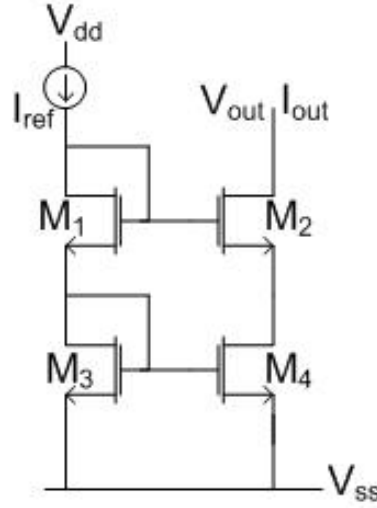


FIGURE 4.9: Typical Cascode Current Mirror

$$V_{out-min} = 2V_{sat} + V_t + V_{ss} \quad (4.4)$$

Therefore, the minimum drop across the cascode mirror will be approximately 2-3V. Not forgetting the PMOS counterpart at the top of the circuit presented in figure 4.8, means that the total drop is now approximately 4-6V for the mirrors alone. The cascoded current mirror has a higher output impedance at the expense of higher total voltage drops. This essentially provides a perfect node for current to be extracted from, which is one of the fundamental attributes required by the circuit.

Using equation 4.4 with the circuit in figure 4.8 then means that there is a $2V_{sat} + V_t$ drop across M_{10} and M_{12} . This in turn means that the V_y to V_x swing is limited to $2V_{sat} + V_t + V_{gs} = 3V_{sat} + 2V_t \approx 3 - 3.5V$, thereby defining a requirement for the power supply. [64]

4.4 Current Swing Analysis

Clearly the minimum current that can be mirrored (assuming all transistors are in saturation) will be limited by the noise floor. In practice however, the maximum current however is to be limited by the current I_s . Point X in figure 4.7 is redrawn in figure 4.10. By Kirchoff's laws (equation 4.5),

$$I_d + I_x = I_s \quad (4.5)$$

Then clearly $I_x \leq I_s$ or else current would be driven up M_3 .

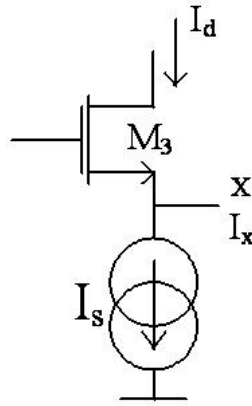


FIGURE 4.10: Current Limiting Node

4.5 Noise Analysis [60]

In order to perform noise analysis on the Class-AB Current Conveyor (figure 4.8), it would be simpler to analyze the circuit in figure 4.7 first. Note that while this analysis is performed, V_{dd} and ground are assumed to be noiseless. The voltage noise at node Y is given as,

Voltage noise at Y = the gate noise M_3 + drain-source noise of M_4 + noise from I_{SU} .

Note that no noise from I_{SL} is apparent as there is no impedance for the I-V transformation. The voltage noise at node Y is then expressed as equation 4.6.

$$\overline{V_{yeq}^2} = \frac{\overline{i_{ds3}^2}}{g_{m3}^2} + \frac{\overline{i_{ds4}^2}}{g_{m4}^2} + \frac{\overline{i_{su}^2}}{g_{m4}^2} \quad (4.6)$$

The current noise at node Y can be simply written as the addition of the sources of current noise; I_{SU} and I_{SL} , thereby,

$$\overline{i_{yeq}^2} = \overline{i_{su}^2} + \overline{i_{sl}^2} \quad (4.7)$$

The current noise at node X is then given by the summation of the drain-source noise from M_3 (the g_m of a diode connected transistor) and the noise from I_s

$$\overline{i_{xeq}^2} = \overline{i_{ds1}^2} + \overline{i_s^2} \quad (4.8)$$

Finally at node Z, the current noise is the addition of I_s and the drain-source current noise of M_4 that is being driven down to node Z. Thereby,

$$\overline{i_{zeq}^2} = \overline{i_{ds2}^2} + \overline{i_s^2} \quad (4.9)$$

The equation for g_m is represented as in 4.10 assuming strong inversion and saturation:

$$g_m = \frac{2I_d}{(V_{gs} - V_t)^2} \quad (4.10)$$

Therefore from equation 4.6, for small amounts of voltage noise at node Y there should be a big W, small L and small $(V_{gs} - V_t)$. From 4.7, for low current noise at node Y, the bias current should be small. Finally, from equation 4.8 and equation 4.9, in order to have a small amount of current noise at node X and Z, the bias current I_s should be small, while the $\frac{W}{L}$ ratio should be small [64]. Clearly a conflict in choosing the relative sizes (W / L) of the transistors has occurred, however there is also another factor related to the size of a transistor: matching. Current mode circuits depend heavily on matching to maintain the correct DC levels and unity gain from the current mirrors. In general,

$$\sigma = \frac{AVTO}{\sqrt{W * L}} \quad (4.11)$$

Where σ is the matching parameter, AVTO = 30.1 for an NMOS, and 24.3 for a PMOS. So for good matching (thereby maintaining the circuit function), the PMOS and NMOS transistors must be large. [65]

4.6 Summary

This chapter culminated in the presentation of a Class AB Dual Rail Current Conveyor illustrated in figure 4.11.

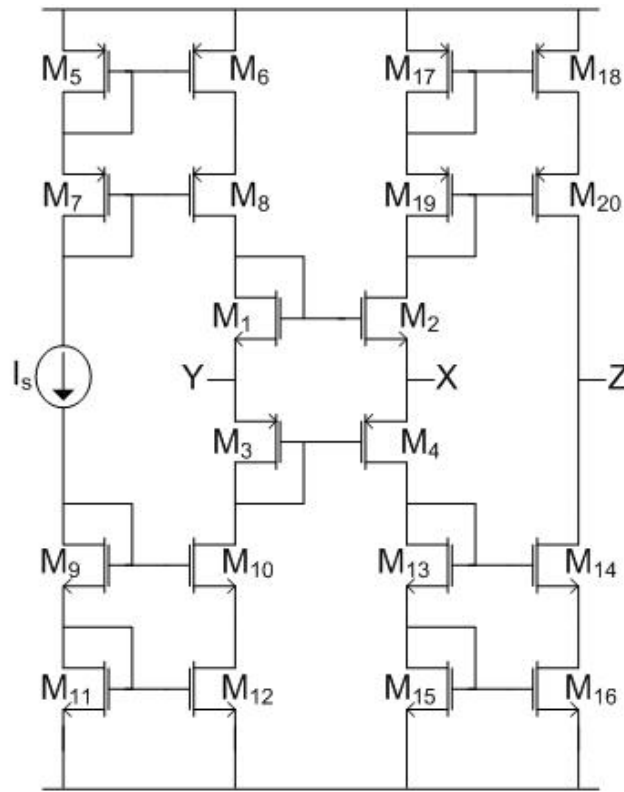


FIGURE 4.11: Class AB-Dual Rail-Current Conveyor

Its function is to provide a virtual ground (set at Y) and low impedance node to the input current (at X), while mirroring the input current to a high impedance output node (Z). As will become clear in the next chapter, the current conveyor will be used as the first block (an interface) connected to the WE, as a replacement to the op-amp stated in figure 3.13. The CMOS current conveyor presented in this chapter is based on the quadratic law. However, the basic current conveyor topology of figure 4.11 would not vary if Bipolar (Junction) Transistor (BJT's) were to be used [58]. In the next chapter the current conveyor with devices working in weak inversion will be discussed. In other words in the next chapter, the exponential of BJT employed in a current conveyor configuration will be replaced by the exponential of the sub-threshold MOS operation.

Chapter 5

Sinh Current Amplifier

In this chapter we first present concisely the basic regions of operation of a typical MOS transistor with the emphasis given upon its subthreshold/weak-inversion operation. Subsequently, we present a novel CMOS current amplifier which bases its operation upon the hyperbolic-sine law implemented by means of weakly-inverted MOS devices. The structure and operation of the novel sinh current amplifier is explained in full. An error analysis of the complete block is also provided.

5.1 Elementary Transistor Theory

Metal-oxide-semiconductor-field-effect-transistors are the building blocks that allow digital and analog integrated circuits to be fabricated. MOSFET technology has allowed for enhancements in the mobile phone industry, computers, general consumer electronics, satellite communications etc. MOSFET's can be used for ultra low power design and efficient and fast digital circuits. This combined with the cost factor explains why CMOS is currently the dominant technology for IC design. [66] [67] [68] [69]

The MOSFET can be described as a voltage dependent resistor. The biasing of the transistor determines the exact relationship between the potentials applied to the device and the current through the transistor. In other words, it is the biasing which defines the 'mode of operation' that the transistor is in. There are three main areas of MOSFET operation which are widely used, the above threshold saturation region, the triode region and the subthreshold region. In this chapter we exploit primarily the subthreshold operation of MOS device and this is the reason why a concise review of mainly that region

is offered here. Figure 5.1 depicts an NMOS transistor where g, b, d and s denotes the gate, bulk, drain and source terminals of the transistors respectively. In what follows we treat mainly NMOS devices. However the derivation of the relation to the p-type devices is straight forward. [70] [71] [72] [73] [75].

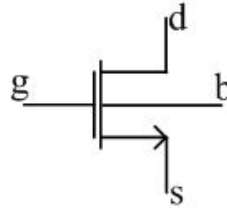


FIGURE 5.1: NMOS Transistor

5.1.1 $I_d - V_{ds}$ Characteristics

Figure 5.2 depicts the $I_d - V_{ds}$ (drain current vs drain source voltage) plot across different levels of channel inversion. Clearly the biasing of the transistor i.e. the selection of the V_{gs} , V_{ds} , (and V_{bs}) voltages causes the device to behave in distinct ways across a range of current values from a few pA's to several mA's. The region of operation which will be considered within this chapter is denoted the 'weak inversion region'. It is displayed in greater detail by figure 5.3. Observe that in the weak inversion region the drain currents vary typically from a few tenths of 1 nA to several hundred of μ A's when $V_{gs} < V_{th}$ (with V_{th} denoting the threshold of the device).

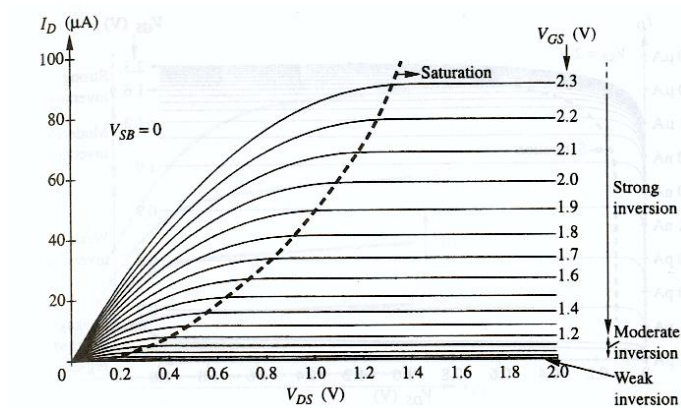


FIGURE 5.2: Typical $I_{ds} - V_{ds}$ Curves for an NMOS Transistor. Extracted from [78]

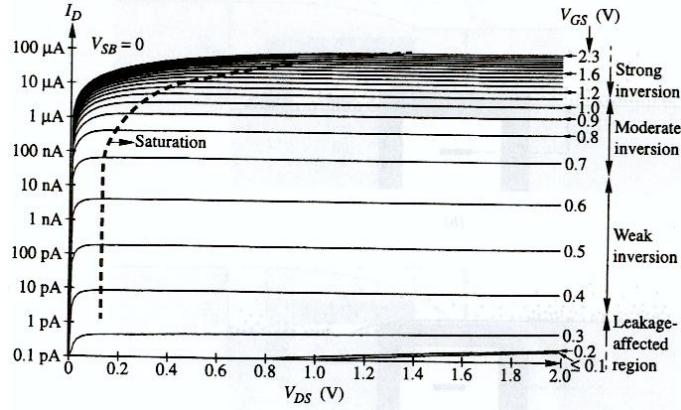


FIGURE 5.3: Typical $I_{ds} - V_{ds}$ Curves for an NMOS Transistor. Extracted from [78]

5.1.2 Saturation Region

When $V_{gs} \geq V_{th}$, the transistor is modeled to a first-order by equation 5.1.

$$I_d = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{th})^2 \quad (5.1)$$

Where μ_n , C_{ox} and $\frac{W}{L}$ denote the electron mobility, the capacitance per unit area and the aspect ratio of the device. Note the absence of V_{ds} dependence in equation 5.1. Indeed, when in saturation (and in strong inversion), there is *nearly* no variation in the I_d value for a changing V_{ds} value. If such a dependence needs to be taken into consideration, then the RMS of relation 5.1 needs to be multiplied by the factor $(1 + \lambda V_{ds})$ with λ now denoting the ‘channel length modulation’ factor. The intended use of the device in this region of operation is either as a switch or to provide gain. [68] [74] [78]

5.1.3 Linear Region

The next region is the linear region also known as the triode region. In this region the gradient of the $I_d - V_{ds}$ curves (see figure 5.2) is to a first order constant. When $V_{gs} > V_{th}$ and $V_{ds} < (V_{gs} - V_{th})$. Here the transistor is mathematically modeled as:

$$I_d = \mu_n C_{ox} \frac{W}{L} \left[(V_{gs} - V_{th}) V_{ds} - \frac{V_{ds}^2}{2} \right] \quad (5.2)$$

In this region the transistor acts as a resistor whose value can be controlled by varying the V_{gs} values [79]. Observe that when $\frac{V_{ds}^2}{2} \gg (V_{gs} - V_{th})V_{ds}$, i.e. when $\frac{V_{ds}}{2} \gg (V_{gs} - V_{th})$, then,

$$I_d = \mu_n C_{ox} \frac{W}{L} (V_{gs} - V_{th}) V_{ds} \quad (5.3)$$

with the factor $\mu C_{ox} \frac{W}{L} (V_{gs} - V_{th})$ playing the role of a V_{gs} controlled resistor value.

5.1.4 Weak Inversion

The weak inversion region is characterized by the condition $V_{gs} < V_{th}$. It can be shown that the drain current I_d is given in this case by,

$$I_d = I_{d_o} \frac{W}{L} e^{\frac{kV_{gb}}{V_t}} \left(1 - e^{-\frac{V_{ds}}{nV_t}} \right) \quad (5.4)$$

Where $k V_{gb}$ is the potential on the surface of the semiconductor.

Relation 5.4 holds when $V_{bs} = 0$, also when $V_{ds} \gg 4nV_t$ then 5.4 reduces to:

$$I_d = I_{d_o} \frac{W}{L} e^{\frac{V_{gs}}{nV_t}} \quad (5.5)$$

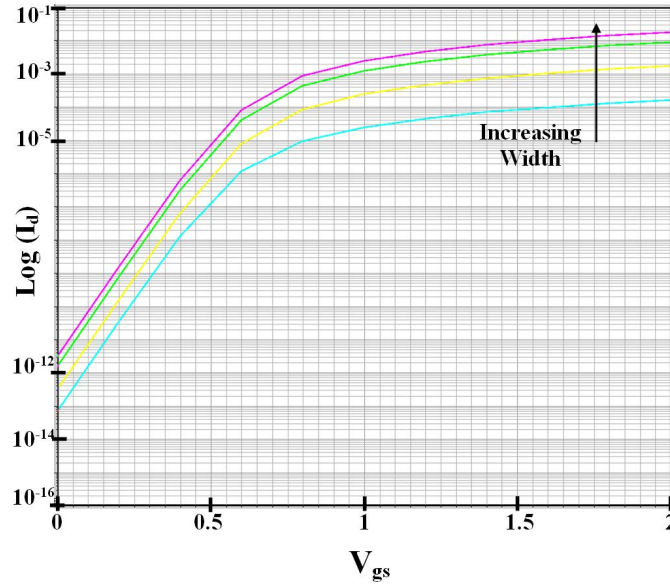
Which codifies an exponential dependence of the drain current I_d upon the V_{gs} ($< V_{th}$) value.

In the above relations I_{d_o} is a process dependent parameter given by,

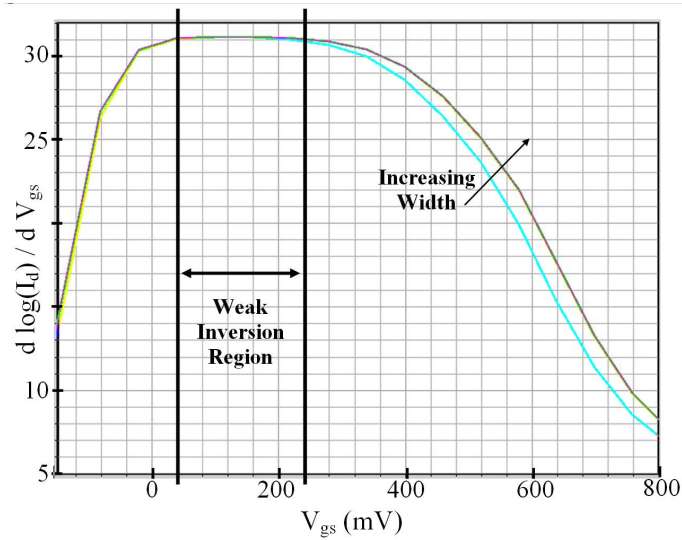
$$I_{d_o} = \frac{W}{L} \mu \frac{\epsilon_{ox}}{d_{ox}} (n - 1) V_t \quad (5.6)$$

Where n is the subthreshold slope factor which is technology dependent and usually takes values between 1 and 2, $\frac{W}{L}$ is the aspect ratio of the device, and $V_t = \frac{kT}{q} = 25mV$ at room temperature is known as the thermal voltage. $\frac{\epsilon_{ox}}{d_{ox}}$ is the ratio of the permittivity of the insulator and the insulator thickness. [78]

Figure 5.4 shows a Log I_d vs V_{gs} plot of a MOS transistor [80]

FIGURE 5.4: $\text{Log } I_d$ vs V_{gs} Curve

Observe that the current level ranges between 0.1pA and 10mA and increase with greater width values. Figure 5.5 illustrates the relationship between $d[\log I_d]/dV_{gs}$ and V_{gs} . Strictly speaking and bearing in mind figure 5.5 value for which $d[\log I_d]/dV_{gs}=0$ denotes the weak inversion region.

FIGURE 5.5: Plot of $\frac{d\text{Log}I_d}{dV_{gs}}$ vs V_{gs}

Observe that the width of the weak inversion region illustrated in figure 5.5 varies with the aspect ratio of the device.

5.2 Sinh Amplifier

This section details the creation of the sinh current amplifier by utilizing the weak inversion exponential mathematical model of the MOS transistor. Initially an E_+ and E_- cell will be combined in order to realize an I-to-sinh(V) block via a bias I_o . Subsequently a sinh(V)-to-I transformation will be detailed via bias I_1 . Therefore the input to output gain will be described as the ratio of I_1 to I_0 . Though the circuit is externally linear, it is internally non-linear.

5.2.1 Exponential Transconductor Cells (E Cells)

Figure 5.6 illustrates a transistor configuration known as an E_+ cell. The cell operation resides in two assumptions. First, that the transistors are all of the same size and dimensions and hence matched, and secondly, that they all operation in the weak inversion region.

Applying KVL around the loop shown in figure 5.6 yields equations 5.7.

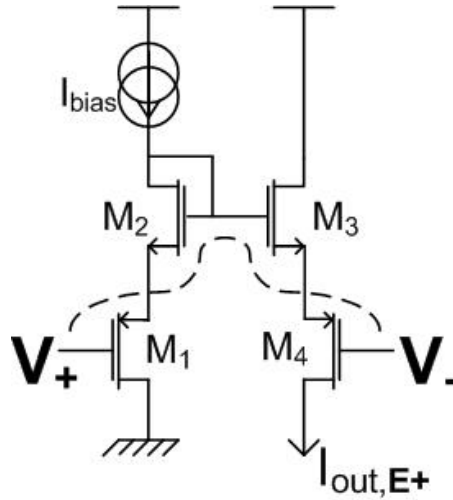


FIGURE 5.6: CMOS transistor configuration of an E_+ Cell; $I_{out,E+} = I_{bias} e^{\frac{(V_+ - V_-)}{2nV_t}}$

$$V_+ + V_{sgM1} + V_{sgM2} - V_{sgM3} - V_{sgM4} - V_- = 0 \quad (5.7)$$

Re-arranging equation 5.5 gives:

$$V_{gs} = nV_t \ln \left[\frac{I_d}{I_{do} \frac{W}{L}} \right] \quad (5.8)$$

Substituting in equation 5.8 to 5.7 and re-arranging gives,

$$I_{out,E+} = I_{bias} e^{\frac{(V_+ - V_-)}{2nV_T}} \quad (5.9)$$

Observe that equation 5.9 now describes an exponential dependence of that output current $I_{out,E+}$ of the block upon the voltage difference $(V_+ - V_-)$. The block shown in figure 5.6 is the weak-inversion equivalent of the BJT-based E_+ cells used for the realization of log-domain filters. [57], [82], [83]

Figure 5.7 shows an E_- cell realized by means of MOS transistors.

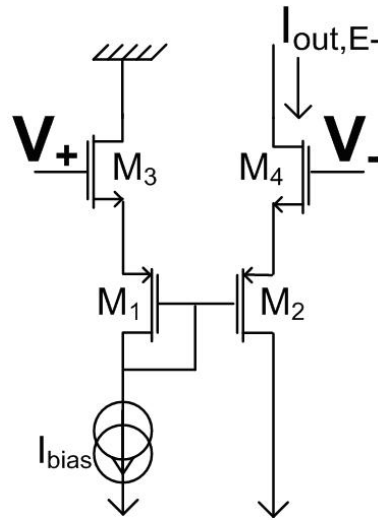


FIGURE 5.7: CMOS transistor configuration of an E_- Cell; $I_{out,E-} = I_{bias} e^{\frac{-(V_+ - V_-)}{2nV_T}}$

Following an analysis procedure similar to the one described above it can be shown that,

$$I_{out,E-} = I_{bias} e^{\frac{-(V_+ - V_-)}{2nV_T}} \quad (5.10)$$

The topology of figure 5.7 is the weak-inversion equivalent of the BJT-based E-cell also used for the realisation of log-domain filters. [57], [81], [82], [83]

A common feature of both the E_+ and the E_- cells is that they can be viewed as exponential-voltage-to-current blocks. In other words the E Cells are non-linear time-invariant blocks. The main operational difference between the two is that the E_+ cell pushes current to a node whereas the E_- cell draws current from a node. The properties of BJT-based E Cells including their inaccuracies have been studied by many ([57], [84], [85]), always in the context of log domain processing. It is not an understatement

to stress that E cells allow for elegant log-domain topologies as verified by the plethora of simulated and measured log-domain circuit. In what follows we present certain E cell-based blocks which when combined appropriately can give rise to the novel Sinh Current Amplifier.

5.2.2 I-to-Sinh(V) Block

By combining one E_+ cell and one E_- cell as shown in figure 5.6 and 5.7 and by driving an input current I_{in} into the low impedance node V_x (figure 5.8), holds:

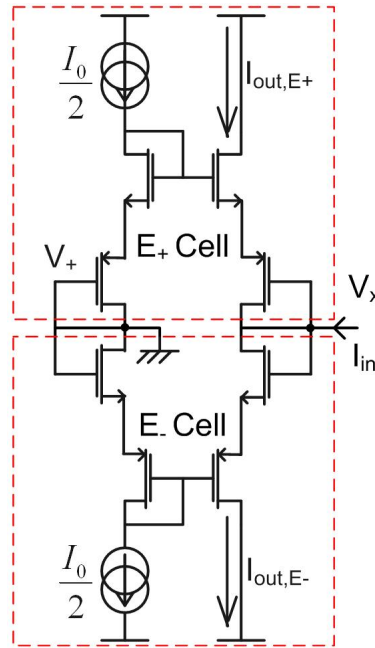


FIGURE 5.8: I-to-sinh(V) block response

$$I_{in} + I_{out,E+} = I_{out,E-} \quad (5.11)$$

Which when considering 5.9 and 5.10 for the $I_{out,E\pm}$ expression leads to equation 5.12

$$I_{in} = \frac{I_o}{2} \left[e^{\frac{-V_x}{2nV_t}} - e^{\frac{V_x}{2nV_t}} \right] \quad (5.12)$$

Since the V_+ terminals (see figure 5.6 and 5.7) of both E cells are grounded. From 5.12 it is straight forward to deduce that:

$$I_{in} = I_o \sinh\left(\frac{V_x}{2nV_t}\right) \quad (5.13)$$

The sinh relationship of V_x to I_{in} in equation 5.13 is displayed by figure 5.9.

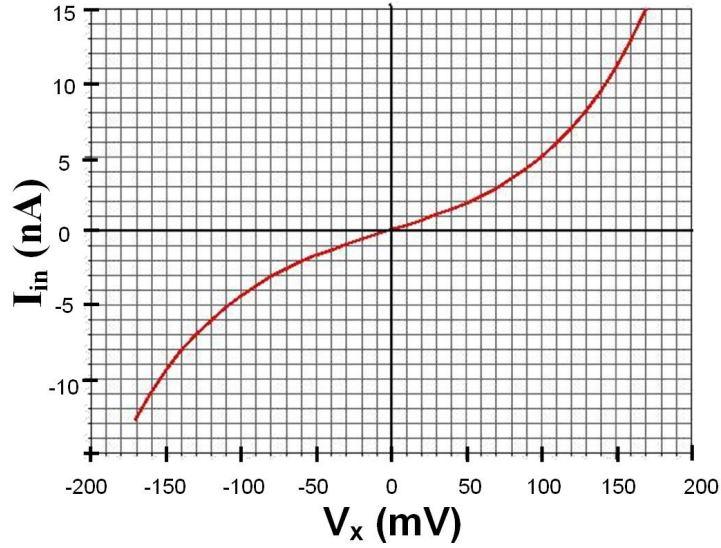


FIGURE 5.9: I-to-sinh(V) block response

Equation 5.13 maybe re-arranged as,

$$V_x = 2nV_t \sinh^{-1}\left(\frac{I_{in}}{I_o}\right) \quad (5.14)$$

The inverse sinh relationship of I_{in} to V_x in equation 5.14 is displayed by figure 5.10.

In other words, the block of figure 5.8 can be seen as a converter of an input current I_{in} to a voltage V_x which has a $\sinh^{-1}$ dependence upon the current I_{in} .

5.2.3 Sinh(V)-to-I Block

By combining a pair of E cells as shown in figure 5.11 and by driving the combination with the voltage V_x it is clear that,

$$I_{outE+} = \frac{I_1}{2} e^{\frac{V_x}{2nV_t}} \quad (5.15)$$

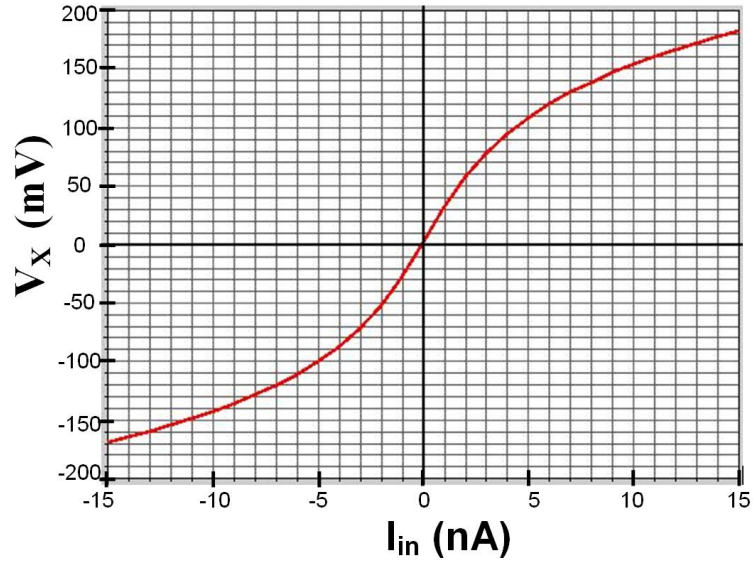


FIGURE 5.10: Sinh(V)-to-I Block response

$$I_{outE-} = \frac{I_1}{2} e^{\frac{-V_x}{2nV_t}} \quad (5.16)$$

The above relations allow for the difference current $I_{outE-} - I_{outE+}$ to be expressed as equation 5.17.

$$I_{outE-} - I_{outE+} = I_1 \sinh\left(\frac{V_x}{2nV_t}\right) \quad (5.17)$$

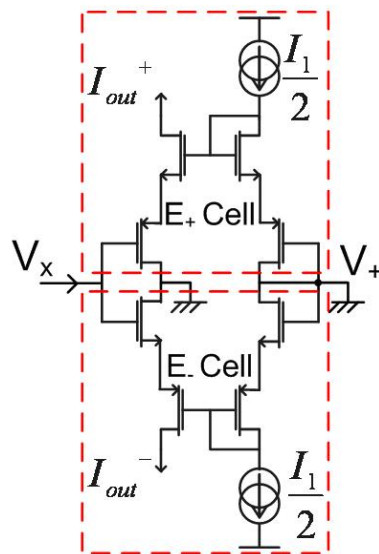


FIGURE 5.11: Sinh(V)-to-I Block

5.3 The Proposed Sinh Current Amplifier

Bearing in mind relations 5.14 and combining it with 5.17 provides:

$$I_{out-} - I_{out+} = I_1 \sinh \left[\frac{2nV_t \sinh^{-1}(\frac{I_{in}}{I_0})}{2nV_t} \right] \quad (5.18)$$

this in turn yields:

$$I_{out-} - I_{out+} = I_{in} \left(\frac{I_1}{I_0} \right) \quad (5.19)$$

In other words by combining an I-to-sinh(V) block (characterized by 5.14) with a sinh(V)-to-I block (characterized by 5.17) a linear current gain can be achieved between the differential output current ($I_{out-} - I_{out+}$) and I_{in} so long as $\frac{I_1}{I_0} > 1$. It is exactly this observation which allows for the proposition of the novel Sinh Current Amplifier shown in figure 5.12 whose basic operation can be explained as follows:

- an input current I_{in} is converted according to 5.14 to an auxiliary voltage V_x
- the same voltage V_x is converted to two currents I_{out+} and I_{out-} according to 5.15 and 5.16.
- the lower and upper current mirrors ensure the creation of the output current $I_{out} = I_{out-} - I_{out+}$ at a high impedance node according to equation 5.17
- the output current I_{out} is an I_1/I_0 times amplified replica of the input current I_{in} thanks to 5.19.

At this point it would be useful to stress that the aforementioned amplification mechanism relies on two basic assumptions: a) that all devices operate in their weak-inversion regime and b) that all devices within an E cell are matched. The fact that, for given transistor sizes there will be an upper current limit as far as conformity with the weak-inversion exponential law is concerned, suggests that the gain factor (which is the ratio of two weak-inversion currents) will exhibit in practice an upper limit.

In addition to the above two basic operation assumptions, another two need to be stressed. More specifically: the desired operation of the circuit relies upon the matching

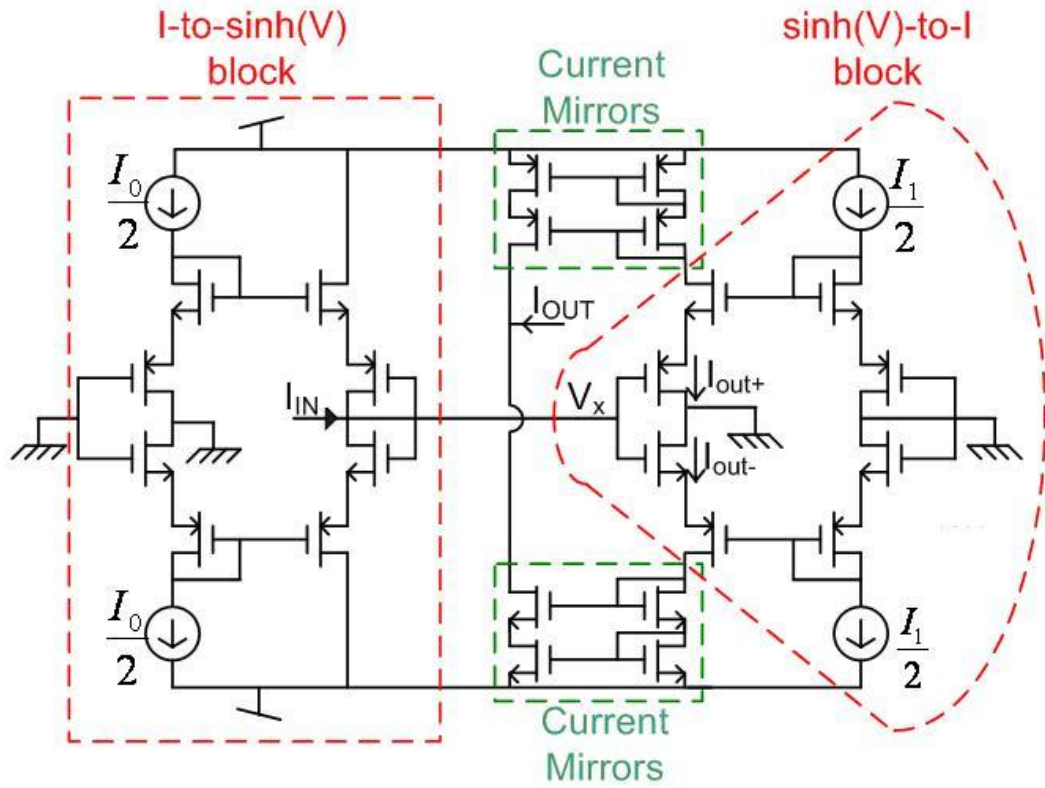


FIGURE 5.12: Sinh Class AB Current Amplifier topology

of the DC current biasing sources within the I-to-sinh(V) and sinh(V)-to-I blocks and the matching of the devices comprising the amplifier's current mirrors. In what follows we perform error analysis in an effort to assess the impact of such error sources on the amplifiers anticipated operation.

5.3.1 Impact of an offset voltage at the V_x node

Measurements of fabricated Sinh Current Amplifier chips (shown in the next chapter) have shown that the output amplifier current is sensitive to the presence of an offset voltage at the V_x node. It is for this reason that in this section we analyze the effect that an offset voltage V_{off} developed at node V_x has on the output current of the current amplifier. In general, device mismatches and/or offsets already associated with other blocks could give rise to V_{off} . Recalling the ideal V_x value provided by equation 5.14, it is clear that when the presence of V_{off} leads to a real V_x value,

$$V_{x,real} = V_{x,ideal} + V_{off} \quad (5.20)$$

$$V_{x,real} = 2nV_t \sinh^{-1} \left(\frac{I_{in}}{I_0} \right) + V_{off} \quad (5.21)$$

then the output $\sinh(v)$ -to-I block of the amplifier would produce the following output current (see figure 5.12):

$$I_{out} = I_1 \sinh \left[\frac{2nV_t \sinh^{-1} \left(\frac{I_{in}}{I_0} \right) + V_{off}}{2nV_t} \right] \quad (5.22)$$

Re-arranging leads to 5.23,

$$I_{out} = I_1 \sinh \left[\sinh^{-1} \left(\frac{I_{in}}{I_0} \right) + \frac{V_{off}}{2nV_t} \right] \quad (5.23)$$

Applying hyperbolic expansion leads to:

$$I_{out} = I_1 \left[\frac{I_{in}}{I_0} \cosh \left(\frac{V_{off}}{2nV_t} \right) + \cosh \left(\sinh^{-1} \frac{I_{in}}{I_0} \right) \sinh \left(\frac{V_{off}}{2nV_t} \right) \right] \quad (5.24)$$

Allowing

$$G_1 = \cosh \left(\frac{V_{off}}{2nV_t} \right) \quad (5.25)$$

and

$$G_2 = \sinh \left(\frac{V_{off}}{2nV_t} \right) \quad (5.26)$$

Substituting 5.25 and 5.26 into 5.24 leads to equation 5.27,

$$I_{out} = G_1 \frac{I_1}{I_2} I_{IN} + G_2 I_1 \cosh \left(\sinh^{-1} \frac{I_{in}}{I_0} \right) \quad (5.27)$$

Considering that in general $\sinh^{-1}(x) = \ln(x + \sqrt{x^2 + 1})$, then 5.27 is transformed to 5.28

$$I_{out} = G_1 \frac{I_1}{I_0} I_{IN} + G_2 I_1 \cosh \left(\ln \left(\frac{I_{in}}{I_0} + \sqrt{\left(\frac{I_{in}}{I_0} \right)^2 + 1} \right) \right) \quad (5.28)$$

Applying the cosh transformation,

$$I_{out} = G_1 \frac{I_1}{I_0} I_{IN} + G_2 I_1 \left[\frac{e^{\ln \left(\frac{I_{in}}{I_{o1}} + \sqrt{\left(\frac{I_{in}}{I_{o1}} \right)^2 + 1} \right)} + e^{-\ln \left(\frac{I_{in}}{I_{o1}} + \sqrt{\left(\frac{I_{in}}{I_{o1}} \right)^2 + 1} \right)}}{2} \right] \quad (5.29)$$

This can be re-written as:

$$I_{out} = G_1 \frac{I_1}{I_0} I_{IN} + G_2 I_1 \frac{1}{2} \left[\frac{I_{in}}{I_{o1}} + \sqrt{\left(\frac{I_{in}}{I_{o1}} \right)^2 + 1} + \frac{1}{\frac{I_{in}}{I_{o1}} + \sqrt{\left(\frac{I_{in}}{I_{o1}} \right)^2 + 1}} \right] \quad (5.30)$$

Realising that in general $x + \sqrt{x^2 + 1} + \frac{1}{x + \sqrt{x^2 + 1}} = x + \sqrt{x^2 + 1} + \frac{x - \sqrt{x^2 + 1}}{-1} = 2\sqrt{x^2 + 1}$, allows equation 5.30 to be reduced to 5.31

$$I_{out} = G_1 \frac{I_1}{I_0} I_{IN} + G_2 I_1 \left[\sqrt{\left(\frac{I_{in}}{I_0} \right)^2 + 1} \right] \quad (5.31)$$

or equivalently:

$$I_{out} = G_1 \frac{I_1}{I_0} I_{IN} + G_2 \left[\sqrt{\left(\frac{I_{in}}{I_0} I_1 \right)^2 + I_1^2} \right] \quad (5.32)$$

Since $\frac{I_1}{I_0} I_{IN} = I_{out-ideal}$, recall 5.19 then 5.32 can be expressed as,

$$I_{out} = G_1 I_{out-ideal} + G_2 \sqrt{I_{out-ideal}^2 + I_1^2} \quad (5.33)$$

Recalling 5.25 and 5.26

$$I_{out} = \cosh \left(\frac{V_{off}}{2nV_t} \right) I_{out-ideal} + \sinh \left(\frac{V_{off}}{2nV_t} \right) \sqrt{I_{out-ideal}^2 + I_1^2} \quad (5.34)$$

$$I_{out} = \cosh\left(\frac{V_{off}}{2nV_t}\right) I_{out,ideal} + \left[1 + \tanh\left(\frac{V_{off}}{2nV_t}\right) \frac{\sqrt{I_{out,ideal}^2 + I_1^2}}{I_{out,ideal}} \right] \quad (5.35)$$

From 5.35 it is clear that when $I_{out,ideal}$ is set to a high value M such that $M \gg I_1$, then

$$\lim_{I_{out,ideal} \rightarrow M} I_{out} = M \cosh\left(\frac{V_{off}}{2nV_t}\right) \left[1 + \tanh\left(\frac{V_{off}}{2nV_t}\right) \right] \quad (5.36)$$

The above relations reveal that:

- a) When $V_{off} = 0$, the $\cosh\left(\frac{V_{off}}{2nV_t}\right) = 1$ and $\tanh\left(\frac{V_{off}}{2nV_t}\right) = 0$ leading to $I_{out} = I_{out-ideal}$ as expected
- b) When $V_{off} \neq 0$ and large current gains are targeted then the ideally expected output current $I_{out-ideal}$ will be scaled by the factor of:

$$Gain = \cosh\left(\frac{V_{off}}{2nV_t}\right) \left[1 + \tanh\left(\frac{V_{off}}{2nV_t}\right) \right] \quad (5.37)$$

Figure 5.13 illustrates the dependence of this term upon $x = \frac{V_{off}}{2nV_t}$

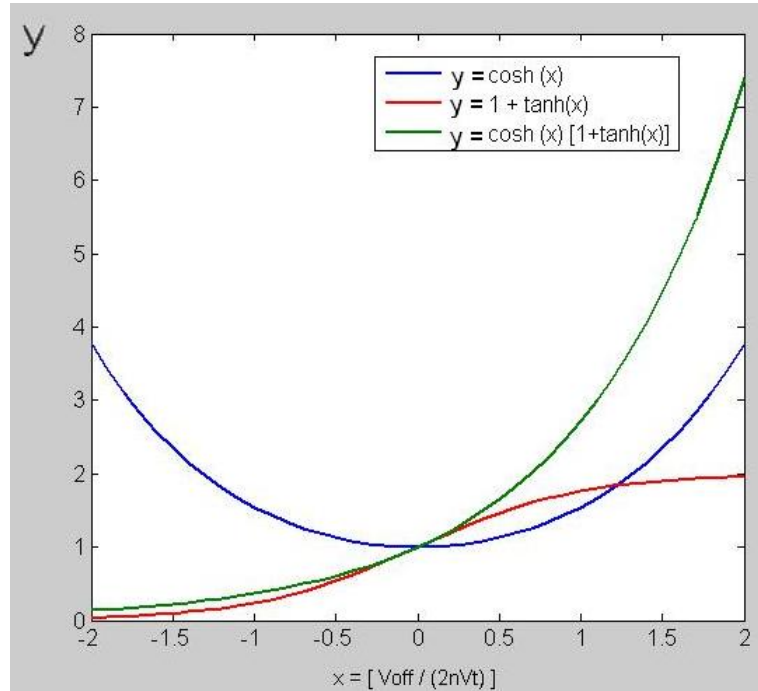


FIGURE 5.13: Plotting of the terms $\cosh(x)$, $1 + \tanh(x)$ and, $\cosh(x)[1 + \tanh(x)]$ of equation 5.37

Figure 5.14 illustrates the dependence of $I_{out-real}$ upon V_{off} when $I_{out-ideal}$ is set to 1000nA's.

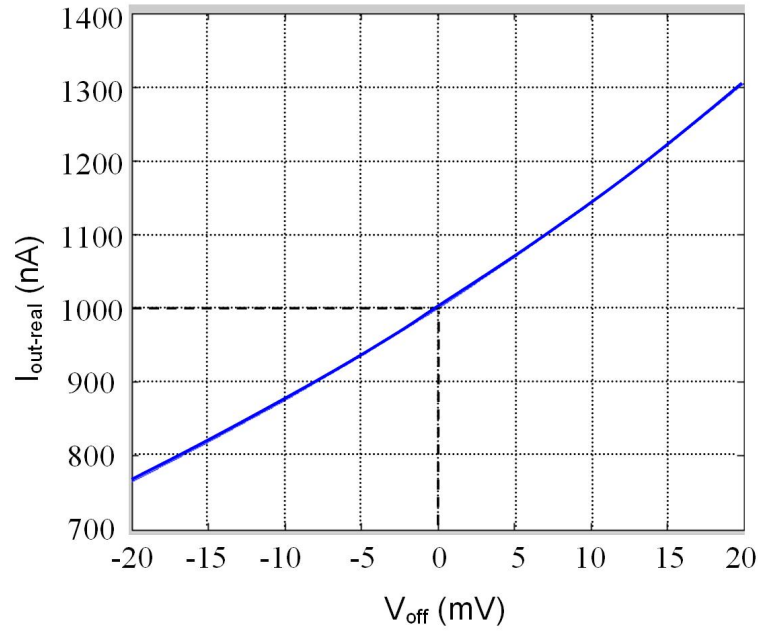


FIGURE 5.14: $I_{out-real}$ vs V_{offset} when $I_{out-ideal} = 1000(\gg I_1)$

Figure 5.15 represents equation 5.34 and plots $I_{out-real}$ as a function of $I_{out-ideal} = 0 - 250$ nA's and $I_1=50, 100$ and 200 nA's while V_{off} takes values of -20 mV, 0 mV, $+20$ mV.

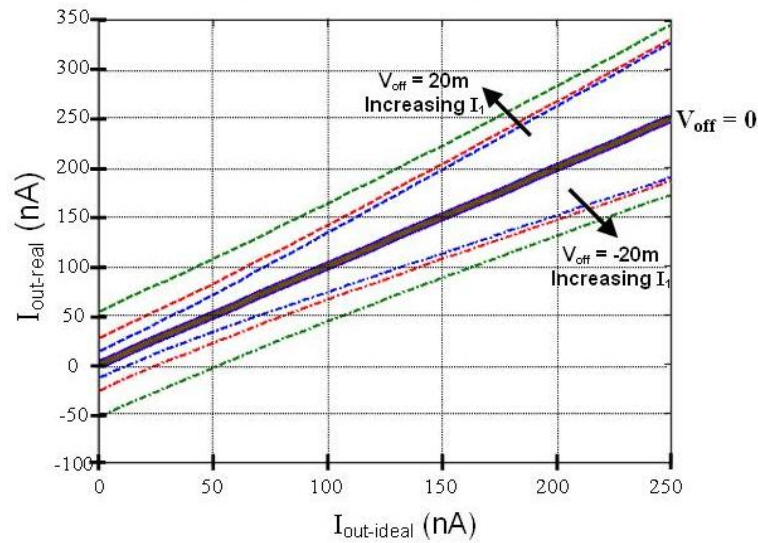


FIGURE 5.15: $I_{out-real}$ vs $I_{out-ideal}$ when $I_1=50, 100, 200$ nA's and $V_{off}=-20, 0 +20$ mV

From the above analysis it should be clear that the optimal operation of the current amplifier will be ensured when $V_{off} \approx 0$. It is important to note that though the presence

of V_{off} does alter the achieved value of the gain it does not seem to lead to any form of distortion at the output despite the use of highly non-linear circuit blocks.

5.4 Error analysis of the Sinh Current Amplifier

In this section we provide a full error analysis of the proposed novel amplifier. In particular we will consider the impact of:

- a) DC biasing current errors (affecting the operation of E_+ , E_- and Sinh blocks)
- b) Current mirror errors (affecting the mirroring operations needed for the creation of $I_{out-total}$ of the amplifier)

Let us assume that an E_+ cell is characterized by a DC current $\frac{I_{o1} \pm \delta_1}{2}$ with δ_1 denoting the ‘error current’ associated with nominal current I_{o1} due to design and/or fabrication errors. An analysis similar to the one presented before yields for an E_+ cell (see figure 5.16) when the p and n devices are assumed matched and of the same aspect ratio:

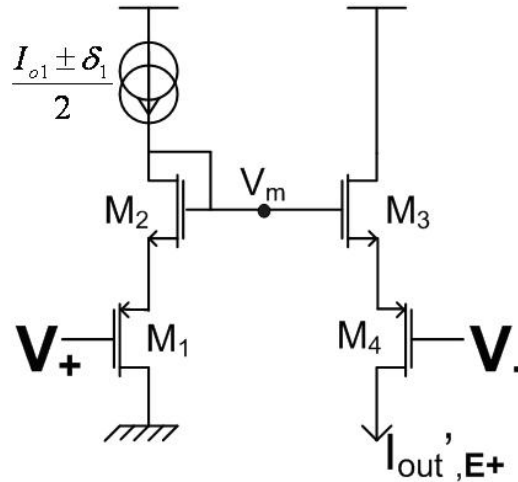


FIGURE 5.16: E_+ error cell

Utilising equation 5.7 and 5.8, the circuit depicts figure 5.16 may be expressed as,

$$V_+ + 2nV_t \ln \left[\frac{\frac{I_{o1} \pm \delta_1}{2}}{I_{d_o} \frac{W}{L}} \right] = 2nV_t \ln \left[\frac{I_{outE+}}{I_{d_o} \frac{W}{L}} \right] + V_- \quad (5.38)$$

Reducing equation 5.38 leads to;

$$V_+ - V_- = 2nV_t \ln \left[\frac{I_{out,E+}}{\frac{I_{o1} \pm \delta_1}{2}} \right] \quad (5.39)$$

with $I_{out,E+}$ now doubling the modified output current of the E_+ cell due to the error δ_1 . Re-arranging 5.39 for $I_{out,E+}$:

$$I_{out,E+} = \frac{(I_{o1} \pm \delta_1)}{2} e^{\frac{V_+ - V_-}{2nV_t}} \quad (5.40)$$

Similarly for the output current $I_{out,E-}$ of the typical E_- cell shown in figure 5.17 it will hold when an error current δ_2 is associated with it:

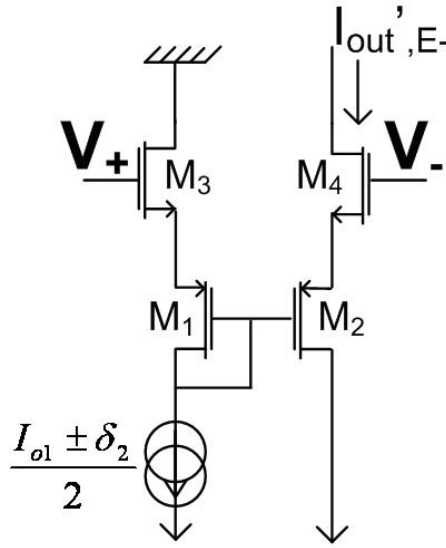


FIGURE 5.17: E_- error cell

$$I_{out,E-} = \frac{(I_{o1} \pm \delta_2)}{2} e^{\frac{V_- - V_+}{2nV_t}} \quad (5.41)$$

Recalling the structure of the compressive $\sinh^{-1}$ stage of the amplifier - shown in figure 5.11 - and bearing in mind that the auxiliary voltage V_x will be generated by combining two output currents $I_{out,E+}$ and $I_{out,E-}$ it can be shown that:

$$\hat{I}_{in} = \frac{(I_{o1} \pm \delta_2)}{2} e^{\frac{V_- - V_+}{2nV_t}} - \frac{(I_{o1} \pm \delta_1)}{2} e^{\frac{V_+ - V_-}{2nV_t}} \quad (5.42)$$

Under the practically reasonable assumption that:

$$\pm \delta_1 = \pm \delta_2 \quad (5.43)$$

Equation 5.42 yields:

$$I_{in} = (I_{o1} \pm \delta_1) \sinh\left(\frac{V_+ - V_-}{2nV_t}\right) \quad (5.44)$$

The relation in 5.44 can now codify the impact of the error δ_1 at node V_x of the current amplifier; when V_+ is grounded (see figure 5.12) then gives:

$$V_- = \hat{V}_x = 2nV_t \sinh^{-1}\left[\frac{I_{in}}{I_{o1} \pm \delta_1}\right] \quad (5.45)$$

Proceeding with our error analysis we observe that the error including $\hat{V}_x$ will not be expanded by the two E cells of the expansive Sinh part of the amplifier. Clearly each one of the two cells of this part will in general be associated with an error current. Assuming that δ_3 and δ_4 are the error currents associated with the E_+ and E_- cells of the expansive amplifier part respectively, it holds:

$$I_{out,E+}^{\hat{}} = \frac{I_{o2} \pm \delta_3}{2} e^{\left[\frac{\hat{V}_x}{2nV_t}\right]} \quad (5.46)$$

$$I_{out,E-}^{\hat{}} = \frac{I_{o2} \pm \delta_4}{2} e^{\left[-\frac{\hat{V}_x}{2nV_t}\right]} \quad (5.47)$$

which leads to:

$$I_{out,tot}^{\hat{}} = \frac{I_{o2} \pm \delta_4}{2} e^{\left[-\frac{\hat{V}_x}{2nV_t}\right]} - \frac{I_{o2} \pm \delta_3}{2} e^{\left[\frac{\hat{V}_x}{2nV_t}\right]} \quad (5.48)$$

Relation 5.48 does not take into consideration any errors indicated by the output stage current mirrors, however the current components $I_{out,E+}^{\hat{}}$ and $I_{out,E-}^{\hat{}}$ will create the total output current of the current amplifier after they have been mirrored by the upper and lower current mirrors with errors λ_3 and λ_4 respectively. Hence in general it will hold:

$$I_{out,tot}^{\hat{}} = \lambda_4 \frac{I_{o2} \pm \delta_4}{2} e^{\left[-\frac{\hat{V}_x}{2nV_t}\right]} - \lambda_3 \frac{I_{o2} \pm \delta_3}{2} e^{\left[\frac{\hat{V}_x}{2nV_t}\right]} \quad (5.49)$$

Under the reasonable assumption that,

$$\pm \delta_4 = \pm \delta_3 \quad (5.50)$$

and

$$\lambda_4 = \lambda_3 = \lambda \quad (5.51)$$

relation 5.49 yields:

$$I_{out,tot}^{\sim} = \lambda \frac{I_{o2} \pm \delta_3}{2} \sinh\left(\frac{\hat{V}_x}{2nV_t}\right) \quad (5.52)$$

Bearing in mind 5.45, and 5.52 gives:

$$I_{out,tot}^{\sim} = \lambda \frac{I_{o2} \pm \delta_3}{I_{o1} \pm \delta_1} I_{in} \quad (5.53)$$

Which can be expressed in an equivalent manner as:

$$I_{out,tot}^{\sim} = \lambda \frac{1 \pm \epsilon_3}{1 \pm \epsilon_1} G_i I_{in} \quad (5.54)$$

Where:

- λ denotes the error of the output stage current mirrors,
- ϵ_3 denotes the % error in the generation of the DC biasing current of value I_{o2} (i.e. the current controlling the expansive sinh operation),
- ϵ_1 denotes the % error in the generation of the DC biasing current of value I_{o1} (i.e. the current controlling the compressive $\sinh^{-1}$) operation), and
- $G_i = \frac{I_{o2}}{I_{o1}}$ = the ideal current gain.

Equation 5.54 provides a number of real errors associated with the Sinh Class AB Current Amplifier depicted in figure 5.12. ϵ_1 denotes the error of $\frac{\delta_1}{I_{o1}}$, and ϵ_3 being $\frac{\delta_3}{I_{o2}}$. λ represents the output current mirror of the current amplifier. Each of these errors causes

ϵ_1	ϵ_3	λ	Percentage error of I_{out}
10%	0%	1	9%
0%	10%	1	10%
1%	0%	1	1%
0%	1%	1	1%
0%	0%	0.99	1%
1%	1%	0.99	3%

TABLE 5.1: Dependence of % error of $I_{out,ideal}$ upon ϵ_1 , ϵ_3 and λ

a deviation from the ideal desired output of the amplifier. Table 5.4 shows the percentage error of I_{out} at the output of the Sinh amplifier, when ϵ_1 , ϵ_3 and λ has an error.

5.5 Conclusion

The Sinh Current Amplifier (illustrated in figure 5.18) is a novel circuit currently under patent.

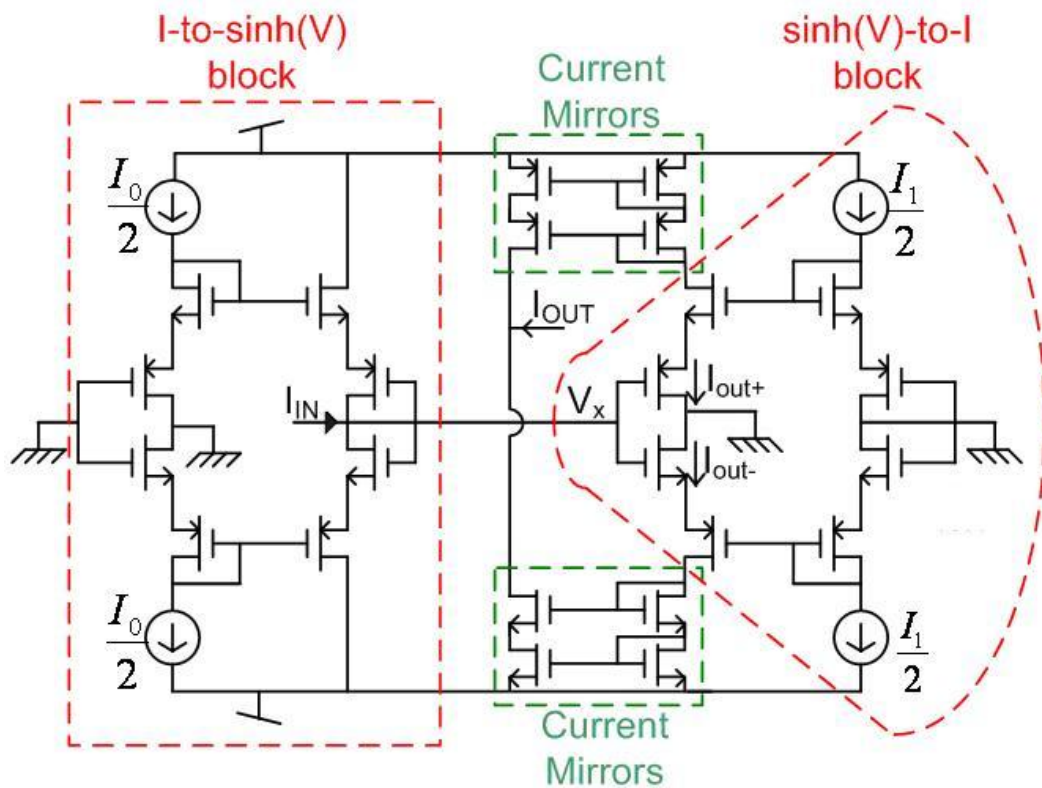


FIGURE 5.18: Sinh Class AB Current Amplifier topology

It utilizes MOS transistors in their weak inversion region exploiting their exponential relationship between the drain current and the gate source voltage. By doing this, an input current may be converted to a Sinh voltage (I to $\sinh(V)$) via a bias current I_0 . With a small modification to the circuit, the reverse may be performed and a voltage to inverse Sinh current may be achieved (V to $\sinh^{-1}(I)$) via bias current I_1 . In doing so a 'current to Sinh voltage to current' (I to $\sinh(V)$ to I) conversion is performed, thereby making the circuit Externally Linear, but Internally Nonlinear (ELIN). The ideal gain of the circuit is given by the ratio of I_1 to I_0 . A current mode current amplifier has been designed.

Chapter 6

Sinh Current Amplifier Results

Combining the Current Conveyor and the Sinh Current Amplifier creates a current-mode sensor interface circuit that can perform the same function as that of the op-amp based current amplifier on the right hand side of figure 3.13 (simplified in figure 6.1). Figure 6.2 shows the proposed circuit to replace the circuit in figure 6.1.

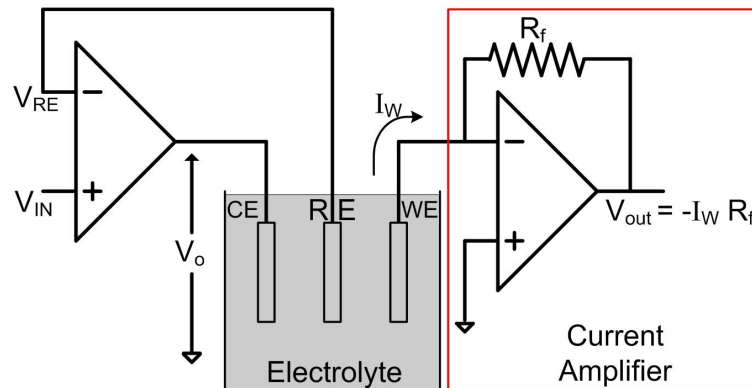


FIGURE 6.1: Traditional three electrode potentiostat theoretical measurement. Extracted from [38]

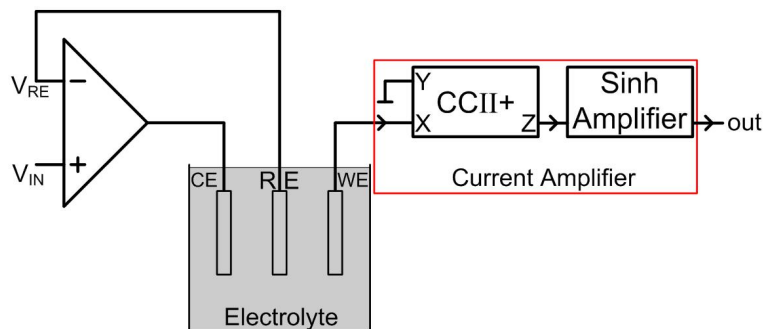


FIGURE 6.2: Proposed three electrode potentiostat theoretical measurement

The Current Amplifier in figure 6.1 performs two functions, firstly it provides a virtual ground node for the current to flow into. Secondly the op-amp is required to provide sufficient gain. The disadvantage of the op-amp is that the input node is directly connected to a large resistor. Resistors are inherently noisy devices, this causes large amounts of noise to be placed on the input signal. Op-amps also require a number of passive components making them bulky. These undesirable attributes can be overcome by the proposed current mode design figure 6.3. As explained in chapter 5 a virtual ground is provided when node Y is connected to ground, and may provide gain of 1000x (tested).

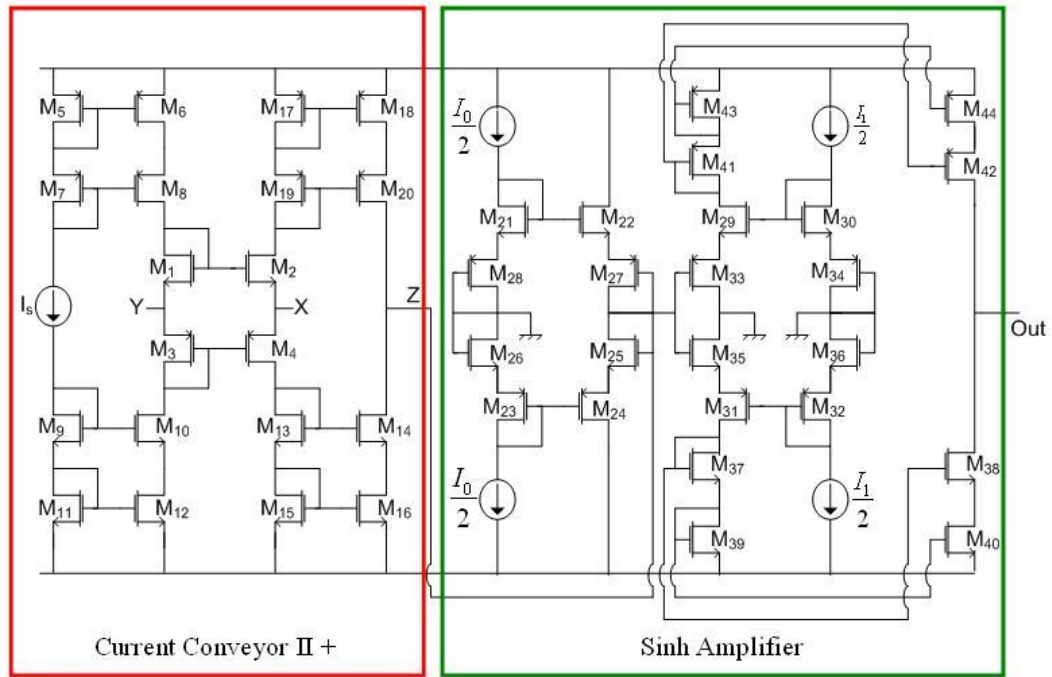


FIGURE 6.3: Current Mode Sensor Interface Circuit

This chapter provides simulated and measured results of the proposed sensor-interfacing topology. The topology shown in figure 6.3 has been fabricated in two commercially available CMOS technology, the AMS 0.8 μ m and the AMS 0.35 μ m. In what follows we provide simulated and measured results from both technologies.

6.1 AMS 0.8 μ m Results

6.1.1 Simulation Results

Figure 6.4 illustrates typical small-signal AC responses for current gains of 20, 40 and 60 dB's.

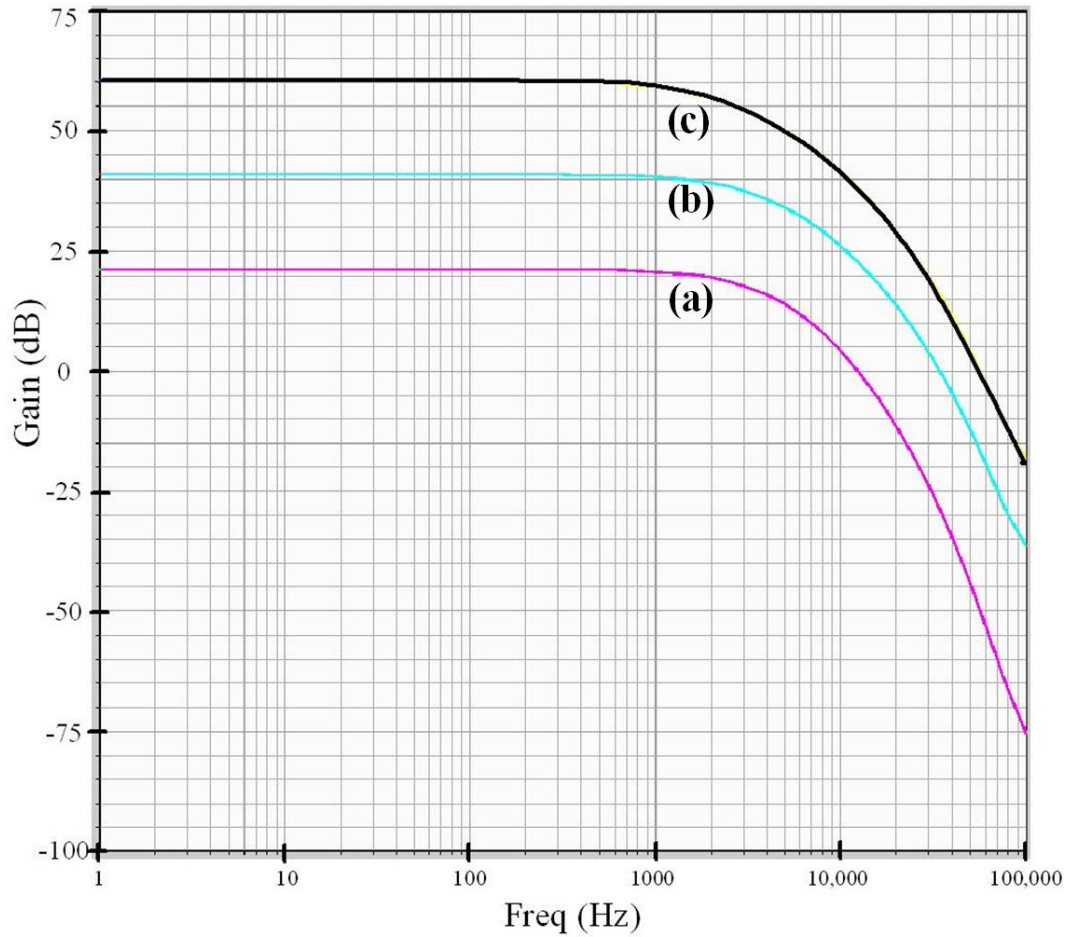


FIGURE 6.4: Typical Frequency responses of the topology of figure 6.3 gains of (a) 20, (b) 40 and (c) 60dB's

Observe that the -3dB bandwidth ranges from 1.15kHz (20dB gain) to 1.05kHz (60dB gain). The 20, 40 and 60dBs gain factor were achieved with the $\frac{I_0}{2}$ current value set to 1nA, whereas the $\frac{I_1}{2}$ current value is set to 12n, 140n and 2050nA respectively. Figure 6.5 illustrates typical transient responses for an input frequency of 100Hz and the gain set to x10, x100 and x1000.

Figure 6.6 illustrates the dependence of the output current THD levels as a function of the amplitude of the input current signal when the input current frequency is set to 100Hz.

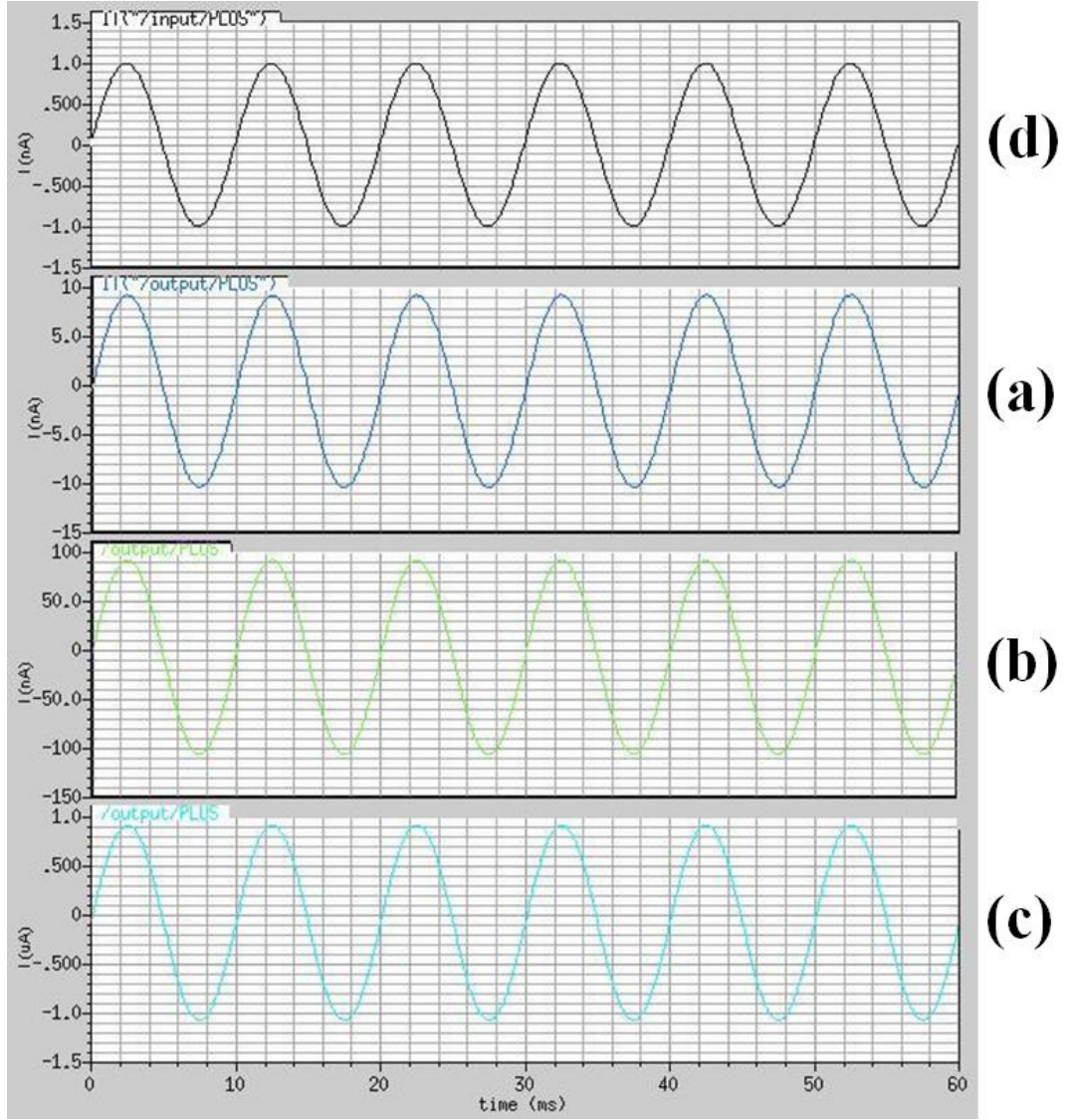


FIGURE 6.5: Typical Transient Waveforms of the topology of figure 6.3 for gains of (a) x10, (b) x100 and (c) x1000 and the (d) input current

Figure 6.7 illustrates the dependence (and deviation from ideality) of the output current I_{out} when the amplitude of the input current I_{in} varies for gains set to x10, x100 and x1000.

Observe that for input currents higher than 3nA deviations from ideality occur. This should be attributed to derivations of the devices from the exponential conformity of the weak inversion region with some of the devices entering the triode region for high input current and gain values. Table 6.1 summarizes the simulated results corresponding to the $0.8\mu\text{m}$ CMOS Sinh Amplifier, whereas table 6.2 codifies sizes of all the devices shown in figure 6.8

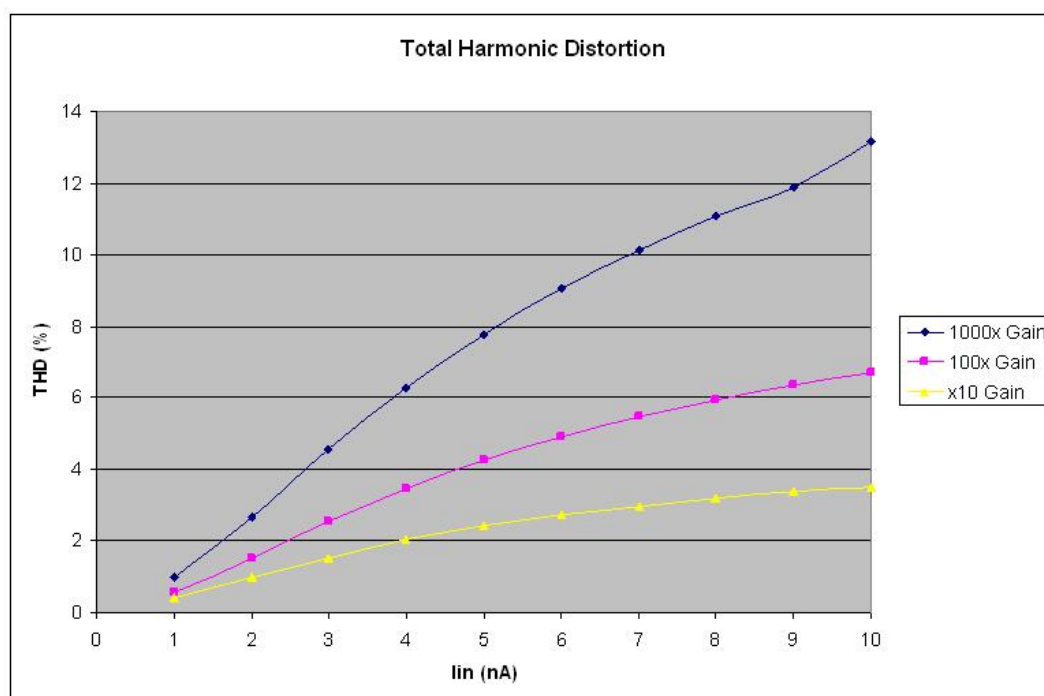


FIGURE 6.6: Output THD

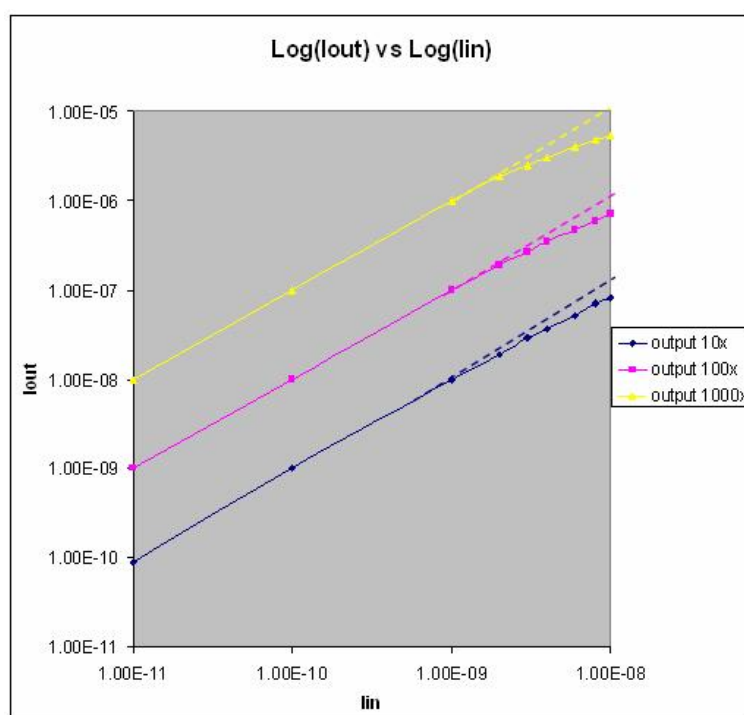


FIGURE 6.7: Current Input vs Current Output

Current Gain factor Nominal	Output impedance of the sensor (Ω)	current gain deviation (%)	Bandwidth (kHz) (3dB cut-off point)	Current consumption (A)	Power Supply (V)	Technology
x1000	1G	3	2.45	5 μ	± 4	0.8 μm
	100M	4	2.65			
	50M	4	2.44			
	10M	15	2.65			
x100	1G	4	3.5	500n		
	100M	3	3.5			
	50M	4	3.5			
	10M	15	3.5			
x100	1G	≤ 1	2.8	110n		
	100M	5	2.8			
	50M	5	2.8			
	10M	15	2.8			

TABLE 6.1: Sinh Current Amplifier Specifications

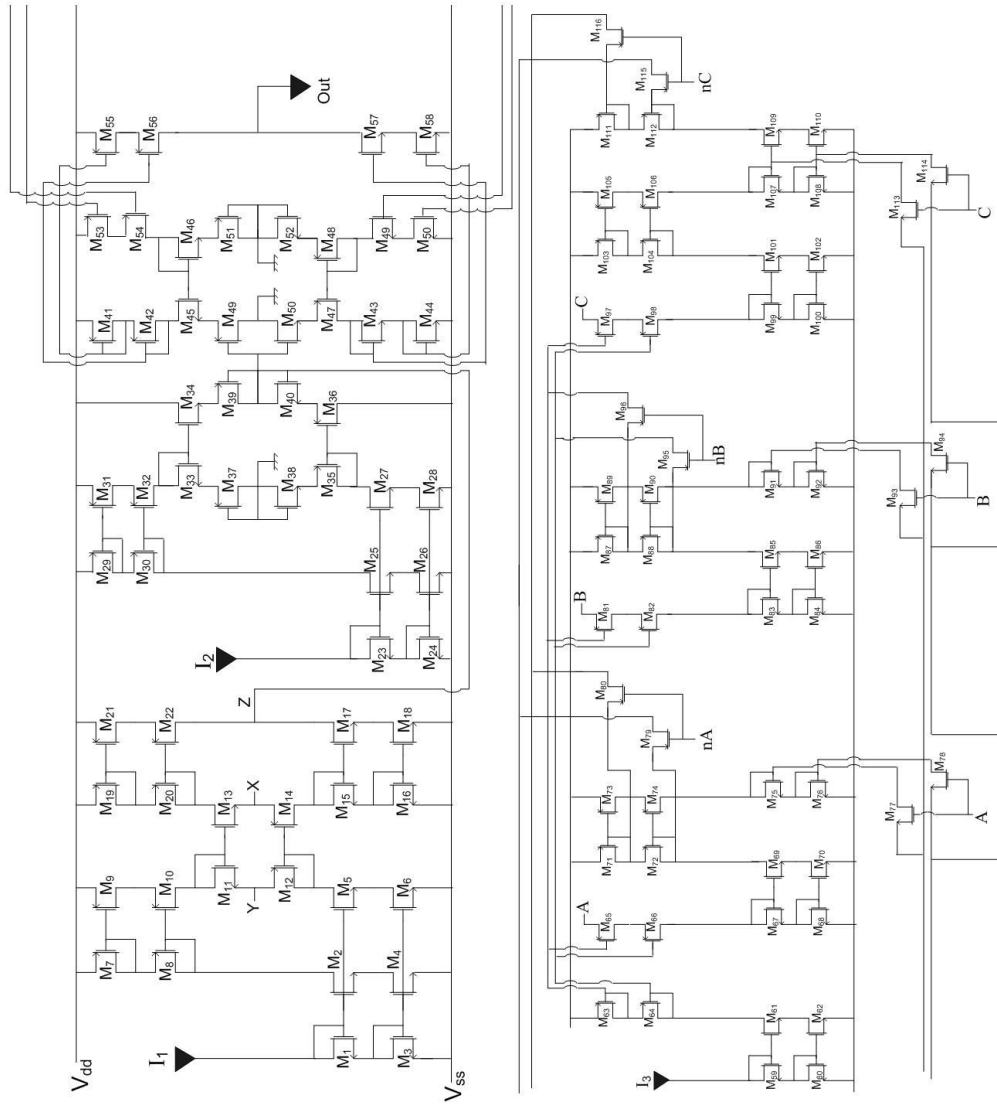


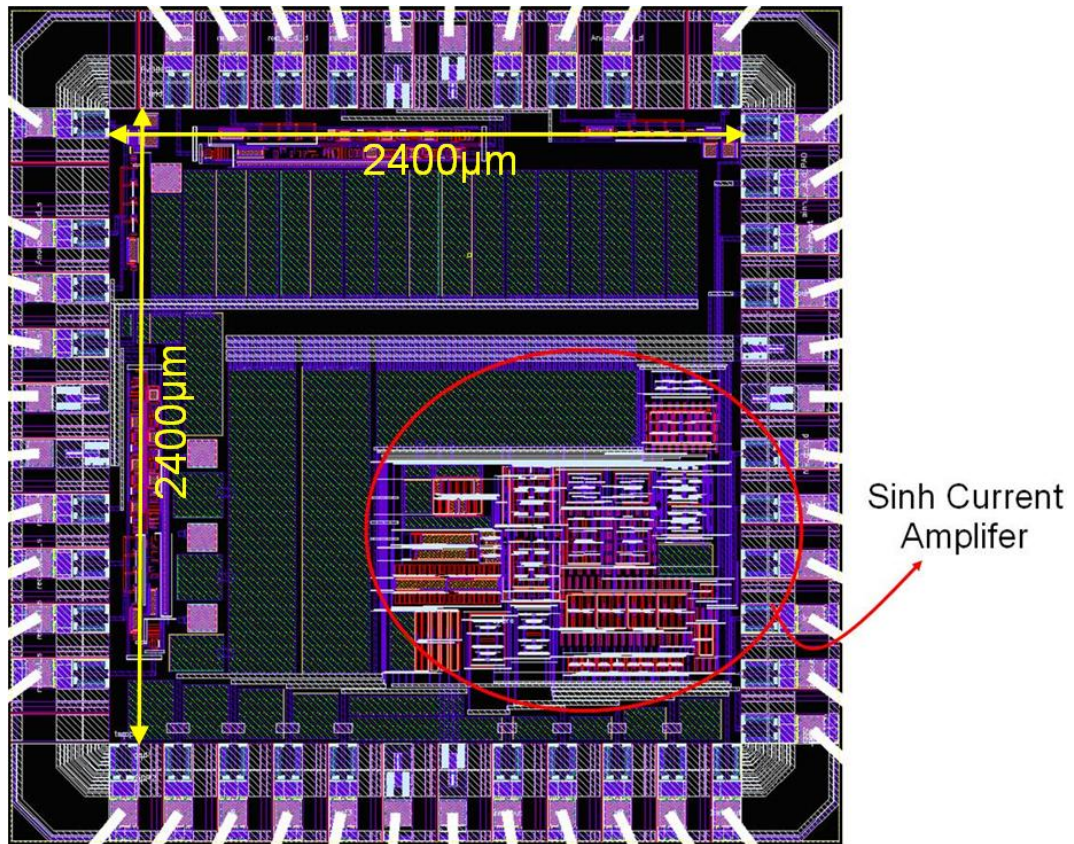
FIGURE 6.8: Sinh Amplifier transistor topology in 0.8μm process

$M_{55/56/65/66}$	$200\mu\text{m} / 10\mu\text{m}$
$M_{57/58}$	$70\mu\text{m} / 10\mu\text{m}$
$M_{67/68/83/84}$	$35\mu\text{m} / 190\mu\text{m}$
$M_{67/68/83/84}$	$35\mu\text{m} / 190\mu\text{m}$
$M_{69/70}$	$385\mu\text{m} / 10\mu\text{m}$
$M_{71/72}$	$100\mu\text{m} / 20\mu\text{m}$
$M_{85/86}$	$105\mu\text{m} / 10\mu\text{m}$
$M_{99/100}$	$35\mu\text{m} / 10\mu\text{m}$
all other NMOS	$35\mu\text{m} / 10\mu\text{m}$
all other PMOS	$100\mu\text{m} / 10\mu\text{m}$

TABLE 6.2: Transistor sizes of Sinh Current Amplifier depicted in figure 6.8

6.1.2 Measured Results

Figure 6.9 illustrates the AMS $0.8\mu\text{m}$ mask layout of the sinh amplifier shown in Figure 6.8 whereas Figure 6.10 illustrates the $0.8\mu\text{m}$ chip microphotograph.

FIGURE 6.9: AMS $0.8\mu\text{m}$ mask layout of the Sinh Amplifier

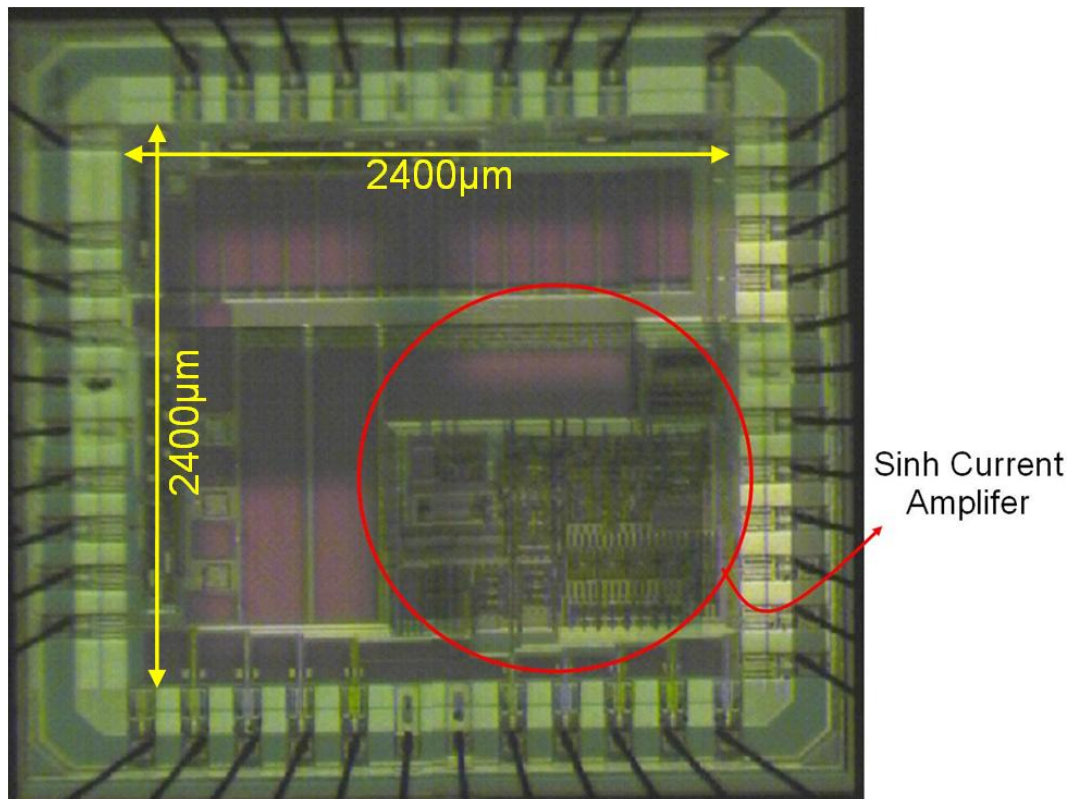


FIGURE 6.10: 0.8μm chip microphotograph

Figure 6.11 depicts the laboratory setup for testing the Sinh current amplifier. Keithleys provide accurate current bias's, while dual voltmeters allow the positive, negative and ground supply rails.

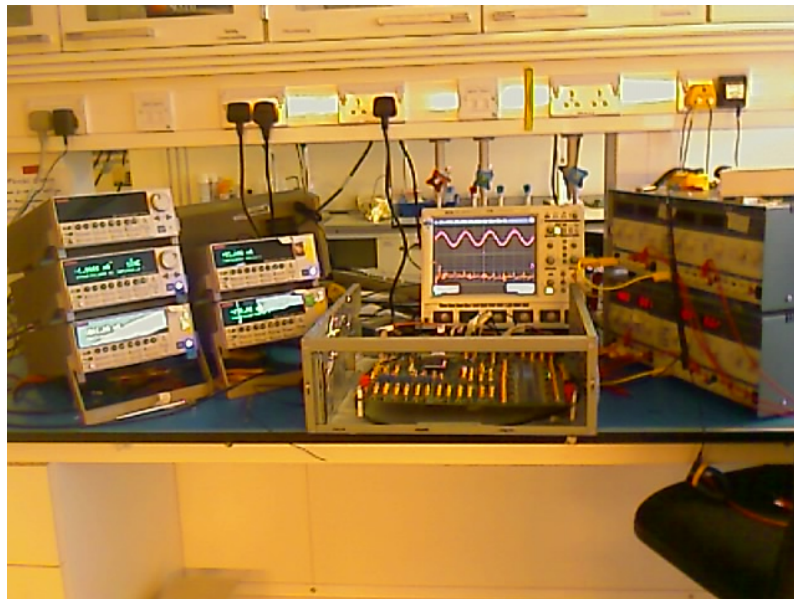


FIGURE 6.11: Test and measurement setup

Figure 6.12 illustrates the basic experimental setup for testing the Sinh current amplifier.

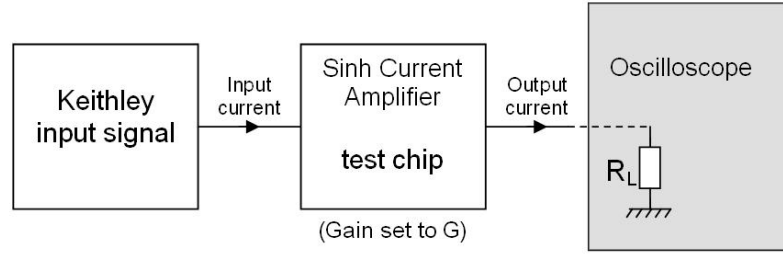


FIGURE 6.12: Laboratory setup for the Sinh Current Amplifier

Details of the set gain G and R_L are provided in the legend of figures 6.13, 6.14 and 6.15

Figure 6.13, 6.14 and 6.15 illustrates the measured AC responses from 5 separate chips (Chip 10, 11, 13, 18 and 19) for gains of x10, x100 and x1000 respectively when the input amplitude varies. Figure 6.16, 6.17 and 6.18 represent the dB gain vs Log frequency of the graphs in figures 6.13, 6.14 and 6.15 respectively.

Referring to figure 6.13, observe that for input currents below 7nA's we achieve accurate x10 amplification. In these cases the 3dB bandwidth was measured to be $\approx 160\text{Hz}$. For input currents higher than 6nA the circuit exhibits deviations from the ideally achievable gain due to the fact that not all devices operate in weak-inversion.

Figure 6.14 and 6.15 corresponds to x100 and x1000 gains respectively when the input amplitude varies. Deviations now occur from the 3nA input current onwards. For each of the x10, x100 and x1000 measured results $\frac{I_o}{2}$ was set to 1nA, whereas $\frac{I_i}{2}$ was set to 11nA, 135nA and 2200nA respectively.

Figure 6.16, 6.17 and 6.18 illustrates the dB responses corresponding to the gain factors of the x10, x100 and x1000 respectively.

Consider the result when the input current I_{IN} is set to 1nA for chips 10-19 of the Sinh Current Amplifier, with the amplification set to x10 (illustrated in figure 6.13). The overlapping lines show small chip-to-chip variations which suggest the viability of the Sinh Current Amplifier as far as manufacturing is concerned.

(Note also that the chip numbers tested for the Sinh Current Amplifier are from 10 to 19, this is due to the fact that the chips 1-9 have been used and tested for the radio blocks presented in the next section.)

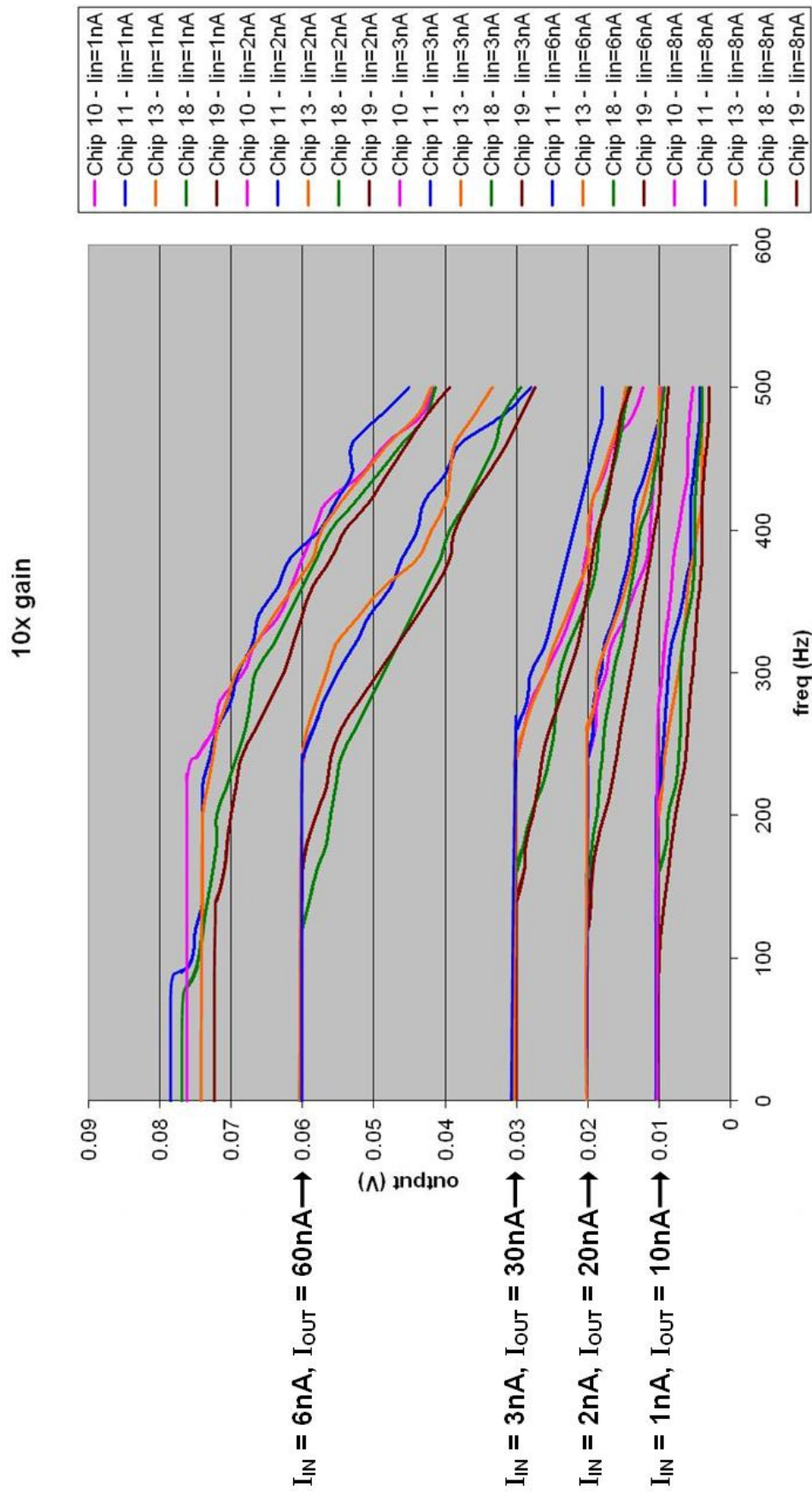


FIGURE 6.13: $I_{in} = 1n, 2n, 3n, 6n$ and $8n$ for the test conditions (see figure 6.12): $G = 10, R_L = 1M\Omega$

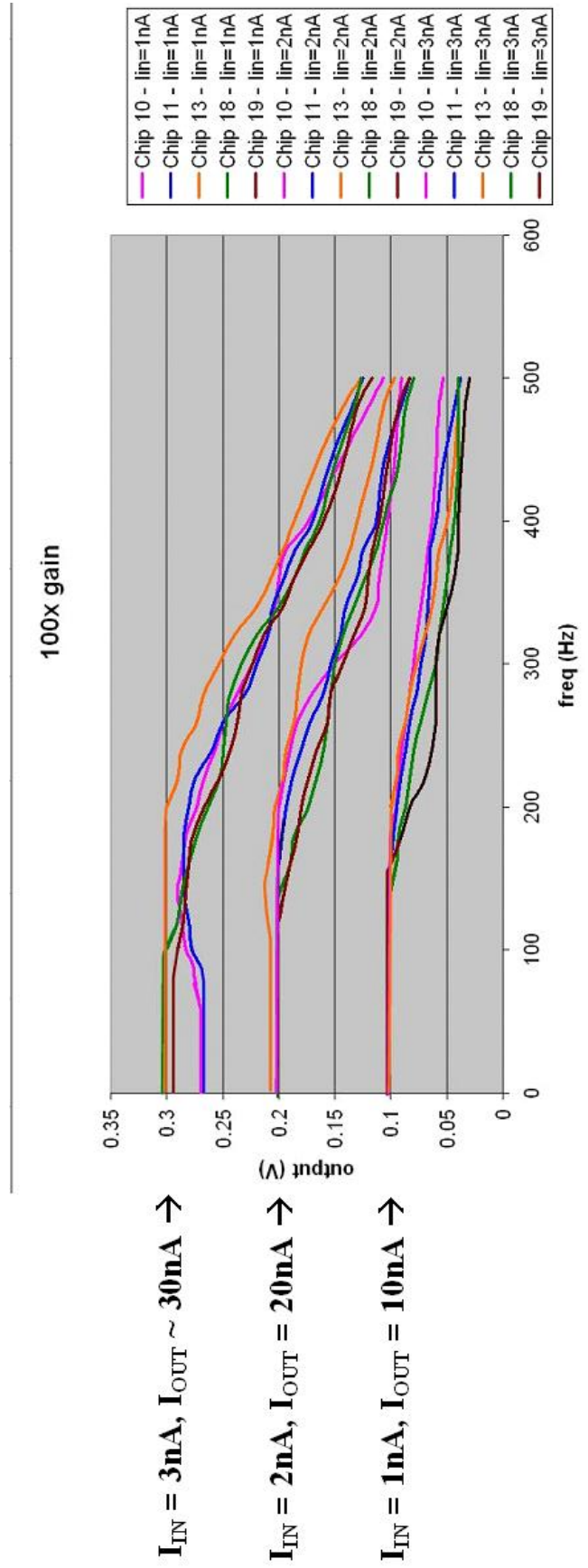


FIGURE 6.14: $I_{in} = 1n, 2n$ and $3n$ for the test conditions (see figure 6.12): $G = 100, R_L = 1M\Omega$

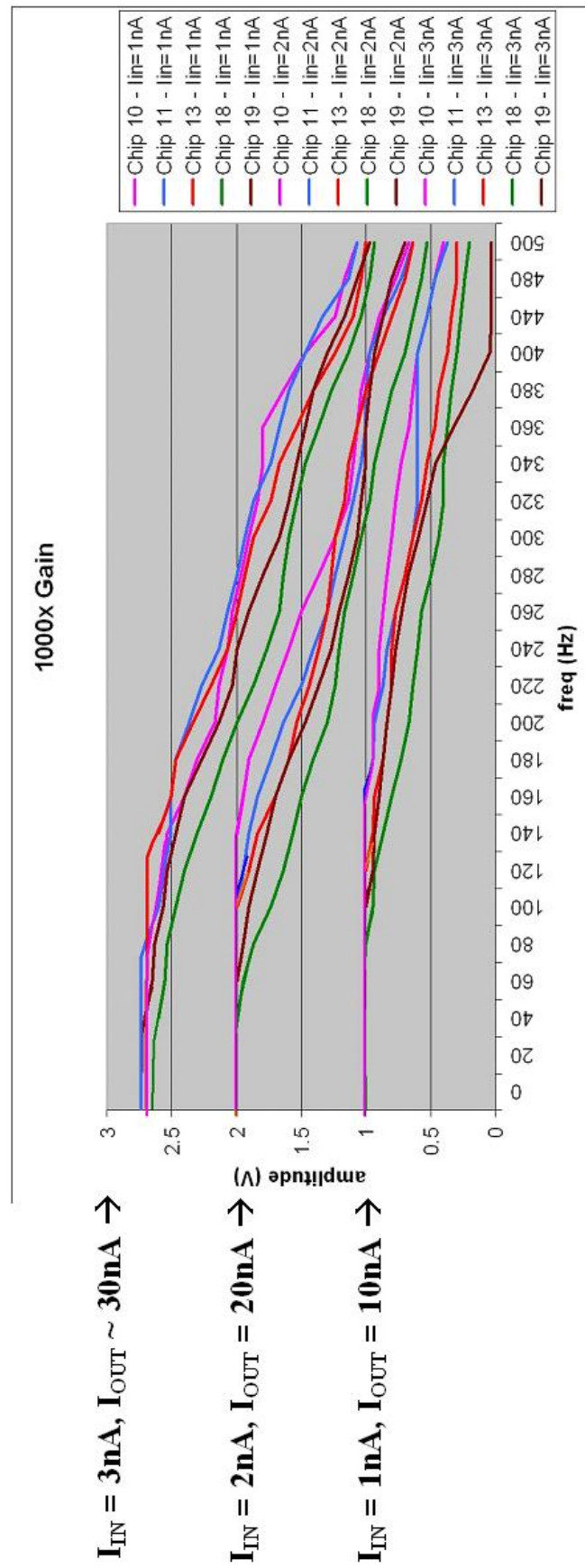


FIGURE 6.15: $I_{in} = 1n, 2n$ and $3n$ for the test conditions (see figure 6.12): $G = 1000, R_L = 1M\Omega$

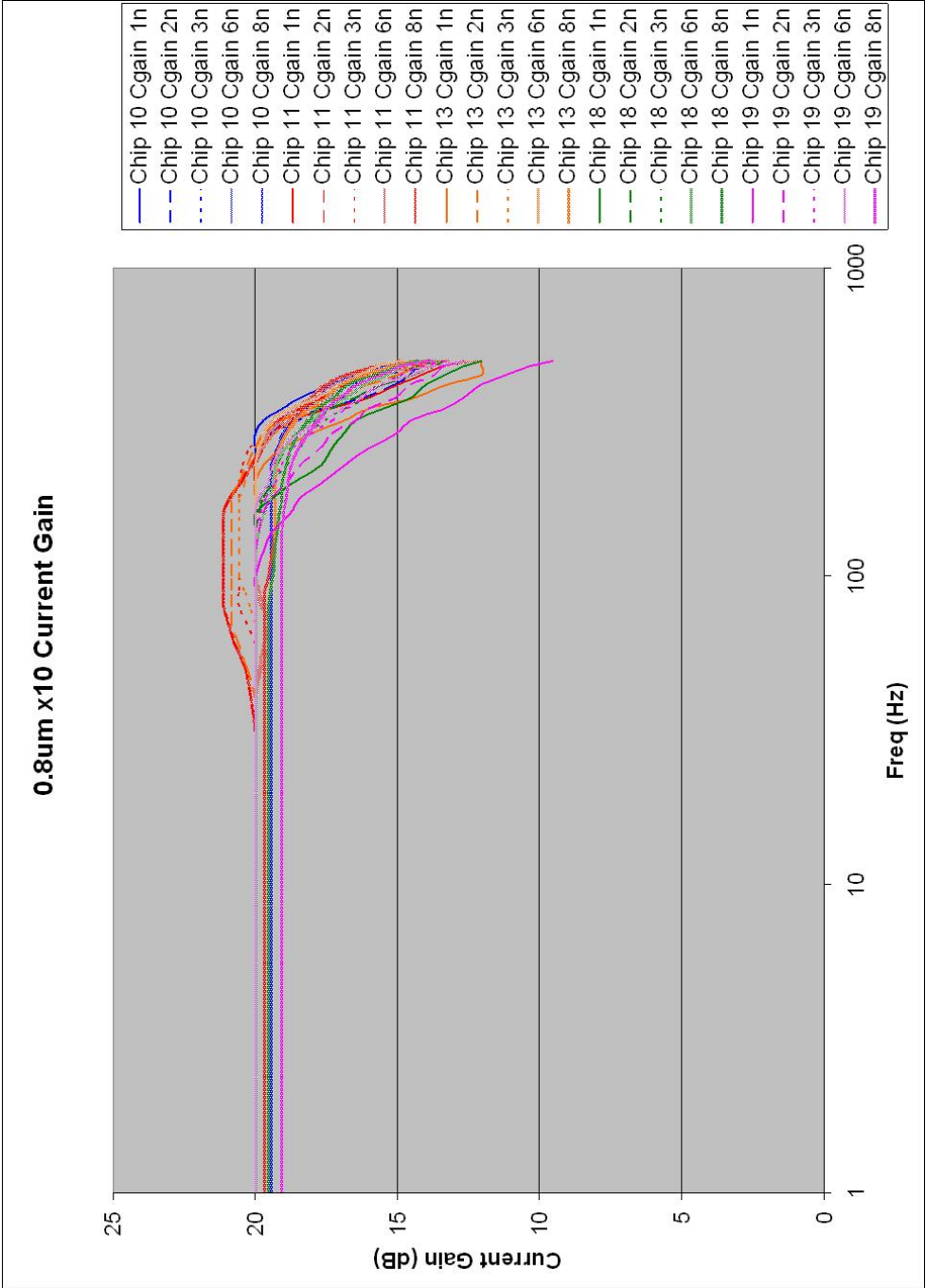


FIGURE 6.16: 20dB Gain for $I_{in} = 1n, 2n, 3n, 6n$ and $8n$

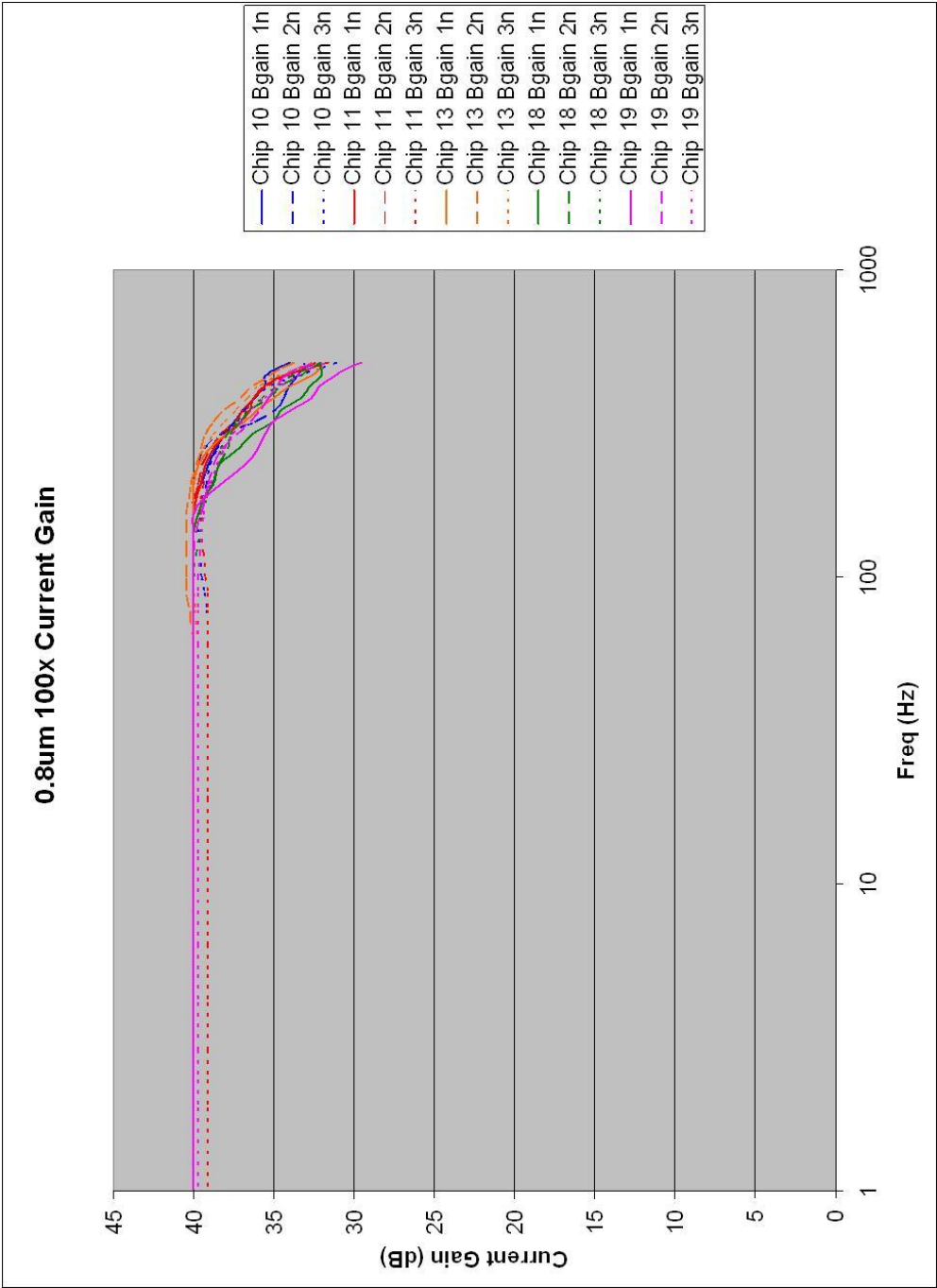


FIGURE 6.17: 40dB Gain for $I_{in} = 1n, 2n$ and $3n$

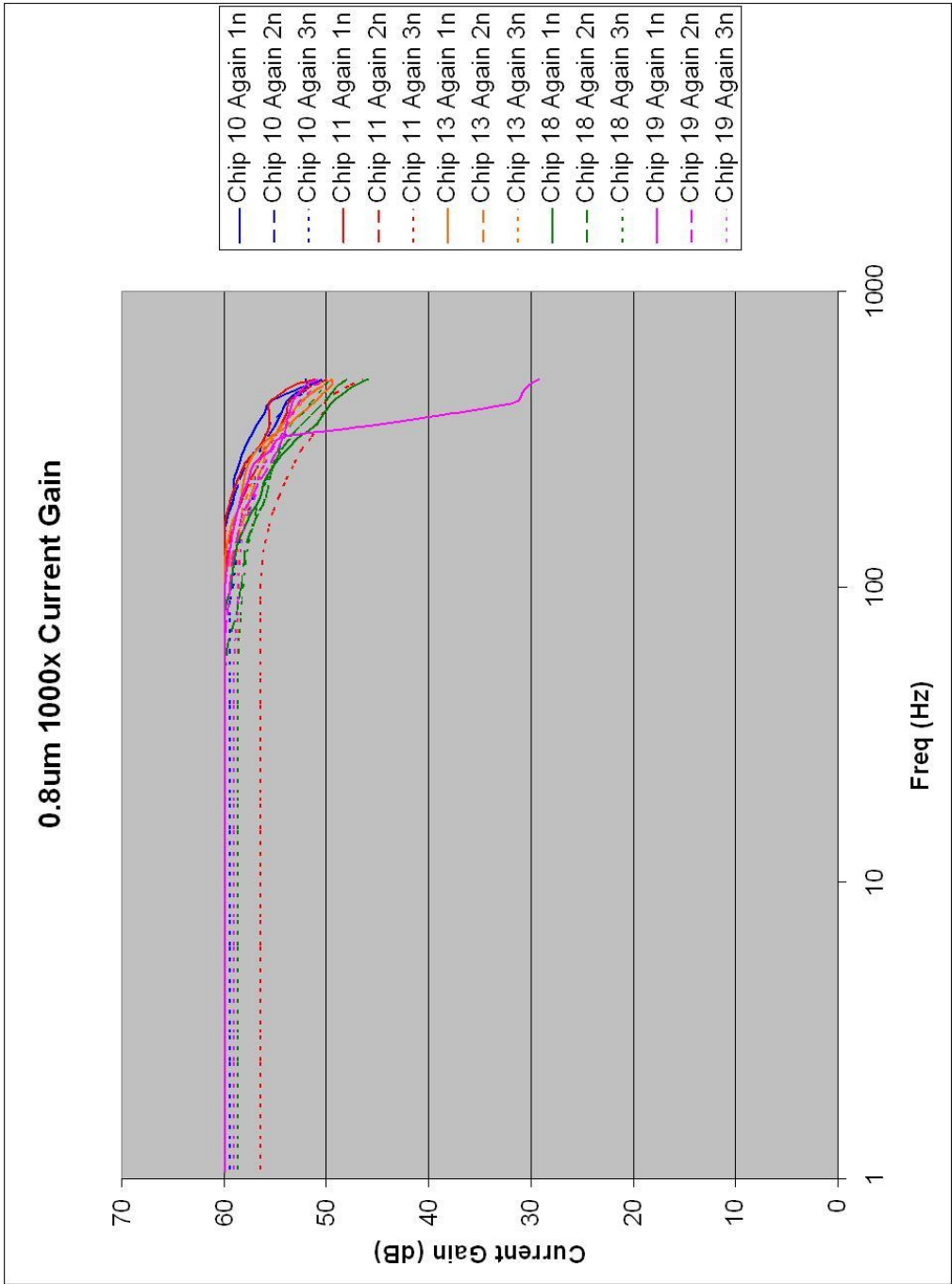


FIGURE 6.18: 60dB Gain for $I_m = 1n, 2n$ and $3n$

Figure 6.19 illustrates a typical transient response for the x1000 gain case when $I_{in} = 2nA$ and the input tone has a frequency of 80Hz. Observe that the second harmonic situated at 160Hz lies 40dB below the 80Hz fundamental corresponding to 1% HD_2 . For screened measurements this difference becomes even smaller since the impact of 50Hz noise is displayed.

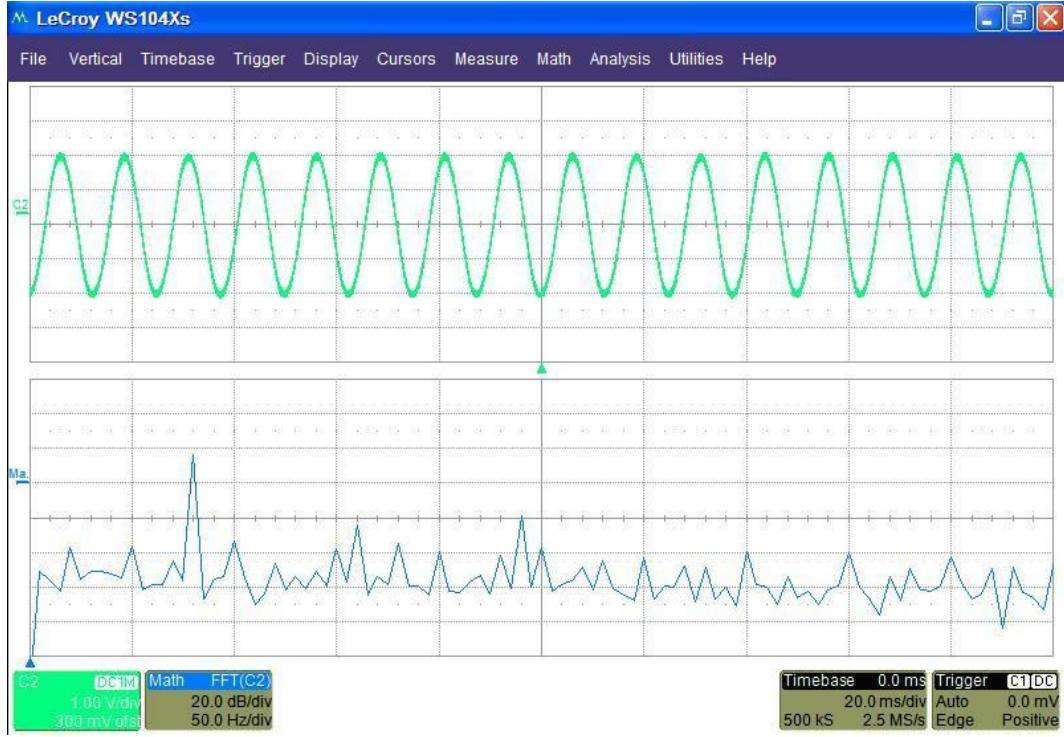


FIGURE 6.19: $I_{in} = 2nA$ at 80 Hz at 1000x gain

6.2 AMS 0.35 μm Results

The proposed combination of the current conveyor and sinh amplifier shown in figure 6.3 was also fabricated in the AMS 0.35 μm process. Given that the 0.8 μm simulation results presented in the previous section are representative and confirm the validity of the proposed amplification scheme, in this section we proceed by presenting measured results from the 0.35 μm . Figure 6.20 shows the mask layout of the 0.35 μm design whereas figure 6.21 illustrates a microphotograph of the chip. Figure 6.22 illustrates the total schematic layout of the AMS 0.35 μm Sinh Current Amplifier while table 6.3 lists the device sizes.

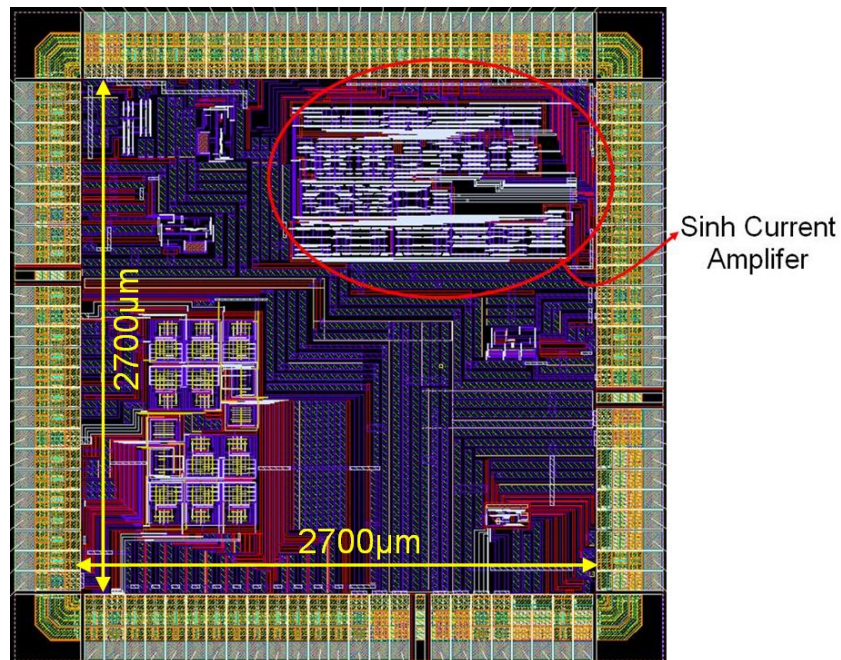


FIGURE 6.20: AMS 0.35μm mask layout of the Sinh Amplifier

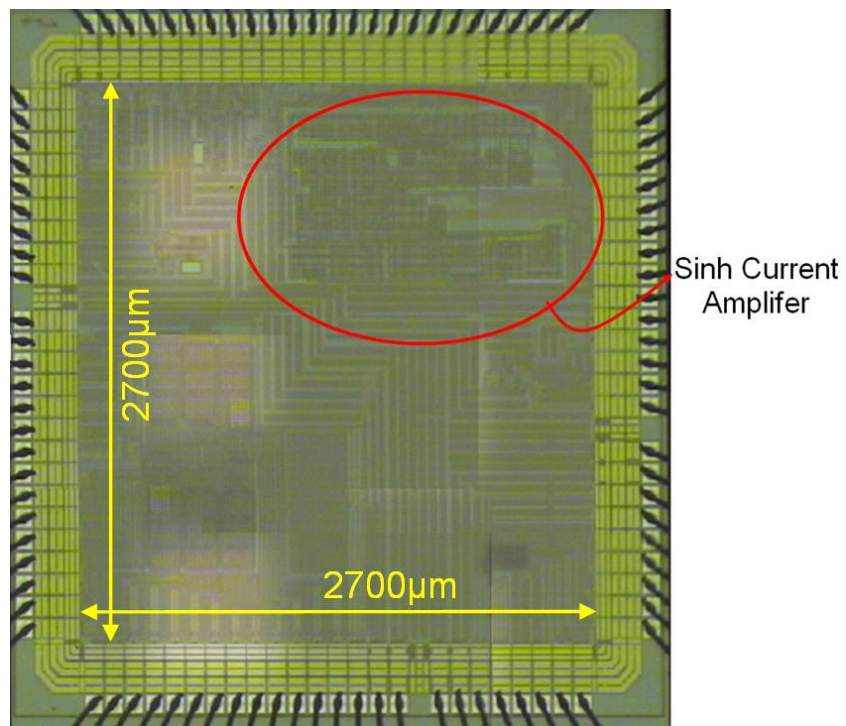


FIGURE 6.21: 0.35μm chip microphotograph

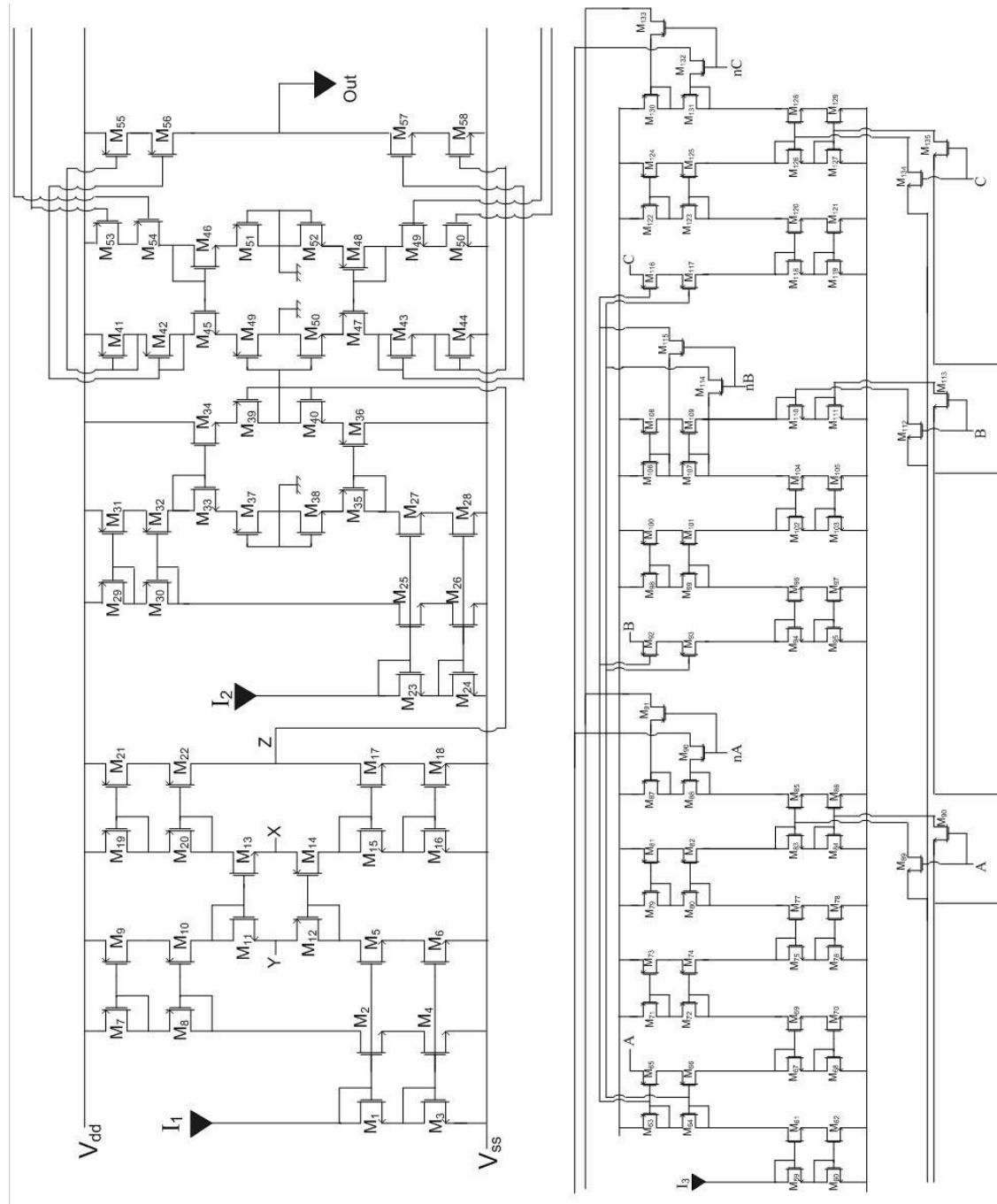


FIGURE 6.22: Sinh Amplifier transistor topology in 0.35μm process

$M_{69/70/77/78}$	315 μm / 10 μm
$M_{73/74/81/82/86/87}$	350 μm / 10 μm
$M_{100/101/124/125}$	140 μm / 10 μm
$M_{96/97}$	350 μm / 10 μm
$M_{104/105}$	245 μm / 10 μm
$M_{120/121}$	210 μm / 10 μm
all other NMOS	35 μm / 10 μm
all other PMOS	70 μm / 10 μm

TABLE 6.3: Transistor sizes of Sinh Current Amplifier depicted in figure 6.22

Figure 6.23 illustrates typical 0.35 μm measured results when the current gain is set to $\times 100$ ($\frac{I_0}{2} = 1\text{n}$ and $\frac{I_1}{2} = 140\text{n}$) and the input current amplitude takes the values of 10, 15 and 20nA. Measured results from five chips (chip 2, chip 3, chip 4, chip 5 and chip 6) are provided. As shown in figure 6.24 the roll-off for the 0.35 μm designs starts at 200Hz with the -3dB point reached at 400Hz.

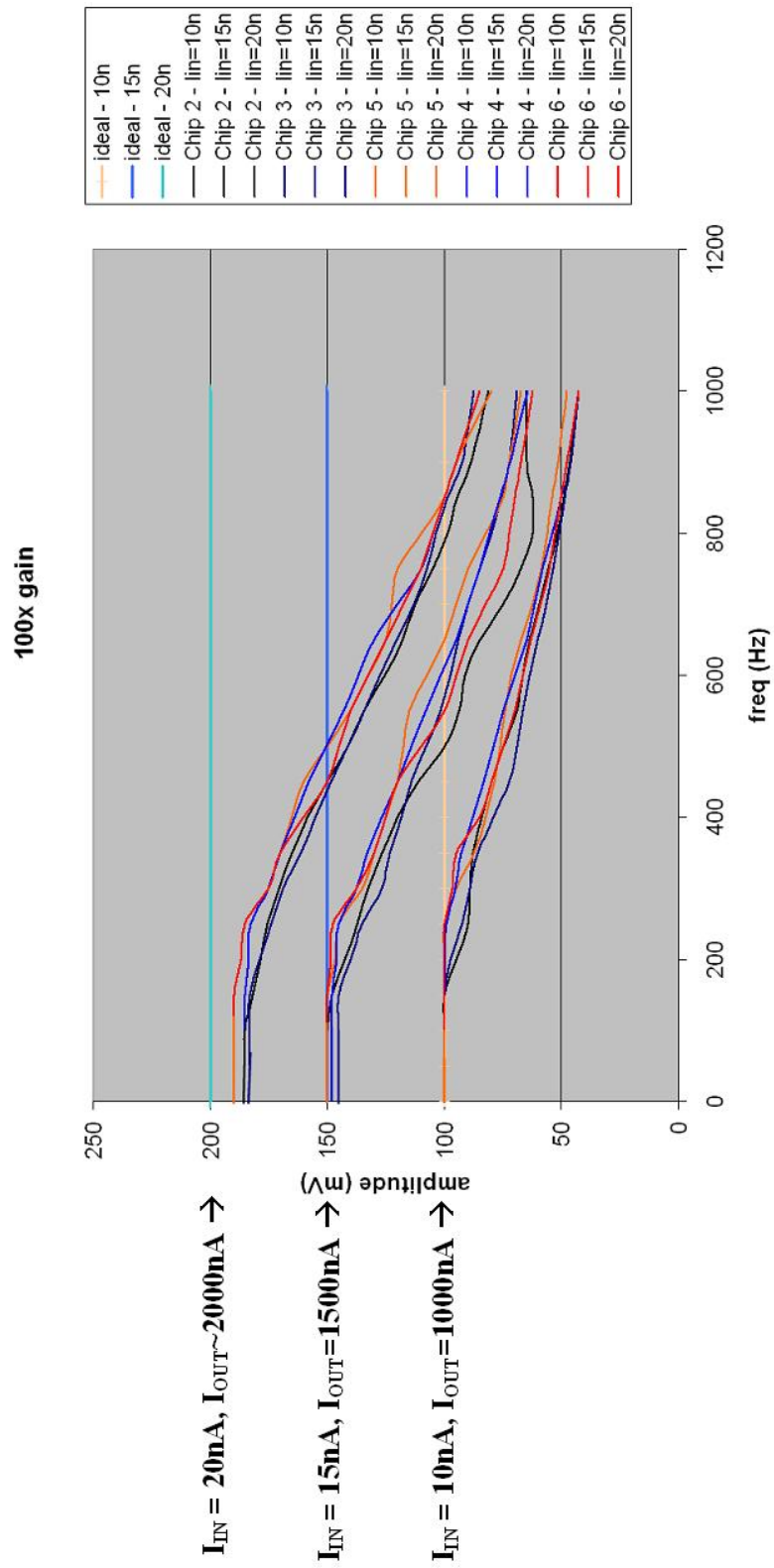


FIGURE 6.23: $I_{in} = 10\text{n}$, 15n and 20nA for the test conditions (see figure 6.12): $G = 100$, $R_L = 100\text{k}\Omega$

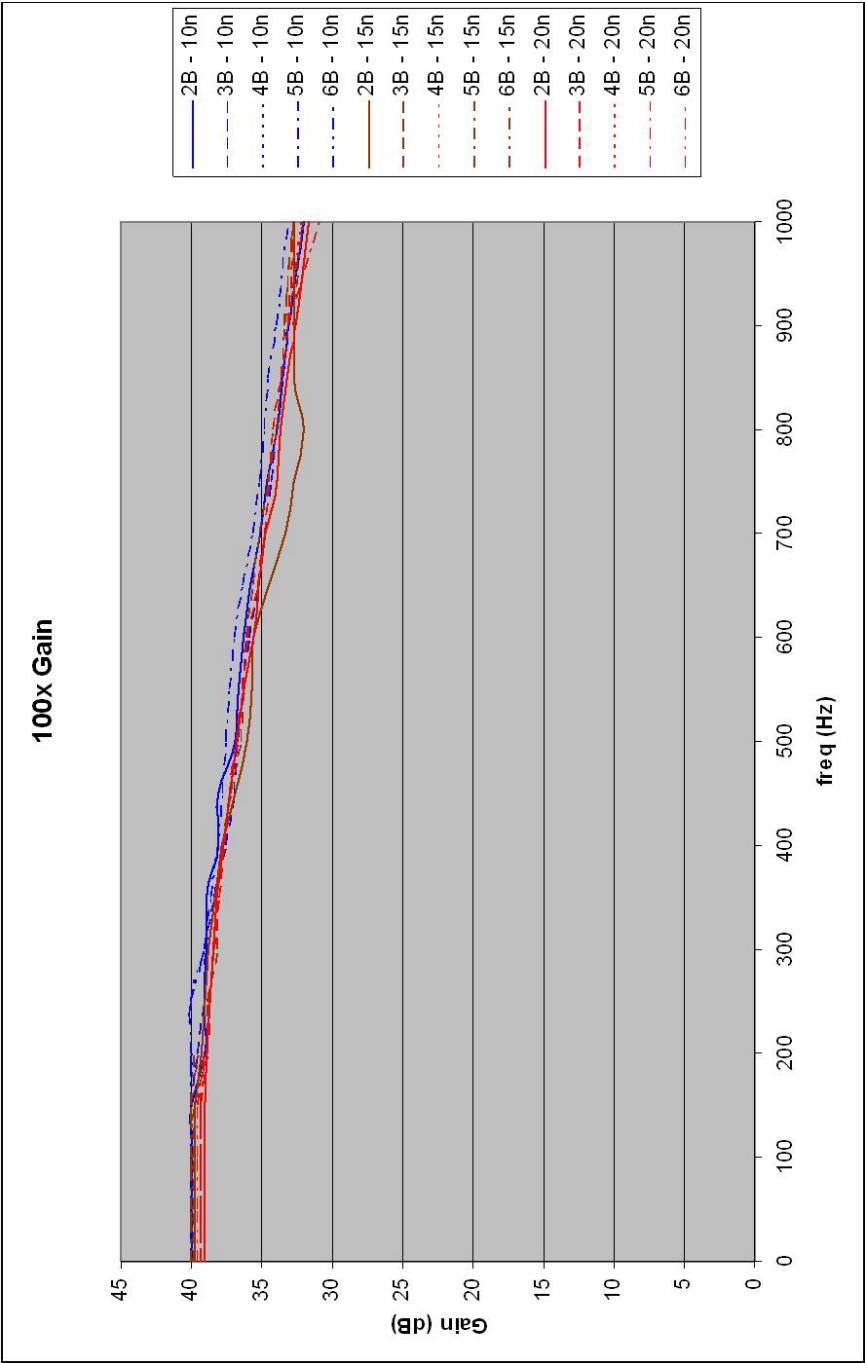


FIGURE 6.24: 100x Gain for $I_{in} = 10n, 15n$ and $20nA$

Figure 6.25 illustrates a typical transient response for the x100 gain case when the single tone input current amplitude is set to 10nA at 80Hz. Observe that the 160Hz second harmonic is 28dBs below the 80Hz fundamental.

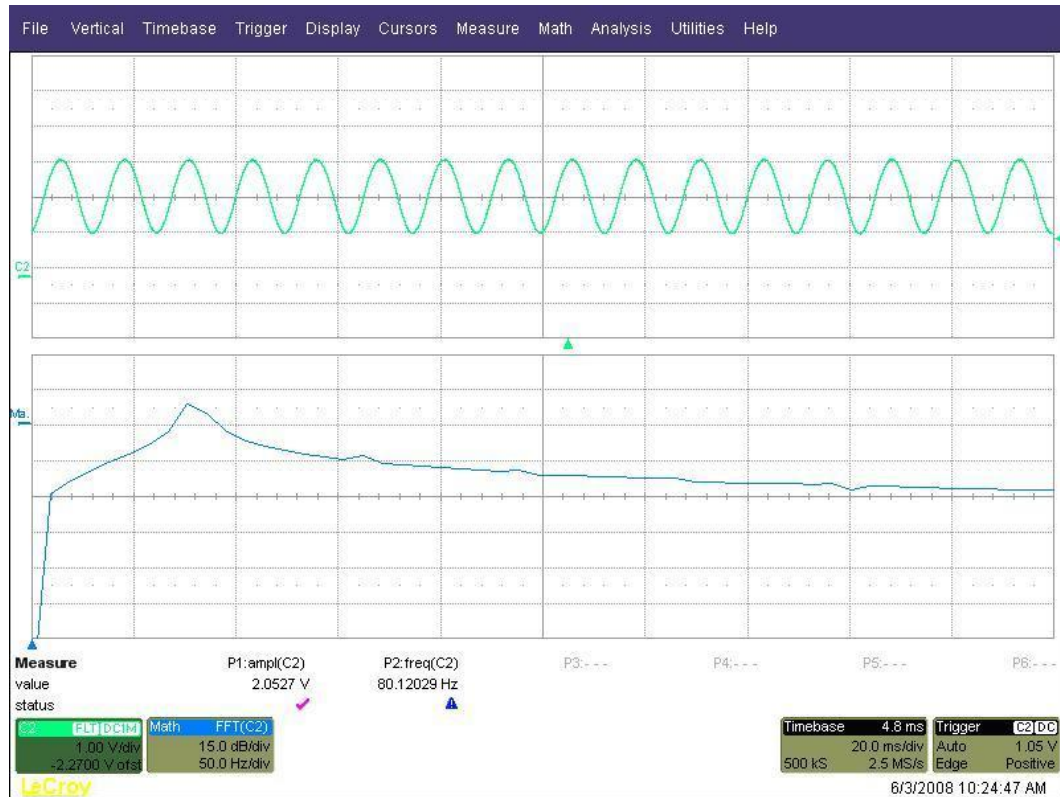


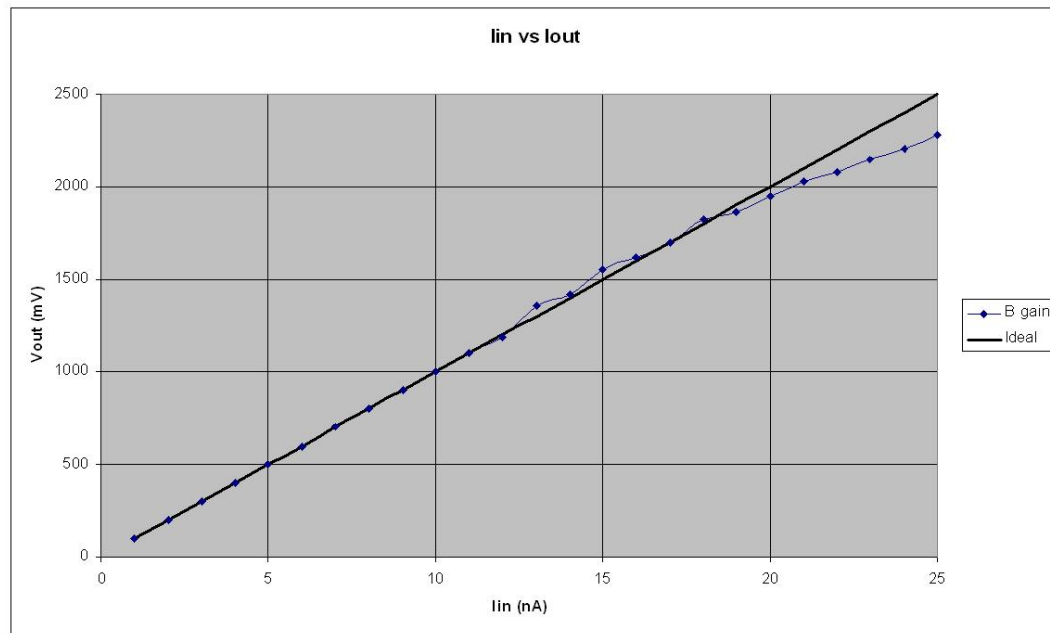
FIGURE 6.25: Transient and frequency spectrum measured results for a gain of x100 when the single tone input current amplitude is set to 10nA at 80Hz

Figure 6.26 depicts the input - output response of the 100x gain of the 0.35 μ m Sinh Amplifier. Linear and accurate gain is held between 0 - 20nA.

6.3 Conclusion

6.3.1 General

A novel current mode sensor interface circuit has been designed. The results were confirmed by simulations and practically in a lab. Gain of 1000x was achieved and recorded while maintaining linearity. The specifications are shown in table 6.4.

FIGURE 6.26: I_{in} vs I_{out} for 100x Gain

Gain	x10	x100	x1000	x100
Process	0.8 μ m AMS			0.35 μ m AMS
Power Supply	± 4 V	± 4 V	± 4 V	± 4 V
Power Consumption	0.88 μ W	4 μ W	44 μ W	95 μ W
Size	1300 μ x 1200 μ m			1500 μ x 900 μ m
3dB Point	160Hz			400Hz
Input referred noise integrated over a bandwidth of 1KHz	2pA			2pA
Current Range value for which deviations from nominal gain are below 1%	100p-6n	100p-2.5n	100p-2.5n	3n-16n

TABLE 6.4: Measured Sinh Current Amplifier results

The Sinh current amplifier is presently under patent. Its design provides an alternative to the (currently used) op-amp configuration, thereby providing lower noise to the signal path. The size of the circuit is small enough to allow other circuits to be placed on the same die thereby creating a laboratory on a single chip, while the chip-to-chip variation is small.

6.3.2 Measured results from a practical sensor

The Sinh amplifier was tested as an interface to a practical sensor. A three electrode electrochemical sensor was used, consisting of an Ag/AgCl electrode as a reference electrode, a platinum wire as the counter electrode and a $125\mu\text{m}$ wide platinum disk working electrode. The WE was prepared for the experiment by being polished (5 min in $0.5\mu\text{m } Al_2O_3$, and 10 min in $0.05\mu\text{m } Al_2O_3$). The measurement was set up so that a cyclic voltammetry input signal was fed into a 0.2mM solutions of Ferrocene in aqueous buffer with 0.15M NaCl as the supporting electrolyte. A periodic triangular waveform that oscillated between 0 and -0.7V with a scan-rate of 50mV/sec was applied as the excitation potential the solution. The virtual ground node was applied to the WE via the current conveyor of the Sinh Current Amplifier, while the output current of the WE was recorded by both the Keithley and the Lecroy Oscilloscope. The practical setup is illustrated in figure 6.27.

The results recorded through the prototype Sinh Amplifier chip were plotted on the oscilloscope whereas the results recorded through the Keithley were plotted in Matlab (see figure 6.28)

Referring to figure 6.28, observe that the half period on the oscilloscope corresponds to 8sec. The current amplitude recorded from Keithley and Matlab varies between 5.5nA and -6nA, while in the Sinh Current Amplifier case (gain set to x100) the output voltage was recorded varying from 55mV to -70mV, which means that the sensor current was recorded as varying from 5.5nA to -7nA.

Figure 6.29 illustrates the results from figure 6.28 as a hysteresis curve. The red curve represents the result from the ‘traditional’ method of measurement, and the blue curve, represents the Sinh Current Amplifier’s results.

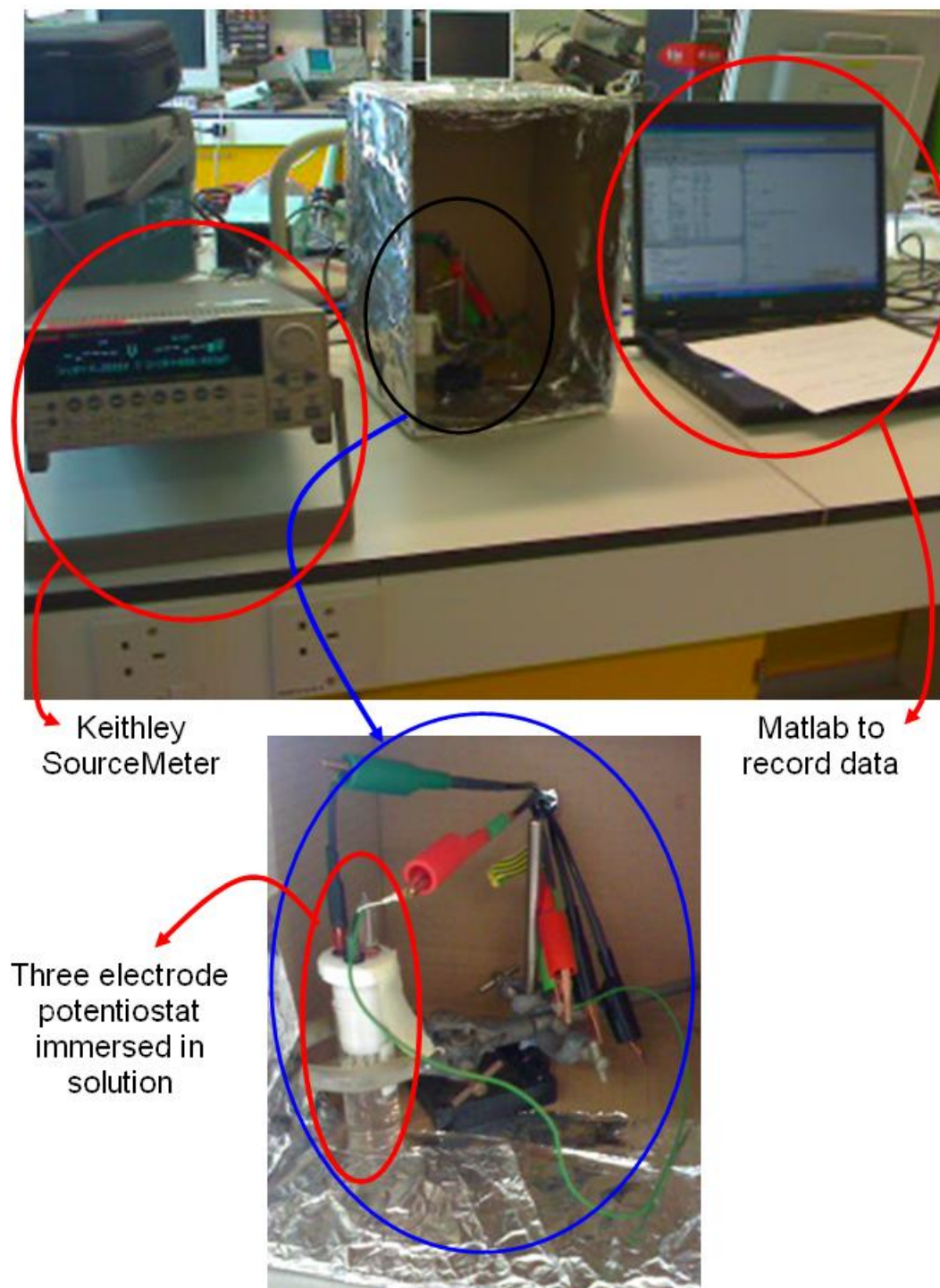


FIGURE 6.27: Practical sensor interfacing setup (Equipment used: Keithley 6220 Precision Current Source and 6221 DC and AC Current Source, TTI Thurlby Thandy Instruments PL320QMT, Lecroy Wavesurfer 434 350MHz Oscilloscope, Lecroy Wavepro 7300A 3GHz Oscilloscope)

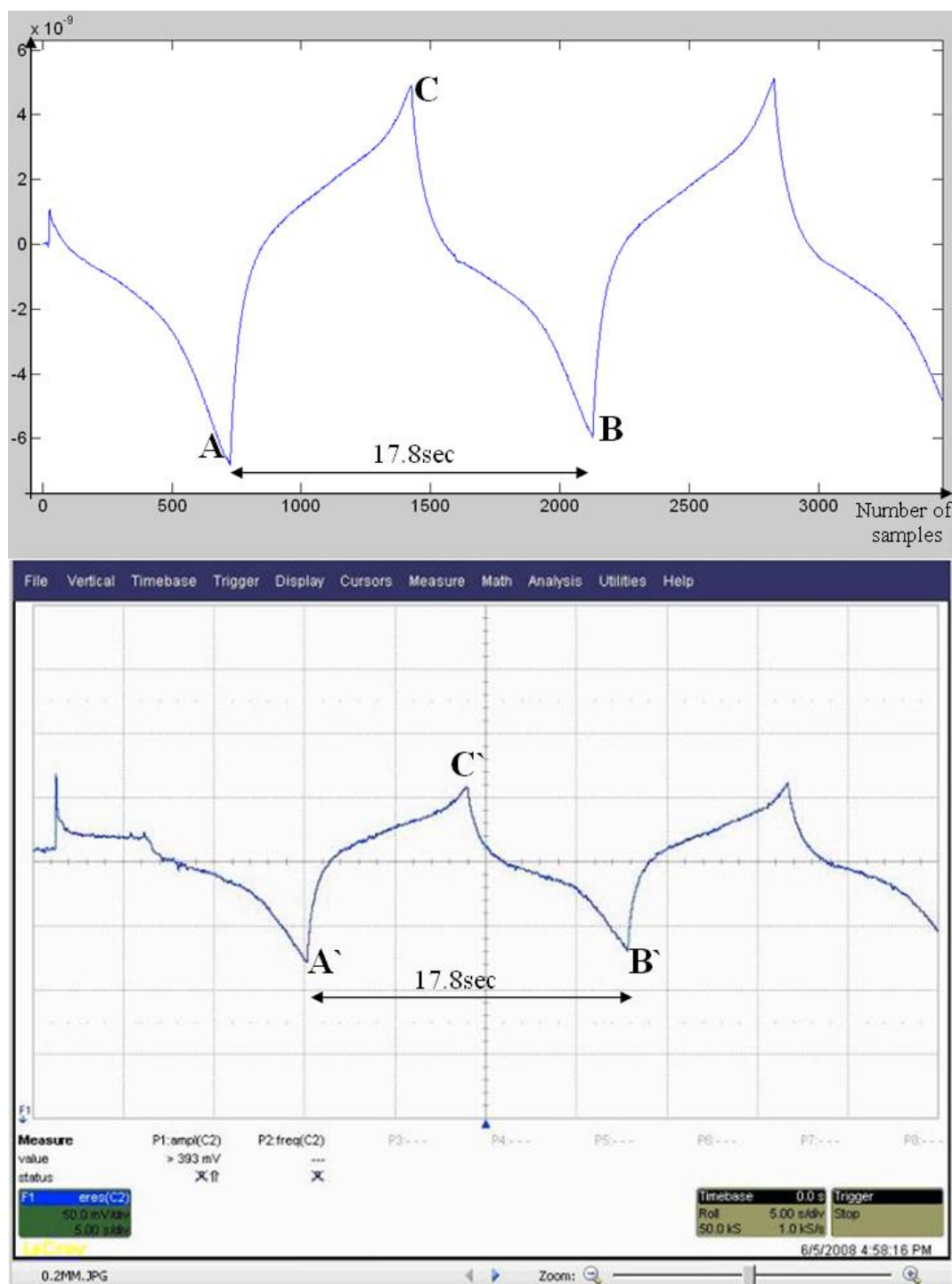


FIGURE 6.28: Results from the 0.2mM solution. a) recorded current from Matlab through Kiethley, and b) recorded current from the Oscilloscope through the Sinh Current Amplifier prototype chip

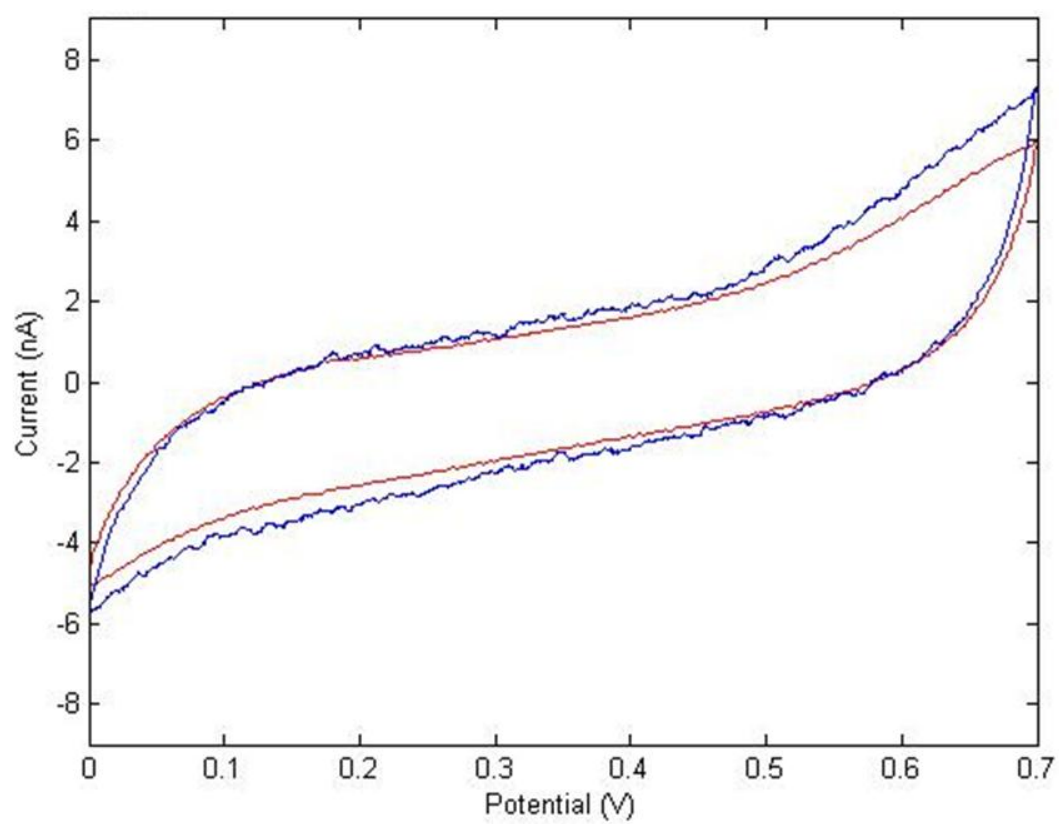


FIGURE 6.29: Hysteresis curve of the results from a 0.2mM solution under a cyclic voltammetry input

Chapter 7

Summary and Discussion of the Sinh Current Amplifier Approach

The demand for an on-line, in-situ, real-time physiochemical monitoring system in order to characterize the behavior of a growing cell-culture has increased in recent years. By recording temporally evolving spatial variations of culture parameter values (e.g. dissolved oxygen, glucose, pH, ammonia, etc), a profile of the culture behavior can be created.

The most common method of current amplification for biological cell cultures takes the form of an op-amp configured as a current amplifier. Figure 7.1 illustrated the typical way of interfacing with chemical electrodes placed within a cell culture.

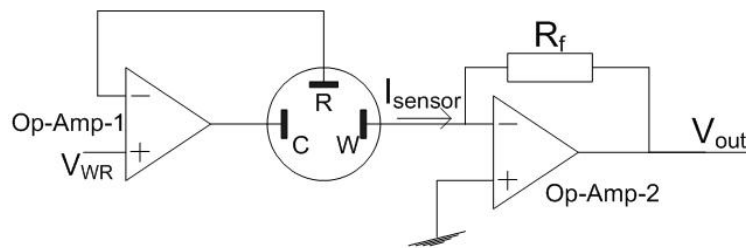


FIGURE 7.1: Typical op-amp-based interfacing with three-electrode sensors

Referring to figure 7.1: the reference (R) electrode ensures the potential drop across the working (W) electrode remains of appropriate value and constant. The counter (C) electrode provides current. The output current flows through the working electrode which is held at virtual-ground for current to be driven into. Op-amp-2 provides sensed current-to-voltage conversion. Note that the sensor current flows through the resistor R_f , a noisy component.

Contrary to the above typical measured setup out Sinh Amplifier-based interfacing can take the form illustrated in figure 7.2

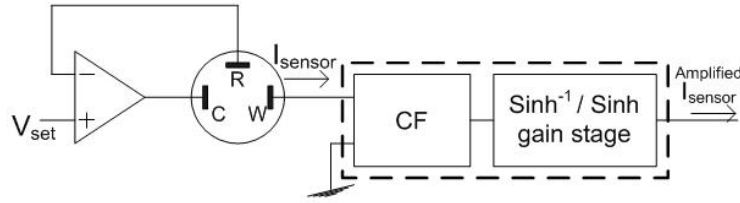


FIGURE 7.2: The Sinh current-amplifier based interfacing (compare with figure 7.1)

A Current Conveyor block is configured as current follower (CF) providing a low-impedance, virtual-ground node for the sensor current to be driven into. Subsequently our novel Sinh amplifier circuit is used to provide 60dBs (1000x) gain. This level of gain has been confirmed both by simulations and measurements.

The Sinh Current Amplifier has been designed, analyzed, simulated, fabricated and tested. It consists of two parts: initially the input current is transformed (via a bias current I_0) from I_{in} to a voltage $V_x \approx \sinh^{-1} \frac{I_{in}}{I_0}$. Subsequently the second part performs a voltage- V_x -to-a-current (via a current bias I_1) expansion of the form: $I_{out} = I_1 \sinh(V_x)$. This compression and expansion method results in an input-to-output current gain of $\frac{I_1}{I_0}$. The sinh current amplifier circuit is an externally linear internally-non-linear (ELIN) weak inversion, low power, high gain, current amplifier circuit. The circuit was analyzed, verified and simulated in the Cadence IC Design Framework with the commercially available AMS $0.8\mu\text{m}$ and $0.35\mu\text{m}$ CMOS processes. Subsequently the design was laid out (consuming an area of $1300\mu\text{m} \times 1200\mu\text{m}$) and fabricated providing practical measured results which have confirmed the function of the proposed Sinh Current Amplifier.

Table 7.1 summarizes the measured performance of the $0.8\mu\text{m}$ and $0.35\mu\text{m}$ designs.

From table 7.1, it is clear that the $0.35\mu\text{m}$ process offers better results in terms of 3dB bandwidth, while the $0.8\mu\text{m}$ offers lower power consumption.

The Sinh Current Amplifier has the potential to replace op-amp-based current amplification solutions. The Sinh Current Amplifier is characterized by reduced power supply levels, generally lower power consumption and the fact that it can operate open-loop and provide current amplification in a resistorless manner. Together with a short-range radio it could provide lab-on-chip monitoring solutions. Furthermore its translates to a bipolar design with the potential of higher speed operation is diverse.

Gain	x10	x100	x1000	x100
Process	0.8 μ m AMS			0.35 μ m AMS
Power Supply	± 4 V	± 4 V	± 4 V	± 4 V
Power Consumption	0.88 μ W	4 μ W	44 μ W	95 μ W
Size	1300 μ x 1200 μ m			1500 μ x 900 μ m
3dB Point	160Hz			400Hz
Input referred noise integrated over a bandwidth of 1KHz	2pA			2pA
Current Range value for which deviations from nominal gain are below 1%	100p-6n	100p-2.5n	100p-2.5n	3n-16n

TABLE 7.1: Sinh Current Amplifier Specifications

It should be stressed that though the Sinh Current Amplifier operates off ± 4 V, it is possible to reduce the power supply while maintaining the 60dB of current gain. This would be achieved by cascading three amplifiers side by side with a gain of 10 each. In this case the trade-off will be reducing the power supply by increasing the size. By cascading the amplifiers, the power supply can be reduced by 40%.

Part III

Wireless Unit

Chapter 8

Introduction to Wireless Sensors

The novel current-mode-sinh-amplifier designed in the previous section is to be used in an incubator as shown in figure 8.1. The incubator is required to control the environment of the chemical reaction taking place. This control thereby allows engineers to completely monitor which external stimuli causes the cell culture to react down which path. By controlling the reaction and monitoring what the cell culture becomes a greater understanding may be achieved.



FIGURE 8.1: Incubator

Clearly the cell cultures must be completely isolated from any external elemental effects that are undesirable. With that in mind the incubator must be completely sealed for the

duration of the experiment in order to maintain a constant environment for the reaction in which to take place. The call for a wireless device arises.

The use of biosensors along side wireless devices is not a novel idea, however the method in which they are implemented is different in most cases. The desirability for low power in all cases defines certain design criteria, for example, in most cases it is the driving of the antenna that drains most battery power in transmitters. Therefore if only a short range transmission is needed then the power required is lower than if a higher range is wanted. Encoding is also another factor, many transmitter systems include encoding techniques to protect the data signal from being intercepted by 'hijackers'. However if the data signal is transmitter over a short range then, the 'hijackers' would be in immediate proximity to the wireless unit. These and other factors are present when designing wireless devices.

This chapter begins by introducing a literature review. Wireless standards are presented, from the commercial Bluetooth and Zigbee IEEE 802.15 'wireless personal area networks', to short range inductive link telemetry. Subsequently wireless sensors are reported.

8.1 Literature Review

One could identify three main routes for designing wireless units for the aforementioned application. The first is the mainstream route of using a commercially available wireless boards based around Bluetooth or Zigbee standards. The second relates to the sub-cm range design of Inductive Links. A third alternative would be an application specific design.

8.1.1 Bluetooth - Zigbee

Bluetooth's frequency ranges from 2.4GHz - 2.48GHz within the Industrial-Scientific-Medical (ISM) band. Due to the vast number of devices using this frequency range, Bluetooth employs frequency hopping techniques. This technique allows a number of devices to operate within the 2.4GHz ISM band without interference or cross talk. Frequency hopping techniques divide the frequency band into several hop channels. The channel is divided into a consecutive number of slots ($625\mu\text{s}$ wide), and a different

slot is used for each hop channel resulting in 1600 hops per second. Frequency Hopping dictates that the operating frequency of a device changes 1600 times a second. Therefore in the unlikely occurrence of two Bluetooth devices operating at the same frequency, that would only take place for 1600th of a second. Figure 8.2 illustrates an indicative two channel frequency hopping case. [86] [87]

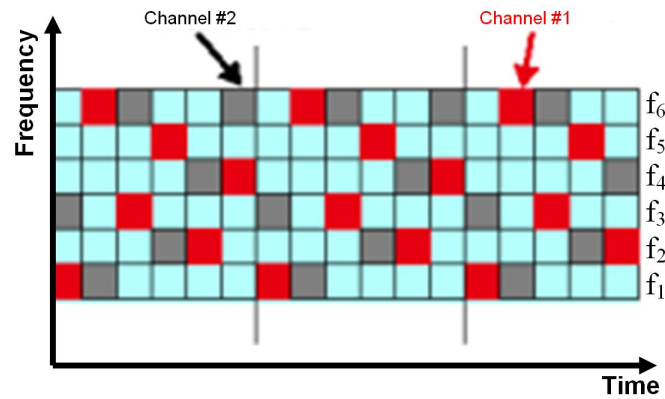


FIGURE 8.2: Indicative Two Channel Frequency Hopping case. Extracted from [86]

Considering the example of a cordless phone and its base station, the base station is known as the master, and the handset is known as the slave. Data needs to travel both ways, the master and slave cannot both transmit and receive data at the same time since that would lead to a clash. Due to this the master and slave take turns to transmit packets of data. When a master and slave 'talk', it is said to have formed a piconet. The hop sequence is said to be decided by the identity of the piconet master, as well as the phase of its clock. Each packet of data transmitted is preceded by an access code. This means that a device does not need to worry about processing a signal that has nothing to do with itself. The access code tends to be 72bits, followed by a 54bit header (which has the address of the slave as well as what type of data the payload is carrying), and then the payload that may vary from 0-2745bits. Bluetooth uses frequency shift keying (FSK) to transmit its data. [88] [89]

Figure 8.3 illustrates the commercially available Bluetooth Sensor Development Kit advertised by [90]. The Kit operates via two separate systems. The Transducer Interface Module (TIM) integrates the users' sensor with its' inbuilt Analog to Digital Converter and processes the signal for Bluetooth (IEEE 1451 compliant) transmission. This data are received by the Network Capable Application Processor (NCAP) unit which maybe up to 30 meters away. The NCAP then allows the data from the sensor to be processed by the PC and recorded.

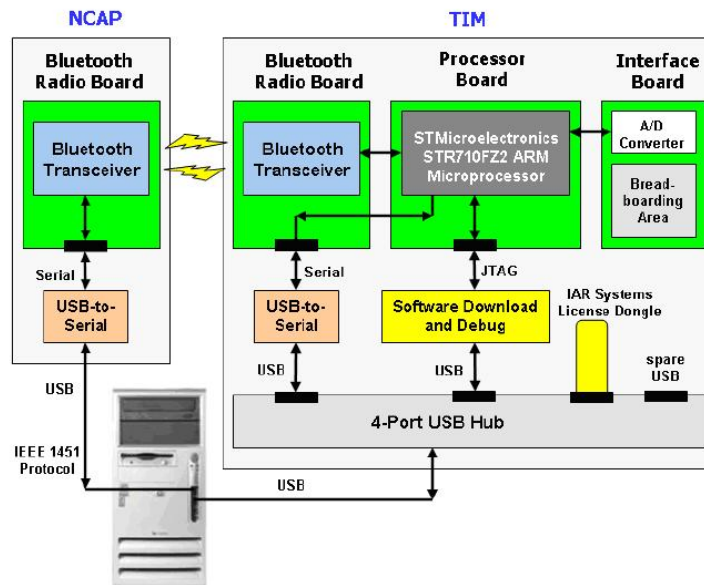


FIGURE 8.3: Bluetooth Sensor Development Kit. Extracted from [90]

ZigBee is similar to Bluetooth as far as transmission of data is concerned. The main difference is much lower bit rate. Whereas Bluetooth is known to transmit 750kbps, ZigBee transmits between 20 - 250kbps. This means that the engineer can trade off bandwidth for power. Both Zigbee and Bluetooth use similar circuit architectures for transmission, and both transmit and receive using analog radio sections, and then do the signal processing in the digital domain. [91]

8.1.2 Inductive Link Telemetry

For implantable devices, one of the major considerations is power consumption. Certain types of batteries cannot be used to power implantable devices as they would not be able to sustain the circuit for a sufficient amount of time. Therefore ideally any device within the body needs to be either wirelessly powered or have extremely low power dissipation so that the (rechargeable) battery last for years. The key device for wireless power transfer is the inductor. When two coils are brought into close proximity they become mutually magnetically coupled. Should two coils (A and B) be placed in close proximity to one another, and an AC current flows through A, for example then due to the current in A, a changing magnetic field is created which due to proximity changes the magnetic flux through coil B and induces a current to it. Hence it is Faraday's Law which allows the wireless powering of an implanted circuit from an externally driven coil. Conversely the induction of voltage can be used to transmit the data from the

sensor back out to the external device. When the same antenna is used, space can be saved on the chip [93]. Figure 8.4 depicts the intuitive circuit model of an inductively coupled transmitter receiver system. Values of the inductor and capacitor are chosen to provide the desired frequency of operation. L_t is assumed to be an ideal inductor while R_t is a summation of the losses encompassed within the transmitter circuit. Conversely R_r is a representation of the losses within the receiver. The transmitter circuit is excited by a V_t voltage source, while the voltage across C_r is denoted as V_r .

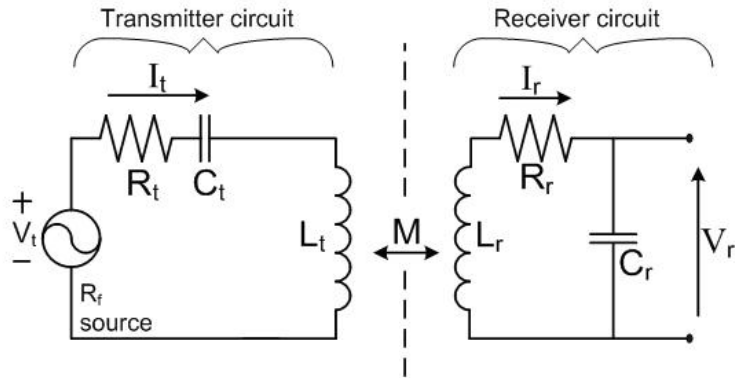


FIGURE 8.4: Circuit Representation of an Inductive Link. Extracted from [93]

In this example, power is transmitted for wireless neural stimulation. Table 8.1 illustrates the efficiency and ability for this type of wireless powering where table 8.2 specifies the conditions of case 1-5.

TABLE 8.1: Cases for table 8.2

	Transmitter Coil	Receiver
Case 1:	90mm	1.5mm
Case 2:	90mm	1.5mm with ferrite core
Case 3:	320mm	2mm
Case 4:	140mm	0.4mm
Case 5:	140mm	0.4mm with ferrite core

An initial part in the ‘inductive link’ design has to do with the power transfer efficiency (η) of the link. The efficiency is important as it gives an indication of the induced voltage to the secondary (implanted/receiver) coil. From table 8.1 [93] it can be seen that the efficiency depends upon certain parameters. The first is the ratio of the size of the sensor/implanted coil to the driving external coil (transmitter). The second is the number of turns and the thickness of the wires. Since in general the whole requirement for an implanted system is to be small, factors like the number of turns in the coils, the diameter of the coil and the diameter of the wire itself can affect sizes. [94]

TABLE 8.2: Summary of the Power Supply Characteristics for Five Cases of Transmitter and Receiver Coils. Where X_{cr} receiver capacitor reactance, M = mutual inductance, P = Power of the transmitter source signal and $R_{eq} = X_{cr}^*$ Receiver's coil's Q. . Extracted from [93]

Case	Transmitter				Receiver					Power Supply		
	freq (MHz)	diameter (mm)	turns	L (μ H)	diameter (mm)	length (mm)	L (μ H)	X_{cr} (ohm)	M (nH)	Vr / Vt	Req (k ohm)	power (mW)
1a	2	90	14	40	1.5	3	2.17	27	21	0.83	1.1	7.9
1b	20	90	5	4	1.5	3	2.17	270	7.4	3	11	10
2a	2	90	14	40	1.5	3	10.85	135	104	4.1	54	39
2b	20	90	5	4	1.5	3	10.85	1350	37	14.8	5.4	50
3a	2	320	8	40	2	3	3.64	45	8	0.3	1.8	0.7
3b	20	320	3	4	2	3	3.64	450	3	1.2	18	0.9
4a	2	140	11	40	0.4	3	0.178	2.24	0.54	0.02	0.09	0.06
4b	20	140	4	4	0.4	3	0.178	22.4	0.2	0.08	0.9	0.09
5a	2	140	11	40	0.4	3	0.89	11.2	2.7	0.11	0.45	0.32
5b	20	140	4	4	0.4	3	0.89	112	1	0.41	4.5	0.46

Another significant factor affecting the link efficiency is the orientation of the coils to one another. Figure 8.5 illustrates indicative types of alignment. Any mis-alignment causes the efficiency to drop. When the coil (mis-)alignment changes, the induced voltage will also vary. [95]

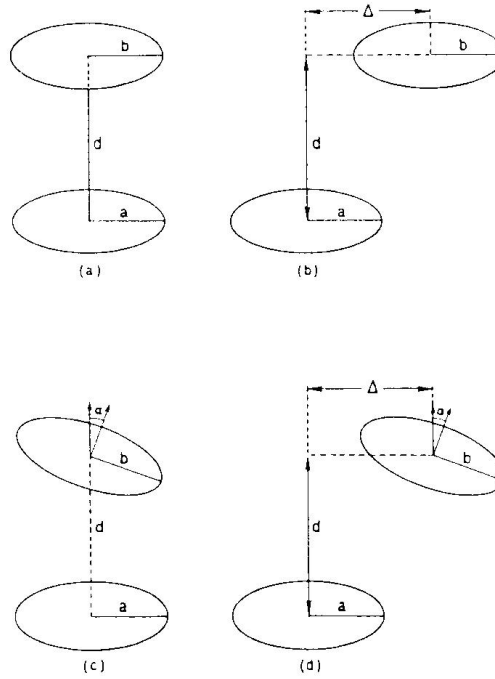


FIGURE 8.5: Coil Alignments, (a) Ideal alignment, (b) Lateral alignment, (c) Angular misalignment, (d) General misalignment. Extracted from [95]

Figure 8.4 may also be considered as a transmission method known as ‘Load Shift Keying’ (LSK). LSK technique can be explained by means of figure 8.6. The internal circuit’s resonant frequency is changed by modulating the load resistance. Changing this load will then affect the mutual inductance (M) between the two antennas which in turn leads to a change in the voltage drop across the external transmitter (V_{L1}). [96]

Looking at the impedance (Z_1) of the external circuit:

$$Z_1 = \frac{V_1}{I_1} = R_1 + Z_r + j \left[\omega L_1 - \left(\frac{1}{\omega C_1} \right) \right] \quad (8.1)$$

where ω denotes the chosen frequency of operation. The impedance (Z_2) of the secondary coil is

$$Z_2 = \frac{V_2}{I_2} = j\omega L_2 + \frac{1}{\frac{1}{R_2} + j\omega C_2} \quad (8.2)$$

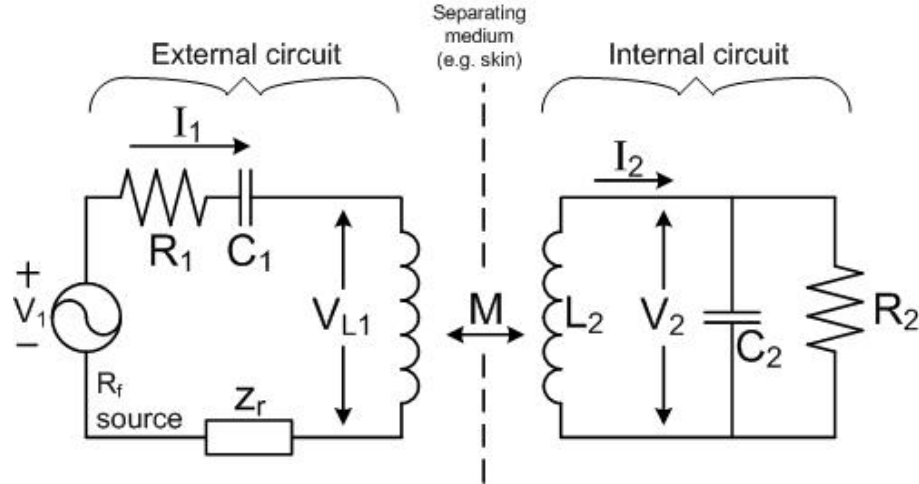


FIGURE 8.6: Schematic for the explanation of the Load Shift Keying Technique. Extracted from [96]

$$Z_2 = \frac{R_2}{1 + \omega R_2^2 C_2^2} + j \left(\omega L_2 - \frac{\omega C_2 R_2^2}{1 + \omega R_2^2 C_2^2} \right) \quad (8.3)$$

Both the primary and secondary circuits operate at the resonant frequency so that Z_1 and Z_2 are purely resistive.

$$0 = j \left(\omega L_2 - \frac{\omega C_2 R_2^2}{1 + \omega R_2^2 C_2^2} \right) \quad (8.4)$$

$$\frac{L_2}{C_2 R_2^2} = \frac{1}{1 + \omega R_2^2 C_2^2} \quad (8.5)$$

Hence, Z_2 becomes:

$$Z_2 = \frac{R_2}{1 + \omega^2 C_2^2 R_2^2} = \frac{L_2}{R_2 C_2} \quad (8.6)$$

The mutual inductance is given as:

$$M = k \sqrt{L_1 L_2} \quad (8.7)$$

Where k denotes the coupling coefficient

Z_r is the reflected impedance appearing as part of the total impedance of the primary coil. Thereby, Z_r is given as,

$$Z_r = \frac{(\omega M)^2}{Z_2} \quad (8.8)$$

It can be shown (8.2) that the voltage V_{L1} across the primary coil is given by:

$$V_{L1} = \frac{V_1}{\omega C_1(R_1 + \omega^2 k^2 L_1 C_2 R_2)} \quad (8.9)$$

From equation 8.9, it is apparent that the voltage across the transmitting antenna (L_1) depends on the load R_2 of the implant circuit. Hence a change in the load value changes the amplitude of the transmitter. This method is highly dependent on the mutual inductance between the two coils: size, power, distance and orientation all play a role. Distance is the major issue in this case. The problem with the distance is that if the antennas are too far apart, the induced voltage will not be enough to power the implant circuit. Circuits utilizing this method tend to operate under a 1cm in range. [96]

Figure 8.7 shows a wireless capacitive sensor utilizing the load-shift-keying method for data transmission from the implanted unit to the external monitoring system. A frequency generator is used to drive the external antenna which then transmits that signal to the implanted circuit. The implant receives the signal and converts it to a DC level. This is used to power the sensor itself. Data from the sensor drive the transistor M_{tx} , whose function is to modulate the load resistance of the implant which according to, from equation 8.9 cause a change in the amplitude of the signal at the external circuit. This modulation is subsequently detected by the external circuit.

8.1.3 Application Specific Radio Design

Due to the lack of specific radio systems available for low-power, low-range transmission, that are small, many engineers design their own that are specific to their parameters and their application. One such device is the ‘Laboratory-in-a-Pill’ which was designed by engineers at the University of Glasgow. Data are collected by pH and temperature sensors and processed (digitized and encoded) by 20mm² ASIC. The signal is then passed on to a transmitter which sends the data to an awaiting base station where sensor

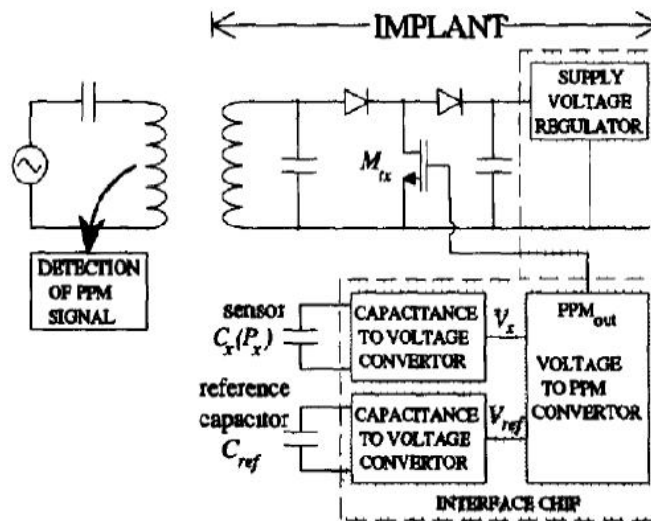


FIGURE 8.7: Capacitive Wireless Load-Shift-Keying Sensor System. Extracted from [97]

data are decoded and displayed on a laptop. The general circuit architecture is described by figure 8.8. [98]

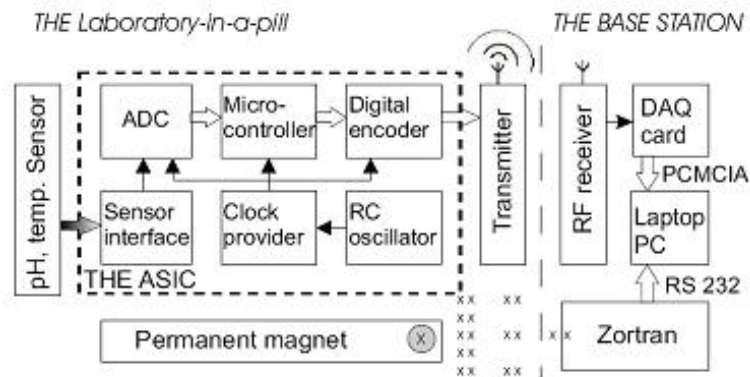


FIGURE 8.8: Laboratory-in-a-pill Device. Extracted from [98]

Figure 8.9 illustrates another example of a wireless device designed at the University of Michigan. The simplicity of the design is that data from each sensor are digitized and passed to the transmitter. The transmitter operates when its input is at logic 1, and switches off when the input is at logic 0. The oscillator section is based around a Colpitts Oscillator with the carrier switched on and off. The drain inductor required for the oscillations also acts as the transmitting antenna. L_t is 115nH, the transmitting frequency is 315MHz operating off a 3V battery at 200 μ A, however, the transmitter section is located completely off-chip and implemented by means of passive components making it bulky. [99]

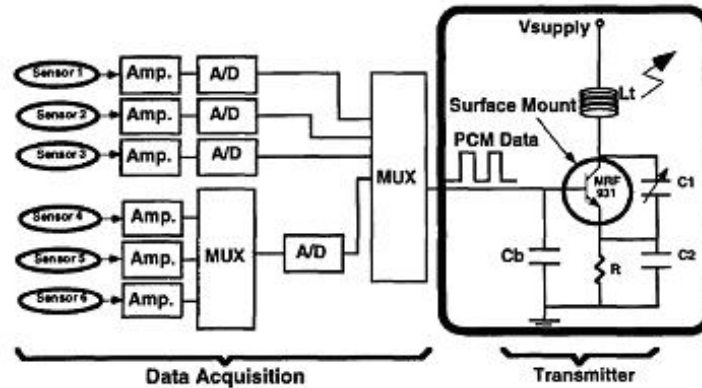


FIGURE 8.9: Biotelemetry Microsystem for Measuring Multiple Physiological Parameters: Extracted from [99]

8.2 ISM Bands

A crucial factor that must be considered when designing radio systems is the frequency of transmission. The frequency controls a number of specifications of the system, if too low the data rate will be limited, if too high then the power dissipation will be significantly higher. The choice of frequency is not an arbitrary one since in general the spectrum is government-regulated. However there are banks of free bands for those looking into amateur radios and other wireless testing applications. Table 8.3 shows the bank of ISM bands. [100]

TABLE 8.3: Frequency ranges used for ISM-systems

Frequency Range	Comment	Allowed Field strength Transmission Power
135 kHz	low frequency, inductive coupling	72 dB μ A/m
6.765 .. 6.795 MHz	medium frequency (ISM), inductive coupling	42 dB μ A/m
7.400 .. 8.800 MHz	medium frequency, used for EAS (electronic article surveillance) only	9 dB μ A/m
13.553 .. 13.567 MHz	medium frequency (13.56 MHz, ISM)	42 dB μ A/m
26.957 .. 27.283 MHz	inductive coupling, contactless smartcards	42 dB μ A/m
433 MHz	medium frequency (ISM), inductive coupling	10 .. 100 mW
868 .. 870 MHz	UHF (ISM), backscatter coupling	500 mW, Europe only
902 .. 928 MHz	UHF (SRD), backscatter coupling	4 W - spread spectrum, USA/Canada only
2.400 .. 2.483 GHz	SHF (ISM), backscatter coupling	4W-spread Spec-USA/Canada, 500mW-Europe
5.725 .. 5.875 GHz	SHF (ISM), backscatter coupling	4W USA/Canada, 500 mW Europe

Clearly if the frequency is one of the lower bands, then the data rate may be limited. Also if the frequency is low then the transmission range will also be low. On the other hand the frequency of transmission is too high, then the power consumption of the circuit increases.

8.3 Conclusion

The design of smart sensors has been introduced in this chapter. A smart sensors is a wireless sensor. The three choices available when designing smart sensors are, 1) to buy an off-the-shelf device, which usually tend to utilize Bluetooth or Zigbee standards thereby being large power consuming circuits. 2) Use a very short range wireless link that requires the wireless transfer of power. However the transmission distance of these devices tend to be sub-cm, and require perfect orientation of their antenna. Therefore this tends to be unusable, 3) to design an application specific wireless link for the purpose in mind. Previously designed versions are either bulky or require high battery drain, thereby needing one specific for the system in mind.

Chapter 9

Transmitter

9.1 PLL Based Radio

A wireless unit is required for data transfer from a sensor interface circuit placed within an incubator to some external unit that will connect to a PC which may interpret the results. As the monitored chemical reactions are generally slow (hours, days even weeks), the data rate will also in general be low. In the incubator, the transmitting antenna can be situated close to the inside wall. On the outside, the receiver antenna may also be placed on the incubator wall. By reducing the transmitting distance, the power consumption may also be reduced. However in reality the transmitting and the receiving antenna might not be perfectly aligned. The wireless device should be able to deal with small variations of antennae positioning. Clearly if the radio circuits are small, then they can be manufactured on the same die as the Sinh Current Amplifier designed in chapter 5 thus keeping the design simple.

9.1.1 Types of Transmission

Simple wireless transmission comes in three modes, ASK, PSK and FSK (figure 9.1).

Amplitude Shift Keying (ASK) represents changes in amplitude as different input logic levels. However this may be problematic should there be any movement in the antenna, or if the received signal is weak. Phase Shift Keying (PSK) uses changes in phase to represent data in the format of logic 1's and logic 0's. The design of radio systems which uses the method of transmission requires that each path within the circuit have their

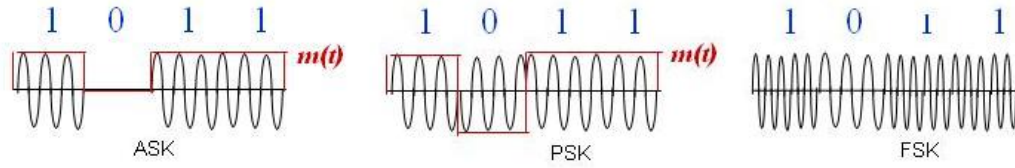


FIGURE 9.1: ASK, PSK and FSK

delay's minimized. Frequency Shift Keying (FSK), states that a change in frequency represents logic 1 and 0.

9.1.2 Proposed Radio Design

A VCO is a voltage controlled oscillator, that is, the input voltage - which in our case will ultimately be the data coming from the Sinh current amplifier - controls the output frequency. When those data are transmitted and the reverse is performed by the receiver, then a wireless unit is designed. The transmitter converts a logic 1 or 0 to a high or a low frequency, while the receiver converts - by means of a Phase Locked Loop (PLL) - those frequencies to logic 1's and 0's respectively. The block diagram of this simple radio is shown in figure 9.2.

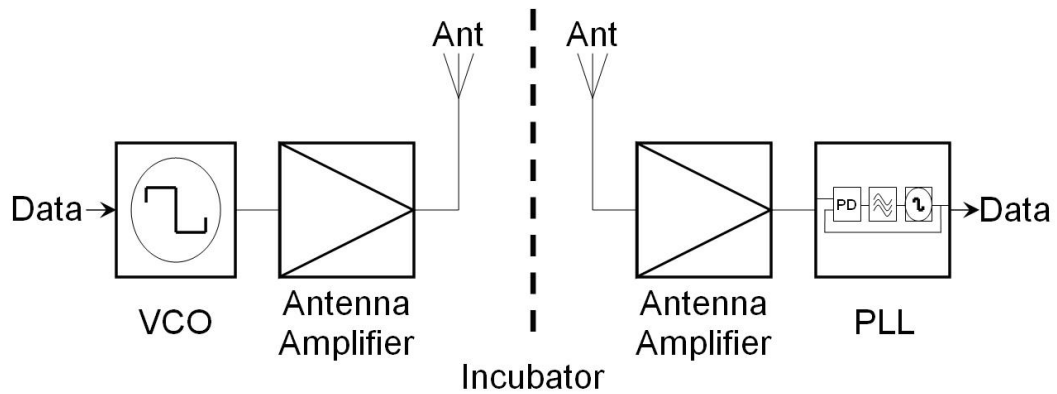


FIGURE 9.2: The proposed simple radio: VCO transmitter, PLL receiver. Extracted from [101]

The PLL works by having an identical VCO to that within the transmitter (VCO_{tran}). The PLL makes the output frequency of its VCO (VCO_{rec}) equal to that of VCO_{tran} . By making the two outputs the same and the two VCO's being of the same 'model', then their inputs must match. The data being fed into VCO_{tran} is recreated at VCO_{rec} .

In what follows a simple wireless unit, along the lines explained above, for the transmission of data from the Sinh Current Amplifier is to be elaborated. In our case the

optimal method of data transmission is FSK, utilizing different frequencies to represent logic 1's and 0's allows for the VCO to be used as the transmitter. Within the receiver, a Phase Locked Loop is used to decode the transmitted signal.

9.2 Oscillators

The heart of the transmitter is essentially the oscillator itself. There are many options in choosing the oscillator, however prior to its design, the frequency of operation should be stated. When choosing the frequency table 8.3 is imperative. Frequencies higher than 20MHz are used by amateur radio enthusiast, walkie-talkie, GSM or other powerful wireless devices. On the other hand, lower frequencies are difficult to design for as they require larger component sizes. Therefore the operation frequency that the wireless device is to be designed for was chosen to be the 13.553-13.567MHz range.

The call for wireless devices and circuits, has lead to a greater need for oscillators and clocks. In an attempt to match the demand for smaller and faster oscillators more and more groups are interested in researching this area of analogue design. The most commonly used harmonic oscillators are those which use resonant LC tanks - LC oscillators. Their popularity arises due to the simplicity of their design and implementations. However the LC oscillators suffer in size as the physical dimensions of the inductor tends to be far greater than any active on-chip device. The performance of the LC oscillator is also attributed to the quality factor Q of both the inductor and the capacitor. Whereas previously, small and high Q inductors were difficult to fabricate on-chip, recent advance in the research of monolithic IC's have allowed these obstacles to be overcome. [102] [103]

Inductor - Capacitor oscillators consist of three parts (figure 9.3). Firstly an amplifier to re-enforce the oscillation swings, secondly an LC tank which stores and discharges energy from the inductor and capacitor and finally an output feedback branch to the input of the amplifier which helps overcome the effect of damping caused by the LC tank.

9.2.1 LC Oscillator

A typical LC oscillator is shown in figure 9.4.

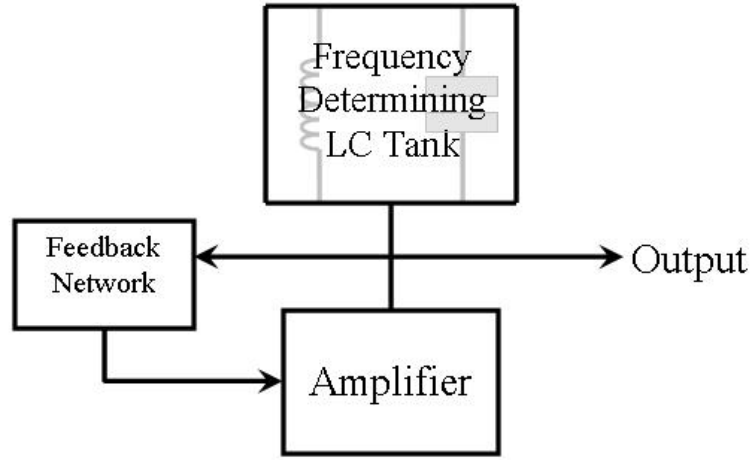
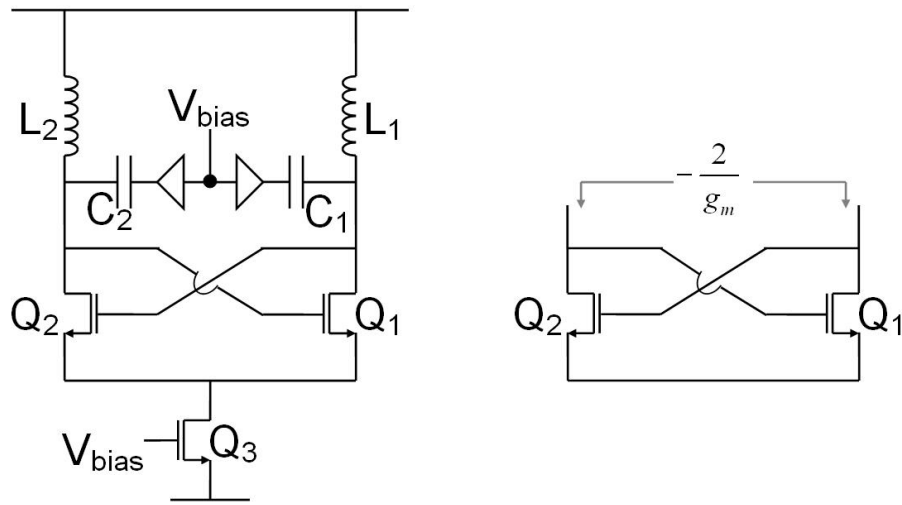


FIGURE 9.3: LC oscillator Basic diagram. Extracted from [102]

FIGURE 9.4: (a) Typical Differential LC oscillator, (b) Negative impedance $\left(-\frac{2}{g_m}\right)$ of cross coupled pairs. Extracted from [102]

It operates based on the principle that the LC tank creates a resonant frequency. Consider an impulse response (figure 9.5b) applied to the inductor L_1 , the LC tank would cause a damped ringing response whose frequency is dictated by equation 9.1 (illustrated by figure 9.5c). Under normal conditions this ringing would dampen. However due to the operation of the cross coupled Q_1 and Q_2 the ringing (oscillations) increase in amplitude until they swing between the power supply rails [104]. Hence Q_1 and Q_2 alternate between the on and off state. [105]

$$freq = \frac{1}{2\pi\sqrt{LC}} \quad (9.1)$$

The frequency of oscillation of the LC oscillator is determined by the inductor and

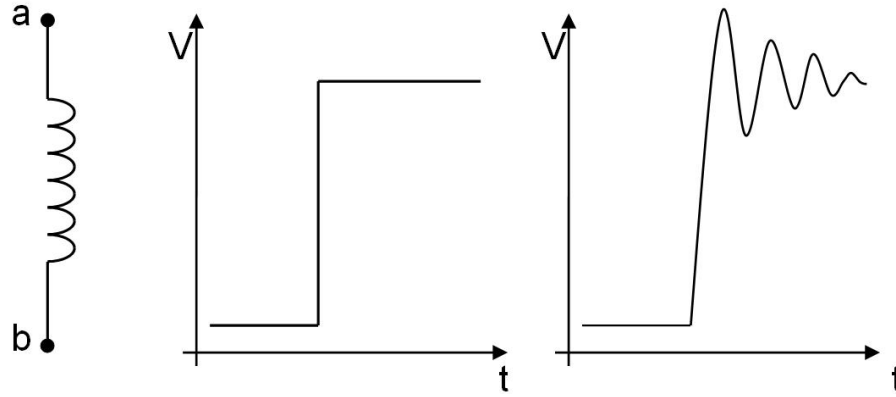


FIGURE 9.5: (a) Inductor, (b) Impulse response applied to an inductor, (c) ringing response of the inductor.

capacitor along both branches of the circuit illustrated in figure 9.4. Due to the cross coupling effect of M_1 and M_2 a negative impedance of $-\frac{1}{g_m}$ occur at each of the drain terminals of the transistors.

9.2.2 Colpitts Oscillator

Combining a resonator with an active component is also the way to create a Colpitts oscillator. It uses a resonator composed of capacitors with positive feedback provided by the MOS transistor for oscillations to occur. Figure 9.6 shows the configuration of a typical Colpitts circuit. The frequency of oscillation is decided by the sizing of the capacitors and inductors and given in equation 9.2. [106]

$$freq = \frac{1}{2\pi \sqrt{L \left(\frac{C_1 C_2}{C_1 + C_2} \right)}} \quad (9.2)$$

Note how the capacitively coupled Colpitts oscillator takes the feedback (referring figure 9.3) from between C_1 and C_2 in figure 9.6.

Consider that the circuit in figure 9.4 is implemented, a capacitor size of 10pF, and an inductor of 10 μ H yields an output frequency of 16MHz. Generally speaking a 10 μ H inductor is a bulky component susceptible to noise.

The Colpitts oscillator can achieve high voltage swings compared to its cross coupled counterpart, however the Colpitts is unlikely to be used on chip as it is highly susceptible to common mode noise (substrate and supply). Also in order to obtain the desired

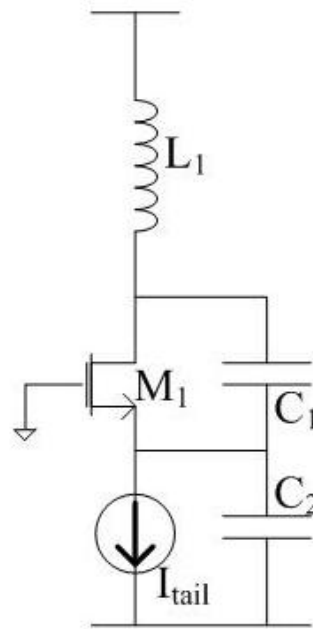


FIGURE 9.6: Typical Colpitts Oscillator. Extracted from [106]

frequency output exact capacitor and inductor dimensions are required. Therefore structures using inductors are challenging. [107]

9.3 Ring Oscillator

Ring oscillators are invaluable circuit blocks in today's electronic world. Many digital chips require clock signals to perform their functions. From switched-capacitor circuits to ADCs, digital clock signals are required. The simplest way to construct this is by means of a ring oscillator. A ring oscillator is based on an inverter chain with an odd number of stages (if it were an even number of stages, the output would be the same as the input).

9.3.1 Ring Oscillator Analysis

The ring oscillator can take on a number of different structures, from a differential ended, to a current-based design. Figure 9.7 shows a basic inverter structure. Here the operation is simple: when the input is low, the NMOS turns off, and the PMOS turns on, giving the output a path to the positive power supply rail. When the input is high, the NMOS turns on, and the PMOS turns off, giving the output a path to the lower

supply rail. When the input switches the output becomes high. From this, it should be clear that the time that the output stays ON is determined by the size of the capacitor and the amount of current drawn (size of the transistor).

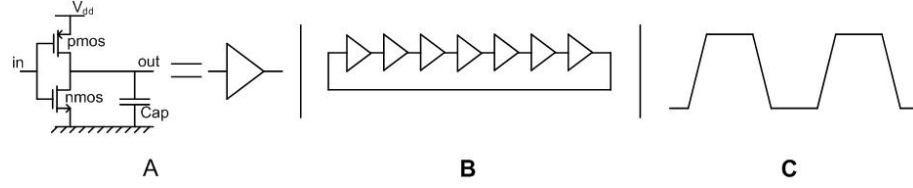


FIGURE 9.7: (A) a basic inverter, (B) an example of a seven-stage ring oscillator, (C) typical output waveform from a ring oscillator

The frequency of oscillation depends on the rise and fall time as well as the ON and OFF time of the transient wave (figure 9.7). Initially looking at the fall time, that is the time for the output to fall from a logic one to a logic zero. Figure 9.8 shows that t_{fall} is the time for the output to fall from $0.9V_{dd}$ to $0.1V_{dd}$ (The reason that it is not between V_{dd} and zero, is to take into account noise that may affect the operation).

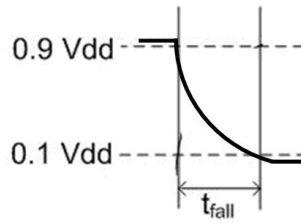


FIGURE 9.8: A definition of t_{fall} . Extracted from [112]

The time interval t_{fall} may also be defined as the time needed for the capacitor (in figure 9.7a) to discharge through the NMOS to ground. When this happens, the NMOS transistor will cross two different regions of operations. In the initial phase, the time taken for the voltage in figure 9.8 to fall from $0.9V_{dd}$ to $(V_{dd} - V_{tn})$, the quadratic equation for the saturation region holds. In the second phase, while the voltage is between $(V_{dd} - V_{tn})$ to $0.1V_{dd}$, the transistor is within the triode region. [108] [109]

There are two phases:

1. During phase (1) the differential equation governing V_{out} of the inverter stage depicted in figure 9.7a is given by:

$$C \frac{dV_{out}}{dt} + \frac{\mu_n C_{ox}}{2} \left(\frac{W}{L} \right) (V_{dd} - V_{tn})^2 = 0 \quad (9.3)$$

We have to solve for $V_{out}(t)$ in general and then calculate t_{fall_1} which corresponds to V_{out} falling from $0.9V_{dd}$ to $V_{dd} - V_{tn}$.

2. During phase (2) the differential equation governing V_{out} is given by:

$$C \frac{dV_{out}}{dt} + \mu_n C_{ox} \left(\frac{W}{L} \right) \left[(V_{dd} - V_{tn})V_{out} - \frac{V_{out}^2}{2} \right] = 0 \quad (9.4)$$

Again we have to solve for $V_{out}(t)$, and then calculate t_{fall_2} which corresponds to V_{out} falling from $V_{dd} - V_{tn}$ to $0.1V_{dd}$.

Phase 1. It holds:

Re-arranging 9.3 leads to,

$$dt = \frac{CdV_{out}}{\frac{1}{2}\mu_n C_{ox} \frac{W}{L} [(V_{dd} - V_{tn})^2]} \quad (9.5)$$

Where 9.5 represents the time taken for the voltage at the output node of that specific inverter to fall from $0.9V_{dd}$ to $V_{dd} - V_{tn}$, hence 9.5 maybe expressed as,

$$t_{fall_1} = \frac{C(0.9V_{dd} - (V_{dd} - V_{tn}))}{\frac{1}{2}\mu_n C_{ox} \frac{W}{L} [(V_{dd} - V_{tn})^2]} \quad (9.6)$$

Phase 2. It holds:

Re-arranging 9.4 leads to,

$$dt = \frac{CdV_{out}}{\mu_n C_{ox} \left(\frac{W}{L} \right) \left[(V_{dd} - V_{tn})V_{out} - \frac{V_{out}^2}{2} \right]} = 0 \quad (9.7)$$

Where 9.7 represents the time taken for the voltage at the output node of that specific inverter to fall from $V_{dd} - V_{tn}$ to $0.1V_{dd}$, hence 9.7 maybe expressed as,

$$t_{fall_2} = \frac{C(V_{dd} - V_{tn} - 0.1V_{dd})}{\mu_n C_{ox} \left(\frac{W}{L} \right) \left[(V_{dd} - V_{tn})V_{out} - \frac{V_{out}^2}{2} \right]} = 0 \quad (9.8)$$

Combining phase 1 and phase 2, then allows the total fall time to be measured.

$$t_{fall} = t_{fall1} + t_{fall2} \quad (9.9)$$

Substituting equation 9.6 and 9.8 into 9.9 and rearranging leads to 9.10

$$t_{fall1} + t_{fall2} = \frac{C}{\mu_n C_{ox} \frac{W}{L}} \left[\frac{(0.1V_{dd} + V_{tn}) \left[(V_{dd} - V_{tn})V_{out} - \frac{V_{out}^2}{2} \right] + \frac{1}{2} \left[(0.9V_{dd} - V_{tn}) \left[(V_{dd} - V_{tn})^2 \right] \right]}{\frac{1}{2}(V_{dd} - V_{tn})^2 \left[(V_{dd} - V_{tn}) - \frac{V_{out}^2}{2} \right]} \right] \quad (9.10)$$

Assuming that the threshold voltage is approximately half of the power supply ($V_{tn} \approx \frac{1}{2}V_{dd}$)

Then, equation 9.10 may be re-written as,

$$t_{fall1} + t_{fall2} \approx \frac{C}{\mu_n C_{ox} \frac{W}{L}} \left[\frac{(0.9V_{dd}) \left[\frac{1}{2}V_{dd}V_{out} - \frac{V_{out}^2}{2} \right] + \frac{1}{2} \left[\left(\frac{V_{dd}}{2} \right)^3 \right]}{\frac{1}{2} \left(\frac{1}{2}V_{dd} \right)^2 \left[(V_{dd} - V_{tn}) - \frac{V_{out}^2}{2} \right]} \right] \quad (9.11)$$

Assuming then, that the power supply (V_{dd}) is less than or equal to 2V, then the term $\frac{1}{2} \left(\frac{1}{2}V_{dd} \right)^3$ becomes negligible, hence reducing 9.11, leaves, [110] [111], [112]

$$t_{fall_{total}} \approx (3 \rightarrow 4) \frac{C}{\mu_n C_{ox} \frac{W}{L} V_{dd}} \quad (9.12)$$

Using a similar method, the rise time of the inverter depicted within figure 9.7 maybe expressed as [110] [111] [112],

$$t_{rise_{total}} \approx (3 \rightarrow 4) \frac{C}{\mu_p C_{ox} \frac{W}{L} V_{dd}} \quad (9.13)$$

9.3.2 The Role of the Number of Stages of a Ring Oscillator

For a 3 stage ring oscillator the propagation of the signals will be as shown in figure 9.9(b). The signals appear as they propagate through the circuit. Figure 9.9(d) illustrates the case of a 5 stage ring oscillator. Comparing figure 9.9b with 9.9d it should be clear that an increase in the number of stages N will lead to a decrease of the oscillation frequency as it takes longer for the signal to go through one full period. Each ‘pass’ of the signal through one of the odd-numbered stages of the oscillator will contribute a characteristic time delay similar to the approximate values given in the previous section.

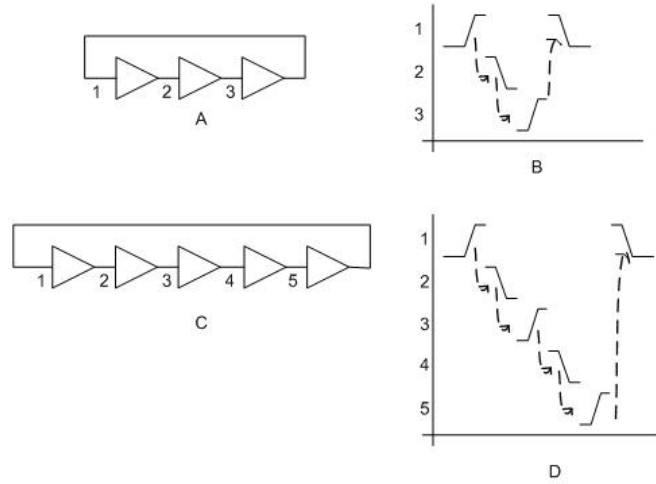


FIGURE 9.9: (a) 3 stage ring oscillator, (b) 'wave' propagation through circuit in a, (c) 5 stage ring oscillator, (d) 'wave' propagation through circuit in c.

The frequency of oscillation of the Ring Oscillator illustrated in figure 9.9 may be expressed as twice the inverse of the time delay through each inverter (as the signal must go through the ring twice to complete one period). If the delay through each inverter is given as τ , then

$$f_{osc} = \frac{1}{2N\tau} \quad (9.14)$$

With N denoting the total number of stages. [113] [114] [115]

More accurately, the average delay through an inverter may be expressed as $\tau = \left(\frac{t_{fall} + t_{rise}}{2}\right)$, so that, [116] [117] [118]

$$f_{osc} = \frac{1}{N(t_{fall} + t_{rise})} \quad (9.15)$$

This may be re-expressed as equation 9.16 when comparing 9.12 and 9.13 with equation 9.15,

$$f_{osc} = \frac{1}{N \left(\frac{4C}{\mu_n C_{OX} \frac{W}{L} V_{dd}} + \frac{4C}{\mu_p C_{OX} \frac{W}{L} V_{dd}} \right)} \quad (9.16)$$

At an initial glance, and bearing in mind the single stage topology of figure 9.7a it seems that the capacitor value C in 9.16 should correspond to the capacitor value of figure 9.7. However the parasitic capacitances of the NMOS and PMOS devices should be taken

into consideration. For a minimum sized transistor of the $0.8\mu\text{m}$ AMS process, the parasitic capacitance is estimated to be 4.5fF . An increase in the size of the transistor will increase the parasitic capacitance proportionally. For example,

For a $\frac{1.6\mu}{0.8\mu}$ (2 by 1) device $C_{par} = 7\text{fF}$,

For a $\frac{1.6\mu}{1.6\mu}$ (2 by 2) device $C_{par} = 9\text{fF}$,

Once the parasitics are taken into consideration, then the capacitor value C_{tot} at each stage of the RO would become: $C_{tot} = (\text{PMOS parasitic cap}) + (\text{NMOS parasitic cap}) + (\text{output capacitor})$

9.3.3 Example

As an example, if we consider a 5 stage RO built by inverter stages such as those illustrated in figure 9.10 then,

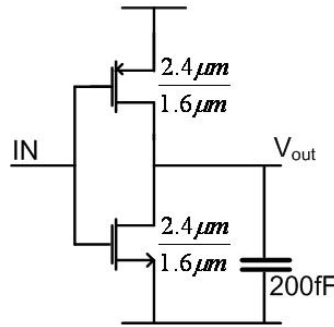


FIGURE 9.10: Inverter model, of a 5 stage ring oscillator.

The NMOS parasitics will be, $\frac{2.4\mu}{1.6\mu} = \frac{3W_{min}}{2L_{min}} = 3 \text{ by } 2 = 11.5\text{fF}$, and the PMOS parasitics will be $\frac{2.4\mu}{1.6\mu} = \frac{3W_{min}}{2L_{min}} = 3 \text{ by } 2 = 11.5\text{fF}$ and given that the output capacitor is set to 200fF , it will hold,

$$C_{tot} = 200\text{f} + 11.5\text{fF} + 11.5\text{fF} = 223\text{fF} \quad (9.17)$$

Leading to a frequency of oscillation of $f_{osc} = 7.8\text{MHz}$ when taken into consideration that for the $0.8\mu\text{m}$ AMS process $\mu_n C_{ox} \approx 28\mu\text{A}/\text{V}^2$ while $\mu_p C_{ox} \approx 137\mu\text{A}/\text{V}^2$. The value taken from the simulator is 7.2MHz (deviation close to 7% with respect to the simulated value).

If the number of stages fixed to 5, the power supply fixed to 2V, and the transistors are kept at a fixed size, then the f_{osc} is controlled only by the capacitance at each inverter stage. Figure 9.11 and 9.12 illustrated both the simulated and the approximate theoretical values of oscillation frequencies as a function of the capacitor value C. In general, the theoretically predicted results are close to the simulated ones.

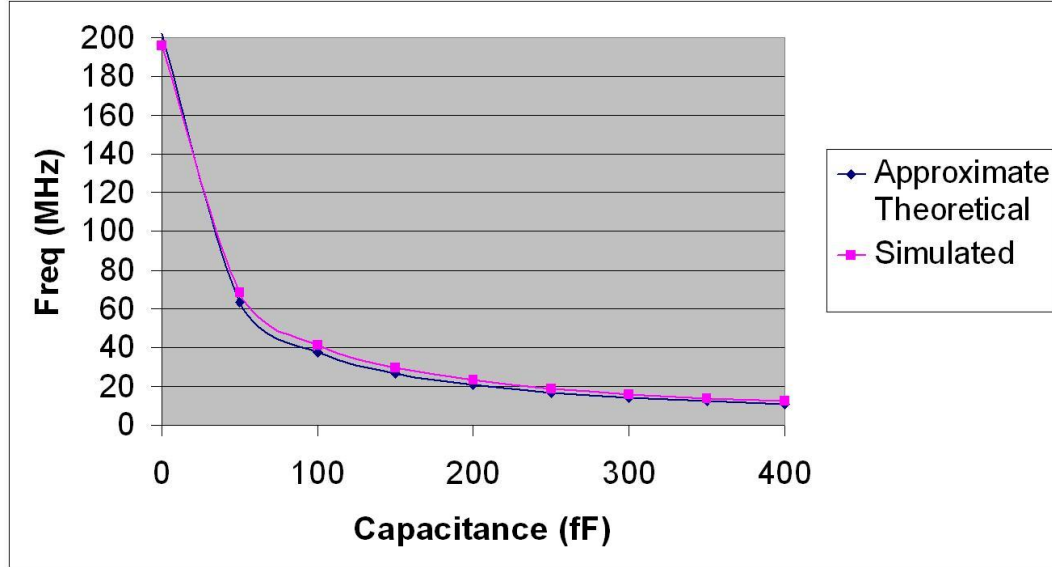


FIGURE 9.11: Capacitance controlled oscillation frequency: $N = 5$, $\frac{W}{L}_n = \frac{3.2\mu}{0.8\mu}$, $\frac{W}{L}_p = \frac{3.2\mu}{0.8\mu}$, square wave ring oscillator; frequency range: 202-11MHz

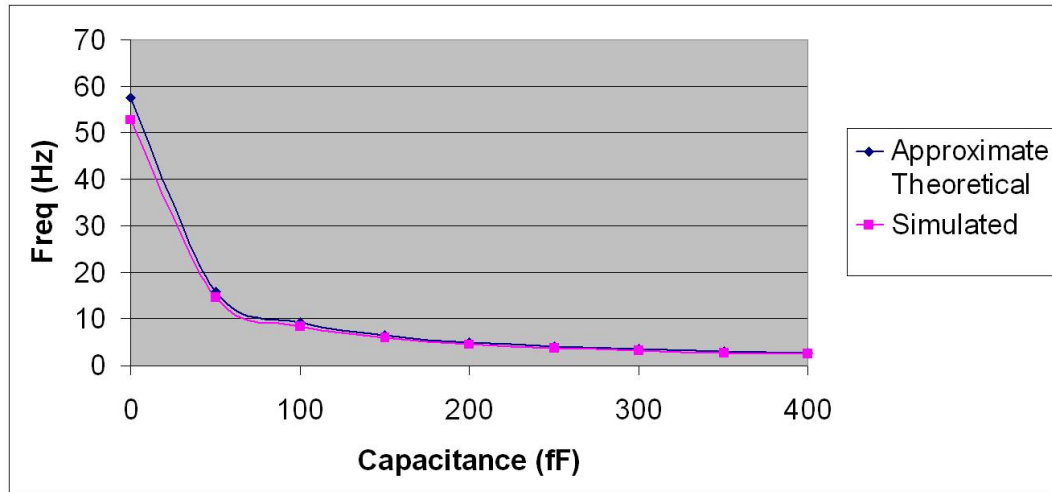


FIGURE 9.12: Capacitance controlled oscillation frequency: $N = 5$, $\frac{W}{L}_n = \frac{1.6\mu}{1.6\mu}$, $\frac{W}{L}_p = \frac{1.6\mu}{1.6\mu}$, square wave ring oscillator; frequency range: 60-2MHz

9.3.4 Variable MOS Capacitor

In order to transform a ring oscillator into a voltage controlled ring oscillator, one of the parameters in equation 9.16 must change with respect to applied voltage. As N , μ , C_{ox} , W and L are all fixed once the circuit has been fabricated, and V_{dd} may be shared, then the only viable option is to vary the capacitance with respect to voltage. In order to do this a variable controlled capacitor (varactor) is required.

Figure 9.13a illustrates the transistor-based configuration of a MOS varactor, while 9.13b illustrates its capacitive model.

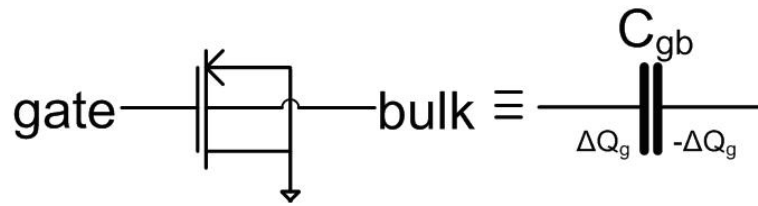


FIGURE 9.13: a) PMOS varactor, b) Capacitive equivalence

1. Initially assume that the gate voltage V_g is greatly positive.
 - The positive charge on the gate leads to a strong negative charge under the gate causing an excess of electrons below the gate (within the channel). This is known as Accumulation.
2. Decreasing V_g , (making it less positive)
 - As the charge on the gate becomes less positive, there is less of a negative charge under the gate, hence there are fewer electrons in the channel compared to the accumulation phase.
3. Continue to decrease V_g (till $V_{gb} = V_{fb}$)
 - Accumulation region completely disappears leaving the body neutral (known as the Flatband region)
4. Decreasing V_g to below V_{fb} (V_g moves towards 0v from a positive voltage)
 - The charge on the gate becomes less positive causing a repulsion of electrons which leaves positively charged ions under the gate (depletion region illustrated in figure 9.14).

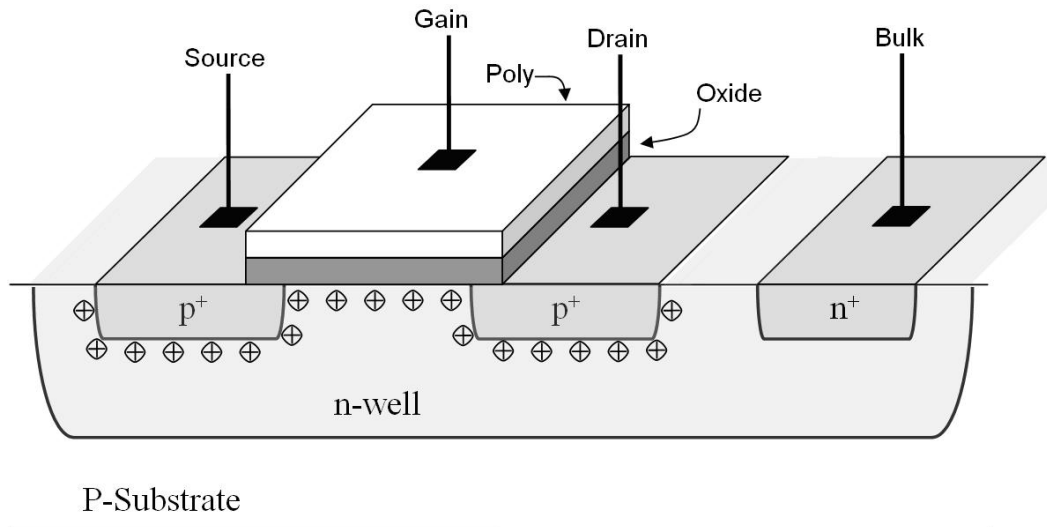


FIGURE 9.14: PMOS transistor in depletion mode. Extracted from [80]

5. Decreasing V_g further,

- The charge on the gate decreases, the depletion region becomes deeper and the negative charge on the gate causes a positive charge in the channel. (Inversion region illustrated in figure 9.15)

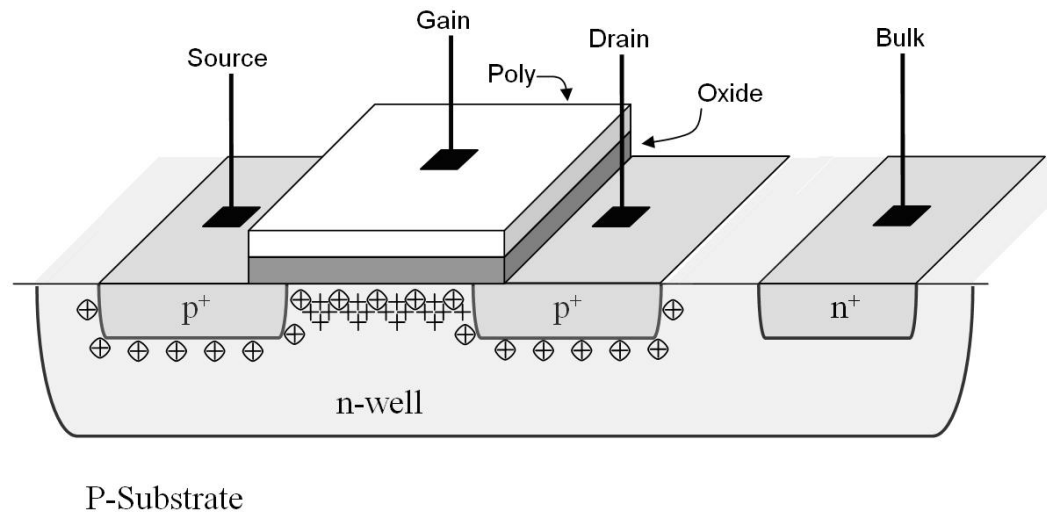


FIGURE 9.15: PMOS transistor in inversion mode. Extracted from [80]

Analyzing figure 9.13a, V_{gb} is the potential across the gate and bulk of the PMOS transistor. This may be considered as the combination of the potential across the oxide (ϕ_{ox}) and the potential across the substrate (ϕ_s). Therefore,

$$\delta V_{gb} = \delta \phi_{ox} + \delta \phi_s \quad (9.18)$$

As δQ_g is the charge at the gate, when the gate bulk voltage is present, C_{gb} may then be expressed as equation 9.19, and represented as figure 9.16,

$$\frac{1}{C_{gb}} = \frac{d\phi_{ox}}{dQ_g} + \frac{d\phi_s}{dQ_g} \quad (9.19)$$

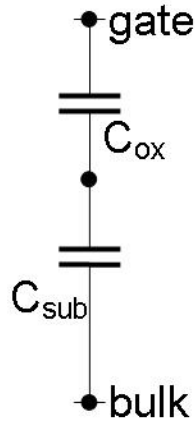


FIGURE 9.16: Gate-Bulk Capacitance Model [119]

Referring to figure 9.13b, $-\delta Q_g$ may be expressed as the charge applied to the substrate δQ_c , hence:

$$\frac{1}{C_{gb}} = \frac{1}{\frac{dQ_g}{d\phi_{ox}}} + \frac{1}{-\frac{dQ_c}{d\phi_s}} \quad (9.20)$$

Note that $\frac{dQ_g}{d\phi_{ox}}$ represents C_{ox} .

If the potential across the semiconductor is varied ($d\phi_s$), the charge within the semiconductor will vary (dQ_c). The excess charge required must enter the substrate through the bulk connection, therefore,

$$C_c = -\frac{dQ_c}{d\phi_s} \quad (9.21)$$

Hence equation 9.20 may now be re-written as,

$$\frac{1}{C_{gb}} = \frac{1}{C_{ox}} + \frac{1}{C_c} \quad (9.22)$$

Note that the inversion layer spreads in to the depletion region, defining the substrate capacitance as a parallel combination between the depletion and inversion region. Therefore, equation 9.22 becomes,

$$\frac{1}{C_{gb}} = \frac{1}{C_{ox}} + \frac{1}{C_{inv} + C_{dep}} \quad (9.23)$$

Equation 9.23 allows a graph of C_{gb} vs V_{gb} to be plotted. During the accumulation phase, ϕ_s is positive and there is an abundance of electrons in the channel which provide a direct path from the bulk connection to the channel side of the oxide. Hence C_{gb} is effectively only the oxide capacitance, C_{ox} . As V_{gb} decreases, the charge on the gate decreases causing the formation of a depletion region while the inversion layer has not yet formed, hence C_{gb} drops (equation 9.23). As V_{gb} decreases further still, the charge on the gate decreases to a point where holes are attracted into the channel. This creates the inversion layer, as the inversion layer gets stronger, C_{inv} denominates, the $1/(C_{inv} + C_{dep})$, thereby returning C_{gb} to C_{ox} .

Figure 9.17 illustrates the intuitive PMOS's gate bulk capacitance vs gate voltage for small and slow incremental variations of δV_{gb} . However, should the δV_{gb} be at a higher frequency, then the dotted line in figure 9.17 will represent the PMOS's gate bulk capacitance. The required charge within the substrate when V_{gb} is rapidly changing, is provided by the covering or uncovering of acceptor atoms at the bottom of the depletion region. The inversion layer cannot change fast enough as it is isolated between the oxide and the depletion region, therefore, the inversion layer is never fully formed.

Figure 9.18 illustrates capacitance vs gate bulk potential of a PMOS 15μ by 9μ m transistor simulated in Cadence using the 0.8μ m Design Kit.

Figure 9.19 illustrates the frequency vs DC input graph of a three stage voltage controlled ring oscillator.

Figure 9.20 illustrates the frequency vs capacitance of a three stage ring oscillator.

By comparing figure 9.19 and 9.20 provides a C_{gb} vs V_{gb} for the PMOS varactor illustrated inset in figure 9.21.

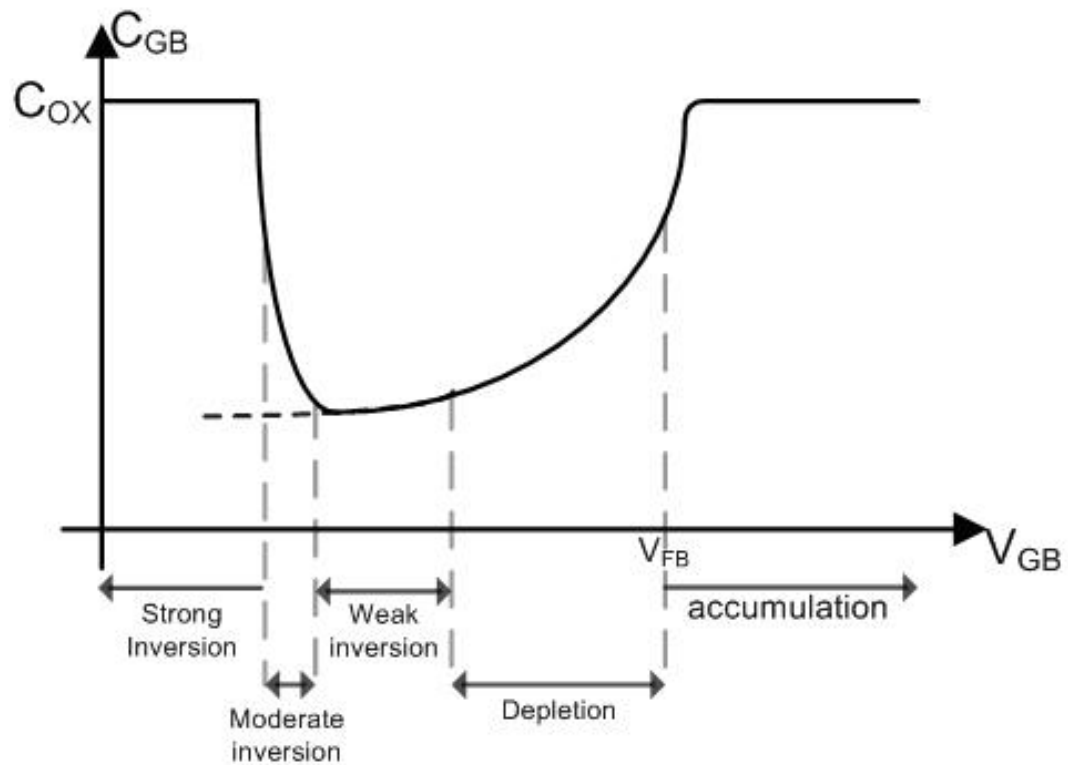


FIGURE 9.17: PMOS varactor C_{gb} vs V_{gb} , (dashed line for high frequencies)

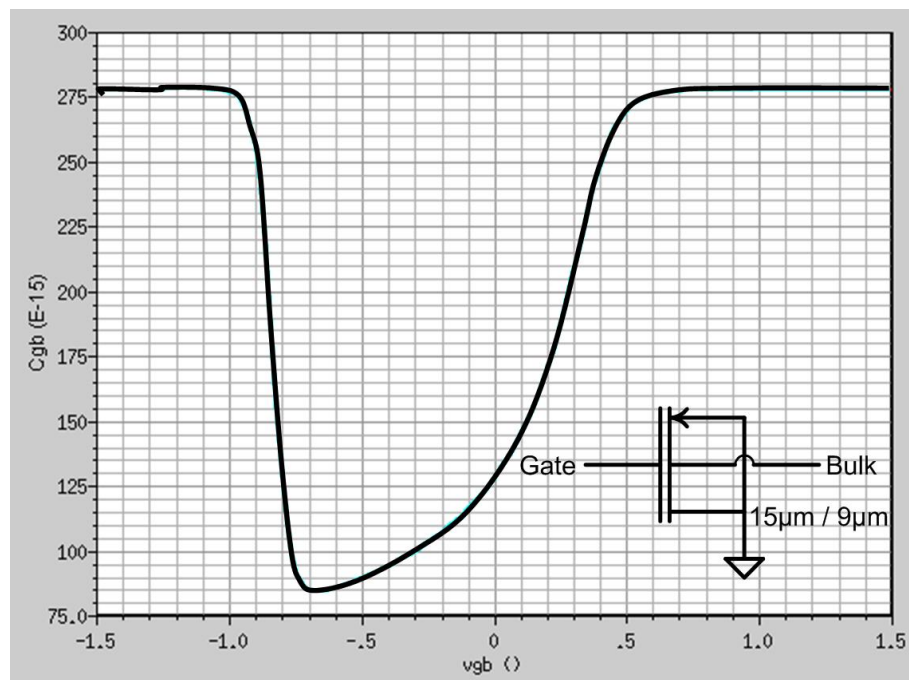


FIGURE 9.18: Simulated PMOS varactor (inset): C_{gb} vs V_{gb}

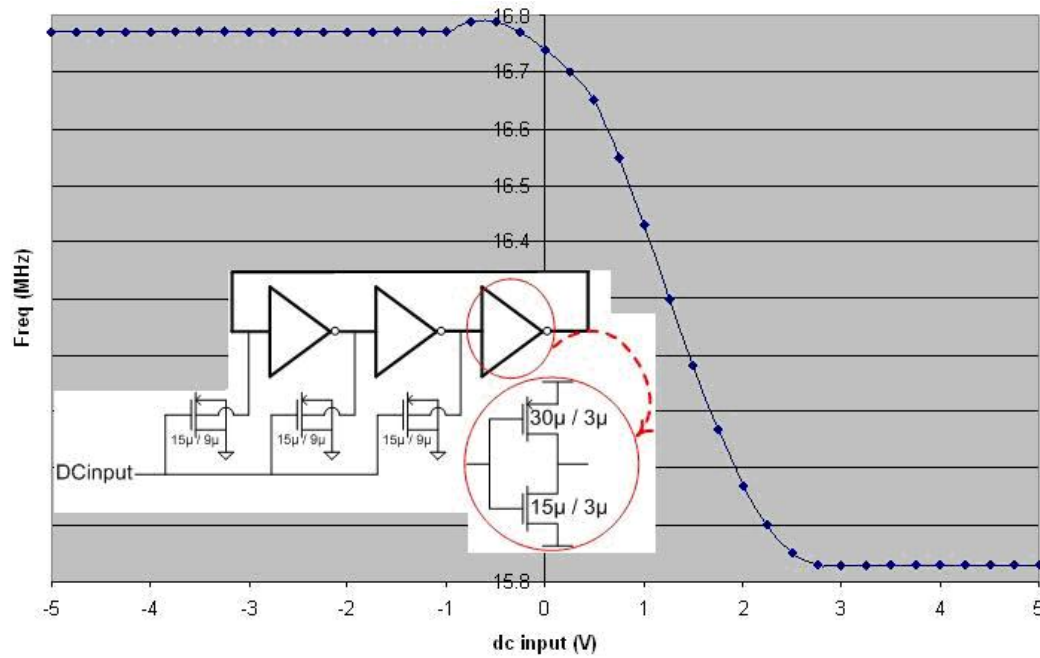


FIGURE 9.19: Frequency vs DC input of the VCRO (inset)

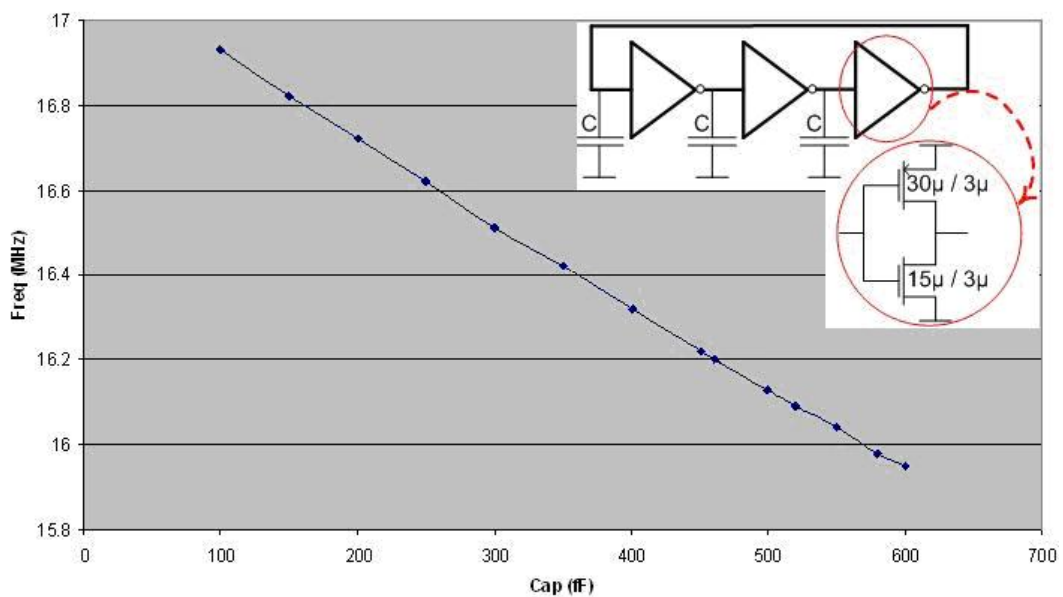
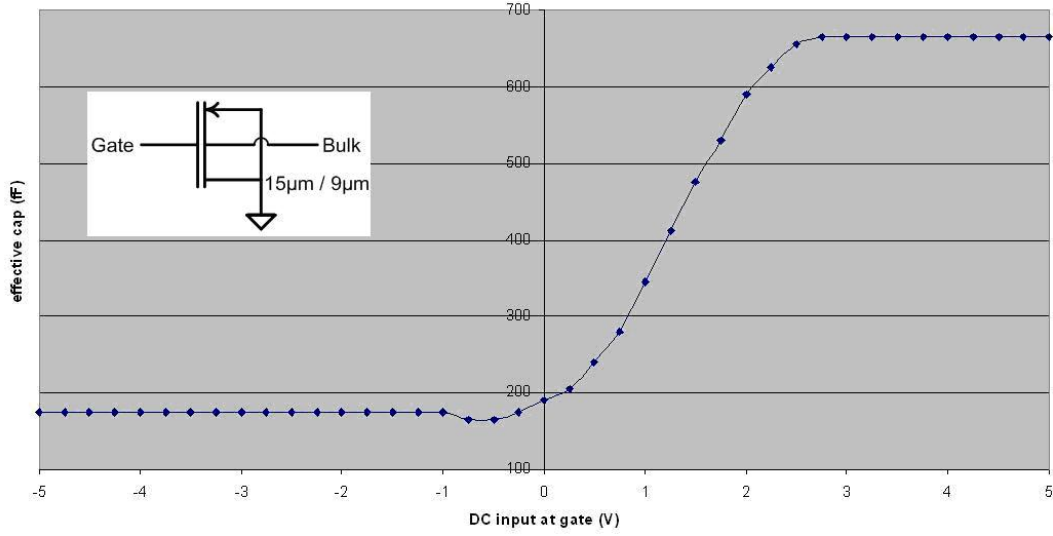


FIGURE 9.20: Frequency vs capacitance of a ring oscillator (inset)

9.3.5 Multitapped Ring Oscillator

Figure 9.22a illustrates a standard single-ended RO whereas figure 9.22b illustrates a conventional VCRO whose last stage incorporates a MOS varactor as explained in the previous section. Figure 9.22c illustrates a multi-tapped VCO where each one of the stages contains a MOS varactor along with the capacitor C_{fixed} corresponding to each

FIGURE 9.21: C_{gb} vs V_{gb} for the PMOS varactor (inset)

stage. In what follows we investigate theoretically, the conditions for which the oscillation frequency f_{osc1} of the conventional VCRO of figure 9.22b and multi-tapped topology shown in figure 9.22c (f_{osc2}) are equal. The analysis assumes that the number of stages and all device sizes are the same for both oscillators. According to 9.22

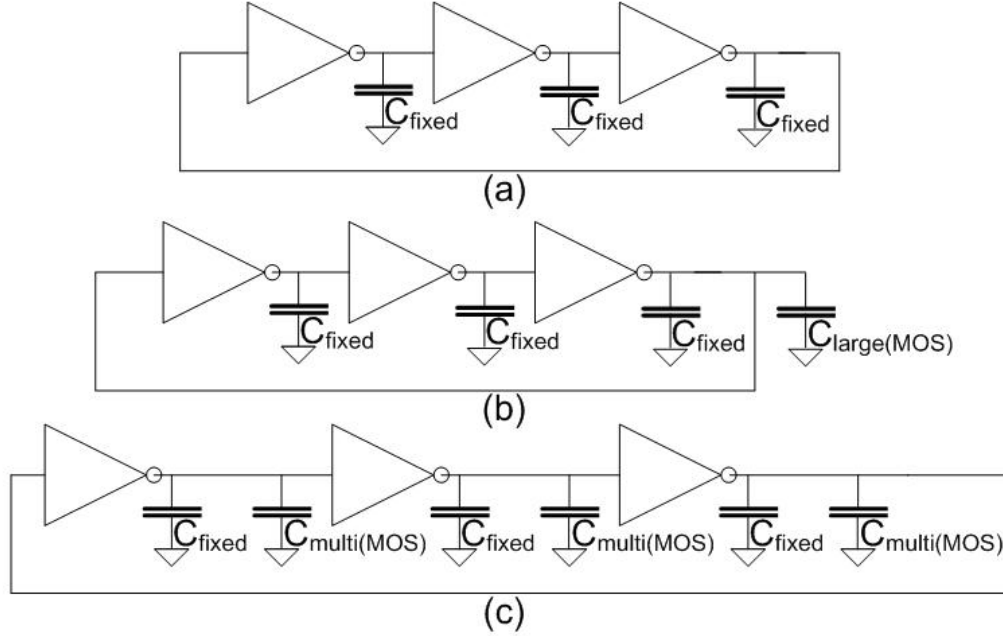


FIGURE 9.22: (a) Ring Oscillator, (b) Conventional VCO, (c) Multitapped VCO

$$f_{osc2}(fig9.22c) = \frac{1}{N} \frac{1}{4 [C_{fixed} + C_{multi}]} \frac{1}{\frac{1}{\mu_n C_{ox} (\frac{W}{L})_n V_{dd}} + \frac{1}{\mu_p C_{ox} (\frac{W}{L})_p V_{dd}}} \quad (9.24)$$

C_{fixed} includes the capacitor to ground at each inverter stage plus the transistor parasitics. For f_{osc1} it will hold since the last stage has a different capacitor value:

$$f_{osc1}(fig9.22b) = \frac{1}{[(N-1)[t_{fall} + t_{rise}] + [t_{fall} + t_{rise}]_{final-stage}} \quad (9.25)$$

which can be re-expressed as:

$$f_{osc1}(fig9.22b) = \frac{1}{\left[(N-1) \left(\frac{4C_{fixed}}{\mu_n C_{ox} \left(\frac{W}{L} \right)_n V_{dd}} + \frac{4C_{fixed}}{\mu_p C_{ox} \left(\frac{W}{L} \right)_p V_{dd}} \right) + \left(\frac{4(C_{fixed} + C_{large})}{\mu_n C_{ox} \left(\frac{W}{L} \right)_n V_{dd}} + \frac{4(C_{fixed} + C_{large})}{\mu_p C_{ox} \left(\frac{W}{L} \right)_p V_{dd}} \right) \right]} \quad (9.26)$$

By direct comparison of 9.24 and 9.26 it should be clear that,

$$N4[C_{fixed} + C_{multi}] = (N-1)4C_{fixed} + ((4C_{fixed}) + (4C_{large})) \quad (9.27)$$

Then $f_{osc1} = f_{osc2}$, however, equation 9.27 reduces to,

$$NC_{multi} = C_{large-MOS} \quad (9.28)$$

In other words relation 9.28 reveals that in order for f_{osc1} to equal f_{osc2} , $C_{multi} = \frac{C_{large-MOS}}{N}$. These smaller (than C_{large}) C_{multi} capacitor values suggest that the amplitude of the signal fed-back through the MOS varactor should reduce.

9.3.6 Multi-tapped Ring Oscillator: properties and comparison with conventional Ring Oscillator

In this section we examine in a rather detailed manner, the properties and behavior of the signal appearing on the control (DC input) line of the MOS varactor for both the multi-tapped and the conventional VCO. Referring to the multi-tapped case (see figure 9.23), when the MOS varactor control terminals (DC input) are all connected together, then signals fed back through each of the many MOS varactors will appear on the control line (DC input) affected of course by the MOS varactor non-linearity. Due to the nature

of operation of the RO, each of these signals will be delayed through each inverter stage by θ , whereas the delay through each MOS capacitor is symbolized as ϕ .

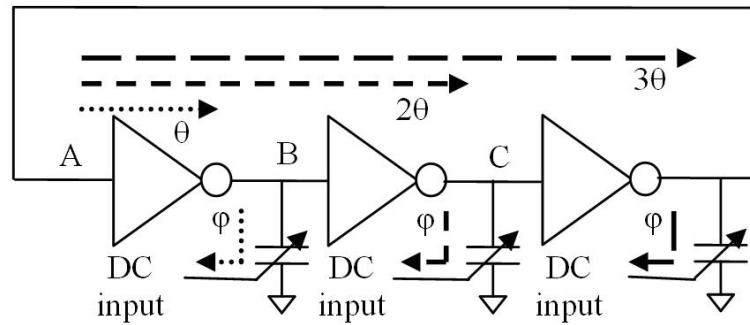


FIGURE 9.23: Three-stage voltage controlled ring oscillator

Figure 9.24 illustrates in a rather idealized manner the waveform at points A, B and C of figure 9.23. (Due to the charging and discharging of the capacitors the waveforms at A, B and C will actually be skewed).

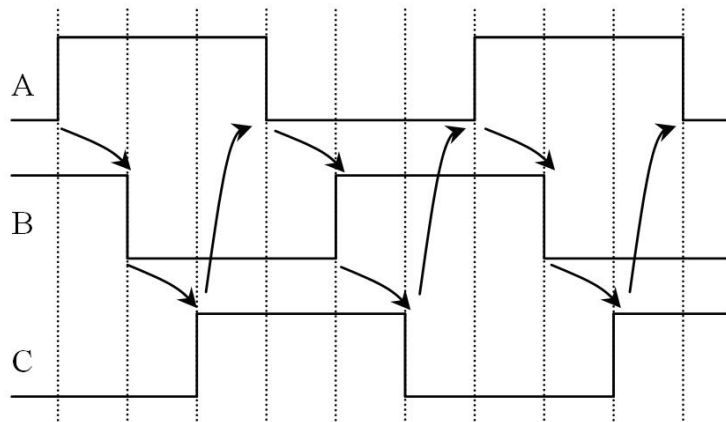


FIGURE 9.24: Signal Analysis

Due to the charging and discharging rate the current at the control line does not smooth out. Clearly this current will in general be affected by the size of the MOS varactor. As explained in the previous paragraph, when a multi-tapped RO is designed to operate at the same frequency as a conventional one with the same number of stages N , then $C_{multi} = \frac{1}{N} C_{large-MOS}$. These reduced (MOS) varactor values suggest that the current fed back through each of the multi-tapped MOS varactors will be smaller than the current fed back through the single MOS varactor of the conventional case. Before examining this behavior it is worth considering the conventional case. However, prior to this it is worth investigating the effect of the superposition action taking place at the control line in the multi-tapped case.

Figure 9.25 illustrates signals on the control line of two sets of three-stage multi-tapped oscillators (figure 9.26); one for which all control inputs are connected together and one for which they are not. Figure 9.25 illustrates the results of the circuit depicted in figure 9.26. As can be seen, the amplitude variation is smaller by about 20% when all control inputs are combined together. In an effort to understand further how this signal cancellation takes place we now investigate it analytically though in a rather approximate manner.

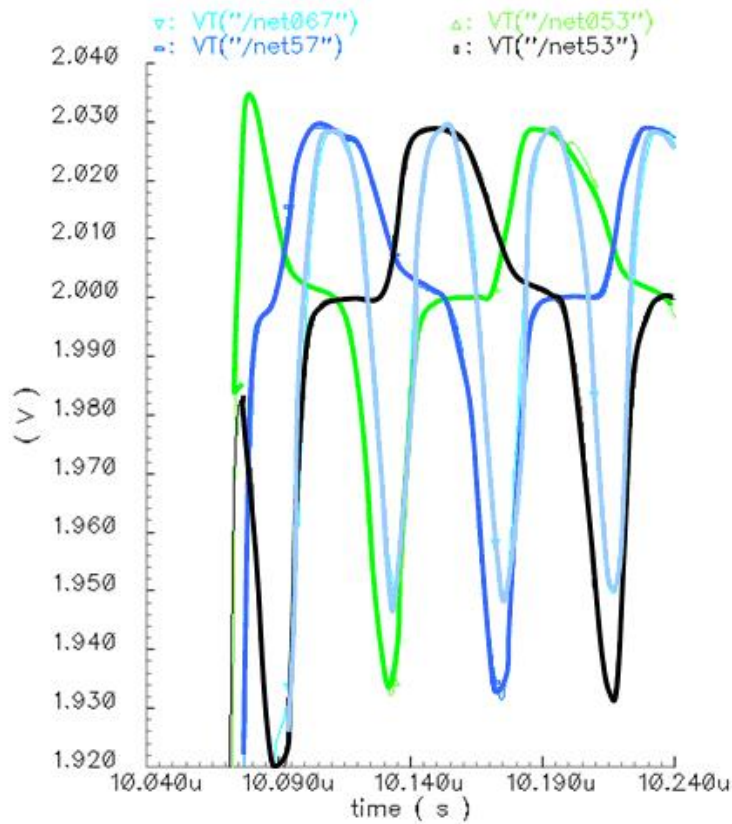


FIGURE 9.25: Comparison of two 3-stage multi-tapped RO's (also consult figure 9.26) with the MOS capacitor control lines all connected together ('net67' trace) and when they are not. Superposition of signals seems to lead to amplitude reduction. All PMOS varactors are of the same size.

Under the assumption that all MOS varactor are identical and that the signals appearing at each one of the control lines are (very approximately admittedly) of triangular form (this can be justified qualitatively by the fact that the capacitors are being charged and discharged and empirically by graphs similar to 9.27) then the following can be argued.

In general a triangular waveform of peak-to-peak amplitude equal to 1 unit will be given by,

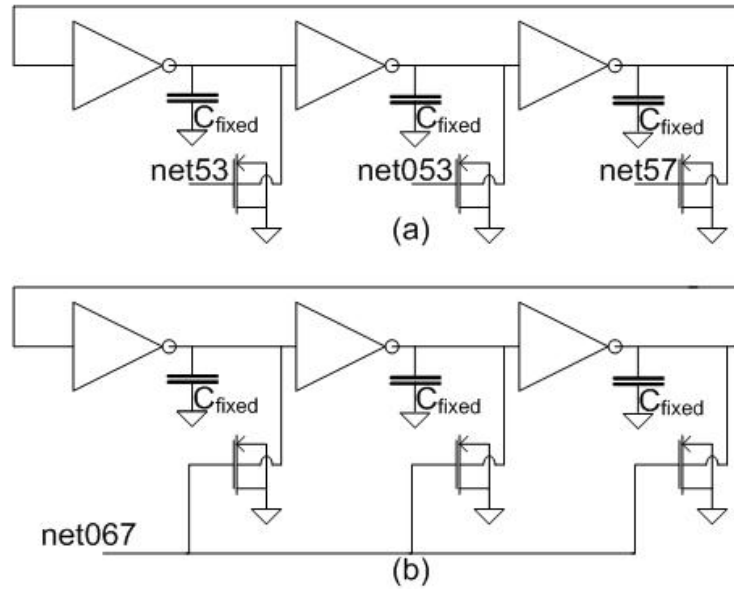


FIGURE 9.26: a) Three stage multi-tapped ring oscillator with individual inputs, b) Three stage multi-tapped ring oscillator with all inputs connected together. Note all PMOS varactors are of the same size.

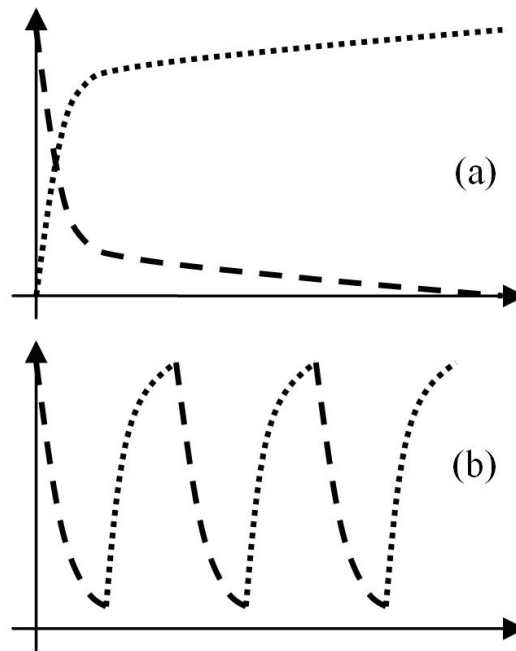


FIGURE 9.27: (a) shows expected charging and discharging of a capacitor and (b) shows what would happen if the charging and discharging occurred at high frequency

$$x_{\omega t} = \frac{8}{\pi^2} \sum_{k=1}^{\infty} \sin\left(\frac{k\pi}{2}\right) \frac{\sin(k\omega t)}{k^2} \quad (9.29)$$

Given the assumption of matched MOS varactor it is reasonable to deduce that each one

of them would introduce the same delay; hence, the signals appearing at the control line will be delayed versions of 9.29. Given that the period of oscillation $T_{osc} = 2N\tau$ with τ denoting the delay of an individual stage, the signals from an N stage oscillator would have the form:

$$x_{1(\omega t)} = \frac{8}{\pi^2} \sum_{k=1}^{\infty} \left[\sin\left(\frac{k\pi}{2}\right) \frac{\sin(k\omega(t - \tau))}{k^2} \right] \quad (9.30)$$

$$x_{2(\omega t)} = \frac{8}{\pi^2} \sum_{k=1}^{\infty} \left[\sin\left(\frac{k\pi}{2}\right) \frac{\sin(k\omega(t - 2\tau))}{k^2} \right] \quad (9.31)$$

$$x_{N(\omega t)} = \frac{8}{\pi^2} \sum_{k=1}^{\infty} \left[\sin\left(\frac{k\pi}{2}\right) \frac{\sin(k\omega(t - N\tau))}{k^2} \right] \quad (9.32)$$

Bearing in mind that

$$\tau = \frac{T_{osc}}{2N} \rightarrow \omega\tau = \frac{\omega T_{osc}}{2N} = \frac{\pi}{N} \quad (9.33)$$

Relations 9.30, 9.31 and 9.32 can be re-written as follows:

$$x_{1(\omega t)} = \frac{8}{\pi^2} \sum_{k=1}^{\infty} \left[\sin\left(\frac{k\pi}{2}\right) \frac{\sin(k\omega(t - \frac{k\pi}{N}))}{k^2} \right] \quad (9.34)$$

$$x_{2(\omega t)} = \frac{8}{\pi^2} \sum_{k=1}^{\infty} \left[\sin\left(\frac{k\pi}{2}\right) \frac{\sin(k\omega(t - \frac{k2\pi}{N}))}{k^2} \right] \quad (9.35)$$

$$x_{N(\omega t)} = \frac{8}{\pi^2} \sum_{k=1}^{\infty} \left[\sin\left(\frac{k\pi}{2}\right) \frac{\sin(k\omega(t - \frac{kN\pi}{N}))}{k^2} \right] \quad (9.36)$$

The superposition signal will now be given by,

$$X_s(\omega t) = x_1(\omega t) + x_2(\omega t) + \dots + x_N(\omega t) \quad (9.37)$$

Figures 9.28a, 9.28b and 9.28c show confirming results for various for various values of N (N=3, 5, 7).

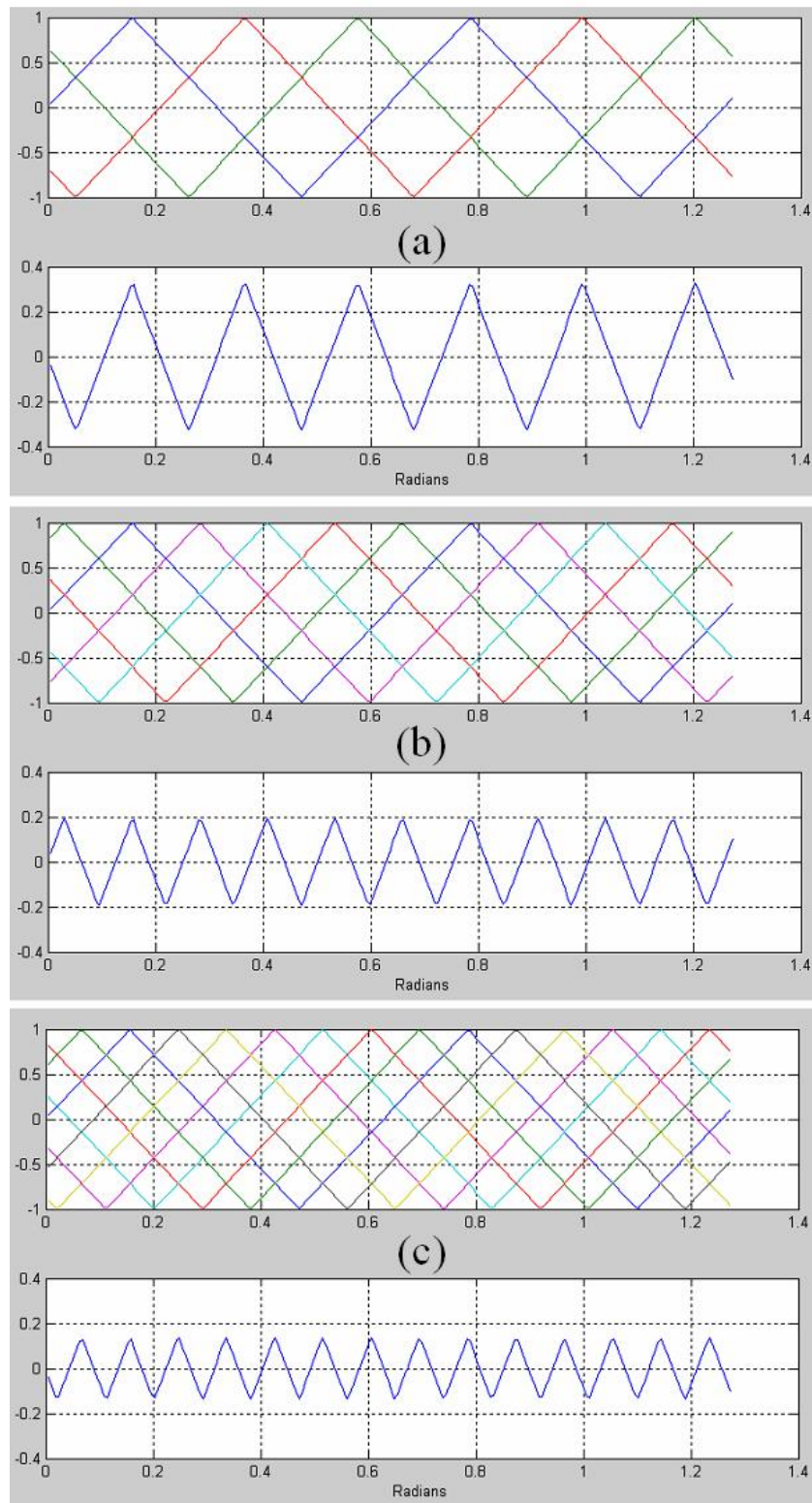


FIGURE 9.28: The effect of superposition (relation 9.37) for a) $N=3$, b) $N=5$ and c) $N=7$, with the amplitude = 1 unit and $\omega = 10$. Observe that as N increases the amplitude of X_s decreases

From the above it must have become clear that the superpositioning action leads to reduced signal levels on the control lines. The comparison between the multi-tapped and the conventional case by means of simulation results reveals a significant reduction of the signal amplitude for the multi-tapped case. Figure 9.29a illustrates a 7 stage multi-tapped oscillator, whereas figure 9.29b illustrates a conventional version corresponding to the same oscillation frequency. Figure 9.30 and 9.31 show the signals on the control line for the multi-tapped and the conventional case respectively.

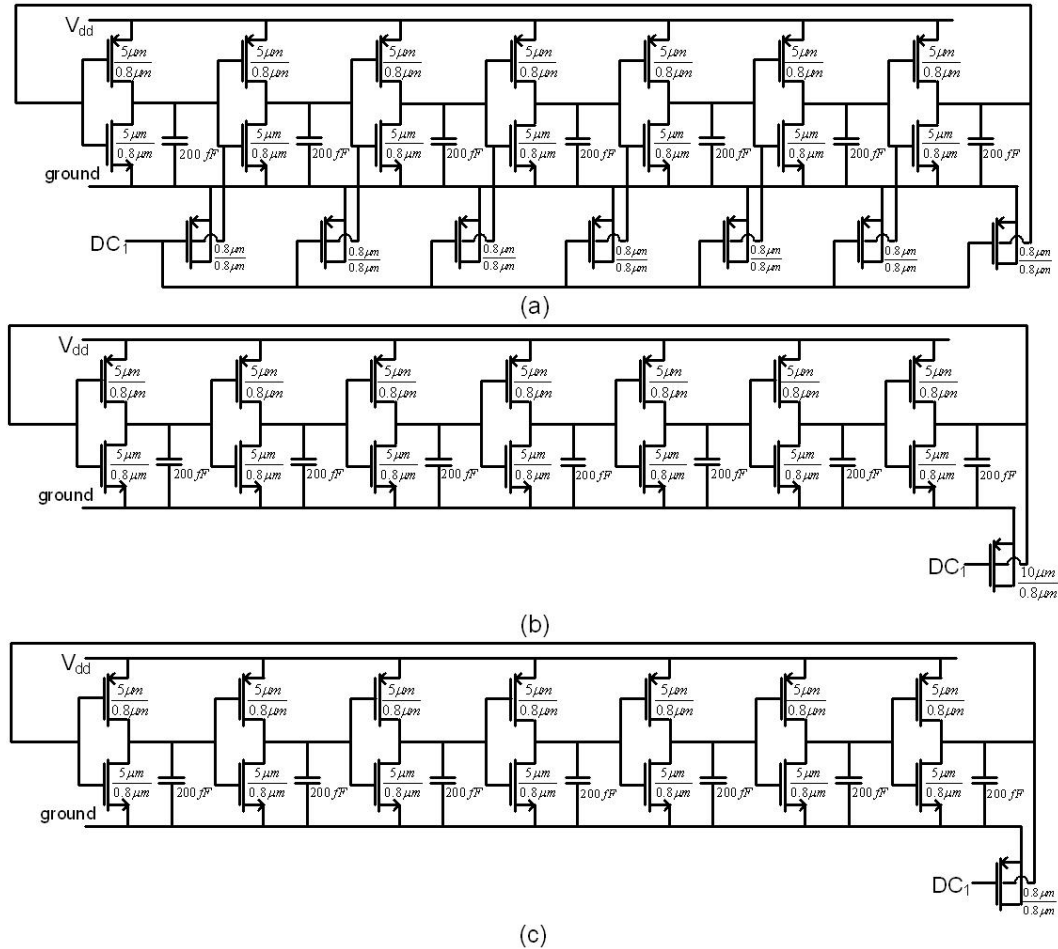


FIGURE 9.29: a) Multi-tapped Oscillator, b) Single Tap Oscillator, c) reduced size varactor from (a) used in Single Tap Oscillator

Clearly the multi-tapped case corresponds to lower signal amplitude. This is facilitated both by the fact that the superposition action takes place but also from the fact that the MOS capacitors for the multi-tapped case are smaller than the single MOS capacitor of the conventional case (bearing in mind figure 9.28). Figure 9.30 represents the circuit if figure 9.29a, the multi-tapped feedback noise was recorded as 39mV, while in the conventional case (figure 9.31) the feedback noise is 549mV. The multi-tapped circuit provides a 93% reduction in feedback noise. This reduction operates by a two fold

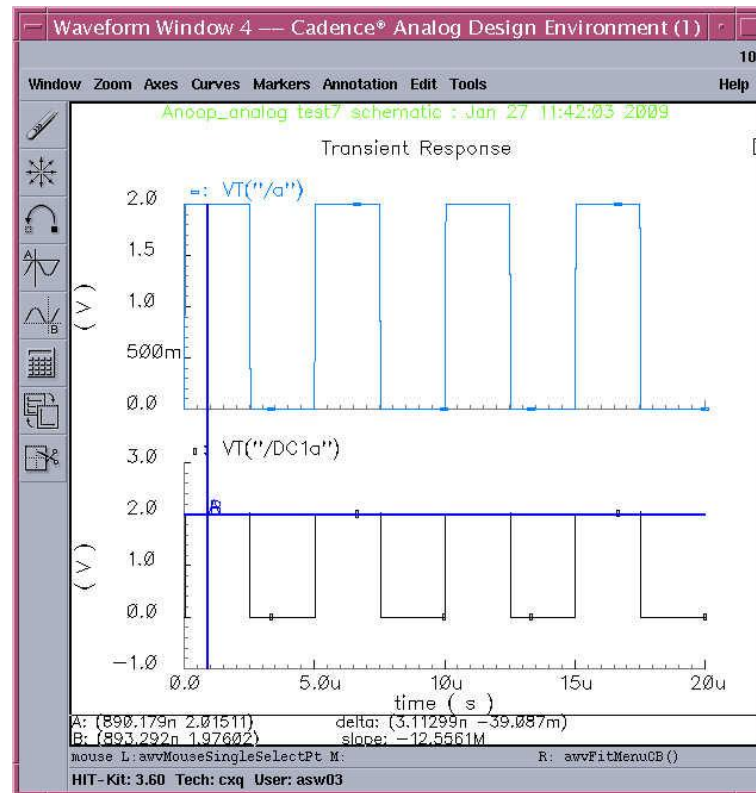


FIGURE 9.30: Single output control line for the multi-tapped oscillator (9.29a)

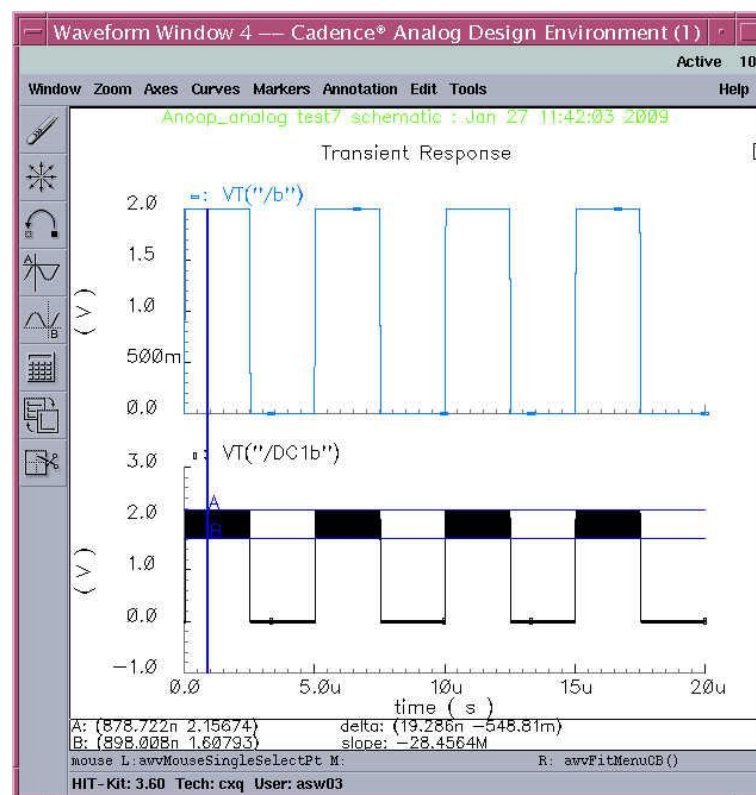


FIGURE 9.31: Single output control line for the single tapped oscillator (9.29b)

mechanism, 1) reduction in varactor size, 2) signal cancellation. To illustrate the signal cancellation figure 9.32 depicts the results of the circuit in figure 9.29c.

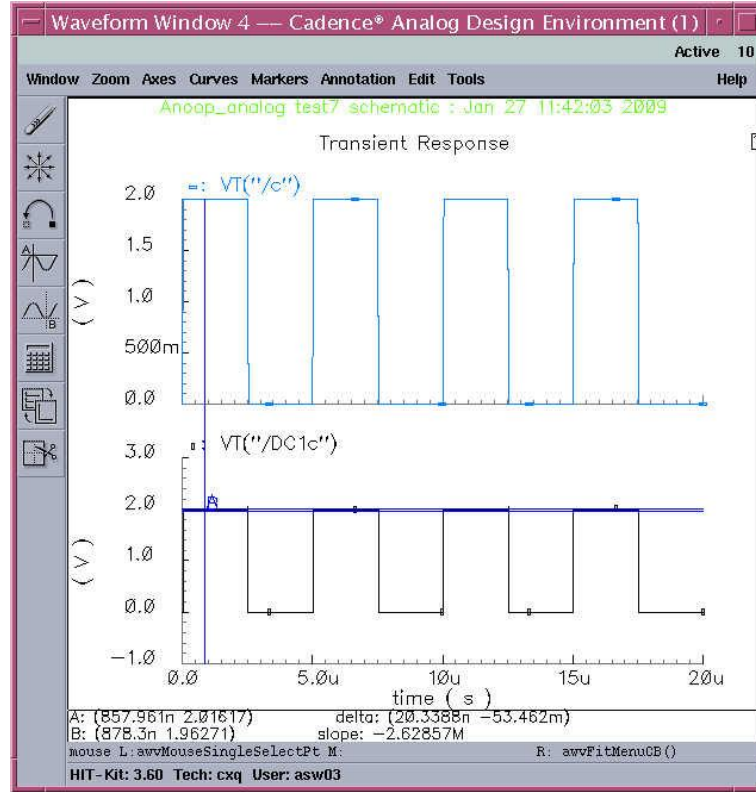


FIGURE 9.32: The reduced size MOS transistor capacitor single tapped oscillator. Clearly multi-tapping reduces the unwanted signal on the control line (9.29c).

Simulation results for different numbers of stages would also confirm the above behaviour. For a single-tap 5-stage oscillator for example with a single tap PMOS capacitor of $10\mu\text{m} \times 0.8\mu\text{m}$ and for a 0-2V DC input variation, the VCO frequency ranges from 25.24MHz to 25.29MHz; for the multi-tapped case with $1.6\mu\text{m} \times 0.8\mu\text{m}$ PMOS capacitors, the output frequency ranges from 24.73MHz to 24.94MHz. However, the reduction of the amplitude of the unwanted signal on the control line reaches an approximated 90%. For a 3 stage oscillator (multi-tapped, $\frac{0.8\mu\text{m}}{0.8\mu\text{m}}$ PMOS capacitors, $9\text{MHz} \pm 0.03\text{MHz}$ vs. Single-tapped, $\frac{3\mu\text{m}}{0.8\mu\text{m}}$ PMOS capacitors, $9\text{MHz} \pm 0.03\text{MHz}$) as reduction of 82% of the amplitude of the unwanted signal is achieved (40mV vs. 7mV).

9.3.7 Jitter Noise Analysis

The material covered in this section is based primarily on references [128] and [129]
When designing an oscillator, one of the most important considerations is jitter noise. Jitter noise is the occurrence of “non-idealities” in the spectrum of the desired signal.

Should figure 9.33a show the ideal output signal of the oscillator, then figure 9.33b shows its ideal spectrum. However due to real world occurrences the actual spectrum of the oscillator will appear more like that in figure 9.33c. In other words, the spectrum line of the oscillator will be characterized by a finite width. This can be attributed to noise (unwanted signals) occurring during the transient waveform. For example see figure 9.34. [121]

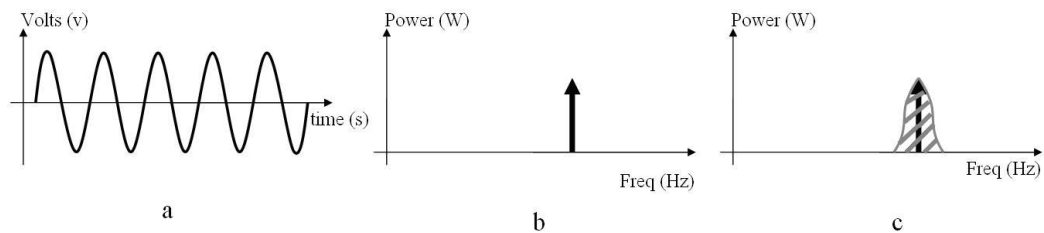


FIGURE 9.33: (a) Perfect sine wave in the time domain, (b) Perfect sine wave in the frequency domain, (c) 'Real' sine wave in the frequency domain

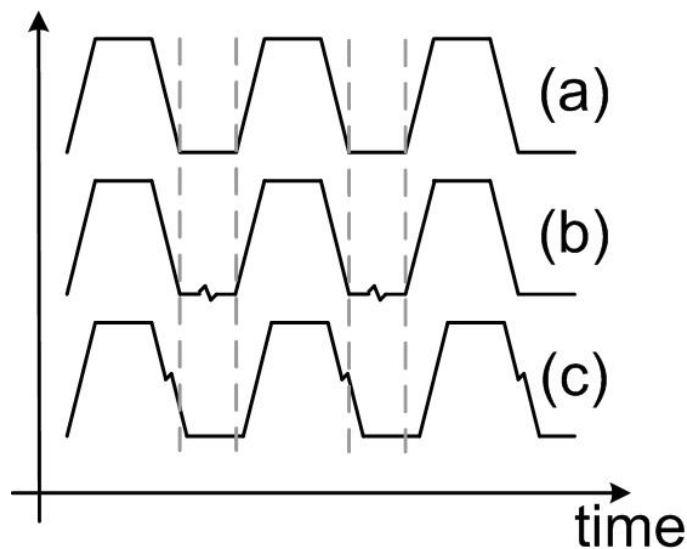


FIGURE 9.34: (a) The ideal transient oscillator signal, (b) the signal in a) with noise injected when the signal is 'low' and (c) the signal in a) with the noise on a transitional period.

Now specifically looking at the noise for a ring oscillator case, as noise may occur anywhere in the time domain, it is important to consider where the greatest error could occur. Assume that the signal is noise free until a noise spike appears to the circuit. In the transient signal, there are two main points where the spike can occur. Either when the signal is high or low, or on the transition period of 'low to high' or 'high to low' (see figure 9.34).

Note that if the current noise is injected when the transient is at a low, the overall frequency is not changed (see figure 9.34b). If however the noise is added during a

transitional period, then the frequency has is affected (see figure 9.34c). As a variation in the frequency will change the operation of the oscillation.

As reported by [120], jitter $\sigma_{t_{dl}}$ may be written as in 13.31 (full analysis in Appendix A).

$$\sigma_{t_{dl}} = \frac{2kT\gamma_N CV_{DD}}{I_N^2(V_{DD} - V_{tN})} \quad (9.38)$$

k is the Boltzmann constant, T represents the absolute temperature, γ_N is the noise coefficient and finally I_N is the NMOS current. In other words, the jitter is proportional to the power supply levels, the integrating capacitor value and the temperature whereas it is inversely proportional to the square of the current and then device overdrive.

9.3.8 Summary of the VCO Design

The heart of the transmitter unit is the oscillator itself, in order to significantly reduce the high frequency feedback noise a novel Multi-tapped Voltage Controlled Ring Oscillator has been designed. The multi-tapped oscillator provides two fold reduction in feedback noise, firstly through the reduction in the dimension of the MOS capacitor and then of signal cancellation. The multi-tapped oscillator may also be used to overcome any manufacturing errors that may occur. In order for a ‘clean’ (in terms of frequency domain) output, jitter noise should be minimized. This is done by using small capacitors, low power supply and the MOS transistors should have small widths and lengths.

9.4 Antenna Interface

As explained before we aim at implementing a 13.56MHz short-range link. Consequently a pair of 13.56MHz antennae have been used. Figure 9.35 illustrates the antenna used.

Figure 9.36 illustrates the experimental setup used for testing how the distance between the two antennae affects the voltage amplitude received. More specifically: antenna A is driven by means of a signal generator with a 13.56MHz voltage signal. Antenna B receives the transmitted signal at various distances from antenna A and for different voltage swings forced at antenna A. Figure 9.37 illustrates the variation of the received

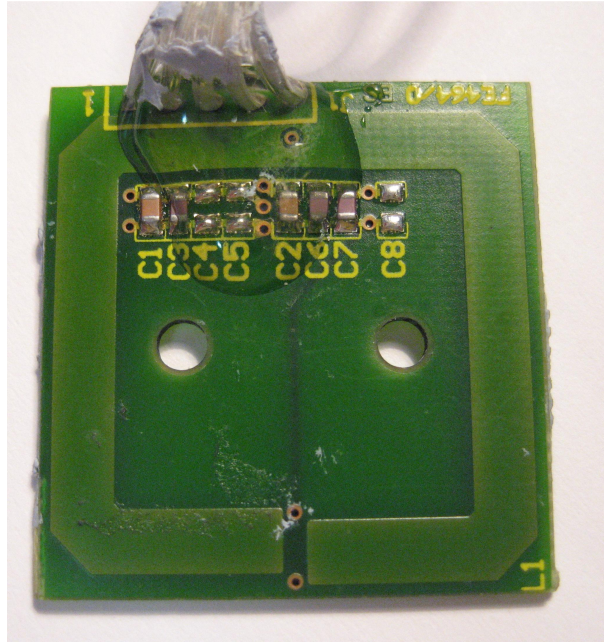


FIGURE 9.35: The Copytag 13.56MHz antenna used, its dimensions are 35mm by 34mm, cost: £46.53

voltage levels as a function of the distance between the antennae. From the measured results of figure 9.37 it can be seen that for distances higher than approximately 3.5cm the received voltage levels start to converge for all transmission swing levels. The maximum useful range for the specific pair of antenna seems to be close to 8cm.

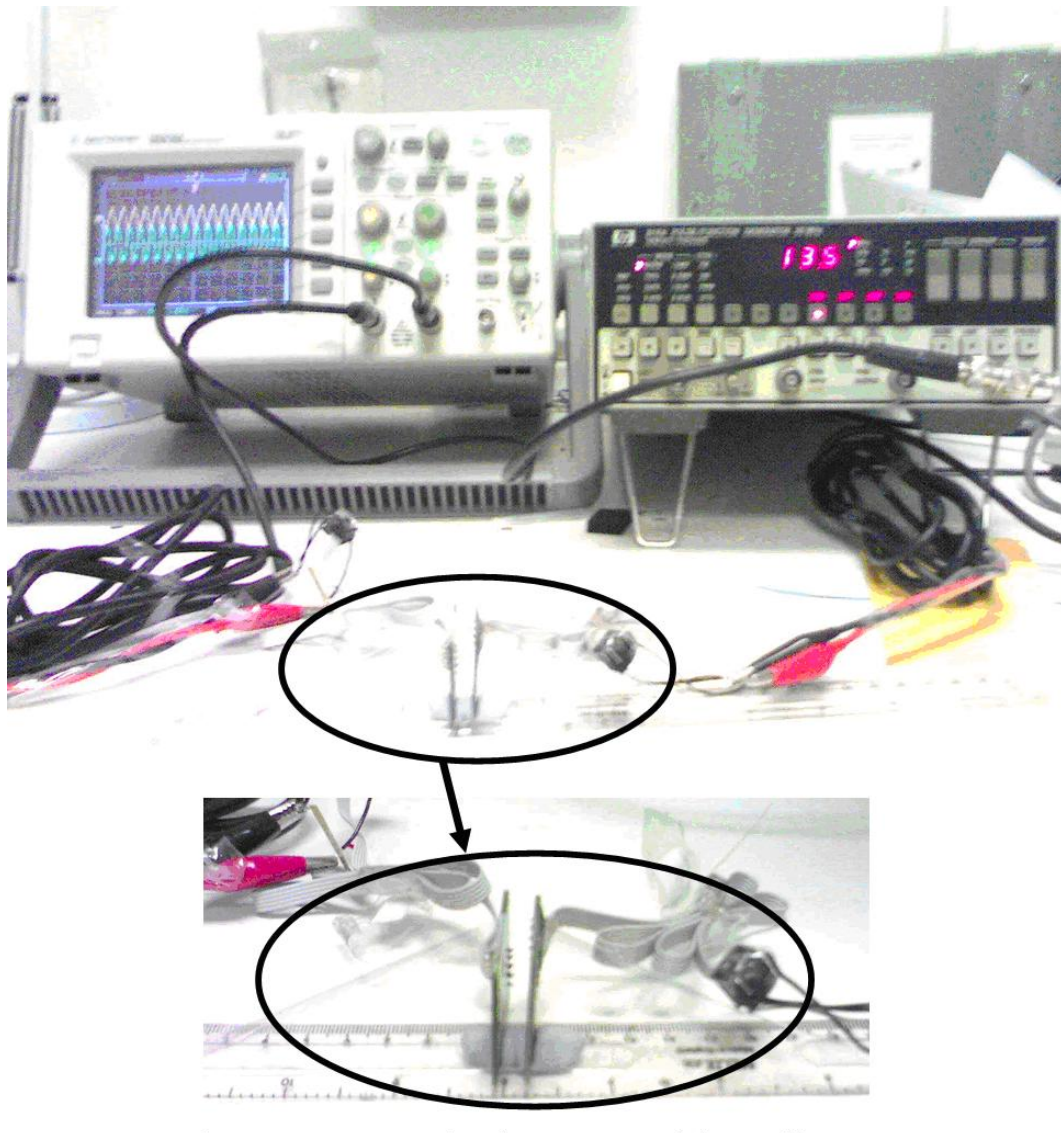


FIGURE 9.36: Experimental setup used for testing the antenna link. A Agilent/HP 8116A Signal generator and a Agilent DSO3062A oscilloscope were used.

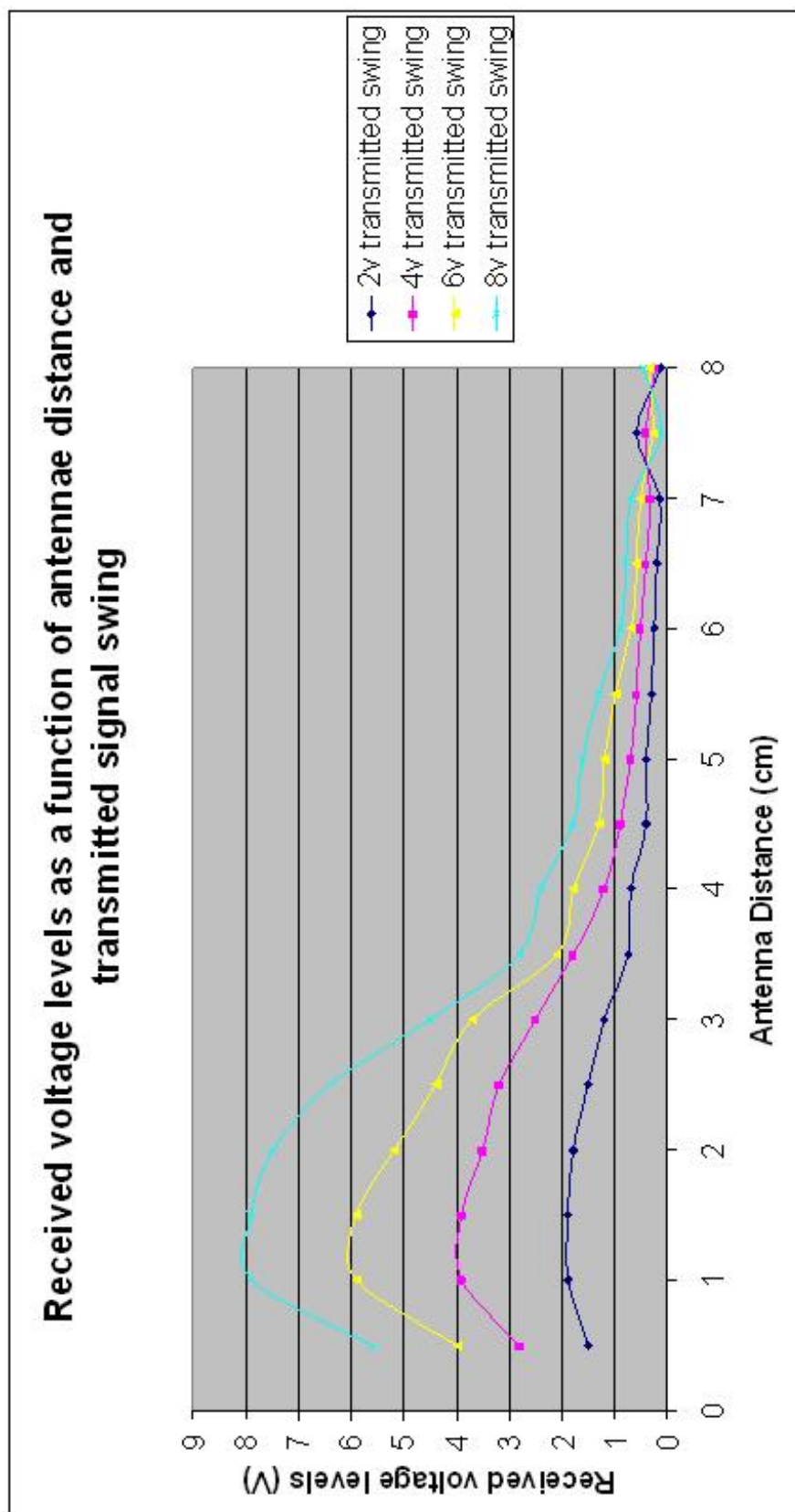


FIGURE 9.37: Measured results of the antenna link

Subsequently, the link was S-characterized by means of the Agilent spectrum analyzer shown in figure 9.38.

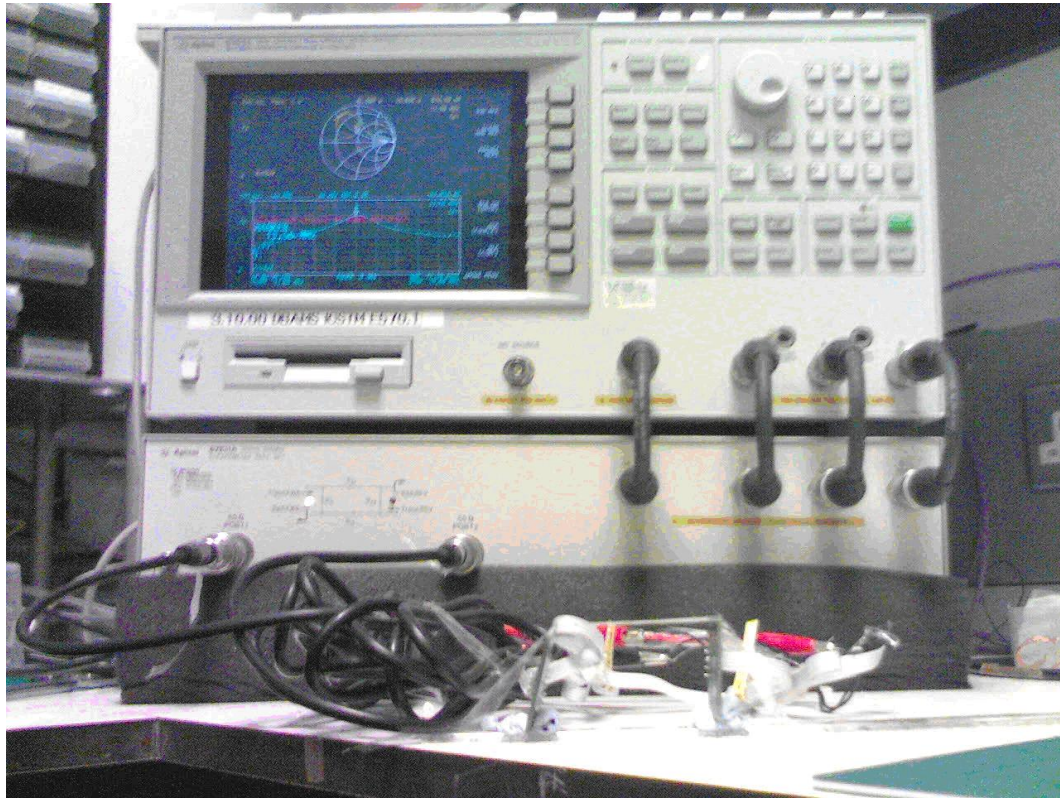
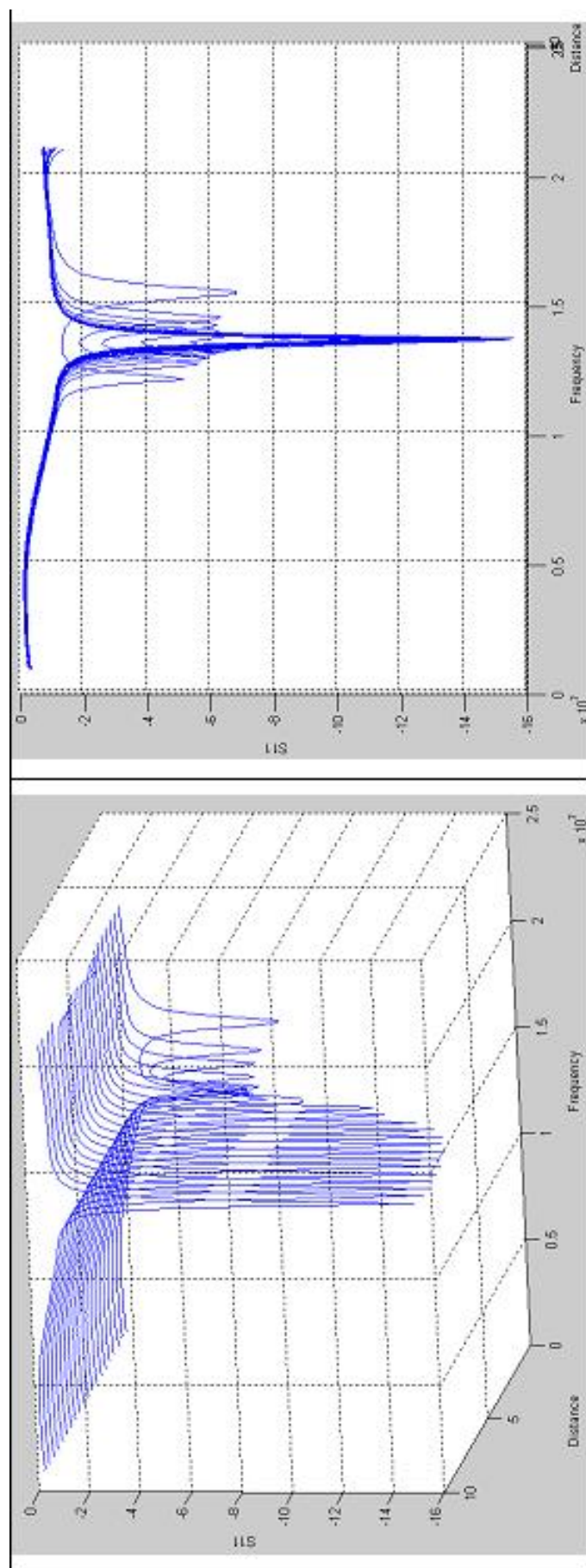
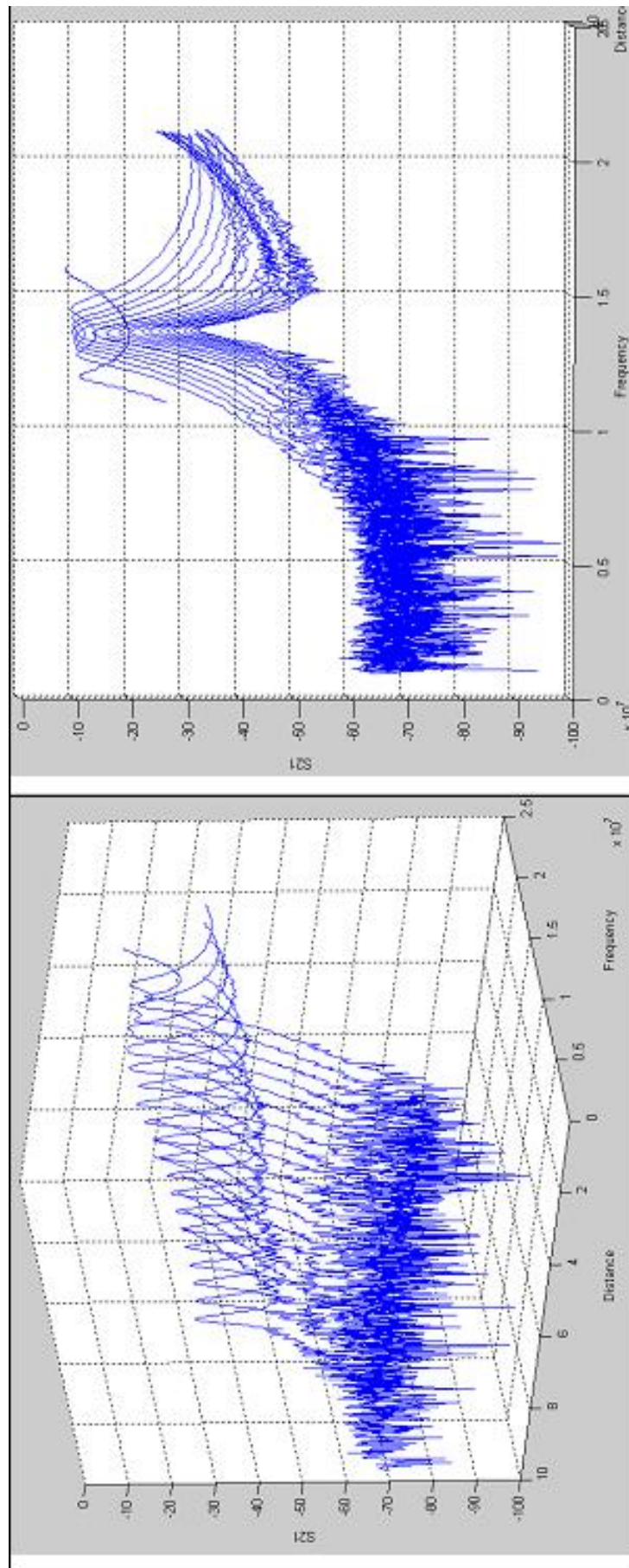


FIGURE 9.38: Experimental setup for the S-characterisation of the link

Figure 9.39 and 9.40 illustrate the dependence of S_{11} and S_{21} respectively as a function of both the antenna distance and the frequency. The measured S_{11} results confirm the fact that the antennae are tuned for the 13.56MHz ISM band. Figure 9.40 illustrates the dependence of S_{21} as a function of both the antennae distance and the frequency whereas figure 9.41 illustrates the position of the S_{11} and S_{21} on the Smith Chart. The data of figure 9.41 allows for matching for a given distance. Examining specifically the S_{11} values, it seems that the further apart the antennae are to one another, the better matched they are to one another.

FIGURE 9.39: Measured S_{11} results of the antenna link

FIGURE 9.40: Measured S_{21} results of the antenna link

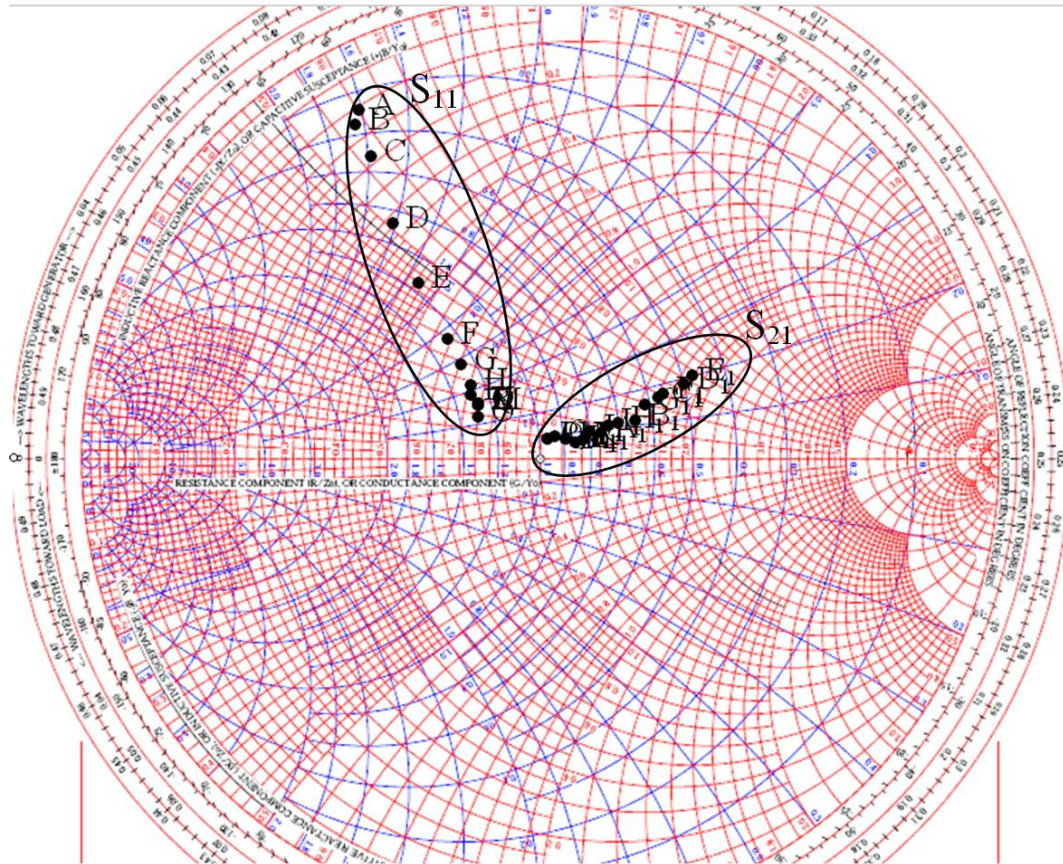


FIGURE 9.41: Smith Chart positioning of the measured S_{11} and S_{21} values for different distances between the antennae. (A=0.5cm, B=1cm, C=1.5cm, D=2cm etc)

9.5 Antenna Driver

The driver circuit must be able to drive an antenna. The antennas are designed to have a 50Ω input impedance when the signal being driven into it is at a frequency of 13.56MHz. Therefore the driver circuit acts as the interface between the antenna and the VCRO.

The output of the VCRO does not have the power to drive the 50Ω impedance antennae, hence a driver circuit is required. The circuit provides greater current while maintaining the voltage swing at the output. Capacitors are used to smooth the square wave output of the VCRO to a sine wave. The driver current is displayed within figure 9.42a, with the equivalent model in figure 9.42b.

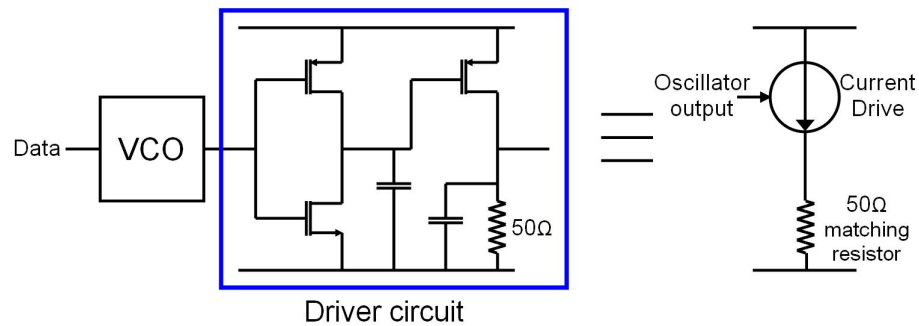


FIGURE 9.42: The transmitting antenna driver circuit

9.6 Conclusion

The transmitter (shown in figure 9.43) is designed from a multi-tapped ring oscillator combined with the antenna driving circuit. The VCRO has two inputs,

1. one for logic 1 or 0 (which represents the data) and,
2. fine-tuning the VCRO frequency range.

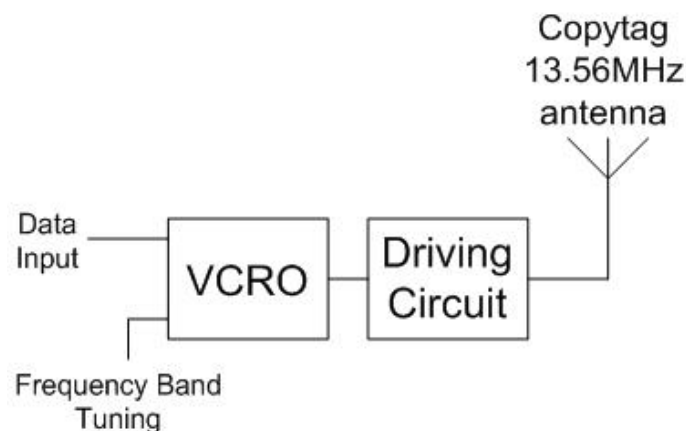


FIGURE 9.43: Block diagram of the transmitting unit

The VCRO will take on the structure of figure 9.44

The DATA conveying transistor is of minimum size in order for the 13.553-13.567MHz ISM band to be achieved (figure 9.45).

Due to the inaccuracies that may occur during the manufacturing process, it is useful, even practically imperative to have the second input to set the VCRO's frequency range. The FREQUENCY TUNING INPUT allows the 13.553 - 13.567MHz frequency band to be shifted up or down in frequency (figure 9.46).

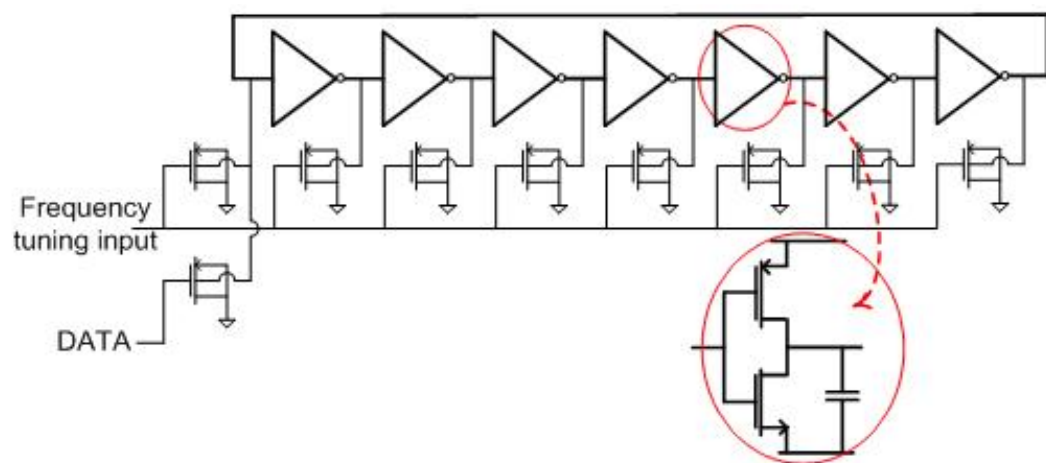


FIGURE 9.44: Circuit diagram of the VCRO circuit

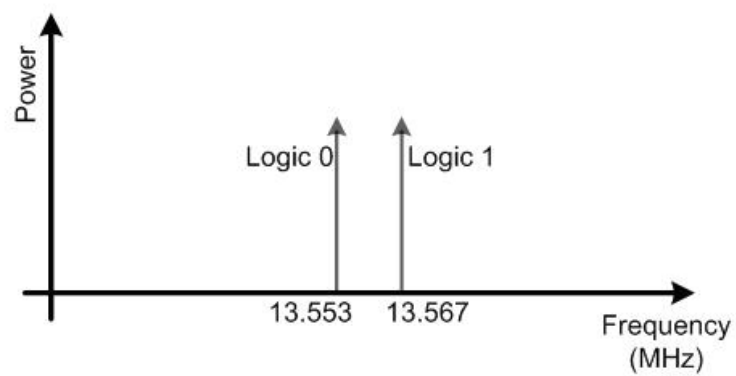


FIGURE 9.45: Output frequency of the circuit in figure 9.44 when subjected to a logic 1 or 0 at the DATA terminal

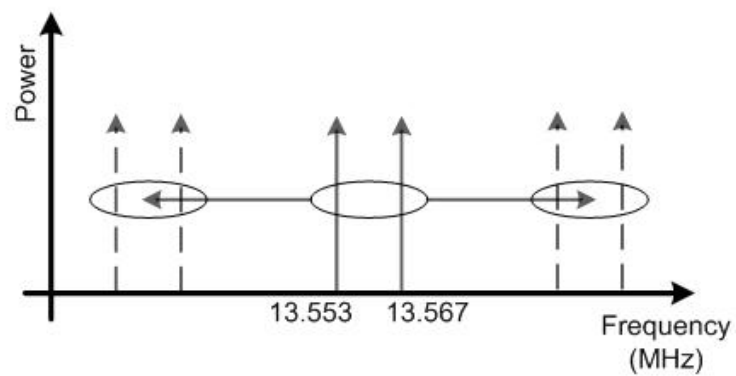


FIGURE 9.46: Output frequency of the circuit in figure 9.44 when subjected to a variation in the Frequency tuning input terminal

Chapter 10

Receiver

The transmitter has been designed by using FSK modulation. This is based simply on the idea that a frequency f_1 represents a logic 0 and f_0 represents a logic 1. Due to the frequency range being the 13.56MHz ISM band then f_1 and f_0 will be 13.553MHz and 13.567MHz respectively. However a decoding mechanism is required, the block which has the ability to do this is known as the Phase Locked Loop (PLL). This chapter discusses the design of the receiver circuit, beginning initially with the antenna amplifier, subsequently the PLL decoder is discussed.

10.1 Amplifier

The first step in any receiver is an amplifier. In general a signal received by an antenna will be too weak to be directly processed and therefore an amplifier is required. In most present day wireless units the first block tends to be a Low Noise Amplifier (LNA). This block requires an inductor biasing network to be correctly tuned for amplification with the desired frequency band [125] [128]. As the frequency is around the 13.56MHz, the inductors which make up the biasing network would be large. As the frequency is low, simple amplification methods can be utilized. As the signal is single-ended, a single (active) transistor amplifier may be used. Simply put, the input signal is biased to a positive DC level and applied to the gate of a common source amplifier (see figure 10.1).

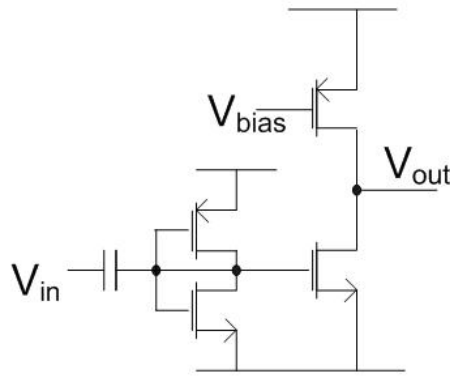


FIGURE 10.1: Receiver Antenna Amplifier

10.2 Phase Locked Loop - Theory Summary

The generic make-up of a PLL is shown in figure 10.2

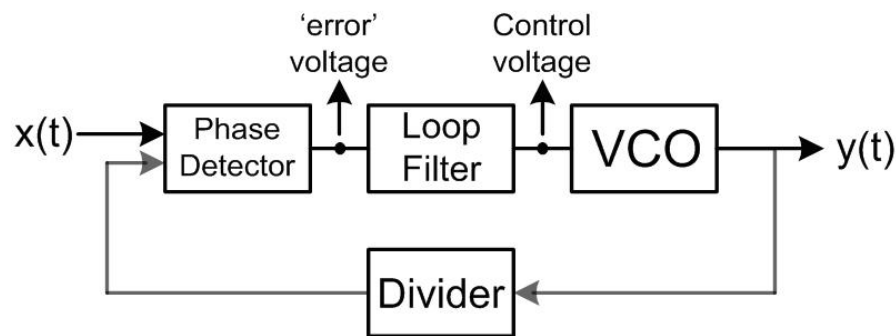


FIGURE 10.2: Traditional Phase Locked Loop

The PLL works on the principle of attempting to force the signals $y(t)$ to become equivalent to $x(t)$ (assuming the divider is set to 1). The VCO (voltage controlled oscillator) oscillates initially at a free running frequency, this frequency is then fed in to the divider, where the frequency is divided and a comparison / reference frequency is generated (assuming that the division is set to 1). The comparison frequency (usually the lowest divided frequency) is fed back to the phase detector (PD). The PD compares the phase of the reference signal $x(t)$ to that of the divider output. If there is a difference in frequency or phase, the PD will output an error voltage. The loop filter (LPF) removes any high frequency components from this voltage and generates a DC voltage level proportional to the difference of the inputs, known as the control voltage. The control voltage is then applied to the VCO and the frequency of operation is adjusted. The new phase and frequency is fed round the loop, until the difference in phase and frequency between $x(t)$ and $y(t)$ becomes negligible. Once this occurs the PLL is said to be locked.

Due to the function of the divider, from one input frequency (the output of the VCO), a number of output frequencies can be obtained. Also if the divider output, is fed into the PD, accurate multiples of the comparison frequency (times by one, two, four and eight) can be obtained. (Note that the divider is not used in this application and so is assumed to be a divide-by-1 (which is just a wire)).

10.2.1 Voltage Controlled Oscillator

The VCO outputs a waveform whose frequency is proportional to the DC control voltage input.

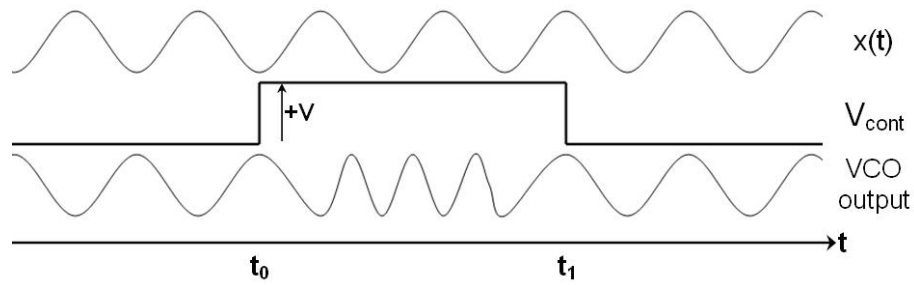


FIGURE 10.3: Voltage controlled oscillator operation basics

Let us assume that when $t < t_0$ the two waves have similar frequencies but are out of phase. To reduce the error, let us assume that V_{cont} needs to be increased by $+V$ at $t = t_0$, so that the VCO's output frequency is increased (figure 10.3). When $t = t_1$, the phase error has decreased to zero hence V_{cont} returns to its original value. Now the two signals have the same frequency and phase (note, that the same result could have been obtained by lowering the VCO frequency instead of raising it). [122]

Realizing the significance of the history of V_{cont} , the output of the VCO is not only determined by the present value of V_{cont} but also the history of V_{cont} . So initially the output phase of the VCO is independent of the reference signal. [123]

The output frequency of the VCO may be written as

$$\omega_{out} = \omega_{FR} + K_{VCO}V_{cont} \quad (10.1)$$

Where ω_{FR} denotes the free running frequency of the voltage controlled oscillator. K_{VCO} denotes the 'gain' of the VCO (hz/s/V).

Equation 10.1 codifies the frequency of the VCO, while its phase is given by equation 10.2

$$\phi_{out}(t) = K_{VCO} \int v_{cont} dt \quad (10.2)$$

This then leads to the input output transfer function to be

$$\frac{\phi_{out}(s)}{V_{cont}(s)} = \frac{K_{VCO}}{s} \quad (10.3)$$

The integration in equation 10.2 simply means that $\phi_{out}(s)$ is insensitive to the high frequency content of $V_{cont}(s)$. This means that if the input to the VCO changes too fast, then there will be no difference in the output phase or frequency. This will in turn limit the sensitivity of the VCO. [124]

10.2.2 Phase Detector

An ideal phase detector (PD) produces an output error signal whose dc value is directly proportional to the change in phase of the two (periodic) inputs.

$$\overline{V_{out}} = K_{PD} \Delta\phi \quad (10.4)$$

Where K_{PD} = gain in (V/rad) and $\Delta\phi$ denotes input phase difference.

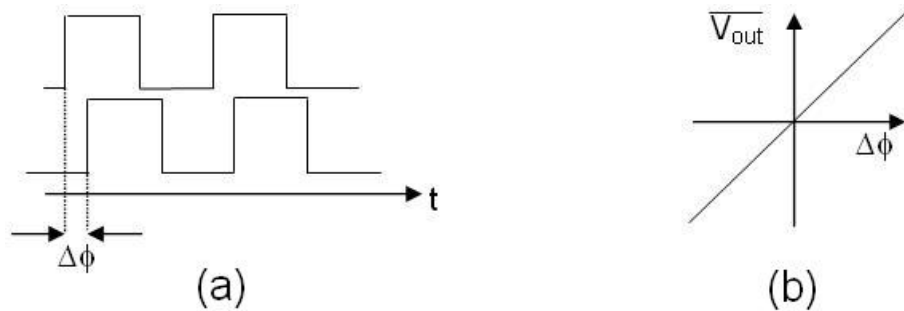


FIGURE 10.4: Basic phase detector operation: the phase difference $\Delta\phi$ in (a) produces a dc output voltage $K_{PD}\Delta\phi$ (b)

It should be stressed that ideally the relationship between $\overline{V_{out}}$ and $\Delta\phi$ is linear [125] [126]. Clearly while dealing with square waveforms a simple XOR CMOS logic gate will provide the operation of the phase detector shown in figure 10.4a.

10.2.3 Loop Filter

If a simple filter is used (as in figure 10.5), then the transfer function is given as,

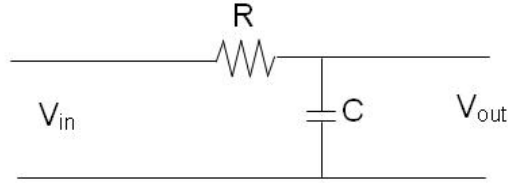


FIGURE 10.5: Elementary Loop Filter

$$V_{out}(s) = \frac{X_C(s)}{R + X_C(s)} V_{in}(s) \quad (10.5)$$

Re-arranging and substituting

$$G_{LPF}(s) = \frac{V_{out}}{V_{in}} = \frac{1}{1 + \frac{s}{\omega_{LPF}}} \quad (10.6)$$

The filter smooths any high frequency signals that may appear at the output of the PD (as in figure 10.6). [74]

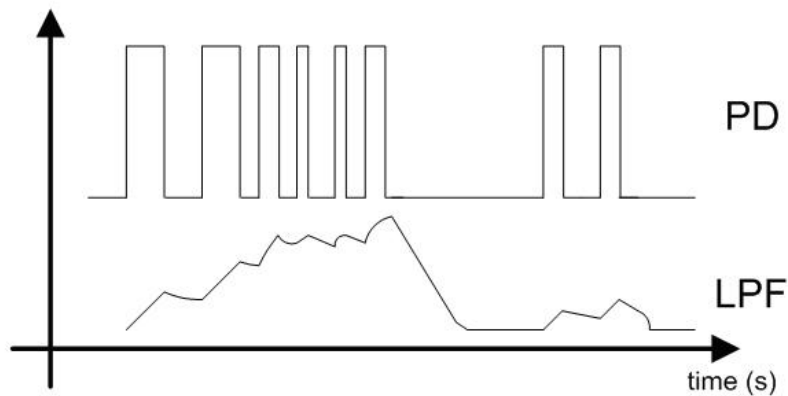


FIGURE 10.6: PD LPF output waveform typical examples

10.2.4 Loop Dynamics

Based on the above, the PLL can be redrawn as in figure 10.7.

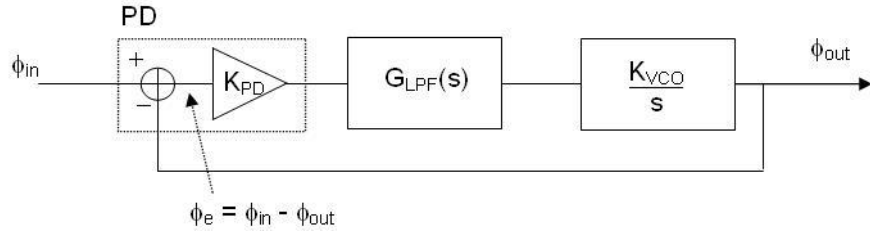


FIGURE 10.7: Basic PLL Model

The relationship between the input and output phase becomes,

$$\frac{\phi_{OUT}(s)}{\phi_{IN}(s)} = H(s) = \frac{K_{PD}K_{VCO}G_{LPF}(s)}{s + K_{PD}K_{VCO}G_{LPF}(s)} \quad (10.7)$$

Substituting and rearranging (bear in mind 10.6):

$$H(s) = \frac{K_{PD}K_{VCO}}{\frac{s^2}{\omega_{LPF}} + s + K_{PD}K_{VCO}} \quad (10.8)$$

Which may be re-written as,

$$H(s) = \frac{K_{PD}K_{VCO}\omega_{LPF}}{s^2 + s\omega_{LPF} + K_{PD}K_{VCO}\omega_{LPF}} \quad (10.9)$$

From the previous equation we see that the PLL is a second order system with the poles dictated by the LPF and the VCO. From general control theory, the denominator of equation 10.8 can take the form:

$$s^2 + 2\zeta\omega_n s + \omega_n^2 \quad (10.10)$$

Where ζ is the damping factor and ω_n is the natural frequency of the system.

From 10.9 and 10.10,

$$2\zeta\omega_n = \omega_{LPF} \quad (10.11)$$

and,

$$\omega_n^2 = \omega_{LPF} K_{PD} K_{VCO} \quad (10.12)$$

In practical terms, ζ is a crucial factor in the operation of the PLL. The quantity ζ denotes the degree of damping within the PLL. Consider the circuit shown in figure 10.8a and assume that both VCO's are of the same 'model'. If a step input is applied to VCO_A , then the V_c response will be directly related to ζ (illustrated in figure 10.8b).

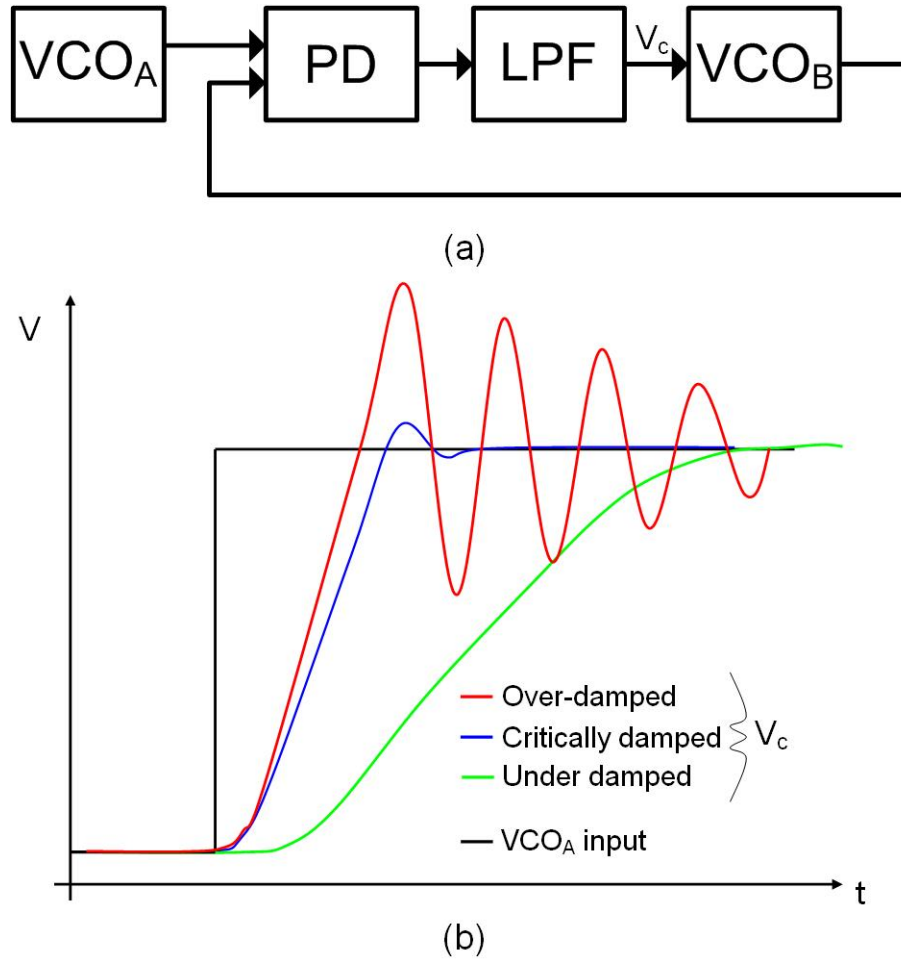


FIGURE 10.8: (a) PLL model used for ζ analysis, (b) ζ value effects on V_c

If ζ (equation 10.11) is too high, then the filter's cut off frequency is close to the natural running frequency of the VCO, and so the resulting response is oscillatory. Should ζ now be too low, then the cut off frequency is also extremely low so that the response now becomes under-damped hence the loop takes longer to lock. Ideally for the loop to be critically damped, ζ must be between 0.5 and 1. [122] [127] [129] [130].

10.2.5 Summary

The PLL part of the wireless unit will be set up as in figure 10.9.

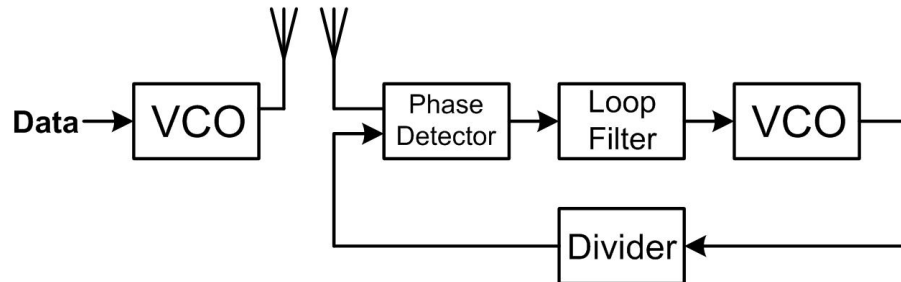


FIGURE 10.9: PLL Concept-Based Radio

Here the data that is fed in to the transmitter's VCO will be a square wave (the output of a ADC). This knowledge can be used to design a more efficient PLL. Whereas before, it was said that it would be optimal if ζ is between 0.5 and 1, now there is a different case. Looking closely at figure 10.8b, it can be seen that as long as the second lobe (the one which drops) does not fall further than half the V_{dd} then the designer can use two inverters to fix the signal to a high. By doing this the designer is free to design the PLL with out any constraints mentioned.

10.3 Summary

A receiver illustrated in figure 10.10 has been designed for the transmitter unit previously described. Note that the multi-tapped VCRO described here is of the same model as that within the transmitter block. When the signal arrives at the antenna and is pre-processed by the amplifier, the frequency received maybe slightly modified. That is, the 13.553MHz - 13.567MHz frequencies maybe jointly shifted left or right (in the frequency spectrum). These errors can be practically overcome during the testing phase by means of the tuning of the 'DC input' of the multi-tapped VCRO.

Figure 10.11 illustrates the entire wireless unit combining both the transmitter and the receiver circuit.

The VCRO in the transmitter works off an FSK transmission method. The receiver is essentially a PLL which has the same model of VCRO to that of the transmitter's. The VCRO in the receiver is modified to match the transmitter's frequency. If the two

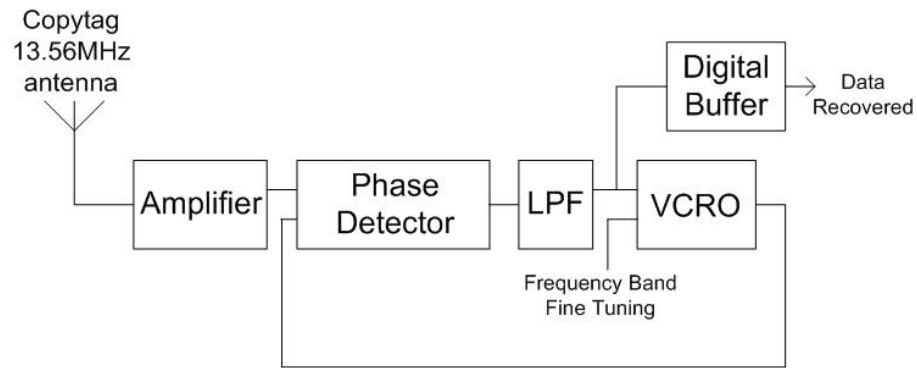


FIGURE 10.10: PLL-based Receiver

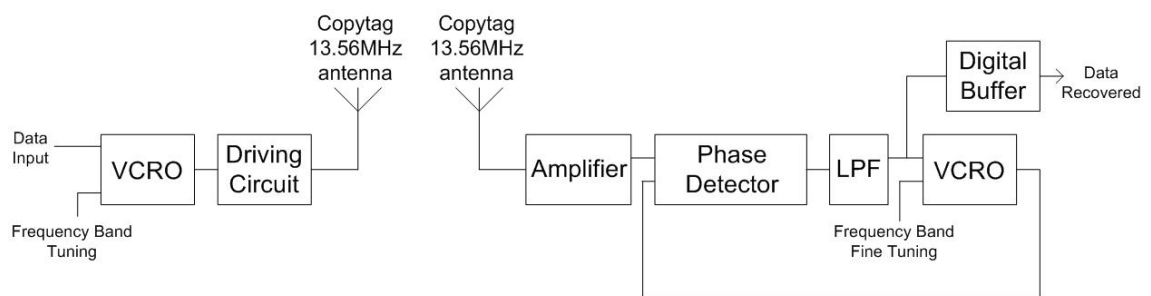


FIGURE 10.11: The proposed short range radio

VCRO's have the same output, then it is fair to state that they have the same input. The receiver then buffers and outputs the transmitters' VCRO input thereby recovering the data signal.

Chapter 11

Simulated and Measured Results of the proposed Radio Link Blocks

The radio system was explained and analyzed in the previous two chapters in full. The full radio system is shown in figure 11.1. The Copytag 13.56MHz antenna model, which was S-characterized in full in the previous chapter, was incorporated in the simulated radio link. In other words the simulation of the radio link includes not only the realistic transistor models provided by the foundry but also the S-parameters of the antenna link extracted experimentally.

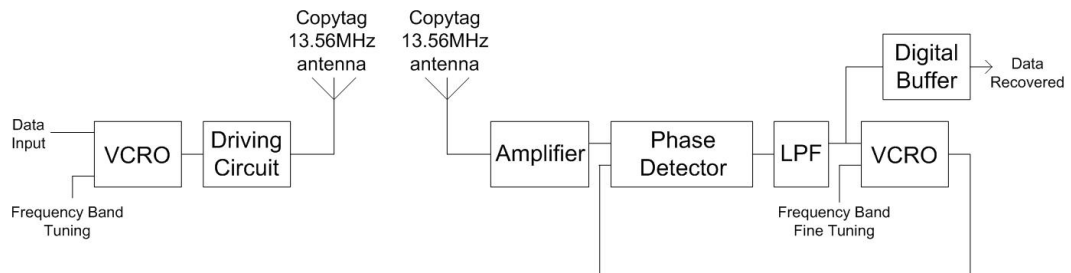


FIGURE 11.1: Block-level schematic of the simulated 13.56MHz radio

This chapter displays the transistor level circuits as well as the simulated and measured results. Cadence spectre was utilized for simulation purposes with the designed operation being confirmed by two different technologies ($0.8\mu\text{m}$ and $0.35\mu\text{m}$).

11.1 Simulated Results

The transmitter's multi-tapped VCRO circuit is displayed in figure 11.2. As explained in previous chapters, the multitapping allows signal cancellation to occur. The frequency range output of the VCRO is 13.567 and 13.553MHz respectively. As the input (DC_1) of the multi-tapped transistors varies from 0 to 2v the frequency varies from 16.584-16.56MHz to 10.255-10.246MHz respectively.

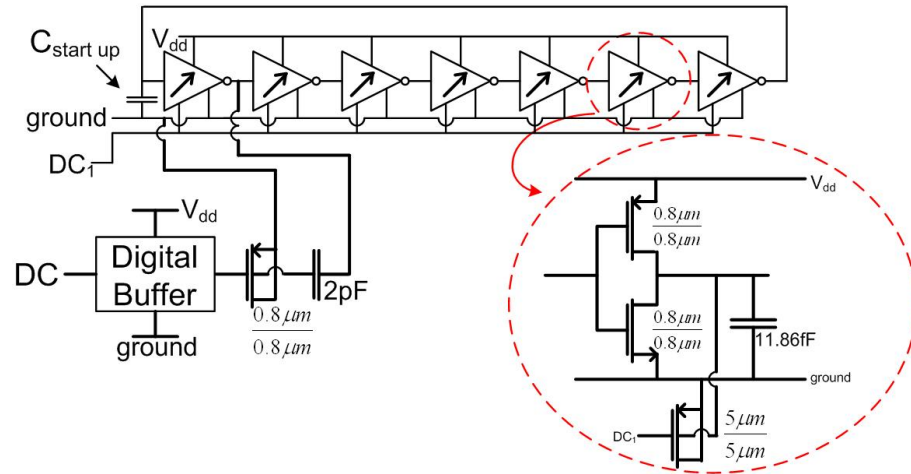


FIGURE 11.2: The Transmitter's multi-tapped VCRO Circuit.

The antenna driver circuit consists of a smoothing capacitor network with a current driving PMOS transistor in order to obtain a sine wave. The simulated circuit is shown in figure 11.3.

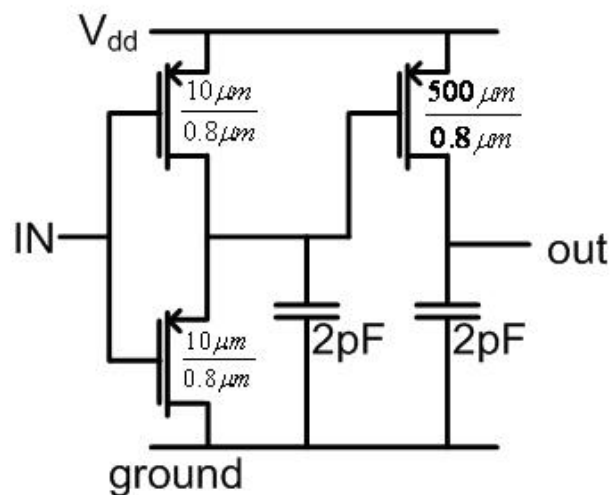


FIGURE 11.3: Antenna Driver Circuit

The Receiver's recovery circuit consists of a number of cascaded common source single ended amplifiers separated by DC blocking capacitors. The full circuit is depicted in figure 11.4.

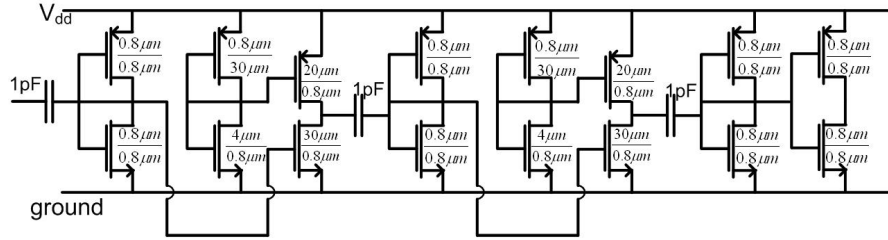


FIGURE 11.4: Recovery circuit

The receiver makes use of a D-Flip-Flop (dff) to mitigate any non-linearity after the amplification of the previous stage (figure 11.1). By using the dff, the waveform received by the antenna is 'hardened' (figure 11.5). As the frequency here is divided by two (by the dff), the same must be done subsequently at the receivers VCRO. The dff is shown in figure 11.5.

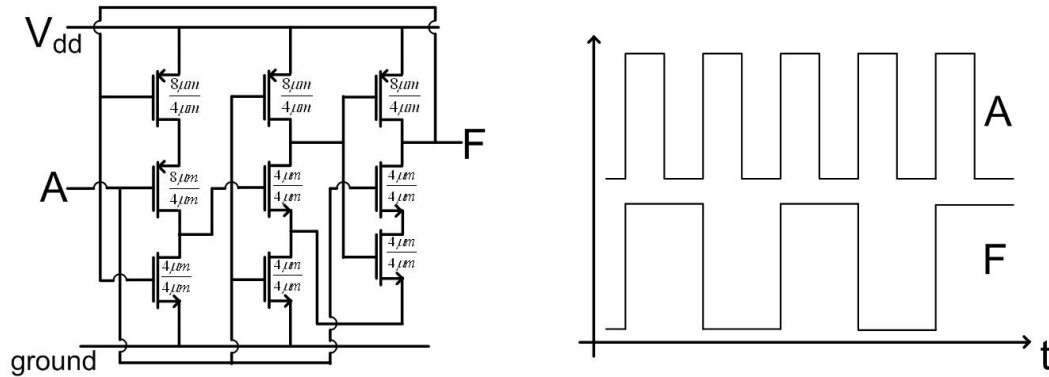


FIGURE 11.5: (a) D-Flip-Flop Circuit, (b) D-Flip-Flop Hardening Function

The Phase Detector is realized by means of an XOR gate. The XOR gate is made up from standard logic gates shown in figure 11.6.

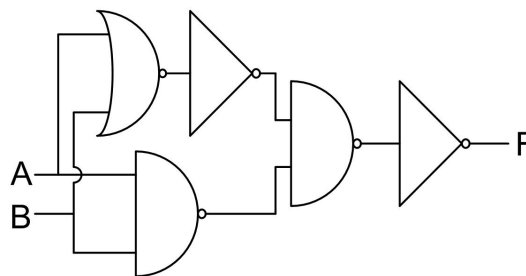


FIGURE 11.6: Phase Detector XOR

Due to the frequency difference at the inputs of the XOR gate, its output spikes for very short amounts of time. As the LPF is passive, the phase gain (K_{LPF} depicted by the positive gradient of figure 10.6) of the XOR gate is of extreme importance.

Figure 11.7a shows an example of the output of the XOR phase detector. Figure 11.7b illustrates the output of the LPF under standard conditions. Clearly due to K_{LPF} being insufficient, a charge pump (SSweak) is required to provide sufficient gain (figure 11.7c).

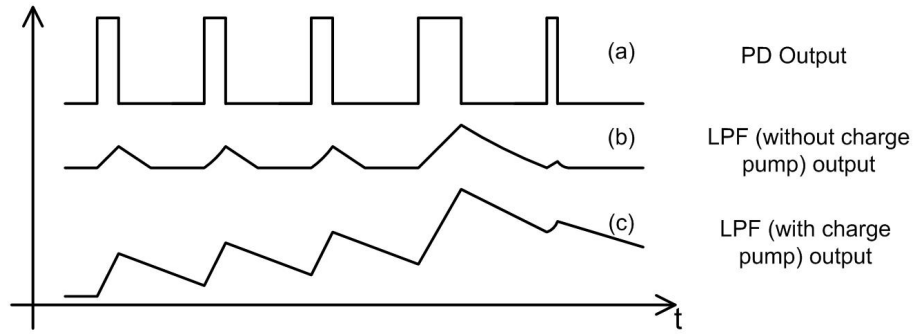


FIGURE 11.7: Waveforms of the LPF output with and without a Charge Pump

The charge pump is based on a simple comparator circuit that amplifies the applied voltage above a preset level (11.8a). The LPF is shown in figure 11.8b, it is based upon a passive RC design. However as on-chip resistors can be hard to implement, due to this, the resistors replaced with MOS transistors.

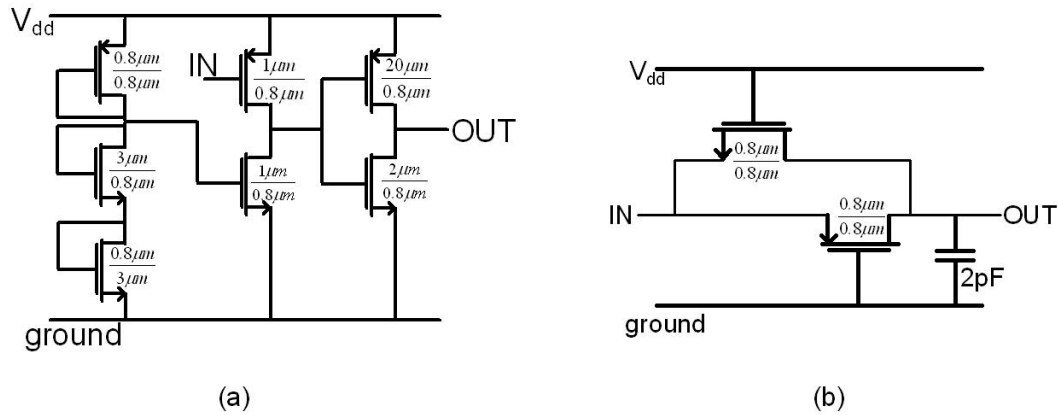


FIGURE 11.8: Charge Pump and RC LPF

The full radio circuit shown in figure 11.1 was simulated successfully indicative confirming results plotted in figure 11.9. The receiver takes an initial $25\mu s$ as a ‘turn on’ start up time. However, after that, the acquisition time is approximately $2\mu s$. (Where with the term ‘acquisition time’ we refer to the time needed for when the output to change in response to an input change).

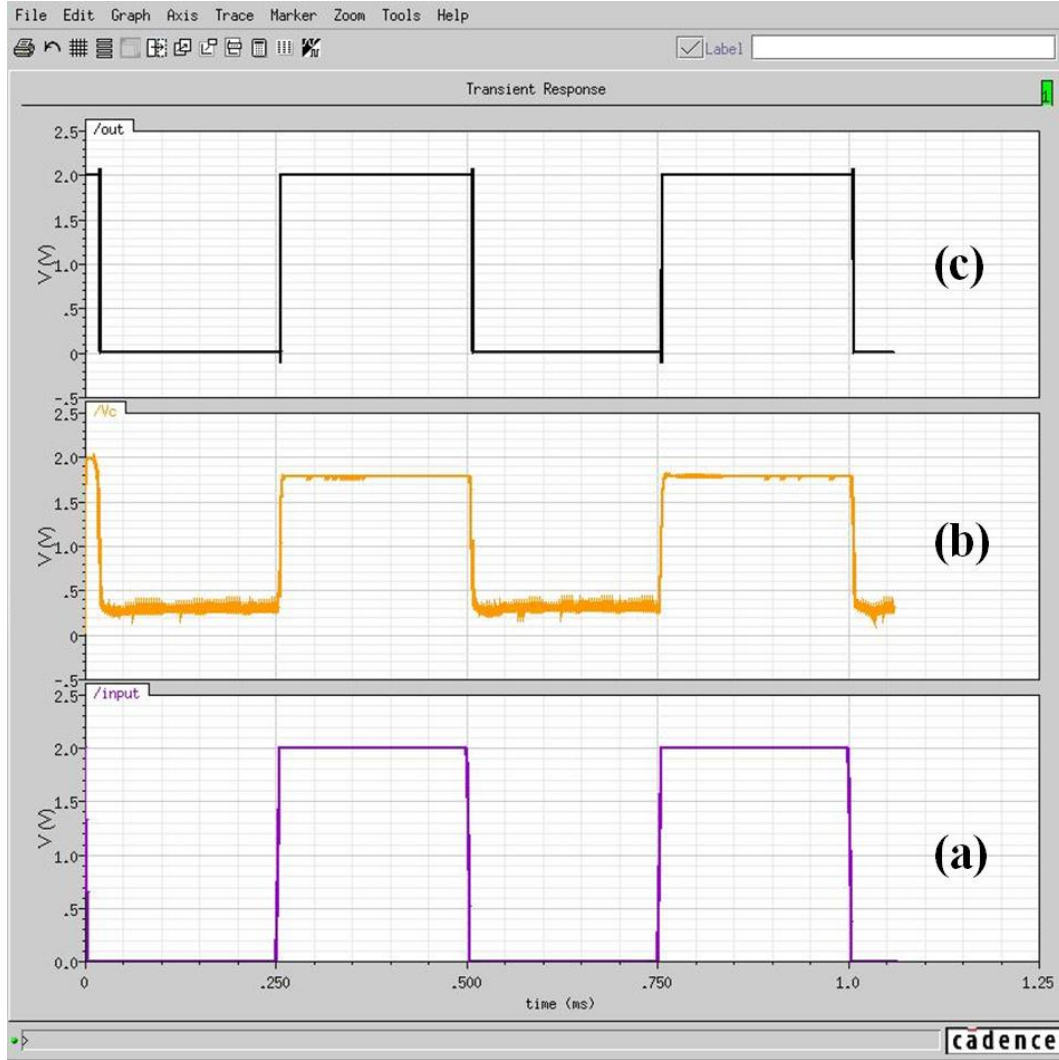


FIGURE 11.9: Simulated (a) Input, (b) Control Voltage and (c) Output ($V_{CO_{receiver}}$ input) of the Full Wireless System for a Range of 2.5cm

11.2 Measured Results

The multi-tapped oscillator was initially tested in the lab. The DC_1 voltage was varied and the output frequency was recorded. A number of chips were tested. Their combined measured results are displayed in figure 11.10. The chip-to-chip variations are relatively small for 8/11 of the prototype IC's. Also observe the fairly good linear dependence of the recorded frequency of oscillation with the DC_1 input voltage.

Figure 11.11 shows the DC_1 voltage required to obtain the desired 13.56MHz frequency range for different chips.

Figure 11.12a illustrates the experimental setup in order to test the transmitters operation. Figure 11.12b displays a transient response recorded from the oscillator for a

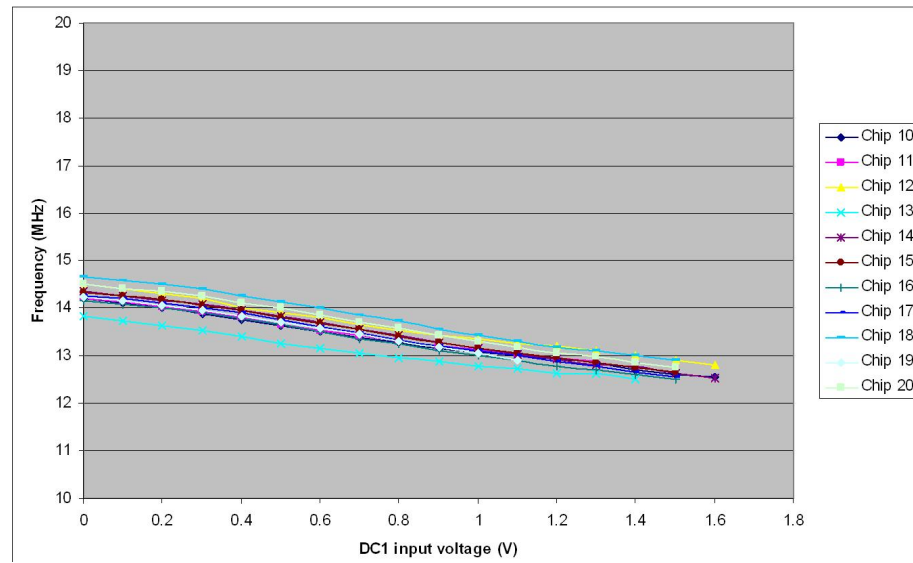


FIGURE 11.10: Inter-chip tuning and variation of the multitapping VCRO transmitter as a function of the input voltage DC_1

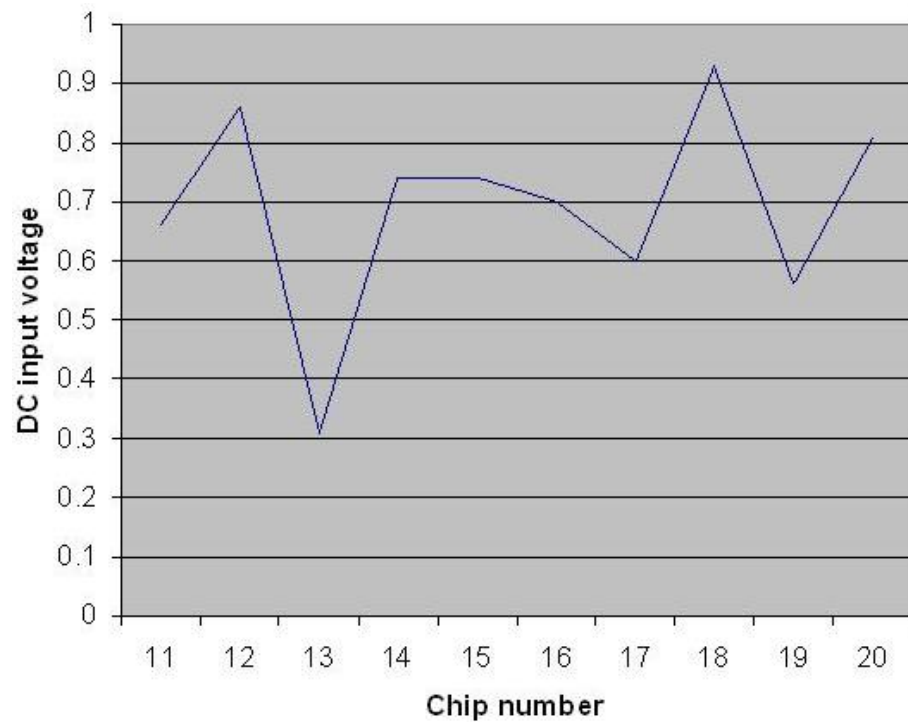
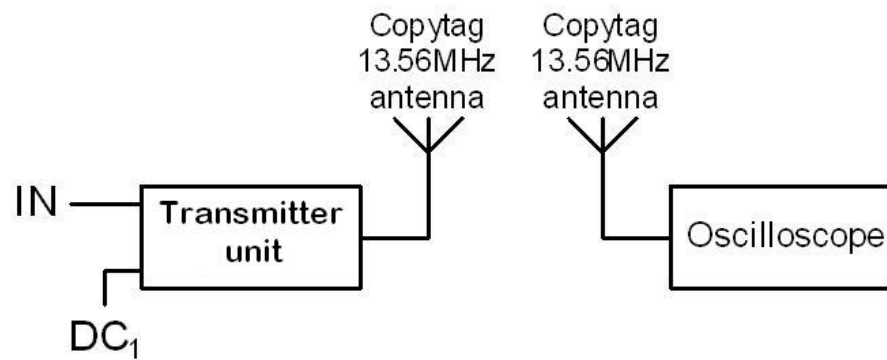


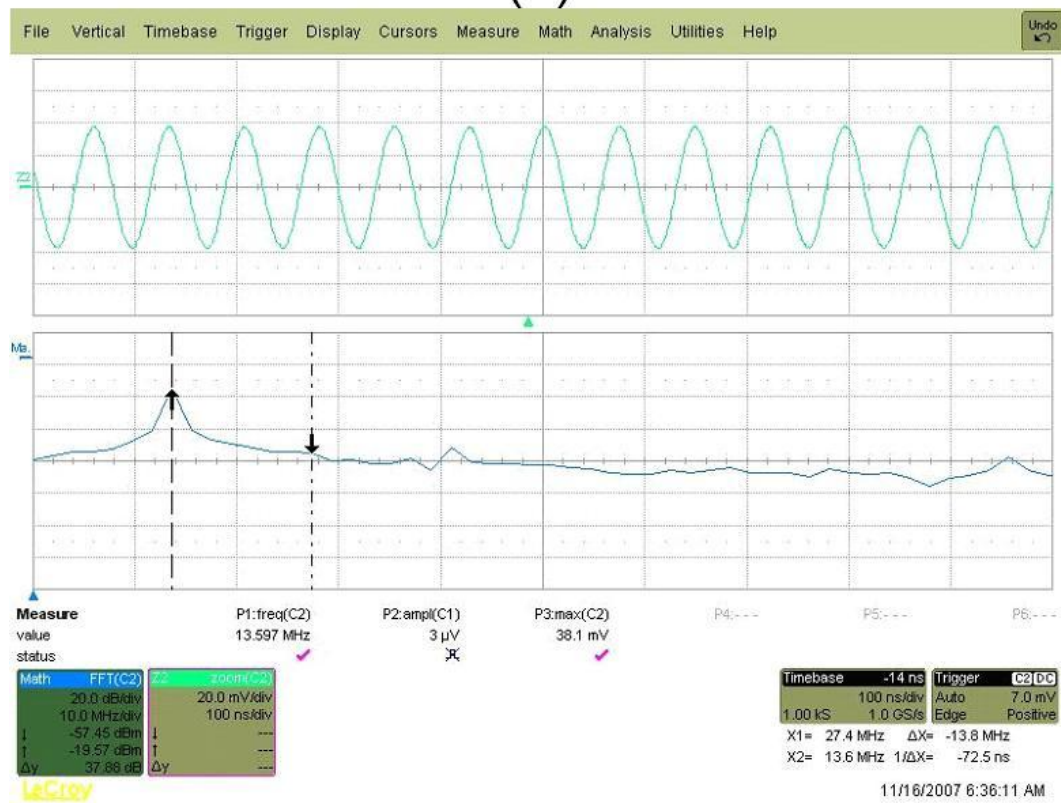
FIGURE 11.11: DC_1 input voltage to needed to achieve the correct 13.56MHz frequency

range of 2cm.

Finally figure 11.13 shows the received voltage levels.



(a)



(b)

FIGURE 11.12: Transmitters' (a) practical setup, (b) transient response with the antenna placed 2cm apart

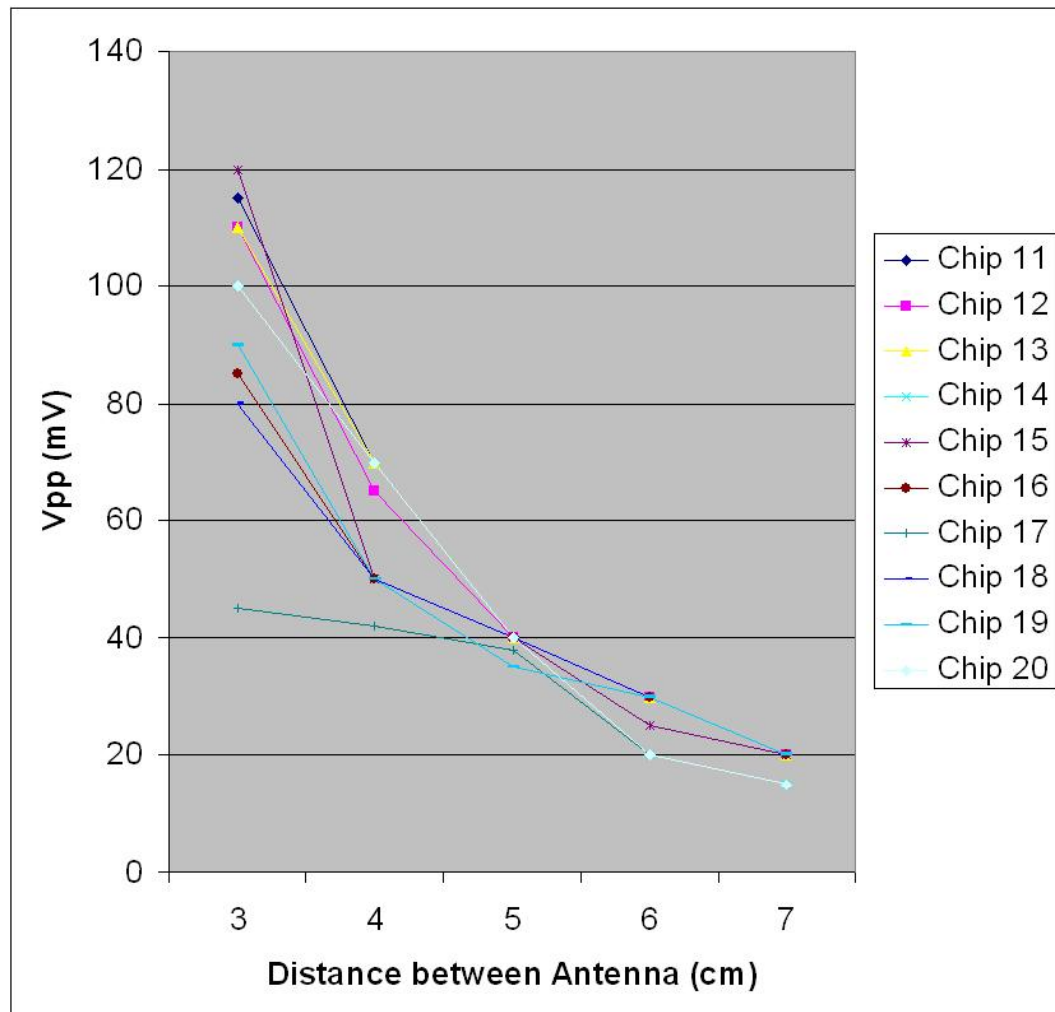


FIGURE 11.13: $V_{peak-to-peak}$ vs distance, for the practical setup of the circuit illustrated in figure 11.12

11.3 Conclusion

The radio block was designed, analyzed simulated and fabricated. Simulation results of the transmitter and receiver blocks at 2.5cm apart were successfully presented. A novel multi-tapped voltage controlled oscillator was introduced and successfully tested in the laboratory. The multi-tapping requires calibration post-fabrication in order to overcome any process or manufacturing errors. The transmitter was connected to antenna A while antenna B was connected to the oscilloscope.

The VCRO (figure 11.14) gave a 20KHz frequency variation when the input *DC* data input was varied, while the multi-tapped input (DC_1) allowing a frequency range covering 12.5MHz to 14.5MHz (illustrated in figure 11.15)

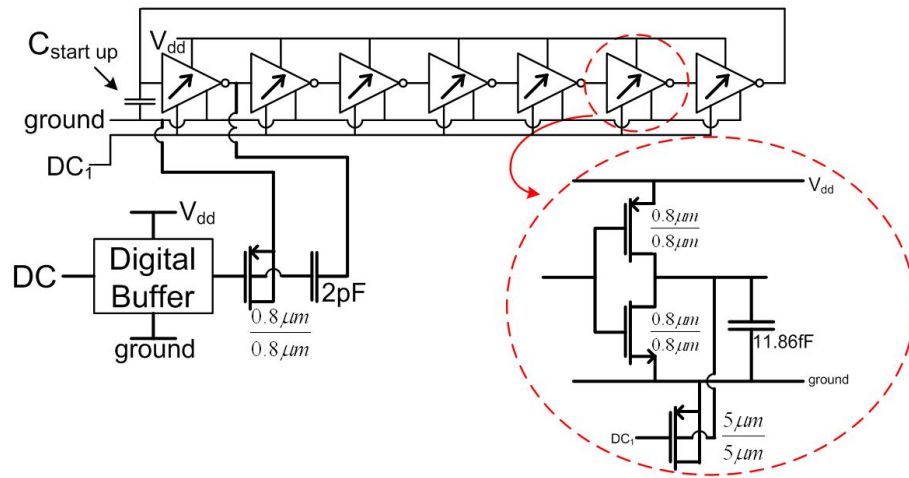


FIGURE 11.14: The Transmitter's Multi-Tapped VCRO Circuit.

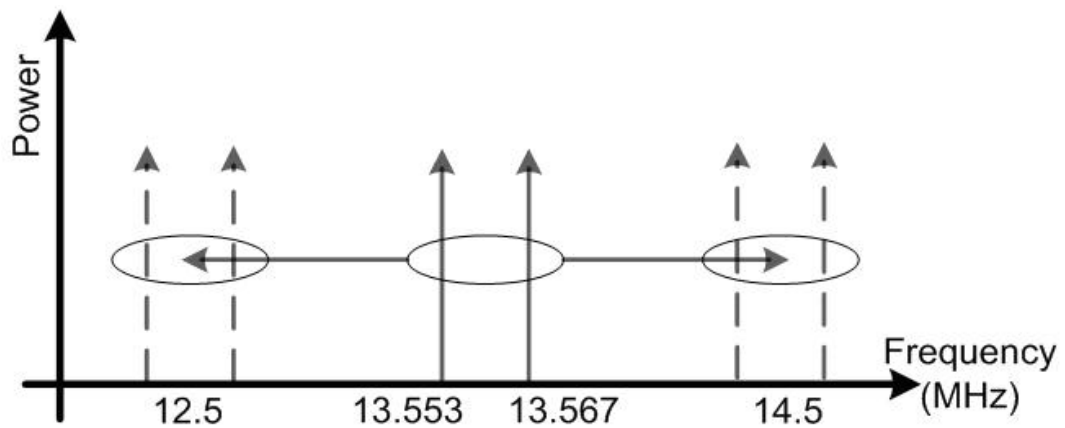


FIGURE 11.15: Output frequency of the circuit in figure 11.14 when subjected to a variation at the data and frequency tuning input

However the operation of the radio could not be verified as the receiver did not operate as desired. This maybe due to

- The frequency range being too small for the PLL to lock
- Amplifier block not functioning as desired
- Charge pump comparator not providing enough power to drive through the loop filter
- DC blocking capacitors not large enough to block the DC component of the input signal
- The bond wire connection from the die to pin of the chip is inductive. This inductance modifies the high frequency signal being applied to the antenna, hence forces the VCO frequency outside the lock range.

Part IV

Conclusion

Chapter 12

Conclusion

Stem cells are predicted to become the medical breakthrough of the future. With a greater understanding of the transformation that stem cells go through when transforming into ‘specialized’ cell, they maybe manipulated to replenish dead cells within the body. This would provide a cure to such conditions as Parkinson’s disease. In order to get a better understanding of stem cells they will be placed within an incubator (to be isolated from external stimuli) - illustrated in figure 12.1 - and their reactions monitored to different chemical stimuli, to do this a potentiostat is employed. The potentiostat outputs a current which is a measure of the changes within the electrolyte. However as this current is too small to be measured directly, some interface is required. As the solution is within an incubator, a wireless unit is required.



FIGURE 12.1: Incubator

12.1 Sinh Current Amplifier

Figure 12.2 illustrates the standard laboratory setup of a three-electrode-potentiostat. The potentiostat provides a current output which is driven into an current amplifier which provides two functions. 1) to provide a virtual ground node for current to be driven into and 2) to provide sufficient gain for the working electrode current to be displayed as an output.

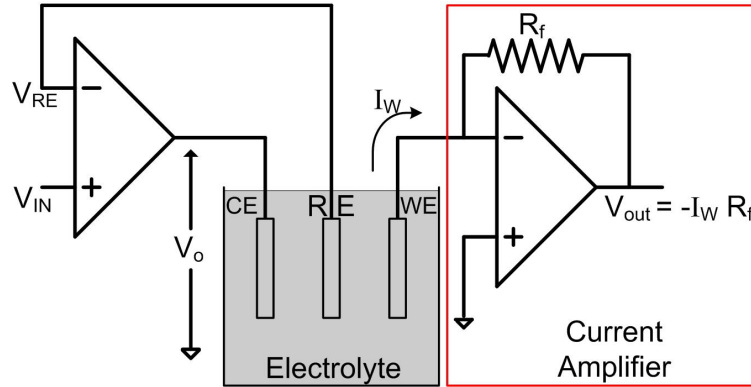


FIGURE 12.2: Traditional three electrode potentiostat theoretical measurement [38]

Figure 12.3 depicts the novel setup of the potentiostat. The current amplifying op-amp is replaced with a current conveyor (CCII+) and the Sinh Current Amplifier. The current conveyor provides a virtual ground node for current to be sunk to. The Sinh Current Amplifier allows sufficient gain for the working electrode current to be displayed.

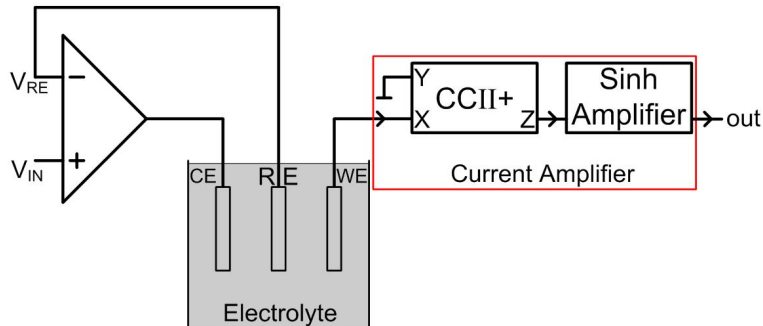


FIGURE 12.3: Proposed three electrode potentiostat theoretical measurement

The current conveyor (illustrated in figure 12.4) is constructed from a dual rail class AB current conveyor which provides a low impedance virtual ground node at its input, and mirrors the input to the output.

The Sinh Current Amplifier (illustrated in figure 12.5) is based on a novel weak inversion synthesis technique. It operates in two stages, initially an input current is converted

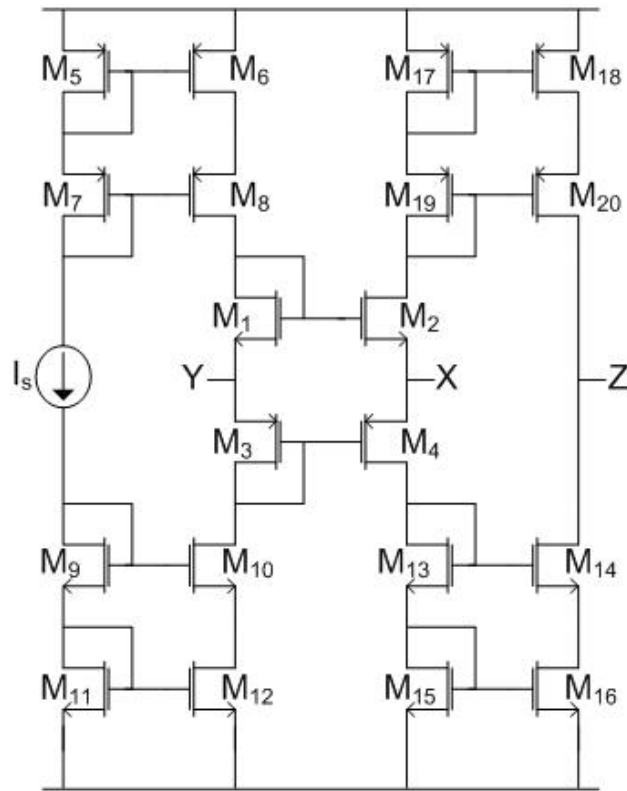


FIGURE 12.4: Class AB-Dual Rail-Current Conveyor

to an intermediate sinh voltage via a bias current of I_0 . Secondly the process is reversed with the sinh voltage be converted to an output current via bias I_1 . The gain of the circuit is equivalent to the ratio of the currents I_1 and I_0 .

The operation of the current amplifier designed was designed, simulated, fabricated and tested in both the $0.8\mu\text{m}$ and $0.35\mu\text{m}$ AMS processes. The results are listed in table 12.1. The operation was also practically verified via laboratory experiment where the current amplifier acted as the interface between a $125\mu\text{m}$ platinum working electrode immersed in a 0.2mM of Ferrocene in an aqueous buffer with 0.15NaCl as the supporting electrolyte.

The Sinh Current Amplifier has the potential to replace op-amp-based current amplification solutions. The Sinh Current Amplifier is characterized by reduced power supply levels, generally lower power consumption and the fact that it can operate open-loop and provide current amplification in a resistorless manner. Together with a short-range radio it could provide lab-on-chip monitoring solutions. Furthermore its translates to a bipolar design with the potential of higher speed operation is diverse.

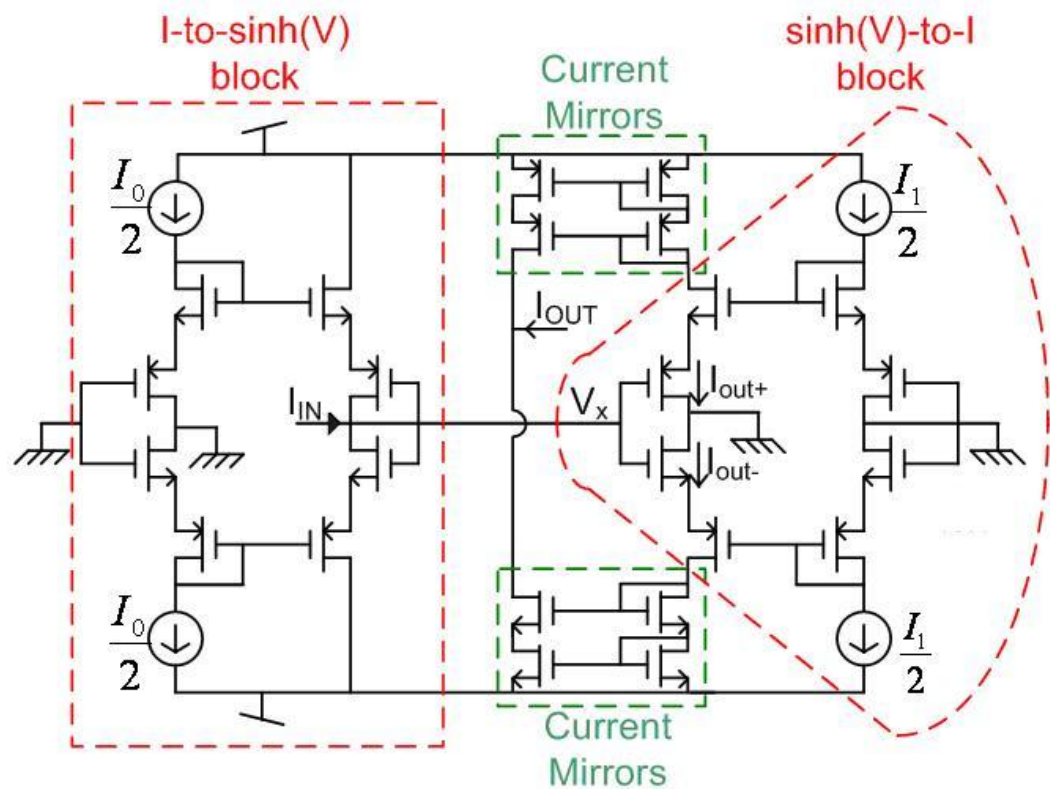


FIGURE 12.5: Sinh Class AB Current Amplifier

Gain	x10	x100	x1000	x100
Process	0.8μm AMS			0.35μm AMS
Power Supply	±4V	±4V	±4V	±4V
Power Consumption	0.88μW	4μW	44μW	95μW
Size	1300μ x 1200μm			1500μ x 900μm
3dB Point	160Hz			400Hz
Input referred noise integrated over a bandwidth of 1KHz	2pA			2pA
Current Range value for which deviations from nominal gain are below 1%	100p-6n	100p-2.5n	100p-2.5n	3n-16n

TABLE 12.1: Sinh Current Amplifier Specifications

12.2 Radio

The Sinh Current Amplifier of the previous section is designed to be used within an incubator while monitoring a cell culture. In order for the culture to be completely isolated from external stimuli, the incubator must be completely sealed. Hence a wireless unit is required. Due to the dimension of the incubator wall, and the low data rate, a low power Phase Locked Loop based radio was designed. The VCRO based transmitter and PLL based receiver are illustrated in figure 12.6

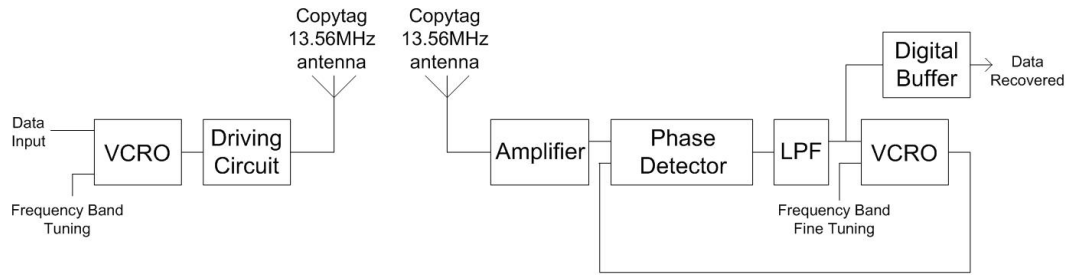


FIGURE 12.6: Block-level schematic of the simulated 13.56MHz radio

The VCRO has two inputs, one for data and the second to provide a correction system which overcomes any process and manufacturing errors. The transmitter may then be tuned to ensure that it is within the 13.56MHz ISM frequency band by performing post-fabrication calibration. The transmitted consisted of the VCRO which provides an output frequency of 13.567MHz and 13.553MHz for a data input of logic 1 and 0 respectively. The 13.56MHz signal is then amplified and transmitted via a COPYTAG 13.56MHz antenna.

At the receiver end, the signal is amplified and passed to the PLL. The PLL contains a $VCO_{receiver}$ of similar ‘model’ to that of the transmitters. By forcing the output of the $VCO_{receiver}$ and the received signal to be the same, then the input’s to both the $VCO_{transmitter}$ and $VCO_{receiver}$ must be the same - the data signal has been recovered.

The proposed system was designed and simulated and the operation verified in the $0.35\mu\text{m}$ and $0.8\mu\text{m}$ AMS processes. The transmitter was tested with the VCRO frequency tuning input verified, providing a 20KHz (13.553MHz to 13.573MHz) spread to a data input variation whereas the Frequency Band Tuning input varied the output frequency output from 12.5MHz to 14.5MHz. This allowed any process and manufacturing errors to be overcome.

12.3 Summary

The combination of the Sinh Current Amplifier and the Wireless Radio has the potential to form the basis for a complete laboratory on a (3mm by 3mm) chip. By the addition of an intermediate ADC (which may also be placed on-chip), a totally wireless sensor node can be realized. This wireless sensor may then be mounted on the head of a sensor electrode (submerged in a solution) and provide real time physiological monitoring of a cell culture. The Sinh Current Amplifier was implemented in both the 0.35 and 0.8 μ m technologies, each of which had its own advantages. The 0.35 μ m version proved to be of higher bandwidth, while the 0.8 μ m versions was of lower power consumption. The wireless block's transmitter unit's functionality was verified by means of measured results. However, the wireless block's receiver units' total functionality was not proven with measured results. On the other hand, the ability to control the multitapped voltage controlled ring oscillator's frequency range was indispensable when ensuring that the transmitter operated to be within the 13.56MHz range.

Chapter 13

Appendix A: Jitter Noise [121]

In order to analyze the noise in a ring oscillator, the first step is to consider the integral of the random noise bounded by time t_d . Consider the current noise signal in:

$$V_n = \frac{1}{C} \int_0^{t_d} i_n dt \quad (13.1)$$

With V_n now denoting the voltage noise signal appearing at the integrating node.

To find the spectral density of the samples of integrated noise over time, we can perform the analysis over a fixed unit time window w_{t_d} and also assume that the current noise is uniform over time. Then, [121]

$$V_n(\tau) = \frac{1}{C} \int_0^\infty i_n(\tau) w_{t_d}(t - \tau) d\tau \quad (13.2)$$

Relation 13.2 codifies the convolution of the signals $i_n(t)$ and W_{t_d} :

$$V_n(t) = \frac{1}{C} [i_n(t) * w_{t_d}(t)] \quad (13.3)$$

Applying Laplace transforms,

$$V_n(f) = \frac{1}{C} I_n(f) W_{t_d}(f) \quad (13.4)$$

Consequently, for the power spectral density (PSD) $S_{v_n}(t)$ will hold cite:

$$PSD = S_{v_n}(f) = \frac{1}{C^2} |W_{t_d}(f)|^2 S_{i_n}(f) \quad (13.5)$$

Since the mean square of value of the integrated noise at the end of the integration window is given by 13.6,

$$V_n^2(f) = \int_0^\infty S_{v_n}(f) df \quad (13.6)$$

or bearing in mind 13.5, then:

$$V_n^2(f) = \frac{1}{C^2} \int_0^\infty S_{i_n}(f) |W_{t_d}(f)|^2 df \quad (13.7)$$

Assuming that $W_{t_d}(f)$ has a frequency dependence of the form $\frac{\sin(\pi t_d f)}{\pi f}$, then

$$\int_0^\infty |W_{t_d}(f)|^2 df = \int_0^\infty \left| t_d \frac{\sin(\pi t_d f)}{\pi t_d f} \right|^2 df = t_d \text{sinc}(f t_d) \quad (13.8)$$

Let,

$$\pi t_d f = x \pi t_d = \frac{dx}{df} \quad (13.9)$$

Then re-writing 13.8 gives:

$$\int_0^\infty |W_{t_d}(f)|^2 df = \frac{1}{\pi t_d} \int \left(t_d^2 \frac{\sin^2(x)}{x^2} \right) \quad (13.10)$$

Reducing then gives,

$$\int_0^\infty |W_{t_d}(f)|^2 df = \frac{t_d}{\pi} \int \left(\frac{\sin^2(x)}{x^2} \right) \quad (13.11)$$

$$\int_0^\infty |W_{t_d}(f)|^2 df = \frac{t_d}{\pi} \frac{\pi}{2} \quad (13.12)$$

$$\int_0^\infty |W_{t_d}(f)|^2 df = \frac{t_d}{2} \quad (13.13)$$

Substituting equation 13.13 into 13.7, then leads to 13.14.

$$V_n^2(f) = \frac{t_d}{2C^2} \int_0^\infty S_{i_n}(f) \quad (13.14)$$

Therefore the voltage noise depends on the current PSD multiplied by a factor bounded by a time window. The greater the time window, the greater the noise.

Looking specifically at the ring oscillator high-to-low transition state (t_{dl}), then any noise will change the time of crossing the $V_{dd}/2$ point. The crossing will be given by the ‘ideal voltage plus the noise voltage’ represented in equation 13.15.

$$\int_0^{t_{dl}} \frac{I_N + i_{nN}}{C} dt = \frac{V_{DD}}{2} \quad (13.15)$$

Assuming that an ideal step input (from logic ‘0’ to ‘1’) is applied to the input of an inverter, t_{dl} is the time taken for the output of the inverter to reach $V_{dd}/2$.

$$t_{dl} = \frac{CV_{DD}}{2I_N} \quad (13.16)$$

The mean square value is defined as in equation 13.17

$$\sigma^2 = \frac{1}{SNR^2} = \left(\frac{Noise}{Ideal} \right)^2 \quad (13.17)$$

Therefore for the $\sigma_{t_{dl}}^2$:

$$\sigma_{t_{dl}}^2 = \left(\frac{\int_0^{t_{DL}} i_{nN} dt}{I_N} \right)^2 \quad (13.18)$$

Combining equations 13.15 and 13.16, leads to:

$$t_{dl} = \int_0^{t_{DL}} \left(\frac{I_N + i_{nN}}{C} dt \right) \frac{C}{I_N} \quad (13.19)$$

$$t_{dl} = \left[\int_0^{t_{DL}} \left(\frac{I_N}{C} dt \right) + \int_0^{t_{DL}} \left(\frac{i_{nN}}{C} dt \right) \right] \frac{C}{I_N} \quad (13.20)$$

$$t_{dl} = \left[\int_0^{t_{DL}} (I_N dt) + \int_0^{t_{DL}} (i_{nN} dt) \right] \frac{1}{I_N} \quad (13.21)$$

$$t_{dl} = \left[\int_0^{t_{DL}} (1 dt) + \int_0^{t_{DL}} \left(\frac{i_{nN}}{I_N} dt \right) \right] \quad (13.22)$$

$$t_{dl} = \int \left(\omega_{td}(t-x) + \frac{1}{I_N} \int i_n \omega_{td}(t-x) \right) \quad (13.23)$$

$$t_{dl} = \frac{1}{I_N^2} W_{td}(f)^2 S_{in}(f) \quad (13.24)$$

Therefore the spectral density of t_{dn} can be written as:

$$S_{t_{dl}} = \frac{t_d^2}{I_N^2} \text{sinc}^2(ft_d) S_{i_n}(t) \quad (13.25)$$

With the mean square value being:

$$\sigma^2 = \int_0^\infty S_{t_{dl}} df = \int_0^\infty \frac{t_{dl}^2}{I_N^2} \text{sinc}^2(ft_{dl}) S_{i_{nN}} \quad (13.26)$$

$$\sigma^2 = \int_0^\infty S_{t_{dl}} df = \frac{S_{i_{nN}}}{I_N^2} \int_0^\infty t_{dn}^2 \text{sinc}^2(ft_{dl}) \quad (13.27)$$

$$\sigma^2 = \int_0^\infty S_{t_{dl}} df = \frac{S_{i_{nN}}}{I_N^2} \int_0^\infty |W_{td}(f)|^2 df \quad (13.28)$$

$$\sigma^2 = \int_0^\infty S_{t_{dl}} df = \frac{S_{i_{nN}}}{I_N^2} \frac{t_{dl}}{2} \quad (13.29)$$

Since the spectral noise of a FET is given by 13.30, then jitter may be written as in 13.31.

$$S_{i_{nN}} = 8kT\gamma_N \frac{I_{DNsat}}{V_{DD} - V_{tN}} \quad (13.30)$$

$$\sigma_{t_{dl}} = \frac{2kT\gamma_N CV_{DD}}{I_N^2(V_{DD} - V_{tN})} \quad (13.31)$$

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