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Power Converter Design for HVDC Applications

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Declaration

I herewith declare that the work produced here was either conducted by myself or where collaborative work occurred, it is indicated. All information has been attributed to its original source. This thesis has not previously been presented in identical or similar form to any other British or foreign examination board.

This work was conducted from October 2012 to July 2016 under the supervision of Prof. Tim C. Green at Imperial College London.

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Abstract

This thesis investigates the design of modular voltage source converters for High Voltage Direct Current (HVDC) applications. The first half of the thesis focuses on the design of existing multilevel HVDC technology. A design methodology for sizing modular converters for a given grid code specification, and with given design constraints in terms of peak sub-module voltage rating and capacitor size, is developed and used as the basis of comparing converter designs. Results show that the half-bridge MMC requires an energy storage in the region of 35 kJ/MVA in order to achieve a good balance between sub-module capacitor size, and required number of sub-modules.

The design of the Hybrid MMC, which combines half- and full-bridge sub-modules in the design in order to achieve DC fault tolerance, is then investigated using the same design methodology, an advantage of which is that the optimum modulation index can be determined, rather than assumed. Results show that the highest efficiencies may be achievable if the converter is operated at a modulation index of 1.2. The power-loss and thermal properties of several converters are then analysed. The Alternate Arm Converter and over-modulating Hybrid MMC show the greatest efficiencies, though the AAC suffers from relatively high junction temperatures within its director switches.

The potential of designing overload capability into MMCs, to enable them to provide system support services such as frequency response is then investigated. Results show 30% overload ratings may be achievable with only a 10% required increase in the number of sub-modules within the converter. System studies show that significant response improvements to the AC

system can be made even if the converters need to be dynamically rated to prevent excessive junction temperatures being reached.

The second half of this thesis focuses on a brand new multilevel thyristor-augmented structure called a power-group, which has the potential to allow voltage source converters that are tolerant to faults on both the AC and DC network to be constructed, while having efficiencies similar to those achievable with Current Source Converter (CSC) technology. Results show that this is possible while also retaining high quality current waveforms and independent control of real and reactive power.

Results throughout the thesis are backed up by a combination of simulation and experimental work using a lab-scale multilevel converter that was constructed during the project.

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1 Introduction

Historically the main use of High Voltage Direct Current (HVDC) systems has been the bulk transmission of power over long distances and inter-connecting neighbouring asynchronous AC systems. Recently new applications have been found, most prominently the interconnection of large offshore wind-farms to onshore grids [1]. HVDC stations are significantly more expensive that the AC equivalent transformer. However as the transmission distance increases, HVDC becomes the more economic choice over AC due to its lower incremental cost with distance. This lower incremental cost is due to the lower losses within a DC transmission line or cable, a reduced conductor size requirement, as well as reduced right of way requirements in transmission corridors. This is illustrated in Fig. 1.1.



Figure 1.1: AC and DC transmission cost versus length for AC and DC systems

For overhead lines this becomes true at transmission at a distance of approximately 500-800 km, depending on factors such as power rating, land cost and electricity prices, reducing to around 50-150 km when considering cable systems due to the increased capacitance per length of a transmission cable in comparison to an overhead line [2, 3].

Power converters, capable of processing power at a Gigawatt scale with operating voltages in the several hundreds of kilovolts, are the key technology which enables HVDC systems. The converters themselves are physically large, complex devices, containing thousands of power electronic devices, control equipment, filtering elements, cooling systems and ancillary equipment. A converter has additional losses, lower reliability and reduced availability in comparison to the AC transformers. HVDC does however have several key benefits over AC transmission which can make it the correct techno-economic choice in certain applications [2].

- The transmission distances possible are not limited by the reactive power requirement of the conductor system, or by power angle stability limitations.
- It can connect asynchronous AC areas together.
- Power flow through the converter station can be directly controlled.
- It has a higher power density per conductor cross section vs. AC systems, and improved utilisation of a line or cable's voltage insulation design. This results in reduced right of way and reduced conductor requirement for a given power rating.

1.1 History of HVDC

1.1.1 Early technology and Line Commutated Converters

HVDC systems have been a part of the conventional power system for many years. The advent of HVDC began with the invention of the mercury-arc valve in 1902. The first transmission systems using these technologies were realised in the 1930s and 1940s. Before this series connected motor-generator units were used to transmit power at DC as early as 1889 [4].

The Gotland transmission scheme, a 20 MW system commissioned in 1954 with a 98 km sub-sea cable that linked the island of Gotland to mainland Sweden, could be considered the first 'modern' DC transmission scheme. This was quickly followed by several other schemes, notably the 160 MW link across the English channel, linking the French and British power systems together. Power ratings of these schemes climbed rapidly, culminating in the Nielson River DC Transmission System, a $\pm 450\,kV$ system with a power rating of 1.62 GW. Mercury-arc valve based systems were then phased out in favour of newer thyristor based solid-state systems with higher power densities and efficiency. The first notable thyristor based scheme was the Back-to-Back asynchronous inter-connector between Quebec and New Brunswick [5]. Thyristor based schemes are still the most popular converter technology for the bulk transfer of power over long distances. The recent Rio Madeira scheme in Brazil is capable of transferring 6.3 GW of power over a distance of 2,135 km, with future schemes in planning stages with even higher power ratings [6].

A typical converter circuit arrangement for thyristor based HVDC converters is shown in Fig. 1.2. Two six-pulse bridge are operated in series, with a 30^o phase shift introduced through the use of transformers with star-star and star-delta windings. The amount of active power flow can be controlled by varying the firing angle of the thyristors with respect to the AC voltage waveform.

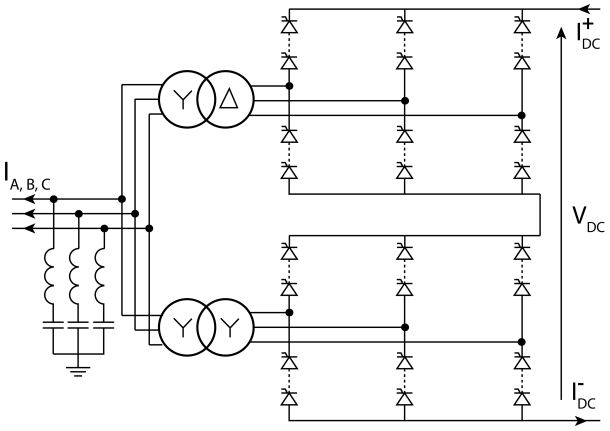


Figure 1.2: 12-Pulse Line Commutated Converter

Thyristor and mercury-arc valve HVDC converters require an external AC voltage to commutate the switch and force it out of conduction. For this reason they are commonly referred to as Current Source Converters (CSC) or Line Commutated Converters (LCC). They appear as a current source to the grid that they are connected to and are incapable of generating their own AC voltage waveforms.

LCC systems are a very robust technology that allows extremely high power levels to be achieved. However they have several disadvantages from a power systems perspective:

- They lack independent control of real and reactive power.
- They require a large amount of reactive power compensation.
- They require substantial current waveform filtering.
- They rely on the external grid to commutate the thyristor valves, meaning they cannot operate into a weak grid.
- They are unable to black-start an AC system.
- Power reversal requires an inversion of the DC voltage polarity.

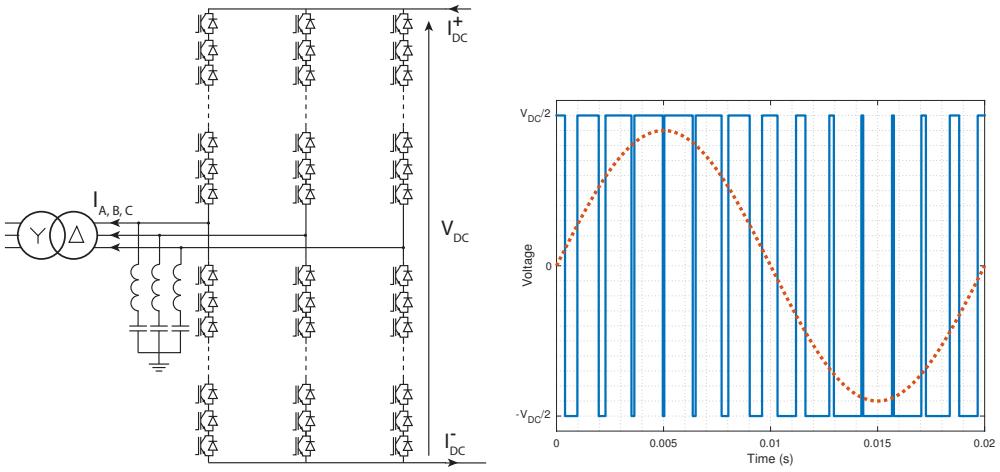
1.1.2 Voltage Source Converters

For a converter to act as a voltage source, and thus achieve independent control of real and reactive power, it requires power electronic switches that are capable of both turning on and switching off. Converters with such capability are referred to as Voltage Source Converters (VSC).

Power electronic switches with both the current handling capabilities and voltage blocking capability required to design HVDC scale VSCs were not feasible until the introduction of the Insulated Bipolar Gate Transistor (IGBT). Other technologies, such as the Power MOSFET and the Gate Turn Off Thyristor had made lower scale VSCs for drive applications practical.

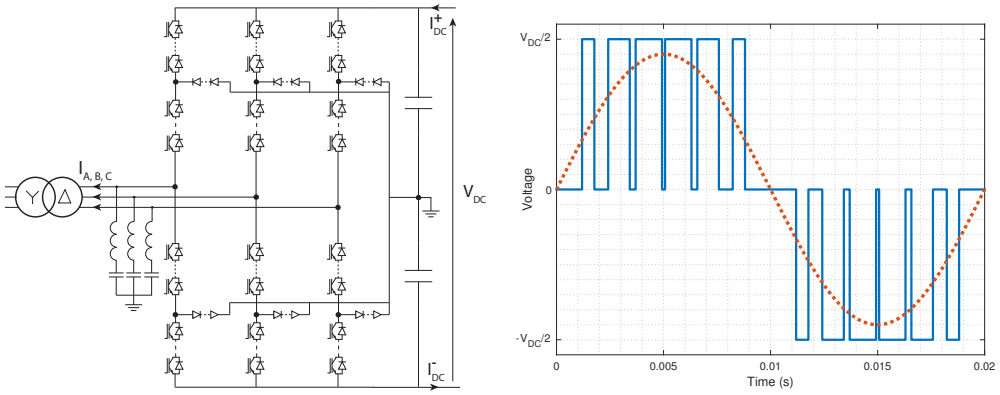
The first commercial transmission scale VSC based HVDC scheme was commissioned in Gotland, Sweden in 1999 by the engineering company ABB, who had also pioneered the original Gotland LCC based scheme [7]. The scheme used a two-level converter, as illustrated in Fig. 1.3, with a sinusoidal-pulse width modulated voltage output. Such schemes suffered from relatively high losses due to the switching frequency required to keep the harmonic distortion low and have a requirement for filters to remove the higher order harmonics generated by the converter. Achieving a valve stack of series IGBT devices capable of switching the DC bus voltage was one of the main technical achievements in the project. A single valve may contain several hundred devices in series. If a single device within the valve switches earlier or later than the other devices in the series chain it would be exposed to the full voltage of the DC link, far exceeding its rated blocking voltage, resulting in destruction of the device.

The two-level topology initially used for HVDC applications was then replaced by a three level neutral Point Clamped (NPC) topology, illustrated in Fig. 1.4. This was done to drive down the requirement for high switching frequencies, with the aim of reducing the losses that result from this. This NPC topology was then replaced with a more optimised two-level design that reduced the switching frequency required and used more advanced IGBT modules [8]. Power levels increased steadily over the following decade, with schemes such as the East-West Inter-connector, linking Ireland and Wales reaching 500 MW.



(a) Converter schematic (b) Voltage waveform

Figure 1.3: 2-Level HVDC converter



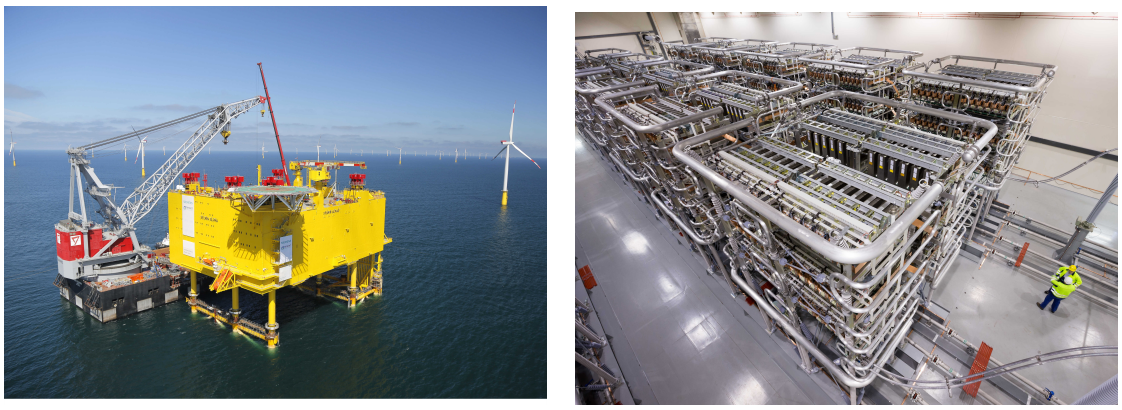
(a) Converter schematic (b) Voltage waveform

Figure 1.4: 3-level neutral point clamped HVDC converter.

Up to 2010, the market for VSC HVDC was monopolised by ABB. This changed with the introduction of the Modular Multilevel Converter (MMC), which is discussed in detail in Section. 1.2.3. The first commercial installation of this topology was the Trans Bay Cable project by Siemens [9], linking San Francisco with Pittsburgh through an 85 km sub-sea cable through San Francisco bay. The scheme was rated to 400 MW and operated at $\pm 200\ kV$.

Since its introduction the MMC has proliferated in use. Some of the most notable cases are

the North Sea wind-farms ordered by TenneT. There are ten wind-farms in total, either already operational or under construction as of writing. BorWin (3 HVDC Links), HelWin (2 Links) and DolWin (3 Links) schemes and SylWin (2 Links). All of these schemes, apart from BorWin 1, are based upon MMC topologies. The various schemes are being supplied by a combination of ABB, Siemens and GE Grid. The average power is in the region of 800 MW, with most operating at a DC voltage close to $\pm 300\ kV$. Fig 1.5 shows an outside view of the offshore platform from the BorWin2 scheme, as well as a picture of the inside of the valve hall.



(a) Offshore platform - copyright: TenneT. (b) Valve hall - copyright: Siemens.

Figure 1.5: SylWin1 HVDC link.

1.1.3 Multi-terminal Systems

The increasing demand for renewable energy sources, has also driven a resurgence in the idea of constructing multi-terminal DC systems. Most HVDC links to date have been point-to-point, with two terminals and either a cable or overhead line connecting them. VSC based systems are particularity well suited to use in multi-terminal systems as they are capable of reversing the direction of power-flow by reversing the current flow, unlike in LCC based systems where the voltage polarity must be reversed. The most notable multi-terminal VSC systems to date are the Zhoushan system [10], which contains five terminals rated to 400/300/100/100/100 MW,

and the Nan'ao system [11], which contains one onshore 200 MW station, and two island based stations rated to 100 MW and 50 MW. The implementation of multi-terminal HVDC systems have numerous challenges which must be overcome [12].

- Control of DC networks.
- AC and DC system interactions, particularity where the power rating of the DC system becomes a significant fraction of the AC systems to which it is connected.
- DC system protection [13]. This will be discussed further in Section. 1.2.2.
- Techno-economic issues regarding who pays for, owns and operates such multi-terminal networks. This is a particular challenge as most multi-terminal networks are envisaged to connect numerous countries, or even continents together.

There have been numerous proposals for pan-continental HVDC networks, which would overlay existing AC grids, but provide much more flexible operation, as well as enabling power to be transmitted over longer distances. One example of a proposed multi-terminal network is the European Wind Energy Associations 2020 vision shown in Fig. 1.6. Other examples of such proposals are the now defunct Desertec proposal [14], which proposed building large amounts of Concentrating Solar Power stations in North Africa, and then exporting the power back to Europe through a multi-terminal HVDC grid and the North Sea Offshore Grid, which is an active proposal by the European Commission [15]. It aims to establish an offshore DC network that links Germany, the United Kingdom, Ireland, Belgium, the Netherlands, Denmark, Sweden, Luxembourg and France.

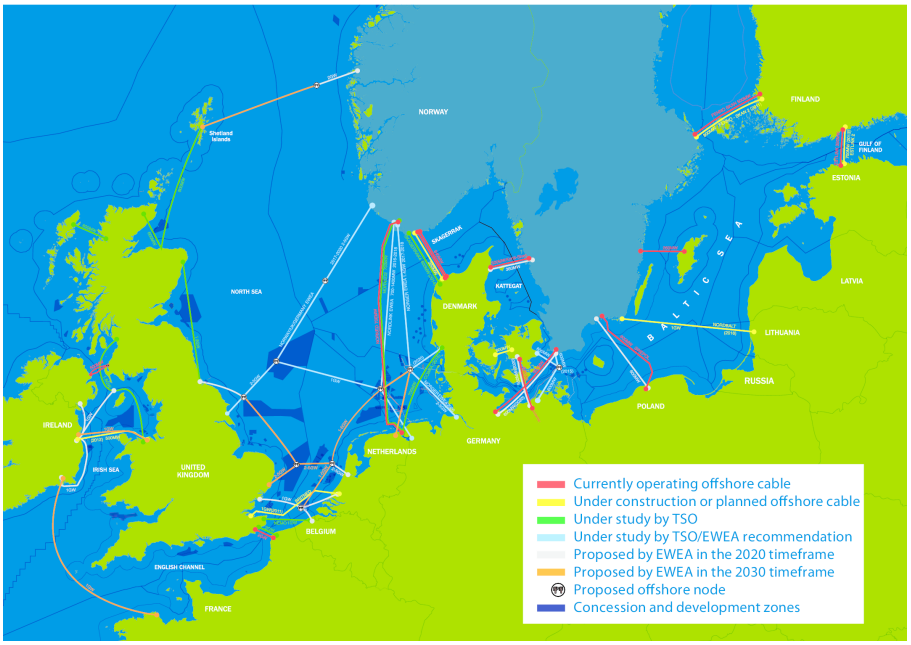


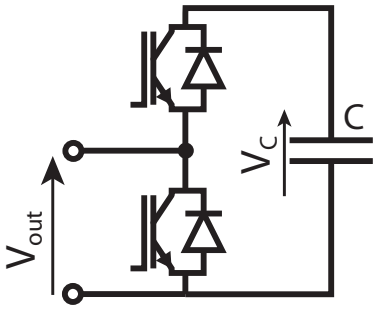
Figure 1.6: European wind energy association 2020 vision plan [16].

1.2 Multilevel Converters

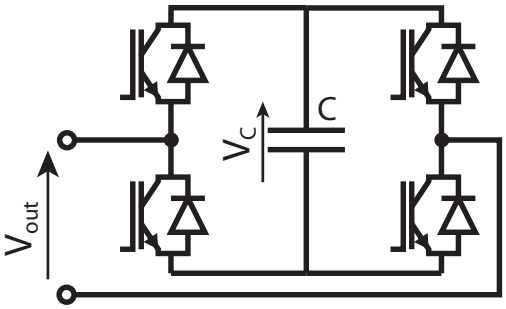
By increasing the number of voltage levels within a converter, the harmonic content of the resulting waveforms can be decreased. This results in a reduced requirement for filtering, reduced electromagnetic interference and reduced losses due to a lower switching frequency requirement. This was ABB's driving motivation in switching from the original two-level design to the three-level NPC. The operational principle of the NPC can be further expanded up to higher number of levels, however this number of diodes required in the NPC is quadratically proportional to the number of levels, which enforces a practical limitation on the number of levels [17].

The introduction of the Modular Multilevel Converter [18], discussed in the following section, and the can be seen as a landmark in HVDC technology. Not purely for the converter topology itself, but for the modular multilevel concept it introduced. Two of the basic building blocks of modular converters, the half-bridge and full-bridge sub-module are shown in Fig. 1.7. Numerous

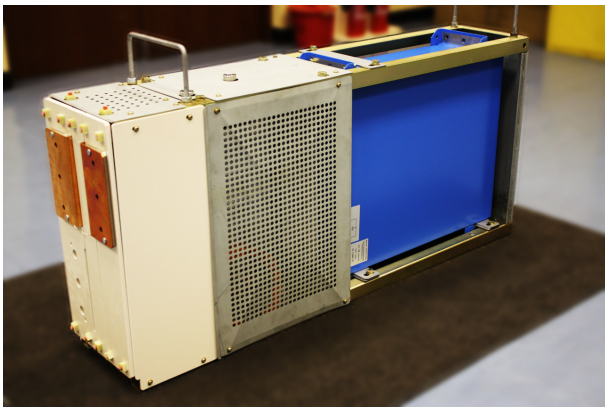
other sub-module arrangements are possible, however these are the two most common. The half-bridge sub-module is capable of generating a positive voltage output, while the full-bridge sub-module can generate both positive and negative voltage outputs. The precursor to this topology was a delta arrangement STATCOM [19], developed by Alstom Grid, which used full-bridge sub-modules and Gate Turn-Off Thyristors as the switching devices.



(a) Half-bridge sub-module



(b) Full-bridge sub-module

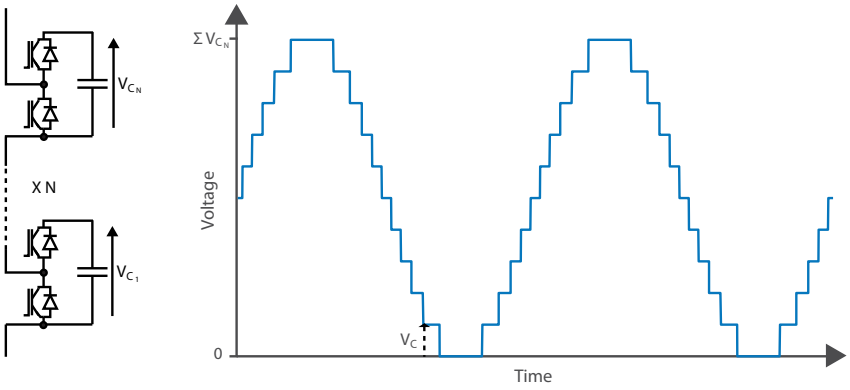


(c) Sub-module - copyright: GE Grid

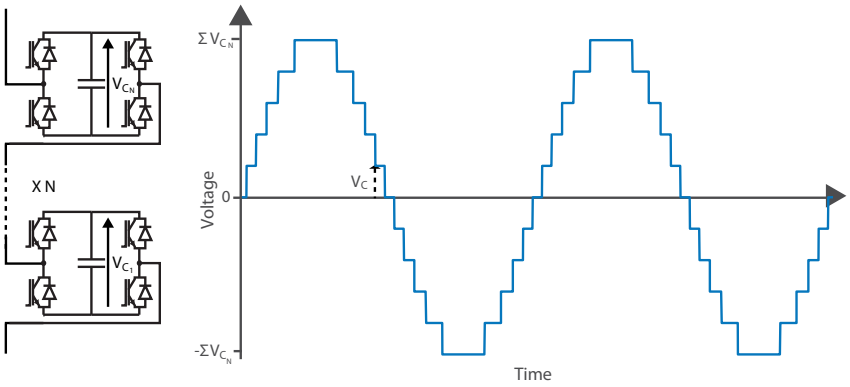
Figure 1.7: Sub-module for modular HVDC applications.

Each sub-module contains a floating sub-module capacitor, controlled to a nominal voltage. By switching the IGBTs within the sub-module, this capacitor can be inserted into the current path, or bypassed. The voltage of sub-module capacitor can therefore be made to appear across the output terminals of the sub-module. By connecting sub-modules in series a stack or chain-

link valve can be formed, capable of generating stepped voltage waveform with many levels. This is illustrated in Fig. 1.8.



(a) Half-Bridge sub-module stack



(b) Full-Bridge sub-module stack

Figure 1.8: Series arrangement of sub-modules to form a valve stack.

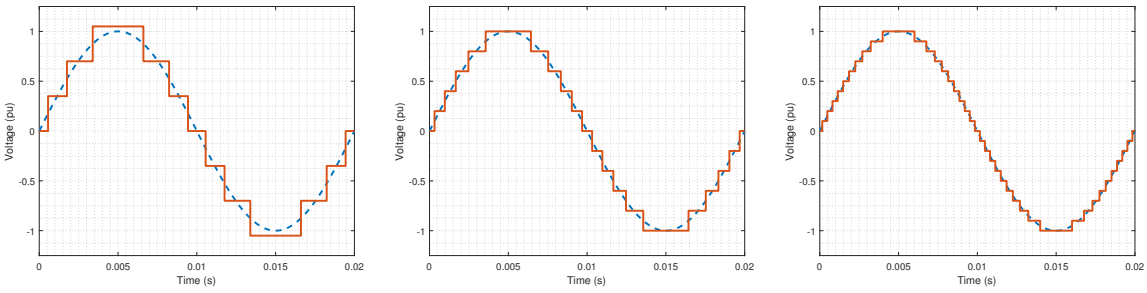
This stepped voltage waveform can be achieved while keeping the switching frequency of individual sub-modules to a low value. This leads to a modular design, where one converter comprises several hundred smaller sub-modules, each of which is functionally a converter in its own right. This has several advantages in terms of design:

- The sub-module capacitor is a convenient power source for deriving the supply power for the IGBT gate drivers, eliminating the need for ancillary circuits or power supply

transformer arrangements.

- Each IGBT must only block the voltage of its local sub-module capacitor, allowing high voltage converters to be designed without the need to series operate IGBTs.
- The modular design enables redundancy to be easily designed into the converter, and simplifies manufacturing.

This modular design approach allows converters with a large number of levels to be achieved, without the penalty in terms of increased device count that previous generations of multilevel circuit topologies incurred [20]. An example of the voltage waveforms that can be achieved with a relatively low number of levels is given in Fig. 1.9.



(a) 7 levels (b) 10 levels (c) 21 levels

Figure 1.9: Multilevel approximation to a sine wave.

For a HVDC scale converter, which may operate with a DC voltage in the region of 1 MV, the required number of series operated sub-modules within the converter is in the hundreds. The harmonic distortion of such converters can therefore be extremely low. This reduces or eliminates the need for filtering of the AC and DC current waveforms generated by the converter.

The application of the modular multilevel principle is not limited to just AC-DC converters, but also to DC-DC converters [21, 22, 23] as well as AC-AC converters [24, 25, 26, 27]. The MMC itself has also found application in lower voltage motor drive applications [28]. Such applications can introduce challenges in operating an MMC which are not applicable to HVDC

scale MMCs. In motor drive applications the main additional challenges are related to designing the converter to operate over a wide frequency range, which impacts the converters energy storage requirement, as well as operating with only a small number of sub-modules.

1.2.1 Energy and Voltage Deviation

The voltage that each sub-module can generate is determined by the voltage of its sub-module capacitor. This is determined by the stored charge within the capacitor. The voltage capability of a series stack is sub-modules is therefore linked to the overall amount of stored energy within the converter. When a sub-module capacitor is inserted into the current path it will be either charged or discharged. This causes a voltage ripple to be imposed on the sub-module capacitor voltages as the stored charge within the capacitor is increased or reduced by conducted current that passes through it.

The energy deviation of a stack of sub-modules refers to the cycle-by-cycle deviation of the stored energy within that stack. If the average power processed by a stack of sub-modules is zero, i.e the average power on both sides of the converter are equal, than the energy content within each stack will return to its starting point at the end of each electrical cycle. Any imbalance between the powers on either side of the converter will result in a deviation in the total stored energy content within the converter.

1.2.1.1 Voltage Balancing

Not all sub-modules within a series stack will see identical currents. Their voltage will therefore drift away from each other over time if there is no control mechanism present to prevent this. One of the most common methods of preventing this is the use of a sorting algorithm, which was initially presented in the first paper on the MMC [18]. The sorting algorithm works by ranking each sub-module based on their measured capacitor voltages. The sub-module with the lowest/highest capacitor voltage is then preferentially inserted first, depending on if the current direction is such that it will charge/discharge the sub-modules, and so on until the voltage reference has been achieved.

An illustration of the sorting algorithm being applied to a stack of 10 sub-modules within an MMC is given in Fig. 1.10. The first sub-module within the stack (sub-module 1) is highlighted in bold and is used to illustrate the operation of the sorting algorithm. When the power of the stack (given by the product of the voltage generated by the stack of sub-modules and the current flowing through it) is positive, the stack is absorbing energy and so the sub-modules that insert their capacitors will increase their voltage and vice-versa. When the rank of sub-module 1 is above the number of inserted sub-modules, such as between t=0.02 s and t = 0.03 s, it is not used to generate a voltage and so its voltage remains static. When its rank is below the number of inserted sub-modules, such as between t=0.013 s and t=0.02 s, it is used to generate a voltage, and so its capacitor voltage will change due to the charging/discharging action of the current flowing through it. The rank of each sub-module is updated at several points throughout each cycle, ensuring that the sub-module voltages do not diverge from each other. These updates to the rank of each sub-module are commonly referred to as rotations.

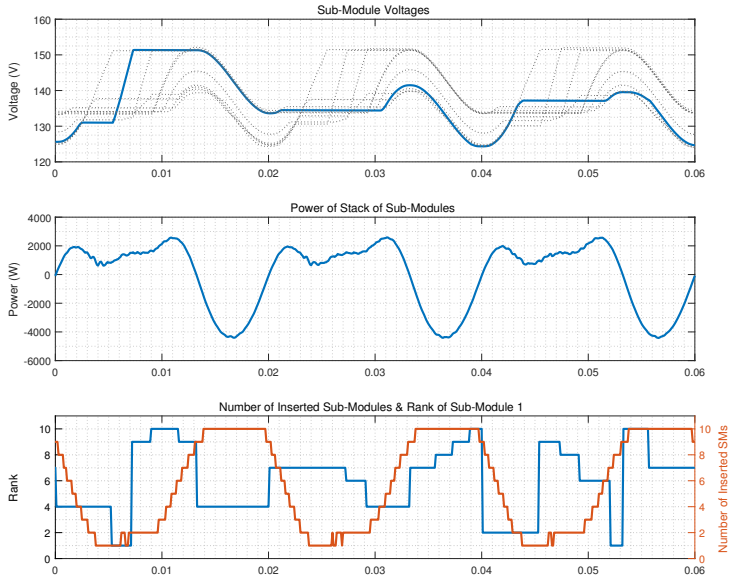


Figure 1.10: Sub-module voltage balancing using the sorting algorithm.

Another common method of stack voltage generation and the voltage balancing of sub-modules is the Phase-Shifted Pulse Width Modulation (PS-PWM) method presented in [29, 30, 31]. In this method each sub-module has its own triangle wave carrier waveform which is phase-shifted from its neighbouring sub-modules by $\frac{2\pi}{N}$ radians, where N is the number of sub-modules per stack. The controller's voltage reference for the entire stack is normalised by the sum of the sub-module voltages and passed to every sub-module. Voltage balancing between sub-modules is handled in a distributed manner by having a sub-module compare its voltage level to the mean of the sub-module voltages within the stack and adding a proportional gain onto the modulation index, so that it is either inserted more or less depending on the current flow direction.

1.2.1.2 Energy Balancing

The energy content within a modular converter may be disturbed by fault scenarios, either internal or external to the converter, resulting in a net overall energy deficit/surplus or an asymmetry in how the stored energy is distributed through the converter. To rebalance the converter it is necessary to have some form of Energy Management System (EMS) implemented within the converter control, which is capable of controlling the stored energy content within the converter back to its nominal set-point [17].

The balancing of the overall energy content within the converter can be performed by adjusting the processed power on both sides of the converter (i.e AC-side and DC-side for an AC-DC converter). This imbalance in power will result in a net increase or decrease in the energy stored within the converter. To account for asymmetric imbalances some form of horizontal balancing, and vertical balancing mechanisms are also required. Horizontal balancing concerns the balance of energy between different phases within the converter, while vertical balancing concerns the balance of energy content contained in stacks of sub-modules which are located within the same phase.

An example of energy balancing in a modular converter is given in Fig. 1.11. At t=0.05 s an asymmetric AC fault occurs which results in an imbalance between the powers on the AC and DC side of the converter. This results in a disturbance to the voltage levels of the sub-modules within the converter. The overall energy balancing mechanism adjusts the balance of power between the AC and DC side of the converter, bringing the total energy within the converter back to its nominal level. The horizontal balancing currents adjust the energy balance between the phases of the converter so that each phase contains an equal amount of energy. The vertical balancing currents address any imbalance between the stacks of sub-modules that are located within the same phase.

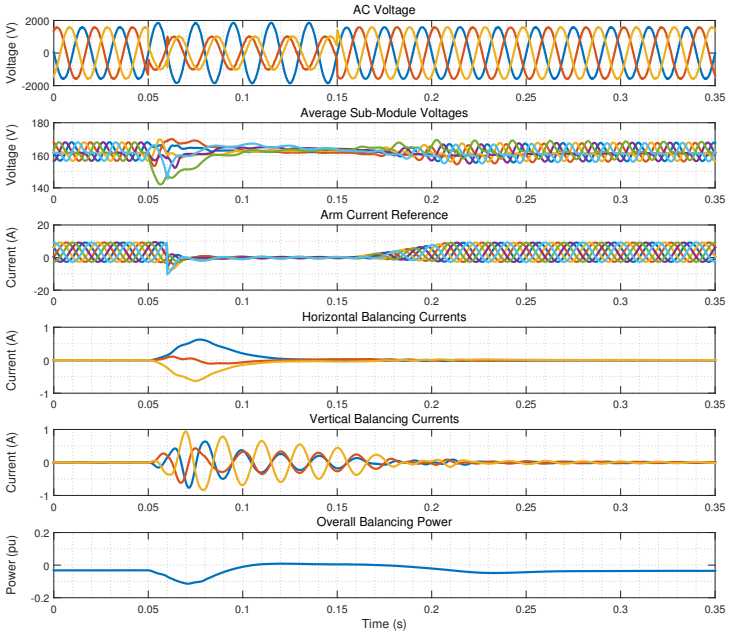
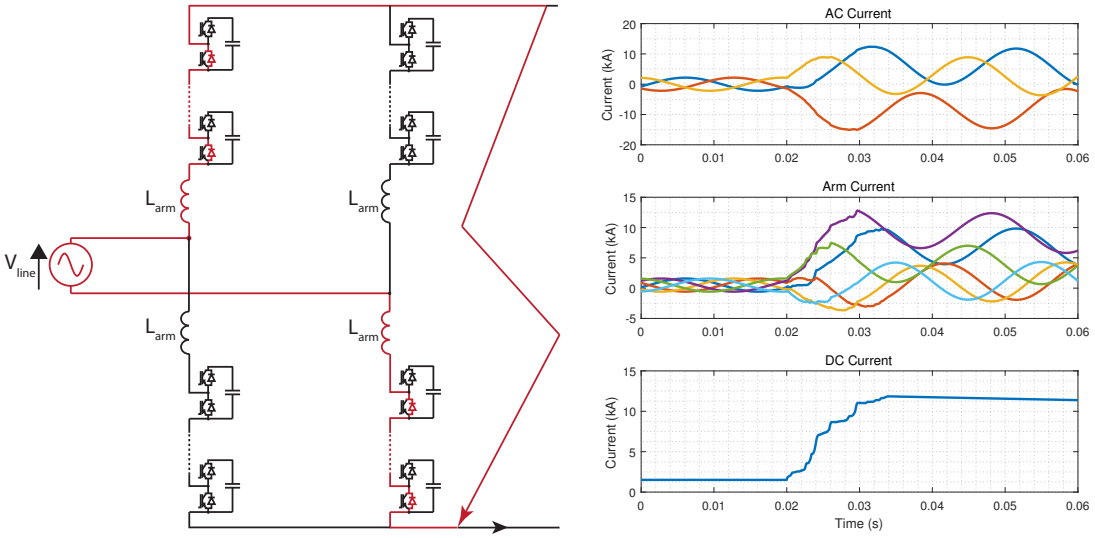


Figure 1.11: Energy balancing in a modular multilevel converter due to a disturbance caused by an AC fault.

1.2.2 DC Faults

In VSC converters, such as the two-level converter and the half-bridge MMC, there is an uncontrollable path through anti-parallel IGBT diodes in the event of a DC fault. This is illustrated in Fig. 1.12. This results in a large DC side fault current due to the uncontrolled rectification of AC current through the converter, with the magnitude of the fault current limited only by the impedance of the AC network. In point-to-point systems, DC faults can be cleared by opening the AC side breakers. This protection approach may not be suitable for multi-terminals systems for several reasons. Clearing a DC fault through this method would require each terminals AC breaker to be opened, the DC grid would then have to be de-energised and the faulted line isolated. The DC grid, and all converter stations at the terminals would then have to be re-energised and then re-synced to their respective AC systems. This approach may take a considerable amount of time, and may not be adequate for multi-Gigawatt schemes that interconnect several AC systems.



(a) Uncontrolled current path through anti-parallel diodes

(b) AC, DC and internal converter currents

Figure 1.12: DC fault response of a non-DC fault tolerant converter.

Alternatives to clearing DC faults with AC side breakers are the use of fast acting DC circuit breakers, capable of detecting and clearing a DC fault within a short ($< 10\ ms$) time-frame [32]. DC circuit breakers pose a significantly large more challenging design problem than AC circuit breakers. This is because in an AC systems the stored energy within the system will naturally be brought to zero twice per cycle, providing opportunities to break any arcs that form when the breaker opens. In a DC system this is not true, meaning that the energy within the system must be absorbed by the breaker itself in order to interrupt a fault current.

The design of a HVDC circuit breaker from ABB [33] is illustrated in Fig. 1.13. The main conduction path during normal operation is through a fast mechanical breaker and a load commutation switch of anti-series IGBTs rated to a low voltage. This design results in low on-state losses. In parallel with this is a branch of sub-modules that each contain a varistor. Each sub-module can either bypass or insert its varistor into the current path. An inductor is placed in series with the breaker to limit the rate of rise of current during a fault event. When a fault is detected the load commutation switch IGBTs are switched off, this commutates the fault

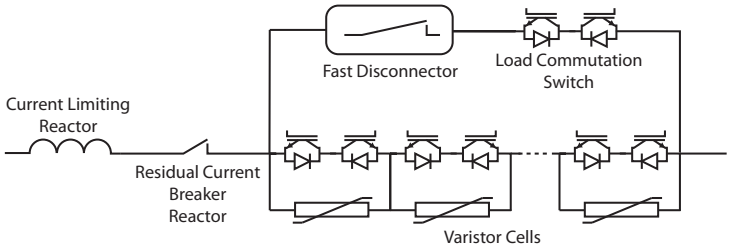
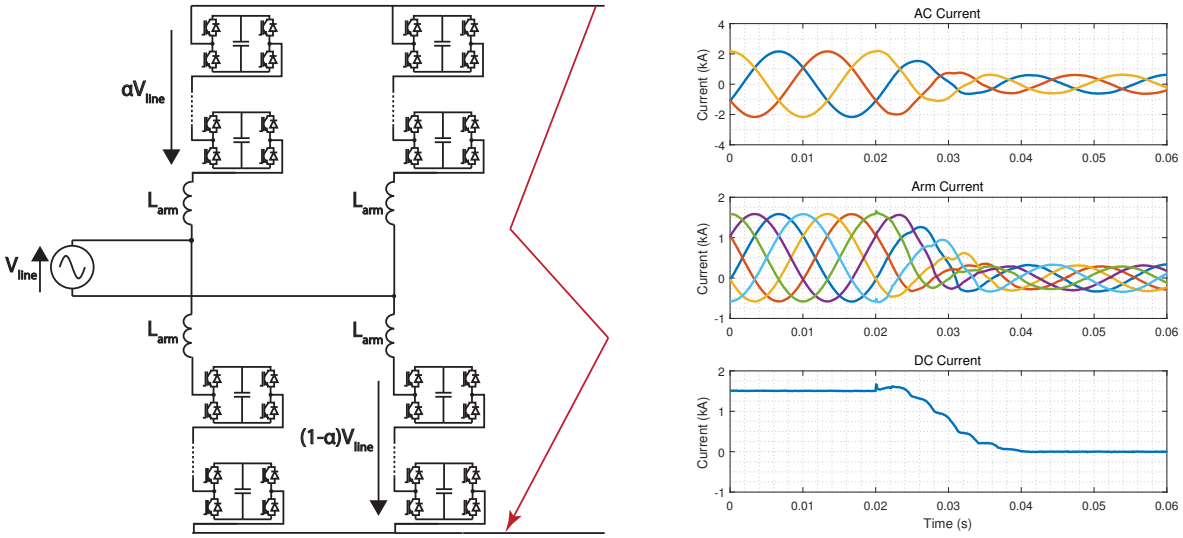


Figure 1.13: Hybrid DC circuit breaker design -adapted from [33].

current from the main branch into the varistor sub-module branch, allowing the fast disconnecter to open under zero current conditions. This means the fast disconnecter reduces the required voltage withstand requirement of the load commutation switch, resulting in a design with very low on-state losses.

With the fault current now in the varistor sub-module branch, the breaker can then control the effective fault impedance by varying the number of varistor sub-modules that are inserted into the fault current path. This means the breaker can either drive the fault current to zero, or act in current limiting mode if required, depending on the protection strategy employed. When the current has been driven to zero, the residual circuit breaker opens and the fault is fully cleared.

An alternate option for dealing with DC faults, that does not involve circuit breakers, is to design HVDC converters that are capable of either blocking the fault current, or retaining current control throughout the fault, meaning that the AC fault contribution to a DC fault can be prevented. To do this the converter stacks must be capable of generating enough negative voltage to oppose the voltage from the healthy AC grid during the DC fault, necessitating the use of sub-modules that are capable of generating a negative output voltage, such as full-bridges. This is illustrated in Fig. 1.14. In the event of a DC fault the fault could be isolated by waiting for the stored energy within the DC system to discharge into the fault, the faulted line could then be cleared by dis-connectors that are only required to open under zero current conditions. Fault tolerant converters may be particularly useful for overhead line applications,



(a) AC voltage opposed by converter arms with negative voltage capability

(b) AC, DC and internal converter currents

Figure 1.14: DC fault response of a DC fault tolerant converter.

where non-permanent faults such as flash-overs due to lightning and tree strikes may occur.

1.2.3 Modular Multilevel Converter

The Modular Multilevel Converter (MMC), introduced in [18], has become the standard topology for implementing VSC based HVDC schemes, supplanting previous generations of two- and three-level topologies. Since its introduction the number of suppliers of competing VSC HVDC products has also expanded rapidly, with the market now containing in the region of 6 suppliers, around half of which are Chinese. This is a stark contrast to the VSC market of a decade ago, where ABB was the sole manufacturer capable of supplying VSC HVDC products.

A circuit diagram of the MMC is shown in Fig. 1.15. The converter is composed of 6 arms, two of which constitute a phase leg of the converter. Each arm contains an arm inductor, necessary for control purposes, as well as a series stack of half-bridge sub-modules.

The AC currents within an MMC split between the upper and lower arms of each phase. Under balanced conditions the DC current splits evenly between the three phases. Each arm of

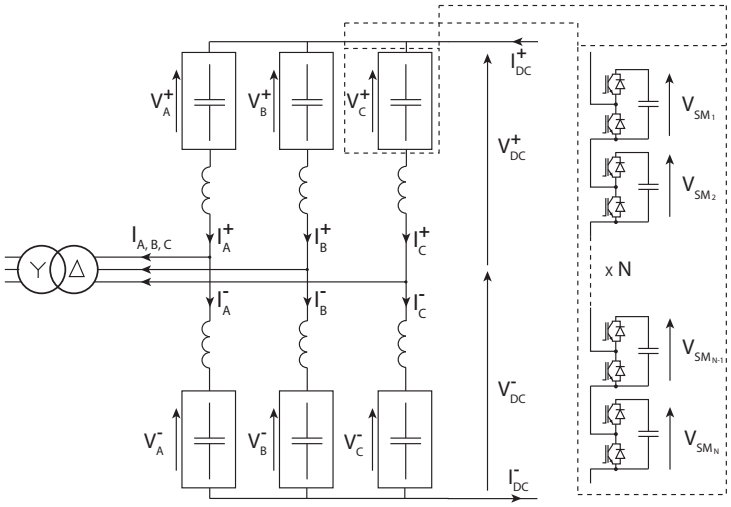


Figure 1.15: Schematic of Modular Multilevel Converter.

the converter therefore conducts a combination of the AC current and the DC current. The AC currents cancel each other out at the positive and negative DC rails, resulting in a smooth DC current that requires little to no filtering. Example voltage and current waveforms from one arm of an MMC operating at unity power-factor are shown in Fig. 1.16. Each arm generates an AC voltage with a DC offset. In its standard arrangement, the converter is operated with an AC voltage that is below the DC rail voltage. This means that the voltage each stack must generate is always positive, meaning half-bridge sub-modules can be used.

The MMC has a well-documented issue with uncontrolled circulating currents that can occur under certain control schemes [34, 35, 36, 37]. These circulating currents appear due to a common mode voltage being imposed across the arm inductor. This common mode voltage appears due to the sum sub-module voltage ripple not being accounted for in the modulation scheme.

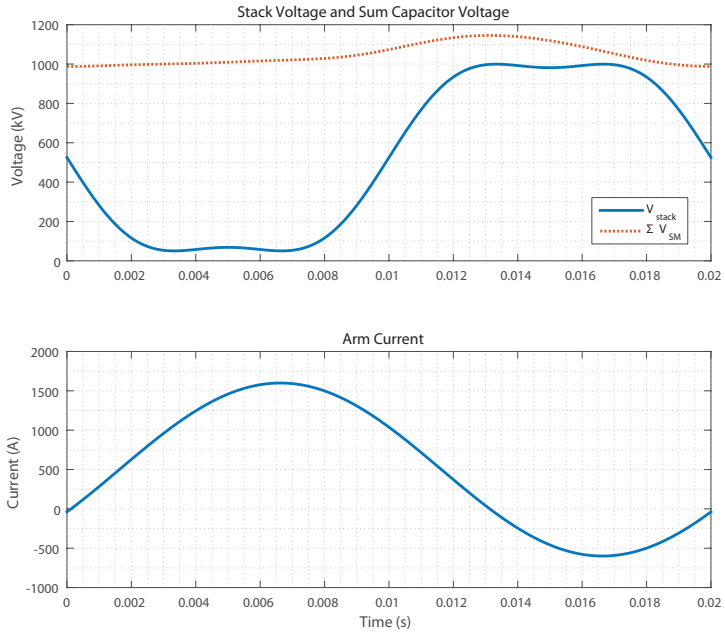


Figure 1.16: Stack voltage and arm current of an MMC at unity power factor.

1.2.4 Alternate Arm Converter

The Alternate Arm Converter (AAC) [38, 39] is a hybrid voltage source converter topology [40, 41] which combines the IGBT switches (called the director switches) of a two-level converter with stacks of sub-modules similar to those of the MMC. The circuit diagram of an AAC is shown in Fig. 1.17. The prime motivation in the development of the AAC was to achieve a DC fault tolerant converter, without sacrificing the efficiency of the converter to a large degree. It also has the advantage of requiring a reduced number of sub-modules in comparison to the MMC; this may have advantages for offshore applications, where volume may be of concern.

The basic operational principles of the AAC, adapted from [42], are illustrated in Fig. 1.18. The director switches within each arm are closed for half of each cycle, while the director switch in the other arm of that phase is open. The AC current on each phase is then 'directed' through the arm with a closed director switch, resulting in each arm conducting for only half an electrical cycle. The director switch and sub-modules within the arm which is open work together to block

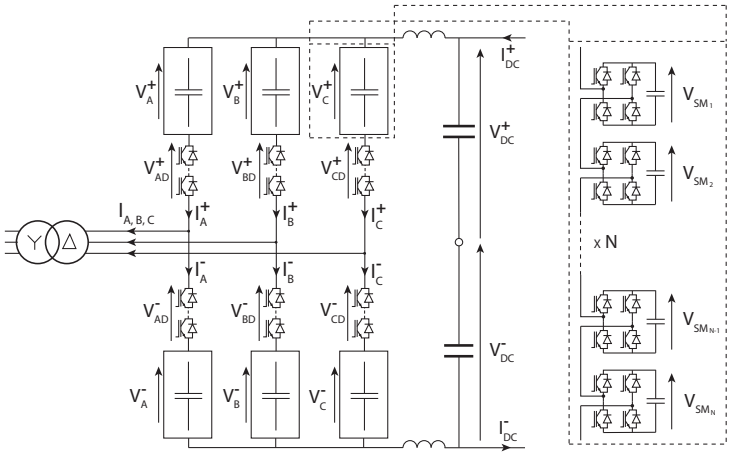


Figure 1.17: Schematic of Alternate Arm Converter.

the required voltage.

This operational mode results in the DC current being formed from the direct rectification/inversion of the AC current waveform. This has several implications: The DC current contains a six-pulse ripple, requiring DC side filtering. The AC and DC side power flows are coupled, resulting in the converter requiring to be operated at a AC to DC voltage ratio of $\frac{\pi}{4}$ (~ 1.27), referred to as the 'sweet spot'.

For energy balancing reasons, it was found to be necessary to operate the converter so that there are two periods during each cycle, referred to as the overlap periods, where the upper and lower director switches within each arm are both open at the same time. This allows balancing currents to be run between the upper and lower arms of the converter. This enables the converter to be operated when it is not exactly at the sweet spot, without the stored energy content within the converter being

A new operational mode of the AAC, aimed at addressing several of the shortcomings of the previous design has been proposed [43, 44], and is the mode considered within this thesis. In this new operational mode, an Extended Overlap (EO) period of 60 degrees is used. Under this operational mode, one phase of the converter is always in an overlap period throughout the entire electrical cycle. This ensures a continuous path for the DC current. The AC currents

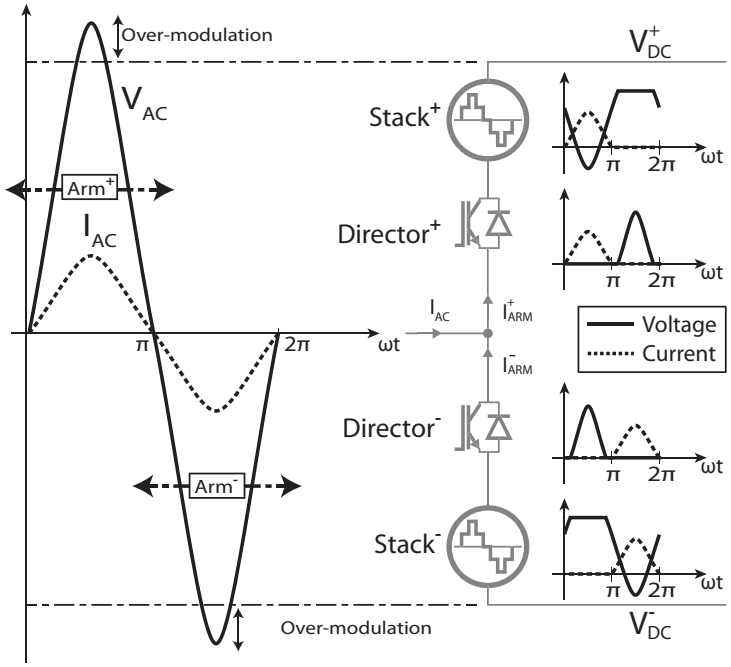


Figure 1.18: Idealised voltage and current waveforms over one cycle in the AAC - Taken with permission from [42].

can be made to follow the path shown in Fig. 1.19.

The AC currents cancel at the midpoint of whichever phase is in overlap. This eliminates the six-pulse ripple from the DC current waveform, and allows the AC and DC side powers to be decoupled. This ensures a continuous conduction path for the DC current, allowing a smooth DC current waveform to be achieved. The EO mode of operation also allows the DC and AC side powers to be decoupled, resulting in an elimination of the sweet-spot energy relationship between the AC and DC side voltage magnitudes. The EO-AAC has the following advantages over the original AAC topology:

- Removal of the six pulse ripple from the DC side current waveform, eliminating the need for a large DC side capacitance and filter.

- Elimination of the 'sweet-spot' energy balance relationship between the DC and AC side voltage magnitudes.

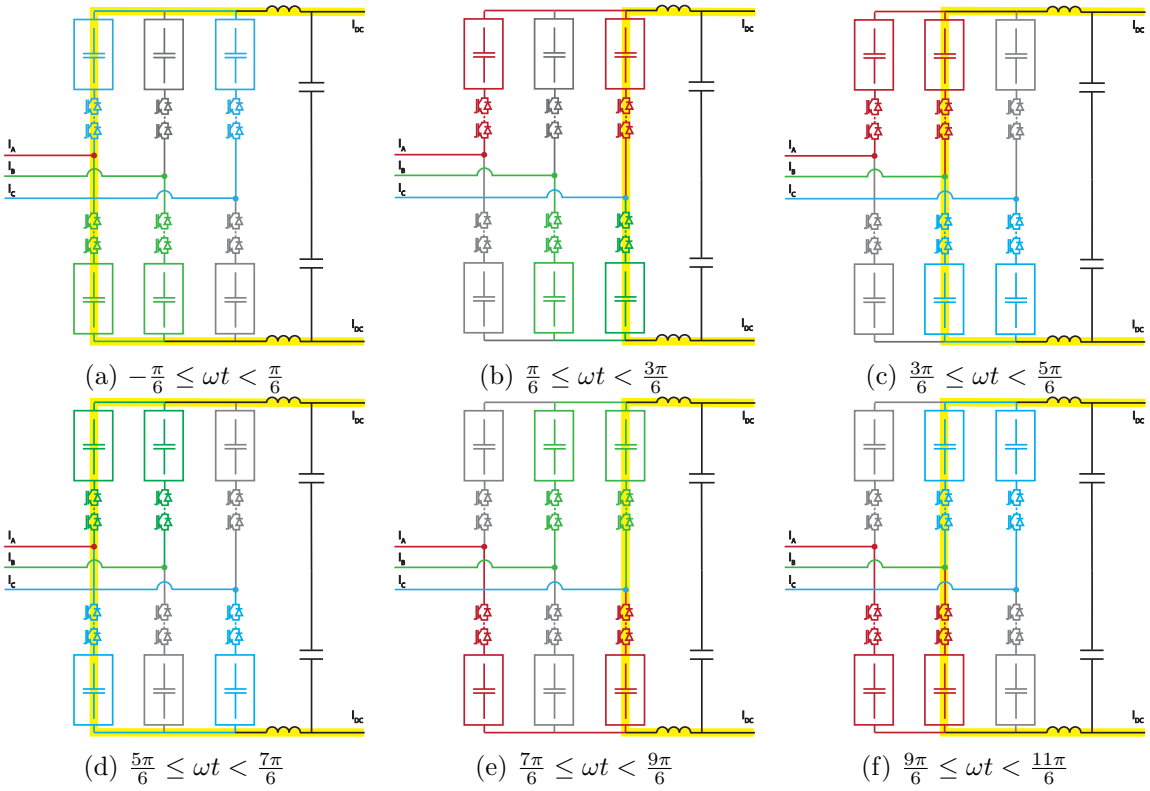


Figure 1.19: Current paths within the EO-AAC throughout one full electrical cycle.

- Replacement of the inductors within each arm with a pair of DC side inductors, reducing the overall volume of the converter.
- Little to no discontinuities in the arm current waveform.

It achieves these features, whilst retaining the three main advantages of the original AAC topology, namely:

- DC fault ride through capability.
- Reduced energy storage requirement in comparison to the MMC.
- Improved efficiency in comparison to the full-bridge MMC.

The EO-AAC is operated with a zero sequence harmonic voltage, as shown in Fig. 1.20,

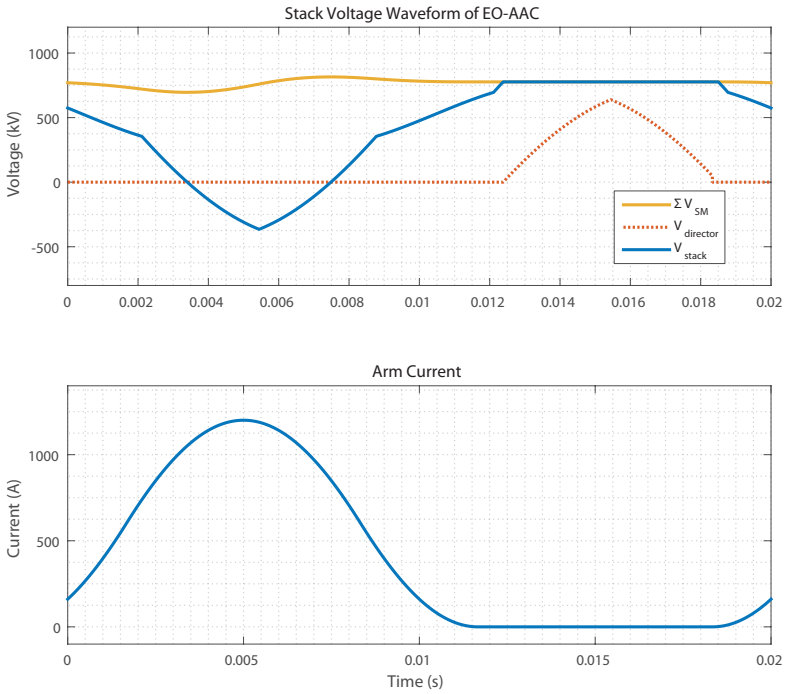


Figure 1.20: Stack voltage waveform and arm current of the EO-AAC. Top: Stack voltage waveform generated by a combination of the stack of sub-modules and the director switch. Bottom: Arm current waveform at unity power factor.

imposed on the AC phase voltage waveform [45]. This zero sequence flattens the voltage that the converter is required to generate during the overlap period since a longer overlap period implies that the voltage generation capability of the stacks of SMs within each arm must be increased. This voltage generation requirement has a strong impact on the number of SMs which must be included within the converter, and therefore the overall converter efficiency. A star-delta transformer is used to prevent any zero-sequence components from being transmitted to the AC grid.

1.3 Thesis Structure

This thesis structured as follows:

Chapter 2 details the work undertaken in developing a lab-scale experimental multilevel converter which is used to generate results at several points within this thesis.

Chapter 3 investigates the design of the Modular Multilevel Converter, with an emphasis on design for realistic converter design requirements from an AC grid perspective. The analysis is then extended to the case of the Hybrid Modular Multilevel Converter, which combines full- and half-bridge sub-modules within its stacks so as the achieve DC fault tolerance.

Chapter 4 investigates the power-loss and thermal characteristics of several converter topologies. A Finite Element Model of a heat-sink mounted IGBT is detailed. Transfer function from this model are combined with a power-loss block to estimate the overall power-losses within each topology, as well as the distribution of losses within the converter itself.

Chapter 5 investigates how overload capacity, for providing grid services such as fast frequency support, could be built into Modular Multilevel Converters. A focus is placed on the use of controlled circulating currents to get around the limitation imposed by the peak arm current limit of the converter. The potential of dynamically rating converters based upon their estimated device junction temperatures is investigated. Simulations of such a scheme implemented in a test network that is representative of the Great Britain network are then carried out.

Chapter 6 introduces a proposed hybrid multilevel structure, composed of sub-modules and thyristors, for achieving high efficiency voltage source converters, while retaining features such as DC fault tolerance and high quality AC and DC current waveforms.

Chapter 7 concerns the design, control and operation of converters based upon the Power-Group concept. Chapter 8 then investigates what converter topologies are most suited fore augmentation using power-groups. The final chapter then investigates the dynamic response of power-group augmented converters, several modifications to the converters circuit layout and control scheme are proposed to address issues highlighted by the fault study.

1.3.1 Original Contributions

The original contributions within this thesis by the author are detailed below:

The converter control system used within this thesis was developed by Dr. Michael Merlin, with some modifications to allow operation as the Hybrid MMC and the power-group augmented converters made by the author.

The lab-scale experimental converter detailed in Chapter 2 was designed and built collaboratively, with the people involved identified at the start of that chapter.

The work in Chapter 3, on developing a method for designing MMCs for a given P/Q specification, as well as the work on optimising the operating point of the Hybrid MMC are the work of the author, and was done with some helpful discussion and advice from Dr. Michael Merlin.

The heat-sink mounted thermal model of an IGBT and the IGBT power-loss blocked described in Chapter 4 were developed by the author based upon previous work in the literature, which is cited in the relevant sections. The analysis of the thermal and power-loss characteristics of the converters in this chapter are solely the work of the author.

The idea of using circulating currents to suppress the peak arm current within an MMC, examined in Chapter 5, had been proposed in the literature and the relevant citations are given. The author has expanded on this previous work and looked at how this impacts the converter design and operation when this method is applied to achieving a short-term overload capability, which has not previously been examined. The system study section of Chapter 5 was carried out collaboratively with Dr. Claudia Spallarossa and Dr. Inma Martinez-Sans.

The power-group concept, which is examined in Chapters 6-9, was proposed by the author, and is based upon a previous circuit proposed by the late Prof. Colin Oates who was involved in a consultancy project that was undertaken during the course of the author's PhD studies. The proposed power-group turn-on and turn-off procedures detailed in Chapter 7 were developed with some assistance and feedback from Dr. Michael Merlin and the engineers from Grid Solutions, who are identified at the start of Chapter 6. The power-group centralised controller developed in Chapter 7 is solely the work of the author. The converter topologies examined

Chapter 8 were identified through a collaborative process of investigation and discussion with the engineers from Grid Solutions, as well as Dr. Michael Merlin. The work on the dynamic and fault response of power-group augmented converters in Chapter 9 is solely the work of the author.

2 Design and Build of a Lab-Scale Multilevel Converter Demonstrator

This chapter describes the work that undertaken in designing, building and commissioning a lab-scale prototype multilevel converter which is used for experimental verification of results in several parts of this thesis. The build of the converter was a massive effort, taking three people who started with virtually no hardware design experience approximately 2 years to complete. Virtually every single PCB and system within the converter has undergone numerous revisions, hacks and upgrades, some of which will probably undergo at least another round of revisions in the future. At the time of writing a second converter of identical electrical specification is under construction, with numerous improvements to various parts of the design being implemented from the lessons learned in building the first converter.

My main partners in constructing the converter were Philip Clemow and Geraint Chaffey. Thanks should also go to Catriona Sheridan, Tom Luth, Michael Merlin and Claudia Spallarossa for their help with soldering various parts of the converter. Special thanks also to Michael for all of the work in adapting the simulation version of the converters controller into the implementation that runs on the hardware.

The completed converter integrated into its cabinet is shown in Fig. 2.1a. The Opal-RT OP5600 real-time controller occupies the upper part of the system. The grid interface transformer (bright orange) is at the base, various inductors (blue) can be seen in the middle of the converter. The sub-modules (black) are arrayed at the right-hand side of the converter. A view of the right-hand side of the cabinet, showing the array of 60 sub-modules, is shown in

Fig. 2.1b. The director switches for each arm, which allow operation as an AAC, are arrayed at the bottom and can be distinguished by their blue snubber capacitors.



(a) Front view (b) Array of sixty sub-modules

Figure 2.1: Multilevel converter demonstrator.

2.1 Converter Specification

The initial brief for the converter was for it to be capable of operating as either an MMC or as an AAC. Operation as an AAC requires full-bridge sub-modules, though to retain maximum flexibility the sub-module was designed with a tap connection that allows them to be operated as true half-bridges. The nominal specification for the converter is given in Table. 2.1. The

control for the converter was implemented on an Opal-RT OP5600 real-time simulation system. This allowed testing of the controller in simulation models before implementation in hardware. This allows changes to the controller to be rapidly implemented in the simulation model, before being compiled and loaded on to the Opal-RT controller.

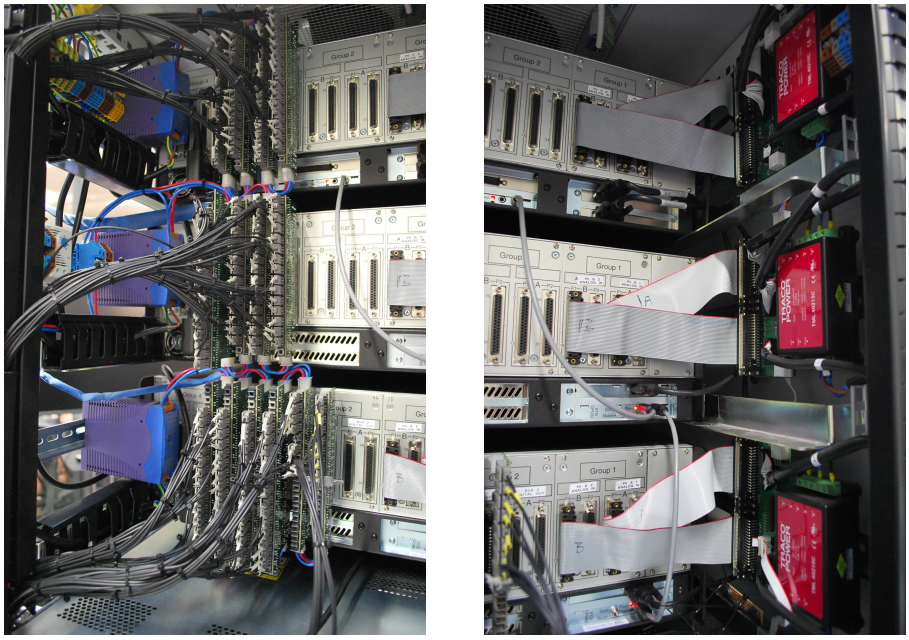
Table 2.1: Demonstrator Multilevel Converter Specification

Characteristic	Value
DC Voltage	+-750
Power Rating	15 kW
Number of Sub-Modules per Arm	10
Sub-Module Type	Half/Full-Bridge
AC Voltage	1170 V (AAC) / 950V (MMC)
Sub-Module Capacitor	500/770/890/1160 μF
Transformer Arrangement	Star-Delta
Transformer Turns Ratio	2.82

2.2 Controller and I/O system

The control signals from the OPAL to the sub-modules, as well as other ancillary circuits such as the contractor control boards, are transmitted though fibre-optic links. The use of fibre-optics ensures the OPAL remains isolated from the electrical circuit, as well as providing good noise immunity for the control signals. The OPAL's inbuilt digital out connections are connected to an optical out board, for transmission through fibre optics. This is shown in Fig. 2.2a.

Currents and voltages within the converter are measured using LEM voltage and current sensors, which provide isolated measurement using the Hall effect. The LEMs output a current output proportional to the measured current on the primary side. This current is sent through ribbon cables back to the OPAL analogue in measurement boards, shown in Fig. 2.2b, where they are terminated through a resistor. The OPAL then measures the voltage across this resistance. The signals are then scaled internally to give the correct magnitudes.



(a) Optic fibres for digital out commands

(b) Analog measurement boards and terminations

Figure 2.2: I/O Arrangement at the back of the Opal-RT controller.

Numerous currents and voltages are measured for control and measurement purposes within the converter. All six arm currents are measured, as well as the three secondary side AC currents and the two DC currents. All sixty sub-modules have separate capacitor voltage measurements. The primary and secondary side AC line voltages are measured, as well as each DC pole voltage.

2.3 Sub-Module Design

The sub-module is the most critical component within multilevel converters. As the converter is designed for experimental work the sub-module was designed to be robust to both over-current and over-voltage events. The sub-module design is shown from two angles in Fig. 2.3. The sub-module is composed of two boards, one of which contains the capacitor bank and LEM voltage transducer, and the other main board which contains the full-bridge arrangement of IGBTs, gate-drivers and associated control circuit. The IGBTs are mounted on a fan cooled

heat-sink which can be seen at the bottom of the board.

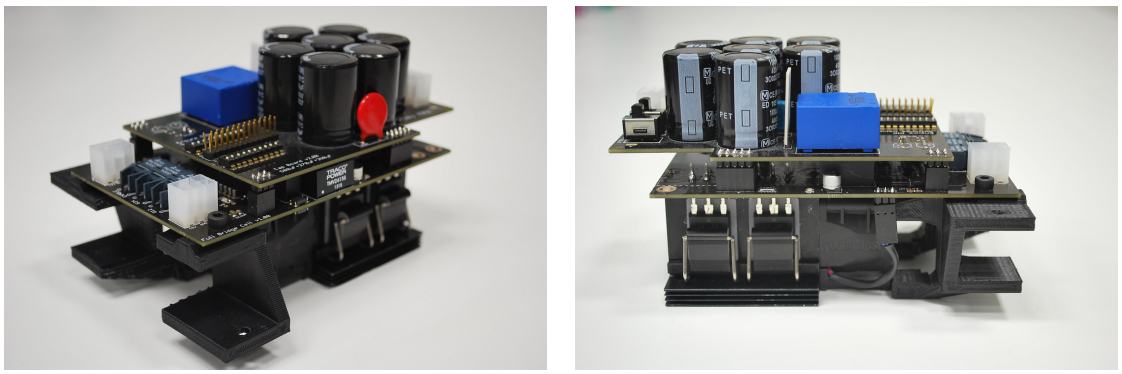


Figure 2.3: Sub-module design.

2.3.1 Control Circuit

A top-down view of the sub-module with the capacitor board removed is shown in Fig. 2.4. The board is electrically split into two parts. The right-hand side contains the power circuit, while the left hand side contains the control circuit, as well as the plugs which provide power to the board.

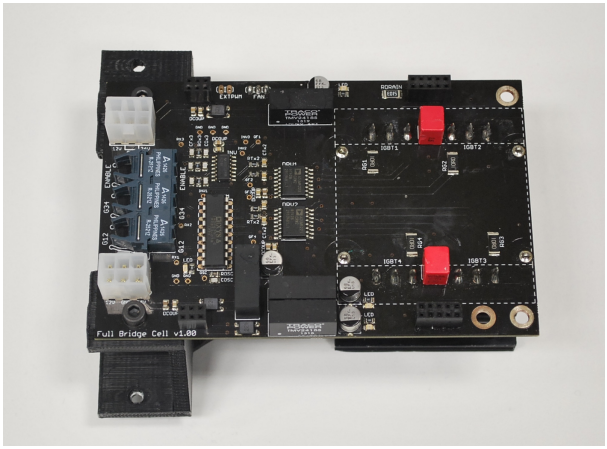


Figure 2.4: Top-view of main sub-module board.

On the left-hand side of the board, the power-plugs (white) can be seen. These were designed so that many sub-modules could be daisy-chained together, rather than providing separate leads to each sub-module. This plug contains a main 24V supply, and 12 V supply which is used to power the sub-modules, and a shared return path for both supplies. The 24 V supply is used to power the Traco Isolated DC-DC Converters which provide isolated power to the control circuit, as well as to the gate-drivers in the power circuit

The control circuit is electrically isolated from both the supply circuit, and from the power circuit. This was done to provide good noise immunity. Its power is derived through one of the Traco Converters which provides 5 V. The inputs to the control circuit are three optical receivers, which receive digital commands sent from the Opal-RT controller. These optical receivers can be seen on the left-hand side of the board, in between the two white plugs. The three signals are composed of an enable signal which de-blocks the sub-module when it is high, a signal that controls what state the left-hand side of the full-bridge is in, and a signal that controls what state the right hand side of the full-bridge is in. These signals from the optical receivers are passed through an inverting Schmitt trigger buffer, which acts as a buffer to the output for the optical receivers, as well as inverting the logic. The outputs of the Schmitt trigger is passed to an IXDP 630 PWM Control Chip (16 pin DIP chip). This chip implements the dead-time for each pair of IGBTs within the full-bridge, converting the three logical signals received from the optical receivers into four signals which are sent to inputs of the gate drivers. The length of dead-time applied by the PWM Control Chip is controlled by an RC oscillator pair. The gate-drivers used are ADUM 4223 isolated half-bridge drivers, one is used for each IGBT pair within the full-bridge. The input and output stage of the gate-driver is electrically isolated from each other.

2.3.2 Power Circuit

The power circuit occupies the right hand side of the board. An isolation barrier runs through the middle of the board, separating the control and power circuits. The ADUM 4223 acts as the

interface between the control and power circuits, bridging the isolation barrier. Three TRACO isolated power supplies provide power to the gate drivers on the power circuit. One of these TRACO's provides power for the two low-side IGBTs, while the two high-side IGBTs each have their own TRACO. The gate resistors for each IGBT can be seen at the top of the board in the centre. Two film capacitors (red) can be seen located between each IGBT pair. This provides high frequency filtering for the DC link in the sub-module. Two ten pin headers can are located at the top and bottom of the power circuit. These are where the electrical connection to the capacitor board is made. The external electrical terminals for the sub-module are located on the right-hand side of the board. The terminal at the top-right of the board connects to the mid-point of the left-hand IGBT pair. There are two terminal at the bottom-right of the board. The terminal closest to the edge connects to the mid-point of the right-hand IGBT pair. The other terminal is a tap point which connects to the negative point of the sub-modules DC bus. This tap allows the sub-module to be operated as a true half-bridge, electrically bypassing the right-hand IGBT pair.

The IGBTs used are IRGP4550DPBF ultrafast IGBTs rated to block 600 V and conduct a 50 A load current continually at a case temperature of 100^oC. The nominal peak current that the converter switches during normal operation is 10 A, while the nominal sub-module voltage, depending on converter topology, is in the region of 110-170 V. The IGBTs were chosen to be over-rated by such a large margin to account for fault situations. The IGBTs are mounted on a heat-sink which has its own cooling fan.

2.3.3 Capacitor Board

The capacitor board, which can be seen mounted on top of the sub-module in Fig. 2.3, contains the capacitor bank which forms the sub-module capacitor, as well as the LEM voltage transducer which provides isolated measurement of the capacitor bank. It connects electrically and mechanically to the main sub-module board through four sets of header pins, one pair of which is purely there for mechanical reasons.

The capacitor board has one main bank of five 100 μF capacitors in parallel. Switches then allow 270 μF and 390 μF capacitors to be added to this bank, giving four possible sub-module capacitor sizes. This variable capacitor arrangement was done as converter is designed to be capable of operating as several different topologies, each of which has different stored energy requirements. One design issue with this arrangement is the imbalance in size between some of the capacitors, leading to uneven current sharing between the capacitors. Future revisions of this board, which are being prototyped at time of writing, will feature three switch-able banks, each formed of different numbers of the same capacitor, ensuring more even sharing of current.

The current loop output of the LEM sensor is transmitted back to the analog measurement board at the OPAL through ribbon cables. One ribbon cable is shared between each set of 10 sub-modules within each arm.

2.3.4 Director Switch Design

The director switch within each arm, used for operation as an AAC, is formed of two series IGBTs, both driven by the same ADUM 4223 gate driver that is used within the sub-modules. It design is derived from the sub-module design and uses the same heat-sink and board dimensions. Its design is shown in Fig. 2.5.

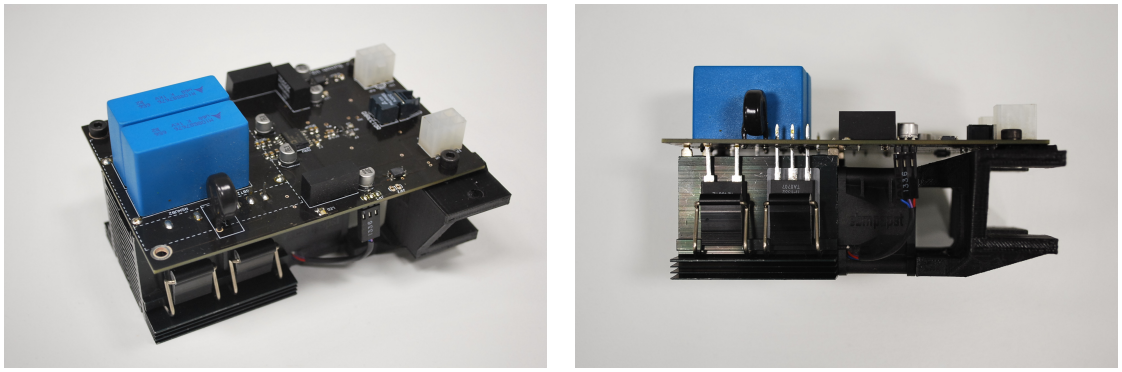


Figure 2.5: Director switch design.

The design target selected for the director switch was for it to be capable of safely switching a 2 pu over-current while blocking the entire pole-to-pole DC voltage of 1500 V. To achieve this two IXGX32N170H1 1.7 kV IGBTs operated in series were used. The propagation delay between the two channels of the gate-driver were measured and found to be less than one nanosecond. Under testing this was found to be close enough to ensure good transient sharing of voltage between the two devices during switching operations. To absorb the inductive energy stored within the arm inductors each IGBT has an RC snubber placed across it. The snubber capacitors (blue) can be seen mounted on top of the director-switch, while the snubber resistors, which are in a TO-247 package, are mounted on the heat-sink along with the IGBTs. A Metal Oxide Varistor (MOV) is also placed across each device, this can be seen on the top of board, mounted close to the snubber capacitor. This MOV protects the IGBTs in the event of an over-voltage.

2.4 Overall Experimental Set-up

The overall experimental set-up used for testing the converter is shown in Fig. 2.6. The external grid voltage is generated by a controllable 90 kVA TriPhase converter. This allows the AC voltage to be adjusted depending on which converter topology the multilevel converter is operating as. It is also capable of synthesising AC side faults.

The DC bus is formed of two series operated 1 kV, 15 kW DC power supplies. For operation during rectifying mode a bipole arrangement of 15 kVA TriPhase inverters is used in parallel with the DC supplies.

For simulating DC side faults (credit to Geraint Chaffey and Philip Clemow) a fault resistor and large IGBT are used. A protection circuit of thyristors are used to prevent the DC fault from being applied to the TriPhase Bipole converters.

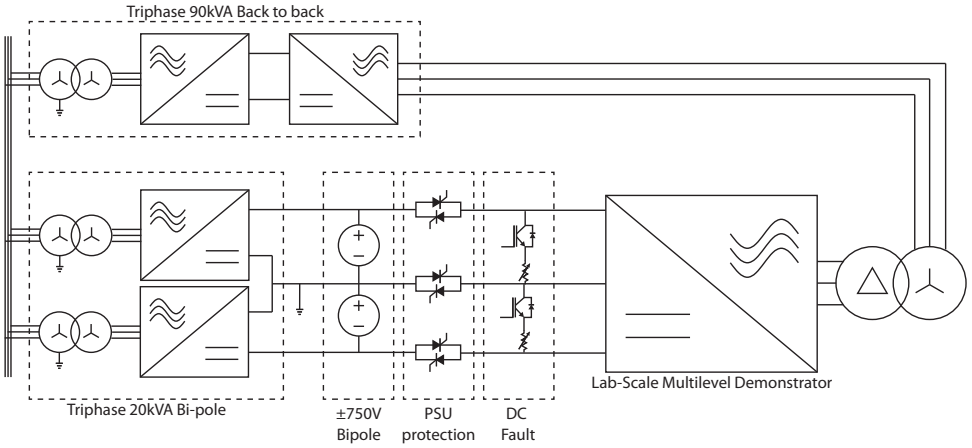


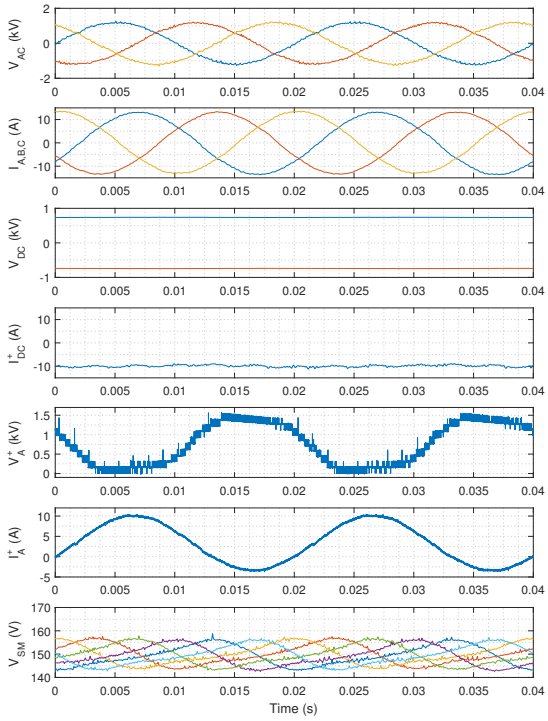
Figure 2.6: Experimental setup for testing of multilevel demonstrator converter - Credit: Philip Clemow

2.5 Experimental Results

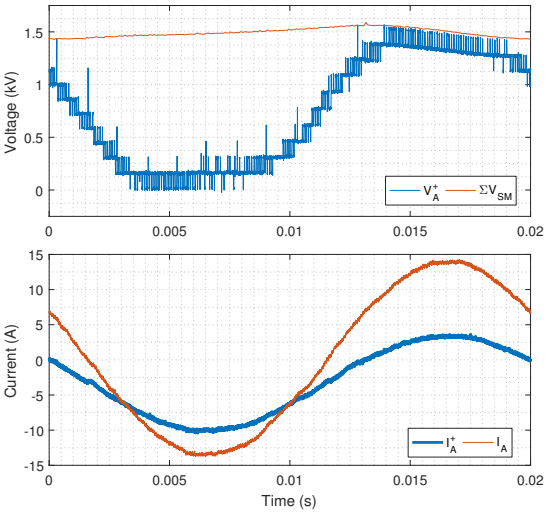
The converter is used to generate results in several chapters within this thesis. Some selected results and presented here to show the converters performance as both an MMC, and as an EO-AAC.

2.5.1 Operation as Modular Multilevel Converter

Results from the converter when operating as an MMC are shown in Fig. 2.7. The converter exhibits good performance, with high quality AC- and DC-side current waveforms. The sub-modules voltages are also well controlled to their nominal set-point.



(a) From Top: Converter AC line voltages, converter phase currents, DC pole to ground voltages, DC current, phase A upper arm stack voltage, phase A upper arm current, average SM voltage in each stack of SMs.



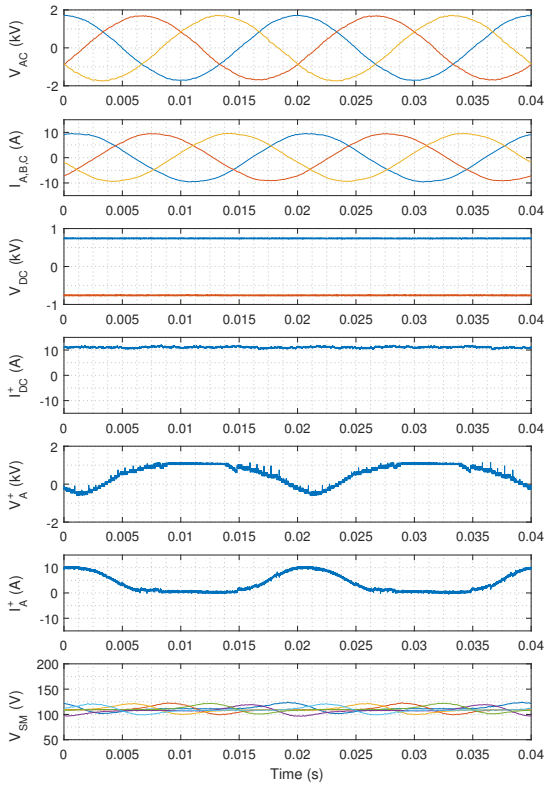
(b) One cycle of operation. Top: Phase A upper arm stack voltage, director switch voltage and sum SM voltage - Bottom: Phase A upper arm current and phase current.

Figure 2.7: Converter operating as an MMC at a set-point of 1 pu P and 0 pu Q.

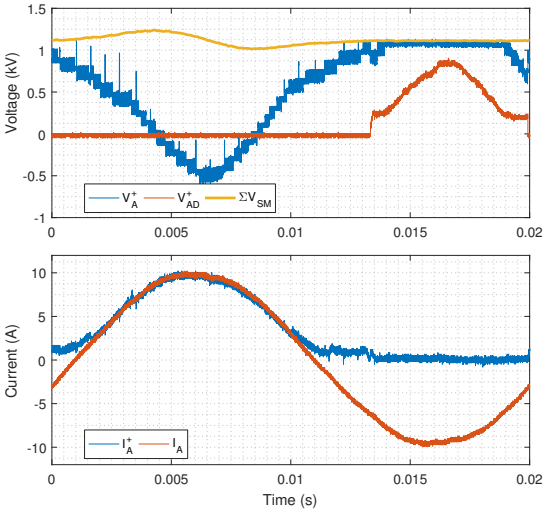
2.5.2 Operation as Alternate Arm Converter

Results from the converter when operating as an EO-AAC in steady-state at 1 pu active power (inverting) and 0.5 pu reactive power (capacitive) are shown in Fig. 2.8a. The converter exhibits good performance, capable of generating low distortion AC side current waveforms. The DC current is also free from six-pulse ripple, verifying the EO-AACs ability to generate a smooth DC current without the need for a large DC side filter. The sub-module voltages are also stable around their nominal set-point.

The voltage generated by each stack of sub-modules, the average SM voltages within each stack, and director switch voltage of the upper arm of phase A over one cycle are shown in the



(a) From Top: Converter AC line voltages, converter phase currents, DC pole to ground voltages, DC current, phase A upper arm stack voltage, phase A upper arm current, average SM voltage in each stack of SMs.



(b) One cycle of operation. Top: Phase A upper arm stack voltage, director switch voltage and sum SM voltage - Bottom: Phase A upper arm current and phase current.

Figure 2.8: Converter operating as an EO-AAC at a set-point of 1 pu P and 0 pu Q.

upper plot of Fig. 2.8b. The lower plot shows the arm current overlaid with the phase current. It can be seen that for part of the cycle, the arm is conducting only the phase current. During the overlap periods, the arm is conducting the phase current from a different phase, as well as the DC current. When the director switch is open, the arm is not conducting and the director switch and stack of sub-modules work together to generate the necessary voltage.

2.5.3 DC Fault Test

The results from the EO-AAC withstanding a 200 ms fault on the DC bus is shown in Fig. 2.9. Pre-fault the converter was set to -1 pu active power (rectifying) and -0.5 pu reactive power (inductive). The controller is set to retain the reactive power set-point through the DC fault. The results of this test are shown in Fig. 2.9.

At the instance of the fault, the DC bus voltage rapidly collapses with a large spike of the DC current from the DC bus capacitor which reaches 68.5 A. This peak current is shown off the scale of the plot to show the finer details of the DC current during the test. The DC bus under-voltage event is detected by the control system, and the converter does not contribute to the DC side fault current. The converter maintains good control over the AC side currents, quickly dropping its active power and moving into STATCOM mode. The DC current can be seen to go to zero after the DC bus capacitor has been drained.

After fault clearance the converter recharges the DC bus and resumes active power flow. As the DC current is measured outside the DC bus capacitor, no current is measured during the recharging stage until the bus voltage becomes high enough to forward bias the protection thyristors.

The converter exhibits good ability to maintain the energy levels within the sub-modules during the DC fault. A slight disturbance is seen at the start of the fault, however the energy management system prevents the sub-modules from running away from their set-point. After the fault clears, the sub-modules are returned to their nominal voltage levels within approximately 100 ms.

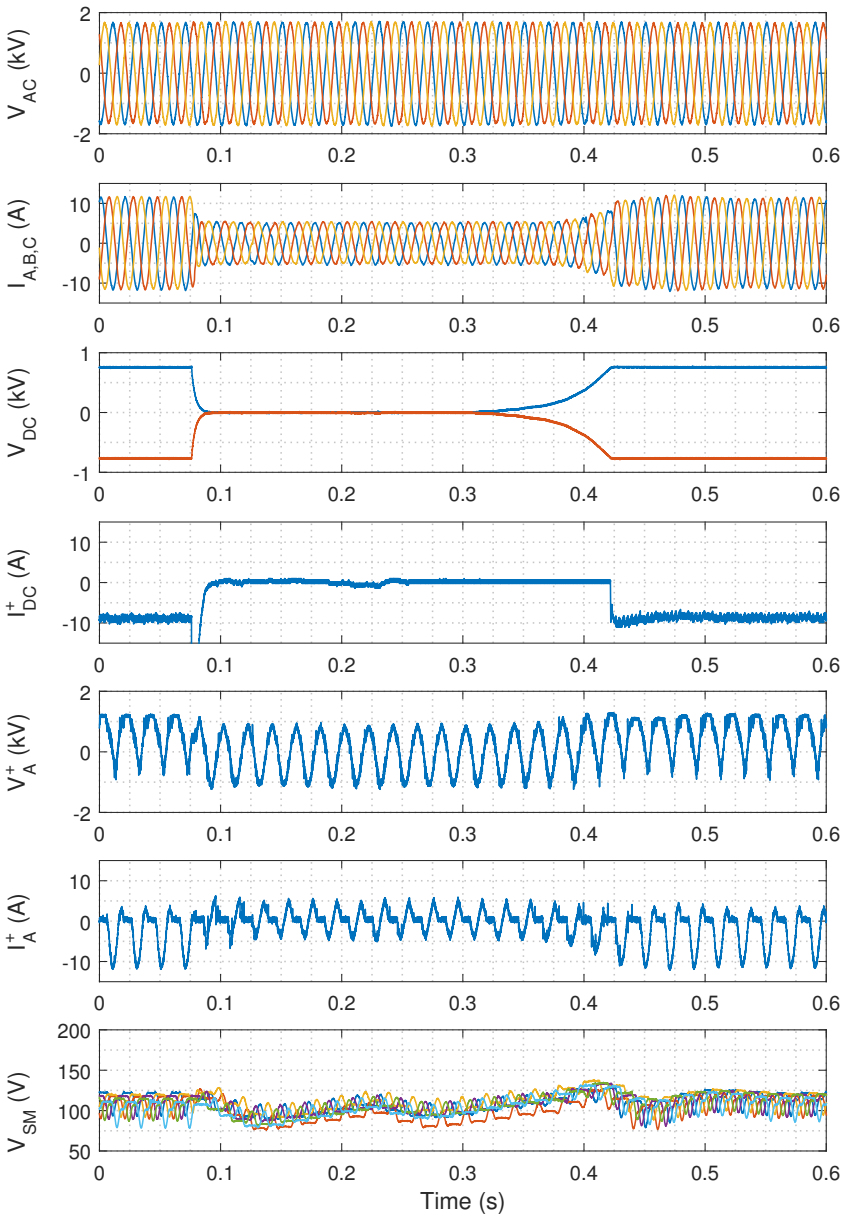


Figure 2.9: DC pole to pole fault with a 9.4 Ω fault impedance. Pre-fault set-point is -1 pu P and -0.5 pu Q. The format is the same as in Fig. 2.8a.

3 Design of Modular Multilevel Converters

In this chapter, the design of Modular Multilevel Converters is investigated, with an emphasis on the sizing of the sub-module capacitor and how this impacts the required number of sub-modules in the converter. Analytic expressions for the current, voltage, power and energy deviation of a stack of sub-modules within a converter stack are derived as a function of the converters power set-point. These expressions are then used as the basis of a methodology that has been developed to design a half-bridge MMC for a given P/Q specification. The requirements for voltage source converters specified by the Grid Code of the Great Britain network are used to provide a realistic design specification. The analysis for the MMC is then expanded to cover the case of the Hybrid MMC, which is designed to be tolerant to DC faults.

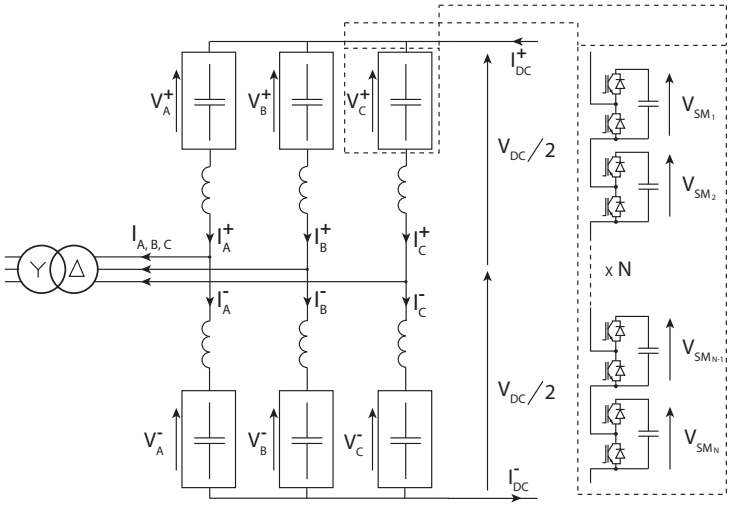


Figure 3.1: Schematic of Modular Multilevel Converter

3.1 Overview of Major Works in Literature

The MMC was introduced as a concept in [18]. Its basic operation is described as well as early control strategies for controlling the voltage of each sub-module within the converter. The main advantages of the converter are identified, namely its modularity and easy scalability, as well as the high quality waveforms that are achievable without any AC or DC side filtering equipment.

In [35] the authors investigate the interaction between the AC voltage and power set-points, and the internal voltages and currents within the MMCs. The analysis is based upon the voltage references for each stack of sub-modules, which are set as sinusoidal references which sets the number of sub-modules that are inserted within each stack. As this techniques does not account for the time-varying voltage within each sub-module some error is introduced between the requested stack voltage, and the generated stack voltage. This causes a circulating current to flow through the converter, which the analysis correctly predicts.

In [46], the required level of energy storage within an MMC is investigated. An expression for the minimum energy storage requirement as a function of the peak rated sub-module voltage, nominal stack voltage and peak to peak energy deviation of the stack is derived. The possibility of changing the nominal sub-module voltage depending on the converters set-point is also explored. A case study finds that the minimum required energy level within a grid connected MMC operated with third harmonic injection is in the region of 21 kJ/MVA, when only set-points at unity power factor are considered.

In [39], the required sub-module capacitor size in both the modular multilevel converter, as well and the alternate arm converter is investigated. The analysis is based on the assumption that the ripple on the sub-module capacitor voltages be limited to +-10% of their nominal value. The papers find that in the case of the MMC, the minimum energy storage requirement to achieve this is in the region of 39 kJ/MVA, while in the case of the AAC the minimum energy storage requirement is 12.5 kJ/MVA

In [47], the internal dynamics and control of MMCs are investigated. This paper proves that the MMC can be analysed based upon the sum capacitor voltage, rather than the individual

capacitor voltages, which simplifies the analysis. Expressions for the capacitor ripple voltage are derived. Two controllers, which compensate for the capacitor ripple voltage and so reduce the magnitude of any circulating current within the converter are also introduced.

In [48], two modulation methods for MMCs are compared. The first is direct modulation whereby the reference signal for each stack directly controls the number of inserted sub-modules. The second is modulation reference method takes account of the ripple on the capacitor voltage, and so does not introduce an unintentional circulating current

In [49], a design methodology for dimensioning MMCs from an industrial perspective is presented. Unlike most other papers on the design of MMCs, this paper takes both the impact of the converter transformer, and the variation in the AC voltage magnitude into account. Guidelines on the expected leakage reactance of a transmission scale transformer are given, as well as the required size of the arm inductors.

3.1.1 Converter Design Requirements

As discussed in [49], HVDC converters must be designed so that they are capable of meeting their contractual obligations for available active and reactive power capability. They must do this while also meeting specifications for harmonic distortion and remaining competitive in terms of efficiency. The GB Grid code gives the following specifications for grid connected voltage source converters:

- Be capable of operating at full rated active power at a leading power factor of 0.95, and a lagging power factor of 0.85, over an AC voltage variation of $\pm 5\%$.
- Be capable of remaining transiently stable through any AC side fault for a duration of 140 ms, and be capable of resuming at least 0.9 pu of pre-fault power within 0.5 seconds.
- Reduce active power output under AC fault conditions in proportion to the drop in AC voltage magnitude.

These requirements are used as the basis for the design of the converters in the following sections.

3.2 Operating Limits

To make the best utilisation of the sub-modules the converter should be designed so that it can properly operate across its entire P/Q specification. The design of the converter should be so that a good balance between both the capital cost of the converter, and efficiency is reached. The P/Q capability of multilevel converters is limited by four factors, which will be described in the following subsections.

3.2.1 Current Limit

There is a limit imposed on converters P/Q capability by the peak current that the IGBTs within the converter can reliably continuously switch during normal operation. As will be discussed in Section. 5.1.2, the IGBTs within the converter may be capable of switching off currents significantly higher than the peak current rating of the valve. However they may not be able to do so continuously due to the large thermal shock associated with switching off such large over-currents. In addition fault events can cause a loss of current control, and so the peak rating of the valve must be chosen so that the worst case over-current event can still be safely turned-off by the IGBTs.

3.2.2 Peak Sub-Module Voltage Limit

One key design aspect of the sub-modules within MMCs, that will have a strong impact on the expected reliability of both the IGBTs and sub-module capacitor, is the peak rated voltage that the sub-module is designed to be capable of continuously operating at [49]. To prevent this peak rated voltage from being breached during normal operation, the nominal voltage that the sub-modules are operated at must be chosen so that the peak voltage reached by the sub-

modules under the worst case normal operating condition does not exceed this limit. This is illustrated in Fig. 3.2.

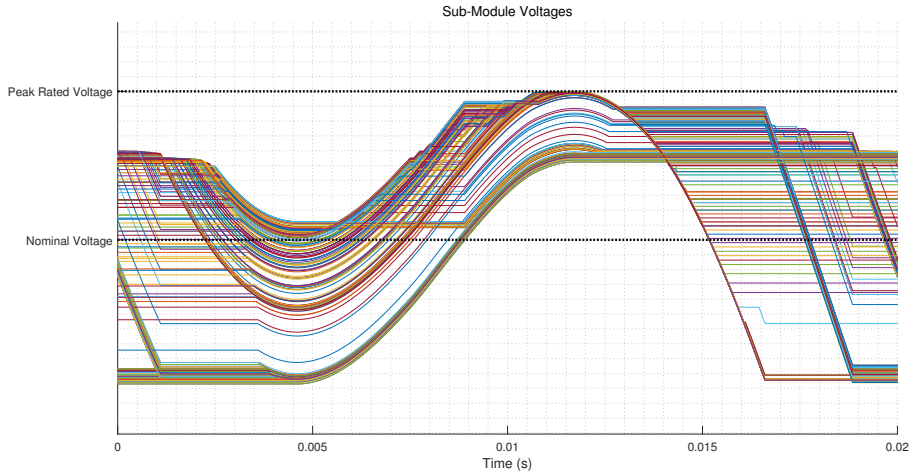


Figure 3.2: Sub-module voltages fluctuating around the nominal voltage, but staying below the peak rated voltage, over the course of one cycle.

A HVDC converter might be expected to have a service life of 20-30 years (175200-262800 hours), with maintenance intervals every 1-2 years. To achieve this the sub-modules themselves must be designed for reliable operation. The failure rate of IGBTs and diodes is strongly influenced by the DC bus voltage that they are operated at [50]. This is due to cosmic ray induced failure mechanisms. For example, taking the data from [50], the failure rate due to cosmic ray induced mechanisms for an ABB 5SNA 1200E330100 device operated at a DC bus voltage of 2000V is 50 Failure in Time[1] (FIT), while at 2100V it is 1200 FIT, and at 2200V it is 7000 FIT.

The film capacitors used within power applications also have limitations on the peak voltage that they can withstand. Events like an over voltage can cause a breakdown in the plastic film dielectric that is used to form the capacitor [51, 52]. Film capacitors have a self-healing property under this condition whereby the breakdown causes a plasma to be formed by the dielectric at

[1]The term Failure in Time (FIT) is defined as a failure rate of 1 per billion hours of operation

the breakdown point within the layer. This plasma evaporates the metal conducting layer near the breakdown region, the rapid expansion of this combined plasma then cools and causes an insulating layer to be formed over the breakdown region, stopping the discharge. Other events like partial-discharge caused by air bubbles being formed between the internal layers of the capacitor also cause damage and a reduction in the overall capacitance of the capacitor. Both of these events are related to the voltage stress applied across the capacitor, as well as external factors such as temperature and humidity.

3.2.3 Voltage Limits

If the converter is put into a situation where it can no longer generate the necessary voltage, then the converter will lose some measure of current control. The effects of this could vary from a small disturbance to the harmonic quality of the current waveforms, to a dangerous over-current event. There are two voltage limits that restrict a half-bridge MMC's P/Q capability, both of which are illustrated in Fig. 3.3, and are detailed in the paragraphs below.

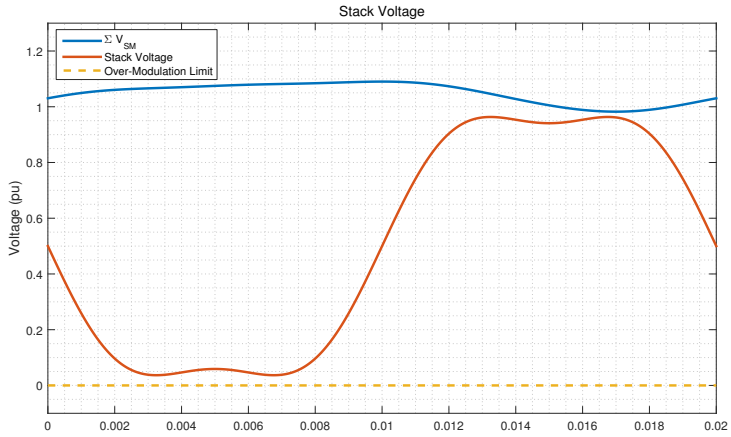


Figure 3.3: Voltage generated by a stack of sub-modules within an MMC. The sum voltage capability of the sub-modules defines the maximum voltage that can be generated by the stack, while the use of half-bridge sub-modules prevents the stack from generating a negative voltage output.

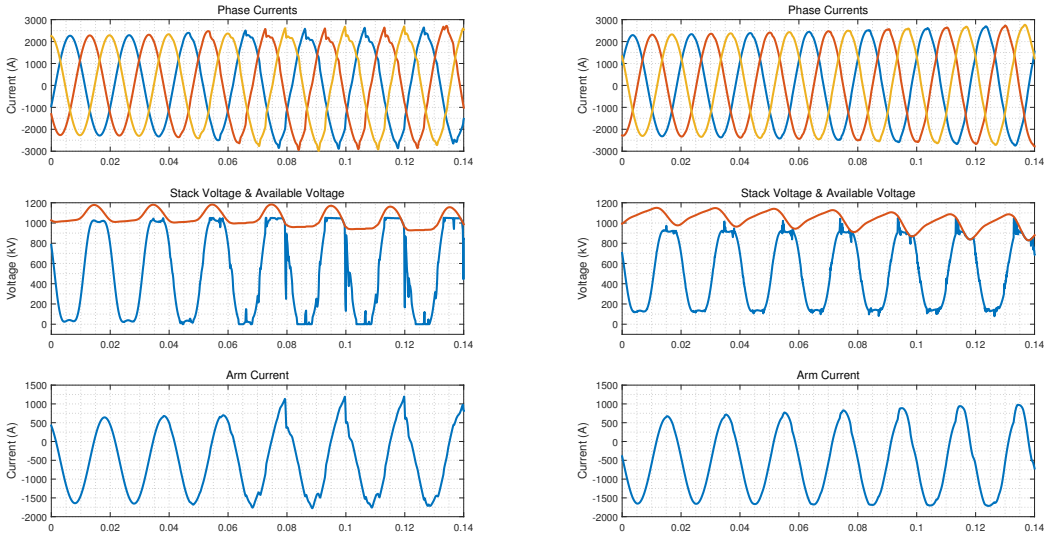
The first voltage limit that restricts an MMC's P/Q capability is termed the *over-modulation limit* within this thesis. The peak phase voltage that the converter can generate is bound by the DC pole voltage. In a half-bridge MMC that uses half-bridge sub-modules, the minimum voltage that a stack can generate is limited to zero volts. This prevents the converter from generating a voltage greater than the DC pole voltage. Attempting to generate a voltage higher than the DC pole voltage (i.e attempting to over-modulate) will result in an uncontrolled current flow from the AC to the DC system, with a potential disturbance to the DC voltage levels of the system.

The other voltage limit imposed on the converters P/Q capability is termed the *stack voltage limit*. This limit is imposed by the voltage capability of each stack of sub-modules within the converter, given by the instantaneous sum of the capacitor voltages within each stack. Due to the cycle-by-cycle ripple imposed on the sub-module capacitor voltages, the voltage capability of each stack is a time varying value. If the converter attempts to generate a voltage greater than the available voltage within the stack, then the stack will saturate to this value, leading to a loss of current control as the converter can no longer meet the voltage demand from the current controller.

Figure 3.4 shows two simulation results of an MMC losing current control. The first simulation shows it losing control due it breaching the over-modulation limit, and the second due to breaching the stack voltage limit. The results shown focus on one arm of the converter. In the case of the loss of current control due to breaching the over-modulation limit, shown in Fig. 3.4a, the converters capacitive power set-point was increased while its active power set-point was set to a fixed amount. As the reactive power set-point increases the converter attempts to over-modulate its output but cannot, resulting in current control being lost. This result in distortions to both the phase currents and to the arm currents. The initial loss of current control due to the attempt to over-modulate then results in a disturbance to the energy levels within the converter, resulting in the stack voltage limit then being breached.

In the case of loss of current control due to breaching the stack voltage limit, shown in

Fig. 3.4b, the converters inductive reactive power was ramped upwards while its active power set-point was fixed. In this case the voltage that the converter must generate reduces. However the sum voltage ripple on the sub-module capacitors increases, causing the available voltage within the stack of sub-modules to intersect with the requested demand from the current controller. The stack can no longer generate the required voltage and distortions to the arm current waveforms result.



(a) Current control loss due to a breach of the over-modulation limit.

(b) Current control loss due to a breach of the stack voltage limit.

Figure 3.4: Current control loss in a modular multilevel converter.

3.3 Half-Bridge Modular Multilevel Converter

This section details a derivation of general expressions for the currents, voltages, power exchange, and energy deviation of the stacks of sub-modules within a modular multilevel converter. These derivations are then used to formulate a dimensioning methodology for rating an MMC for a given P/Q specification, whilst making the best utilisation of the sub-modules within the converter. This method is easily automated, which allows numerous designs to be

compared. This design methodology for the half-bridge MMC is then later modified for the case of the Hybrid MMC, which is detailed in Section. 3.4.

3.3.1 Derivation of expressions for the converters internal voltage, current and energy deviation waveforms

This subsection details the derivation of expressions for the arm currents, the stack voltage, and the stack energy deviation as a functions of the converters set-point, AC voltage magnitude, DC voltage magnitude, arm inductor size, and leakage inductance of the converters grid interface transformer. The derived expressions are then later used to design the converter for a given P/Q specification.

For clarity the following definitions are used within this thesis. A converter arm refers to all components that are located between the AC phase connection point at the converter side of the grid interface transformer, and and a DC connection point. The MMC therefore has six arms, two per phase, each containing an arm inductor and a series arrangement of sub-modules. The arm within a phase that connects the AC point to the positive DC connection point is referred to as the upper arm, while the arm that connects the AC point to the negative DC terminal is referred to as the lower arm. An arm current refers to the current flowing through one of these arms. The stack voltage refers to the voltage generated by the stack of sub-modules within a converter arm, excluding any voltage across any inductance within the arm.

The following definitions for the power generated by the converter are used, and are illustrated in Fig. 3.5. Positive active power refers to power that is delivered from the DC system to the AC system (inverting), while negative active power refers to power delivered from the AC system to the DC system. Positive reactive power is capacitive (i.e the converter is generating a voltage higher than the AC grid it is connected to) while negative reactive power is inductive (i.e the converter is generating a voltage lower than the AC grid it is connected to).

The derivations are done using the assumption that the ratio of the AC to DC voltage ratios is a variable. In a half-bridge MMC, this ratio has strict limits imposed by the converter inability

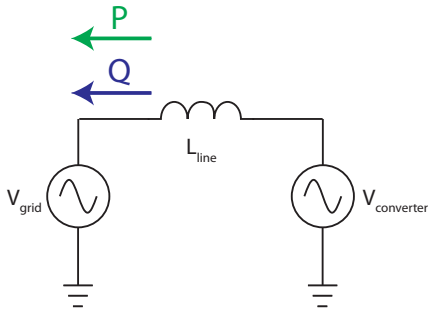


Figure 3.5: Real and reactive power definition used within thesis. Positive active power is power delivered by the converter from the DC system to the AC system. Positive reactive power is capacitive power delivered to the AC system.

to generate a voltage higher than its DC pole voltage. However later in the chapter, an MMC variant which is capable of over-modulating is considered.

The modulation index of the converter, m, is used to define as the ratio between the nominal peak phase voltage, to the DC pole voltage, as given in (3.1). A modulation index of 1 implies that the converter is generating an AC voltage waveform in which the peak of the phase voltage is equal that of the DC pole voltage.

$$V_{\text{phase}}(\omega t) = m\frac{V_{DC}}{2}sin(\omega t) \tag{3.1}$$

In this work the modulation index is chosen to refer to the relationship between the magnitudes of the peak AC phase voltage at the point-of-common coupling with the grid, and the nominal DC voltage at the positive pole of the DC bus. The voltage at this point can be written as (3.2). K_{AC} is used to represent the variation in the AC voltage around its nominal value. This variation is typically in the region of $\pm 5\%$.

$$V_{\text{pcc}}(\omega t) = mK_{\text{AC}}\frac{V_{\text{DC}}}{2}sin(\omega t) \tag{3.2}$$

Rearranging (3.2) allows the RMS line voltage to be expressed as a function of the modulation index, and the DC voltage, as given in (3.3).

$$V_{\mathrm{LL}} = mK_{\mathrm{AC}}\frac{V_{\mathrm{DC}}}{2}\sqrt{\frac{3}{2}} \tag{3.3}$$

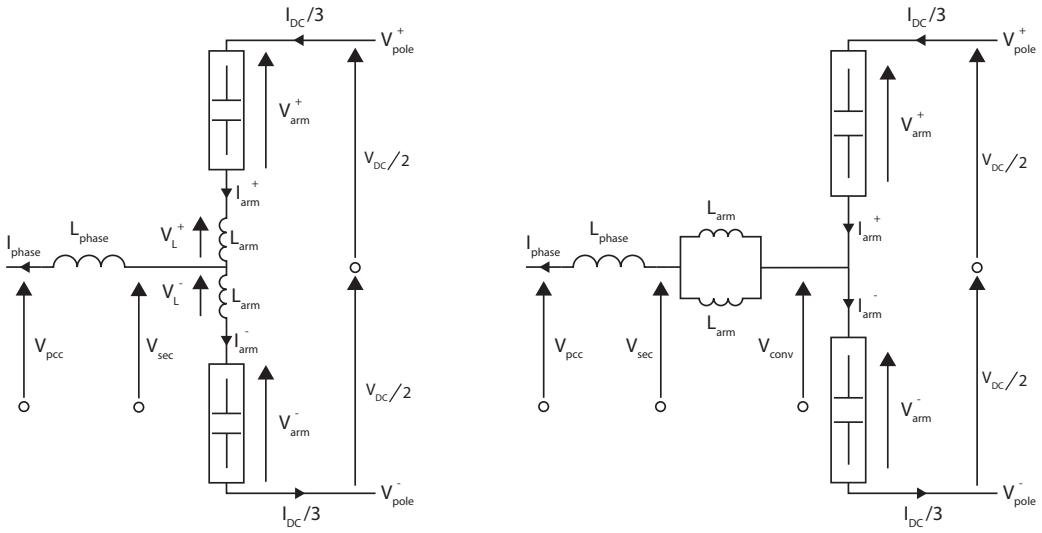
The converter will typically be interfaced to the AC grid through a transformer. This allows the voltage at the converter side of the transformer to be selected to make the most utilisation of the DC terminal voltage. The inclusion of a delta winding on the converter side of the transformer also prevents any zero sequence components from entering the AC system. This also gives the added benefit of allowing the converter to be operated with third harmonic injection, enabling the converter to boost its AC voltage output by an additional 15% [53].

The leakage inductance of a transmission scale transformer is significant, in the region of 0.14 pu [49]. The voltage rise across the converter transformer can therefore not be ignored when calculating the internal voltage waveforms within the converter. In addition, any any P/Q set-point calculation should be done referenced to the converters point of common coupling (PCC) with the AC grid, rather than at the converter terminals. Failing to do so ignores the relatively large reactive power demand of the transformer itself. In addition to the leakage reactance of the transformer, the MMC also has inductors located within each arm of the converter. These exist for control purposes, and to limit the rate of rise of current through the converter during fault scenarios. A single phase presentation of an MMC is shown in Fig. 3.6a, where L_{phase} is the leakage reactance of the converter transformer, and L_{arm} gives the size of the arm inductors.

In an MMC, the phase current is split evenly between the upper and lower arms. The result is that the voltage placed across the upper and lower arm inductors are equal in magnitude, but electrically shifted by half a cycle. The voltage at the top of the upper inductor, and the voltage at the bottom of lower arm inductor are therefore the same. This means that from the AC side, the two phase inductors appear in parallel, while they represent no impedance from the DC side during steady-state operation [54].

To simplify the analysis, it is useful to exploit this fact and do the analysis based on a virtual AC point (V_{c}), that represents the voltage at the top of the upper arm inductor, and the bottom of the lower arm inductor. This allows the converter to be represented as in Fig. 3.6b, with the

arm inductors appearing in parallel with each other, and in series with the leakage reactance of the transformer.



(a) Arm inductors included within the arms of the converter.

(b) Arm inductors referenced to AC side.

Figure 3.6: Single phase representations of a modular multilevel converter.

The voltage at the this virtual point, V_{c}, can be then calculated from (3.4), where $\overline{S_{\mathrm{pcc}}}$ is the complex power as measured at the pcc.

$$V_{\mathrm{c}} = V_{\mathrm{pcc}} + \frac{\overline{S_{\mathrm{pcc}}}^{*}}{V_{\mathrm{pcc}}} j\omega(L_{\mathrm{phase}} + \frac{L_{\mathrm{stack}}}{2}) \tag{3.4}$$

This can be expressed using the per unit system as in (3.5).

$$\begin{aligned} V_{\mathrm{conv_{pu}}} &= K_{\mathrm{AC}} + \frac{\left|S_{\mathrm{pcc_{pu}}}\right|^{*}}{K_{\mathrm{AC}}} j(X_{\mathrm{phase_{pu}}} + \frac{X_{\mathrm{arm_{pu}}}}{2}) \\ &= \big(K_{\mathrm{AC}} + \frac{\left|S_{\mathrm{pcc_{pu}}}\right|}{K_{\mathrm{AC}}} \sin(\phi_{\mathrm{pcc}})(X_{\mathrm{phase_{pu}}} + \frac{X_{\mathrm{arm_{pu}}}}{2})\big) + j\big(\frac{S_{\mathrm{pcc_{pu}}}}{K_{\mathrm{AC}}} \cos(\phi_{\mathrm{pcc}})(X_{\mathrm{phase_{pu}}} + \frac{X_{\mathrm{arm_{pu}}}}{2})\big) \end{aligned} \tag{3.5}$$

The voltage at V_{c} can then expressed as in (3.6), where the value of K_{c} is given by (3.7).

$$V_{\mathrm{c}}(wt) = mK_{\mathrm{c}}V_{\mathrm{DC}}\sin(\omega t) \tag{3.6}$$

$$K_{\mathrm{c}} = \sqrt{\left(K_{\mathrm{AC}} + \frac{\left|S_{\mathrm{pcc_{pu}}}\right|}{K_{\mathrm{AC}}}\sin(\phi_{\mathrm{pcc}})(X_{\mathrm{phase_{pu}}} + \frac{X_{\mathrm{arm_{pu}}}}{2})\right)^2 + \left(\frac{\left|S_{\mathrm{pcc_{pu}}}\right|}{K_{\mathrm{AC}}}\cos(\phi_{\mathrm{pcc}})(X_{\mathrm{phase_{pu}}} + \frac{X_{\mathrm{arm_{pu}}}}{2})\right)^2} \tag{3.7}$$

To calculate the phase current it is also useful to calculate the AC side power as measured at V_{conv}. This can be calculated as in (3.8).

$$\begin{aligned}
\overline{S_{\mathrm{conv_{pu}}}} &= \overline{V_{\mathrm{conv_{pu}}}} \times \overline{I_{\mathrm{phase_{pu}}}}^{*} \\
&= \left(K_{\mathrm{ac}} + \frac{\overline{S_{\mathrm{pcc_{pu}}}}^{*}}{K_{\mathrm{ac}}} j(X_{\mathrm{phase_{pu}}} + \frac{X_{\mathrm{arm_{pu}}}}{2})\right)\frac{\overline{S_{\mathrm{pcc_{pu}}}}}{K_{\mathrm{ac}}} \\
&= \overline{S_{\mathrm{pcc_{pu}}}} + j\frac{\overline{S_{\mathrm{pcc_{pu}}}}^{*}\overline{S_{\mathrm{pcc_{pu}}}}}{{K_{\mathrm{ac}}}^2}(X_{\mathrm{phase_{pu}}} + X_{\mathrm{arm_{pu}}}/2) \\
&= \overline{S_{\mathrm{pcc_{pu}}}} + j\frac{\left|S_{\mathrm{pcc_{pu}}}\right|^2}{{K_{\mathrm{ac}}}^2}(X_{\mathrm{phase_{pu}}} + X_{\mathrm{arm_{pu}}}/2)
\end{aligned} \tag{3.8}$$

3.3.1.1 Derivation of Arm Current

The currents flowing through the converter can then be derived based upon the converters P/Q set-point and the AC voltage magnitude, in this analysis both referenced to V_{c} .

The phase current, I_{phase}, can be given as in (3.9), where ϕ_{c} is given by $\angle S_{\mathrm{c}}$.

$$I_{\mathrm{phase}}(\omega t) = \sqrt{\frac{2}{3}}\frac{|S_{\mathrm{c}}|}{V_{\mathrm{c}}}\sin(\omega t - \phi_{\mathrm{c}}) \tag{3.9}$$

Subbing in (3.3) allows the phase current to be given in terms of the DC voltage and the modulation index. This is given in (3.10).

$$I_{\text{phase}}(\omega t) = \frac{2}{3}\frac{|S_{\text{c}}|}{mK_{\text{c}}V_{\text{DC}}}\sin(\omega t - \phi_{\text{c}}) \tag{3.10}$$

The DC current can be expressed as in (3.11), where K_{DC} is a scalar used to represent any deviation of the DC voltage from its nominal value.

$$I_{DC} = \frac{|S_{\text{c}}|\, cos(\phi_{\text{c}})}{2K_{\text{DC}}V_{\text{DC}}} \tag{3.11}$$

In an MMC operating under balanced conditions the phase current is split evenly between the upper and lower arms, whilst the DC current is divided equally between all three phase legs. The arm current flowing through the upper arm of a phase leg can then be expressed as in (3.12).

$$I_{\text{stack}}(\omega t) = \frac{|S_{\text{c}}|}{3mK_{\text{c}}V_{\text{DC}}} sin(\omega t - \phi_{\text{c}}) + \frac{|S_{\text{c}}|\, cos(\phi_{\text{c}})}{6K_{\text{DC}}V_{DC}} \tag{3.12}$$

3.3.1.2 Derivation of the power and energy exchange of a stack of sub-modules

The voltage generated by the stack of sub-modules within the upper arm of the converter, V_{stack}, is given by the difference between the DC voltage and the voltage at V_{c}. Assuming the use of third harmonic injection, with the magnitude of the third harmonic given by a scalar (K_{3rd}) relative to the magnitude of the fundamental, the voltage of the stack can be written as in (3.13).

$$V_{\text{stack}}(\omega t) = K_{\text{DC}}V_{\text{DC}} - \left(mK_{\text{c}}V_{\text{DC}}\sin(\omega t) + K_{\text{3rd}}mK_{\text{c}}V_{\text{DC}}\sin(3\omega t)\right) \tag{3.13}$$

The power exchange of the stack can then be written as a product of the arm current and the stack voltage as in (3.14).

$$P_{\text{stack}}(\omega t) = \Big(K_{\text{DC}}V_{\text{DC}} - \big(mK_{\text{c}}V_{\text{DC}}\sin(\omega t) + K_{3\text{rd}}mK_{\text{c}}V_{\text{DC}}\sin(3\omega t)\big) \times \Big(\frac{|S_{\text{c}}|}{3mK_{\text{c}}V_{\text{DC}}}\sin(\omega t - \phi_{\text{c}}) + \frac{|S_{\text{c}}|\cos(\phi_{\text{c}})}{6V_{\text{DC}}}\Big) \quad (3.14)$$

Expanding terms, P_{stack} can be then be written as (3.15).

$$P_{\text{stack}}(\omega t) = \frac{|S_{\text{c}}|}{3}\Bigg(\frac{K_{\text{DC}}}{K_{\text{c}}m}\sin(\omega t - \phi_{\text{c}}) + \frac{1}{2}\cos(\phi_{\text{c}}) - \sin(\omega t)\sin(\omega t - \phi_{\text{c}}) - \frac{mK_{\text{c}}}{2K_{\text{DC}}}\cos(\phi_{\text{c}})\sin(\omega t) - K_{3\text{rd}}\sin(3\omega t)\sin(\omega t - \phi_{\text{c}}) - \frac{K_{3\text{rd}}mK_{\text{c}}}{2K_{\text{DC}}}\cos(\phi_{\text{c}})\sin(3\omega t)\Bigg) \quad (3.15)$$

Integrating this stack power allows the exchange of energy between the stack of sub-modules and the AC and DC systems, ΔE_{stack}, to be derived. This is given in (3.16).

$$\Delta E_{\text{stack}}(\omega t) = \frac{|S_{\text{c}}|}{3\omega}\Bigg(-\frac{K_{\text{DC}}}{mK_{\text{c}}}\cos(\omega t - \phi_{\text{c}}) + \frac{1}{2}\cos(\phi_{\text{c}})\omega t + \frac{1}{4}\sin(2\omega t - \phi_{\text{c}}) - \frac{1}{2}\cos(\phi_{\text{c}})\omega t + \frac{mK_{\text{c}}}{2K_{\text{DC}}}\cos(\omega t)\cos(\phi_{\text{c}}) + \frac{K_{3\text{rd}}}{8}\big(\sin(4\omega t - \phi_{\text{c}}) - 2\sin(2\omega t + \phi_{\text{c}})\big) + \frac{K_{3\text{rd}}mK_{\text{c}}}{6K_{\text{DC}}}\cos(\phi_{\text{c}})\cos(3\omega t)\Bigg) \quad (3.16)$$

Simplifying this gives (3.17)

$$\Delta E_{\text{stack}}(\omega t) = \frac{|S_{\text{c}}|}{3\omega}\Bigg(-\frac{K_{\text{DC}}}{mK_{\text{c}}}\cos(\omega t - \phi_{\text{c}}) + \frac{1}{4}\sin(2\omega t - \phi_{\text{c}}) + \frac{mK_{\text{c}}}{2K_{\text{DC}}}\cos(\omega t)\cos(\phi_{\text{c}}) - \frac{K_{3\text{rd}}}{4}\sin(2\omega t + \phi_{\text{c}}) + \frac{K_{3\text{rd}}}{8}\sin(4\omega t - \phi_{\text{c}}) + \frac{K_{3\text{rd}}mK_{\text{c}}}{6K_{\text{DC}}}\cos(3\omega t)\cos(\phi_{\text{c}})\Bigg) \quad (3.17)$$

The overall time varying energy within the stack (E_{stack}) can be then be calculated by adding the energy exchange of the stack to the nominal amount of stored energy within the stack, as in (3.18).

$$E_{\text{stack}}(\omega t) = E_{nom} + \Delta E_{\text{stack}}(\omega t) \tag{3.18}$$

Assuming that divergence of the sub-module capacitor voltages from each other relatively small, the available voltage within the stack, V_{avail}, given by the sum of the instantaneous sub-module capacitor voltages, can then be calculated as in (3.19).

$$V_{\text{avail}}(\omega t) = \sqrt{\frac{2E_{\text{stack}}(\omega t)}{C/N}} \tag{3.19}$$

The average sub-module voltage can then be calculated by dividing the available voltage within the stack, by the number of sub-modules, as in (3.20).

$$V_{\text{SM}_{\text{avg}}}(\omega t) = \frac{V_{\text{avail}}(\omega t)}{N} \tag{3.20}$$

Figure 3.7 shows energy deviation waveforms of an MMC with m=0.95, normalised by the apparent power as measured at the PCC, at four different operating conditions. As there are no DC terms within the energy deviation expression the net exchange of energy into and out of the stack of sub-modules within the converter arm can be seen to be zero over each fundamental cycle.

The normalised peak and minimum energy deviation of an MMC with m=0.95, with variation in the converters power angle, is given in Fig. 3.8. The peak and minimum values can bee seen to be symmetric for rectifying and inverting operation. The peak energy deviation can be seen to be larger for capacitive power factors. The minimum energy deviation however significantly greater for inductive power factors, than for capacitive power factors.

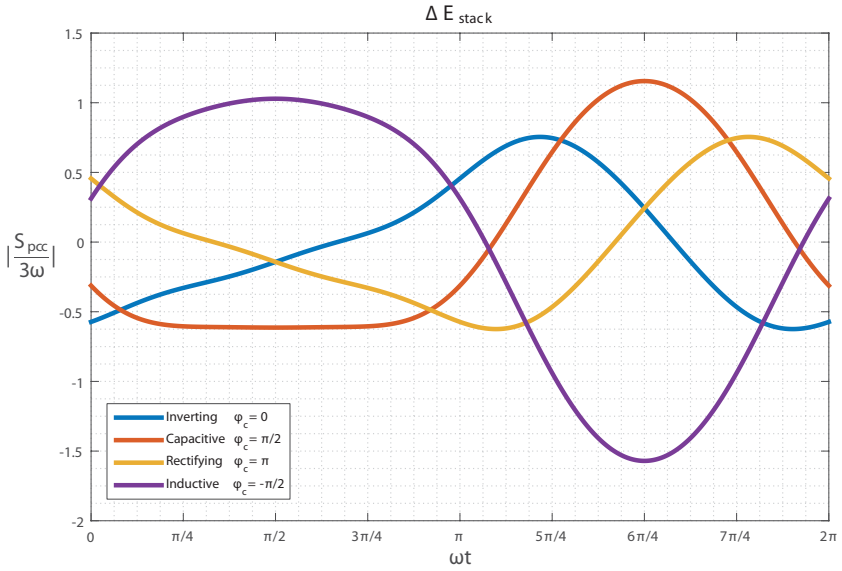


Figure 3.7: Energy deviation of a stack of sub-modules in an MMC with m=0.95.

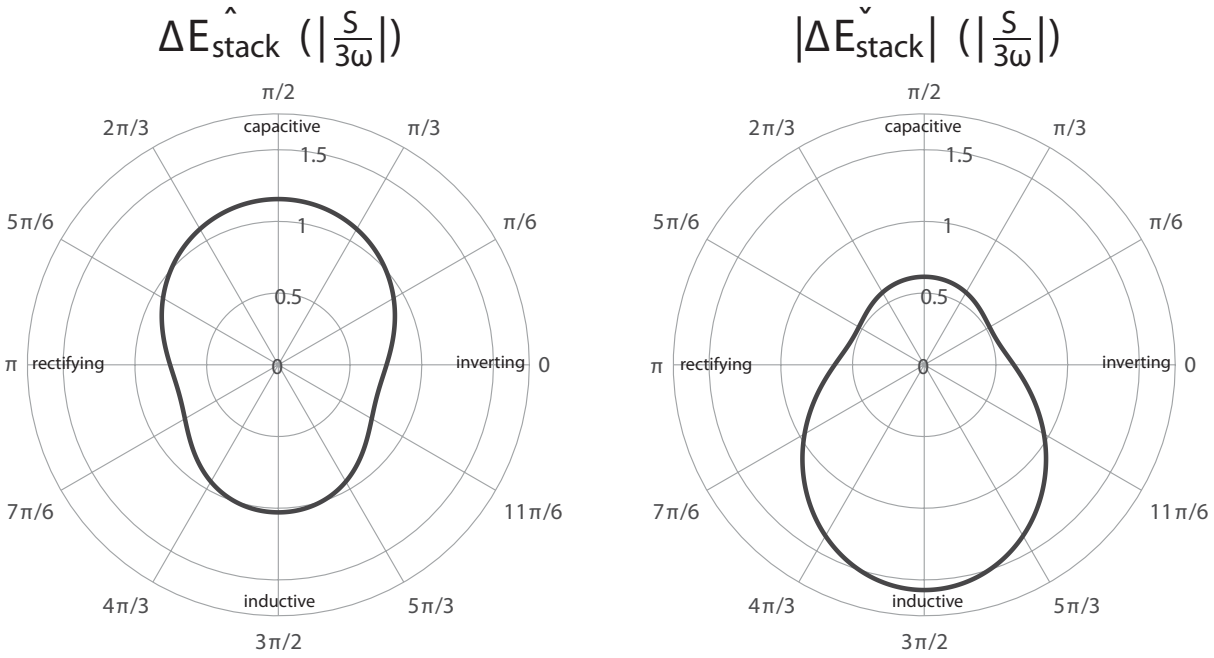


Figure 3.8: Normalised peak and minimum energy deviation of the MMC with variation in the power angle. Converter operated at a modulation index of 0.95.

3.3.1.3 P/Q Capability Diagram

Using the above derivations it is possible to generate a P/Q capability graph for an MMC. This is done by sweeping the converters set-point results across a mesh-grid and then finding the critical points which cause an operational limit to be breached. An example P/Q capability graph is given in Fig. 3.9.

In general, the following observations can be made; The capacitive reactive power-capability is limited by a combination of the over-modulation limit and the peak sub-module limit. The converters inductive reactive power capability is limited by the stack voltage limit. At power factors close to unity the converters active power factor is limited by the arm current limit. As the converters power factor is then moved away from unity, it is then limited by one or more of the other limits.

3.3.2 Design of the MMC for a Given P/Q Specification

The derivations in the above section allow the P/Q capability of an MMC to be analysed for a given AC voltage variation, sub-module capacitor size, number of sub-modules and nominal sub-module voltage. However to make the best utilisation of the sub-modules, and so maximise the converter's efficiency, the converter should be designed so that the outer limiting factors on its P/Q capability, intersect with the converter's design specification.

3.3.2.1 AC Voltage Selection

The maximum output voltage of the half-bridge MMC is constrained by the DC terminal voltage. For efficiency reasons it is desirable to operate with the highest possible AC to DC voltage ratio, whilst still being able to meet the P/Q specification across the given variation in AC voltage. This minimises the magnitude of the AC component of the arm current, which in turn then impacts the energy deviation of the overall stack, and the sub-module capacitor ripple.

As the phase voltage at the converter terminals can be described as (3.7), where the value of K_c can be calculated from (3.21).

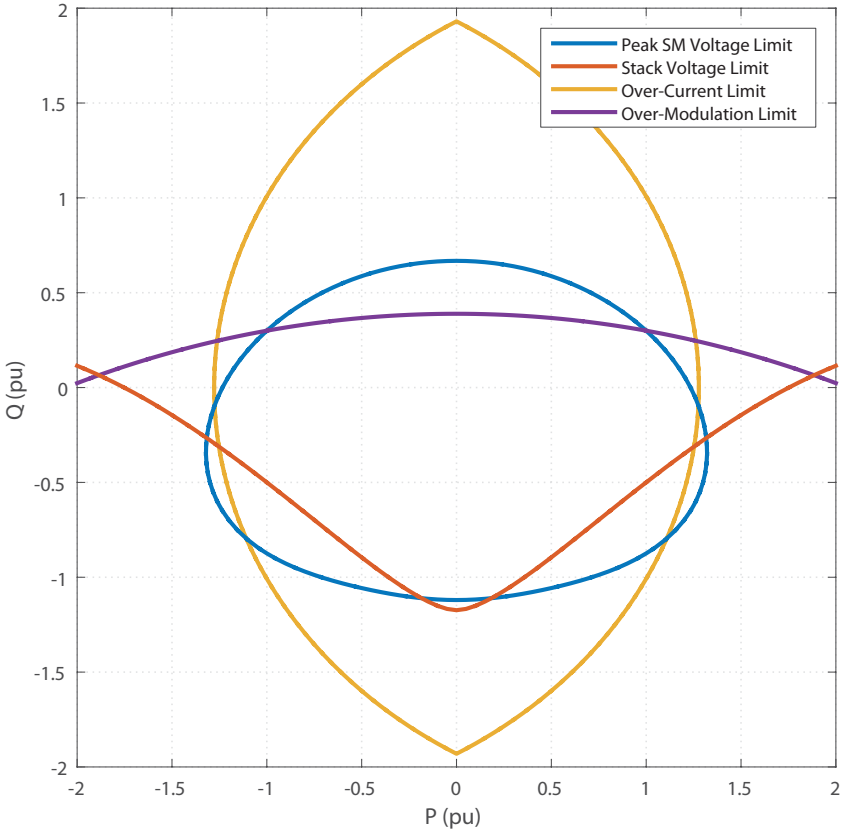


Figure 3.9: Example P/Q capability graph for an MMC.

$$V_{\mathrm{c}}(wt) = mK_{\mathrm{c}}V_{\mathrm{DC}}\sin(\omega t) \tag{3.21}$$

The use of third harmonic injection allows the peak of the AC phase voltage to be boosted by 15% above the DC terminal voltage [53]. Some safety margin should be included within the design. This can be included in the design process by the introduction of an over-modulation safety factor ($K_{\mathrm{mod}_{\mathrm{safety}}}$), which defines how close to the DC terminal voltage the converter is allowed to come. Setting the peak allowable voltage, defined in terms of $K_{\mathrm{mod}_{\mathrm{safety}}}$, equal to the peak of the converter voltage gives (3.22).

$$(1 - K_{mod_{safety}})V_{DC} = \frac{1}{1.15}mK_cV_{DC} \tag{3.22}$$

Rearranging this in terms of the modulation index, and subbing (3.7) in for K_c, gives the expression (3.23), which can be solved to find the maximum allowable modulation index. By sweeping across the outer points of the P/Q specification, the limiting case can be found. Typically the limiting point is rated active power, rated capacitive power at the maximum rated AC voltage above nominal.

$$m = \frac{(1 - K_{mod_{safety}}) \times 1.15}{\sqrt{\left(K_{\mathrm{AC}} + \frac{S_{\mathrm{pcc}_{\mathrm{pu}}}}{K_{\mathrm{AC}}}\sin(\phi_{\mathrm{pcc}})(X_{\mathrm{phase}_{\mathrm{pu}}} + \frac{X_{\mathrm{arm}_{\mathrm{pu}}}}{2})\right)^2 + \left(\frac{S_{\mathrm{pcc}_{\mathrm{pu}}}}{K_{\mathrm{AC}}}\cos(\phi_{\mathrm{pcc}})(X_{\mathrm{phase}_{\mathrm{pu}}} + \frac{X_{\mathrm{arm}_{\mathrm{pu}}}}{2})\right)^2}} \tag{3.23}$$

3.3.3 Design with a known Nominal Energy Storage

Methodologies for designing an MMC from two separate starting points are presented. The first starting point, presented in this sub-section, assumes that the converter will be designed using a known nominal energy storage within the converter stacks, and with a defined maximum voltage rating on the sub-module. The required sub-module capacitor size, nominal sub-module voltage and minimum number of sub-modules are then solved for. The nominal energy storage

represents the sum of the energy stored within each sub-module capacitor within the stack, when the sub-module capacitor is at its nominal voltage level. The second methodology, described in Subsection. 3.3.4, allows the converter to be designed when the size of the sub-module capacitor is already known.

3.3.3.1 Solving for the Nominal stack Voltage

When designing the converter, it is important to consider some safety margins to allow for disturbances to the energy levels within the converter due to fault conditions. These safety margins can also be used to account for the failure of sub-modules within the converter over time. The energy safety margin, E_{safety}, introduced here represents the amount of energy that a converter stack can be perturbed downwards, and still be capable of generating all specified PQ set-points across the specified variation in AC and DC voltages.

The maximum voltage that the converter stack is capable of generating is given by the sum of the sub-module capacitor voltages within the stack. This voltage is a time varying value due to the energy deviation of the stack over each cycle. When dimensioning the converter, it must be ensured that the converter has sufficient voltage capability to meet the voltage demand at all operating points across the specified variation in external grid conditions. At the same time, it is desirable to include the minimum amount of sub-modules required, with some safety margins added, to maximise the converters efficiency.

The nominal rated stack voltage, V_{rated}, is given by the sum of the sub-module capacitor voltages, when the sub-modules are all balanced and at their nominal voltage. This is expressed in (3.24)

$$V_{\text{rated}} = N \times V_{\text{SM}_{\text{nom}}} \tag{3.24}$$

Fig. 3.10 shows the stack voltage and stack energy of an MMC when it is operating at its design limit. The available voltage within the stack, considering the safety margin, intersects the stack voltage at one point during the cycle, denoted ωt_{crit}.

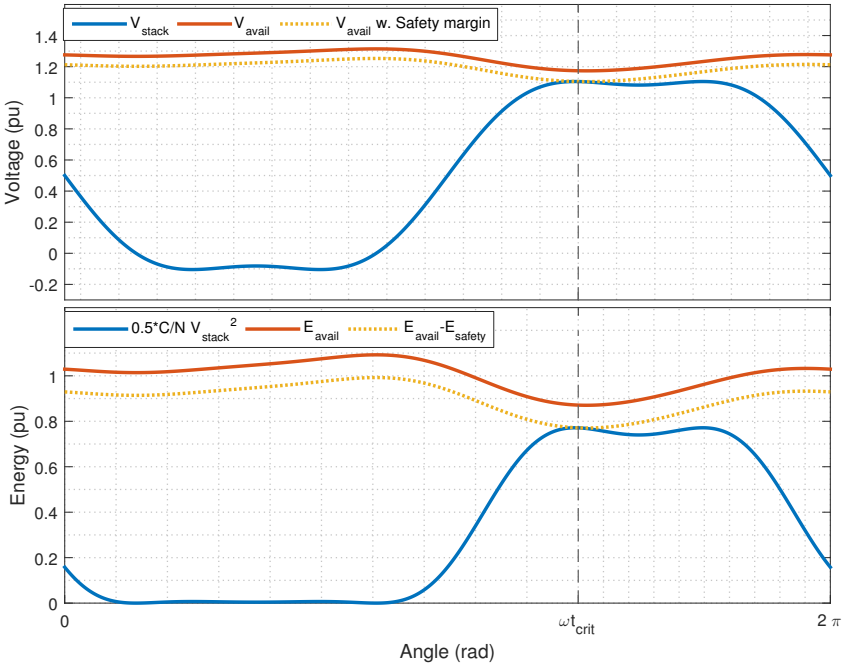


Figure 3.10: Stack voltage and stack energy levels when the converter is operating against its limit. Top: Stack voltage, available voltage and available voltage with safety margin. Bottom: Stack energy, stack energy with safety margin and instantaneous required energy to meet voltage demand.

At this point in the cycle, when all sub-modules within the stack are inserted, i.e. the stack is generating its maximum possible output voltage, the energy within the stack (E_{stack}) can be calculated from (3.25).

$$E_{\text{stack}}(\omega t_{\text{crit}}) = \frac{1}{2}\frac{C}{N}V_{\text{stack}}(\omega t_{\text{crit}})^2 \tag{3.25}$$

The stored energy within the converter stack can also be described as the nominal energy within the stack, E_{nom}, plus the cycle-by-cycle variation of the energy, $\Delta E(wt)$, minus the safety margin in terms of energy, E_{safety}. This is expressed in (3.26).

$$E_{\text{stack}}(\omega t) = E_{\text{nom}} + \Delta E(\omega t) - E_{\text{safety}} \tag{3.26}$$

The nominal energy within the stack can be calculated from the nominal voltage rating of the stack of sub-modules, as given in (3.27).

$$E_{\text{nom}} = \frac{1}{2}\frac{C}{N}{V_{\text{rated}}}^2 \tag{3.27}$$

Substituting (3.27) into (3.26) gives (3.28).

$$E_{\text{stack}}(\omega t) = \frac{1}{2}\frac{C}{N}{V_{\text{rated}}}^2 + \Delta E(\omega t) - E_{\text{safety}} \tag{3.28}$$

(3.25) and (3.28) can be equated to give (3.29).

$$\frac{1}{2}\frac{C}{N}V_{\text{stack}}(\omega t_{\text{crit}})^2 = \frac{1}{2}\frac{C}{N}{V_{\text{rated}}}^2 + \Delta E(\omega t_{\text{crit}}) - E_{\text{safety}} \tag{3.29}$$

Dividing both sides of (3.29) by the expression for the nominal energy given in (3.27) gives (3.30).

$$\frac{V_{\text{stack}}(\omega t_{\text{crit}})^2}{V_{\text{rated}}} = 1 + \frac{\Delta E(\omega t_{\text{crit}})}{E_{\text{nom}}} + \frac{E_{\text{safety}}}{E_{\text{nom}}} \tag{3.30}$$

This can then be rearranged in the form of (3.31), which gives the required rated voltage of the stack.

$$V_{\text{rated}} = V_{\text{stack}}(\omega t_{\text{crit}})\sqrt{\frac{1}{1 + \frac{\Delta E(\omega t_{\text{crit}})}{E_{\text{nom}}} - \frac{E_{\text{safety}}}{E_{\text{nom}}}}} \tag{3.31}$$

By sweeping the converters set-point across the outer points of the given P/Q specification, and the given AC and DC voltage variation, the worst case value can be found for the rated voltage of the stack can be found. The worst case values of $V_{stack}(\omega t_{crit})$ and $\Delta E(\omega t_{\text{crit}})$ can then be denoted as $V_{\text{stack}}^{\text{crit}}$ and ΔE^{crit}, respectively.

The value of ωt_{crit} can be found be finding the maximum value of the difference between the square of the stack voltage, normalised by the square of the peak stack voltage, and the energy

deviation of the stack, normalised the nominal energy stored within the stack. This can be expressed as in (3.32).

$$\omega t_{crit} = \arg \max_{\omega t} \left\{ \frac{V_{stack}(\omega t)^2}{\hat{V_{stack}}^2} - \frac{\Delta E_{stack}(\omega t)}{E_{nom}} \right\} \tag{3.32}$$

3.3.3.2 Solving for the Sub-Module Capacitor Size and Nominal Sub-Module Voltage

Once the rated voltage of the stack has been determined, the nominal sub-module voltage, $V_{\mathrm{SM_{nom}}}$, and the sub-module capacitor size, C, must be found. To make the best utilisation of the sub-modules this peak continuous voltage rating of the sub-module should be reached under the worst case operating condition under steady-state operation [49]. To solve for this condition it is useful to assume that the sub-modules are all tightly controlled around their mean value, and then solve for the peak rated mean sub-module voltage ($V_{\mathrm{SM}}^{\mathrm{max}}$). For practical dimensioning, the value of $V_{\mathrm{SM}}^{\mathrm{max}}$ could be reduced by a margin $(1-\alpha)$ below the actual peak sub-module limit. The size of this margin would then be dependent on the sub-module voltage balancing algorithm used. This is illustrated in Fig. 3.11.

In a similar manner to how the rated voltage of the stack was solved for it is useful to solve for the nominal sub-module voltage on an energy basis. This can be done by equating the difference between the energy within the sub-module when it is at its peak rated voltage and when it is at its nominal voltage, with the peak positive energy deviation of the overall stack. The nominal energy within a sub-module can be given by (3.33).

$$E_{\mathrm{SM_{nom}}} = \frac{E_{\mathrm{nom}}}{N} \tag{3.33}$$

The nominal energy within the stack (E_{nom}) can be written in terms of the rated stack voltage, as in (3.34).

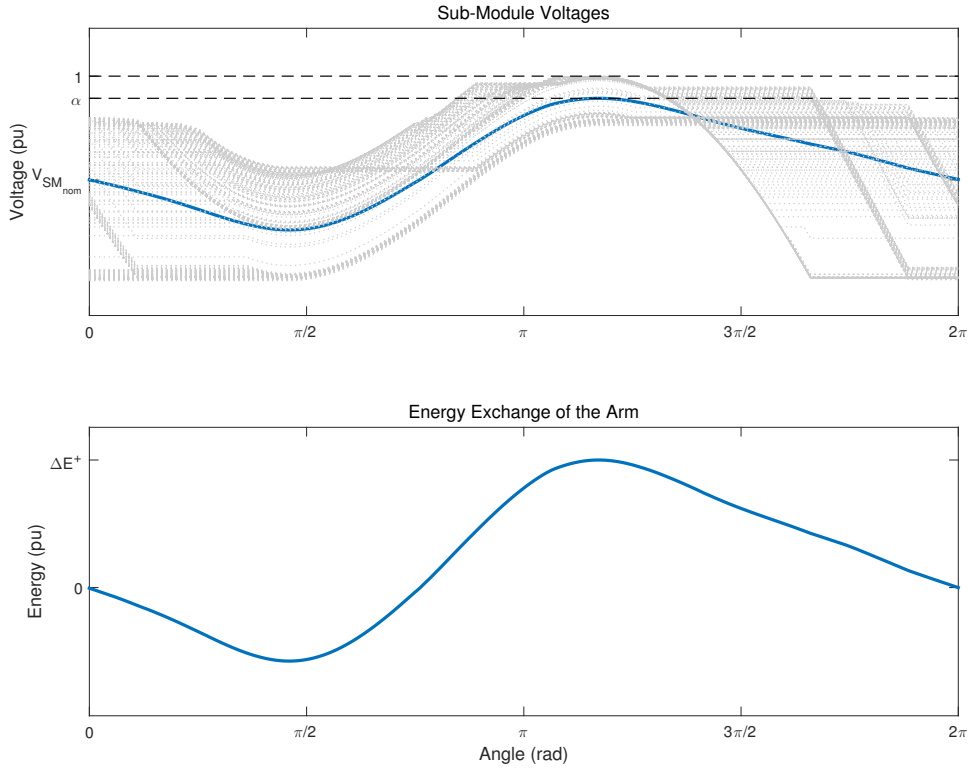


Figure 3.11: Sub-module voltages and stack energy levels when the converter is operating against the peak sub-module voltage limit.

$$E_{\text{nom}} = \frac{1}{2}\frac{C}{N}{V_{\text{rated}}}^2 \tag{3.34}$$

Rearranging (3.34) in terms of N gives (3.35).

$$N = \frac{C{V_{\text{rated}}}^2}{2E_{\text{nom}}} \tag{3.35}$$

Subbing (3.35) and (3.34) into (3.33) allows the nominal sub-module energy to be expressed in terms of the nominal stack energy, the sub-module capacitor size and the rated voltage of the stack. This is expressed in (3.36).

$$E_{\text{SM}_{\text{nom}}} = \frac{2E_{\text{nom}}^2}{C{V_{\text{rated}}}^2} \tag{3.36}$$

The energy within a sub-module when it is at the peak rated mean voltage can be expressed as in (3.37).

$$E_{\mathrm{SM_{Max}}} = \frac{1}{2} C V_{\mathrm{SM}}^{\mathrm{max}2} \tag{3.37}$$

The nominal energy within the stack can be expressed as in (3.34), in terms of the rated voltage of the stack, the sub-module capacitor size and number of sub-modules.

The nominal energy within the sub-module, $E_{\mathrm{SM_{nom}}}$, can then be given by the maximum sub-module energy, minus the maximum positive energy deviation of an individual sub-module. Assuming that the voltage balancing algorithm keeps the sub-modules voltages to within a tight tolerance band, the maximum positive energy deviation of a sub-module can be considered to be the maximum positive energy deviation of the overall stack under the worst case operating condition ($\hat{\Delta E}$), divided by the number of sub-modules within the stack. The nominal sub-module energy can be expressed as in (3.38).

$$E_{\mathrm{SM_{nom}}} = \frac{1}{2} C V_{\mathrm{SM}}^{\mathrm{max}2} - \frac{\hat{\Delta E}}{N} \tag{3.38}$$

Subbing in (3.35) gives (3.39)

$$E_{\mathrm{SM_{nom}}} = \frac{1}{2} C V_{\mathrm{SM}}^{\mathrm{max}2} - \frac{2 E_{\mathrm{nom}} \hat{\Delta E}}{C V_{\mathrm{rated}}^2} \tag{3.39}$$

Equating (3.36) and (3.39) gives (3.40).

$$\frac{2 E_{\mathrm{nom}}^2}{C V_{\mathrm{rated}}^2} = \frac{1}{2} C V_{\mathrm{SM}}^{\mathrm{max}2} - \frac{2 E_{\mathrm{nom}} \hat{\Delta E}}{C V_{\mathrm{rated}}^2} \tag{3.40}$$

Rearranging in terms of the sub-module capacitor, C, gives (3.41), which allows the required capacitor size to be found.

$$C = \sqrt{\frac{4 E_{\mathrm{nom}} (E_{\mathrm{nom}} + \hat{\Delta E})}{V_{\mathrm{rated}}^2 V_{\mathrm{SM}}^{\mathrm{max}}}} \tag{3.41}$$

The number of sub-modules within a stack, N, and the nominal sub-module voltage, $V_{SM,nom}$ can then be solved from (3.42) and (3.43).

$$N = \frac{1}{2}\frac{C}{E_{\text{nom}}}V_{\text{rated}}^2 \tag{3.42}$$

$$V_{SM_{\text{nom}}} = \frac{V_{\text{rated}}}{N} \tag{3.43}$$

3.3.4 Design with a known sub-module capacitor size

For practical reasons, it may be desirable to design a converter with pre-determined sub-module capacitor size. This could be due to limited variety of available capacitor sizes, or if the sub-module capacitor is a standard design which is used for numerous different projects, which may have varying specifications in terms of P/Q capability and AC voltage variation. This can be done by first solving for the critical angle, and then simultaneously solving for the nominal sub-module voltage and the rated stack voltage.

3.3.4.1 Condition on the Peak Sub-Module Voltage

The nominal energy within a sub-module can be expressed as in (3.44), based upon the maximum allowable sub-module voltage, the peak positive energy deviation of the stack and the number of sub-modules. It can also be written as in (3.45), based upon the nominal sub-module voltage and number of sub-modules within the stack.

$$E_{\text{SM}_{\text{nom}}} = \frac{1}{2}CV_{\text{SM}}^{\text{max2}} - \frac{\hat{\Delta E}}{N} \tag{3.44}$$

$$E_{\text{SM}_{\text{nom}}} = \frac{1}{2}CV_{\text{SM}_{\text{nom}}}^2 \tag{3.45}$$

Equating (3.44) and (3.45) and rearranging in terms of the nominal sub-module voltage gives

(3.46)

$$V_{\mathrm{SM}_{\mathrm{nom}}} = \sqrt{V_{\mathrm{SM}}^{\mathrm{max}2} - \frac{2\hat{\Delta E}}{NC}} \tag{3.46}$$

3.3.4.2 Condition on the Stack Voltage Limit

The condition for the stack voltage can be solved for as follows. At the critical angle, the energy within the stack (E_{stack}) is given by (3.47).

$$E_{\mathrm{stack}}(\omega t_{\mathrm{crit}}) = \frac{1}{2}\frac{C}{N}V_{\mathrm{stack}}(\omega t_{\mathrm{crit}})^2 \tag{3.47}$$

The stored energy within the converter stack can also be described as the sum of the energy within the sub-modules at their nominal voltage, plus the cycle-by-cycle variation of the energy, $\Delta E(wt)$, minus the safety margin, E^{+}_{safety}. This is expressed in (3.48).

$$E_{\mathrm{stack}}(\omega t) = N\frac{1}{2}CV^2_{\mathrm{SM}_{\mathrm{nom}}} + \Delta E(\omega t) - E^{+}_{\mathrm{safety}} \tag{3.48}$$

(3.47) and (3.48) can be equated to give (3.49), which is only valid at the critical angle ($\omega_{\mathrm{t}_{\mathrm{crit}}}$). The unknown expressions within this equation are the number of sub-modules (N), and the nominal sub-module voltage ($V_{\mathrm{SM}_{\mathrm{nom}}}$).

$$\frac{1}{2}\frac{C}{N}V_{\mathrm{stack}}(\omega t_{\mathrm{crit}})^2 = N\frac{1}{2}C{V_{\mathrm{SM}_{\mathrm{nom}}}}^2 + \Delta E(\omega t_{\mathrm{crit}}) - E^{+}_{\mathrm{safety}} \tag{3.49}$$

The exact location of the critical angle is dependant on the level of energy storage within the converter governed by both N and $V_{\mathrm{SM}_{\mathrm{nom}}}$ and is closely correlated with the lowest energy and highest voltage points of the stacks.

Taking (3.49) and dividing both sides by the expression for the nominal energy (given by $N\frac{1}{2}CV^2_{\mathrm{SM}_{\mathrm{nom}}}$) gives (3.50).

$$\frac{V_{stack}^2(\omega t)}{N^2 V_{SM_{nom}}^2} = 1 + \frac{\Delta E(\omega t) - E_{\text{safety}}^+}{N\frac{1}{2}CV_{SM_{nom}}} \tag{3.50}$$

Rearranging this expression gives (3.51).

$$NV_{SM_{nom}} = V_{stack}(\omega t)\sqrt{\frac{1}{1 + \frac{\Delta E(\omega t) - E_{\text{safety}}^+}{N\frac{1}{2}CV_{SM_{nom}}^2}}} \tag{3.51}$$

The critical point is the point which maximises (3.51), i.e maximises the required voltage capability within the stack. When first solving for this point an estimate for the nominal energy (E_{nom}^{est}) within the converter can be made. The critical angle can then be found from (3.52). To ensure the critical angle has been found, the entire design process can be iterated with the value of E_{nom}^{est} updated based on the previous results. This has been found to converge within 1-2 iterations of this process.

$$\omega t_{crit} = \arg\max_{\omega \text{t}} \left\{ V_{stack}(\omega t)\sqrt{\frac{1}{1 + \frac{\Delta E(\omega t) - E_{\text{safety}}^+}{E_{nom}^{est}}}} \right\} \tag{3.52}$$

3.3.4.3 Solving for the number of Sub-Modules and the nominal Sub-Module Voltage

Substituting (3.46) into (3.51), simplifying and then grouping terms gives the third order polynomial expression (3.53). Solving for the roots of (3.53) and then choosing the lowest positive root (in order to maximise the converter's efficiency) that satisfies the condition: $V_{\text{SM}_{\text{nom}}} \leq V_{\text{SM}}^{\max}$, gives the required number of sub-modules within the stack.

$$N^3\Big(\frac{C}{2}V_{\mathrm{SM}}^{\mathrm{max4}}\Big) + N^2\Big(V_{\mathrm{SM}}^{\mathrm{max2}}\big(-\hat{\Delta E} + \Delta E(\omega t_{\mathrm{crit}}) - E_{\mathrm{safety}}^{+}\big) - \big(\hat{\Delta E}V_{\mathrm{SM}}^{\mathrm{max2}}\big)\Big) + N\Big(-\frac{2\hat{\Delta E}}{C}\big(-\hat{\Delta E} + \Delta E(\omega t_{\mathrm{crit}}) - E_{\mathrm{safety}}^{+}\big) - \frac{C}{2}V_{\mathrm{SM}}^{\mathrm{max2}}V_{\mathrm{stack}}(\omega t_{\mathrm{crit}})^2\Big) + V_{\mathrm{stack}}(\omega t_{\mathrm{crit}})^2\hat{\Delta E} = 0 \quad (3.53)$$

The nominal sub-module voltage can then be found by substituting the resulting value of N into (3.44). To design for a given P/Q specification, the required value of N can be checked for each outer point of the P/Q specification, with the values of $V_{\mathrm{stack}}^{\mathrm{crit}}$ and ΔE^{crit} recalculated for each operating point. The maximum value of $\hat{\Delta E}$ across the P/Q specification. The required number of sub-modules can then be taken as the resulting worst case value of N.

3.3.5 Analysis

lb:ThermalChap Using the methods detailed in the sections above, a sweep of converter designs with variation in both the nominal energy storage and the sub-module capacitor size are made for a converter designed to meet the GB grid code requirements. The design specifications of the converter are given in Table. 3.1. Arm inductors that are 0.2 pu in size are chosen based upon the results presented in [49]. The energy safety margin was chosen as 3 kJ/MVA based upon simulation experience of AC fault ride through requirements. The DC voltage was chosen based on rating of the maximum available XLPE cable [55]. A 1500 A DC current was chosen to line up with the IGBT that is modelled in the following Chapter 4. A $K_{mod_{safety}}$ value of 0.05 was chosen to give some control margin in case of variations in the DC voltage, without excessively de-rating the converter. Accurately setting this value would require a full system study to be undertaken.

The results of the sweep of converter designs are shown in Fig. 3.12a and Fig. 3.12b respectively. It can be seen that as the nominal energy of the converter is decreased the required number of sub-modules within the converter increases rapidly. This is because the ratio of the

Table 3.1: Modular multilevel converter design specification.

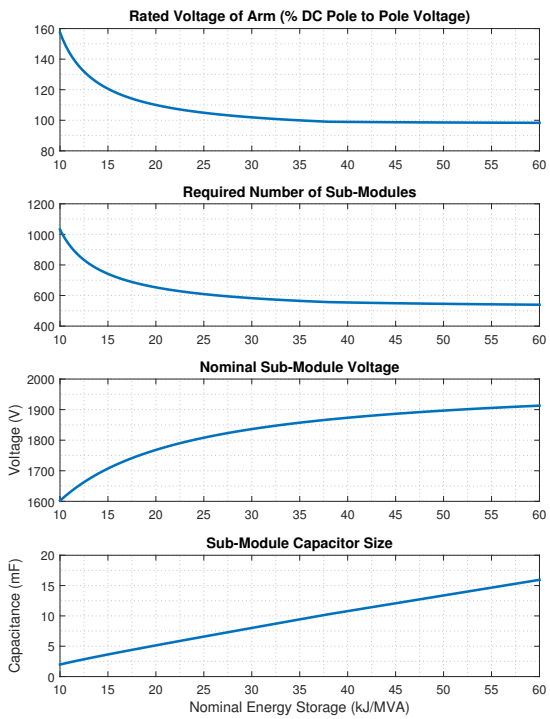
Characteristic	Value
Rated Power	1575 MW
Rated DC Current	1500 A
DC Voltage	±525 kV
AC Voltage Variation	±5%
Transformer Leakage Reactance	0.14 pu
Arm Inductor Size	0.2 pu
Peak Rated Sub-Module Voltage	2000 V
Over-Modulation Safety Factor	0.05
Energy Safety Margin	3 kJ/MVA
$K_{mod_{safety}}$	0.05

energy deviation of the stack, to the overall energy within the stack increases. To compensate for this, the sub-module voltage must be reduced in order to prevent the peak sub-module limit from being breached while at the same time the overall rated voltage of the stack must be increased in order to prevent the stack voltage limit from being breached.

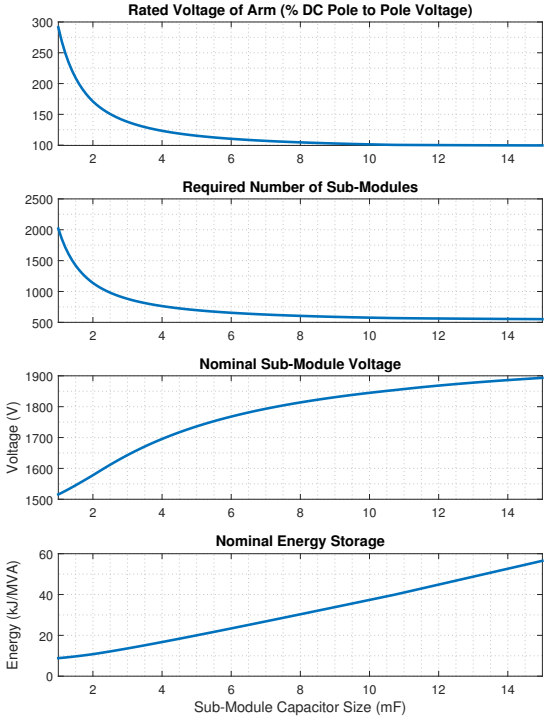
Most work on the design of the MMC has assumed that the rated voltage of the stack is equal to the DC pole to pole voltage. Using this analysis it can be seen that this condition is satisfied when the nominal energy within the converter is ∼35 kJ/MVA, or with a sub-module capacitor of ∼9 mF. In [46] it was estimated that the minimum energy storage requirement was 22.5 kJ/MVA. However this values was estimated assuming the converter only operates at unity power-factor, without variation in the AC voltage. When the energy levels within the converter are increased past ∼35 kJ/MVA, the rated voltage decreases slightly below the DC pole to pole voltage and settles asymptotically, with little reduction in the required number of sub-modules once the stored energy within the converter is increased past ∼40 kJ/MVA.

3.3.5.1 Analysis Verification

To verify the analysis, a detailed simulation of a converter using the parameters of an MMC designed with 30 kJ/MVA. The P/Q capability graphs for this converter are shown in Fig. 3.13.



(a) Converter designed with a fixed nominal energy storage level.

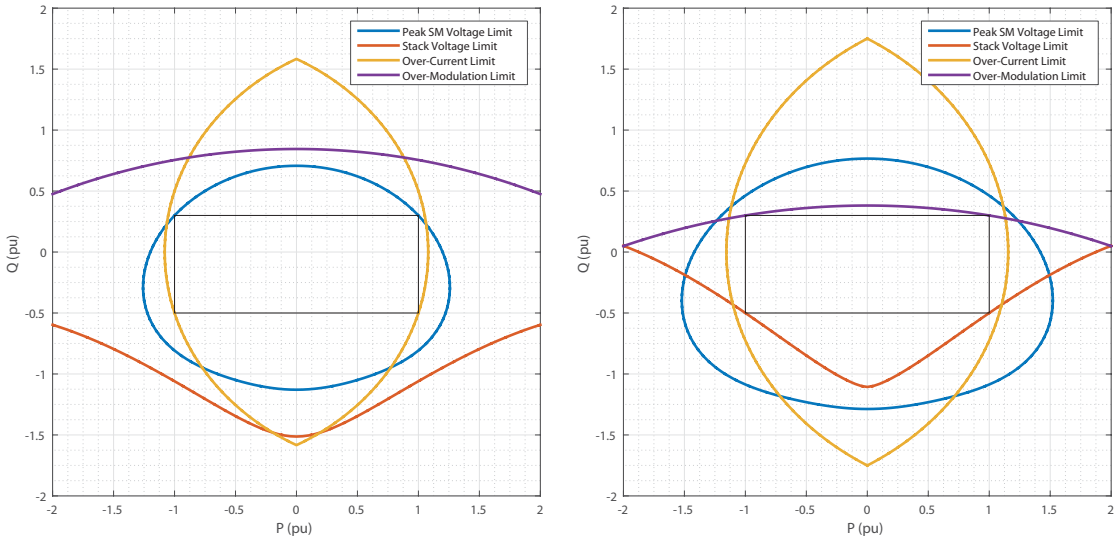


(b) Converter designed with a fixed sub-module capacitor size.

Figure 3.12: Design of a Modular Multilevel Converter to meet the GB grid code requirements.

The GB Grid Code P/Q specification is shown in the black rectangular box.

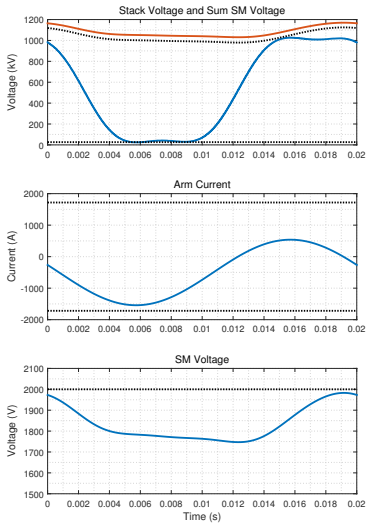
Four outer points of the P/Q envelope were tested using the simulation model. The results of these tests are shown in Fig. 3.14. As expected the converters P/Q capability is limited by one of the limiting factors at each point tested, with the simulation results agreeing with the analytic results with close approximation.



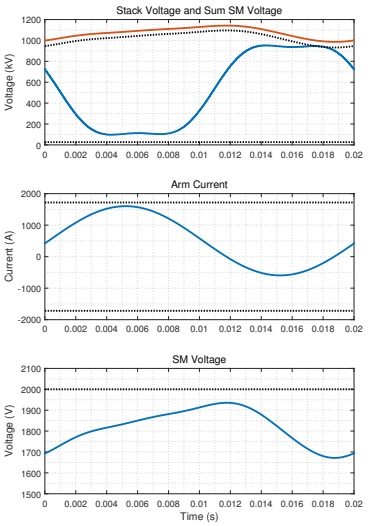
(a) AC voltage: 95% nominal.

(b) AC voltage: 105% nominal.

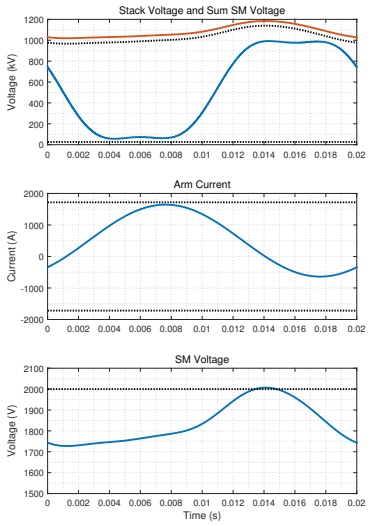
Figure 3.13: P/Q capability graphs of an MMC with 30 kJ/MVA energy storage designed to meet the GB grid code requirement.



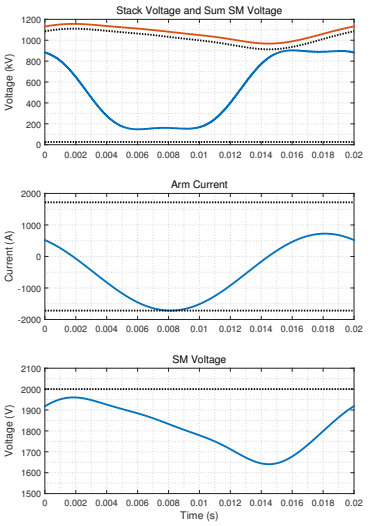
(a) P: -1 Q: 0.3
AC voltage: 105% nominal
Converter limited by over-modulation limit



(b) P: 1 Q: -0.5
AC voltage: 105% nominal
Converter limited by stack voltage limit



(c) P: -1 Q: 0.3
AC voltage: 95% nominal
Converter limited by peak sub-module voltage limit



(d) P: 1 Q: -0.5
AC voltage: 95% nominal
Converter limited by stack current limit

Figure 3.14: Simulation verification of converter P/Q capability. Top sub-plot shows the stack voltage, sum sub-module voltage and asafety margin. Middle plot shows arm current. Bottom plots shows the average sub-module (SM) voltage. Operating limits shown in dashed lines.

3.4 Hybrid Mixed-Stack Modular Multilevel Converter

The previous section focused on the design of the half-bridge MMC. This topology delivers a converter with high efficiency and controllability. However it remain weak to DC side faults due to the half-bridge stacks inability to generate a negative voltage output. If fault tolerance is a required feature of the converter, as it may be in overhead line applications or multi-terminal networks, than this issue could be solved by replacing the half-bridge sub-modules with full-bridge sub-modules. However this leads to a doubling in the conduction losses within the converter. An interesting compromise between these options is a hybrid design [56], where each stack contains a mixture of half-bridge and full-bridge sub-modules. By including a sufficient level of full-bridges within the stacks, the converter could be designed to be DC fault tolerant, without compromising the overall efficiency of the converter to the same extent that a wholly full-bridge design would. This Hybrid MMC design in illustrated in Fig. 3.15.

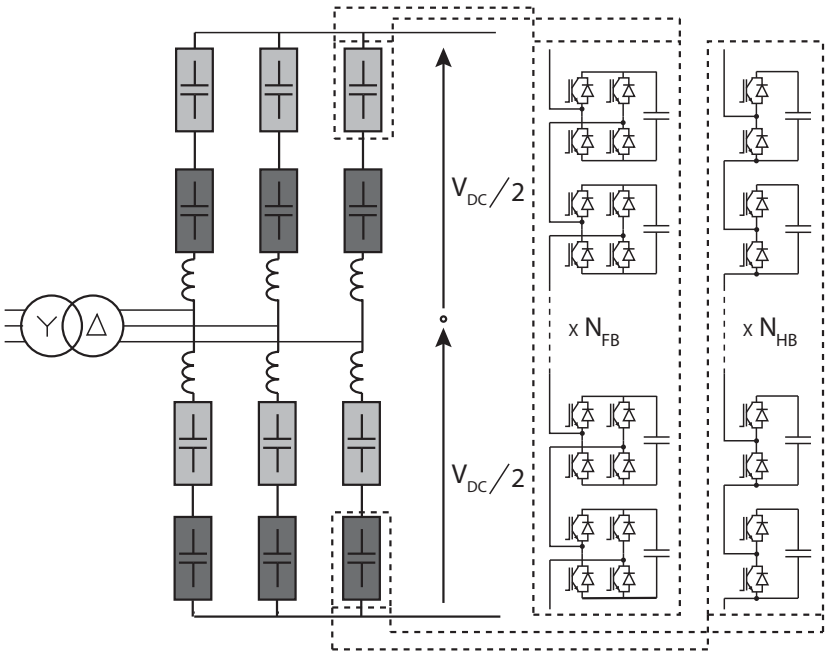


Figure 3.15: Hybrid modular multilevel converter.

The inclusion of full-bridge sub-modules within the converter stacks means that the converter's output voltage is no longer constrained by the DC pole voltage (i.e $\pm\frac{V_{DC}}{2}$) [57], allowing the converter to be designed to over-modulate its output during normal operation. The question of what the most efficient AC to DC Voltage ratio to operate at is addressed within this section. The design methodology from the previous section is adapted and expanded to the case of this topology.

The previous section of this chapter has examined how to size a half-bridge MMC for a given P/Q specification. It was found that the energy deviation of the stacks of sub-modules within each arm has a strong impact on the required rating of the converter. The modulation index that the Hybrid MMC is operated at has been found to have a strong impact on the energy deviation of the converter. This is illustrated in Fig. 3.16, which gives the normalised peak and minimum energy deviation of an MMC, with variation in modulation index. The peak energy deviation can be seen to reduce for all power angles with an increasing modulation index. The minimum energy deviation can be seen to decrease for inductive power factors, while for capacitive power factors an inverse relationship can be seen.

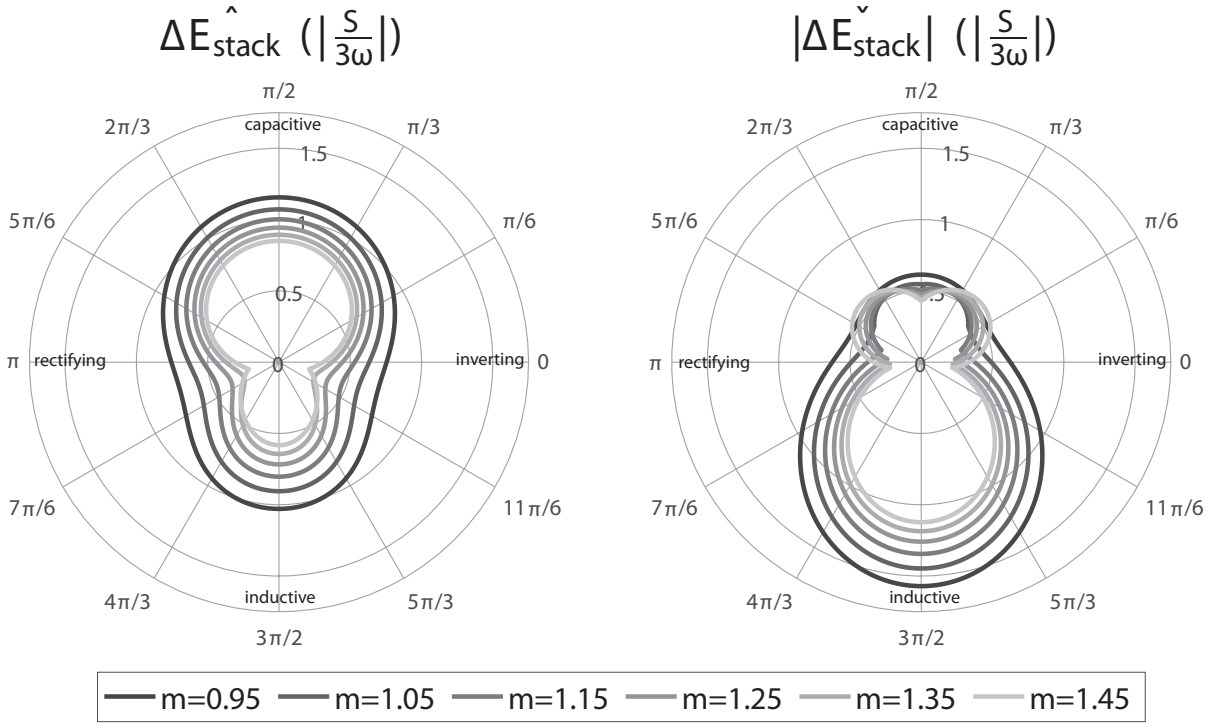
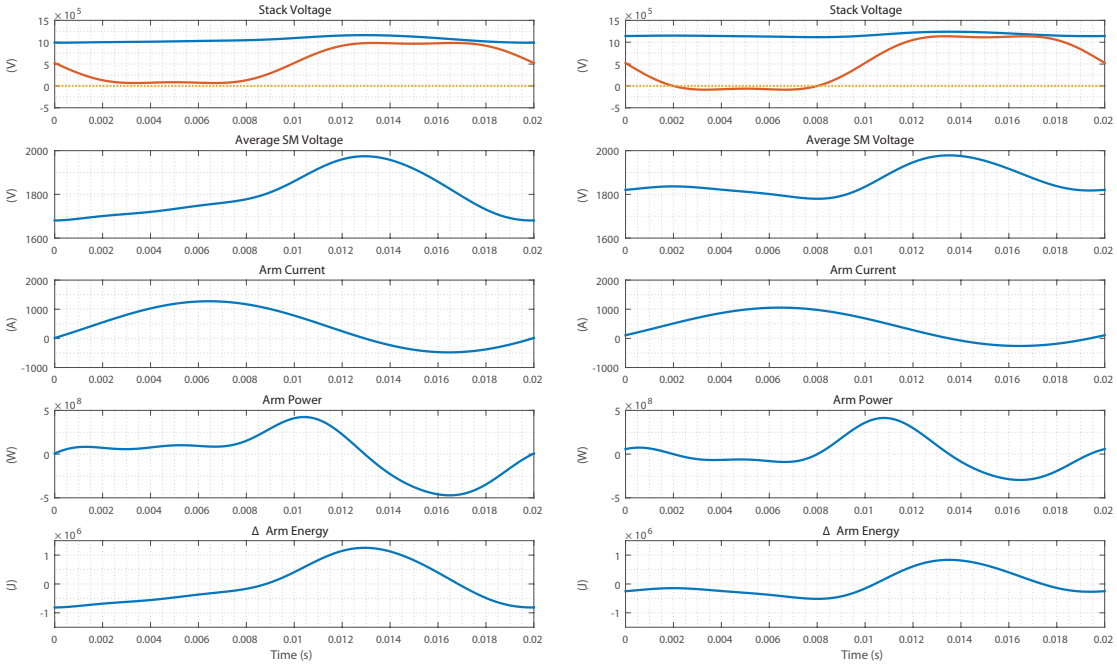


Figure 3.16: Normalised peak and minimum energy deviation of the MMC with variation in the modulation index and power angle.

Waveforms from two Hybrid MMCs are shown in Fig. 3.17. The first converter, shown in Fig. 3.17a, is designed with a modulation index of 0.9, and does not utilise the negative voltage capability of its full-bridge sub-modules during normal operation. The second converter, shown in Fig. 3.17b, operates at a modulation index of 1.2, and so over-modulates its output voltage. For part of the cycle the stack voltage goes negative, allowing the converter to generate a voltage higher than the DC terminal voltage.

Figure 3.17 illustrates several points about the design of the Hybrid MMC. As the AC to DC voltage ratio increases, the AC current magnitudes for a given power set-point will reduce. However at the same time the converter stacks must be rated to generate a higher peak voltage. The change in modulation index also impacts the power and energy deviation of the stack. As shown in the previous section, the magnitude and shape of the energy deviation waveform can



(a) m=0.9 (b) m=1.2

Figure 3.17: Hybrid modular multilevel converter generating 1 pu P and 0.3 pu Q.

have a large impact on the required rated voltage of the stack, and on the nominal sub-module voltage selection. This section of this chapter investigates which AC to DC voltage ratios are the most attractive in terms of power efficiency, as well as the overall impact of the modulation index selection on the converters design and operation. The design methodology for the half-bridge MMC, developed in the previous section, is expanded to the case of the Hybrid MMC. A sweep of modulation indexes is then made, with the resulting impact on the converters efficiency and required number of sub-modules and semiconductor devices assessed. The results indicate that a modulation index in the region of 1.2 may the best choice from an efficiency perspective.

3.4.1 Overview of Major Work in the Literature

The possibility of designing the Hybrid MMC to over-modulate its output, and all of the impacts that this will have on its dimensioning have received some attention [58, 57, 59], but a full investigation into what modulation index results in the highest efficiencies has not yet been performed. In [57], the design of the Hybrid MMC, considering operation at modulation indexes of 0.8163 and 1.633 was investigated. Modulation indices between these two values were not considered, but an expression for the required number of full-bridge sub-modules to block the AC side contribution to a DC fault was derived. Issues with voltage divergence between the full-bridge and half-bridge sub-modules at higher modulation indexes were identified. In [59] analytical expressions for the energy deviation and sub-module capacitor voltage ripple of full-bridge converters as a function of the modulation index were presented. The authors proposed a modulation index of 1.4 as this resulted in the elimination of the fundamental component within the SM capacitor voltage ripple. In [58], an MMC design using Semi-Full-Bridge sub-modules is presented, but efficiency results are not given. Following the lead in [59], the authors show experimental results of the converter operating at a modulation index of 1.4. In [60] a method for charging of the sub-modules during AC side start-up of the converter was presented. An expression for the capacitor ripple voltage was derived as a function of the modulation index. In [61] the design of Hybrid MMCs using various different SM topologies was investigated. However, the analysis was performed assuming a relatively low modulation index of 0.81 in all cases. Other works have focused on the control of Hybrid MMC [62] and its DC fault ride through capability [63, 60] as well as reliability aspects of the design [64]. Other multilevel converter topologies have also been designed to over-modulate their output. The Alternate Arm Converter has been designed to operate at a modulation index of $\frac{4}{\pi}$ (≈ 1.27) as this results in a net zero deviation in the stored energy within the converter over each cycle.

3.4.2 Design of the Hybrid MMC

The analysis that follows makes several assumptions. Firstly that the sub-module capacitor size, and peak rated voltage of the sub-module are assumed to be the same for both the half-bridge and full-bridge sub-modules within the stack.

Under these assumptions, the required positive voltage rating of the stack in the Hybrid MMC can be determined in an identical manner to the half-bridge MMC, using either of the methodologies developed in Section. 3.3.

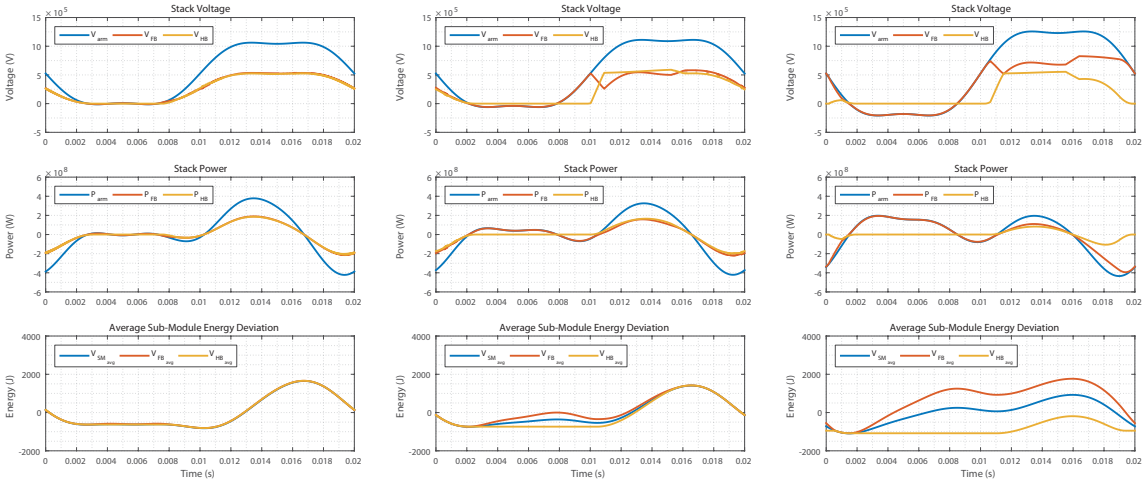
The required voltage rating of the full-bridge portion of the stack is dependent on what strategy the converter employs during DC faults, and if the converter is expected to be able to operate as a STATCOM during the loss of the DC system. The two fault strategies that the converter can employ during DC faults are to:

- Actively block all of its sub-modules, driving the AC current to zero and preventing any AC side current contribution to the DC fault.
- Remain connected to both the AC and DC buses during the DC fault and retain control over the AC side currents.

3.4.2.1 Maximum Modulation Index & Peak Sub-Module Voltage

As noted in [57], the hybrid has a limitation on the maximum modulation index that can be achieved before it becomes impossible to maintain the correct balance of energy between the full-bridge and half-bridge portions of the stack, without increasing the ratio of full-bridge to half-bridge sub-modules beyond what it is necessary to successfully deal with DC side faults.

This is because for the part of the cycle when the converter stack is generating a negative voltage, only the full-bridge sub-modules can be utilised. This limits the voltage balancing mechanisms ability to prevent the energy content of FB sub-modules from deviating away from the mean value of the overall stack. This issue is illustrated in Fig. 3.18 for the Hybrid MMC, showing example cases at three modulation indexes.



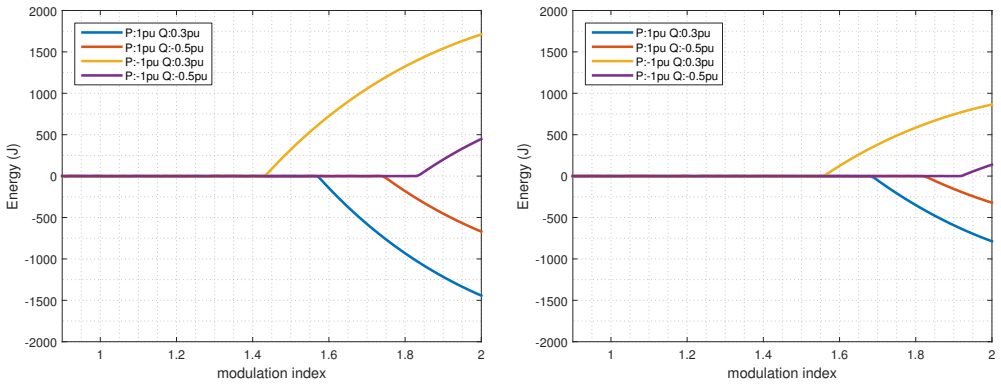
(a) m=1.1 (b) m=1.3 (c) m=1.5

Figure 3.18: Stack voltage, power and average sub-module energy deviation in the Hybrid MMC at different modulation indexes. Converter generating an output of 1 pu P and 0.3 pu Q in all cases.

In [57], a derivation that aims to find the maximum practical modulation index was presented. However the derivation assumed that only a specific portion of the full-bridge portion of the stack is used for negative voltage generation. They found that a modulation index greater than 1.3 causes the full-bridge to diverge in voltage from the half-bridges.

No satisfactory analytical method was found that gave satisfactory results on the maximum upper modulation index for a given modulation index and ratio of full- to half-bridge sub-modules. Instead a script which implements a perfect voltage balancing mechanism was implemented, and then the modulation index stepped across a range to allow the upper limits to be found. Both design cases, where the converter is designed to block the fault current under DC fault conditions, and when it is designed to be capable of operating as a STATCOM were examined. The difference in energy between the average energy within a full-bridge and half-bridge within the stack at the end of one fundamental cycle was then checked. The four outer points of the GB grid specification were checked for each case. The results are shown in Fig. 3.19. Values of zero indicate that balancing is possible across each cycle, whereas non-

zero values indicate that the converter will not be able to balanbce the energy content in the full-bridge and half-bridge sub-modules. From these results, a practical limit of 1.4 on the modulation index can be inferred if the converter is designed to fault block. The converter designed for DC fault ride through can operate at a slightly higher modulation index due to an increased ratio of full-bridges to half-bridges within each stack.



(a) Converter designed to DC fault block.

(b) Converter designed for DC fault ride through.

Figure 3.19: End of cycle energy deviation between full- and half-bridge sub-modules within Hybrid MMC with variation in set-point and modulation index.

Another design issue that has been identified in the Hybrid MMC is that while it still may be possible to balance the full-bridge and half-bridge portions of the stack over each cycle, it may not be possible to do this by the time the overall energy deviation of the stack reaches its maximum point. This condition would result in an imbalance between the peak average voltages that the full- and half-bridge portions of the stack reach, which may require further de-rating of the sub-modules. This issue is illustrated in Fig. 3.18c.

To mitigate this problem a closed loop controller has been developed which adjusts the nominal voltage for the full-bridge sub-modules and the half-bridge sub-modules, so as to even the peak average voltage that each set of sub-modules reaches. This adjustment is done on an overall energy balance basis, so that the overall nominal energy levels within the stack are not

disturbed. The controller is illustrated in Fig. 3.20.

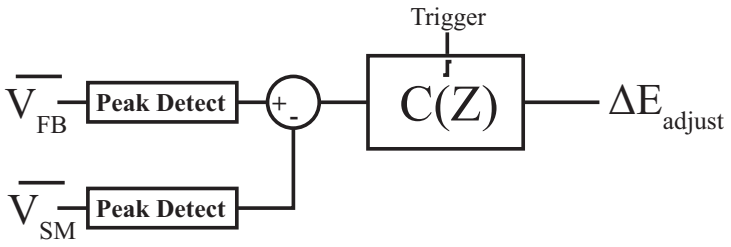


Figure 3.20: Nominal voltage set-point controller.

The error signal for the controller is generated by comparing the measured peak, over the previous cycle, of the average full-bridge sub-module voltage, to the peak average sub-module voltage. The output of the controller then adjusts the set-point for the nominal energy in each portion of the stack, as in (3.54) and (3.55). The controller adjusts its output once a cycle.

$$E_{\mathrm{FB}} = E_{\mathrm{nom}} K_{\mathrm{FB}} + \Delta E_{\mathrm{adjust}} \tag{3.54}$$

$$E_{\mathrm{HB}} = E_{\mathrm{nom}} \left(1 - K_{\mathrm{FB}}\right) + \Delta E_{\mathrm{adjust}} \tag{3.55}$$

The nominal voltage that for each sub-module type is then calculated from (3.54) and (3.55). The measured sub-modules within the stack are then normalised by these values, and then passed to the sub-module voltage balancing mechanism.

$$V_{\mathrm{FB}_{\mathrm{nom}}} = \sqrt{\frac{2E_{FB}}{K_{FB} NC}} \tag{3.56}$$

$$V_{\mathrm{HB}_{\mathrm{nom}}} = \sqrt{\frac{2E_{HB}}{\left(1 - K_{FB}\right) NC}} \tag{3.57}$$

The operation of this controller is illustrated in Fig. 3.21. The controller is activated at t=0.1

seconds. Before this an imbalance between the peak full-bridge and half-bridge voltages can be seen, with the full-bridge sub-modules reaching higher peak voltages. When the controller is activated the nominal set-points of full- and half-bridge are quickly adjusted, and reach and equilibrium point where the peak voltages of both sets of sub-modules are roughly equal. Using this controller, the assumption that the nominal sub-module voltage can be chosen based upon the maximum energy deviation is considered valid.

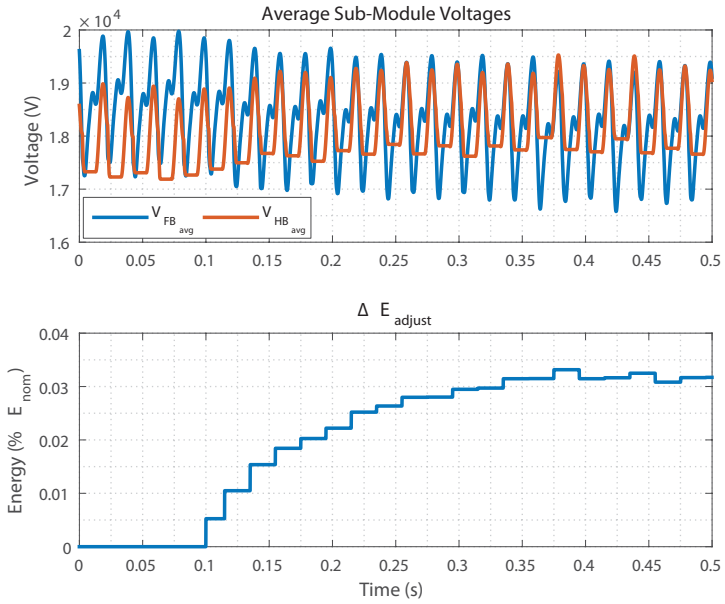


Figure 3.21: Controller adjusting the nominal voltage of the full- and half-bridge sub-modules to balance the peak voltage reached by each group within a hybrid stack.

3.4.2.2 Rating for Blocked Operation during DC Faults

If the converter is designed simply to block the AC fault current contribution to the fault then the full-bridge portion of the stack can be sized according to the maximum AC line voltage, following the analysis presented in [57].

When a DC fault happens the DC voltage can drop down to zero volts. Examining the circuit diagram shown in Fig. 3.22, it can be seen the AC line voltage is blocked by the series

combination of a full-bridge stack within an upper arm of the converter, and a full-bridge stack within a lower arm of the converter.

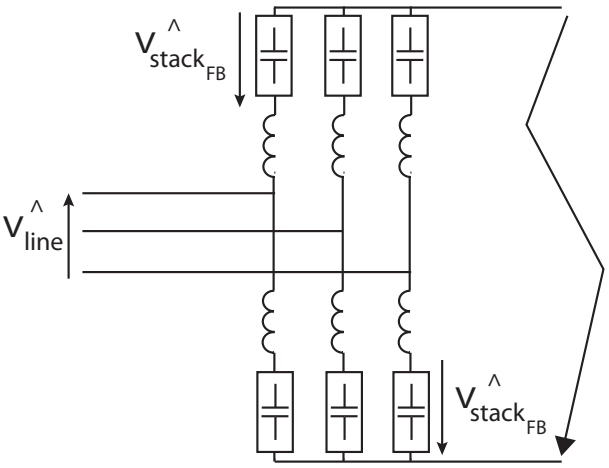


Figure 3.22: Peak reverse voltage requirement of the converter stacks in a mixed-stack MMC under a pole-to-pole DC short circuit conditions.

The full-bridge stacks must therefore be rated as in (3.58), to generate a negative voltage equal to half of the peak AC line voltage.

$$V_{\mathrm{Rated_{FB}}} = \frac{\sqrt{2}}{2} \hat{k_{\mathrm{AC}}} V_{\mathrm{LL}} \tag{3.58}$$

Substituting in the expression for the line to line voltage from (3.3), and simplifying gives expression (3.59), for the rated negative voltage, $V_{\mathrm{Rated_{FB}}}$, that each stack of the converter must be capable of generating.

$$V_{\mathrm{Rated_{FB}}} = \frac{\sqrt{3}}{2} m \hat{K_{\mathrm{AC}}} V_{\mathrm{DC}} \tag{3.59}$$

The number of required full-bridges, N_{FB}, within each stack is then given by the rating of the full-bridge stack, divided by the nominal sub-module capacitor voltage.

$$N_{\mathrm{FB}} = \frac{\sqrt{3}}{2} \frac{m\hat{K_{\mathrm{AC}}} V_{\mathrm{DC}}}{V_{\mathrm{SM_{nom}}}} \tag{3.60}$$

3.4.2.3 Rating for DC Fault Ride Through & STATCOM Operation

If the converter needs to be rated to perform a DC fault ride through, then the sizing of the full-bridge can be carried out in a similar manner to the overall stack, based upon the worst case energy deviation under DC Fault conditions, or the peak energy deviation condition, whichever is found to be the limiting condition on the converter's operation.

Sizing Under Stack Voltage Capability Restriction Depending on the converters specification for STATCOM operation, either the stack voltage capability, or the peak sub-module voltage limit could be the limiting factor in the converters design. For the case where the stack voltage capability is the limiting factor the required ratio of full-bridge to half-bridge sub-modules can be determined by following the methodology given below.

The overall number of sub-modules within the stack is given by N. The ratio of full-bridge to half-bridge sub-modules is given by K_{FB}. The number of the full-bridge sub-modules within the stack can then given by $N_{\mathrm{FB}} = K_{\mathrm{FB}}N$. Under the assumption that the same capacitor and nominal voltage are used for both the full- and half-bridges, then the ratio K_{FB} also describes the ratio of the energy stored within the full-bridge, to the overall energy stored within the stack. In this case, the value of K_{FB} can then be solved for by adapting (3.49) for the DC Fault (DCF) case. This is given in (3.61), where $V^{\mathrm{crit\ DCF}}$ and $E^{\text{-}}_{\mathrm{safety}}$ are the stack voltage and energy deviation of the stack at the critical point under DC fault conditions, and $E_{\mathrm{safety_{FB}}}$ is whatever safety margin is applied upon the design. The critical point should be chosen so that it occurs when the stack voltage is negative, as the converter will be able to utilise its half-bridge sub-modules to generate voltage during the positive portion of the stacks voltage waveform.

$$\frac{1}{2}\frac{C}{K_{\mathrm{FB}}N}V_{\mathrm{stack}}^{\mathrm{DCF}}(\omega t_{\mathrm{crit}})^2 = K_{\mathrm{FB}}N\frac{1}{2}C{V_{\mathrm{SM}_{\mathrm{nom}}}}^2 + \Delta E^{\mathrm{DCF}}(\omega t_{\mathrm{crit}}) - \bar{E}_{\mathrm{safety}} \tag{3.61}$$

Multiplying across and placing in terms of K_{FB} gives the polynomial expression given in (3.62). This can be solved to give the required value of K_{FB}.

$$K_{\mathrm{FB}}^2(NV_{\mathrm{SM}_{\mathrm{nom}}})^2 + K_{\mathrm{FB}}(NV_{\mathrm{SM}_{\mathrm{nom}}})^2\Big(\frac{\Delta E^{\mathrm{DCF}}(\omega t_{\mathrm{crit}}) - \bar{E}_{\mathrm{safety}}}{N\frac{1}{2}C{V_{\mathrm{SM}_{\mathrm{nom}}}}^2}\Big) - V_{\mathrm{stack}}^{\mathrm{DCF}}(\omega t_{\mathrm{crit}})^2 = 0 \tag{3.62}$$

Sizing Under Peak Sub-Module Voltage Limitation If the peak sub-module voltage limit is found to be the limiting factor in the converter its reactive power specification under DC fault conditions then the required ratio of full-bridge to half-bridge within the stack can be solved for using the following method.

The maximum nominal energy that a sub-module can be operated at under DC fault conditions can be determined using the expression given in (3.63), based upon the energy within the sub-module when it is at its peak rated voltage, and the peak positive energy deviation of the stack, divided by the number of full-bridge sub-modules.

$$E_{\mathrm{SM}_{\mathrm{nom}}} = \frac{1}{2}CV_{\mathrm{SM}}^{\mathrm{max2}} - \frac{\hat{\Delta E^{\mathrm{DCF}}}}{K_{\mathrm{FB}}N} \tag{3.63}$$

This can be rearranged in terms of K_{FB}, as in (3.64).

$$K_{\mathrm{FB}} = \frac{\hat{\Delta E^{\mathrm{DCF}}}}{N\big(\frac{1}{2}CV_{\mathrm{SM}}^{\mathrm{max2}} - E_{\mathrm{SM}_{\mathrm{nom}}}\big)} \tag{3.64}$$

3.4.3 Results

A detailed design sweep of a Hybrid MMC designed using the methodology presented in the previous section was carried out for three sub-modules capacitor sizes. The inputs to the design script are given in Table 3.2, and are chosen to match those give in Table 3.1. The arm inductor

sizes are reduced to 0.1 pu as the converter no longer needs to be rated for the peak fault current experienced during DC pole to pole faults [49], 0.1 pu was found to be sufficient for control purposes. The P/Q specification used is taken from the GB grid code requirements for voltage source converters [65]. It calls for the converter to be capable of generating 0.3/-0.5 pu reactive power, whilst at rated active power over a ±5% variation in AC voltage. The DC voltage is assumed to be well controlled to its nominal value.

Table 3.2: Converter Design Specification

Design Inputs	
Rated Power	1.575 GW
DC Current	1500 A
Modulation Index	1.2
Q at Rated Power	0.3/-0.5 pu
Q under DCF	0.3/-0.5 pu
DC Voltage	+-525 kV
AC Voltage Variation	+-5%
Peak sub-module Voltage	2000 V
E_{safety}	3 kJ/MVA
$E_{\text{safety}_{\text{FB}}}$	3 kJ/MVA
Transformer Leakage Reactance	0.14 pu
Arm Inductor	0.1 pu

The results of this design sweep are shown in Fig. 3.23. As the modulation index is increased, the rated voltage of the stack needs to rated for a comparatively smaller amount above the peak stack voltage demand. This is due to the reduced energy deviation. For the two smaller capacitor sizes considered, a decrease in the required rating of the stack above the peak voltage demand is seen. In addition to this the sub-modules within the converter need to have the nominal voltage de-rated below $V_{\text{SM}}^{\text{max}}$ by a smaller amount, leading to increased utilisation of the sub-modules. These factors combine to reduce the required increase in sub-modules as the modulation index increases. Sizing the converter to perform STATCOM operation under DCF conditions comes at a penalty of an increased ratio of full-bridges to half-bridges in all cases.

The variation in the the value of N with the sub-module capacitor used is quite large at

low values of m. As m is increased this difference is reduced. For the case with the smallest considered capacitor size the value of N decreases initially as m is increased, before increasing again once a value of m=0.95 is reached. The overall number of devices (N_{Dev}) within the current path (1 for each half-bridge, 2 for each full-bridge) increases at a relatively shallow incline as the modulation index increases.The RMS current flowing through the arm ($I_{\mathrm{arm}}^{\mathrm{RMS}}$) decreases as the modulation index is increased due to the reduced AC current component flowing through the converter arms. The product of $I_{\mathrm{stack}}^{\mathrm{RMS}}$ and N_{Dev}, which can be used as an estimate of the expected power-losses within the converter, shows a notable decrease as the modulation index is increased from 0.8 to 1.2. From 1.2 to 1.4 it is relatively level, with a slight upwards trend observed as the modulation index increases past 1.4.

Efficiency estimates for Hybrid MMC designs using the three considered sub-module capacitor sizes with stepped changes in modulation index were undertaken using the power-loss calculation method presented in [66]. The results of this are shown in Fig. 3.24. The IGBT used was a 3.3 kV 1500A device from ABB semiconductors [67]. The results show a relatively sharp decrease in the overall losses as design is pushed into the over-modulation. Most of the gains in terms of efficiency improvements are accrued by a modulation index of 1.2, with a levelling out in losses past this point. At lower modulation indexes there is noticeable variation in the power-losses with the sub-module capacitor used. This difference is reduced as the modulation index is increased. This indicates that a sub-module capacitor which may be an uneconomic choice for use in a design which does not over-modulate, such as a half-bridge MMC, may be a more viable choice in an over-modulating design. This could offset some of the increased capital cost associated with the increased number of sub-modules if the converter is designed to over-modulate.

3.4.4 Experimental Results

To verify the design methodology presented, as well as verifying the operation of the converter at a modulation index of 1.2, a Hybrid MMC was dimensioned and tested using the lab-scale

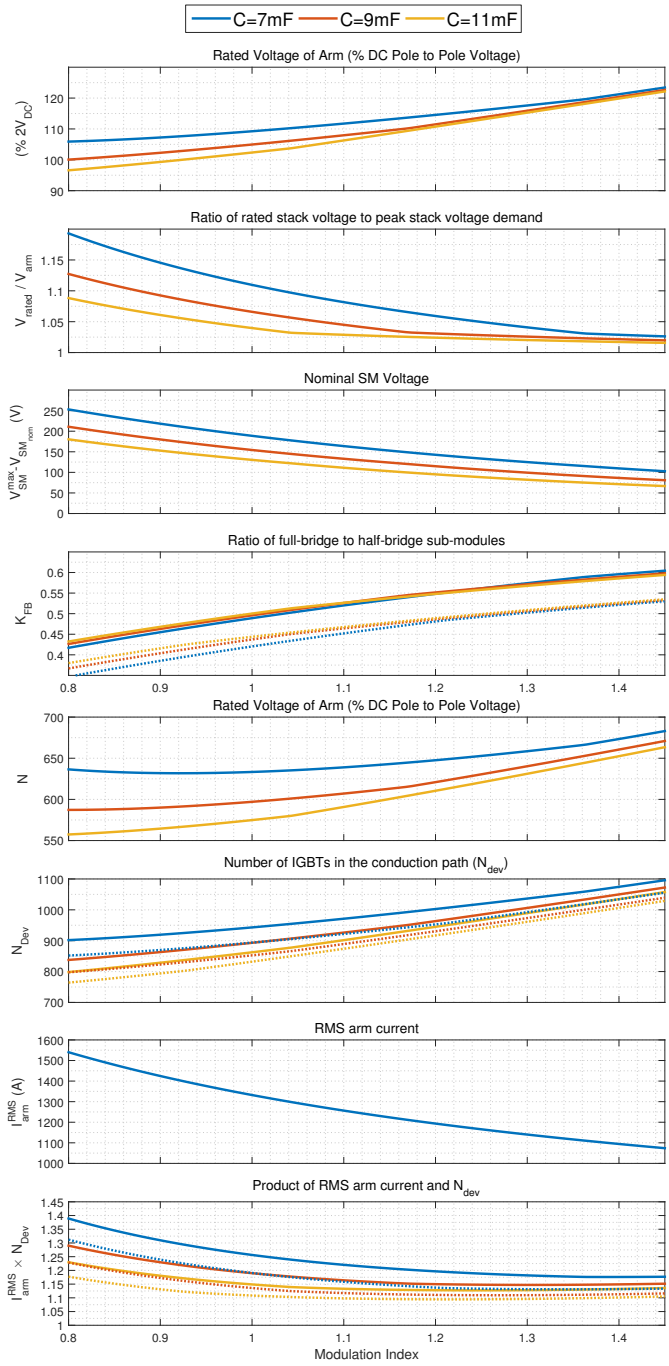


Figure 3.23: Hybrid MMC design variation with modulation index. Solid lines show rating for STATCOM operation, dashed lines show rating for blocked operation.

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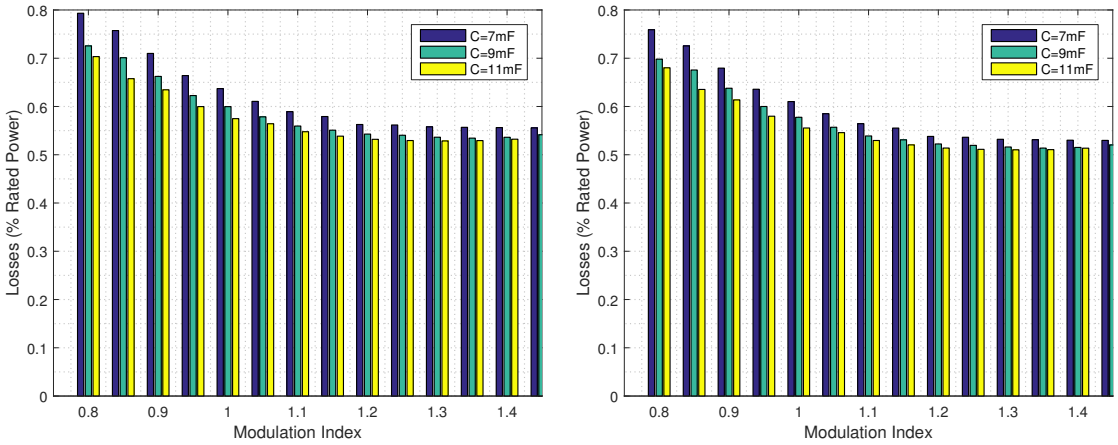


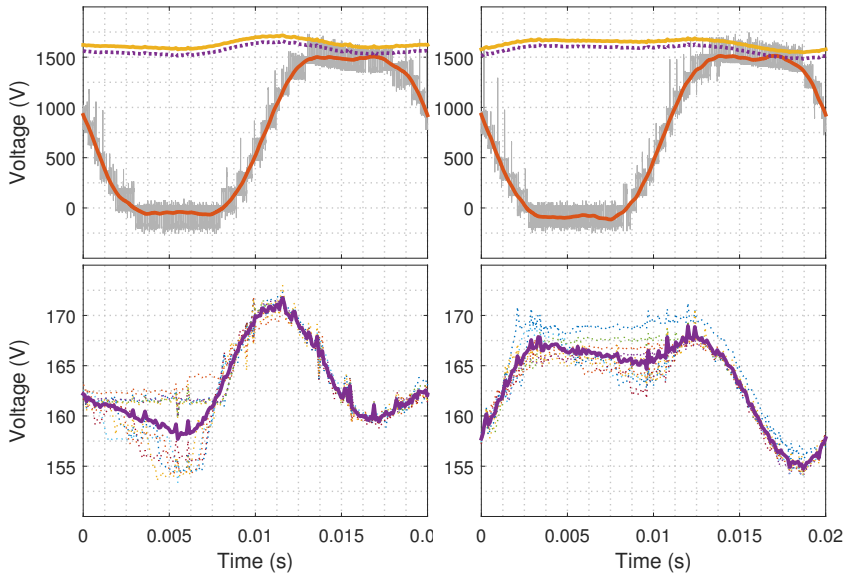
Figure 3.24: Variation in estimated losses in a Hybrid MMC designed with a 9 mF sub-module capacitor with the modulation index. a) Rating for STATCOM operation during DC faults b) Rating for DC fault blocking

multilevel converter. Because the lab-scale converter has only 10 sub-modules per stack, it was not possible to do the experiment using a design with $K_{\mathrm{FB}} = 0.55$ and a modulation index of 1.2. A sweep of design inputs, with variation in the sub-module capacitor, DC voltage and peak rated sub-module voltage was undertaken. By relaxing the AC voltage variation on the P/Q capability to 0%, a solution was found with a required number of sub-modules close to 10, and a required number of FBs close to 5. The inputs and outputs from the design is given in Table 3.3. The leakage inductance of the transformer is significantly below that of the simulation model, given in Table 3.2, due to the limitations of experimental rig.

The converter was run using the parameters from the table above, with the values of N and N_{FB} rounded to 10 and 5 respectively. Two outer points of the P/Q specification were tested during steady-state operation. Results from each run are given in Fig. 3.25. The sub-module voltages were logged using the OPAL-RT controllers data acquisition system. The arm current and stack voltage were logged with an oscilloscope using a current probe and differential voltage probe. A moving average of the measured stack voltage was generated and overlaid on the measured stack voltage. The converter can be seen to be operating close to its design limits in both set-points tested, with the mean sub-module voltage reaching

Table 3.3: Design Inputs and Solution

Design Inputs		Design Solution	
Rated Power	15kW	N	9.932
m	1.2	N_{FB}	5.095
Q at Rated Power (pu)	0.3/-0.5	Nominal sub-module Voltage	162 V
Q under DCF (pu)	0.3/-0.5	Nominal Energy Storage	40.2 kJ/MVA
SM Capacitor	770 uF	Rated Voltage of Stack	1.609 kV
DC Voltage	725 V	Rated Voltage of FBs	0.825 kV
AC Voltage (RMS L-L)	1066 V		
AC Voltage Variation	+-0%		
Peak sub-module Voltage	170 V		
E^{+}_{safety}	3 kJ/MVA		
E^{-}_{safety}	3 kJ/MVA		
Transformer Leakage Reactance	6 mH (0.025 pu)		
Arm Inductor	23.5 mH (0.095 pu)		



(a) a) (b) b)

Figure 3.25: Hybrid MMC experimental verification. Top: stack voltage, moving average of stack voltage, sum sub-module capacitor voltage, design safety limit (dashed line. Middle: sub-module Voltages (dashed) and mean sub-module voltage (solid). Bottom: arm current a) P: -1 Q: 0.3 - converter limited by Peak Sub-Module Voltage Limit b) P: -1 Q: -0.5 - converter limited by Stack Voltage Limit

The converter was also tested under a DC fault scenario, the results of which are shown in Fig. 3.26. Prior to the fault the converter was set to generate -1 pu active power and 0.3 pu reactive power. When the DC fault is detected the converters controller is programmed to drop its active and reactive power set-point, and then ramp back up to its reactive power set-point after one cycle. During the DC fault the converter periodically attempts to recharge the DC bus by injecting a small amount of active power into the DC system. When the fault is cleared the controller detects a rise in the DC voltage when it injects active power. The controller then actively recharges the DC bus voltage and ramps back to its pre-fault set-point. The sub-module voltages are well controlled during the fault, with a slight disturbance to their levels at point of fault inception and during the re-charge stage. The converter retains current control throughout the fault.

A close up of the DC fault results, focusing on the internal converter currents and voltages in the upper arm of phase A the 5 cycles following the fault inception is given in Fig. 3.27. The filtered moving average of the stack voltage can be seen to be moving slightly past the safety margin, but still below the overall available voltage within the stack. This is because the fault results in some disturbance to the energy levels within the converter. Such disturbances can be expected and are one of the reasons why the energy safety margin was included within the design specification. In addition the lab-scale converter has 5 FB sub-modules, whereas the design called for 5.095. The rated negative voltage capability of the stack is therefore slightly below the required level given by the design method.

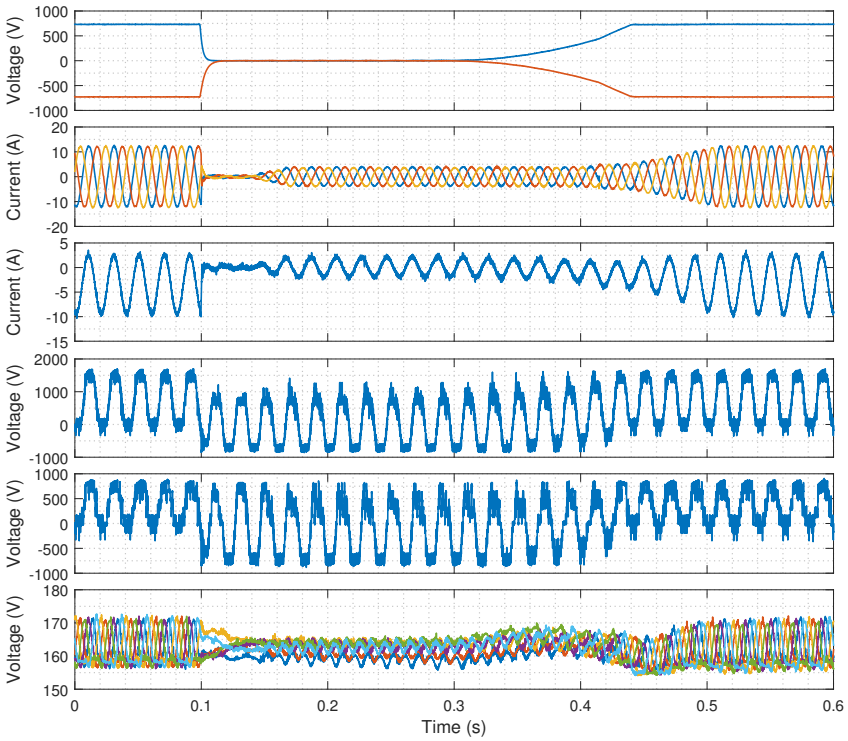


Figure 3.26: Experimental results from the lab-scale multilevel converter operating as a Hybrid MMC going through a DC fault scenario. Pre-fault set-point is P: -1 pu Q: 0.3 pu. From top: DC pole voltages, AC side current at secondary side of transformer, upper arm current - phase A, upper stack voltage, FB portion of stack voltage, average sub-module voltages.

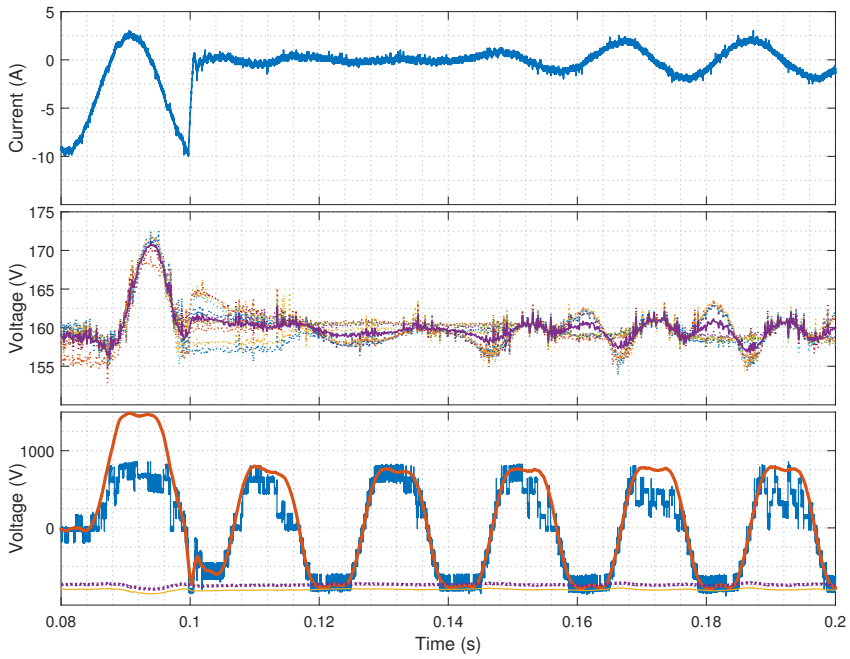


Figure 3.27: Internal current and voltages of upper arm of the phase A during DC fault. Top: Arm current Middle: sub-module voltages (dashed) and mean sub-module voltage (solid) Bottom: moving average filtered overall stack voltage, stack voltage generated by FBs, available negative voltage and safety margin

3.5 Chapter Conclusion

In this chapter a methodology based upon analytical derivations for sizing both a half-bridge MMC and the Hybrid MMC were presented. Results indicate that a practically sized MMC must have a least 30 kJ/MVA of energy storage in order to function correctly. Designs with lower amounts of energy storage are possible, however they require both the rated voltage of the stack to be increased past the DC pole to pole voltage, and the nominal sub-module voltage to be chosen significantly below the rated peak sub-module voltage. This results in a large increase in the required number of sub-modules for the converter to function. There was also found to be little benefit in increasing the nominal energy storage within the converter past 40 kJ/MVA.

For the Hybrid MMC inclusion of full-bridge sub-modules allows the AC voltage magnitude to be decoupled from the DC voltage magnitude. This allows greater freedom in the converters design. Moving from an under-modulating design, to a design with a modulation index of 1.2 was found to result in an almost 10% reduction in power-losses. This is achieved without resulting in a large requirement for additional sub-modules and power electronic devices. The energy deviation was also found to decrease as the modulation index increases, making smaller sub-module capacitor sizes a practical option.

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4 Semiconductor Power-Loss and Thermal Modelling

This chapter details an investigation into the power-loss and thermal characteristics of several converter topologies. Particular attention is paid to topologies which are DC fault tolerant, including the Hybrid MMC investigated in the previous chapter and the Alternate Arm Converter. To achieve this a thermal model of a heat-sink mounted IGBT as well power-loss blocks for the estimation of the losses within the semiconductor devices were developed. These models are combined to allow a closed-loop estimation of device junction temperatures taking temperature dependent variation in characteristics into account.

4.1 Thermal and Power-Loss Modelling

Manufacturers typically require that the maximum temperature at the junction of the silicon dies reached within IGBT modules be limited to below 150 ^oC, or 125 ^oC, and that the operating temperature under normal conditions be limited to 80% that of the maximum value [68, 69]. Devices with higher current ratings are typically limited to the lower value of 125 ^oC. Operating the device above this level can lead to a breakdown in reverse voltage blocking capability and thermal runaway, leading to device destruction. The system must be designed so that the junction temperature never exceeds this value.

In addition to damage to the device caused by excessive temperatures, any cycles power-losses and junction temperature that a module undergoes during its operation can have a large

impact on the expected lifetime of the module. This cycling is broken down into two time scales. The first cycling, called power cycling, occurs at time frames of around 2 seconds. This thermal cycling causes stress in the soldering of the electrical connections within the IGBT module due to the different coefficients of linear expansion. If the power cycling causes the soldering to deteriorate sufficiently then the device will experience electrical failure. Cycles at a longer time frame and with a larger change in temperature ($\triangle T_j$) are referred to as thermal cycling. This causes unequal expansion of the insulation substrate and the copper base-plate within the modules, which results in fatigue to the solder layer between them [68]. This can lead to device failure as it causes the thermal resistance of the module to increase, leading to thermal runaway as the device can no longer dissipate the power-losses incurred within the silicon dies. Manufacturers usually supply power cycle and thermal cycle capability curves for IGBT modules which allow the estimation of the lifetime of the modules. The degradation of lifetime is dependent on absolute junction temperature as well as the magnitude of the power or thermal cycle [70]. Looking beyond lifetime issues for high power applications, it is desirable to keep the junction temperature as low as reasonably possible. This is because the level of thermally generated electron hole pairs increases with temperature, thus decreasing the devices conductivity and leading to an increase in power losses.

4.1.1 ANSYS Finite Element Based Modelling of a heat-sink mounted IGBT

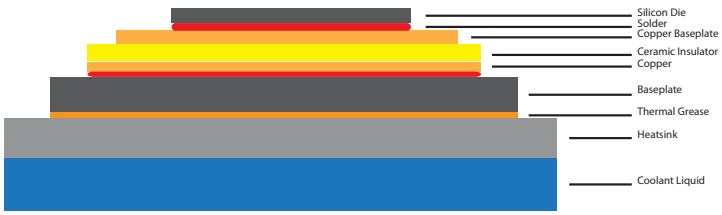
As it is impractical for this thesis to experimentally acquire a thermal model of a water-cooled device one has been developed using the Finite Element Method (FEM) electronics thermal simulation package ANSYS IcePak. The module used is from ABB Semiconductors [70] and is used for several of their high power devices, with voltage ratings in the 3.3-4.5 kV range and current ratings in the region of 1000-1800 A. This device was chosen as it is typical of the IGBT modules used in the construction of modular multilevel converters, with the exception of ABB's Cascaded Two Level Converter [29], which utilsies series connected press-pack devices.

The external view, as well as a diagram illustrating the internal construction of one of the

these modules, is shown in Fig. 4.1. Each IGBT is formed out of a parallel connection of several IGBT dies and diode dies that are connected together through an internal bus-bar and wire-bond connections. For a high-power IGBT, such as the one used in this chapter, there can be as many as 24 IGBT dies connected in parallel, with 12 diode dies. The electrical connections to the module are made via bolt that protrude from the top of the devices case. This connection are directly connected to aluminium busbars within the module. These busbars are connected to the IGBT and diode silicon dies within the module. These dies are grouped in three, two IGBT dies and one diode die, mounted upon a copper sub-busbar. Two of these groups are then mounted upon a ceramic insulator, 6 of which form the overall module. The ceramic insulators are bonded to baseplate formed of Aluminium Silicon Carbide (AlSiC). The baseplate forms the outer surface of the bottom of the IGBT module packaging.



(a) External view - Source: ABB.



(b) Internal construction

Figure 4.1: IGBT High-Pak module.

Following the method in [71], the cooling liquid is not modelled, as effectively modelling the cooling liquid requires the use of a fluid dynamics finite element modelling. Instead the cooling effect of the coolant on the heat-sink is modelled by applying a heat transfer coefficient to the boundary. This heat transfer coefficient was found and verified by experiment in [71] and is given a value of 4400 $W/K.m^2$.

The density, specific heat capacity and conductivity values used within the ANSYS model of the modules internal layers are given in Table. 4.1. Following the thermal modelling approach in [71], several layers are combined for modelling purposes.

Table 4.1: Devices internal layers physical properties.

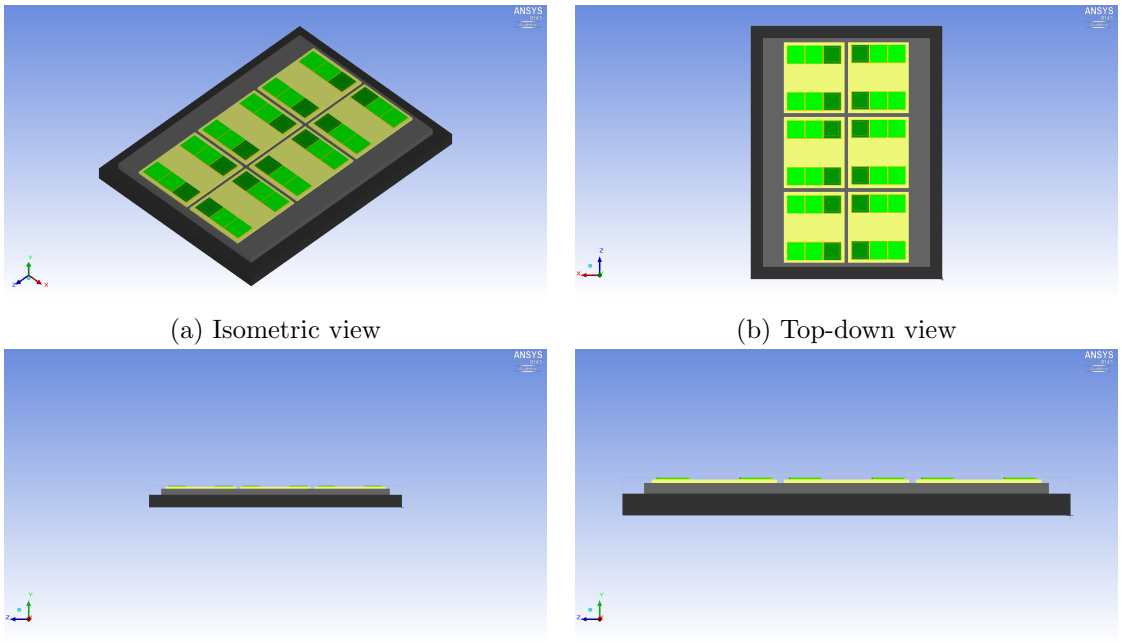
Material	Density (kg/m^3)	Specific Heat ($J/kg.K$)	Conductivity ($W/m.K$)
Silicon and Solder	2330	556.9	130
Copper	8933	195	387.6
Ain, Solder & Copper Layer	4172.4	249	153
Thermal Grease	1000	1000	1
AlSiC	2890	808	165
Extruded Aluminium	2800	900	205

Table 4.2: IGBT module internal layer dimensions.

Layer	Material	Length (mm)	Width (mm)	Depth (mm)
Silicon Die	Silicon and Solder	14.06	14.34	0.52
Copper Substrate	Copper	45	15.17	0.3
Ceramic Insulation	Ain, Solder & Copper Layer	49.535	58	1.5
Baseplate	AlSiC	137	187	5
Thermal Grease	Thermal Grease	137	187	0.05
Heat-Sink	Extruded Aluminium	157	207	10

The IGBT module, modelled within ANSYS IcePak is shown in Fig. 4.2. The modules internal bus-bars and bond-wires are not modelled. This was found to not be necessary in [71]. This is because the thermal impedance from the silicon dies, through the bond-wires and the modules

bus-bars path is dominated by the route down through the modules base-plate to the heat-sink.



(a) Isometric view

(b) Top-down view

(c) Isometric view

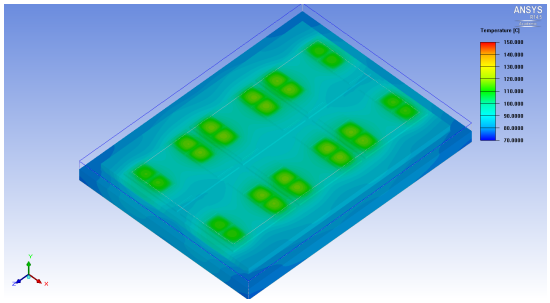
(d) Top-down view

Figure 4.2: IGBT module modelled within ANSYS IcePak.

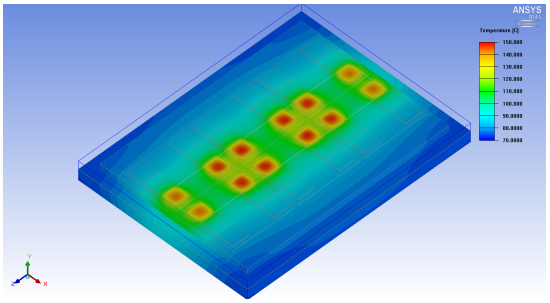
The transient thermal step response of the device is determined by inserting a 2-d heat source on top of each silicon die within the model, following [66]. Each heat source is set so that the total power applied in each case is 1 kW. In the case of the IGBT dies this 1 kW of heat is divided between 24 dies, whilst in the case of the diode it is divided between 12 dies. Measurement points are placed at the geometric centre of each silicon die, and then at each layer of the cooling path to ambient, below the die measurement points. Screen-captures of the simulation showing the final steady state temperatures reached are shown in Fig. fig:TransThermANSYS.

The diodes reach a higher temperature because the heat dissipated in both cases is a constant, but the number of diode dies is half that of the IGBT dies. A cross section through the x-axis, directly through four silicon dies, is shown in Fig. 4.4.

The transient thermal impedance response for each test is shown in Fig. 4.5.

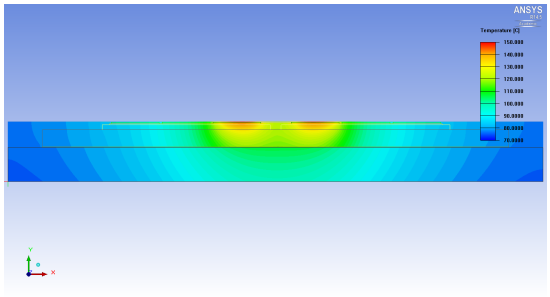


(a) IGBT dies heated.

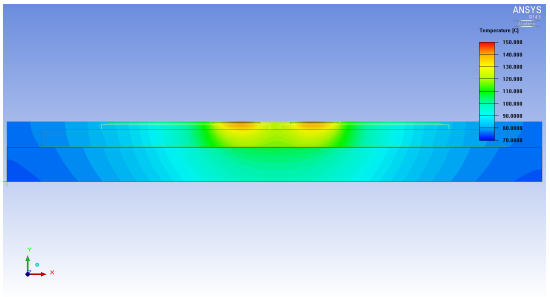


(b) Diode dies heated.

Figure 4.3: ANSYS transient thermal step response final temperature on the surface of IGBT module.



(a) IGBT dies heated.



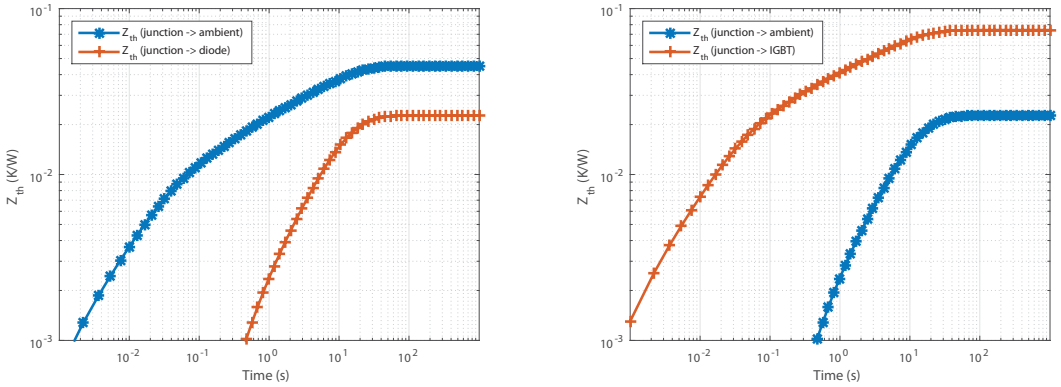
(b) Diode dies heated.

Figure 4.4: ANSYS transient thermal step response final temperature on the surface of IGBT module.

The results for each transient thermal impedance response are fitted to an equation in the form of (4.1). The curve fits are done using Matlab's curve fitting toolbox. This equation can then be transformed into the Laplace domain for use in Matlab simulations.

$$Z_{th}(t) = \sum \gamma_i \big(1 - \exp(\frac{-t}{\tau_i})\big) \tag{4.1}$$

The results of the curve fitting are shown in Table. 4.3. The results for the thermal impedance from the IGBT junction to the diode junction match very closely with the results from the diode junction to the IGBT junction. This is to be expected due to the symmetry of the tests. An average of the terms is used when calculated the cross-coupling impedance results.



(a) IGBT dies heated.

(b) IGBT dies heated.

Figure 4.5: Transient thermal impedance response of heat-sink mounted IGBT

(4.1) can be represented in the Laplace domain in the form of (4.2).

$$Z_{th}(s) = \sum \frac{\frac{\gamma_i}{\tau_i}}{s + \frac{1}{\tau_i}} \tag{4.2}$$

Transforming each transient thermal impedance into the Laplace domain results in a set of three transfer functions which represent the thermal impedance of the IGBT and diode junctions to ambient, as well as cross coupling impedances between both junctions. These Laplace equations can then be embedded within circuit level simulations.

$$Z_{th_{IGBT->Ambient}}(s) = \frac{0.2145s^3 + 3.081s^2 + 4.751s + 0.7442}{s^4 + 61.94s^3 + 419.6s^2 + 373.7s + 33} \tag{4.3}$$

$$Z_{th_{Diode->Ambient}}(s) = \frac{0.4298s^3 + 5.732s^2 + 6.876s + 1.028}{s^4 + 60.67s^3 + 383.5s^2 + 291.3s + 27.68} \tag{4.4}$$

$$Z_{th_{junction<->junction}}(s) = \frac{0.001194s + 0.0001187}{s^2 + 0.2152s + 0.01047} \tag{4.5}$$

Table 4.3: Transient thermal impedance curve fitting results.

(a) IGBT dies heated - IGBT junction to ambient.

i	τ_i	γ_i
i	0.0184	0.0034
i	0.1524	0.0037
i	1.072	0.0050
i	10.08	0.0104

(b) Diode dies heated - Diode junction to ambient.

i	τ_i	γ_i
1	0.01865	0.0070
2	0.1616	0.0078
3	1.33	0.0078
4	9.013	0.0145

(c) IGBT dies heated - IGBT junction to diode junction.

i	τ_i	γ_i
1	7.242	0.0049
2	13.75	0.0061

(d) Diode Dies Heated - Diode junction to IGBT junction.

i	τ_i	γ_i
1	7.242	0.0049
2	13.75	0.0064

4.1.2 Power-loss estimation blocks

To estimate the power-losses within individual IGBTs within a circuit level simulation of a modular converter blocks have been created within Simulink. These blocks are based upon the work presented in [66]. The output of the power-loss blocks are applied to the thermal model of the IGBT, with junction temperature feedback then applied to the power-loss block in a closed loop manner to give some junction temperature dependant scaling of device characteristics.

The power-losses within an IGBT module can be characterised into five categories:

- IGBT conduction losses
- IGBT turn-on losses
- IGBT turn-off losses
- Diode conduction losses
- Diode reverse recovery losses

Curves for each characteristic are extracted from the manufacturers data-sheet and transformed into look-up tables within simulink. In the case of the IGBT and diode conduction

losses, curves at junction temperatures of 25 ^oC and 150 ^oC are given. The switching loss characteristics are specified at a junction temperature of 125^oC, with no other curves given at other temperatures.

4.1.2.1 Conduction Losses

The conduction losses within the diode dies and IGBTs are both calculated in the same manner. The current flowing through the device is passed to two look-up tables, one with the extracted V-I characteristic at 150 ^oC and the other at 25 ^oC. The junction temperature of the device fed back from the thermal model is used to average between the two curves to get a temperature corrected forward voltage drop. This is then multiplied by the current flowing through the device to get the instantaneous power dissipation.

4.1.2.2 Switching losses

Switching events are detected based upon logic blocks which take the devices gate signal, current and voltage as inputs. The device data-sheets specify switching losses in terms of energy. Simulation models of converters are implemented as fixed time-step simulations. When a switching loss is detected, the switching energy is divided by the time-step of the simulation and applied as a single pulse of power one time-step in length.

$$P_{loss} = \frac{E_{switch}}{T_{step}} \tag{4.6}$$

An example of the power-loss and thermal model block operating is given in Fig. 4.6. The sharp spikes in the power losses correspond to switching losses while the steady. The junction temperatures. In this case most of the losses occur in the IGBT dies. The cycle-by-cycle ripple in the die junction temperatures can also be seen.

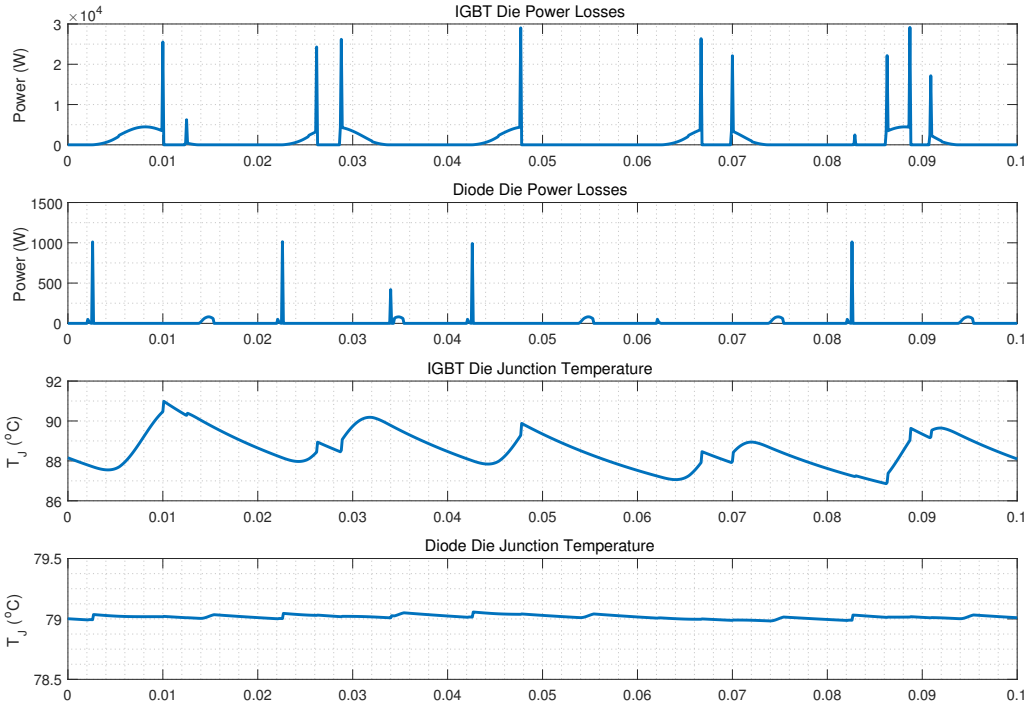


Figure 4.6: Power losses and junction temperatures within an IGBT module.

4.2 Power-loss and thermal characteristics of converters

In this section the power-loss calculation method and IGBT thermal model described in the previous sections are used to investigate and compare the power-loss and thermal characteristics of several multilevel converters, including the half-bridge MMC, several variants of the Hybrid MMC and the Alternate Arm Converter. The converters are all simulated at a $\pm 525kV$ scale and a $1.575GW$ power rating. The MMC based converters were designed using the methodology presented in Section. 3. The AAC was designed using the same 9 mF sub-module capacitor as the MMC converters. Its nominal sub-module voltage was chosen through manual adjustment using a simulation model so that the peak voltage reached is the same 2000 V design limit as the MMC based topologies. The considered topologies are summarised below:

- A half-bridge MMC that operates at m=0.96.

- The EO-AAC operating at its optimal AC to DC voltage ratio.
- A Hybrid MMC designed for DC fault ride through that operates at m=0.96.
- A Hybrid MMC that uses semi full-bridge sub-modules (described in Section. 4.2.1.1) and that operates at m=0.96.
- Hybrid MMC designs at m=1.2, one of which is designed for DC fault ride through, the other for DC fault blocking.

The characteristics of the six considered converters are given in Table. 4.5.

Table 4.5: Converter specifications.

	Half-Bridge MMC	AAC	Hybrid MMC	Hybrid MMC w. Sparse FB	Hybrid MMC	Hybrid MMC
V_{DC}	$\pm 525kV$	$\pm 525kV$	$\pm 525kV$	$\pm 525kV$	$\pm 525kV$	$\pm 525kV$
V_{AC}	617 kV	857 kV	617 kV	617 kV	772 kV	772 kV
Modulation Index (m)	0.96	1.332	0.96	0.96	1.2	1.2
DC Fault Strategy	NA	DCFRT	DCFRT	Block	DCFRT	Block
C	9 mF	9 mF	9 mF	9 mF	9 mF	9 mF
Nominal sub-module Voltage	1.836 kV	1.91 kV	1.836 kV	1.836 kV	1.882 kV	1.882 kV
Number of Half-Bridges	589	0	297	338	277	320
Number of Full-Bridges	0	367	292	251	348	305
Total number of sub-modules	589	367	589	589	625	625
Number of Director Switches	0	354	0	0	0	0
Number of IGBTs	1178	1822	1762	1516	1946	1860
Number of Additional Diodes	0	0	0	251	0	0
Nominal Energy Storage (kJ/MVA)	34	22.95	34	34	37.95	37.95

Because of the number of converters examined in this section, the analysis is split into sections based upon sub-module type. The last section then presents the overall power-losses within each converter, as well as the maximum device junction temperatures and overall required number of IGBTs, sub-modules and capacitors within each converter. An ambient coolant temperature of 70 ^oC is assumed for all cases.

4.2.1 Overview of Work in the Literature

Work in the literature on this area has mostly focused upon the half-bridge MMC. In [72] the power-losses and thermal characteristics of MMCs is investigated. The study is carried out

using power-loss and thermal models that employ junction temperature feedback. The authors find that there is a significant imbalance in the junction temperatures between the upper and lower IGBTs within each sub-module of the MMC when it is processing active power.

In [72], the impact of thermal cycling stress on the estimated lifetime of IGBTs within MMCs used for drive applications is investigated, considering various control strategies. The authors conclude that the zero sequence voltage imposed on the converters waveform may have a significant impact on the distribution of losses within the converter.

In [73], the potential for using circulating currents within Modular Multilevel Converters to limit the amplitude of thermal cycling caused by changes in output power are investigated. The authors find that it is possible to reduce the change in junction temperature within during a stepped load change from 1 pu to 0.5 pu active power by 50%.

In [74] average models of the conduction and switching losses within an MMC are derived and validated against simulation results. The authors found that the modulation method that they considered, based upon nearest level control and the sorting algorithm, introduces a slow cycling in junction temperatures between IGBTs in different sub-modules within the converter.

In [75] a steady-state model of an MMC, including device losses as well as losses in the inductors and cooling system, is developed.

In [76] the development of an electro-thermal model of an MMC implemented on an FPGA for real-time applications is detailed.

In [77] analytical expressions for the losses within an MMC are derived. The authors find the overall losses are in the region of 0.92% when operating at rated power. This is with a relatively small IGBT (800 A) and a 200 MW test case converter. The switching losses are also comparatively large in comparison to the results from other authors.

4.2.1.1 Sparse Full-Bridge

The Sparse or Semi Full-Bridges, shown in Fig. 4.7 has attracted some attention [78, 79, 61] as a possible method of implementing Hybrid Modular Multilevel Converters with DC fault

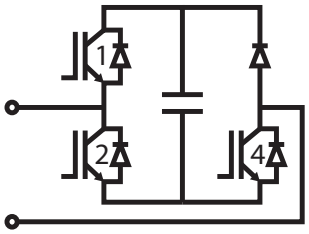


Figure 4.7: Sparse full-bridge sub-module.

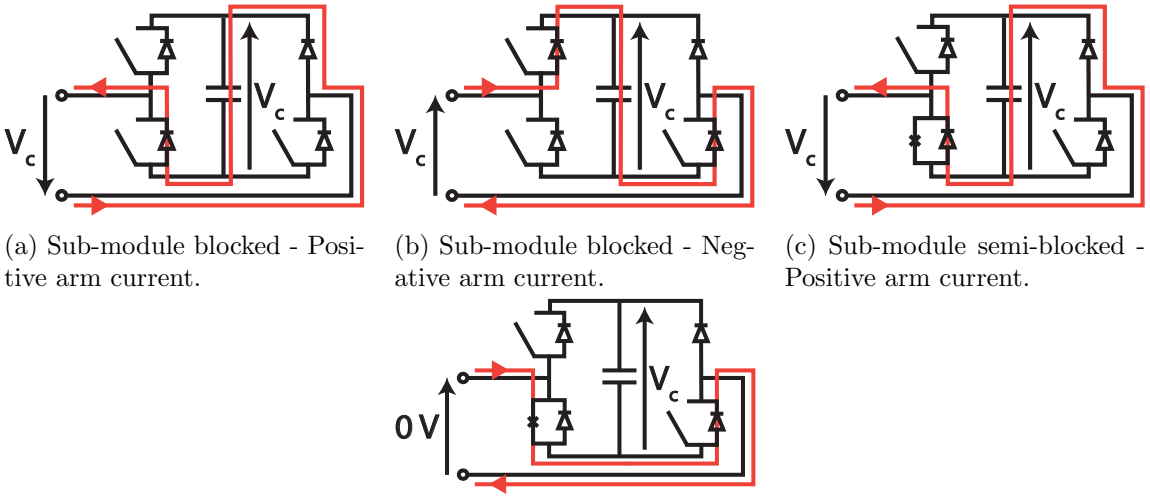
tolerance, while reducing the required number of IGBT modules within the converter. The upper right IGBT module (3) is replaced by a diode, with the diode only conducting during fault situations when the sub-module is blocked. The power-loss and thermal characterisitcs of a Hybrid MMC that is constructed using this sub-module type is investigated as part of this Chapter.

Constructing the Hybrid MMC using these sub-modules leads to a reduction in the required number of IGBT modules in the converter, with some expected gains in terms of capital cost. However this comes with the following disadvantages:

- Removal of the ability to generate a controlled negative voltage at both current polarities
- Removal of the zero-voltage generation state using the upper two IGBTs. This means the lower right IGBT (4) must continually conduct the arm current.
- Converter must be designed to not over-modulate its output during normal operation.

Two options exist for using the Semi Full-Bridge to deal with DC side faults. The sub-modules could be blocked, as shown in (a) and (b) of Fig. 4.8, in which case they will generate either a positive or negative output voltage depending on the current direction, driving the arm current to zero. Alternatively the converter could utilise the two semi-blocked states shown in (c) and (d) of Fig. 4.8 for the portion of the cycle where the stack must generate a negative voltage. This allows the converter to retain partial control over the currents flowing through the converter arms. By attempting to generate a negative stack voltage, the controller will

quickly drive the current to zero. The converter can then remain connected to both the DC and AC buses during such fault situations. However, unlike the Hybrid MMC with full-bridge sub-modules, and the AAC, the Hybrid MMC with semi full-bridge sub-modules is not capable of controlling the AC side currents to a non-zero value i.e it cannot function in STATCOM mode during DC side faults.



(a) Sub-module blocked - Positive arm current.

(b) Sub-module blocked - Negative arm current.

(c) Sub-module semi-blocked - Positive arm current.

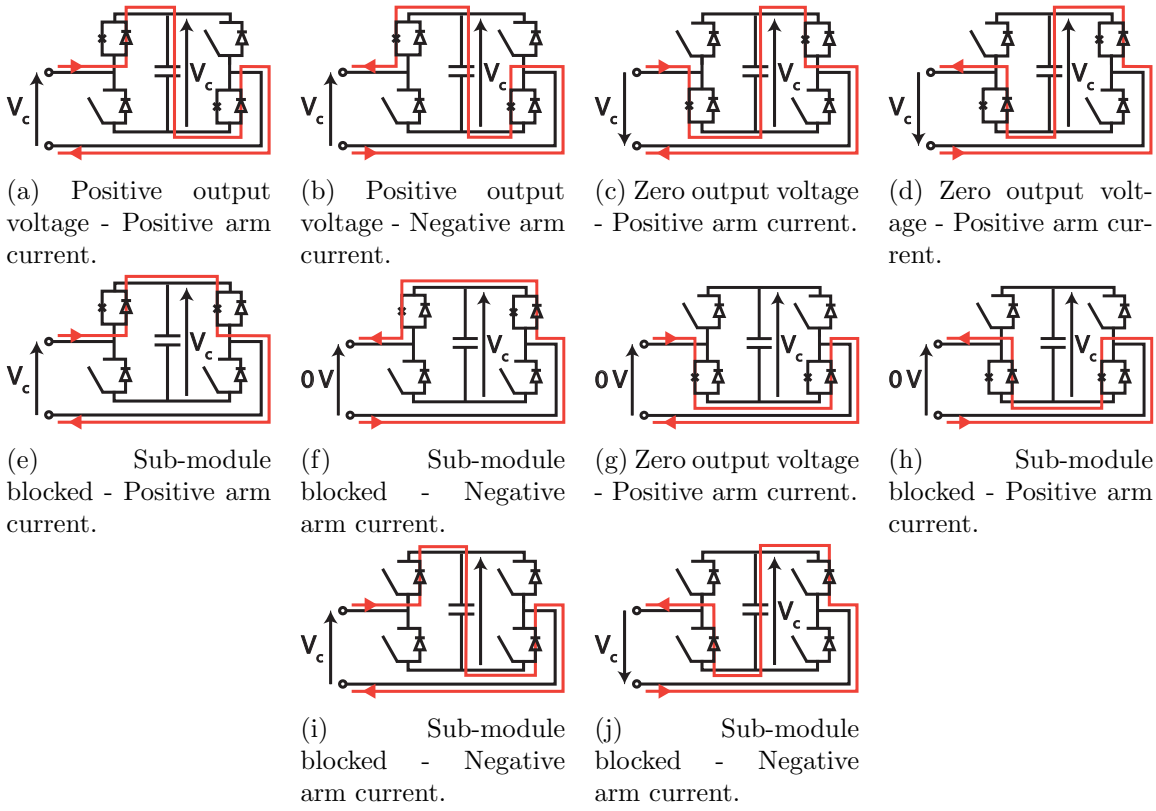
(d) Sub-module semi-blocked - Negative arm current

Figure 4.8: Current paths through semi full-bridge sub-module.

4.2.2 Zero Voltage Duty Cycle in Full-Bridge Sub-Modules

All of the converters examined in this section utilise either half- or full-bridge sub-modules. Half-bridge sub-modules contain only two active states, and one blocked state where all IGBTs are turned off. However full-bridge sub-modules have four active states, two of which result in the same output voltage, this is illustrated in Fig. 4.9.

The existence of two active state that result in zero voltage outputs means that there exists some flexibility in what path the current takes through each sub-module. The zero-voltage state duty cycle (δ_{zv}) is defined here as the ratio of how often the lower path through IGBTs 2 and



(a) Positive output voltage - Positive arm current.

(b) Positive output voltage - Negative arm current.

(c) Zero output voltage - Positive arm current.

(d) Zero output voltage - Positive arm current.

(e) Sub-module blocked - Positive arm current.

(f) Sub-module blocked - Negative arm current.

(g) Zero output voltage - Positive arm current.

(h) Sub-module blocked - Positive arm current.

(i) Sub-module blocked - Negative arm current.

(j) Sub-module blocked - Negative arm current.

Figure 4.9: Full-bridge current flow routes.

4 is utilised, as opposed to the upper path through IGBTs 1 and 3. A δ_{zv} of 0% corresponds to only IGBTs 2 and 3 being used, while a δ_{zv} of 100% corresponds to only IGBTs 1 and 4 being used.

By adjusting the value of δ_{zv}, some control over the distribution of power losses within the sub-module can be gained. This is illustrated in Fig. 4.10 for the case of a full-bridge in an AAC operating at rated inverting power. By adjusting δ_{zv} the power-losses in the IGBT modules 1 and 4 can be made to vary by approximately 800 W, corresponding to a temperature swing of 24 ^oC.

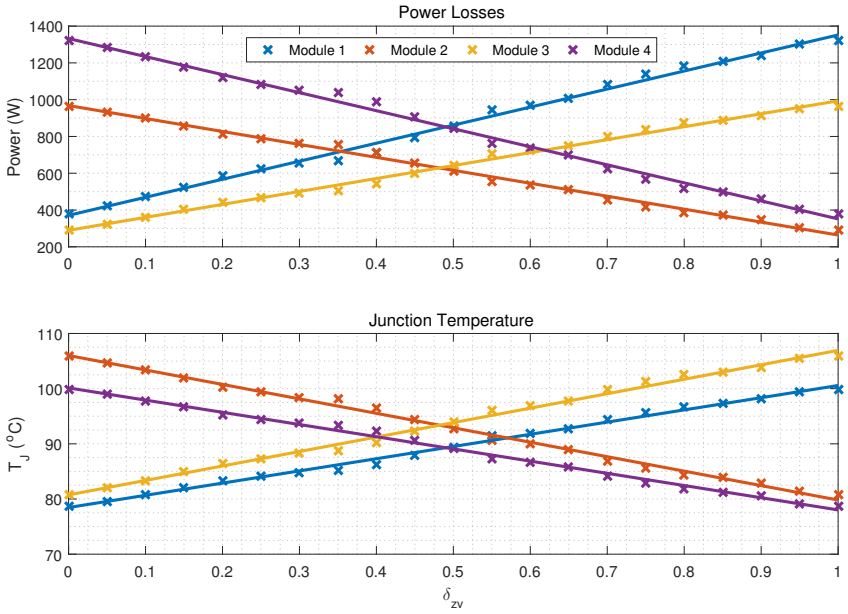


Figure 4.10: Variation in power-loss and resulting junction temperatures with a full-bridge with δ_{zv}.

This flexibility could be used to re-distribute the losses within a full-bridge sub-module if one of the devices is detected to be experiencing higher junction temperatures. An example simulation of this is given in Fig. 4.11. The power-losses within IGBT 1 were increased by 100% at t=5 s. The controller detects the increase in junction temperature and adjusts δ_{zv} in response. The dashed lines show the resulting temperature if δ_{zv} was kept to a constant 0.5 throughout. The maximum junction temperature reached in the sub-module can be seen to decrease if δ_{zv} is adjusted to account for the uneven spread in losses.

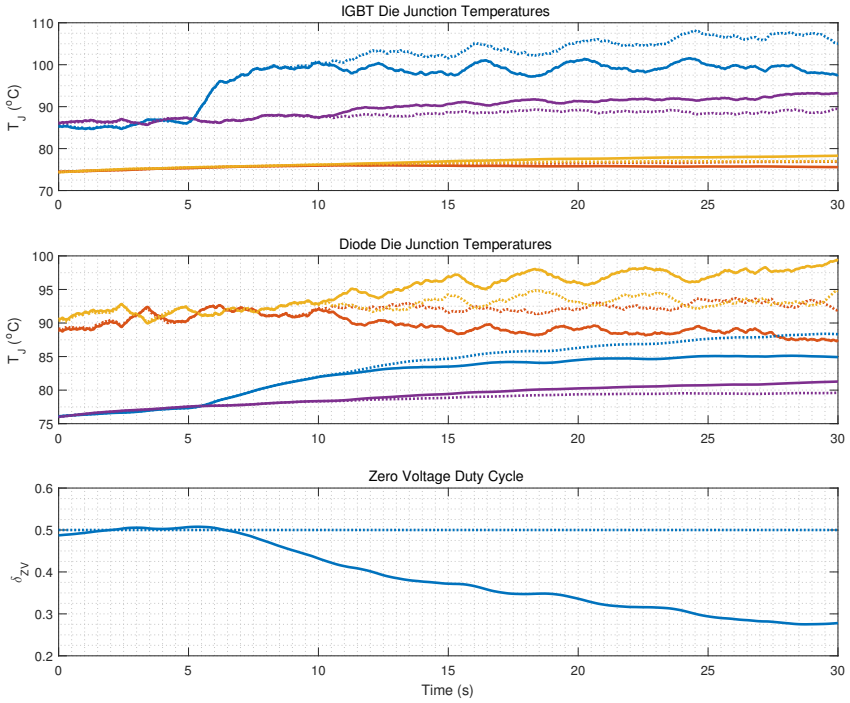
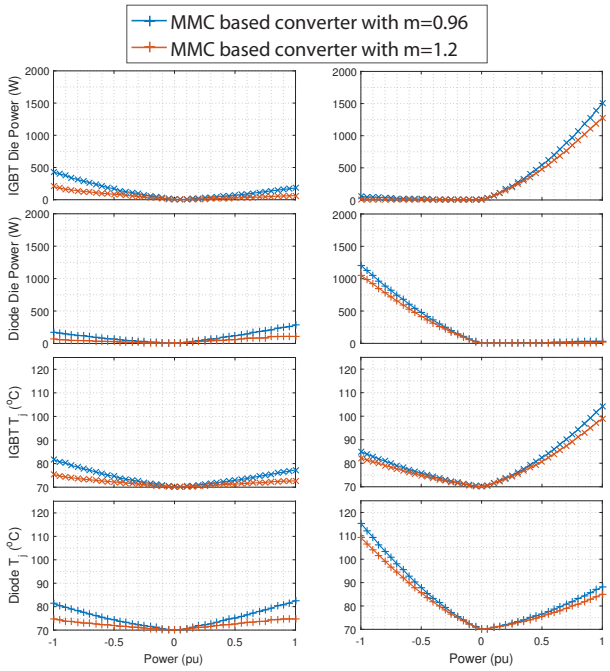


Figure 4.11: Online zero-voltage duty cycle adjustment to re-balance the junction temperatures in a sub-module with failing IGBT module. Dashed line shows response if zero-voltage duty cycle is held constant.

4.2.3 Half-Bridge Thermal and Power Loss Characteristics

The power-losses and steady-state junction temperatures within the half-bridge sub-modules of the considered MMC based topologies are shown in Fig. 4.12. The power-loss distribution between the upper and lower IGBT module is uneven for all cases, with the lower IGBT module exhibiting significantly more power-losses. The diode in the lower sub-module is under the most thermal stress, reaching 114^oC at m=0.96 and 110^oC at m=1.2. This occurs when the converter is operating in rectifying mode. The Hybrid MMC designs that operate at m=1.2 exhibit slightly lower power-losses and junction temperatures. This is due to the lower current magnitudes that it must conduct for a given power set-point



(a) IGBT module 1. (b) IGBT module 2.

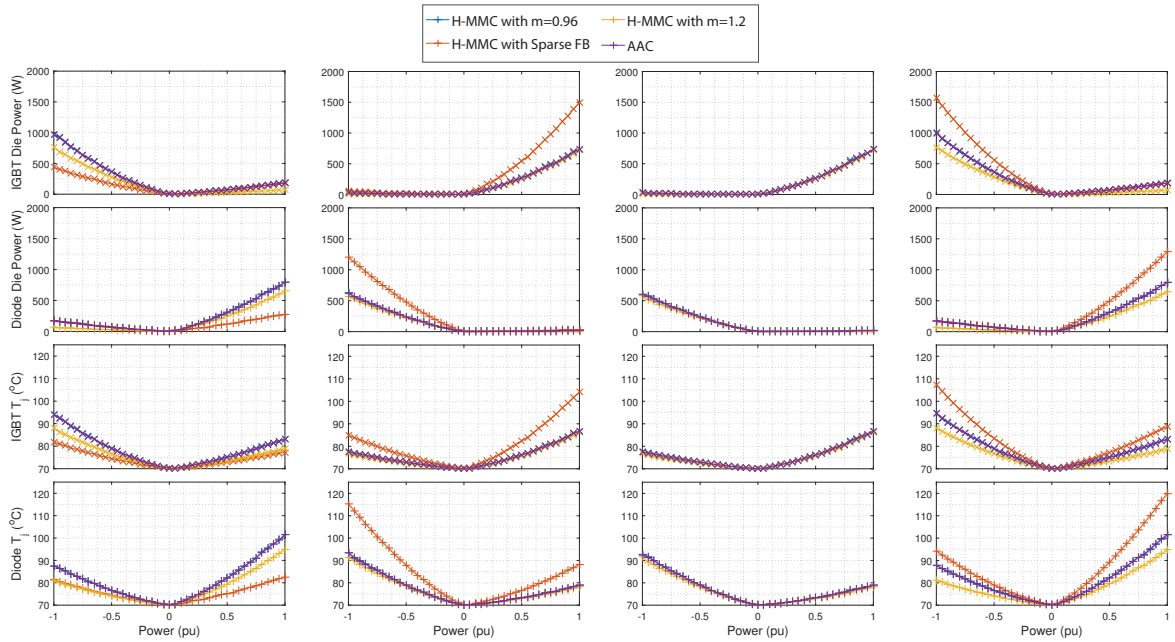
Figure 4.12: Power-loss distribution within the half-bridge sub-modules within the considered topologies.

4.2.4 Full-Bridge Sub-Module

The power-losses and associated junction temperatures within the sub-modules of the converter designs that utilise full-bridge sub-modules are given in Fig. 4.13. In all cases the δ_{zv} for each sub-module was set to 50%.

The distribution of power-losses within both the AAC and the Hybrid MMC at m=0.96 are almost identical, with IGBTs 1 and 4 showing higher loading than IGBTs 3 and 4. This is because IGBTs 3 and 4 only conduct during one of the two zero voltage generation states, while IGBTs 1 and 4 conduct during positive voltage generation and one zero voltage state each. The maximum IGBT temperature reached is $\sim 95\ ^oC$, while the maximum diode temperature reached is $\sim 100\ ^oC$. The Hybrid MMC designs at m=1.2 show a slightly lower loading one IGBTs 1 and 4. The maximum IGBT temperature reached is $\sim 88\ ^oC$, while the maximum

diode temperature reached is $\sim 95\ ^oC$. This is due to the lower current magnitudes through the converter. IGBTs 2 and 3 show similar loading to in the Hybrid MMC design at m=0.96. This is because at m=1.2, the full-bridges negative voltage state is utilised, resulting in IGBTs 2 and 3 conducting more current. The Hybrid MMC with Semi Full-Bridges exhibits a large degree of imbalance between its three IGBT modules, with both IGBTs 2 and 4 under considerable thermal stress. Max junction temperatures of 115 ^oC and 120 ^oC respectively are reached in these sub-modules, close to the operating limit of the IGBT modules.



(a) IGBT module 1 (b) IGBT module 2 (c) IGBT module 3 (d) IGBT module 4

Figure 4.13: Power-loss and junction temperatures within the IGBT modules within three different Hybrid MMC designs. From top: IGBT die losses, diode die losses, IGBT junction temperature, diode die losses.

4.2.5 Director Switch

Unlike other sub-module types the director switch of the AAC conducts the whole arm current and is nominally soft-switched, meaning switching losses should be negligible. The power-losses

and resulting junction temperatures of the AAC's director switch are given in Fig. 4.14.

The losses in both the IGBT and diode are similar to that of IGBT 4 in the sparse full-bridge sub-module in the hybrid MMC. The maximum diode junction temperature reaches approximately 120^oC, approximately 50^oC above the ambient coolant temperature of 70^oC. The maximum IGBT temperature reached is approximately 107^oC.

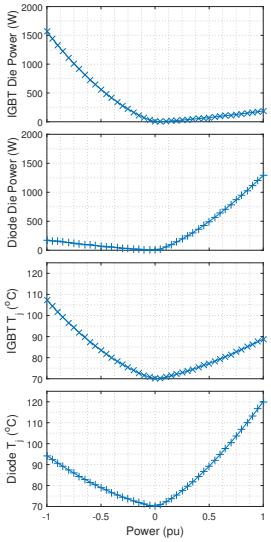


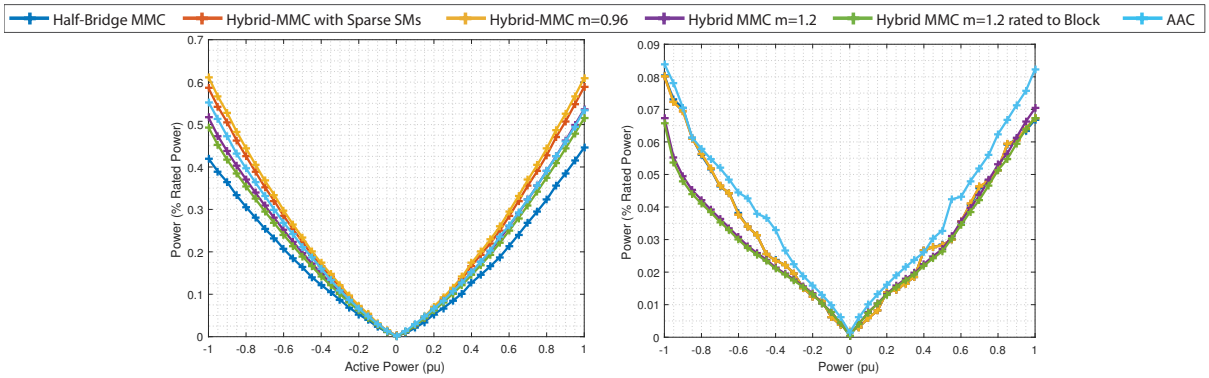
Figure 4.14: Power-loss and junction temperature distribution within the director switch of the AAC.

4.3 Overall Converter Efficiency Comparison and Conclusion

The overall power-losses within the considered converters, with variation in set-point, are given in Fig. 4.15. The Hybrid MMC that is designed to simply block DC faults at a modulation index of 1.2 is the most efficient DC fault tolerant converter considered. The Hybrid MMC at m=1.2 that is designed to operate as a STATCOM, and the AAC are broadly comparable in terms of efficiency, and are both slightly less efficient than the half-bridge MMC. The non over-modulating Hybrid MMC designs are the two least efficient DC fault tolerant topologies

considered.

The switching losses within each topologies are given in Fig. 4.15b. The switching losses in each case are low in comparison to the overall losses within the converter, being dominated by the conduction losses by a factor of approximately 7-10, depending on topology.



(a) Overall semiconductor losses.

(b) Overall switching losses.

Figure 4.15: Overall power-losses within the considered converter topologies.

4.4 Chapter Conclusion

This chapter introduced a thermal model of a heat-sink mounted IGBT, as well as a power-loss model which can be used in conjunction with the thermal model to get estimates of a converters overall power-losses, as well as the junction temperatures reached by the devices within the converter.

These were then used to investigate the expected power-losses within several converter topologies. An overview of the study conducted in this chapter is given Table. 4.6. The half-bridge MMC is the most efficiency topology, however it is weak to DC side faults. The other converters studied were design to be DC fault tolerant, and in some cases, capable of operating as a STATCOM during such condition. The Hybrid MMC and the AAC give broadly comparable efficiencies. The AAC however has a slightly lower required device count, and requires

significantly less sub-modules ($\sim 57\%$) than the Hybrid MMC. The use of sparse full-bridges eliminates the option of designing the Hybrid MMC to over-modulate. This limits the efficiency that can be achieved. In addition the removal of one of the zero-voltage states in the full-bridge sub-modules results in higher junction temperatures and overall losses being reached.

Table 4.6: Overview of converter design, power-loss and thermal characteristics.

	Half-Bridge MMC	AAC	Hybrid MMC	Hybrid MMC w. Sparse FB	Hybrid MMC	Hybrid MMC
Modulation Index (m)	0.96	1.332	0.96	0.96	1.2	1.2
DC Fault Strategy	NA	DCFRT	DCFRT	Block	DCFRT	Block
Total number of sub-modules	589	367	589	589	625	625
Number of IGBTs	1178	1822	1762	1516	1946	1860
Number of Additional Diodes	0	0	0	251	0	0
Max IGBT Junction Temperature (^oC)	104.05	107.27	104.18	107.35	99.02	99.02
Max Diode Junction Temperature (^oC)	115.5	120.01	115.4	120.11	109.24	109.24
Power Loss at Rated Inverting Power	0.4462	0.5527	0.6097	0.5889	0.5365	0.5148
Power Loss at Rated Rectifying Power	0.42	0.5344	0.612	0.5857	0.5167	0.4935

5 Design of Converters to Achieve Overload Capability

This chapter investigates how overload capacity might be included within the converter design specification of MMCs, and what design penalties must be paid in order to achieve this. The first half of the chapter investigates the aspects of the design relating to the required de-rating applied to each sub-module and the overall required number of sub-modules. The second half examines the potential for dynamically rating the converter during overload, so as to not exceed a defined maximum junction temperature limit.

The maximum power ratings currently available for VSC systems are in the region of 1.8 GW in a single sub-sea cable based link and 2.5 GW in an on-shore system [80]. As the technology further matures, even higher power ratings can be anticipated and VSC converters of such high power rating may be expected to provide ancillary services to the AC systems in which they are located [81]. These services could include, for example, fast frequency response in support of the AC system during a frequency disturbance or emergency power re-routing in case of loss of an AC or DC transmission line. The provision of these features implies that the converter must have some level of power capability reserved above its nominal rating.

Overload capability in voltage source converters may enable VSC based HVDC to provide the following system support features:

- Emergency power re-routing during the loss of an AC or DC transmission circuit.
- Frequency support through neighbouring synchronous areas interconnected through HVDC

[82, 83, 84].

- Power oscillation damping using HVDC systems [85, 86].

Overload capability is available for Current Source Converters (CSC) based HVDC systems [87]. For example the Three Gorges-Changzhou and Three Gorges-Guangdon HVDC bipolar links are designed for a nominal rating of 3 GW, with a continuous overload rating of 3.48 GW, and a five second overload rating of 4.5 GW [88]. Such overload capability has not yet been demonstrated or presented as an option by VSC manufacturers.

This chapter will investigate the potential for designing overload capacity into Modular Multilevel Converters, with a focus placed on the half-bridge variant of the MMC, as this is the de-facto standard topology which is in use today. The main limitations in providing overload capacity are first discussed. The potential of using circulating current to get around the limitation imposed by the peak arm current limit is then assessed, and the design penalty incurred in achieving an overload rating investigated. The last section in this chapter then looks at dynamically rating the converter, allowing it to inject a short-term temperature restricted overload for a short period of time. The application of this short-term dynamic overload of HVDC to frequency support provision is then investigated using a power system model that is representative of the GB network.

5.1 Design Factors that Limit Overload

As discussed in Chapter 3, the P/Q capability of MMCs is limited by several factors, and is strongly influenced not only by the current processing capability of the IGBTs within the converter, but also by the energy deviation of the converter and the resulting ripple imposed on the sub-module capacitor voltages.

The limits imposed by the stack voltage capability and the peak sub-module limit are both influenced by the overall energy storage within the converter, as well as the number of sub-modules included within each stack. These limits can therefore be designed around by increasing

the size of the sub-module capacitor, increasing the number of sub-modules, or a combination of both approaches. The limit imposed by the peak turn-off current of the IGBT switches within the converter therefore is the main barrier that must be surmounted, as this will be independent of the number of sub-modules within the converter. The following sections, adapted from [89] and [90], give a description of the operation of IGBTs, followed by some discussion on this may impact the peak current rating of the sub-modules within modular converters.

5.1.1 Current Handling Capability of IGBTs

The Insulated Gate Bipolar Transistor (IGBT), introduced in the 1980s, has become one of the most widely used switches for high power applications. It has widely replaced both the Power MOSFET and Bipolar Junction Transistors. In some ways it can be seen as hybrid of its two predecessors as it combines the high current carrying capability of the BJT with the simple gate driving mechanism of the Power MOSFET. Conceptually an IGBT can be considered as similar to a Darlington arrangement of a MOSFET and a BJT, whereby the MOSFET provides the base current for the BJT [89]. The peak turn-off current of most modern IGBTs is typically twice the nominal rated current of the device i.e. a 1.5 kA device will be specified by the manufacturer to be capable of switching off 3 kA providing the switching lines of the device stay within the SOA, and the junction temperature of the device is not exceeded. The rated current of the device itself is specified based upon the power dissipation capability of the device itself.

5.1.1.1 Operating Principle

The cross section of a single n-channel IGBT cell is shown in Figure 5.1. Such a cross section would between 2-10 μm in width, with a single IGBT chip containing several million such cells [90].

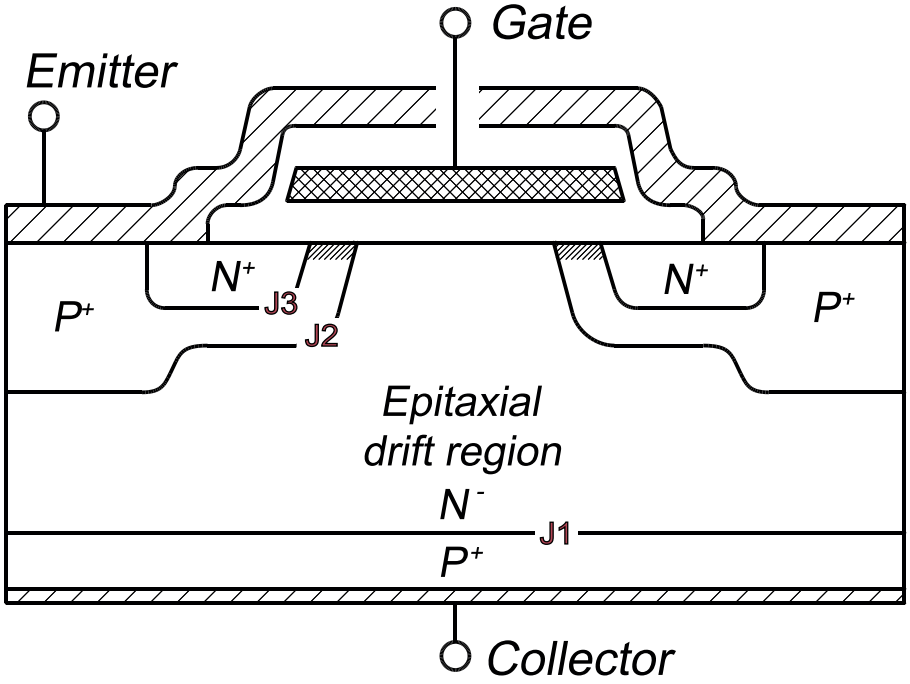


Figure 5.1: Structure of an IGBT [91].

Forward Blocking If the Collector to Emitter voltage, V_{CE}, is positive whilst the voltage from the Gate to Emitter voltage, V_{GE}, is held to zero volts, then junctions J1 and J3 are forward biased and junction J2 is reverse biased, blocking the applied voltage and preventing any current flow through the device.

Turn on and Toward Conduction If V_{GE} is then raised above the required threshold voltage, V_{TH}, an inversion layer in the P base region is formed. This allow electrons to flow from the $n+$region to the $n-$ drift region. In order to maintain space charge neutrality holes are attracted through the now forward biased pn junction at J1. This causes an approximately equal excess amount of minority and majority carriers to gathered in the $n-$drift region, drastically increasing the conductivity of this region. The flow of the minority carriers from the collector and the majority carriers from the emitter results in a net current flow through the device.

When the potential drop across the inversion layer becomes close to the difference between

V_{GE} and V_{TH}, the MOSFET structure exhibits pinch off, limiting the electron flow through the channel. This causes saturation of the collector current .

Turn Off If the device is forward conducting and V_{GE} is lowered back below V_{TH}. The inversion layer between the P base region is removed, halting the flow of electrons from the emitter into the $n-$drift region. This removes most of the base current for the internal pnp structure. However there is still a significant amount of excess charge stored in the $n-$ drift region which can only be removed by recombination. This results in a characteristic tail current in I_{c} as the IGBT resumes forward blocking.

Reverse Blocking If a negative V_{CE} is applied to the device the pn junction J2 is reverse biased and no current can flow. In most VSC topologies this feature is unneeded as it is necessary to parallel the device with an anti-parallel diode as the load will usually contain an inductive element.

Punch Through V. Non Punch Through Devices IGBTs can be sorted into two broad categories, Punch Through (PT) and Non Punch Through (NPT) arrangements. The arrangement shown in Figure 5.1 is a PT device. A PT device contains an additional $n+$ buffer epitaxial layer between the $p+$region at the collector and the $n-$ drift region. In PT devices during Reverse blocking the depletion layer completely depletes the $n-$ drift region and moves into the additional $n+$ region. This is referred to as 'punching through'. The $n+$ region prevents the depletion region from reaching the $p+$ substrate, which would results in breakdown of the device. It is infeasible to grow a $n+$ buffer epitaxial layer that is deep enough to support voltages above 1200V. For this reason for HV applications PT IGBTS are usually used. The addition of the $n+$ buffer also drastically reduces the devices reverse blocking capability, for DC application however this feature is rarely needed.

5.1.1.2 Failure Mechanisms

IGBTs have several failure mechanims, which are described in the following paragraphs.

Latch Up During forward conduction, a portion of the minority carriers injected into the $n-$ drift region flows directly into the $p+$ region at the emitter, through the devices parasitic pnp structure. If this current reaches a large enough level, the voltage drop across the p body layer is enough to the inject electrons into the p base of the internal parasitic npn structure, which in turn leads to an injection of current into the p region of the parasitic pnp structure. This causes a positive loop gain between the two structures, resulting in latch up, where removing V_{GE} no longer controls the current flow through the device [89].

Safe Operating Area The Safe Operating Area (SOA) of an IGBT is defined as the area of simultaneous collector current (I_{c}) and collector-emitter voltage (V_{CE}) that the device can withstand and successfully turn-on and turn-off without failure, such as latch up or thermal breakdown [92]. The SOA can be broken down into the Forward-Bias Safe Operating Area (FBSOA) and the Reverse Bias Safe Operating Area (RBSOA).

The FBSOA defines the collector current and collector-emitter voltages under which the device can safely turn-on and conduct during its on-state without failure. It is important for designing short circuit protection.

The RBSOA defines the boundary of simultaneous collector current and collector-emitter voltage that the device can withstand and successfully turn off. Most modern high power IGBTs have nearly rectangular SOA. The switching trajectory can be shaped to keep it within the SOA by adjusting the gate resistance, usually at a penalty of increased switching losses, or by using snubber circuits across the device to absorb some of the inductive energy from the load being switched. A snubber will come at the cost of increased expense and size, as well as associated losses in some designs. An example switching trajectory is shown in Fig. 5.2. This trajectory is close to exceeding the SOA, which could result in device failure.

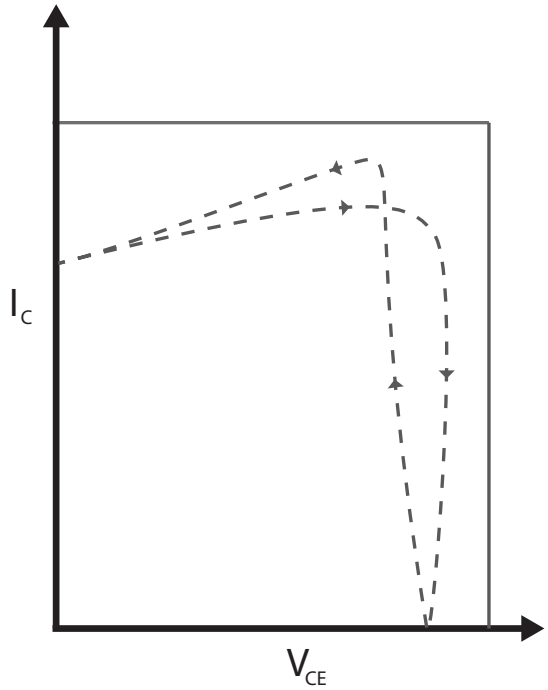


Figure 5.2: Example SOA with switching trajectories for hard switches of inductive load.

Junction Temperature Increasing the junction temperature past the design limits can result in a sudden decrease in the SOA of the device, leading to sudden destruction or latch-up during a switching event. In addition it has an impact on the reliability and lifetime of devices, as discussed in Chapter 4.

Short Circuit Protection Short circuit conditions in power converters can occur due to numerous mechanisms. In the case of a half-bridge sub-module the most likely cause is a failure in the other IGBT within a half-bridge pair. Modern high power IGBTs are rated to survive short circuit conditions, provided the necessary protection is implemented ont he IGBT gate-driver.

As the short-circuit current rises the device will be driven out of saturation and the collector-emitter voltage will rise. This increase in the collector-emitter voltage can be used to detect the short-circuit condition and cause the gate-drive to drive the devices gate low. During short-

circuits the combination of high-current, as well as an increase in collector-emitter voltage results in a large amount of power being dissipated in the device junction. The duration of the short-circuit must therefore be limited to prevent damage to the device. This maximum length of this duration is typically in the region of $10\mu s$ [93].

5.1.2 Converter Current Limits

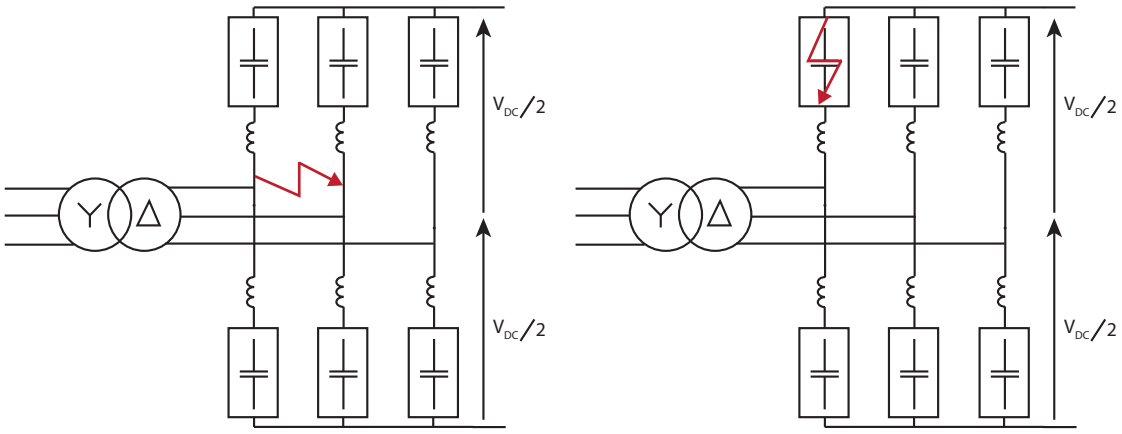
In [94], which is a paper from a semiconductor manufacturer, the authors discuss the testing of a 3.3 kV 1500 A IGBT module which they market for use within MMCs. The authors present successful results from several tests, including turn-off of a load current of four times rated current (6000A), as well as the reverse recovery performance of the IGBTs diode when it is commutated with a load current of 4500 A. Both of these tests were performed with DC bus voltages of 2500 V. Despite the capabilities of such IGBTs, manufacturers have exhibited a large conservatism on choosing the peak current rating of the valves within HVDC, in comparison with the current magnitudes that the devices are capable of switching. Below is a quote from a HVDC manufacturer [29]:

> One further limitation of VSC technology is the current capability of the IGBT. Today, the largest available IGBT has a maximum turn-off current of 4000 A, effectively giving 1800 A DC transmission.

In an MMC operating at a modulation index close to 1, the peak arm current is roughly equivalent to the DC current. The above quote indicates that they apply a de-rating factor of approximately 0.45 to the peak current rating of the arm, in comparison to the peak turn-off capability of the IGBTs within the converter. This is unlikely to be driven by junction temperature considerations as this manufacturer utilises press-pack devices, which are cooled from both sides. The junction temperature of such devices can therefore be expected to be lower than the values given in Chapter 4, which considered converters that use IGBTs with High-Pak cases. The conservatism placed on the peak arm current is therefore likely driven by the need

to deal with fault scenarios which can result in uncontrollable over-current events. The peak current rating of the valve must therefore be chosen so that the worst case peak fault current remains within the turn-off capability of the IGBTs [95].

In [95], which is a paper from GE Grid, DC side faults, internal flash-over causing a line-to-line fault at the converter side of the transformer (as illustrated in Fig. 5.3a), and an internal flash-over across one valve of the converter (as illustrated in Fig. 5.3b) are identified as the most serious fault scenarios which result in uncontrolled over-currents. For the DC pole to pole fault and the line to line fault cases the rate of rise of current is limited by the arm inductors within converter, the converters controller can therefore detect and block such faults in a relatively short amount of time. A simulation results of an internal line-to-line fault in an MMC are shown in Fig. 5.4. The fault causes the converter to loose current control, with the fault current quickly rising. The controller detects the over-current and blocks the converter, which drives the current through the converter back to zero. In order to block the converter the IGBTs must turn-off and commutate the current into the anti-parallel diode paths, requiring them to switch the over-current. The authors of [95] found that the required peak current handling capability to be close to 2 pu. For the internal flash-over fault it was found to be necessary to rely on the IGBT drive units short-circuit protection to extinguish the fault current.



(a) Flash-over causing internal line-to-line fault.

(b) Flash-over across one of the valve stacks.

Figure 5.3: Modular Multilevel Converter internal faults.

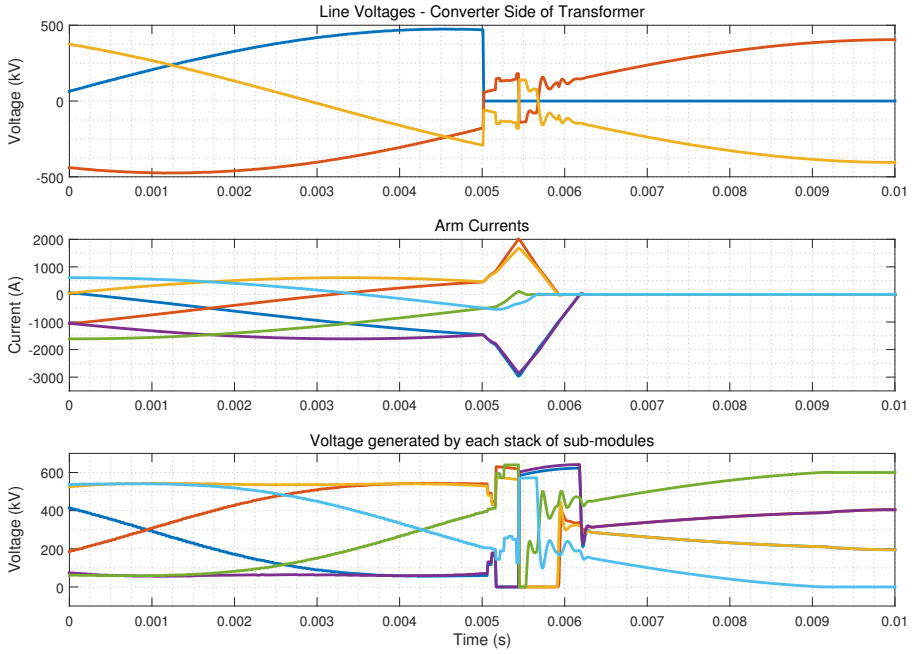


Figure 5.4: Internal line-to-line fault in an MMC - Controller is set to block if an over-current of 2.9 kA is detected.

5.2 Overload Techniques

As discussed in the previous section, increasing the allowable peak arm current within a converter even if only temporarily, may place the converter in danger of damage if a fault was to occur while the converter is operating in the overload region due to a potential increase in the over-current levels that may occur.

One interesting approach which may be used to get around this is the use of circulating currents to suppress the magnitude of the peak arm current for a given set-point. This was proposed in [96], which examined the expansion of the P/Q operating envelope of MMCs through optimisation methods. These circulating currents are common mode between the upper and lower arms of each phase, and form a balanced three phase set between all three phases. This means they do not impact the AC and DC side current waveform. An example of circulating current being used to suppress the peak magnitude of the arm current is given in Fig. 5.5. The use of such circulating currents allows the limitation imposed by the converters arm current limit to be expanded by approximately 30%. In [96], at each operating point the nominal sub-module voltage, circulating current, and zero sequence voltage of the converter was optimised to maximise the overall P/Q capability of the converter. Controlled circulating currents have also been proposed to reduce the energy deviation of the sub-modules during normal operation [97].

When considering the design for overload any optimisation technique that can be applied to the design, should also apply to the design of the converter during normal operation. This section will examine the design of overload in Modular Multilevel Converters under the following assumptions. Circulating current is not utilised during normal operation, for energy deviation reduction or otherwise. The zero sequence voltage injected into the converter voltage waveforms is kept in phase with the fundamental component of the voltage generated by the stacks of sub-modules. The sub-module capacitor voltage is fixed to be controlled to its nominal values at all operating points. The design of converters with overload capacity where optimisation techniques, such as those in [96], are available for use during normal operation could be investigated

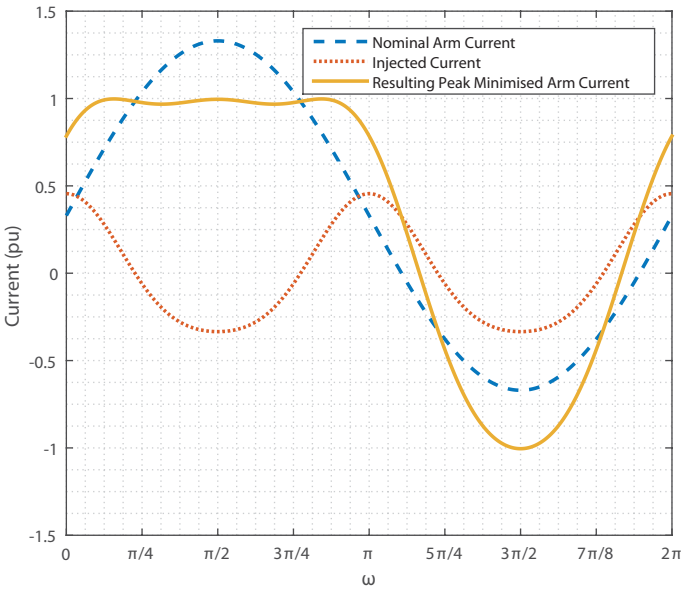


Figure 5.5: Peak arm current suppression using circulating current.

in future work.

5.2.1 Stack voltage, power and energy deviation

In Chapter 3, a method for designing an MMC for a given P/Q specification was presented. This method depended upon analytical derivations of the converters internal voltage, current and energy deviation waveforms. These derivations were made assuming that any circulating current within the converter is well suppressed and controlled to zero. In this subsection a small extension to this derivation is made to take account of the impact of circulating current on the converters internal waveforms.

The arm current within an MMC, with a circulating current component composed of even harmonics, can be written as in (5.1).

$$I_{\mathrm{arm}}(\omega t) = \frac{2}{3}\frac{|S_{\mathrm{c}}|}{mK_{\mathrm{c}}V_{\mathrm{DC}}}sin(\omega t - \phi_{\mathrm{c}}) + \frac{|S_{\mathrm{c}}|cos(\phi_{\mathrm{c}})}{3K_{\mathrm{DC}}V_{\mathrm{DC}}} + \frac{2}{3}\frac{|S_{\mathrm{c}}|}{mK_{\mathrm{c}}V_{\mathrm{DC}}}\sum_{\mathrm{n}=1}^{k} A_{\mathrm{n}}\sin(2n\omega t - 2n\phi_{\mathrm{c}} + \phi_{\mathrm{n}}) \quad (5.1)$$

By superposition, the circuit of an MMC can be split into AC and DC sides [54], as shown in Fig. 5.6. The voltage V_c can be calculated from (3.6). This simplifies the derivation of the stack voltage waveform.

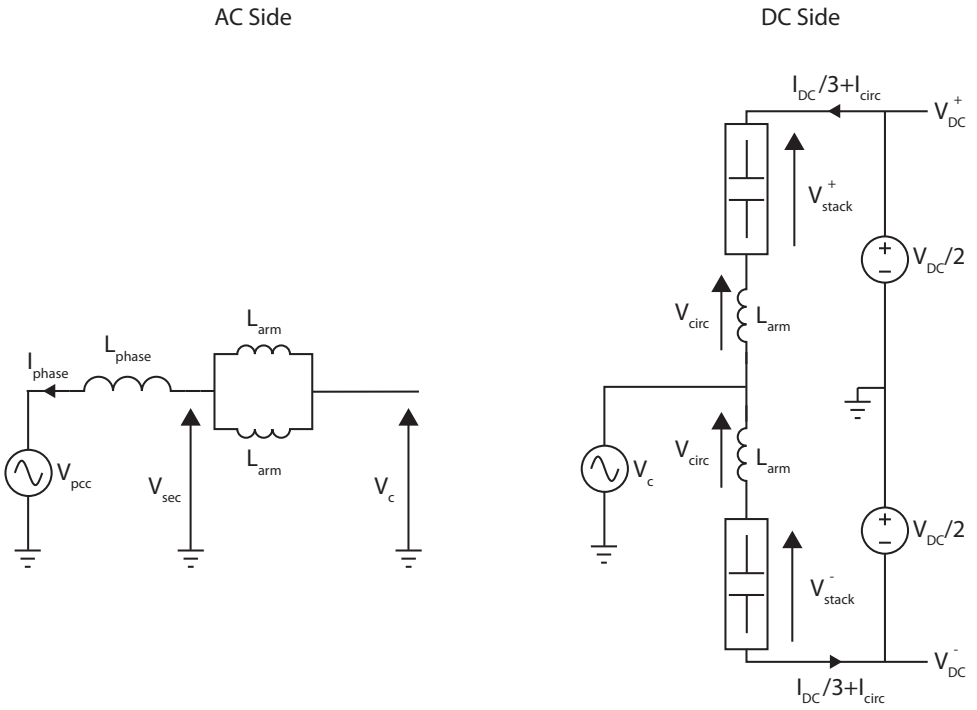


Figure 5.6: MMC Circuit diagram split into AC and DC sides.

The circulating current imposes an additional voltage across the arm inductors of the converter. This additional voltage, V_{circ}, can be written as in (5.2).

$$V_{\mathrm{circ}} = L_{\mathrm{arm}}\frac{2}{3}\frac{|S_{\mathrm{c}}|}{mK_{\mathrm{c}}V_{\mathrm{DC}}}\sum_{\mathrm{n}=1}^{k} 2n\omega A_{\mathrm{n}}\cos(2n\omega t - 2n\phi_{\mathrm{c}} + \phi_{\mathrm{n}}) \quad (5.2)$$

The voltage generated by the stack of sub-modules can then be given by (5.3).

$$V_{\text{stack}} = \frac{V_{\text{DC}}}{2} - V_{\text{circ}} - V_{\text{c}} \tag{5.3}$$

The resulting full expressions for the arm current and stack voltage, given in (5.1) and (5.3), could then be multiplied together and then integrated to give an expression for the overall energy deviation of the stack of sub-modules. However this leads to a very long derivation, with twelve terms in the expanded expression for the stack power. To avoid this, the stack power and energy deviation are determined by numerically multiplying the expressions for the arm current and the stack voltage together to find the power of the stack, and then numerically integrated to get the energy deviation and then integrating. The final energy deviation of the stack is then by calculated by subtracting any DC component from the result. The design of an MMC to a given specification can then be performed using the methodology given in Chapter 3.

5.2.2 Circulating current for active power extension during normal operation

The use of second harmonic alone allows up to ∼25% additional apparent power to be processed by the converter [96]. By including some fourth harmonic in the circulating current it was found to be possible to push this limit to ∼30%. The ratio of fourth to second harmonic and the relative magnitude of the circulating current to the AC component of the arm current was numerically optimised to give the waveform with three maxima shown in Fig. 5.5. This numerical optimisation can decrease the peak magnitude of the arm current by a factor of ∼ 0.3345 the AC component of the arm current. The expression for the circulating current in phase A of the converter is given in (5.4).

$$I_{circ}(\omega t) = k\frac{2}{3}\frac{|S_c|}{mK_cV_{DC}}\big(0.3947\sin(2\omega t - 2\phi_c + \frac{\pi}{2}) + 0.06034sin(4\omega t - 4\phi + \frac{\pi}{2})\big) \tag{5.4}$$

The relative magnitude of the injected circulating current, k, is calculated from (5.5), where $I_{arm_{AC}}$ and $I_{arm_{DC}}$ are the AC and DC components of the arm current reference and ACL is the arm current limit. The value of k is bound between -1 and 1. This calculation injects just enough circulating current to keep the peak arm current at the specified arm current limit.

$$k = \begin{cases} 0 & \text{if } I_{arm_{AC}} + \left|I_{arm_{DC}}\right| \leq ACL \\ \left(0 \leq \frac{I_{arm_{AC}} + \left|I_{arm_{DC}}\right| - ACL}{0.3345 I_{arm_{AC}}} \leq 1\right) \times \text{sign}(I_{arm_{DC}}) & \text{otherwise} \end{cases} \tag{5.5}$$

A simulation of a converter ramping into the overload region, utilising circulating current to keep the peak current to below the specified arm current limit is given in Fig. 5.7. The arm current limit in this case was set to be equal to the peak current at 1 pu active power. When the converter starts to ramp to 1.3 pu, at t=0.1 s, circulating current is injected into the arm current reference for the converters controller, maintaining the peak arm current to the same level as at 1 pu.

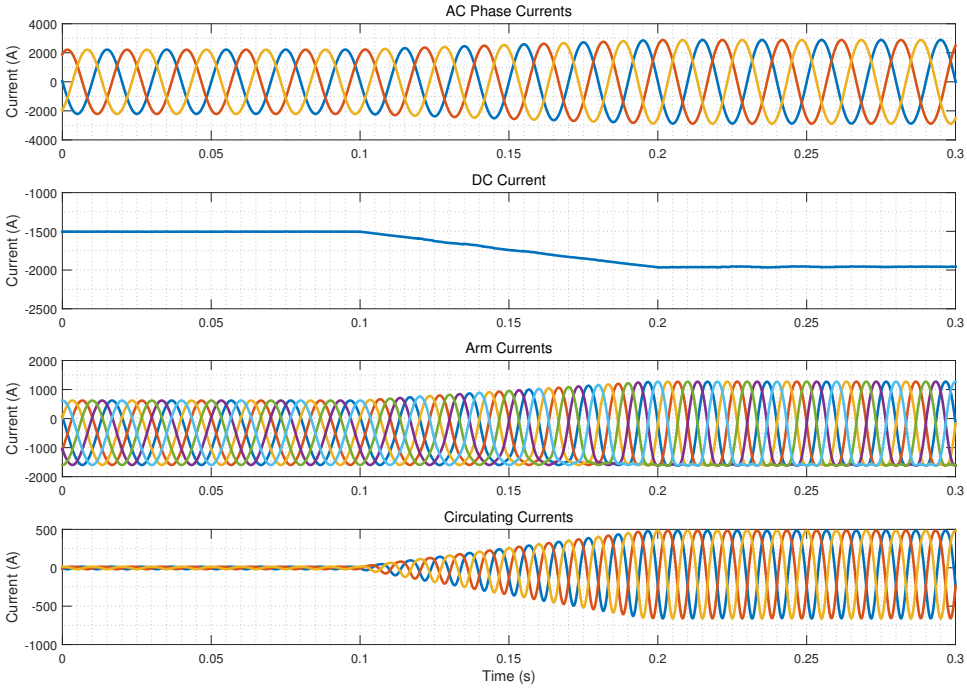


Figure 5.7: Power ramp in an MMC from 1 pu to 1.3 pu active power - circulating current used to maintain the peak arm current to the pre-ramp value.

5.3 Design of Overload Capacity

In this section the design of overload capacity into Modular Multilevel Converters will be considering two scenarios. In first scenario it will be assumed that the IGBTs used within the converter are capable of switching the peak overload currents, without placing the converter in risk of failure in the event of a fault scenario. The P/Q capability of the converter is therefore limited by the other operational limits imposed on the converter. The other scenario will assume that circulating current must be used to expand the P/Q capability of the converter past its normal operating limitations.

Figure. 5.8 shows the impact that the peak suppressing circulating current has on the converters internal energy deviations and voltage waveforms. The grey lines in each sub-plot show the boundary where circulating current is used to suppress the peak arm current. The circulating current can be seen to have a clear impact on the magnitude of the peak and minimum

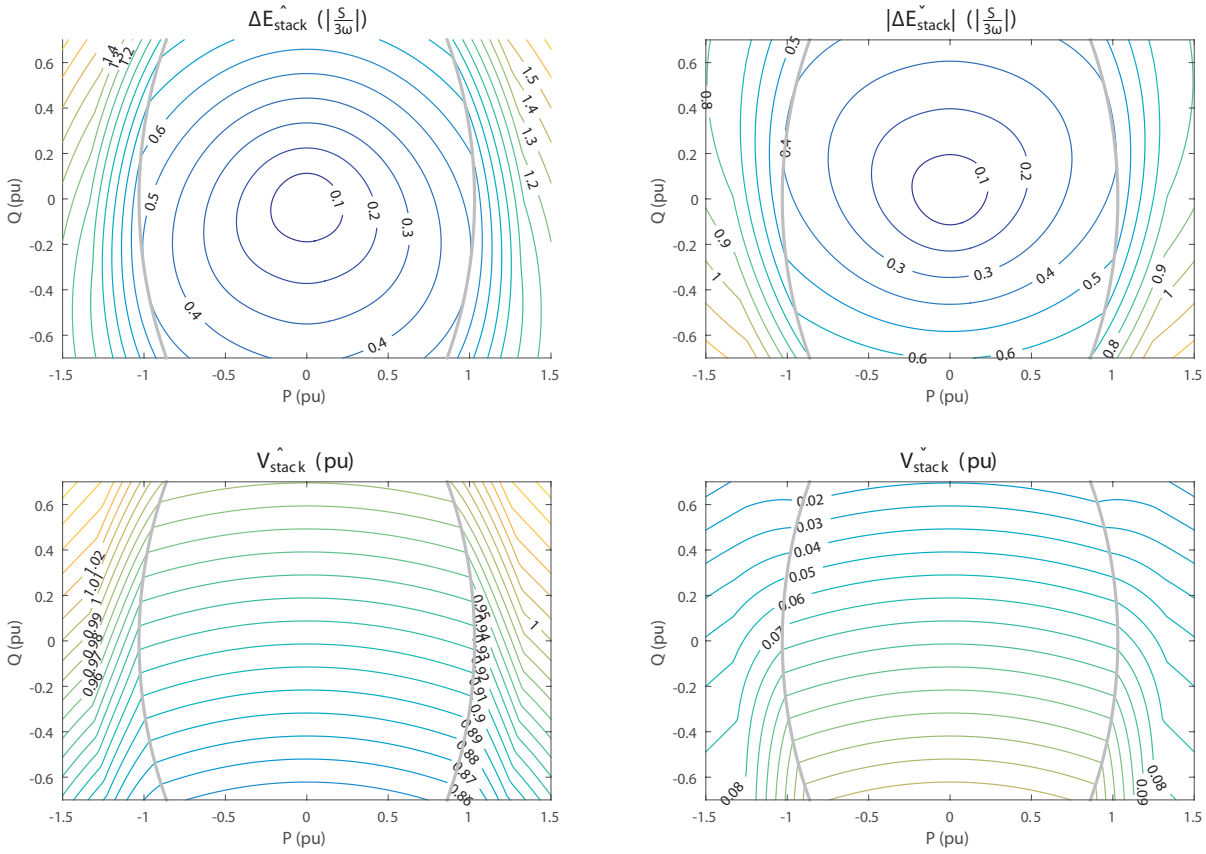


Figure 5.8: Impact of peak current suppressing circulating current on an MMCs internal energy deviation and voltage waveforms - grey line shows point at which circulating current is injected.

energy deviation of the converter. This increase in energy deviation will translate into a design penalty in terms of the de-rating that is applied to each sub-module in order to limit the peak sub-module voltage reached, as well as the required overall number of sub-modules within each stack.

The base case scenario that will be considered in this section is the MMC design with a 9 mF sub-module capacitor, designed using the methodology given in Chapter 3. The specifications of this base case converter are given in Table. 5.1.

A comparison of the required number of sub-modules, the required amount of de-rating applied to the nominal sub-module voltage and the overall required voltage rating of stack, for

Table 5.1: Overload base case modular multilevel converter specification.

Characteristic	Value
Rated Power	1575 MW
DC Voltage	±525 kV
AC Voltage Variation	±5%
Transformer Leakage Reactance	0.14 pu
Arm Inductor Size	0.2 pu
Peak Rated Sub-Module Voltage	2000 V
Over-Modulation Safety Factor	0.05
Energy Safety Margin	3 kJ/MVA
Sub-module capacitor size	9 mF
Number of sub-modules per stack	591
Nominal sub-module voltage	1831
Nominal stored energy	33.92 kJ/MVA

both cases, is given in Fig. 5.9. The requirement to use circulating current can be seen to have a much steeper design penalty as the rated overload capacity is increased, in comparison to the case where an oversized semi-conductor is used. To achieve a 30% overload rating requires an approximate 10% increase in the number of required sub-modules if circulating current must be used, while only a 3% increase is required if an over-sized semiconductor is used.

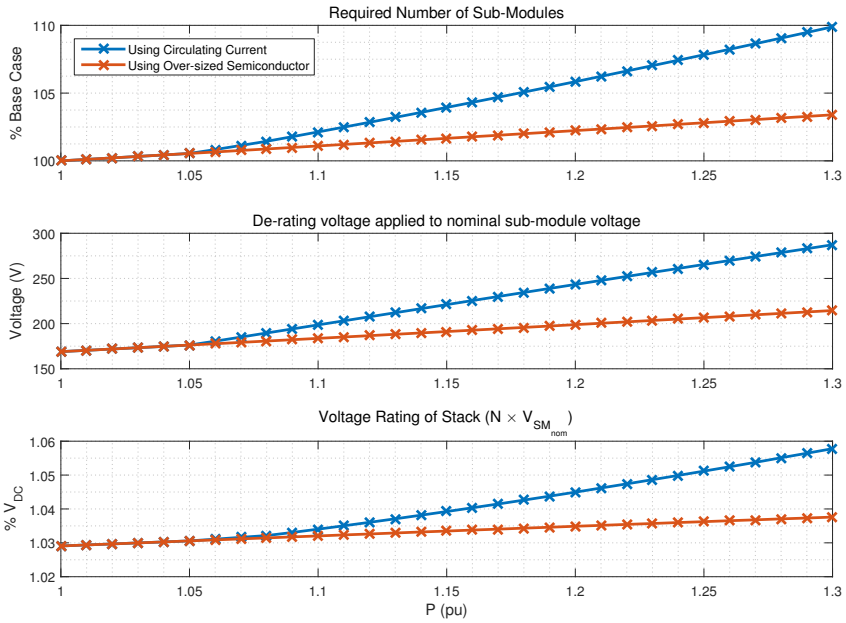
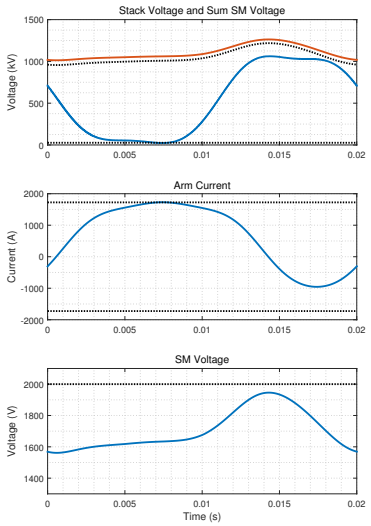


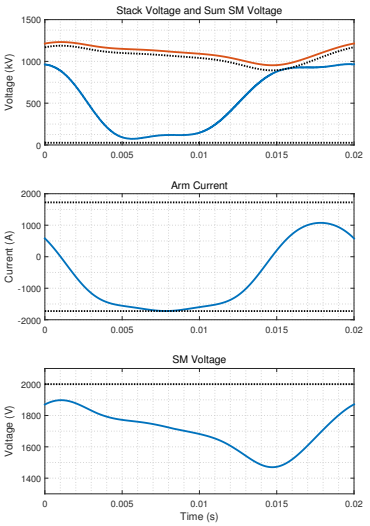
Figure 5.9: Design comparison for achieving overload capability.

5.3.1 Design Verification

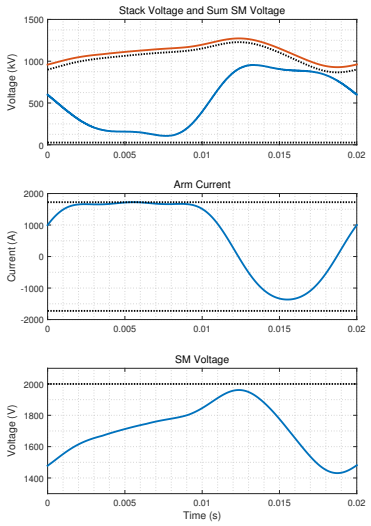
The accuracy of the design MMC methodology has already been verified in Section. 3.3.5.1 for the case of the MMC operating without circulating current. For this reason only the MMC design utilising circulating current is verified. Four of the outer points on the P/Q envelope were tested using a simulation model of the converter rated for an overload rating of 30%. The results of this are shown in Fig. 5.10. The converter operates against it design limit, as expected, at the tested operating points.



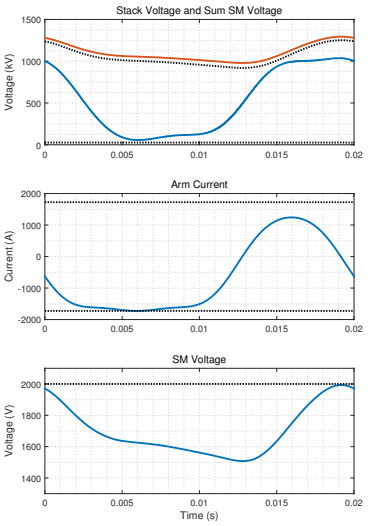
(a) P: 1.3 pu Q: 0.3 pu
AC voltage: 105% nominal
Converter limited by over-modulation limit.



(b) P: -1.3 pu Q: -0.5 pu
AC voltage: 105% nominal
Converter limited by stack voltage limit.



(c) P: 1.3 pu Q: -0.5 pu
AC voltage: 95% nominal
Converter limited by arm current limit.



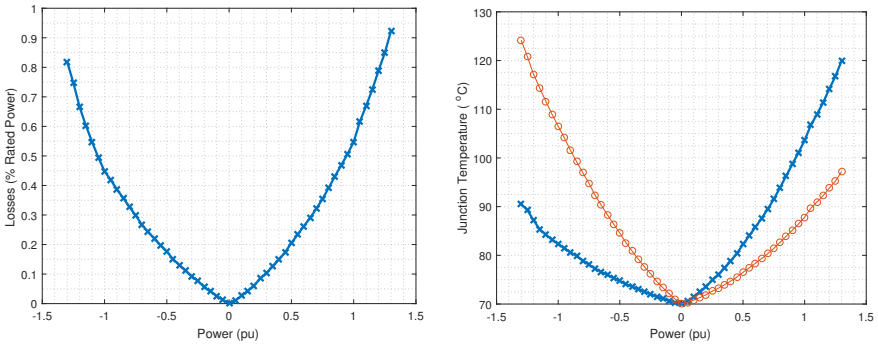
(d) P: 1.3 pu Q: 0.3 pu
AC voltage: 95% nominal
Converter limited by peak submodule voltage limit .

Figure 5.10: Simulation verification of P/Q Capability of converter rated for 30% overload achieved using circulating current

5.4 Dynamic Thermal Rating Of Converters during Overload Conditions

The previous sections of this chapter investigated potential methods of designing overload capacity into Modular Multilevel Converters. This study highlighted that overloads in the region of 30% could be achieved, while respecting the voltage limits of the converter, the peak sub-module voltage limit and the arm current limit. This was achieved with a design penalty of approximately 10% additional sub-modules required within the converter.

Fig. 5.11 shows the estimated power-losses and junction temperatures within a Modular multilevel converter that uses circulating current to achieve an overload rating of approximately 30%. The overall increase in power-losses moving from 1 pu to 1.3 pu is approximately 80% in inverting mode and 68% in rectifying mode. The maximum junction temperatures reached at 1.3 pu, assuming a 70^oC ambient coolant temperature is 124^oC during rectifying mode and 120. These junction temperatures are and are close to the 125^oC operating limit of most high power IGBTs. Section. 5.4 will explore the idea of dynamically rating the converter, based upon the estimated instantaneous maximum junction temperatures within the converter, so as to limit the junction temperatures reached to significantly below these levels.



(a) Overall power losses. (b) Junction temperatures.

Figure 5.11: Power-losses and junction temperature in an MMC with circulating current used to achieve overload.

Figure. 5.11 illustrates that even if the other factors that limit the converters P/Q capability can be designed around, the junction temperatures that the devices reach in the overload region may become the dominant factor that limits the converters overload capability. This section will consider the dynamic thermal rating of a modular multilevel converter, exploiting the slower thermal dynamics of the IGBT module and heat-sink, so that the full overload capability of the converter can be utilised for a short period of time, before the converters set-point is dropped back down so as the limit the maximum temperature reached by the IGBTs to a level significantly below the steady-state junction temperature. In Chapter 4 a transient thermal model of a heat-sink mounted IGBT was developed. This is model is used in conjunction with the power-loss block also introduced in Chapter 4 to investigate this idea.

The following section in this chapter contains some power system simulation results, investigating the application of temperature-restricted dynamic overload to frequency support provision in a power system simulation that is representative of the GB network. This work was done collaboratively with Claudia E. Spallarossa and Inma Martinez Sans.

5.4.1 Dynamic Temperature Restricted Overload

Figure 5.12 shows the layers of the cooling path in an IGBT module from the silicon die to the ambient cooling liquid, as well as simulation results showing the difference in temperatures between the internal layers of the IGBT in response to a stepped change in heat dissipated at the IGBT dies. The upper layers of the IGBT module, such as the silicon die, copper substrate and ceramic insulation can be seen to heat up very quickly. The lower layers in the cooling path, such as the baseplate and the heat-sink heat up at much lower rates, as well as contributing a large part of the overall thermal impedance from the silicon die to the ambient cooling liquid. When considering dynamic thermal rating it is the response of these slower elements that will be exploited.

A simulation of the IGBT junction temperatures of an MMC doing a stepped reference change from 1 pu to 1.3 pu is shown in Fig. 5.13. During the initial portion of the transient (from 20-30

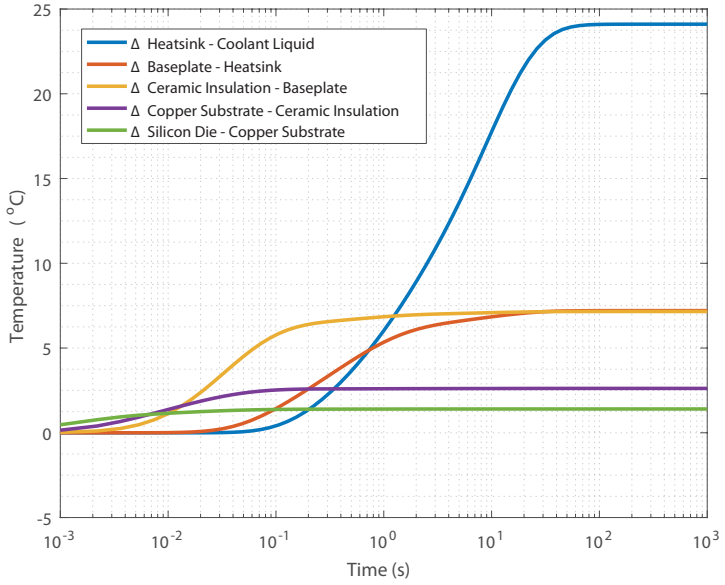


Figure 5.12: Difference in layer temperatures in IGBT module in response to a stepped 1 kW of heat at the IGBT dies.

s) the junction temperature rises quite rapidly. This corresponds to the silicon dies, copper and ceramic substrates heating. The following response is from the slower thermal dynamics of the baseplate and the heat-sink itself heating up. The 90% rise time of the system is $\sim$ 15.4 seconds, while the 75% rise time is $\sim$ 15.4 seconds, the 50% rise time is $\sim$ 15.4 seconds and the 25% rise time is $\sim$ 0.35 seconds.

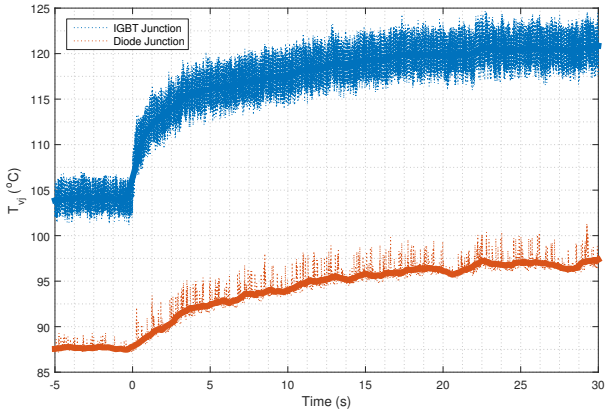


Figure 5.13: Junction temperature sin the lower IGBT of a half-bridge MMC during a stepped reference change from 1 pu to 1.3 pu - circulating current used to achieve overload.

To exploit this short term thermal response a dynamic overload controller was developed, which actively limits the allowable power based on the estimated junction temperatures within the converter, allowing the peak junction temperature to be restricted to a specified limit. The overview of the control scheme is given in Fig. 5.14. The power loss estimate block outputs an estimate of the losses within the converter. These losses are then applied to the transient thermal model of a heat-sink mounted IGBT. The maximum estimated junction temperature from the thermal model is then compared to the specified junction temperature limit, $T_{vj_{Limit}}$, to generate an error signal which is passed as an input to an integral controller. The output of this integral controller is set to saturate between the rated power of the converter, S_{rated}, and the maximum allowable overload power, S_{max}. This prevent the overload controller from interfering with the converter during normal operation. The output of this integral controller then limits the magnitude of the power reference, S_{ref}, that is sent to the converter.

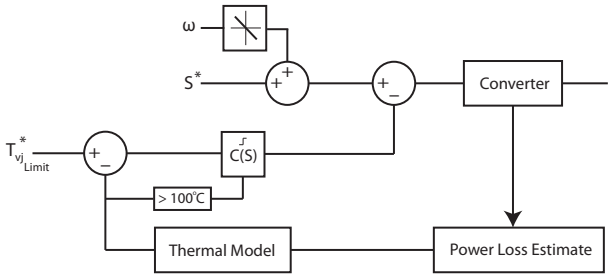


Figure 5.14: Dynamic overload controller

An example of this controller operating is given in Fig. 5.15. In the simulation results shown an MMC was attached to a voltage source representing an AC grid. This voltage source was used to synthesise an AC frequency event. A frequency-droop controller was added to the converter's controller power reference generator, causing it to increase its power output in proportion to the frequency deviation of the voltage source. The dashed lines represent the overall power reference sent to the converter, corresponding to S^* in Fig. 5.14. The solid line shows the measured power output of the converter, which is set to a maximum allowable value of 1.3 pu. When the junction temperature exceeds the specified limit of 110^oC the overload controller restricts converters power output back down, keeping the maximum junction temperature at the specified limit.

An example of the dynamic overload rating which may be achieved is given in Fig. 5.16. The plot show the power curves that the converter can follow and still keep the peak junction temperature of the device below the specified limit. The dotted line shows the interpolated point where the converter's power would have to be ramped back down to prevent over-heating of the devices. This plot was generated using and the overload controller described above. With the 10 ^oC of thermal overhead the converter has a steady-state overload rating of 1.14 pu. Short-term overloads of up to 1.3 pu are allowable for up to 2 seconds before the overload controller constrains the converter's active power set-point back down.

A worst case of operating a 1 pu active power prior to overloaded operation was assumed for the given curves, this means the converter has the minimum amount of available thermal

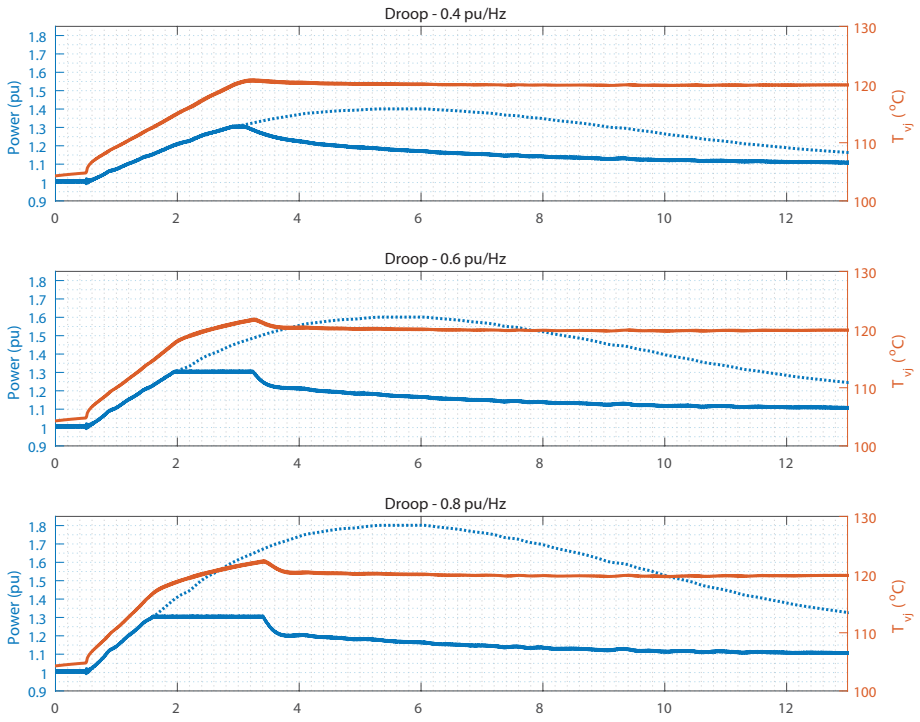


Figure 5.15: Dynamic overload example. Dashed blue line shows power reference, solid blue line shows achieved power set-point.

overhead before moving into the overload region. The rating will be different depending on whether the converter is operating as an inverter or rectifier because of the thermal imbalance between the diode and IGBT junction temperatures within the module. In a point-to-point link the worst case will be the limiting factor, however in multi-terminal networks this may not be the case.

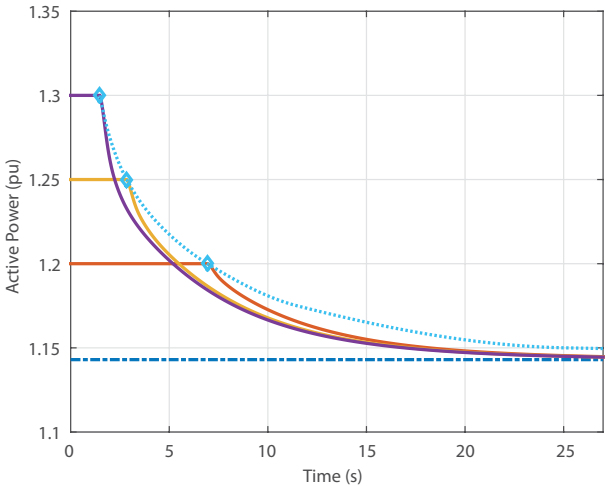


Figure 5.16: Transient overload rating curve assuming 10^oC of exploitable thermal overhead.

Other elements in the HVDC system, such as the cable system and converter transformers, may also impose thermal limits on the amount of time the overload capability is available. Overloading of transmission scale transformers is a well understood and utilised in practice in many power-systems [98, 99]. The temperature dynamics of transformers under overload conditions occur over long time-scales, for example in [100], an approximate 30% overload was found to be acceptable for a 1 hour period. Dynamic rating of overhead lines and cables has also been investigated (albeit for AC systems) and found to have similar time constants [101, 102]. The short-term response of an HVDC system, is therefore expected to be dominated exclusively by the limitations imposed by the converter itself, with the other elements within the overall system limiting the power transfer capability at longer time-scales.

5.4.2 Application to Primary Frequency Frequency Response in a Multi-Bus System

This work was carried out collaboratively with Dr. Claudia E. Spallarossa and Dr. Inmaculada Martinez-Sans

This section presents the results of an investigation into the application of the overload con-

troller scheme detailed to providing frequency support in a using a three-machine GB equivalent test system implemented in DIgSILENT PowerFactory.

The specification of the converter used in this study is given in Table. 5.2. The arm inductance and leakage inductance values are larger than has been previously used in this thesis due to how the author of the the MMC model implemented it in DIgSILENT [103].

Table 5.2: HVDC SYSTEM DATA

V_{dc}	Converter rated DC voltage	±525 kV
$V_{ac}(L-LRMS)$	Converter rated AC voltage	643 kV
P_{rated}	Converter rated power	2.55 GW
L^{up}, L^{low}	Arm inductances	140 mH (0.27 pu)
X_{tf}	Transformer leakage + line reactance	20.75 %
l	DC line length	300 km
I_{rated}	DC line rated current	2.4 kA
R'	DC line resistance	0.0113 Ω/km
L'	DC line inductance	0.362 mH/km
C'	DC line capacitance	0.212 μF/km

The IGBT used for this converter was a 1.2 kA 5SNA 1200E3300. This IGBT was chosen due to the desire to have converters in the region of 2.55 GW, 30% larger than the 1.8 GW loss of infeed limit that currently exists for the GB system. Each converter station in this chapter is considered to be formed of two parallel converters of a rating of 1.25 GW. This IGBT module uses the same package as the 5SNA 1500E3305 IGBT considered in other chapters of this thesis. To achieve the power ratings of 2.55 GW, each each converter station is considered to be comprised of a parallel arrangement of two of the converters. The power-losses from a detailed switching model of this MMC were characterised in Simulink and then exported as a table for use in a DIgSILENT Reduced Dynamic Model of an MMC, which is integrated into a Great British power network representative model.

5.4.2.1 AC system description

The system used in simulations was based off the test system presented in [104]. The three areas represent Southern Scotland, Northern Scotland and England/Wales. Two HVDC links each rated to 2.55 GW operating at $\pm 525kV$ are connected to this system, representing a connection to either mainland Europe, or to a future multi-terminal offshore network.

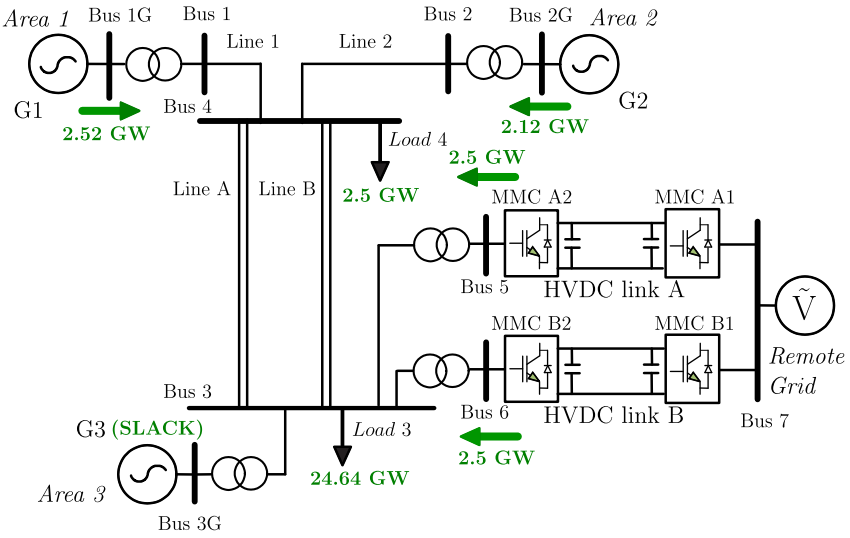


Figure 5.17: Three-area GB test system with two MMC-based HVDC connections (HVDC link A and HVDC link B) to mainland Europe - Credit: C.E Spallarossa and I.S Martinez

The operating condition chosen for the simulations was based upon the one described in [104], and assumes a low demand scenario with 22.5 GW of synchronous generation, and 5.1 GW of additional infeed being provided by the HVDC links. The overall inertia constant of the system is 3.39 s. The system is operated with 2.5 GW of spinning reserve to secure against the loss of one of the two HVDC interconnectors. The Security and Quality of Supply Standard (SQSS) for the GB network requires that frequency does not vary outside a ± 0.5 Hz range for more than 60 seconds and imposes a limit on the maximum frequency deviation of 0.8 Hz for large infrequent infeed losses [105].

Two different fault response controls are considered in the system study. The first is a

frequency proportional droop controller. The second is a maximum release controller, which commands the converter to inject as much power as possible if the frequency is detected to pass below a safety threshold.

5.4.2.2 Simulation Results

Fig. 5.18 shows the response of the system to the loss of one of the HVDC links. Three cases are considered, the first is a base case scenario, where the remaining HVDC link cannot provide any frequency support. The other two cases are results with frequency-droop controller and the maximum release controller. The amount of thermal margin that can exploited by the remaining HVDC link was set to 10 ^oC above the max steady-state junction temperature. Prior to the fault each HVDC link is injected rated power into the GB grid. The loss of one of the links therefore results in a loss of infeed of 2.55 GW.

In the case with no frequency support the frequency drops below the security limit of 49.2 Hz, reaching a nadir of 49.06 Hz, despite the 2.5 GW of spinning reserves in the system. The system response shows significant improvement with the introduction of the dynamic overload scheme. The nadir frequency reached with the maximum release controller is 49.54 Hz, and 49.43 Hz when the frequency-droop controller is used. The steady-state frequency is all three cases is similar, recovering to approximately 49.7 Hz.

For the maximum release case the converter is able to inject its maximum overload power for approximately two seconds following the detection of the frequency event, before the overload controller constrains the converters power output back down to limit the maximum junction temperature reached. The nadir frequency reached in this case is 49.54 Hz, significantly improved on the 49.06 Hz reached when no overload is available.

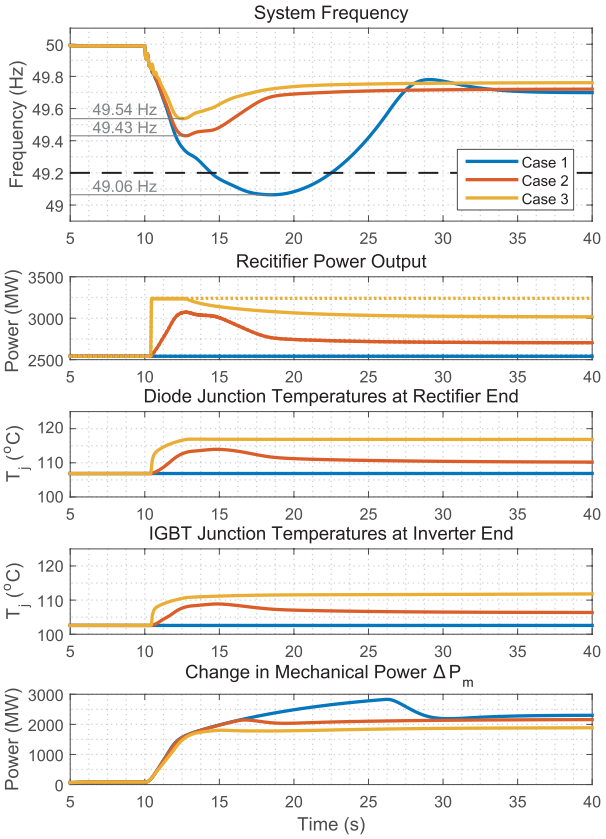
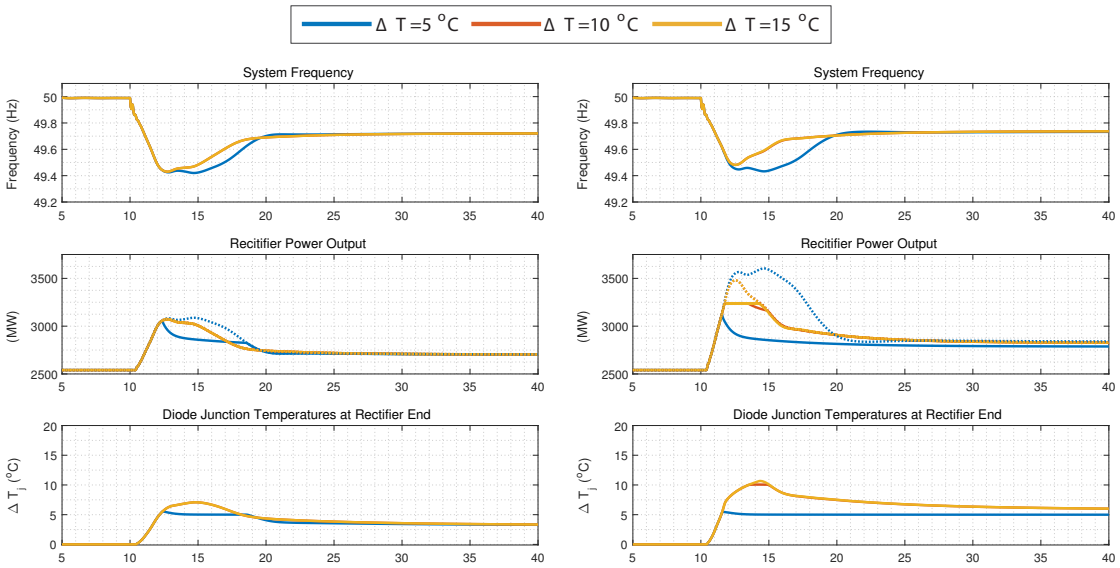


Figure 5.18: System response to HVDC link B outage: 1) no frequency response from HVDC (blue traces); 2) frequency response from HVDC with a frequency-power droop controller (red traces); 3) frequency response from HVDC with a maximum power release controller (orange traces)

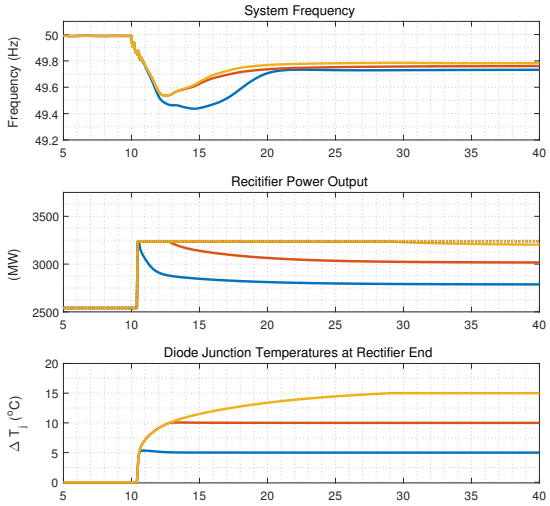
Sensitivity to available thermal overhead The test scenario was repeated, however this time the amount of exploitable thermal overhead was varied, from 5^oC, representing a case with very little exploitable thermal overhead, to 15^oC. The results of these simulations are given in Fig. 5.19. Interestingly the system response is still significantly improved even in the case with a thermal overhead of only 5^oC. The higher droop gain value and the maximum release controller show similar responses in this scenario. The converter quickly responds to the frequency event, injecting its maximum possible overload power. This is then constrained downwards by the overload controller. The nadir frequency reached for all cases is above 49.4 Hz. The highest

frequency nadir is observed for the maximum release power controller with thermal overhead of 10^oC and above. In general there is little difference observed between cases where there is 10^oC and 15^oC of thermal overhead available. A slight difference is observed in the new post-fault steady-state frequency reached by the system due to the higher steady-state overload capability available.



(a) Frequency-power droop controller with gain K.

(b) Frequency-power droop controller with gain $2K$.



(c) Maximum power release controller.

Figure 5.19: Comparison of HVDC frequency support controllers for different $\Delta T_j = T_{max} - T_j$ values.

5.5 Chapter Conclusion

This chapter investigated how overload capacity could be built into Modular Multilevel Converters, in order to enable system support services such as frequency response. The peak arm current limit, enforced due to the need to have due to over-current events caused by fault situations, was identified as the main barrier to achieving an overload rating. The potential of using circulating currents to get around this issue was investigated. Results indicate that a 30% overload could be achievable with a design penalty of approximately 10% additional sub-modules required in the converter design.

The junction temperatures reached by the IGBTs within the converter may be another factor that limits the converters overload capability. This chapter introduced the idea of dynamically rating a converter operating in the overload region so as to limit the maximum junction temperature reached in the converters IGBTs to below a specified operating limit. This operating limit may be significantly below the steady-state junction temperatures that would be reached if the converter operated continuously in the overload region.

An overload controller has been developed which dynamically sets a limit on the converters active power capability. This overload controller was then implemented in an MMC reduced dynamic model and integrated into a test system which is representative of the GB network. The usefulness of this scheme to providing primary frequency support to the network in the event of a loss of infeed event was then investigated. Results indicate that the scheme makes significant improvement to the overall response of the system, even in cases where the exploitable overhead in terms of temperature is very low.

6 Power-Groups: Design and Operation

This thesis chapter details the work undertaken in developing a modular structure, composed of a stack of sub-modules in parallel with a thyristor valve, with the aim of achieving Voltage Source Converters with near-CSC efficiency levels, whilst retaining the controllability advantages of VSC technology.

Most of the work presented in this chapter, and the following chapters, was carried out whilst undertaking a consultancy study for GE Grid Solutions (formerly Alstom Grid). I would like to thank Kevin Dyke, the late Colin Oates, Dave Trainer, Francisco Moreno and Konstanstin Vershinin for the opportunity to work on this topic, as well as providing helpful feedback during numerous meetings.

This chapter is structured as follows; the first section gives an introduction to the power-group concept. The second section gives some background detail on thyristors and their operation, as well as detailing their limitations. The following section details the operational considerations in achieving a practical power-group design, including the control of the thyristor turn-on and turn-off, as well as a snubber design for the thyristor valve.

6.1 Introduction

The introduction of the Modular Multilevel Converter can be considered a major step change in both the efficiency and the controllability of voltage source converters, and the beginning of a new generation of circuit arrangements. The topology allowed a vast reduction in the required switching frequency of the semiconductor devices, resulting in a converter where the

semi-conductor losses are nearly completely dominated by the conduction losses. Despite this, the efficiency levels achievable with MMC converters are not on par with the efficiency levels that can be achieved using thyristor-based Current Source Converters (CSC). This is down primarily to the difference in the characteristics of the devices used in VSC and CSC converters.

A comparison of the forward voltage drop in a 8 kV thyristor from IXYS Westcode, and a 3.3 kV IGBT from Infineon is shown in Fig. 6.1. The forward voltage drops of the devices have been normalised by the devices' peak rated blocking voltage to give an indication of the conduction losses that may be expected for a given power processing capability. The relative drop across the thyristor device is approximately one quarter that of the IGBT.

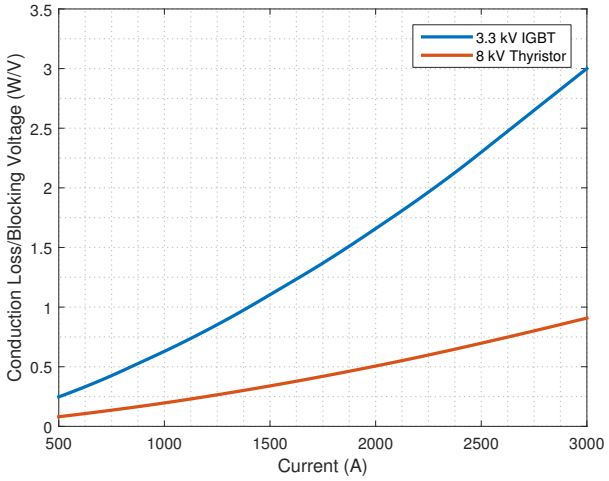
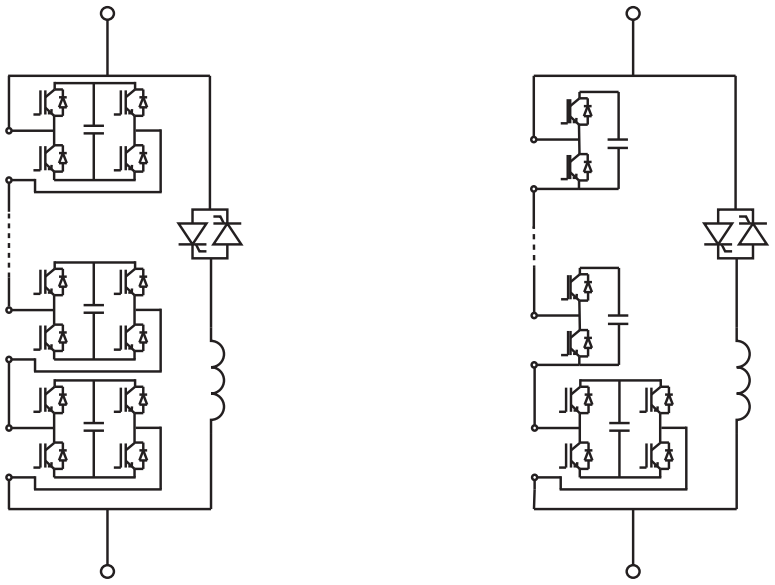


Figure 6.1: Normalised conduction loss against current for a 3.3 kV IGBT and an 8kV Thyristor.

Efficiency improvements in wholly IGBT based converters can only reasonably be expected to come about due to improvements in IGBT technology. Another generational leap in efficiency may be expected if Silicon Carbide semiconductors with adequate voltage and current ratings for HVDC applications become commercially available.

6.2 Power-Group Concept

Power-groups (PG) are proposed here as a modular structure, comprising of a series stack of sub-modules in one branch,with a parallel branch containing anti-parallel thyristor valves in series with a commutating inductance. The stack of SMs is capable of generating a voltage output, while the thyristor branch acts as a low impedance bypass path which can be used when the stack of SMs within the power-group is not required to generate a voltage. When the stack of sub-modules is required to generate a voltage again the thyristor can be commutated off by applying a reverse voltage generated by the stack of sub-modules. In this manner the thyristor can be made to act as a fully controllable switch. Two potential power-group structures are shown in Fig. 6.2. For the case of the half-bridge power-group structure, at least one full-bridge sub-module capable of generating a negative voltage would have to be included in each power-group to allow the thyristor current to be commutated, as will be described in Section. 6.4.1.



(a) Full-bridge stack.

(b) Hybrid stack with half-bridges and a single full-bridge.

Figure 6.2: Power-group structures.

Power-groups could be used as the building blocks for implementing any converter based upon a modular multilevel design. This is illustrated for the case of a power-group augmented MMC in Fig. 6.3.

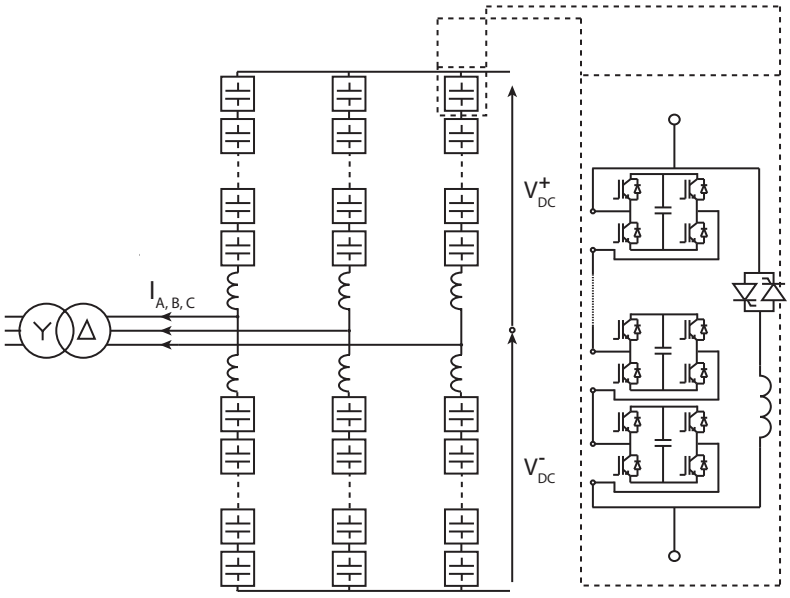


Figure 6.3: Modular Multilevel Converter augmented with stacks formed out of series connected power-groups.

The thyristor valve within each power-group can be utilised when the sub-modules within the power-group are required to generate zero volts. Opportunities to do this can be created by dividing the overall voltage to be generated between power-groups so that they are mostly assigned to either generate their full available output voltage (i.e. insert all sub-modules within the power-group) or generate zero volts. One power-group within the arm will generate an intermediate voltage, so as to allow fine current control. This is illustrated in Fig. 6.4 for the case of an MMC which has been augmented with five power-group structures per converter arm. The top sub-plot shows how the stack voltage is divided between the five power-groups within the arm. The middle sub-plot shows the voltage generated by the sub-modules within the first power-group within the arm. It can be seen that the power-group mostly generates

either zero volts, or its full available voltage. For a small part of the cycle it generates an intermediate voltage. The lowest sub-plot shows the path that the arm current takes through the first power-group. When the power-group is generating a voltage the arm current flows through the sub-modules and the thyristor valves are in a blocking state. When the power-group is set to generate zero volts the thyristor valve is fired, and the current commutated from the SM path within the power-group into the thyristor valve. When the power-group is required to generate a voltage again the current is commutated from the thyristor valve back into the sub-modules.

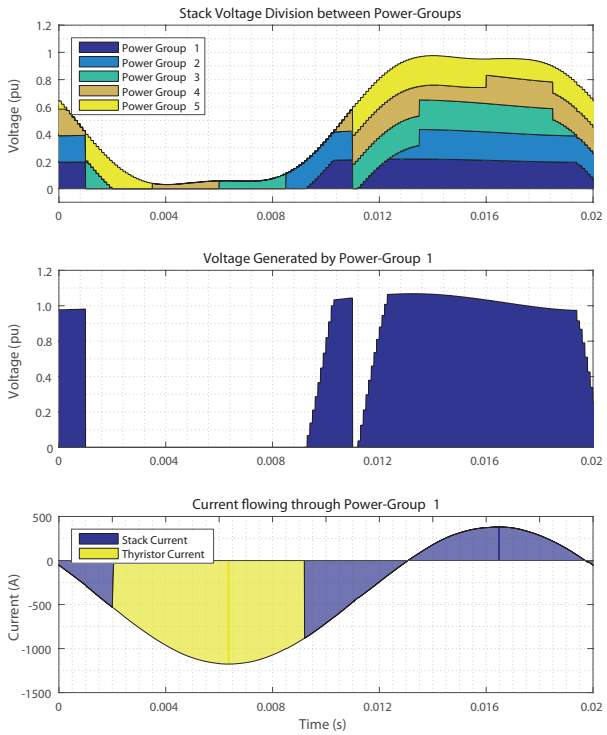
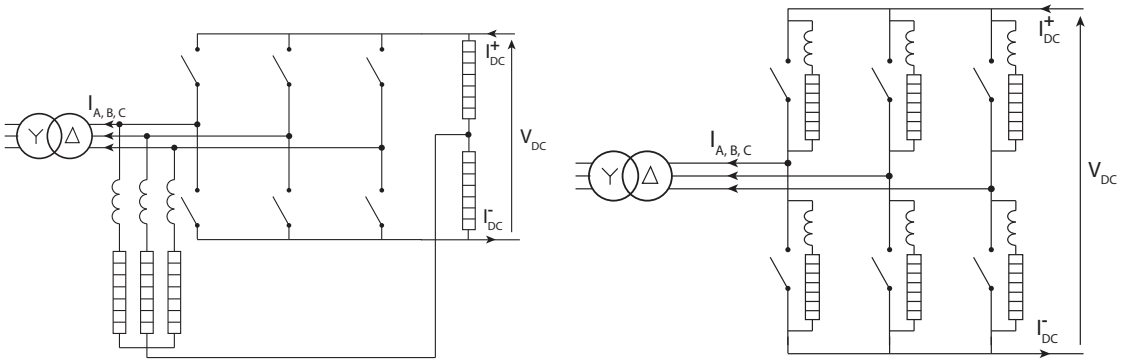


Figure 6.4: De-composition of stack voltage into power-group voltages and current through a power-group in a power-group augmented MMC. Top: Stack voltage divided between power-groups (pu on DC pole to pole voltage). Middle: Voltage generated by power-group 1 within the arm (pu on the available voltage capability within the power-group). Bottom: Current path of arm current through power-group 1.

The Power-Group concept was inspired by the Controlled Transition Bridge (CTB) introduced

by the late Prof. Colin Oates in [106], two variants of which are shown in Fig. 6.5. The CTB is a hybrid converter which combines a six pulse bridge, with stacks of sub-modules. The six pulse bridge switches at the fundamental line frequency and performs the bulk of the power-processing and voltage generation. The multilevel stacks exist to reduce the harmonics generated by the six pulse bridge, as well as managing finer current control. The inclusion of the controllable multilevel stacks means the six pulse bridge could potentially be formed out of thyristors, rather than self-commutating devices such as IGBTs. The commutation of the thyristors could then be managed by the multilevel stacks.



(a) Variant with star STATCOM and DC side stacks.

(b) Augmented modular multilevel converter variant.

Figure 6.5: Controlled transition bridge variants.

The first CTB variant shown in Fig. 6.5a contains a star arrangement of sub-modules stacks, the centre point of which is connected to the mid-point of a pair of stacks on the DC side. The second variant shown in Fig. 6.5b was termed the Augmented Modular Multilevel Converter (A-MMC). In this case the stacks of sub-modules are placed in parallel with each valve of the six-pulse bridge. The A-MMC was a major source of inspiration for the Power-Group concept.

In comparison to other thyristor based voltage source converters such as the Controlled Transition Bridge and Augmented Modular Multilevel Converter, converters augmented with power-group structures do not require the entire stack of sub-modules to be bypassed, or for one phase

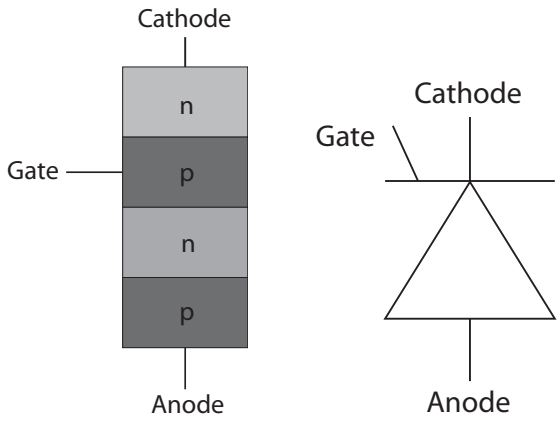
of the converter to be clamped to a DC rail, but instead some fraction of the overall sub-module stack can be bypassed through the thyristor branches in each power-group. Thus the potential efficiency improvement may be achieved without compromise on the quality of the converters output waveform. The power-group concept may be particularly interesting for use in DC fault tolerant converters that require the use of sub-modules that are capable of generating a bipolar output voltage. They may help mitigate the loss penalty that the use of additional IGBTs in full-bridge sub-modules entails.

6.3 Thyristors

This section details the operating principles and limitations of thyristors, in order to provide context for how they will impact the design and operation of power-group structures.

Thyristors are bipolar switching devices which function in a similar manner to a controllable diode. They are capable of blocking voltages in both the forward and reverse direction, allowing current conduction in the forward direction upon the application of a gate current. Once this gate signal is applied the device becomes uncontrolled and requires the current through it to be externally commutated before it can regain its voltage blocking capability.

The structure of a thyristor is shown in Fig. 6.6. It is a four-layer device composed of alternating p-type and n-type layers of silicon. The gate connection of the device is to the p-type layer closest to the cathode of the device. While the device is turned off it is capable of blocking both forward and reverse current because of the forward and reverse facing pn junctions.

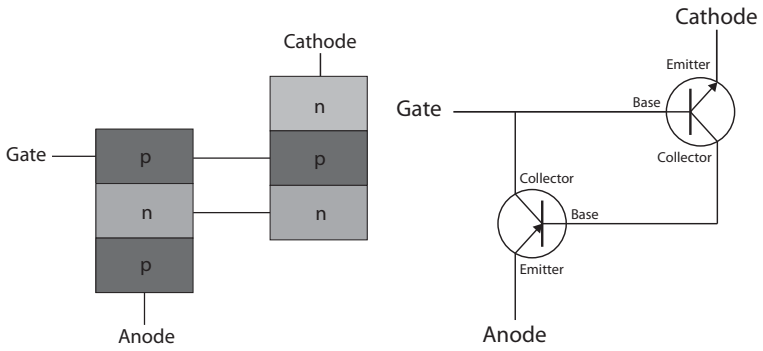


(a) Construction (b) Symbol

Figure 6.6: Thyristor construction and symbol.

6.3.1 Turn-On Characteristic

One of the classic ways of explaining the operation of a thyristor is the use of the two-transistor model, as shown in Fig. 6.7. The thyristor can be split into two linked structures, one forming a *pnp* structure, and the other a *npn* structure. The thyristor's gate is connected to the base of the *npn* structure and the collector of the *pnp* structure. The thyristor may be turned on by application of a gate current, typically a few amps in magnitude, when there is a positive voltage from its anode to cathode. The applied gate current is injected into the base of the *npn* structure, causing the current amplifying BJT structure to draw a current from its collector to its emitter. This amplified current is drawn through the base of the *pnp* structure, causing further amplification of the current. This current then adds to the gate current, causing a positive feedback loop between the *pnp* and the *npn* structures. This feedback action increases until both structures are driven into saturation and the device is in its fully on mode.



(a) Split into pnp and npn structure.

(b) Representation as two BJTs.

Figure 6.7: Two-transistor model of thyristor.

6.3.1.1 Turn-On Losses

When the thyristor first turns on, the load current will not flow equally throughout the entire silicon wafer, instead it is concentrated at first in a region around the gate terminals. The thyris-

tor then goes through a carrier spreading stage as more of the silicon area enters conduction. During this period the forward voltage drop of the thyristor will be higher than it will be when the whole silicon area is in a fully conducting state. The spreading loss, caused by this higher forward voltage drop can considered be to be excess conduction losses. From the data-sheet of the ABB 8 kV 2.12 kA 5STP 20Q8500 thyristor, this spreading loss can be expected to be in the region of 1.2 joules for a rectangular current pulse.

6.3.2 Turn-Off Characteristics

Thyristors can only be turned off if the current flowing from anode to cathode is driven to zero by external circuit conditions. This is typically accompanied by application of a reverse voltage. When this happens thyristors experience a reverse recovery effect due to the evacuation of stored charges within the device's junction.

An illustration of the thyristor turn-off process, adapted from [107], is shown in Fig. 6.8. At the start, the thyristor is in a blocking state with positive forward voltage V_D from its anode to cathode terminals. Upon application of a firing pulse the thyristor enters its forward conduction state, no longer blocking the voltage and conducting the load current.

At turn-off, the anode current is commutated by an external voltage, decreasing through the zero-crossing and then turning negative while the thyristor goes through reverse recovery. The rate at which the anode current is commutated is governed by the magnitude of the external commutating voltage and the inductance within the circuit.

The thyristor will not regain its forward voltage blocking capability until recombination of the carriers at the central *pn* junction takes place. This typically takes much longer than the length of the reverse recovery time (t_{rr}). The minimum required time between the zero crossing of the anode current and the re-gaining of forward voltage blocking capability is called the thyristor turn-off time (t_q). If a forward voltage is applied before this recombination effect has completed the thyristor is at risk of re-entering conduction. In power-group applications this would lead to an effective short-circuiting of the parallel stack of sub-modules. As the turn-off

time is a recombination effect the impact of the rate of charge evacuation from the junction during reverse recovery has limited impact on the magnitude of t_q. The t_q value has positive correlation with [108]:

- Device junction temperature T_j
- Forward current magnitude I_T
- Rate of commutation of anode current $\frac{-di_T}{dt}$
- Rate of reapplied forward voltage $\frac{dV_D}{dt}$

And negative correlation with:

- The peak reverse current I_{RM}
- The reverse voltage V_{RM}

6.3.2.1 Turn-Off Losses

Similar to diodes, thyristors exhibit turn-off losses due to the recovery of stored charge within the device when a reverse voltage is applied across them. For high voltage thyristors, this recovered charge can be relatively large. The turn-off loss that can be expected is approximately linearly dependant on the reverse commutating voltage magnitude, and so if a large commutating voltage is used the turn-off losses may be high.

6.3.3 Operating Limitations

Like all power semiconductor devices, thyristors have limitations on both their current carrying capability and voltage blocking capability. In addition to these limitations they also have di/dt limits during turn on and dV/dt limits when in a blocking state that must be respected. These limits are detailed below.

6.3.3.1 di/dt Limits

Thyristors have limits on the acceptable rate of rise of current through the device during turn-on. This is due to the spreading phenomenon detailed in Section 6.3.1.1. If the rate of rise of current rises fast enough whilst the device is still not fully turned on, localised losses in the regions of the thyristor structure that have turn-on will be heated to the point of damage. The Infineon T2871N thyristor has a critical rate of rise of current limit of $300A/\mu s$.

6.3.3.2 dV/Dt Limits

Thyristors have limits upon the rate of change of applied voltage in the forward direction that they are able to withstand without accidental triggering occurring. This accidental triggering can occur due to the induced currents within the junction capacitance of the device caused by the applied voltage. The Infineon T2871N thyristor has a critical dV_D/dt limit of $2000V/\mu s$.

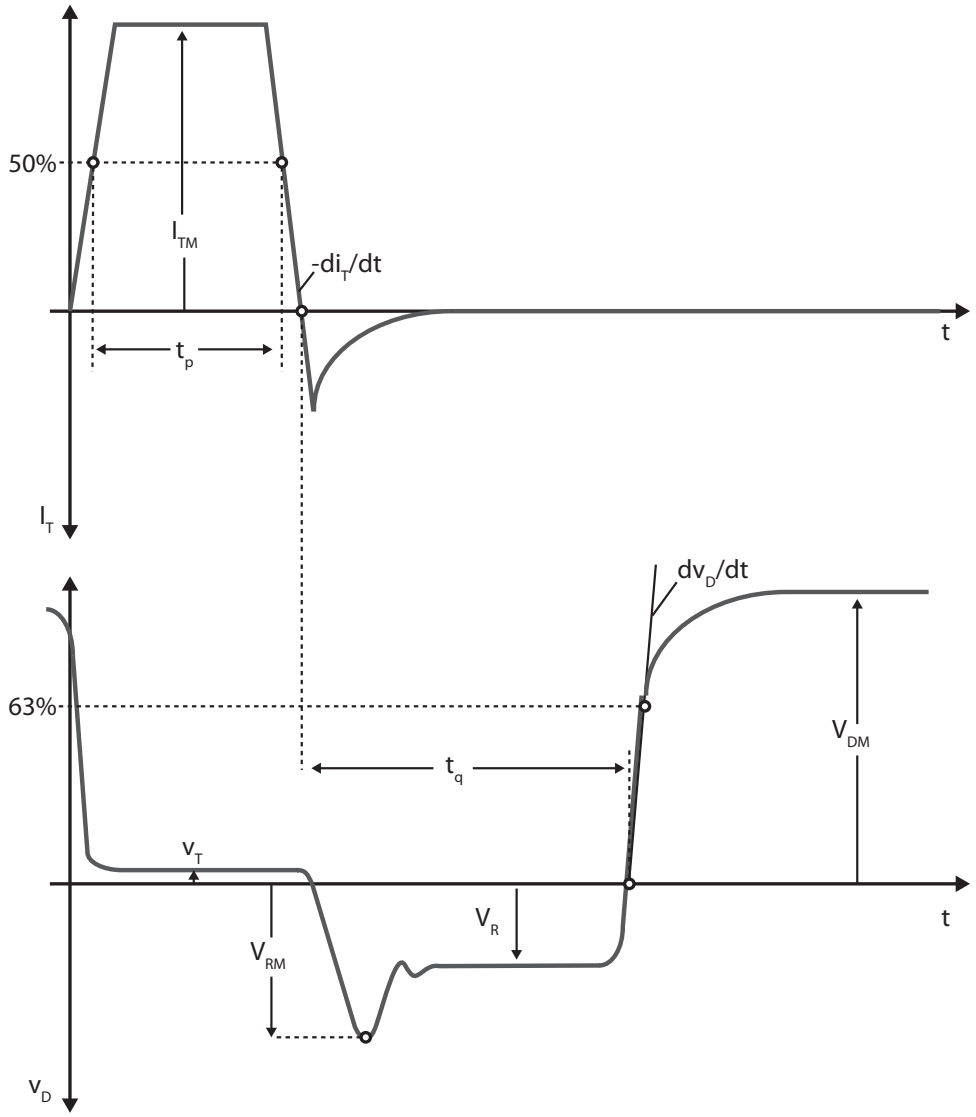


Figure 6.8: Thyristor turn-off characteristics - Adapted from [107].

6.4 Power-Group Design

This section details the design challenges that must be taken into consideration in realising a power-group structure. The section is framed around the design of an example power-group with 8 sub-modules per power-group, however most of what is presented is easily scalable to power-group designs with different number of sub-modules.

For modularity and voltage clearance design reasons it may be desirable to manufacture power-groups with a small number of sub-modules per power-group. A power-group could then take the form of a single rack of sub-modules, such as the design from Alstom Grid shown in Fig 6.9, which is then augmented with a thyristor valve that is located at one end of the rack.



Figure 6.9: Power-Module of 8 sub-modules - Credit: Alstom Grid.

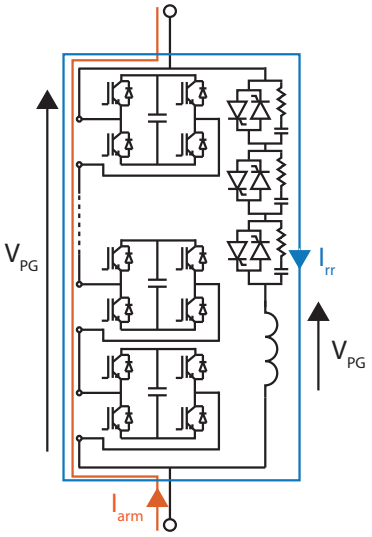
The example power-group design considered in this thesis consists of 8 full-bridge sub-modules in parallel with a thyristor valve composed of three 8 kV phase-control thyristors. The full design specifications of this power-group are given in Table. 6.1.

Table 6.1: Power-group design specification.

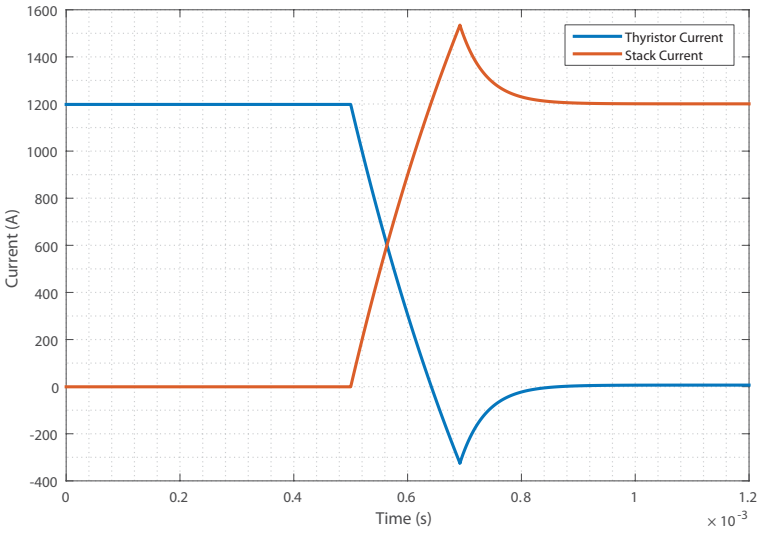
Number of Sub-Modules Per Power-Group	8
Number of Thyristor per Valve	3
Nominal Sub-Module Voltage	1800 V
Peak Sub-Module Voltage	2000 V
Nominal Power-group Voltage	14.4 kV
Rated Peak Current	1500 A
IGBT Device	Infineon FZ1500R33HE3 - 3.3 kV 1.5 kA
Thyristor Device	Infineon T2871N - 8 kV 2.62 kA

6.4.1 Turn-On and Turn-Off Process

In power-groups the turn-on and turn-off of the thyristor valve can be actively controlled by using the parallel stack of sub-modules to generate voltage which will drive a circulating current around the power-group, either forcing the current into or out of the thyristor valve. This is illustrated in Fig. 6.10 for the case of the turn-off of the thyristor valve.



(a) Current paths for arm current and reverse recovery current.



(b) Thyristor and arm currents.

Figure 6.10: Overshoot in arm current due to thyristor reverse recovery.

It will be necessary to include some inductance in series with the thyristor valve in order to allow these circulating currents to be controlled. This inductor will have several roles; Firstly to limit the rate of rise of current through the thyristor during the initial thyristor turn-on process. Secondly to limit the rate of fall of current, and reverse recovery current magnitudes, through the thyristor during the turn-off process. Lastly, as will be discussed in Section. 6.4.2, it has an important interaction with the snubber network placed across of the thyristor valve to limit the dV/dt values experienced by the thyristor.

To ensure the thyristor valve turns on when it is fired it will be necessary for it to be forward biased prior to it receiving a firing signal. Initially natural commutation of the arm current from the sub-module path to the thyristor branch was considered (i.e firing the thyristor valve when the sub-modules are set to a zero voltage state), however advice from GE engineers was that this would result in unreliable turn-on. When the thyristor is fired this forward voltage will then appear across the commutating inductor. The commutating inductor must therefore be sized so as to limit the di/dt of the current through the thyristor during turn-on to sensible levels to prevent damage to the thyristor.

The magnitude of the voltage used to commutate the thyristor valve will also directly impact the magnitude of turn-off power losses within the thyristor valve. It may also be important to ensure low reverse recovery current magnitudes. In power-group applications, the reverse recovery current, I_{rr}, will circulate in the path shown in Fig. 6.10a. This means that during the turn-off process the stack of sub-modules will experience a current that is equal to the arm current, plus the reverse recovery current. Some coordination of timing may be necessary to ensure that no sub-module undertakes a switching operation during the commutation period in order to protect the IGBTs from attempting to switch this large current, which may be beyond their Safe Operating Area capabilities. After the current has been forced through the zero crossing, the voltage across the valve must then held negative for a period of time, termed the hold-off time ($t_{hold-off}$), that exceeds the turn-off time (t_q) of the thyristor. After the hold-off time has expired the power-group would then be available to generate a voltage.

6.4.1.1 Commutating Voltage Generation

In power-groups with many sub-modules per power-group, it may be acceptable to use a single sub-module, with a voltage in the region of 1.8 kV, to generate the commutating voltage for turn-on and turn-off of the thyristor valve. However in designs with fewer sub-modules per power-group, such as the 8 sub-module example power group being discussed, this may not be suitable as it would lead to a requirement for a large commutating inductor and high turn-off losses. It might be possible to include a dedicated turn-off off sub-module within the stack that operates at a lower voltage and is not used for voltage generation. However this leads to increased design complexity, as well as a single point of failure in the event that this turn-off sub-module fails.

One potential method of generating a low voltage, which could be used to control both the turn-on and turn-off of the power-group thyristor, case would be to use the difference between two sub-module voltages to generate the commutating voltage. By inserting one sub-module in a positive direction, and another in the negative direction the differential voltage between the two sub-modules could be placed across the thyristor valve. This may allow voltages in the region of 100-200 V to be used, lessening the required size of the commutating inductor, and decreasing the turn-off losses experienced within the thyristor valve. For the example power-group this would result in commutating voltages in the region of $33 - 60\ V$ per thyristor, leading to turn-off losses in the region of 1 joule per turn-off event. This concept is illustrated in Fig. 6.11. This method of generating the commutating voltage is applicable to any power-group structure with at least two sub-modules, one of which must be capable of generating a bipolar output voltage.

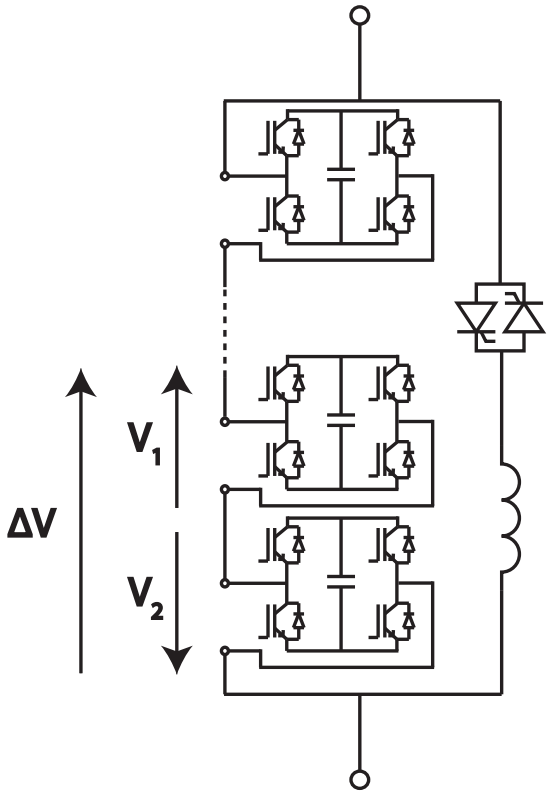


Figure 6.11: Intermediate sub-module commutating voltage generation.

The power-group controller should ensure that the correct differential voltage is available before the power-group thyristor is fired. This could be achieved by actively discharging a sub-module by inserting it into the current path prior to firing the thyristor valve. Once the correct differential voltage is achieved the thyristor valve could be forward biased and then fired.

To ensure that the thyristor is fully turned-off, the hold-off time is required to be longer than the t_q of the thyristor valve. During this time the thyristor valve should have a reverse voltage imposed on it to ensure that it has been fully turned off. If a large phase-control thyristor, such as the T2871N device is to be used, than this hold-off time may be significant. The data-sheet specified t_q value for this thyristor is 550 μs, however this is given for lower dV/dt values (20 $V/\mu s$) than will be experienced in power-group applications ($\sim 200V/\mu s$). For this reason it is considered likely that this hold-off time may have to be in the region of 1 ms.

The sub-modules generating this reverse voltage will be in the current path of the arm current, resulting in them either being charged or discharged. For a converter with peak arm current of 1500 A and a 6 mF sub-module capacitor this would result in a 250 V change in voltage over a hold-off time of 1 ms. For the differential voltage the effective capacitance of the two series sub-module capacitors will be in series, meaning the expected change in the differential voltage would be in the region of 500V. Thus holding the differential pair in the current path for the entire hold-off time will not be feasible.

The proposed solution to providing a reverse voltage for the entire hold-off time is to use the differential voltage for a period t_{Diff}, long enough to commutate the inductor and recover the stored charge within the thyristor valve and then use the stack of sub-modules to place a larger reverse voltage across the thyristor valve for a period t_{Rev}, which comprises the remainder of the hold-off period. Because the stored charge within the thyristor should be mostly evacuated by this point this should result in only minor additional turn-off losses within the thyristor valve when this larger reverse voltage is applied. To limit the voltage deviation of the sub-module used to generate the reverse voltage, the duty could be rotated between different sub-modules within the power-groups stack. The period t_{Rev} could also be used to pre-emptively actively discharge a sub-module to use as the lower charged sub-module for the differential voltage generation pair the next time the power-group thyristor is turned-off. The overall proposed turn-off procedure is shown in Fig. 6.12.

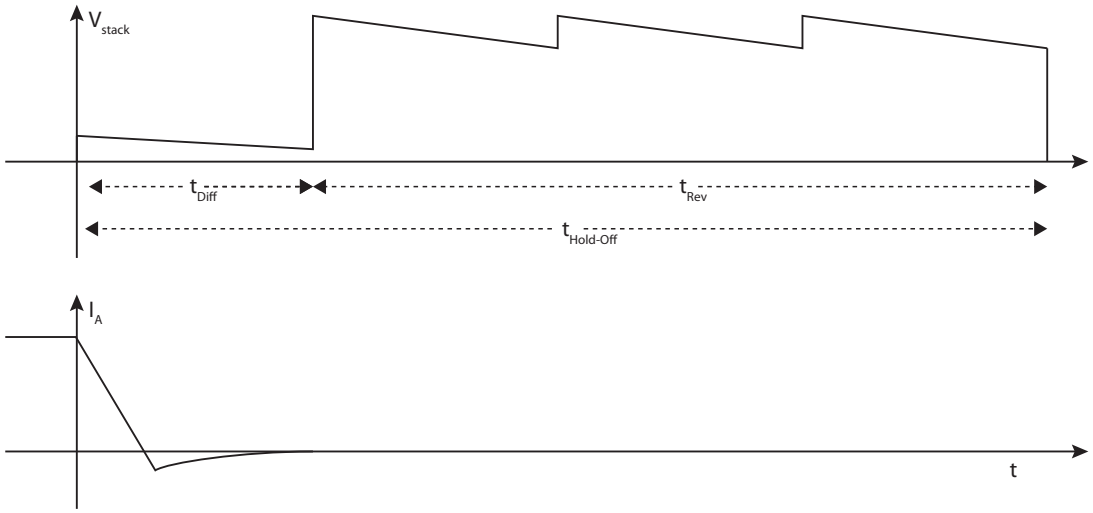
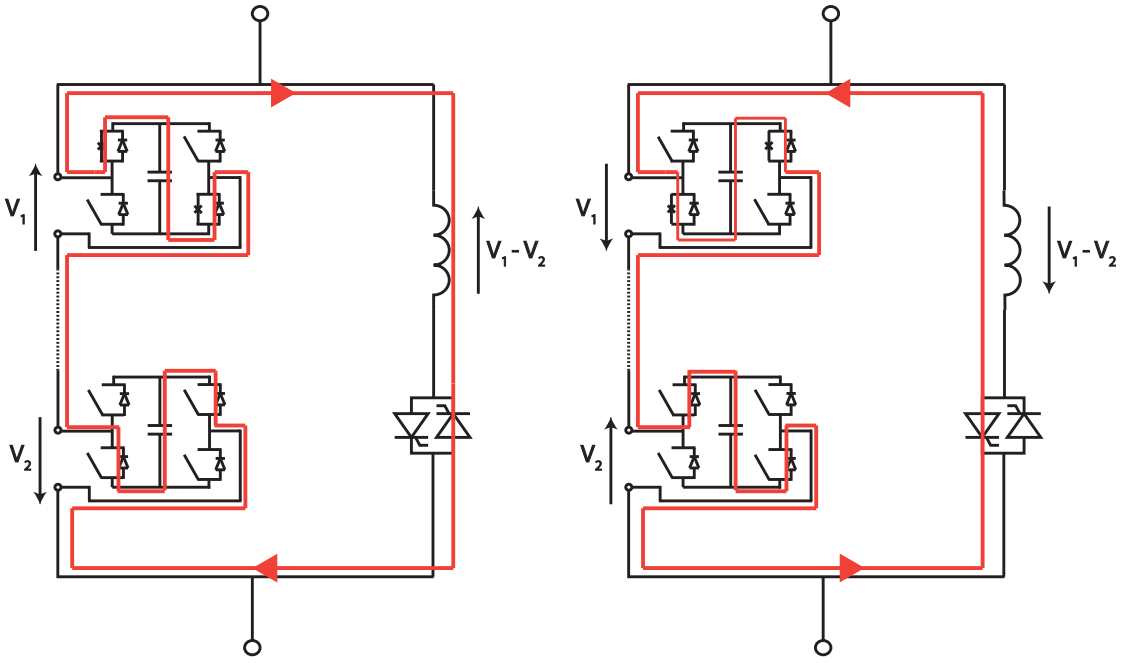


Figure 6.12: Power-group thyristor turn-off procedure showing a period of differential voltage being applied, followed by whole sub-module voltages in rotation.

The required co-ordination between the switching times of the two separate sub-modules used to generate the differential voltage may be of concern. If there is a sizeable delay (in the order of micro-seconds) between the sub-module switching times, then a full sub-module voltage could be applied across the conducting thyristor valve. This could result in the sub-module driving an uncontrolled forward current through the thyristor, or the thyristor being either turn-on or turned-off at a very large di/dt value, depending on the applied voltage polarity. The solution proposed here is to block one of the full-bridge sub-module as part of the turn-on and turn-off procedures. This is illustrated in Fig. 6.13 for the case of generating a turn-off voltage. The sub-module with the lower voltage is blocked, while the sub-module with the higher voltage is actively switched into the correct polarity. This naturally results in a differential voltage being applied across the commutating inductor, without having to simultaneously switch both sub-modules. It has been found to be possible to apply this technique to both the thyristor turn-on and turn-off.



(a) Commutation of the upwards facing thyristor valve.

(b) Commutation of the downwards facing thyristor valve.

Figure 6.13: Commutation of the thyristor valve with a differential voltage - Sub-module with lower capacitor voltage blocked.

6.4.1.2 Overall Turn-On and Turn-Off Procedure

The following paragraphs give a step-by-step description of the proposed power-group thyristor turn-on and turn-off procedure. Each paragraph has its own accompanying figure showing the state of the sub-modules, as well as the current path through the power-group. Lines in grey are non-conducting, while lines in black are conducting.

Step 1 Thyristor valve is turned off and the arm current in conducting through the sub-modules. The sub-modules are free to generate any requested voltage from the controller. The thyristor valves block the voltage generated by the sub-modules.

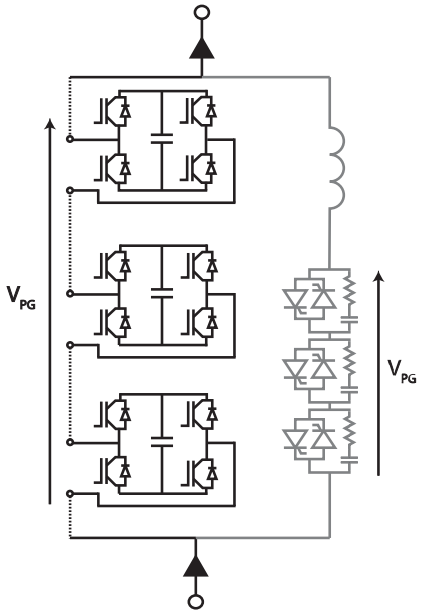


Figure 6.14: Step 1: Power-Group generating voltage output, thyristor valves blocking.

Step 2 The controller logic that controls which power-groups thyristors are used decides to bypass this power-group and utilise its thyristor by-pass branch. All sub-modules apart from the sub-module that will be used as the lower voltage sub-module in the differential pair (V_{SML}) are bypassed. V_{SML} is inserted into the current path in order to discharge it so that the correct difference voltage can be achieved for the turn-on/turn-off of the thyristor valve. The thyristor valve blocks the output voltage of V_{SML} (V_L). During this time the thyristor valve to be fired is reverse biased by V_L. The output voltage V_L can be either additive or subtractive from the overall converter voltage waveform, depending on the polarity of the arm current and overall stack voltage waveform. This can be compensated for through control as discussed in Section 7.6.

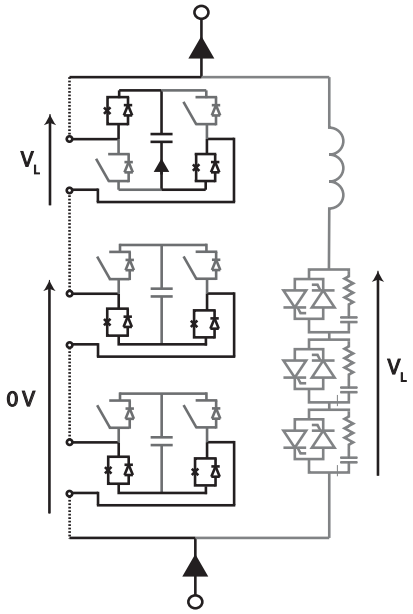


Figure 6.15: Step 2: Active discharge of the sub-module which will have the lower voltage in the differential pair.

Step 3 When the target voltage of V_{SML} has been achieved, the sub-module which is used as the higher voltage sub-module in the difference pair (V_{SMH}) is switched from a bypass state to a blocked state. Its output voltage (V_H) is dependent on the arm current direction and is such that it opposes the current flow. As V_{SML} is inserted so that it is discharging its capacitor, the output voltages V_L and V_H are of opposite polarity. A forward voltage (with respect to the upwards facing thyristors) corresponding to the difference ($V_H - V_L$) between the two sub-module capacitors is applied across the thyristor valve. Again this voltage can be either additive or subtractive from the overall converter voltage waveform, and can be compensated for through control. During this period the difference voltage will increase due to the charging/discharging action of the arm current. This results in V_{SMH} increasing in voltage and V_{SML} decreasing in voltage. To limit this, the firing pulse for the thyristor should be sent shortly after the thyristor is forward biased by this step.

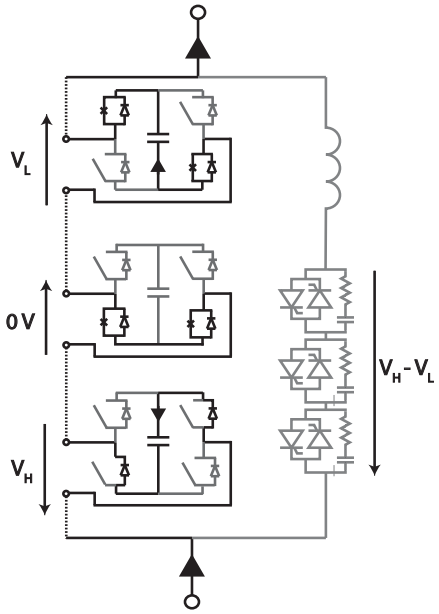


Figure 6.16: Step 3: Higher voltage sub-module is blocked, resulting in a differential voltage forward biasing the thyristor valve.

Step 4 The upwards facing thyristor valve is sent a gate pulse. The voltage across it collapses and the difference voltage ($V_H - V_L$) now appears across the commutating inductor. This voltage drives a circulating current around the path shown in red, driving the arm current from the sub-module path into the thyristor branch. The di/dt through the thyristor valve is determined by the magnitude of the difference voltage and the commutating inductor. As the voltage across the snubber at turn-on is low, the discharge current from the snubber into the thyristor should be modest. V_{SMH} and V_{SML} will continue to charge/discharge while the current commutates. The current has been found to commutate fully through simulation within approximately 40 μs.

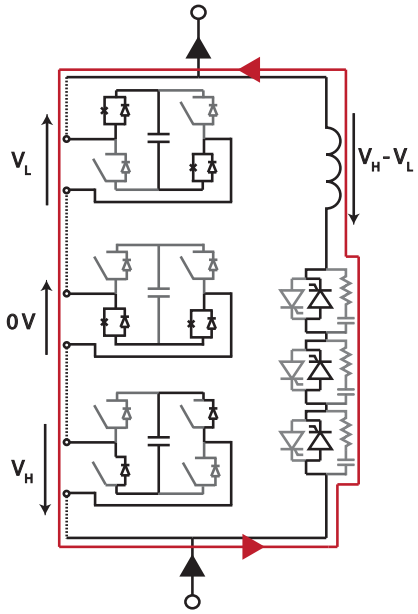


Figure 6.17: Step 4: Upwards facing thyristor valve is fired, current commutates from sub-modules into the thyristor valve.

Step 5 The current in the sub-module path is forced through zero. Some reverse current due to recovery of the diodes within the sub-modules may be expected. The blocked sub-module (V_{SMH}), which has a higher capacitor voltage than the sub-module that is inserted in a negative polarity (V_{SML}), outputs a voltage which opposes any current flow. Both sub-modules are therefore effectively blocked. The overall sub-module path is effectively open-circuited and the arm current flows wholly through the thyristor branch.

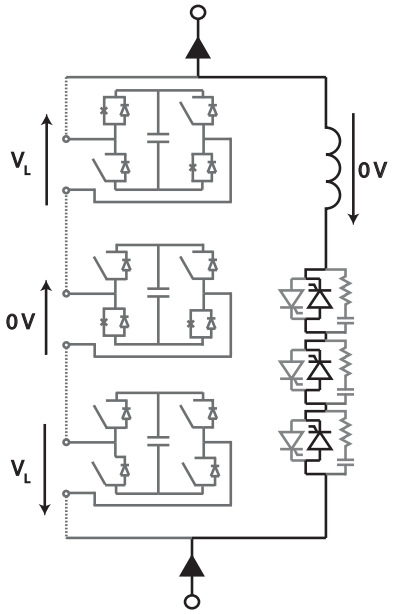


Figure 6.18: Step 5: Turn-On process completes. Arm current flows in the thyristor valve.

Step 6 V_{SML} is then blocked for the remainder of the period when the thyristors conduct the arm current, this is done in preparation for the turn-off procedure. V_{SMH} could then either remain blocked or set into bypass. All other sub-modules within the arm are kept in a bypass state. In the event of a sudden arm current polarity change (in a fault event), which commutates the thyristor and forces the current back into the sub-module path, the maximum voltage applied across the thyristor valve will be 2 sub-module voltages (1 sub-module voltage if V_{SMH} is set to bypass), limiting the risk of dV/dt triggering of the other thyristor non-conducting valve.

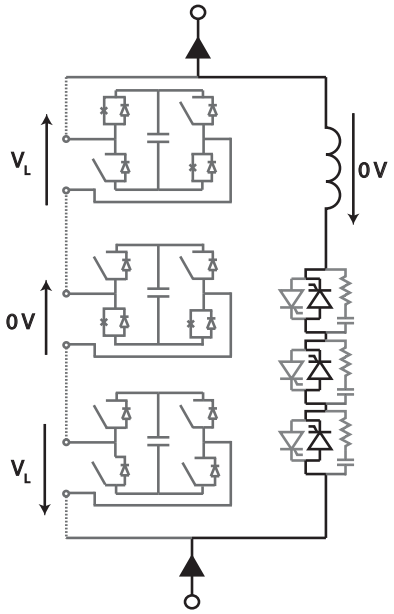


Figure 6.19: Step 6: Turn-On process completes. Arm current flows in the thyristor valve.

A spice simulation of this turn-on procedure is shown in Fig. 6.20. Time 0-50 μs corresponds to step 1, when the sub-modules are conducting the arm current. Time 50-350 μs corresponds to step 2, where V_{SML} is being actively discharged. Time 350-400 μs corresponds to step 3, where V_{SMH} is blocked causing a forward voltage to be applied across the thyristor valve. At t=400 μs (step 4) the thyristor valve is fired and the current is forced from the sub-module path into the thyristor branch. The initial di/dt is low ($\sim$4 A/μs) and increases once the inductor is driven into saturation. The current fully commutates after 20 μs (step 5). At t=500 μs V_{SML} is then blocked (step 6).

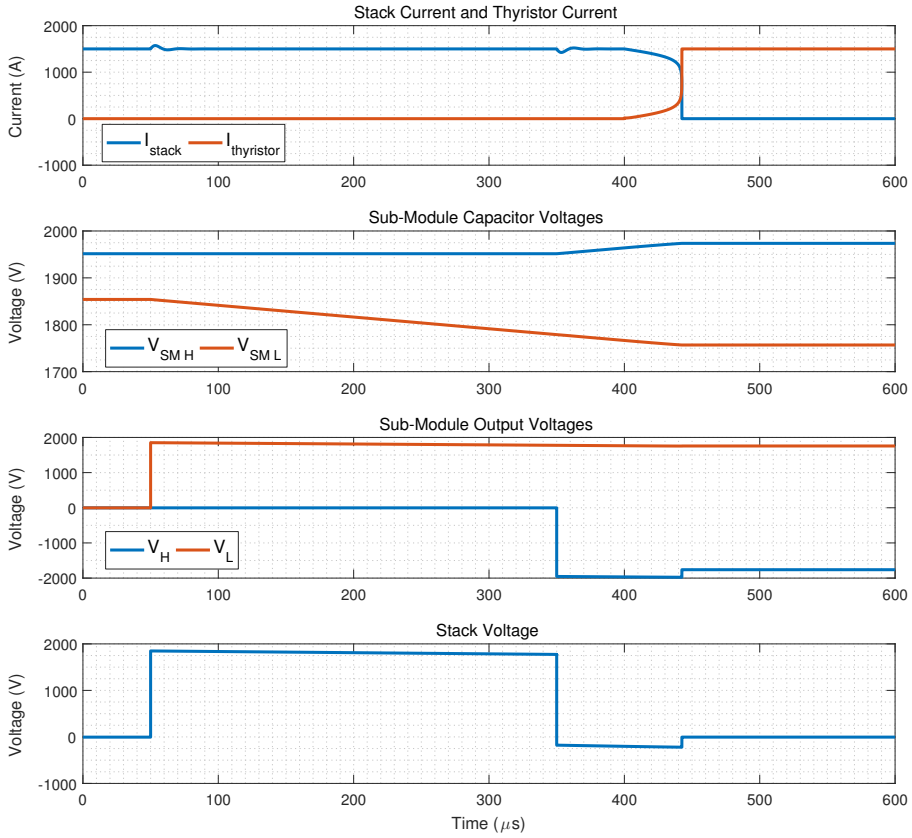


Figure 6.20: Overall power-group turn-on process.

Step 7 After conducting the arm current for some period of time the decision to commutate the power-group thyristor valve is made from a centralised controller. The sub-module with the higher capacitor voltage, V_{SMH} , is switched with an output polarity that will drive a circulating current around the red path shown, driving the current from the thyristor and back into the sub-module path. The sub-module with the lower capacitor voltage V_{SML} remains blocked and so outputs a voltage which opposes any current flow. A difference voltage corresponding to $V_H - V_L$ is imposed across the commutating inductor. The thyristor current is driven through zero and continues negative until the thyristor junction recovers its reverse voltage blocking capability. The voltage of the sub-modules used to impose the difference voltage start to converge due to the charging/discharging action of the arm current. The turn-off process can be expected

to take longer than the turn-on process due to the need to keep the thyristor reverse biased while it recovers. The difference voltage will decrease in magnitude during this time and could potentially result in the thyristor becoming forward biased again if the starting differential voltage is not of sufficient magnitude. For a converter with a 6 mF sub-module capacitor and a 1500 A peak arm current a 200 V differential voltage has been found to give reliable operation in simulations.

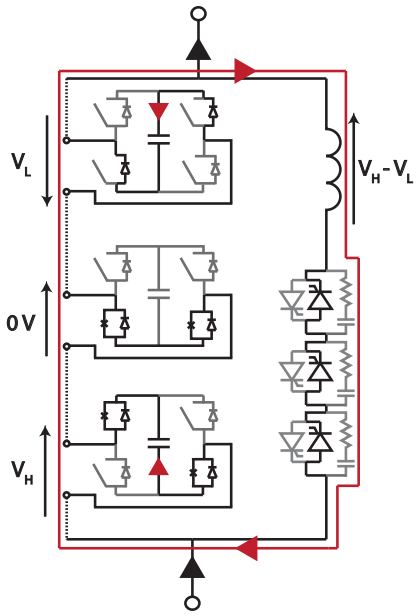


Figure 6.21: Step 7: Sub-module with higher voltage is switched and drives circulating current around red path in order to commutate thyristor off.

Step 8 The thyristor junction recovers and the commutating voltage $V_H - V_L$ is now across the thyristor valve, while the remainder of the stored charge within the thyristor junction is recovered. The sub-modules conduct the arm current plus the reverse recovery current from the thyristor valve, which continues to circulate around the red path.

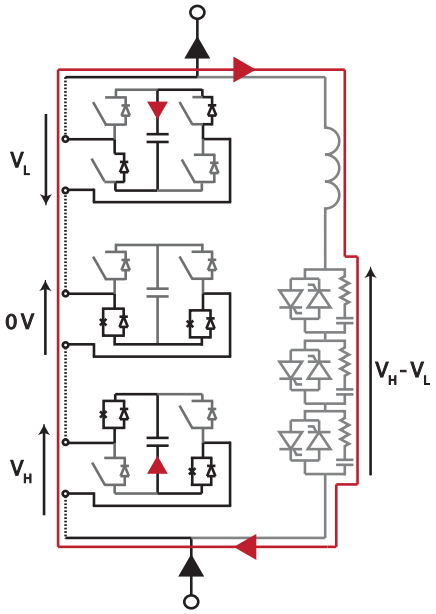


Figure 6.22: Step 8: Thyristor current crosses through zero, reverse recovery current continues to circulate around red path.

Step 9 The stored charge within the thyristor valve is recovered (approximately 300 μs after V_{SMH} is switched) and the arm current is conducting through the sub-module path. The thyristor valve remains reverse biased.

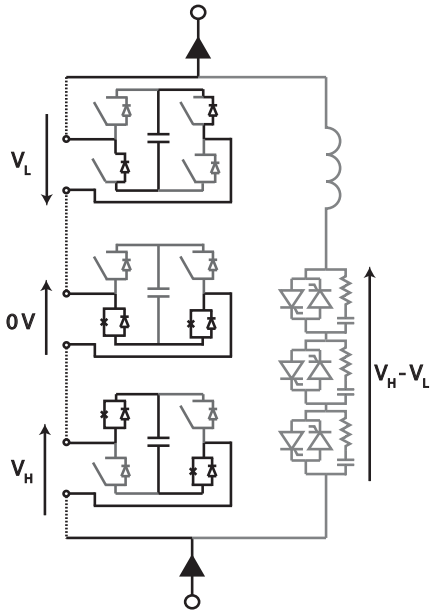


Figure 6.23: Step 9: Thyristor recovers, arm current flows through sub-module path.

Step 10 A larger reverse voltage can be imposed across the thyristor valve for the remainder of the turn-off period to ensure it turns off. As the stored charge has mostly been recovered by this point the larger reverse voltage can be applied without a large penalty in terms of turn-off losses incurred. This also allows another sub-module to be used apart from the pair used to generate the differential voltage.

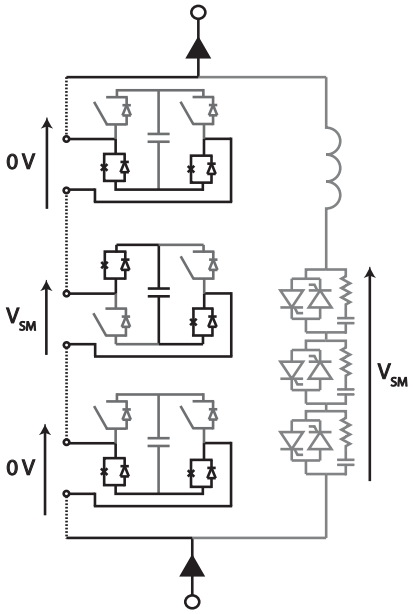


Figure 6.24: Step 10: Larger reverse voltage from a sub-module applied across thyristor valve.

Step 11 After the thyristor valve has been held reverse biased for a sufficient time (an additional 300-700 μs depending on the thyristors characteristics) the turn-off process has been completed. The power-group is now able to use its sub-modules to generate an output voltage.

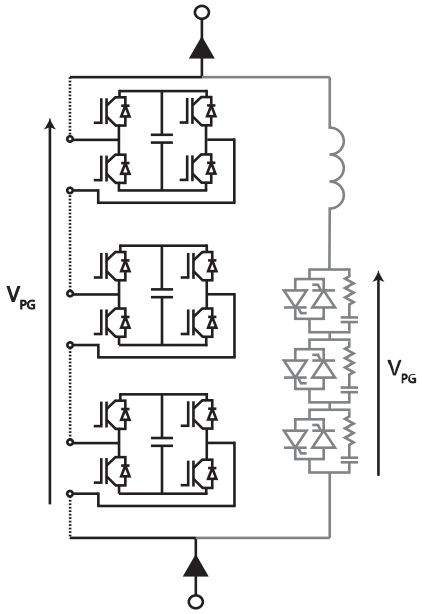


Figure 6.25: Step 11: Thyristor turn-off process completes, power-group is free to generate a voltage output.

Figure. 6.26 shows a SPICE simulation of the overall proposed turn-off procedure. At t=0 μs the differential voltage is applied in order to commutate the thyristor (step 7). The thyristor current is driven down through zero, forcing the arm current back into the sub-module path. The sub-module path conducts the arm current and the thyristor reverse recovery current. At t=160 μs the thyristor junction recovers and the commutating voltage appears across the thyristor, causing turn-off losses. The thyristor current decays from its peak reverse current until it is close to zero (step 9). At t=300 μs a full sub-module voltage reverse voltage is then applied at across the thyristor for the remainder of the turn-off period (step 10). This period can be expected to take an additional 300-700 μs, and so is not included in the plot. When this is complete the power-group turn-off procedure is fully completed and the power-group can now generate a voltage using its sub-modules (step 11).

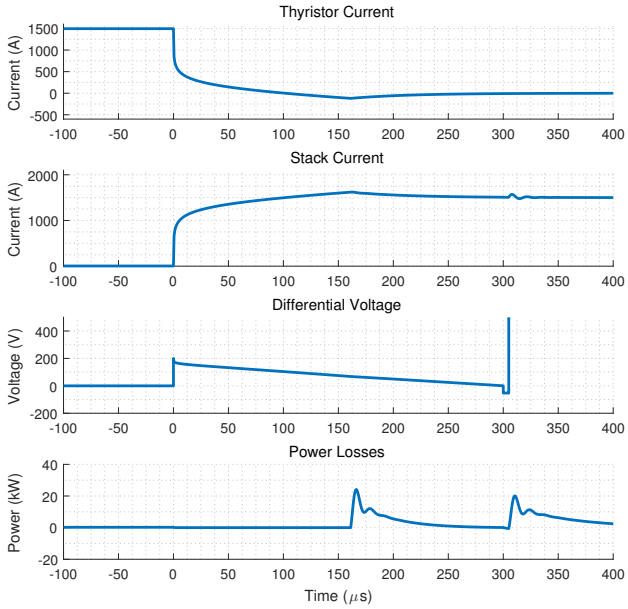


Figure 6.26: SPICE simulation of overall power-group turn-off procedure.

The overall turn-on and turn-off process for a power-group, as simulated in simulink, is shown in Fig. 6.27. No reverse recovery effects are seen because the limitations of the thyristor models within simulink. Prior to firing the thyristor a sub-module is actively discharged (t=0.0035 s) so that the target differential voltage can be achieved. The thyristor is then fired (t=0.0037 s). The thyristor then conducts the arm current for several milliseconds. At turn-off the thyristor is commutated by applying a differential voltage from two of the sub-modules (t=0.00725 s). After the thyristor current has been commutated and the reverse recovery process completed, the differential pair of sub-modules are switched to zero and three other sub-modules are rotated in duty in order to keep the thyristor valve reverse biased (t=0.0075 s). After the hold-off period is finished the turn-off procedure has completed and the power-group is free to generate a voltage using its sub-modules.

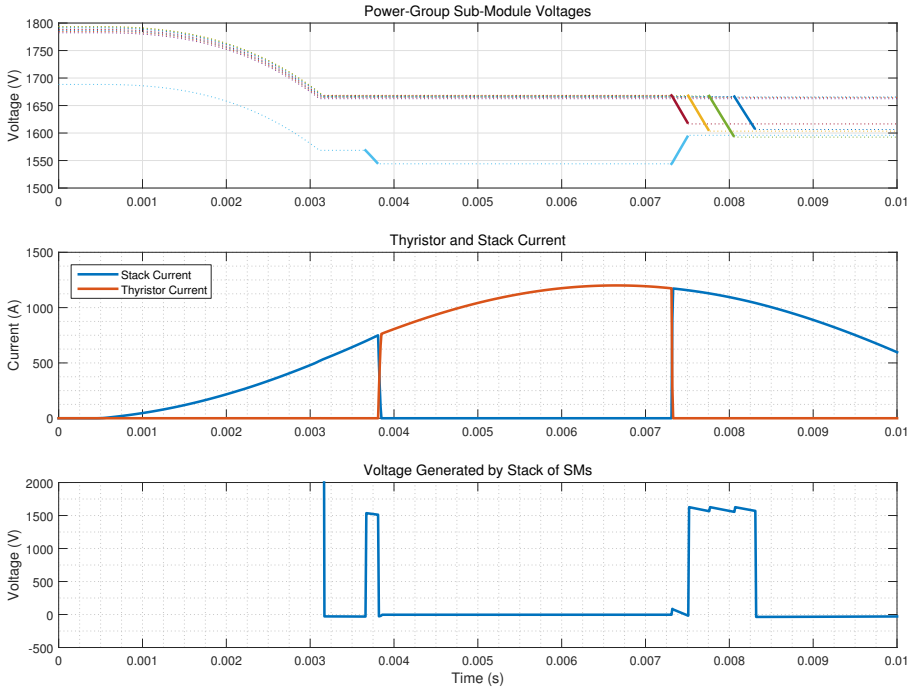


Figure 6.27: Power-group turn-on & turn-off process simulated in Simulink.

6.4.1.3 SPICE modelling of Power-Group Turn-Off Process

This section details the modelling of the power-group turn-off process which has been carried out using PSPICE. The model has been created with the aim of capturing the thyristor reverse recovery characteristic, allowing the interaction between the sub-module capacitor size, commutating inductor size, and the thyristor turn-off characteristics to be investigated.

One of the common methods of modelling thyristor reverse recovery characteristics is the use of the exponential model [109], in which the reverse recovery current is modelled in two stages given by eq. (6.1) and illustrated in Fig. 6.28. When the thyristor anode current (I_A) goes through the zero crossing the reverse recovery is modelled in two stages, up until the peak reverse recovery current (I_{RM}) it decreases at a constant di/dt. When the peak is reached the decay of the recovery current is modelled by an exponential function.

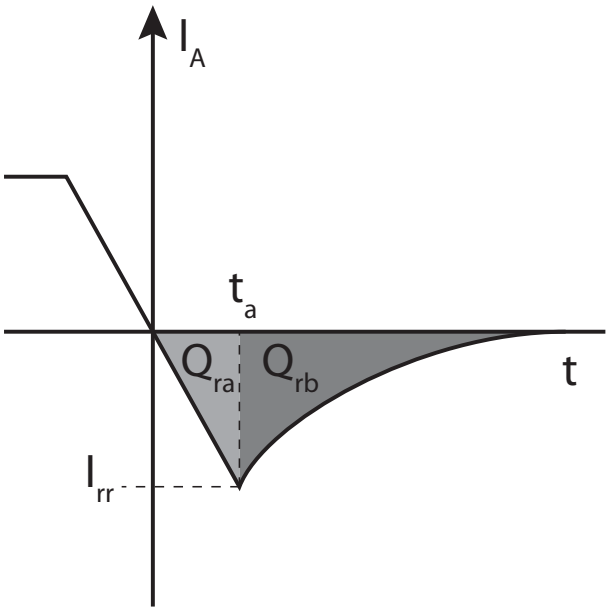


Figure 6.28: Thyristor reverse recovery exponential model.

$$I_A(t) = \begin{cases} -\frac{di}{dt} \times t & \text{if } t \leq t_a \\ -I_{rr} e^{\frac{-(t-t_a)}{\tau}} & \text{if } t > t_a \end{cases} \tag{6.1}$$

The value of Q_{rr} is assumed to be determined by the di/dt value of the thyristor anode current at the zero crossing, measuring the di/dt by taking a linear line from its peak value, to the when it reaches the zero crossing. The curve showing the relationship between Q_{rr} and di/dt was extracted from the device's data-sheet and a power function fitted to it. At the zero crossing the SPICE model logs the di/dt value and determines the value of Q_{rr} to use for the next stage of the simulation.

The exponential model assumes a constant di/dt in the time period from $t = 0$ to $t = t_a$. In the power-group turn-off procedure this will not necessarily be the case as the differential voltage generated by the stack will be of time decreasing value during this period. To account for this the expected relationship between the recovered charge before the peak reverse recovery current (Q_{r1}) and the overall recovered charge (Q_{rr}) is used to determine when the recovery

current should peak. Extracting the given values from the device data-sheet of the recovered charge (Q_{rr}) and the peak reverse recovery current (I_{RM}) and comparing the calculated value of the recovered charge before the reverse recovery current peak (Q_{r1}) and the overall recovered charge (Q_{rr}) reveals an approximately constant relationship of $Q_{r1} \approx 0.36 \times Q_{rr}$ across the given range of values.

Under the above assumption, the remaining charge to be evacuated from the device during the exponential part of the recovery current is given by (6.2)

$$Q_{r2} = \int_{t_a}^{\infty} I_{rr} e^{\frac{-(t-t_a)}{\tau}} dt \tag{6.2}$$

Setting $Q_{r2} = 0.64 Q_{rr}$ and solving for τ leads to an expression (6.3).

$$\tau = \frac{0.64 Q_{rr}}{I_{RM}} \tag{6.3}$$

To model the thyristor, the approach presented in [110] is used. The thyristor is modelled as a variable resistor whose value is changed to make the current through the thyristor follow a determined current profile. This approach is useful as it is relatively simple to implement and is computationally efficient.

Until time t_a, the thyristor is modelled as a low resistance. The value of R_{thy} can be determined by examining the simple equivalent circuit shown in Fig. 6.29.

The current through the thyristor (I_{thy}) can be expressed as (6.4).

$$I_{thy} = -\frac{V_L + V_{stack}}{R_{thy}} \tag{6.4}$$

Rearranging for R_{thy} and setting I_{thy} to the exponential model of the recovery current gives (6.5). The behavioural model of the thyristor is switched to this expression at time t_a, when amount of recovered charge reaches $0.36 Q_{rr}$. The value of the peak reverse recovery current ,I_{RM}, is logged at this time. The value for τ, from expression (6.3), can then be calculated.

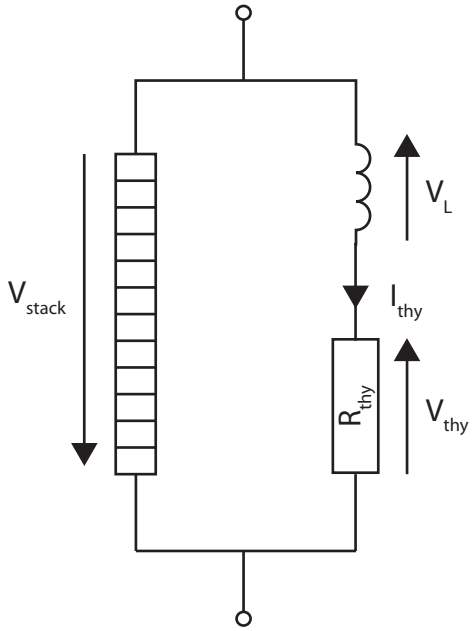


Figure 6.29: Power-Group turn off equivalent circuit.

$$R_{thy} = -\frac{V_L + V_{stack}}{I_{RM} e^{-\frac{t-t_a}{\tau}}} \tag{6.5}$$

6.4.1.4 Commutation inductor Sizing

Simulation results of the turn-off using differential voltage generation when using a linear inductor are given in Fig. 6.30. In this case a 300 V differential voltage was used as this was found to be necessary to evacuate the charge within the thyristor before the larger reverse voltage is applied at 300 μs. The minimum inductor size must therefore be in the region of 30 μH in order to limit the turn-on di/dt to the region of 10 A/μs.

As the inductor becomes larger, the time it takes for the thyristor current to reach the zero crossing increases. As will be discussed in Section 6.4.2, the commutation inductor size significantly impacts the design of the dV/dt limiting snubber network placed across the thyristor valve. If the design calls for a larger inductor size, this could be countered by increasing the magnitude of the differential voltage applied. However, this will come at a cost of increased

turn-off losses. In all inductor size cases, except the 45 μH case, the thyristor reaches the zero crossing and recovers before the larger reverse voltage is applied across the valve. In these cases, the losses within the valve are in the region of 1.5-3 Joules, significantly below the losses experienced when a full sub-module is used to commutate the thyristor valve. In the case of the 45 μH inductor the stored charge within the thyristor is not fully evacuated before the larger reverse voltage is applied. This results in relatively large turn-off losses of 6.9 Joules.

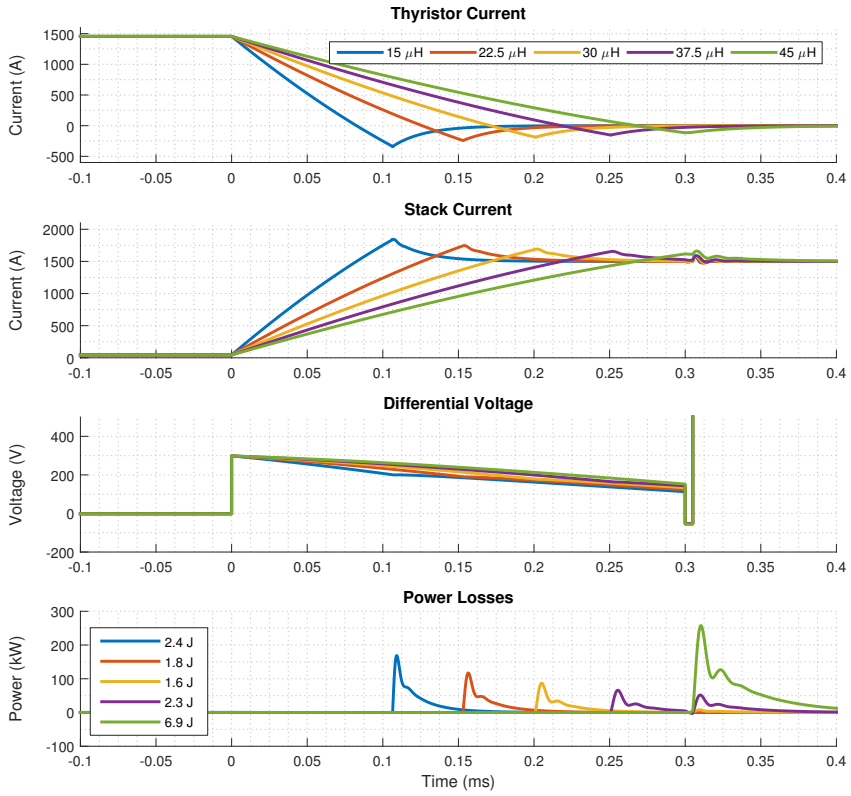


Figure 6.30: Turn-off process using a 300 V differential voltage with 6 mF sub-module capacitors and a linear commutation inductor. Overall energy loss given in the last sub-plot.

A saturable inductor could also be used as this could allow a physically smaller inductor, as well as making lower differential voltage magnitudes practical, as the current can be driven to zero faster than when a linear inductor is used. Simulation results of the turn-off procedure

when using a saturable inductor with a 300 A saturation characteristic are given in Fig.6.31. The use of the saturable inductor allows the use of higher inductances, whilst still allowing the thyristor to recover within 0.3ms. The overall turn-off losses incurred are in the region of 1-2 Joules for all cases. The peak value of the reverse recovery current reduces as the inductor size is increased, decreasing from approximately 500 A when a 15 μH inductor is used, to 80 A when a 45 μH inductor is used.

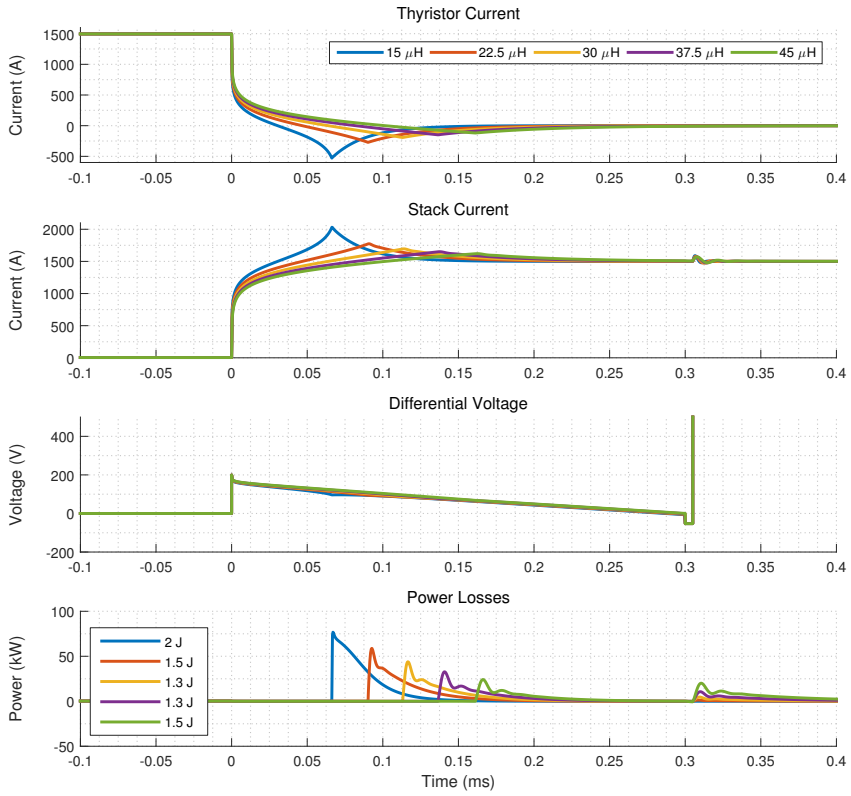


Figure 6.31: Turn-off process using a 200 V differential voltage with 6 mF sub-module capacitors and a saturable inductor with a saturation characteristic at 300 A. Overall energy loss given in the last sub-plot.

6.4.2 Snubber Design

As discussed in Section 6.3.3.2 thyristors are particularly sensitive to failure due to excessive dV/dt values. In power-group applications the thyristor valve will be operated in parallel with a stack of sub-modules which is capable of generating very high dV/dt values. To limit this dV/dt stress, the power-group design must include some snubber circuits across each of the thyristors. The snubber proposed is a simple RC circuit across each thyristor valve, which is in series with the commutating inductor. A circuit diagram of the full power-group arrangement is given in Fig. 6.32.

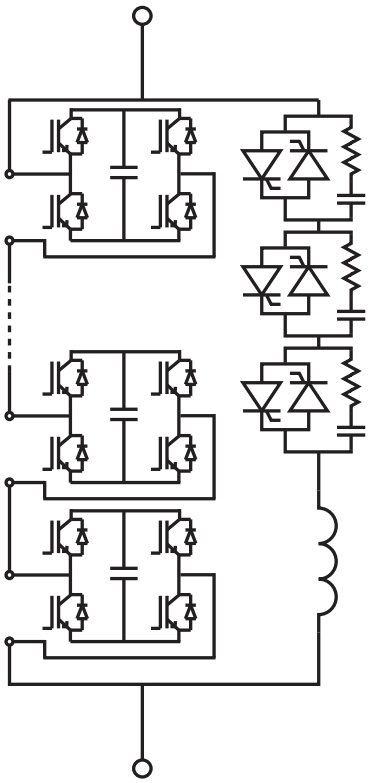


Figure 6.32: Power-group design including thyristor snubber circuit.

The snubber will draw a current from the stack of sub-modules during sub-module switching events, because of the charging up of the snubber capacitor. This current may be add to or

subtract from the converter's arm current. The design of the snubber must then take the peak current draw into consideration to prevent potential damage to the IGBTs due to over-currents.

If the entire stack of sub-modules is switched simultaneously, then the snubber design may be so onerous as to be infeasible. One method of easing the snubber design would be to enforce timed switching of the sub-modules within the power-groups, so that the sub-modules are inserted in a controlled staircase ramp. This is illustrated in Fig. 6.33. The snubber design would then only have to be capable of limiting the dV/dt values generated by the switching of single sub-modules, rather than the entire sub-module stack. This will require a local controller capable of managing the timed switching of each sub-module. Additionally the dynamic response of the converter may also be affected due to this slewing of the voltage output of each power-group. The impact of this is assessed in Chapter. 9.

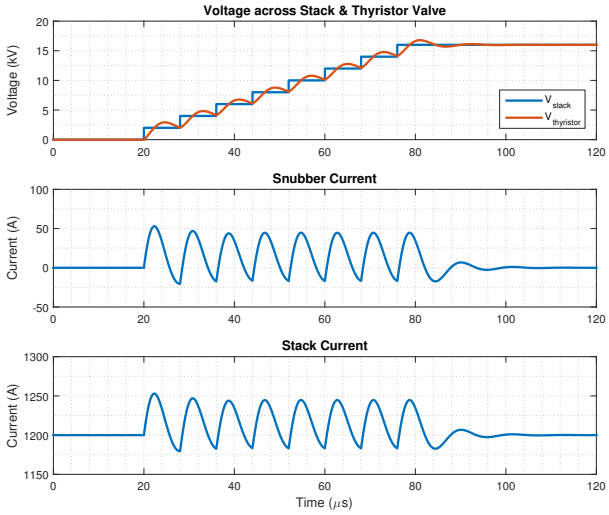


Figure 6.33: Controlled switching of power-group sub-module stack.

In typical thyristor applications, the snubber resistor must also be sized so that it limits the discharge of the snubber capacitor into the thyristor during turn-on. In power-group applications this may not be a concern if the forward voltage across the thyristor at turn-on is relatively low. If differential voltage generation is used then the voltage across each thyristor at firing

will be in the region of 60 V. The minimum required snubber resistor size to limit the discharge current into the thyristor to a sensible limit of 100 A is around 0.6 ohms.

The Infineon T2871N has a critical dV/dt limit of 2000 $V/\mu s$. A practical snubber design should limit the actual peak dV/dt to a level significantly below this. A design target of reaching dV/dt of 200 $V/\mu s$, an order of magnitude below the critical level, was chosen in this thesis. In the example power-group this corresponds to 600 $V/\mu s$ across the entire thyristor valve.

The required settling time of the snubber will depend on the time interval between switching of sub-modules in a power-group. This in turn will be impacted by the required time-step of the converters controller. If a power-group must be capable of achieving its voltage reference within one controller time-step, the time interval between switching must be at least the controller time-step divided by the number of sub-modules within a power-group. If a controller frequency of 20 kHz is required then for a power-group with 8 sub-modules the switching time interval should be in the region of 6 μs. When examining the settling times of the snubber it was found that the snubber network may not necessarily have reached a steady state from the previous sub-module switching event before another sub-module is switched in. From simulation experience having settling times in the region of 4 times ($\sim$ 25 μs) the switching time interval was found to give acceptable results.

If differential voltage generation ($\sim$150-200 V) is used to control the turn-on and turn-off of the thyristor than the minimum required inductor size to limit the di/dt during turn-on is in the region of 15-20 μH. A design sweep for three inductor sizes is given in Fig. 6.34. Limiting the dV/dt stress across the valve to below the target of 600 V/μs (200 V/μs per thyristor) was found to be impossible for the 15 μH inductor size considered. Limiting the dV/dt values to this target becomes possible at the 30 μH and 45 μH inductor sizes considered.

Achieving a settling time of 20 μs with a 30 μH inductor gives a required resistor value of 3 Ω and capacitor value of 0.85 μH. The peak current draw with these values is in the region of 120 A. For the 45 μH inductor the required values are in the region of 4.5 Ω and 0.6 μF. This design results in a peak current draw in the region of 80 A.

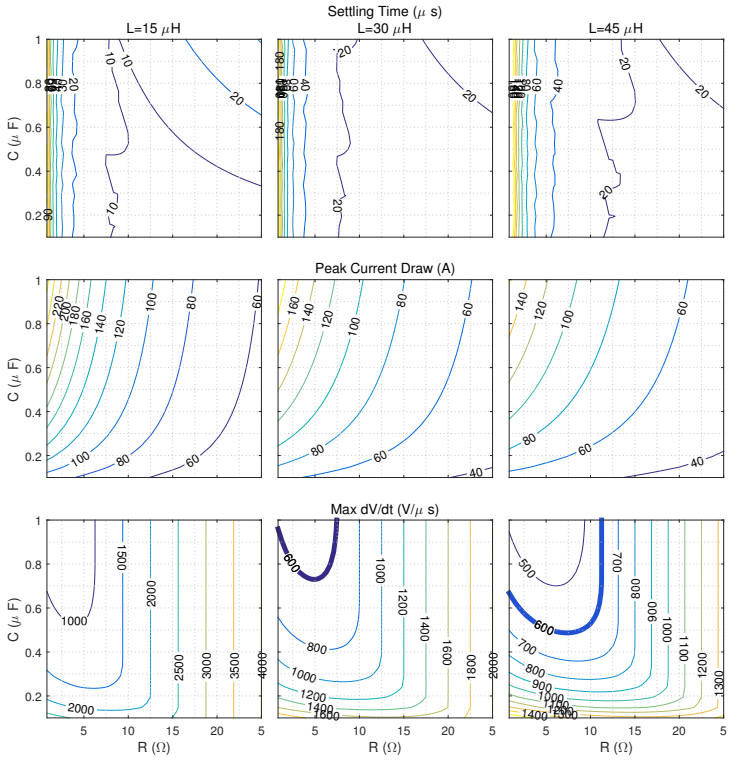


Figure 6.34: Power-group snubber design.

A spice simulation of a power-group with the snubber design with a 45 μH inductor is given in Fig. 6.35. The losses within the entire snubber network during a ramped voltage increase from zero volts to full output voltage is 0.95 Joules. This corresponds to ∼0.1 Joules per sub-module switching event. For comparison the turn-off loss within a single IGBT at full load current can be expected to be in the region of 2 Joules.

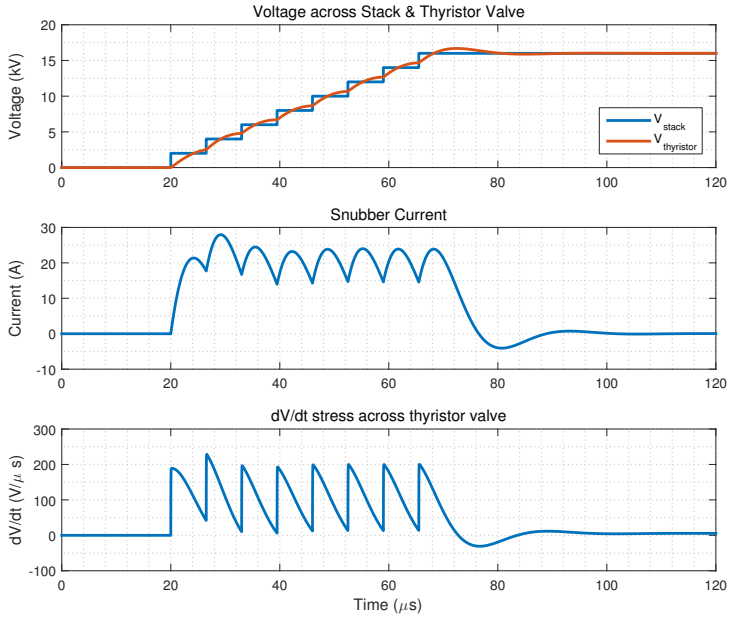


Figure 6.35: Power-group snubber design.

6.4.3 Power-Group Asymmetric Voltage Capability Recovery

As discussed in Section. 6.4.1.1, after the differential voltage is used to commutate the thyristor valve a larger reverse voltage should be applied across the thyristor valve for the remainder of the hold-off time to ensure that the thyristor fully turns off. This leads to a large delay in the power-group being free to generate a voltage. The turn-off process proposed in Section. 6.4.1.1 uses a single sub-module to generate this reverse voltage, however it may be possible to allow the power-group to use any voltage, up to its full available voltage, once the polarity of the voltage is such that the previously active thyristor valve remains reverse biased. This means that there may an asymmetry in how fast the voltage capability of a power-group can be recovered, depending on whether the upwards or downwards facing thyristor was conducting. If the upwards facing thyristor is conducting the power-group may be free to generate any positive voltage once the differential voltage period (t_{diff}) has finished, while a negative voltage generation must be restricted until the hold-off time has completed ($t_{hold-off}$). The converse is true if the downwards facing thyristor valve was conducting.

A SPICE simulation of a power-group doing a controlled ramp up to its full available voltage after using a differential voltage to commutate the thyristor valve is shown in Fig. 6.36. In this example the current was flowing through the downwards facing thyristor, meaning negative voltage capability can be recovered after the differential voltage period. In the simulation a controlled switching of sub-modules to the power-groups full negative voltage is applied $300\mu s$ after the start of the turn-off process. Because the stored charge within the thyristor valve is evacuated before this large reverse voltage is applied, the turn-off losses within the valve are still maintained to a low level. The reverse recovery model of the thyristor that has been used in this work may not adequately capture this case where the reverse voltage applied across the valve changes. If performing this quick ramp in voltage does cause significant losses it utilisation might be restricted to emergency situations where the converter is required to regain as much voltage capability as quick as possible. Such scenarios are investigated in Chapter. 9.

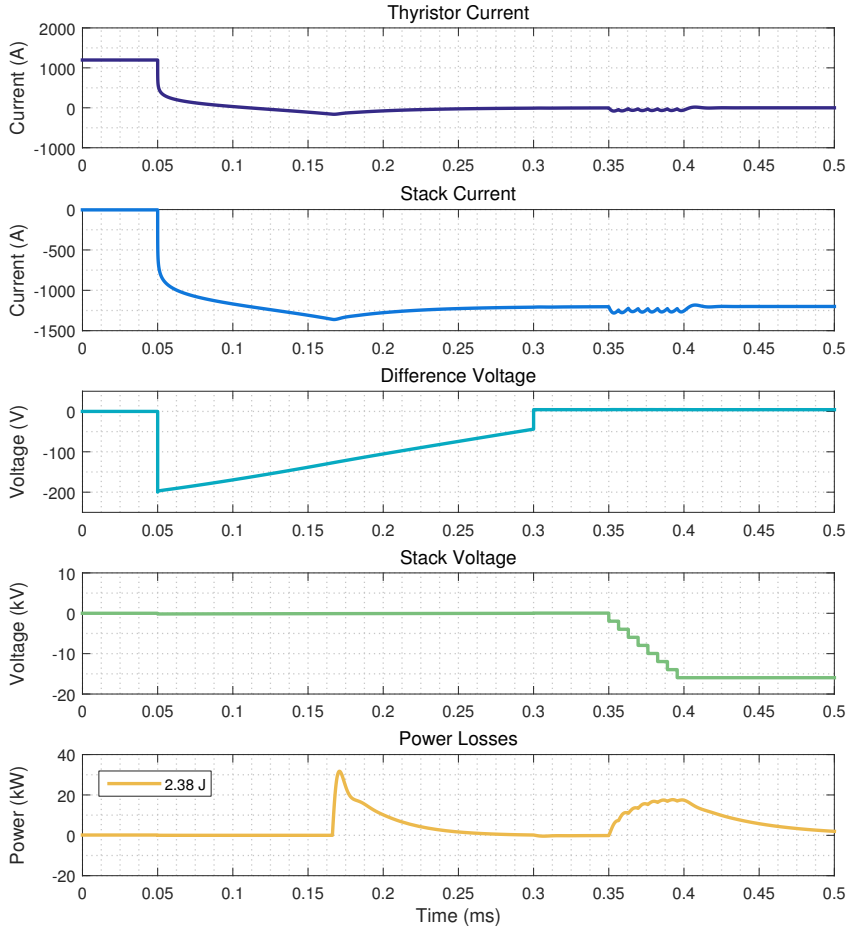


Figure 6.36: Power-group turn-off process with ramp to full voltage after differential voltage generation.

6.5 Conclusion

This chapter has introduced the novel idea of power-groups, composed of a modular structure of sub-modules in parallel with a thyristor valve. The main aim of this development of this structure has been to allow DC fault tolerant voltage source converters to be achieved, without a major loss of converter efficiency. The main design challenges that such a structure entails have been identified, notably the turn-on and turn-off control of the thyristor valve. The potential of using differential voltages, generated by two sub-modules, to control both the turn-

on and turn-off procedures with minimal losses has been investigated. A detailed procedure for performing the turn-on and turn-off of the thyristor valve has been given. The following chapters will investigate how a series arrangement of power-groups can be operated together to form a converter arm, what converter topologies are most suitable for augmentation with power-groups, and then how the use of power-groups impacts the converters dynamic response and fault ride through capability.

7 Power-Groups: The Design Considerations for a Centralised Controller

The previous chapter introduced the concept of power-groups, and detailed the design and operation of a single power-group. To form a power converter, power-groups must be series connected to form a stack which is controlled to appear as a voltage source. The power-group turn-on and turn-off procedures introduce several challenges in achieving this, most notably the required hold-off period that must be respected to ensure the power-group thyristor valves full turns off. This chapter details the development and operation of a Power-Group Centralised Controller (PGCC) that is used to manage a set of power-groups that have been series connected to form a stack within a multilevel converter, while respecting the operational limits of the individual power-groups.

The primary function of the PGCC is to transform the stack voltage reference, received from the converter's current controller, into IGBT gate signals and thyristor firing pulses for the sub-modules and thyristors within each power-group. The PGCC must do this whilst also achieving the following functions:

- Managing the power-group thyristor turn-on process.
- Managing the power-group thyristor turn-off process.

- Limiting the voltage deviation between the sum sub-module voltages of each power-group within a converter arm.

- Limiting the voltage deviation between sub-modules within each power-group.

The PGCC must achieve all of these functions whilst also achieving high utilisation of the power-group thyristors in order to achieve the efficiency improvement expected of the power-group concept.

The PGCC is subdivided into several subsystems, an overview of which is shown in Fig. 7.1. The function and workings of each sub-system are detailed in the sections that follow.

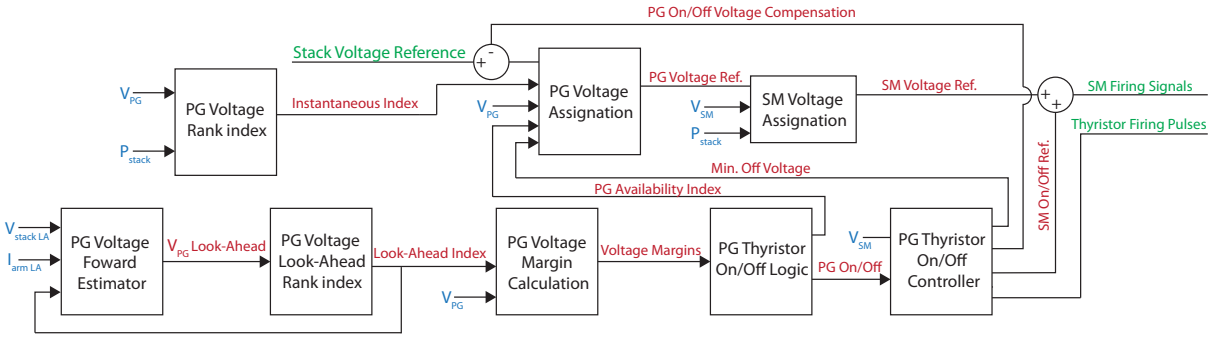


Figure 7.1: Power-group centralised controller overview. Control input/output signals are shown in green, measurement signals are shown in blue, internal signals in red.

For clarity the following definitions are used within this chapter. A power-group is referred to as *active* if its thyristor valve is not conducting and its series connected stack of sub-modules is free to generate either a positive or negative voltage. A power-group is referred to as *bypassed* if its thyristor has been fired and is conducting, and its sub-modules are generating zero volts.

7.1 Stack voltage Capability

Each time a power-group's thyristor is fired the voltage capability of the sub-modules within that power-group will cease being available for the current controller to use. This is illustrated

for the case of a power-group augmented MMC in Fig. 7.2. In order for the converter to retain proper current control, the available voltage within the arm of the converter must be maintained at a level above the requested stack voltage from the current controller.

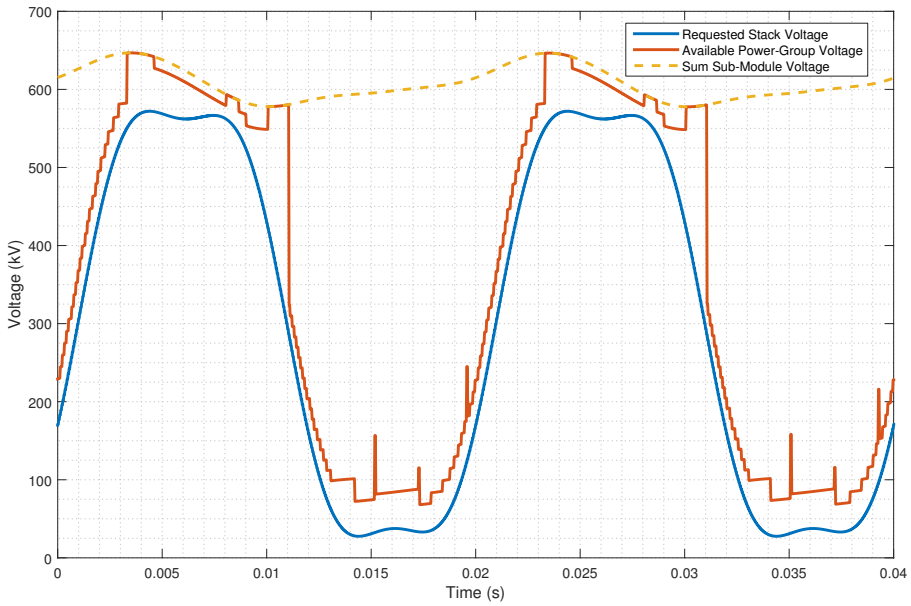


Figure 7.2: Requested stack voltage, sum available power-group voltage, and sum sub-module voltage in an augmented Modular Multilevel Converter.

Because of the necessity to reverse bias each power-group thyristor valve after it has been commutated off, there is an unavoidable delay between when a power-group is commanded to turn-off its thyristor, and when it is actually available to generate a voltage, as discussed in Section. 6.4.1. This leads to an interesting control challenge in implementing a power-group augmented converter. To be able to meet the stack voltage reference the PGCC must be able to predict what the stack voltage demand will be ahead of time, and keep sufficient level of active power-groups. This prediction must look-ahead by at least the power-group hold-off time in order to allow power-groups sufficient time to make themselves available to generate a voltage. When bypassing a power-group by turning on a thyristor valve, the PGCC must also ensure that this action will not cause a subsequent shortfall voltage.

7.2 Power-Group Voltage Levels & Voltage Margins

To determine which power-groups are used to generate a voltage output, and so are kept active, the controller maintains a rank ordered list of the power-groups. The ordering of this rank is controlled by the power-group voltage balancing mechanism described in Section. 7.7. The voltage of a power-group k is denoted V_{PG_k}, and is defined as the sum of its sub-module voltages. For a power-group composed of full-bridge sub-modules it defines the maximum positive or negative voltage that the power-group can generate.

$$V_{PG_k} = \sum_{n=1}^{N_{SM_{PG}}} V_{SM_{k_n}} \tag{7.1}$$

The controller that has been developed to manage the timing of the turn-on and turn-off control of each power-group thyristor is based upon the concepts of voltage levels and voltage margins that will now be introduced. To generate the requested stack voltage from the current controller power-groups are deployed in order starting with the lowest ranked power-group. When the first power-group has fully deployed (i.e. all of its sub-modules are generating a voltage output) the next power-group is deployed, and so on. The voltage level of a power-group is the minimum requested stack voltage from the current controller, that will just cause a power-group to be set to generate its full voltage capability (i.e insert of all of sub-modules).

The voltage level of a power-group can be defined as the sum of the voltages of the power-groups which are lower in insertion rank, plus that power-groups voltage, as given in (7.2).

$$V_{level_k} = \sum_{n=1}^{k} V_{PG_{ranked_k}} \tag{7.2}$$

If the stack voltage is below a power-groups voltage level then the power-group is either generating zero-volts or an intermediate voltage below its full voltage capability. This voltage level concept is illustrated in the first sub-plot of Fig. 7.2.

The voltage level of a power-group will vary over time due to two factors. Firstly due to

energy deviation of the sub-modules within the arm, causing the voltage of each power-group to vary. Secondly due to changes in the power-group insertion rank, controlled by the power-group voltage balancing mechanism. When the power-group insertion rank changes the voltage level of a power-group tends to go through a sharp increase or decrease. One example of this occurs just after t=0.01 s in Fig. 7.2.

The voltage margin of a power-group is given by the absolute value of the stack voltage, V_{stack}, with the power-groups voltage level and voltage subtracted, as given in (eq:Vmargin).

$$V_{margin_k} = |V_{stack}| - V_{level_k} - V_{PG_k} \tag{7.3}$$

It is used as a measure of how far away, in terms of requested stack voltage, a power-group is from being used to generate part of the overall stack voltage waveform. The voltage margin of a power-group is shown in the second sub-plot of Fig. 7.2. A voltage margin of zero corresponds to a point where the power-group is just about to be used to contribute to voltage generation. If the voltage margin is negative then the power-group is generating zero-volts. If the margin is positive but below the full available voltage within the power-group then the power-group is generating an intermediate voltage using some of its sub-modules. An example of intermediate voltage generation occurs at this occurs at t=0.046 s in Fig. 7.2. If the power-groups voltage margin is above the available voltage within the power-group then it is generating its maximum available voltage.

The voltage margins of each power-group are the primary means of deciding when a power-group is allowed bypass itself by using its thyristor valve, and when a turn-off command to a power-group with a conducting thyristor is sent.

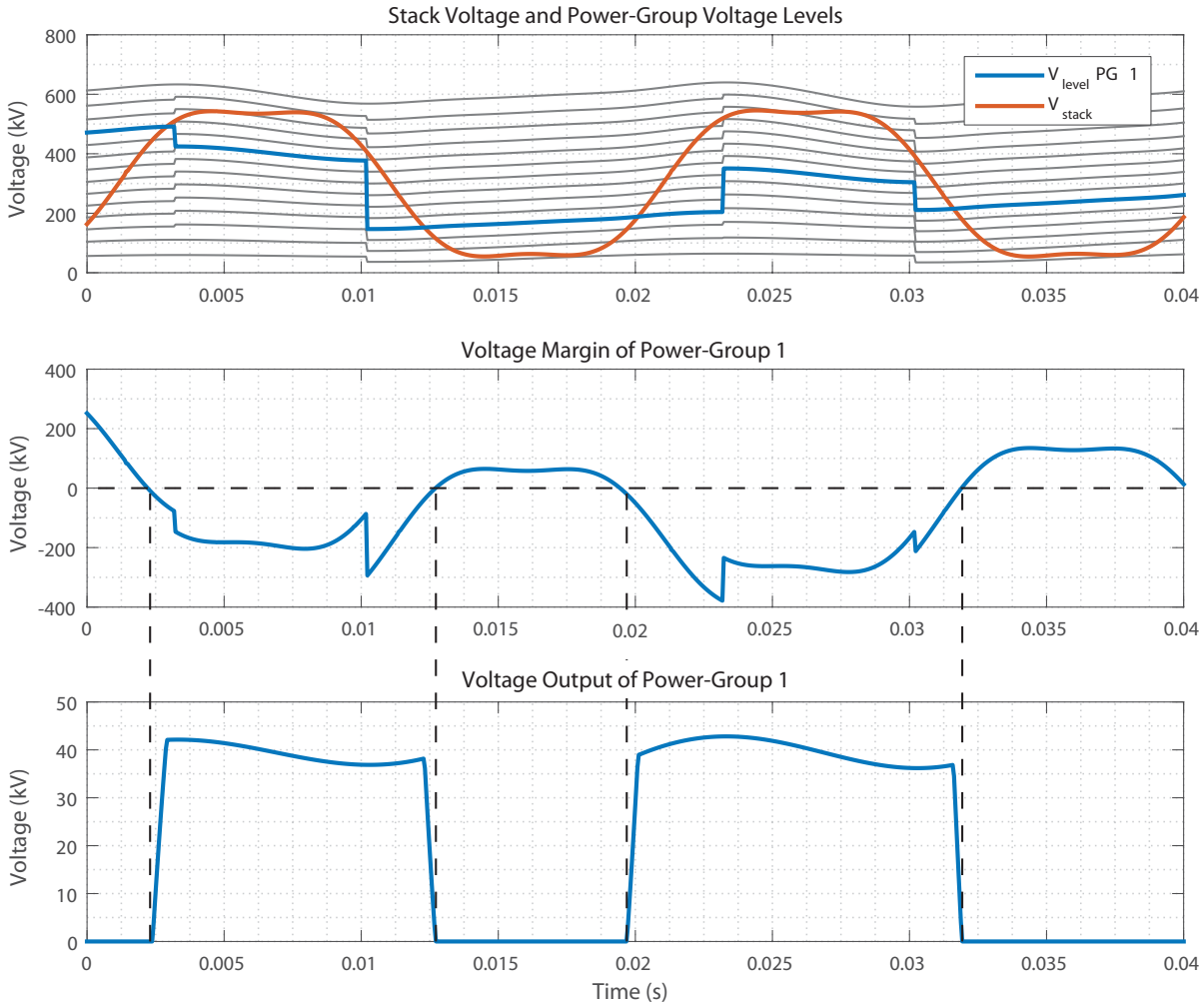


Figure 7.3: Illustration of the concept of voltage levels and voltage margins within a power-group augmented modular multilevel converter. Power-group voltage margin zero crossings and associated change in voltage output are shown using dashed lines.

7.3 Look-Ahead Voltage Margin Estimation

As discussed in Section 7.2, in order to properly manage the turn-on and turn-off logic of the power-group thyristors, some forward looking prediction of the stack voltage demand must be made. This look-ahead estimate is used as the basis for calculating:

- If a power-group's thyristor may be fired without causing the converter to run out of voltage.
- The right time for a power-groups to go through the turn-off process in order to meet any future voltage demand.

To be effective, this look-ahead horizon needs to be at least the length of the thyristor hold-off time.

The use of a single look-ahead period, advanced in time slightly beyond the thyristor hold-off time was tried. This was found to be ineffective for some converter topologies, particularly those that have sharp transitions in the stack voltage waveform. For this reason a look-ahead estimate for each controller time-step up to the look-ahead horizon, is calculated and used within the PGCC. This is illustrated in Fig. 7.4.

In the PGCC, each power-group's voltage-level and voltage margin is calculated at each forward point within the look-ahead horizon. This results in voltage-levels and voltage margins that are $N_{PG} \times N_d$ matrices, where N_{PG} is the number of power-groups in the arm, and N_d is the number of controller time-steps within the look-ahead horizon. The first row each matrix represents the instantaneous values of each signal, whilst each subsequent row is an estimate of that value advanced by one time-step.

Setting this look-ahead horizon to be slightly longer than the power-group hold-off time was found to give acceptable results. Using the look-ahead voltage margins of each power-group allows the PGCC to predict when a power-group will be required to generate a voltage, with enough time available for the power-group to go through the turn-off process.

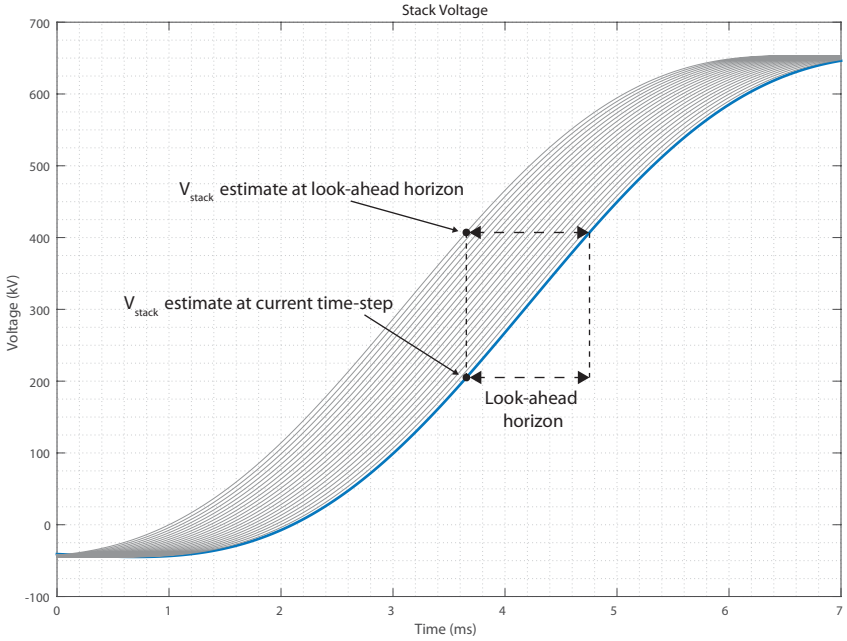


Figure 7.4: Estimated look-ahead stack voltages in increments of the controller time-step up to the look-ahead horizon

In order to calculate the voltage levels and voltage margins of a power-group at a point ahead in time, the power-group rank index at that point must be known. For this reason the insertion rank index of the power-groups for each time-step within the look-ahead horizon needs to be decided in advance. This leads to an interesting challenge in implementing effective voltage balancing between power-groups. The method that has been adopted for calculating the advance insertion rank indexes is detailed in Section.7.7.

7.4 Power-Group Thyristor On/Off Logic

The *Power-Group Thyristor On/Off Logic* sub-system controls which power-groups should use their thyristor to bypass themselves, and which power-groups must be kept active and available to generate a voltage upon command. The logical output of this controller is passed to the *Power-Group On/Off Controller*, which controls the actual thyristor turn-on and turn-off

processes. Its operation is based upon a series of logic conditions based on each power-groups voltage margins. A power-group may set its voltage output to zero and bypass itself by turning on its thyristor if all of the following conditions are met:

- Its voltage margin is above the *turn-on margin* threshold across the entire look-ahead horizon. When the power-groups voltage margin is sufficiently above zero, the PGCC can be confident the power-group will not be required to generate a voltage and so its thyristor may be used. A *turn-on margin* of 10% of the DC bus voltage was found to give good results.

- The magnitude of arm current is above a threshold value. This prevents the thyristor from being fired at times when the arm current is about to go through the zero crossing, which would cause the current to naturally commutate into the parallel sub-module stack anyway.

A power-group is set to turn off it's thyristor if any of the following conditions are met:

- Its voltage margin falls below the *turn-off margin* at any point across the look-ahead horizon. This indicates that the power-group will be required to generate a voltage.

- The arm current falls below the arm current turn-off threshold. This indicates that the arm current may be about to pass through zero, and so will be commutated off naturally.

- It receives a turn-off signal from the fault detection subsystem, detailed in Section. 7.10.

The look-ahead voltage margin for a power-group within a power-group augmented converter is shown in Fig. 7.5. When the power-groups voltage margins are positive it is not being used for voltage generation and so can make use of its thyristor. At $t \approx 0.075s$ the voltage margin at the look-ahead horizon goes negative, which indicates that the power-group will soon be used to generate a voltage. The power-group goes through the thyristor turn-off process and makes itself available to generate a voltage.

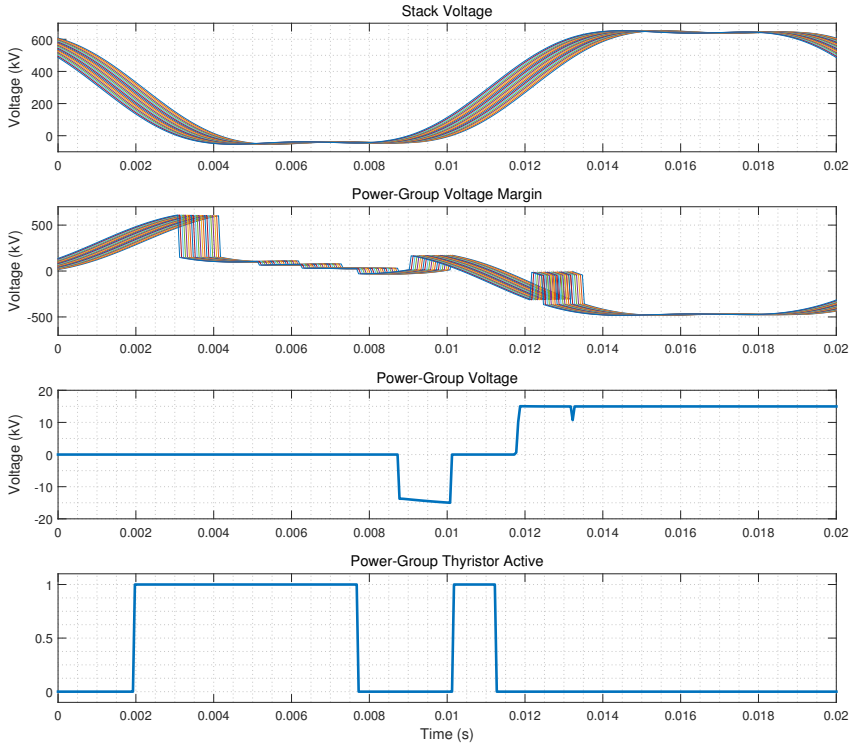


Figure 7.5: Voltage Margin Calculation Across the Look-Ahead Horizon

7.4.1 Availability Flag

In the PGCC each power-group is assigned an availability flag, denoted by α, that indicates whether a power-group is available to generate a voltage or not. A value of 1 indicates that a power-group is available, a value of 0 indicates that the power-group either has a conducting thyristor, or is undergoing either the turn-on or turn-off process. The availability flag is used to ensure power-groups that have conducting thyristors are not assigned a voltage reference, and also to determine the amount of available voltage within the converter. The availability indices are passed to the *Power-Group Voltage Assignation* system, detailed in Section. 7.6, which uses it to determine which power-groups it can assign a voltage to.

Separate availability flags are used for positive and negative voltage capability, denoted α^+ and α^-, respectively. This is done to account for the fact that the power-group should be able

to generate its full voltage as long as it keeps the thyristor which was active reverse biased.

The positive and negative available voltage within the stack can then be given by (7.4) and (7.5), respectively.

$$V_{avail}^{-} = \sum_{k=1}^{N_{PG}} \alpha^{+} V_{PG_k} \tag{7.4}$$

$$V_{avail}^{-} = -1 \times \sum_{k=1}^{N_{PG}} \alpha^{-} V_{PG_k} \tag{7.5}$$

This leads to an asymmetry in how quickly a power-group can regain its voltage generation capability which depends on whether the arm current was flowing through the upwards or downwards facing thyristor valve. The timings of when this flags are set to one or zero are detailed in the next section.

An example simulation of a power-group augmented Modular Multilevel Converter is shown in Fig. 7.6. When the arm current is positive the converter regains positive voltage faster than negative voltage. The inverse effect is seen when the arm current is negative.

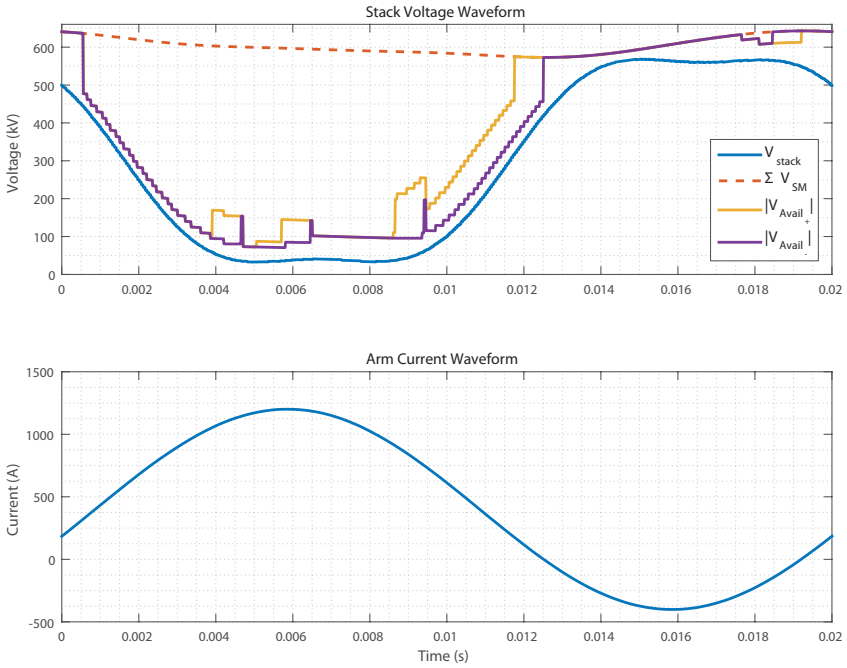


Figure 7.6: Positive and negative voltage capability asymmetry in a power-group augmented modular multilevel converter

7.5 Power-Group Thyristor On/Off Controller

This sub-system receives the logical command to from the *Power-Group On/Off Logic* which indicates whether a power-groups thyristor may be fired, or if a conducting thyristor should be turned off. When receiving a logical command that goes high, this sub-system implements the thyristor turn-on procedure detailed in Section. 6.4.1. When this logical command goes low again this sub-system implements the power-group thyristor turn-off procedure. This sub-system also control the availability flags for each power-group.

The overall thyristor turn-on and turn-off procedure is illustrated in Fig. 7.7. At the start of the figure the power-group thyristor valve is off and both the positive and negative availability indices are set to 1, allowing the power-group to be used to generate any voltage from its full negative to full positive voltage output capability. When the *Power-Group Thyristor On/Off Logic* subsystem detects that all conditions for allowing the thyristor to be fired are met, the

power-group on/off logic then goes high, indicating that the power-groups thyristor may be fired. At the same time both availability flags are set to zero. This prevents the *Power-Group Voltage Assignation* system from assigning the power-group a voltage reference. The *Power-Group Thyristor On/Off Controller* then directly sends a command to one sub-module within the power-group, discharging it so that the correct difference voltage can be achieved when the thyristor valve needs to be commutated off. Once this is achieved the thyristor valve is sent a firing pulse and begins conducting.

When the *Power-Group Thyristor On/Off Logic* subsystem detects a condition that causes a thyristor turn-off event, the power-group on/off logic then goes low. The *Power-Group Thyristor On/Off Controller* directly sends commands to the two sub-modules within the power-group that are being used to generate the correct difference voltage. This difference voltage is held for a period t_{diff}, commutating the thyristor valve. After this period either the positive or negative (depending on whether the upwards or downwards facing thyristor valve was conducting) voltage availability flag is set to one, allowing the power-group to be used for unipolar voltage generation. A minimum voltage command, V_{MinV}, is sent to the *Power-Group Voltage Assignation* system, to ensure the thyristor valve remains reverse biased for t_{Rev}, the remainder of the hold-off time. When the hold-off period expires, the thyristor turn-off process has completed. Both voltage availability flags are set to one and the minimum voltage command is set to zero. The power-group is then available to generate its full voltage in either polarity.

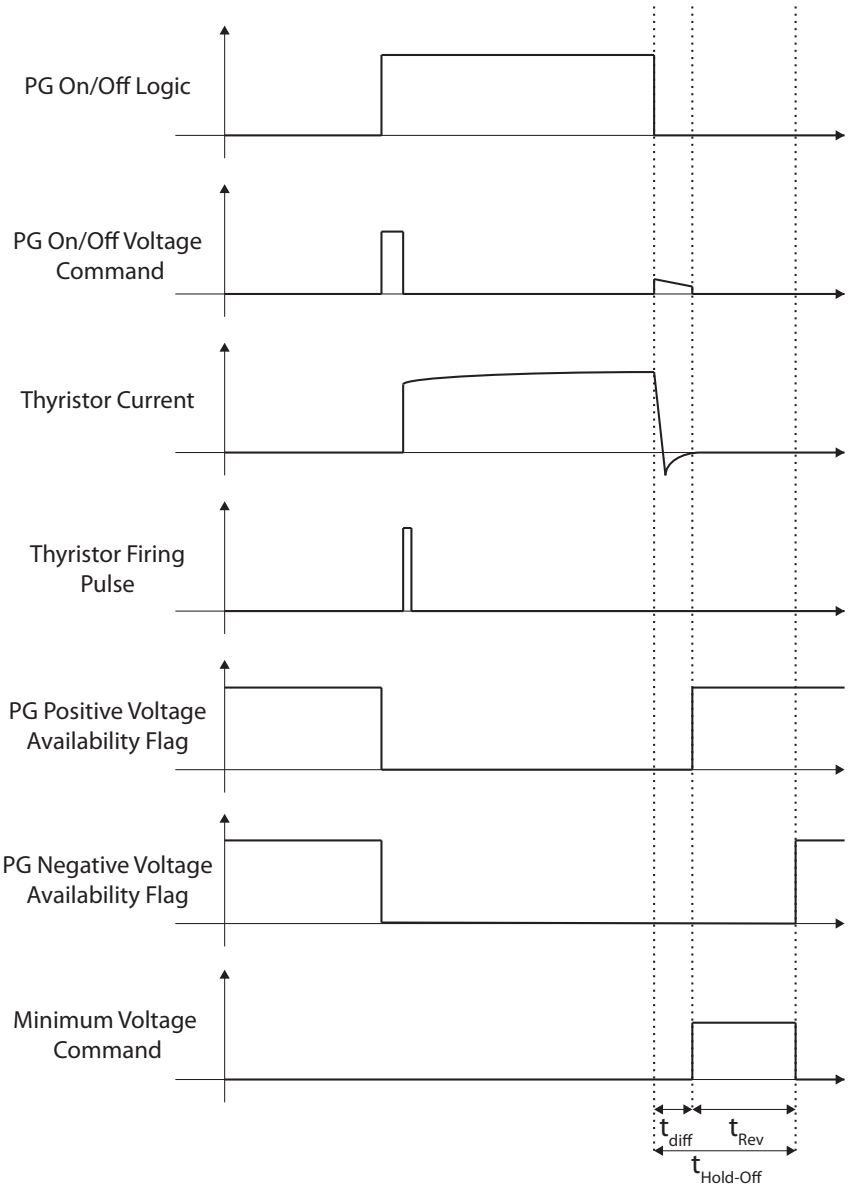


Figure 7.7: Overall power-group turn-on and turn-off process

7.6 Power-Group Voltage Assignation

This sub-system converts the stack voltage reference from the converter current controller, into individual voltage references for each power-group within the converters arm. This system has been developed with the requirement that no power-group which has an conducting thyristor can be assigned a voltage reference. It also ensures that a power-group is held reverse biased to a minimum voltage level, V_{MinV}, during the thyristor turn-off process.

Power-groups which are going through either the active discharge of a sub-module at thyristor turn-on or the differential voltage stage of the turn-off process are sent direct commands from the *Power-Group Thyristor On/Off Controller*, bypassing the voltage assignation system. If this was ignored in the power-group voltage assignation stage, the voltage actually generated by the arm would have an error corresponding to the sum power-group turn-on/turn-off voltages. To compensate for this a feed-forward signal ($V_{OffComp}$), corresponding to the sum of the turn-on/turn-off voltage, is subtracted from the stack voltage reference (V_s) to get (V_{stack}). In addition to this the sum minimum voltage level is also subtracted from the stack voltage reference, this voltage is added to each power-groups reference at the end of the assignation process. The reference voltage, V_{ref}, which is to be divided up between power-groups is given as in (7.6).

$$V_{ref} = V_s - V_{OffComp} - \sum_{k=1}^{n} V_{MinV_k} \tag{7.6}$$

The *Power-Group On/Off Controller* assigns each power-group sub-module a Minimum Off-Voltage, (V_{MinV}), which ensures a power-group keeps its thyristor reverse biased to a minimum voltage level during the thyristor turn-off procedure. In this subsystem the Minimum Off-Voltage is then subtracted from each power-group's measured voltage and multiplied by the positive and negative availability indices to get (7.7) and (7.8). These values represent the maximum positive and negative voltages available within each power-group which can be contributed in order to meet V_{ref}.

$$V_{PGavail_{+_k}} = (V_{PG_k} - |MinV_k|) \times \alpha_{+_k} \tag{7.7}$$

$$V_{PGavail_{-_k}} = (V_{PG_k} - |MinV_k|) \times \alpha_{-_k} \tag{7.8}$$

The value of $V_{PGavail}$ which is then used in the voltage assignation process is chosen as in (7.9), depending on the polarity of V_{ref}.

$$V_{PGavail_k} = \begin{cases} V_{PGavail_{+_k}} & \text{if } V_{ref} \geq 0 \\ V_{PGavail_{-_k}} & \text{if } V_{ref} < 0 \end{cases} \tag{7.9}$$

The values of $V_{PGavail}$ are sorted by the instantaneous insertion index ($Rank_{inst}$), which is detailed in Section 7.7.1, to get $V_{PGavail_{ranked}}$. The voltage levels and margins of this sorted list of power-group voltages are then calculated. The power-groups are then assigned voltage references as in (7.10)

$$V_{PG_{rankedref_k}} = \begin{cases} V_{PGavail_{ranked_k}} \times sgn(V_{ref}) & \text{if } V_{ref} > V_{PGlevel_{ranked_k}} \\ 0 & \text{otherwise} \end{cases} \tag{7.10}$$

The last power-group in the sorted list that has an available voltage, but which has not been assigned a voltage reference (denoted by k_{last}) is then assigned a voltage reference as in (7.11).

$$V_{PG_{ref_{k_{last}}}} = (\left|V_{ref}\right| - sumn = 1^{k_{last}-1} V_{PG_{rankedref_k}}) \times sgn(V_{ref}) \tag{7.11}$$

The voltage references for each power-group are then unsorted by the insertion rank. The values of V_{MinV} are then added to each power-groups assigned voltage reference. This ensures that each power-group achieves at least this value, ensuring that any thyristors going through the turn-off process are kept reverse-biased.

7.7 Power-Group Voltage Balancing Mechanism

Power-group voltage balancing presents a particular challenge. In a non-augmented multilevel converter a sub-module that is generating a voltage and has become under or over-charged can swapped with any other sub-module within the stack that is not generating a voltage. This means the voltage deviation of the sub-modules from each other can be limited by relatively simple voltage balancing algorithms.

In power-group applications, voltage balancing is more difficult due to the turn-off process that power-groups with an active thyristor must go through. This means only the power-groups that do not have conducting thyristors, or are not under-going the turn-off process, can be readily swapped to limit the voltage deviation.

A sorting algorithm is a common method of limiting the voltage deviation of sub-modules from each other in modular converters. Each sub-module is ranked according to its capacitor voltage. The insertion rank is determined based on either ascending or descending voltage depending whether the arm is generating or absorbing power. When a voltage is to be generated, the low-level control uses the sub-module with the highest insertion rank, and then so on, until then voltage reference is achieved.

Two separate insertion rank indexes are used within the PGCC. The Instantaneous Index ($Rank_{inst}$) is passed to the *Power-Group Voltage Assignation* sub-system, and is used to decide in what order power-groups are to be inserted in order to generate the requested voltage demand from the current controller. The Look-Ahead Index ($Rank_{LA}$) is used to calculate the voltage margins of each power-group in order to drive the power-group turn-on and turn-off logic.

7.7.1 Power-Group Instantaneous Voltage Balancing

This subsystem generates the instantaneous insertion index ($Rank_{inst}$) used by the *Power-Group Voltage Assignation* system. The turn-on/off control detailed in Section. 7.4 is designed to maintain the available voltage within the arm above the instantaneous stack voltage demand from the current controller. This means that at all times the PGCC will aim to keep more

power-groups active than are required to generate the requested stack voltage.

As the PGCC uses a separate insertion rank to control the voltage margin calculation, the instantaneous insertion index can be freely updated without causing any unwanted thyristor turn-on or turn-off events. Because the voltage assignation system also effectively ignores power-groups that are bypassed, a rotation of the instantaneous insertion index has the effective result of only re-sorting the power-groups are active. This was found to be critical in reducing the voltage deviation of the power-groups from each other, and in preventing large over-voltage events.

Rotations of the instantaneous insertion rank is set to trigger when:

- A power-group crosses an over-voltage threshold.
- A power-group cross an under-voltage threshold.
- The instantaneous power of the arm crossed through zero.

This balancing mechanism is illustrated in Fig. 7.8, with the trigger for over/under voltage events shown. Power-Groups that have are bypassed are shown in dashed grey, whilst active power-groups are shown in colour. When a power-group over-voltage event occurs, such as at t=0.0056 s, a rotation in the instantaneous insertion index is triggered. This re-sorts the active power-groups depending on the sign of the arm power. In this case the power-groups with lower voltages are now preferentially used to generate the voltage demand from the current controller.

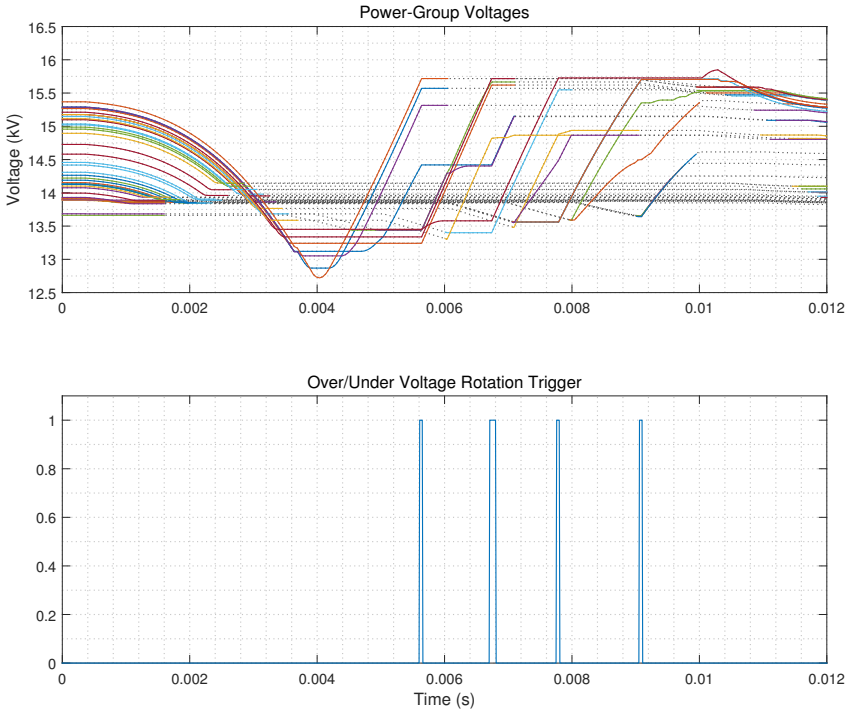


Figure 7.8: Instantaneous power-group voltage balancing.

7.7.1.1 Power-Group Look-Ahead Index Generation

This sub-system generates the power-group insertion index at the look-ahead horizon. This forward insertion-index from this sub-system is then passed through a tapped delay line, with a delay of N_d samples. This results in a $N_{PG} \times N_d$ array of insertion indices, with each being passed to the voltage level and margin calculation system.

The look-ahead index controls which power-groups will be available to generate a voltage, and which will be bypassed. For power-group voltage balancing purposes this subsystem must make intelligent decisions on what way to rank the power-groups. This presents a challenge as the voltage of a power-group can change by a large amount during the look-ahead horizon. This is particularly true for topologies with relatively small sub-module capacitors, such as the alternate arm converter. For example, a sub-module with a 4 mF capacitor operating in a converter with a peak arm current of 1200A could experience a change in voltage of approximately 300V,

assuming a 1 ms hold-off time. This is easily enough for a power-group to move from being one of the lowest charged power-groups, to being one of the highest charged power-group's within the stack, or vice-versa. For this reason, using the instantaneous power-group voltage measurements when calculating the insertion-index at the look-ahead horizon was found to result in occasional large over- or under-voltages.

To make effective decisions on how the power-groups should be ranked, a predictive estimate of what the power-group voltage would be at the look-ahead horizon was found to be required. The details of how this estimate is made is given in Section. 7.9. These predicted power-group voltages are used when generating the look-ahead insertion index and for use in calculating the look-ahead values of the voltage margins of each power-group. The predicted arm power at the look-ahead horizon is also used to decide if the lowest charged or highest charged power-groups are inserted preferentially.

Rotation Triggering A high number of power-group rotations is undesirable as it would reduce the utilisation of the power-group thyristors, and so reduce the hoped for efficiency gains. It has been found to be effective to trigger a rotation of the insertion index during the following events:

- The predicted power of the arm, at the look-ahead horizon, goes through a zero crossing.
- A predicted power-group voltage exceeds a defined over-voltage threshold.
- A predicted power-group voltage exceeds a defined under-voltage threshold.

Triggering on the arm power zero crossings was found to be effective, as at these points either the stack voltage or arm current will be zero, meaning power-groups can be rotated with little penalty as nearly all power-groups will be active. This is illustrated in Fig. 7.9.

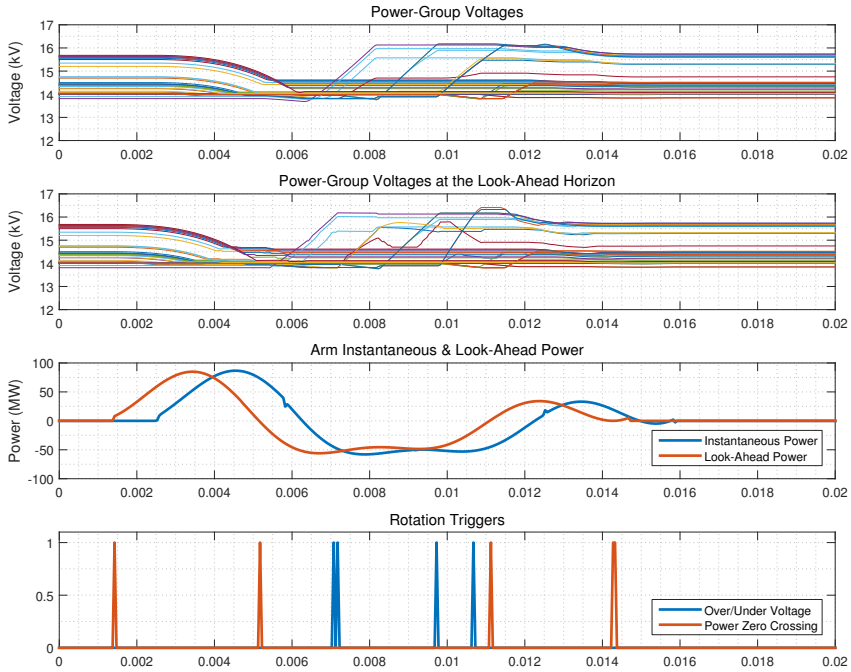


Figure 7.9: Power-group voltage balancing using look-ahead estimates of the power-group voltages and stack power.

7.8 Sub-Module Voltage Assignation

This sub-system converts the voltage reference for each power-group, received from the *Power-Group Voltage Assignation* system, into individual commands for the sub-modules within each power-group. In a similar manner to the power-group voltage assignation, this must be done so that the sub-modules within each power-group do not deviate in voltage from each other. To achieve this each power-group has its own sub-module insertion index ($Rank_{SM}$), which controls in what order sub-modules are used for voltage generation.

Due to the voltage assignation method adopted, power-groups spend most of their time generating either zero volts or their full available voltage. During these situations there is no scope to do voltage balancing as all sub-modules within the power-group are in the same state and can not be swapped. The sub-module assignation system is set to implement a rotation in the sub-module insertion rank of a power-group whenever that power-group is sent

an intermediate voltage command.

In practice the thyristor turn-on and turn-off process also contribute significantly to ensuring that the sub-modules within each power-group do not diverge from each other in voltage. This is illustrated in Fig. 7.10. In this example the power-group is assigned an intermediate voltage at 0.004 seconds, it can be seen how the sub-modules with the highest voltages are used to generate the voltage, discharging them towards, and then past the sub-modules which are lower in voltage. The power-group is turned off procedure at $t \approx 0.01s$, and it can be seen that the turn-off procedure acts to bring the sub-modules closer together in voltage.

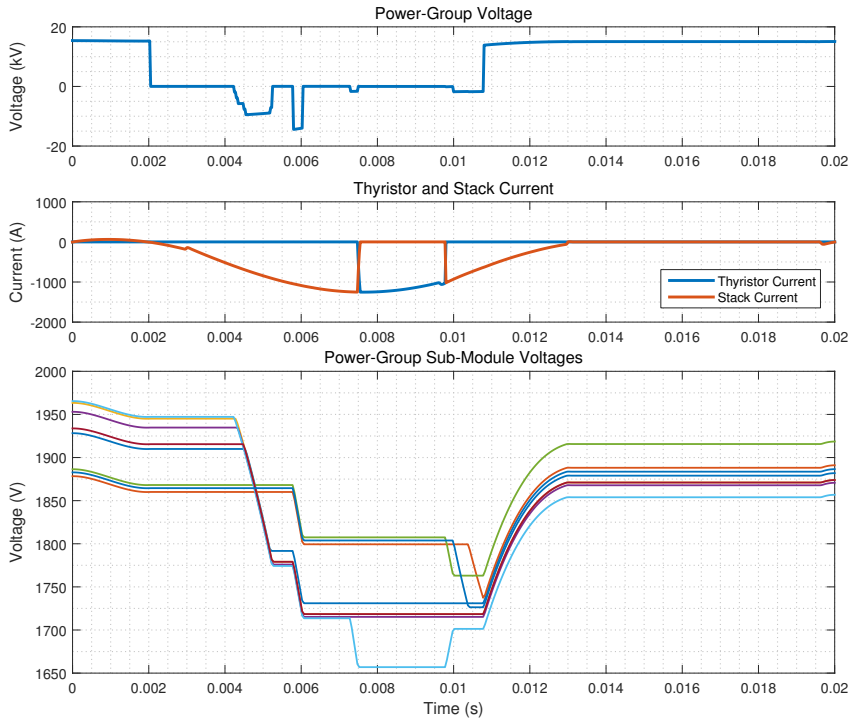


Figure 7.10: Sub-modules within a power-group.

7.9 Power-Group Look-Ahead Voltage Estimation

Because of the relatively long required hold-off time of the power-groups (in the region of 1 ms) , the voltage of power-group can change by a relatively large amount across the look-ahead horizon. This leads to a challenge in implementing effective power-group voltage balancing. The solution that has been developed to solve this problem is based on a predictive method which provides an estimate of what each power-group voltage will be at each time-step up to the look-ahead horizon, N_d time-steps ahead. The method is illustrated in the flowchart in Fig. 7.11.

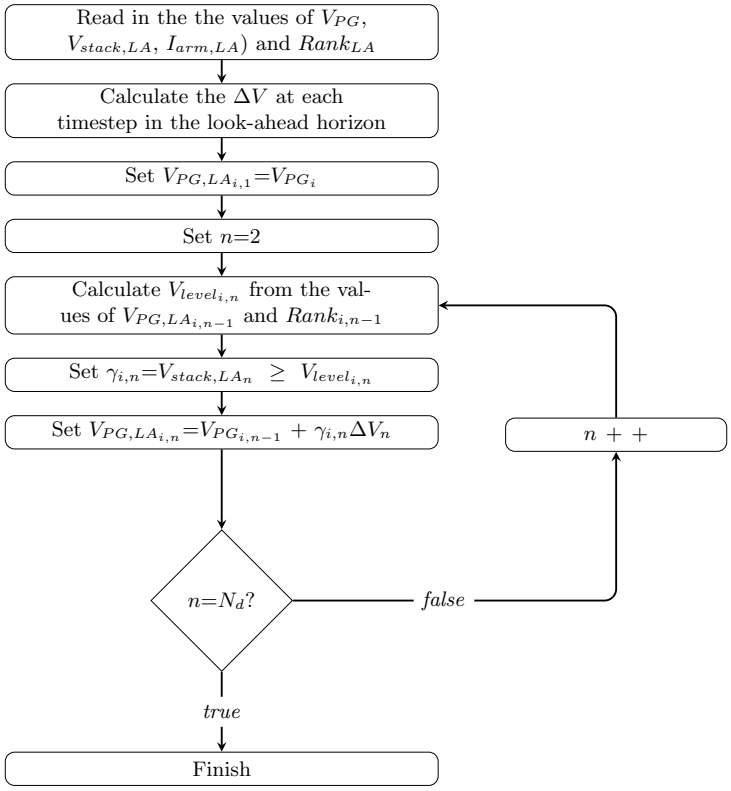


Figure 7.11: Power-group look-ahead voltage estimation process.

Firstly, the change in voltage that a power-group will experience if it used for voltage generation is calculated for each time-step, as given by (7.12).

$$\Delta V_n = \frac{I_{arm_n} T_{step}}{C} \times sgn(V_n) \tag{7.12}$$

The power-groups are ranked according to the insertion rank at that time-step, and then voltage level (V_{level}) of each power-group is calculated. Power-groups with negative voltage levels have a logical index (γ) of one assigned to them, and power-groups with a positive voltage level have a logical index of zero. The estimated voltage of each power-group at that time-step is then calculated by (7.13).

$$V_{PG_{k,n}} = V_{PG_{k,n-1}} + \gamma_n \Delta V_n \tag{7.13}$$

The time-step is then incremented forwards, and the process repeated until N_d time-steps have been processed.

Fig. 7.12 is an illustration of the estimated look-ahead and actual power-group voltages in a power-group augmented MMC. The look-ahead value gives a generally acceptable estimate of the power-groups voltage. Some discrepancies are seen, these are likely to be because of changes in the instantaneous voltage insertion index, causing the effective rank of a power-group to differ from the look-ahead value. Overall the method gives a good estimate of when a power-group will breach either its over or under-voltage limits. This allows for effective triggering of power-group rotations in advance of these occurrences.

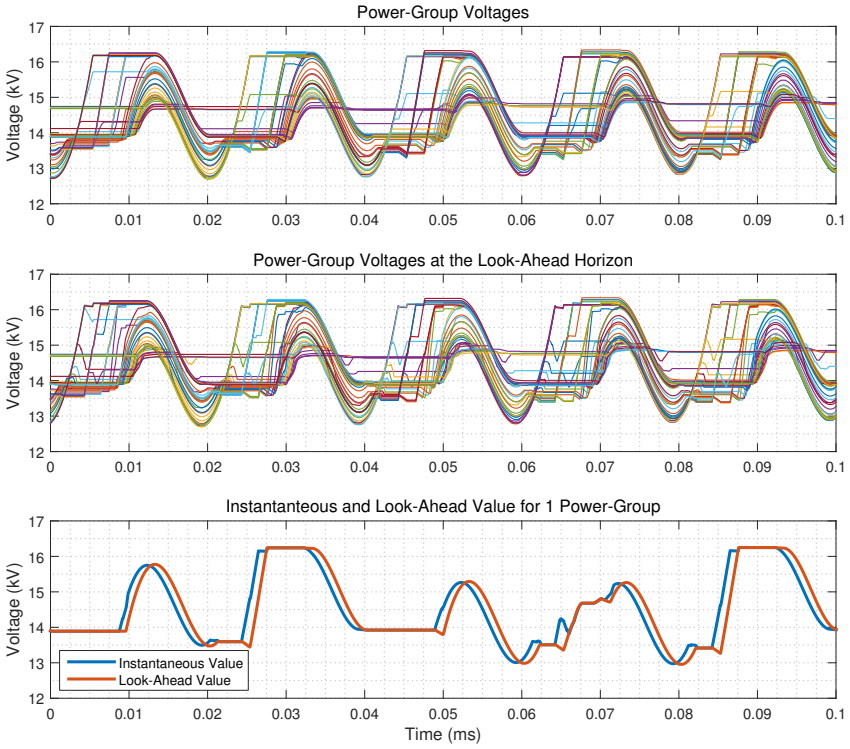


Figure 7.12: Power-group look-ahead voltage estimation in an augmented MMC.

7.10 Fast Fault Detection

In fault scenarios the converter may have to make sudden set-point adjustments, and respond to rapid changes in either of the AC or DC side voltage waveform. In such scenarios it will be important to turn-off all power-group thyristors and regain the maximum voltage capability of each converter arm as soon as possible. A fast fault detection method is proposed to quickly detect fault events send a turn-off commands to any power-groups that have active thyristors. The detection method is illustrated in Fig. 7.13.

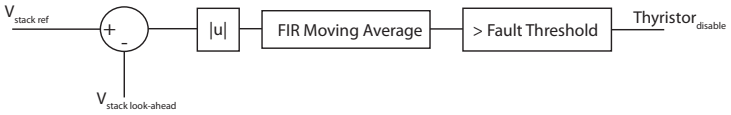


Figure 7.13: Fast fault detection method.

The instantaneous stack voltage demand from the current controller is compared to the estimated value of what the stack voltage should be at the converter's PQ set-point. If the absolute value of this filtered signal exceeds a threshold value, a power-group disable signal is sent to the rest of the PGCC. The fault detection block also disables the use of the power-group thyristors if any of the converter's energy levels, DC voltage, or AC voltage are outside of tolerance bands for these variables. As false detection carries only the penalty of a temporary decrease in the converter;s efficiency, due to the power-group thyristors being disabled, this method can be made quite sensitive, resulting in the power-group thyristors being disabled very shortly after a fault.

Fig. 7.14 shows the response of the proposed fast fault detection method to a fault situation in a power-group augmented converter. The method successfully rejects the short-sharp transients in the stack voltage waveform seen in the converter's stack voltage before the fault. This is important for converter topologies such as the Alternate Arm Converter, which must be able to control sharp transitions in the arm current waveform, and so can expect such spikes in the stack voltage waveform. When the fault occurs it is quickly detected, setting the thyristor enable signal to zero.

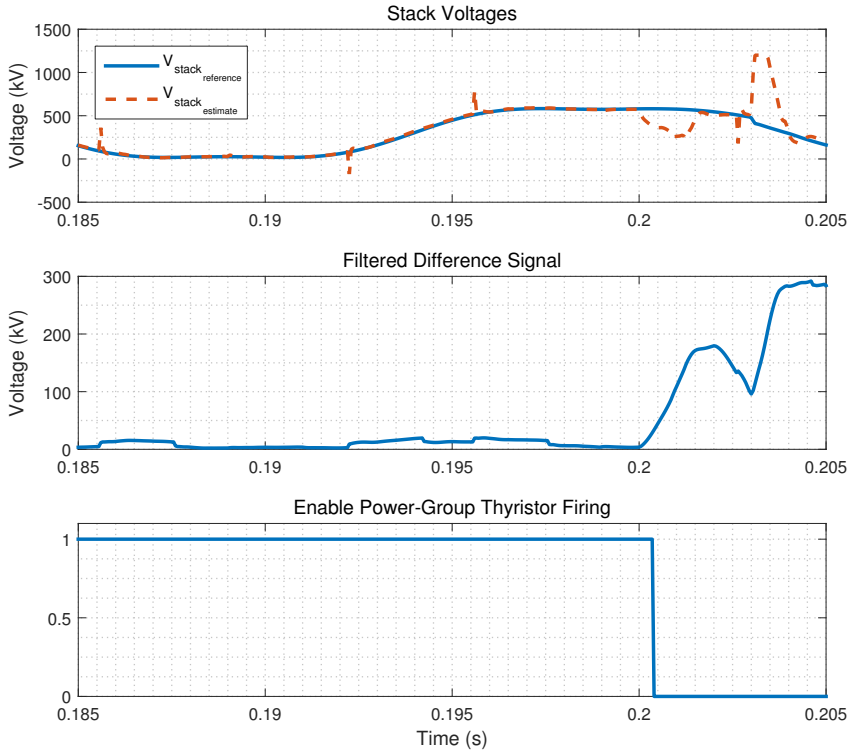


Figure 7.14: Fast fault detection method response to an AC side fault.

7.11 Chapter Conclusion

This chapter has detailed the working principles of the Power-Group Centralised Controller (PGCC) which has been developed to over-come the main control issues that the power-group concept introduces. These issues stem from the requirement for each power-group to have a significant hold-off time after its thyristor is disabled, and before it is able to generate a voltage output. This limits how fast the controller can re-gain the voltage capability of a power-group which is utilising its thyristor to bypass itself.

The PGCC address this issues by using forward looking predictions of the voltage demand from the current controller, as well as forward estimates of the average sub-module voltage within each power-group. This enables it to make good utilisation of the thyristors within each power-group, while also keeping enough voltage capability within each stack of power-group to

retain proper current control while also limiting the deviation of the sub-modules to reasonable levels. A fault detection mechanism for quickly disabling the use of power-group thyristors has also been presented. The following chapter will investigate what converter topologies are most suitable for augmentation with power-groups.

8 Power-Groups: Converter Topologies

Chapter 6 introduced the concept of power-groups as a modular structure incorporating thyristors which could be used to improve the efficiency of any converter based upon the modular multilevel concept. The design and operation implications that constructing a modular converter out of such a structure were identified. In Chapter 7, a Power-Group Centralised Controller (PGCC) capable of dealing with the control implications that the power-group concept introduces was also presented.

The focus of this chapter is an investigation into what converter topologies are the most promising candidates for augmentation with power-groups. The topologies of interest within this chapter are the Modular Multilevel Converter (MMC) and the Extended Overlap Alternate Arm Converter (EO-AAC). The study of these two converter topologies led to a proposal for two variants based upon the EO-AAC, which make better utilisation of the power-group concept. Efficiency results for all converter types are estimated and compared with the base converter.

All converters were simulated at a scale of $\pm 300kV$ $900MW$. An emphasis is placed upon converters which are capable of riding through faults on the DC side. However it is recognised that non DC fault tolerant converters might also be augmented using the power-group concept.

8.1 Converter Modelling and Power-Loss

Simulating a full-switching model of a power-group augmented HVDC converter represents a significant challenge in achieving reasonable compilation and execution times. A converter operated at a DC bus of $\pm 300kV$, will have in the region of 240 separate power-groups, each

containing 8 sub-modules, a thyristor valve and a commutating inductance.

The solution that has been adopted is to use a combination of a Reduced Dynamic Model (RDM) of the majority of the arm, whereby most power-groups are represented by a controlled voltage source in series with one detailed power-group switching model. This allows the power-group thyristor turn-on and turn-off process to be verified using the switching model, while keeping the overall computational complexity low. The converter controller is not aware of which portion of the stack is represented by the RDM, and which is represented by the detailed power-group model.

The RDM that has been adopted keeps track of the voltage of each individual sub-module within the converter, rather than treating the entire arm as an averaged element. The voltage variation of each sub-module is calculated as depicted in Fig. 8.1. The voltage output of each sub-module is calculated by multiplying the sub-modules command by its capacitor voltage from the previous time-step. The energy exchange of each sub-module is then calculated by integrating the product of the arm current and the voltage output generated by each sub-module over each time-step. The voltage of the sub-module capacitor is then calculated based on its energy.

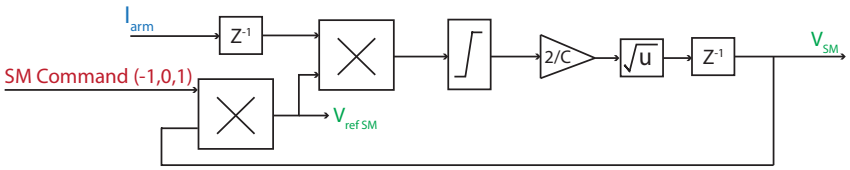


Figure 8.1: Sub-module voltage variation calculation.

The voltage outputs of each sub-module within a power-group are summed to get the voltage generated by each power-group. To limit the dV/dt across the thyristor valve the sub-modules must be inserted in a stepped manner, as discussed in Section. 6.4.2. This places a limit on how fast the converter can modulate its output voltage. To capture this in the simulation, the voltage outputs of each power-group are placed through a slew rate limiter. These slewed

power-group voltages are then summed to get the overall voltage reference for the arm.

The series valve of power-groups within the converter arm are represented by an ideal voltage source which is placed within a full-bridge arrangement, as shown in Fig. 8.2. The absolute of the overall voltage reference is passed to the controlled voltage source, the gates of the full-bridge are set to control the output voltage of the bridge to the correct polarity. This full-bridge arrangement is used to allow the blocking behaviour of the full-bridge sub-modules within the power-groups to be properly captured in simulation.

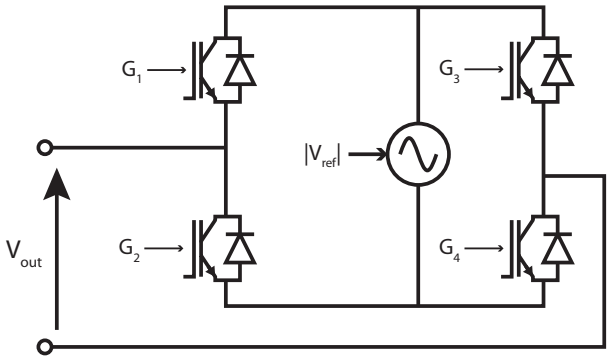


Figure 8.2: Reduced dynamic model of a stack of power-groups.

8.1.1 Power-Losses Estimates

IGBT losses within the converter studied are estimated using the methodology presented in Section. 4.1.2. Conduction losses within the thyristors follow the same method. For each case, efficiency estimates are made using device characteristics at junction temperatures of 125^oC.This may result in some slight over estimation of the conduction losses within the converters.

The values of the thyristor valve turn-off losses are taken from SPICE simulations presented in Section. 6.4.1.4. Turn-off losses are estimated as 2 J per thyristor valve, and are assumed to be independent of the magnitude of the anode current flowing through the thyristor prior to turn-off. This assumption is backed up by the results in Section. 6.4.1.4.

Turn-on losses may be extremely hard to estimate without a more detailed model of a thyris-

tor, which captures the forward voltage characteristic of the device during turn-on. Some manufacturers give data for turn-on losses, however these are assuming that the load currents only path is through the thyristor. In power-group applications the arm current has an alternate path through the stack of sub-module and will divide itself between depending on the lowest impedance path. For this reason turn-on losses in power-group applications may be expected to be very small. From discussion with Thyristor Valve specialists at GE, the thyristors have been assigned a turn-on loss of 2 J/kA.

The loss values for the snubber are taken from the SPICE modelling of the power-group snubber network performed in Section. 6.4.2. These simulation results gave loss values in the region of 0.1 J per sub-module switching event.

8.1.1.1 Power-Group Loss Modelling

Initial efficiency results were calculated using just the single detailed power-group within each arm. However, it was found that power-groups do not make completely even use of their thyristor, even over longer simulation times up to 2 seconds. Variations in the thyristor usage were found to be in the region of $\pm 20\%$.

For this reason calculating the power-losses using just a single power-group, which is modelled in detail was found to give un-reliable results, with the estimated efficiency of the converter varying by large amounts, depending on the thyristor usage of that one power-group within the arm.

The solution that has been adopted to solve this is to use a signal from the PGCC to indicate for each power-group whether the current is in either the sub-module path or thyristor path. The gate signals for the sub-modules are then used to map path the current takes through each IGBT in each sub-module. These signals are then passed as a vectorised input to the power-loss block described in Section. 4. This allows the losses within each semiconductor device within the entire converter arm to be calculated.

A comparison of the losses within a power-group using the detailed switching model, and the

losses using the mapped current is shown in Table. 8.1. The overall error between the losses calculated from the detailed method, and using the current mapped losses calculation is low, with the main difference being in the switching losses, which are estimated to be slightly higher in the current mapped method.

Table 8.1: Power-group power loss calculation method comparison.

Loss (W)	Detailed	Current Mapped	Error (%)
IGBT Conduction	9435	9424	0.12
IGBT Switching	3414	3637	6.53
Thyristor Conduction	1042	1043	0.1
Thyristor Turn-Off	540	540	0
Thyristor Turn-On	198.5	198.5	0
Snubber Loss	535	535	0
Overall Loss	15160	15380	1.45

8.2 Converter Comparison Methodology

This section describes the investigation into the efficiencies of several different converter topologies. The converters studied are based upon the MMC and the EO-AAC, though power-groups could also be used for any multilevel converter topology.

One of the metrics that has been devised for comparing power-group augmented converters is the thyristor utilisation ratio, (ϕ_{thy}) , which is introduced here. The thyristor utilisation ratio (ϕ_{thy}) is used as a measure of how much the thyristor path through each power-group is used relative to the path through the stack of sub-modules. This then gives a good measure of how suited a converter topology is to power-group augmentation. A high thyristor utilisation ratio indicates that most of the arm current flows through the thyristor path, making good usage of the power-group concept. The thyristor utilisation ratio can be calculated as in (8.1).

$$\phi_{thy} = \frac{\overline{|I_{thy}|}}{\overline{|I_{stack}|}} \tag{8.1}$$

In this study the efficiency of the converters will be compared at 6 different points on a P/Q envelope. Estimates at both inverting and rectifying operation are given at a 0.95 leading power-factor, 0.95 lagging power-factor and unity power-factor. AC and DC voltages are assumed to be at their nominal values.

The simulation and control variables which are common between all of the converter topologies in the next section are given in Table. 8.3. The thyristor *turn-on* and *turn-off margins* are used by the PGCC to control the thyristor turn-on and turn-off logic. The values given have been manually tuned to give good utilisation of the power-group thyristors. This was described in Section. 7.4. The power-group peak and minimum voltages are used as control inputs to the power-group voltage balancing mechanism, detailed in Section. 7.7.

Characteristic	**Value**
DC Voltage (kV)	± 300
Rated Power (MW)	900
Transformer Leakage Inductance (pu)	0.14
Thyristor Turn-On Margin	$0.1V_{DC}$
Thyristor Turn-Off Margin	$0.05V_{DC}$
Power-Group Peak Voltage (kV)	$16kV$
Power-Group Min Voltage (kV)	$12.5kV$

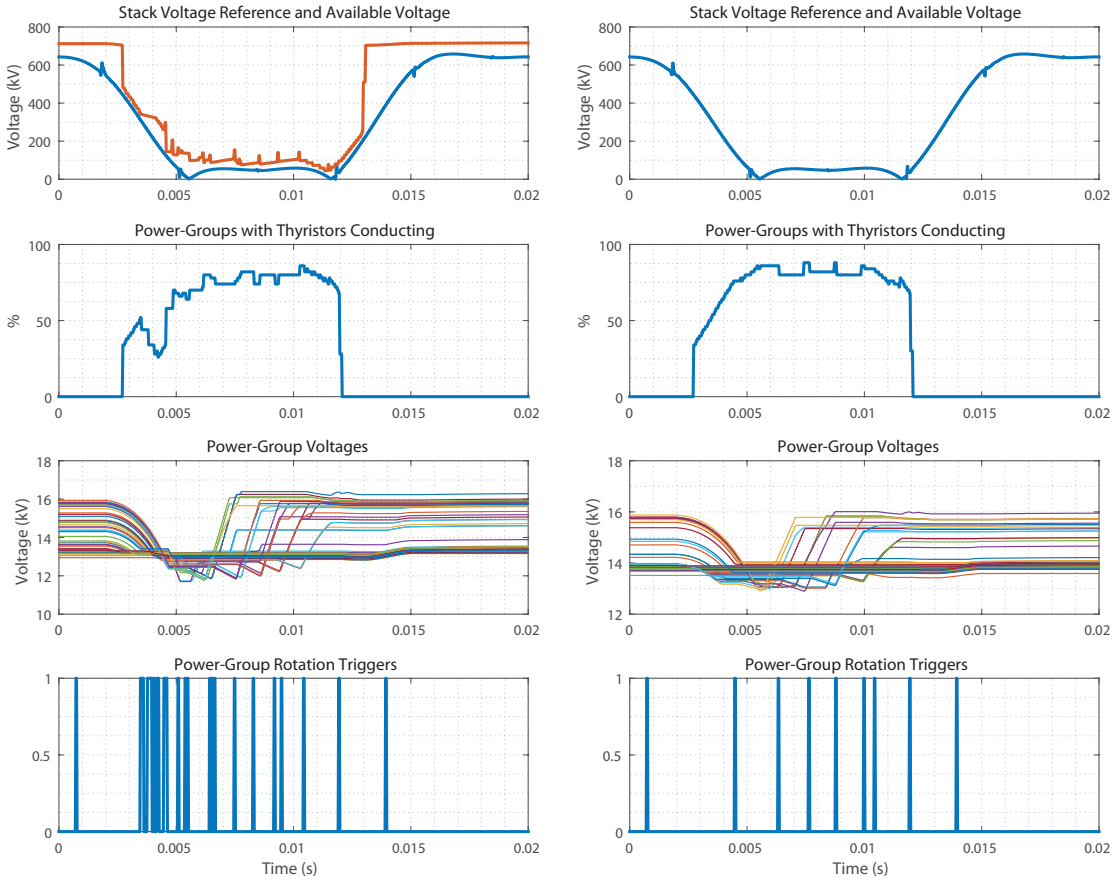
Table 8.2: Power-group augmented converters - common design elements.

8.2.1 Impact of Sub-Module Capacitor Size on Thyristor Utilisation and Efficiency

In non-augmented modular multilevel converters, the sizing of the sub-module capacitor is driven by the requirement to limit the sum ripple on the sub-module voltages, in order to prevent the converter from not having sufficient voltage capability, as well as the requirement to limit the

peak voltage that any sub-module experiences [49].

In power-group augmented converters another factor comes into play which is how the sub-module capacitor size impacts how often power-group voltage balancing rotations must take place in order to limit the deviation of power-group voltages from each other. Frequent rotations limit how long a power-group may keep its thyristor conducting before it is required to disable its thyristor and generate a voltage output. This is illustrated in Fig. 8.3 for power-group augmented converters operated with 12.5 kJ/MVA and 25 kJ/MVA of stored energy. In both simulations, the PGCC was set to maintain the maximum and minimum power-group voltages within the same limits. To achieve this, the converter with a nominal energy storage of 12.5 kJ/MVA, must use power-group rotations at a higher frequency.



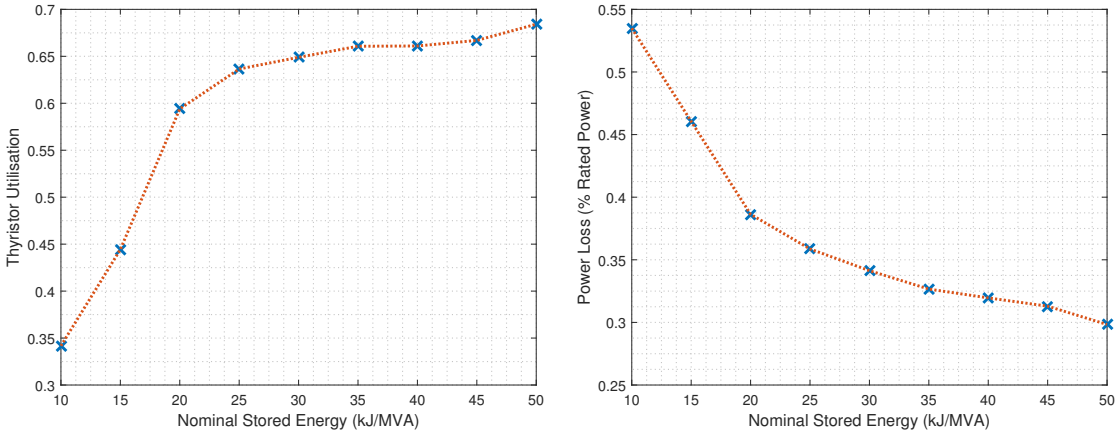
(a) 12.5 kJ/MVA nominal stored energy.

(b) 25 kJ/MVA nominal stored energy.

Figure 8.3: Impact of sub-module capacitor size on power-group thyristor usage in a power-group augmented converter.

The variation in the estimated power-losses and thyristor utilisation, with variation in the nominal stored energy, in a power-group augmented converter based upon the EO-AAC is shown in Fig. 8.4. It can be seen that with a lower amount of energy within the utilisation of the power-group thyristors is affected, with a subsequent impact on the power-losses within the converter.

The nominal energy levels within the converters examined within the next section have been set so that the energy storage within the converter is sufficient to make proper use of the power-groups. For converters based upon the MMC, this results in nominal energy levels of



(a) Thyristor utilisation.

(b) Converter losses

Figure 8.4: Impact of sub-module capacitor size on power-group thyristor usage.

35 kJ/MVA being used, this is in line with the expected energy storage requirement in a non-augmented MMC. For converters based upon the AAC, nominal energy levels in the region of 25 kJ/MVA were found to be required to ensure good thyristor utilisation. This is above the approximate 12.5 kJ/MVA storage requirement of a non augmented AAC [39]. It should be noted that some of the topologies based upon the AAC in the following section have stacks that are rated for higher voltage ratings, with resulting increases in the number of sub-modules, than the EO-AAC presented in Section 1.2.4. The increased energy storage requirement therefore does not directly correlate into an equivalently increased sub-module capacitor size.

8.3 Converter Efficiency Comparison

8.3.1 Augmented Modular Multilevel Converter

The first converter topology which will be explored as a candidate for augmentation is the Power-Group Full-Bridge Modular Multilevel Converter (A-MMC). The full-bridge variant of this topology is chosen as this will allow the proposed power-group turn-off method to be used. MMC variants that include a mixture of full and half-bridge sub-modules within each power-

group could also be considered, but are not included in this thesis.

The characteristics of the simulated converter are given in Table. 8.3.

Characteristic	**Value**
DC Voltage (kV)	±300
AC Voltage (kV)	490
DC Current (kA)	1.5
N. of sub-modules per PG	8
Voltage Rating of Stack (PU)	1
N. of power-groups per Valve	42
N. of sub-modules per Valve (GW)	336
Nom. Energy (kJ/MVA)	35
sub-module Capacitor Size (mF)	9.6
N. of IGBTS per Valve	1344
N. of Thyristors per Valve	252

Table 8.3: Augmented modular multilevel converter - specification.

The waveform of a single arm of the converter, when operating at 1 pu rated inverting power is shown in Fig. 8.5. During the peak of the arm current waveform the stack is mostly bypassed, which should result in a significant decrease in conduction losses. Because the MMC has continuous current conduction within the arms, there is current flowing through the stacks when the arm is generating close to its maximum voltage, when little to no power-groups are using their thyristor. When the stack voltage is at its peak the power-groups within the arm are nearly all conducting though the IGBT path.

A comparison of the calculated losses in this topology, in both its standard non-augmented configuration and its power-group augmented variant, is given in Table. 8.4. Significant reduction in the IGBT conduction losses within the augmented converter are seen. Switching losses remain relatively constant, with a slight increase in the augmented variant. The power-group augmented variant has additional losses caused by the power-group thyristor and snubber, however the additional losses by these elements are dominated by the reduction in IGBT conduction losses.

Loss estimates of the A-MMC at several outpoints of P/Q envelope are given in Table. 8.5.

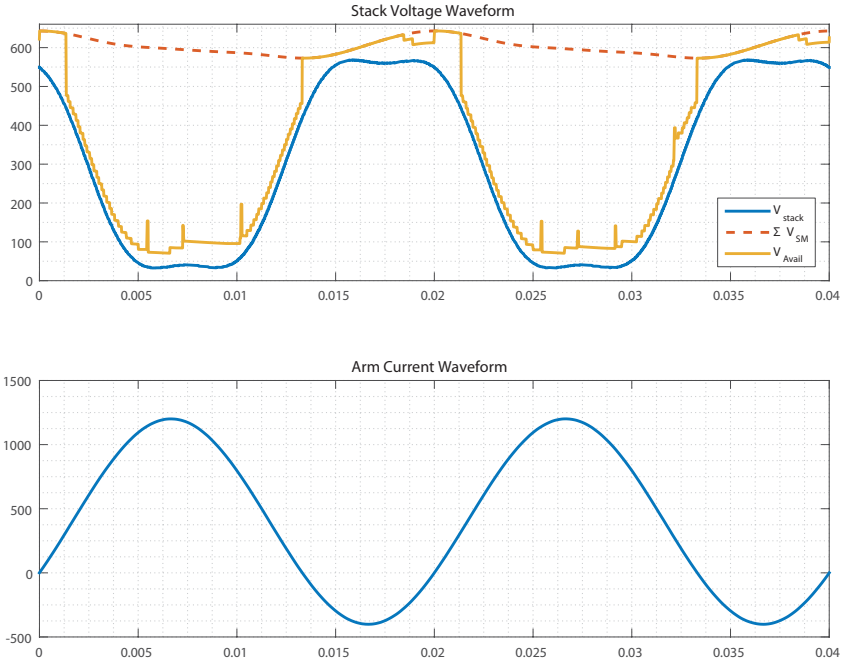


Figure 8.5: Power-group augmented modular multilevel converter operating at rated inverting power.

The converter exhibits only modest increases in power-losses when operating away from unity power-factor. The average thyristor utilisation factor is in the region of 0.5. The loss estimates for the A-MMC are relatively promising, indicating that power-groups may allow fault-tolerant converter with efficiencies close to the half-bridge MMC to be achieved.

Table 8.4: Comparison of augmented & non-augmented power losses at 1 pu inverting operation.

Loss Type (% Rated Power)	Non-Augmented	Augmented
IGBT Conduction	0.719	0.296
IGBT Switching	0.087	0.093
Thyristor Conduction	NA	0.045
Thyristor Turn-Off	NA	0.003
Thyristor Turn-On	NA	0.016
Snubber Loss	NA	0.005
Overall Loss	0.806	0.458

Table 8.5: A-MMC efficiency estimates (losses in % rated power).

P (pu)	1	1	1	-1	-1	-1
Q (pu)	0	0.3	-0.3	0	0.3	-0.3
Thyristor Utilisation	0.515	0.480	0.524	0.540	0.533	0.504
IGBT Conduction	0.296	0.339	0.305	0.283	0.307	0.324
IGBT Switching	0.093	0.094	0.103	0.084	0.093	0.098
Thyristor Conduction	0.045	0.044	0.047	0.047	0.048	0.045
Thyristor Turn-Off	0.003	0.003	0.004	0.004	0.004	0.004
Thyristor Turn-On	0.016	0.013	0.019	0.021	0.027	0.021
Snubber Loss	0.005	0.006	0.005	0.005	0.006	0.005
Overall Loss	0.458	0.499	0.483	0.443	0.484	0.499

8.3.2 Augmented Extended Overlap Alternate Arm Converter

In this section a power-group augmented variant of the Extended Overlap Alternate Arm Converter (EO-AAC), which is detailed in Section. 1.2.4, is considered. The specifications of the simulated converter are given in Table. 8.6.

The stack voltage and current waveform of this converter operating at 1 pu inverting power are shown in Fig. 8.6. Unlike the MMC, the stack voltage spends relatively little amount of time generating zero volts. This indicates that there is a reduced potential to use the thyristors within each power-group.

The loss comparison between the augmented and non-augmented variants of this topology are shown in Table. 8.7 . Some mild reduction in the conduction losses within the sub-modules

Table 8.6: Augmented extended overlap alternate arm converter - specification.

Characteristic	**Value**
DC Voltage (kV)	±300
AC Voltage (kV)	490
DC Current (kA)	1.5
N. of sub-modules per PG	8
Voltage Rating of Stack (PU)	$\frac{2}{3}$
Voltage Rating of Director Switch(PU)	$\frac{2}{3}$
N. of power-groups per Valve	28
N. of sub-modules per Valve	224
N. of IGBTs per Director Switch	203
Nom. Energy (kJ/MVA)	25
sub-module Capacitor Size (mF)	10.3
N. of IGBTS per Valve	1099
N. of Thyristors per Valve	168

is seen, however the amount is relatively low. A significant portion of the losses within the converter come from the director switch. This loss is not affected by use of power-groups within the converter arms. A hybrid power-group arrangement, containing a mix of director switches IGBTs and full-bridge sub-modules could be considered for this topology to further decrease the losses.

Table 8.7: Comparison of augmented & non-augmented EO-AAC power losses at 1 pu inverting operation

Loss Type (% Rated Power)	Non-Augmented	Augmented
IGBT Conduction	0.353	0.256
IGBT Switching	0.082	0.087
Dir. Switch Conduction	0.170	0.170
Dir. Switch Switching	0.001	0.001
Thyristor Conduction	NA	0.010
Thyristor Turn-Off	NA	0.002
Thyristor Turn-On	NA	0.033
Snubber Loss	NA	0.004
Overall Loss	0.605	0.563

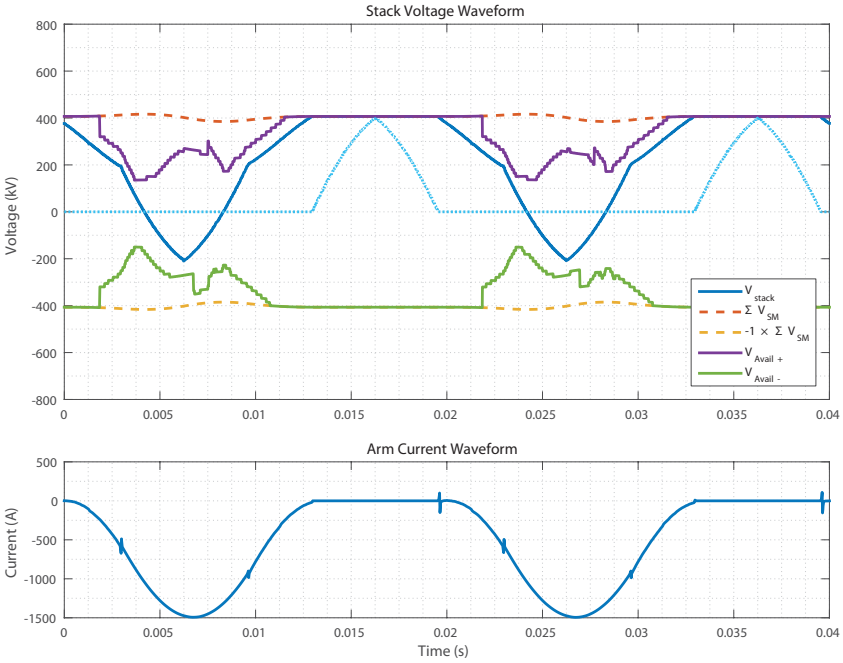


Figure 8.6: Power-group augmented extended overlap alternate arm converter operating at rated inverting power.

The estimated losses within the augmented EO-AAC at several set-points is given in Table. 8.8. The thyristor utilisation is low in comparison the augmented MMC, averaging at 0.23. The efficiencies in all cases are also below that of the A-MMC, indicating that the EO-AAC, in its standard arrangement is not an attractive candidate for power-group augmentation.

Table 8.8: EO-AAC efficiency estimates (losses in % rated power).

P (pu)	1	1	1	-1	-1	-1
Q (pu)	0	0.3	-0.3	0	0.3	-0.3
Thyristor Utilisation	0.263	0.197	0.345	0.381	0.335	0.344
IGBT Conduction	0.256	0.294	0.234	0.213	0.245	0.234
IGBT Switching	0.087	0.098	0.077	0.078	0.074	0.100
Dir. Switch Conduction	0.170	0.179	0.177	0.150	0.159	0.157
Dir. Switch Switching	0.001	0.001	0.001	0.000	0.000	0.001
Thyristor Conduction	0.010	0.008	0.014	0.015	0.014	0.014
Thyristor Turn-Off	0.002	0.002	0.002	0.002	0.002	0.002
Thyristor Turn-On	0.033	0.033	0.027	0.033	0.034	0.035
Snubber Loss	0.004	0.005	0.004	0.003	0.004	0.004
Overall Loss	0.563	0.620	0.536	0.494	0.532	0.548

8.3.3 Augmented Trapezoidal - Alternate Arm Converter

In the EO-AAC, the third harmonic voltage that has been imposed upon the converters voltage waveform was chosen as part of an optimisation to improve the efficiency of the converter. It does this by optimising the required ratio of director switches to full-bridge sub-modules within the arm, whilst still retaining the EO-AAC DC fault ride through capability [111].

The use of power-groups within the EO-AAC may change the result of this optimisation, as a power-group with an active thyristor will have significantly lower conduction losses than either a sub-module or director switch. For this reason an Alternate Arm Converter that operates using a a more traditional third harmonic voltage waveform imposed may be a desirable option. This converter topology has been named the Augmented Trapezoidal Alternate Arm Converter (AT-AAC), to reflect the use of power-groups, and the more standard third harmonic injection used.

As the zero sequence voltage is now subtractive from the AC voltage waveform, the peak voltage that the converter must generate is also reduced. This means the converter arms need an overall lower voltage rating. This may also bring some benefits in station layout due to the reduced isolation voltage requirement. The ratings of the simulated converter are given in

Table. 8.9.

Table 8.9: Augmented trapezoidal alternate arm converter - specification.

Characteristic	**Value**
DC Voltage (kV)	±300
AC Voltage (kV)	490
DC Current (kA)	1.5
N. of sub-modules per PG	8
Voltage Rating of Stack (PU)	1
Voltage Rating of Director Switch(PU)	0.15
N. of power-groups per Valve	46
N. of sub-modules per Valve	336
N. of IGBTs per Director Switch	46
Nom. Energy (kJ/MVA)	25
sub-module Capacitor Size (mF)	6.9
N. of IGBTS per Valve	1518
N. of Thyristors per Valve	276

Simulated waveforms of a converter arm are shown Fig. 8.7. Due to the third harmonic injection used the converter generates a very low voltage at the peak of the AC voltage waveform. This corresponds to when the arm current is at its peak. This indicates the utilisation of the thyristors should be high.

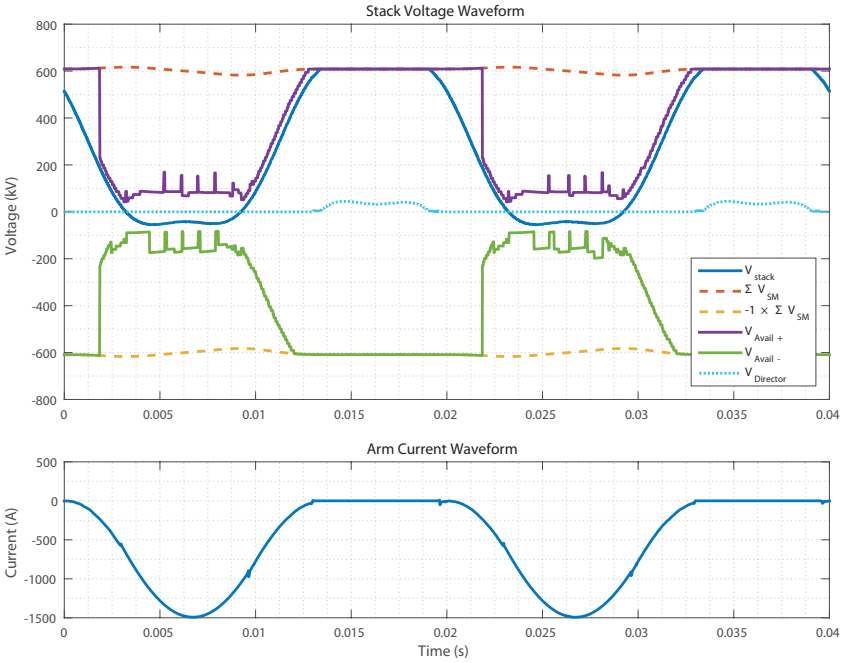


Figure 8.7: AT-AAC operating at rated inverting power.

A comparison of power-losses within the AT-AAC in both its augmented and augmented variant is given in Table. 8.10. As expected the non-augmented variant has higher power-losses than the non-augmented EO-AAC. The losses of the augmented converter however are very promising, with the conduction losses within the IGBTs being reduced by a factor of 2.6.

Power-loss estimates for the AT-AAC at different operating points are given in Table. 8.11. Promising efficiency values at all operating points are seen, with overall losses approaching 0.3% of rated power in the best case operating condition. This is similar to the efficiency values that would be expected in a LCC based HVDC converter, whilst retaining full P/Q capability and DC fault tolerance.

Table 8.10: Comparison of augmented & Non-Augmented AT-AAC power losses at 1 pu inverting operation

Loss Type	Non-Augmented	Augmented
IGBT Conduction	0.630	0.156
IGBT Switching	0.067	0.074
Thyristor Conduction	NA	0.051
Thyristor Turn-Off	NA	0.004
Thyristor Turn-On	NA	0.018
Snubber Loss	NA	0.007
Overall Loss	0.697	0.310

Table 8.11: Power-losses of augmented trapezoidal alternate arm converter across the P/Q envelope (losses in % rated power).

P (pu)	1	1	1	-1	-1	-1
Q (pu)	0	0.3	-0.3	0	0.3	-0.3
Thyristor Utilisation	0.629	0.570	0.725	0.725	0.703	0.734
IGBT Conduction	0.179	0.218	0.136	0.130	0.151	0.125
IGBT Switching	0.080	0.086	0.061	0.063	0.071	0.058
Dir. Switch Conduction	0.038	0.041	0.040	0.034	0.036	0.036
Dir. Switch Switching	0.000	0.000	0.000	0.000	0.000	0.000
Thyristor Conduction	0.037	0.036	0.044	0.043	0.043	0.045
Thyristor Turn-Off	0.004	0.003	0.003	0.003	0.003	0.003
Thyristor Turn-On	0.049	0.046	0.038	0.034	0.041	0.032
Snubber Loss	0.005	0.006	0.005	0.005	0.006	0.005
Overall Loss	0.392	0.435	0.327	0.312	0.351	0.303

8.3.4 Elimination of the Director Switch in the AT-AAC

The AT-AAC shows promising improvements in efficiency over both the A-MMC and the EO-AAC. As the voltage rating of the director switch within this topology has to be rated for a low voltage, approximately 15% of the DC bus voltage, it may be an attractive option to eliminate it from the design completely, constructing the entire stack out of full-bridge power-groups. This has the advantage of simplifying the design of the converter, as well as removing any concerns regarding the hard switching of the series IGBTs within the director switch. The EO-AAC in this form resembles an MMC that is designed to over-modulate its output, with circulating current used to reduce the overall energy deviation of the sub-modules within the converter. Eliminating the director switch also introduces the possibility of designing the converter to allow continuous conduction through the arms. This would allow MMC style balancing currents to be used, rather than relying on the overlap periods to run balancing currents. Doing so would require arm inductors to be included within the converter. The details of the simulation model of the director switch-less AT-AAC are given in Table. 8.12.

Table 8.12: Director switch-less augmented trapezoidal alternate arm converter - specification.

Characteristic	**Value**
DC Voltage (kV)	±300
AC Voltage (kV)	490
DC Current (kA)	1.5
N. of sub-modules per PG	8
Voltage Rating of Stack (PU)	1.2
N. of power-groups per Valve	50
N. of sub-modules per Valve	400
Nom. Energy (kJ/MVA)	25
sub-module Capacitor Size (mF)	5.8
N. of IGBTS per Valve	1600
N. of Thyristors per Valve	300

Simulated waveforms of the AT-AAC operating at 1 pu inverting power are shown Fig. 8.8.

The top most sub-plot shows the voltage generated by the series arrangement of power-groups within the upper arm of phase A. The blue line shows the absolute of the overall voltage generated by the stack of power-groups. The yellow line shows what proportion of the arm has been bypassed through the thyristor path, while the dashed red line shows the sum of the sub-modules voltages within all power-groups within the arm. As the stack voltage decreases more and more power-groups within the arm are set to bypass themselves. The controller maintains enough power-groups with voltage generating capability (i.e without a conducting thyristor valve) in order to still be able to meet the voltage demand from the current controller. The period where the arm is generating a minimum voltage corresponds to the period where the magnitude of the arm current is greatest. Most power-groups within the arm can be bypassed through their thyristor branch at this point, resulting in significant reduction in conduction losses within the converter.

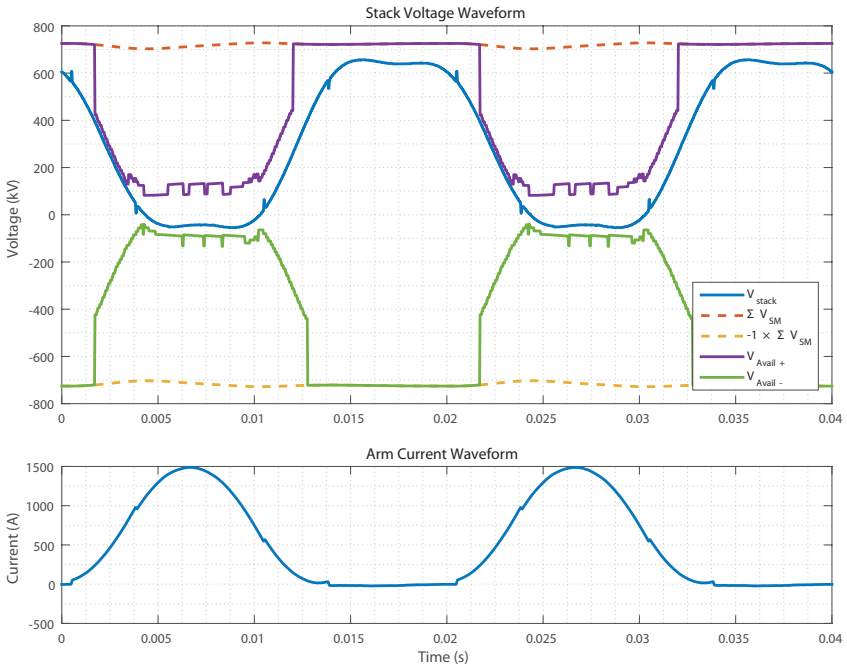


Figure 8.8: AT-AAC without director switch operating at rated inverting power.

Power loss estimates of the AT-AAC without director switch are given in Table. 8.13. Improved efficiency results over the AT-AAC variant that includes a director switch are seen at each set-point tested, with power-losses below 0.3% rated power seen at rectifying operation at a lagging power factor.

Table 8.13: Power-losses of AT-AAC without director switch across the P/Q envelope (losses in % rated power).

P (pu)	1	1	1	-1	-1	-1
Q (pu)	0	0.3	-0.3	0	0.3	-0.3
Thyristor Utilisation	0.717	0.645	0.778	0.766	0.740	0.796
IGBT Conduction	0.156	0.207	0.120	0.130	0.157	0.111
IGBT Switching	0.074	0.091	0.067	0.073	0.089	0.063
Thyristor Conduction	0.051	0.048	0.057	0.055	0.055	0.059
Thyristor Turn-Off	0.004	0.004	0.004	0.004	0.004	0.004
Thyristor Turn-On	0.018	0.019	0.016	0.017	0.021	0.013
Snubber Loss	0.007	0.007	0.008	0.006	0.009	0.007
Overall Loss	0.310	0.376	0.272	0.285	0.336	0.256

8.3.5 Augmented Clamped - Alternate Arm Converter

The idea of looking at clamping the stack voltage waveform to the DC rail to increase the utilisation of the thyristor within the converter arms was proposed by Francisco Moreno from GE Grid during a consultancy meeting.

In a three wire delta system the converter transformer presents an effective infinite impedance to zero sequence components. To increase the utilisation of the thyristors, and so further increase the efficiency of the converter, the idea of twice per phase clamping each phase to a DC rail for a period of 60 degrees is investigated. As the converter will be operated in a three wire delta system, this would not result in any disturbance to the AC current waveforms as two line voltages will remain controlled at all times throughout the cycle. When a phase of the converter is clamped to a DC rail, either the upper or lower arm within the converter would be required

to generate zero volts, representing a chance to activate every thyristor within the converter arm, and so increase the utilisation of the power-group thyristors. Example waveforms of a converter operated in this mode with Alternate Arm currents is given in Figure. 8.9

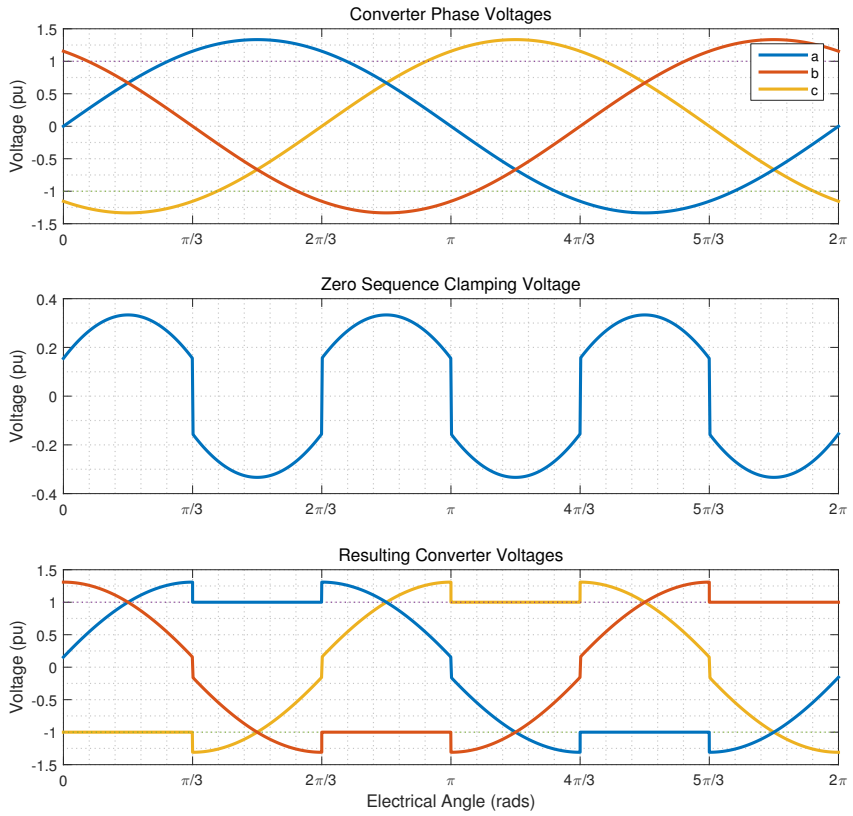


Figure 8.9: Converter waveforms with clamping action.

Given the converter voltages V_a, V_b and V_c, measured with respect to the midpoint of the DC bus, the zero sequence clamping voltage (V_{zsc}) that is injected into the converter waveform can be expressed as in (8.2).

$$V_{zs} = \begin{cases} V_{DC^-} - V_c & 0 \leq \phi < \frac{\pi}{3} \\ V_{DC^+} - V_a & \frac{\pi}{3} \leq \phi < \frac{2\pi}{3} \\ V_{DC^-} - V_b & \frac{2\pi}{3} \leq \phi < \frac{\pi}{2} \\ V_{DC^+} - V_c & \frac{\pi}{2} \leq \phi < \frac{4\pi}{3} \\ V_{DC^-} - V_a & \frac{4\pi}{3} \leq \phi < \frac{5\pi}{3} \\ V_{DC^+} - V_b & \frac{5\pi}{3} \leq \phi < 2\pi \end{cases} \tag{8.2}$$

This variant of the AAC will be referred to as the Augmented Clamped Alternate Arm Converter (AC-AAC).

8.3.5.1 Turn-on and turn-off voltage cancellation

During the start of the clamp period some power-groups in the arm may have to actively discharge a sub-module in order to achieve the correct differential voltage for the turn-off process. In addition, towards the end of the clamped period some of the power-groups must go through the turn-off process in order to make themselves available to generate the requested voltage. Both of these processes result in the converter arm generating a voltage. If every power-group within the arm is set to turn-on its thyristor during this period then there would be no available voltage within the arm for the PGCC to use to compensate for this uncontrolled voltage.

To get around this problem a solution involving adding the uncontrolled turn-on and turn-off voltages to the converters zero-sequence voltage was investigated. This approach works, with disturbances to the arm current waveform caused by the on/off voltages effectively removed. However doing so was found to require an uprating in the stack voltage capability of the converter. The solution that is proposed instead is to not completely deplete the stack voltage capability during the clamped period. Instead a small amount of voltage capability could be retained, allowing effective cancellation of the turn-on and turn-off voltages. This can be achieved by changing the power-group turn-on and turn-off voltage margin thresholds within the PGCC

during the clamped period.

An example waveform of the stack voltage and current of an AC-AAC is shown in Fig. 8.10.

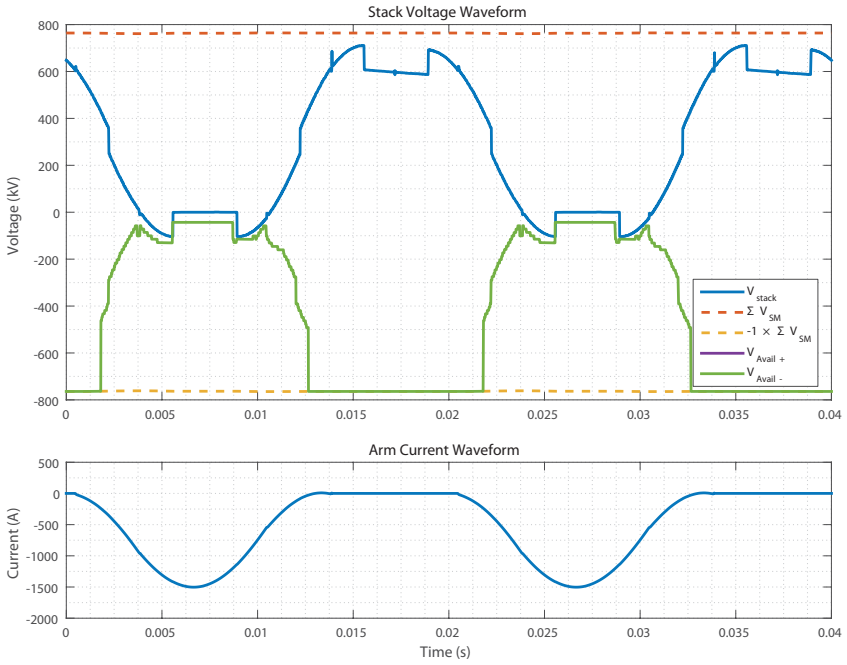


Figure 8.10: AC-AAC without director switch operating at rated inverting power.

8.3.5.2 Efficiency Estimates of the AC-AAC

As the variant of the AT-AAC without a director switch proved to be more efficient, the AC-AAC with full rated stacks of power-groups without a director switch is considered in this section. The ratings of the simulated converter are given in Table. 8.14.

The power-losses within the AC-AAC at several set-points are given in Table. 8.15. In comparison to the AT-AAC the thyristor utilisation has improved, with values approaching 0.8. The increased thyristor utilisation achieved by the clamping action however does not result in any significant gains in efficiency, with power-losses broadly in line with the AT-AAC. As the AC-AAC requires the stacks to be rated to a higher voltage the clamping action, whilst an

Table 8.14: Augmented clamped alternate arm converter - specification.

Characteristic	**Value**
DC Voltage (kV)	±300
AC Voltage (kV)	490
DC Current (kA)	1.5
N. of sub-modules per PG	8
Voltage Rating of Stack (PU)	1.25
N. of power-groups per Valve	53
N. of sub-modules per Valve	424
Nom. Energy (kJ/MVA)	25
sub-module Capacitor Size (mF)	5.5
N. of IGBTS per Valve	1696
N. of Thyristors per Valve	318

interesting idea, does not appear to provide any significant benefits.

Table 8.15: Power-losses of AC-AAC without director switch across the P/Q envelope (losses in % rated power).

P (pu)	1	1	1	-1	-1	-1
Q (pu)	0	0.3	-0.3	0	0.3	-0.3
Thyristor Utilisation	0.661	0.543	0.759	0.779	0.652	0.783
IGBT Conduction	0.206	0.304	0.147	0.128	0.228	0.126
IGBT Switching	0.097	0.119	0.075	0.074	0.104	0.070
Thyristor Conduction	0.049	0.042	0.059	0.058	0.051	0.061
Thyristor Turn-Off	0.005	0.005	0.005	0.005	0.005	0.004
Thyristor Turn-On	0.038	0.036	0.037	0.045	0.051	0.031
Snubber Loss	0.008	0.008	0.008	0.008	0.009	0.008
Overall Loss	0.404	0.514	0.331	0.317	0.449	0.300

8.3.6 Conclusion

A summary of all of the converters that have been tested is given in Table. 8.16. For comparison purposes the power-losses within a non-augmented MMC and a Mixed Stack MMC are also given. Several promising topologies have been identified, with the AT-AAC variant without director switches identified as the converter with the highest efficiency.

Table 8.16: Overall converter comparison - power-losses given at rated inverting power.

Converter	A-MMC	AEO-AAC	AT-AAC	AT-AAC	AC-AAC	MMC	Mixed Stack MMC
Director Switch		✓	✓				
Number of IGBTs	1344	1099	1518	1600	1696	668	1002
Number of Thyristors	252	168	276	300	318	NA	NA
Thyristor Utilisation	0.515	0.263	0.629	0.717	0.661	NA	NA
Power-Loss (% rated power)	0.458	0.563	0.392	0.310	0.404	0.442	0.57

The AT-AAC is a very promising topology. The efficiency of this converter is significantly higher than the Hybrid-MMC, and better than the MMC in its standard half-bridge configuration. It achieves this whilst also retaining the ability to retain control over the AC side currents during DC faults. This converter also has the benefit of requiring a smaller sub-module capacitor in comparison to the MMC. This comes at a cost of requiring significantly more IGBTs within the converter, in addition to the required thyristors and associated ancillary components within each power-group.

9 Power-Groups: Dynamic Response and Fault Ride Through

This chapter details the investigation into the dynamic response of power-group augmented converters during fault scenarios. HVDC converters must be capable of riding through various faults on the AC side, and be capable of providing system support during these fault events. For power-group augmented converters to be a viable concept, it will have to be shown that they are capable of surviving such scenarios. To investigate this a full fault study of several different fault scenarios using variation in the fault inception point-on-wave was undertaken. Several changes, which result in an improved fault response, to both the converters controller and the converters circuit arrangement are proposed.

The requirement to enforce a hold-off time on each power-group during the turn-off of the power-group thyristor, during which the voltage capability of that power-group must be restrained, will have an impact on the dynamic response of the converter. In Chapter. 6, the required hold-off time is estimated to be in the region of 1 ms, the impact that this has on the fault response of the converter will be explored in this chapter.

The response of an AT-AAC to a fault on the AC side is shown in Fig. 9.1. For clarity only the stack voltage and current within the worst affected arm is shown. During steady-state operation the PGCC maintains enough voltage capability within the arm to meet the voltage demand from the current controller. The fault results in a sharp change in voltage demand from the current controller, which the converter is unable to meet because of the utilisation of the power-group thyristors. This results in a loss of current control, resulting in an over-current

event occurring. The negative voltage capability of the converter is regained quickly due to the power-groups asymmetric voltage capability. The converter is unable to meet the voltage demand from the current controller for a period of time approximately equal to the hold-off time of the power-groups.

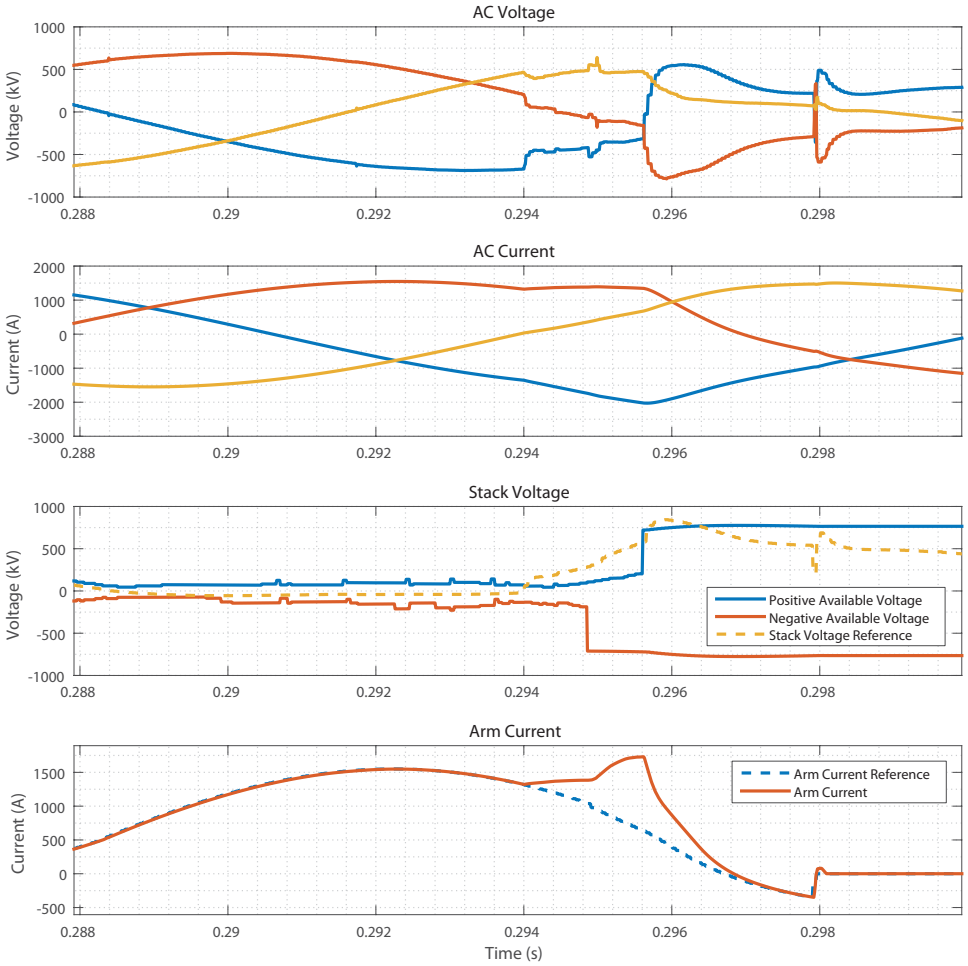


Figure 9.1: Response of an AT-AAC to a three phase fault to 0.3 pu retained voltage.

9.1 Test System

The AT-AAC variant with no director switch is considered to be the most promising converter topology examined in Chapter. 8. For this reason only the dynamics and fault response of this converter are chosen to be considered in the chapter. The characteristics of the test converter,the AC system, and the DC system are given in Table. 9.1.

Table 9.1: Augmented trapezoidal alternate arm converter - specification.

Characteristic	**Value**
DC Voltage (kV)	±300
AC Voltage (kV)	490
DC Current (kA)	1.5
N. of SMs per PG	8
Voltage Rating of Stack (PU)	1.2
N. of PGs per Valve	50
N. of SMs per Valve	400
SM Nom. Energy (kJ/MVA)	25
SM Capacitor Size (mF)	5.8
DC Capacitor Nom. Energy (kJ/MVA)	2
DC Inductor Size (pu)	0.02
PG Turn-On Margin	$0.1 \times V_{dc}$
PG Turn-Off Margin	$0.05 \times V_{dc}$
PG Hold-Off Time	1 ms
Transformer Leakage Reactance (pu)	0.14
Grid Short Circuit Ratio	12.5
Grid X/R Ratio	15
Length of DC Cable	200 km
Resistance per unit length (Ω/km)	0.0376
Inductance per unit length (mH/km)	0.189
Capacitance per unit length (F/km)	0.207

The converter in test has been set into P-V mode, where its active power is set as a reference and the reactive current demand is set by a control loop which attempts to regulate the measured AC voltage at the PCC to 1 pu. During faults the reactive current control loop causes the

converter to inject reactive power into any under-voltage event on the AC grid. For line to line faults the converter is set to inject no current into the fault to prevent over-voltages from occurring on the healthy phase.

The AC system is modelled as a voltage source behind an impedance. The impedance is sized so that the grid has a Short Circuit Ratio of 2.5, with an X/R ratio of 15. The DC system is modelled as an ideal voltage source connected to the DC bus of the converter under test through a 150 km long distributed parameter cable.

9.2 Design factors that impact fault response of Power-group Augmented Converters

This section investigates the main design and control parameters that affect the fault response of power-group augmented converters. A fault phenomenon, caused by the power-group usage is identified, and a solution proposed. The impact of the converters inductor arrangement into the converters fault response is investigated. A change to the controllers current reference calculation is suggested. The viability of increasing the converters power-group turn-off margin is investigated. Finally the fault response of the converter if the hold-off time can be reduced from its assumed 1 ms length is investigated. Converter efficiency estimates when using a faster distributed gate thyristor are also given.

9.2.1 Fast Fault Detection

The Fast Fault Detection block, detailed in Section. 7.13, controls when the power-groups within are sent a command to turn-off during fault scenarios. The fault response of the converter was found to be highly sensitive to the tuning of the low-pass filter within the Fast Fault Detection block, and to the fault detection threshold. Setting the low-pass filter to filter the signal over one half a fundamental cycle, and the threshold value to 8% of the DC bus voltage was found to give a fault detection time of approximately 0.2 ms, whilst giving good noise tolerance during

normal operation.

9.2.2 Arm DC Sum Error Compensation

One of the first issues that was highlighted by the fault study was the need to add an additional subsystem that modifies the voltage reference generated by the current controller to account for the error in stack voltages. The issue observed is that during fault situations, where the controller attempts to meet a sudden change in voltage demand, there may not be enough voltage within the arm to meet the voltage reference. This gives rise to situations where the converter does not properly support the DC voltage. This causes a large common-mode current to be drawn from the DC side, through the arms of the phase which are not supporting the voltage. This is illustrated in Fig. 9.2.

The DC side of the system has a low impedance due to the presence of the DC bus capacitors, if they are present, as well as the capacitance of the DC cable. The common-mode current is only limited by the inductance in the path, which is given by the sum of the DC and arm inductors. In a power-group augmented converter based upon the EO-AAC, these inductors may be small in size, or not present at all in the case of arm inductors.

The solution that has been adopted (credit to Michael Merlin for his discussions on this topic) is to take the error in voltage, between the voltage reference and the available voltage, and adding it as a reference to the other arm within that phase. The modified voltage reference for each arm, $V_{ref,mod}$, is calculated as in (9.1)

$$V_{\mathrm{ref_{mod}}} = V_{\mathrm{ref}} + V_{\mathrm{comp}} \tag{9.1}$$

Where the compensation voltage, V_{comp}, is calculated as in (9.2)

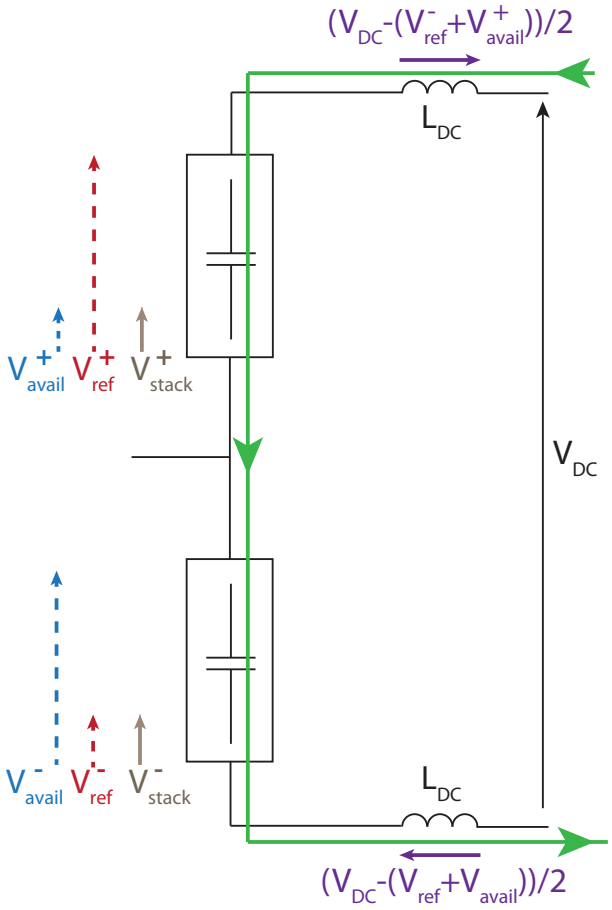


Figure 9.2: Common mode fault current path due to error in available voltage. The upper arm in this figure is incapable of meeting its voltage reference.

$$V_{comp} = \begin{cases} V_{ref_{op}} - V^{+}_{Avail_{op}} & \text{if } V_{ref_{op}} > V^{+}_{Avail_{op}} \\ V_{ref_{op}} - V^{-}_{Avail_{op}} & \text{if } V_{ref_{op}} < V^{-}_{Avail_{op}} \\ 0 & \text{otherwise} \end{cases} \tag{9.2}$$

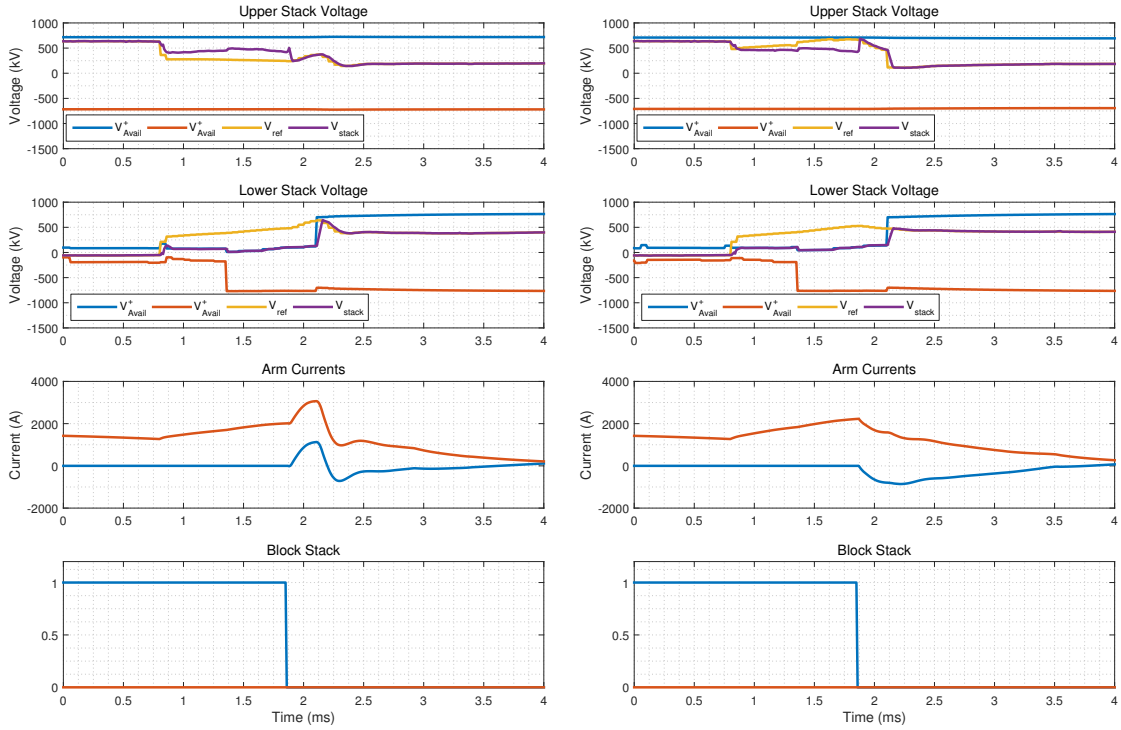
Where $V_{ref_{op}}$, $V^{+}_{Avail_{op}}$, $V^{-}_{Avail_{op}}$ refer to the other arm within the phases voltage reference, positive available voltage and negative available voltage respectively.

In this manner the converter prioritises maintaining control over the DC side currents that enter the converter. The AC side of the systems has significantly higher impedance than the DC

side of the system. This is down to the impedance of the transformer, as well as the impedance of the AC system itself.

A comparison of the fault response of a converter with, and without DC Sum Error Compensation is shown in Fig. 9.3. In both converters the sub-modules within the converter are blocked to allow the arm to act as a director switch. During this period the lower blocked arm is uncontrolled and generates the voltage necessary to drive the current flowing through it to zero. The upper arm is unable to achieve its voltage reference due to a lack of available voltage, and so the converter loses control over the AC side current, causing an over-current event in the upper arm. The lower arm remains blocked and so prevents any common mode current from flowing. When the lower arm is unblocked it is able to achieve its voltage reference from the current controller, however because the upper arm is still unable to generate its requested voltage the converter no longer properly supports the DC bus voltage. This causes a common mode current to flow through both arms, resulting in a sudden worsening in the over-current event. The peak over-current in this case reaches approximately 3000 A, which is a likely destructive amount.

In the case where DC Sum Error Compensation is used the error of the upper arm is added as a reference to the lower arm, this prevents the sudden loss over the DC side currents when the lower arm is unblocked, with fault current now divided between the upper and lower arms. The peak fault current in this case is approximately 2200 A, significantly reduced in comparison to the case with no DC Sum Error Compensation. This is still a serious and potentially destructive over-current event however.



(a) Without DC sum error compensation.

(b) With DC sum error compensation.

Figure 9.3: Worst affected arm in an AT-AAC during a line to line fault at the converter transformer.

9.2.3 Fault Study

In order to ensure that the worst case scenarios were found, the inception angle of each fault was varied by $\frac{\pi}{6}$ intervals referenced to the voltage waveform at the primary of the converter transformer. This was done to ensure the worst case scenarios for each fault case was found. The results of the fault study for the test system are given in Table. 9.2.

The most severe fault situation that was identified is the line to line fault at the transformer during inverting operation, with peak currents reaching close to 3.5 kA, significantly outside of the devices SOA. Large over-currents, of a similar magnitude, were also found to occur during the DC pole to pole fault during rectifying operation, and the three phase fault during inverting operation.

Table 9.2: Peak currents experienced in fault study.

Fault Case	Pre-Fault Power (pu)	Peak Current	Fault Inception Angle
Three Phase Fault	1	1596	0
Three Phase Fault	-1	2300	$\frac{9\pi}{6}$
Single Line to Ground Fault	1	1596	0
Single Line to Ground Fault	-1	1782	$\frac{9\pi}{6}$
Line to Line Fault at Transformer	1	1597	0
Line to Line Fault at Transformer	-1	3495	$\frac{7\pi}{6}$
DC Pole to Pole Fault	1	3416	0
DC Pole to Pole Fault	-1	1531	0

The simulation results of the worst case line to line fault simulation are given in Fig. 9.4. A large over-current is seen in one of the phase currents. Because of the alternate arm action of the converter, this fault current is also seen flowing through one of the arms into the DC side.

The stack voltages and currents of the worst affected phase of the converter in this scenario is shown in Fig. 9.5. A large error between the requested and achieved voltage in the lower arm is seen. This results in a loss of current control, with subsequent over-current event. When the converter recovers its full voltage capability it regains current control and the fault current is driven towards zero.

The following subsections of this chapter will deal with changes to the design and control of the converter, with the aim of reducing these over-currents to within practical levels.

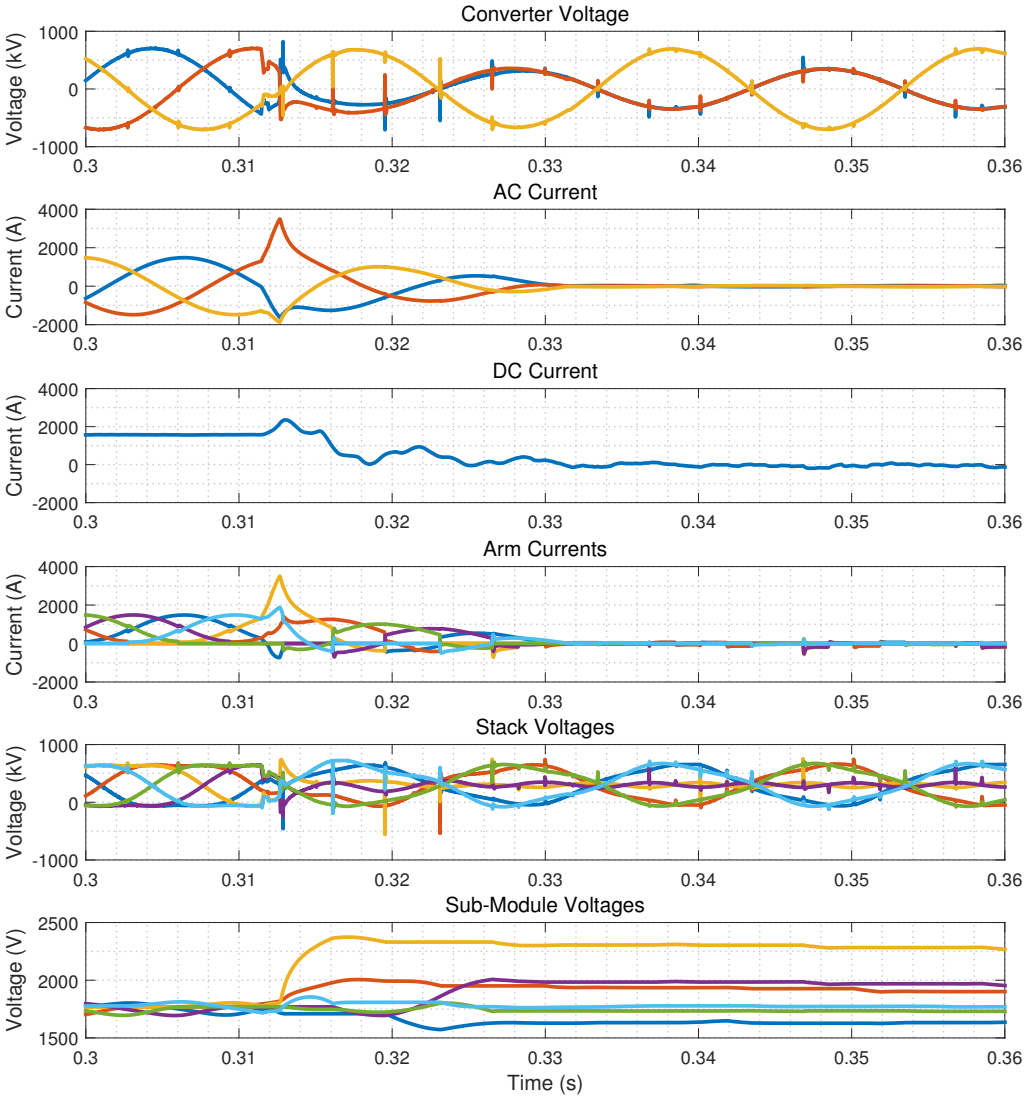


Figure 9.4: AT-AAC response to a line-to-line fault at the transformer - worst case scenario found.

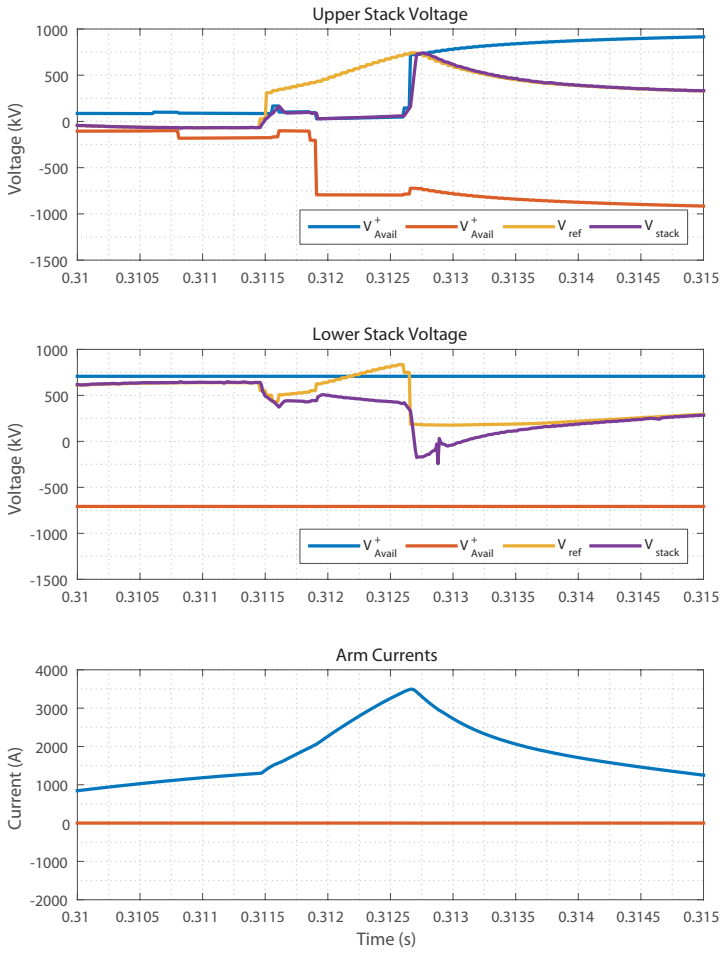


Figure 9.5: AT-AAC response to a line-to-line fault at the converter transformer - worst case scenario found - Phase with highest peak fault current shown.

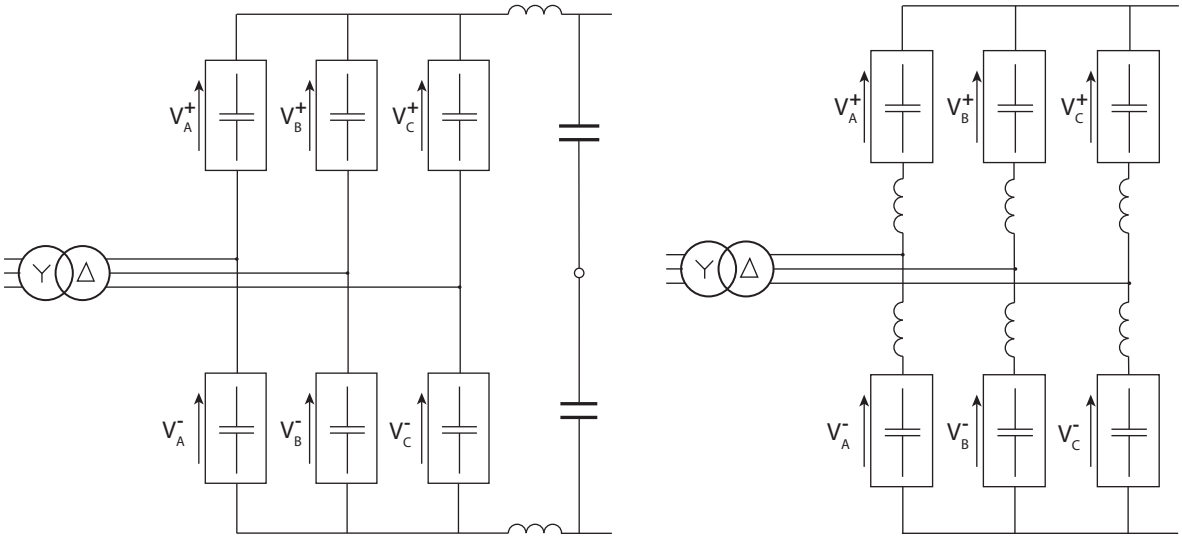
9.2.4 Impact of Inductor Arrangement and Arm Current Control Strategy

The AT-AAC variant that has been considered so far uses the inductor arrangement of the non-augmented EO-AAC. As no director switch is included within the converter the director switch action is achieved by actively blocking stacks, i.e. all IGBTs within the arm are sent a zero gate voltage commands. As the overall nominal voltage within the arm is greater than the peak voltage placed across it the arm therefore acts as an open-circuit and forces the current flowing through it to zero. This mode of operation allows the inductor arrangement for the EO-AAC, discussed in Section. 1.2.4, where the only inductors required for control reasons are a pair of DC inductors, and the impedance presented by the transformer.

One design option that exists is to change the inductor arrangement so that there is some level of inductance within each arm. Both converter arrangements are shown in Fig. 9.6. The introduction of arm inductors allows the converter to be operated with continuous conduction through each arm, with the alternate arm action achieved through current control. Whilst this removes the advantage of a reduced number of required inductors within the converter, it was found that the fault response of the AT-AAC when operated in this mode is significantly improved.

Whilst designing the converter with arm inductors has the drawback of increasing the required number of inductors within the converter from two to six, it does bring some additional benefits. The energy balancing of the converter can be achieved using more traditional MMC style circulating currents, rather than the methods based upon overlap discussed in Section. 1.2.4. This means balanced sinusoidal current sets can be used, further reducing the need for any filtering on the DC side. It also opens up options for having the converter switch operation to MMC mode, or to use circulating currents to suppress the peak current in the converter, as discussed in Chapter 5. This could allow for overload capacity to be easily designed into the converter.

A comparison of the fault response of the AT-AAC designed with both inductor arrangements is shown in Fig. 9.7. In the case of the AT-AAC, the DC inductor has been removed and the arms inductors that are 0.05 pu in size were inserted. The AC side current response is similar



(a) AT-AAC with DC inductors and director switch action achieved through blocking of stacks.

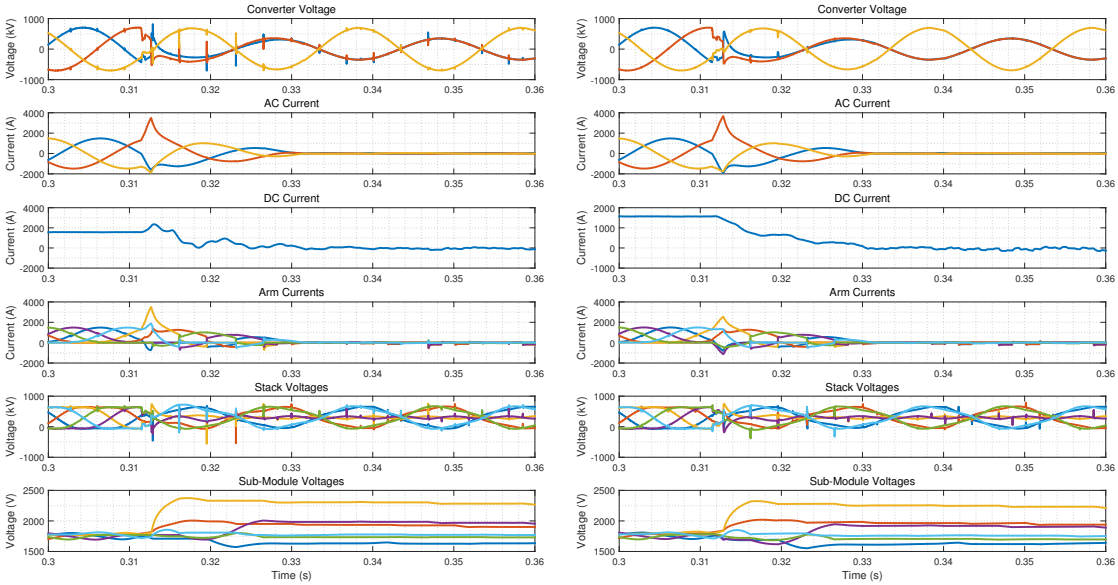
(b) AT-AAC with arm inductors and alternate arm operation achieved through current control.

Figure 9.6: Inductor arrangement possibilities for the AT-AAC.

in both cases, with the peak AC current magnitude in the case with arm inductors slightly higher than the case with DC inductors. The peak current flowing through the arms of the converter operated with arm inductors is significantly reduced however, with the fault current now splitting between the upper and lower arms of each phase.

Fig. 9.8 shows a close up of the currents within both converter arrangements during this fault. The fault current is can be seen splitting between the upper and lower arms in the case with arm inductors, whilst it can only conduct through the un-blocked arm in the case with a DC side inductance.

The fault study was repeated, focusing on the fault scenarios which were found to result in the worst over-currents. The results of this study are shown in Table. 9.3. Significant reductions in the peak fault currents through the arms of the converter are. In the case of a three phase fault during inverting operation the peak current is reduced from 2300 A to 1682 A. In the case of a line to line fault during inverting operation the peak current is reduced from 3495 A to 2546 A. In the case of a DC fault during rectifying operation the peak current is reduced from



(a) AT-AAC With DC inductor and blocked stacks during director switch action.

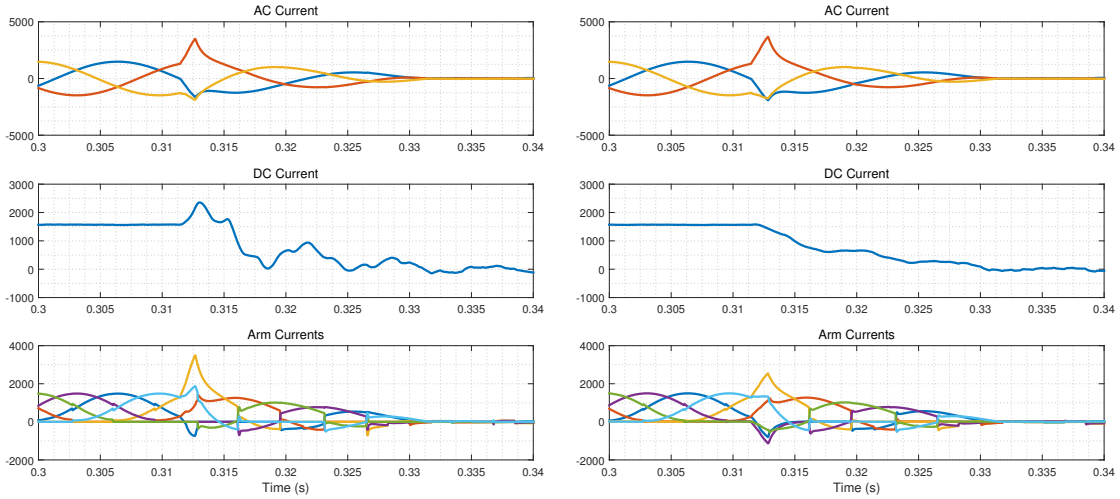
(b) AT-AAC with arm inductors and alternate arm operation achieved through current control.

Figure 9.7: Response of AT-AAC to a line-to-line fault at the converter transformer.

3416 A to 2338 A.

Table 9.3: Peak currents experienced in fault study - converter operated with arm inductors.

Fault Case	Pre-Fault Power (pu)	Peak Current	Fault Inception Angle
Three Phase Fault	-1	1895	$\frac{5\pi}{6}$
Single Line to Ground Fault	-1	1618	$\frac{10\pi}{6}$
Line to Line Fault at Transformer	-1	2546	$\frac{7\pi}{6}$
DC Pole to Pole Fault	1	2338	$\frac{11\pi}{6}$



(a) AT-AAC With DC inductor and blocked stacks during director switch action.

(b) AT-AAC with arm inductors and alternate arm operation achieved through current control.

Figure 9.8: Response of AT-AAC to a line-to-line fault at the converter transformer.

9.2.5 Over-Current Based Set-Point Adjustment

Using Arm DC Sum Error Compensation, detailed in Section. 9.2.2, prevents any large DC side fault current contribution entering the arms of the converter. The over-currents in the converter are dominated by the fault current contribution from the AC side. This sections proposes a controller change, aimed at reducing the AC side fault current contribution. The proposed change is based on the measured maximum over-current within the converter. If an over-current in one arm is detected, the current references for all arms are reduced proportional to the amount of over-current in the worst affected arm. Because the converter is operated in a delta system the three phase currents must sum to zero. The phase with the highest over-current is the one that has the least available voltage within its arms at the point of fault inception. By driving the phase currents in the other phases, which are less affected by the fault, towards zero the over-current on the worst affected fault should also be reduced.

The modified current reference, $I_{\mathrm{arms}_{\mathrm{ref}_{\mathrm{mod}}}}$, can be expressed as in (9.3)

$$I_{\text{arms}_{\text{ref}_{\text{mod}}}} = I_{\text{arms}_{\text{ref}}} k_{mod} \tag{9.3}$$

Where the over-current reduction gain, $k_{ref,mod}$, is given by (9.4), where I_{ocl} is an over-current limit and $k_{overcurrent}$ is a gain.

$$k_{ref,mod} = \begin{cases} (max(|I_{arms}|) - I_{ocl}) k_{overcurrent} & \text{if } max(I_{arms}) > I_{ocl} \\ 1 & \text{otherwise} \end{cases} \tag{9.4}$$

The operation of this set-point adjustment is illustrated in Fig. 9.9. The over-current is detected and the current references for the arms reduced proportionally. The arm current references are undisturbed by the over-current set-point adjustment before the fault, and after the converter has managed to drive the fault current back below the over-current limit.

A comparison of the fault response of an AT-AAC with and without over-current based set-point adjustment is shown in Fig. 9.10. The converter specifications and fault scenario are identical in both simulations. The over-current set-point is set to 1600 A, and $k_{overcurrent}$ is set to $\frac{1}{600}$. The set-point adjustment has little impact on the AC side currents, however the peak current flowing through the converter is reduced, with the fault current now more evenly split between the upper and lower arms of the worst affected phase.

The fault study was repeated for the worst case scenarios identified. The results of this fault study are shown in Table. 9.4. In the case of the line-to-line fault, the peak currents was reduced by more than 400A, from 2546 A to 2112 A. A modest improvement to the peak current seen during the DC pole-to-pole fault is also seen.

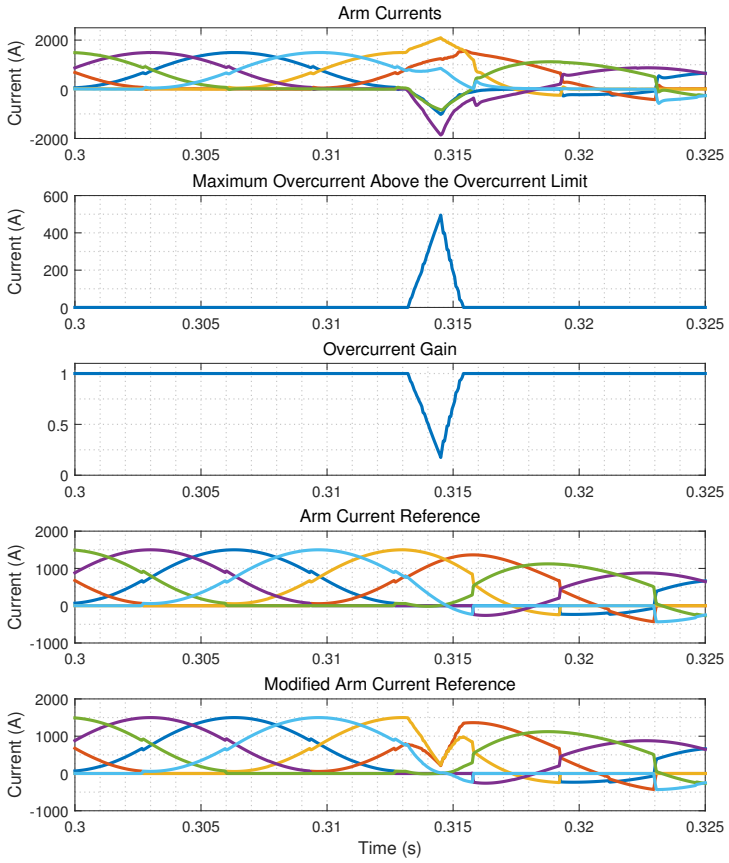
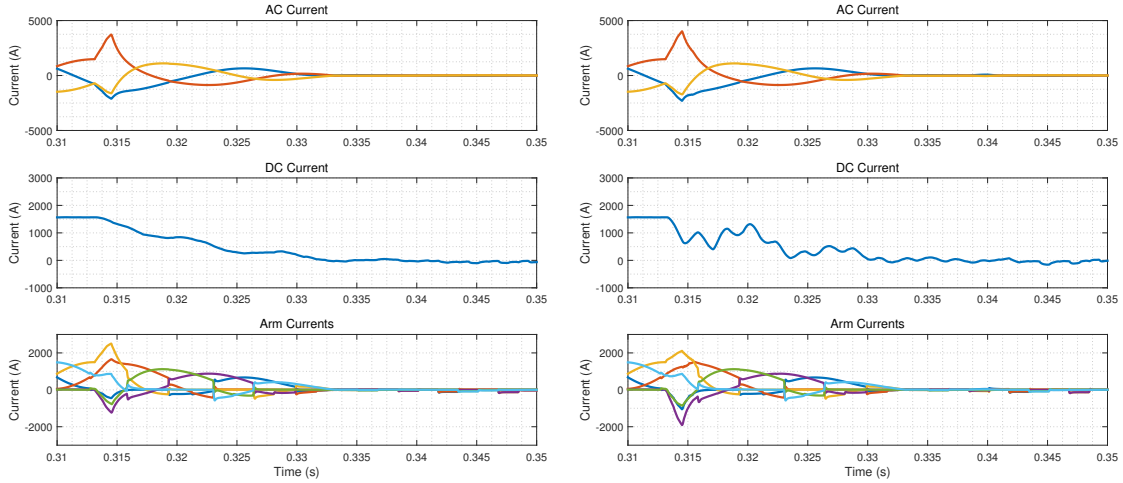


Figure 9.9: Over-current based set-point adjustment during a line-to-line fault in an AT-AAC.

Table 9.4: Peak currents experienced in fault study - converter operated with arm inductors and over-current set-point adjustment.

Fault Case	Pre-Fault Power (pu)	Peak Current	Fault Inception Angle
Three Phase Fault	-1	1746	$\frac{5\pi}{6}$
Single Line to Ground Fault	-1	1611	$\frac{10\pi}{6}$
Line to Line Fault at Transformer	-1	2112	$\frac{8\pi}{6}$
DC Pole to Pole Fault	1	1990	$\frac{11\pi}{6}$



(a) Without over-current based set-point adjustment.

(b) With over-current based set-point adjustment.

Figure 9.10: Response of AT-AAC to a line-to-line fault at the converter transformer.

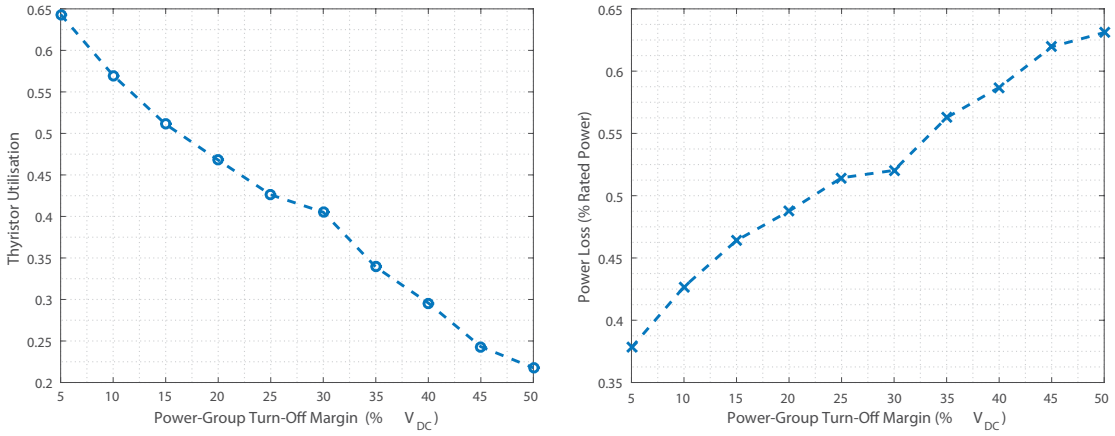
9.2.6 Impact of Power-Group Turn-On and Turn-Off Margin on Fault Response

The loss of current control in the studied converter is caused by the inability of the converter to achieve the voltage demand requested from the current controller. For control reasons, the PGCC must retain a level of voltage capability r, which is above the expected voltage demand from the current controller. The magnitude of this retained voltage is set by the turn-on and turn-off margins, which are used to drive the on/off logic for the power-group thyristors. This is described in Section. 7.4.

By increasing these margins the PGCC will retain a greater amount of available voltage within each arm. This will increase the converters ability to meet any sudden change in voltage demand, potentially reducing the magnitude of any over-currents experienced during fault scenarios. This comes at a cost of decreasing the utilisation of the power-group thyristors, resulting in the efficiency gains achieved by the power-group concept being reduced. This benefits and costs of this are investigated in this section.

Increasing the turn-on and turn-off margins can be expected to give a negative penalty in terms of efficiency. This is because more IGBT devices will be kept within the current path, rather than being bypassed by the power-group thyristors. Fig. 9.11 shows the variation in both the calculated power-losses and the thyristor utilisation with the magnitude of the turn-on margin within an AT-AAC. The turn-on margin in each case was set to a magnitude of 5% V_{DC} above the turn-off margin. It can be seen that increasing the turn-off margin causes a sharp decrease in the thyristor utilisation, with resulting increasing in the power-losses within the converter.

To assess the impact that increasing the power-group turn-off margin will converter fault response the worst case line-to-line fault identified in the sections above was re-run, with variation in the turn-off margin. The arm currents in the worst affected phase for each simulation run are shown in Fig. 9.12. A notable decrease in the peak fault currents experienced can be seen as the turn-off margin is increased. The most notable jump is in the move from a turn off margin



(a) Thyristor utilisation.

(b) Power-losses.

Figure 9.11: Variation of the thyristor utilisation and power-losses with the power-group turn-off margin in an AT-AAC.

of $0.05 \times V_{DC}$ to $0.10 \times V_{DC}$. The peak current in this case is reduced from $2450A$ to $2050A$.

With turn-off margins of $0.3 \times V_{DC}$ and above the over-current is effectively limited to close to zero.

The estimated efficiency values for the AT-AAC with the turn-off margin increased to $0.1 \times V_{DC}$ is given in Table. 9.5. The penalty in terms of power-losses in each case is an additional 0.1% of rated power, an approximate 33% increase over the losses when the turn-off voltage margin was maintained at $0.05 \times V_{DC}$. The large losses penalty that increasing the turn-off margin incurs indicates that this is not an attractive option for improving the fault response of the converter.

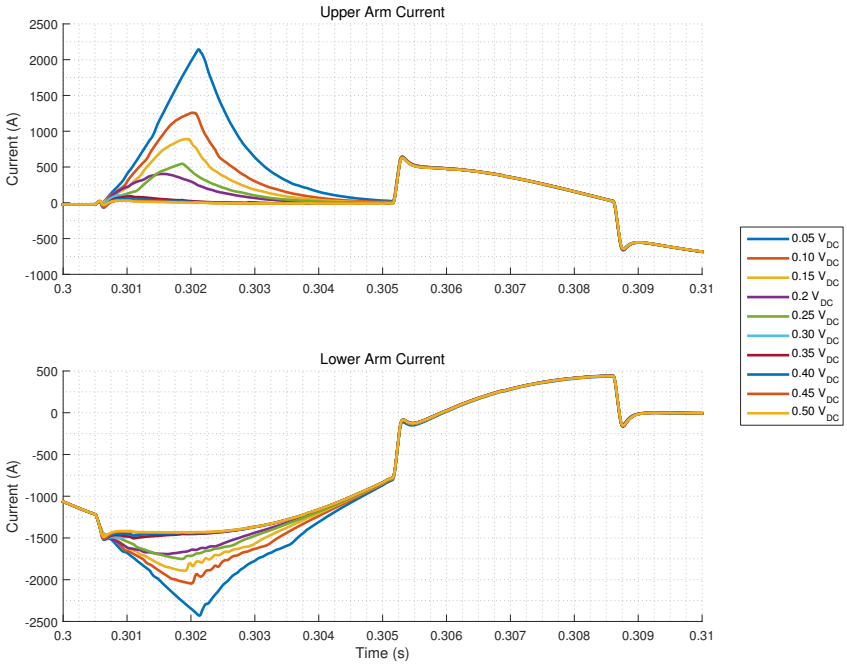


Figure 9.12: Arm Currents in the worst affected phase of an AT-AAC during a line-to-line fault with variation in the power-group turn-off margin.

Table 9.5: Power-Losses of AT-AAC with a turn-off Margin of $0.1 \times V_{DC}$

P (pu)	1	1	1	-1	-1	-1
Q (pu)	0	0.3	-0.3	0	0.3	-0.3
Thyristor Utilisation	0.580	0.498	0.640	0.693	0.628	0.710
IGBT Conduction	0.248	0.314	0.218	0.179	0.234	0.170
IGBT Switching	0.092	0.108	0.078	0.080	0.098	0.074
Thyristor Conduction	0.095	0.086	0.109	0.116	0.110	0.122
Thyristor Turn-Off	0.001	0.001	0.001	0.001	0.001	0.001
Thyristor Turn-On	0.007	0.007	0.005	0.006	0.006	0.005
Snubber Loss	0.017	0.018	0.019	0.015	0.023	0.018
Overall Loss	0.459	0.534	0.430	0.396	0.470	0.391

9.2.7 Impact of Required Hold-Off Time on Fault Response

In this section the viability of decreasing the power-groups hold-off time, and so increasing the speed at which the converter regains its full voltage capability is investigated. Reducing the hold-off time will be dependent on whether the thyristor valve in each power-group will reliably turn-off within the allocated time frame.

The design of the power-group presented in Chapter. 6 assumed the use of an Infineon T2871N 8 kV thyristor that is designed for phase control applications, and so is optimised for low on state losses, rather than a fast recovery time. The Infineon T2871N thyristor has a data-sheet specified turn-off time of 550 μs, specified at a junction temperature of 125^oC and a dV/dt of $20V/\mu s$. In the snubber design section it was found that the peak dV/dt could be limited to values of approximately $200V/\mu s$. For this reason a large safety margin was imposed on the hold-off time, with a value of 1000 μs being considered. Determining the actual hold-off time required would necessitate extensive type testing of a power-group structure.

It should be noted that the device junction temperature has a significant impact upon the device junction turn-off time, and the data-sheet specified turn-off time is given at the devices maximum rated temperature. Because the losses within the thyristor are expected to be low, and the thermal impedance of such large press-pack packages is also low, the rise in temperature from ambient to the device junction can be expected to be minimal. This may somewhat counter the increased hold-off time necessitated by the high dV/dt values.

An alternative option would be to use a different thyristor, sacrificing low on state losses and blocking voltage capability for a faster recovery characteristic. The alternative thyristor chosen for comparison is the R1127NC36 3.6 kV distributed gate thyristor from Westcode. A comparison of two thyristors is given in Table. 9.6. The T2871N device has significantly better forward conduction characteristics and voltage blocking capability in comparison the R1127NC36 thyristor. The advantage of the R1127NC36 device is its much reduced turn-off time characteristics in comparison to the T2871N thyristor. When comparing turn-off times of thyristors it is important to examine the conditions under which the turn-off time is specified.

The R1127NC36 thyristor is specified at a dV/dt of 200 $V/\mu s$, whereas the T2871N device is specified at 20 $V/\mu s$.

As a power-group valve composed of the R1127NC36 device would require 7 devices in series, the actual dV/dt this device would experience is reduced by a factor of 3/7, in comparison to the valve composed of T2871N thyristors. Considering the snubber design presented in Section. 6.4.2, this means each R1127NC36 device would experience a peak dV/dt values in the range of of $86V/\mu s$, below the data-sheet specified dV/dt value for the thyristors turn-off time.

Table 9.6: Comparison of phase control thyristor and fast distributed gate thyristor.

Device Manufacturer	Infineon	Westcode
Device Code	T2871N	R1127NC36
Thyristor Type	Phase Control	Distributed Gate
Repetitive Peak Off-State Voltage (V)	7500	3600
Repetitive Peak Reverse Voltage (V)	8000	3600
Forward Voltage at 1500 A (V)	1.38	2.2
Datasheet Specified T_q (μs)	550	250
T_q specified dV_D/dt ($V/\mu s$)	20	200
T_q specified di_D/dt ($A/\mu s$)	10	60
T_q specified T_j (^oC)	125	125

The efficiency estimates of the AT-AAC when using this device are given in Table. 9.7. An increase in power losses of approximately 0.1% of rated power at inverting and rectifying unity power factor is seen. It should be noted that these power-loss estimates are still lower than the half-bridge MMC, whilst gaining DC fault-ride-through capability. The losses are also broadly equivalent with the losses calculated with the T2871N device when the converter operated with a turn-off margin of 10% V_{DC}, as investigated in Section. 9.2.6. This indicates that if the fault currents reached with a hold-off time of 1000 μs and a turn-off margin of 5% V_{DC} are considered unacceptably high, the R1127NC36 thyristor would be a more attractive option for decreasing the peak fault current levels than increasing the turn-off margin. The reduced hold-off time possible with this thyristor would also add additional benefits, such as simplifying power-group

voltage balancing, discussed in Section. 7.7.

Table 9.7: Power-Losses of AT-AAC using the R1127NC36 thyristor.

P (pu)	1	1	1	-1	-1	-1
Q (pu)	0	0.3	-0.3	0	0.3	-0.3
Thyristor Utilisation	0.763	0.693	0.800	0.792	0.749	0.803
IGBT Conduction	0.129	0.178	0.111	0.116	0.150	0.112
IGBT Switching	0.085	0.106	0.075	0.082	0.102	0.075
Thyristor Conduction	0.186	0.176	0.201	0.197	0.192	0.203
Thyristor Turn-Off	0.001	0.001	0.001	0.001	0.001	0.001
Thyristor Turn-On	0.006	0.008	0.005	0.005	0.006	0.005
Snubber Loss	0.017	0.019	0.021	0.016	0.022	0.020
Overall Loss	0.424	0.487	0.414	0.417	0.473	0.416

The fault study was repeated with the hold-off time set to 750 μs and 300 μs. The 750 μs case represents an optimistic value for the hold-off time if the T2871N device is sued, whilst the 300 μs could be achieved if the R1127NC36 thyristor is used. The results for both hold off times are shown in Table. 9.8. Reducing the hold-off time to 750 μs allows the peak current to be reduced to $\sim$2000 A, while reducing it to 300μs allows it to be reduced to $\sim$1800 A.

Table 9.8: Peak currents experienced in fault study with variation in power-group hold-off time.

(a) Hold-off time of $750\mu s$.

Fault Case	Pre-Fault Power (pu)	Peak Current	Fault Inception Angle
Three Phase Fault	-1	1687	$\frac{5\pi}{6}$
Single Line to Ground Fault	-1	1552	$\frac{10\pi}{6}$
Line to Line Fault at Transformer	-1	2010	$\frac{8\pi}{6}$
DC Pole to Pole Fault	1	1855	$\frac{11\pi}{6}$

(b) Hold-off time of $300\mu s$.

Fault Case	Pre-Fault Power (pu)	Peak Current	Fault Inception Angle
Three Phase Fault	-1	1620	$\frac{5\pi}{6}$
Single Line to Ground Fault	-1	1552	$\frac{10\pi}{6}$
Line to Line Fault at Transformer	-1	1783	$\frac{8\pi}{6}$
DC Pole to Pole Fault	1	1657	$\frac{11\pi}{6}$

9.3 Conclusion

The power-group concept introduces some unavoidable delays into the converters response during fault scenarios. This results in unavoidable over-current events, which can potentially reach very high levels. A fault mechanism that results in the converter not fully supporting the DC bus voltage was identified, and a controller modification to prevent this identified. The inductor arrangement of the converter was found to have a large impact on the peak fault currents in the converter, with a circuit arrangement with inductors located within each arm resulting in significantly lower fault currents. This requirement eliminates some of the converter variants, examined in Chapter 8, that are based upon the EO-AAC that include director switches. An over-current based set-point adjustment modification to the controllers current reference generation has also been proposed which further decreases the peak fault current experienced by the converter.

The maximum fault current reached within the converter, after all improvements to both the

converters circuit layout and controller were implemented, was 2112 A. This peak fault current could be reduced through either reducing the power-group hold-off time, or by increasing the power-group turn-off margin. Both of these options result in an increase in power-losses, which is undesirable. Advice from GE engineers was that the peak fault current of 2112 A was safely within the turn-off capability of the IGBTs considered, and so the use is not considered necessary to utilise either of these options.

The power-group concept provides some very interesting and promising results for allowing high-efficiency, DC fault tolerant converters that are capable of generating high-quality AC and DC side current waveforms to be achieved. Efficiency results higher than the half-bridge MMC, whilst retaining the above qualities is a very encouraging end result of the work done in developing the concept.

Future work on power-group augmented converters could focus on their application in non DC fault tolerant converters, as well as hybrid power-group designs, which utilise both half-bridge and full bride sub-modules. This could allow even higher efficiencies to be achieved. Hybrid power-group designs, which utilise both half-bridge and full bride sub-modules could also be of interest. The use of power-groups in other HVDC applications, such as DC-DC converters could also be investigated.

10 Conclusion

Conclusion on the Design of Modular Voltage Source Converters

The work presented in this thesis has focused on two broad topics. The first concerns the design of Modular Multilevel Converters (MMCs). A methodology for designing MMCs for a given P/Q specification, based upon analytical expressions for the converters internal voltage, current and energy deviation waveforms, has been presented and verified. This methodology includes four design limits in terms of voltage and current, and solves for the required minimum number of sub-modules within the converter, while still enabling the converter to meet its specification in terms of P/Q capability. Analysis of the half-bridge MMC shows that a good trade-off between the sub-module capacitor size and the required number of sub-modules is achieved with a distributed energy storage within the sub-modules capacitors in the region of 30-35 kJ/MVA, with little gain in terms of reduction in the number of sub-modules if the amount of energy storage is increased past this point. The analysis was expanded to the case of the Hybrid MMC, which combines half- and full-bridge sub-modules within each converter arm, in order to achieve tolerance to DC side faults. The Hybrid MMC has more flexibility, in comparison to the standard MMC, in its design with regard the AC to DC voltage ratio at which it operates. When considering the overall converter design (number of required sub-modules, capacitor size, and efficiency) a good balance appears to be achieved if the converter is set to operate at a modulation index in the region of 1.2. This results in an approximate 10% reduction in losses in

comparison to operating at a modulation index of below 1, with a 6% increase in the required number of sub-modules. An issue regarding the balancing of energy between the full- and half-bridges so that both sub-modules make the most utilisation of their peak voltage ratings have been identified, and a solution proposed.

The power-loss and thermal characteristics of several converters have been investigated, with an emphasis on converters that are tolerant to DC faults. Results show that the Alternate Arm Converter (AAC) and the over-modulating Hybrid MMC are the two most efficient DC fault tolerant converter topologies out of those considered, though both have higher power-losses than the half-bridge MMC. The director switch IGBTs in the AAC, and the lower right IGBT in the sparse full-bridge sub-module exhibit the highest power-losses, and therefore the highest steady-state junction temperature, out of all topologies studied. This indicates that alternate IGBTs, such as press-pack devices, may be a sensible option for these topologies.

The last chapter in the first 'half' of the thesis has examined the possibility of including overload capacity within MMCs, in order to enable system services, such as frequency support, emergency power re-routing or power oscillation damping. This thesis has considered the case where there is no exploitable overhead in terms of current limit that can be used in the overload region. To get around this, circulating currents are intentionally injected into the arm current waveforms, allowing more power to be processed by the converter for a given peak arm current limit. These circulating currents impact the energy deviation of the stack of sub-modules within each arm, and so impact the overall design of the converter. Results show that a 30% overload is achievable using this method, with a 10% increase in the required number of sub-modules within the converter. The junction temperatures reached by the semiconductor devices when operating within the overload region were found to be high, and may be a limiting factor in achieving an overload rating. The potential to dynamically rate the converter, so as to limit the peak junction temperature reached by the devices, was investigated. Results show that converters with such features can significantly improve the system response of an AC system during a loss of in-feed event, even in cases where there is little thermal overhead that may be

exploited, resulting in overloads that can only be sustained on timescales of 2-3 seconds.

Conclusion on Power-Groups

The last four chapters of this thesis have focused on the development of power-groups, a brand new concept proposed within this thesis, which combines the sub-modules of a multilevel converter, and the thyristors of a current source converter into one structure, which could be used to form any kind of modular converter.

The inclusion of thyristors within a VSC structure requires the turn-on and turn-off of the thyristors within each power-group to be controlled by the sub-modules within the parallel stack, in order to ensure reliable turn-on and turn-off under all conditions. The required size of the commutating inductance placed in series with each thyristor valve, and the turn-off losses incurred within the thyristors were found to be strongly correlated with the magnitude of the voltages used to control the turn-on and turn-off processes. A new method of generating these voltages by using the difference in capacitor voltages between two sub-modules within the parallel stack has been proposed. This method results in low turn-off losses within the thyristor valve, ensuring the efficiency gains achieved through the superior conduction characteristics of the thyristors are not eroded, also only a relatively small commutation inductor is required and this may allow a more compact power-group design to be achieved. A realistic dV/dt snubber design for the power-group thyristor valve has been presented, the design of which has been simplified by limiting the switching of the sub-modules within the power-group so that they switch in a stepped manner. This prevent excessive dV/dt stress being placed upon the thyristor valve.

The requirement to hold the thyristor valve in each power-group reverse biased for a period of time following turn-off limits the speed at which the voltage capability of a power-group can be recovered. This was found to have a large impact on several aspects of the control of a power-group augmented converter. A Power-Group Centralised Controller (PGCC) has been

developed to address these issues. The PGCC is based upon several forward looking estimates of the voltage demand from the current controller, as well as estimates of the sub-modules voltages within each power-group.

The power-group concept could potentially be applied to any modular converter topology. Several power-group augmented multilevel converters, based upon the MMC and the AAC, have been investigated in order to find what arrangement results in the highest efficiencies. A variant of the AAC, which uses a different third harmonic waveform and eliminates the director switch, stands out as the converter with the best balance of efficiency and device count. This converter topology has been named the Augmented Trapezoidal Alternate Arm Converter (AT-AAC). Power-loss estimates for this converter are below 0.3 % for several operating points, in comparison to power-losses of 0.45 % for a half-bridge MMC and 0.51% for the over-modulating Hybrid MMC. This is a significant improvement, particularly when considering the AT-AAC is tolerant to DC side faults.

The last chapter in this thesis investigated the dynamic response and fault ride through behaviour of the AT-AAC to faults on both the AC and DC network. The use of power-groups limits the ability of the converter to respond to fault scenarios, and so it was found that some loss of current control is inevitable. Initial results indicated that fault currents of over 2 pu could be expected. These over-currents have been vastly reduced to approximately 1.3 pu through a combination of operating the converter with inductors located within each arm, as well as modifications to the converters controller. These over-currents are within the turn-off capability of the IGBTs considered for use in this application, and so are not considered an impediment to the actual realisation of the AT-AAC.

Publications Arising from this Thesis

Power loss and thermal characterization of IGBT modules in the Alternate Arm Converter

P.D. Judge, M.M.C Merlin, P.D. Mitcheson, T.C. Green

Energy Conversion Congress and Expo. September 2013

Dynamic thermal rating of a Modular Multilevel Converter HVDC link with Overload capacity

P.D. Judge, T.C. Green

IEEE Powertech Conference 2015

Hardware Testing of the Alternate Arm Converter Operating in its Extended Overlap Mode

P.D. Judge, G. Chaffey, P. Clemow, M.M.C Merlin, T.C. Green

Cigre HVDC Conference 2015

Paper was jointly awarded the best student paper award.

Reliability Analysis of MMCs Considering Sub-module Designs with Individual or Series Operated IGBTs

J. Guo, J. Liang, X. Zhang, P. D. Judge, X. Wang, T.C. Green

IEEE Transactions on Power Delivery. Early Access May 2016

Dimensioning and Modulation Index Selection for the Hybrid Modular Multilevel Converter

P.D. Judge, G. Chaffey, P. Clemow, M.M.C Merlin, T.C. Green

In Draft - Expected submission to IEEE Transactions on Power Electronics in June 2016

Lab-scale experimental multilevel modular HVDC converter with temperature controlled cells

P. Clemow, P.D. Judge, G. Chaffey, M.M.C Merlin, T.C. Green

IEEE European Conference on Power Electronics and Applications

Reliability Model of MMC Considering Periodic Preventive Maintenance

B. Wang, X. Wang, Z. Bie, P.D. Judge, X. Wang, T.C. Green

In Review - IEEE Transactions on Power Delivery

Frequency Service Provision from MMC-Based HVDC Systems using Dynamic Temperature-Restricted Overload Capability

I. Martinez-Sans, P.D. Judge, B. Chaudhari, T.C. Green

In Review - IEEE Transactions on Power Delivery

The Augmented trapezoidal Alternate Arm Converter: A Power-group Augmented DC Fault Tolerant Voltage Source Converter

I. Martinez-Sans, P.D. Judge, B. Chaudhari, T.C. Green

Completed - To be submitted to Cigre HVDC Conference 2016

Power-Groups: A Thyristor Augmented Multilevel Structure for Achieving High Efficient DC fault Tolerant Voltage Source Converters. Part I: Design & Operation

P.D Judge, M.M.C Merlin, T.C Green, D. Trainer, K. Vershinin

In Draft - Expected submission to IEEE Transactions on Power Delivery in September 2016

Power-Groups: A Thyristor Augmented Multilevel Structure for Achieving High Efficient DC fault Tolerant Voltage Source Converters. Part II: Control, Converter Topologies & Dynamic Response

P.D Judge, M.M.C Merlin, T.C Green, D. Trainer, K. Vershinin

In Draft - Expected submission to IEEE Transactions on Power Delivery in September 2016

Bibliography

[1] T. Garrity, "Shaping the future of global energy delivery," *IEEE Power and Energy Magazine*, vol. 1, no. 5, pp. 26–30, Sep. 2003.

[2] M. P. Bahrman and B. K. Johnson, "The ABCs of HVDC transmission technologies," *IEEE Power and Energy Magazine*, vol. 5, no. 2, pp. 32–44, Mar. 2007.

[3] Siemens AG. High Voltage Direct Current Transmission - Proven Technology for Power Exchange. [Online]. Available: http://www.energy.siemens.com/br/pool/hq/power-transmission/HVDC/HVDC_Proven_Technology.pdf

[4] J. Arrillaga, *High Voltage Direct Current Transmission*, A. Johns and D. Warne, Eds. The Institute of Engineering and Technology Press, 1998.

[5] V. Sood, *HVDC and FACTS Controllers - Application of Static Converters in Power Systems*, M. Pai and A. Stankovic, Eds. Kluwer Academic Publishers, 2004.

[6] M. Pinto, A. Pagioro, and R. Azevedo, "The Rio Madeira HVDC System, Implementation and Commissioning of Bipole 1 and the Connector to Acre-Rondonia," *Cigre Colloqium - HVDC and Power Electronics to Boost Network Performance*, 2013.

[7] Gotland HVDC light. ABB. [Online]. Available: http://new.abb.com/systems/hvdc/references/gotland-hvdc-light

[8] S. Dodds, B. Railing, K. Akman, B. Jacobson, T. Worzyk, and B. Nilsson, "HVDC VSC (HVDC Light) Transmission - Operating Experiences," *Cigre 2010*, 2010.

[9] J. Gerdes, "Siemens Debuts HVDC PLUS with San Franciscos Trans Bay Cable," *Siemens Living Energy*, no. 5, p. 31, 2011.

[10] Zhoushan Multi-terminal DC Interconnection. State Grid Corporation of China. [Online]. Available: http://www.cepri.com.cn/aid/details_71_262.html

[11] X. Li, Z. Yuan, J. Fu, Y. Wang, T. Liu, and Z. Zhu, "Nanao multi-terminal VSC-HVDC project for integrating large-scale wind generation," in *2014 IEEE PES General Meeting — Conference Exposition*, Jul. 2014, pp. 1–5.

[12] D. V. Hertem and M. Ghandhari, "Multi-terminal VSC HVDC for the European supergrid: Obstacles," *Renewable and Sustainable Energy Reviews*, vol. 14, no. 9, pp. 3156–3163, 2010. [Online]. Available: http://www.sciencedirect.com/science/article/pii/S1364032110002480

[13] L. Tang and B. T. Ooi, "Locating and isolating DC faults in multi-terminal DC systems," *IEEE Transactions on Power Delivery*, vol. 22, no. 3, pp. 1877–1884, Jul. 2007.

[14] "Clean Power from Deserts - the Desertec Concept for energy, water and Climate security," 2008, available online. [Online]. Available: http://www.desertec.org/fileadmin/downloads/DESERTEC-WhiteBook_en_small.pdf

[15] "The north seas countries' offshore grid initiative memorandum of understanding," 2010. [Online]. Available: http://www.ewea.org/fileadmin/files/library/publications/research-notes/MoU_definitief.pdf

[16] 20 year offshore network development master plan. European Wind Energy Agency. [Online]. Available: http://www.ewea.org/fileadmin/swf/factsheet/3_thepowergrid.pdf

[17] M. M. C. Merlin, "Hybrid multi-level HVDC converter and multi-terminal DC networks," Ph.D. dissertation, Department of Electrical and Electronic Engineering, Imperial College London, 2012.

[18] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *Power Tech Conference Proceedings, 2003 IEEE Bologna*, vol. 3, Jun. 2003.

[19] J. D. Ainsworth, M. Davies, P. J. Fitz, K. E. Owen, and D. R. Trainer, "Static var compensator (statcom) based on single-phase chain circuit converters," *IEE Proceedings - Generation, Transmission and Distribution*, vol. 145, no. 4, pp. 381–386, Jul 1998.

[20] F. Z. Peng, W. Qian, and D. Cao, "Recent advances in multilevel converter/inverter topologies and applications," in *Power Electronics Conference (IPEC), 2010 International*, Jun. 2010, pp. 492–501.

[21] J. A. Ferreira, "The multilevel modular DC converter," *IEEE Transactions on Power Electronics*, vol. 28, no. 10, pp. 4460–4465, Oct. 2013.

[22] D. Montesinos-Miracle, M. Massot-Campos, J. Bergas-Jane, S. Galceran-Arellano, and A. Rufer, "Design and control of a modular multilevel DC/DC converter for regenerative applications," *IEEE Transactions on Power Electronics*, vol. 28, no. 8, pp. 3970–3979, Aug. 2013.

[23] T. Luth, M. Merlin, T. Green, F. Hassan, and C. Barker, "High-frequency operation of a DC/AC/DC system for HVDC applications," *Power Electronics, IEEE Transactions on*, vol. 29, no. 8, pp. 4107–4115, Aug. 2014.

[24] M. Glinka and R. Marquardt, "A new AC/AC multilevel converter family," *IEEE Transactions on Industrial Electronics*, vol. 52, no. 3, pp. 662–669, Jun. 2005.

[25] J. Wang, B. Wu, D. Xu, and N. R. Zargari, "Multimodular matrix converters with sinusoidal input and output waveforms," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 1, pp. 17–26, Jan. 2012.

[26] M. Glinka and R. Marquardt, "A new AC/AC-multilevel converter family applied to a single-phase converter," in *Power Electronics and Drive Systems, 2003. PEDS 2003. The Fifth International Conference on*, vol. 1, Nov. 2003, pp. 16–23Vol.1.

[27] S. Angkititrakul and R. W. Erickson, "Control and implementation of a new modular matrix converter," in *Applied Power Electronics Conference and Exposition, 2004. APEC '04. Nineteenth Annual IEEE*, vol. 2, 2004, pp. 813–819vol.2.

[28] M. Hagiwara, K. Nishimura, and H. Akagi, "A medium-voltage motor drive with a modular multilevel PWM inverter," *IEEE Transactions on Power Electronics*, vol. 25, no. 7, pp. 1786–1799, Jul. 2010.

[29] B. Jacobson, P. Karlsson, G. Asplund, L. Harnefors, and T. Jonsson, "VSC-HVDC Transmission with Cascaded Two-Level Converters," in *CIGRE*, 2010.

[30] K. Ilves, L. Harnefors, S. Norrga, and H.-P. Nee, "Analysis and operation of modular multilevel converters with phase-shifted carrier PWM," in *Energy Conversion Congress and Exposition (ECCE), 2013 IEEE*, 2013, pp. 396–403.

[31] M. Hagiwara and H. Akagi, "PWM control and experiment of modular multilevel converters," in *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE*, 2008, pp. 154–161.

[32] C. M. Franck, "HVDC circuit breakers: A review identifying future research needs," *IEEE Transactions on Power Delivery*, vol. 26, no. 2, pp. 998–1007, 2011.

[33] M. Callavik, A. Blomberg, J. Hafner, and B. Jacobson, "The hybrid HVDC breaker: An innovation breakthrough enabling reliable HVDC grids," *ABB Grid Systems Technical Papers*, 2012.

[34] Q. Tu, Z. Xu, and L. Xu, "Reduced switching-frequency modulation and circulating current suppression for modular multilevel converters," *Power Delivery, IEEE Transactions on*, vol. 26, no. 3, pp. 2009–2017, Jul. 2011.

[35] K. Ilves, A. Antonopoulos, S. Norrga, and H. P. Nee, "Steady-state analysis of interaction between harmonic components of arm and line quantities of modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 27, no. 1, pp. 57–68, Jan. 2012.

[36] D. Siemaszko, A. Antonopoulos, K. Ilves, M. Vasiladiotis, L. Angquist, and H. P. Nee, "Evaluation of control and modulation methods for modular multilevel converters," in *Power Electronics Conference (IPEC), 2010 International*, Jun. 2010, pp. 746–753.

[37] Q. Song, W. Liu, X. Li, H. Rao, S. Xu, and L. Li, "A steady-state analysis method for a modular multilevel converter," *IEEE Transactions on Power Electronics*, vol. 28, no. 8, pp. 3702–3713, Aug. 2013.

[38] D. Trainer, C. Davidson, C. Oates, N. Macleod, D. Critchley, and R. Crookes, "A new hybrid voltage-sourced converter for HVDC power transmission," in *Cigre Session*, 2010.

[39] M. M. C. Merlin and T. C. Green, "Cell capacitor sizing in multilevel converters: cases of the modular multilevel converter and alternate arm converter," *Power Electronics, IET*, vol. 8, no. 3, pp. 350–360, 2015.

[40] A. Nami, J. Liang, F. Dijkhuizen, and G. D. Demetriades, "Modular multilevel converters for HVDC applications: Review on converter cells and functionalities," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 18–36, Jan. 2015.

[41] M. Perez, S. Bernet, J. Rodriguez, S. Kouro, and R. Lizana, "Circuit topologies, modeling, control schemes, and applications of modular multilevel converters," *Power Electronics, IEEE Transactions on*, vol. 30, no. 1, pp. 4–17, Jan. 2015.

[42] M. M. C. Merlin, T. C. Green, P. D. Mitcheson, D. R. Trainer, R. Critchley, W. Crookes, and F. Hassan, "The alternate arm converter: A new hybrid multilevel converter with DC-fault blocking capability," *IEEE Transactions on Power Delivery*, vol. 29, no. 1, pp. 310–317, Feb. 2014.

[43] S. Fekriasl, M. Merlin, T. Green, K. Dyke, F. Moreno, O. Jasim, and M. Bazargan, "Improvements in or relating to the control of converters," Patent EP2 884 653, Jun., 2015. [Online]. Available: http://www.freepatentsonline.com/EP2884653A1.html

[44] D. Trainer, T. Green, M. Merlin, and D. Soto-Sanchez, "Ep 2727234 a1," May 2014. [Online]. Available: https://www.google.com.ar/patents/EP2727234A1?cl=en

[45] F. Moreno, M. Merlin, D. Trainer, G. T.C., and K. Dyke, "Zero phase sequence voltage injection for the alternate arm converter," in *AC and DC Power Transmission, 2015. ACDC. 10th IET International Conference on*, Feb. 2015.

[46] K. Ilves, S. Norrga, L. Harnefors, and H.-P. Nee, "On energy storage requirements in modular multilevel converters," *Power Electronics, IEEE Transactions on*, vol. 29, no. 1, pp. 77–88, Jan. 2014.

[47] L. Harnefors, A. Antonopoulos, S. Norrga, L. Angquist, and H. P. Nee, "Dynamic analysis of modular multilevel converters," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 7, pp. 2526–2537, Jul. 2013.

[48] A. Antonopoulos, L. Angquist, and H.-P. Nee, "On dynamics and voltage control of the modular multilevel converter," in *Power Electronics and Applications, 2009. EPE '09. 13th European Conference on*, 2009, pp. 1–10.

[49] C. Oates, "Modular Multilevel Converter design for VSC HVDC applications," *Emerging and Selected Topics in Power Electronics, IEEE Journal of*, vol. 3, no. 2, pp. 505–515, Jun. 2015.

[50] A. S. Ltd, "Failure rates of hipak modules due to cosmic rays application note 5sya 2042-04," Tech. Rep., 2013.

[51] Film capacitors: Robustness and fail-safe. Compotech. [Online]. Available: http://www.compotec-electronics.com/wordpress/wp-content/uploads/COMPOTEC-Film-Capacitors-Robustness-and-Fail-Safe.pdf

[52] General technical information: Film capacitors. Vishay. [Online]. Available: http://www.vishay.com/docs/26033/gentechinfofilm.pdf

[53] J. A. Houldsworth and D. A. Grant, "The use of harmonic distortion to increase the output voltage of a three-phase PWM inverter," *Industry Applications, IEEE Transactions on*, vol. IA-20, no. 5, pp. 1224–1228, Sep. 1984.

[54] S. Norrga, L. ngquist, K. Ilves, L. Harnefors, and H. P. Nee, "Frequency-domain modeling of modular multilevel converters," in *IECON 2012 - 38th Annual Conference on IEEE Industrial Electronics Society*, Oct. 2012, pp. 4967–4972.

[55] A. Gustafsson, M. Saltzer, A. Farkas, H. Ghorbani, T. Quist, and M. Jeroense, "The new 525 kV extruded HVDC cable system, ABB technical paper," 2014. [Online]. Available: http://new.abb.com/cables/cables/525-kv-extruded-hvdc-cable-system

[56] G. P. Adam, K. H. Ahmed, and B. W. Williams, "Mixed cells modular multilevel converter," in *Industrial Electronics (ISIE), 2014 IEEE 23rd International Symposium on*, Jun. 2014, pp. 1390–1395.

[57] R. Zeng, L. Xu, L. Yao, and B. W. Williams, "Design and operation of a hybrid modular multilevel converter," *IEEE Transactions on Power Electronics*, vol. 30, no. 3, pp. 1137–1146, Mar. 2015.

[58] K. Ilves, L. Bessegato, L. Harnefors, S. Norrga, and H. P. Nee, "Semi-full-bridge submodule for modular multilevel converters," in *2015 9th International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia)*, Jun. 2015, pp. 1067–1074.

[59] K. Ilves, S. Norrga, and H. P. Nee, "On energy variations in modular multilevel converters with full-bridge submodules for AC-DC and AC-AC applications," in *Power Electronics and Applications (EPE), 2013 15th European Conference on*, Sep. 2013, pp. 1–10.

[60] R. Zeng, L. Xu, L. Yao, and D. J. Morrow, "Precharging and DC fault ride-through of hybrid mmc-based HVDC systems," *IEEE Transactions on Power Delivery*, vol. 30, no. 3, pp. 1298–1306, Jun. 2015.

[61] J. Qin, M. Saeedifard, A. Rockhill, and R. Zhou, "Hybrid design of modular multilevel converters for HVDC systems based on various submodule circuits," *IEEE Transactions on Power Delivery*, vol. 30, no. 1, pp. 385–394, Feb. 2015.

[62] S. Lu, L. Yuan, K. Li, and Z. Zhao, "An improved phase-shifted carrier modulation scheme for hybrid modular multilevel converter," *IEEE Transactions on Power Electronics*, vol. PP, no. 99, pp. 1–1, 2016.

[63] S. Cui and S. K. Sul, "A comprehensive DC short circuit fault ride through strategy of hybrid modular multilevel converters (mmcs) for overhead line transmission," *IEEE Transactions on Power Electronics*, vol. PP, no. 99, pp. 1–1, 2016.

[64] J. Xu, P. Zhao, and C. Zhao, "Reliability analysis and redundancy configuration of mmc with hybrid submodule topologies," *IEEE Transactions on Power Electronics*, vol. 31, no. 4, pp. 2720–2729, Apr. 2016.

[65] *The Grid Code - Issue 5, Revision 12*, National Grid Std. [Online]. Available: http://www2.nationalgrid.com/UK/Industry-information/Electricity-codes/Grid-code/The-Grid-code/

[66] Z. Luo, "A thermal model for igbt modules and its implementation in a real time simulator," Ph.D. dissertation, University of Pittsburgh, 2002.

[67] 5SNA 1500E330305 data sheet. ABB Semiconductors. [Online]. Available: http://new.abb.com/semiconductors/igbt-and-diode-modules

[68] (2007, Dec) IGBT Modules Application Note: The 5th Generation IGBT Chip use. Mitsubishi Electric Ltd. [Online]. Available: http://www.mitsubishielectric.com/semiconductors/files/manuals/igbt_note_e.pdf

[69] Application Note: Thermal Design and Temperature Ratings of IGBT Modules. ABB Semiconductors. [Online]. Available: http://www.abb.com/semiconductors

[70] Load-cycling capability of HiPak IGBT Modules. ABB Semiconductors. [Online]. Available: http://www.abb.com/semiconductors

[71] U. Drofenik, D. Cottet, A. Müsing, J. M. Meyer, and J. W. Kolar, "Modelling the thermal coupling between internal power semiconductor dies of a water-cooled 3300V/1200A HiPak IGBT module," in *Proceedings of Power Conversion and Intelligent Motion Conference*, 2007.

[72] X. Han, Q. Yang, L. Wu, and M. Saeedifard, "Analysis of thermal cycling stress on semiconductor devices of the modular multilevel converter for drive applications," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2016, pp. 2957–2962.

[73] M. K. Bakhshizadeh, K. Ma, P. C. Loh, and F. Blaabjerg, "Indirect thermal control for improved reliability of modular multilevel converter by utilizing circulating current," in *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2015, pp. 2167–2173.

[74] A. Schoen, A. Birkel, and M. M. Bakran, "Modulation and losses of modular multilevel converters for HVDC applications," in *PCIM Europe 2014; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management; Proceedings of*, May 2014, pp. 1–8.

[75] S. Rodrigues, A. Papadopoulos, E. Kontos, T. Todorcevic, and P. Bauer, "Steady-state loss model of half-bridge modular multilevel converters," *IEEE Transactions on Industry Applications*, vol. 52, no. 3, pp. 2415–2425, May 2016.

[76] Z. Shen and V. Dinavahi, "Real-time device-level transient electrothermal model for modular multilevel converter on FPGA," *IEEE Transactions on Power Electronics*, vol. 31, no. 9, pp. 6155–6168, Sep. 2016.

[77] L. Yang, C. Zhao, and X. Yang, "Loss calculation method of modular multilevel HVDC converters," in *Electrical Power and Energy Conference (EPEC), 2011 IEEE*, Oct. 2011, pp. 97–101.

[78] A. Nami and L. Wang, "A multilevel converter with hybrid full-bridge cells," Patent, Jul. 24, 2014, pCT/EP2013/051,027. [Online]. Available: http://www.google.dj/patents/WO2014111164A1

[79] R. Marquardt, "Modular multilevel converter: An universal concept for HVDC-networks and extended DC-bus-applications," in *Power Electronics Conference (IPEC), 2010 International*, Jun. 2010, pp. 502–507.

[80] A. Gustafsson, M. Jeroense, P. Sunnegårdh, M. Saltzer, H. Ghorbani, and H. Rapp, "New developments within the area of extruded HVDC cables," in *AC and DC Power Transmission, 11th IET International Conference on*, Feb. 2015, pp. 1–5.

[81] R. H. Renner and D. Van Hertem, "Ancillary services in electric power systems with HVDC grids," *IET Generation, Transmission Distribution*, vol. 9, no. 11, pp. 1179–1185, 2015.

[82] O. D. Adeuyi, M. Cheah-Mane, J. Liang, N. Jenkins, Y. Wu, C. Li, and X. Wu, "Frequency support from modular multilevel converter based multi-terminal HVDC schemes," in *2015 IEEE Power Energy Society General Meeting*, Jul. 2015, pp. 1–5.

[83] L. M. Castro and E. Acha, "On the provision of frequency regulation in low inertia AC grids using HVDC systems," *IEEE Transactions on Smart Grid*, vol. PP, no. 99, pp. 1–11, 2015.

[84] T. M. Haileselassie and K. Uhlen, "Primary frequency control of remote grids connected by multi-terminal HVDC," in *IEEE PES General Meeting*, Jul. 2010, pp. 1–6.

[85] D. V. Hertem, O. Gomis-Bellmunt, and J. Liang, *Power system oscillation damping by means of VSC-HVDC systems.* Wiley-IEEE Press, 2016, pp. 528–. [Online]. Available: http://ieeexplore.ieee.org/xpl/articleDetails.jsp?arnumber=7435166

[86] T. Smed and G. Andersson, "Utilizing HVDC to damp power oscillations," *IEEE Transactions on Power Delivery*, vol. 8, no. 2, pp. 620–627, Apr. 1993.

[87] X. Aidong, W. Xiaochen, H. Chao, J. Xiaoming, and L. Peng, "Study on overload capability and its application of HVDC transmission system in China southern power grid," in *Power Engineering Society Conference and Exposition in Africa, PowerAfrica '07. IEEE*, Jul. 2007, pp. 1–4.

[88] R. Dass, B. Linden, S. Rinaldo, and S. Cheung, "Operation experience from bulk power HVDC links from Three Gorges complex," *Cigre 2006*, 2006.

[89] M. Rashid, *Power Electronic Handbook*, 2nd, Ed. Elsevier Academic Press, 2007.

[90] IGBT applications handbook. On Semiconductors. [Online]. Available: http://www.onsemi.com/pub_link/Collateral/HBD871-D.PDF

[91] C. Buttay. Cross section of a classical insulated gate bipolar transistor (IGBT). File used under Creative Commons Attribution Share Alike 3.0 Licence.

[92] *Semiconductor Devices Discrete Devices Part 9: Insulated Gate Bipolar Transistors IGBTs*, International Electrotechnical Commission Std.

[93] Applying IGBTs - Application Note 5SYA 2053-04. ABB Semiconductors. [Online]. Available: https://library.e.abb.com/public/ab119704d4797bc283257cd3002ac5e0/Applying%20IGBTs_5SYA%202053-04.pdf

[94] X. Gong, "A 3.3kV IGBT module and application in modular multilevel converter for HVDC," in *Industrial Electronics (ISIE), 2012 IEEE International Symposium on*, May 2012, pp. 1944–1949.

[95] T. Xu, M. W. Donoghue, and C. C. Davidson, "IGBT overcurrent turn-off tests for the mmc-based vsc valves," in *Power Electronics and Applications (EPE), 2013 15th European Conference on*, Sep. 2013, pp. 1–10.

[96] S. Norrga, L. Ängquist, and K. Jlves, "Operating region extension for multilevel converters in HVDC applications by optimisation methods," in *AC and DC Power Transmission (ACDC 2012), 10th IET International Conference on*, 2012, pp. 1–6.

[97] X. Li, Q. Song, W. Liu, S. Xu, Z. Zhu, and X. Li, "Performance analysis and optimization of circulating current control for modular multilevel converter," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 2, pp. 716–727, Feb. 2016.

[98] S. Tenbohlen, T. Stirl, and M. Stach, "Assessment of overload capacity of power transformers by on-line monitoring systems," in *Power Engineering Society Winter Meeting, 2001. IEEE*, Jan. 2001, pp. 329–334.

[99] V. M. Montsinger and P. M. Ketchum, "Emergency overloading or air-cooled oil-immersed power transformers by hot-spot temperatures," *Transactions of the American Institute of Electrical Engineers*, vol. 61, no. 12, pp. 906–916, Dec. 1942.

[100] T. Weekes, T. Molinski, and G. Swift, "Transient transformer overload ratings and protection," *IEEE Electrical Insulation Magazine*, vol. 20, no. 2, pp. 32–35, Mar. 2004.

[101] D. A. Douglass and A. A. Edris, "Real-time monitoring and dynamic thermal rating of power transmission circuits," *IEEE Transactions on Power Delivery*, vol. 11, no. 3, pp. 1407–1418, Jul. 1996.

[102] R. S. Olsen, J. Holboll, and U. S. Gudmundsdttir, "Dynamic temperature estimation and real time emergency rating of transmission cables," in *PES General Meeting, 2012 IEEE*, Jul. 2012, pp. 1–8.

[103] C. E. Spallarossa, M. M. C. Merlin, Y. Pipelzadeh, and T. C. Green, "Reduced dynamic model of a modular multilevel converter in powerfactory," in *2015 IEEE 16th Workshop on Control and Modeling for Power Electronics (COMPEL)*, July 2015, pp. 1–7.

[104] O. Anaya-Lara, F. Hughes, N. Jenkins, and G. Strbac, "Influence of wind farms on power system dynamic and transient stability," *Wind Engineering*, vol. 30, no. 2, pp. 107–127, 2006.

[105] (2012) NETS Security and Quality of Supply Standard, version 2.2. National Grid. [Online]. Available: http://www2.nationalgrid.com/UK/Industry-information/Electricity-codes/SQSS/The-SQSS/

[106] C. Oates and K. Dyke, "The Controlled Transition Bridge," in *Power Electronics and Applications (EPE'15 ECCE-Europe), 2015 17th European Conference on*, Sep. 2015, pp. 1–10.

[107] (2012) Technical information: Bipolar semiconductors. Infineon Technologies. [Online]. Available: http://www.infineon.com/dgdl/Infineon_Bipolar-AN20012_01_Technical_Information-AN-v1.0-en.pdf?fileId=db3a304412b407950112b40ec42b126a

[108] B. Williams, *Power Electronics: Devices, Drivers and Applications.* Macmillan, 1987.

[109] Application Note 5SYA 2020-02: Design of RC snubbers for phase control. ABB Switzerland Ltd. [Online]. Available: https://library.e.abb.com/public/27552f27f7688d5cc12573e90032b2cb/Design%20of%20RC%20snubbers%20for%20PCT_5SYA%202020-02NewLay.pdf

[110] J. Bernardes and S. Swindler, "Modeling and analysis of thyristor and diode reverse recovery in railgun pulsed power circuits," in *2005 IEEE Pulsed Power Conference*, June 2005, pp. 79–82.

[111] F.J.Moreno, M. Merlin, D. Trainer, T. Green, and K. Dyke, "Zero phase sequence voltage injection for the alternate arm converter," in *AC and DC Power Transmission, 11th IET International Conference on*, Feb. 2015, pp. 1–6.