LOW-TEMPERATURE SOLUTION-PROCESSED METAL OXIDE SEMICONDUCTORS FOR LARGE-AREA ELECTRONICS

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DECLARATION

This thesis describes the work carried out between October 2014 and February 2018 in the Experimental Solid State (EXSS) Physics group of Imperial College London, under the supervision of Prof. Thomas D. Anthopoulos. The contents of this thesis are my own work and includes nothing, which is the outcome of work done in collaboration, except where explicitly stated in the text. The material in this thesis has not been previously submitted, in part or whole, for a degree, diploma or other qualification at any University or institution.

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ABSTRACT

In recent years, solution-processed metal oxide semiconductor thin-film transistors (TFTs) have shown great promise as an emerging technology in the field of large-area electronics. This has been possible due to a range of favourable properties, such as high charge carrier mobility, low power consumption, optical transparency and mechanical flexibility. However, emerging electronic applications such as high-definition displays demand TFTs with ever increasing performance characteristics that are inaccessible by existing technologies. This thesis focuses on developing TFTs based on metal oxides beyond the current state-of-the-art performance via low-temperature (<250°C), solution-processed methods and the compatibility of these devices on temperature sensitive and inexpensive flexible plastic substrates.

The work first explores low-dimensional high performance ultra-thin (<15 nm) In_2O_3/ZnO heterojunction (HJ) TFTs, in which the In_2O_3 and ZnO layers were deposited via ultrasonic spray pyrolysis (SP) in ambient conditions and spin coating, respectively. Using this bi-layer approach, the impact of the second semiconducting layer on the electrical performance and on the interface(s) was studied using different characterisation methods. The results demonstrated TFTs with enhanced electron mobilities of 40 – 50 cm^2/Vs.

The next part of this work explores a facile n-type doping approach of the HJ TFTs described in the previous part. An additional layer of fullerenes (pristine and doped) was introduced on top of the oxide bi-layers to study the concept of hybrid modulation doping (MOD) in organic-metal oxide layered semiconductors. Using electrical and optical characterisations, the effect of this extra doping layer was evaluated on the HJ TFT performance.

The third part discusses the utilisation of high-κ oxides (ZrO_2, Y_2O_3 and ZrO_2:Y_2O_3 blend) dielectric system for high-performance In_2O_3/ZnO HJ TFTs on inexpensive flexible polyimide (PI) substrates, where all layers were deposited via spin coating. Using these dielectrics, TFTs with electron mobilities 15 – 25 cm^2/Vs and a reduced operating voltage (± 2V) were observed.

The final part introduces the concept of hybrid perovskite-oxide phototransistors, where $CH_3NH_3PbI_3$ perovskite nanocrystals (NCs) were deposited on top of two different bi-layer TFTs (In_2O_3/ZnO and In_2O_3/Al-ZnO) to study their light response. The transistors were exposed to light at different wavelengths and the results demonstrate a high photoresponse at shorter wavelengths, i.e. near UV region with maximum responsitivity of around 10^4 (A/W), which is at least a few orders of magnitude higher than previously reported values for metal-oxide based phototransistors.

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LIST OF PUBLICATIONS

1. H. Faber†, **S. Das**† († Equal contribution), Y.-H. Lin, N. Pliatsikas, K. Zhao, T. Kehagias, G. Dimitrakopulos, A. Amassian, P. A. Patsalas, T. D. Anthopoulos, "Heterojunction oxide thin-film transistors with unprecedented electron mobility grown from solution", Science Advances **3**, 1–10 (2017).

2. **S. Das**, Y.-H. Lin, N. A. Hastas, T. D. Anthopoulos, "Hybrid modulation-doping of heterojunction metal oxide thin-film transistors for mimicking photodetectors". To be submitted.

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1. INTRODUCTION

1.1 Background

A transistor, commonly used as an solid-state electronic switch in current logic circuits, is the backbone of all modern-day electronic devices. Before it's invention, a thermionic valve or a vacuum-tube triode was the basic building block for electronics, which relied on the thermal emission of electrons from a heated cathode to an anode as its working principle. However, the numerous drawbacks of this device, such as bulk size, ineffective power usage, limited lifespan, high production costs, etc., led to the development of a transistor, in a bid to push this technology forward. Since then, transistors have become a vital component in modern-day electronics ranging from basic circuits to the most complex integrated circuits (ICs).

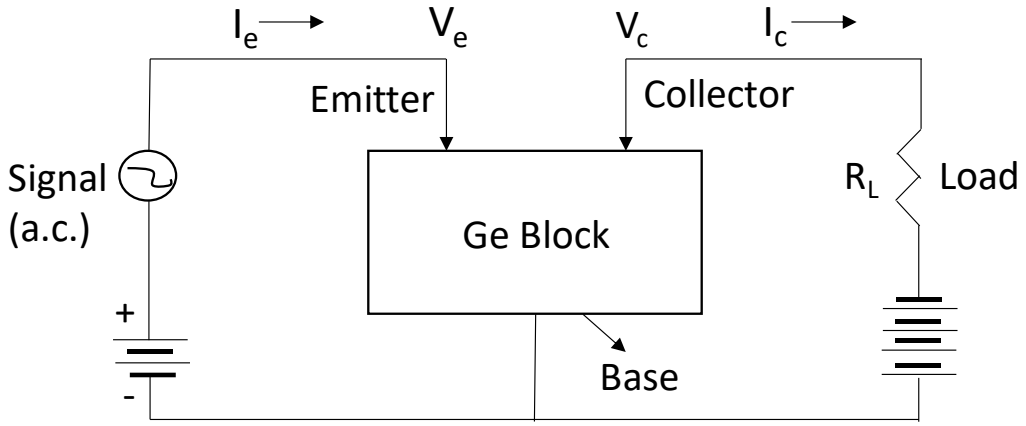


Figure 1: Schematic of n-type Ge crystal bipolar junction transistor (BJT) illustrating circuit for amplification of an a.c. signal and conventional direction for currents. I_e and I_c describe the emitter and collector currents with V_e and V_c being the corresponding voltages. A p-type inversion layer, controlled by the base bias, was formed near the crystal surface. By applying V_e, there is a current flow through the inversion layer to collector side. Reproduced from [1,2].

The pioneering work of Julius Edgar Lilienfield in the 1920s illustrating the initial "transistor-like" concept[3–5], as well as, Oskar Heil's patent[6] in 1935 suggesting how the resistance can be controlled in a semiconducting material, were both major breakthroughs in the field of electronics. Based on these reports, the first transistor device was fabricated based on germanium (Ge) crystal in 1947 by John Bardeen, Walter Brattain and William Shockley at Bell Laboratories[1,2]. This invention marked the beginning of a new era in the electronics industry, starting with the fabrication of the first portable radio in 1958.

Silicon (Si), the most well-known semiconductor to date, has indisputably remained the vital material in electronics with its widespread usage in all aspects of daily life. After the first Si based transistor was demonstrated in the 1950s[7], there was a rapid progress made in Si-based technologies building the foundation of current day electronics. However, the omnipresence of Si-technology started to get challenged after the introduction of a new class of semiconducting materials, namely metal-oxides. This materials class possesses a wide range of promising chemical and electronic properties, such as high charge carrier mobility and visible transparency together with a potential for low power consumption and compatibility with flexible substrates, making them an intriguing subject for numerous modern-day electronic applications.

Amongst the different types of transistor structures, the thin-film transistor (TFT) has recently been attracting a considerate amount of interest, due to its potential to fabricate transistors on a variety of substrates utilising thin-films of semiconductors (other than Si). The first TFT was fabricated using evaporated cadmium sulfide (CdS) and Si layers as the semiconductor and gate electrode, respectively[8]. Following this development, in 1973, Thomas P. Brody and his colleagues reported an operating active-matrix liquid crystal

display (AMLCD) based on TFTs made of cadmium selenide (CdSe)[9]. However, due to the toxicity of CdSe, other semiconducting materials were considered as the channel material, starting with the report of using tellurium (Te) by Masataka Matsuura and his colleagues[10]. But, this semiconducting material was characterised by low on-off current ratios making it unsuitable for high-performance devices. Hence, the focus shifted to the use of polycrystalline Si (poly-Si) and hydrogenated amorphous silicon (a-Si:H). In 1979, a breakthrough was achieved in the TFT technology with the demonstration of a-Si based TFTs[11]. Due to favourable properties and relatively simple fabrication process, a-Si soon became the centre of attention for the research and development of these TFTs for high-performance flat-panel displays (FPDs).

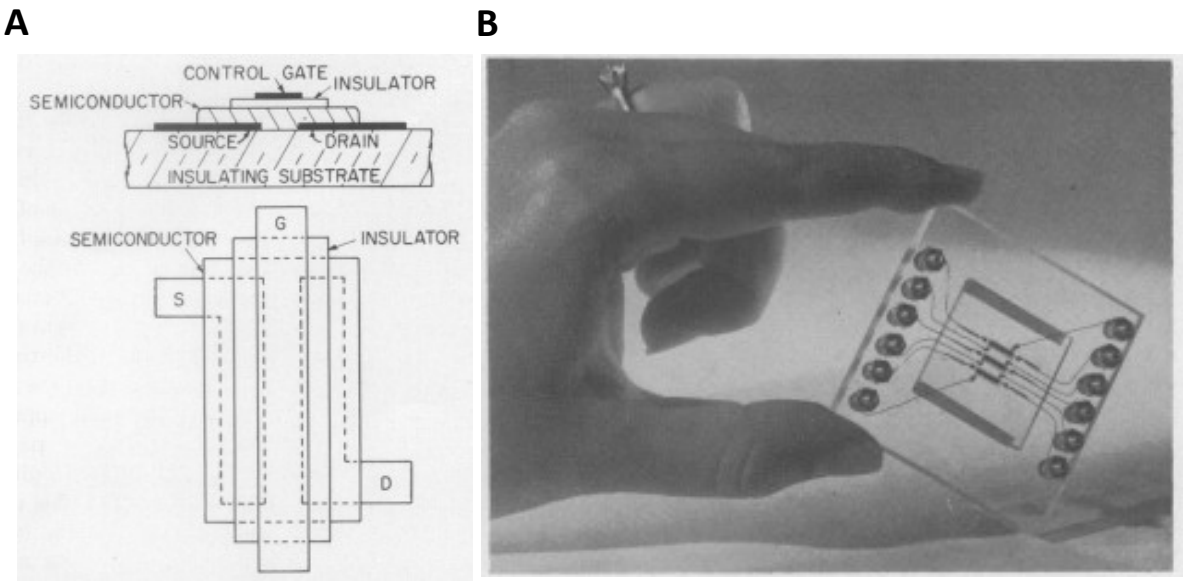


Figure 2: (A) Cross-sectional and top view of first TFT fabricated by Paul Weimer, and **(B)** photo of CdS based TFTs fabricated on a 1-in square glass substrate. Taken from [12].

As the display market started to grow and the technological demands increased, it was soon realised that a more complex circuitry was required, with multiple TFTs in a chip

for a better performance and at a reasonable cost. This could not be realised with Si-based TFTs due to the limitation in performance together with high mass market costs. In addition, the small bandgap of Si renders the materials unsuitable for novel applications in transparent displays. Another drawback, the relatively high processing temperatures associated with the Si-based TFT fabrication made it a complex process for its incorporation onto plastic substrates. Luckily, due to the flexibility of TFT compositions and processing, more choices were made available for semiconducting materials, such as carbon-based fullerene and graphene, organic semiconductors and metal-oxide semiconductors.

With initial reports of organic TFTs yielding promising device performance (mobility values of 10^{-5} – 0.1 cm^2/Vs), the focus began to shift towards the development of new organic materials with improved charge-transport mechanisms[13–18]. Even though these materials showed promise, organic TFTs exhibited poor environmental stability[19–22], making it difficult for these devices to enter the consumer electronics sector and compete with other established TFT technologies. Another class of semiconductors, namely metal-oxides started gaining attention for their use in TFTs, due to the advantages possessed in all the afore-mentioned aspects compared to other types of TFTs.

Since the initial reports of TFTs based on metal-oxide semiconductors around the late 1990s and early 2000s by different groups[23–26], there has been a growing interest and demand in oxides for use in TFTs. These TFTs showed various features, such as high electron mobilities (> 10 cm^2/Vs), ease in fabrication, high optical transparency, better stability under different conditions and potential for mass production. These properties made them an ideal candidate for high-performance devices and thus, a replacement for Si based TFTs for use in unconventional applications, such as, optical displays and transparent electronics.

This has led to the research and development of metal-oxides by major companies for flat-panel display applications. The success of metal-oxide TFTs in such a short span of time is an indication of possibly one of the swiftest transfers of research (academic and fundamental) works to the mass-production of electronics in history, with the first back-panel prototypes using indium-gallium-zinc oxide (IGZO) TFTs reported in 2008 by Samsung followed by the first oxide-based TFT display produced for the mass market in 2012 by Sharp Laboratories[27].

Following the successful development of metal-oxide TFTs, researchers in industry and educational institutes started investigating methods aiming to understand and develop less expensive materials and low-cost deposition methods required for stable, reproducible, large-area, disposable electronics. With metal-oxides available in non-toxic precursor-solvent systems, the focus began to shift towards solution-processing methods, for example, spray pyrolysis, spin coating, printing, etc., making them promising candidates to replace existing expensive vacuum-based technology which was required for Si-based devices.

1.2 Motivation

Semiconductors or a semiconductor layer remains an important material for high-performance electronic devices and hence, the development of semiconducting materials is still considered to be of upmost importance with significant focus on it over the years. Until recently, Si was seen as the main semiconductor for electronic applications, however, with the introduction of metal-oxide semiconductors, a new era was unlocked with oxide based devices exhibiting better performances than a-Si and showing promising signs of fast approaching that of poly-Si devices. With such rapid progress and recent reports of display

panels based on oxide TFTs for the consumer electronic market, there has been a considerable interest in the search for cost-effective production methods for the future generations of large-area, high-definition displays. Even though vacuum-based processing methods have shown to yield devices with good performance, they are associated with high-cost and certain limitations regarding the development of new materials. This has led to the development of solution-based fabrication methods for oxide semiconductors, with these materials offering high-performance devices with high electron mobilities and a considerably lower production cost.

Considering the factors mentioned above, the primary goal of this research was to develop a low-cost solution-processable oxide-based material system suitable for large-area electronics processed at low-temperatures. The initial part focused on a heterojunction TFT system based on In_2O_3/ZnO, deposited via spray pyrolysis and spin coating. This was followed by (a) a doping approach on the HJ TFTs using an additional layer of fullerenes doped at different concentrations, and (b) a study of the light response of these TFTs by depositing perovskite nanocrystals on top of the HJ layer. Finally, work was also carried out to implement the use of high-κ dielectrics in an attempt to operate the HJ TFTs at lower voltages. The use of low-temperatures for deposition/processing would enable the realisation of a new range of unconventional flexible electronics without the need for an expensive manufacturing process, while not compromising on their electrical properties.

1.3 Thesis outline

The remaining part of this thesis is sectioned into different chapters.

- **Chapter 2** presents a general review of the literature and theoretical foundation for metal-oxide semiconductors, including the charge transport mechanism in these materials. The chapter concludes with a brief summary of the working principles of a transistor, mainly focusing on the TFTs.
- **Chapter 3** discusses all the experimental methods used for device fabrication together with the electrical and material characterisation techniques employed for this research.
- **Chapters 4 – 7** comprise the main part of this research, including results and key experimental findings, providing a better insight into the field of solution-processed metal-oxide TFTs processed at low-temperatures.
    - **Chapter 4** presents a bi-layer TFT approach using a In_2O_3/ZnO heterojunction deposited via spray pyrolysis and spin-coating.
    - **Chapter 5** reports on a hybrid modulation-doping (MOD) approach employed on the previously reported heterojunction TFTs.
    - **Chapter 6** presents the use of high-κ oxide dielectric systems on the In_2O_3/ZnO TFTs and its incorporation on inexpensive, flexible substrates (polyimide).
    - **Chapter 7** introduces perovskite nanocrystals deposited on top of the heterojunction TFTs to study the response of light at different intensities/wavelengths.
- **Chapter 8** includes a summary of the thesis focusing on the results and discussions from each chapter.
- **Chapter 9** provides the list of references.

2. THEORY OF SEMICONDUCTORS AND THIN-FILM TRANSISTORS

This chapter focuses on more general remarks and theory of metal-oxide semiconductors followed by a basic introduction about thin-film transistor (TFT) operation and common methods which were used to characterise the TFTs and extract key parameters.

2.1 Metal-oxide semiconductors (MOS)

2.1.1 Electronic structure

The majority of the metal-oxides reported to date exhibit n-type (electron transporting) behaviour due to the complex nature of achieving hole transport in these materials. This can be better illustrated by analysing their electronic structures, consisting of valence band maximum (VBM) and conduction band minimum (CBM). Metal-oxides are characterised by complex electronic structures and an inconsistent carrier conduction, rising as a result of the interactions between the metal and oxygen orbitals[28,29]. Unlike Si, where the VBM and CBM are formed by sp^3 σ (bonding) and sp^3 σ^* (anti-bonding) states of the sp^3 hybridised orbitals of Si, in metal-oxides (known to be valence compounds), the VBM and CBM are composed of different ionic species. These species possess a high degree of ionicity within their chemical bonding. The CBM primarily consists of the antibonding between spatially-spread metal ns (n denotes the principal quantum number) and oxygen 2p orbitals, with the possibility of a direct overlap of the neighbouring metal orbitals resulting in distinctive electron transport properties in metal-oxides[30]. On the contrary, the VBM consists of the bonding and nonbonding 2p orbitals of oxygen ions which are characterised by large

electronegativity and strong directivity causing the VBM to possess small band dispersions and deep energy levels. Therefore, there is a large bandgap present (as a result of the energy difference in bonding states), causing transparency in the visible spectrum. The overall structure consists of a highly dispersive CBM and a localised VBM with the electrons possessing smaller effective masses, thus making it difficult for metal-oxides to introduce holes as dopants and/or obtain a high hole mobility[30]. Apart from the electronic structure, the specific ionic bonding schemes in metal-oxides also contribute to the good n-type conductivity, even in the amorphous state. This is better illustrated in the figure below.

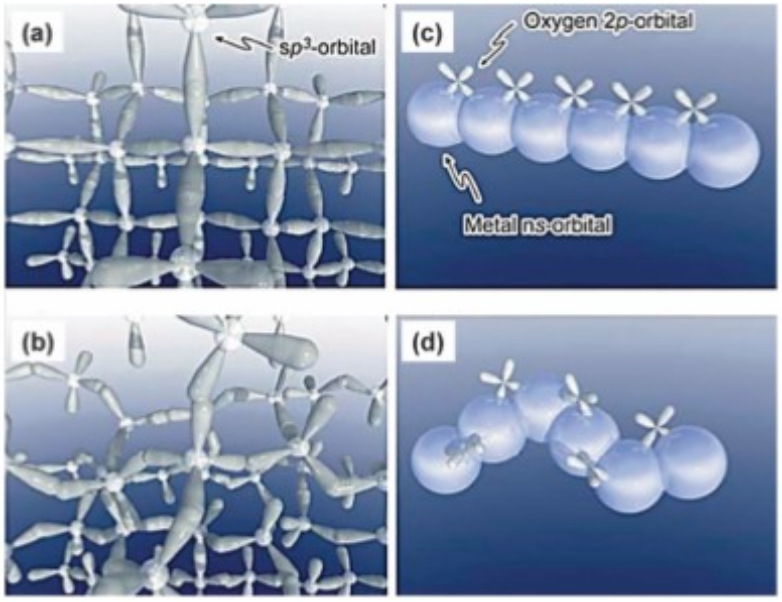


Figure 3: Conduction paths in **(a)** crystalline Si, **(b)** amorphous Si, **(c)** crystalline metal-oxide, and **(d)** amorphous metal-oxide. Taken from [26].

The nature of conduction in crystalline and amorphous Si is known to be anisotropic. However, in amorphous Si, the presence of a disordered conduction leads to the formation of localised states above the VBM and below the CBM, which contributes to the low carrier mobilities. In quantum mechanical terms, a localised state is defined as a state of motion where an electron can be found in any location within an area of a material of linear extent

smaller than that of the material (e.g. states near the fermi energy). On the other hand, for metal-oxides, the close proximity of the large metal ns orbitals (for both ordered and disordered states) contributes to an efficient electron transport and thus, a higher carrier mobility.

Although this particular electronic structure of metal-oxides permits the charge transport mechanism, the presence of the large bandgaps prevents the thermal generation of carriers leading to the low carrier densities. As such, further mechanisms are necessary in order to improve and explain the conductivity of metal-oxides, which is usually related to the non-stoichiometric nature of the oxide systems[31]. Till date, the existence of native point defects, such as metal interstitials (M_i) and/or oxygen vacancies (V_o) in n-type metal-oxides is considered to the cause for the high conductivity. Other possible ways of enhancing the conductivity include the growth of these materials under oxygen deficient, metal rich environment and by intentionally doping the host oxide (by adding impurities), enabling a better control on the electrical properties of the oxide semiconductors.

2.1.2 Charge transport

The figure below shows the different mechanisms involved in the charge transfer.

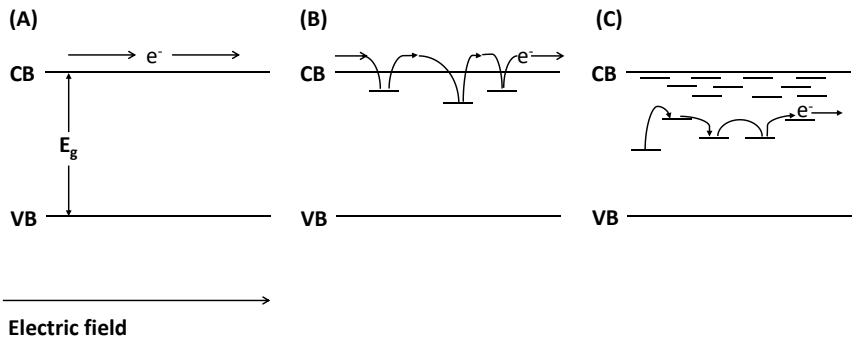


Figure 4: Schematic sketch of **(A)** band-like, **(B)** trap and release-like, and **(C)** hopping-like transport mechanisms.

A band-like transport is usually seen at or around room temperatures for inorganic crystalline semiconductors that are highly ordered and almost defect-free, such as Si and Ge and some metal-oxides. The excitation of charge carriers from the valence band (VB) into the conduction band (CB) can take place either thermally or by the presence of photons. Moreover, by introducing dopant atoms into the semiconductor material, additional carriers can be induced causing the formation of electronic states near the band edge.

The second transport process is called the multiple trap and release (MTR), in which the carriers are trapped in electronic states inside the bandgap and eventually released into the CB within a time frame depending on the distance between the trap state and the band edge relative to the available thermal energy. The states can be induced by lattice defects (presence of grains) and dangling bonds and can behave either as donor or acceptor states. This mechanism is usually observed in polycrystalline materials characterised by additional localised electronic states within their bandgap.

Finally, the hopping-like transport is common in materials like a-Si:H or polymeric organic semiconductors at room temperatures and metal-oxides at lower temperatures. The existence of a high number of states within the bandgap leads to the misalignment of the fermi level (E_F) and CB, causing the transport to happen via hopping along/between the localised states. For materials with hopping-like transport, the linear mobility is dependent on the field applied, which indicates an increase in the mobility with increasing V_{GS} (voltage applied to the gate electrode). This observation is based on the assumption that the density of trap states within the bandgap starts increasing with decreasing distance to the CB, which is why at low V_{GS}, mobility values are smaller due to the existence of a large energetic and spatial distance between the localised states in the bandgap. On the other hand, at a high

V_{GS}, more carriers are injected into the semiconductor filling up more states, causing the E_F to shift towards the CB. The injected charge carriers are much faster because of the smaller energetic and local distance of the states in the bandgap, thus leading to higher mobility values.

Activation energy (E_A), defined as the energy required by the carrier (electrons or holes) to overcome a potential barrier in order to complete a conduction process, is a key parameter for charge transport in semiconductors and can be determined via temperature dependent measurements. The analysis of these measurements indicates different types of mechanisms dominating a material within a temperature range, namely percolation conduction (PC) and trap limited conduction (TLC), discussed in detail in Chapter 4.

2.2 Thin-film transistors (TFTs)

A transistor is a three terminal device, namely, the source, drain and gate electrode and is commonly used as a switch in digital logic circuits. It also includes a semiconducting material deposited between the source and drain electrodes, and a dielectric layer (also known as the insulating layer) between the semiconductor and gate electrode. There are different transistor structures [Fig. 5 (A-D)] available depending on the relative position of the three terminals with respect to the semiconductor, such as bottom-gate top-contact (BG-TC), bottom-gate bottom-contact (BG-BC), top-gate bottom-contact (TG-BC), and top-gate top-contact (TG-TC), with each structure having their own advantages and disadvantages depending on the materials used for device fabrication. A major disadvantage of the BG-TC configuration is the presence of parasitic capacitance leading to a slow response of the devices and circuits. Additionally, in the bottom-gate configuration, the semiconductor layer

is usually exposed to air (or the surrounding atmosphere) which can introduce undesirable effects, such as adsorption, diffusion and desorption of gases. However, this characteristic/property can also be used to explore or modify properties of the layer, e.g. by adsorbing impurities during annealing via plasma treatment, and/or to study the impact of the device being exposed to different gaseous species in the atmosphere. Furthermore, the processing of BG-TC structures is relatively easier compared to the other structures. All the investigations in this thesis were conducted in the BG-TC transistor structure.

Thin-film transistors (TFTs) are a special type of field-effect transistors (FETs) fabricated by depositing thin films of metallic contacts, a dielectric layer and a semiconductor layer onto a substrate.

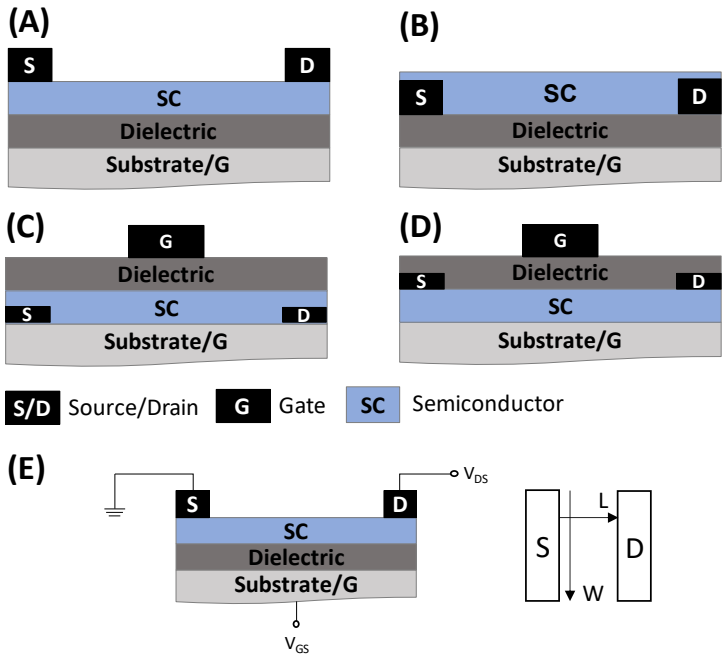


Figure 5: (A) – (D) Different transistor structures, **(E)** Schematic of a BG-TC transistor.

In Fig. 5 (E), the channel length (L) is the distance between the source and the drain electrodes and the channel width (W) is the distance over which the source contact and

drain contact run parallel with respect to each other, with the resultant area of the transistor channel given by L × W. The length (L)/width (W) of the transistors characterised in this work were 100 µm/1 mm (for results in Chapters 4 and 5) and 40 µm/1 mm (for Chapters 6 and 7).

Since the semiconductors used in this thesis were all n-type materials, i.e. materials showing electron conduction, the working principle of n-type transistors will be considered. By applying a positive voltage to the gate electrode (V_{GS}), the charge carriers (electrons) are attracted due to the electric field resulting from the applied V_{GS} leading to the formation of a conductive channel at the dielectric/semiconductor interface. The formation of the channel is aided by the accumulation of the delocalised electrons due to the voltage drop across the dielectric and semiconductor. Additionally, biasing the drain terminal with a small voltage (V_{DS}) causes the electrons to flow from the source to the drain terminal, via the field-induced channel, thus resulting in a current flow (I_D) through the device. This current is modulated by the accumulation of electrons at the dielectric/semiconductor interface (also known as the field-effect), a principle similar to metal-oxide-semiconductor-field-effect-transistors (MOSFETs). In other words, the channel resistance is controlled by the applied gate voltage with the channel acting as a variable resistor and I_D being directly proportional to V_{DS}. This behaviour is only valid when $V_{DS} << V_{GS} - V_{TH}$ and $V_{GS} > V_{TH}$, where V_{TH} is the threshold voltage and defined as the minimum gate voltage required to induce mobile electrons at the dielectric/semiconductor interface for accumulation to take place in the channel and thus leading to the formation of the conductive route between the source and drain terminals. This is called the linear operating region where I_D increases linearly with V_{DS}. On the contrary, when a negative voltage is applied to the gate, the mobile electrons are

removed from the interface leading to a reduction in conductivity, also known as depletion. The I_D for the linear mode of operation is given by the equation[14,18]:

$$I_D = \mu C_{OX} \frac{W}{L} (V_{GS} - V_{TH}) V_{DS} \quad \textbf{(1)}$$

where C_{OX} represents the gate capacitance per unit area, and μ is the channel linear mobility.

When V_{DS} starts increasing and the condition $V_{DS} << V_{GS} - V_{TH}$ is no longer valid, the channel resistance increases as well. Eventually, it reaches the point where $V_{DS} = V_{GS} - V_{TH}$, causing the depletion region to be more dominant and the depth of the channel at the drain terminal becomes zero resulting in pinch-off (defined as the threshold voltage below which the TFT is turned off). Beyond this point, I_D remains constant even with an increase in V_{DS} and this is known as the saturation operating region of the transistor. The depletion region is the insulating area where there are no excess mobile electrons present, with a large depletion region implying no current flow through the TFT. The saturation drain current can be obtained by the equation[14,18]:

$$I_D = \mu C_{OX} \frac{W}{L} \frac{(V_{GS} - V_{TH})^2}{2} \quad \textbf{(2)}$$

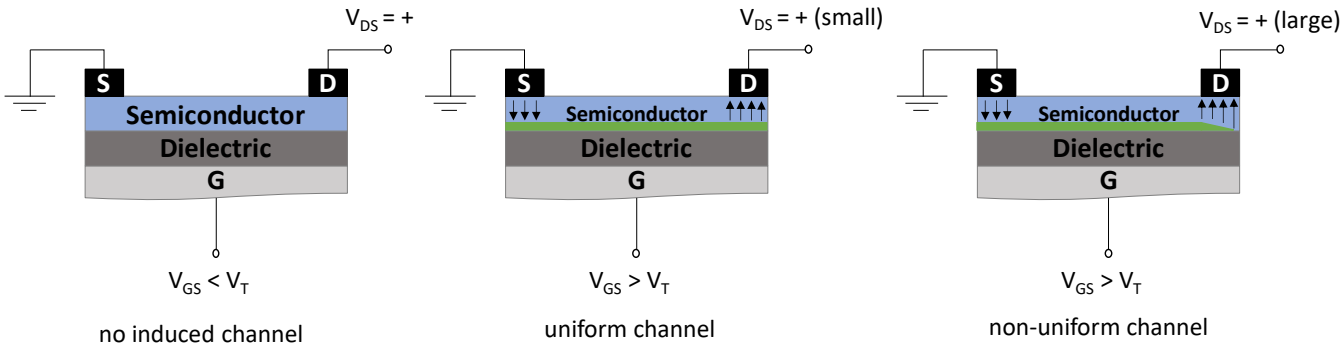


Figure 6: Ideal n-type TFT operation.

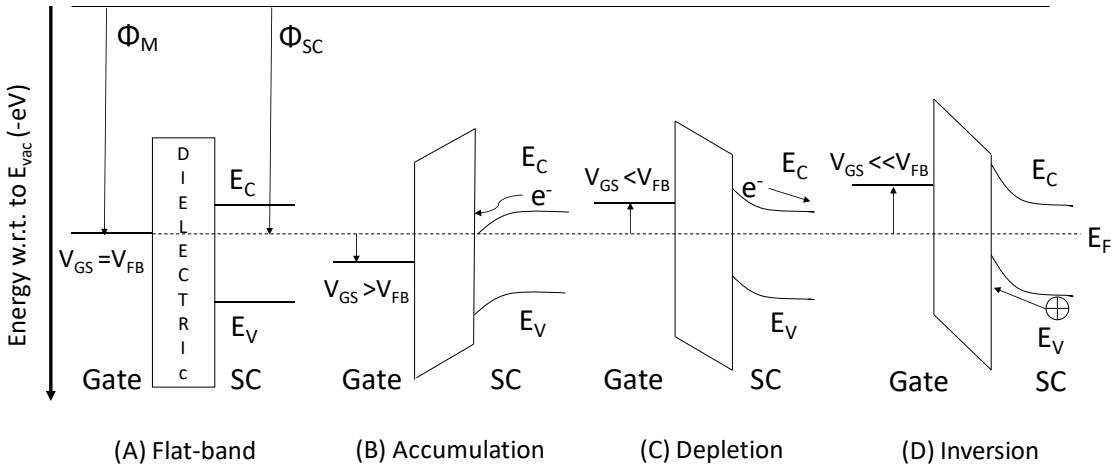


Figure 7: Schematics for different operating modes for n-type TFT illustrating the different operating regimes: **(A)** flat-band, **(B)** accumulation, **(C)** depletion, and **(D)** inversion.

To help understand the working principle in more detail, it is important to analyse the band diagram of the structure formed by the gate electrode, dielectric layer and semiconductor layer at diverse gate voltages (V_{GS})[32].

The external field induced by the gate electrode can lead to four different regimes by which the semiconductor's conductivity can be modified. These regimes are better known as the **(A)** equilibrium or flat-band state, **(B)** accumulation region, **(C)** depletion region, and **(D)** inversion region, as shown in the figure above for a n-type semiconductor. In case **(A)**, the fermi levels (E_F) of the gate electrode and semiconductor are in equilibrium, i.e. they are aligned and there is no band-bending happening within the semiconductor. In this instance, the work functions of the gate and semiconductor material match (V_{FB} = 0 V), due to which the conductivity of the semiconductor is equal to its intrinsic conductivity when there is no external electric field applied. When a positive external voltage is applied at the gate electrode ($V_{GS} > V_{FB}$), as in case **(B)**, the voltage across the dielectric and semiconductor drops leading to the downward band-bending and accumulation of the delocalised

electrons, causing an increase in the conductivity. This downward band-bending is even more distinct when $V_{GS} >> V_{FB}$. In case **(C)**, upon the application of a negative gate voltage ($V_{GS} < V_{FB}$), the mobile electrons are repelled from the interface causing the depletion of electrons in the channel and hence the upward band-bending. In theory, if the V_{GS} is decreased even further ($V_{GS} << V_{FB}$), holes (minority charge carriers) start accumulating at the interface, as shown in **(D)**. This is known as the inversion regime. However, this behaviour essentially never happens in metal oxide TFTs.

Fig. 8 below illustrates the two most important electrical measurements describing a TFT performance, the transfer and output characteristics.

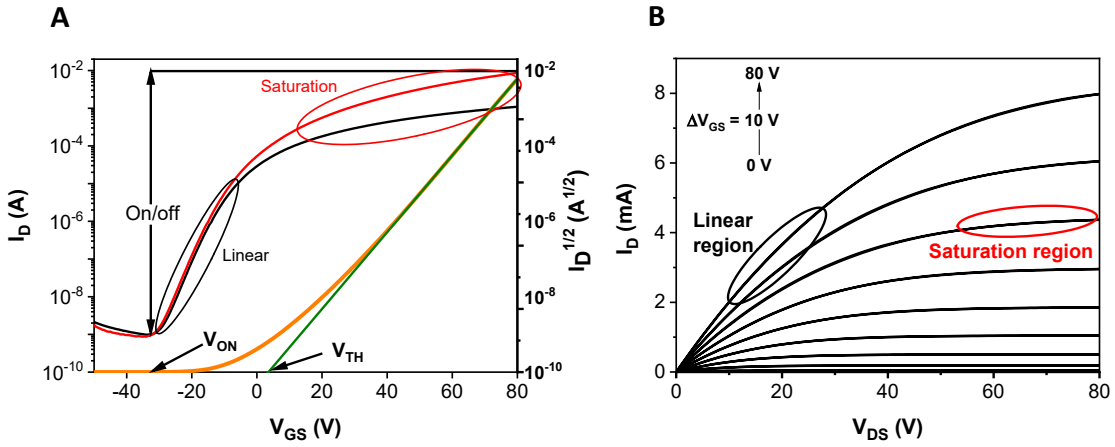


Figure 8: (A) Transfer characteristics (measuring I_D as a function of V_{GS} at a fixed V_{DS}), **(B)** Output characteristics (I_D vs. V_{DS} at varying V_{GS}) of a n-type TFT.

Certain important parameters can be extracted from the transfer characteristics, such as linear mobility (μ_{lin}), saturation mobility (μ_{sat}), onset voltage (V_{ON}), threshold voltage (V_{TH}), drain (channel) current on/off ratio, and subthreshold swing (SS), to provide an estimation of the device performance. The field-effect mobility in the two different operating regimes can be calculated using the gradual channel approximation[14,18]:

$$\mu_{lin} = \frac{L}{WC_i V_{DS}} \frac{\partial I_{D,lin}}{\partial V_{GS}} \quad (3)$$

$$\mu_{sat} = \frac{L}{W C_i} \frac{\partial^2 I_{D,sat}}{\partial V_{GS}^2} \quad (4)$$

with channel length L and width W, dielectric capacitance C_i per unit area, and drain and gate voltage V_{DS} and V_{GS}, respectively.

The onset voltage (V_{ON}) is the voltage at which the I_D starts increasing abruptly above the off-current level. The extraction of V_{TH} is done by extrapolating the linear fit of the square root of the saturation drain current, $I_{D(sat)}^{1/2}$, to the x-axis of V_{GS}, as shown in the transfer curve above. An important region, known as the subthreshold region, is the region between V_{ON} and V_{TH}, with the corresponding operation defined as subthreshold conduction. The subthreshold swing (SS) gives information about trap density and the switching behaviour of the transistor and thus, a smaller value for SS is desirable for electronic applications. SS is defined by the equation:

$$SS = \frac{\partial V_{GS}}{\partial (log I_D)} \quad (5)$$

Different factors are responsible for the on-state current and off-state current in the drain current on/off ratio. While the on-state current primarily depends on the semiconductor mobility and capacitance of the gate dielectric material, the magnitude of the off-state current is determined by the gate dielectric material utilised. By employing a robust dielectric material, a large leakage current through the gate can be prevented during transistor operation. However, the presence of un-patterned semiconductor layers and gate electrodes can lead to a high gate leakage due to the bulk conductivity of the semiconductor and conduction pathways at the substrate interface, respectively. A high on/off ratio in

transistors is desirable for a clean and clear switching behaviour, with typical values in the range of 10^6. These high values are often necessary for TFTs to be successfully used as electronic switches.

2.3 High-electron-mobility transistors (HEMTs)

One of the most commonly used semiconductor devices is the high-electron-mobility transistor (HEMT)[33], also known as the modulation-doped FET (MODFET). HEMTs rely on the field-effect modulation of the high-mobility two-dimensional electron gas (2DEG) formed at the heterointerface consisting of selectively doped semiconductor pairs with different bandgaps (E_g), such as GaAs/AlGaAs[34] (Gallium Arsenide/Aluminium Gallium Arsenide). Such devices are known to exhibit exceptional charge transport properties, with enormous carrier mobilities and as such higher switching speeds.

The staggering carrier mobilities and switching speeds of the HEMT devices can be attributed to the wide bandgap element being doped with donor atoms, and hence the presence of excess electrons in its conduction band. An important aspect of the HEMT devices is the ability to modify the band discontinuities across the CB and VB separately, allowing an accurate control over the electrons flowing in and out of the device. As electrons are the main carriers required in HEMTs, a process of graded-doping is applied in one of the materials which causes the conduction band discontinuity to be smaller while the valence band discontinuity remains the same. This leads to the diffusion of electrons into the CB of adjacent material with a narrow bandgap, causing a change in the potential and thus creating an electric field between the two materials. The resulting field causes the electrons to be pushed back to the CB of the wide bandgap material and this diffusion

process carries on until the electron diffusion and electron drift balance reach an equilibrium state. Due to this, a junction at equilibrium similar to a p-n junction is created with the undoped narrow bandgap material in possession of excess majority charge carriers, which yields the high switching speeds of the HEMTs. Additionally, since the low bandgap material is undoped, there are no donor atoms present for scattering to take place, which in turn results in the high mobilities.

The first HEMT device was based on AlGaAs/GaAs and was developed by Takashi Mimura and his colleagues in 1980[35], following efforts to demonstrate metal-oxide-semiconductor field-effect transistors (MOSFETs) based on GaAs. In a superlattice consisting of multiple alternating thin layers of undoped GaAs and n-type AlGaAs, the electrons generated by the donors in AlGaAs layer are transferred into the GaAs layer forming a depleted AlGaAs layer. This is because of the fact that heterojunctions formed by materials with different bandgaps form a quantum well in the CB side of the undoped material. Herein, the electrons can move swiftly without any collisions or other detrimental effects due to the absence of impurities and the presence of high mobility electrons generated using the heterojunction. Once these electrons are accumulated into the GaAs potential wells, they become trapped leading to a reduced ionised donor scattering and thus, high carrier mobilities. In other words, this effect causes the creation of a very thin layer with a high concentration of mobile electrons, causing the channel to have a very low resistivity or high electron mobility.

3. DEVICE FABRICATION PROCESS AND CHARACTERISATION METHODS

3.1 Device fabrication

3.1.1 Precursor solution preparation

The preparation methods of all the precursor solutions used to obtain the thin-films for this work are discussed in this section. For In_2O_3, indium nitrate [$(In(No_3)_3)$] (99.99% Indium Corporation of America) was dissolved in de-ionised (DI) water (for spray coating) and 2-methoxyethanol (2ME) (for spin coating) at a concentration of 30 mg/ml. The resulting solutions were stirred at room temperature for about an hour and overnight, respectively. For ZnO precursor solution, zinc oxide nanopowder (>97% Sigma-Aldrich) was dissolved in ammonium hydroxide (50% v/v; Alfa Aesar) at 10 mg/ml and stirred at room temperature overnight. The Al:ZnO (Al-doped-ZnO) solutions were prepared by adding a high-purity Al pellet (size 3 mm diameter $\times$ 3 mm height, 99.999% Kurt J. Lesker) into the ZnO precursor solution for a set period of time (till the Al pellet was removed from the solution). Before deposition, the resultant solution was filtered using 0.45 µm PTFE filters to make sure the solution was free of any impurities or residues. For the Li:ZnO (Li-doped-ZnO) solutions, Lithium acetate ($LiOOCCH_3$) was dissolved in ammonium hydroxide yielding Lithium acetate solution. The Li-doping process was completed by blending the ZnO precursor solution with the Lithium acetate solution at appropriate wt%.

For the preparation of the OMD (organic molecular doping) precursor solutions discussed in Chapter 5, a fullerene derivative, i.e. [6,6]-phenyl-C_{61}-butyric acid methyl ester ($PC_{60}BM$, 99.5%, Solvenne BV) was dissolved in chlorobenzene (CB) at 20 mg/ml and stirred at room temperature for 30 mins. For the C_{60}:C_{70} blend precursor solution, unsubstituted C_{60} (99.5% Sigma-Aldrich) and C_{70} (99% Solvenne BV) fullerenes were dissolved in 1,2-Dichlorobenzene (DCB) at a concentration of 10 mg:10 mg in 1ml of DCB and stirred at room temperature for 60 mins. For the study of the doping effect, the molecular dopant, (4-(1,3-dimethyl-2,3-dihydro-1H-benzoimidazol-2-yl)phenyl)dimethylamine (N-DMBI, 98% from Sigma-Aldrich, 1 mg/ml in CB), was added to the resultant fullerene and fullerene derivative solutions in the molar ratios ranging from 0.005% to 2% to form the OMD precursors.

The high-κ oxide dielectric solutions were prepared by dissolving (i) Yttrium oxide nanoparticles (10% weight) stock solution in iso-propanol (IPA) in the ratio 1:4, and (ii) zirconium (IV) acetylacetonate [Zr(C5H7O2)4)] (98%, Sigma–Aldrich) in N,N-dimethylformamide, (DMF, C3H7NO) (99.8%, Sigma–Aldrich), at a concentration of 90 mg/ml in inert gas atmosphere with the addition of ethanolamine (MEA, C2H7NO) (≥99%, Sigma–Aldrich) at 20 µl/ml. The resulting solutions stirred in N_2 atmosphere for 1 hour at 75 – 80° C to enhance hydrolysis. For the different blends, Y_2O_3 and ZrO_2 were mixed in different ratios with the solutions stirred under the conditions described above.

The methylammonium lead triiodide perovskite nanocrystals ($CH_3NH_3PbI_3$ NCs) used for the phototransistor work in Chapter 7 were synthesised by collaborators from the Department of Physics, University of Oxford – Dr. Yasser Hassan and Dr. Yen-Hung Lin. The preparation was done by briefly dissolving the perovskite precursor salts using the compound solvent acetonitrile (ACN) saturated with methylamine (MA). This resulted in the

blending of 0.5 M of both lead iodide (PbI_2) and methylammonium iodide (MAI) with ACN forming a black dispersion of $CH_3NH_3PbI_3$ perovskite, which was dissolved into translucent pale-yellow solution of the perovskite precursors upon bubbling dry MA gas into the ACN. This was followed by the fabrication of the NCs via the ligand-assisted reprecipitation (LARP) technique, by injecting 0.2 mL of the perovskite precursor from the ACN/MA compound solvent into anhydrous toluene (5mL) as the anti-solvent, containing 1 mL of oleic acid (OA) and 0.2 mL of oleylamine (OLAm) as ligands, while maintaining the reaction temperature at 60° C under vigorous stirring for 2 mins. Finally, the perovskite NCs were purified using an anti-solvent comprised of ethyl acetate and methyl acetate in a 2:1 ratio. Typically, the toluene colloidal solution of NCs was added to the anti-solvent in a ratio of 1:3 v/v and were centrifuged at 8000 rpm for 20 minutes to precipitate the NCs. The supernatant was discarded and the precipitate re-dissolved in toluene. This washing process was repeated twice and finally the resultant red supernatant colloidal solution in anhydrous toluene was filtered using a PTFE syringe filter (Whatman, 0.2 μm) before further use of the NCs in device fabrication.

The deposition of these precursor solutions was carried out via spray pyrolysis and spin-coating, details of which (including the deposition parameters) are described in detail in the following chapters.

3.1.2 Substrate cleaning and preparation procedure

In this study, transistors were fabricated in bottom-gate top-contact (BG-TC) structure on highly doped Silicon, Si (Si^{++}) wafers with either (400 nm ± 5%) or (100 nm ± 5%) thermally-oxidised silicon dioxide (SiO_2) (Active Business Company GmbH), acting as the gate electrode and gate dielectric (polished surface with a geometric capacitance,

C_i = 8.6 nF/cm^2 for 400 nm SiO_2 or C_i = 34.4 nF/cm^2 for 100 nm SiO_2) respectively. Other substrates used were glass slides (thermally-resistive and chemically-durable borosilicate glass, BOROFLOAT®) or polyimide (PI resin, PI 2555 HD microsystems) films (i.e. flexible substrates). To obtain the plastic substrates, the PI resin was spin-coated at 1500 rpm for 30 seconds on top of carrier substrates (Si/SiO_2 wafers or glass slides) followed by annealing at 280° C in N_2 for 2 hours (slow ramp). This step was repeated four times and the final thickness of the PI film was calculated to be 3.8 µm.

The cleaning procedure for both Si^{++}/SiO_2 wafers and glass slides was the same, which involved subsequent ultra-sonication in (i) DI water with Decon 90 detergent (Decon Laboratories) 1-3% v/v, (ii) DI water, to remove any leftover detergent from the substrates, (iii) acetone and (iv) IPA for 10 – 15 mins each. Different beakers were used for each solvent to prevent any contamination. The substrates were then dried by blowing dry nitrogen (N_2) over the surface followed by an ultraviolet (UV) ozone treatment (using UVOCS® model T0606E) for 15 mins. The UV ozone process helps to remove residual hydrocarbons from the substrate surface and improve surface energy (wettability) for the solution-based deposition methods. Afterwards, the different layers were deposited by the methods described below.

During the cleaning, fabrication and characterisation process, skin contact with the substrate or films was avoided by handling the samples with tweezers and by wearing protective nitrile gloves.

3.1.3 Spray pyrolysis and spin-coating of thin-films

There are several solution-based deposition methods available for the deposition of thin-films onto substrates[36], out of which spin-coating is the most commonly used one. Another method, ultrasonic spray pyrolysis (SP) is fairly simple to set up and well suited for upscaling,

large area deposition etc. For this work, the SP process involved using a syringe pump that delivered the precursor solution at a defined liquid feed rate to the spray nozzle where the precursor was atomised to form a fine mist of small droplets. With the aid of a filtered carrier gas (N_2), the precursor mist was then directed onto a heated surface where a chemical reaction was initiated between the constituents to forming the final metal oxide compound. The processing temperature and the droplet size are important parameters as they control evaporation, precipitate formation and vaporisation of the droplet. The liquid flow rate was set to 2 ml/min and the temperature of the surface below was 250° C, with the total time for spray deposition set at 10 mins. A stencil mask was used during the spraying to create patterned In_2O_3 layers.

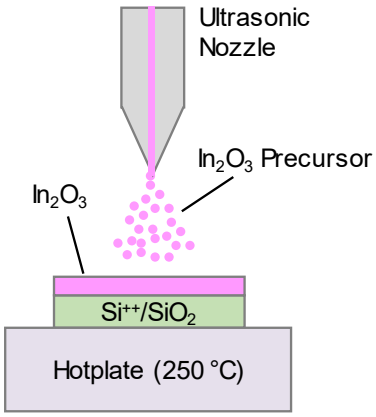


Figure 9: Schematic of an ultrasonic spray pyrolysis (SP) process.

This deposition method can be regarded similar to chemical vapor deposition (CVD), in which the droplets convert to their vapour phase as it approaches the heated surface. Alternatively, it is seen as a liquid layer-by-layer thin-film deposition method. Some important parameters controlling the effectiveness of this process and creating uniform,

smooth films include (i) solution composition, (ii) flow rate of gas and solution; (iii) nature and temperature of substrate; (iv) distance between nozzle and substrate, and (v) deposition time. SP can be considered suitable for large-area, high-throughput manufacturing without sacrificing the film quality. It also permits the blending of precursor solutions before deposition allowing the creation of films with multiple components along with effective doping, making it an advantageous deposition method[28].

In spin-coating, a precursor solution is poured onto the substrate, and a thin layer can be formed by spinning the substrate (at the required speed), for the desired film thickness. As the thickness of the film is determined by several factors, such as viscosity of the solution, spin-speed, acceleration, duration of spin, deposition conditions (environment, temperature) etc., an optimisation of spin-coating parameters is necessary to obtain a smooth and uniform film. An excessive amount (e.g. volume in excess of 200 µl) of precursor solution was used to avoid any discontinuities in coating the surface. The spin-coating process can be divided into four major stages during which the precursor solution evolves into a thin-film: (i) pouring the solution onto the substrate or wafer followed by the solution being spread over the surface due to centrifugal force (assisted by gravity), (ii) acceleration of the substrate until the desired rotation speed achieved, also called spin-up, (iii) a constant spin speed of the wafer causing the viscous forces of the solvent to control the thinning behaviour of the solution, and (iv) constant spin speed at which the wafer rotates leading to the evaporation of the solvent. The final evaporation step together with the thermal annealing at an optimised temperature leads to the formation of the solid thin-film on the substrate. Spin-coating can be regarded as the most used solution-based deposition

method for oxides due to its simplicity and the use of cost efficient materials to produce good quality films even at low temperatures.

For each spin-coated film studied in this thesis, the deposition parameters are discussed in the relevant sections of this thesis.

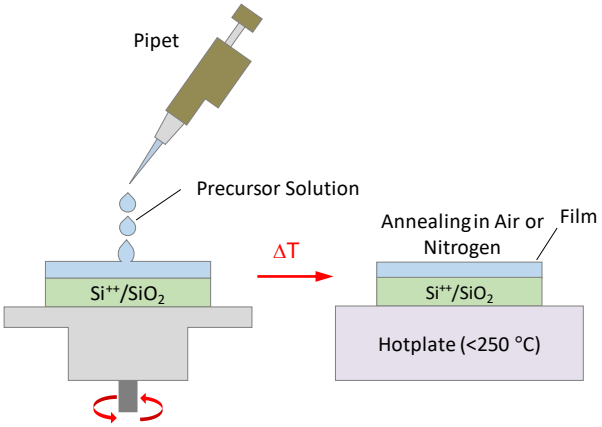


Figure 10: Schematic of a spin-coating process followed by thermal annealing.

3.1.4 Metal contact deposition

For the final fabrication step, thermal evaporation was carried out in a chamber under high vacuum (≈ 5×10^{-6} mbar) to deposit the metal (aluminium, Al) contacts (Source/Drain) onto the prepared substrates. The substrates were loaded into a substrate holder and placed inside the chamber whilst the Al metal pellet or wire was placed into a source crucible, located at the bottom of the chamber. Once the desired vacuum level had been achieved and the chamber was ready for metal evaporation, the heating element connected to the crucible was subjected to suitable voltages causing an electric current to pass through it. The voltage was applied in a way to make sure the current increases gradually over a period of time to avoid any damage to the crucible from thermal shock. Due to the voltage applied and electric current passing through the crucible, the metal would first melt and then

evaporate. The evaporated metal vapours passed through shadow masks (necessary to acquire specific patterns) onto the substrates. The vacuum present ensured an effective evaporation by directing the vapours to the substrates, where they condensed back to the solid state. In the absence of the high vacuum or when evaporation is performed close to atmospheric pressure, the metal deposition is usually non-uniform creating uneven or discontinuous layers. With the help of a crystal sensor present inside the chamber, the deposition rate (0.5 – 1 A/s) and power supply to the crucible was monitored accordingly. The final thickness of the Al contacts was 50 – 70 nm and for the transistor design, channel lengths and widths were 30 – 100 µm and 1000 µm, respectively.

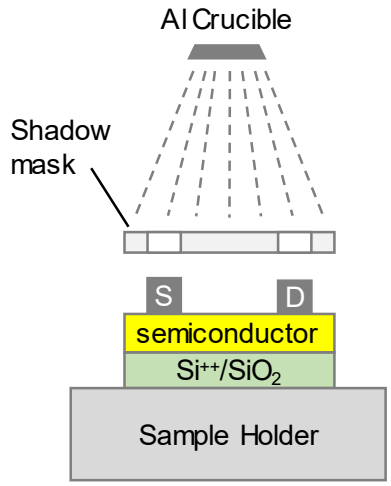


Figure 11: Schematic of a thermal evaporation process to deposit metal contacts (Al S/D).

3.2 Electrical characterisation

3.2.1 Current – Voltage (I-V) measurements

Out of the different electrical characterisation methods known, the analysis of data acquired from experimental current – voltage (I-V) measurements are the main sources to assess TFT performance. Through these measurements and the acquired data, the fundamental

parameters for a TFT, discussed earlier in Chapter 2 can be determined and/or extracted. The I-V measurements were carried out using an Agilent B2902A or a Keithley 4200-SCS semiconductor parameter analyser (SPA) together with a probe station, fitted with four source/measure units (SMUs). Each of these units can be connected to the terminals of an electronic device (TFTs, in this case) via a micromanipulator probe and can be used to provide simultaneous high accuracy and high resolution I-V measurements. Different testing conditions were used to measure different TFTs, depending on the required performance: (i) in an inert gas (N_2) atmosphere (with O_2 and H_2O levels < 10 ppm), (ii) under high vacuum (≈ 10^{-5} mbar), (iii) at room temperature, in a dark environment, and (iv) different temperatures. To control and set different temperatures, a cryogenic probe station (Janis Research, ST-500) was used to cool down samples with liquid N_2 under high vacuum (≈ 10^{-5} mbar).

Optoelectronic characterisation for phototransistor devices demonstrated in Chapter 7 was carried out inside a nitrogen filled glovebox by measuring the transfer characteristics under dark conditions and under various light illumination intensities from three LEDs (red, λ_{peak} = 630 nm; green, λ_{peak} = 525 nm; and blue, λ_{peak} = 432 nm). The LEDs were driven via a Keithley 2400 source meter, while the illumination intensities (E_{opt}) that was generated by LEDs at varying current levels was measured using a Thorlabs S120UV power sensor. For dynamic characterisation of the same devices, change in the transistor channel current due to an external optical stimulus (light pulse) was measured. This was done by biasing the device at fixed V_{DS} and V_{GS} using an Agilent B2902A SPA, similar to electrical characterisation. The variation in channel current was subjected to amplification by a Stanford Research Systems SR570 current preamplifier, and then recorded by an Agilent

DSO6014A oscilloscope. Different LEDs driven by an Agilent 33220A function generator were used to generate the optical pulses.

The results obtained from the measurements were recorded and saved into a spreadsheet file and thoroughly analysed using the software Origin (OriginLab).

3.2.2 Capacitance – Voltage (C-V) measurements

Impedance spectroscopy measurements, such as the capacitance–voltage (C-V), are used to acquire geometrical capacitance values of gate dielectrics as well as the charge profiling (distribution of charge) within semiconductor layers. In this thesis, C-V measurements were carried out on metal-insulator-semiconductor (MIS) structures to study the charge distribution throughout different semiconductor films. The fabrication and evaluation of the MIS devices were carried out similarly to previously reported work[37], using the following structure (shown in Fig. 12 below): thermally evaporated Al bottom electrode (which was oxidised via UV/ozone exposure creating a 2 – 4 nm thick layer of Al_2O_3), solution-processed ZrO_2 film, semiconductor layers sequentially deposited by either spray pyrolysis or spin-coating, thermally evaporated Al top electrode.

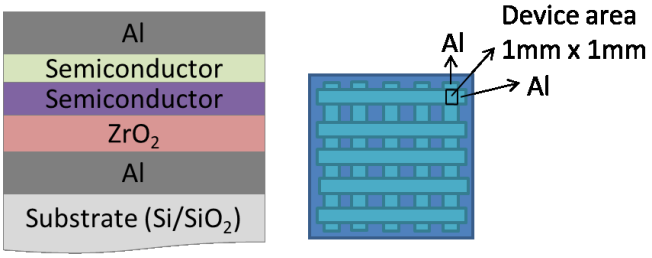


Figure 12: Schematic of a MIS structure for C-V Measurements, left: cross section and right: top-view.

The charge profiling or the apparent free carrier concentration ($N_{C\text{-}V}$) was obtained using the MIS structure together with a parallel-plate capacitor configuration[37],

$$N(x) = \frac{2}{e\varepsilon_r\varepsilon_0 A^2 \frac{d(1/C^2)}{dV}} \quad (6)$$

As a function of depth (x) from the top electrode:

$$x = \frac{\varepsilon_r\varepsilon_0 A}{C} \quad (7)$$

where ε_r is the semiconductor permittivity, ε_0 the vacuum permittivity, *A* the active area, *C* is the capacitance value of the insulator, *V* is the voltage applied and e the charge of an electron.

3.3 Material/optical characterisation

3.3.1 Atomic force microscopy (AFM)

Atomic force microscopy or AFM, a well-known material characterisation technique, works by combining the principles of the scanning tunnelling microscopy (STM) and stylus profilometry principle to provide surface profiles (roughness and morphology) of high resolution (nanoscale) for materials and devices. In the earlier versions of AFMs, the cantilever oscillation was detected using a tunnelling current (essentially putting at STM on top of the cantilever) as opposed to the laser system used nowadays. Unlike STM, which can only be used to image conducting or semiconducting surfaces, AFM has the capability to image non-conducting surfaces, oxides and even biological samples, making it an advantageous tool.

A typical AFM system setup consists of a sharp tip (made of Si or Si_3N_4) mounted on a flexible cantilever, a helium-neon laser and a position-sensitive photo-detector (PSPD). The cantilever, which is applying a very low force onto the substrate, scans across the sample

surface in a rastering fashion, line by line. While scanning the tip can be attracted or repelled due to inter-atomic forces taking effect especially where the sample surface topography changes. From the amount of cantilever deflection the surface height of the sample can be determined at any given point within the rastered area. To measure the degree of deflection, the laser beam is focused on the tip of the cantilever and the reflected beam recorded by the PSPD. Any change of deflection angle of the tip results in a corresponding change of signal being picked up by the photodiode.

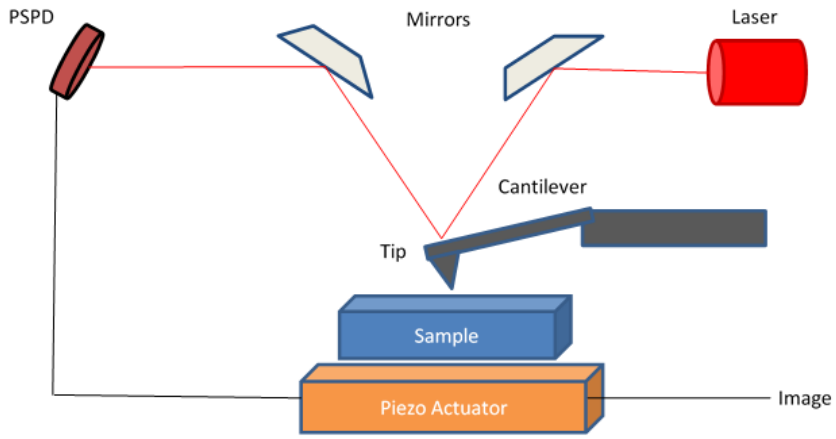


Figure 13: Schematic of an AFM system.

The three operational modes for a standard AFM are non-contact, intermittent contact and contact mode. Out of those three, the intermittent contact mode, also called the tapping mode or AC mode is the most common method used to image surface profiles due to (i) the effective scans, especially for large area scans, (ii) reduced chances of sample damage, especially for soft samples, and (iii) the ability to overcome particular limitations of the other modes. In this study, all AFM measurements were done in the intermittent contact mode using an Agilent 5500 AFM system in air to image surface topography/study film morphology.

3.3.2 Transmission electron microscopy (TEM)

Another microscopy technique used in this thesis was transmission electron microscopy (TEM). A beam of electrons is sent towards an ultra-thin sample and the spatially distributed intensity of the beam after its transmission is recorded with a suitable detector. The acquisition of high-resolution images at the nanoscale is possible due to the small de Broglie wavelength of electrons. Additionally, a different imaging mode of the TEM, called high-resolution TEM (HRTEM) can be used for direct imaging of atomic structures for samples via phase contrast imaging techniques. This microscopy method can also be used to measure electron diffraction patterns, which would assist in investigating crystal structures of a solid sample.

For this work, the TEM images and analysis were performed by collaborators from two research groups/institutes: (i) Prof. Aram Amassian and his colleagues at King Abdullah University of Science and Technology (KAUST), Saudi Arabia for the TEM results in Chapter 4, and (ii) Dr. Martyn McLachlan and his colleagues at Imperial College London, UK for the results in Chapter 5. For the bi-layer TFTs in Chapter 4, a Titan 80-300 Super Twin microscope (FEI Company) operating at 300 kV and a JEOL 2011 electron microscope operating at 200 kV were used to perform HRTEM imaging and analysis. A Charged couple device (CCD) camera (Model: US4000, Gatan Inc.) was used to record HRTEM images. Two TEM sample preparation techniques were used as follows: (i) ion beam milling (Ga ion beam, 30 kV, and 9 nA) to cut a specimen from the bulk sample, which was then attached to a Cu grid in a lift-out method and further thinned down to ca. 50 nm thickness and cleaned (2 kV and 28 pA) to remove areas that were damaged during the thinning process. Before the milling process, the sample surface was protected against ion bombardment via

electron beam–assisted carbon and platinum deposition. (ii) The standard sandwich technique, followed by tripod polishing to reach a 30-nm-edge thickness. Electron transparency to less than 15 nm was achieved by precision low-voltage (5 to 1 keV) Ar^+ ion milling in a Gatan precision ion polishing system. On the other hand, for the hybrid MOD doping work in Chapter 5, cross-sections for TEM imaging were prepared by using a FEI Helios Nanolab DualBeam focused ion beam (FIB)/scanning electron microscope (SEM). The successful operation of the FIB was carried out at accelerating voltages of 30, 5, and 2 kV, while the SEM operation was carried out at 5 kV. A JEOL JEM-2100F TEM operating at 200 kV accelerating voltage was used to acquire the TEM images, to measure the thickness of the layers in the device stack and to observe their nanostructures.

3.3.3 X-ray photoelectron spectroscopy (XPS)

The most common use of photoelectron spectroscopy, such as X-ray photoelectron spectroscopy (XPS) is for surface chemical analysis. The orbital character or the original electronic states of a material can be analysed using XPS. The application of high-energy photons onto the material to be studied results in the release of photoelectrons whose kinetic energy contains information on the electronic states. An electronic analyser is necessary to acquire this information with respect to emission angles and kinetic energies. As the name suggests, XPS uses an X-ray source, which allows the study of core-levels at higher binding energies. Another type of spectroscopy, ultraviolet photoemission spectroscopy (UPS) makes use of a UV light as the photon source to study the valence band states, using information from liberated valence electrons. For the results in Chapter 4, the Core-level (CL) and valence band (VB) X-ray Photoelectron Spectra (XPS) were acquired in a KRATOS Axis Ultra DLD system equipped with a monochromated Al Kα X-ray source, a

hemispherical sector electron analyser and a multichannel electron detector. Depth profile analysis was performed by mild, destructive in-situ sputter etching using a 500 eV defocused Ar^+ beam in order to achieve the required depth resolution. The XPS measurements were acquired using 20 eV pass energy resulting in a full width at half maximum of the Ag-3d peak less than 500 meV. Spectral shifts due to charging of the surface were evaluated and subtracted based on the spectral positions of the C-1s peak of adventitious Carbon and Ar-2p peak after sputter etching.

In this thesis, the XPS measurements and analysis were carried out by Prof. Panos A. Patsalas and his colleagues at Aristotle University of Thessaloniki, Greece.

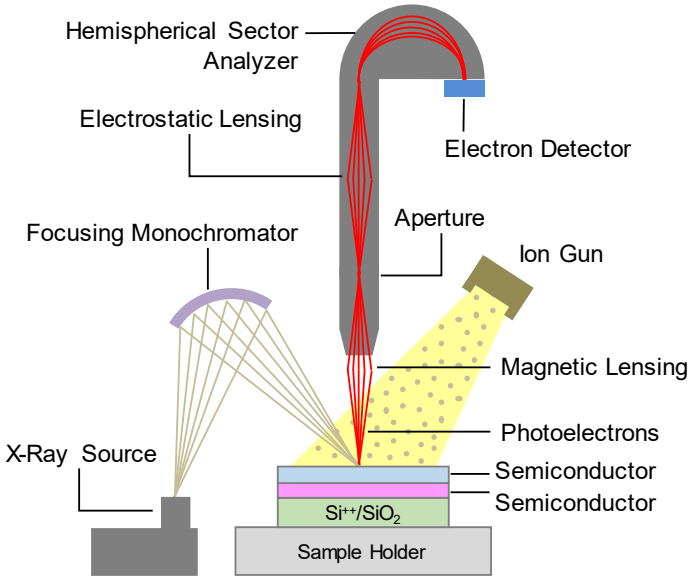


Figure 14: Schematic of XPS depth profiling measurement setup.

3.3.4 Ultraviolet-visible-near-infrared absorption spectroscopy

The optical properties (transmission, reflectance and absorption) of metal oxide thin-films were investigated using an optical spectroscopy method called ultraviolet-visible-near-infrared (UV-Vis-NIR). Absorbance spectra were calculated using the measured transmission

and reflectance data. The working principle is based on a pair of monochromatic light beams, one allowed to pass through a sample (with the transparent films) and the other one through a reference sample, in order to measure the transmitted light intensity through the film. Apart from examining the transparency of the films, UV-Vis-NIR spectroscopy can also be used to measure optical energy bandgaps. For these measurements, the films were deposited on quartz substrates from the precursor solutions to obtain accurate measurements, and the measurements were performed using a Shimadzu UV-2600 UV-vis spectrophotometer equipped with an ISR-2600 Plus integrating sphere.

3.3.5 Air photoemission spectroscopy/system (APS)

The APS or air photoemission system (model SKP5050/APS02 from KP Technology) allows measurements of the work function (Φ) with two distinct techniques, via Kelvin Probe (KP) or air photoemission spectroscopy. Work function, defined as the energy difference between the Fermi energy and vacuum level, corresponds to the minimum energy required to remove an electron from the metal. It is generally a characteristic of the surface material and also determines the electrical nature of the metal-semiconductor contacts formed (ohmic or rectifying).

The Kelvin Probe technique can perform high resolution (≈ 1 to 3 meV) relative work function measurements with respect to a reference sample with known work function value. A vibrating tip positioned in close proximity above the grounded sample acts as a vibrating capacitor device allowing a high-resolution work function measurement in a non-contact and non-destructive manner. The KP approach is especially well suited to measure relative differences between multiple samples. In this section, the first approach to measure the work-function is discussed in detail, in which the Kelvin Probe is utilised in a non-contact

and non-destructive manner. The setup resembles the situation of a parallel plate capacitor where the vibrating tip and sample constitute the respective plates. When an electrical contact is made (a bias is applied) between the Kelvin Probe tip and the sample, the alignment of the Fermi levels (which is different compared to the work functions before contact) leads to electrical charges being generated on the respective surfaces. The ability to detect these charges permits the KP to measure surface potentials while the KP tip is oscillating. A typical average distance of the tip from the sample surface is around ≈ 1 mm during measurements, while an electrical contact is connected to the sample to create the vibrating capacitor structure. As the work function is extremely sensitive to the conditions of the surface, it can be affected by evaporated or adsorbed layers, surface charging, surface reconstruction, layer imperfections, contamination of the surface, etc. Thus, the KP measurements for the oxide layers were carried out in a dry nitrogen environment chamber at room temperature directly after the fabrication process (layers deposited on ITO-glass substrates) to minimise these detrimental environmental impacts. The system used in this work was a KP Technology Scanning Kelvin Probe system, SKP 5050.

In contrast to KP, an absolute way to determine the work function of metals (or valence band/HOMO level of semiconductors) is based on the principles of photoemission in air, using a variable energy light source with a (current) detector to determine the photoelectric work-function. When a beam of light of sufficient energy is incident on a semiconducting material or a metal, electrons can be liberated from the surface of the material, an occurrence known as the photoelectric effect. The photon energy determines whether or not electrons are being liberated and hence, by adjusting the energy of the

incoming light (i.e. wavelength), the absolute work-function can be measured by detecting the ejected photoelectrons from the material. The incident photon energy (E_{ph}) is given by

$$\boldsymbol{E_{ph} = \frac{hc}{\lambda}} \quad \textbf{(8)}$$

where *h* is Planck's constant (6.6×10^{-34} J.s), *c* is the speed of light (3×10^{8} m/s) and λ is the wavelength of light (in nm).

The APS setup consists of the application module and the digital control unit which controls the motorised monochromator, subjected to a light source. A computer is used to steer the monochromator to the suitable wavelength followed by the light being fed into a fibre optic. The resulting light illuminates the sample leading to an ejection of electrons from the surface given that $E_{ph} > \Phi$. The ejected electrons are detected using a positively charged KP tip placed at a distance of ≈ 1mm from the sample. Since the tip is positively charged, it attracts the negatively charged electrons, following fundamental principles of charge interaction. This leads to the formation of a small photocurrent between the sample and the tip. Initially, it was believed that the direct detection of electrons flowing through ambient air was not feasible over such length scales. However, the current understanding is that the electrons are accelerated to the tip forming ions in the process which contribute to the photocurrent. The module control unit amplifies the photocurrent and feeds it to the Data Acquisition System (DAS) from which the absolute work function can be calculated using Fowler's photoemission analysis[38].

For this thesis, APS measurements were carried out to measure the absolute work function of a silver (Ag) sample which was used as a reference for measuring the work functions of Indium oxide (In_2O_3) and Zinc oxide (ZnO) using the KP technique.

4. HETEROJUNCTION METAL-OXIDE BASED THIN-FILM TRANSISTORS

Solution-processed metal oxide semiconductor thin-film transistors (TFTs) hold great promise for large-area electronic applications. This Chapter demonstrates the use of a low-dimensional, solution-grown In_2O_3/ZnO heterojunction instead of the conventional single-layer semiconductor channel. The results of this work demonstrate In_2O_3/ZnO TFTs exhibiting band-like electron transport, with significantly higher mobility values (≈ 45 cm^2/Vs) than single-layer In_2O_3 and ZnO transistors. The following sections analyse and discuss the findings of the work to understand the improvement in device performance.

4.1 Introduction

Due to a variety of promising characteristics of metal oxide semiconductors, like high charge carrier mobility, tunable energy band structure, optical transparency, low power consumption, and chemical stability[25,26,32,39,40], TFTs based on metal oxides have shown promise for a range of applications in the emerging field of large-area electronics. Another key advantage of metal oxides is their compatibility with solution-based processing at low temperatures[28,41] under ambient conditions. Those conditions make solution-processing a suitable method and a viable alternative in the semiconductor industry, compared to the established vacuum-based processing techniques for TFTs.

Prior to the commencement of this work, there were several reports of single layer metal oxide TFTs exhibiting electron mobilities around or exceeding 10 cm^2/Vs[42–47]. However, these oxides were often associated with defects hindering the extrinsic electron

transport properties. To overcome this limitation and to have an enhanced performance, different approaches were proposed and demonstrated[41,48,49], out of which a noteworthy strategy involved the use of multiple layers of semiconductor channels[50–54]. By using this multilayer approach and the right combination of materials, the performance enhancement can be attributed to an electron transfer and confinement at the heterointerface occurring due to a conduction-band offset[37,50,53,55]. This is a similar behaviour seen in conventional high electron mobility transistors (HEMTs) comprising AlGaAs/GaAs heterointerface channels[56–60]. In these devices, the possible formation of a two-dimensional electron gas (2DEG) at the critical heterointerface aids in the realisation of transistor devices with electron mobilities close to the theoretical limits set by the scattering of phonons when impurity scattering is absent in the semiconductor[56,57]. Recent reports provided evidence of quantised energy states in low-dimensional, solution-processed oxide layers, mainly In_2O_3[61] and ZnO[62], together with the demonstration of oxide based superlattice TFTs with electron mobilities around 25 – 45 cm^2/Vs[37]. Although promising, these TFT devices depended on complex manufacturing methods and involved elaborate multi-layered architecture designs[37,50]. Thus, to overcome this challenge in order to enhance the performances of oxide TFTs, scalable manufacturing methods yielding high quality oxide heterointerfaces was deemed necessary and also seen as a remarkable progress[28].

This study follows up on the single layer semiconductor TFTs work done by Faber et al.[47], Petti et al.[46] and Lin et al.[63,64] and reports the growth of low-dimensional solution-processed metal oxide heterostructures consisting of In_2O_3 and ZnO layers, and their implementation in TFTs exhibiting high electron mobility values. This bi-layer channel approach helped to overcome certain limitations of single layer semiconductor channel TFTs

characterised by defects. Ultra-thin (≤ 15 nm) In_2O_3/ZnO heterojunctions (HJ) were grown reliably over large areas at processing temperature < 250° C via sequential ultrasonic spray pyrolysis and spin coating methods. The charge transport in these HJ transistors was found to be superior compared to the single layer devices, with the maximum electron mobility values calculated to be ≈ 45 cm^2/Vs. In addition to the enhanced mobility values, these TFTs illustrated a dramatic change in the charge transport mechanism, details of which are discussed in the later section. The atomically sharp In_2O_3/ZnO interface and the presence of the quasi-2DEG (q-2DEG) at its vicinity causes both the change in charge transport and the enhancement of mobility.

4.2 Results

Bottom-gate, top-contact (BG, TC) transistors were fabricated on Si(Si^{++}) wafers with 400 nm SiO_2 based on solution-processed In_2O_3, ZnO, and In_2O_3/ZnO heterostructures with aluminium (Al) source/drain (S-D) electrodes. The In_2O_3 films were deposited via ultrasonic spray pyrolysis in air at 250° C, exhibiting epitaxial-like characteristics and a thickness of 4 – 7 nm, while the polycrystalline ZnO layers (6 – 7 nm) were processed via spin-coating method followed by a thermal annealing at 210° C. The In_2O_3/ZnO heterostructures were grown via sequential spray coating deposition of In_2O_3 at 250° C and spin-coating of ZnO at 210° C, respectively. The spin-coating parameters used for ZnO were 4000 rpm for 30 secs followed by the annealing step for 45 – 50 mins. The final fabrication step was the deposition of the top Al S/D electrodes via thermal evaporation under high vacuum. Fig. 15 schematically shows the fabrication steps.

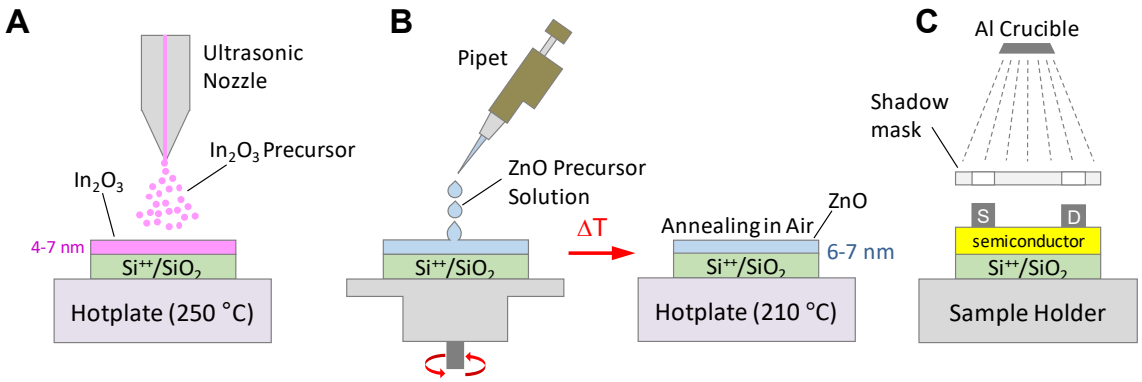


Figure 15: Material growth and transistor fabrication. **(A)** Ultrasonic spray pyrolysis used to grow the In_2O_3, **(B)** Spin-coating of ZnO followed by thermal annealing in air, and **(C)** thermal evaporation of Al S-D electrodes.

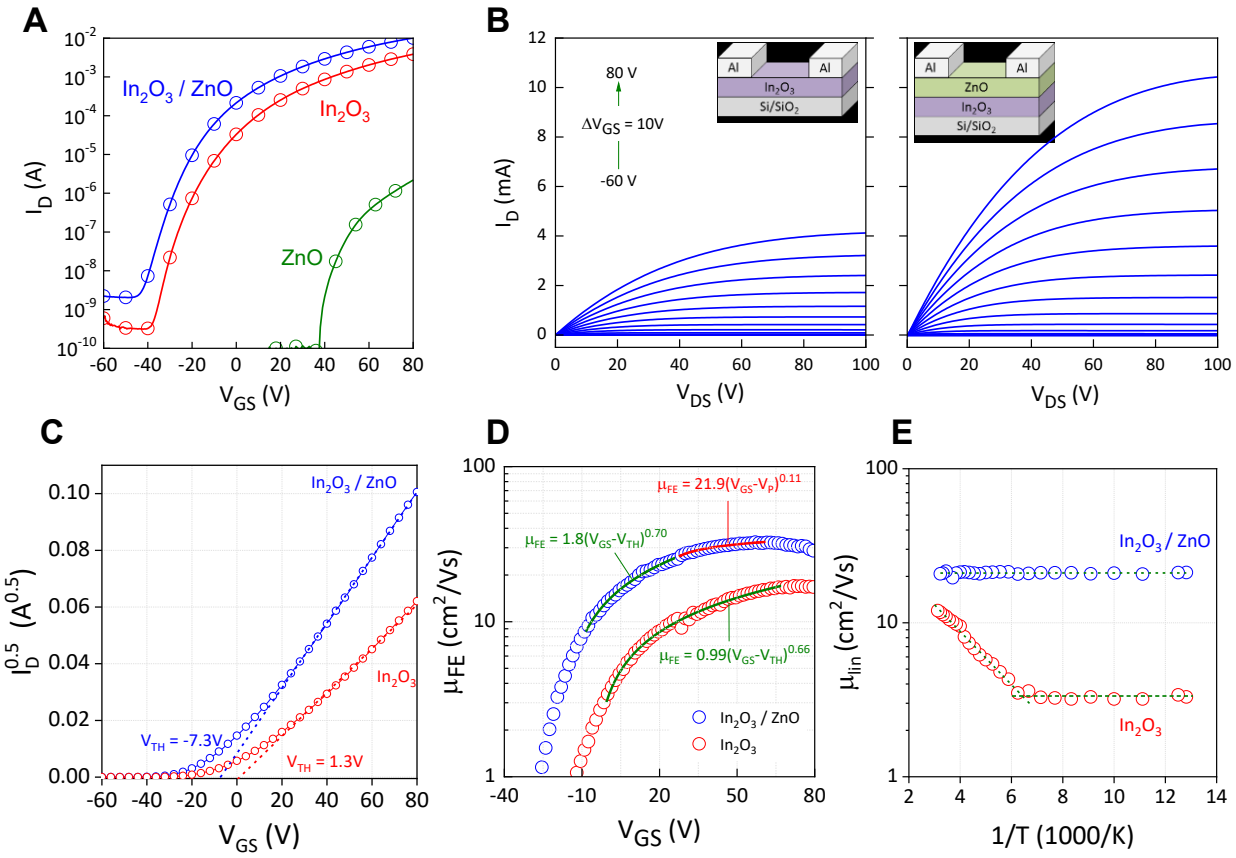


Figure 16: Electrical characterisation of fabricated TFTs. **(A)** Transfer characteristics measured in the saturation regime (V_{DS} = 100 V) for single-layer ZnO and In_2O_3 and In_2O_3/ZnO heterojunction transistors, (**B**) Output characteristics of In_2O_3 and In_2O_3/ZnO transistors, (**C**) Plots of $I_D^{1/2}$ versus V_{GS} for In_2O_3 and In_2O_3/ZnO transistors, (**D**) Gate-voltage dependence of the electron mobilities in single-layer In_2O_3 and In_2O_3/ZnO transistors, (**E**) Arrhenius plot of the electron mobility (linear) of single-layer In_2O_3 and In_2O_3/ZnO heterojunction transistors as a function of inverse temperature measured between 78 and 300 K and extracted according to Eq. 3 at $V_{GS} - V_{TH}$ = 20 V.

Fig. 16(A) shows the transfer characteristics (drain current, I_D vs. gate voltage, V_{GS}) measured in the saturation regime (V_{DS} = 100 V) of the single layer In_2O_3 and ZnO TFTs, as well as the In_2O_3/ZnO HJ device. All devices measured had a channel width, W = 1 mm and length, L = 100 µm. To benchmark the level of performance and/or to provide a reference to compare these devices, the characteristics of the single layer TFTs are analysed first.

In_2O_3 based TFTs show a typical *n*-channel behaviour with electron field-effect linear mobility (μ_{FE}) of ≈ 16 cm^2/Vs and channel current on/off ratios of 10^6, in line with previous work[47]. On the contrary, the ZnO transistors processed via spin-coating were characterised by high turn-on voltages (V_{ON}) around ≈ +40 V and a relatively low μ_{FE} of < 1 cm^2/Vs. Even though the current on/off ratio and V_{ON} for the In_2O_3/ZnO HJ TFTs were found to be similar to the In_2O_3 device, the HJ device illustrated the ability to sustain significantly higher currents, which can be attributed to the enhanced electron channel mobility values. The analysis of the transfer characteristics reveals that the HJ TFTs exhibit nearly 100 × higher μ_{FE} than the single layer ZnO devices and at least a factor of two higher than the single layer In_2O_3 transistors with average and peak μ_{FE} of ≈ 30 cm^2/Vs and > 45 cm^2/Vs, respectively. The impact of mobility on the current-driving capabilities of the transistors can be better illustrated by looking at the output characteristics of In_2O_3 and In_2O_3/ZnO devices, shown in Fig. 16(B). From the threshold voltage (V_{TH}) plot shown in Fig. 16(C) (plots of $I_D^{1/2}$ vs. V_{GS}), the HJ TFTs exhibit consistently more negative V_{TH} of ≈ -7.3 V as compared to the single layer In_2O_3 TFTs (≈ 1.3 V). This suggests the existence of a higher concentration of electrons in the channel region for the HJ TFTs, the origin of which will be discussed later. Fig. 16(D) shows the analysis of the gate-voltage (V_{GS}) dependence of μ_{FE} carried out to investigate the origins of the stark differences in electron transport measured between the single layer

In_2O_3, ZnO and that of the In_2O_3/ZnO HJ transistors. The analysis follows the power law equation[65]:

$$\boldsymbol{\mu_{FE} = K\,(V_{GS} - V_{TH,P})^{\gamma}} \quad \textbf{(9)}$$

where, V_{GS}, V_{TH} and V_P represent the gate, threshold and percolation voltages, respectively. Percolation voltage is defined as the lowest concentration/occupation probability at which an insulating material gets converted to a conductive material and is derived by plotting E_A vs. $V_{GS} - V_{TH}$, followed by a linear extrapolation to the intersection at E_A = 0 eV[37]. The prefactor *K* and the exponent γ relate to the nature of the transport mechanism. Specifically, *K* includes the percolation term from the Thomas-Fermi approximation[66] for both transport mechanisms, namely the trap limited conduction (TLC) and the percolation conduction (PC). For PC, a type of band-like transport mechanism, the contribution of the spatial characteristics of the potential barriers is also included in the prefactor *K*. The power exponent γ, on the other hand, is dependent either on the temperature (*T*) for TLC, or the spatial characteristics of the potential barriers for PC. Therefore, the different charge transport mechanisms dominating channel conduction can be predicted by the value of γ. As shown in the figure above, the fitting of the μ_{FE} evolution over a wide range of V_{GS} values for the different devices leads to an indication of the dominant conduction process. Based on the report by Lee et al.[65], it was shown that γ values close to 0.7 indicate TLC, whereas values of ≈ 0.1 imply a PC dominated transport process. From Fig. 16(D) it can be seen that the evolution of μ_{FE} for the In_2O_3 TFT yields a better fit over a wide range of V_{GS} values using γ = 0.66, implying TLC as the conduction process. For the In_2O_3/ZnO heterojunction TFTs, on the other hand, the value for γ varies from 0.7 to 0.11, for lower and higher gate fields respectively, demonstrating a transition from TLC to a PC-dominated transport process.

Additionally, a temperature dependent measurement of μ_{FE} was carried out in the linear bias regime (μ_{LIN}) to provide further evidence of the existence of the contrasting electron transport mechanisms for the In_2O_3 and In_2O_3/ZnO transistors. Fig. 16(E) demonstrates the Arrhenius plots of μ_{LIN} between the temperatures 78 K and 300 K for the two devices, from which it is evident that the In_2O_3 transistor exhibits a temperature-activated behaviour, a typical characteristic of TLC, with the μ_{LIN} remaining constant around 3 – 4 cm^2/Vs within the range of 78 K ≤ *T* ≤ 160 K, after which an exponential increase is seen to a value of 12 cm^2/Vs for T > 160 K. The presence of electron traps in the In_2O_3 layer lead to an activation energy (E_A) in the 160 ≤ *T* ≤ 300 K region of about ≈ 40 meV. A parallel trend was observed for single ZnO layer TFTs, implying the consistency with TLC as there is a temperature dependence for the γ exponent of μ_{LIN}[65]. On the contrary, the In_2O_3/ZnO heterojunction TFTs exhibit a temperature-independent μ_{LIN} across the entire temperature range used for this study, indicating that the electron transport in the heterojunction TFTs is most probably dictated by PC, which is exclusively associated with the spatial distribution of the potential barriers[65]. Thus, from the electrical measurements, it can be stated that the charge transport/conduction mechanism in single layer of In_2O_3 and ZnO TFTs was shown to be fundamentally different to the In_2O_3/ZnO heterojunction TFTs.

Further electrical characterisation was carried out to study of the effects of ambient atmosphere (nitrogen, N_2 and air) on the transfer characteristics of the In_2O_3/ZnO heterojunction TFTs and the gate-bias stress stability of the same devices. This investigation was undertaken as long-term stability is an important parameter playing a major role for any electronic device.

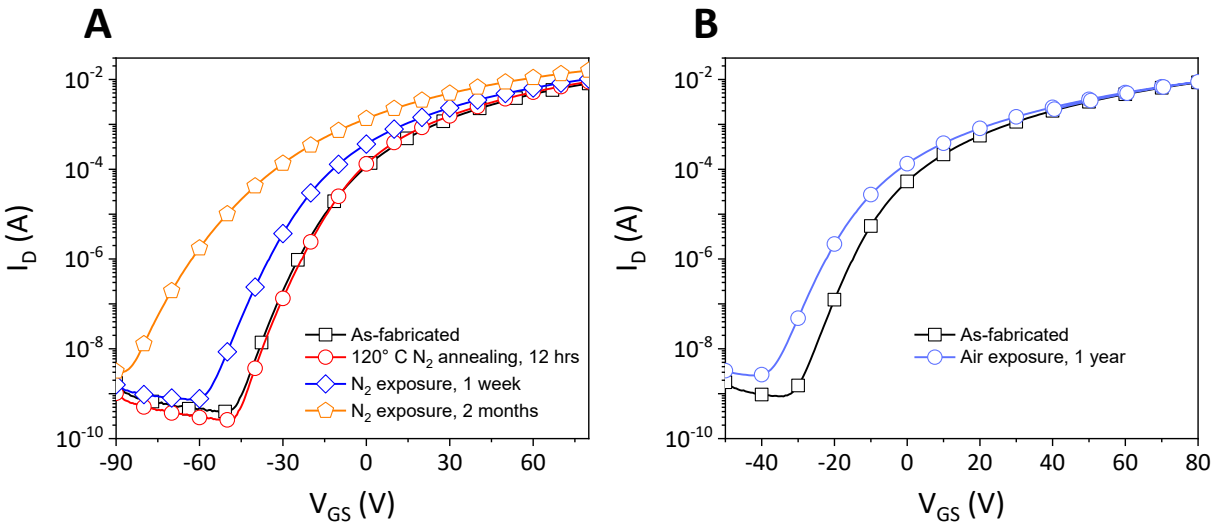


Figure 17: Transfer characteristics of In_2O_3/ZnO heterojunction TFT measured in the saturation regime (V_{DS} = 80 V) under different ambient atmosphere: **(A)** nitrogen, N_2 and **(B)** air (devices were exposed to air and then measured in a N_2 glovebox).

The figure above, Fig. 17 shows the transfer characteristics of the In_2O_3/ZnO HJ TFT after fabrication and after exposure to nitrogen, N_2 (left plot) and air (right plot) atmosphere. When the devices were annealed overnight in N_2, there is hardly any difference to the device performance, as can be seen from the black and red lines on the plot. This observation leads to the assumption that there are no additional carriers introduced in the channel or trap states created due to the annealing step. However, upon exposing the same devices to N_2 for 1 week and 2 months, there is a change – a negative shift in the turn-on voltage (V_{ON}) added with an increase in the transistor's drain current level at the on-state (I_{ON}) but without any significant alteration in the transistor's drain current at the off-state. This can be attributed to the increase in the conductivity due to the filling of electron traps, causing more current to flow through the device. Another possible explanation might be oxygen (O_2) desorption creating a back channel leading to an increase in the overall conduction. On the contrary, when the heterojunction device is exposed to air

for 1 year, there is a slight negative shift in the V_{ON} but without any change on the I_{ON} levels. A possible explanation for the shifts seen for both conditions is the doping of the semiconductor due to a slow diffusion of Al, with a bigger shift for N_2 exposure due to O_2 desorption.

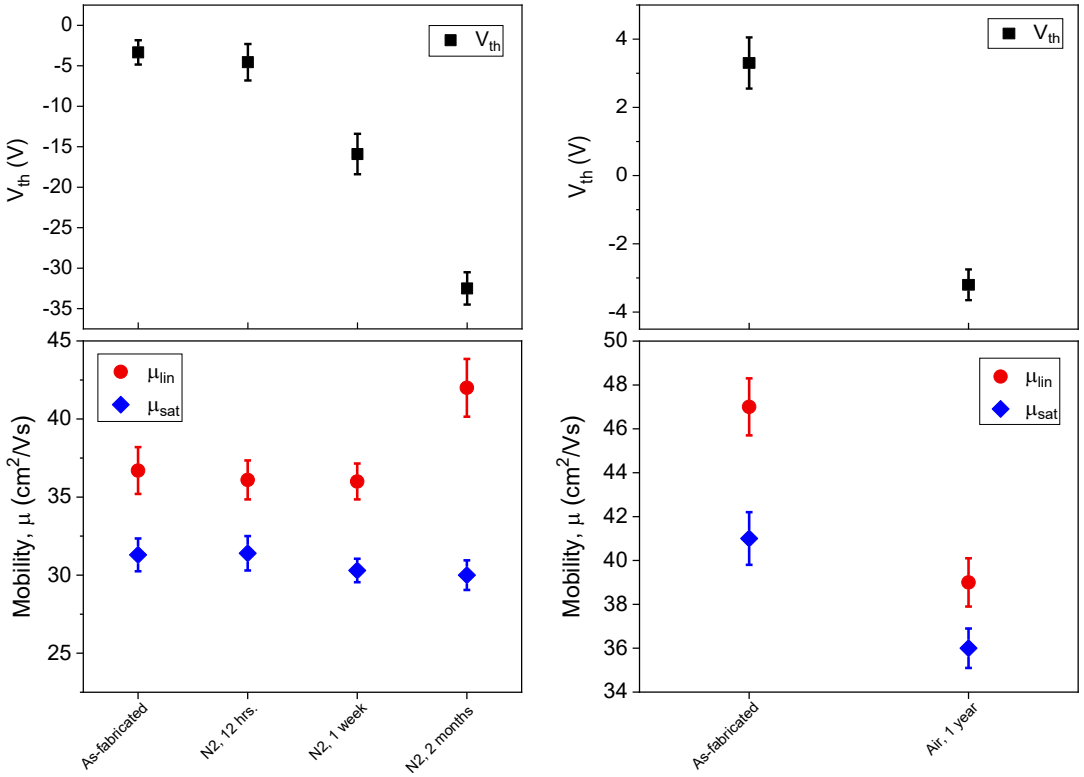


Figure 18: Evolution of V_{th} (V) and mobility (μ) for In_2O_3/ZnO TFT after exposure to different conditions.

Fig. 18 above and Tables 1 & 2 below shows the threshold voltage (V_{th}) and electron mobility (μ) for the devices after exposure to the different environments mentioned above, aiming to provide a better insight into the stability tests for the heterojunction TFTs. Even after the annealing and exposure to the different conditions, the mobility values remain high (≈ 30 – 45 cm^2/Vs), while the V_{th} decreases. This complements the transfer

characteristics shown in Fig. 17**.** Looking at the consistent and high mobility values shown in the plot and tables, it can be concluded that these devices retain their high performance even after exposure to different conditions, a remarkable fact considering the presence of inevitable defects at such low-processing temperatures.

	As-fabricated	**Overnight N_2 annealing, 120° C**	**N_2 exposure, 1 week**	**N_2 exposure, 2 months**
Threshold voltage, V_{th} (V)	-3.34	-4.56	-15.9	-32.5
Linear mobility, μ_{lin} (cm^2/Vs)	36.7	36.1	36	42
Saturation mobility, μ_{sat} (cm^2/Vs)	31.3	31.4	30.3	30

Table 1: Evolution of V_{th} and μ for In_2O_3/ZnO TFT in N_2.

	As-fabricated	**Air exposure, 1 year**
Threshold voltage, V_{th} (V)	3.3	-3.2
Linear mobility, μ_{lin} (cm^2/Vs)	47	39
Saturation mobility, μ_{sat} (cm^2/Vs)	41	36

Table 2: Evolution of V_{th} and μ for In_2O_3/ZnO TFT in air.

For the gate-bias stress measurements, the shift in the threshold voltage (ΔV_{th}) of the transparent In_2O_3/ZnO transistors under varying gate-bias stress (applied gate voltage of V_{GS} = ± 60 V and ± 40 V, drain voltage V_{DS} = 80 V) was studied under dark conditions. This

was done to avoid any light induced shifts of V_{th}. The total operation time was set to 12 hours (720 mins) with interruptions of 120 s. to measure the transfer characteristic at given time intervals. After the 12 hours of bias stress, no bias was applied over a period of 2 hours (120 mins) to see if and to what extent the V_{th} shift would recover.

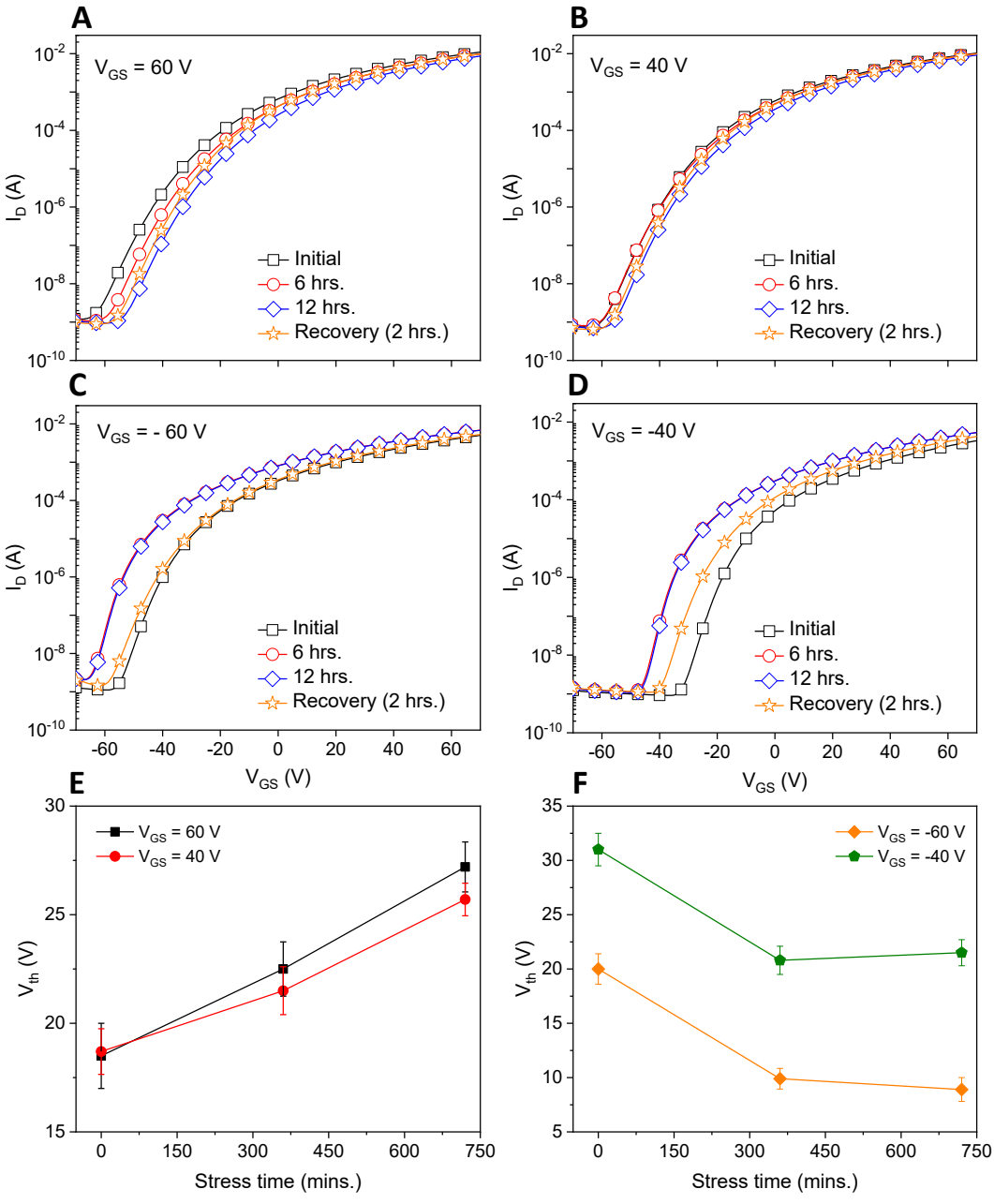


Figure 19: Gate-Bias stress stability measurements of In_2O_3/ZnO HJ TFT at different V_{GS}. **(A)** 60 V, **(B)** 40 V, **(C)** -60 V, **(D)** -40 V, and plot of V_{th} vs. stress time for various bias conditions **(E)** positive gate bias, **(F)** negative gate bias.

By applying a gate-bias stress to the devices, a maximum shift of ± 10 – 15 V in the V_{th} was seen, depending on the polarity and magnitude of the gate-bias applied but without significantly changing the drain current levels, as shown in the figure above. The shift in the voltage was also seen to be dependent on the bias-stress duration, indicating a charge tunnelling mechanism[67]. The shifts in the V_{th} can be attributed to the trapping of charges in the dielectric and/or the creation of defects in the channel layer[67–70]. For the positive shift upon the application of a positive V_{GS}, the presence of the defects in the dielectric acting as the charge trapping centres can be considered responsible. On the other hand, the negative shift seen when a negative V_{GS} is applied indicates the origin of such behaviour to be at the semiconductor/dielectric interface or semiconductor bulk material. After the recovery time, a change in the V_{th} was observed, with a positive shift for positive V_{GS} and a more prominent negative shift for negative V_{GS}. Fig. 19(E-F) summarises these results by illustrating the rate of shift in V_{th} vs. stress time for the various bias conditions.

From these results, it can be stated that the In_2O_3/ZnO heterojunction TFTs developed in this study have shown to be considerably stable under ambient conditions as well as when a bias-gate stress was applied.

To examine the origin of the different electron transport mechanisms for the different devices discussed earlier, the surface topography of each respective oxide layer was investigated using intermittent contact mode AFM.

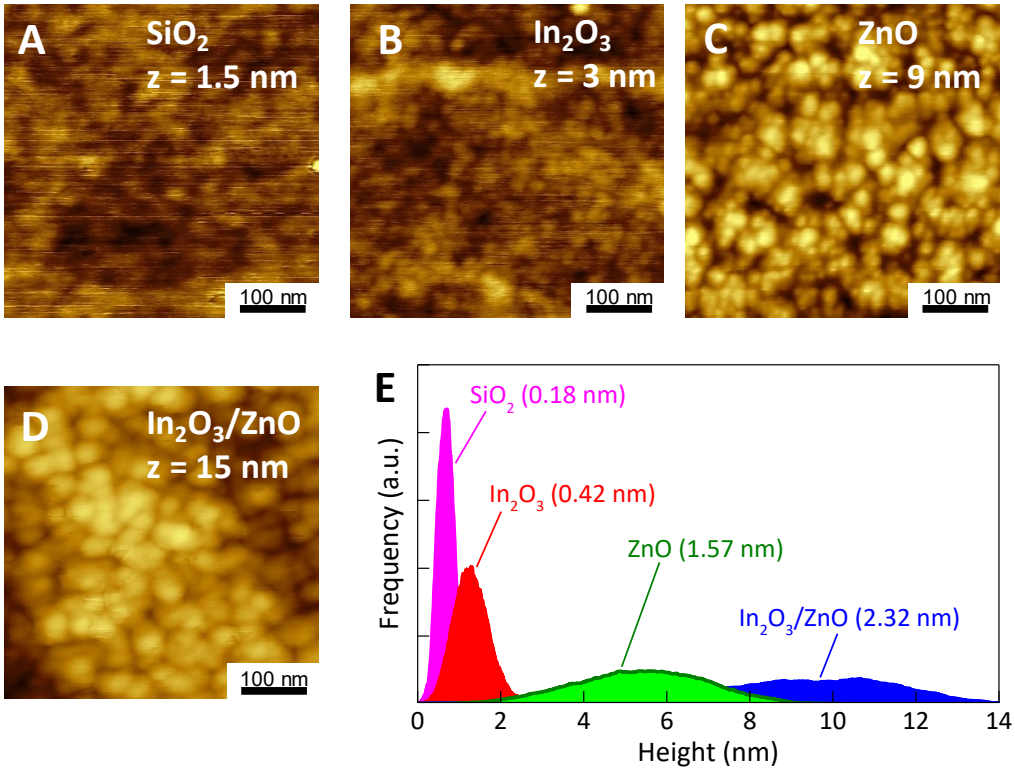


Figure 20: Surface topography of single and heterojunction metal-oxide transistor channels using AFM. High resolution AFM images for **(A)** the substrate, Si^{++}/SiO_2, **(B)** a layer of In_2O_3 deposited onto the substrate, $Si^{++}/SiO_2/In_2O_3$, **(C)** a ZnO layer on the substrate, $Si^{++}/SiO_2/ZnO$, **(D)** the heterostructure deposited on the substrate, $Si^{++}/SiO_2/In_2O_3/ZnO$, and **(E)** the corresponding height histograms of the different layers providing a better illustration of the differences between the surface topographies.

Fig. 20 illustrates AFM topography images of all the layers. The SiO_2 surface scan reveals a featureless and atomically smooth structure with a root mean square (RMS) roughness (σ_{RMS}) of around ≈ 0.18 nm, as expected. The In_2O_3 layers grown by spray pyrolysis also show tremendously flat and featureless surfaces over several micrometres, σ_{RMS} ≈ 0.42 nm, a characteristic comparable to semiconductor quantum-well structures grown using sophisticated vacuum-based methods, like molecular beam epitaxy (MBE)[71], metal-organic chemical vapour deposition (MOCVD)[72], and metalorganic vapour phase epitaxy[73]. This is a remarkable observation considering the simple processing method used,

ultrasonic spray pyrolysis in ambient atmosphere. On the other hand, the surface topography scans of the single layer ZnO reveals the presence of crystallites with a higher surface roughness of $\sigma_{RMS} \approx 1.57$ nm, as compared to the previous layers. By depositing the ZnO onto the In_2O_3 to form the heterostructure, a similar surface topography is observed, but with slightly enlarged ZnO crystallites. This can be attributed to the different contact angles of aqueous solutions on SiO_2 and In_2O_3 surfaces together with the diverse conditions under which ZnO crystallisation and growth occurs[74,75]. Compared to the single layers of In_2O_3 and ZnO, the In_2O_3/ZnO heterojunctions exhibit an increased surface roughness of $\sigma_{RMS} \approx 2.32$ nm, due to the larger ZnO crystallites.

Further characterisation was carried out via high-resolution transmission electron microscopy (HRTEM) to examine the microstructure of the In_2O_3/ZnO heterojunctions. This characterisation and analysis were done by a collaborating group, Prof. Aram Amassian and his colleagues at King Abdullah University of Science and Technology (KAUST), Saudi Arabia.

In the figure below**,** Fig. 21(A) illustrates the cross-section HRTEM image of the In_2O_3/ZnO heterostructure deposited on Si/SiO_2. The combined thickness of the heterojunction is approximately ≈ 10 nm and is characterised by an atomically-sharp interface, a noteworthy discovery considering the simple deposition methods used to deposit the layers. The In_2O_3 layer featured highly crystalline elongated platelets with a thickness of ≈ 3 nm. Further analysis by performing geometric phase analysis (GPA) with a spatial resolution of 0.4 nm confirmed the In_2O_3 microstructure to be in the shape of elongated platelets with crystals laterally extending over 35 ± 5 nm. On the contrary, the ZnO layer was found to be approximately ≈ 6 nm thick featuring randomly oriented nanocrystals on the In_2O_3 surface.

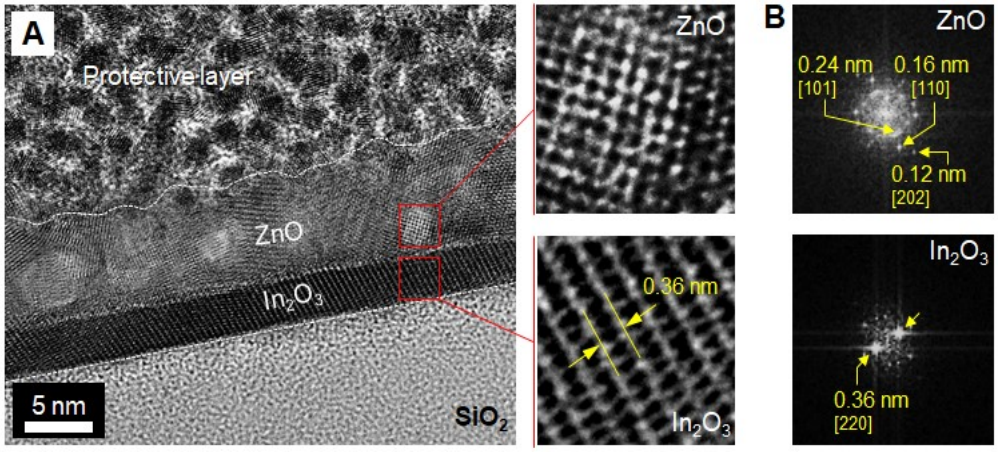


Figure 21: HRTEM analysis of solution-processed In_2O_3/ZnO heterostructures. **(A)** Representative HRTEM image of In_2O_3/ZnO heterostructure deposited on SiO_2, **(B)** FFT patterns obtained from the selected areas of the In_2O_3 and ZnO layers highlighted in **(A)**.

Fast Fourier transform (FFT) analysis of the highlighted areas in Fig. 21(A) is shown in Fig. 21(B), providing additional evidence of the polycrystallinity of the top ZnO layer with the three prominent spacings corresponding to the [220], [110], and [101] planes of the hexagonal wurtzite structure, whilst for the bottom In_2O_3 layer, the 0.36 nm lattice spacing corresponds to the [220] crystal plane of the body centred cubic (bcc) structure of In_2O_3. Although no straightforward structural relationship between the layers of In_2O_3 and ZnO could be identified (bottom In_2O_3 layer doesn't cause a templated growth for ZnO), the HRTEM data verifies that the low-temperature sequential solution-based deposition methods chosen in this work can lead to the formation of a seamless, continuous In_2O_3/ZnO heterointerface with low interface roughness. Additionally, no evidence of alloying or materials intermixing or the creation of misfit dislocations were found. The interesting microstructural feature (clear interface between both semiconductors) might be due to the chemistry and low viscosity of the precursor used to grown ZnO layers, ammonium hydroxide. This is because a low viscosity aids the formation of a good interface.

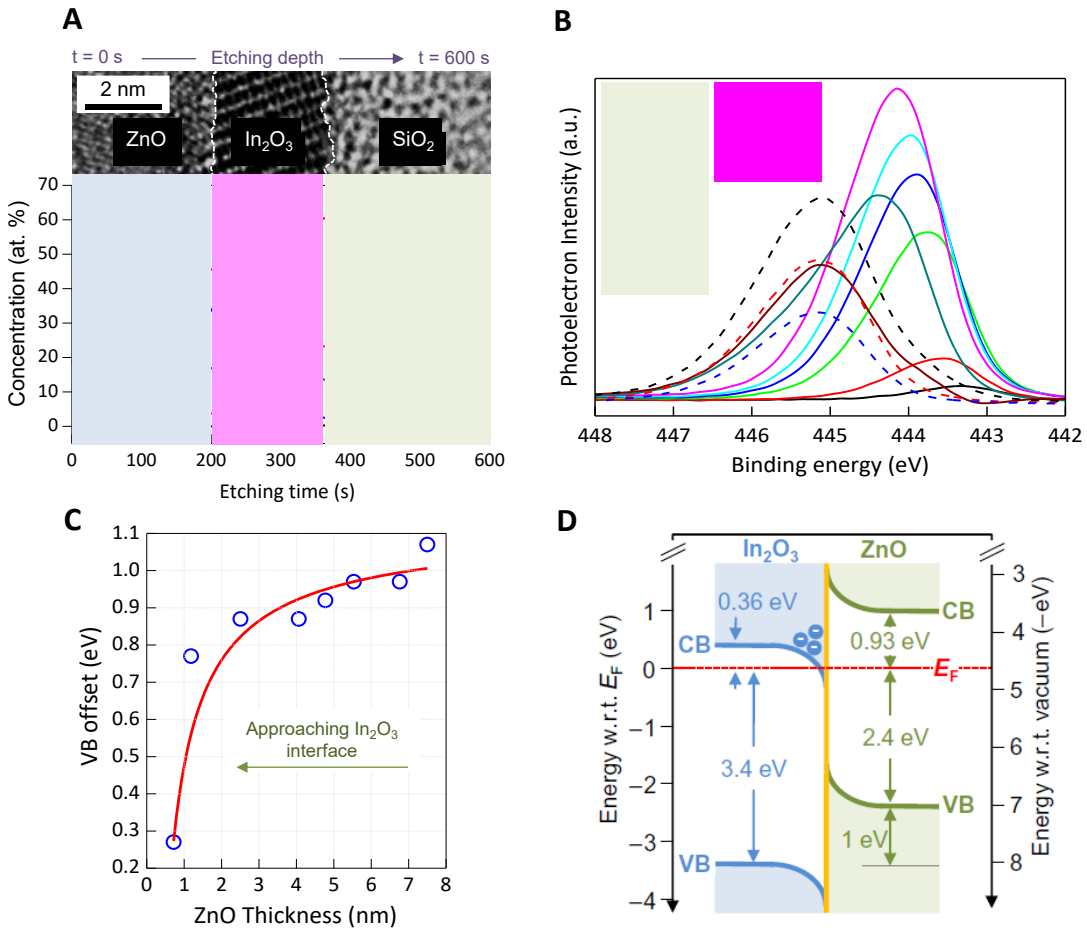


Figure 22: XPS analysis of single-layer In_2O_3 and In_2O_3/ZnO heterojunctions.

This was followed up by another characterisation method, x-ray photoelectron spectroscopy (XPS). In combination with a mild in situ Ar^+ etching, XPS was used to investigate the electronic states in the single In_2O_3 layer and In_2O_3/ZnO heterojunction as a function of etching depth. This method was additionally used to acquire the elemental profile and energy band structure of the heterointerface. As stated in Chapter 3, the XPS measurements and analysis were done by Prof. Panos A. Patsalas and his colleagues at Aristotle University of Thessaloniki, Greece.

The integral area of the In-*3d*, Zn-*2p*, O-*1s*, C-*1s* (adventitious carbon) and Si-*2p* photoelectron lines were used after background subtraction and considering the relevant sensitivity factors. The analysis shows In_2O_3 to be nearly stoichiometric, while ZnO exhibits a slight oxygen deficiency. To examine the chemical analysis of the different layers, special attention was given to the O-1s core level spectra, which are sensitive to the chemical state of O and the neighbouring atoms[47,76–78]. The ultra-thin layers of In_2O_3 and ZnO showed evidence of containing In-O and Zn-O bonds at their respective lattice sites, together with minor contributions from In-OH and Zn-OH that were detected on the surfaces.

Fig. 22(A) is an illustration of the depth resolved elemental composition of the low-dimensional solution-processed In_2O_3/ZnO heterostructure obtained using successive XPS spectra at different etching time (depth). The detection of a small quantity of In at the heterojunction surface (etching time = 0 secs.) can be attributed to the thin layer of ZnO (4 – 6 nm), which is comparable to the escape depth of the In-3d photoelectrons. A similar trend can be observed for the In_2O_3 layer as it is transparent to the Si-2p photoelectrons, leading to an apparent presence of Si at etching time of ≈ 150 secs. This data acquired from XPS analysis are in line with the HRTEM analysis discussed earlier, whilst also validating the structural and chemical composition of the In_2O_3/ZnO heterojunction.

The In-3d core level spectra recorded at varying etching times for the single layer In_2O_3 (dashed lines) and the In_2O_3/ZnO heterojunction (solid lines) is shown in Fig. 22(B)**,** (Note: the times indicated for the heterojunction correspond to ZnO & In_2O_3 etching). From the figure, it can be stated that there is no spectral variation in the core level spectra of In_2O_3 with an increase in the etching time, demonstrating a depth-independent electronic structure. On the other hand, for the In_2O_3/ZnO heterojunction, a strong dependence of the

In-3d core level spectra with etching depth can be observed. This observation can be attributed to the Fermi level pinning, a process observed at metal-semiconductor interfaces which creates an energy barrier for the charges (electrons or holes) due to band-bending at the interface. In this work, the effect of Fermi level pinning is caused due to the transfer of electrons from ZnO to In_2O_3[37]. By studying the valence band offset (VBO) between ZnO and In_2O_3 using the experimentally determined relative spectral positions of the Zn-2p and In-3d core levels, it was able to study the fermi level pinning effect in more detail. Fermi level pinning acts as a parasitic resistance degrading the device performance radically. The spectral positions were determined by considering the value of the upper edge of the valence band spectra of bulk In_2O_3 and ZnO, following the method proposed by Kraut et al[79]. The VBO between the In_2O_3 and ZnO was determined using the equation:

$$\boldsymbol{VBO = \left(E^{bulk}_{In-3d} - E^{bulk}_{In-VB}\right) - \left(E^{bulk}_{Zn-2p} - E^{bulk}_{Zn-VB}\right) - \left(E^{exp}_{In-3d} - E^{exp}_{Zn-2p}\right)} \quad \textbf{(10)}$$

Here, In-*3d* and Zn-*2p* represent the spectral positions of the corresponding core level spectra and VB is the upper edge of the valence band spectra of bulk In_2O_3 and ZnO; '*bulk*' and '*exp*' superscripts are an indication of the values obtained from bulk (> 20 nm) and ultra-thin samples (< 10 nm), respectively. Fig. 22(C) illustrates the evolution of the VBO between the In_2O_3 and ZnO for different ZnO thickness, determined by monitoring the Zn-2p and In-3d core levels after each etching step. For ZnO thickness > 5 nm, the VBO reaches a constant value of ≈ 1 eV. The corresponding conduction band offset (CBO) was calculated by considering the energy bandgap (E_g) of the individual layers of In_2O_3 (3.76 eV) and ZnO (3.33 eV). A schematic of the resulting energy band diagram of the In_2O_3/ZnO heterojunction reconstructed based on XPS, optical absorption, and Kelvin probe measurements is shown in Fig. 22(D). Due to the large CBO, there is a transfer of electrons from the CB of ZnO layer to

the In_2O_3 leading to the formation of a spatially confined sheet of free electrons (electron gas) at the vicinity of the heterointerface on the In_2O_3 side.

To illustrate this behaviour and verify the existence and location of the confined charges, the apparent charge carrier concentration across the heterojunction was evaluated via a quantitative C-V analysis of metal-insulator-semiconductor (MIS) capacitor structures. Usually, from the data acquired from C-V analysis for heterointerfaces with the presence of a 2D-confined electron sheet, there should be a clear spike in the carrier profile which indicates the exact position of the critical interface.

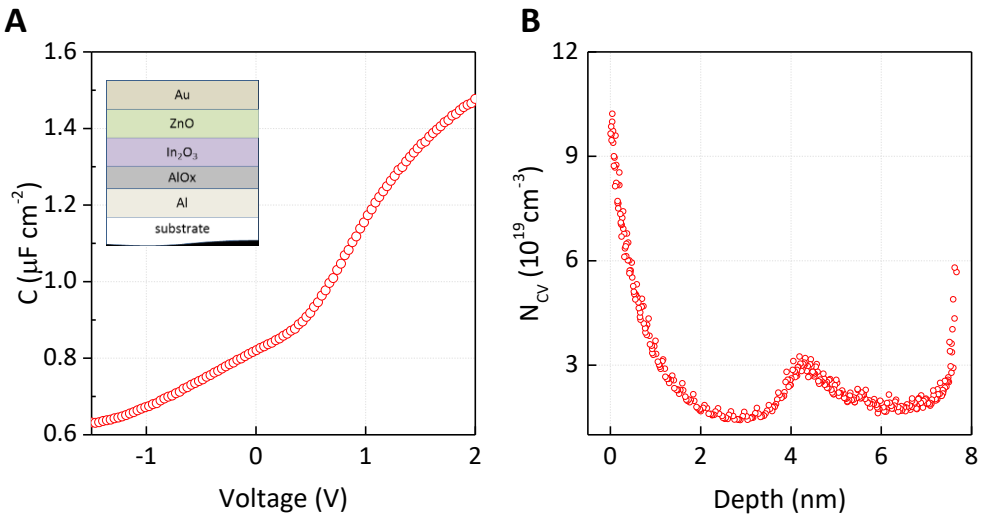


Figure 23: C-V measurements and analysis.

Fig. 23(A) shows the C-V characteristic of a representative MIS device with In_2O_3/ZnO structure measured at room temperature (inset – schematic cross-section of the MIS capacitor structure), and Fig. 23(B) shows the apparent free electron profile (N_{CV}) as a function of heterojunction depth, x, (starting from top electrode x = 0 nm) for the same MIS

capacitor. The results clearly show a significantly enhanced concentration of free electrons located right at the position of the In_2O_3/ZnO interface. The spike seen in the charge carrier profile reaches a maximum value of ≈ 3.1 × 10^{19} cm^{-3} with a width of 1 – 2 nm. The width values were primarily determined by the roughness of the interface and agrees with the height histograms shown earlier. The CB discontinuity measured using XPS and optical absorption spectroscopy techniques, combined with the high structural quality of the In_2O_3/ZnO heterointerface and the presence of a 2D-confined sheet of electrons at the heterointerface, explains the percolation conduction transport mechanism in In_2O_3/ZnO heterojunction transistors.

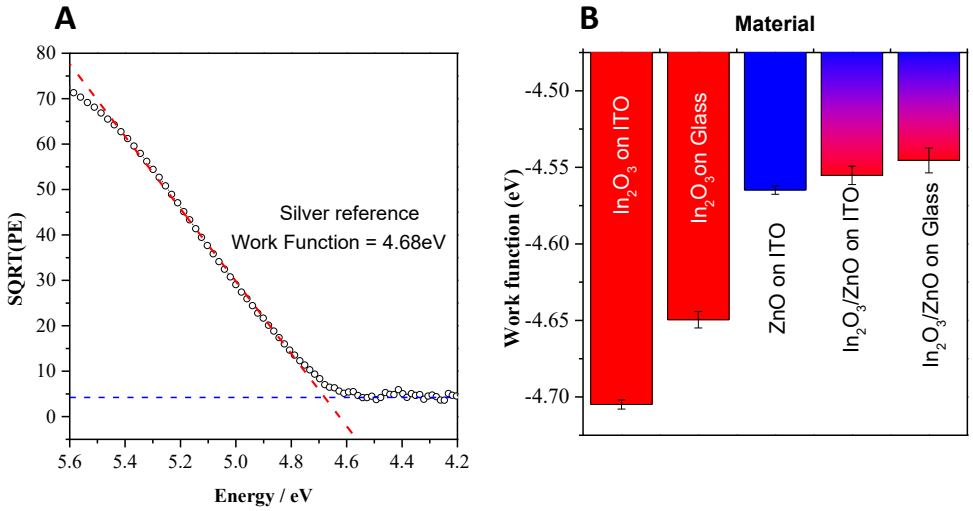


Figure 24: Work-function measurement of **(A)** Silver (Ag), and **(B)** In_2O_3, ZnO and In_2O_3/ZnO on different substrates.

The measurements carried out to calculate the work-functions of Silver (Ag), In_2O_3, ZnO and In_2O_3/ZnO were done using Air photoemission system (APS) and Kelvin probe, whose working principle were described in Chapter 3. Fig. 24(B) illustrates the work-functions measured for each metal oxide system together with the work-function of Ag

(measured to be 4.68 eV) used as the reference for measuring work-functions of the other materials. Here, single layer In_2O_3 deposited on ITO and glass substrates exhibit work-function values of 4.70 eV and 4.65 eV, respectively. Single layer ZnO on ITO substrates was measured to be 4.57 eV while the growth of In_2O_3/ZnO on both ITO and glass leads to reduced work-functions, with values measured to be ≈ 4.55 eV. This change can be attributed to the transfer of electrons from the CBM of ZnO to that of In_2O_3, with TEM images (Fig. 21) concluding the presence of a sharp interface without any impact of the materials intermixing or alloying. These results demonstrate the ability to tune work-functions using carefully engineered bilayer metal oxide structures.

4.3 Discussion

This work demonstrated the first low-dimensional, atomically sharp In_2O_3/ZnO heterojunctions grown via solution-based methods at low temperatures and its incorporation in TFTs. Even though heterojunction TFTs using different solution-processed amorphous ternary and quaternary metal-oxide compounds, like InZnO, AlInZnO or InGaO, have been reported earlier[51,52,80–82], it has been challenging to fabricate transistors with an increased electron mobility beyond the values obtained from the individual constituent materials[55]. The In_2O_3/ZnO heterojunction TFTs developed for this work not only exceed the performance of single layer In_2O_3 and ZnO transistors, but can also be compared to already established state-of-the-art devices processed from vacuum-based methods[32,46,83]. The improved performance level of the HJ TFTs can be attributed to the following factors: (i) growth of epitaxial-like crystalline In_2O_3 layers using ultrasonic spray pyrolysis in ambient conditions, (ii) the formation of a seamless and dislocation-free heterointerface of

In_2O_3/ZnO by spin-coating the top ZnO layer, and (iii) the existence of a q-2DEG system (sheet of free electrons) confined at the vicinity of the atomically-sharp In_2O_3/ZnO heterointerface because of the large CB discontinuity. Other reasons possibly contributing to the improved performance could be the top ZnO layer passivating the In_2O_3 surface defects and/or an improved injection behaviour of electrons into the active layer. The latter could be due to the electron injection barrier being suppressed caused by the lowering of the Schottky barrier because of the existence of surface electron accumulation. Due to the combination of these unique features, a drastic change in the electron transport mechanisms was observed, starting with an increase in electron mobility followed by the transition from a trap limited to a percolation dominated transport process, as shown in the figures earlier. Additional evidence in support of this vital change was provided by the temperature dependence of μ_{LIN}, through which we notice the temperature-activated charge transport in In_2O_3 TFTs and a temperature-independent behaviour for the In_2O_3/ZnO HJ devices. The latter observation is a trait indicating the trap-free band-like electron transport mechanism not observed previously in metal-oxide based TFTs.

From the AFM images, we notice the smooth, highly crystalline and epitaxial-like In_2O_3 layer which was shown to be of critical importance as it was able to facilitate the formation of the atomically sharp In_2O_3/ZnO heterointerface after the sequential spin-coating of the top ZnO layer. The latter trait together with the large CB energy offset between the single layers of In_2O_3 and ZnO resulted in the formation of a space charge layer confined and highly delocalised along the 2D heterointerface. This electron gas-like or q-2D free-electron system, experimentally demonstrated by depth-resolved XPS and C-V charge profiling measurements, facilitated a significant increase in the free electron concentration

within the In_2O_3 layer. The remarkable fact with this system and its increased charge concentration was the ability to avoid adverse effects usually associated with Coulombic scattering, a phenomenon seen in traditional extrinsically doped semiconductor transistor devices[53,57]. Looking at the energy-band diagram, it is evident that due to the higher/increased electron concentration, the Fermi level of the heterojunction would be shifted closer to the CB of In_2O_3, enabling access to the otherwise inaccessible extended states. Additionally, the ultra-thin nature of the In_2O_3 layer might cause the quantisation of the energy states (sub-bands)[61] perpendicular to the transport plane (z direction) without any effects to their in-plane delocalisation. The exceptional structural quality together with the low-dimensionality of the solution-processed In_2O_3 layers could indeed one day allow the observation of charge transport processes similar to the ones reported for traditional state-of-the-art 2DEG heterojunction devices[57]. However, more research and work are needed to unlock the true potential of such systems and the devices based on them.

4.4 Conclusion

To summarise, this study focused on the development of solution-processed In_2O_3/ZnO transistors exhibiting band-like electron transport mechanism with significantly higher mobility values (or enhanced electron transport) as compared to single material-based devices, such as In_2O_3 and ZnO TFTs. The enhancement in device performance was shown to originate from the presence of a q-2DEG at the vicinity of the atomically sharp heterointerface, which was induced by the large CB offset between the two oxide semiconductors, In_2O_3 and ZnO. The findings of this study can be regarded as guidelines for the design of solution-grown low-dimensional metal-oxide heterointerfaces. These pose an

alternative strategy to TFT development with superior performance characteristics to mature and existing thin-film semiconductor technologies but with the added advantage of being produced at a smaller fraction of the cost and with an enormous potential for widespread technological applications. After the successful development of the In_2O_3/ZnO heterojunction TFT, additional ideas for further enhancing oxide based TFTs include further heterointerface engineering, the use of different or new materials, as well as advanced doping schemes[56,57]. For example, the deposition of suitable solution-processed seed layers before depositing the oxide layers could aid in controlling and improving the crystal quality of the subsequent In_2O_3 layer, and thus have an impact on the resulting heterointerface. Additionally, a n-type doping approach of the top ZnO layer using well-known and previously reported routes[84] was considered an option to provide an extra parameter with the potential of tuning the confined electrons at the q-2DEG, and hence the transistor characteristics, in a process similar to modulation-doped AlGaAs/GaAs heterojunction field-effect transistors (MODFETs)[56,57,85]. This doping concept was applied to the heterojunction TFT, results of which are discussed in the next chapter. More broadly, these high-mobility In_2O_3/ZnO TFTs could also be extended and used as transparent conductive electrodes where the incorporation of multiple charged high-mobility heterointerfaces could be exploited to increase the layer conductivity of solution-processed transparent superlattices, and thus enabling their use as conductive electrodes for large-area opto/electronics.

5. HYBRID MODULATION-DOPING OF HETEROJUNCTION METAL-OXIDE BASED THIN-FILM TRANSISTORS

This chapter reports an n-type hybrid doping approach of organic semiconductors ($PC_{60}BM$ and C_{60}:C_{70} blend) deposited on the previously demonstrated In_2O_3/ZnO TFTs. Electrical and optical characterisations were carried out to evaluate the doping performance, with the highest electron mobilities calculated to be 30 – 40 cm^2/Vs. The results of this work contribute towards the understanding of modulation doping (MOD) in organic-metal oxide layered semiconductors and therefore provides a new strategy to utilise high mobility TFTs without Coulomb scattering or other adverse doping effects. These devices can serve as an ideal testing platform for an array of modern-day electronic applications, such as TFT backplanes for medical imaging[86], wearable and colour pixel sensors[87,88] and photodetectors[89].

5.1 Introduction

The key to address the challenge of the emerging field of large-area electronics (LAE) is to develop cost-effective, high-volume deposition protocols and high-quality materials[37,90–92]. In the last decade, the continuous development of high-performance organic molecules (OMs)[93] and transparent metal oxides (TMOs)[28,53] has the potential to enable LAE with unattainable functionality that no other material families can easily offer[28,32,86]. Regarding TFTs as the main building block for LAE, devices based on OMs[93] and TMOs[28,53] have shown excellent electrical performance and stability[92,94], outshining incumbent amorphous-silicon based technologies and fast approaching devices made of polycrystalline silicon.

The previous chapter demonstrated the use of multiple metal oxide semiconducting channel layers for TFTs showing a remarkable improvement in device performance. This was attributed to the formation of a 2DEG at the critical heterointerface due to the transfer and subsequent confinement of electrons, thus enhancing the electron transport properties. Another approach gaining considerable attention in a bid to improve TFT performance is doping[94–97]. Doping involves the introduction of a foreign agent into the host material to tune their electrical properties. Together with the understanding and controlling of defects in semiconductors, an accurate control of important parameters such as threshold voltage[98,99] and carrier mobility[95,100,101] can be addressed through doping. Although advantageous, this approach can often lead to dopant segregation and lattice distortions, causing changes in the bulk properties of the host material which would have adverse effects on the charge transporting properties. In addition to this, the presence of ionised dopant atoms leads to an unwanted Coulomb Scattering effect. Such negative effects of doping can be overcome using modulation doping (MOD)[102–105]. In a MOD process, a doped and an intrinsic semiconductor with different energy levels are brought together, leading to the flow of carriers from the doped material to the intrinsic semiconductor. This causes an alignment of the Fermi energy and a subsequent bending of the band edges at the interface. The transferred charges (electrons or holes) are then confined near the interface leading to the formation of a 2DEG/2DHG. Due to the physical separation of space charge from dopant atoms, the scattering of carriers is curtailed causing the field-effect mobility values to be close to the theoretical limits set by phonon scattering in the absence of impurity scattering.

Previous work has reported the successful hybrid MOD approach in low-dimensional TMO and OM TFTs[95,96]. Electrical and optical characterisations of a well-known air stable

dopant demonstrated a device performance with a different type of charge transfer mechanism, known as the hydride transfer. However, accommodating the additional charge carriers induced by the dopants or the additional layer on top was found to be challenging with the observation of charge/Coulomb scattering[96], leading to a drop in the performance levels. Additionally, these devices were also characterised by reduced layer dimensionality due to the thin layer on top which can be considered as a reason for the adverse scattering effect. This chapter reports a simplified model by using an extra organic molecular doping (OMD) layer of fullerenes (pristine and doped at different concentrations) on top of the In_2O_3/ZnO HJ to study the cascading doping effect all the way to the 2DEG channel, also called the hybrid MOD process. From the electrical characterisations carried out, there was evidence of additional carriers being introduced into the channel from the OMD layer, whilst also illustrating these devices being able to accommodate the foreign carriers without any adverse Coulomb scattering effect. Thus, the successful demonstration of these hybrid OMD-TMO TFTs can be regarded as an ideal device platform with the potential to fulfil a majority of requirements needed for low-temperature, solution-processed photodetectors and sensors[106].

5.2 Results and discussion

The resulting HJ In_2O_3/ZnO TFTs, used as the host semiconductors for OMD devices, exhibit a typical n-type behaviour, as shown below in Fig. 25, with threshold voltage (V_{th}) of -3.85 V, electron linear-mobilities (μ_{lin}) of 33 cm^2/Vs, electron saturation-mobilities (μ_{sat}) of 25 cm^2/Vs and channel current on/off ratios of ≈ 10^7 to 10^8.

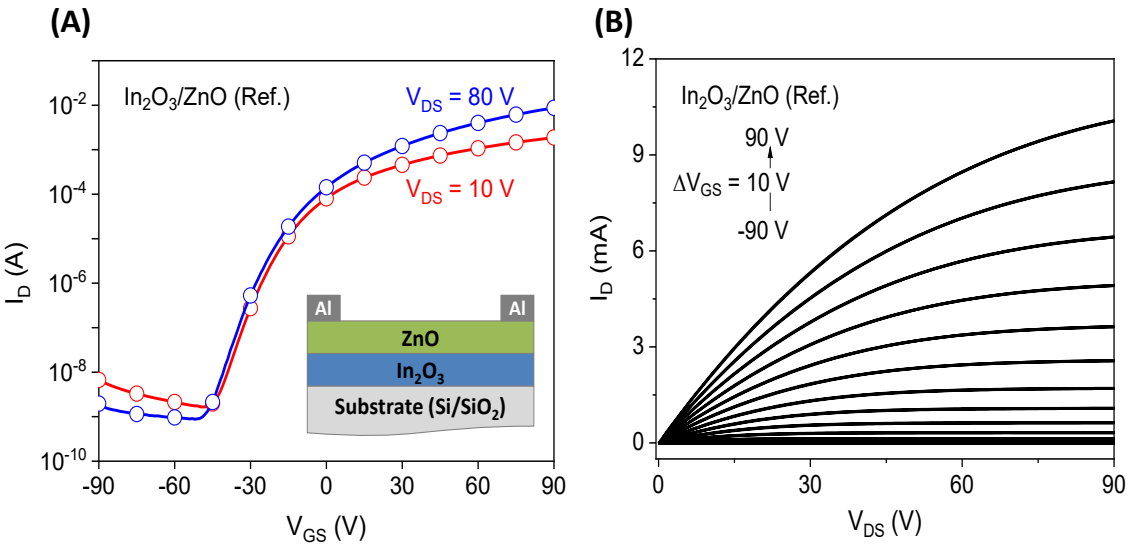


Figure 25: Electrical characterisation of the HJ oxide (In_2O_3/ZnO) TFT. **(A)** Transfer characteristics measured in the linear and saturation regime, **(B)** Output characteristics of In_2O_3/ZnO transistor.

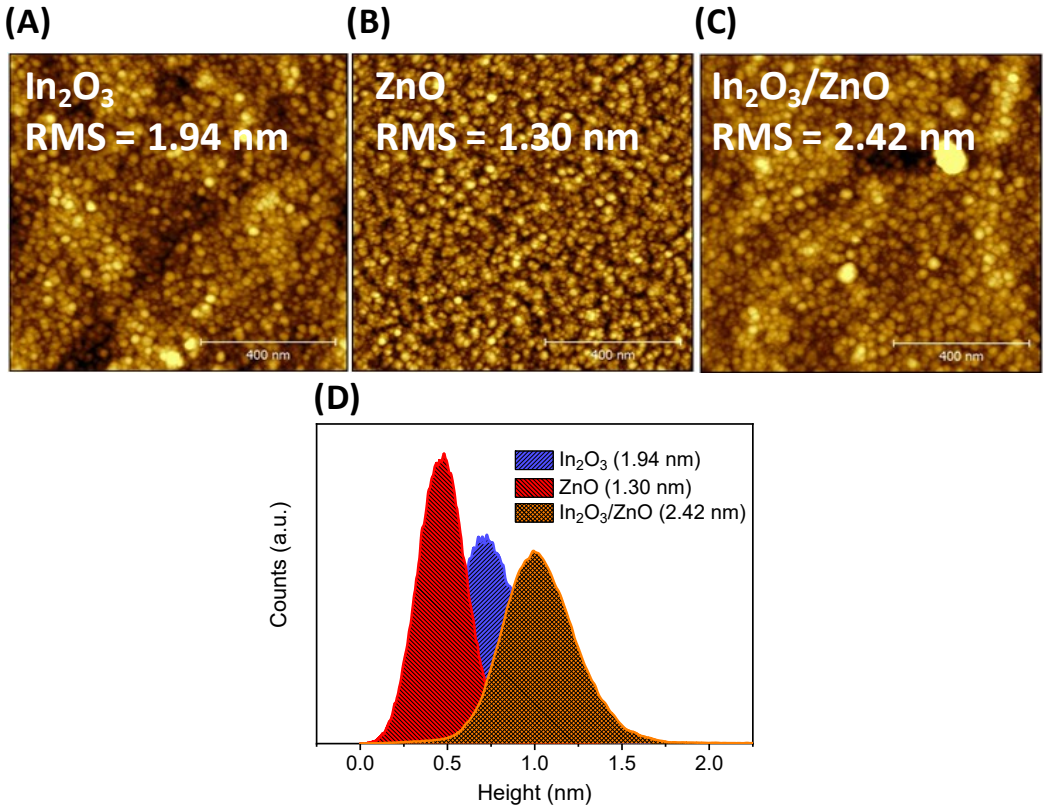


Figure 26: AFM images to study surface topography of the oxide channels. All scans show an area of 1 μm^2. **(A)** a layer of In_2O_3, **(B)** a layer of ZnO, **(C)** the heterostructure In_2O_3/ZnO, and **(D)** the relevant height histograms of the different layers providing a better illustration of the differences between the surface topographies.

AFM measurements were carried out on the different semiconducting channel layers to study the film morphologies. Fig. 26 above illustrates very smooth surfaces for In_2O_3, ZnO, In_2O_3/ZnO with RMS surface roughness ranging from 1.3 nm to 2.4 nm. These results suggest the oxide layers could serve as an excellent platform for further processing the OMD layer on top as excessive roughness would likely disrupt or hinder the molecular doping process.

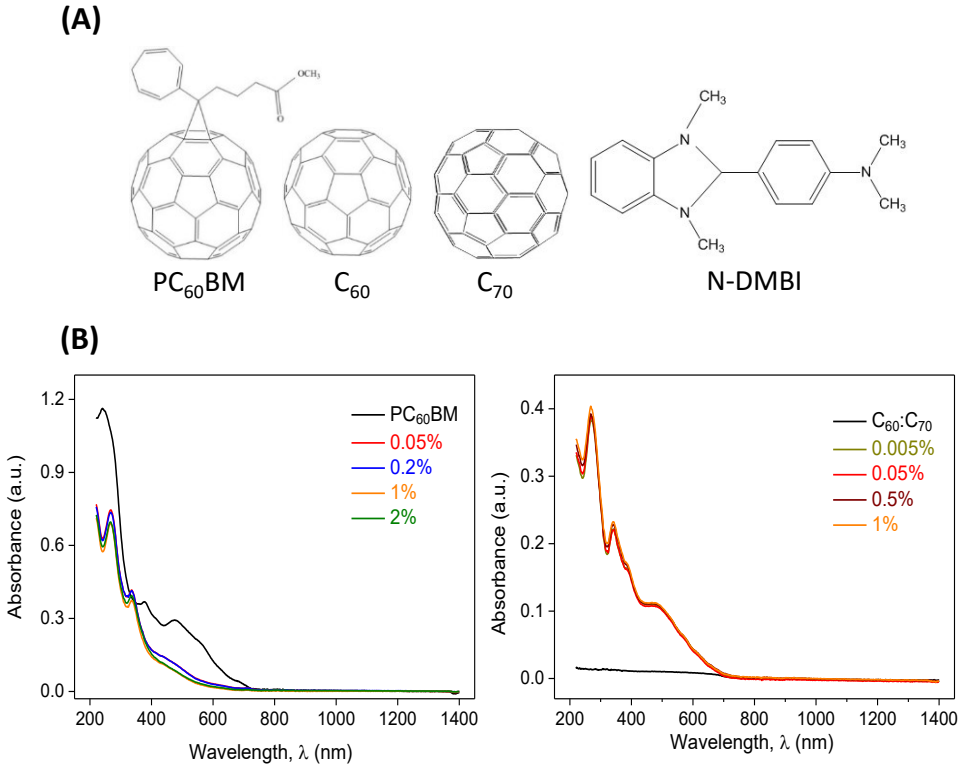


Figure 27: Molecular structure of the OMs and dopant used, and **(B)** UV-Vis-NIR absorbance spectra for pristine and doped OM films of $PC_{60}BM$ and C_{60}:C_{70} (1:1).

The molecular structures of the OMD materials, i.e. $PC_{60}BM$ ([6,6]-phenyl-C_{61}-butyric acid methyl ester), C_{60}, C_{70}, and the dopant N-DMBI ((4-(1,3-dimethyl-2,3-dihydro-1H-benzoimidazol-2-yl) phenyl) dimethylamine), are depicted in Fig. 27(A). To understand the doping effect in detail, ultraviolet-visible (UV-Vis) spectroscopic measurements were performed. The absorbance spectra, calculated from the transmittance and reflectance

data, for the pristine and doped fullerene layers in Fig. 27(B) demonstrates the n-type behaviour of the N-DMBI dopant. New absorption peaks are seen upon doping the neat films in the near ultraviolet region (350 – 400 nm), implying the creation of fullerene anions due to the donation of electron(s) from the dopant to the fullerenes[95,96]. The doping mechanism in these systems (fullerenes/N-DMBI) is different from electron-transfer dopants, discussed in detail later in the Chapter.

One important aspect regarding the doping of fullerene layers or by extension any doping process in organic materials is that the addition of extrinsic molecules (as against molecules of the intrinsic host material) often leads to material segregation during preparation[95,96]. As a result, dopant molecules, once they do not dissolve and/or form segregation, could not contribute extra charge carriers to the host semiconductors. To study this potential detrimental effect, the direct observation on the film morphology was carried out using AFM to study the intrinsic and doped fullerene thin-films deposited via spin coating on Si/SiO_2 substrates.

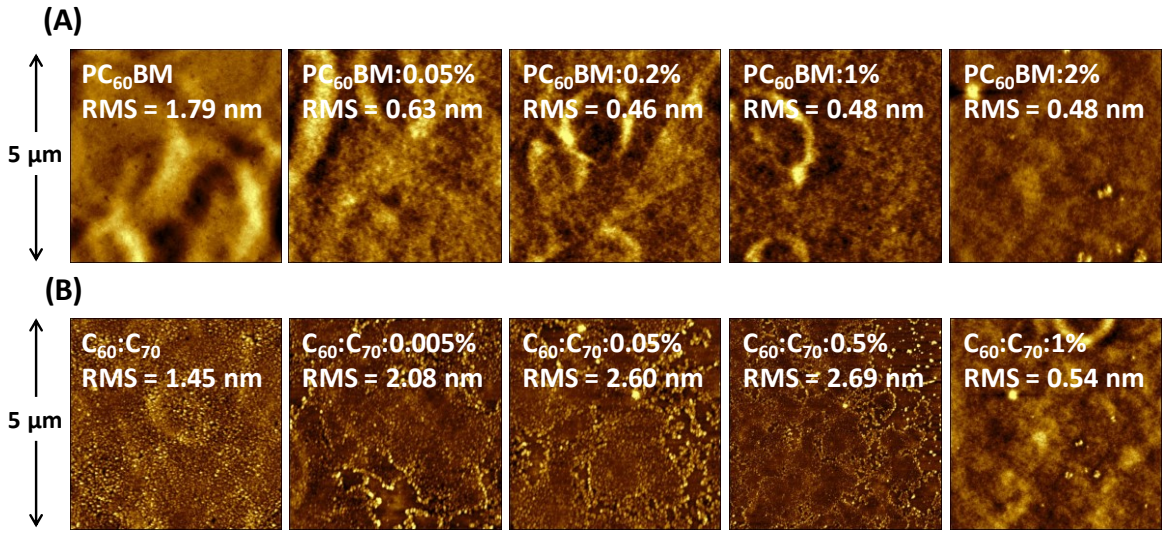


Figure 28: AFM images of pristine and doped (at different concentrations of N-DMBI) OM films. **(A)** $PC_{60}BM$ series, **(B)** C_{60}:C_{70} series.

High-resolution AFM images in Fig. 28 show the film topography for pristine fullerene films followed by the deposition of N-DMBI on top and the doped fullerene films at different concentrations of N-DMBI. The spin coating parameters used for the fullerene and dopant layers were 2000 rpm for 45 secs. (ramp 2) and subsequently annealed at 80° C for 10 mins. Both the deposition and annealing were carried out under N_2 environment. For $PC_{60}BM$/N-DMBI, the films tend to get smoother with increasing concentration of the dopant (smaller RMS values). On the other hand, for the C_{60}:C_{70}/N-DMBI films, there is no definite pattern and the roughness of the layers seems very similar (high RMS values) except at 1%, which shows lower roughness (low RMS values). The rough nature of the films could be due to the reaction of the dopant with the fullerene blend forming structures (most likely, N-DMBI nucleated nanocrystals) on the film.

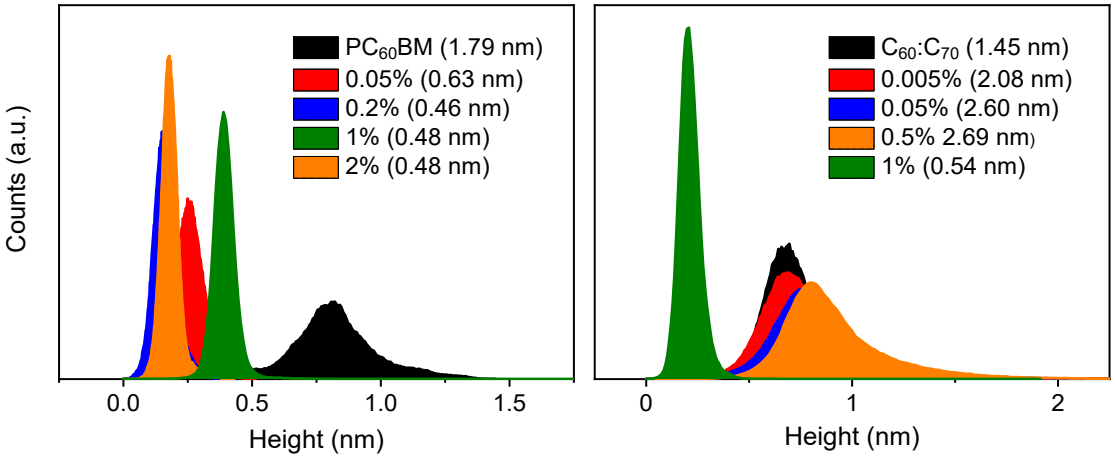


Figure 29: Height distribution plots for the pristine and doped OMs/fullerenes, $PC_{60}BM$ series on the left and C_{60}:C_{70} series on the right.

Further analysis was carried out by looking at the height distribution for both intrinsic and doped fullerene layers, with results showing the presence of only one intense

peak in all doping levels, as shown in Fig. 29 above. These AFM results indicate the high homogeneity of these films and no sign of significant segregation, demonstrating the successful incorporation of the dopant in the host fullerene materials.

The HRTEM analysis in Fig. 30 provides enough evidence of the existence of polycrystalline metal oxide layers separated by an atomically sharp-heterointerface, a remarkable fact considering the simple and low-temperature processes employed. The fringes in the images indicate the presence of crystals with a lattice spacing of 1 – 1.1 nm (for the $PC_{60}BM$ OM layer) and 0.3 nm (for TMOs). Surface analysis done by AFM confirms the crystallinity (presence of crystal grains) in Fig. 26. The figure below also illustrates a very clear ZnO/In_2O_3 interface while the OM/ZnO interface is diffuse, which means that there is blending of the ZnO and OM layer.

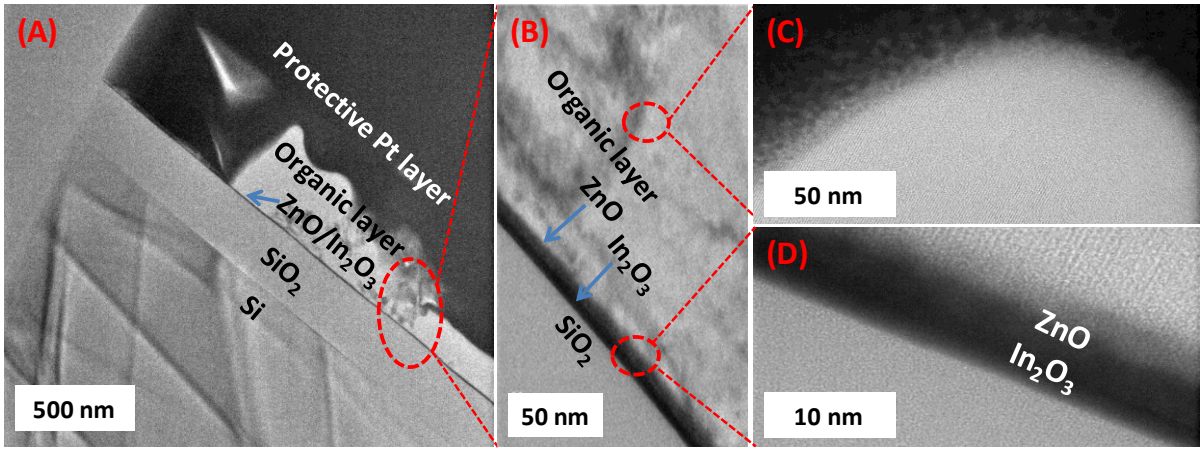


Figure 30: Different magnification HR-TEM images of the transistor channel cross-section. **(A)** Representative TEM images of the $In_2O_3/ZnO/PC_{60}BM$ deposited on Si^{++}/SiO_2, **(B)** Magnified image of the highlighted area in **(A)**, **(C)** Magnified image of the $PC_{60}BM$ area selected in **(B)**, **(D)** Image illustrating the In_2O_3/ZnO interface.

To evaluate the doping performance on the fabricated transistors, electrical characterisations of the devices were performed, results of which are discussed in this

section. The energy-band diagram for the different materials used is also shown below, which aids in the understanding of tuning of the Fermi level (E_F), electron transfer and band bending. The corresponding E_F values for In_2O_3, ZnO and Al (aluminium electrode) shown in the energy-band diagram were obtained from Kelvin Probe measurements, while the $PC_{60}BM$, C_{60}:C_{70} and N-DMBI values were taken from literature[107,108].

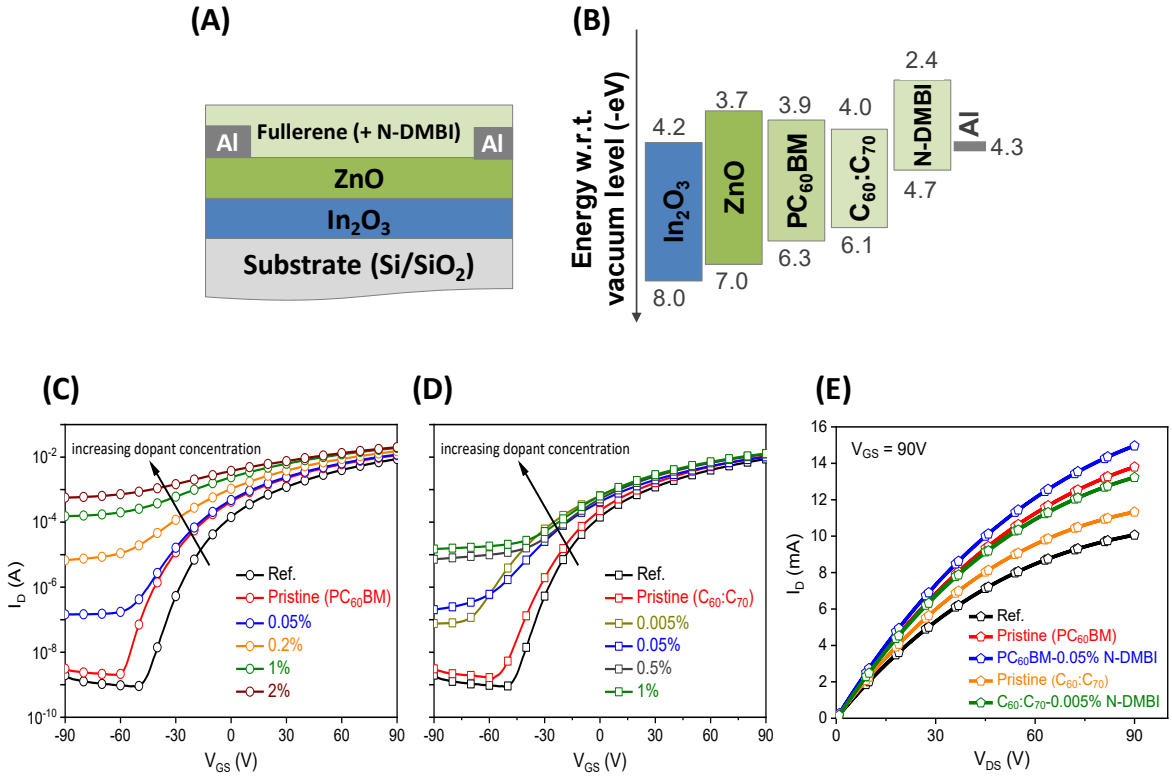


Figure 31: (A) TFT schematic of BG-TC structures; **(B)** energy band diagram for the different materials used; **(C)** transfer characteristics for $PC_{60}BM$ series in the saturation regime (V_{DS} = 80 V); **(D)** transfer characteristics for C_{60}:C_{70} series in the saturation regime (V_{DS} = 80 V); and **(E)** output characteristics (at V_{GS} = 90 V) for the reference, pristine and doped TFTs. The channel length (L) and width (W) for all devices measured were 100 µm and 1mm, respectively. Note: reference - In_2O_3/ZnO TFT, pristine (In_2O_3/ZnO/fullerene TFT) and doped [In_2O_3/ZnO/fullerene:N-DMBI, at different molar concentrations (0-2%) TFT].

Looking at the transfer characteristics, there is a gradual increase in the transistor's drain current level at the off state (i.e. I_{OFF}) together with a negative shift in the turn on voltage (V_{ON}) without any significant change to the transistor's drain current level at the on

state (I_{ON}) as the doping concentration increases. This leads to a certain point where the transistor channel becomes highly conductive, leading to a deterioration of the device's drain current on/off ratio. This change in the transfer characteristics of the TFTs on adding the OMD layer as compared to the reference device can be attributed to the n-type doping effect which causes an increase in the conductivity due to the transfer of free electrons (doped carriers) from the lowest unoccupied molecular orbital (LUMO) of the dopant to the fullerene layer and eventually to the CB of In_2O_3 layer followed by the confinement of the electrons at the sharp interface, leading to an increased charge carrier concentration within the ultra-thin channel layer, usually resulting in more current due to the thermal equilibrium E_F moving closer (upwards) to the CB of the channel. The change/shift in the E_F alignment causes the bending of the band edges at the interface[102–105]. The corresponding output characteristics for the same devices are shown in Fig. 32 below.

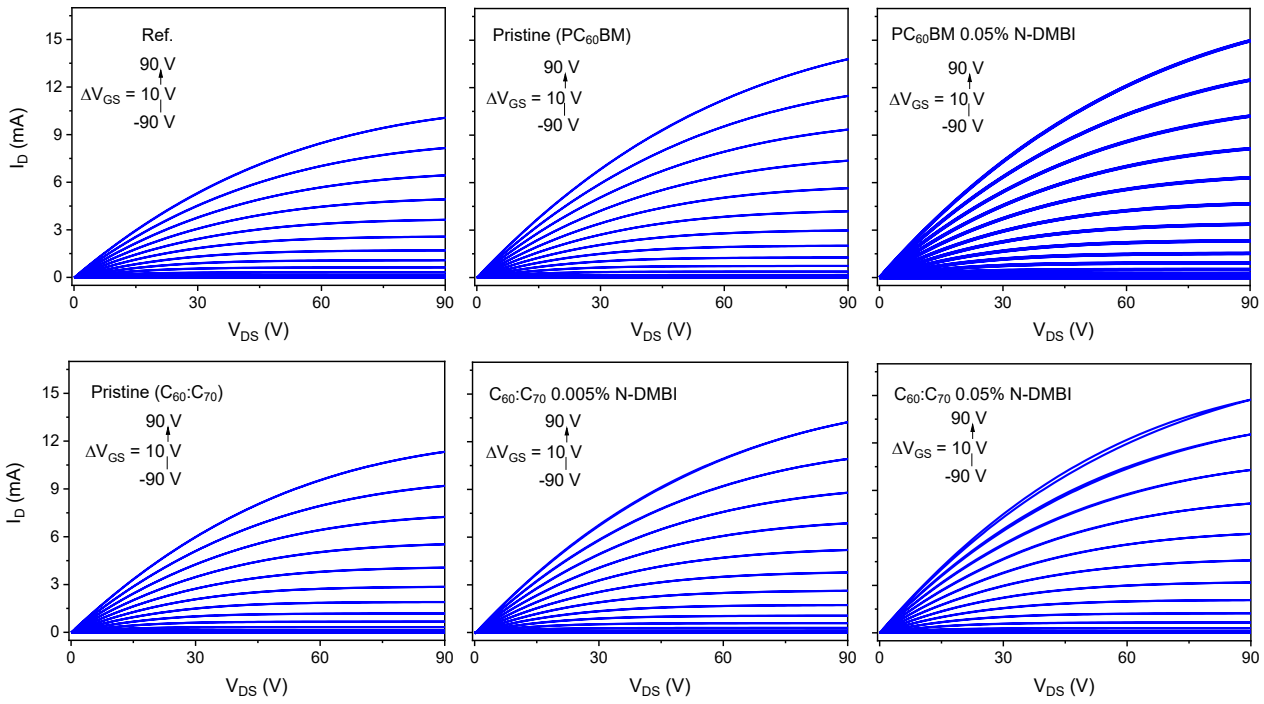


Figure 32: Output characteristics for the reference, pristine and doped In_2O_3/ZnO heterojunction TFTs based on $PC_{60}BM$ or C_{60}:C_{70}.

A similar observation was made in the work described in the previous chapter (In_2O_3/ZnO HJ TFTs), where there was an apparent migration of electrons from ZnO to In_2O_3 due to the (CB) offsets causing band bending at the heterointerface, leading to the formation of a 2DEG[37,53,92]. However, the results in this work are in sharp contrast to some other work reported[96], where upon doping the ZnO with fullerene, there is a negative shift in V_{ON} along with a decrease in the I_{ON}, but without any significant impact on the I_{OFF}. The decrease in the I_{ON} can be attributed to the increase in the charge carrier density which induces severe Coulomb scattering. For this work, the adverse scattering effect was minimised by employing the 2DEG channel, which can be confirmed by the consistent I_{ON} levels (i.e. no decrease in the I_{ON}). Another possible explanation for the changes in device performance (shift in the V_{ON}) might be due to the fact that these devices were characterised (electrical) in a nitrogen atmosphere, during which oxygen desorption might have played a role in the creation of a back channel leading to an increase in the overall conduction (electron concentration within the channel) of the device[109–111].

Moreover, there is no significant impact on the transfer characteristics of the HJ device on adding a layer of fullerene - $PC_{60}BM$ (Fig. 31(C)) and C_{60}:C_{70} blend (Fig. 31(D)), which can be attributed to i) the negligible interactions between the OMs and Zn^{2+} ions and/or the presence of OH groups on ZnO top surface, and ii) high LUMO level of $PC_{60}BM$, in line with literature and previously reported works[96]. From these results, one can state the N-DMBI could easily dope the fullerene layer(s) without any additional treatment, and the doping efficiency of $PC_{60}BM$ is higher compared to the C_{60}:C_{70} blend. The difference in the dopant concentration behaviour for the $PC_{60}BM$ and C_{60}:C_{70} is thought to be because of the different electronic structures of the molecules, the solubility differences of the material

and reaction kinetics of the transfer[95]. In general, it can be seen that the OMD doping scheme can introduce significant changes to the transfer characteristics (regardless of the fullerene system) even at very small dopant concentrations, as demonstrated for the C_{60}:C_{70} system at the lowest concentration of 0.005%.

Unlike the conventional direct electron transfer in the In_2O_3/ZnO HJ TFTs or in the case of n-type dopants, charge transfer takes place through a two-step process for the hybrid devices for this work, known as the hydride transfer process, previously shown to be effective for n-type doping of various fullerenes and its derivatives[112]. The dopant N-DMBI, after cleaving a C-H bond in solution via a spontaneous reaction, initiates a hydride or hydrogen atom transfer to the fullerene layer leading to a net charge transfer into the host semiconductor. This is followed by the formation of fullerene radical anions, stable organic cations, and hydrogen-reduced fullerenes responsible for the doping effect[112]. Looking at the energy-band diagram in Fig. 31(B), it can be stated that electrons are transferred to the fullerenes from N-DMBI due to the hydride transfer, followed by a transfer to the ZnO and subsequently to the In_2O_3 due to the low E_F. Dopants relying on the hydride transfer mechanism are attracting a lot of interest. They are able to combine a high doping efficiency with a much-desired chemical stability[95], as the hydride affinity and reaction kinetics of the host semiconductor with the dopant together with their electron affinity play a major role in selecting the materials. The difference in the doping mechanism for such systems is an important characteristic that should be considered while employing N-DMBI or related hydride-donor dopants.

Further analysis was carried out to quantify the doping efficiency and to estimate the additional charge carriers generated by the OMD layer in the channel region for $PC_{60}BM$

series and C_{60}:C_{70} series, with the results shown in Fig. 33. These results complement the transfer characteristics shown in Figs. 31(C-D), through which there is evidence for the increase in carrier concentration upon adding the pristine and doped OMD layer to the HJ channel.

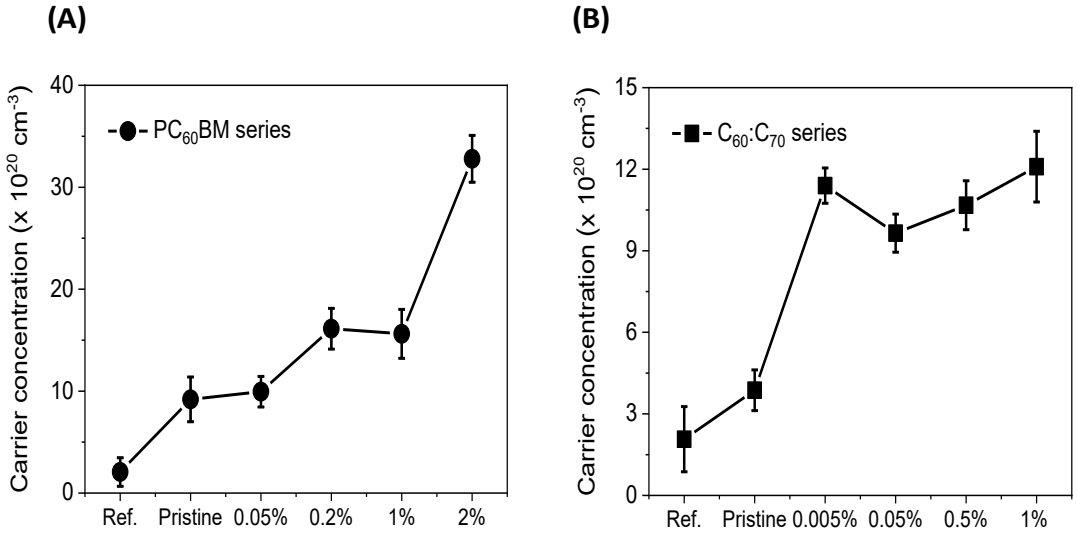


Figure 33: Electron concentrations for **(A)** the $PC_{60}BM$ series, and **(B)** the C_{60}:C_{70} series at various dopant concentrations.

For the $PC_{60}BM$ series in **(A)**, there is a gradual increase in the carrier concentration with an increase in the dopant concentration. A similar behaviour is observed in the C_{60}:C_{70} series in **(B)**, however, the overall carrier density is lower and there is a sudden spike observed at 0.005% N-DMBI. More importantly, the plots here estimating the change in carrier concentration demonstrates the ability of the fabricated TFTs to accommodate additional carriers causing an increase in the channel conductivity while negating the adverse Coulomb scattering effect seen previously. The carrier concentration for each device was calculated in the linear region (V_{DS} = 10 V) at V_{GS} = 0 V using the equation[113]:

$$n_{FET} = \frac{C_i(V_{GS} - V_{TH})}{e} \quad (11)$$

where n_{FET} is the carrier concentration in the channel (or number of charge carriers per unit volume), C_i is the gate-channel capacitance per unit area, V_{GS} is the gate voltage, V_{TH} is the threshold voltage in the linear operation regime of the TFTs, and e is the elementary charge of an electron (1.6×10^{-19} C)[113].

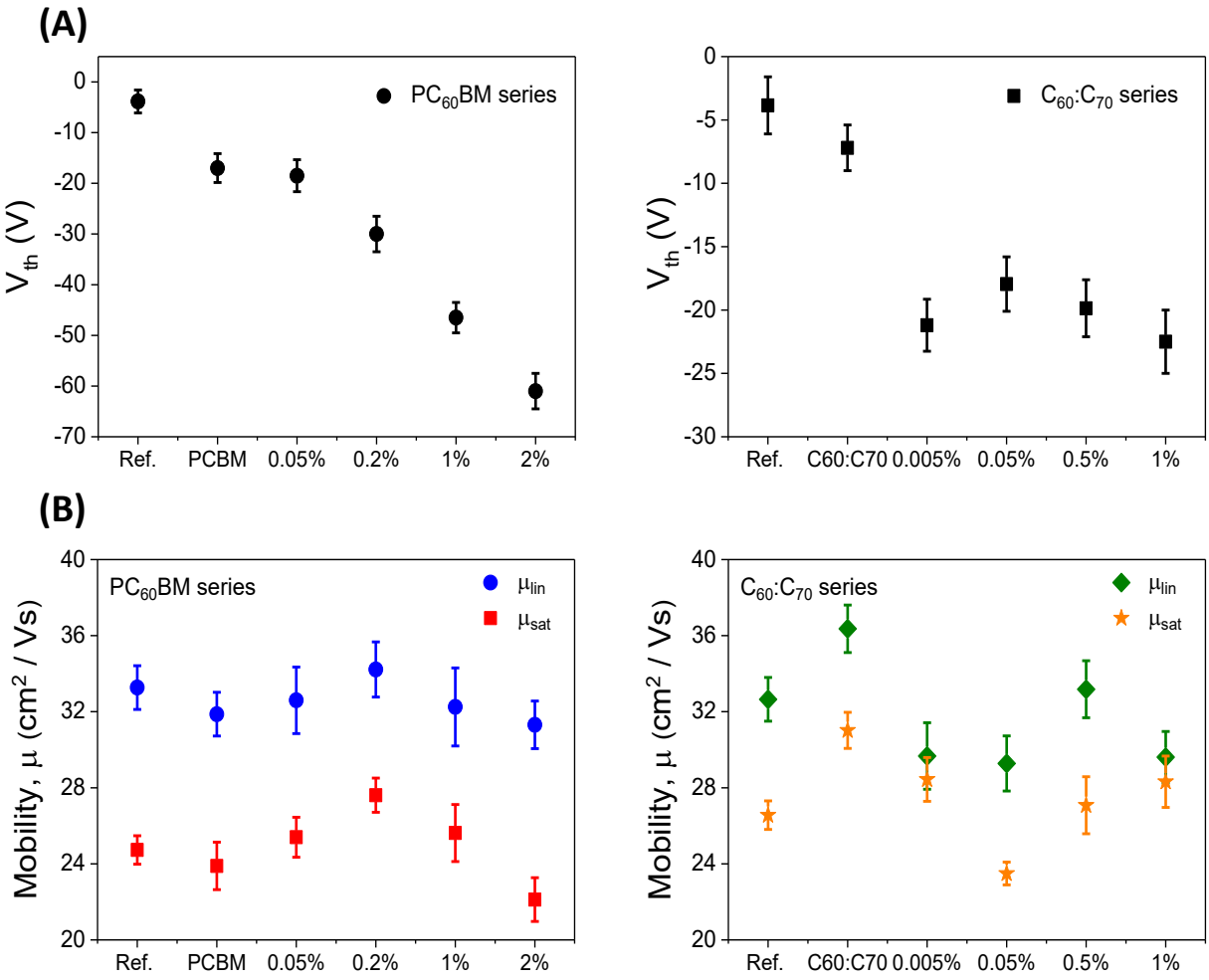


Figure 34: Evolution of **(A)** Threshold voltage (V_{th}) and **(B)** electron mobility (μ) plot vs. dopant concentration of heterojunction In_2O_3/ZnO TFTs with $PC_{60}BM$ or C_{60}:C_{70} based OMD layer.

Fig. 34 shows the **(A)** threshold voltage (V_{th}) and **(B)** electron field-effect mobility (μ) of HJ TFTs for each fullerene derivative as a function of dopant concentration. This will provide a better insight into the doping efficiency for the fullerenes. For both the $PC_{60}BM$ and C_{60}:C_{70}, the mobility values remain high (≈30 – 40 cm^2/Vs) throughout the doping process (particularly, in $PC_{60}BM$ and except for 1% in C_{60}:C_{70}) while the V_{th} decreases with the increase in dopant concentration. This is in agreement with the transfer characteristics discussed earlier and can be justified by the addition of free carriers from the dopant molecule. From the mobility values shown in the plot, it can be stated that the doping does not have a significant effect on the mobility values, which suggests that the OMD approach does not improve the charge transport in the HJ TFTs. However, looking at the consistent and high mobility values, there is evidence that the charge transfer in these devices takes place without a disruption to the stoichiometry and long-range transport. Compared to previously published reports[109,114–118] for TFTs at this level of processing temperature, these TFTs exhibit much higher mobility values, a remarkable fact considering the presence of inevitable defects at such low-temperatures and the simple deposition methods used.

These results prove that cascading doping from the doped fullerenes is possible to the 2DEG channel of the TMO HJ TFTs, demonstrated by the increased off-currents. However, the OMD doping approach cannot enhance device performance unless the channel layer is doped directly, where an increase in the charge carrier density in ZnO leads to an improvement in the performance. This hypothesis can be further confirmed by the energy-band diagram for the In_2O_3/ZnO HJ illustrated in the previous chapter, where a severe upward band-bending of the ZnO/In_2O_3 interface at the ZnO side is seen. Due to this band-bending a more negative voltage would be required for the bands to flatten and thus

preventing any further transfer of charge carriers into the 2DEG channel. In general, this work was able to demonstrate an oxide-based model with an additional 10 – 15 nm OMD layer deposited on top able to withstand additional carriers. According to literature[119–122], doping improves the overall charge transport due to reduced contact resistance and/or filling of electron traps by the free electrons donated by the dopant, and by decreasing the barrier for carrier injection but in this case, there is no significant change for the on-state. This might be due to (i) the traps being already filled by the pristine fullerene layer or the ZnO layer on top of the In_2O_3 and/or (ii) the shift of the E_F. Other extrinsic effects such as structural defects, impurities etc. might have a role to play as well but that is beyond the scope of this work.

5.3 Conclusion

To summarise, this chapter demonstrates the hybrid modulation doping (MOD) of low-dimensional, ultrathin bi-layer oxide/organic (In_2O_3/ZnO/OMs) TFTs, sequentially deposited by solution processing, a process through which the conductivity of a critical metal oxide heterointerface could be modulated. Different studies carried out to understand the n-type doping effects of the top OMs with N-DMBI at different concentrations showed the transfer and confinement of free electrons from the doped OMs to the host semiconductor over the sharp interface, initially to ZnO and subsequently to the conduction band minimum (CBM) of In_2O_3, leading to an increase in the conductivity/off-current (or a shift in the onset voltage). Although the additional OMD doping approach did not improve the overall charge transport/mobility of the bi-layer oxide TFTs or the device performance, this work provides an insight about a different doping approach (and the charge transfer process) in

semiconductors. The results also demonstrate an excellent oxide-based TFT which can act as an ideal platform for sensor and detector applications due to its ability to accommodate charge carriers generated by the dopant. Additionally, there were demonstrations of high performance In_2O_3/ZnO HJ TFTs with electron mobility values around 30 – 40 cm^2/Vs, which are higher than previously reported values for similar materials around the processing temperature used. This simple yet powerful approach can be regarded as genuine competition with existing technologies and applicable to a wide range of materials combinations and for high performance TFTs.

6. FLEXIBLE LOW-VOLTAGE METAL-OXIDE THIN-FILM TRANSISTORS USING HIGH-κ DIELECTRICS ON POLYIMIDE FILMS

The following chapter demonstrates the use of high-κ dielectric layers grown via solution-processed, UV-light assisted deposition methods and their implementation in flexible ultra-thin heterojunction In_2O_3/ZnO TFTs. These devices operate at low-voltages (± 2 V) with electron mobilities of 25 cm^2/Vs. However, these dielectrics were characterised by high leakage currents, which, if optimised, could aid towards the realisation of high performance oxide-based electronics.

6.1 Introduction

The presence of the dielectric layer is of utmost importance for transistors, as it determines stability and overall device performance. As discussed in Chapter 3, the dielectric material determines the channel current levels and also helps in preventing large leakage currents. Chapters 4 and 5 illustrated the successful demonstration of TFTs based on oxide (In_2O_3/ZnO) semiconductors using silicon dioxide (SiO_2) as the dielectric layer. The SiO_2 layer, acting as the gate dielectric with a low dielectric constant or relative permittivity (low-k ≈ 3.7 – 3.9) can be attributed to the high voltage TFT operation shown earlier. Moreover, in modern Si based technology, an increase in the density of electrical elements and devices in electronic products has led to major concerns regarding rising power consumption and heat dissipation[123–125]. In other words, the scaling down of transistors (and thus thinner gate dielectric layers) has led to an increase in leakage currents due to the tunnelling effect through the potential barrier, and hence leading to circuit instability and high-power

dissipation. For these reasons, the development of high-κ materials are preferable[126] in a bid to reduce the operating voltage and leakage current of TFTs to meet the increasing demands of device scaling. In this work, the primary focus was on finding a solution-processable dielectric material system allowing low-voltage operation, and not so much about the scaling down of devices. This is made possible by the fact that high-κ materials allow low-voltage device operation even at increased thickness of the gate dielectric, which would assist in mitigating tunnelling leakage currents and improve the reliability of devices.

Numerous oxide-based candidates have already been reported to replace conventional dielectrics such as SiO_2, amongst which, aluminium oxide (Al_2O_3)[127,128], yttrium oxide (Y_2O_3)[127,128] and zirconium oxide (ZrO_2)[129,130] have shown promising results due to good stability, high breakdown voltage and higher relative permittivity[131]. The figure below (Fig. 35) illustrates some of these promising materials.

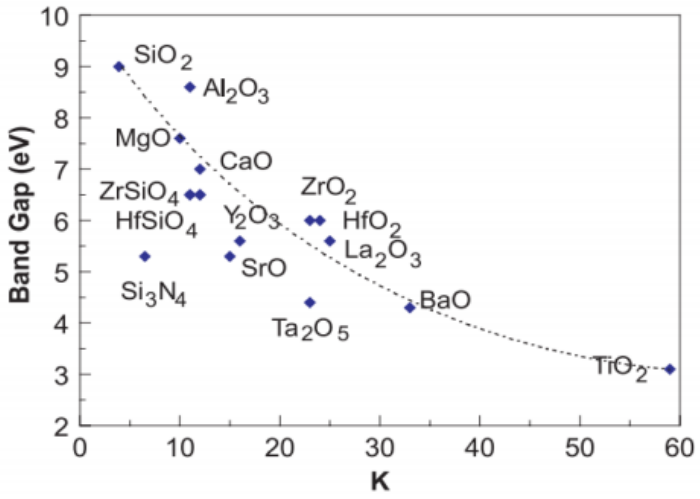


Figure 35: Plot of dielectric constants vs. bandgap of various gate oxide materials[132].

To understand how utilising a high-κ dielectric material helps in reducing the operating voltage of a TFT, it is important to understand the relationship of the accumulated

charge in the channel ($Q_{channel}$) with the geometrical capacitance per unit area of the gate dielectric (C_G) and the gate voltage required (V) in a Metal-oxide-semiconductor (MOS) capacitor structure.

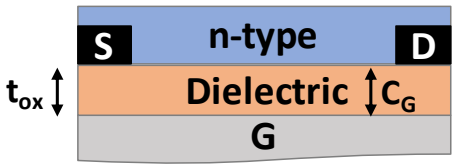


Figure 36: Schematic of a MOS structure.

The MOS structure illustrated above resembles a parallel plate capacitor. Based on fundamental device physics, $Q_{channel}$ can be described by the equation:

$$\boldsymbol{Q_{channel} = C \times V} \quad \textbf{(12)}$$

$$\boldsymbol{C = C_G = \frac{\varepsilon_{ox}}{t_{ox}} \times A} \quad \textbf{(13)}$$

$$\boldsymbol{A = L \times W} \quad \textbf{(14)}$$

where, ε_{ox} is the permittivity of the dielectric ($\varepsilon_{ox} = \varepsilon_o\ \varepsilon_{dielectric}$, with ε_o denoting the permittivity of free space = 8.85×10^{-12} F/m), t_{ox} is the thickness of the dielectric layer, and A is the area of the transistor with L and W representing the length and width of the transistor channel respectively. By using the gradual channel approximation, for gate voltages above the threshold voltage (V_{TH}), the density of $Q_{channel}$ at the dielectric/semiconductor interface is given by:

$$\boldsymbol{Q_{channel} = C_G \times (V_{GS} - V_{TH})} \quad \textbf{(15)}$$

Based on the equations above, the geometrical capacitance (C_G) of the channel is dependent on the relative permittivity of the dielectric (ε_{ox}) and its thickness. Hence, C_G can

be increased either by increasing the dielectric permittivity and/or by reducing the dielectric layer thickness. Thus, the operating voltage of the transistor can be reduced drastically by increasing the C_G due to the same amount of charge being induced at a lower V_G bias.

The objective of the work described in this Chapter was to demonstrate low operating voltage TFTs on flexible polyimide (PI) films using different dielectric materials with high-κ. The previously demonstrated low-dimensional solution-processed high mobility heterojunction In_2O_3/ZnO was used as the channel layer. With this in mind, the following section focuses on the introduction of different high-κ oxide-based materials, namely ZrO_2, Y_2O_3 and a ZrO_2:Y_2O_3 blend and their deposition via UV light-assisted and solution-processed methods for use as the gate dielectric. Fig. 35 above illustrates the two materials, ZrO_2 and Y_2O_3 exhibiting very similar properties, which would imply no significant changes when they are blended together. However, one might argue that by mixing these materials, changes in the surface properties, different trap situations, potential templating and/or a change in the conversion temperature of precursor might be a possibility. For the blend, different concentrations of ZrO_2 and Y_2O_3 were used: ratios of 1:2, 1:4 and 1:8, respectively. BG-TC TFTs were fabricated for this study with Al electrodes evaporated as the gate on flexible PI substrates. Following the precursor solution preparation discussed in Chapter 3, the dielectric layers were deposited via spin coating with the deposition parameters set at 3000 rpm for 30 secs in nitrogen (N_2). This was followed by curing the films using a metal halide lamp (250 mW/cm^2) with an UVA spectrum filter for 1.5 hrs (90 mins.) in ambient air without any thermal annealing treatment. The UV curing process lead to the formation of a hybrid high-κ dielectric with the bottom Al layer irradiated to form a thin layer (2 – 4 nm) of Al_2O_3 followed by the ZrO_2, Y_2O_3 and ZrO_2:Y_2O_3 blend, thus enhancing the overall dielectric

strength. The UV curing process used for the dielectric conversion is relatively powerful, with high energy UV light breaking the precursor bonds and further characterised by the presence of reactive ozone. Additionally, it can be considered as a source of unintentional heating effect to the PI substrates underneath. Nonetheless, this heating is far below the tolerance levels for PI films and most plastic films or foils. Moreover, the deposition process for the high-κ dielectrics is free of any direct thermal-annealing steps and the use of such oxide-based dielectric layers provides a versatile method permitting an accurate control of the surface energy, a crucial aspect for solution-based deposition methods. Using MIM structures (described in Chapter 3) and from literature, the C_i values were calculated to be 235 nF/cm^2, 650 nF/cm^2 and ≈ 205 nF/cm^2 for solution-processed ZrO_2, Y_2O_3 and ZrO_2:Y_2O_3 blend (1:1), respectively. The dielectric constants for ZrO_2 and Y_2O_3 were estimated to be ≈ 9.1 and ≈ 16.2 based on previous experimental work and analysis carried out using the same precursor materials[127,129,130,133]. The film thicknesses were measured via AFM to be around 5 –7 nm (ZrO_2), ≈ 90 nm (Y_2O_3) and ≈ 80 – 90 nm (ZrO_2:Y_2O_3 blend). The difference in the thicknesses of the individual materials are significant, with the limitation for a thicker ZrO_2 film due to the low solubility of the precursor. For the channel layer, a heterojunction In_2O_3/ZnO was used. Unlike the work previously described in this thesis, the deposition of both oxide channel layers for this work was carried out via spin coating at 4000 rpm at 30 secs followed by thermal annealing at 210° C for 45 – 50 mins. The final fabrication step was the thermal evaporation of top Al S/D contacts in high vacuum, completing the final TFT setup as schematically shown in the figure (Fig. 37) below.

The ultra-thin heterojunction TFTs based on high-κ dielectrics exhibit hysteresis-free operation with current on/off ratio of 10^3, maximum electron mobility of ≈ 25 cm^2/Vs and a

reduced operating voltage of ± 2 V. This work, with optimisations to improve the on/off ratios, can be regarded as a significant step towards the understanding and utilisation of high-performance oxide electronics fabricated using simple processing methods for low-power electronic applications.

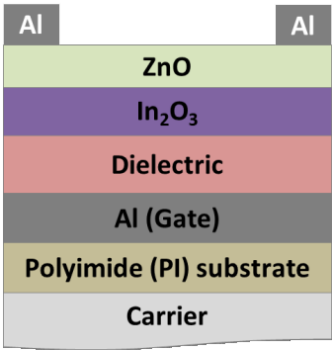


Figure 37: Schematic of the utilised TFT structure on a 3.8 µm thick substrate.

6.2 Results and discussion

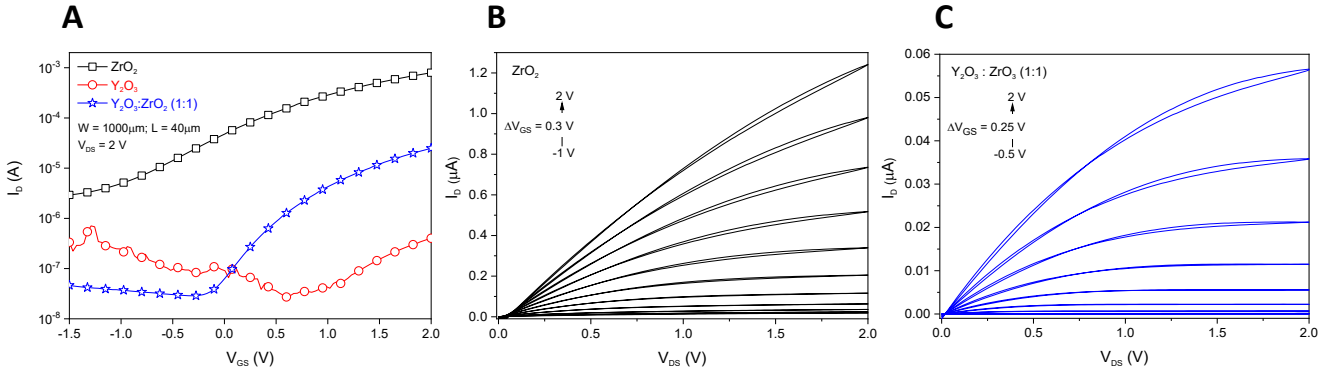


Figure 38: Electrical characterisation of fabricated TFTs based on ZrO_2, Y_2O_3 and Y_2O_3:ZrO_2 blend – **(A)** transfer characteristics using all 3 dielectrics, and output characteristics of **(B)** ZrO_2 based TFT and **(C)** ZrO_2:Y_2O_3 (1:1) based TFT.

To test the concept of using high-κ oxide-based dielectrics to reduce operation voltage, initial attempts of this work focused on the fabrication and characterisation of

In_2O_3/ZnO heterojunction TFTs using the individual dielectric layers. The results of the electrical characterisation are illustrated above in Fig. 38.

These results demonstrate the low (or reduced) operation voltage of the In_2O_3/ZnO HJ TFTs, although the devices exhibit reduced on/off ratios in the order of ≈ 10^2 – 10^3. The relatively low on/off ratio value can be attributed to the significant gate leakage current, results and analysis of which are discussed later in this Chapter. The low-operation voltage can be complemented by the threshold voltages calculated: -0.5 V (ZrO_2), 0.68 V (Y_2O_3) and 0.36 V (ZrO_2:Y_2O_3 1:1 blend). Comparing the TFTs based on the different dielectrics, i.e. ZrO_2, Y_2O_3 and the blend, devices based the ZrO_2:Y_2O_3 1:1 blend exhibit the best performance with linear mobility of 3.83 cm^2/Vs and saturation mobility of 3.81 cm^2/Vs. Thus, the next step was to optimise the high-κ dielectric and fabricate the same kind of TFTs but using only blend dielectric layers with different relative concentrations of ZrO_2 and Y_2O_3.

The behaviour of the TFTs based on the blend dielectric layers were similar to the devices illustrated in the previous section, with current on/off ratios of 10^2 – 10^3 (due to high gate leakage currents), reduced operation voltage range (and V_{th}) but with an increase in the electron mobility values. The mobility tends to increase when the concentration of ZrO_2 in the dielectric blend is higher, with highest values calculated to be ≈ 15 – 25 cm^2/Vs, as can be seen in the mobility plots shown later. This can be attributed to the better performance of ZrO_2 as a thin dielectric layer compared to Y_2O_3, which can also be seen from the results in Fig. 38(A). To understand the impact of mobility on the current-driven capabilities of these TFTs, the output characteristics of a few selected devices based on the dielectric blend are shown in Fig. 39(C-F). From these graphs, it can be seen that the current

level increases with an increase in the ZrO_2 concentration (i.e. additional charge carriers in the channel region), which in turn causes an increase in the mobility values.

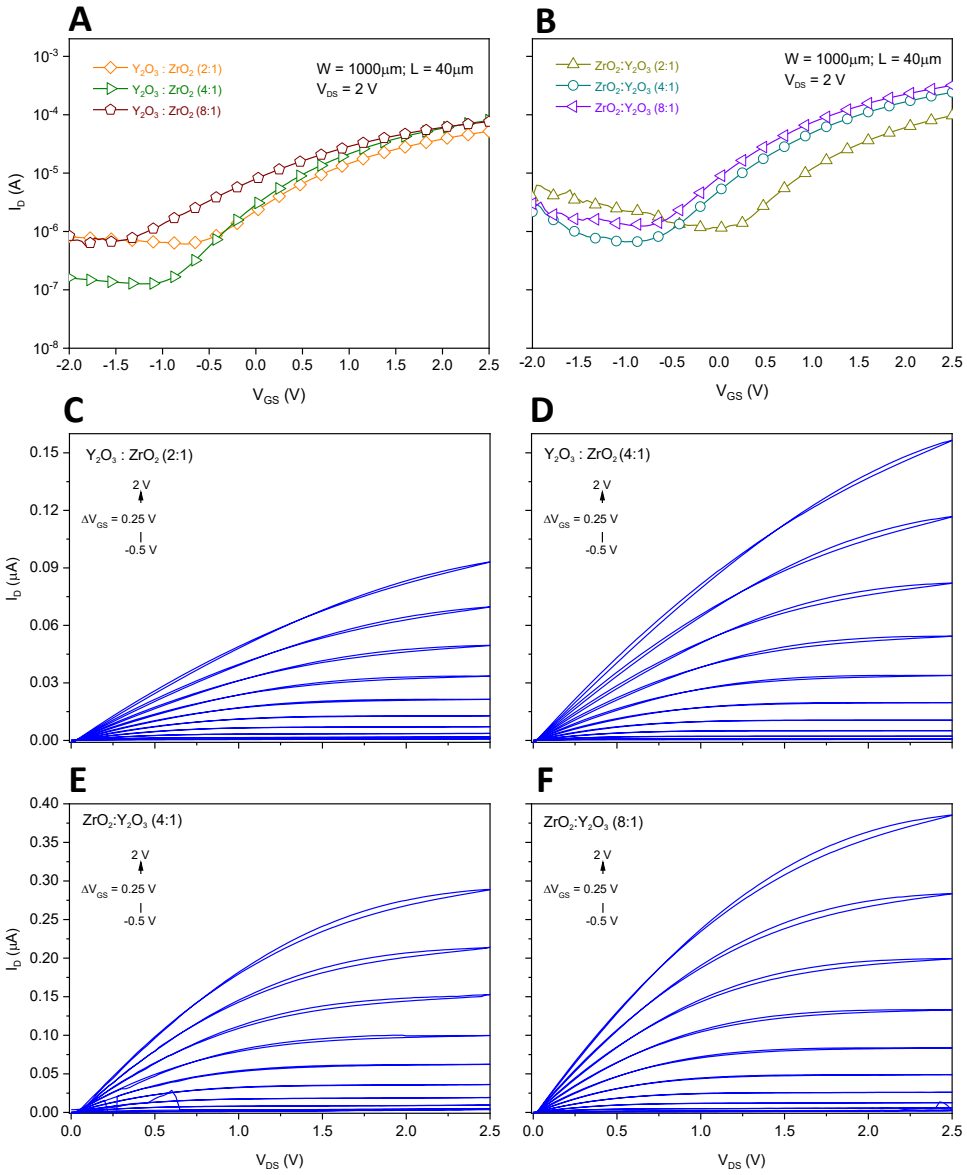


Figure 39: Electrical characterisation of In_2O_3/ZnO HJ TFTs based on Y_2O_3:ZrO_2 blend dielectrics: **(A)** - **(B)** transfer characteristics, **(C) – (F)** output characteristics.

After the successful demonstration of low-operation voltage In_2O_3/ZnO HJ TFTs on flexible PI films, focus shifted to the study of optical properties of transparent oxide films. This was carried out via UV-Vis-NIR spectroscopy, described in detail in Chapter 3. The films

were deposited onto quartz substrates using spin-coating using the deposition parameters discussed earlier.

From UV-Vis-NIR measurements, optical bandgap values were extracted via Tauc analysis[134], with the values obtained illustrated in the figure below (Fig. 40). The Tauc analysis method is a plot of $(\alpha h\nu)^X$ vs. the incident photon energy ($h\nu$), followed by an extrapolation of the linear part of the plot to $(\alpha h\nu)^X = 0$ to obtain the bandgap values. α is defined as the optical absorbance of the material used, and X is an exponent which depends on the nature of the material bandgap i.e. direct or indirect. Since both ZrO_2 and Y_2O_3 are known to be direct bandgap materials, X = 2 was used for calculations.

The bandgap values calculated for Y_2O_3 and ZrO_2 were 5.2 eV and 5.4 eV, as shown in Fig. 40(A) and Fig. 40(B), which are in agreement with previously reported values[135–137]. More importantly, there is a slight increase in bandgap values (5.2 eV – 5.5 eV) when the two dielectrics, namely ZrO_2 and Y_2O_3, are mixed at different concentrations, as can be seen from the Tauc plots below (Fig. 40(C) and Fig. 40(D)). A possible explanation for the change in bandgap could be the varying thicknesses of the layers, with the Y_2O_3 layers being significantly thicker (≈ 90 nm) than the ZrO_2 layers (5 nm). This is because the film thickness is a factor used to determine the α in the Tauc-plot analysis. Upon changing the blend ratio, a gradual, if not linear, change of certain properties can be expected. Additionally, an increase in the carrier concentration, also known as the Burstein-Moss band-filling effect[138,139], might have an effect on the bandgap values. Looking at the transfer characteristics above, there is strong evidence suggesting the change in current levels and hence the carrier concentration.

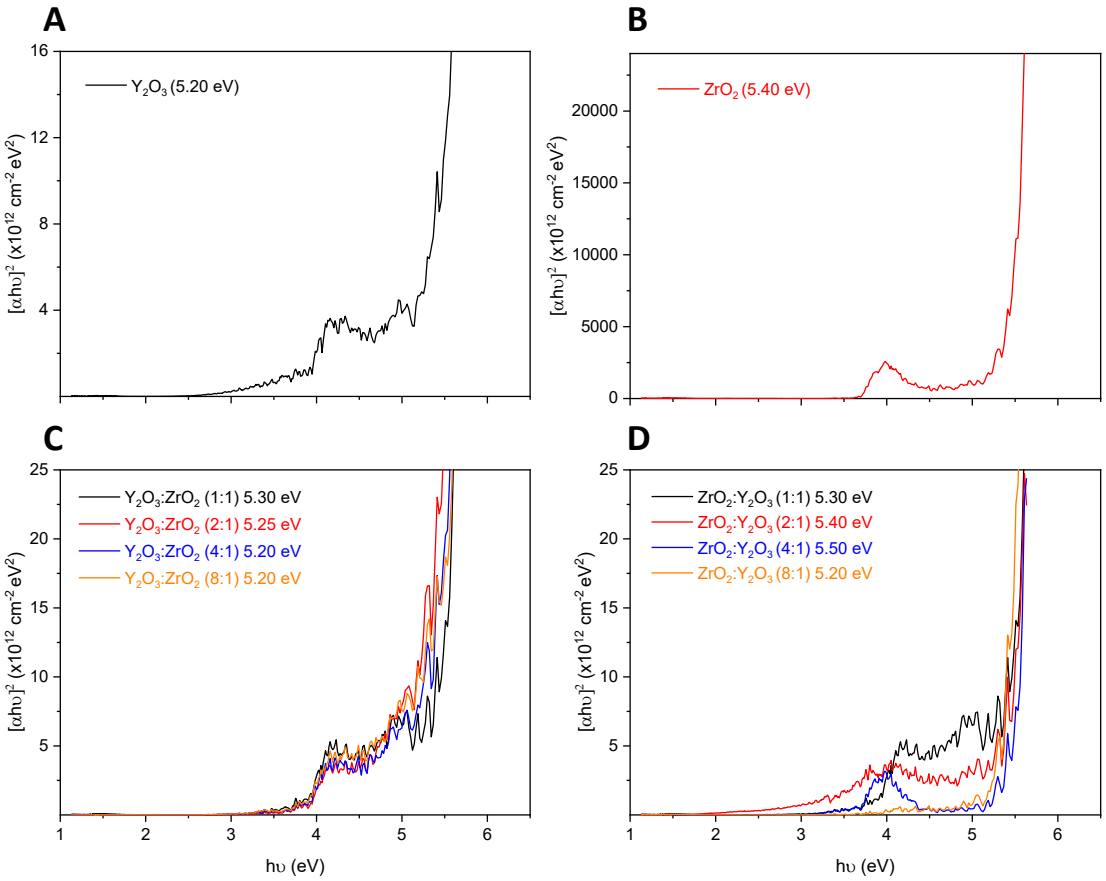


Figure 40: Tauc plots calculated from the optical spectra of different dielectric films to determine their optical bandgaps. **(A)** Y_2O_3, **(B)** ZrO_2, and **(C-D)** blend dielectrics.

Following the optical spectroscopy study, the film morphology for different films was investigated via AFM. This is crucial, as the film quality is highly related to device performance (lateral charge transport). From the figure below (Fig. 41), the roughness of individual layers can be estimated, with the PI film (0.30 nm) and the ZrO_2 dielectric layer (0.25 nm) exhibiting very smooth nature. The significant increase in the roughness for Y_2O_3 (14.76 nm) can be attributed to its high thickness, which is also partially responsible for the rough nature of the ZrO_2:Y_2O_3 1:1 blend (12.91 nm).

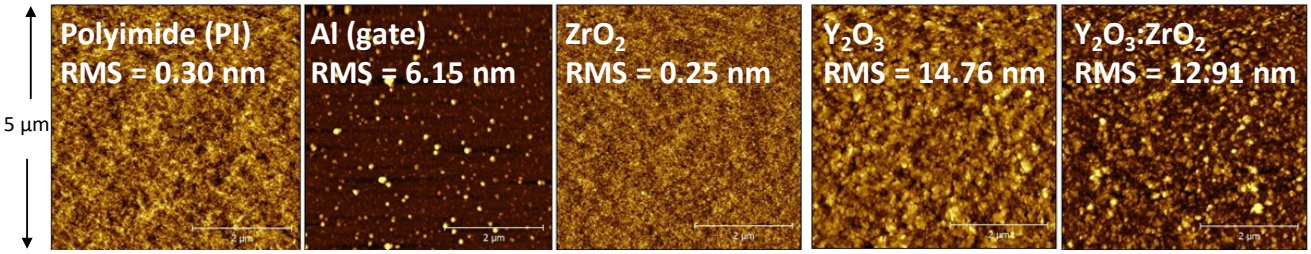


Figure 41: AFM images for PI film deposited on a carrier, Al (gate) electrode/PI, and the dielectric layers used – ZrO_2, Y_2O_3 and ZrO_2:Y_2O_3 deposited on top of the PI/Al layers.

Further AFM scans were carried out on dielectric blend layers, and the figure below (Fig. 42) presents images of the layers with different concentrations of Y_2O_3. For the Y_2O_3:ZrO_2 films, the roughness is similar (≈ 10 – 12 nm) even when the concentration of Y_2O_3 is higher in the blend. However, for the ZrO_2:Y_2O_3 films showed a remarkable change in the film morphology, presenting several features on the surface, together with an increased roughness (RMS = 19 – 22 nm). These features resembling artefacts with similar size, shape and orientation were found throughout the film and were verified by multiple AFM scans on different batches of fabricated films. This is an unusual observation, because the TFTs with higher concentrations of ZrO_2 demonstrated better performance compared to other devices, as shown in the transfer and output characteristics earlier. Considering the performance, it was expected that these films would be smoother and without any significant features or particles contributing to the better device performance. However, since imaging results showed the opposite, further optical microscopic studies were done via polarised optical microscopy (POM) at larger magnifications (under dark field conditions) to provide a clearer insight into the film (or surface) quality, with POM images presented later in this chapter.

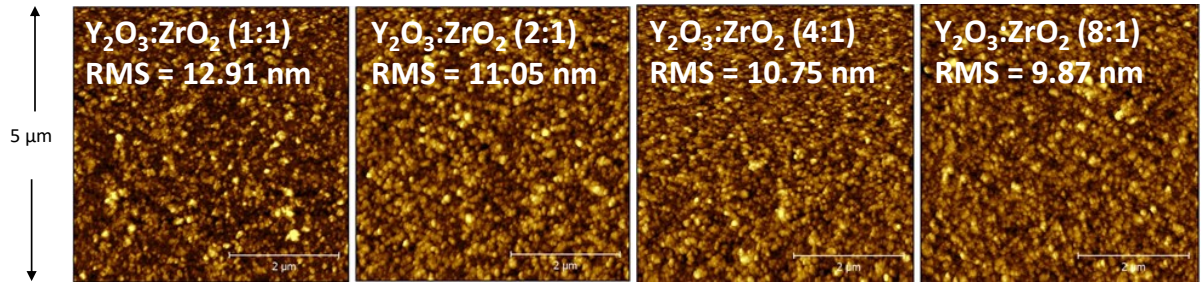


Figure 42: AFM images (size 5 µm × 5 µm) for ZrO_2:Y_2O_3 blend dielectric layers at different concentrations of Y_2O_3.

The AFM film morphology study concluded by scanning the semiconducting channel layers, with the obtained images displayed below. Individual layers of spin coated In_2O_3 and ZnO exhibit roughness values of 0.18 nm and 0.72 nm respectively, while the In_2O_3/ZnO heterojunction used as the channel layer for this work shows similar roughness values to ZnO, with RMS = 0.71 nm. These AFM images illustrate the successful deposition of all layers, and are in agreement with AFM scans completed for previous chapters in this thesis.

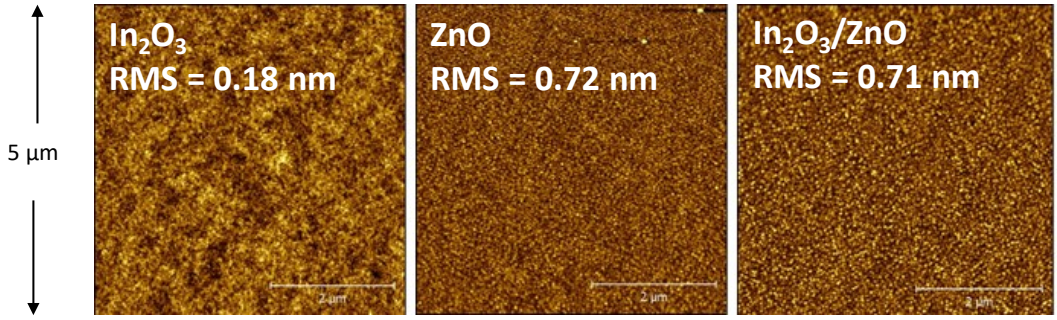


Figure 43: AFM images (size 5 µm x 5 µm) for metal oxide semiconductors used as the channel layer.

To understand the unusual film characteristics for the ZrO_2:Y_2O_3 blend, POM was carried out using a Nikon Eclipse LV100 Optical Microscope under dark field conditions with the acquired images illustrated below in Fig. 44.

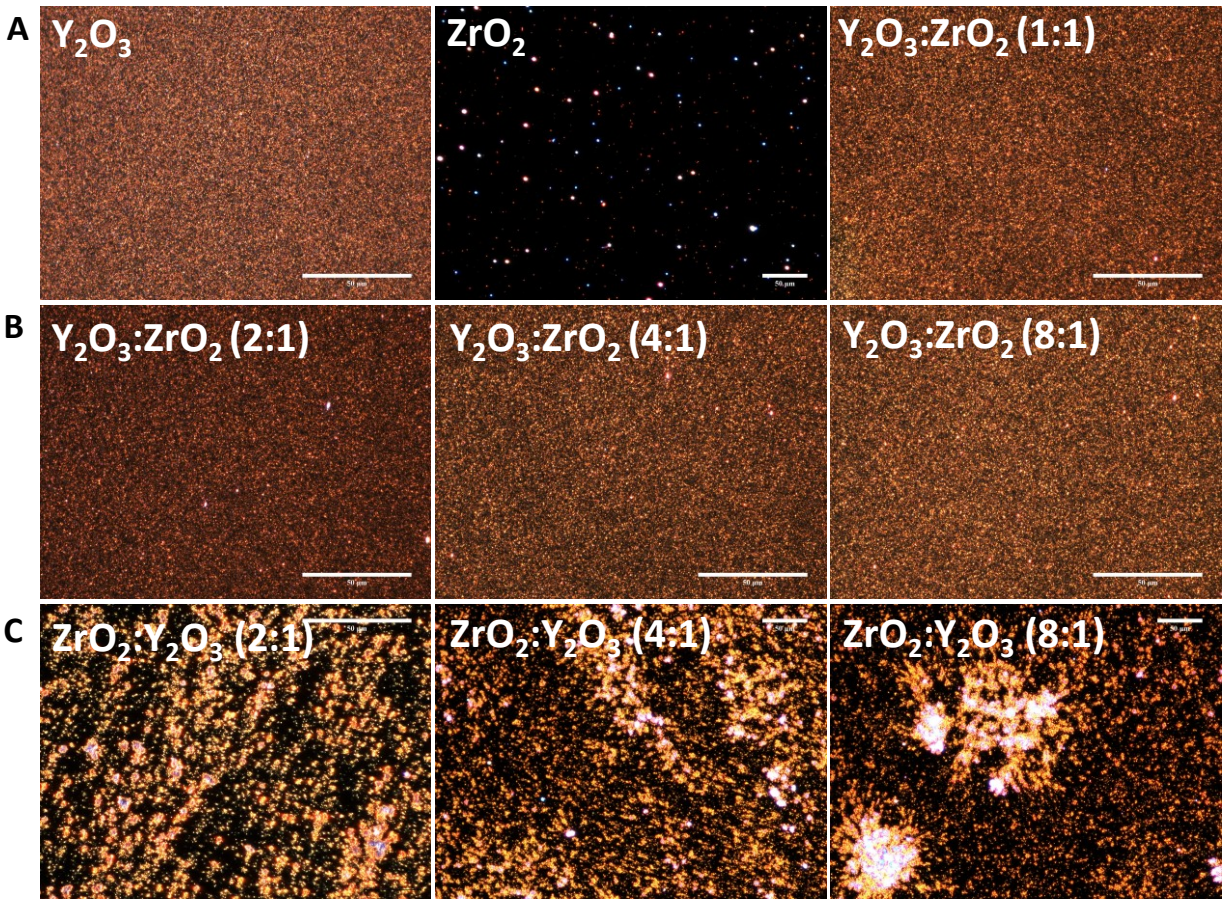


Figure 44: Polarised optical microscopy (POM) images under dark field conditions for various dielectric layers.

Individual layers of Y_2O_3, ZrO_2 and the Y_2O_3:ZrO_2 blend (2:1, 4:1 and 8:1) exhibit a smooth nature with no significant features seen on the surface. However, when the ZrO_2 concentration is increased in the blend, the films show unusual mountain-like features or rough patches which account for the layer's increased roughness, as can be seen in Fig. 44(C). Furthermore, this suggests that the ZrO_2:Y_2O_3 films are not uniform, which could be considered an unexpected characteristic, considering the devices with these films exhibit the best performance in terms of electron mobility and current levels. A better understanding of this phenomenon can be regarded as an important step towards utilising these high-κ dielectrics; however, it is beyond the scope of this study.

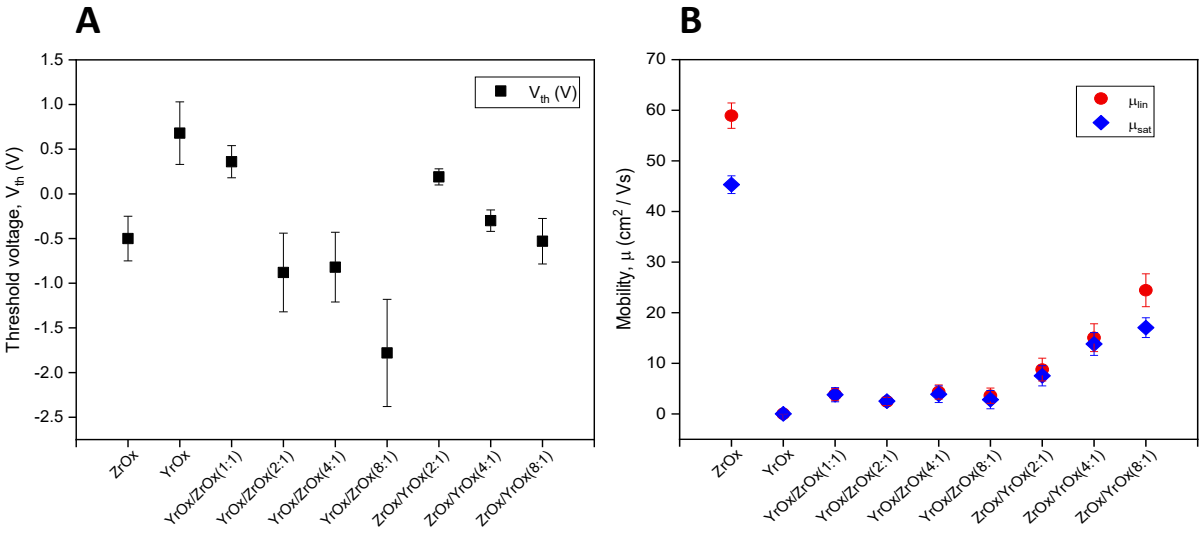


Figure 45: Evolution of **(A)** threshold voltage (V_{th}), and **(B)** electron mobility for the TFTs based on different dielectric layers.

	V_{th} (V)	μ_{lin} (cm^2/Vs)	μ_{sat} (cm^2/Vs)
ZrO_2	-0.5	58.94	45.31
Y_2O_3	0.68	0.02	0.03
Y_2O_3:ZrO_2	0.36	3.83	3.81
2% Y_2O_3:ZrO_2	-0.88	2.48	2.53
5% Y_2O_3:ZrO_2	-0.82	4.35	3.90
8% Y_2O_3:ZrO_2	-1.78	3.62	2.83
2% ZrO_2:Y_2O_3	0.19	8.77	7.55
5% ZrO_2:Y_2O_3	-0.3	15.07	13.82
8% ZrO_2:Y_2O_3	-0.53	24.45	17.05

Table 3: Threshold voltage and electron mobility for TFTs based on various dielectric layers.

Fig. 45 and Table 3 above summarise crucial TFT parameters for the devices based on different dielectric layers. Based on these, it can be confirmed that the objective of this work to demonstrate flexible low-voltage TFTs was achieved. However, as mentioned

earlier, these TFTs are characterised by low current on/off ratios of 10^2 – 10^3, which are several orders of magnitude lower than the TFTs fabricated (10^5 – 10^6) in Chapters 4 and 5. For the different dielectrics used, results suggest that a single layer of ZrO_2 is a more suitable dielectric candidate for TFTs, compared to single layers of Y_2O_3, due to the higher electron mobility values. When ZrO_2 and Y_2O_3 are blended together, the mobility values and current on/off ratios are enhanced compared to the Y_2O_3 TFTs. For varying concentrations of Y_2O_3, mobility values are around 4 cm^2/Vs. On the other hand, with an increase in ZrO_2 concentration in the blend, mobility values are enhanced further with maximum values calculated to be 25 cm^2/Vs for the ZrO_2:Y_2O_3 (8:1) blend. These results illustrate the presence of a higher concentration of electrons in the channel region and the ability of these TFTs to sustain larger currents than the other studied TFTs in this chapter, and in agreement with the transfer characteristics shown in Figs. 38 & 39. These results also confirm the efficiency or suitability of ZrO_2 as a dielectric material with the best performing devices observed at highest concentration of ZrO_2 (8%) in the dielectric blend.

In addition to the characterisations already illustrated, a study was carried out to investigate the gate-bias stress stability on TFTs based on ZrO_2, Y_2O_3:ZrO_2 (1:1) and ZrO_2:Y_2O_3 (8:1), results of which are discussed below. This study was necessary to examine the long-term stability under constant bias stress of the TFTs, which is considered to be a vital parameter for electronic devices.

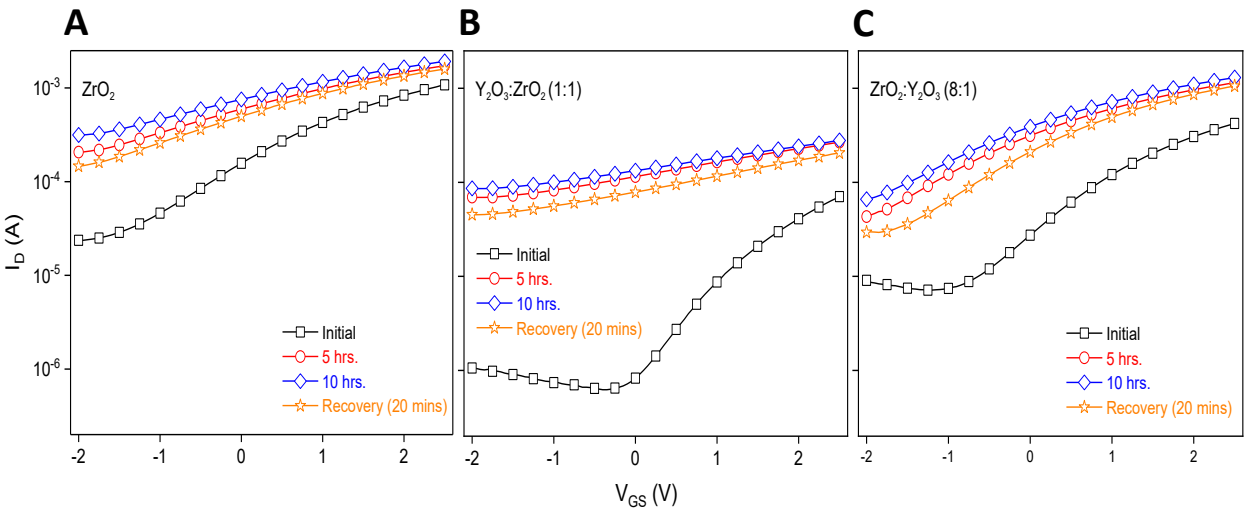


Figure 46: Gate-Bias stress stability measurements (at V_{DS} = 2 V) of In_2O_3/ZnO TFT based on different dielectric layers: **(A)** ZrO_2, **(B)** Y_2O_3:ZrO_2 (1:1), and **(C)** ZrO_2:Y_2O_3 (8:1).

Gate-bias stress measurements were carried out under dark conditions with the voltage applied at gate terminal (V_{GS}) set to 1 V with V_{DS} set to 2 V. The total operation time was set to 10 hours (600 min) with an interruption of 60 s. in order to measure the transfer characteristics and a recovery time of 20 min (after the 10 hours) during which V_{DS} and V_{GS} were 0 V. By applying the gate-bias stress, an increase in the I_{OFF} was observed, with the effect being more prominent in the TFT based on Y_2O_3:ZrO_2, as shown in Fig. 46(B). Additionally, the drain current levels (I_{ON}) increased, illustrating a more conductive nature of TFTs, which seemed to be dependent on the duration of the bias-stress. This is similar to the results shown in Chapter 4 for the In_2O_3/ZnO HJ TFTs and can be attributed to the charge tunnelling mechanism[67]. As expected, the devices showed a positive shift and a decrease in the drain current level once it is measured after the recovery time. It is worth noting that these gate-bias stress measurements were carried out after the devices were peeled off the rigid substrates and bent on a small tube, demonstrating the flexibility of the TFTs.

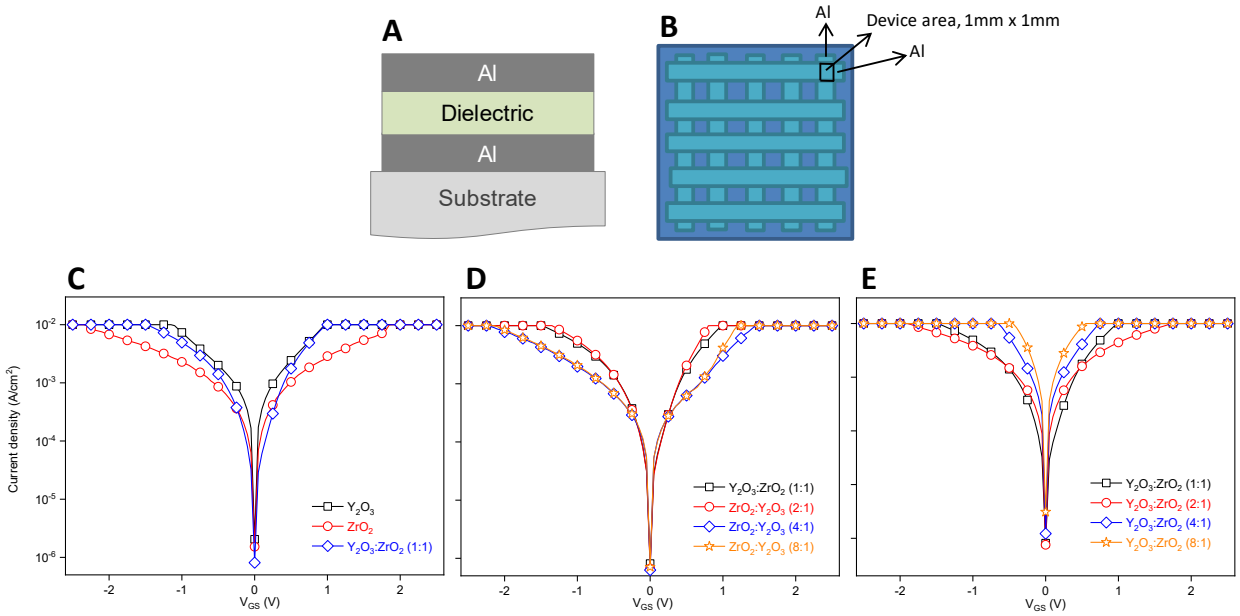


Figure 47: (A) Schematic of the MIM structure to measure gate leakage current, **(B)** top-view of the devices indicating the area measured per junction, **(C)-(E)** gate leakage current density for various dielectric materials used.

Plots in Fig. 47 illustrate the current density (A/cm^2) measured for the dielectric layers as a function of V_{GS} (or applied bias) and offer insight into the leakage current levels and the quality of the dielectric material. From these results, it is clear that the films exhibit high leakage currents (10^{-2}) and thus a very conductive nature. This is unusual as a decent dielectric usually yields values < 10^{-4} A/cm^2. An important observation is that in the TFTs the gate leakage current levels are higher than the drain current levels by an order of magnitude (10^{-3} – 10^{-4} A), leading to the low (or reduced) current on/off ratios. The data illustrates the dielectrics not exhibiting any insulating behaviour. To understand this better, plots of gate current (I_G) vs. gate voltage (V_{GS}) together with the transfer characteristics (I_D vs. V_{GS}) are shown in the figure below.

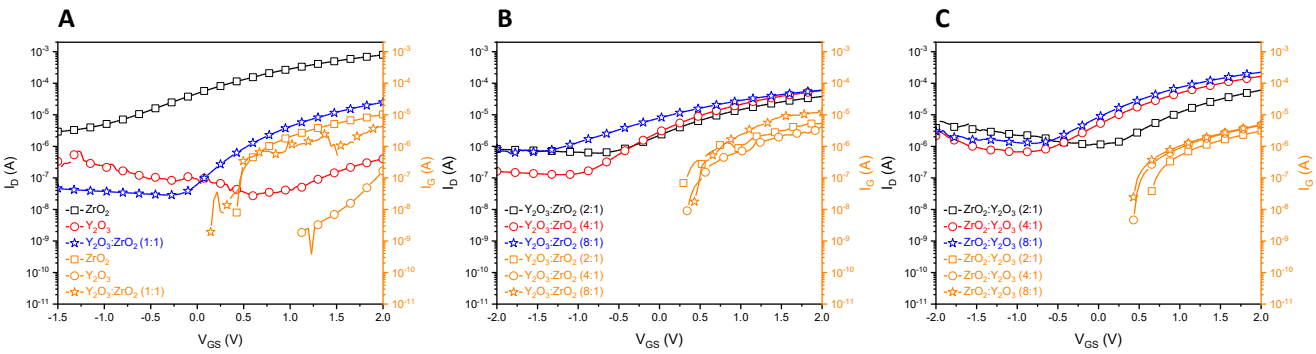


Figure 48: Drain current (I_D), gate current (I_G) vs. gate voltage (V_{GS}) for In_2O_3/ZnO TFTs based on ZrO_2, Y_2O_3 and Y_2O_3:ZrO_2 blend dielectrics.

Possible explanations for the high current density and hence high leakage could be the presence of very fine pinholes and/or the imperfect atomic structures in the dielectric layers. Moreover, high-κ oxide materials usually contain an increased concentration of intrinsic defects and grain boundaries, acting as preferred pathways for impurity diffusion and leakage currents, thus leading to the high I_{OFF} in TFTs[140]. Another possibility is the nature of the yttrium oxide precursor used for preparing the dielectric films. Since the precursor material was in the form of nanoparticles, there is bound to be some degree of porosity (i.e. not fully filled matter), making it harder for the Y_2O_3 dielectric to prevent current leakage. A rapid post annealing treatment of the dielectric films in air after deposition (and before the top electrode is evaporated) at high temperatures can suppress the defect states and improve insulating quality of the films, and thus reduce gate leakage currents. However, it is important to note that very high temperatures would not be ideal as they may destroy the underlying Al electrodes. As a potential pathway, novel techniques such as photonic curing might offer a solution to achieve high temperatures while keeping the flexible substrates intact.

6.3 Conclusion

To summarise, the work demonstrated solution-processed, UV-light irradiated high-κ ZrO_2, Y_2O_3 and ZrO_2:Y_2O_3 blend dielectrics over large areas and under ambient conditions followed by their application in low-voltage In_2O_3/ZnO heterojunction TFTs on flexible PI films. Structural analysis of the materials reveals good film uniformity over large areas for the individual ZrO_2 and Y_2O_3 layers, with ZrO_2 exhibiting a significantly lower surface roughness. The thicker layers of Y_2O_3 and ZrO_2:Y_2O_3 show increased surface roughness, while the blend layers with higher concentrations of ZrO_2 present mountain-like features on their surfaces. Additionally, all dielectric materials fabricated for this work are characterised by high permittivity values, however, they also allow high gate leakage currents. The In_2O_3/ZnO heterojunction TFTs based on these dielectrics display n-type behaviour with low-operation voltages (± 2 V), on/off current ratios of 10^2 – 10^3, and electron mobilities as high as 25 cm^2/Vs. With further optimisations to reduce the gate leakage current, this work and the proposed materials can be regarded as an ideal platform for high-performance electronic applications without any limitations on substrate choice.

7. HYBRID PEROVSKITE-METAL OXIDE PHOTOTRANSISTORS

This chapter demonstrates hybrid phototransistors developed via solution-processing of metal-halide perovskites and the previously reported metal oxides, In_2O_3 and ZnO to study light response. Using different electrical characterisations and other detailed analysis, it was observed that the perovskites behaved as the absorption layer while the bi-layer oxide was the channel layer. These hybrid phototransistors showed good photoresponse with responsivity of 10^4 A/W, photosensitivity ≈ 10^4, and specific detectivity of 10^{13} Jones, which are at least a few orders of magnitude higher than previously reported values for metal-oxide based phototransistors[141,142]. The results of this work could serve as a great potential to widen the range of applications of metal-oxide based opto/electronic devices.

7.1 Introduction

Continuous advancements in developing novel materials and device architecture have enabled field-effect phototransistors to thrive in a variety of modern large-area photodetection technologies with their unique, nonlinear responsivity and intrinsic amplification[143]. This is because phototransistors provides an excellent platform offering light-sensing abilities together with electrical switching, making them an ideal candidate for electro-optical transducer for amplification of signals[144–146]. This is particularly desirable for overcoming noise levels in conventional photodiodes[147]. A transistor's three-terminal structure/architecture is primarily responsible for tuneable gain mechanism being controlled by gate field, hence enabling a controllable sensitivity and lower noise levels compared to conventional two-terminal photodiodes[148].

Successful information extraction from input lies at the heart of all detection technologies and phototransistors are no exception to this rule. To best utilise the unique properties of functional materials for phototransistor applications, a phototransistor requires active materials with high optical absorption and excellent charge transport. Metal-halide perovskites (MHPs) have emerged as promising materials for optoelectronics due to their properties such as tuneable bandgap[149], low exciton binding energy[141] and solution processability[45,141–143]. Aside from their applications of photovoltaic cells, MHPs has attracted an increasing interest in photodetection[149,150]. The electrical property of a phototransistor can be modulated by either the gate terminal or the incident light. However, it is known that, due to ion movement, MHPs is challenging for transistor applications[151,152]. Metal oxides on the other hand, are one of the best material families for the applications of field-effect transistors[91,92] but often accompanied with an undesirable photo-persistent effect[153]. An effective way is to adopt a hybrid structure that combines a light absorber and a charge transport layer into a transistor to maximise the capability of each material[45,141,142].

This work demonstrates the development of a hybrid oxide-perovskite transistor architecture being utilised as fast and highly sensitive broadband photodetectors, with resulting devices characterised in dark conditions and under illumination at different light intensities and wavelengths. The fabricated phototransistors illustrate significant photoresponse and excellent dynamic response, as shown in the different figures of merit later in this chapter.

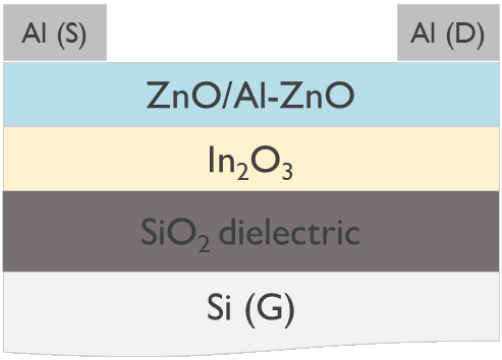


Figure 49: Schematic of the utilised BG-TC TFT structure to study light response, with a heterojunction channel layer of In_2O_3/ZnO or In_2O_3/Al-ZnO.

Bottom gate-top contact (BG-TC) transistors were fabricated on Si^{++}/SiO_2 (100 nm) wafers, as shown in Fig. 49. All substrates were cleaned using the methods described earlier in Chapter 3, while the different layers were deposited via spin coating. For In_2O_3, spin coating parameters were set to 4000 rpm for 30 secs. followed by a thermal annealing step at 210° - 225° C for 1 hour. This step was repeated twice to obtain the desired thickness for In_2O_3. Single layers of ZnO and Al-ZnO were deposited and processed using the same recipe. Transistor fabrication was completed by evaporating 40 – 50 nm thick Al S/D contacts, with the resulting devices having channel length (L) and width (W) of 40 µm and 1 mm, respectively. Spin coating of $CH_3NH_3PbI_3$ NCs was done at 6000 rpm for 30 secs. and annealed at 80° C for 10 mins. in N_2 environment. Finally, a layer of cytop, acting as an encapsulation layer, was deposited on top by spin coating at 2000 rpm for 60 secs. (ramp 9) followed by an annealing step in N_2 at 100° C for 30 mins.

7.2 Results and discussion

This work commenced with an examination of the morphological and structural properties of the synthesised $CH_3NH_3PbI_3$ NCs using TEM, HRTEM and powder X-ray diffraction (PXRD),

followed by a study of optical properties via UV-Vis spectroscopy and steady-state photoluminescence (PL) measurements. Similar to the synthesis, these characterisations and analysis were done by collaborators, Dr. Yasser Hassan, and Dr. Yen-Hung Lin, University of Oxford.

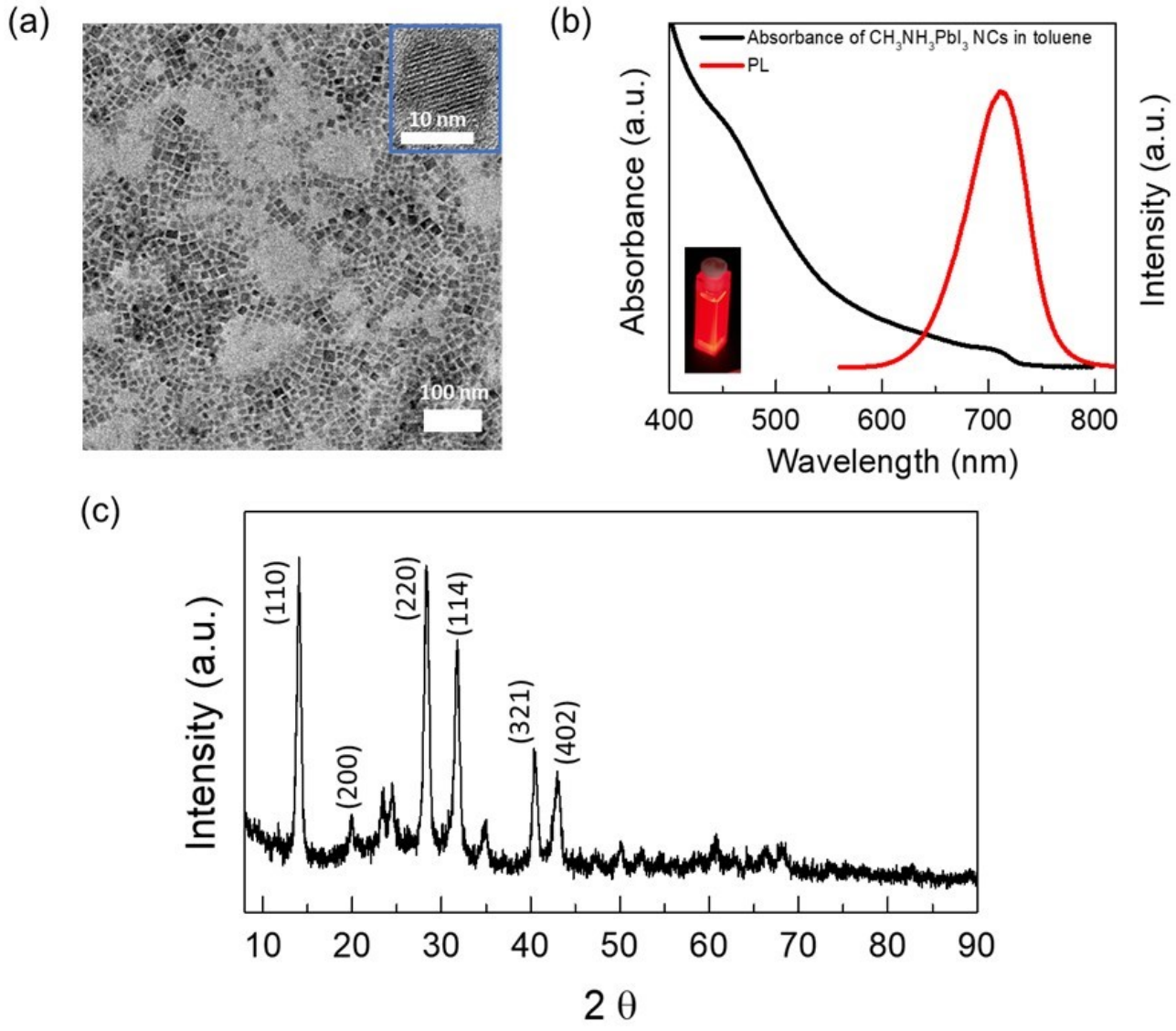


Figure 50: Structural and optical properties and characterisation of $CH_3NH_3PbI_3$ NCs. **(a)** Low-magnification TEM analysis with the size of (10–15) nm. Inset: HRTEM, **(b)** Absorption and steady-state photoluminescence (PL) spectra, and **(c)** Powder X–ray diffractogram. Perovskite reflection peaks are assigned to the tetragonal perovskite crystal lattice. The plot displays the X–ray intensity as a function of twice the diffraction angle (2θ).

Fig. 50(a) shows the TEM (inset: HRTEM of $CH_3NH_3PbI_3$ NCs, confirming the high crystallinity of the NCs used), clearly exhibiting a cubic-shape with a diameter of 10 – 15 nm. Additionally, the HRTEM image illustrates well-developed lattice fringes. FFT from the HRTEM image reveals the (110) and (002) planes with an interplanar spacings of 0.44 nm and 0.63 nm, respectively, identified for the tetragonal phase, and complementing the XRD results in Fig. 50(c). Fig. 50(b) illustrates the room temperature absorption (black line) and steady-state PL emission (red line) spectra for the $CH_3NH_3PbI_3$ NCs dispersed in toluene. From the UV-Vis absorption and PL spectra of the NCs, there is an excitonic peak present at ≈ 700 nm, which is blue-shifted compared to the corresponding bulk films of $CH_3NH_3PbI_3$ as a result of quantum confinement. There is an emission peak with a FWHM of ≈ 40 to 50 nm at 710 nm observed from the steady-state PL spectrum of the NCs and a PL quantum yield of 85%. Further studies were conducted with PXRD patterns seen in Fig. 50(c) of as-synthesised $CH_3NH_3PbI_3$ NCs, with strong reflection peaks indicating high crystallinity of a typical diffraction pattern indexed as $CH_3NH_3PbI_3$ tetragonal phase (space group I4/mcm).

Initial surface topography results include high resolution AFM images of the In_2O_3/ZnO and In_2O_3/Al-ZnO channel layers, followed by an investigation of the same films with perovskite NCs deposited on top, with the images obtained shown in Fig. 51(a). The In_2O_3/ZnO and In_2O_3/Al-ZnO films appear smooth, uniform and featureless with roughness (RMS) of 2.1 nm and 4.9 nm, respectively. Upon depositing the NCs on top, there is an indication of crystal-like structures present and an increase in the roughness with RMS values of 13.1 nm and 8.3 nm. The corresponding height distribution histograms for all films is shown in Fig. 51(b), providing a better illustration of the surface topographies.

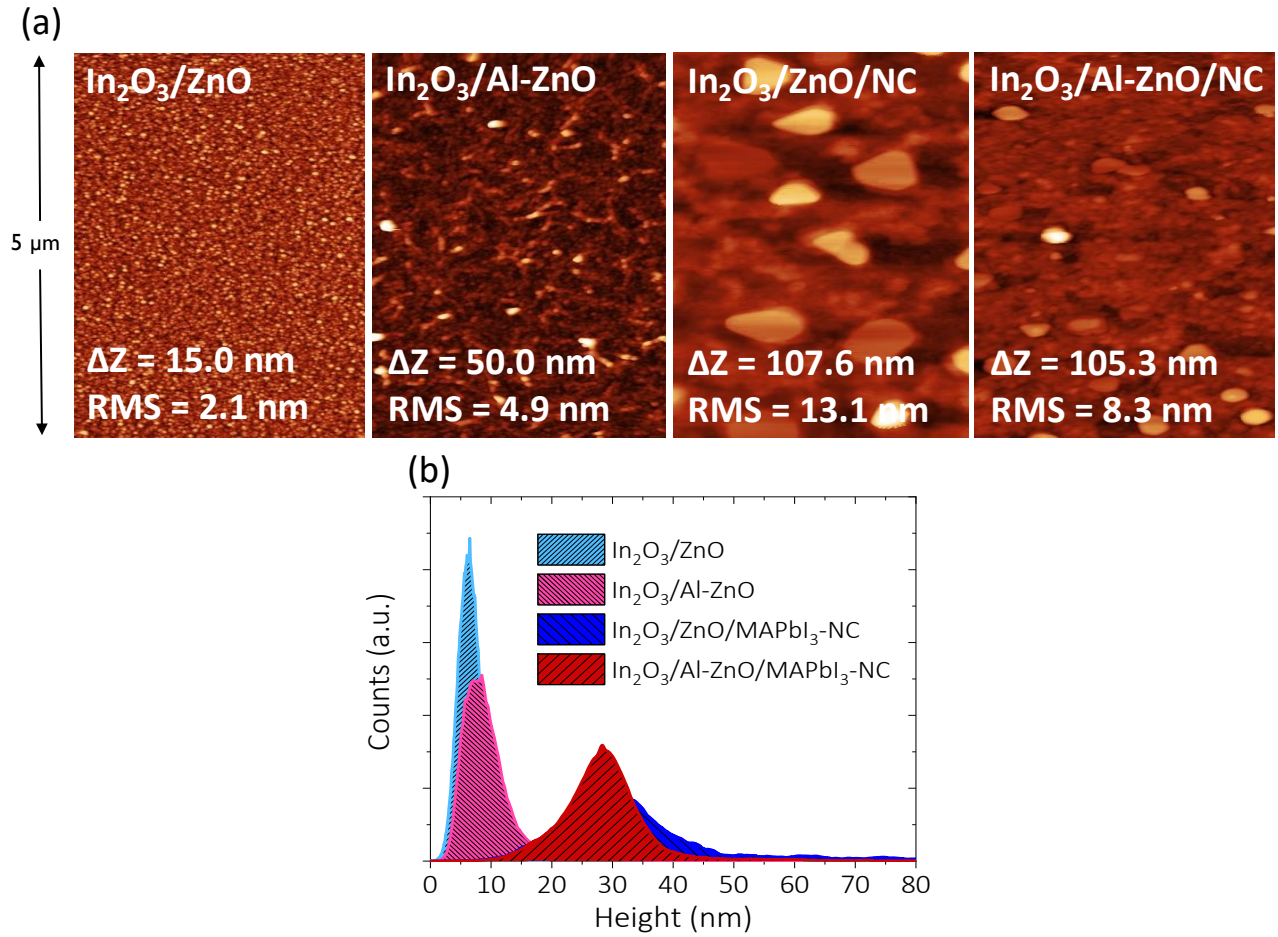


Figure 51: (a) AFM images of the surface topography of pristine In_2O_3/ZnO, In_2O_3/Al-ZnO channel layers and the NCs functionalised In_2O_3/ZnO, In_2O_3/Al-ZnO layers, respectively and **(b)** Height distribution histogram extracted from the AFM images in **(a)**.

Following the optical characterisation, field-effect measurements were carried out to investigate the impact of NCs on charge transport of fabricated In_2O_3/ZnO TFTs. The figure below, Fig. 52 illustrates the device schematic and corresponding transfer characteristics of In_2O_3/ZnO-NCs TFT measured in dark and under different intensities of light illumination (E_{opt}) at V_{DS} = 40 V. The relevant transfer characteristics of the HJ TFTs with and without the NCs measured under different light intensities are illustrated in Figs. S1-S2, Appendix A. These results prove the light absorbing properties of the NCs.

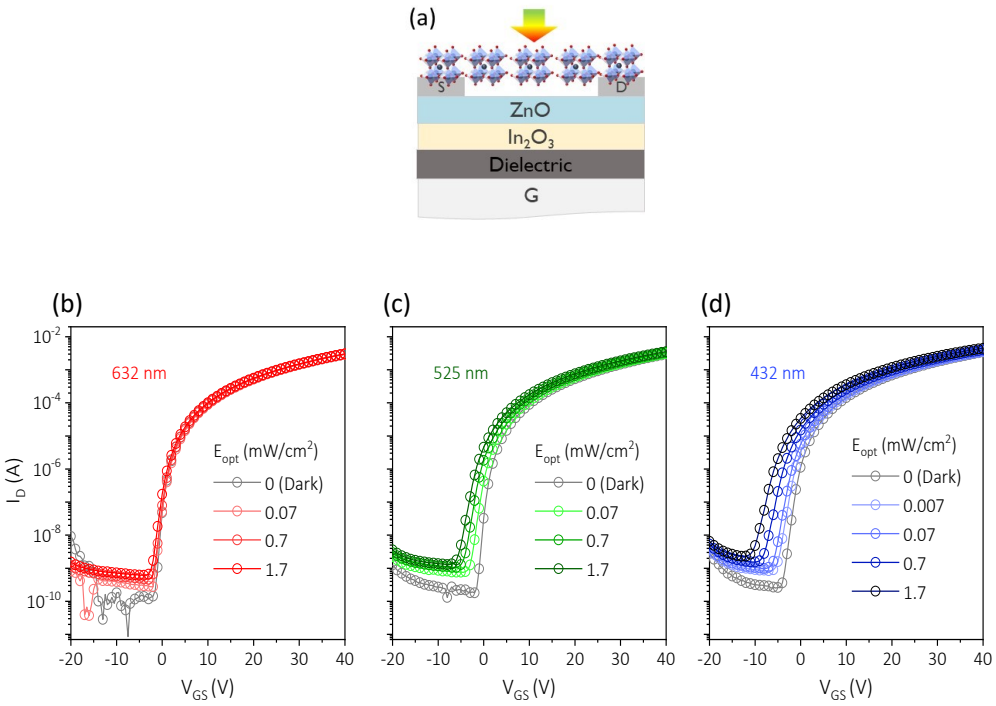


Figure 52: (a) Structure of a BG-TC In_2O_3/ZnO transistor developed, with the NCs deposited on top, **(b) – (d)** set of transfer characteristics measured at V_{DS} = 40 V for the TFTs under red, green, and blue illumination at different intensities.

The fabricated devices exhibit typical n-type behaviour indicating electron accumulation in the channel, with field effect mobilities of 4 – 8 cm^2/Vs. There is a change in device performance with the channel current levels increasing with an increase in light intensity. This is particularly the case for green and blue illumination, with the magnitude of the change being dependent on V_{GS} and illumination intensity. For red light illumination, the response is almost negligible. This characteristic indicates a strong photoresponse at shorter wavelengths (i.e. near UV region) across the entire operation range, with additional charges being introduced in the semiconducting channel region upon optical stimulation/photoexcitation of NCs. An internal signal gain mechanism, together with the generation of additional carriers, can also be attributed for the high photoresponse measured. The changes seen in both on-state and off-state can be attributed to the

amplification effect, a phenomenon not usual for photodetectors. A transistor, most commonly used as a switch in an electronic circuit, only conducts current when a voltage is applied to the base. Without any bias voltage, the transistor is in its off-state. When a base voltage is present, the switch is on and there is a current flow across the collector-emitter path. In an ideal situation, a transistor/switch can only be in one of the two states.

Additionally, there is a small change in the V_{ON} towards negative V_{GS} together with a marginal increase in I_{OFF}. Once more, these observations are more prominent for green and blue illumination. A possible explanation for such behaviour is photoconduction, which causes excitation of electrons/holes from impurity states due to absorption of photons producing a photocurrent[154]. The absorption of photons by the NC layer leads to a transfer of electrons from NCs to ZnO and subsequently to the CB of In_2O_3, causing an increase in electron concentration within the channel. In other words, excitons are formed within the In_2O_3/ZnO channel, which are eventually dissociated into mobile electrons drifting into the Al S/D electrodes as a result of the applied V_{GS} and V_{DS}[155]. This process would explain the negative shift of V_{ON} and also the increase in I_{OFF}.

Photodoping can be another reason for the observed shifts in V_{ON}, which is caused by the desorption of molecular oxygen from the channel surface, i.e. In_2O_3/ZnO due to illumination, similar to previously reported work by Verbakel et al.[111] and Lakhwani et al.[156]. Oxygen desorption causes the creation of a back channel, causing an increase in the channel electron concentration and thus the overall device conduction.

Similar observations were made for phototransistors with In_2O_3/Al-ZnO as the channel layer, with increased current levels in both on-state and off-state with increasing light intensity, especially for green and blue LEDs. These are better illustrated in Fig. 53

below. However, compared to the In_2O_3/ZnO TFTs, these devices are characterised by lower channel currents and hence lower values of responsivity, photosensitivity and detectivity, as can be seen in the results discussed later.

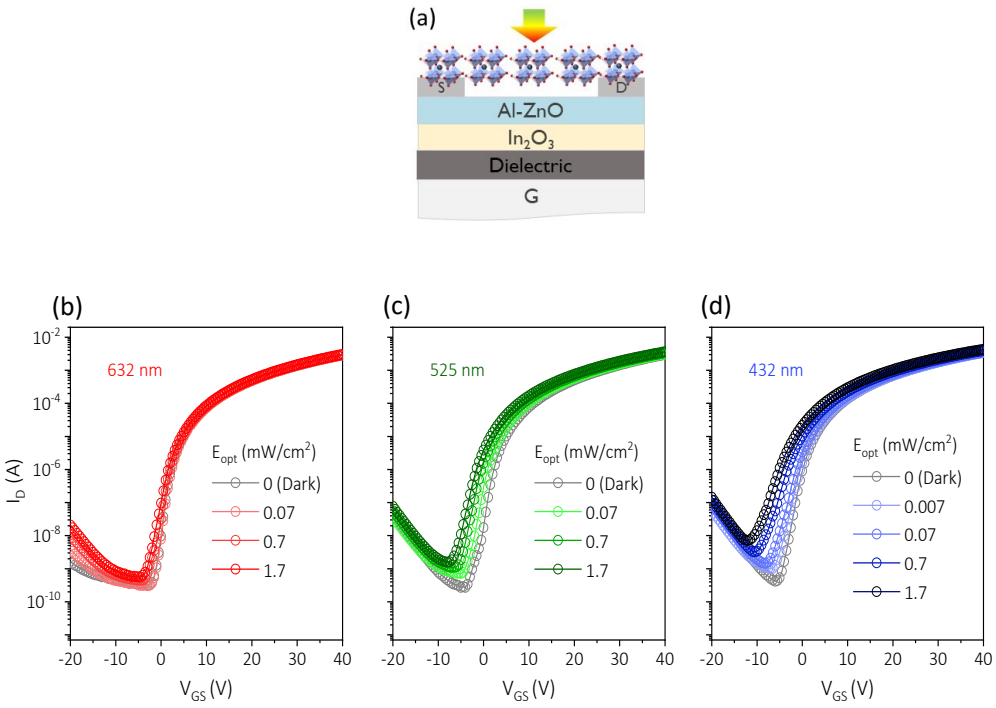


Figure 53: (a) Structure of a BG-TC In_2O_3/Al-ZnO transistor developed, with the NCs deposited on top, **(b) – (d)** set of transfer characteristics measured at V_{DS} = 40 V for the TFTs under red, green, and blue illumination at different intensities.

The performance characteristics of the fabricated phototransistors were further analysed using three figures of merit or important photodetector/photoconductor parameters, namely responsivity (R), photosensitivity (P) and detectivity (D_s^*) under different light illumination intensities. By altering the applied gate-field (V_{GS}), the conductivity of the channel can be modified or controlled and hence the R, P and D_s^* is dependent on V_{GS}, which is why the parameters were calculated as a function of V_{GS} in order to obtain the ideal operating region. Fig. 54 & Fig. 55 below illustrates the different

parameters (responsivity, photosensitivity and detectivity) calculated for In_2O_3/ZnO-NCs & In_2O_3/Al-ZnO-NCs based TFTs to red, green and blue illumination.

R is defined as the efficient conversion of optical power into measurable electrical photocurrent, and is the ratio of photogenerated current to incident optical power (P_{opt}). R can be calculated using the equation:

$$\boldsymbol{R = \frac{I_{ph}}{P_{opt}} = \frac{I_{illumination} - I_{dark}}{E_{opt} \times a}} \quad \textbf{(16)}$$

where *a* defines the device area. On the contrary, P is the ratio of photogenerated current to dark current, and is given by

$$\boldsymbol{P = \frac{I_{ph}}{I_{dark}} = \frac{I_{illumination} - I_{dark}}{I_{dark}}} \quad \textbf{(17)}$$

$I_{illumination}$ and I_{dark} define the device drain current under illumination and dark conditions, respectively. Detectivity values are in respect to noise and defined as

$$\boldsymbol{D^* = \frac{\sqrt{a}.R}{S_{noise}}} \quad \textbf{(18)}$$

where S_{noise} denotes noise spectral density. From the various sources which contribute to the total noise limiting D^*, shot noise from dark current is assumed to contribute the most to the total noise[157]. Hence, shot-noise limited detectivity is given by

$$\boldsymbol{D_S{}^* = \frac{\sqrt{a}.R}{\sqrt{2qI_{dark}}}} \quad \textbf{(19)}$$

where *q* is the charge of an electron, 1.6×10^{-19} C.

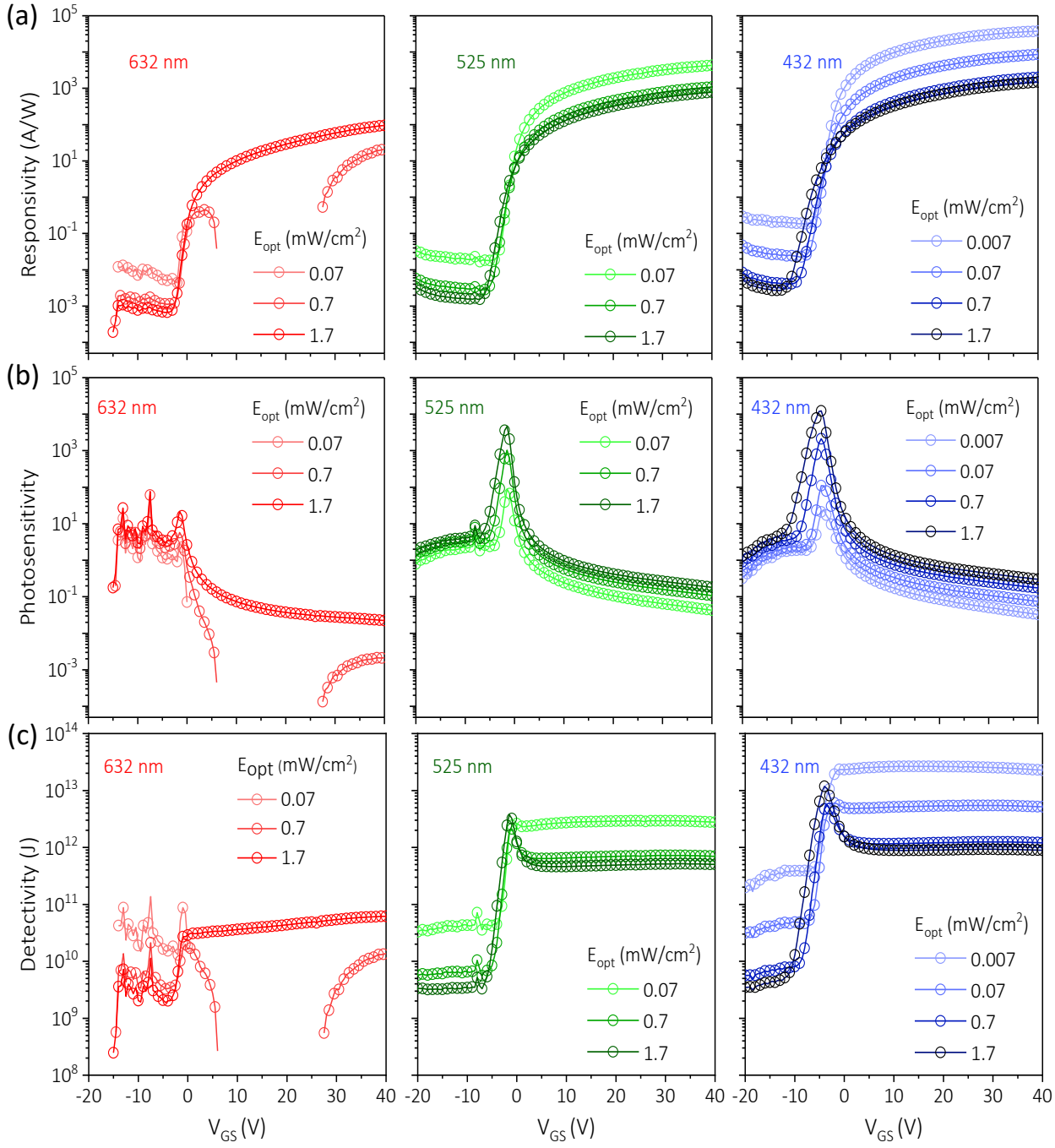


Figure 54: Optoelectronic characterization of the NCs-In_2O_3/ZnO phototransistors. **(a)** Responsivity (R), **(b)** Photosensitivity (P), and **(c)** Detectivity (D_s^*) measured under red, green and blue illumination at different intensities vs. V_{GS} at V_{DS} = 40 V.

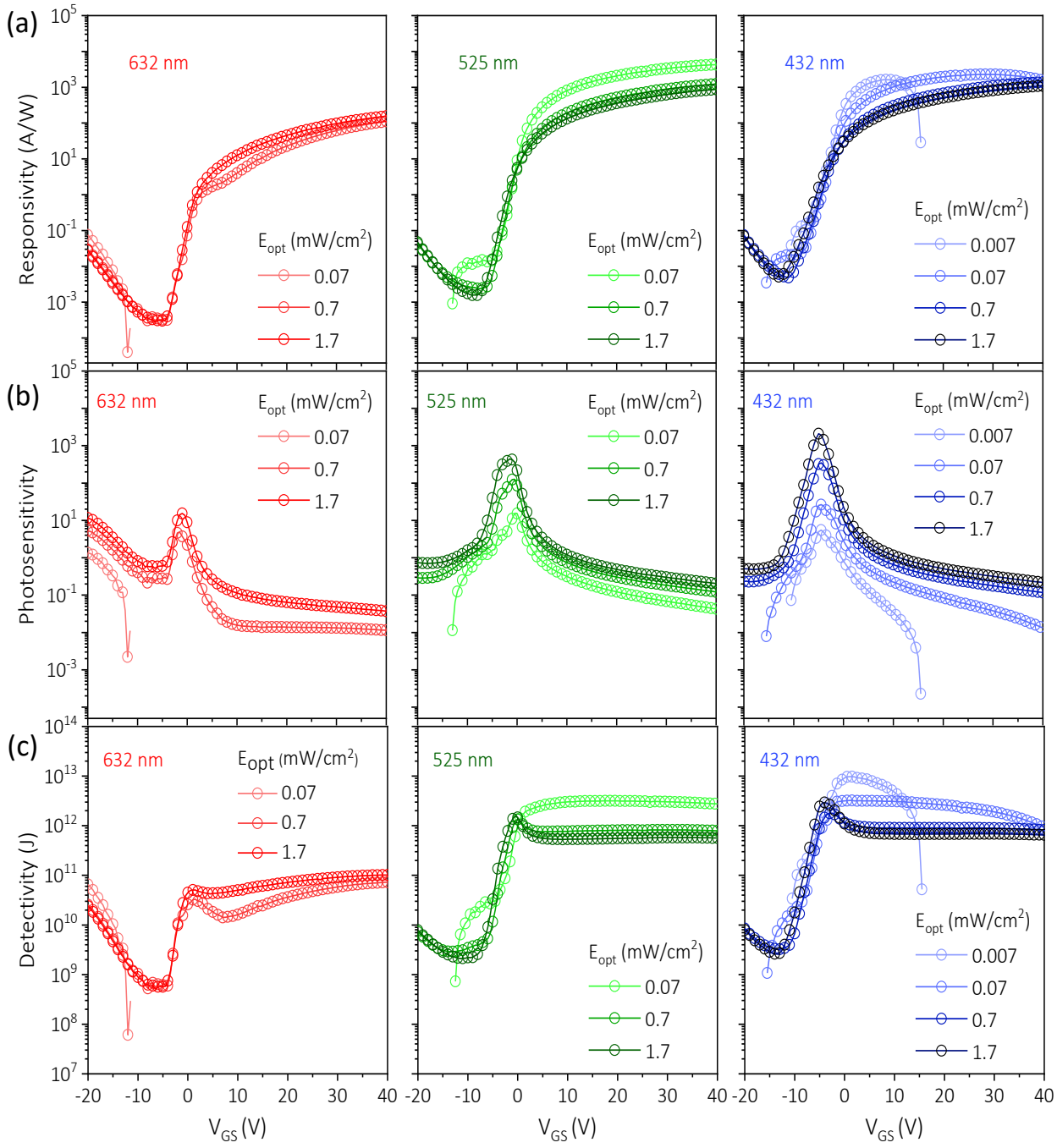


Figure 55: Optoelectronic characterization of the NCs-In_2O_3/Al-ZnO phototransistors. **(a)** Responsivity (R), **(b)** Photosensitivity (P), and **(c)** Detectivity (D_s^*) measured under red, green and blue illumination at different intensities vs. V_{GS} at V_{DS} = 40 V.

For responsivity, increasing V_{GS} leads to an increase in responsivity due to (i) enhanced charge photogeneration and (ii) improved charge transport across the channel. However, lower illumination intensities produce a greater change in current per watt (A/W), as shown in Fig. 54(a) & Fig. 55(a). This can be attributed to the cumulative nature of response over time till it reaches equilibrium, due to which an increasing illumination intensity would produce diminishing gains because of the availability of less oxygen to be desorbed, causing a smaller photodoping effect. Another reason for the observed reduction in responsivity for increased illumination is due to channel current (A) being in the same range, while the illumination or optical power (W) increases.

Photosensitivity, on the other hand, peaks at $V_{GS} \approx -2$ V for green light and $V_{GS} \approx -4$ V for blue light with maximum values of $\approx 10^4$. At these particular V_{GS} biases, the devices are approaching its turn-on voltage range, which causes the photodoping effect to shift the transistor into subthreshold operating regime. This characteristic is opposite to that seen for responsivity, where minimum R values are obtained at these voltages. At these specific values, channel current is turned off while I_{dark} reaches its minimum values, thus leading to maximum P values. In addition to this, another observation was the decrease of P values with an increasing V_{GS}. This is an indication of channel current being primarily dominated by injected carriers at higher V_{GS} while the concentration of photoinduced carriers is less dominant. However, an increase in P with increasing light illumination intensity across the entire operating voltage range highlights the presence of photogenerated carriers at higher V_{GS}. In other words, it can be stated that these devices exhibit a high signal amplification, whilst the response to incident optical power is highly non-linear.

The sensitivity of a detector with respect to noise is given by detectivity, D^* enabling a direct comparison of different devices with varying areas/geometries. Fig. 54(c) & Fig. 55(c) illustrating the specific detectivity for the fabricated devices reveals the area with highest values calculated at around $V_{GS} \approx 2 – 4$ V. This sharp increase seen at these particular voltage range can be attributed to the low levels of background noise which is due to the suppressed channel current. Additionally, at this bias range, channel current is switched off with the lowest levels of shot noise observed, resulting in the highest values of D_S^*. The figure reveals another distinct region after the peak values, demonstrating the saturation of detectivity levels with an increasing V_{GS}. On the contrary, the increasing trend of D_S^* with increasing V_{GS} is a result of the improved current amplification due to the improvement of carrier mobility. From these measurements and analysis, it can be concluded that to completely exploit the signal gain mechanism, the phototransistors should be operated at low optical powers. This leads to the maximum values of D_S^* (3.8×10^{12} Jones and 1.7×10^{13} Jones for green and blue illumination, respectively) being calculated, which is comparable to that measured for previously reported photodetectors.

In order to get a better understanding of photoresponse of the fabricated phototransistors to the different colour LEDs, responsivity (R), photosensitivity (P) and detectivity (D_s^*) were measured and quantitatively analysed at the highest intensity (1.7 mW/cm^2) condition for red, green and blue lights. Figs. 56(a-c) below illustrate these results for the phototransistors based on In_2O_3/ZnO-NCs, indicating a higher response for light with shorter wavelengths. Fig. 56(d) summarises these results with the highest/peak values for R, P and D_s^* plotted against the different LED lights used. The fabricated

phototransistors have the ability to function as photodetectors combining high sensitivity together with a simplified device architecture.

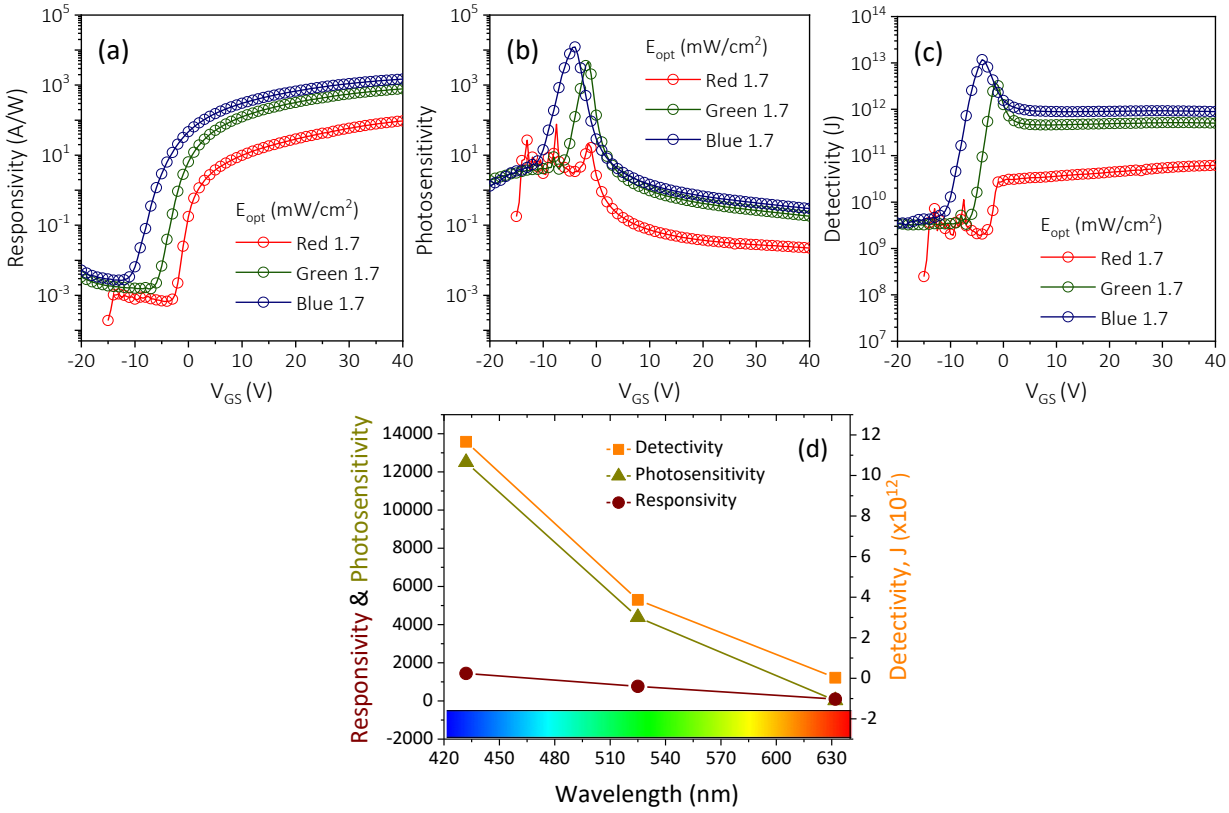


Figure 56: Optoelectronic characterisation for NCs-In_2O_3/ZnO phototransistors. **(a)** Responsivity (R), **(b)** Photosensitivity (P), **(c)** Detectivity (D_s^*), and **(d)** highest calculated values for R, P and D_s^*. All parameters were calculated from transfer characteristics at V_{DS} = 40 V under red, green and blue illumination at highest intensity (E_{opt} = 1.7 mW/cm^2).

A similar analysis was done for the phototransistors with In_2O_3/Al-ZnO as the channel layer, with the results illustrated in Fig. 57. These devices exhibit similar photoresponse behaviour with higher responses measured for shorter wavelengths.

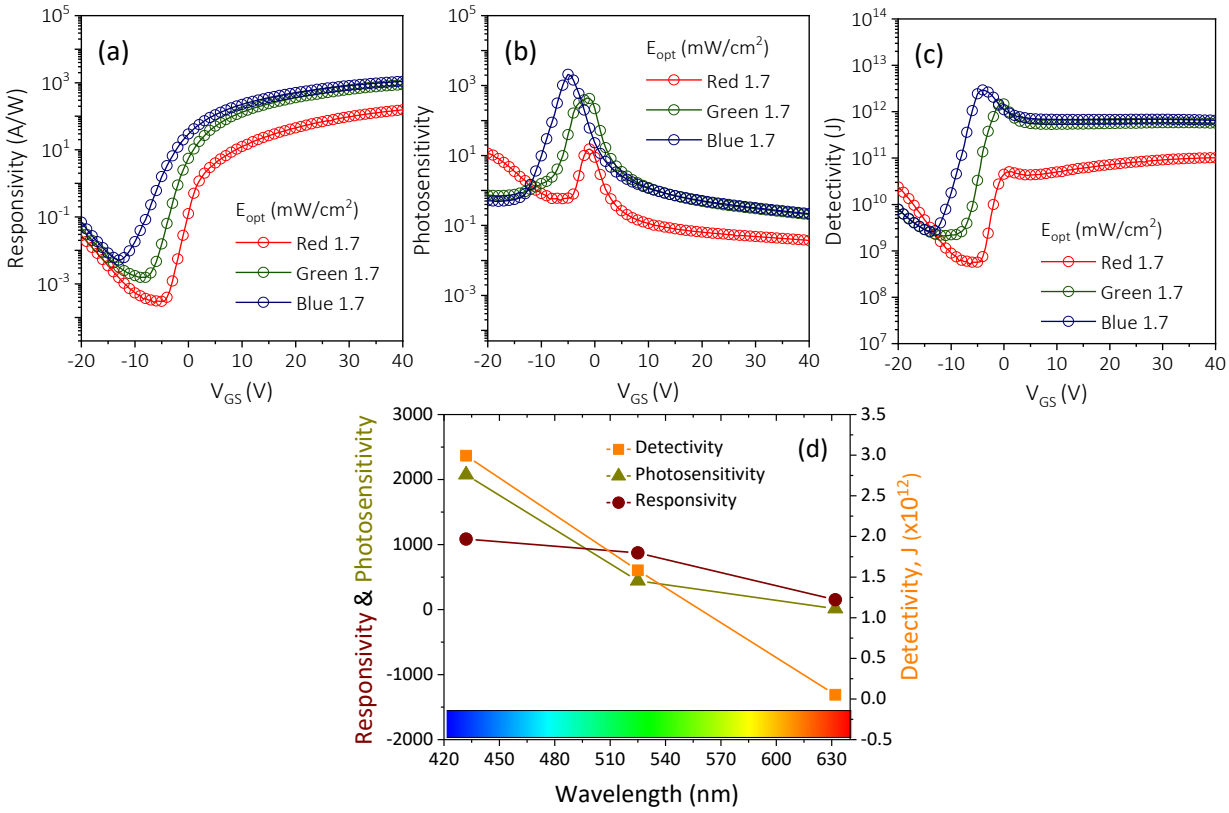


Figure 57: Optoelectronic characterisation for NCs-In_2O_3/Al-ZnO phototransistors. **(a)** Responsivity (R), **(b)** Photosensitivity (P), **(c)** Detectivity (D_s^*)**,** and **(d)** highest calculated values for R, P and D_s^*. All parameters were calculated from transfer characteristics at V_{DS} = 40 V under red, green and blue illumination at highest intensity (E_{opt} = 1.7 mW/cm^2).

In addition to high sensitivity and spectra selectivity, any emerging photodetector technology should have a good temporal response. Hence, the dynamic response of the fabricated phototransistors was studied to provide an insight into the switching behaviour of these devices. This was accomplished by subjecting the devices to a green light pulse and analysing the channel current in real-time utilising the setup shown in Fig. 58(a). A function generator (FG) was used to drive the LED; transistor channel current was monitored using a current amplifier (CA) with the current recorded as a voltage (V_{OUT}) using an oscilloscope.

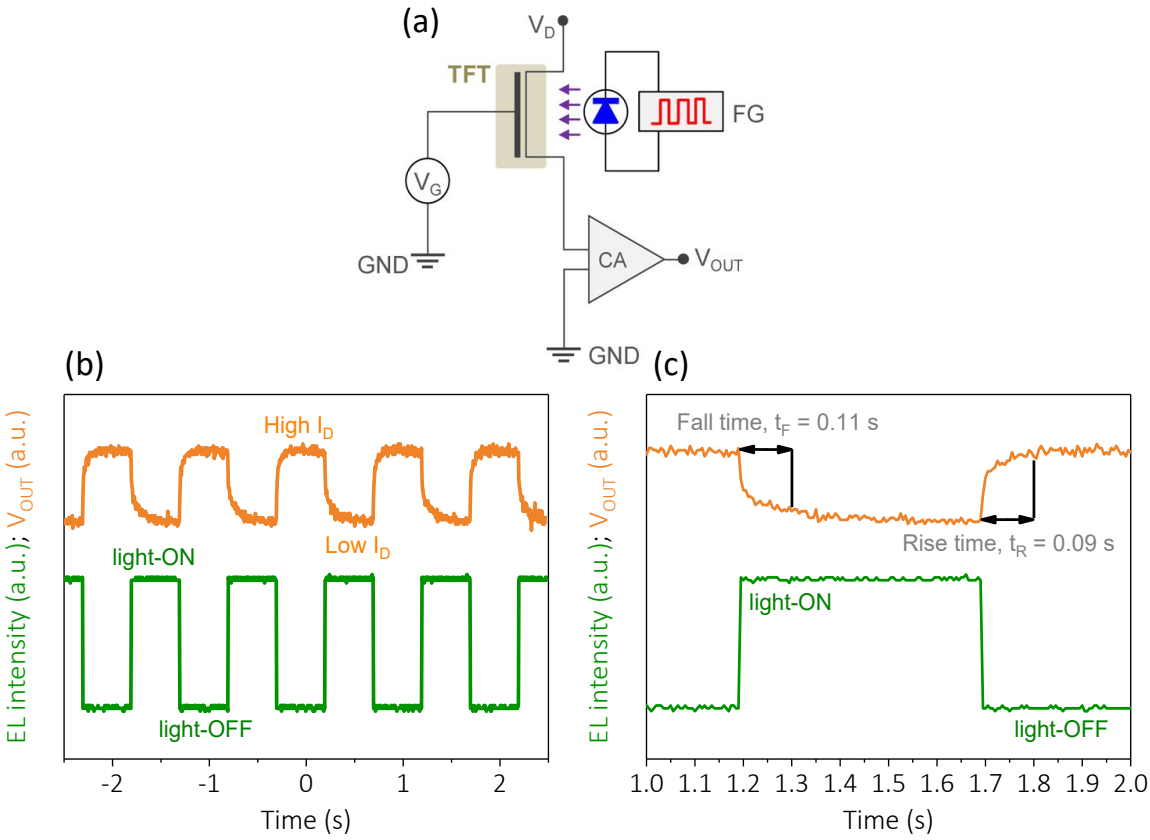


Figure 58: Dynamic characterisation of hybrid oxide-NCs phototransistors. **(a)** Circuitry of the experimental setup utilised, **(b)** response of the channel current (orange trace) to a train of green light pulses (green trace), and **(c)** fall (t_F) and rise (t_R) time analysis obtained from **(b)**.

The dynamic response of channel current to the green light pulse is shown in Fig. 58(b), with fall time (t_F) and rise time (t_R) calculated to be 0.11 secs. and 0.09 secs., respectively, as shown in Fig. 58(c). Fall time is defined as the time for channel current to decrease from 90% to 10% of the maximum value, while rise time is the time required for current to increase from 10% to 90% of maximum value. These results illustrate a fast response of the fabricated phototransistors due to efficient charge carrier generation and overall charge transport within/across the channel.

7.3 Conclusion

To summarise, solution-processed hybrid oxide-perovskite phototransistors were fabricated exhibiting n-type behaviour. The results prove the light absorbing characteristics of $CH_3NH_3PbI_3$ NCs, with the fabricated devices exhibiting large photoresponse, mainly at shorter wavelengths of electromagnetic spectrum. Moreover, a strong gating effect was observed for light with shorter wavelengths, which was able to modulate the channel current independently. The phototransistors with channel lengths of 40 µm, notably, demonstrate the capability to operate at high frequencies with a response time of 0.2 secs. These devices, with promising photoresponse (responsivity, ≈ 10^4 A/W, photosensitivity ≈ 10^4 and detectivity ≈ 10^{13} Jones) can be regarded as an ideal platform for developing fast photodetectors and are comparable to other hybrid oxide-perovskite based phototransistors/photodetectors reported. A major factor contributing to such promising results is primarily due to the intrinsic gain mechanism associated by utilising a three-terminal device architecture. Overall, these hybrid oxide-perovskite phototransistors can be considered promising candidates for alternative photodetector technologies.

8. SUMMARY

This thesis has discussed a few different approaches to overcome some of the challenges faced by the large-area electronics sector in relation to the use of low-temperature, solution-processed metal-oxide and organic semiconductors for TFTs. A key aspect of this thesis was a focus on the growth of different films and analysing the electrical properties of the semiconductors. The following section summarises the key findings as outlined in the preceding chapters of this thesis and also discusses the future research prospects in this field of electronic technology.

Chapter 4 introduced the concept of using a low-dimensional, solution-grown (via ultrasonic spray pyrolysis and spin coating) In_2O_3/ZnO heterojunction channel instead of a single-layer semiconductor channel for fabricating TFTs. This multi-layered approach led to an enhancement in device performance, with significantly higher charge carrier mobility values (≈ 45 cm^2/Vs) than single-layer transistors. This was due to the transfer and subsequent confinement of electrons at the atomically sharp heterointerface leading to the formation of a quasi-2DEG at its vicinity, a behaviour similar to conventional HEMTs consisting of heterointerface channels. In addition to the high mobility values, the In_2O_3/ZnO HJ TFTs illustrated a dramatic change in their charge transport mechanism compared to single-layer In_2O_3 TFTs. Further electrical characterisations provided evidence of the overall stability of these devices under ambient atmospheres while AFM and TEM studies revealed the correlation of good film morphologies on device performance.

In Chapter 5, a facile n-type hybrid doping approach of organic semiconductors ($PC_{60}BM$ and C_{60}:C_{70} blend) using the dopant, N-DMBI on the previously demonstrated In_2O_3/ZnO TFTs was introduced. An additional organic molecular layer (10 – 15 nm) of fullerenes, doped at different concentrations, was spin coated on top of the HJ layer to study the cascading doping effect to the 2DEG channel. From the electrical characterisations carried out, there was no evidence of any improvement in the device performance/charge transport, with mobility values calculated in the range of 30 – 40 cm^2/Vs. However, these TFTs were able to accommodate additional carriers generated into the channel from the dopant/organic layer without any adverse (doping) effects. The results aid in the understanding of modulation doping (MOD) in organic-oxide semiconductors whilst also providing a new, simple and powerful strategy to utilise an excellent TFT platform for photodetectors and senor applications.

Chapter 6 focused on the introduction and use of different high-κ oxide-based gate dielectric materials, deposited via UV light assisted and solution-processed methods, to fabricate TFTs. By using these materials, the operating voltage of ultra-thin In_2O_3/ZnO TFTs was reduced to about ± 2 V. Additionally, the entire fabrication process was demonstrated to be compatible with the use of temperature-sensitive flexible polyimide (PI) films/substrates. In terms of performance, the fabricated devices exhibited hysteresis-free operation with current on/off ratios of 10^3, electron mobilities of ≈ 25 cm^2/Vs together with the reduced operating voltage range. With optimisations to improve the current on/off ratios, this work can be regarded as an important step towards the understanding and utilisation of high-performance electronics for low-power electronic applications.

Finally, Chapter 7 demonstrated a phototransistor concept by developing hybrid oxide-perovskite TFT architectures for fast and highly sensitive broadband photodetectors. The oxide semiconducting and perovskite layers were deposited via sequential spin casting at temperatures < 250° C, with the fabricated devices characterised in dark conditions and under illumination at different light intensities and wavelengths. The phototransistors exhibited significant photoresponse, especially at shorter wavelengths of the electromagnetic spectrum, and excellent dynamic response/switching behaviour. The results illustrate the light absorbing characteristics of the perovskite nanocrystals and the potential of these hybrid devices for alternative photodetector technologies.

Overall, this work aided in determining new and different approaches to demonstrate low-dimensional metal oxide transistors exhibiting high electrical performance. Due to their enhanced performance, these devices can be adapted for various potential electronic devices for large-area applications, which cannot be met by existing incumbent technologies. Moreover, this work is likely to be applicable to a range of oxide systems and fabrication techniques due to the flexibility of solution-processing. Whilst this thesis only focused on a limited range of materials, the simplicity and universality associated with this method could easily be incorporated with other semiconductors and dopants.

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APPENDIX A

This section contains additional/supplementary figures for some of the results discussed earlier in the thesis.

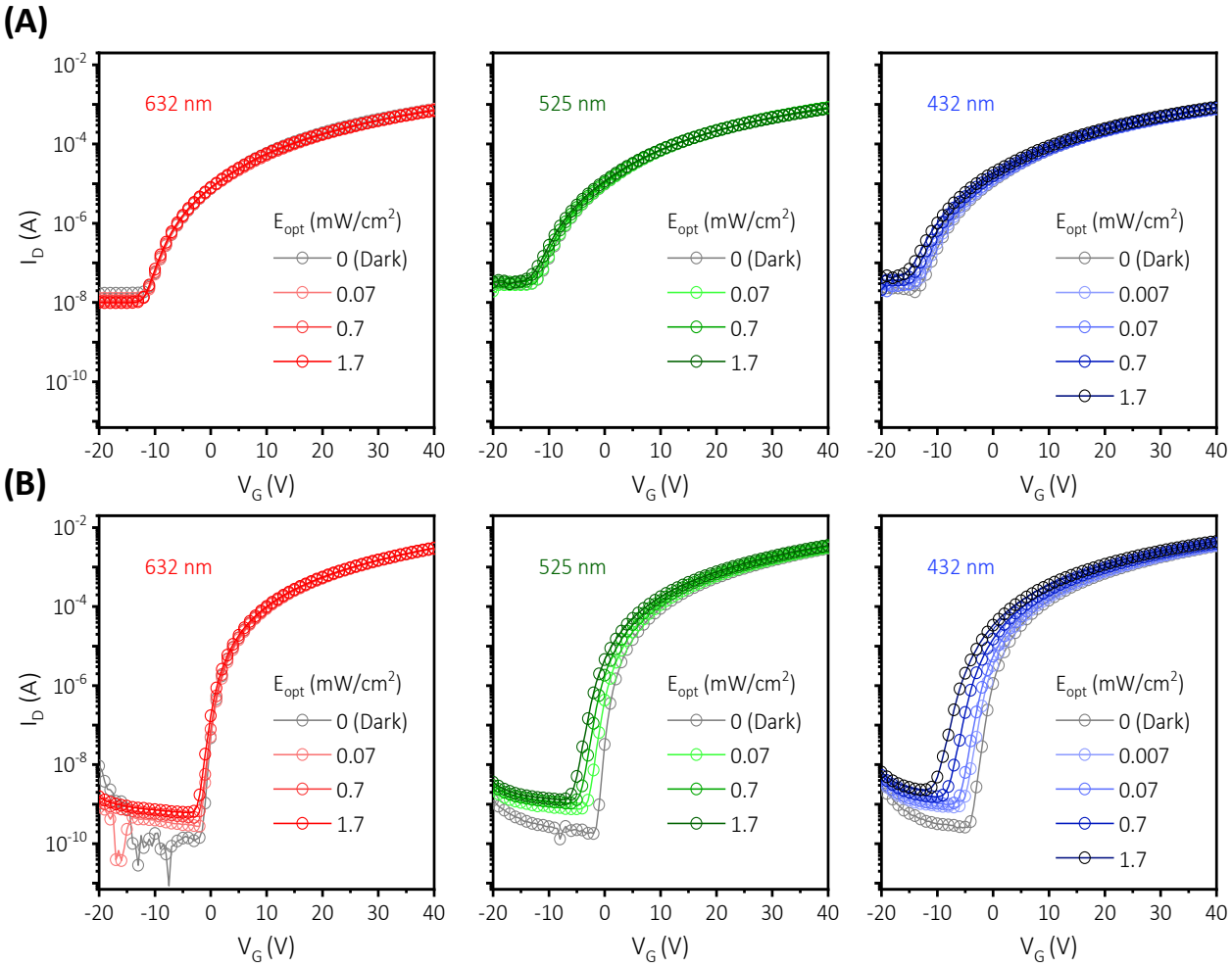


Figure S1: Transfer characteristics of In_2O_3/ZnO transistor measured at V_{DS} = 40 V under red, green, and blue illumination at different intensities; **(A)** without the NCs deposited on top, **(B)** with the NCs deposited on top.

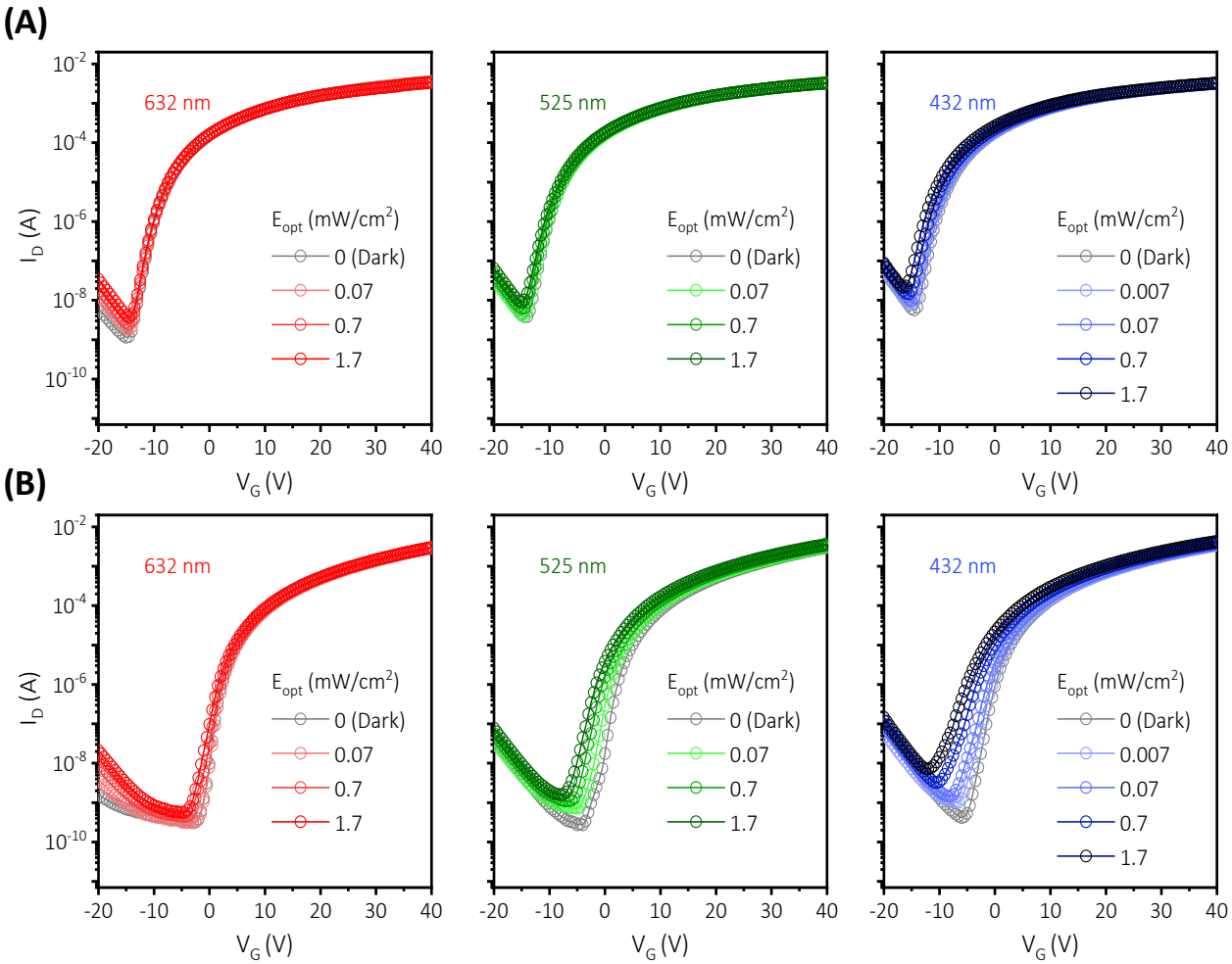


Figure S2: Transfer characteristics of In_2O_3/Al-ZnO transistor measured at V_{DS} = 40 V under red, green, and blue illumination at different intensities; **(A)** without the NCs deposited on top, **(B)** with the NCs deposited on top.

APPENDIX B

Part of Chapter 4 included in this thesis has subsequently been published and is available online. This appendix includes permission to use/reproduce the published content.

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