

A Novel Neural Recording System Utilising Continuous Time Energy Based Compression

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Abstract—This work presents a new data compression method that uses an energy operator to exploit the correlated energy in neural recording features in order to achieve adaptive sampling. This approach enhances conventional data converter topologies with the power saving of asynchronous systems while maintaining low complexity & high efficiency. The proposed scheme enables the transmission of 0.7kS/s, while preserving the features of the signal with an accuracy of 95%. It is also shown that the operation of the system is not susceptible to noise, even for signals with 1 dB SNR. The whole system consumes 3.94 μ W with an estimated area of 0.093 mm².

I. INTRODUCTION

Advances in neurophysiology have allowed scientists to understand the neural system on the cellular level and diagnose brain disorders, such as blindness, epilepsy, depression and Parkinson's disease. It has also been demonstrated that information from brain activity can give the ability to restore movement in paralysed parts and control robotic body parts or computer cursors [1]. Neurons transfer information by changing the electrical potential of the cell's membrane and creating Extracellular Action Potentials (EAPs), known as spikes. Information about brain activity is encoded in the timing and amplitude of these spikes. Their amplitude is approximately between 20 μ V and 5 mV [2], their duration is roughly 1msec and they are fired by neurons at a rate of 100Hz. Modern neural recording systems enable successful tracking, analysis and transmission of the neuronal activity.

These systems are usually battery based. Power dissipation has to be very low, so that battery does not need to be changed frequently and systems can be autonomous. This limitation restricts also the amount of data that can be transmitted out of the chip, since large output data rates will significantly increase the power consumption [3]. Bitrates of 2 Mbits/s and 40 Mbits/s result to a power dissipation of 14mW and 120mW respectively [3]. Increased power dissipation can damage the surrounding tissue, therefore it must not overcome the value of 10mW [4]. This limits the bitrate of the system to roughly 1 Mbit/s. The output data rate is also limited by the bandwidth of the biotelemetry unit.

By reducing the number of transmitted samples and the amount of dissipated power, the number of recording channels can significantly increase and scientists will be able to monitor the activity of a larger brain area. For that purpose, different temporal sparsity based data compression techniques have been developed. In [5], [6] the whole signal is sampled and then spike detection is applied, in order to keep only the samples that correspond to spikes. An improvement is shown in [7],

where B. Gosselin and M. Sawan propose a circuit with the spike detector used in the analogue part of the system. Data conversion circuits that follow this approach will sample the signal only when a spike event occurs. A different approach is illustrated in [8], where an adaptive sampling scheme is presented, based on the features of the neural signal. The above techniques rely on the fact that information about brain activity is encoded in spikes and therefore transmitted data can be reduced while spike integrity can be maintained. Wavelet transform and Compressed sensing based techniques have also been developed [9]. They allow almost lossless compression, but their design is more complex leading to increased design area.

This paper presents a novel data compression scheme that achieves adaptive sampling with low complexity by employing a SAR ADC whose clock frequency is dependent on the energy of the neural signal. The core block is the programmable clock generator that generates pulses at a rate which is proportional to its biasing current. The paper is organised as follows: Section II introduces the concept and system architecture; Section III details the circuit implementation; Section IV describes the simulated results; and Section V concludes the paper.

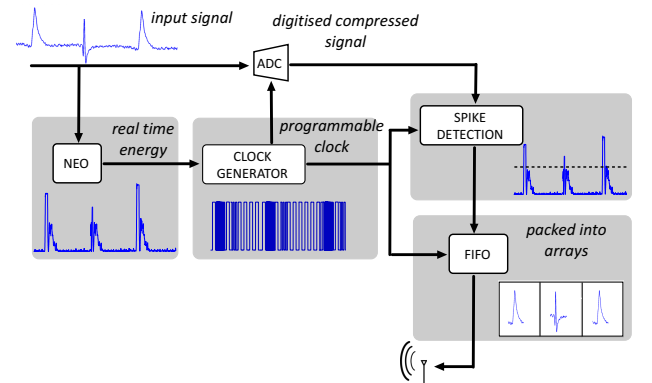


Fig. 1: System architecture of the proposed data compression system.

II. CONCEPT AND SYSTEM ARCHITECTURE

The operation of the system relies on the fact that the energy operator of the neural signal, boosts the SNR of the neural signal by decreasing the noise susceptibility and increasing the amplitude of the spikes. A clock generator, modulated by that energy signal, will give in the output a square pulse waveform, whose frequency is high during spike events and very low for the rest of the signal thus achieving energy modulated

frequency. By clocking an ADC with this waveform we acquire a digitised signal which consists mainly of sampled spikes and compressing the recording in an autonomous way. In most applications the information needed is the classification of the spike that arrives each time at the receiver. Therefore, the aim of this system was to minimise the number of transmitted samples while spike features are maintained and spikes can be classified with high accuracy. This objective directs the optimization and specification of each sub block quantitatively when post processing the adaptively resampled recording results as objective.

The system architecture comprises four basic blocks, as depicted in Fig 1. The non-linear energy operator (NEO) that calculates the real time energy of the signal, which is input to the programmable clock generator. The ADC is clocked by the energy modulated square pulse waveform and finally, spikes are detected in the digitised signal, in order to discard the redundant recordings, and are saved into a FIFO before transmission.

Its advantage comparing to circuits that use spike detection to avoid useless samples, is that, the sampling frequency is determined by the features of the AP and this ensures that all spikes will always be sampled, since they have high energy comparing to the rest of the signal. This continuous adaptive characteristic is demonstrated in Fig 2.

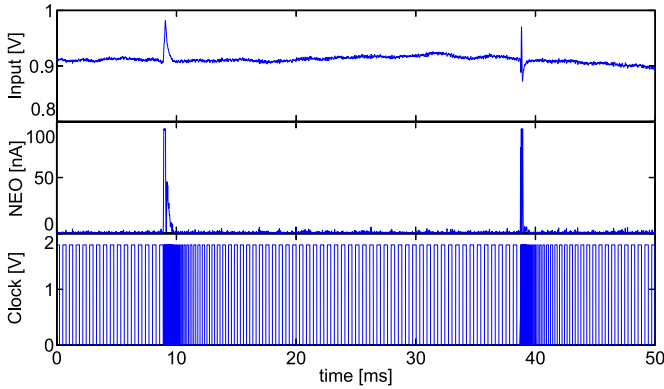


Fig. 2: Proposed concept of the energy modulated clock frequency. Shown are waveforms for the input signal, its real time energy and the generated clock.

III. CIRCUIT IMPLEMENTATION

The circuit has been implemented in a commercially available $0.18\mu\text{m}$ CMOS technology provided by AMS (C18A4) and has been designed to operate from a 1.8V supply. This section details the circuit level design and implementation.

A. Non-Linear Energy Operator

For the energy preprocessor block, the three energy operators described in [10] were tested. Their ability to preserve spike features was simulated in order to quantify which operator will result in better spike sorting performance. These results indicated the Ψ_{ED} operator has slight improvement in terms of accuracy but also noting its simplicity and smaller power budget gives it a considerable advantage over other energy

operators. The energy of derivative operator Ψ_{ED} is given by the equation

$$\Psi_{ED}[x(t)] = \left(\frac{dx(t)}{dt} \right)^2 \quad (1)$$

where $x(t)$ is the input signal. The circuit implementation comprises only a derivative and a multiplier circuit.

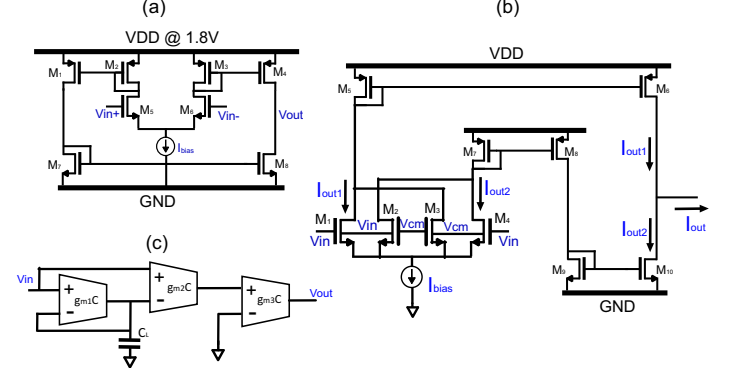


Fig. 3: Circuit implementation of the energy operator. Shown are (a) sub-threshold OTA circuit (b) $g_m C$ based differentiator (c) four quadrant analogue multiplier

The implementation of the differentiator was based in the approach described in [7]. As depicted in Fig. 3(b) the circuit comprises $g_m C$ components. The basic block is the OTA, Fig. 3(a). All transistors apart from M5, M6 are current sources and have to be in saturation. Differential pair transistors are in sub-threshold region, in order to achieve low power and reduced input referred noise [11]. Since the OTA is operating in sub-threshold region, its transconductance will be proportional to its biasing current.

$$g_{m(OTA)} = \frac{I_D}{nV_T} \quad (2)$$

Where V_T is the thermal voltage. The transfer function of the differentiator can then be described by the equation

$$\frac{V_{diff}}{V_{input}} = \frac{s \cdot C}{g_{m1} + s \cdot C} \cdot \frac{g_{m2}}{g_{m3}} \quad (3)$$

Finally, the squarer implemented, which is shown in Fig. 3(c), is based on a *Type V* four quadrant multiplier, realised by four cross coupled transistors in saturation. The original circuit is analysed in [12]. Its output current is

$$I_{out} = I_{out1} - I_{out2} = 4Kxy \quad (4)$$

B. Clock Generator

For this system a novel clock generator has been implemented. The circuit is annotated in Fig. 4. The output frequency of the oscillator is tuned by a biasing current. The design is based on the conventional 3-stage ring oscillator with a modified delay cell, in order to achieve improved noise figure and achieve linear current frequency dependence up to 100nA.

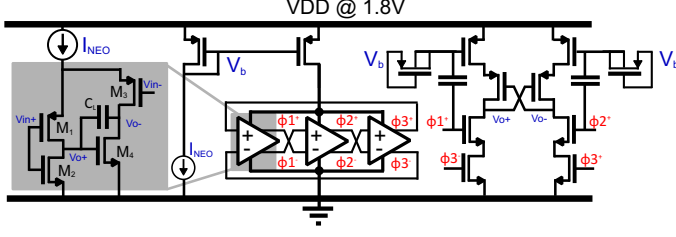


Fig. 4: Schematic illustration of the programmable pulse generator.

Ring oscillator output is connected to a high gain class AB amplifier. The amplifier employs a decision circuit to extend the clock to full voltage range. The final output has full voltage swing and rising and falling time delay of $10^{-3}\%$ of the corresponding frequency, while the amplifier dissipates only 10% additional power. Between the output of the energy preprocessor and the input of the clock generator a current mirror is used. By changing the aspect ratio of its transistors, the resolution of the digitised signal can also be changed.

C. SAR ADC

Fig. 5(a) illustrates the 8-bit SAR ADC circuit. The circuit incorporates top plate sampling and a monotonic switching scheme to further reduce the power dissipation, comparing to conventional SAR ADCs. The implementation consists of a DAC, a dynamic latched comparator, switches, the SAR digital block and was originally described in [13].

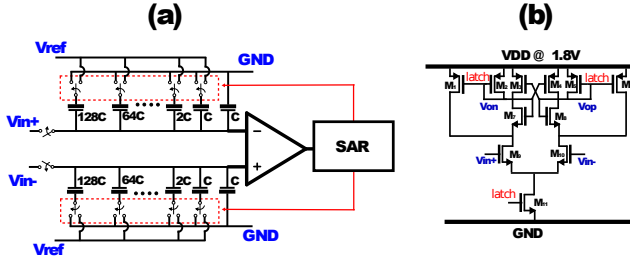


Fig. 5: Circuit implementation of the ADC. Shown are (a) 8-bit differential SAR ADC (b) Dynamic latched comparator

D. Digital Back-End

In the digitised signal, spikes must be separated from the unused data before transmission. A threshold is applied in the energy operator instead of the input signal because the energy operator can decrease any noise components that may exist. After a detection event, N samples are saved into a FIFO. N can be considered as the width of the window that allows the signal to pass and is a system parameter. Changing the window width the processed data can be further compressed. When the FIFO is filled, the data is sent to the output pin. The digital Back-end of the system is depicted in Fig 6. Note that if a spike is processed that has NEO energy below the threshold the ADC will briefly increase sampling speed but not request the transmission of spike data.

IV. SIMULATION RESULTS

Preliminary validation of the proposed implementation has been achieved using schematic level simulations in the

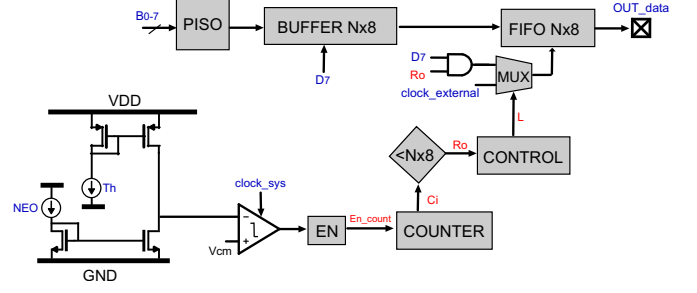


Fig. 6: Asynchronous Digital Interface with handshake & spike detection.

Cadence IC 6.1.5 Design Environment using industry provided transistor models for the commercially. Post-simulation data processing was implemented in Matlab R2014a. For testing, datasets from [14] were scaled to 400mVpp and used to evaluate performance assuming the signal is conditioned by a preceeding low noise amplifier.

Through simulations it was evaluated how small the window size and the resolution of each spike can be, while the spike features are preserved, so that the spikes can be clustered with high accuracy. Before k-means clustering, vectors of detected spikes were projected to a reduced-dimensional space through principle component analysis (PCA), because the k-means algorithm has poor performance in multivariate datasets. The metric used for quantification of results, corresponds to clustering accuracy and is described in [14]

$$FOM[operator] = \frac{S_{acc}}{S_{det}} \quad (5)$$

where S_{det} is the number of spikes that were correctly detected and S_{acc} is the number of spikes that were correctly clustered. Fig. 7 depicts the accuracy of spike clustering for different values of resolution and window size, for the three different energy operators and Fig. 8 shows how k-means clustering on PCA processed data, changes for different parameter values.

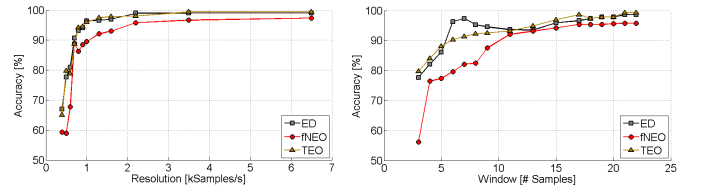


Fig. 7: Post processing of system level simulation results with clustering illustrating a dependence of accuracy for different configurations (a) clustering accuracy for different values of window size. (b) clustering accuracy for different values of signal resolution.

For Ψ_{ED} , it can be observed that for resolution until 2.2 kS/s and a window size of 7 samples, the spikes can be classified with an accuracy of approximately 95%. Further reduction of the window parameter will result in loss of information, and spikes will all look similar. Assuming that less than 100 spikes occur per second and that the bitrate of the system is limited to 1Mbit/s, our design allows the existence of 1500 channels in a neural recording system.

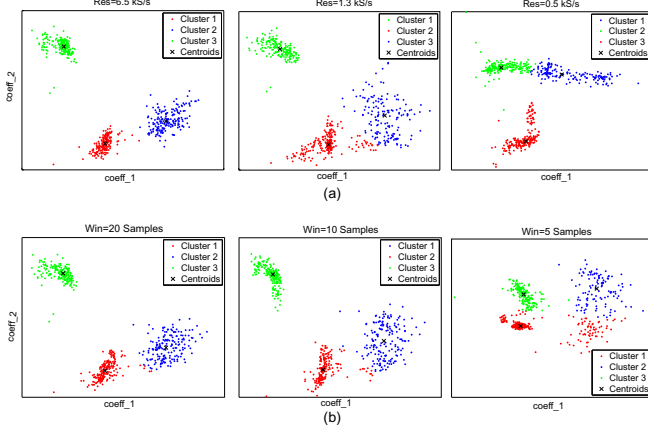


Fig. 8: Corresponding dynamics of feature distribution as system configuration changes (a) K-means clusters for different spike resolution. (b) K-means clusters for different window size.

The system was also simulated for a 1 dB SNR signal, in order to evaluate the performance of the proposed data compression method for noisy signal. Results in Fig. 9, indicate that our system can denoise, even signals with very low SNR and preserve the information about spike types. The whole operation dissipates $3.935\mu W$ of power at an area of 0.093 mm^2 . The overall performance of the system is summarised in Table I.

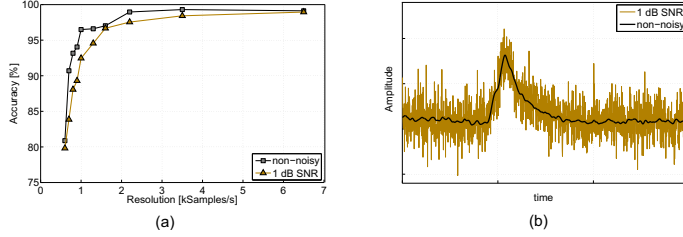


Fig. 9: (a) Accuracy of spike clustering as resolution changes, for a non-noisy and a 1 dB SNR signal. (b) Spike shape with and without noise.

TABLE I: System Performance Summary.

Specifications	Simulation Results
Technology	180 nm
Power Supply	1.8 V
Area	0.093 mm ²
AP Resolution (average)	2.2 kS/s
Clock Frequency (average)	0.53 kHz
Output Data Rate (max)	0.7 kS/s
Power Consumption (average)	3.94 μW
Number of Channels that can be Transmitted	1500

V. CONCLUSION

A novel data compression technique for neural recording systems was proposed. The scheme analysed is exploiting the features of AP, through an energy operator, in order to achieve adaptive sampling. For the design, the performance of three different energy operators was considered and the results

indicated the implementation of the 'Energy of Derivative'. The system has $3.94\mu W$ average power dissipation, at an area of 0.093 mm^2 . System level simulations illustrated how spike features can be preserved, while changing system parameters to change compression ratio. This was achieved for a spike resolution, only 5 times larger than the average sampling frequency. Since neural signals can be noisy, the operation of the design was also tested for low SNR signals and it was shown that noise can be removed efficiently. Output data transmission rate of 0.7 kS/s, while spike clustering can have 95% accuracy was a very promising results. It is concluded that by employing the proposed sampling scheme in a neural recording system, transmission of 1500 channels can be achieved.

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