

UNIVERSITY OF LONDON
IMPERIAL COLLEGE OF SCIENCE AND TECHNOLOGY
DEPARTMENT OF ELECTRICAL ENGINEERING

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DYNAMIC MODELLING OF POWER SYSTEMS
USING MICROPROCESSORS

BY

MASOUD ALIPOUR

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Abstract

The training of staff at power system control centers can be enhanced by using dynamic simulators for exercises in economic load dispatching and system frequency control. In this project an evaluation has been made of the capability of an 8-bit microprocessor for simulating in real time the power/frequency dynamics of a power system.

A motorola M6800 microcomputer kit has been programmed to simulate the longer-term dynamic performance of a single turbo-alternator and associated governor. A variable load, recorded on a cassette tape, can be fed into the simulation and a simple representation of the power/frequency characteristic enables the variations of power system frequency to be computed. The user can change the set-point of the turbine governor and thereby represent the actions of a load dispatcher attempting to maintain a target frequency.

A mimic diagram and control panel has been built to provide the user with a range of generator controls and meters for displaying loads, frequency, costs, etc..... An x-y plotter enables a variety of load curves to be recorded and the responses of user of the simulator to be plotted.

The simulation has been implemented using a wide range of typical parameters and the dynamic response has been checked against analogue simulations. It is evident that there is a trade-off between simulation complexity and performance accuracy in the real time environment. However, memory and I/O expansion would enable more generating units to be simulated and more variables to be output and displayed.

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CHAPTER 1

INTRODUCTION

1.1 General Consideration of Power System Simulators

The fact that electrical energy can not be directly stored in any appreciable quantity plays an important part in the control of an electric power system. There must, therefore, be an exact match at all times between the mechanical power generated and that consumed by the various loads attached to the system. The control problem is increased by the large number and varied nature of the consumers, whose behaviour exhibits random characteristics, and by the fact that the power is generated by many separated plants.

The shortfall between generation and consumption must be constantly monitored in order to adjust the level of generation to meet the load. The generation deficit manifests itself initially as a change of system frequency, since the machine shafts slow down, and this is detected by the speed governors. The governor constitutes the primary form of generation control, since it is a fast acting device which alters the steam or water flow in such a way as to change the power output of the prime mover to maintain near constant speed. A governor is characterised both by its dynamic performance and by its static gain which gives the familiar "droop" characteristic.

In order to change the pattern of generation, or to alter the system frequency, the governor set-point must be changed by actuating the speeder gear. The problem of maintaining frequency and of deciding on the loading levels of different sets is one which is usually solved at a central control centre in a power system, since there are many factors which must be taken into account before a decision can be made. The control problem is further complicated by the inter connection of many smaller systems into one large system using tie lines. This interconnection is performed so that in the event of a fault, mutual assistance can be given, thus lowering the total spinning reserve requirement. Economic advantages can also be obtained if there is a varied plant mix over the constituent sub-systems, such as one area being predominantly hydro, while another might consist of base-load thermal plant. The effects of random loading can be more easily compensated in a highly interconnected system. The whole interconnection concept is not without its difficulties, however, as it requires good frequency control over the whole system, together with control of tie line flows, in order to avoid possible tie line tripping and consequent system inlanding.

To a large extent the need for direct action to control network voltage levels

has been overcome by the installation of automatic voltage regulating equipment. The security aspects of generation and transmission, however, are at present the responsibility of grid control engineers, who rely on considerable operational experience together with off-line load flow studies. Overall system control is based on a combination of manual intervention, fast continuously acting feedback control of local loops for voltage regulation and speed governing together with a slower acting open-loop feed forward type of optimising control or generator scheduling based on predicted load demand. The optimising schedule for changes of bulk generation will usually include a co-ordination of generator costs and line losses subject to constraints on line and plant loading and security. The control responsibility is divided basically according to the frequency of intervention required and to the time scale of the physical phenomena involved. Area level decisions may also include system voltage control by transformer tap positions and excitation control with an optimum scheduling of reactive power flow. Distribution of reactive power will not affect significantly system operating costs, but an optimum allocation may be important for maintaining steady state system stability and voltage levels.

Although to a certain extent the control of power and frequency is interrelated to the control of reactive power and voltage, it is hoped that by dealing with power and frequency separately from voltage control, a better appreciation of the operation of power systems will be obtained.

The control of real power flows and system frequency in an interconnected system with a variety of generating stations available is the task of the control engineers, who allocate the required power among the generators before the load requirements reaches. Now should the total generation available be insufficient to meet the demand the frequency will fall. In this type of situation although the reduction of frequency will cause a reduction in power demand, voltage must be reduced and if this is not sufficient, loads will have to be disconnected and continue to be disconnected until the frequency rises to a reasonable level. The making of the right decisions by control engineers requires experience and this is where the importance of a simulator can be appreciated.

Power system simulators in general are a powerful aid for training engineers in the technique of power system control and economic-load dispatching. Simulators also offer scope for studying alternative operating procedures, analysis of actual system events and demonstration problems. Direct training on a live system has always been operationally limited, costly and educationally very slow. The simulator creates an invaluable link between the theoretical teachings of the class-room and the practical realities of controlling a major power network. Performance can be accurately monitored on the

simulator and precise comparisons made between differing approaches to repeatable load curves. Such comparisons are to a great extent impossible to make directly on a power network due to daily variations in plant availability and consumer load. The action of a control engineer in the event of extreme or unusual system conditions is critical. Often on these occasions even experienced engineers become indecisive, making serious errors purely due to the unfamiliarity of the situation. The simulator can be usefully employed to minimize such risks by covering these areas of operation at the initial training stage and to provide regular refresher courses. 3,4,5,10

In the past six years, a hybrid simulator has been developed for power system control investigations in the power system group of the Electrical Engineering Department at Imperial College. A complete power system dynamic simulator was built by successive postgraduate research students and an extended simulator was successfully used as a test-bed for the investigation of the problems arising in the implementation of real time on-line digital control of multimachine electric power systems. Investigations ranged over load and generating plant modelling including real time digital models for power plants. Load dispatch and automatic frequency control algorithms were implemented and online economic dispatch control programs were developed with security constraints.

The current rapid development in microprocessors makes it worthwhile to study their application in the power system simulator content. And it seems likely that microprocessors interconnected in parallel arrays could function successfully as flexible, powerful power system simulators.

1.2 Organization Of The Thesis

This thesis describes the work carried out by the author on the construction of the digital hardware and software of a simulator. Chapter 2 deals with the analogue simulation patched on an analogue computer at Imperial College, and discusses a model of items of plant being represented. Chapter 3 explains briefly the application of microprocessors for simulation, objectives and choice of a microprocessor. The actual hardware of the Motorola MEK 6800D2 kit and the system are described in chapters 4 and 5 respectively. Chapter 6 deals with the software organization written for this system. The penultimate chapter, chapter 7, describes investigation and studies of the simulator to demonstrate the potential of the whole system. Finally, the conclusions summarize the work which has been carried out and recommendations are made on further developments which might profitably be pursued.

Chapter 2

2.1 Analogue Simulation and System Modelling

To implement adequate control of a power system it is essential to have a clear understanding of the dynamic performance of each element of the system. For instance, the design of fault isolation equipment will necessitate knowledge of the transient behaviour of the network. The performance information can be represented by a set of equations relating voltages and currents to time, which together form a model of the system. If the model derived is accurate it is possible to investigate the operation of various isolation schemes by solution of the equations constituting the model. Results from these simulations can then be used to improve the design without the need for construction and implementation of trial equipment. The main difficulty with this approach is that the model must accurately reflect the performance of the system under all conditions.

The scale of a power system is such that it would be impossible to solve the resulting equations even if it were possible to derive all the necessary data. The time scale of the investigations does however provide a basis on which to introduce simplifying approximations. For example, the voltage variation at a node of the network during the operation of a circuit breaker is unlikely to affect decisions at the plant ordering level. Consequently, only those dynamics which are relevant to a particular time scale need be included in the model.⁴ Thus for load-frequency behaviour of the system in our application, it is unnecessary to consider very rapid transient effects included by, say, network switching since these will be negligible on the time scale of interest for load-frequency control. Furthermore, the problem of reactive power control can be decoupled from that of real power since a mismatch in the real power balance affects primarily the system frequency, but leaves the bus voltage magnitudes essentially unaffected, whereas a mismatch in reactive power affects mainly the bus voltages, with little effect on frequency. The load-frequency control problem can therefore be investigated by means of a simplified power system model which excludes the effects of high-speed transients and control of reactive power and bus voltages.

In an electric power system the many items of plant to be considered include: the prime mover and governing mechanism, the boiler plant, the synchronous machine, the voltage regulating system, and the transmission network, the system loads, etc. But for this particular simulation only a certain number of these items need to be included, the selection of which are dependent on their dominant time constants.

The generator response is very rapid and for our application can therefore be regarded as instantaneous on the load frequency control time scale. Items which would be considered in the model are : the inertia of the whole system comprising rotating parts of different sets, each set with a steam-turbine/governor model including its droop characteristic and associated lags and also the reheated steam-turbine model with its two different sections of high and low pressure stages.

2.2 Steam Turbine

For load/frequency control, the real power output from the sets must be continually adjusted to match the consumer load. Now for a synchronous machine the real power generated is determined by the prime mover torque, which is in turn controlled by the throttling through the main steam valve for a steam turbine, or the water gate for a hydro turbine. The main factors affecting the dynamic response of a steam turbine generator set are the lag due to entrained steam between the inlet valves and the first stage of the turbine, and the lag in changes of power output in the high and low-pressure sections of the turbine. The latter lag is primarily due to the storage action of the reheater. The input of the turbine model is a signal representing steam flow, while the governor produces a signal proportional to valve position, so it is assumed that :

$$\text{Steam flow (V)} = \text{Valve position (X)} * \text{Boiler pressure}$$

But here no boiler simulation is used, so the per-unit values should be the same.

Using a reheater there would be two sections; the high-pressure stage will develop about 25% of the steam power for electrical generation subject only to a small delay of about 0.4s, but at the low-pressure stage there will be another, longer delay, some times as long as 12s. Now if we represent the steam flow by "V" and electric power generated as "Pg" and the two lags by "Th" and "Tl" we will have ;

$$P_g = \left(\frac{1}{4}\right).V. \left\{1 - \exp(-t/T_h)\right\} + \left(\frac{3}{4}\right).V. \left\{\left(T_h/(T_h - T_l)\right) \left[1 - \exp(-t/T_h)\right] - \left(T_l/(T_h - T_l)\right) \left[1 - \exp(-t/T_l)\right]\right\}$$

which can be represented in block diagram form after Laplace transformation as shown in Figure 2.1.

2.3 Steam-Turbine Governor Model

The need to accommodate variable load demand has a profound effect on the design and control of the majority of power station plants. If, by way of illustration, the mechanism by which a consumer load change is imposed on a coal-fired power station is considered then the complexity of the control task should become apparent. Figure 2.2 shows

the main elements of plant in a power station together with the supply system. If the consumer increases the mechanical loading on an induction motor then to supply the increased torque its speed will drop slightly to give an increased rotor current. More current is then drawn from the supply by the stator winding which is derived via the substations and transmission system from the power station generator. The increased current flow in the generator stator is rapidly transferred to a braking effect on the rotor thereby reducing its speed slightly. The governor responds to this speed reduction and allows more steam from the boiler to enter the turbine therefore increases its speed. The sequence does not, however, end there since the increased steam flow will gradually reduce the boiler pressure. Manual or automatic control is then required to increase the fuel, air and water flow in correct proportions in order to increase the heat transferred to the boiler and this restores the steam pressure. Consequently for large sustained electrical load changes compensating changes will be necessitated in a wide range of plant within each power station. There is fortunately a difference in the speed of response which is necessary from the various plant. The large thermal inertia of most boiler systems enables the load frequency performance of the turbine, generator and load to be decoupled from that of the boiler to result in the approximation that for short duration load changes the boiler pressure may be regarded as constant. It is consequently the governor system which principally determines the short term response of the set to load fluctuations.

Many forms of governor system have been devised but all include in some way the variation of the turbine generator shaft speed as the basis on which to alter the current position of the turbine working fluid control valve. In small steam turbine sets the governor may be a direct mechanical drive on to the steam inlet valve but in most cases the primary governing element, typically a Watt centrifugal governor, does not generate sufficient force to move the steam valve directly. Power amplification is therefore needed and often takes the form of an hydraulic servo-system as shown in Figure 2.3. As the turbine shaft speed varies, the centrifugal force on the weights causes their radial position to vary. This movement is transmitted via a lever mechanism to the hydraulic amplifier pilot valve which in turn controls the main ram servomotor. Hence for a given shaft speed the main ram will be displaced by a set distance from a nominal position subject to the limitations of dead space. The opening of a steam valve can consequently be made to depend proportionally on the turbine speed variation from a set point.

Provision is also made for alteration of this set point by way of a speeder motor actuator on the Watt governor. Typical speed droop characteristics for this type of governor are between 4 and 10 per-cent.

Although straight throttling governing may be satisfactory for small turbines, large losses are introduced for high-steam flows. More efficient multinozzle inlet control arrangements, in which the governor opens and closes several steam admission valves in sequence, are normally used for such conditions. However, a degree of throttling is still present and the governor mechanism has been further complicated. More recent turbine governor designs are electronic in an attempt to provide greater flexibility in the form of the controller. 2,11,12,13

A block diagram of the governor representation is shown in Figure 2.4. By ignoring the velocity limits, it is possible to eliminate the droop feedback, and to produce an open loop system. A speed error signal is produced, and multiplied by $1/R$, where R is the droop, and it is then limited, to represent the limits of the flyball sleeve movement. This is then added to the speeder gear setting, P_{ref} , and a low pass filter is included to represent the dynamics of the valves.

2.4 System Inertia Representation

The equations of motion of a rotating synchronous machine can be derived by consideration of forces acting on the machine rotor, that is if

$$T = \text{Mechanical torque} - \text{Electrical torque}$$

then the acceleration of rotor is

$$\frac{dw}{dt} = \frac{T}{I} \quad (I = \text{Moment of Inertia})$$

or;

$$\frac{dw}{dt} = \frac{T}{I} = \frac{\Delta T \cdot w}{I \cdot w} = \frac{\Delta P}{H} \quad (H = \text{Inertia time constant})$$

now, as $f = w$

then upon Laplace transformation we will have ;

$$\frac{f(\text{changes in Frequency or Speed})}{p(\text{changes in Power due to } T)} = \frac{1}{S \cdot H}$$

So the boiler model is ignored and it is only the governor system which principally determines the short term response of the set to load fluctuations.

In the following system model two sets of 500 MW and 120 MW were chosen, typical values were ;

SETS	DROOP	GOVERNOR LAG	HIGH PRESSURE	LOW PRESSURE
500 MW	6%	0.4 s	0.8 s	12 s
120 MW	12%	0.4 s	0.4 s	0.4 s

Inertia constant of the system was taken as 4 s.

Such a system was patched up on an analogue computer (Figure 2.5) at Imperial College and the results were examined. Figure 2.6 presents a comparison between different conditions, where response "B" shows system behaviour at 4% droop, 150MW load with a 500 MW set. The adjacent response "D" is the same system but with 8% droop characteristic, as a result with twice as much difference in settling frequency. Effects of governor gear setting presented by the response "A" which in this case for the same system with 4% droop the difference in steady state frequency has been recovered. Also to show the load effect on the system response a test was carried out with an 8% droop characteristic but only half as much load was applied and as expected the "C" response was achieved. Comparing curves "A" and "B" with curves "C" and "D" it is clear that the settling time increases as the droop of the system increases.

Finally Figure 2.6 clarifies the difference in the responses made by the two different sets used here, showing that the settling time for the 120MW set is shorter. 1,7,8,9,20,21 .

2.5 C.E.G.B. Mini Analogue Power System Simulator at East Grinstead Control Center

In the early stages of this research, with the help of Dr. Short, the author had the chance of attending a short course at C.E.G.B., getting familiar with the operation of a small power system loading simulator (Load and frequency variations only), see appendix A.

The author's experience started with spending time in manipulating the plant noting the system characteristics, individual generator responses, and the interrelating effects of the variables. A load curve was recorded on a magnetic tape, and I was also provided with a similar load curve as a load estimate. From this a generation loading schedule was prepared to meet the expected load with maximum economy. Minor changes were made to account for the deliberate errors introduced in the estimate to give the operator the ability to maintain a steady frequency. An overall summary of the performance was backed up by hard copy of system frequency and cost recorded on the plotter. Later the generators were tripped off and several of these simulators, representing a number of stations, were inter-linked.

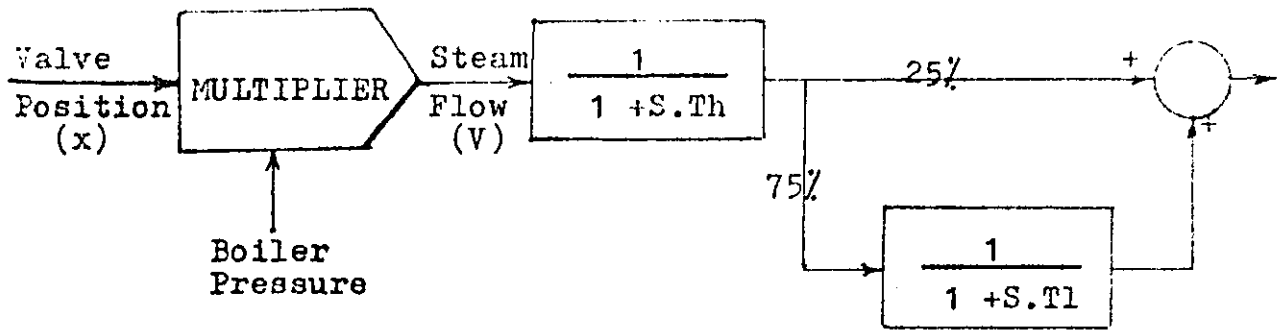


Figure: 2.1

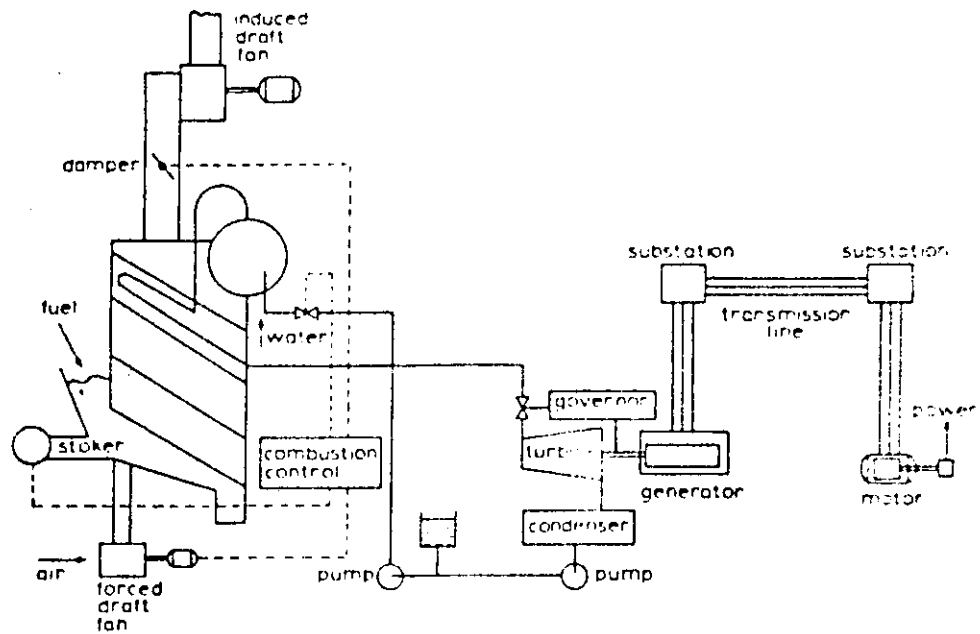


Figure: 2.2

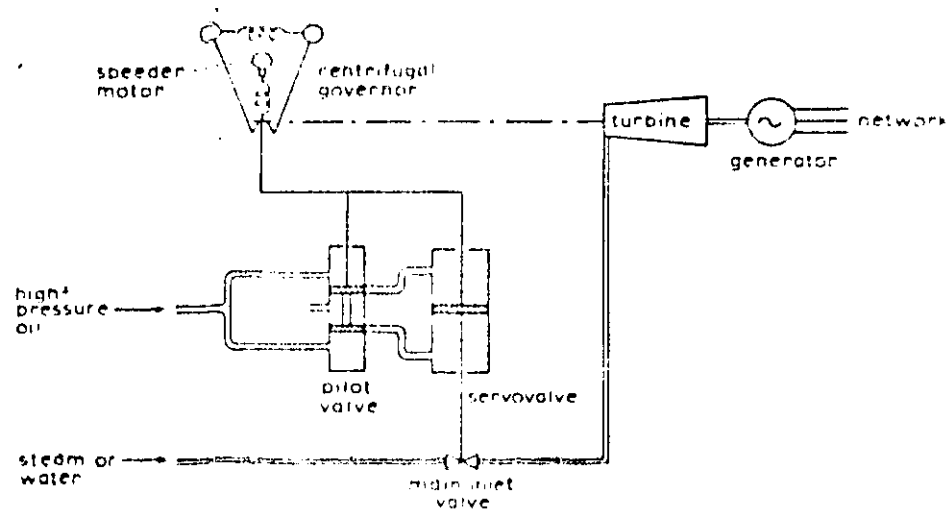


Figure: 2.3

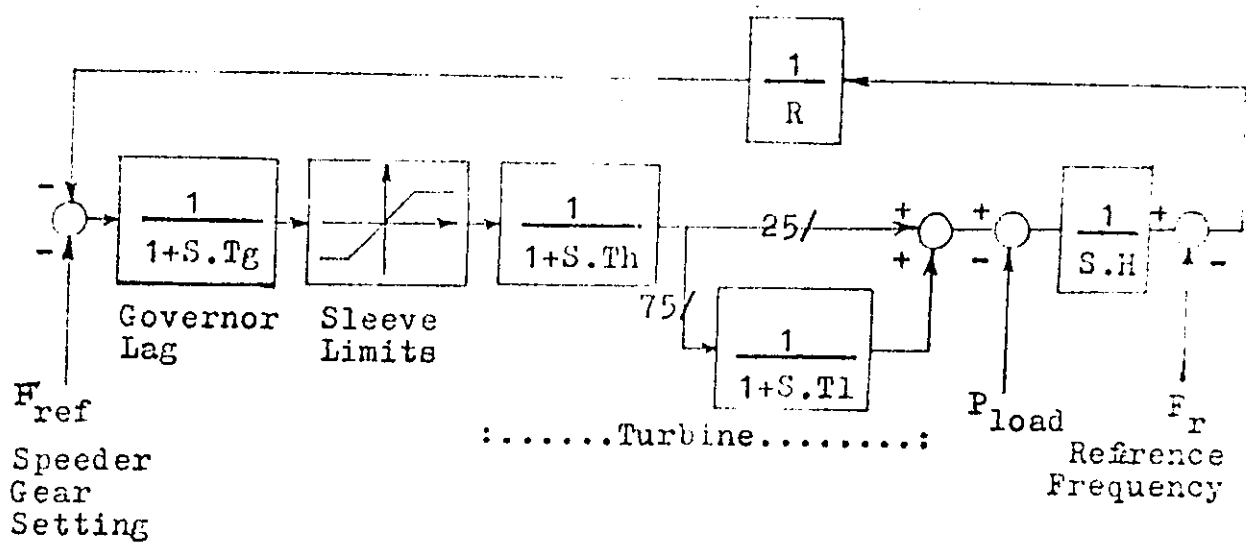


Figure: 2.4 System Block Diagram

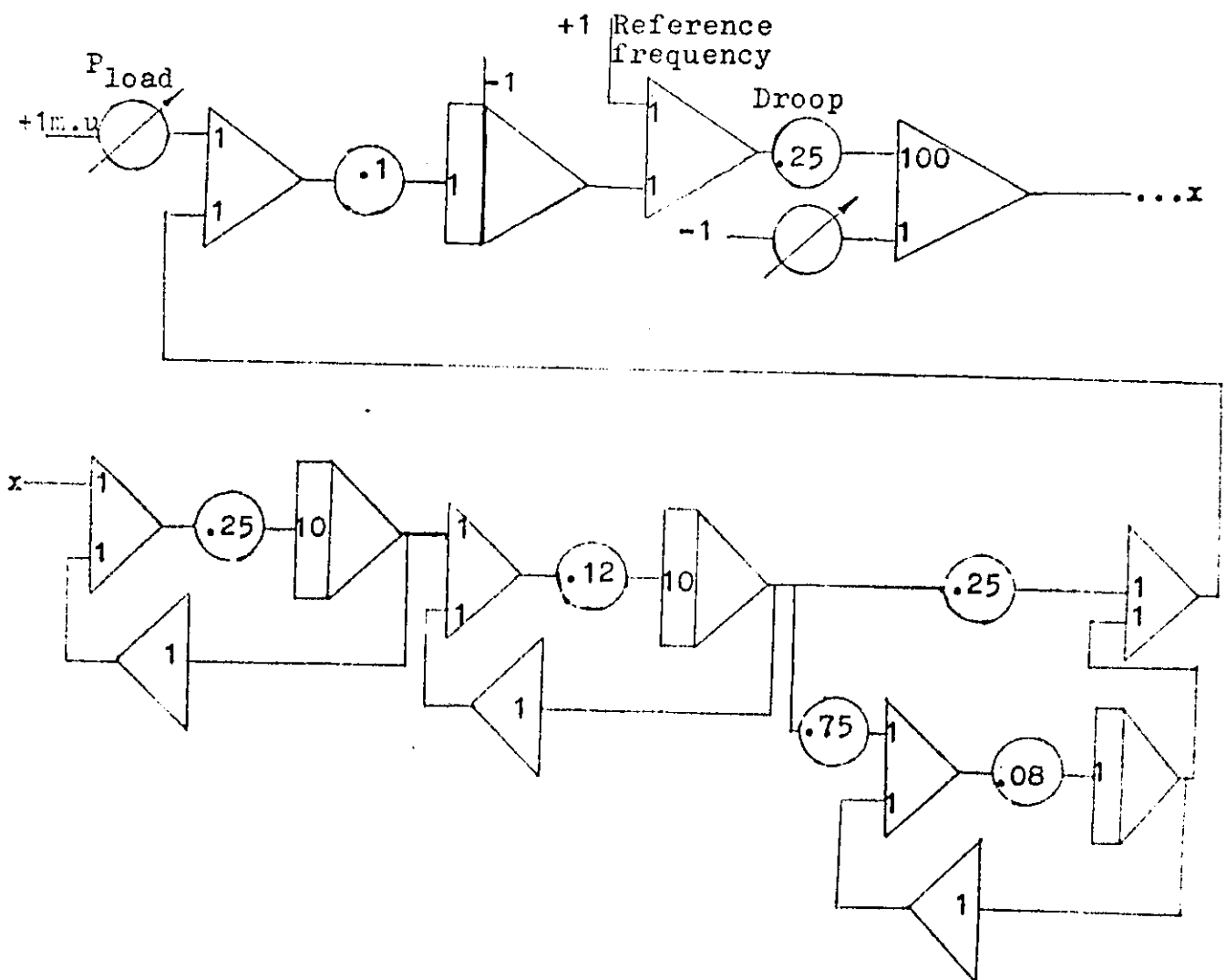
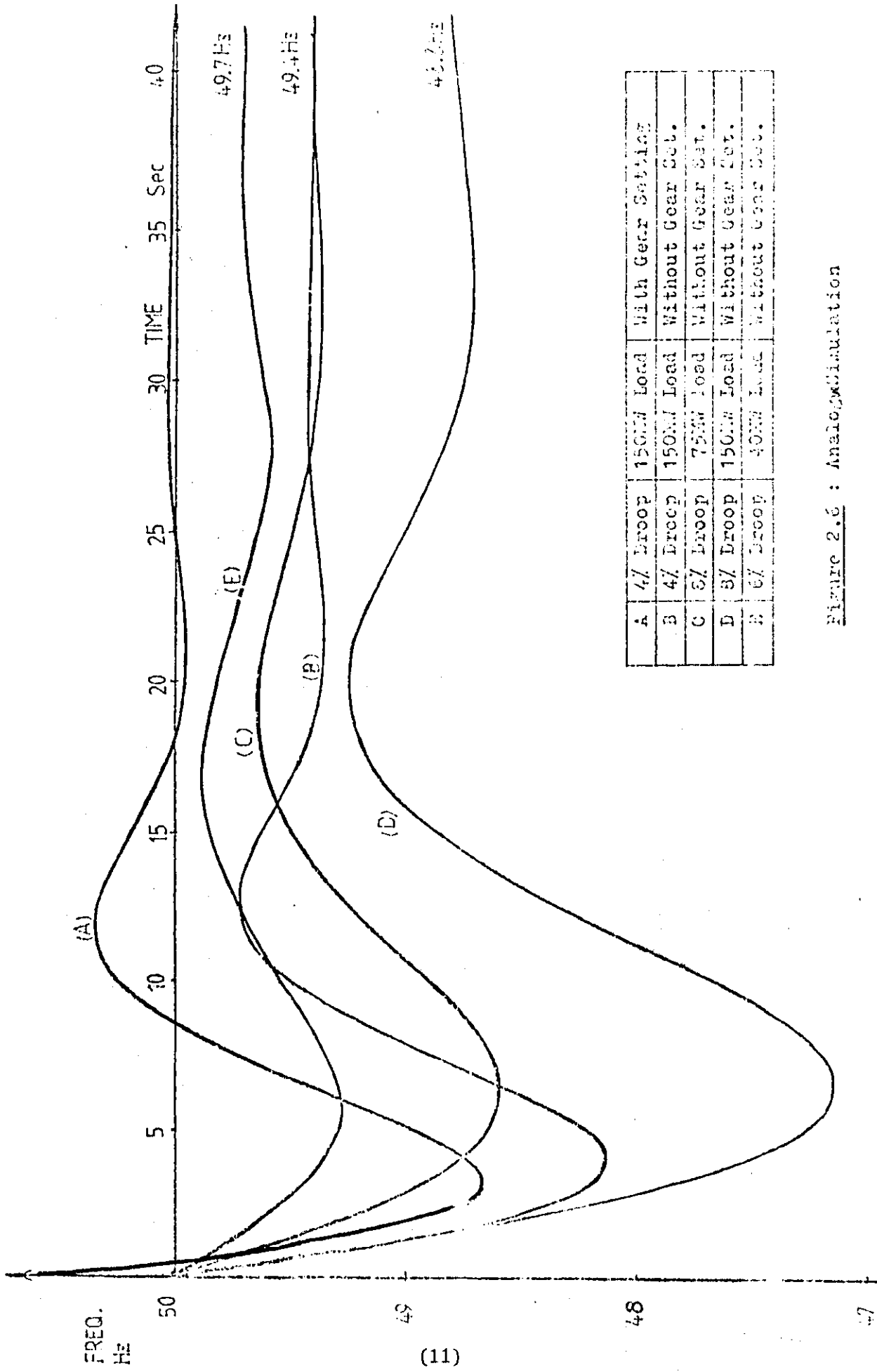
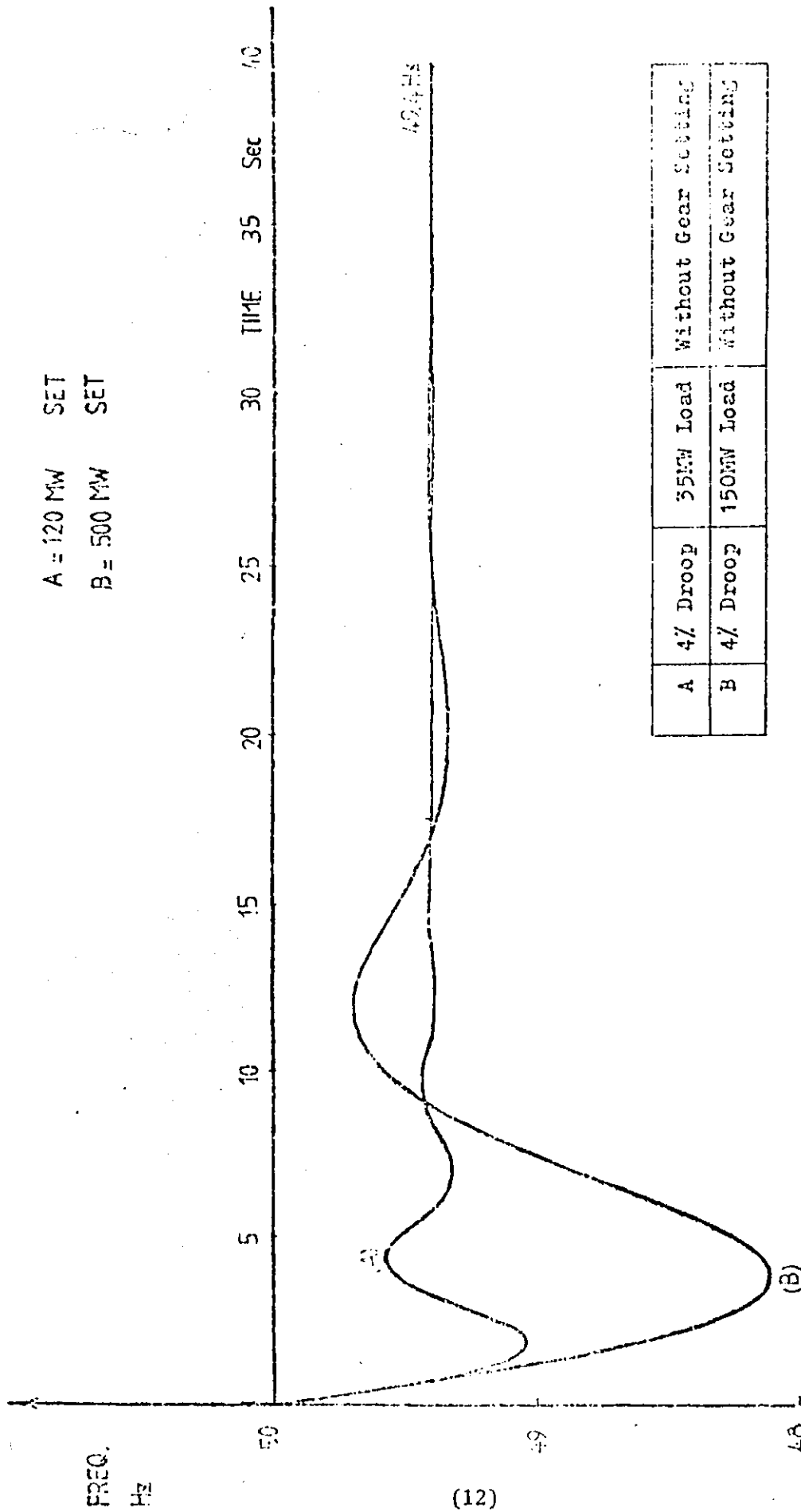


Figure: 2.5 Analogue Simulation Set Up



A	4% Droop	150MW Load	With Gear Setting
B	4% Droop	150MW Load	Without Gear Set.
C	6% Droop	75MW Load	Without Gear Set.
D	6% Droop	150MW Load	Without Gear Set.
E	6% Droop	40MW Load	Without Gear Set.

Figure 2.6 : Analog Simulation



A	4% Droop	35MW Load	Without Gear Setting
B	4% Droop	150MW Load	Without Gear Setting

Figure 2.7 : Analog Simulation

3.1 Objective

Rapid advances in large scale integrated circuit technology in recent years have made it possible to apply digital computing capability where formerly analogue techniques were used. Perhaps the most significant single consequence of LSI research has been the development and production of the microprocessor : a single chip monolithic integrated circuit device that contains some of the basic building blocks of a computer : arithmetic logic unit, control, and bus provisions for the addition of memory and input/output capability. The microprocessor and its essential ancillary devices make up a minimum hardware system which can be programmed and run like a computer. The performance of the designed system depends upon the size and character of the microprocessor instruction set, its speed of operation, the number of binary bits in the address and data buses, the size of memory provided, the nature of the input/output devices and other factors.

For most microprocessor families, the minimum system consists of an MPU (Microprocessing unit), a clock (typical frequency in MHz), a read/write or random access memory (RAM), a read only memory (ROM) and an input/output device commonly called a peripheral interface adapter (PIA).

The capability offered by a microprocessor based computing system (microcomputer) is in suitable control application such as the Dynamic Modelling of Power Systems. The proposal to develop a microcomputer for a power system simulator is based on a desire to take advantage of this previously unavailable technology to apply new techniques to old problems. Traditionally power system simulators have been designed by analogue circuits. However many of the routines used for simulation involve the comparison of several input variables; which are easily executed on a digital machine. In the past, low portability of versatile digital equipment (beside the high level of cost) prevented the application of digital control in power system simulators, but microprocessor digital circuits provide light, compact and mechanically simple computing capability.

For simulator control routines a microcomputer is an excellent tool; it is more versatile than other types of equipment since its mode of operation can be varied by program changes only. Obviously a power system simulator must have several general purpose analogue inputs and analogue output channels.

The impetus for the application of microprocessors to power system simulation is, finally, an interest in developing an inexpensive, versatile, highly reliable and

easy-to-use unit to train power system control engineers at control centres.

3.2 Comparison of Microprocessor Based and Analogue Based Simulators

The flexibility and speed of a microprocessor-based system allows the evaluation of more sophisticated control routines than would be possible with an analogue system of equal cost. In an analogue based system we are committed to a certain technique for solution. Since rectifier firing angle controllers or load switching controllers must be purpose built, any attempt to compare different control policies will be complex and time consuming. Once the basic microcomputer software is written (for restart, interrupt, etc) the control function chosen is dependent on the ability of the programmer and the number of available inputs and outputs to and from the microcomputer.

The cost of a microcomputer based simulator is expected to be less than that of an analogue system with equal capability assuming a moderate level of control policy sophistication.

3.3 Objectives

As the author joined the power system section a case was put forward to Science Research Council Grants for the support of a major project on the application of microprocessors in power system simulation. In this proposal a suitably interconnected set of microprocessors would be performing tasks that currently require large uniprocessors capable of executing millions of instructions per second. This modular approach (Figure 3.1) will ease incremental expandability, and maintenance. On the whole three objectives were seen:

Stage One : To examine and determine the capability of a single microprocessor and associated memory to simulate in real time a single generating plant or load.

Stage Two : To determine the simulator architecture and software structure appropriate to the parallel interconnection of microprocessors for power system studies, including the interaction between generators and loads through the transmission network.

Stage Three : To design, construct and evaluate a flexible expandable multimachine power system simulator.

As will subsequently be shown in this thesis, the author's objectives have been concentrated on the first stage.

3.4 Choice of Microprocessor

Clearly the major multiprocessor simulation had to be carried out by a microcomputer

system of at least 16 bits data handling capability (for faster and greater accuracy of arithmetic operations) but, as the approval of Science Research Council on an expensive project like this normally takes a long time, it was decided in June 1979 to purchase an inexpensive 8 bit machine and commence the modelling of generators and associated governor and turbine simulation. The author had already undertaken his MSc project using a Motorola 6800 microprocessors kit (an 8 bit machine). This involved becoming familiar with the arrangement of a Motorola MEKD2 microprocessors development kit, based on the MC6800, so this machine was chosen for the job.

Other contributing factors were :

- 1) Imperial College Computing Centre has various supportive services for microprocessors users, including a MC6800 Cross Assembler, which facilitates the writing of long instruction set programs.
- 2) There are numerous experienced people working on the MC6800 family with whom to co-operate.
- 3) As will be discussed later, the arrangements of the peripheral interface adaptors as memory locations promised to be a more convenient I/O provision than in some of the competing families.
- 4) Different Components could be readily supplied by local vendors.

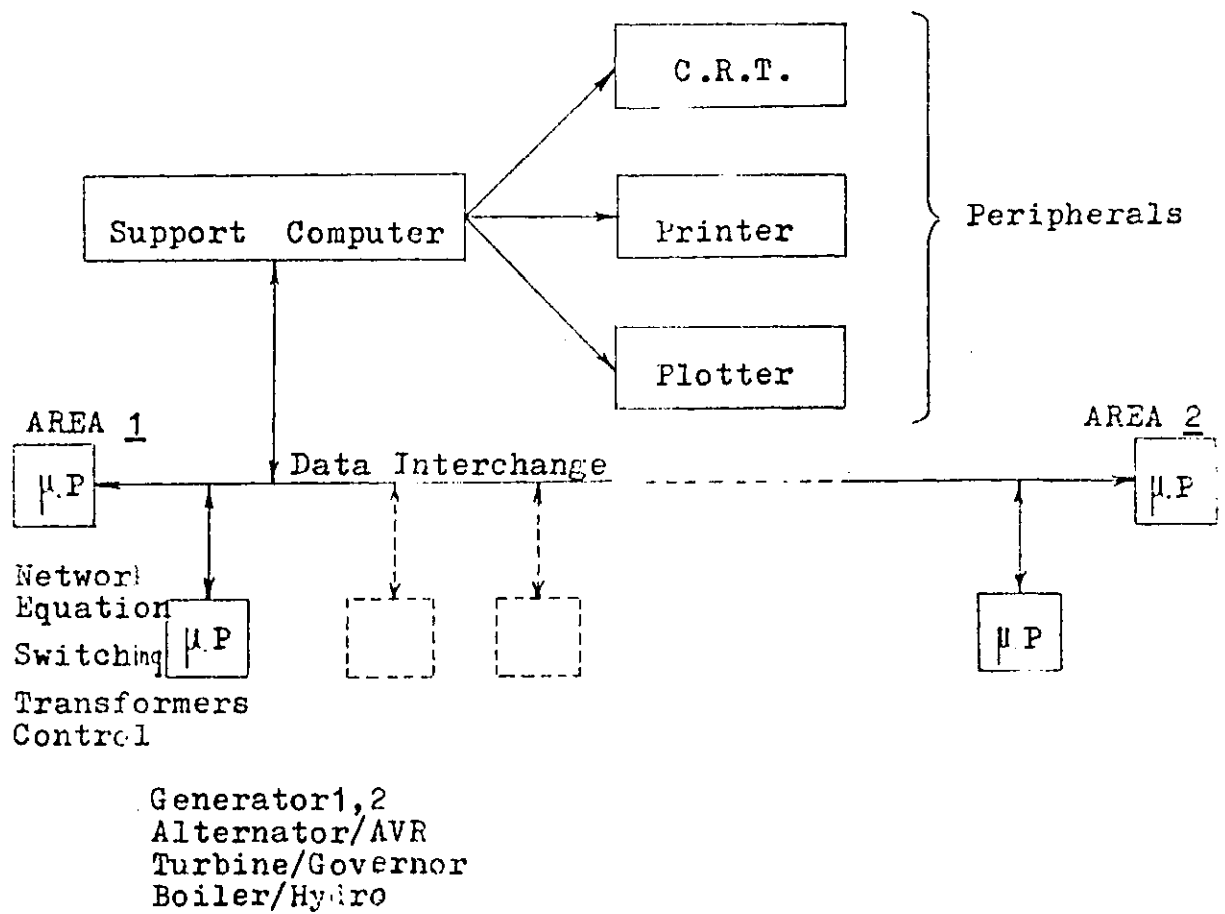


Figure: 3.1

CHAPTER 4

4.1 Motorola MEK 6800D2 Evaluation Kit II

This chapter provides a general description of the Motorola evaluation Kit, the operating instructions and of some system expansion techniques to meet the needs of this project.

The Motorola MEK 6800 D2 Kit microcomputer system (hereafter referred to as MEK/D2), when assembled, is a fully functional microcomputer system based on the MC 6800 Micro-processing unit (MPU) and its family of associated memory and I/O devices. It features a hexadecimal keyboard for data and command entry the MEK/D2 provides an audio cassette I/O data transfer capability. Figure 4.1 presents a functional block diagram of the basic system.

The integral Keyboard/Display Module can be used in conjunction with the JBUG monitor program for entering and debugging user programs.

This kit consists of two separate boards :

- (i) The Keyboard, Display and Audio Cassette module.
- (ii) Memory and Microcomputer module.

The Memory and Microcomputer module includes the following devices :

<u>Quantity</u>	<u>Device</u>
1	MC 6800 MPU
1	ROM with JBUG Monitor
3	RAM (128*8)
2	Peripheral Interface Adapter (PIA)
1	Asynchronous Communication Interface Adapter (ACIA)
1	Clock Generator

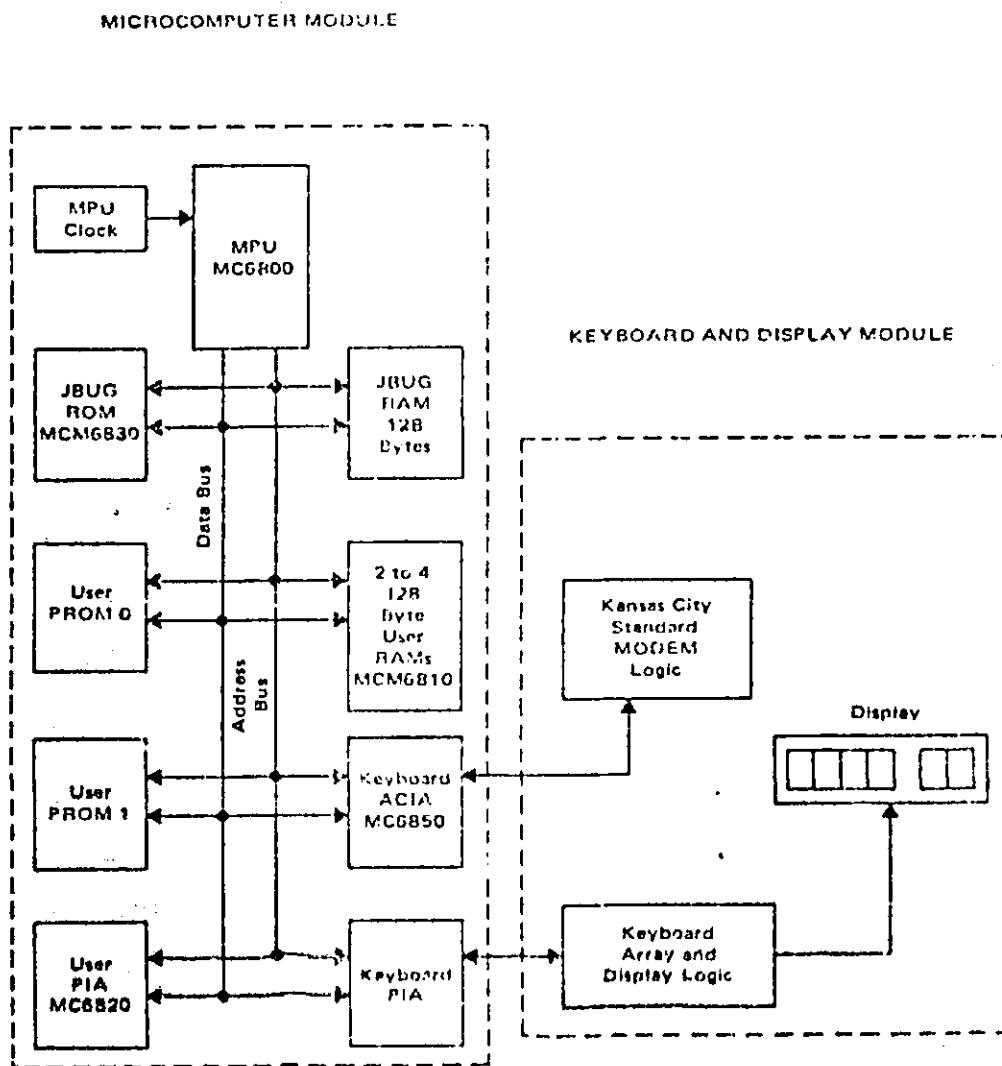


Figure: 4.1 Block Diagram of Basic System

The design of the I/O system is a complex task, and the design of the I/O system is a complex task, and the design of the I/O system is a complex task.

4.1. Input/Output (I/O)

4.1.1. Introduction

Due to the nature of applications in which they are used, the requirements for efficiently handling input/output information is perhaps the most important consideration in microprocessor systems. The M1000 includes a comprehensive set of input/output and interface devices that permits a wide variety of I/O techniques to be used.

Most I/O information can be placed in one of two general categories: control and status signals, and data that is to be processed by the CPU. Each of these categories has its own set of control and status information that is used to manage the I/O system.

(1) Many of the most common general control tasks can be handled by the I/O system.

(2) Because the design of the interface permits all of the I/O signals to pass exactly like other data, location of the memory is not a problem. The I/O system can operate directly on memory and also use the memory as a buffer.

(3) The MPU is able to control simple peripherals and manage control signals. In fact, there is an option to use interrupts with the I/O system. Other features are in progress but a disadvantage is that the I/O system is not programmable.

4.3 Program Controlled Data Transfers

4.3.1 Peripheral Interface Adapter (PIA)

The Peripheral Interface Adapter (PIA) provides a simple method of connecting byte-oriented peripherals to the MPU. The PIA, which is a separate chip, permits the MPU to handle a wide variety of equipment with minimal peripheral logic and simple programming. An Input/Output register in the PIA is used to control the I/O.

Data flows between the MPU and the PIA through a set of eight bidirectional data lines, D0 through D7. The direction of data flow is controlled by the MPU via the Read/Write input to the PIA.

The MPU uses the PIA to control the I/O system. The PIA is a separate chip, and the MPU uses the PIA to control the I/O system.

selecting a particular PIA. Two addressing inputs, RS0, and RS1, are used in conjunction with a control bit within the PIA for selecting specific registers in the PIA. The MPU can read or write into the PIA's internal registers by addressing the PIA via the system Address Bus using these five input lines and the R/W signal. From the MPU's point of view, each PIA is simply four memory locations that are treated in the same manner as any other read/write memory.

The MPU also provides a timing signal to the PIA via the Enable input. The Enable(E) pulse is used to condition the PIA's internal interrupt control circuitry and for the timing of peripheral control signals. Since all data transfers take place during the 02 portion of the clock cycle, the Enable pulse is normally 02.

The "Peripheral side" of the PIA includes two eight-bit bi-directional data buses (PA0-PA7 and PB0-PB7), and four interrupt/control lines, CA1, CA2, CB1, and CB2. All of the lines on the "peripheral Side" of the PIA are compatible with standard TTL logic. In addition, all lines serving as outputs on the "B" side of each PIA (PB0-PB7, CB1, CB2) will supply up to one milliamp of drive current at 1.5 volts.

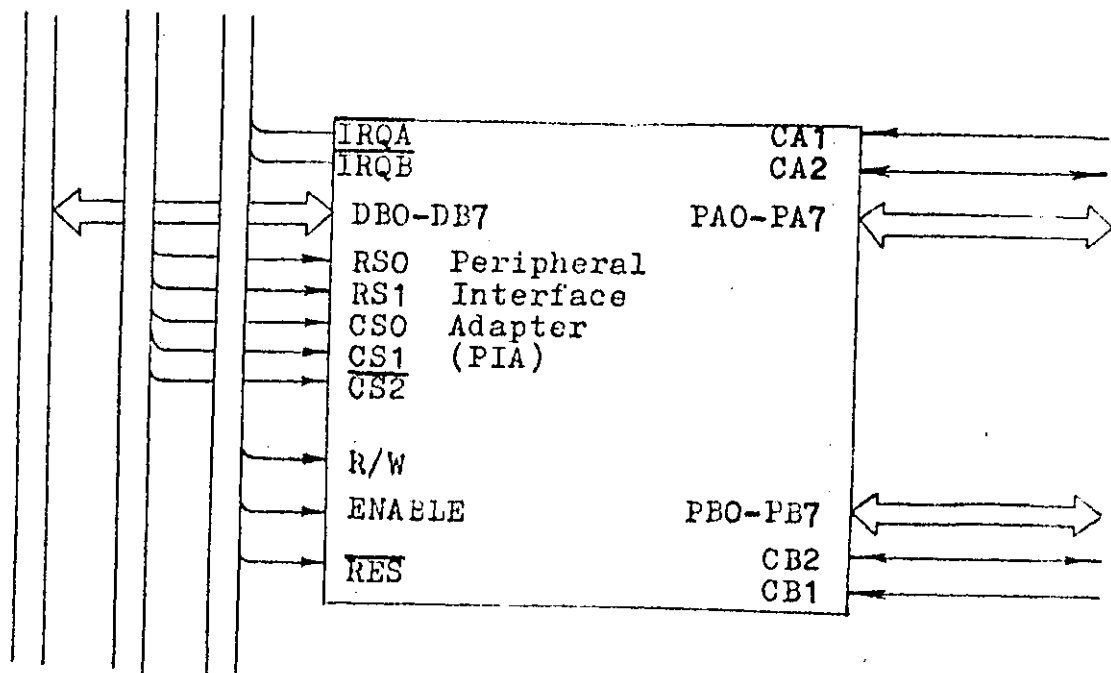


Figure: 4.2 PIA I/O diagram

4.3.2 Internal Organization

An expanded Block Diagram of the PIA is shown in Figure 4.3. Internally, the PIA is

divided into two symmetrical independent register configurations. Each half has three main features : an Output Register, a Control Register and a Data Direction Register. It is these registers that the MPU treats as memory locations, i.e. they can be either read from or written into. The Output and Data Direction Registers on each side represent a single memory location to the MPU. Selection between them is internal to the PIA and is determined by a bit in their Control Register.

The Data Direction Register (DDR) are used to establish each individual peripheral

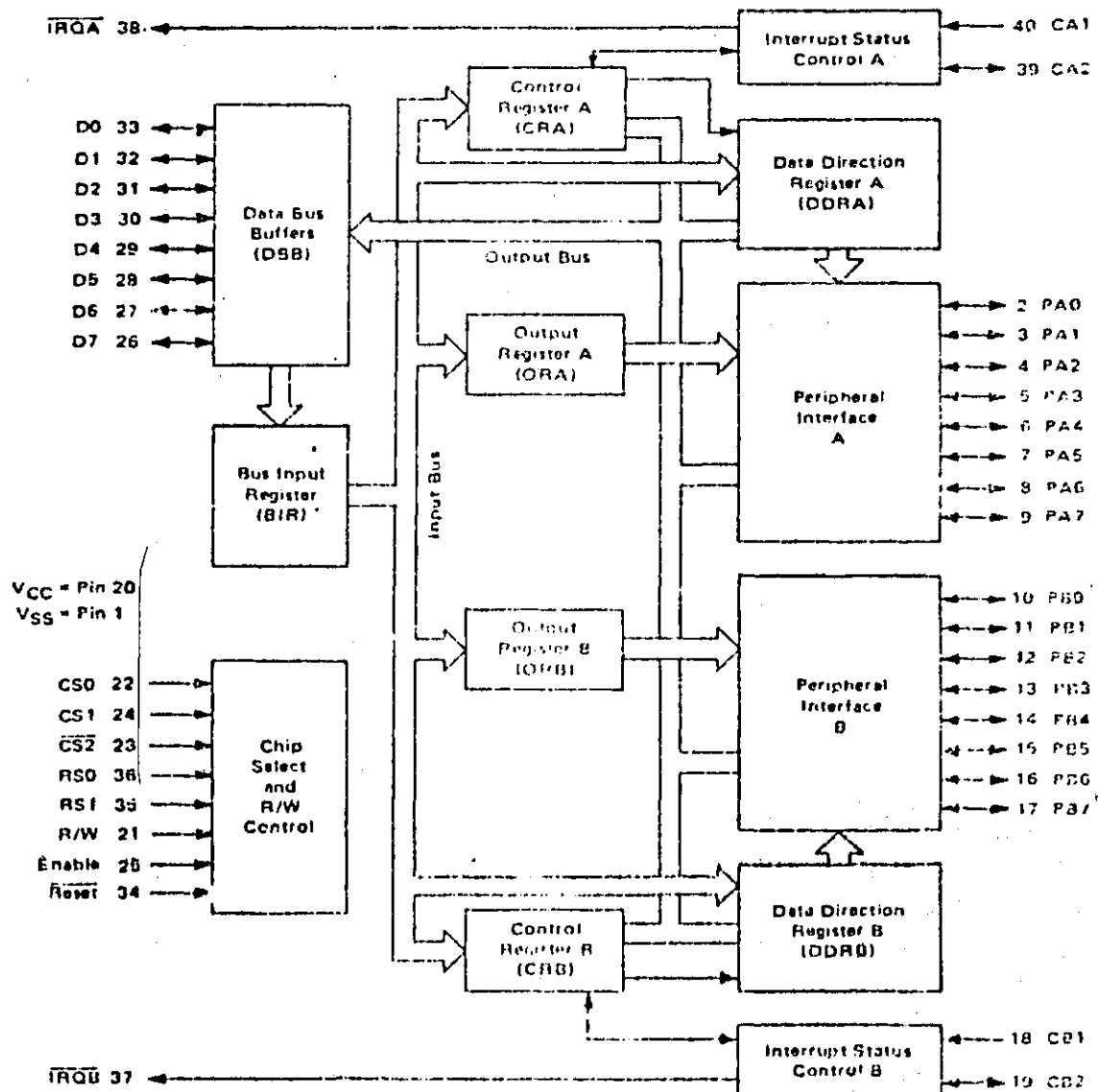


Figure 4.3 : PIA Block Diagram

bus line as either an input or an output. This is accomplished by having the MPU write "ones" or "zeros" into the eight bit positions of the DDR. Zeros or ones cause the cor-

responding peripheral data lines to function as inputs or outputs, respectively.

The Output Register, ORA and ORB, when addressed, store the data present on the MPU Data Bus during an MPU write operation. As used here, an "MPU Write" operation refers to the execution of the "Store" instruction, i.e., writing into Output Register A is equivalent to execution of STA(A) PIA OR(A) by the MPU. Similarly, an "MPU Read" operation is equivalent to execution of the "Load" instruction : LDA (A) PIA OR(A). This data will also appear on those peripheral lines that have been programmed as input, the corresponding bit position of the Output Register can still be written into by the external signal applied on that peripheral data line.

During an MPU Read operation, the data present on peripheral lines programmed as inputs is transferred directly to the system Data Bus. Due to differing circuitry, the results of reading positions programmed as outputs differ slightly between sides A and B of the PIA. On the B side, there is three state buffering between Output Register B and the peripheral lines such that the MPU will read the current contents of ORB for those bit positions programmed as outputs. During an MPU Read of the A side, the data present on the Peripheral lines will effect the MPU Data Bus regardless of whether the lines are programmed as outputs or inputs, for this reason A side was taken as inputs. The bit positions in ORA designated as outputs will be read correctly only if the external loading on the Peripheral lines is within the specification for one TTL load. That is, a logic one level could be read as a logic zero if excessive loading reduced the voltage below 2.0 volts.

The two Control Registers, CRA and CRB, allow the MPU to establish and control the operating modes of the peripheral control lines, CA1, CA2, and CB2. It is by means of these four lines that control information is passed back and forth between the MPU and peripheral devices. The control word format and a summary of its features is shown in Figure 4.4.

The Data Directions Register access bit (b2 =DDR Access) is used in conjunction with the register select lines to select between internal registers. For a given register select combination, the status of the DDR bit determines whether the Data Directions Register (b2 of DDR=0) or the Output Register (b2 of DDR=1) is addressed by the MPU.

Each Control Register has two interrupt request flags, b7=IRQA (B) and b6=IRQA(B0); they are set by transitions on the CA1(CB1) and CA2(CB2) control lines and can be read by an MPU read Control Register Operation. The status of the interrupt flags can not be altered by an MPU write instruction, that is, IRQA(B)1 and IRQA(B)2 are Read only with respect to the MPU. They are indirectly reset to zero each time the MPU reads the

corresponding Output Register or can be cleared with hardware Reset.

In our applications by $b_0=0$, we disable IRQA (B) MPU Interrupt by any active transitions on CA1(CB1), so we wouldn't need to consider b_1 .

When $b_5=0$, b_3 and b_4 of the Control Register perform similarly to b_0 and b_1 , controlling the IRQA (B)2 interrupt via the CA2(CB2) input. The IRQA(B) interrupt terminal, when enabled, responds to either IRQA(B)1 or IRQA(B)2.

If $b_5=1$, CA2(CB2) acts as an output and will function in one of three modes. If b_4 is also equal to one, CA2(CB2) serves as a program controlled set/reset output to the peripheral and follows b_3 as it is changed by MPU Write Control Register operations. If $b_4=0$ when $b_5=1$, CA2(CB2) can be used in either a pulse strobed or handshake mode (used in our applications). Operation of the two sections differ slightly for these two low by the negative transition of the MPU Enable Pulse following an MPU Read Output Register operation and returns high when IRQA1 is next set by CA1. This, in effect, tells the peripheral it has been read and allows it to acknowledge via CA1. The "B" Side operation is similar except that CB2 is taken low following an MPU Write Output Register operation and returned high by the next CB1 transition; this tells the peripheral it has been written into and allows it to respond via CB1.

In the pulse-strobed mode which will be used here, i.e. $b_3=1$, CA2 is again set low by a Read Output Register command, but is now returned high by the negative transition of the next MPU originated Enable Pulse. CB2 operation is similar except that an MPU Write Operation initiates the pulse.

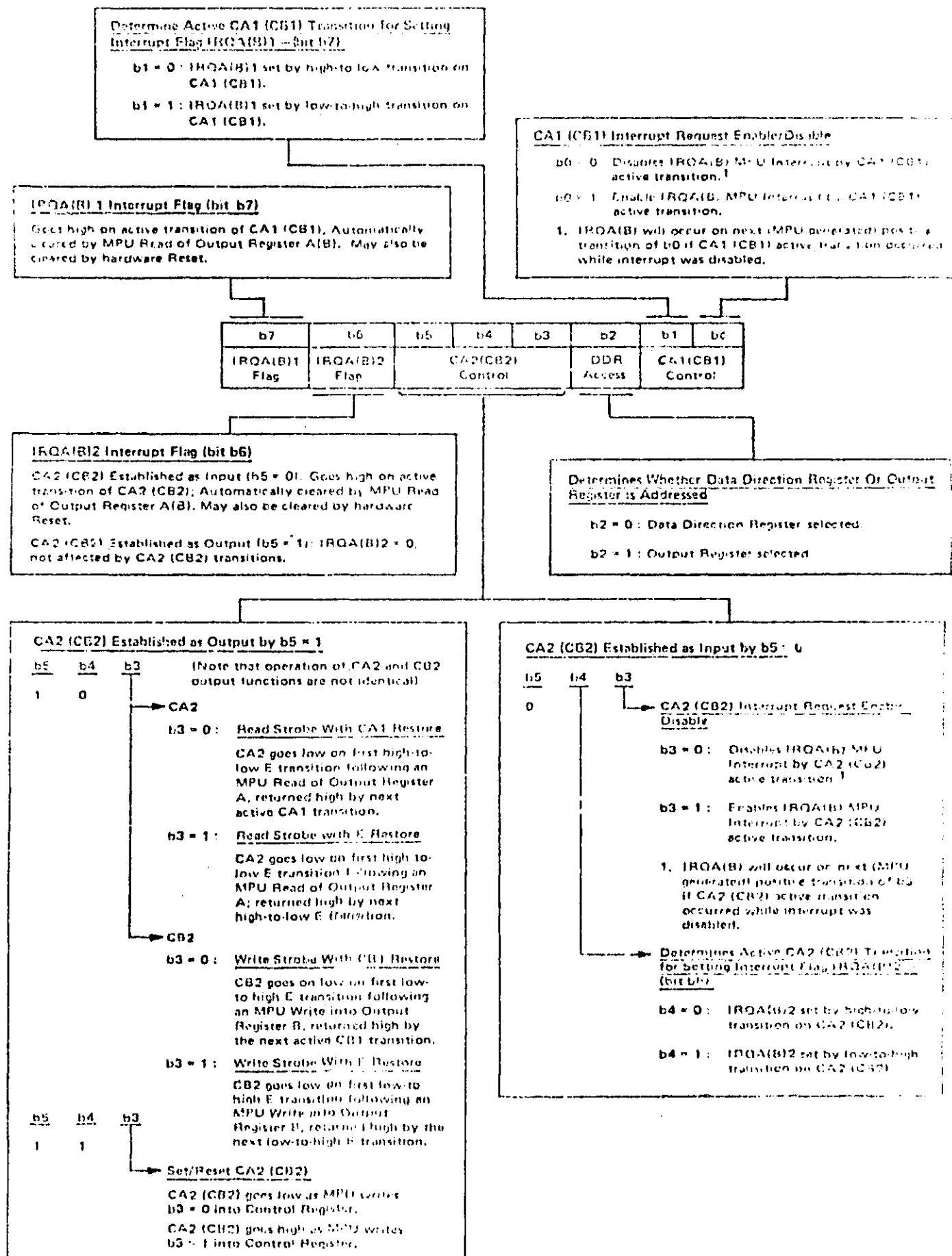


Figure 4.4: PIA Control Register Format

4.5.3 Addressing PIA

As indicated in section 4.3.1, the MPU addresses the PIA via the five chip select and register select inputs and bit 2 of the Control Registers. The correspond between internal registers and the address inputs is shown in Figure 4.5.

CS2	CS1	CS0	RS1	RS2	b2	
0	1	1	0	0	0	Data Direction Register A
0	1	1	0	0	1	Output Register A
0	1	1	0	1	X	Control Register A
0	1	1	1	0	0	Data Direction Register B
0	1	1	1	0	1	Output Register B
0	1	1	1	1	X	Control Register B
X	X	0	X	X	X	PIA Not Selected
X	0	X	X	X	X	PIA Not Selected
1	X	X	X	X	X	PIA Not Selected

X = Doesn't Matter

Figure 4.5 : PIA Register Addressing

Addressing a PIA can be illustrated in conjunction with the system configuration shown in Figure 4.6. The method shown is typical for assigning mutually exclusive memory addresses to the family device without using additional address decode logic. The connections shown in Figure 4.6 assign memory addresses as follows :

RAM	0000-007F
PIA	4004-4007
ACIA	4008-4009
ROM	C000-C3FF (HEXA-DECIMAL NOTATION)

But the address assignment in MEK/D2 kit is slightly different to above, in this kit an address decoder is used with inputs A13, A14, A15, VMA and outputs of $\overline{\text{PROM1}}$, $\overline{4/5}$, $\overline{2/3}$, $\overline{\text{RAM}}$, $\overline{\text{ROM}}$, $\overline{\text{PROM0}}$, $\overline{\text{STACK}}$, $\overline{\text{I/O}}$ which produce different mappings of;

RAM	0000 - 01FF
PIA	8004 - 8007 User's PIA supplied in kit
ACIA	8008 - 8009
ROM	E000 - E3FF

in this particular PIA, $\overline{I/O}$ logic is connected to $\overline{CS2}$ pin making PIA's location in the region of $(8000)_{16}$ and by applying logic 1 to $CS0$ and connecting $A2$ to $CS1$, $A1$ to $RS1$, $A0$ to $RS0$. Here it was essential to add an extra PIA (see later) which could have been placed in any empty space in the memory map. Addresses 8010-8013 were chosen, making the wire wrapping similar to the above connections with only one alteration and that is, connecting $A4$ to $CS1$.

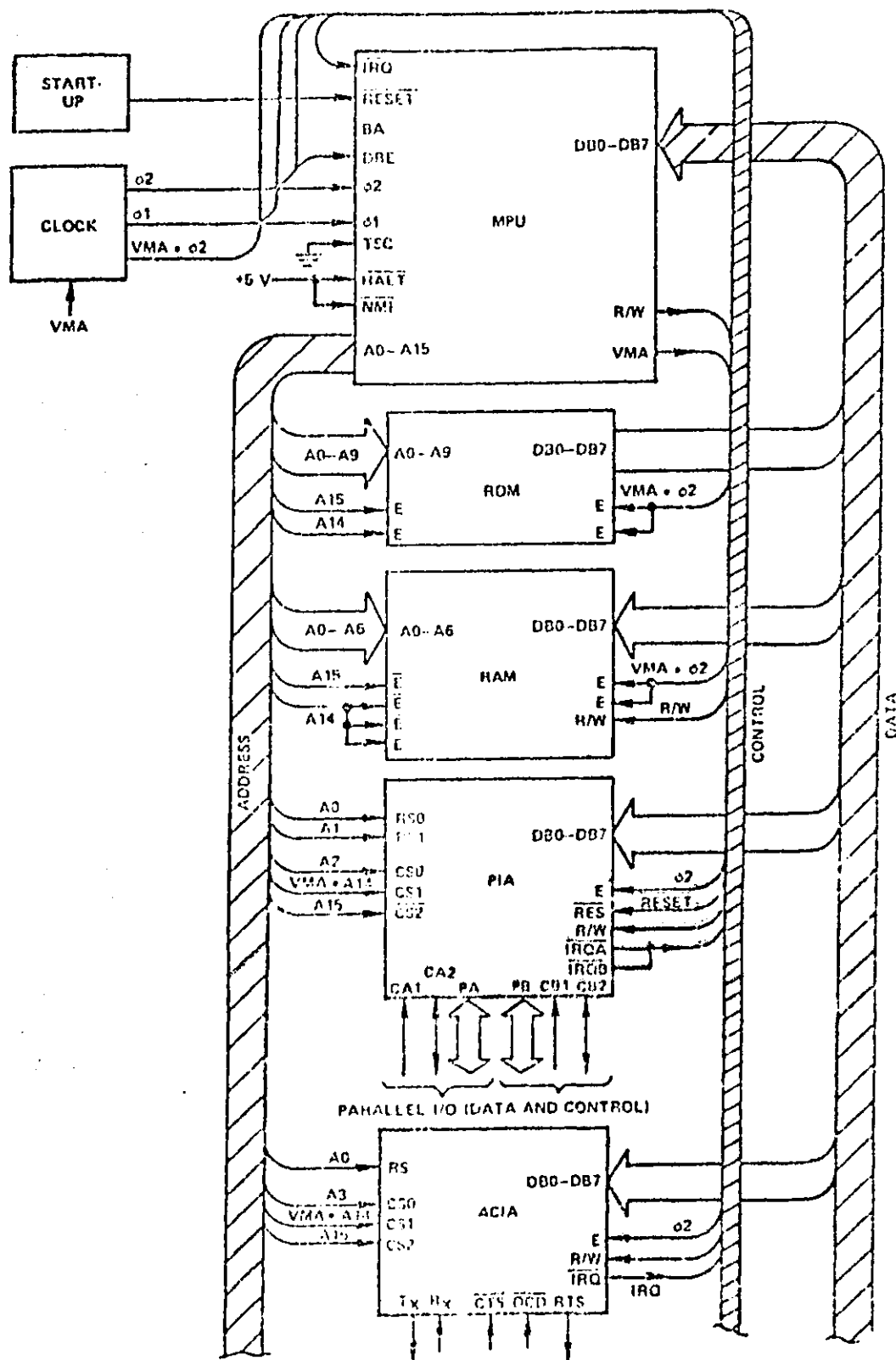


Figure 4.6 : Family Addressing

CHAPTER 5

DIGITAL SIMULATION

5.1 Hardware

This chapter is divided into three sections; (1) Memory expansion, (2) PIA, Sample & Hold and Multiplexer board, (3) Circuitry to drive the meters.

The basic MEK/D2 Microcomputer Module provides for a maximum of 512 bytes of on-board static RAM, Figure 5.1 presents the Bus Peripheral Allocation Map for the basic MEK/D2 system. The decoder output terms which enable the first three 8K blocks of memory beginning with address zero, are RAM, 2/3 and 4/5.

	Address Ranges
JBUG ROM	E000-e3FF
User PROM	C000-C3FF
JBUG Stack/RAM	A000-A07F
Keyboard Module PIA	8020-8023
Keyboard Module ACIA	8008-8009
User PIA	8004-8007
User PROM	6000-7FFF
User RAM	4000-5FFF
User RAM	2000-3FFF
User Static RAM	0000-01FF

Figure 5.1

Figure 5.1

The key integrated circuit for generating system bus chip-select or enabling signals in the MEK/D2 is the high-order address decoder U11 a 2-line to 4-line decoder/Multiplexer. This logic element decodes three most-significant bits, A15, A13, of the address bus in accordance with the following truth table.

A15	A14	A13	Bus Enable Term	Comments
0	0	0	$\overline{\text{RAM}} = 0$	Enables 512 byte array On- Board
0	0	1	$\overline{2/3} = 0$	Enables 8K range of user stack
0	1	0	$\overline{4/5} = 0$	Enables 8K range of user stack
0	1	1	$\overline{\text{PROM}} 1 = 0$	Enables user PROM located at 6000
1	0	0	$\overline{\text{I/O}} = 0$	Enables ACIA located at $(8008)_{16}$
1	0	1	$\overline{\text{STACK}} = 0$	Enables 128 byte RAM used by JBUG
1	1	0	$\overline{\text{PROM}} = 0$	Enables user PROM located at C000
1	1	1	$\overline{\text{ROM}} = 0$	Enables JBUG ROM located at E000

This scheme divides the 64K addressing range of the MPU into 8K blocks. The 512 byte static RAM array is placed in the bottom 8K range, the next two 8K blocks are reserved for expansion RAM, the fourth contains a user PROM, etc.

Expansion for additional memory is accomplished by providing address and data bus buffers as well as some Off-Board control logic. Figure 5.2 presents a functional block diagram summary of the supplemental logic necessary to support Off-Board memory expansion. Shaded blocks represent logic available with the basic MEK/D2 system.

The static RAM's used here require up to 250 ns of data hold following chip deselect. The 10 ns data hold specified for the MC6800 MPU is in-sufficient to meet this requirement. The data bus enable (DBE) stretch network shown must be added if this type of RAM is utilized in the Off-Board expansion array. The Memory Control Handshake Logic provides control and timing signals between logic resident on Off-Board memory systems and the MPU clock module. Data transceivers, with a control logic block, are required to buffer bidirectional data to the Off-Board memory array as shown. The block labeled " Array Select Decoder " represents logic for converting high-order address decode signals to Memory-Block enabling signals. These activate either the On-Board or Off-Board array within the appropriate addressing range of a memory reference instruction.

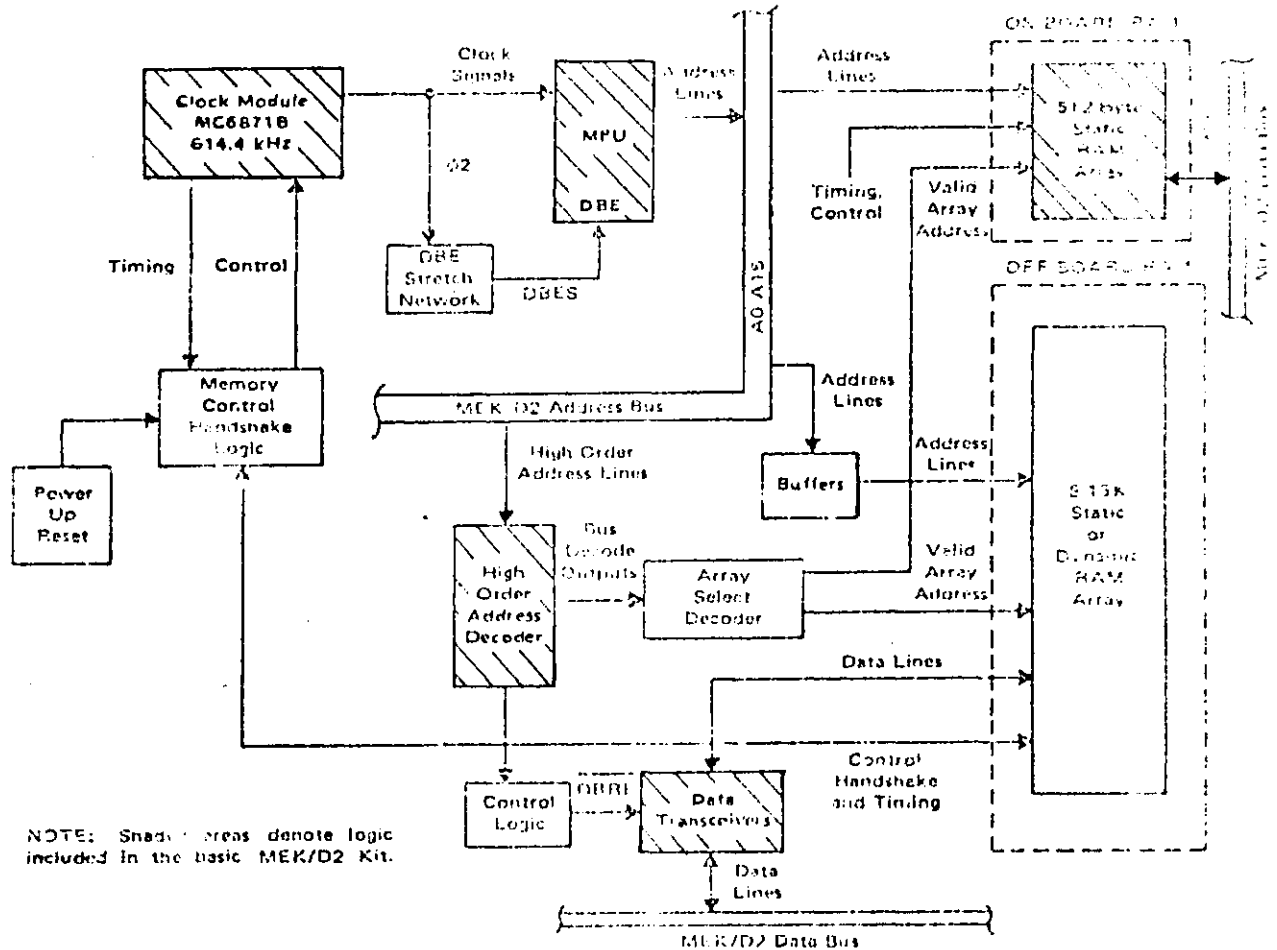


Figure: 5.2

Before giving an explanation of the PIA, Sample & Hold and Multiplexer it is essential to outline briefly the hardware objectives. The essential features of a simulator would be to have the minimum facilities shown in Figure 5.3, i.e. an input representing a changing daily load pattern that is continuously variable, over a range derived from a tape recorder, provision for a base load and, to meet these loads, two variable generators with different displays, controls, characteristics and start-up delays. Also a unit cost would be allocated to each generator to represent the cost per MW at full load.

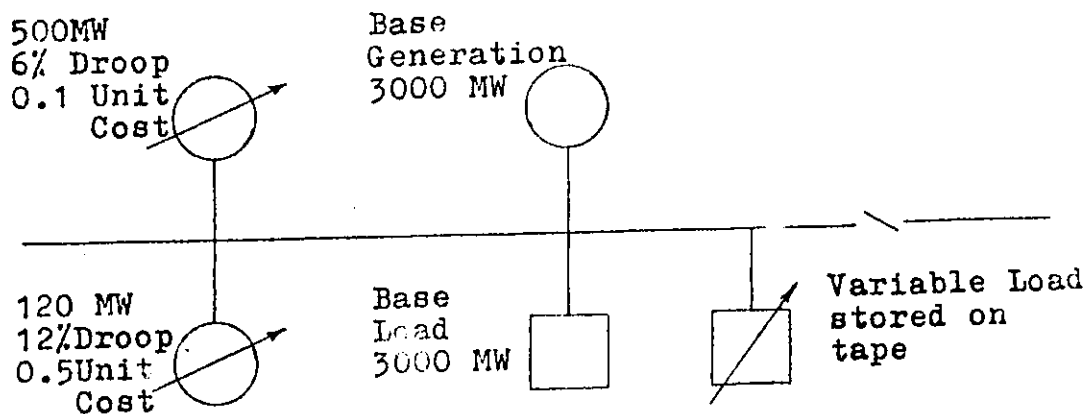


Figure: 5.3

Thus it is essential to have four output signals to drive four different meters, these are; current values of generation on generators No:1 and 2, system frequency, which would be plotted on an X-Y plotter, and finally the total cost, which would be shown on a separate meter.

Also on the other hand three different inputs are needed these are; required generation targets for generators No:1 and 2, the daily load requirement which is to be met.

But as previously mentioned the standard MEK/D2 kit supplies only one PIA for user application which could only handle one input and one output at a time. So strategy had to be devised to expand the input/output capability of kit to the above requirement. A number of different alternatives were considered but the one which was thought to be more economical is as follows; Figure 5.4 gives a general view of the set up and Figure 5.5 presents in more detail the connections for the Sample and Hold unit. Hold step, acquisition time and droop rate are the major consideration in the selection of a hold capacitor value. Also dielectrics with very low hysteresis are polystyrene and polypropylene. A 0.22 μ F polypropylene capacitor was considered adequate which gives a hold step of 0.05 mV, an acquisition time of about 300 μ S and a droop rate of about 3×10^{-4} V/S : for further information refer to R.S. Data Sheet 307-086 . Offset adjustments have also been accounted for. Figure 5.5 clearly shows that at each time one of the four Sample and Holds is chosen to Sample while the rest are in Hold state.

For the input expansion a C-MOS Analog Multiplexer MPC8S was used which is a single-ended monolithic 8 channel analogue multiplexer which features self-contained binary channel address decoding : see Figure 5.6.

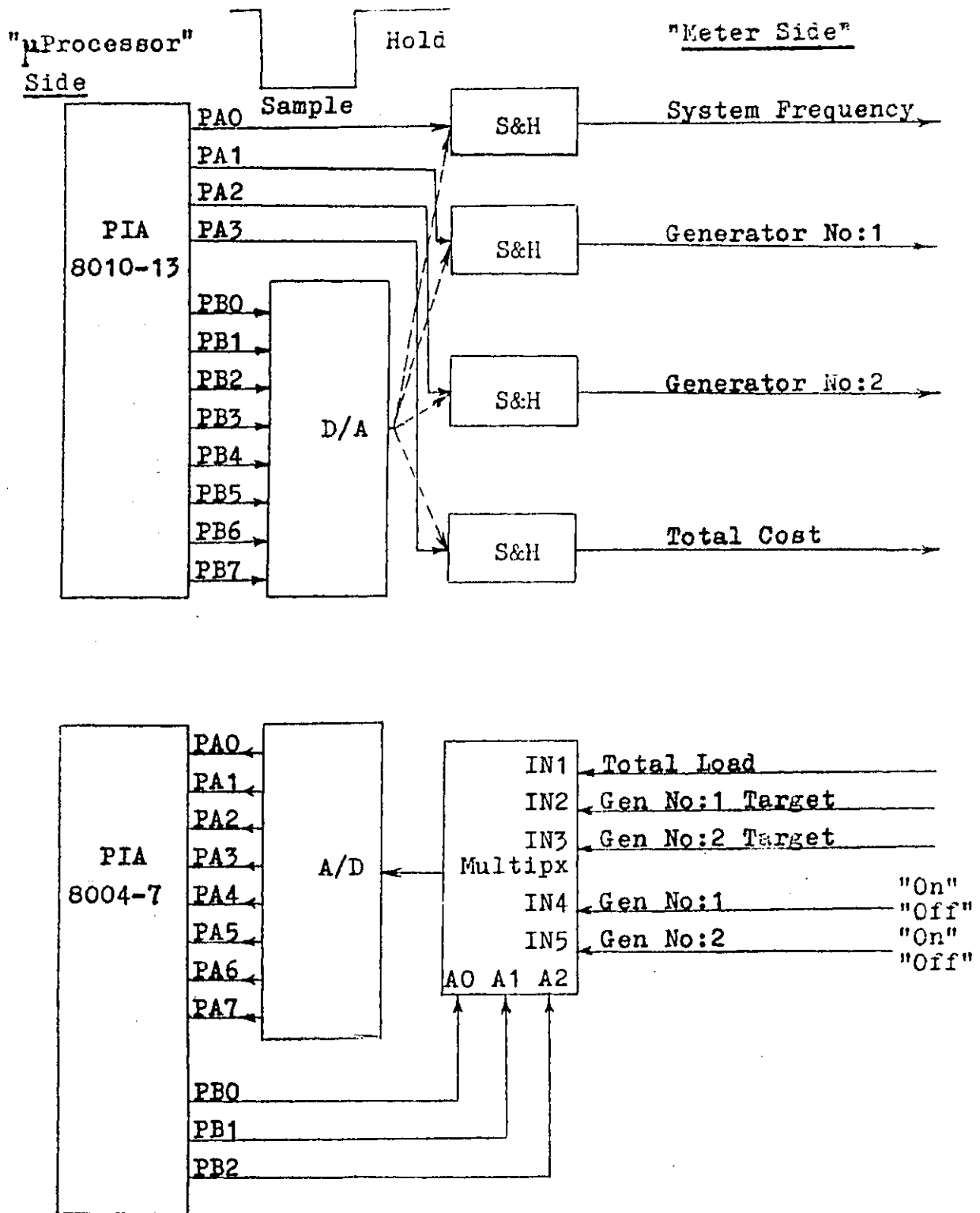


Figure: 5.4 Input/Output Expansion

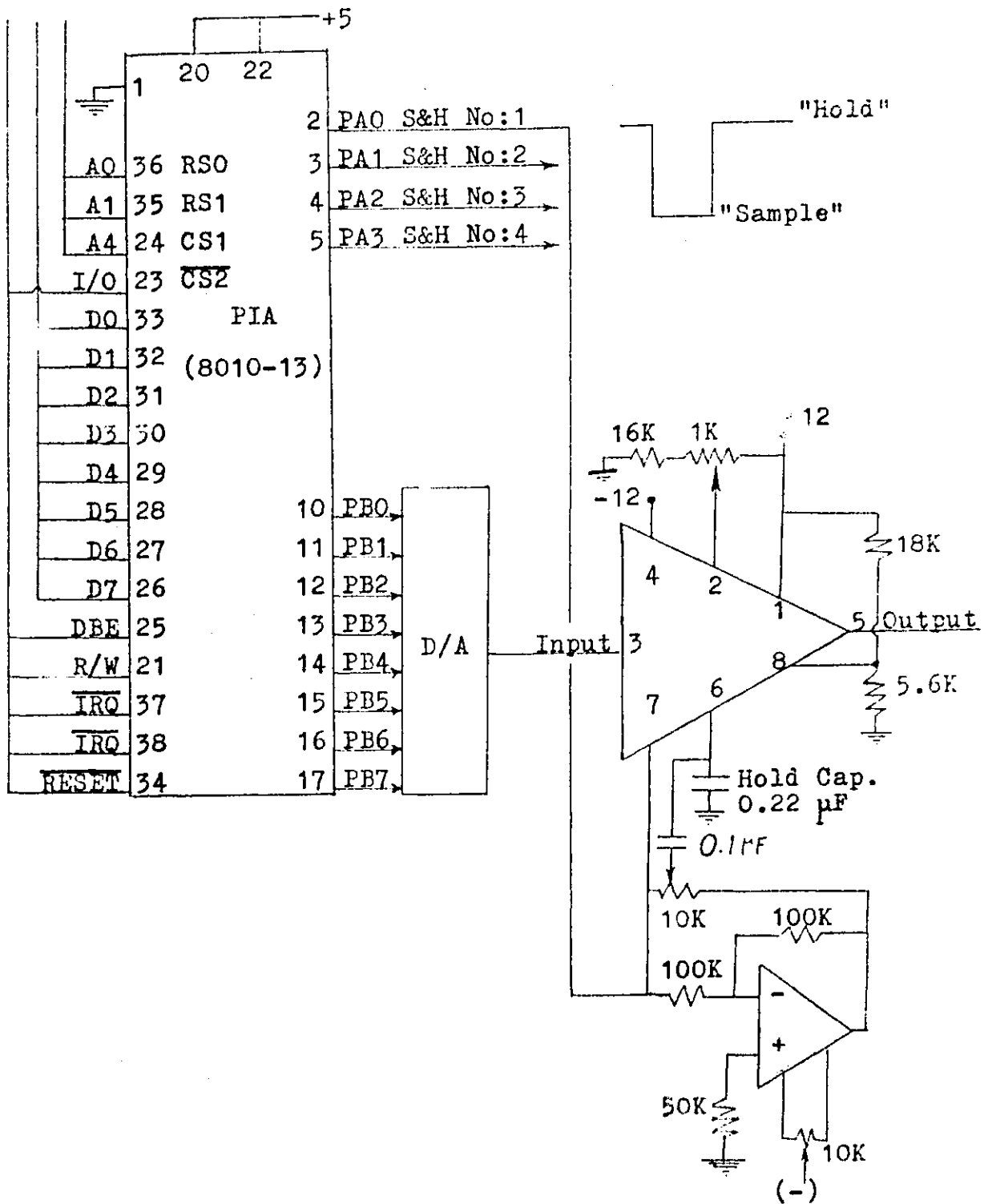
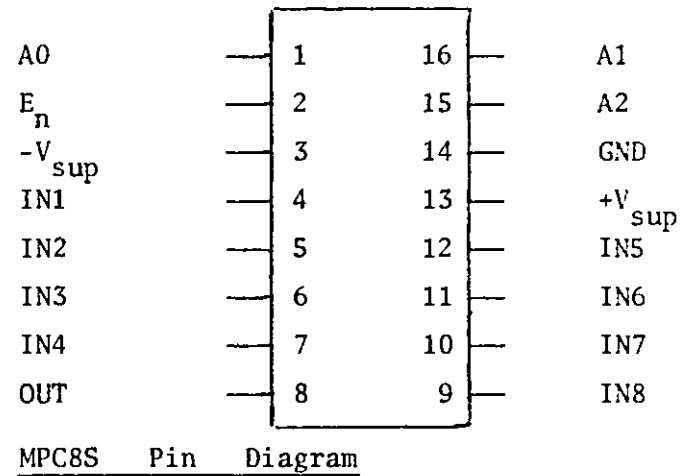


Figure: 5.5 Connections to Sample and Hold

A2	A1	A0	E _n	On Switch
X	X	X	L	None
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

Truth Table

Figure: 5.6



with what has been said in section 4.3.2 about addressing a PIA, Figure 5.5 completes the pin connections required for this additional PIA to be addressed at 8010-8013.

The circuitry to drive the meters is straight-forward : Figure 5.7. One of the requirements was to be able to record a typical daily load curve on a tape recorder so that it could be replayed to observe system frequency behaviour. The tape recorder used here records a-c. signals of about 2 mV peak to peak as a limit. So a.c. variations are recorded, while this signal is being rectified by unit 3 to get a proportional d.c. signal to drive the pointer on an X-Y plotter to follow a daily load curve. With the recorder on replay and the switch S1 on EAR terminal of the recorder it is possible for the total load information to be fed into microprocessor at unit 6 and also to drive a meter. X-axis drive is produced by unit 8 producing a variable time scale on the plotter. These are assembled on MB Board.

Circuitry on G1 and G2 board, Figure 5.8, drives the meters for two generators on momentary action of the push-button switch, unit 3 displays the target generation required. On release of this switch, units 2 and 5 will provide this information of the microprocessor, the related subroutine will respond with a delay equivalent to power station operators and this response is then displayed on the meter by unit 1. All the connecting points are numbered on these boards.

CHAPTER 6

SOFTWARE AND PROGRAM DESCRIPTION

6.1 Introduction

Most segments of program are essential to the proper operation of the microcomputer hardware. A cross assembly of these segments is to be found in Appendix B. This chapter explains the need for these programs and offers supplementary information to that contained in program comment statements.

The program can be divided into a number of segments such as; Initialisation of PIAs and other working registers, generator response to the demands made by the operator, simulation of system inertia and in respect of two sets of 500 MW and 120 MW, the cost calculation of their operation and finally instructions to read and display (input/output). But before going into program description it is essential to describe some points about the method chosen for integration, a first order log and finally the reference level chosen through out this program.

6.2 Integration

The Motorola M6800 used here is an eight bit machine so the data information can vary from $(00)_{16} = 0$ up to $(FF)_{16} = 255$. Therefore the author has chosen $(80)_{16} = 128$ as the reference frequency 50 HZ with upper frequencies represented by numbers greater than $(80)_{16}$ and vice versa, which lead to the reference level through-out the system being $(80)_{16}$ at steady state.

The input/output voltages of A/D and D/A are set to (0-4)volts, so it is essential to allow for numbers either to add up or to subtract downwards. Now at steady state the input to the integrator is $(80)_{16}$ that is about 2V at A/D, the integration process could simply be shown by an example as follows ; Supposing a voltage greater than the reference voltage is to be applied as a step input say $(90)_{16}$ which is step of $(10)_{16}$ with respect to reference level, so a fraction of this difference is added on to a register, (or subtracted if it is a voltage lower, say $(70)_{16}$), see Figure 6.1.

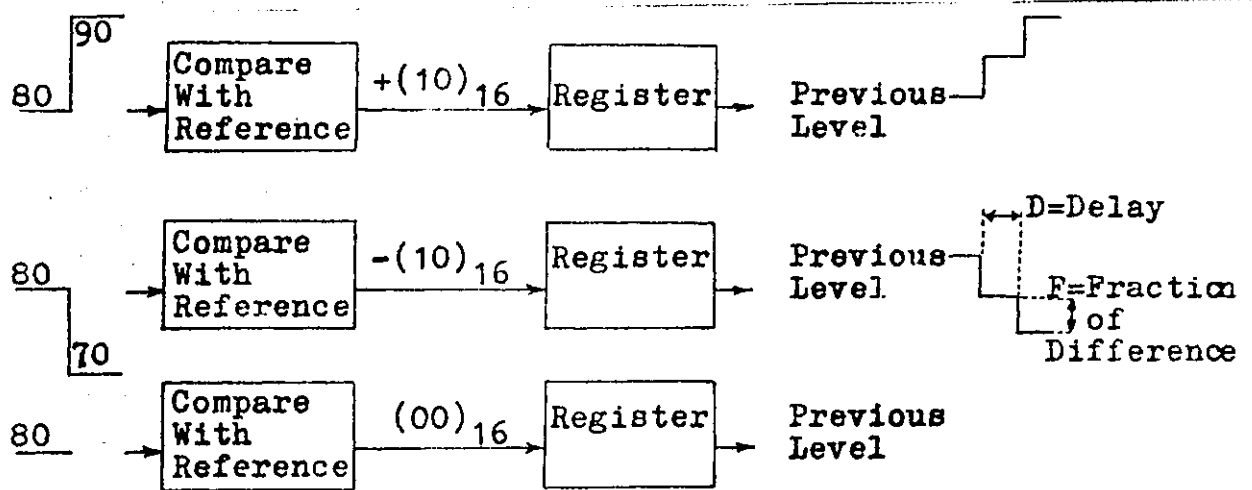


Figure: 6.1

As shown on Figure 6.1 the fraction of difference in input voltage whether higher or lower than reference voltage is added or subtracted from the output of the register after a certain period of delay time. Now it can be appreciated that the time constant of any integration is determined by the proportion of these two values.

Similarly to perform a first order lag $\frac{1}{1+ST}$ in the S plane the routine is the same as the one for integration with a difference that here the present output is compared with the target value to be met as shown in Figure 6.2.

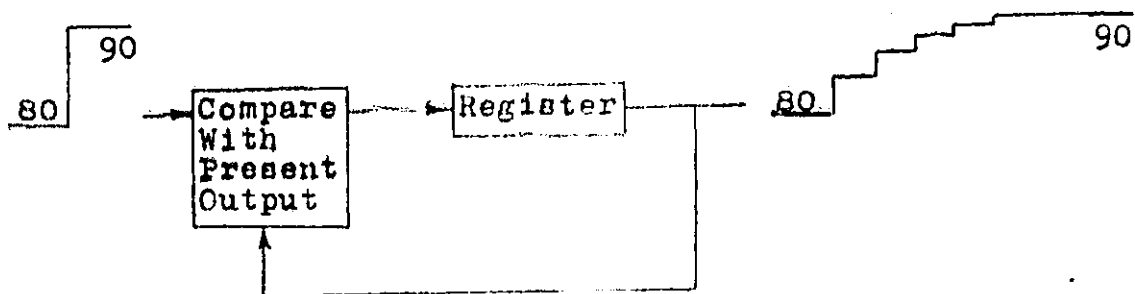


Figure: 6.2

6.3 Program Structure

Figure 6.3 offers a general view of an appropriate software structure. The full listing of the final program in assembly language is listed in Appendix B. As shown in Figure 6.3

the program will consist of generating plant supplying a load such that any generation surplus or deficit causes the system frequency to rise or fall respectively. The generation model consists of two conventional plants of 500 and 120 MW (i.e. plant 1=oil reheat with 6% droop characteristic, plant 2=oil non-reheat with 12% droop characteristic) plus base load plant. The variable load recorded on the cassette tape will be played back and required generation would be met by the operator.

6.4 The Initialization Routine

The program lines from 01010 to 01230 inclusive establishes, the desired I/O configuration and Control Register modes as part of an initialization sequence. Figure 6.4 summarized the use of two PIAs, as shown Peripheral Lines PA0-PA7(A Side) of PIA No:1 are assigned to "read" Analog to Digital Converter, where as three of B side Peripheral Lines PB0=AO, PB1=A1, PB2=A2 are used as outputs to address a certain input at multiplexer, hence, A and B sides of PIA No:1 must be established as inputs and outputs respectively.

Also Peripheral Lines PB0-PB7 (B Side) of PIA No:2 are assigned to "write" to Digital-Analog converter, and four of "A" side Peripheral Lines PA0=Sample 1(Frequency), PA1=Sample 2 (Generator No:1 500MW), PA2=Sample 3(Generator No:2 120MW) and finally PA3=Sample 4 (Total Cost) are used as outputs to enable a certain Sample and Hold unit, hence, A&B sides of PIA No:2 must be established as outputs.

As there is no assurance that the PIA internal register bit positions are initially zero prior to initialization, the sequence from program line 01010 to 01230 should be used, referring to section 4.3.2. by clearing the control register at (8005)₁₆ the data direction register is called at (8004)₁₆ address which then can be cleared to make all peripheral lines as inputs on "A" side, the constant 2C=0010 1100 loaded into the A side Control Register by instruction 01030 has the following effect: b0=0 disables any interrupt $\overline{IRQA}$ so b1 would be in a "don't care" situation, b2=1 selects Output Register A side (which were established as inputs); b3=1, b5=1 selects CA2 as output and as a read strobe with E restore, b6 and b7 are "don't care" since MPU can not write into those two positions:

b7	b6	b5	b4	b3	b2	b1	b0	
0	0	1	0	1	1	0	0	= 2C Hex

Instructions 01060-01070 write "ones" into the B Data Direction Register, thus establishing PB0-PB7 as outputs. The constant loaded into the B side of Control Register by instruction (01080) has the following effect; b0=0 disables any $\overline{IRQB}$ so b1 is don't care; b2=1 selects Output Register B side; b3,b4,b5,b6,b7 are don't care.

b7	b6	b5	b4	b3	b2	b1	b0	
0	0	0	0	0	0	0	0	= 04

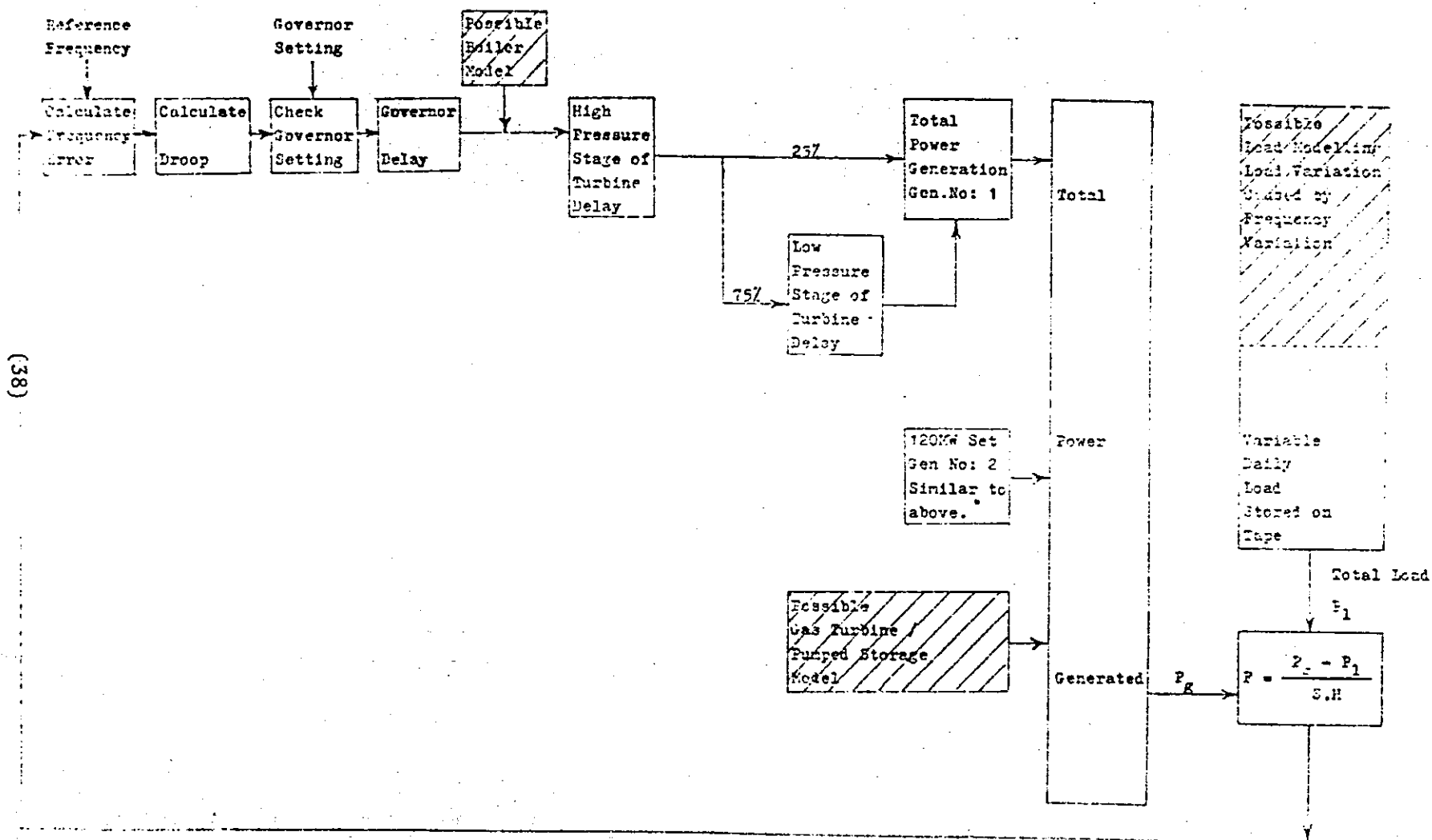


Figure 6.3 "Simulation Program Structure"



Not Included

Instructions 01130 to 01230 are for PIA No:2 in a similar manner the reason that a read strobe with E restore was chosen is to obtain pulses at CA2 or CB2 as a means by which program cycles are "Timed", that is whenever it is written into register 8012 a single pulse is generated and hence a measure of time is achieved by counting these pulses.

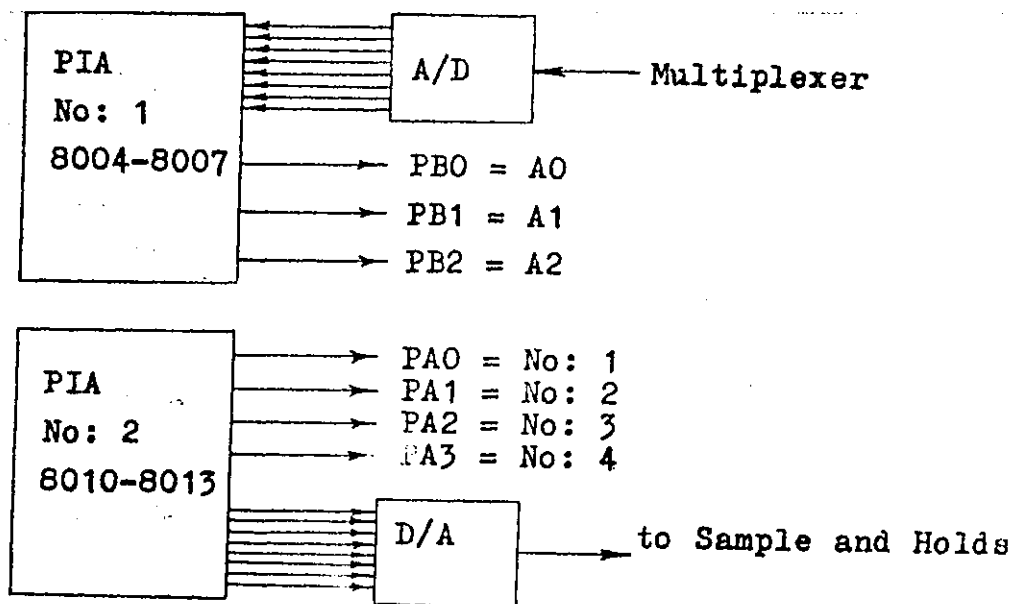


Figure: 6.4

6.5 Generator Units

The program lines from 01270 to 02280 inclusive reads, the desired generation required on 500 MW set i.e. lines (01260-01460) then as in real life but four times faster response is made at (01480-02000) and finally the output is displayed by (02000-02280).

Instructions 01280-01290 choose input No:2 (Generator No:1) of the multiplexer unit but always reading or writing into A/D and D/A respectively. These converters used here take about 0.5mS for conversion hence instructions at lines 01270, 01300 and 01310 are to produce such delay. Instruction at line 01330 reads the target generation. In writing or reading to the Output Register of a PIA, the already available information on this register is always written or read into/from peripherals, therefore to avoid any mixture of information, they are to be written or read twice throughout the program.

Load and deload rate for this 500MW set is assumed to be, say, 100MW per 40 seconds, that is 10MW per second for a four times faster simulation. As shown on lines, 00280 to 00310, four addresses are used as working registers: target generation, generator response, previous output and a scratch register respectively. A flow chart of this program is pre-

sented by Figure 6.5.

To provide a generation of 10 MW per second it is necessary to 'time' the program cycle, and its measured value will vary from 13.6ms (one generator in use) up to 16ms (where both generators are in use). For further details on timing, please refer to Appendix C.

As previously mentioned data numbers vary from $(00)_{16}$ to $(FF)_{16}$ in Hex so total generation was taken to be $(FF)_{16}$ in Hexadecimal equal to 256 and was divided proportionally to represent 500MW and 120MW that is about $(D0)_{16}$ and $(30)_{16}$ in Hexadecimal respectively.

So to make up for appropriate time constant of generator response ($10\text{MW/S} = (04)_{16}/\text{S}$), a fraction of input (here $1/16$) is added or subtracted to or from present output. But this is after a delay time which is calculated as follows :

$(04)_{16}/\text{S}$ is equivalent to $60\text{mV/S} = 0.06\text{V/S}$
(as $4 \times 15\text{mV} = 60\text{mV}$)

Now say;

input = $(X)_{16}$ then output = $0.06 (X)_{16}/\text{S}$

taking $(1/16)$ of input at a time

output = $0.06 * 16 ((X)_{16}/16)/\text{S}$
= $0.96 ((X)_{16}/16)/\text{S}$

Considering that each program cycle takes 16 ms means software program completes 63 cycles per second, so to have above rate of response; it is divided by 0.96. resulting a delay number of $66 = (0042)_{16}$ (Lines 01640 and 01870).

Lines from 02030 up to 02290 will display generator's response on the meter. Address 007D is used as a register to store the up to date value of generator response and that is to be displayed as shown in line number 02030. Then in the following lines, it is written into the output register (with a delay required to write). At line number 02090 the particular Sample and Hold is chosen here named by Sample and Hold No.2, by:

$(FD)_{16} =$ 1 1 1 1 1 1 0 1 $\xrightarrow{\text{Sample}}$
 b7 b6 b5 b4 b3 b2 b1 b0

it is bit (b1) which is low (i.e. Sample) and the other bits high (i.e. Hold). And as explained this should be written on the other side of the PIA i.e. address 8010. For this part of program we have used four different addresses from 007C to 007F each for a different data storage as follows;

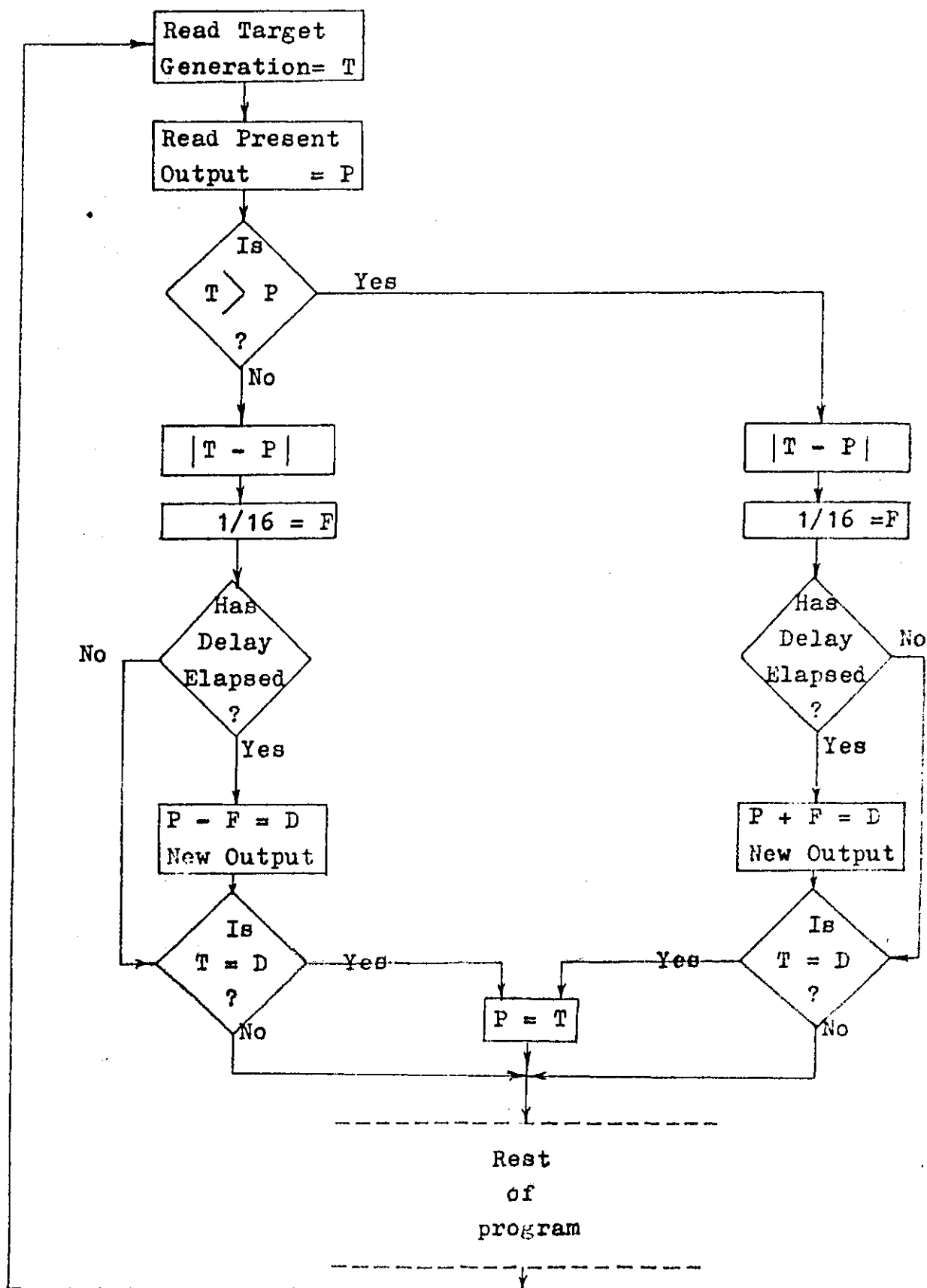


Figure: 6.5

```
007C Present value of Generator 1 response.
007D Previous value of Generator 1 response.
007E Scratch register to store incremental values.
007F Target generation value to be reached demanded by operator.
```

Line numbers from 02320 to 03350 are to simulate generator set No;2 (120MW) and it is similar to what was explained for Gen. No:1(500MW). The only differences are as follows;

Line number 02330 chooses input for the second set, inside multiplexer by;

(02)₁₆ = 0 0 0 0 0 0 1 0 address to choose
 b7 b6 b5 b4 b3 b2 b1 b0 Gen. No:2

Similarly four addresses were used for data storage (from address 006C to 006F) as above. At line number 03150, Sample and Hold No:3 was chosen to sample by:

$$(FB)_{16} = \begin{array}{ccccccccc} & 1 & 1 & 1 & 1 & & 1 & 0 & 1 & 1 \\ & b7 & b6 & b5 & b4 & & b3 & b2 & b1 & b0 \\ & & & & & & & \downarrow & \longrightarrow & \text{Sample} \end{array}$$

and finally if we take a slower load and deload rate for this set, say 5MW per second which then would require a delay constant of (041A) in Hexadecimal, as in this case the fraction taken is (1/2) so;

output = 0.03 * 2 ((X)₁₆/2)
i.e. 63/0.06 = 1050 = (041A)₁₆ (Lines 2690 and 2920)

A subroutine is introduced at next line (03380), this is to allow synchronization of new generators at different time of simulation a simple flow chart is represented in Figure 6.5. To verify between "On" and "Off" states of a generator, it is to load voltage of 3.98 volts which is equivalent to $(FF)_{16}$ in Hexadecimal and zero volts that is $(00)_{16}$ to the Analogue/Digital converter via multiplexer respectively. Hence lines 10210 and 10330 are to load the state of generator No:1 at fourth input, also lines 10490 and 10610 are to load the state of generator No:2 at the fifth input terminal of multiplexer. Note "On" and "Off" states are verified by two switches, refer to Figure 5.4.

This generation should meet the total daily load curve replayed from a cassette tape recorder, which is read by the instructions between lines 03450-03630 inclusive. Instructions at line 03460 chooses the particular load input in multiplexer, by;

(00)₁₆ = 0 0 0 0 0 0 0 0
b7 b6 b5 b4 b3 b2 b1 b0
Address to choose load input on Multiplexer

Instructions between lines 03640-03760 finds the difference between the load and generation provided (Total load is stored at address 0082) and a resultant input is produced with respect to the steady state level of $(80)_{16}$.

6.6 Simulation of System Inertia

As was mentioned in Chapter 2, the inertia of the system is represented by an integration block where its input would be an error between the input to the system and the governor response. This error is stored at address 00F2. This is compared with a constant reference level of (80) in Hexadecimal at address 00F1 and finally the output of the inertia block is stored at address 00F0 which is the frequency of the whole system (address 00F5 is used to store the incremental values during the integration process). This segment is completed between lines 03800-04220 and it's flow chart is represented by Figure 6.6

Instructions at lines 03950 and 04140 present the delay constant which can be calculated as follows; At section 2.4 the inertia constant was chosen to be 4s, that is if a step error of 1MW in power was applied at the input then integration should take place at the rate of $\frac{1}{4}$ MW/S and so for a four times faster simulation, a rate of 1MW/S is needed. This can become clearer with an example; say input error is $(10)_{16}$ in Hexadecimal and so the fraction to increment would be:

$$(10)_{16} \times (\frac{1}{4}) = (04)_{16}$$

and if it is incremented after a delay of about 250 ms it would make up the rate of integration required, but the time taken for each cycle is already mentioned to be about 16ms (=63 cycles/S) therefore a constant delay number of about $(0010)_{16} = 63/4$ is needed, which was stored at addresses $(0000)_{16}$ and $(0001)_{16}$.

To stop any overflow after incrementation, instructions at lines (04000-04030) and (04190-04210) are used, here output is compared with upper limit of $(F0)_{16}$ and the lower limit of $(10)_{16}$, so that if output value exceeds beyond these limits it would be made equal to its appropriate limit.

To match this digital model with its analogue, a negative sign is taken care of by instructions 03990 & 04180, i.e. addition of fractions to the output instead of their subtractions and vice versa, hence an integration with negative sign was produced.

Instructions from line 04250 to 04520 are to plot the frequency of the system. If for any reason excessive frequency deviation is observed, then action is taken to initialise and reorder the system so to restart the procedure all over again. This is accomplished by introducing a subroutine at line 04250. Finally before moving to the next

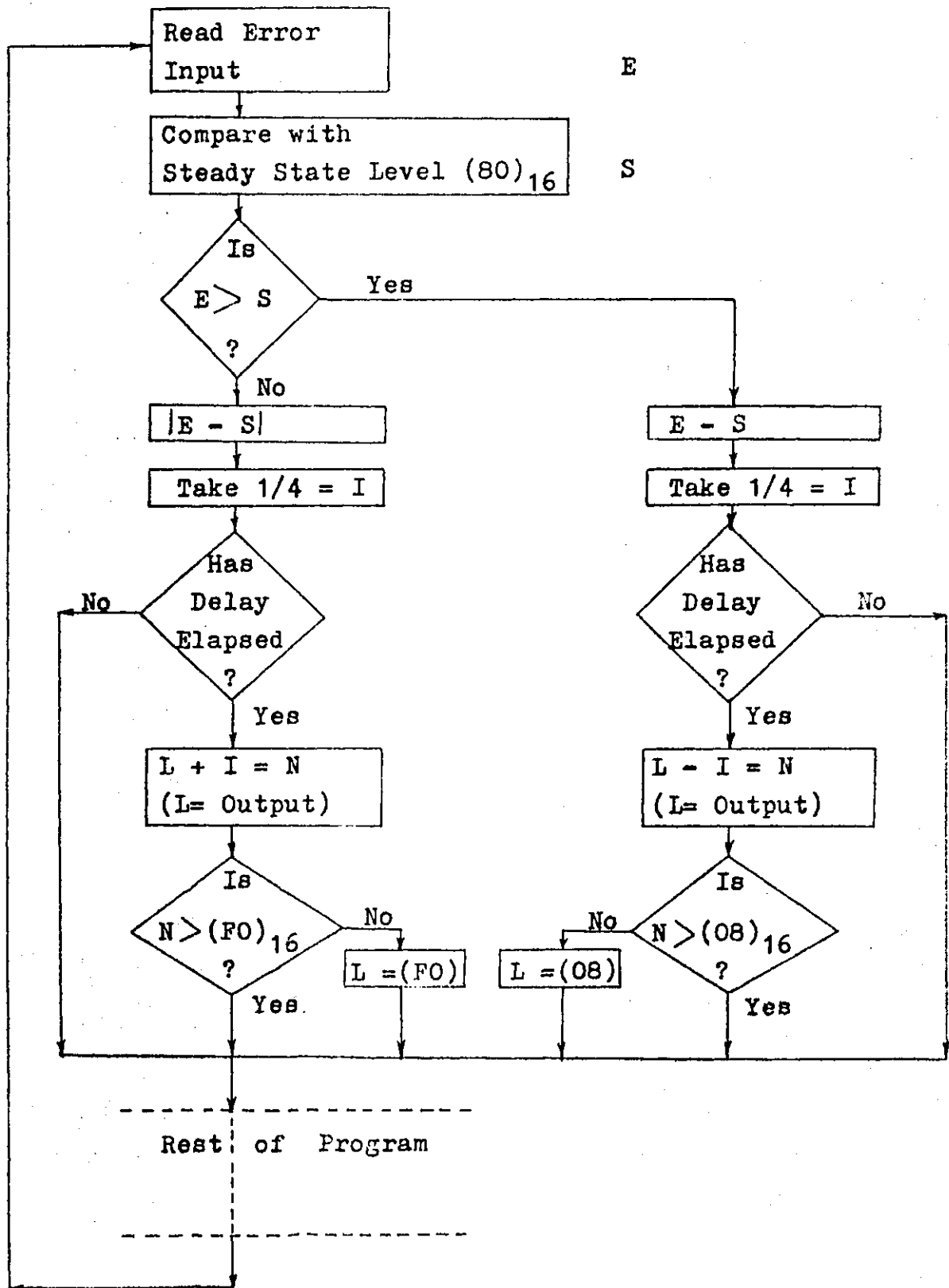


Figure 6.6 : System Inertia

segment as was explained, $(FF)_{16}$ in Hexadecimal chooses Sample and Hold No:1 to display frequency;

$$(FE)_{16} = 1\ 1\ 1\ 1\ 1\ 1\ 1\ 0$$

Sample

6.7 500 MW Set :

A few chart of this segment is represented on Figure 6.8 where Figure 6.7 clarifies registers used to store different states.

Instructions from lines 04560 to 04590 examines the operators demand and if the set is not used microprocessor will jump to the next set. To make the system more realistic a sleeve limiter routine is added, as in lines (04720-04740) and (04650-04670).

The Droop characteristic was taken to be 6%, which means a gain of about 16. Therefore maximum frequency error (Sleeve limit) before multiplication by 16 or $(10)_{16}$ in Hexadecimal, is $(07)_{16}$;

$$\text{i.e. } (07)_{16} \times (10)_{16} = (70)_{16}$$

this is then to be added or subtracted from gear setting C which is $(80)_{16}$ at steady state. Moreover in order to match digital and analogue simulation, instructions at lines (04860-04940) are included to take care of a negative sign in every first order lag response. Also the position limit will represent limits of fully open and fully closed valves. These are included at lines (05120-05140) and (05290-05310) where the lower limit of $(08)_{16}$ represents valve position fully open and upper limit of $(F8)_{16}$ fully closed.

6.7.1 Governor Model

An appropriate delay constant can be found as follows; Referring to Section 2.4 the time constant of this segment of program is 0.4 s . For;

$$\frac{1}{1+0.4S}$$

the first order lag response would start at a rate of 2.5 V/S to a step input of 1V. Whatever the input at any instant of time, fraction of $(\frac{1}{2})$ is taken and therefore;

$$2.5 * (X)_{16} / S \longrightarrow 5 * (X)_{16} / 2/S$$

hence required delay number would be equal to $63/5 = (000C)_{16}$ which is stored at addresses of 0002, 0003 .

6.7.2 High Pressure Stage Model

Since operations of blocks3,4 and 5 are similar, therefore in order to save memory locations in RAM the program is written in a way that only different registers have to

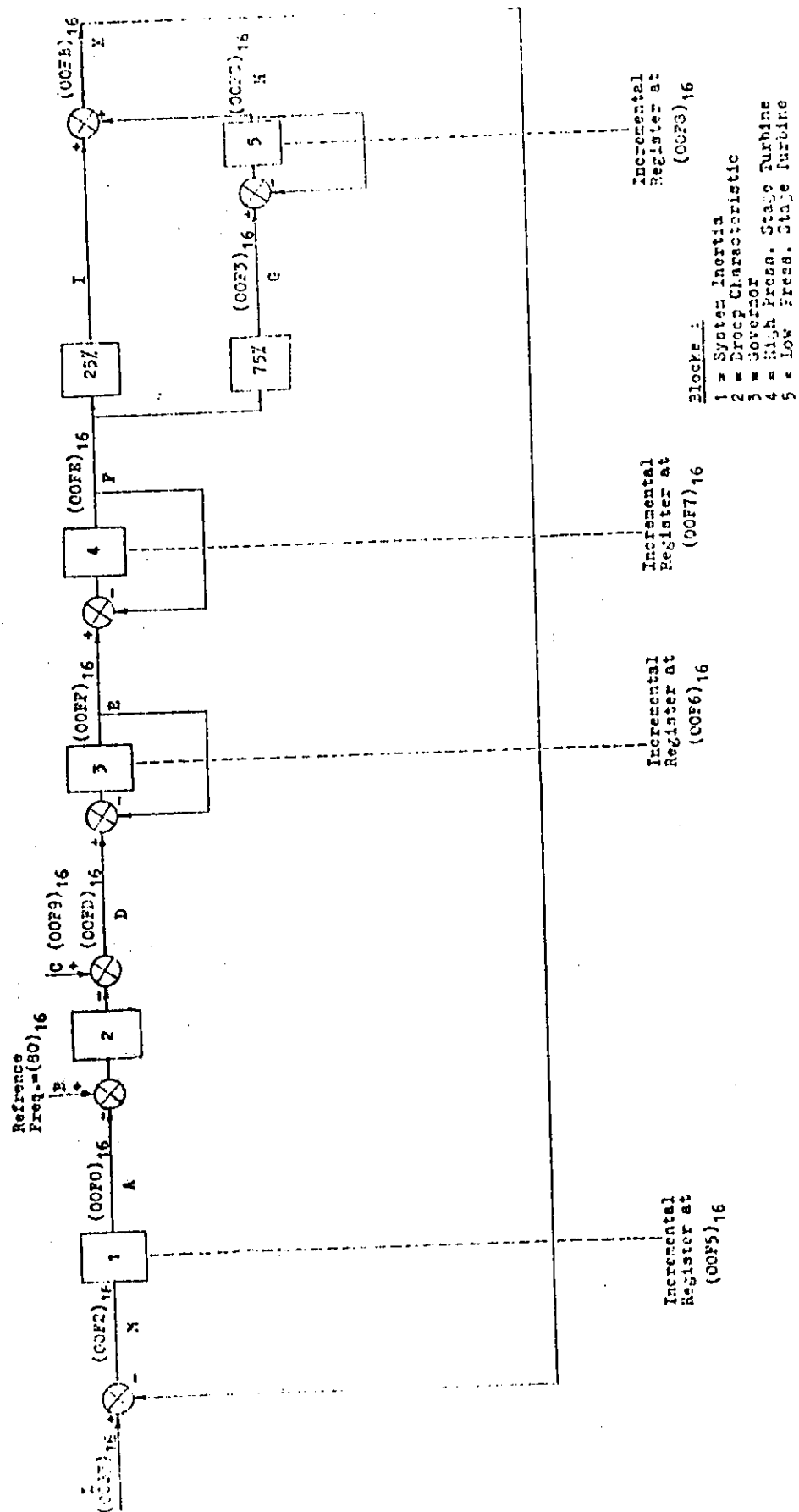


Figure 1.2 : Addressed Used in Registers For 500MW Set
 Similarly Registers For 120MW Set Are From (00E0)16
 To (00EF)16

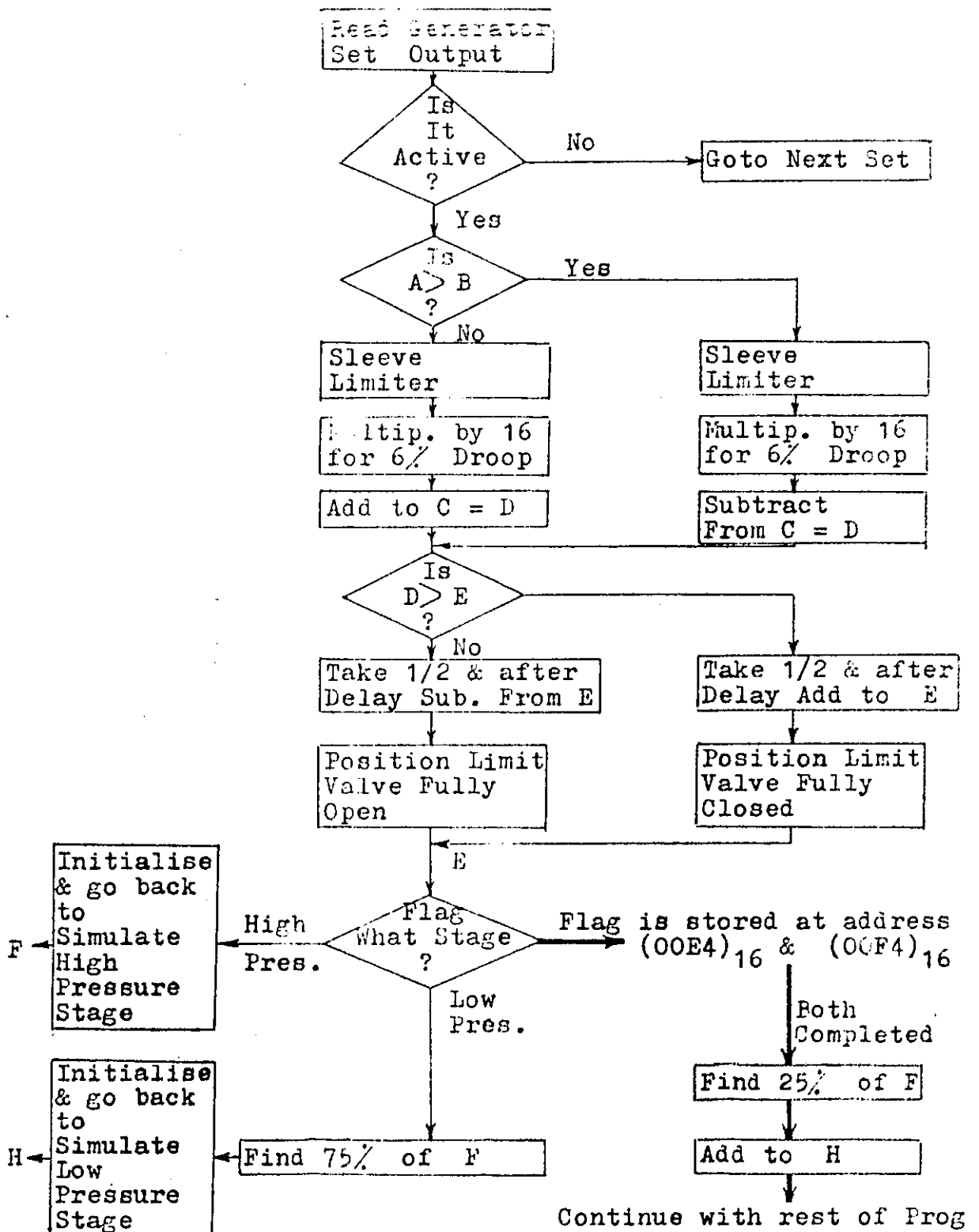


Figure 6.8 : Governor and Turbine
For signals A,B,C,D,E,H See Figure 6.7

be used in repeating the same instructions. This register change is satisfied by lines (05360-05550) which include three subroutines.

The delay time constant could be found in a similar manner to the previous segment. Referring to Section 2.4, the time constant for this high pressure stage of turbine was chosen to be 0.8, i.e. twice as big as that for governor, but on the other hand step input fraction is ($\frac{1}{4}$) (Line numbers 05000-05010 and 05160-05170) therefore the delay number would be the same as previous stage $(000C)_{16}$.

6.7.3. Low Pressure Stage Model

Instruction lines from 05560 to 05940, would change registers in order to go back, using the same instructions to simulate the low pressure stage. As only 75% of the steam goes to the reheater, hence the multiplications represented by lines (05640-05660 and 05730-05750). Throughout this program the steady state level was considered as being $(80)_{16}$ in Hexadecimal so as to compare any level of output with this value, for instance, if the output of the high pressure stage was $(90)_{16}$ (Stored at address $(00FE)_{16}$) then to find the input for the low pressure stage of turbine would have to find, 75% of difference between this $(90)_{16}$ and the steady state value of $(80)_{16}$ which is $(10)_{16}$, and not the $(90)_{16}$ itself.

Referring to section 2.4, the time constant for this low pressure stage was chosen to be perhaps the exaggerated figure of 12s. Now for

$$\frac{1}{1+12S}$$

if an input of 1V is applied then output would start to rise with a rate of 0.833 V/S. Now whatever the input, fraction of $(1/8)$ of input is taken every time as an increment, therefore;

$$0.0833 (X)_{16}/S \quad 0.67 (X)_{16}/8/S$$

so Delay Number = $63/0.67 = (005E)_{16}$

which is stored at addresses $(0006)_{16}$ and $(0007)_{16}$.

After a similar register change routine by three subroutines (lines from 05800 to 05850), first order lag response is repeated for the low pressure stage.

Instructions from line 05950 to 06390 would make the last summation to find governor response of this particular set before it is fed-back. These instructions also include initialisation of all registers before going to next set.

6.8 120MW Set Simulation

Similar instructions were used to simulate this set. The corresponding addresses from $(00E0)_{16}$ to $(00EF)_{16}$ were used to store data with respect to addresses of $(00F0)_{16}$ to $(00FE)_{16}$ which were used for the 500MW set. On this set the droop characteristic was chosen to be 12%, hence the droop subroutine will be a multiplication by 8 and consequently a different limit on sleeve limiter of $(0F)_{16}$ at lines 06530 and 06600.

Referring to Section 2.4, comparing time constants of this set with those of 500MW set would result in a proportional set of delay constants being; $(000C)_{16}$, $(0006)_{16}$, $(0003)_{16}$ for its governor, high and low pressure stage of turbine respectively. Note that the inertia block was taken to be common for both of these two sets. The above simulation is represented from line 06430 to 08270.

6.9 Total Governor Response

A subroutine was introduced at line 08310 which is to verify whether more than one generator is in use, and if so to find the average governor response from those sets. A flow chart of this segment is represented on Figure 6.9. Again as was mentioned in Section 6.7.3, all the states are to be compared with the steady state, $(80)_{16}$ in Hexadecimal, so to average these two responses, the differences with respect to $(80)_{16}$ are averaged.

6.10 Error Signal (Feedback)

Having computed the governor response (Feedback signal) and the input to this system, the error signal can be found.

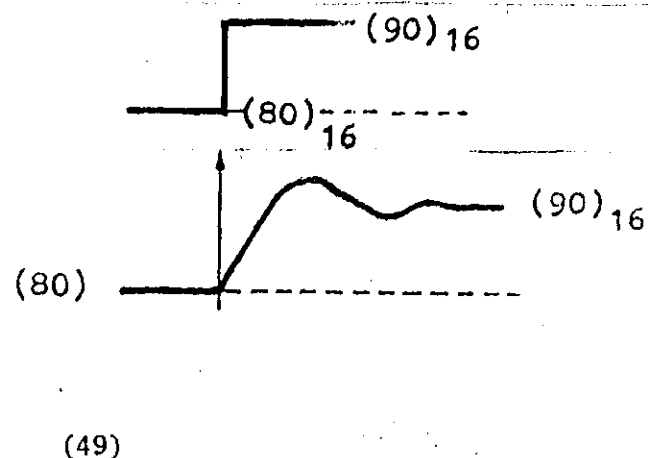
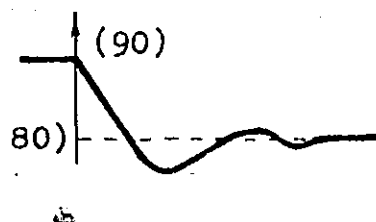
Instructions from line 08550 to 08920 are to find this error. A flow chart of this segment is represented on Figure 6.10. Programming could be made easier by direct intuition into the response wave forms as it follows;

Referring to Figure 6.7, for example

if at point "L" we apply step input of $(10)_{16}$

then response at point "K" would be

and hence at point "M" response would be;



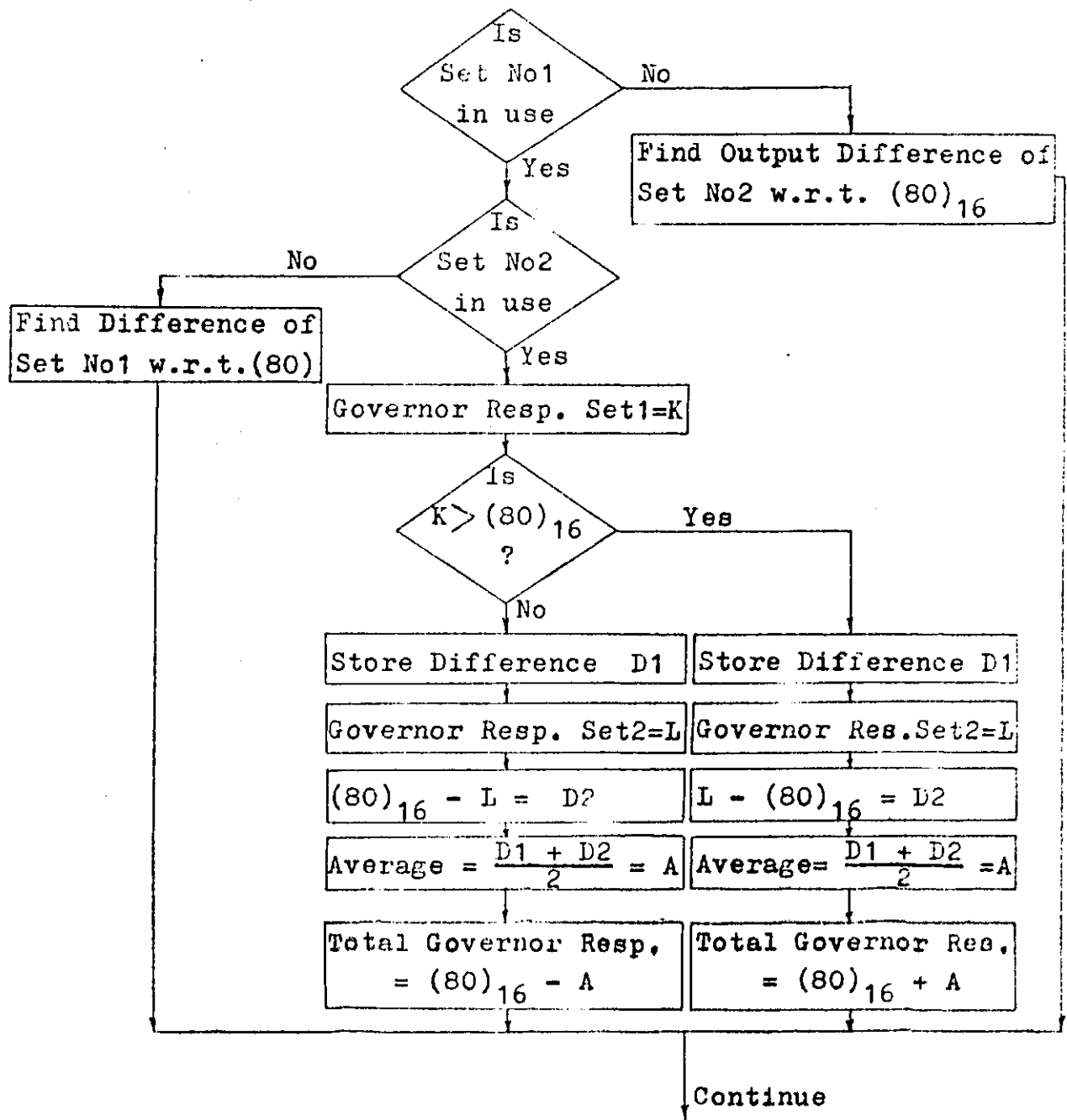


Figure 6.9 : Total Governor Response

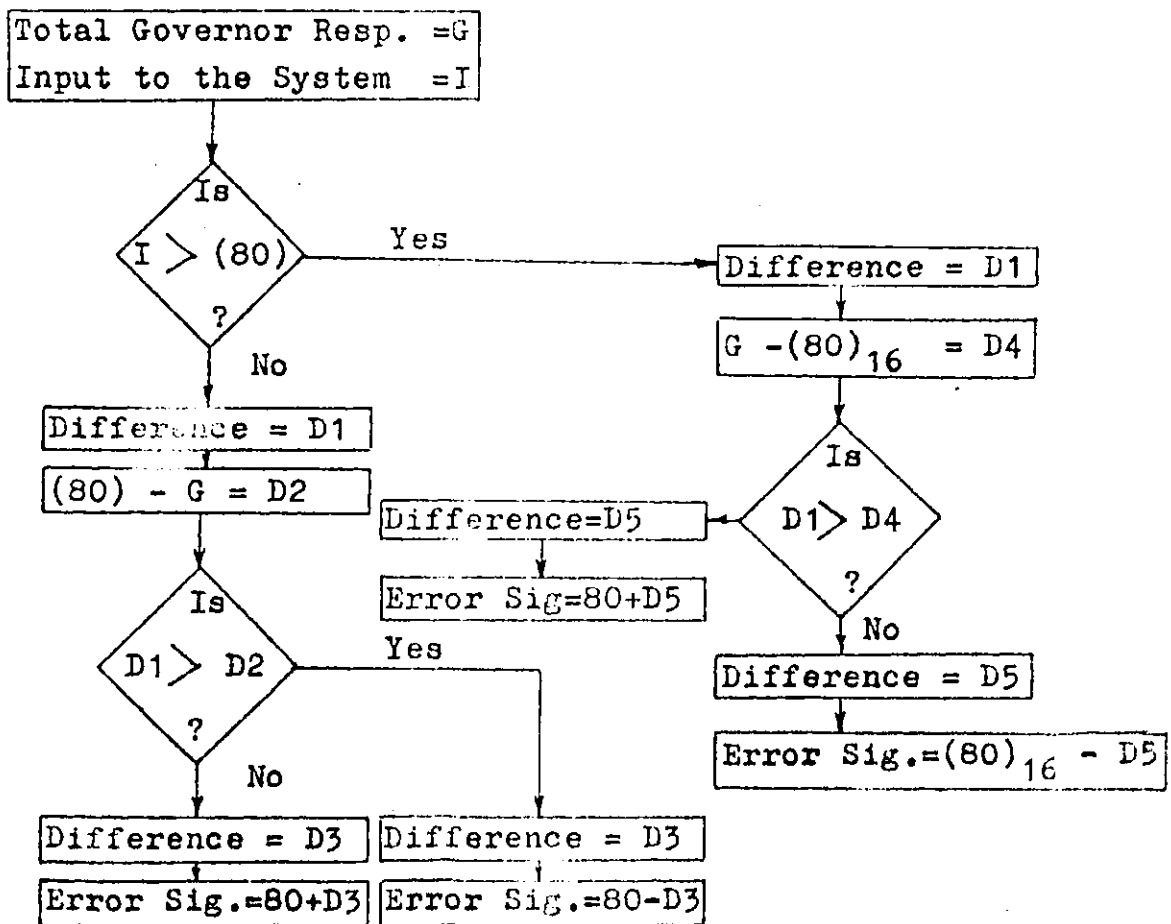
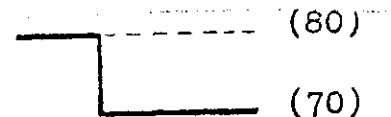


Figure: 6.10 Error Signal Calculation

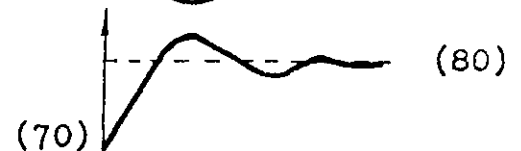
On the other hand if a negative step input was applied,



then response at point "K" would be similar to :



and also at point "M" similar to :



the point which could be made about this prediction is that whatever the situation, the Governor response and the system input, would be on the same side of the steady (80)₁₆ level i.e. they are either both lower or both higher, and this would simplify the flow chart in Figure 6.10.

Also depending on error of governor response with respect to system input and regarding whether they are greater or smaller than steady state value, will decide last summation or subtraction with respect to (80)₁₆.

6.11 Cost

Finally, in order to find the total cost of operation (lines from 08950 to 09040) the integrated output of each set is multiplied by a cost factor. Generator No:2 is taken to be five times more expensive than the first set. The generating cost can also be plotted by Sample and Hold number 4. (Instructions from line 09080 to 09330).

CHAPTER 7

EVALUATION OF DIGITAL SIMULATOR

7.1 General

In this chapter the main display panel is illustrated and its facilities are explained. Procedures are described for recording a daily load curve by using a cassette tape recorder for scheduling generators to meet this load. Single and double generator system responses to a step load have been studied. Also frequency variations have been looked at as a function of variables such as; governor set point, governor droop characteristics, load variations and so on. Finally, an example of a simulation run is described using a typical load schedule, and the frequency response and total generation cost is recorded.

The parameters of each plant are pre-set via the keyboard before commencement of any simulation program run. Thus the plant parameters of the network detailed here together with certain characteristics can be produced to the users specific requirements for closer identification with the system concerned. The generating plant and load characteristics that can be preset by the user to simulate those of the system under study include: loading rates, governor droop, time constants, maximum/minimum limits.

7.1.1 Generators

Two steam turbine/generating units can be represented, each with its own displays, controls and characteristics. There is provision on the display panel for manually synchronising and tripping the generators. A generator's power output can also be pre-set on this panel and the value is indicated on the main display. The rate at which a generator is loaded and deloaded by a turbine driver is automatically simulated. A unit cost is allocated to each generator to represent the cost per MW at full load, Figure 7.1 illustrates a view of the panel.

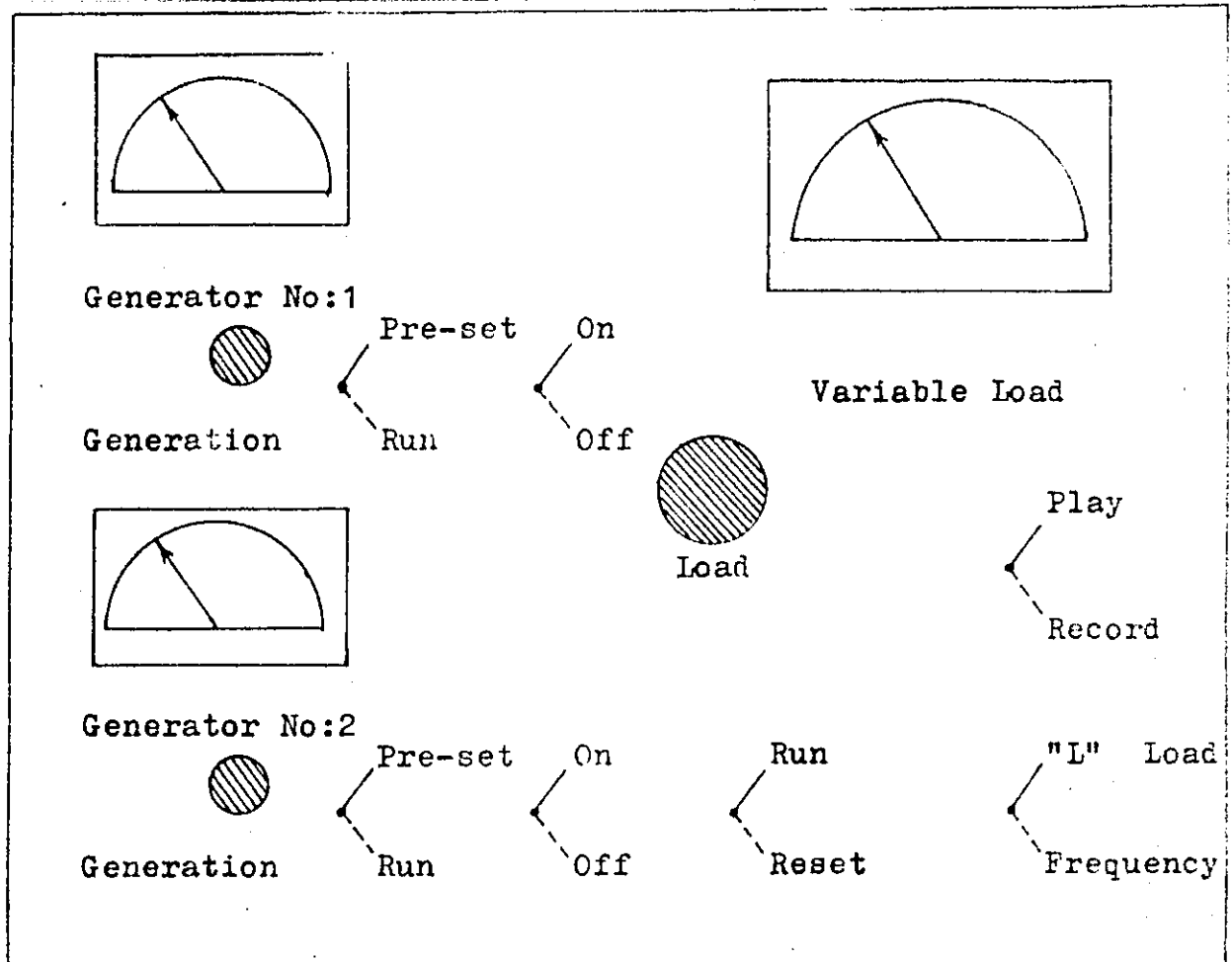


Figure: 7.1 Display Panel

7.1.2 Variable Load

A variable load is used to represent a changing load pattern. The load is continuously variable over its full range and is derived either manually or from a pre-recorded pattern.

The simulator can be operated in various modes and used for many purposes. Brief descriptions of some tests are given below as examples of possible applications.

7.2 Recording a Daily Load Curve

Daily load curves can have many different shapes. One example might be a sudden T.V. pick up at night following the ending of a popular program. A typical pattern is shown in Figure 7.2. In real life the jump might be as big as 150 MW in a short time, but considering the limitations in this digital simulator a more moderate jump is considered (see Figure 7.10 (a)). These load curves can be recorded on a magnetic cassette tape unit by switching the two switches on the panel to positions "Record" and "L", making appropriate scale settings on an X-Y plotter and then recording the load curve already

drown on a graph paper. The knob on the right-hand side of the panel will move the pen vertically in proportion to the load estimate. The X-axis is set to move four times faster than real time. The start of any recording should be synchronised with the zero of the time axis (both at recording and replay of the load curve) "Reset".

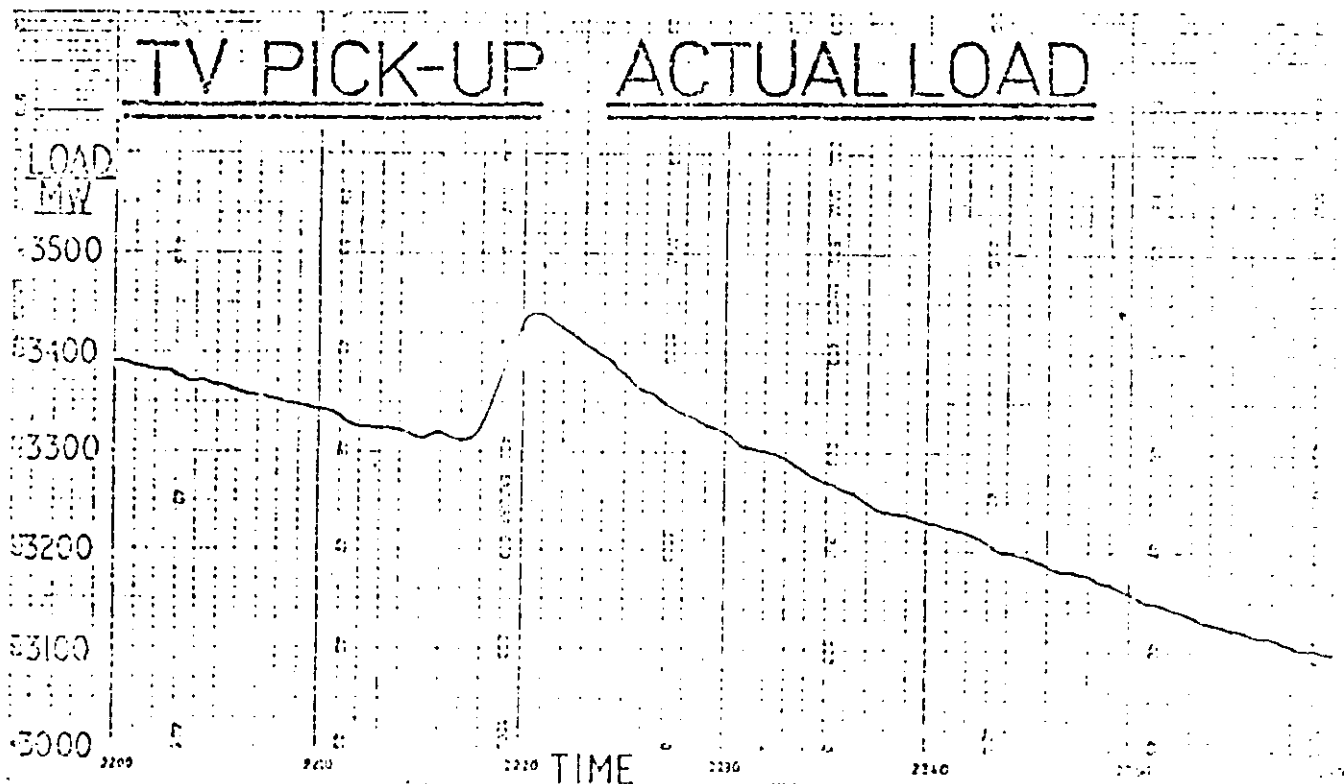


Figure 7.2 A typical daily load curve

7.3 Generator Scheduling

Simulator load scheduling forms have been devised on which different sets can be scheduled to meet the estimated load see Figure 7.11. Some deliberate errors can be introduced in this load estimate so that unexpected immediate action will be required to be taken during operation. The adjustments to prior estimates can be written in boxes provided on the forms (encircled) for future comparisons of optimum frequency control and operating cost.

7.4 Single Generator Response to Step Load

During the initial phase of program development a single generating unit connected to a load model was represented. To test the validity of the program model, comparisons can be made with results obtained from analogue simulation, as discussed on Chapter 2.

500MW
Running at 300MW



$\Delta P_L = 40\text{MW}$ (=8% of full Load)
 $P_L = 300\text{MW}$

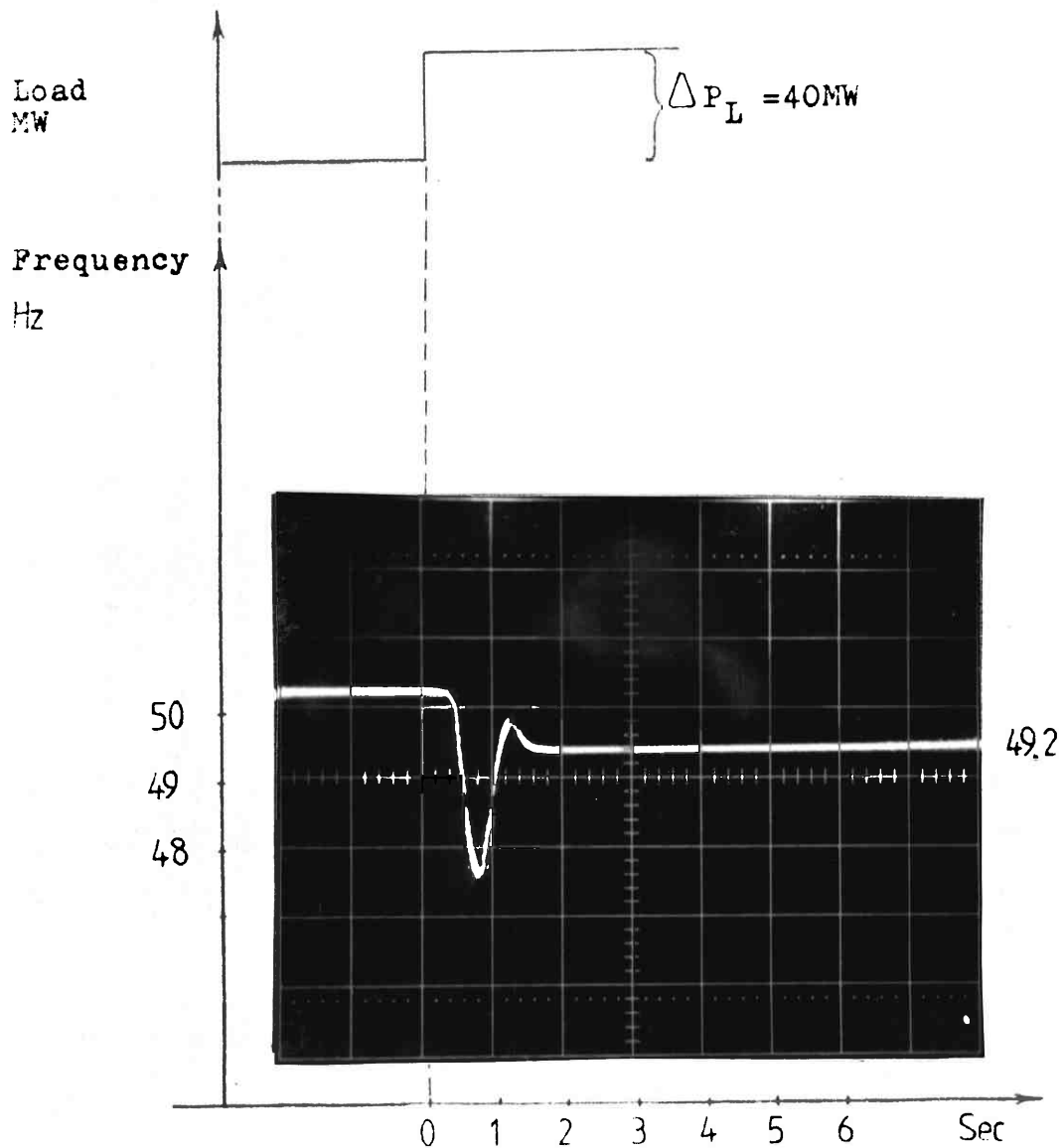


Figure 7.3 : Single Generator Response to ΔP_L of 8%

A position step load of 40MW was applied to a single set of 500MW when system was at steady state, for frequency response of this system refer to Figure 7.3.

As shown there is an initial delay of about 0.3s after the step is applied and frequency drops to about 47.3 Hz and settles to 49.2 Hz in about 1.7s, bearing in mind digital simulation is four times faster than real time. Now referring to analogue response on Figure 2.6;

For a 40MW step load and 6% droop characteristic,

- (i) There is no delay.
- (ii) Frequency over-shoot drops down to about 49.3 Hz.
- (iii) Frequency settles to about 49.7 Hz
- (iv) Settling time is about 35s (Note that Analogue simulation was in real time, therefore this value should be divided by four before it is compared with the settling time of Digital simulation).

Also theoretically it is possible to predict setting frequency of this response, there is a 6% governor droop and a change in load of 40MW which is 8% of the full load,

therefore $f = 0.08 * 0.06 = 0.0048$

which is : $0.0048 * 50 \text{ Hz} = 0.24 \text{ Hz}$

Now comparing this value with the one obtained by digital simulation yields that latter result is out by 0.56 Hz. Also comparing the two analogue and digital frequency responses it is evident that in digital simulation there is a far greater overshoot and a much smaller settling time and a more damped system. These inaccuracies are due to two major errors accruing in digital simulation. One is caused by the fact that number representation in an eight bit microprocessor is a great limitation causing quantisation error and secondly errors created during the integration process at a number of stages in the program. Since these errors are common in the following paragraphs as well, therefore for more elaborate explanation on these, please refer to Section 7.10.

7.5 Two-Generator Response to a Step Load

Further to above step input test a similar test was carried out with two generators connected to an infinite bus-bar and a step load increase of 40MW was applied, Figure 7.4 illustrates the consequent frequency response which can be compared with the case of single generator response of Figure 7.3.

As shown there is an initial delay of about 0.5s after the step is applied and frequency drops to about 47.3 Hz and settles to 49.2 Hz in about 2.8s (Note simulation time

is four times faster than real time).

But according to theoretical results settling frequency for this system would be calculated as follows ;

For a combinational droop characteristic of 6.8% and a load change of 40MW or 6.4% of the full load,

Initially system was at steady state,

500MW

Running at 230MW

120MW

Running at 80MW

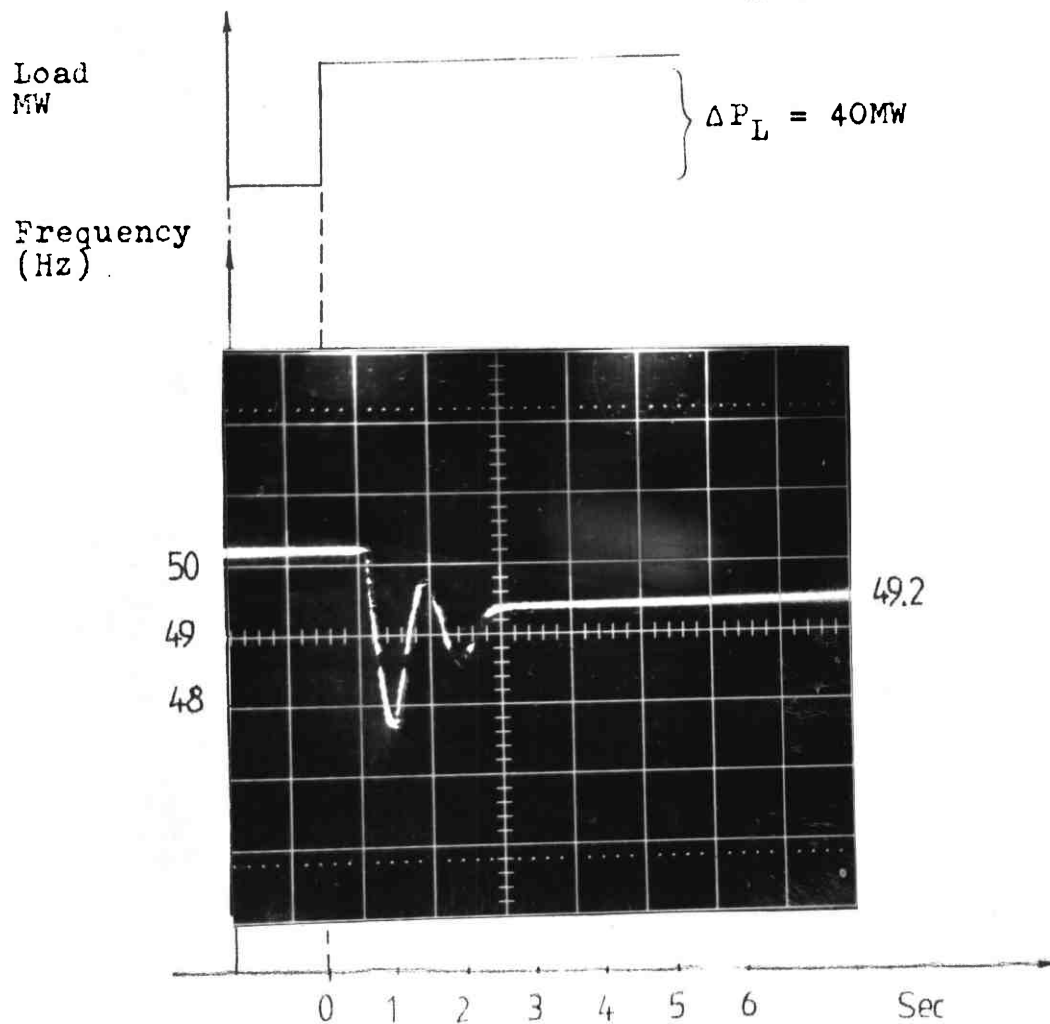
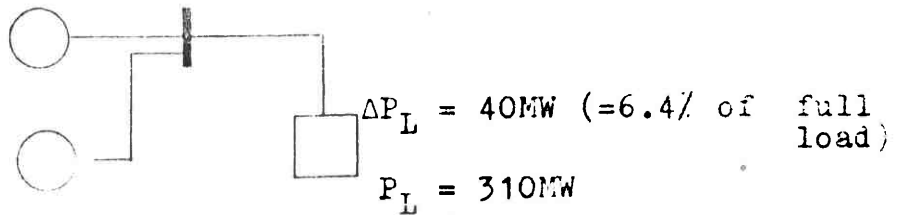


Figure 7.4 : Two Generator response to ΔP_L of 6.4%

then
which is

$$f = 0.064 * 0.068 = 0.0044$$

$$0.0044 * 50\text{Hz} = 0.22 \text{ Hz}$$

hence the settling frequency should be at 49.78 Hz.

Comparing these results with the ones in previous test would indicate that, because of the quantisation errors the difference in settling frequencies remains undetected in digital simulation, that is 49.78 and 49.76 Hz are represented with a single value of 49.2 Hz ($= (82)_{16}$). Also this system is more oscillatory or less damped, that is its closed loop poles are nearer to unstable region and this is what should have been expected since addition of an extra generator would result in a lengthier program cycle and hence a slower sampling rate.

7.6 Restoring System Frequency by Adjusting the Governor Set Point

In the case of the two machine/load simulation, the restoration of system frequency was tested by adjusting the governor set points. The addresses $(00F9)_{16}$ and $(00E9)_{16}$ are used as registers for the governor set points on the 500MW and 120MW generators respectively. By changing these values from the key-board the subsequent change of frequency can be produced and recorded as in Figure 7.5.

As illustrated on this Figure after the step load input was applied there is an initial delay of 0.5s which is followed by a smaller overshoot than in test 7.5 (Step input load response of two generators without gear setting) drooping only to 48.4 Hz and the settling frequency is restored to 50Hz. Similar response can be obtained in case of a single machine/load simulation, where frequency is restored to 50Hz but with a more damped response.

Figure 7.6 shows the value position for different speed errors and speeder gear settings.

Restoration of frequency is satisfied by pre-setting both gear settings at 0.37 p.u. (i.e. $(60)_{16}$ in Hexadecimal) and 0.44 p.u. (or $(70)_{16}$ in Hexadecimal) at addresses $(00F9)_{16}$ for generators No:1 and 2 respectively.

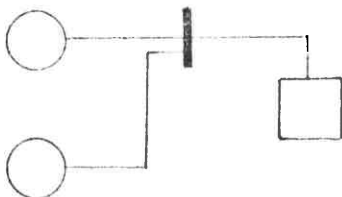
Initially system was at steady state.

500MW

Running at 230MW

120MW

Running at 80MW



$$\Delta P_L = 40\text{MW} (=6.4\% \text{ of full load})$$

$$P_L = 310\text{MW}$$

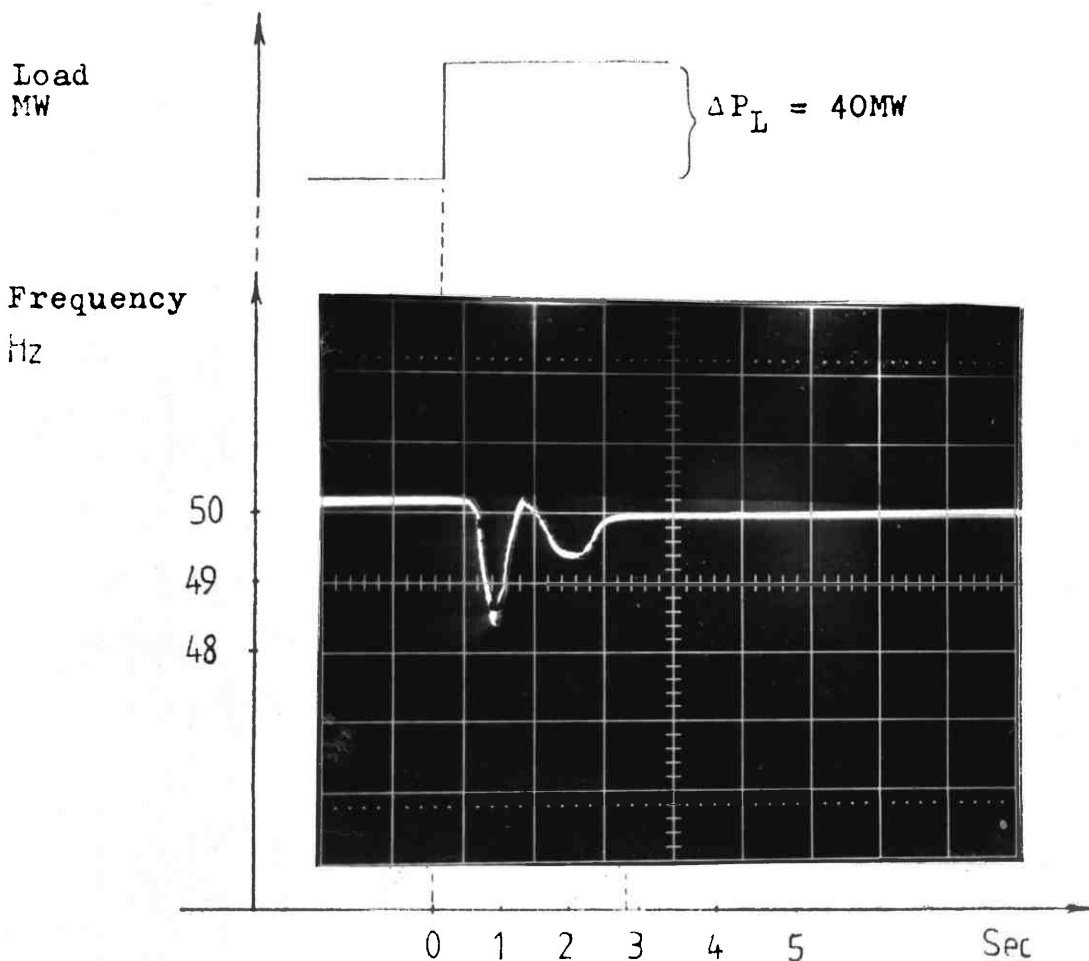


Figure 7.5 : Restoring System Frequency by Adjusting the Governor Set Point

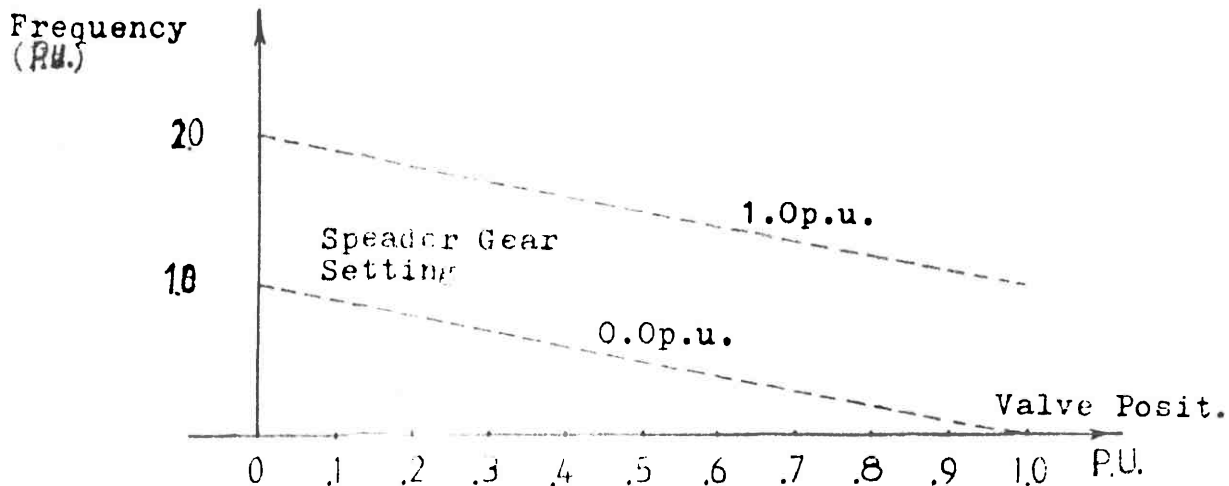


Figure 7.6 : Governor Droop Characteristic

These results can be compared with their calculated values, where frequency of system without any speeder gear setting would settle at 49.78, then a frequency error of 0.22 Hz would be multiplied by two different droop constant (i.e. $1/R$ where $R = 6\%$ & 12%) of 16 and 8 giving required governor settings of (0.43 p.u.) and (0.46 p.u.) respectively for generators No:1 and No:2. This test was also carried out in case of analogue simulation and a very close results to above theoretical values were obtained, the response is shown in Figure 2.6 (A).

Again above error is mainly due to quantisation error, where one of the major further improvements on this project would be to change the scaling of frequency variation in Figure 7.5 where frequencies out-side the limits of say 45 and 55 Hz are not used at all so limited 256 eight bit numbers (from $(00)_{16}$ to $(FF)_{16}$) could be assigned more effectively within those limits, hence more accurate representations could be achieved.

7.7 Variation of Droop Characteristic

In this particular test only one generator (i.e. 500MW) is considered with step input of (20MW), its droop constant (i.e. $1/R$) was halved and the subsequent change in frequency response were produced and recorded as in Figures 7.7 (a) & (b).

Figures 7.7(a) & (b) are both frequency responses to a step load variation of 20MW, both start with a delay of about 0.3s, but the settling frequency error in case (b) is halved as much as case (a) proving the point that frequency error is proportional to the value of Droop (R).

This is true both theoretically and it was tested in the analogue simulation which were represented in Figure 2.6, comparing curves B and D.

Still because of quantisation errors in the digital simulation the above point would not be true at all times, as load MW representations in digital numbers are not accurate enough and particularly with an eight bit machine there are big jumps in quantifying load by digital numbers. Also refer to paragraph 7.10.

7.8 Some Other Tests :

(i) Step load variation can be investigated by the results already achieved, referring to Figures 7.3 and 7.7 (b) it is evident that the frequency response settles with an error proportional to the magnitude of the applied step load. In these two tests, conditions are exactly similar, that is a single generator and a load of 310 MW connected when system was at steady state. Step loads of 40 MW and 20 MW were applied and hence twice as big a fre-

Initially system was at steady state,

500MW

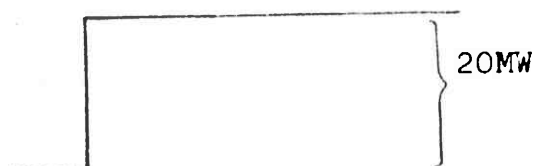
Running at 310MW



$\Delta P_L = 20\text{MW}$ (=8% of full load)

$P_L = 310\text{MW}$

ΔP_L MW
Load Variation



Frequency
(Hz)

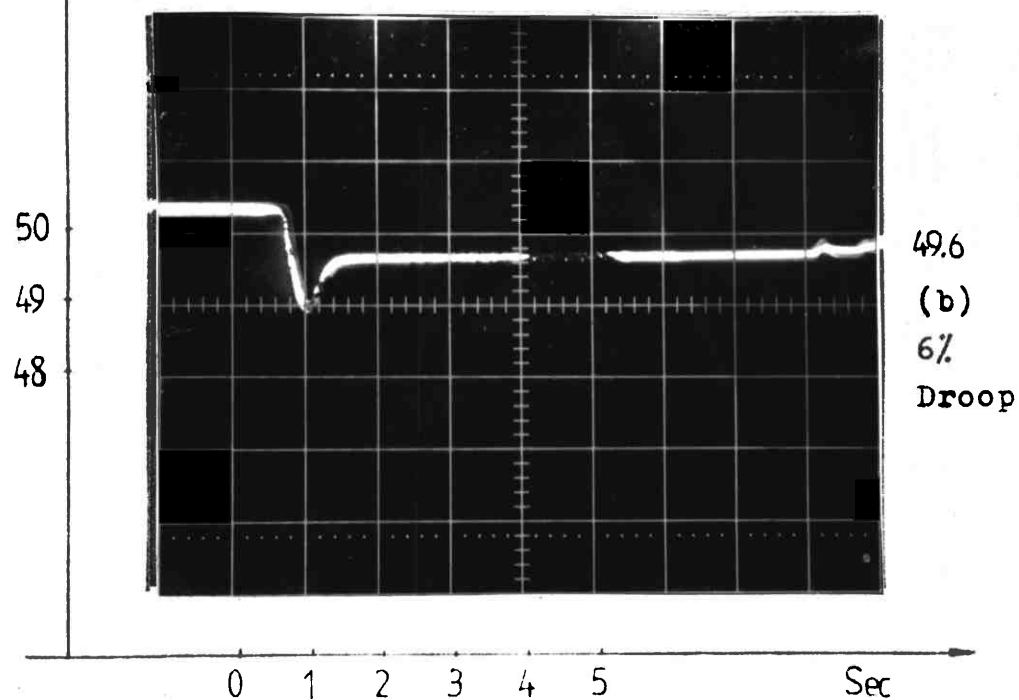
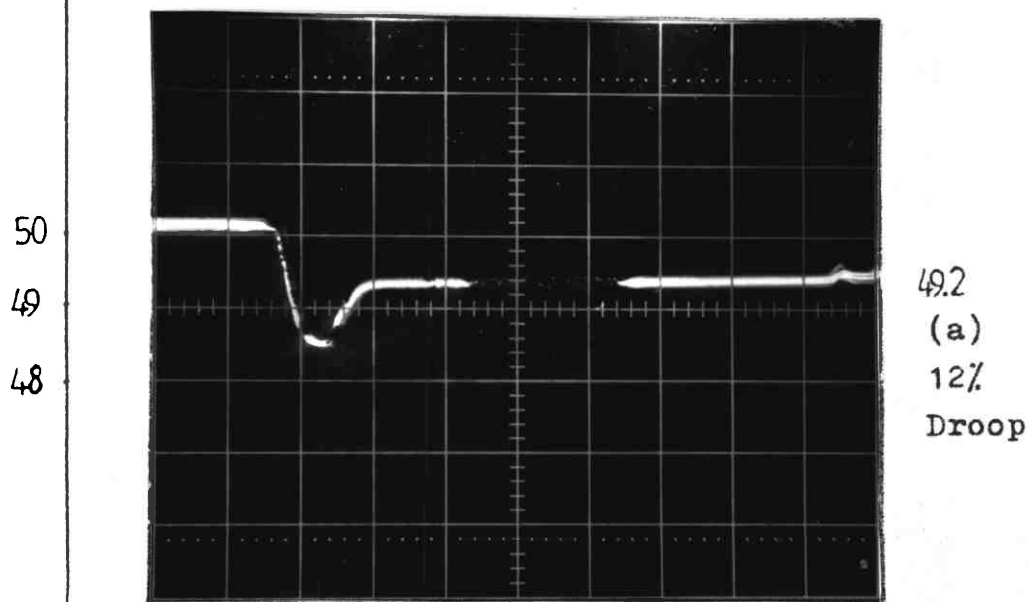


Figure 7.7: Variation of Droop Characteristic

quency error resulted in Figure 7.3. Also as expected with smaller step load, frequency overshoot is not as big as before and drops down to 48.5 Hz and settling time is almost the same, equal to 1.7s.

This is true theoretically and it was also verified in analogue simulation tests of Figure 2.6 cases (C) and (D). Where conditions were similar except for the step load input which was twice as big in case (D). Similar to digital simulation, there, frequency response error was proportional to step load size and in the same manner it was effected the frequency overshoot and finally had little effect on settling time.

Integration and quantisation errors do enable the digital simulation to respond consistently in all cases. Unfortunately as will be explained in Section 7.10 because of the non-linear nature of this system it is difficult to represent this in-consistency analytically.

(ii) Further tests could be performed to determine whether by a step up and step down input it would be possible to obtain the original frequency.

A position step load was applied to a system of a single generator and a load system at steady state. After the system frequency had settled to a value, this step was taken off and a response similar to Figure 7.8 was obtained;

500MW
Running at 310MW

$\Delta P_L = 20\text{MW}$
 $P_L = 310\text{MW}$

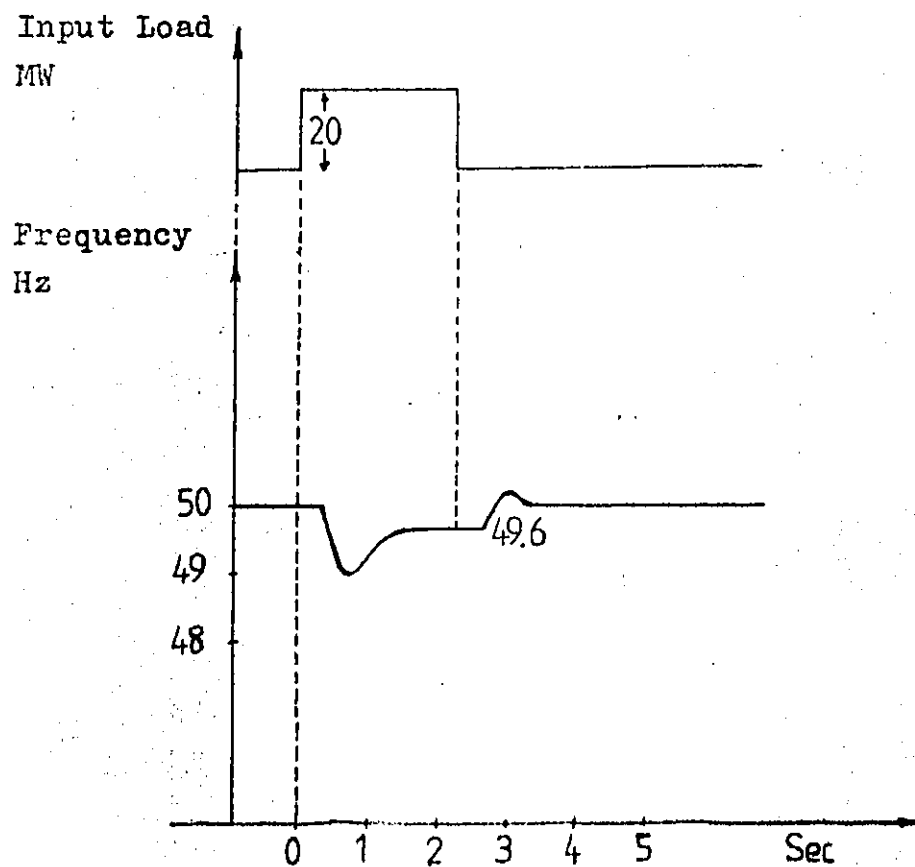


Figure 7.8 : Step in and Step off Response

The first stage of this response is similar to previous tests and when this step was taken off, the frequency response after a small overshoot settles at 50 Hz.

In the second stage of this test a negative step follows the positive step, and the subsequent change on frequency response was produced and recorded as in Figure 7.9.

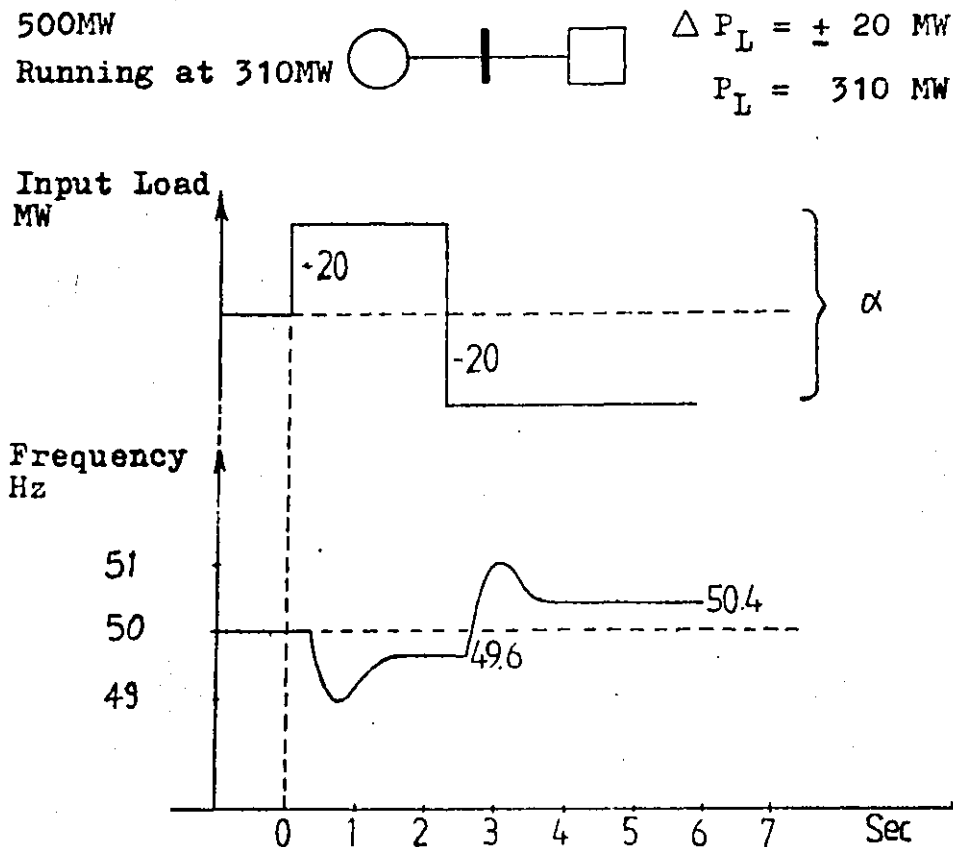


Figure 7.9: Positive and Negative Step Input Response

In this response, the settling frequency obtained after the negative step, is what would have been achieved if a negative step was applied after a steady state condition. A limitation on size of the step level difference "X" (refer to Figure 7.9) exists. It is found by experiment that this is equal to 48MW and if this limit is exceeded then "Reset" action would take place.

(iii) Finally it was essential to investigate the magnitude range of P1 and clarify when it is too large or too small. As previously mentioned in Chapter 6 all blocks performing integrations or first order lags would increment or decrement their output, by a fraction of their input value. For instance the first block representing inertia of the system (see Figure 6.7 or 2.4) would take one quarter of the error signal (with respect

to reference level of $(80)_{16}$) therefore signals in the range $(7D)_{16}$ to $(83)_{16}$ would be unnoticed by this block and this corresponds to about 6MW of load variation from steady state. Also there is an upper limit to step load input when it is too large and the program would go into a "Reset" routine, this was tested to be about 40MW of step load change from steady state condition.

7.9 Recording the Frequency and Cost Variations

This section describes how the digital simulator would be used in normal application of power system simulation, that is meeting a daily load curve with appropriate generation and hence recording system frequency and cost of running the generators. For this purpose two sheets have been prepared. One is placed on the X-Y plotter for recording the daily load curve, system frequency and operational cost, Figure 7.10. The second sheet is given to the operator to schedule generators at different instants of time to meet the estimated load, Figure 7.11. For more realistic simulation of operating conditions, certain scheduling restrictions have to be observed before ordering a change of generation and these are stated at the bottom of this sheet. The two generators have different characteristics and costing rates. Thus, to meet a load, the set i.e. (120MW) should be used as little as possible since its generating costs are higher but at the same time the system should have some spare generation available. Also the software in the microprocessor is written in such a way that the operator could synchronise a set when necessary during operation, but it is assumed that a least one generator is on-line at all times.

A typical simulation run is shown in Figures 7.10 and 7.11. First, the supervisor will record a load curve on a magnetic tape as described in Section 7.2 and provide the student with a similar curve which serves as a load estimate. From this curve, the student prepares his first Generation loading schedule with the basic consideration being to meet the expected load at minimum cost. The tape is replayed and the program is run. With the aid of a clock (or the time scale on X-axis) the student loads the plant according to his schedule. Minor changes will be implemented to account for the deliberate errors introduced in the estimate. The student now learns to anticipate power requirements, maintain a steady frequency, and log his actions. The supervisor gives advice as the program progresses and notes events of interest for later discussion. On completion an overall summary of performance is made, backed up by hard-copy results of-system frequency and cost, recorded on the chart recorder. The next step is to repeat the same load curve with the aim of improving the results or to advance to a new load curve of a more challenging nature. At present the possibilities are limited as only two generators are available and usually gas turbines are needed for fast recovery of generation at critical situations.

From Figures 7.10 and 7.11, it can be deduced that when the input load varies rapidly the operator is less likely to follow the estimated load with an equal amount of generation, hence any short fall or excessive generation will result in the frequency response falling below or exceeding its nominal value of 50Hz respectively. Any change in timing or amount of plant ordering with respect to estimated values could be written on the same loading schedule sheet for further discussions and comparisons at the end of simulation time. Also, contrary to what is expected from an analogue simulation, the frequency of response in this digital simulation is contaminated with noise which will be explained in paragraph 7.10. As is shown, cost of operation could also be recorded and by considering the different cost units allocated to each generator, at time 22.20 (Figure 7.10) where it has to meet the peak load, the cost would be at its maximum value.

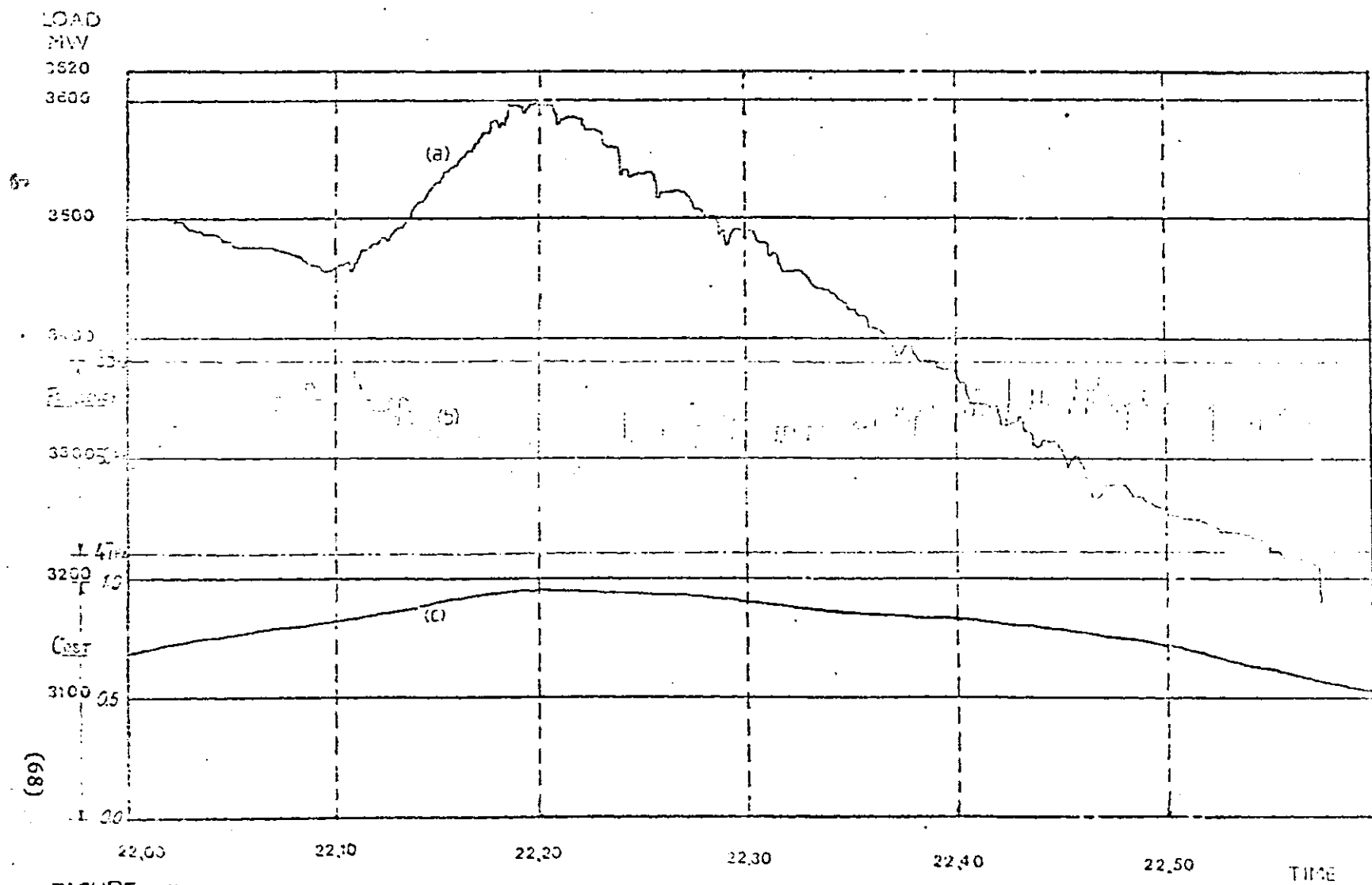


FIGURE: 7.10

SIMULATOR LOADING SCHEDULE

TIME	22.00	22.10	22.20	22.30	22.40	22.50	23.00				
ESTIMATED LOAD	5500	5450	5600	5480	5570	5250	5200				

TIME	22.00	22.10	22.20	22.30	22.40	22.50	23.00				
BASE GENERATION	5000	5000	5000	5000	5000	5000	5000				
GENERATOR NO: 1	450	450	450-100	550-100	250-100	150-500	100				
GENERATOR NO: 2	70-25	95-25	120	120	120	120-25	05				
TOTAL GENERATION	5520-25	5545-25	5570-100	5470-100	5370-100	5270	5100				

GENERATOR DETAILS

	1	2
RATED OUTPUT	500 MW	120 MW
UNIT COST	0.2	1.0
GOVERNOR RESPONSE	6%	12%
LOAD/DELOAD RATE	10MW/MIN	2.5MW/MIN

Scheduling Restrictions for Realistic Simulation of Operating Conditions

1. Minimum time between instructions to individual Generators:-
 - (a) 10 minutes, when the changes required are in the same direction.
 - (b) 20 minutes, when the changes required are in opposite directions.
2. Synchronization of Generators must be ordered on the schedule and implemented at that time.
3. Minimum Generator loading 4% of rated output.

FIG. 7.11

As was mentioned in Section 6.7.2 a sleeve limiter was introduced at the output of system frequency, which would consequently create certain boundary levels, where it limited the system frequency deviation to 47 and 53Hz. Also it was mentioned that if these boundaries were exceeded the program will move to a "Reset" routine to resume another run, and would continue until some action is taken by the operator to match load with equal generation (i.e. step error input is too large see Figure 7.12).

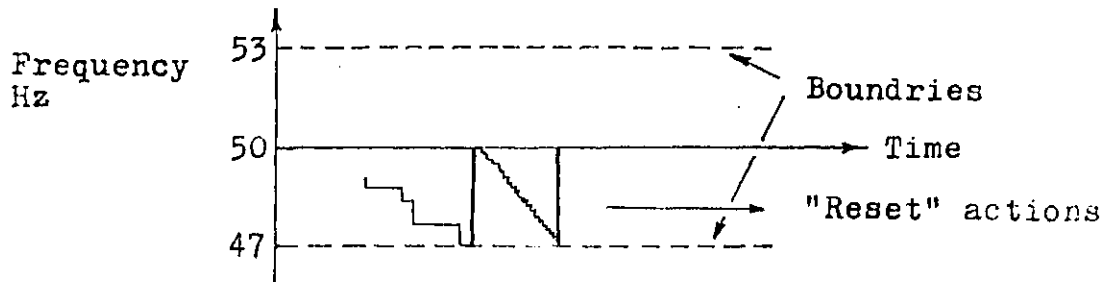


Figure 7.12 Step error input is too large

7.10 Comments

In this Section some tests were carried out with the digital simulator and as mentioned there are inaccuracies which have to be discussed. The following table and comments summarizes some of these defects.

MW Step Load	Digital Representation of Step Load	Simulated Frequency Response	Frequency Representation -ation Simulated	Calculated Frequency Vary Between
Less than 6MW	From (00) ₁₆ to (03) ₁₆	50Hz	(80) ₁₆	50-49.96Hz
Between 8 to 34MW	(04) ₁₆ to (11) ₁₆	49.6Hz	(81) ₁₆	49.96-49.82Hz
Between 36 to 48MW	(12) ₁₆ to (18) ₁₆	49.2Hz	(82) ₁₆	49.82-49.71Hz
More than 48 MW	Greater than (19) ₁₆	"Reset" to 50Hz	"Reset" to (80) ₁₆	

The above table shows that, if say step load changes from 8 to 34 MW were made this

system would only have one level of simulated frequency representation of 49.6Hz, where-as calculated frequency would vary from 49.96 to 49.82 Hz.

In general there are two sources of errors in the software program: Firstly as there is a limited 256 numbers to represent load and etc., some values cann't be represented exactly which then creates what is known as quantisation error. Secondly as for every block of integration or first order lag a division by 2,4 or 8 is carried out, errors would be generated when these divisions are not exact. Figure 7.13 illustrates such sources of errors.

Owing to the finite word-length of the microprocessor, the quantisation of the input signal and that of accumulated outputs at different locations of the simulated control system, then round off or transition noise will be present. The round off noise error has always been a source of error for any digital signal processing system. This has been widely studied by many authors for a variety of digital processing systems, see References 10 and 11.

In the simulated control system no rounding was performed, so all the existing noises due to the finite word-length arithmetic were truncation noise. As shown in Figure 7.13 for a single generator system seven different truncation noise errors exist;

i) e_1 ; this is the truncation noise due to the finite representation of the sampled input signal. It is a constant distributed variable in the range of (-1 to 0), i.e. it has a mean value of -0.5 and variance of $1/12$.

ii) e_2 ; this is the truncation noise due to the division by 4 in the inertia block. It is a stochastic variable which takes four distinct values of 0.0, -0.25, -0.5 and -0.75, each having the probability of 25%.

iii) e_7 ; This is the truncation noise due to the division by 2 in the governor model. It is a stochastic variable which takes two distinct values of 0.0, -0.5 each having the probability of 50%.

iv) e_9 ; This is the truncation noise due to the division by 4 in the high pressure stage of the turbine model. It is a stochastic variable which takes four distinct values of 0.0, 0.25, 0.5, 0.75 each having the probability of 25%.

v) e_{13} : This is the truncation noise due to the division by 8 in the low pressure stage of turbine model. It is a stochastic variable which takes eight distinct values of 0.0, -0.125, -0.25, -0.375, -0.5, -0.625, -0.75, -0.875 each having the probability of 12.5% .

VI) e11 : This is truncation noise due to the division by 4 in the turbine model. It is a stochastic variable which takes two distinct values of 0.0 and 0.5 each having the probability of 50%.

(Viii) e12 : Finally this is truncation noise due to the division by 4 and 2 (where $\frac{1}{4} + \frac{1}{2} = \frac{3}{4}$) in the turbine model. It is a stochastic variable which takes six distinct values of following table with their probability as shown;

0.0	0.25	0.5	0.75	1.0	1.25
12.5%	12.5%	25%	25%	12.5%	12.5%

These additive noises are combined together which would result an additive noise at the output of the system, as is evident from the frequency response of the system in Figure 7.1 This simulated digital control system has a sort of non-linear nature which makes the analysis of the truncation noise error quite difficult. However, the experimental results are quite instructive. From 7.10, it can be seen that when the input load decreases slowly the output frequency will increase where load and generation are not exactly equal and also it is contaminated with less additive noise. On the other hand when the input load decreases with a larger slope, more visible additive noise is observed. So, from these observations, it might be concluded that when input load varies slowly, the system is able to follow these variations and the resulting additive arithmetic noise is less. When the input varies faster, although the system follows these variations, the additive arithmetic noise is fairly large. The latter is found to be due to the large transition time of the negative feedback loop which produces on accumulative behaviour. When the input load varies slowly the truncation noises are cancelled out by the feedback nature of the loop prior to any introduction of a new truncation noise sample.

As discussed before in Section 7.9, when the input load varies rapidly the operator is less likely to follow the load with exactly equal generation. So, in this case, it is more likely to have large input error step which consequently increases the deviation of the output frequency from its nominal level of 50Hz. The instabilities occur if this deviation goes beyond some known boundaries (see Figure 7.12). But these arguments should be even more modified in the presence of noise. As was mentioned above, the additive arithmetic noise increases variation of the system output frequency. This reduces the safety boundaries as illustrated in Figure 7.12.

From Figure 7.14 it is clear that any further deviation of the nominal output frequency from new boundaries may result in instability as the nominal output frequency plus the arithmetic noise can be at a point outside the original boundaries.

Therefore, from the above discussions, it might be concluded that the digital simulator is less stable than its dual analogue simulator system.

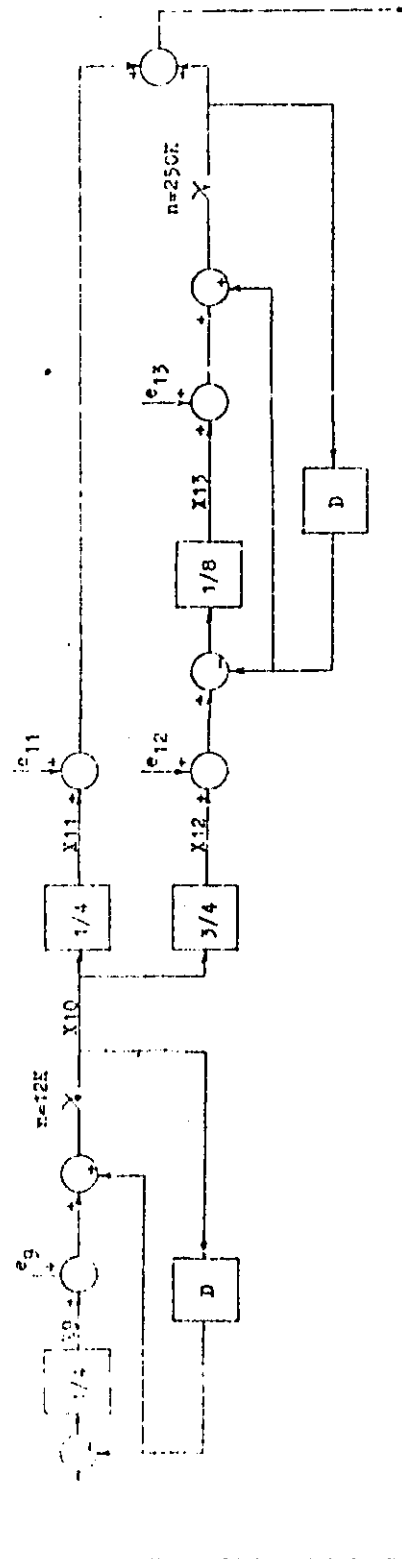
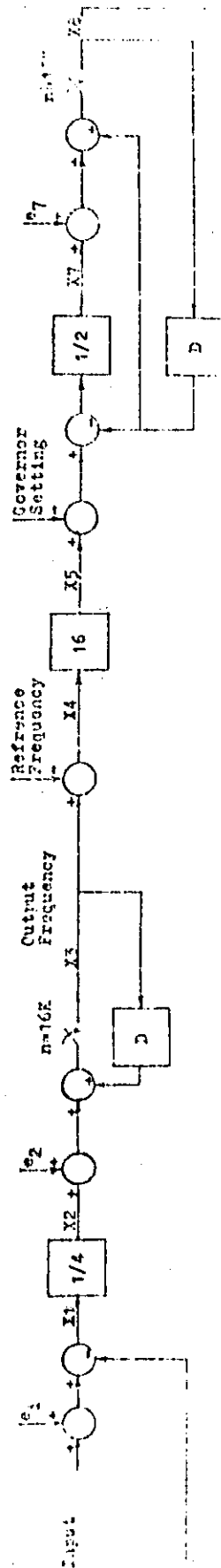


Figure 1.12 : Sources of noises in a single generator system

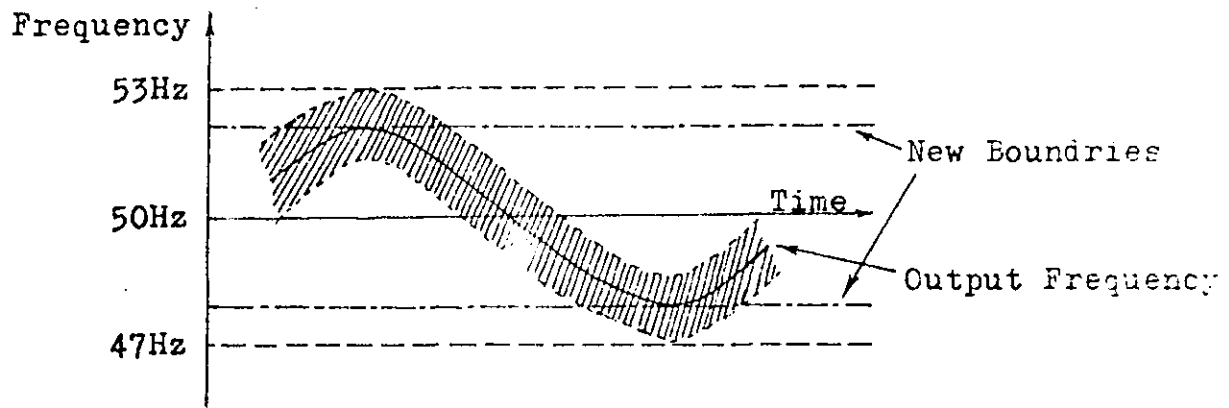


Figure 7.14: Noise Effect on Frequency Boundaries

However, this deviation may be reduced by using microprocessors with longer word-lengths. It should also be added that rounding rather than truncation will result in better digital system performance.

CHAPTER 8

CONCLUSIONS

8.1 General Comments

The simulation of the model in analogue form was described in Chapter 2. This was necessary for comparison and validation of results from the digital simulation. In Chapter 3 a related project was described inter-linking parallel microprocessors, each performing a different task. Chapter 4 explained in more specific terms the use of a Motorola 6800 microprocessor in a small digital simulator. Chapters 5 and 6 then presented an account of the hardware and software organization used for simulation. And finally some test results together with a simulation run were presented in chapter 7.

In general the step load frequency response of the system, whether in an analogue or digital form of simulation, has resulted a frequency variation as shown in Figure 8.1, where range A to B covered the first second (or 4s in real time) following a generation trip. The parameters of importance during the initial transient are, size of generation deficit, system inertia, governor gain and the time constants of the governor and high pressure value. The magnitude of the frequency excursion is decided by what rectification action the plant can provide i.e. longer time constants and smaller governor gains slow down the generating plant response causing a large frequency drop. In range B to C the rate of recovery from the initial frequency fall depends upon how quickly the generation deficit can be restored, the two halves of the generation-load balance are both involved. The generation pick up is still largely controlled by governor gain and plant mix. From C onwards it remains steady. The magnitude of the plateau is almost totally dependent upon the governor droop characteristic.

As a discussion for using assembly language rather than a high level language, it should be emphasized that in real time processing and control (like the simulation explained here) generally involved are high-speed analysis and reaction to random inputs, coordination of correlated functions being performed simultaneously, and detailed control of external devices. And assembly language is the most commonly used level of computer language for microprocessor control and real-time applications due to

- a) In contrast to machine language, it provides a balance between readability and capability to control computer functions.
- b) In contrast to high-level language, it generally executes faster, and it requires less memory space. So at the start of this project since the power system section had already applied for a grant to purchase an expensive developing system, to save time before the grant was approved it was decided to get a relatively cheap

microcomputer kit and commence the modelling of a very small power simulator and use the already available 6800 Motorola cross assembler at Imperial college computer center.

Digital simulation as presented in this project, has inherent a number of inaccuracies and limitations. Sources of these may be briefly summerised as, firstly the simplified power system model chosen and secondly the inaccuracies which have arisen from the fact that data handling is limited to a work-length of eight bits, although there are some ways of over-coming this by considering data as a 16 bit word-length and employing two registers in storing half in one and the other half eight bits of information in the other, say ;

Data :	<u>XXXX</u>	<u>XXXX</u>	<u>XXXX</u>	<u>XXXX</u>	Data Information
	Stored in		Stored in		Varies from
	Accumulator A		Accumulator B		0000 to FFFF

but this method would be more tedious from a programming point of view and would obviously use more instructions and take longer to computer.

Also the programming method which was described in this project works in an inherent fashion, (for simplified explanation see Figure 8.2) where outputs of blocks 1 and 2 will not be updated unless the program makes n1 and n2 complete cycles respectively where n1 and n2 depend on the delays required by each block before they could increase or decrease output to a new value. It is possible to make use of interrupts after some internals and at each interrupt, output of a certain block is up-dated to a new value. In that case the advantage would be that delay time is independent of programcycle, but this method could be slower from a computing point of view.

So the theme of the thesis has been the use of the inherent solution of equations in important areas of a power system simulator, namely, generator model, governor model, reheated turbine model, combined response of generators, generation cost and generator synchronisation. Although only two generating units were represented in this study, the program structure is written in a generalised form to handle any number of generators.

Each complete execution cycle of the program takes about 16 ms with two generators running, which compares with a reduced time of 13.6 ms for a single generator. For this inherent programing method it is difficult to state the maximum number of generators that could be represented, but knowing the time taken for each generator unit (=2.4 ms) it was possible to add a delay loop at the end of the program to represent an extension to 6 generators. The step responses were tested and it is possible to extend the number

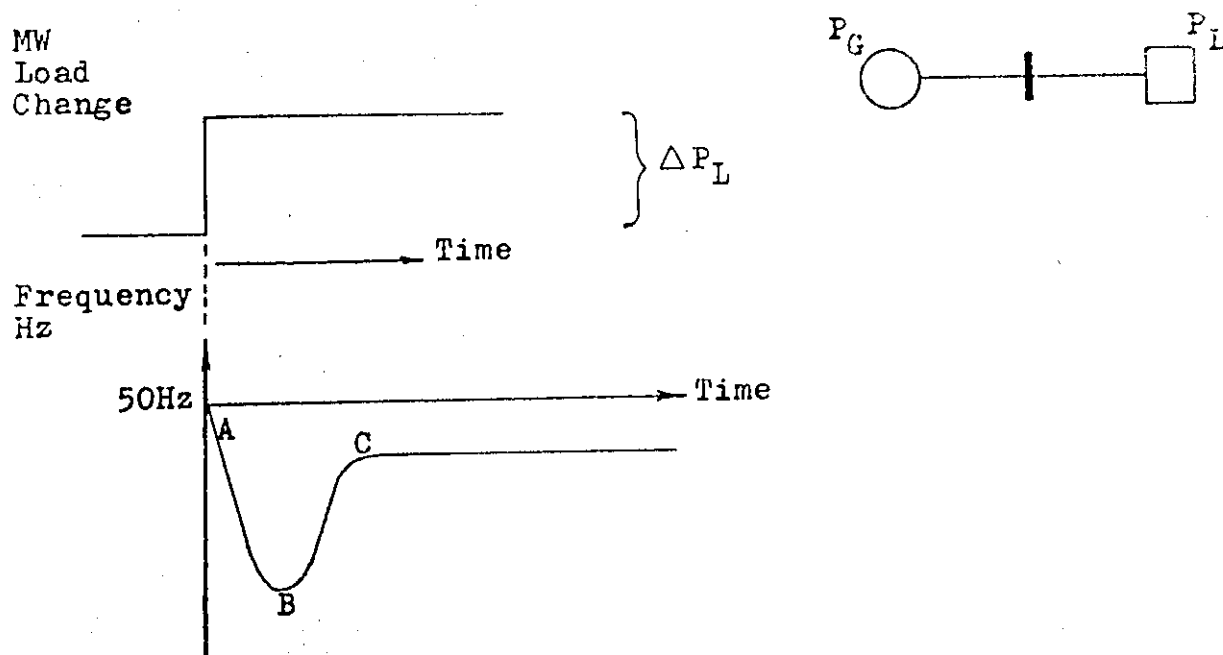


Figure 8.1 General Step Response

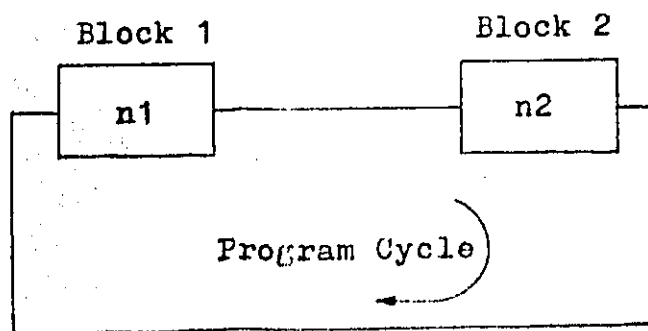


Figure 8.2 Inherent Programming

generators to match the size of C.E.G.B. mini-analogue simulator.

Priority should be given to eliminate errors and truncation noises described in chapter 7. These can be improved by ;

- (i) making a slight change in the method used for simulating first order lag blocks of ;

$$\left(\frac{1}{1 + ST} \right)$$

and briefly this means, instead of having variable steps of incrementation as used here:

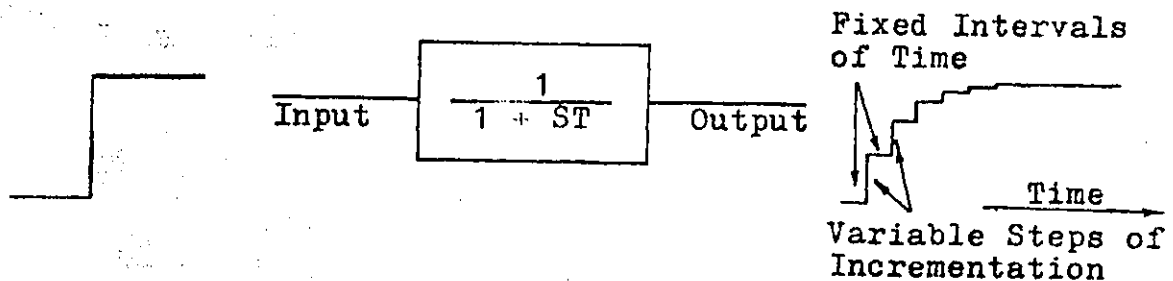


Figure: 8.3 Method used

it is more accurate to use fixed steps of incrementation but variable time internals as shown in Figure 8.4 ;

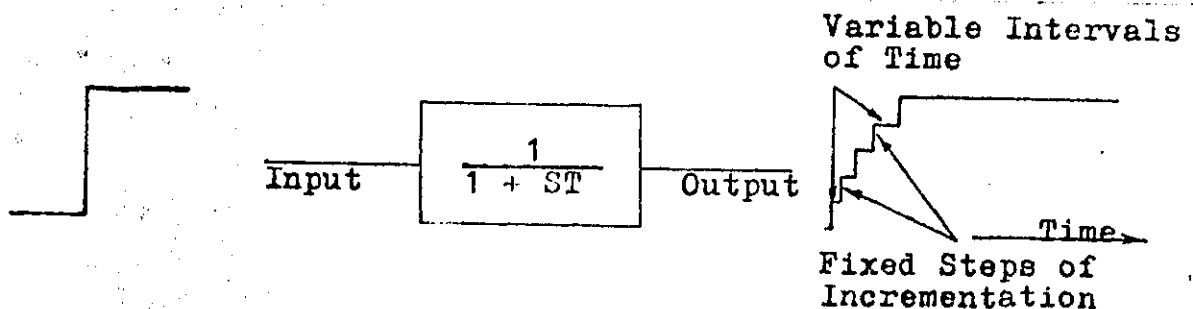
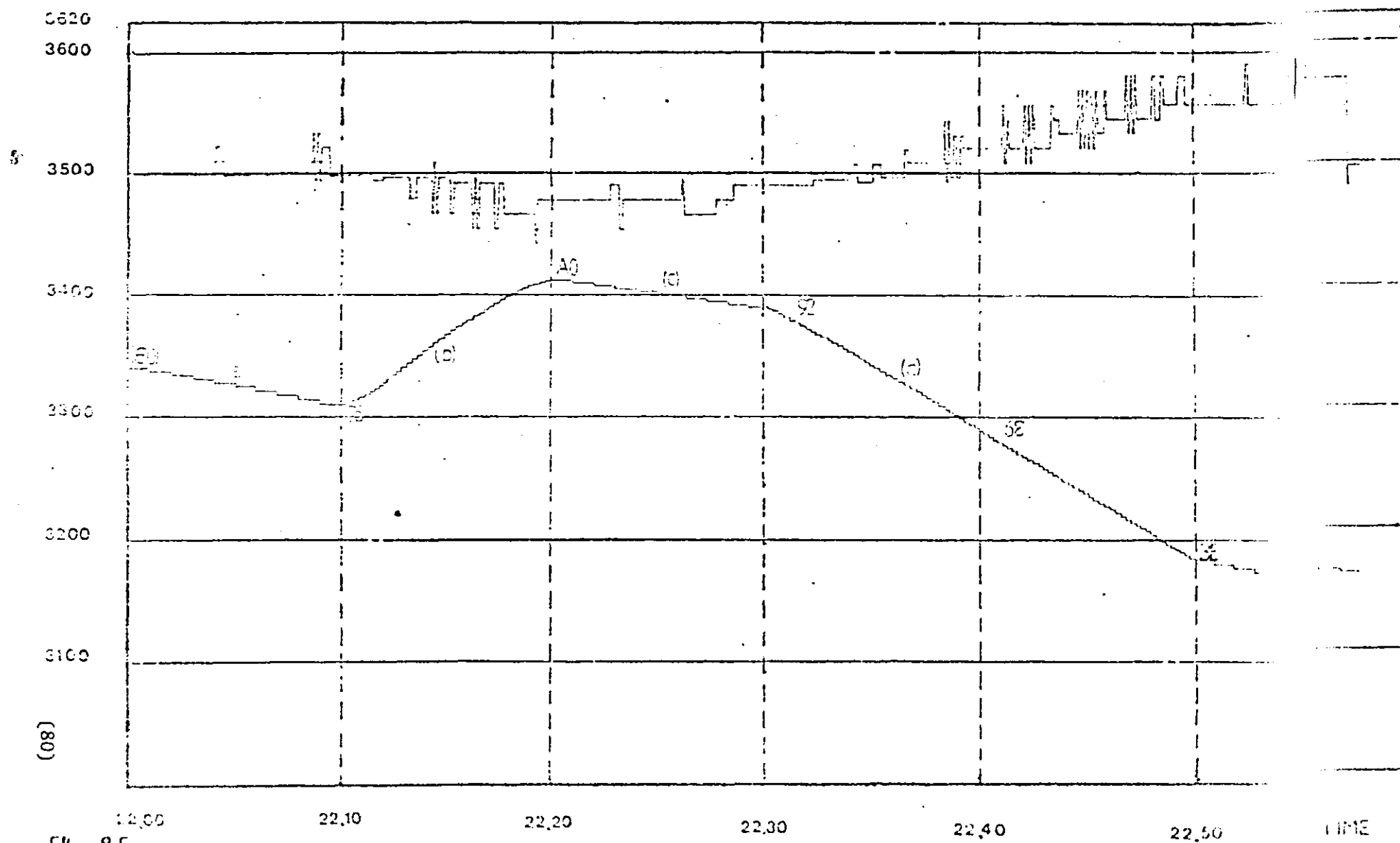


Figure : 8.4 Method Recommended

This error is particularly observed at the moment, when a generator is ordered to reach a target generation so in the early steps of incrementation large steps of generation will be produced, which is a source of error, Figure 8.3.

- (ii) A simulation of the system was run with a daily load input stored not on the magnetic tape but digitally on the microcomputer's RAM. That is, different points of this curve were quantised exactly by hexa-decimal numbers and they were stored at different addresses. As expected a less noisier frequency response was achieved but because of truncation the response was still not free of noise. Figure 8.5 illustrates such a res-

LOAD
MW
3620
3600



ponse. Note that with this simulation only zero time load of 3330 MW was matched and in the following instants, generation was kept constant at 3330MW. Also it is evident that as the variation of the step load become larger, the amount of noise becomes more visible. Comparing the frequency response of this system at regions (a), (b), (c) and (d) proves the above point as regions (a) and (c) with smaller variations in load produce a response with less noise.

(iii) To make frequency response less noisier it is better to introduce rounding off rather than truncation as is done in this project.

(IV) In recent months Motorola has introduced an up-graded version of their eight bit microprocessor (MC6809) which can handle 16 bits of data hence a more accurate data manipulation could be achieved.

Finally, the original contribution in this project is the software program which is written for a mini-digital simulator in assembly language.

8.2 Suggestions For Further Work

The work reported in this thesis has aimed at developing a simple dynamic power system simulator which only deals with real power and frequency variations. Although the simulator has not reached an entirely satisfactory state, it is felt that an insight into the problems has been achieved, there-by making it easier to approach a closer representation of an actual system. In addition to what has been recommended to reduce the level of noise and error in the present digital system there are some further suggestions for further development :

(1) Addition of different generator sets with different characteristics say; 30MW, 60MW and so on, which would make the system simulation more flexible and capable of handling almost any type of typical daily load curve.

(2) Addition of a number of gas turbines or pumped storage plants which have a governor free response and are very useful in recovery of sudden frequency fall.

(3) The use of a double trace X-Y recorder so that frequency and cost variations could be recorded simultaneously.

(4) Adding an option for coupling to a second section of a network; an arrangement for creating a generation/load imbalance in order to facilitate power transfer.

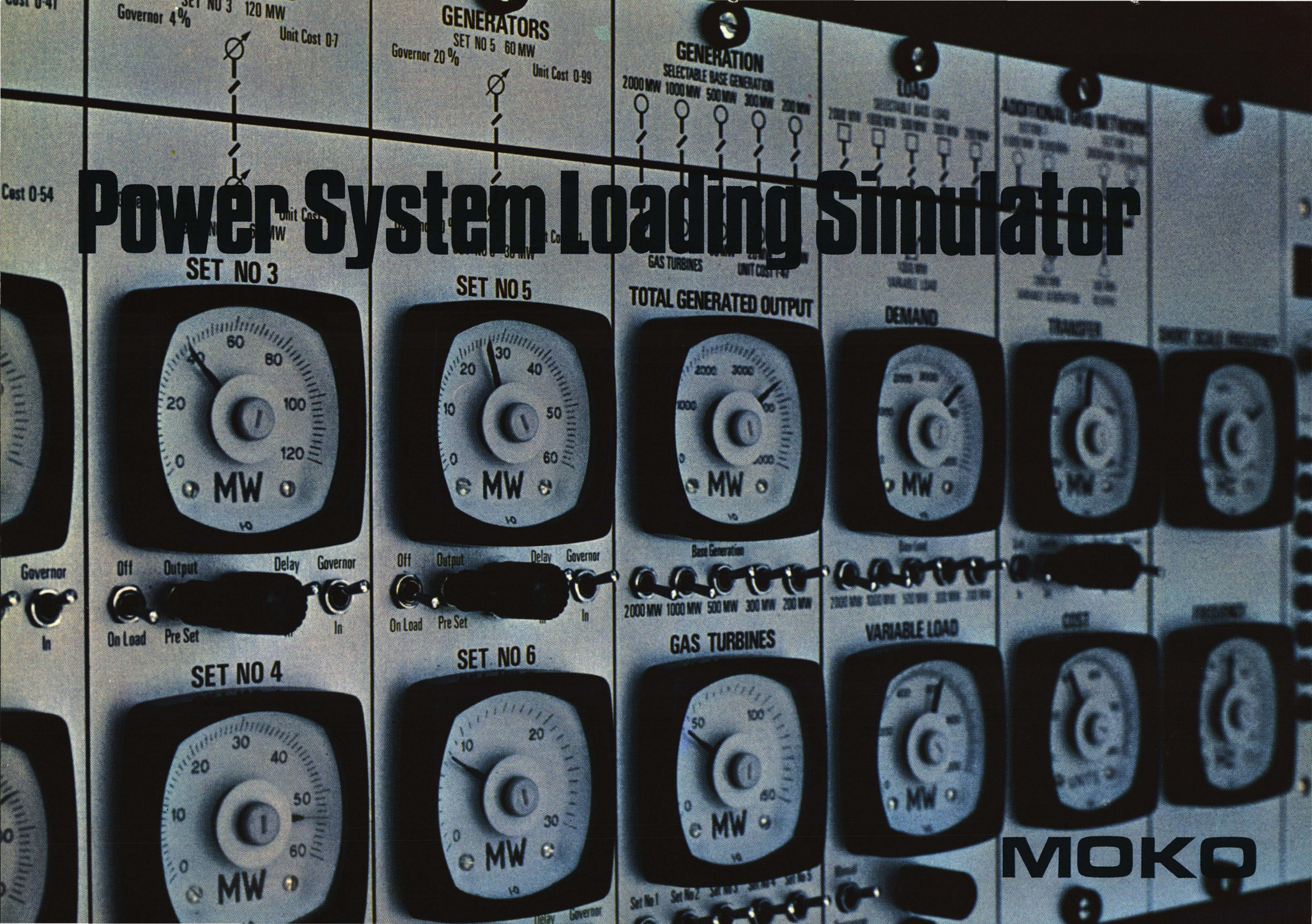
(5) For larger power system simulators there are newly presented multiple micropro-

large mainframe digital computers and are available at a fraction of cost.

APPENDIX : A

"C.E.G.B Mini-analog Training Simulator"

Power System Loading Simulator



MOKO

SYSTEM REPRESENTED BY SIMULATOR

The plant parameters of the network detailed below together with certain characteristics are produced to the customers' specific requirements for closer identification with the system concerned.

GENERATORS Six sets constitute the active Steam Generation of the Primary System, they have individual displays, controls and characteristics. Facilities include arrangements for synchronising and tripping the Generators manually, a choice of running with or without a Governor Response Characteristic and an option of responses associated with time functions.

Controls enable a Generator's output to be pre-set and the value indicated on the main display. The rate at which a Generator is loaded and unloaded by a Turbine Driver is automatically simulated by the equipment.

Built in Boiler response characteristics include Boiler Lag, Boiler Droop, Automatic Boiler Firing, Low Frequency Auxiliary Failure and Over Pressure Steam Release. Simulation of an operator's action to prevent combustion instability at low levels of generation is provided by an automatic shutdown feature.

The Unit Cost allocated to each Generator represents the cost per MW at full load. This is made up of two components, a no load constant when the Generator is synchronised and an incremental cost proportional to the generated output.

BASE GENERATION represents high merit plant required to operate at full load throughout a period of simulation. Five blocks differing in capacity are available for connection to the system in various combinations.

The output is reduced when the Frequency rises above the standard operating value, simulating overspeed governor response, also after an appropriate delay at very low system speeds simulating auxiliary feed failure.

GAS TURBINES Five units are provided with a built in start up delay and have automatic loading and deloading facilities. Cost levels operate as a direct function of MW output.

VARIABLE LOAD is used to represent the changing load pattern, it is continuously variable over its range and derived either manually or from a pre-recorded programme.

The effect of frequency variations on the magnitude of load is simulated by a fixed characteristic and operates over the entire frequency range.

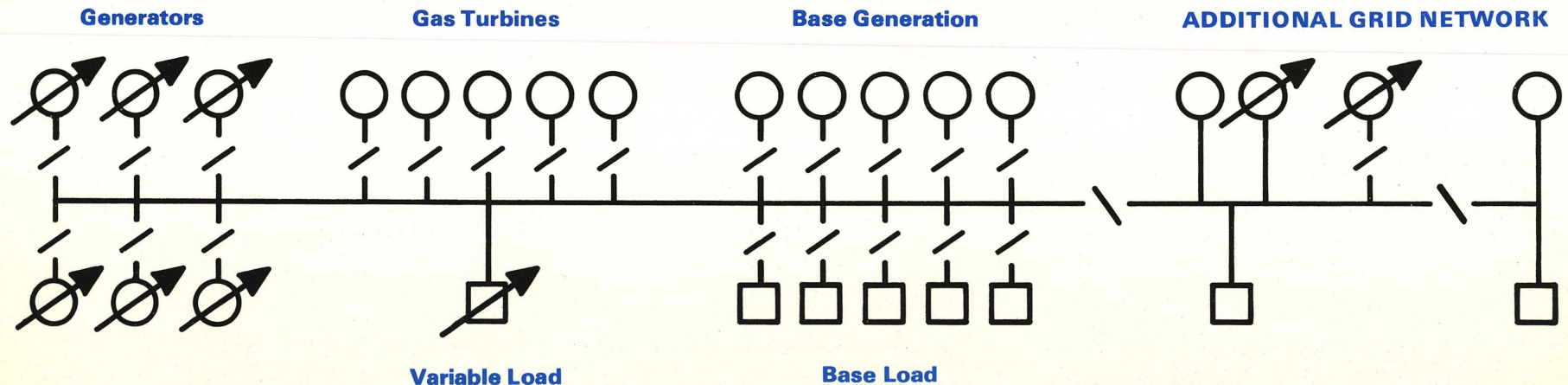
BASE LOAD Selectable blocks of load with a frequency dependant characteristic are available for connection to the system. These compliment Base Generation in magnitude and can be connected in the same way.

ADDITIONAL GRID NETWORK is designed to operate in conjunction with the Primary Network and can be of comparable size or larger.

Representing a complete multi-generator network it operates automatically, simulating the combined effects of machine characteristics and manual intervention to changes in System Frequency. It allows for study of tie line working and demonstration of system disturbances.

Facilities include: An option for coupling a second section of network, of running with or without Spinning Reserve Generation and an arrangement for creating a generation/load imbalance in order to facilitate power transfer.

Simulated responses and characteristics include: Frequency Dependent Load component, Generation Low Frequency Droop (with delay), Steam Release, Convertible Steam Energy Reserve, Combined Governor characteristic varying in response with System Frequency, Reserve Generation response varying to Frequency Deviation and High Frequency Generation shutdown.



GENERAL SPECIFICATION

GENERATORS

Number of Units	6
Output Accuracy	Within 1% relative to rated output
Pre-set Accuracy	Within 2% of reading rel. to full scale
Max. Gen. at Low Frequencies	Reduced by 2% per Hz. below 48Hz.
Automatic Trip Operation	Between 3% & 5% of rated output
Governor Accuracy	Within 4%
Governor Response	Operating between 48.5 & 50.5Hz.
Unit Cost Accuracy	Within 2% of rated cost at full load
No Load Unit Cost	10% of full load cost
Manual Loading	40 minutes $\pm$ 8 minutes*
Manual Deloading	40 minutes $\pm$ 8 minutes*
Boiler Lag	Zero to full load in 30 minutes $\pm$ 6*
Boiler Energy Reserve	4% of full load output MWhrs.
Output Synchronisation	8% to 10% of full rated output

GAS TURBINES

Number of Units	5
Load Time, Zero to Full Load	2 minutes $\pm$ 30 secs.*
Deload Time, Full Load to Zero	2 minutes $\pm$ 30 secs.*
Start Up Delay	2 minutes $\pm$ 30 secs.*
Output Accuracy	Within 2%
Cost Accuracy	Within 2% of rated cost

BASE GENERATION

Number of Selections	5
Dead Band	48Hz. $\pm$ 0.5Hz. to 50.1Hz. $\pm$ 0.5Hz.
Over Speed Governor Response	Maximum 30%/Hz.
Low Frequency Output Droop	2%/Hz. below 48Hz.
Low Frequency Droop Delay	12 minutes to final value*
Unit Cost	Not costed

TOTAL GENERATED OUTPUT

Output Accuracy	Within 2% of total generation
-----------------	-------------------------------

BASE LOAD

Number of Sections	5
Load Frequency Characteristic	2%/Hz.

VARIABLE LOAD

Programme Replay Accuracy	Within 3% of recorded value
Manual Control Accuracy	Within 1% of display reading

AREA DEMAND

Output Accuracy	Within 2% after frequency correction
-----------------	--------------------------------------

GRID SIMULATOR

Frequency Dependent Load	2%/Hz.
Generation Low Frequency Droop	2%/Hz.
Generation Output Droop Delay	12 minutes to final value*
Reserve Gen. Pick-Up Rate	8 minutes minimum*
Simulated Manual Reduction	4 times capacity of Reserve
Steam Release Gen. Reduction	10% maximum
Effective Steam Energy Reserve	1 MW/hr. per 200MW of Generation
Governor Response	Maximum 25%/Hz. at 51Hz.

TRANSFER

Output Accuracy	Within 1% of the scale reading
Pre-set Accuracy	Within 2% of the scale reading

COST

Output Accuracy	Within 1% of the sum of the costs
-----------------	-----------------------------------

FREQUENCY

Long Scale Accuracy	Within $\pm$ 0.025 Hz.
Short Scale Accuracy	Within $\pm$ 0.125 Hz.

CLOCK

Manual Update Rate	0.8 seconds/digit (real time)
Clock Rate	4 times faster than normal time
Display	4 digit 7 segment L.E.D.
Format	24 hour

ANALOGUE DISPLAY INSTRUMENTS

Movement	Moving Coil
Scale	240° 89mm
Accuracy	1%

POWER SUPPLY UNIT

Input Voltage	180-250 or (90-125) 50Hz.
Stabilized Voltages Protection	Electronic Crowbar self restoring
Power Consumption	20W

SIMULATOR CONSOLE

Dimensions	630mm W, 242mm H, 350mm D
Weight	18kg

CHART RECORDER

Type	Flat Bed
Number of Pens	2 (Disposable fibre tip)
Chart Drive	Digital stepper motor
Chart Drive Control	Automatic (from Simulator)
Chart Speed	20mm/minute (real time)
Chart Width	297mm
Dimensions	440mm W, 170mm H, 310mm D
Weight	10kg
Input Voltage	220-240 or (110-120) 50Hz.
Power Consumption	70W

TAPE RECORDER (subject to availability)

Type	Cassette
Number of Tracks	2
Tape used	BASF C90
Dimensions	282mm W, 95mm H, 240mm D
Weight	3kg
Input Voltage	220-240 or (110-120) 50Hz.
Power Consumption	8W

NOTE: Times specified * refer to simulation time scale

DESIGN FEATURES

Module Construction The Simulator is constructed of individual units which are easily removable. If changes in the simulated Power System are required it is a matter of replacing the appropriate modules and not a case of the Simulator becoming obsolete.

Analogue Display Each System Variable drives a high accuracy clearly marked analogue display, affording the operator maximum awareness of system conditions at a glance.

Chart Recorder Specially manufactured for use with the Simulator the Chart Recorder has no external controls, operates automatically, reliably and accurately. Felt tip pens are completely dependable and easily replaced as is the self aligning non-sprocketed chart paper.

System Diagram Above each pair of display units there is a section of system diagram showing the configuration of the respective plant simulated below. Details of specific parameters such as MW capacity, cost rates and governor characteristics are given.

Digital Clock The digital clock indicates simulation time which operates four times faster than real time. It can be pre-set, started, stopped, triggered automatically and used for measuring normal or event time.

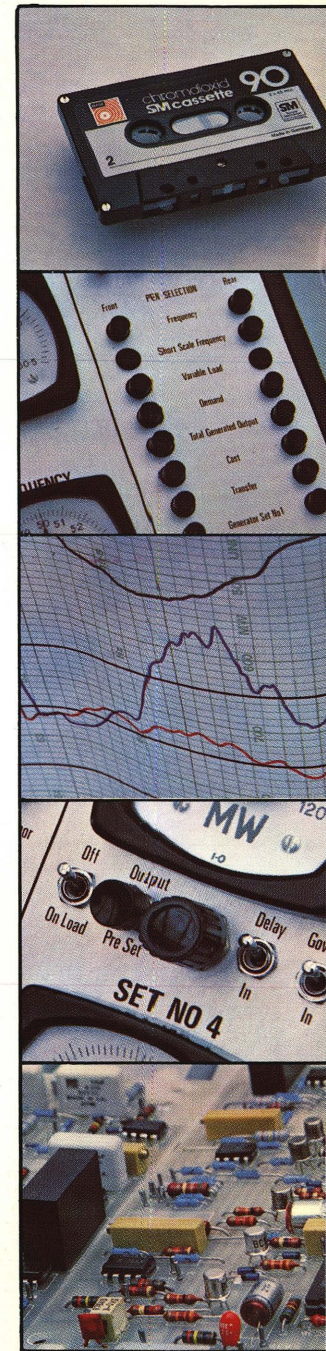
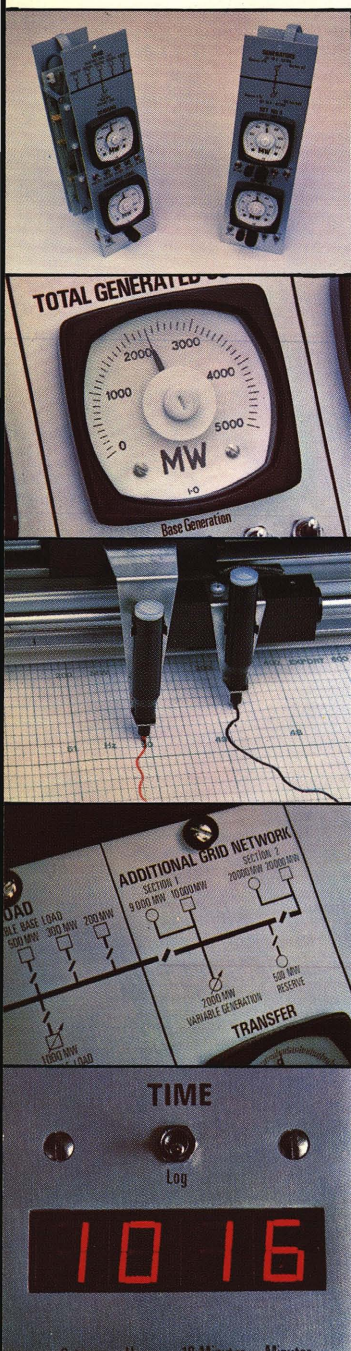
Load Programmes The tape cassette is convenient for recording load programmes and has a capacity for two independent programme simulation periods of a few hours. Load curves can be simply transcribed from chart paper to magnetic tape and replayed as often as required.

Selectable Variables Two rows of push buttons allow the System Variables to be connected to the Chart Recorder for the purpose of making hard copy records of system events.

Simulation Results The Chart paper is specially printed for the customer to suit their individual scaling requirements. Results of a load programme can be over traced using different coloured pens in order to carry out a direct performance comparison.

Control Simplicity To achieve ease in operation with maximum flexibility, controls have been kept to the minimum but with as many characteristics and responses as possible reproduced automatically by electronic simulation.

Electronic Circuitry Modern technology has made it possible to produce hardware of convenient size for processing complex simulation problems and at the same time it provides first class reliability.



EXAMPLE OF APPLICATION

The Simulator can be operated in various modes and used for many purposes. As an example of one application a brief description of general training in load despatching is given below.

Students can work on the Simulator individually or in small groups. They first spend time manipulating the plant noting system characteristics, individual generator responses, the interrelating effects of the variables and continue by deriving and verifying basic power equations. In this way Simulator operating familiarity is also obtained.

The Supervisor will record a load curve on magnetic tape and provide the student with a similar curve which serves as a load estimate. From this curve the student prepares his first Generation Loading schedule with the basic consideration being to meet the expected load with maximum economy.

The programme is replayed and with the aid of the digital clock the student loads the plant according to his schedule. Minor changes will be implemented to account for the deliberate errors introduced in the estimate, these show up on the instrumentation. The student now learns to anticipate power requirements, maintain a steady frequency and log his actions. The Supervisor gives advice as the programme progresses and notes events of interest for later discussion. On completion an overall summary of performance is made backed up by hard copy results of system frequency and cost, recorded on the chart recorder.

Progression is then made by repeating the same load curve with the aim of improving results or advancing to a new one of a more challenging nature. In order to create greater realism the supervisor will at this stage start to impose operating restrictions that are normally encountered in practice, i.e. (minimum generator loading, frequency deviation limits, spare generation requirements, generator synchronization time commitments, minimum time for generator turn round instruction) at the same time he will be looking for greater economy with the most secure set up. Later generators will be tripped and outputs restricted at random to simulate plant failure, tie line working will be investigated by the connection of the Additional Grid Network.

SUPPORTING INSTRUMENTATION

Supporting the displays and controls associated with the simulated Power Plant (described above) are the following variables

COST The active generation of the Primary Network is summated and displayed as a single variable representing the overall instantaneous cost level.

It is possible to plot this value on the Chart Recorder and equate the total cost for a given period of time. A direct minute by minute cost comparison between two attempts at loading a common programme using alternative running arrangements can be made by backwinding the chart paper and over-tracing the first result with the second.

SYSTEM FREQUENCY This is displayed in two ranges in order that deviations of several Hertz can be adequately covered and critical observation of the normal operating range easily made.

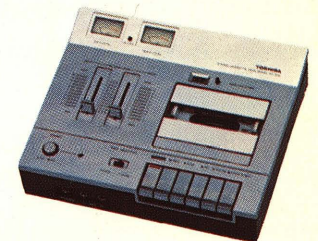
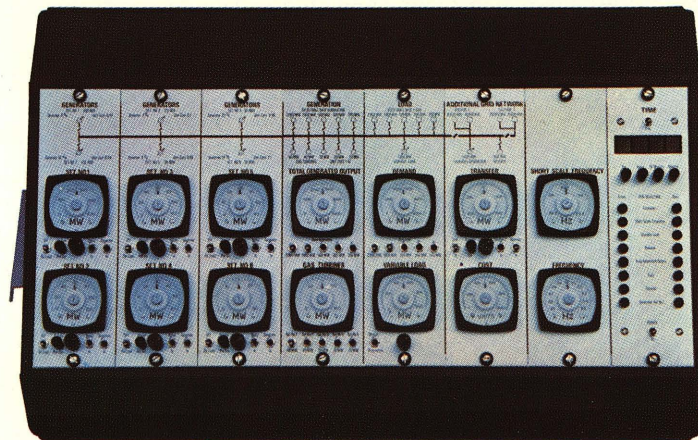
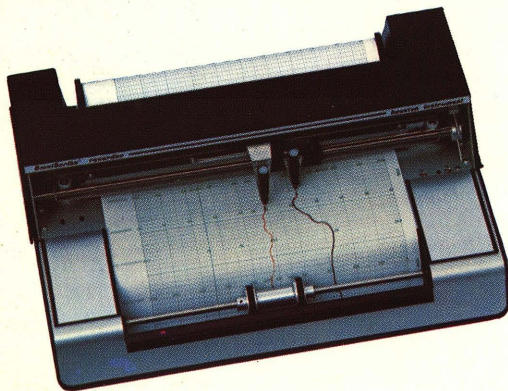
Continuous monitoring is available with the Chart Recorder and performance comparison can again be made by over-tracing results.

TIME This operates at the accelerated rate of four times in order that programmes simulating periods of two or three hours can be replayed within a convenient time. For this reason all other system responses involving time are scaled to the same factor.

When load programmes are replayed the clock is driven directly from the magnetic tape which provides an automatic stop/start facility and ensures accurate synchronization between the load curve and the time displayed.

DEMAND Variable Load and selected blocks of Base Load are frequency corrected and summated to resolve the Primary Networks total effective demand.

TOTAL GENERATED OUTPUT The MW output of Generators, Gas Turbines and Base Generation of the Primary Network are summated and displayed in total.



Why a Power Simulator

SAFE, FAST, INFORMATIVE TRAINING

FUEL ECONOMY

FREQUENCY STABILITY

PERFORMANCE ANALYSIS

DEMONSTRATION

METHOD STUDY

RISK REDUCTION

In recent years world wide awareness of the forthcoming limitations in fuel resources have led to unprecedented cost increases necessitating power utilities to operate under conditions of maximum fuel economy whilst simultaneously satisfying consumer demand and achieving the highest degree of frequency stability.

To these ends the Loading Simulator provides a new and powerful aid for training engineers in the science of power system control and economic load despatching. It further offers scope for studying alternative operating procedures, analysis of actual system events and demonstration of control problems.

Direct training on a live system has always been operationally limited and hazardous, economically costly, educationally uninformative and very, very slow. The Simulator creates an invaluable link between the theoretical teachings of the classroom and the practical realities of controlling a major power network. Learning becomes easier and unbelievably rapid.

Performance can be accurately monitored on the Simulator and precise comparisons made between differing approaches, applied to repeatable load curves. Such comparisons are to a great extent impossible to make directly on power networks due to daily variations in plant availability and consumer load.

The action of a control engineer in the event of an extreme or unusual system condition is critical. Often on these occasions even experienced engineers become indecisive, making serious errors purely due to the unfamiliarity of the situation. The Simulator can be usefully employed to minimise such risks by covering these areas of operation at the initial training stage and by regular refresher courses.

Why a **MOKO** Simulator

SELF-CONTAINED

EASY TO USE

CUSTOMER BUILT

FLEXIBLE

RELIABLE

Built to meet customers' personal plant requirements the MOKO Simulator is a self contained portable unit operating independently of a main processor. The design concept comprises control simplicity with comprehensive facilities provided by internal electronic circuitry, producing a machine which is easy to operate, informative and reliable.

APPENDIX : B

"Mini-digital Simulator's Program Listing"

1

PAGE :

MOTOROLA 16800 CROSS ASSEMBLER, RELEASE 1.2

(85)

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00490
00500
00510 00F0
00520 00F0 80
00530 00F1 80
00540 00F2 80
00550 00F3 80
00560 00F4 03
00570 00F5 00
00580 00F6 00
00590 00F7 00
00600 00F8 00
00610 00F9 80
00620 00FA 00
00630 00FB 80
00640 00FC 80
00650 00FD 80
00660 00FE 80
00670 00FF 80
00680
00690
00700
00710 00E0
00720 00E0 80
00730 00E1 80
00740 00E2 80
00750 00E3 80
00760 00E4 03
00770 00E5 00
00780 00E6 00
00790 00E7 00
00800 00E8 00
00810 00E9 80
00820 00EA 00
00830 00EB 80
00840 00EC 80
00850 00ED 80
00860 00EE 80
00870 00EF 80
00880
00890
00900
00910
00920
00930
00940
00950
00960
00970 2000
00980
00990
01000

```

* INTEGRATION REGISTERS GENERATOR NO:1
 ORG 3F0
 FCB 380 FREQUENCY
 FCB 380 REFERENCE LEVEL
 FCB 380 ERROR INPUT
 FCB 380 LOW PRESSURE STAGE INPUT
 FCB 303 PROGRAM SECTION FLAG
 FCB 300 SCRATCH REGISTER
 FCB 300 SCRATCH REGISTER
 FCB 300 SCRATCH REGISTER
 FCB 300 SCRATCH REGISTER
 FCB 380 GOVERNOR SETTING
 FCB 300 NOT USED
 FCB 380 GOVERNOR RESPONSE
 FCB 380 LOW PRESSURE STAGE OUTPUT
 FCB 380 GOVERNOR INPUT
 FCB 380 HIGH PRESSURE STAGE OUTPUT
 FCB 380 HIGH PRESSURE STAGE INPUT

* REGISTER FOR 120 MW SET
 ORG 3E0
 FCB 380 FREQUENCY
 FCB 380 REFERENCE LEVEL
 FCB 380 ERROR INPUT
 FCB 380 LOW PRESSURE STAGE INPUT
 FCB 303 PROGRAM SECTION FLAG
 FCB 300 SCRATCH REGISTER
 FCB 300 SCRATCH REGISTER
 FCB 300 SCRATCH REGISTER
 FCB 300 SCRATCH REGISTER
 FCB 380 GOVERNOR SETTING
 FCB 300 NOT USED
 FCB 380 GOVERNOR RESPONSE
 FCB 380 LOW PRESSURE STAGE OUTPUT
 FCB 380 GOVERNOR INPUT
 FCB 380 HIGH PRESSURE STAGE OUTPUT
 FCB 380 HIGH PRESSURE STAGE INPUT

* TOTAL GENERATION AFTER DELAY AT 0081
 * TOTAL LOAD DEMAND AT 0082
 * REQUIRED INPUT FOR THE SYSTEM AT 0083
 * TOTAL GOVERNOR RESPONSE AT 0084
 * GENERAL SCRATCH REGISTERS FOR
 * GENERATOR NO:1,2,3... AT 0060 0061
 * ALL 10 SCRATCH REGISTERS AT
 * 007B, 0083, 0084, 0085, 0086
 ORG 12000

* INITIALIZATION OF THE P.I.R.S

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01010          * "A" INPUT, "B" OUTPUT IN 8004-07 "PIA"
01020          *
01030 2000 7F 8005      CLR      $8005      DDP AT 8004
01040 2003 7F 8004      CLR      $8004      ALL LINE1 INPUT FOR "A"
01050 2006 86 2C        LDA A    $12C      OUTPUT REGISTER AT
01060 2008 B7 8005      LTR A    $8005      8004 WITH PULCE ON "FEAD"
01070 200B 7F 8007      CLR      $8007      DDP AT 8006
01080 200E 86 FF        LDA A    $1FF      ALL LINE1
01090 2010 B7 8006      LTR A    $8006      OUTPUT FOR "B" SIDE
01100 2013 86 04        LDA A    $104      OUTPUT REGISTER AT
01110 2015 B7 8007      LTR A    $8007      8006
01120          *
01130          * "A" "B" ARE OUTPUTS IN 8010-13 "PIA"
01140 2018 7F 8011      CLR      $8011      DDP AT 8010
01150 201B 86 FF        LDA A    $1FF      ALL LINE1 ARE
01160 201D B7 8010      LTR A    $8010      OUTPUT FOR "A"
01170 2020 86 04        LDA A    $104      OUTPUT REGISTER 11
01180 2022 B7 8011      LTR A    $8011      AT 8010
01190 2025 7F 8013      CLR      $8013      DDP AT 8013
01200 2028 86 FF        LDA A    $1FF      ALL LINE1 ARE
01210 202A B7 8012      LTR A    $8012      OUTPUT FOR "B" SIDE
01220 202D 86 2C        LDA A    $12C      OUTPUT REGISTER AT
01230 202F B7 8013      LTR A    $8013      8012 PULCE FOR TIMEP
01240          *
01250          * READ GENERATOR NO:1 DEMAND GENERATION AFTER DELAY
01260          *
01270 2032 86 30      LOOP1 LDA A    $130
01280 2034 C6 01      LDA B    $101      SPECIFIES GENERATOR NO:1
01290 2036 F7 8006      LTR B    $8006
01300 2039 4A          MULTP1 DEC A
01310 203A 26 FD      BNE      MULTP1      DELAY REQUIRED TO WRITE
01320 203C C6 30      LDA B    $130
01330 203E 86 8004      LDA A    $8004
01340 2041 5A          DIG1 DEC B
01350 2042 26 FD      BNE      DIG1      DELAY REQUIRED TO READ
01360          * WE HAVE TO READ AND WRITE TWICE
01370 2044 86 30      LDA A    $130
01380 2046 C6 01      LDA B    $101      SPECIFIES GENERATOR NO:1
01390 2048 F7 8006      LTR B    $8006
01400 204B 4A          M1 DEC A
01410 204C 26 FD      BNE      M1      DELAY REQUIRED TO WRITE
01420 204E C6 30      LDA B    $130
01430 2050 86 8004      LDA A    $8004
01440 2053 5A          D0 DEC B
01450 2054 26 FD      BNE      D0      DELAY REQUIRED TO READ
01460          *
01470 2056 97 7F      LTR A    $7F      STORES TARGET GENERATION NO:1
01480          *
01490          * PROGRAM TO GIVE GENERATION RESPONSE
01500 2058 D6 7C      LDA B    $7C      PRESENT GENERATION
01510 205A 10          LDR
01520 205B 22 28      BHI      OPT

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01530 205D 40      NEG A
01540 205E 18      TAB
01550 205F 54      LDP B      TIME CONSTANT
01560 2060 54      LIP B
01570 2061 54      LIP B
01580 2062 54      LIP B
01590 2063 D7 7E   STA B      $7E      INCREMENTAL GENERATION
01600 2065 DE 40   LDN      $40
01610 2067 09      DEB
01620 2068 DF 40   STX      $40
01630 206A 26 41   BNE      HTYET      APPROPRIATE DELAY
01640 206C CE 0042 LDN      $0042
01650 206F DF 40   STX      $40
01660 2071 96 7D   LDA A      $7D
01670 2073 D6 7E   LDA B      $7E
01680 2075 10      IBA
01690 2076 22 02   BHI      J1      BRANCH IF
01700 2078 20 07   BPA      CONST1    TARGET REACHED
01710 207A 97 7C   STA A      $7C      J1
01720 207C D6 7F   LDA B      $7F
01730 207E 10      IBA
01740 207F 22 28   BHI      HTC
01750 2081 96 7F   LDA A      $7F      CONST1
01760 2083 20 26   BPA      OUT
01770 2085 44      GRT      LIP A      TIME CONSTANT
01780 2086 44      LIP A
01790 2087 44      LIP A
01800 2088 44      LIP A
01810 2089 16      TAB
01820 208A D7 7E   STA B      $7E      INCREMENTAL GENERATION
01830 208C DE 40   LDN      $40
01840 208E 09      DEB
01850 208F DF 40   STX      $40
01860 2091 26 1A   BNE      HTYET      APPROPRIATE DELAY
01870 2093 CE 0042 LDN      $0042
01880 2096 DF 40   STX      $40
01890 2098 96 7D   LDA A      $7D
01900 209A D6 7E   LDA B      $7E
01910 209C 18      ABA
01920 209D 97 7C   STA A      $7C
01930 209F 16      TAB
01940 20A0 96 7F   LDA A      $7F
01950 20A2 10      IBA
01960 20A3 22 04   BHI      HTC
01970 20A5 96 7F   LDA A      $7F      TARGET REACHED
01980 20A7 20 02   BPA      OUT
01990 20A9 96 7C   LDA A      $7C      HTC
02000 20AB 97 7D   STA A      $7D      OUT      INPUT TO THE SYSTEM
02010
02020      * DISPLAY PRESENT VALUE OF GENERATION NO:1
02030 20AD 96 7D   HTYET LDA A      $7D      TO BE DISPLAYED GEN NO:1
02040 20AF C6 30   LDA B      $30

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02050 20B1 B7 8012      LTA A  $8012
02060 20B4 5A          ANA      DEC B      DELAY REQUIRED TO WRITE
02070 20B5 26 FD          BNE      ANA
02080 20B7 86 30          LDA A  $130
02090 20B9 C6 FD          LDA B  $1FD      CHOOSES S-H NO:2 (SAMPLE)
02100 20BB F7 8010      LTA B  $8010
02110 20BE 4A          HOLD1 DEC A      DELAY REQUIRED TO WRITE
02120 20BF 26 FD          BNE      HOLD1
02130          * WE HAVE TO READ AND WRITE TWICE
02140 20C1 96 7D          LDA A  $7D
02150 20C3 C6 30          LDA B  $130
02160 20C5 B7 8012      LTA A  $8012
02170 20C8 5A          A0      DEC B      DELAY REQUIRED TO WRITE
02180 20C9 26 FD          BNE      A0
02190 20CB 86 30          LDA A  $130
02200 20CD C6 FD          LDA B  $1FD      CHOOSES S.H. NO:2 SAMPLE
02210 20CF F7 8010      LTA B  $8010
02220 20D2 4A          H1      DEC A      DELAY REQUIRED TO WRITE
02230 20D3 26 FD          BNE      H1
02240 20D5 86 30          LDA A  $130
02250 20D7 C6 FF          LDA B  $1FF      HOLDS ALL
02260 20D9 F7 8010      LTA B  $8010      READING
02270 20DB 4A          L1      DEC A      DELAY REQUIRED TO WRITE
02280 20DD 26 FD          BNE      L1
02290
02300          * READ 120 MM GENERATOR
02310          *
02320 20DF 86 30          LDA A  $130
02330 20E1 C6 02          LDA B  $102      CHOOSES GEN NO:2 INPUT
02340 20E3 F7 8006      LTA B  $8006
02350 20E6 4A          MULTP2 DEC A      DELAY REQUIRED TO WRITE
02360 20E7 26 FD          BNE      MULTP2
02370 20E9 C6 30          LDA B  $130
02380 20EB B6 8004      LDA A  $8004
02390 20EE 5A          DIG12 DEC B      DELAY REQUIRED TO READ
02400 20EF 26 FD          BNE      DIG12
02410          * WE HAVE TO READ AND WRITE TWICE
02420 20F1 86 30          LDA A  $130
02430 20F3 C6 02          LDA B  $102      CHOOSES S.H. NO:2 SAMPLE
02440 20F5 F7 8006      LTA B  $8006
02450 20F8 4A          M2      DEC A      DELAY REQUIRED TO WRITE
02460 20F9 26 FD          BNE      M2
02470 20FB C6 30          LDA B  $130
02480 20FD B6 8004      LDA A  $8004
02490 2100 5A          D2      DEC B      DELAY REQUIRED TO READ
02500 2101 26 FD          BNE      D2
02510          *
02520 2103 97 6F          LTA A  $6F      STOPS TARGET GEN 2
02530          *
02540          * PROGRAM TO PROVIDE GENERATION NO:2
02550 2105 D6 6C          LDA B  $6C      PRESENT GENERATION
02560 2107 10          LDA

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02570 2108 22 28      BHI      GRT3
02580 2108 40      NEG A
02590 2108 16      TAB
02600 210C 54      LDP B      TIME CONSTANT
02610 210D 01      NOP
02620 210E 01      NOP
02630 210F 01      NOP
02640 2110 07 6E      STA B      66E      INCREMENTAL GENERATION
02650 2112 0E 42      LDC      642
02660 2114 09      DEC
02670 2115 0F 42      STA      642
02680 2117 26 41      BNE      NTVET2      APPROPRIATE DELAY
02690 2119 0E 041A      LDC      79041A
02700 211C 0F 42      STA      642
02710 211E 96 6D      LDA A      66D
02720 2120 06 6E      LDA B      66E
02730 2122 10      LBA
02740 2123 22 02      BHI      J2      BRANCH IF
02750 2125 20 07      BBA      CONST2      TARGET REACHED
02760 2127 97 6C      STA A      66C
02770 2129 06 6F      LDA B      66F
02780 212B 10      LBA
02790 212C 22 28      BHI      NTC2
02800 212E 96 6F      LDA A      66F      CONST2
02810 2130 20 26      BBA      OUT2
02820 2132 44      GRT3      LDP A      TIME CONSTANT
02830 2133 01      NOP
02840 2134 01      NOP
02850 2135 01      NOP
02860 2136 16      TAB
02870 2137 07 6E      STA B      66E      INCREMENTAL GENERATION
02880 2139 0E 42      LDC      642
02890 213B 09      DEC
02900 213C 0F 42      STA      642
02910 213E 26 1A      BNE      NTVET2      APPROPRIATE DELAY
02920 2140 0E 041A      LDC      79041A
02930 2143 0F 42      STA      642
02940 2145 96 6D      LDA A      66D
02950 2147 06 6E      LDA B      66E
02960 2149 1B      ABA
02970 214A 97 6C      STA A      66C
02980 214C 16      TAB
02990 214D 96 6F      LDA A      66F
03000 214F 10      LBA
03010 2150 22 04      BHI      NTC2
03020 2152 96 6F      LDA A      66F      TARGET REACHED
03030 2154 20 02      BBA      OUT2
03040 2156 96 6C      LDA A      66C      INPUT TO 2ND SET
03050 2158 97 6D      OUT2      STA A      66D
03060
03070
03080

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* DISPLAY PRESENT VALUE OF 120 MM SET

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03090 215A 96 6D  MTYET2 LDA A  66D      TO BE DISPLAYED (GEN NO:2)
03100 215C C6 30      LDA B  7130
03110 215E B7 8012      STA A  88012
03120 2161 5A      ANA2_  DEC B      DELAY REQUIRED TO WRITE
03130 2162 26 FD      BNE  ANA2_
03140 2164 86 30      LDA A  7130
03150 2166 C6 FB      LDA B  71FB      CHOOSES S.H. NO:3 (SAMPLE)
03160 2168 F7 8010      STA B  88010
03170 216B 4A      HOLD2 DEC A      DELAY REQUIRED TO WRITE
03180 216C 26 FD      BNE  HOLD2_
03190      * WE HAVE TO READ AND WRITE TWICE
03200 216E 96 6D      LDA A  66D      TO BE DISPLAYED
03210 2170 C6 30      LDA B  7130
03220 2172 B7 8012      STA A  88012
03230 2173 5A      A2      DEC B      DELAY REQUIRED TO WRITE
03240 2175 26 FD      BNE  A2
03250 2178 86 30      LDA A  7130
03260 217A C6 FB      LDA B  71FB      CHOOSES S.H. NO:3 (SAMPLE)
03270 217C F7 8010      STA B  88010
03280 217F 4A      H2      DEC A      DELAY REQUIRED TO WRITE
03290 2180 26 FD      BNE  H2
03300 2182 86 30      LDA A  7130
03310 2184 C6 FF      LDA B  71FF      HOLDS ALL
03320 2186 F7 8010      STA B  88010      READINGS
03330 2189 4A      L2      DEC A      DELAY REQUIRED TO WRITE
03340 218A 26 FD      BNE  L2
03350      *
03360      * FIND TOTAL GENERATION
03370      *
03380 218C BD 362E      JCF  17H1      SUBROUTINE
03390      *      WHICH SET
03400      *      IS SYNCHRONIZED
03410      *
03420      *
03430      * READ TOTAL LOAD REQUIRED
03440      *
03450 218F 86 30      LDA A  7130
03460 2191 C6 00      LDA B  7100      SPECIFIES INPUT=TOTAL LOAD
03470 2193 F7 8006      STA B  88006
03480 2196 4A      MULTP0 DEC A      DELAY REQUIRED TO WRITE
03490 2197 26 FD      BNE  MULTP0
03500 2199 C6 30      LDA A  7130
03510 219B 86 8004      LDA B  88004
03520 219E 5A      DIG10 DEC B      DELAY REQUIRED TO READ
03530 219F 26 FD      BNE  DIG10
03540      * WE HAVE TO READ AND WRITE TWICE
03550 21A1 86 30      LDA A  7130
03560 21A3 C6 00      LDA B  7100      SPECIFIES INPUT=TOTAL LOAD
03570 21A5 F7 8006      STA B  88006
03580 21A8 4A      H0      DEC A      DELAY REQUIRED TO WRITE
03590 21A9 26 FD      BNE  H0
03600 21AB C6 30      LDA B  7130

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03610 21AD B6 8004      LDA A 8004
03620 21B0 5A          DEC B          DELAY REQUIRED TO READ
03630 21B1 26 FD          BNE D1
03640 21B3 97 82          LTA A 882      TOTAL LOAD DEMAND
03650 21B5 D6 81          LDA B 881      TOTAL GENERATION
03660 21B7 10          CBA          LOAD - GENERATION
03670 21B8 22 07          BHI 6PT2      IS LOAD > GENERATION ?
03680 21BA 40          NEG A
03690 21BB 16          TAB
03700 21BC 88 80          LDA A 880
03710 21BE 10          CBA
03720 21BF 20 03          BPA 6E0
03730 21C1 C6 80 6PT2    LDA B 880
03740 21C3 1B          ABA
03750 21C4 97 83 6E0    LTA A 883      REQUIRED INPUT TO THE SYSTEM
03760
03770
03780
03790
03800 21C6 96 F2          LDA A 8F2      ERROR INPUT
03810 21C8 D6 F1          LDA B 8F1      REFERENCE LEVEL 80 IN HEX
03820 21CA 10          CBA
03830 21CB 22 21          BHI LOOP2
03840 21CD 40          NEG A
03850 21CE 16          TAB
03860 21CF 54          LIP B          DIVISION=
03870 21D0 54          LIP B          TIME CONSTANT
03880 21D1 01          NOP
03890 21D2 01          NOP
03900 21D3 D7 F5          LTA B 8F5      INCREMENTAL VALUE
03910 21D5 DE 00          LDC 800
03920 21D7 09          DEC
03930 21D8 DF 00          LTX 800
03940 21DA 26 67          BNE LOOP4      APPROPRIATE DELAY
03950 21DC CE 0010        LDI 80010
03960 21DE DF 00          CTP 800
03970 21E1 96 F0          LDA A 8F0
03980 21E3 D6 F5          LDA B 8F5
03990 21E5 1B          ABA          INCREMENT WITH -VE SIGN
04000 21E6 81 F0          CUP A 8F0
04010 21E8 23 22          BLS LOOP3      STOP
04020 21EA 86 F0          LDA A 8F0      ANY
04030 21EC 20 1E          BPA LOOP3      OVER FLOW
04040 21EE 44          LOOP2    LIP A          TIME CONSTANT
04050 21EF 44          LIP A
04060 21F0 01          NOP
04070 21F1 01          NOP
04080 21F2 16          TAB
04090 21F3 D7 F5          LTA B 8F5      INCREMENTAL VALUE
04100 21F5 DE 00          LDC 800
04110 21F7 09          DEC
04120 21F8 DF 00          LTX 800

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04130 21FA 26 47      BNE      LOOP4      APPROPRIATE DELAY
04140 21FC CE 0010    LDM      130010
04150 21FE DF 00      STC      300
04160 2201 96 F0      LDA      A      3F0
04170 2203 D6 F5      LDA      B      3F5
04180 2205 10        LRA
04190 2206 81 08      CMP      A      1108
04200 2208 22 02      BHI      L00 3      STOP
04210 220A 86 03      LDA      A      1108
04220 220C 97 F0      LOOP3  LRA      A      3F0
04230
04240      * PLOTTING FREQUENCY OF THE SYSTEM
04250 220E 7E 25E1    JMP      SUB      SUBROUTINE TO CHECK
04260      * EXCESSIVE FREQUENCY DEVIATION
04270 2211 96 F0      CHECK  LDA      A      3F0
04280 2213 C6 30      LDA      B      1130
04290 2215 B7 8012    LRA      A      18012
04300 2218 5A        ANA0    DEC      B
04310 2219 26 FD      BNE      ANA0      DELAY REQUIRED TO WRITE
04320 221B 86 30      LDA      A      1130
04330 221D C6 FE      LDA      B      11FE
04340 221F F7 8010    LRA      B      18010
04350 2222 49        HOLD0   DEC      A
04360 2223 26 FD      BNE      HOLD0      DELAY REQUIRED TO WRITE
04370
04380 2225 96 F0      * WE HAVE TO READ AND WRITE TWICE
04390 2227 C6 30      LDA      A      3F0
04400 2229 E7 8012    LDA      B      1130
04410 222C 5A        LRA      A      18012
04420 222D 26 FD      A1      DEC      B
04430 222F 86 30      BNE      A1      DELAY REQUIRED TO WRITE
04440 2231 C6 FE      LDA      A      1130
04450 2233 F7 8010    LDA      B      11FE
04460 2236 4A        LRA      B      18010
04470 2237 26 FD      H0      DEC      A
04480 2239 86 30      BNE      H0      DELAY REQUIRED TO WRITE
04490 223B C6 FF      LDA      A      1130
04500 223D F7 8010    LDA      L      11FE
04510 2240 4A        LRA      B      18010
04520 2241 26 FD      L3      DEC      A
04530      BNE      L3      HOLD? ALL
04540      * 500 NM SET
04550      * PENDING?
04560 2243 01      LOOP4  NOP
04565 2244 01      NOP
04570 2245 96 51      * 500NM IN USE
04580 2247 2B 03      LDA      A      351
04590 2249 7E 2395    BHI      110
04600 224C 96 F0      JMP      111
04610 224E C6 80      LDA      A      3F0
04620 2250 10        LDA      B      1130
04630 2251 22 0F      LRA
04640      BHI      11

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04640 2253 40      NEG A
04650 2254 81 07    CUP A 7107 SLEEVE
04660 2256 23 02    BUI 02    LIMITER
04670 2258 86 07    LDA A 7107
04680 225A BD 2270 X2  JIP DROOP GOTO DROOP SUBROUTINE
04690 225D 96 F9     LDA A 3F9 GOVERNOR SETTING
04700 225F 1B      ABA
04710 2260 20 00    BBA 03
04720 2262 81 07    CUP A 7107 SLEEVE
04730 2264 23 02    BUI 04    LIMITER
04740 2266 86 07    LDA A 7107
04750 2268 BD 2270 X4  JIP DROOP GOTO DROOP SUBROUTINE
04760 226B 96 F9     LDA A 3F9 GOVERNOR SETTING
04770 226D 10      CBA
04780 226E 20 06 X3  BBA LOOP7
04790 2270 16      DROOP TAB FOR A & DROOP
04800 2271 58      AIL B CHARACTERISTIC
04810 2272 58      AIL B 1. P=16
04820 2273 58      AIL B 1. E. MULTIPLY BY
04830 2274 58      AIL B 16
04840 2275 39      RTI
04850 2276 97 FD LOOP7 CTA A 3FD INPUT TO GOVERNOR
04860 2278 06 80 LOOP15 LDA B 7180 REFERENCE LEVEL
04870 227A 10      CBA
04880 227B 22 04    BHI B1 TAKING CARE OF
04890 227D 40      NEG A NEGATIVE
04900 227E 1B      ABA
04910 227F 20 04    BBA B2 SIGN IN
04920 2281 16      B1 TAB
04930 2282 86 80    LDA A 7180
04940 2284 10      CBA INTEGRATION
04950 2285 D6 FF B2 LDA B 3FF GOVERNOR OUTPUT
04960 2287 10      CBA
04970 2288 22 1E    BHI LOOP8
04980 228A 40      NEG A
04990 228B 16      TAB
05000 228C 54      DIV2 LIP B TIME CONSTANT
05010 228D 01      DIV4 NOP
05020 228E 01      DIV8 NOP
05030 228F D7 F6    CTA B 3FA INCREMENTAL VALUE
05040 2291 DE 02    LDC 302
05050 2293 09      DEC
05060 2294 26 32    BNE LOOP10 APPROPRIATE DELAY
05070 2296 CE 0000  LDC 310000
05080 2299 DF 02    CTS 302
05090 229B 96 FF    LDA A 3FA GOVERNOR OUTPUT
05100 229D D6 F6    LDA B 3FA INCREMENTAL VALUE
05110 229F 10      CBA SIGN HAS ALREADY TAKEN CARE
05120 22A0 81 03    CUP A 7103 POSITION
05130 22A2 22 1F    BHI LOOP9
05140 22A4 86 03    LDA A 7103 LIMIT
05150 22A6 20 1B    BBA LOOP8

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05160 22A8 44      LOOP8 LIP A      TIME CONSTANT
05170 22A9 01      DIV14 NOP
05180 22AA 01      DIV18 NOP
05190 22AB 16      TAB
05200 22AC D7 F6    STA B 3F6
05210 22AD DE 02    LDI 302
05220 22AE 09      DECI      APPROPRIATE DELAY
05230 22B1 26 15    BNE LOOP10
05240 22B3 CE 0000   LDI 10000
05250 22B6 DF 02    ITI 302
05260 22B8 96 FF    LDA A 3FF    GOVERNOR OUTPUT
05270 22BA D6 F6    LDA B 3F6    INCREMENTAL VALUE
05280 22BC 1B      ARA
05290 22BD 81 F8    CMP A 3F8    POSITION
05300 22BF 23 02    BCL LOOP9
05310 22C1 86 F8    LDA A 3F8    LIMIT
05320 22C3 16      LOOP9 TAB
05330 22C4 D7 FF    STA B 3FF    GOVERNOR OUTPUT
05340 22C6 20 02    BRA LOOP11
05350 22C8 DF 02    LOOP10 ITI 302
05360 22CA 96 F4    LOOP11 LDA A 3F4    FLAG: WHAT STAGE ?
05370 22CC 4A      DEC A
05380 22CD 97 F4    STA A 3F4
05390 22CF 81 01    CMP A 301    HIGH PRESSURE COMPLETED?
05400 22D1 23 26    BCL LOOP13
05410 22D3 86 FE    LDA A 3FE    NO: THEN INITIALISE AND GO
05420 22D5 BD 258D   JIP INIT1
05430 22D8 86 F7    LDA A 3FF
05440 22DA BD 259A   JIP INIT2
05450 22DD 86 04    LDA A 304
05460 22DF BD 25A7   JIP INIT3
05470 22E2 86 0C    LDA A 30C
05480 22E4 B7 229C   STA A 3229C    DIFFERENT DELAY
05490 22E7 B7 22B9   STA A 322B9    TIME
05500 22EA 96 FF    LDA A 3FF
05510 22EC C6 54    LDA B 354    DIFFERENT TIME CONSTANT
05520 22EE F7 228D   STA B DIV4
05530 22F1 C6 44    LDA B 344
05540 22F3 F7 22A9   STA B DIV14
05550 22F6 7E 2278   JMP LOOP15
05560 22F9 81 00    LOOP13 CMP A 300    GOTO SIMULATE HIGH PRES.
05570 22FB 27 43    BEQ LOOP14    YES: THEN DO LOW PRES. STAGE
05580 22FD 96 FE    LDA A 3FE
05590 22FF C6 80    LDA B 380
05600 2301 10      LRA
05610 2302 22 0C    RAI 35
05620 2304 40      NEG A
05630 2305 16      TAB
05640 2306 44      LIP A      PS GOES TO
05650 2307 54      LIP B      THE REHEATER
05660 2308 54      LIP B
05670 2309 1B      ARA

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05680 230A 16          TAB
05690 230B 86 80      LDA A 7180
05700 230D 10        LBR
05710 230E 20 08      BBR A X6
05720 2310 16          TAB
05730 2311 44          LIP A
05740 2312 54          LIP B
05750 2313 54          LIP B
05760 2314 1B          ABR
05770 2315 06 80      LDA B 7180
05780 2317 1B          ABR
05790 2318 97 F3 X6    STA A 1F3
05800 231A 86 FC        LDA A 71FC
05810 231C BD 258D      JIP INIT1
05820 231F 86 F8        LDA A 71F8
05830 2321 BD 259A      JIP INIT2
05840 2324 86 06        LDA A 7106
05850 2326 BD 25A7      JIP INIT3
05860 2329 86 5E        LDA A 715E
05870 232B B7 229C      STA A 1229C
05880 232E B7 22B9      STA A 122B9
05890 2331 96 F3        LDA A 1F3
05900 2333 06 54        LDA B 7154
05910 2335 F7 228E      STA B DIV8
05920 2338 06 44        LDA B 7144
05930 233A F7 22AA      STA B DIV18
05940 233D 7E 2278      JMF LOOP15
05950 2340 96 FE        LDA A 1FE
05960 2342 06 80        LDA B 7180
05970 2344 10          LBR
05980 2345 22 14        BHI R1
05990 2347 40          NEG A
06000 2348 44          LIP A
06010 2349 44          LIP A
06020 234A 16          TAB
06030 234B D7 D4        STA B 1D4
06040 234D 96 FC        LDA A 1FC
06050 234F 06 80        LDA B 7180
06060 2351 10          LBR
06070 2352 D6 D4        LDA B 1D4
06080 2354 1B          ABR
06090 2355 16          TAB
06100 2356 86 80      LDA A 7180
06110 2358 10          LBR
06120 2359 20 0F      BBR A R2
06130 235B 44          LIP A
06140 235D 44          LIP A
06150 235F 97 D4        STA A 1D4
06160 2361 D6 FC        LDA B 1FC
06170 2363 86 80      LDA A 7180
06180 2365 10          LBR
06190 2367 D6 D4        LDA B 1D4

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75 GOES TO
THE REHEATER

LOW PRES. INPUT
INITIALISE AND GO

DIFFERENT DELAY TIME

DIFFERENT TIME CONSTANT

GOTO SIMULATE LOW PRES.
OUTPUT OF HIGH PRES.
REFERENCE LEVEL

25 GOES STRAIGHT THROUGH

OUTPUT OF LOW PRES.

25 GOES STRAIGHT THROUGH

OUTPUT OF LOW PRES.

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06200 2366 1B      ARA
06210 2367 06 80   LDA B 7180
06220 2369 1B      ARA
06230 236A 97 FB P2  LTA A 7FEF      GOVERNOR RESPONSE GEN NO: 1
06240 236C 86 FF     LDA A 7FFF      INITIALISE AND REPEAT ALL
06250 236E BD 258D   JIP      INIT1
06260 2371 86 FB     LDA A 7FEF
06270 2373 BD 259A   JIP      INIT2
06280 2376 86 02     LDA A 7F02
06290 2378 BD 25A7   JIP      INIT3
06300 237B 86 0C     LDA A 7F0C      DIFFERENT DELAY TIME
06310 237D E7 229C   LTA A 7229C
06320 2380 E7 22B9   LTA A 722B9
06330 2383 86 03     LDA A 7F03      INITIALISE FLAG
06340 2385 97 F4     LTA A 7EF4
06350 2387 86 01     LDA A 7F01
06360 2389 E7 228D   LTA A 7D1V4      DIFFERENT TIME CONSTANT
06370 238C E7 228E   LTA A 7D1V8
06380 238F E7 22A9   LTA A 7D1V14
06390 2392 E7 22AA   LTA A 7D1V18
06400
06410      * 120 NM SET
06420
06430 2395 01      B11  NOP
06435 2396 01      NOP      12 120NM IN USE
06440 2397 96 52     LDA A 7552
06450 2399 2B 03     BMT      B12
06460 239B 7E 24E9   JMP      B13
06470 239E 96 F0     LDA A 7EF0      IN USE THEN...
06480 23A0 97 E0     LTA A 7E0
06490 23A2 06 80     LDA B 7180
06500 23A4 10      LBR
06510 23A5 22 0F     BMT      X21
06520 23A7 40      NEG A
06530 23A8 81 0F     CMP A 710F      SLEEVE
06540 23AA 23 02     BLS      X22      LIMITER
06550 23AC 86 0F     LDA A 710F
06560 23AE BD 23C4 X22  JIP      DROOP2      GOTO DROOP SUBROUTINE
06570 23B1 96 E9     LDA A 7E9      GOVERNOR SETTING
06580 23B3 1B      ARA
06590 23B4 20 0C     LBR      X23
06600 23B6 81 0F     CMP A 710F      SLEEVE
06610 23B8 23 02     BLS      X24      LIMITER
06620 23BA 86 0F     LDA A 710F
06630 23BC BD 23C4 X24  JIP      DROOP2      GOTO DROOP SUBROUTINE
06640 23BF 96 E9     LDA A 7E9      GOVERNOR SETTING
06650 23C1 10      LBR
06660 23C2 20 06     LBR      X23      DROOP2
06670 23C4 16      DROOP2 TAB      FOR A 12 DROOP
06680 23C5 58      ALL B      CHARACTERISTIC
06690 23C6 58      ALL B      1 P#8
06700 23C7 58      ALL B      I.E. MULTIPLY BY

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06710 2308 01      NOP      8
06720 2309 39      RTI
06730 230A 97 ED    LOOP27 LTA A  $E0      INPUT TO GOVERNOR
06740 230C 06 80    LOOP25 LDA B  $180      REFERENCE LEVEL
06750 230E 10      LDB
06760 230F 22 04    BHI      B3      TAKING CARE OF
06770 23D1 40      NEG A
06780 23D2 18      RDB      NEGATIVE
06790 23D3 20 04    PBH      B4
06800 23D5 16      TAB      SIGN IN
06810 23D6 86 80    LDA A  $180
06820 23D8 10      LDB      INTEGRATION
06830 23D9 D6 EF    B4      LDA B  $EF      GOVERNOR OUTPUT
06840 23DB 10      LDB
06850 23DC 22 1E    BHI      LOOP28
06860 23DE 40      NEG A
06870 23DF 16      TAB
06880 23E0 04      DIV22 LIP B
06890 23E1 01      DIV42 NOP
06900 23E2 01      DIV82 NOP
06910 23E3 D7 E6    LTA B  $E6      INCREMENTAL VALUE
06920 23E5 DE 12    LDB      $12
06930 23E7 09      DBX
06940 23E8 26 32    BNE      LOOP30      APPROPRIATE DELAY
06950 23EA CE 0000   LDB      $10000
06960 23ED DF 12    LTB      $12
06970 23EF 96 EF    LDA A  $EF      GOVERNOR OUTPUT
06980 23F1 D6 E6    LDA B  $E6      INCREMENTAL VALUE
06990 23F3 10      LDB      SIGN HAS ALREADY TAKEN CARE
07000 23F4 81 08    CUP A  $108      POSITION
07010 23F6 22 1F    BHI      LOOP29
07020 23F8 96 08    LDA A  $108      LIMIT
07030 23FA 20 1B    BFA      LOOP29
07040 23FC 44      LOOP28 LIP A
07050 23FD 01      DIV142 NOP
07060 23FE 01      DIV182 NOP
07070 23FF 16      TAB
07080 2400 D7 E6    LTA B  $E6
07090 2402 DE 12    LDB      $12
07100 2404 09      DBX      APPROPRIATE DELAY
07110 2405 26 15    BNE      LOOP30
07120 2407 CE 0000   LDB      $10000
07130 240A DF 12    LTB      $12
07140 240C 96 EF    LDA A  $EF      GOVERNOR OUTPUT
07150 240E D6 E6    LDA B  $E6      INCREMENTAL VALUE
07160 2410 18      RDB
07170 2411 81 E8    CUP A  $1E8      POSITION
07180 2413 23 02    BLC      LOOP29
07190 2415 86 E8    LDA A  $1E8      LIMIT
07200 2417 16      LOOP29 TAB
07210 2419 D7 EF    LTA B  $EF      GOVERNOR OUTPUT
07220 241A 20 02    BFA      LOOP31

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07330 241C DF 12 LOOP30 ITM 312
07340 241E 96 E4 LOOP31 LDA A 3E4 FLAG: WHAT STAGE ?
07350 2420 4A DEC A
07360 2421 97 E4 STA A 3E4
07370 2423 81 01 CUP A 3E01 HIGH PRES. COMPLETED ?
07380 2425 23 36 BUI LOOP33
07390 2427 86 EE LDA A 3EE NO: THEN INITIALISE AND GO
07300 2429 BD 25B7 JIP 101112
07310 242C 86 E7 LDA A 3EE7
07320 242E BD 25C4 JIP 101122
07330 2431 86 14 LDA A 3E14
07340 2433 BD 25D1 JIP 101132
07350 2436 96 06 LDA A 3E06 DIFFERENT DELAY TIME
07360 2438 B7 23F0 STA A 323F0
07370 243B B7 240D STA A 3240D
07380 243E 96 EF LDA A 3EF
07390 2440 C6 54 LDA B 3354 DIFFERENT TIME CONSTANT
07400 2442 F7 23E1 STA B 01942
07410 2445 C6 44 LDA B 3344
07420 2447 F7 23FD STA B 01942
07430 244A 7E 230C JIP LOOP35 GOTO SIMULATE HIGH PRES. STAGE
07440 244D 81 00 LOOP33 CUP A 3E00 YES: THEN DO LOW PRES. STAGE
07450 244F 27 43 BEQ LOOP34
07460 2451 96 EE LDA A 3EE
07470 2453 C6 80 LDA B 3380
07480 2455 10 STA
07490 2456 22 0C BHI 325
07500 2458 40 NEG A
07510 2459 16 TAB
07520 245A 44 LIP A
07530 245B 54 LIP B 75 GOES TO
07540 245C 54 LIP B THE REHEATER
07550 245D 1B RBA
07560 245E 16 TAB
07570 245F 86 80 LDA A 3380
07580 2461 10 STA
07590 2462 20 08 BRA 326
07600 2464 16 X25 TAB
07610 2465 44 LIP A 75 GOES TO
07620 2466 54 LIP B THE REHEATER
07630 2467 54 LIP B
07640 2468 1B RBA
07650 2469 C6 80 LDA B 3380
07660 246B 1B RBA
07670 246C 97 E3 X26 STA A 3E3 LOW PRES. INPUT
07680 246E 86 EC LDA A 3EEC INITIALISE AND GO
07690 2470 BD 25B7 JIP 101112
07700 2473 86 E8 LDA A 3EE8
07710 2475 BD 25C4 JIP 101122
07720 2478 96 16 LDA A 3E16
07730 247A BD 25D1 JIP 101132
07740 247D 86 03 LDA A 3E03 DIFFERENT DELAY TIME

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07750	247F	B7	23F0	STA A	123F0	
07760	2482	B7	240D	STA A	1240D	
07770	2485	96	E3	LDA A	1E3	
07780	2487	C6	54	LDA B	154	DIFFERENT TIME CONSTANT
07790	2489	F7	23E2	STA B	DIV82	
07800	248C	C6	44	LDA B	144	
07810	248E	F7	23FE	STA B	DIV182	
07820	2491	7E	23C0	JMP	LOOP35	GOTO SIMULATE LOW PRESS.
07830	2494	96	EE	LDA A	1EE	OUTPUT OF HIGH PRESS.
07840	2496	C6	80	LDA B	180	REFERENCE LEVEL
07850	2498	10		LDA		
07860	2499	22	14	BRI	P11	
07870	249B	40		NEG A		
07880	249C	44		LIP A		25 GOES STRAIGHT THROUGH
07890	249D	44		LIP A		
07900	249E	16		TAB		
07910	249F	D7	D5	STA B	1D5	
07920	24A1	96	EC	LDA A	1EC	OUTPUT OF LOW PRESS.
07930	24A3	C6	80	LDA B	180	
07940	24A5	10		LDA		
07950	24A6	D6	D5	LDA B	1D5	
07960	24A8	1B		ABA		
07970	24A9	16		TAB		
07980	24AA	86	80	LDA A	180	
07990	24AC	10		LDA		
08000	24AD	20	0F	BRA	P12	
08010	24AF	44		LIP A		
08020	24B0	44		LIP A		25 GOES STRAIGHT THROUGH
08030	24B1	97	D5	STA A	1D5	
08040	24B3	D6	EC	LDA B	1EC	OUTPUT OF LOW PRESS.
08050	24B5	86	90	LDA A	190	
08060	24B7	10		LDA		
08070	24B8	D6	D5	LDA B	1D5	
08080	24BA	1B		ABA		
08090	24BB	C6	80	LDA B	180	
08100	24BD	1B		ABA		
08110	24BE	97	EB	STA A	1EB	GOVERNOR RESPONSE GEN NO:2
08120	24C0	86	EF	LDA A	1EF	INITIALISE AND REPEAT ALL
08130	24C2	BD	25B7	JIP	101712	
08140	24C5	86	E6	LDA A	1E6	
08150	24C7	BD	25C4	JIP	101722	
08160	24C8	86	12	LDA A	112	
08170	24CC	BD	25D1	JIP	101732	
08180	24CF	86	0C	LDA A	10C	DIFFERENT DELAY TIME
08190	24D1	B7	23F0	STA A	123F0	
08200	24D4	B7	240D	STA A	1240D	
08210	24D7	86	03	LDA A	103	INITIALISE FLAG
08220	24D9	97	E4	STA A	1E4	
08230	24DB	86	01	LDA A	101	
08240	24DD	B7	23E1	STA A	DIV42	DIFFERENT TIME CONSTANT
08250	24E0	B7	23E2	STA A	DIV92	
08260	24E3	B7	23FD	STA A	DIV112	

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00270 24E6 B7 23FE      LTA A  DIV182
00280
00290      * TOTAL GOVERNOR RESPONSE IS AT 0084
00300      *
00310 24E9 7E 2692 B13  JOP      1702      WHICH SET WORKING
00320 24EC C6 80      16  LDA B  1180      REFERENCE LEVEL
00330 24EE 10      LBA
00340 24EF 22 12      BHI      B5
00350 24F1 40      NEG A
00360 24F2 97 D6      LTA A  106      STORE ERROR
00370 24F4 86 80      LDA A  1180
00380 24F6 D6 EB      LDA B  118      GOVERNOR RESPONSE GEN 2
00390 24F8 10      LBA
00400 24FA D6 D6      LDA B  106
00410 24FB 1B      ABA
00420 24FC 44      LIP A      TO FIND AVERAGE
00430 24FD 16      TAB
00440 24FE 86 80      LDA A  1180      REFERENCE
00450 2500 10      LBA
00460 2501 20 0C      BPA      B6
00470 2503 97 D6      LTA A  106
00480 2505 96 EB      LDA A  118      GOVERNOR RESPONSE GEN 2
00490 2507 10      LBA
00500 2508 D6 D6      LDA B  106
00510 250A 1B      ABA
00520 250B 44      LIP A      TO FIND AVERAGE
00530 250C C6 80      LDA B  1180      REFERENCE
00540 250E 1B      ABA
00550 250F 97 84      LTA A  184      TOTAL GOVERNOR RESPONSE
00560 2511 96 83      LDA A  183      INPUT TO THE SYSTEM
00570 2513 C6 80      LDA B  1180      REFERENCE
00580 2515 10      LBA
00590 2516 22 1A      BHI      X11
00600 2518 40      NEG A
00610 2519 97 D3      LTA A  103      STORE ERROR
00620 251B 86 80      LDA A  1180      REFERENCE
00630 251D D6 84      LDA B  184      GOVERNOR RESPONSE
00640 251F 10      LBA
00650 2520 16      TAB
00660 2521 96 D3      LDA A  103
00670 2523 10      LTA
00680 2524 22 06      BHI      X12
00690 2526 40      NEG A
00700 2527 C6 80      LDA B  1180
00710 2529 1B      ABA
00720 252A 20 1D      BPA      X13
00730 252C 16      TAB
00740 252D 96 80      LDA A  1180
00750 252F 10      LBA
00760 2530 30 17      BPA      X13
00770 2532 97 D3      LTA A  103      STORE ERROR
00780 2534 96 84      LDA A  184      TOTAL GOVERNOR RESPONSE

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08790 2536 C6 80          LDA B  7880      REFERENCE
08800 2538 10          LPA
08810 2539 16          TAB
08820 253A 96 D3        LDA A  7D3
08830 253C 10          LPA
08840 253D 22 07        PHI  N14
08850 253F 40          NEG A
08860 2540 16          TAB
08870 2541 86 80        LDA A  7880
08880 2543 10          LPA
08890 2544 20 03        BRA  N13
08900 2546 C6 80        LDA B  7880      N14
08910 2548 1B          BRA
08920 2549 97 F2        STA A  7F2      N13      ERROR INPUT OF SYSTEM
08930
08940      * TOTAL COST CALCULATION
08950
08960 254B 96 7C          LDA A  77C      GENERATOR NO:1
08970 254D 44          LCP A
08980 254E 97 7B        STA A  77B
08990 2550 96 6C          LDA A  76C      GENERATOR NO:2
09000 2552 16          TAB
09010 2553 48          ALL A
09020 2554 1B          BRA
09030 2555 D6 7B        LDA B  77B      GEN2 STINES HOPE EXPENSIVE
09040 2557 1B          BRA      TOTAL COST
09050
09060      * TOTAL COST TO BE DISPLAYED
09070
09080 2558 86 30          LDA A  7830
09090 255A C6 FF          LDA B  78FF
09100 255C F7 8010        STA B  78010      HOLDS ALL
09110 255F 4A          DEC A      M4
09120 2560 26 FD          BNE  M4
09130 2562 97 7B        STA A  77B
09140 2564 C6 30          LDA B  7830
09150 2566 B7 8012        STA A  78012
09160 2568 5A          DEC B      M0
09170 256A 26 FD          BNE  M0
09180 256C 86 30          LDA A  7830
09190 256E C6 F7          LDA B  78F7      CHOOSES S.H. NO:4
09200 2570 F7 8010        STA B  78010
09210 2573 4A          DEC A      M1
09220 2574 26 FD          BNE  M1      DELAY REQUIRED TO WRITE
09230      * READ AND WRITE TWICE
09240 2576 96 7B          LDA A  77B
09250 2578 C6 30          LDA B  7830
09260 257A B7 8012        STA A  78012
09270 257D 5A          DEC B      M2
09280 257E 26 FD          BNE  M2      DELAY REQUIRED TO WRITE
09290 2580 86 30          LDA A  7830
09300 2582 C6 F7          LDA B  78F7      CHOOSES S.H. NO:4

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09310 2584 F7 8010      STA B    $8010
09320 2587 4A          M3      DEC A
09330 2588 26 FD          BNE     M3
09340 258A 7E 2032      JNF     LOOP1
09350
09360
09370
09380
09390      SUBROUTINES
09400 258D B7 228A INIT1  STA A    $228A
09410 2590 B7 22A0      STA A    $22A0
09420 2593 B7 22BD      STA A    $22BD
09430 2596 B7 22C9      STA A    $22C9
09440 2599 39          RTS
09450 259A B7 2294 INIT2  STA A    $2294
09460 259D B7 22A2      STA A    $22A2
09470 25A0 B7 22B1      STA A    $22B1
09480 25A3 B7 22BF      STA A    $22BF
09490 25A6 39          RTS
09500 25A7 B7 2296 INIT3  STA A    $2296
09510 25AA B7 229E      STA A    $229E
09520 25AD B7 22B3      STA A    $22B3
09530 25B0 B7 22BB      STA A    $22BB
09540 25B3 B7 22CD      STA A    $22CD
09550 25B6 39          RTS
09560 25B7 B7 23DE INIT12 STA A    $23DE
09570 25BA B7 23F4      STA A    $23F4
09580 25BD B7 2411      STA A    $2411
09590 25C0 B7 241D      STA A    $241D
09600 25C3 39          RTS
09610 25C4 B7 23E8 INIT22 STA A    $23E8
09620 25C7 B7 23F6      STA A    $23F6
09630 25CA B7 2405      STA A    $2405
09640 25CD B7 2413      STA A    $2413
09650 25D0 39          RTS
09660 25D1 B7 23EA INIT32 STA A    $23EA
09670 25D4 B7 23F2      STA A    $23F2
09680 25D7 B7 2407      STA A    $2407
09690 25DA B7 240F      STA A    $240F
09700 25DD B7 2421      STA A    $2421
09710 25E0 39          RTS
09720
09730      SUBROUTINE CHECK
09740
09750      LIMITS OF FREQUENCY DEVIATION
09760      UPPER LIMIT= 8A IN HEX
09770      LOWER LIMIT= 76 IN HEX
09780
09790 25E1 81 8A      SUB     CNP A    $8A
09800 25E3 22 07      BHI     R21
09810 25E5 81 76      CNP A    $76
09820 25E7 23 03      BLC     R21

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09830 25E9 7E 2211      JNP      CHECK      IS WITHIN LIMITS
09840 25EC 86 80      P21      LDA A      1180      REFERENCE
09850
09860      *      INITIALISE ALL REGISTERS
09870      *
09880 25EE 97 E0      STA A      1E0
09890 25F0 97 E1      STA A      1E1
09900 25F2 97 E2      STA A      1E2
09910 25F4 97 E3      STA A      1E3
09920 25F6 97 E4      STA A      1E4
09930 25F8 97 E5      STA A      1E5
09940 25FA 97 E6      STA A      1E6
09950 25FC 97 E7      STA A      1E7
09960 25FE 97 E8      STA A      1E8
09970 2600 97 E9      STA A      1E9
09980 2602 97 EA      STA A      1EA
09990 2604 97 EB      STA A      1EB
10000 2606 97 EC      STA A      1EC
10010 2608 97 ED      STA A      1ED
10020 260A 97 EE      STA A      1EE
10030 260C 97 EF      STA A      1EF
10040 260E 97 F0      STA A      1F0
10050 2610 97 F1      STA A      1F1
10060 2612 97 F2      STA A      1F2
10070 2614 97 F3      STA A      1F3
10080 2616 97 F4      STA A      1F4
10090 2618 97 F5      STA A      1F5
10100 261A 4F      CLP A
10110 261B 97 F6      STA A      1F6
10120 261D 97 F7      STA A      1F7
10130 261F 97 F8      STA A      1F8
10140 2621 97 F9      STA A      1F9
10150 2623 97 FA      STA A      1FA
10160 2625 97 FB      STA A      1FB
10170 2627 97 FC      STA A      1FC
10180 2629 97 FD      STA A      1FD
10190 262B 7E 2032      JNP      LOOP1      GOTO START OF PROGRAM
10200 262E 86 30      SYN1      LDA A      1180
10210 2630 C6 03      LDA B      1103      4TH INPUT
10220 2632 F7 8006      STA B      18006
10230 2635 4A      C1      DEC A
10240 2638 26 FD      BNE      C1
10250 263B C6 30      LDA B      1180
10260 263E B6 8004      LDA A      18004      "ON" OR "OFF"
10270 2640 5A      C2      DEC B
10280 2643 26 FD      BNE      C2
10290
10300      *      READ AND WRITE TWICE
10310      *
10320 2640 86 30      LDA A      1180
10330 2643 C6 03      LDA B      1103      4TH INPUT
10340 2646 F7 8006      STA B      18006

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10350 2647 4A      C3      DEC A
10360 2648 26 FD      BNE      C3
10370 264A C6 30      LDA B      1130
10380 264C B6 8004      LDA A      18004      "ON" OR "OFF"
10390 264F 5A      C4      DEC B
10400 2650 26 FD      BNE      C4
10410
10420 2652 97 51      STA A      151      STORE AT ADDRESS 51
10430 2654 2B 06      BUI      11      BRANCH IF "ON"
10440 2656 96 6D      LDA A      16D
10450 2658 97 81      STA A      181      TOTAL GENERATION
10460 265A 20 35      BPA      13
10470      * SET NO:2 "ON" OR "OFF"
10480 265C 86 30      51      LDA A      1130
10490 265E C6 04      LDA B      1104      5TH INPUT
10500 2660 B7 8006      STA A      18006
10510 2663 4A      C5      DEC A
10520 2664 26 FD      BNE      C5
10530 2666 C6 30      LDA B      1130
10540 2668 B6 8004      LDA A      18004      "ON" OR "OFF"
10550 266B 5A      C6      DEC B
10560 266C 26 FD      BNE      C6
10570
10580      * READ AND WRITE TWICE
10590
10600 266E 86 30      LDA A      1130
10610 2670 C6 04      LDA B      1104      5TH INPUT
10620 2672 B7 8006      STA A      18006
10630 2675 4A      C7      DEC A
10640 2676 26 FD      BNE      C7
10650 2678 C6 30      LDA B      1130
10660 267A B6 8004      LDA A      18004      "ON" OR "OFF"
10670 267D 5A      C8      DEC B
10680 267E 26 FD      BNE      C8
10690
10700 2680 97 52      STA A      152      STORE AT ADDRESS 52
10710 2682 2B 06      BUI      12      BRANCH IF "ON"
10720 2684 96 7D      LDA A      17D
10730 2686 97 81      STA A      181      TOTAL GENERATION
10740 2688 20 07      BPA      13
10750 268A 96 7D      82      LDA A      17D
10760 268C D6 6D      LDA B      16D
10770 268E 1B      BPA
10780 268F 97 81      STA A      181      TOTAL GENERATION
10790 2691 39      83      RTI      RETURN
10800
10810      * SUBROUTINE 1YH2
10820
10830 2692 96 51      1YH2      LDA A      10051      FLAG
10840 2694 2B 15      BUI      14      BRANCH IF "ON"
10850 2696 96 FB      LDA A      1FB      GOVERNOR RESPONSE
10860 2698 C6 80      LDA B      1180

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10370	269A	10			LDA		COMPARE
10380	269B	22	08		BHI	09	
10390	269D	40			NEG A		
10900	269E	16			TAB		
10910	269F	86	80		LDA A	7180	REFERENCE
10920	26A1	10			LDA		
10930	26A2	7E	250F		JMP	B6	CONTINUE
10940	26A5	06	80	09	LDA B	7180	
10950	26A7	1B			ABA		
10960	26A8	7E	250F		JMP	B6	CONTINUE
10970	26AB	96	52	34	LDA A	950	
10980	26AD	2B	14		BHI	10	BRANCH IF "ON"
10990	26AF	96	EB		LDA A	9EB	
11000	26B1	06	80		LDA B	7180	REFERENCE
11010	26B3	10			LDA		COMPARE
11020	26B4	22	07		BHI	17	
11030	26B6	40			NEG A		
11040	26B7	16			TAB		
11050	26B8	86	80		LDA A	7180	REFERENCE
11060	26BA	10			LDA		
11070	26BB	20	03		BRA	13	
11080	26BD	06	80	37	LDA B	7180	REFERENCE
11090	26BF	1B			ABA		
11100	26C0	7E	250F	38	JMP	B6	CONTINUE
11110	26C3	96	EB	39	LDA A	9EB	
11120	26C5	7E	24EC		JMP	16	RETURN
11130					END		

SYMBOL TABLE

LOOP1	2032	MULTP1	2039	DIG1	2041	H1	204B	D0	2053
J1	207A	CONST1	2081	GPT	2085	HTC	20A9	OUT	20AB
HTYET	20AD	ANA	20B4	HOLD1	20BE	A0	20C8	H1	20D2
L1	20DC	MULTP2	20E6	DIG12	20EE	H2	20F8	D2	2100
J2	2127	CONST2	212E	GPT3	2132	HTC2	2156	OUT2	2158
HTYET2	215A	ANA2	2161	HOLD2	216B	A2	2175	H2	217F
L2	2189	MULTP0	2196	DIG10	219E	H0	21A8	D1	21B0
GPT2	21C1	PE0	21C4	LOOP2	21EE	LOOP3	220C	CHECK	2211
ANA0	2218	HOLD0	2222	A1	222C	H0	2236	L3	2240
LOOP4	2243	B10	224C	N2	225A	X1	2262	N4	2268
N3	226E	DFDOP	2270	LOOP7	2276	LOOP15	2278	B1	2281
A2	2285	DIV2	228C	DIV4	228D	DIV3	228E	LOOP8	22A8
DIV14	22A9	DIV18	22AA	LOOP9	22C3	LOOP10	22C8	LOOP11	22CA
LOOP13	22FA	N5	2310	N6	2318	LOOP14	2340	P1	2358
P2	236A	B11	2395	B12	239E	N22	23AE	N21	23B6
N24	23EC	N23	23C2	DFDOP2	23C4	LOOP27	23CA	LOOP25	23CC
B3	23D5	B4	23D9	DIV22	23E0	DIV42	23E1	DIV32	23E2
LOOP28	23FC	DIV142	23FD	DIV182	23FE	LOOP29	2417	LOOP30	241C
LOOP31	241E	LOOP33	244D	N25	2464	N26	246C	LOOP34	2494
P11	24AF	P12	24BE	B13	24E9	16	24EC	B5	2503
B6	250F	N12	252C	N11	2532	N14	2546	N13	2549
M4	255F	M0	2569	M1	2573	M2	257D	M3	2587
INIT1	258D	INIT2	259A	INIT3	25A7	INIT12	25B7	INIT22	25C4
INIT32	25D1	CUB	25E1	P21	25EC	DYN1	262E	C1	2635
C2	263D	C3	2647	C4	264F	C1	265C	C5	2663
C6	266B	C7	2675	C8	267D	C2	268A	C3	2691
SYN2	2692	C9	26A5	C4	26AB	C7	26BD	C8	26C0
SS	26C3								

APPENDIX : C

"Timing" Procedure of Software Program

Referring to Section 4.3.2, the principal of the method used here can be described as follows :

In establishing (CB2) on PIA (8010-8013) as output, this can be used to produce a pulse, i.e. CB2 goes low on first low-to-high E transition following an MPU Write into Output Register B; returned high by the next low-to-high E transition.

So through-out the program where ever an output is written into output register at address 8012 a pulse is produced. Therefore to measure run time at any segment of this program it is simply to measure time between two pulses at start and finish of that segment on a CRT.

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