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Reliability Analysis of Modular Multi-level Converters for High and Medium Voltage Applications

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Declaration

I herewith declare that the work produced here was either conducted by myself or where collaborative work occurred, it is indicated. All information has been attributed to its original source. This thesis has not previously been presented in identical or similar form to any other British or foreign examination board.

This work was conducted from October 2015 to January 2019 under the supervision of Professor Tim C. Green at Imperial College London.

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Abstract

Modular Multi-level Converters (MMC) are currently the favoured voltage source converter for High Voltage Direct Current (HVDC) systems because they feature a good combination of low power losses and high quality waveforms, with an increasing interest in applying multi-level converters for Medium Voltage Direct Current (MVDC) systems, where those same benefits are expected to be seen but perhaps not to quite the same extent. A further claimed benefit of the MMC is that inclusion of redundant modules yields high reliability, however, there is little formal analysis available concerning how to choose the degree of redundancy in the light of various assumed failure functions of individual components and the choices over the maintenance regime to be used.

This thesis considers two different reliability techniques to determine the required number of redundant Sub-Modules (SM) within an MMC for the cases of both constant-random and wear-out failure functions of SM components. Analysis is performed for both HVDC and MVDC since they differ markedly in the number of SMs present and the scale of redundancy that might be expected. The availability of an MMC is calculated using the *k-out-of-n* model for constant random failures and with a discrete-time Monte Carlo simulation performed on Markov Chains to calculate the availability of an arm due to wear-out failures.

The reduced number of SMs within an arm designed for MVDC results in the number of redundant SMs required to maintain a given level of availability being a large relative addition to the basic arm. This lowers the efficiency of the converter due to greater number of SMs in the conduction path of each arm. This initial finding was for redundancy designed for use

with periodic preventative maintenance, which was the approach taken in HVDC. To improve efficiency at MVDC, it is proposed to change to reactive maintenance which will allow a smaller number of redundant SMs within each arm while maintaining comparable availability.

To improve further the efficiency of an MMC at MVDC, an MMC topology is proposed that features a mixture of SM voltages (and combinations of full- and half-bridges) within each arm. High voltage-rated IGBT modules, which have low-loss conduction characteristics, are used to generate the majority of the arm voltage and a small number of lower voltage-rated IGBT modules, which have low-loss switching characteristics, are used to refine the arm voltage through smaller voltage steps and pulse-width modulation. Power loss and efficiency, as assessed through circuit simulation, are compared for the proposed mixed-SM-voltage MMC and conventional MMCs operated at the same power rating and the same total harmonic distortion. All the converters included redundant modules, based on reactive maintenance, to achieve the same availability. The mixed-SM-voltage MMC has been found to have the highest efficiency of the case-study designs. The control and operation of the mixed-SM-voltage MMC was validated through experimental testing of a lab-scale prototype.

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Nomenclature

Abbreviations

AAC	Alternate Arm Converter
AC	Alternating Current
Al-Caps	Aluminium Electrolytic Capacitors
cdf	cumulative distribution function
DC	Direct Current
FIT	Failure In Time
HV	High Voltage
HVDC	High Voltage Direct Current
LCC	Line Commutated Converter
MLC-Caps	Multi-Layer Ceramic Capacitors
MMC	Modular Multi-level Converter
MPPF-Caps	Metallized Polypropylene Film Capacitors
MTBF	Mean Time Between Failure
MTTF	Mean Time To Failure
MTTR	Mean Time To Repair
MV	Medium Voltage
NPC	Neutral Point Clamped
PCB	Printed Circuit Board
pdf	probability density function
PWM	Pulse Width Modulation
SM	Sub-Module
SOC	State Of Charge
THD	Total Harmonic Distortion
VSC	Voltage Source Converter

Symbols

A	Availability
β	Shape Parameter
$f(t)$	probability density function
$F(t)$	cumulative distribution function
$h(t)$	Hazard Rate
λ	Failure Rate
N	Total Number of Sub-modules in an arm
q	Unavailability (no time dependence)
$q(t)$	Unavailability (time dependence)
$R(t)$	Reliability Function
R_{SM}	Redundant Sub-modules
t	time
T_M	Maintenance Interval

1 Introduction

The small but significant and accelerating increase in global temperatures since the turn of the century has led to governments around the world acting to reduce the volumes of greenhouse gasses being emitted into our atmosphere. The signing of the Paris Agreement strengthened the global response by agreeing to maintain global temperature increases below 2 °C compared to pre-industrial levels [1]. Since the signing of the Paris Agreement, virtually every country in the world is now conscious of the need to meet the energy trilemma: energy affordability, energy sustainability and energy security. The energy trilemma addresses the need to decarbonise the energy sector whilst maintaining affordability for the consumer and not compromising on the security of supply. There is also growing demand for electricity as other sectors, such as heating and transport, reduce their reliance on fossil fuels by moving towards electrical alternatives.

To diversify the renewable generation portfolio and diversify the demand profile across a larger population and area, interconnectors between countries are being installed. These also improve the security of supply. Most interconnectors are hundreds and perhaps thousands of kilometre in length and increasingly they use cables rather than overhead lines to transmit power between countries either to create sub-sea routes or buried cables in sensitive land corridors. The most economical technology to use for long distance transmission is High Voltage Direct Current (HVDC), with Voltage Source Converters (VSC) emerging as the favoured converter technology due to their ability to control both active and reactive power flow on the AC side and effect power reversal through current not voltage reversal on the DC side. Also, as the energy sector moves towards a more sustainable energy mix, it is noticed that most renewable energy

sources are non-synchronous and to connect to an AC network requires an interface through power electronic converters.

The VSC that is now the most popular (for transmission purposes) is the Modular Multi-level Converter (MMC) which was first reported shortly after the turn of the century, [2], and entered commercial service with Siemens a decade later and is now offered in various forms by all major manufacturers.

The MMC consists of hundreds of Sub-Modules (SM) connected in series in each six arms (two per phase). The MMC is able to produce essentially distortion-free waveforms by inserting into or removing from the conduction path the voltage of each SM such that stepped approximation of sinusoidal voltage waveforms are created. The modular design of the MMC allows a number of redundant SMs to be placed within each arm so as to tolerate a small number of SM failures between maintenance events. This is believed to produce a converter with the necessarily small outage time required of these major pieces of infrastructure. However, there is little historical reliability data available publicly for MMCs which is in contrast to the older Line-Commutated Converters (LCC) where extensive data has been collected by operators and analysed through working groups of Cigré. This is in part a result of the strong competition between manufacturers of VSC who continue to innovate in circuit design and control. In contrast, the LCC technology is mature and offerings of LCC have converged around a largely common design.

The availability of an MMC is dependent on the repair time and how fast or frequently maintenance can be performed; the faster maintenance is performed, the more available the converter. HVDC applications tend to have periodic pre-planned maintenance to keep operational costs low since planned outages attract much lower penalty payments than unplanned outages. The approach adopted to maintaining continuous operation between planed maintenance events despite the failure of a number of SMs, is to provide redundant SMs, an approach that mirrors the provision of redundant thyristors in LCC.

Following the successes at HVDC, application of power electronic converters at Medium Voltage DC (MVDC) is an emerging market spurred on by forecast increases in electric vehicle

charging points and battery storage within distribution networks. There is, however, little industrial experience to date and there is no sense that the best topology or maintenance strategy for MVDC converters has been identified as might be argued for MV drive systems. Many open questions remain for which supporting research is needed.

1.1 High Voltage DC Technologies

The bulk of any nation's power system remains AC and where DC is a better choice for a route, it is necessary to install AC-DC conversion to provide the interface at each end. There are two broad categories of technology used for power conversion between AC and DC, which are known as Line Commutated Converters (LCC) (also known as Current Source Converters (CSC)) and Voltage Source Converters (VSC). They use different arrangements of inductors and capacitors to provide a stiff current source or stiff voltage source on the DC-side, but are also implemented with different semiconductor devices [3] [4].

1.1.1 Line commutated converters

Of the two HVDC technologies, LCC is the more mature with the first commercial LCC link introduced in the early 1950s between the island of Gotland and the Swedish mainland using mercury-arc valves [4]. In 1967, one of the mercury-arc valves within the Gotland link was replaced with a thyristor valve, which increased the transmission capacity by 50 % [5]. Following its introduction to LCCs, the thyristor quickly became the favoured technology due to its ability to achieve high power ratings and its robustness during faults [6].

In an LCC, a short pulse of current is applied to the gate of each thyristor to "fire" it and power flow is controlled by varying the firing angle of each valve [3]. The thyristor switches off when the current flowing in the valve reaches zero because of the conditions in the rest of the system (so-called line commutation), with the consequence that LCCs rely on a strong AC system to force the thyristor out of conduction [3].

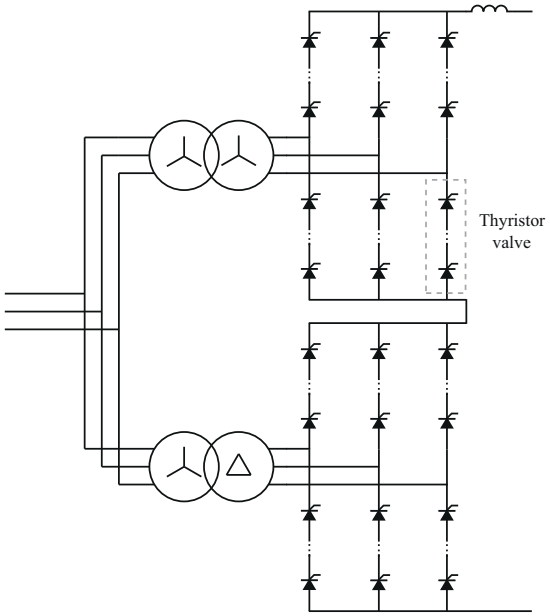


Figure 1.1: 12-pulse thyristor line commutated converter.

A typical LCC is shown in Figure 1.1, where two LCCs are connected in series phase shifted 30° apart using transformers star-star and star-delta. This 12-pulse arrangement has less harmonic ripple observed in the DC-link than the the 6-pulse arrangement and the 5^{th} and 7^{th} harmonics currents on the AC-side are also reduced (essentially eliminated) such that smaller filters are required [3] [7].

1.1.2 Voltage source converters

The first commercial VSC-HVDC was introduced in 1997; again the route between Gotland and the Swedish mainland was the site [4]. VSCs use self-commutated semiconductor switches with full control of turn-on and turn-off, thereby, achieving full control of active and reactive power flow through the converter. This allows VSCs to support and operate with weak AC grids. Modern VSCs also generate significantly less harmonic distortion than LCCs resulting in less, or often no, filtering and achieving an overall smaller converter footprint [8]. These advantages are particularly telling when considering offshore converter applications and renewable energy

sources, where space is at a premium and power generation is intermittent resulting in the need to often restart an isolated AC network of, for instance, wind turbines.

The rapid advancement of VSC-HVDC was made possible with the introduction of the Insulated Bipolar Gate Transistor (IGBT), a self-commutated power electronic switch, at current handling and voltage blocking ratings of the magnitude needed for HVDC applications [9]. Other semiconductor technologies, notably the gate turn-off thyristors (GTO) and its close relation, the integrated-gate commutated thyristor (IGCT) were used in the early development of VSCs in relatively low voltage applications such as MV motor control applications [10] [11] and early VSC-HVDC, notably the "HVDC Light" range from ABB.

The 2-level converter, as shown in Figure 1.2, has series connected semiconductor switches within each arm to achieve higher converter voltage ratings [4]. As noted above, the switches were originally GTO or IGCT but now would be expected to be IGBT. Series connected IGBTs require tightly controlled simultaneous switching of all IGBTs within the same arm otherwise delayed switching in some devices will result in very large stress on a small number of devices, resulting in cascading failure of IGBTs [9]. Increasing the voltage and power rating of VSCs by increasing the number of series devices is challenging and increasingly difficult for this reason. The 2-level VSC is called that because the voltage of each phase can adopt one of two values

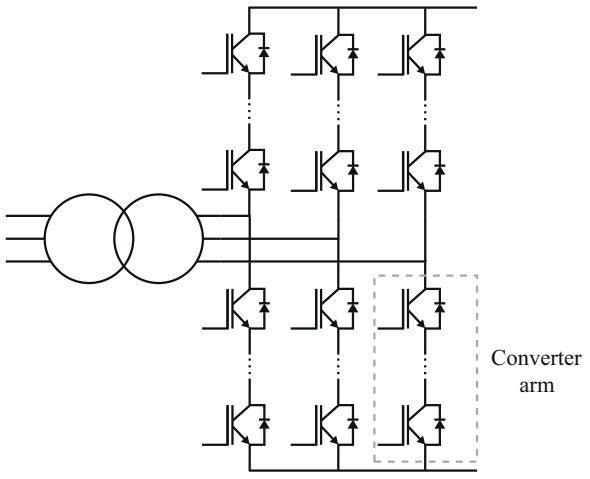


Figure 1.2: 2-level voltage source converter.

depending on which arm is switched on. Pulse Width Modulation (PWM) is then used to create output waveforms composed of sinusoidal AC pulse modulation terms. The high frequency switching required for PWM to achieve low harmonic distortion results in high power loss, with AC-side and DC-side filters may be needed to remove unwanted frequency components [10] [12].

1.1.3 Multi-level voltage source converters

The 2-level converter was the most widely used VSC until new topologies such as the 3-level Neutral Point Clamped (NPC) converter and 5-level flying capacitor converter were introduced [13]. The increased number of voltage levels within an arm lowers the switching frequency required of each IGBT, resulting in reduced power loss and increased efficiency of the converter. The more voltage levels the converter can generate, the fewer (or smaller) harmonics are created reducing the need for AC- and DC-side filters and allowing the converter station to be smaller [4].

NPC and flying capacitor VSCs improve waveform quality compared to the 2-level converter, but suffer from poor scalability in power rating due to the numbers of some components not scaling linearly (and increasingly complex control) whereas series-connected IGBTs in 2-level converters do scale linearly [14].

1.2 Modular Multi-level Converter

The Modular Multi-level Converter (MMC) is currently the favoured VSC-HVDC topology. It was first discussed as an idea in 2003 [2] and introduced commercially in 2010 in the Trans Bay Cable project [15]. The MMC improves AC and DC waveform quality by increasing the number of voltage levels within each arm; the number of components in the circuit grows only linearly with the power rating. The levels are created by having hundreds of SMs in series in each arm. Each SM contains a large-valued capacitor that holds a near-constant voltage, where that voltage can be inserted into the conduction path or bypassed to generate a stepped approximation of a sinusoidal voltage waveform. There is no need for simultaneous switching;

each SM is free to switch at any time and the IGBT voltages are clamped by the local SM capacitor. With a high number of levels the approximation of a sinewave is very good and the unwanted harmonics observed within AC and DC waveforms are all but eliminated and often the AC and DC filters can be dispensed with. The efficiency of the MMC is improved compared to 2- or 3-level VSC topologies due to the low switching frequency of each IGBT, which typically switch at only a little above line frequency rather than at the carrier frequency of a PWM system and yet the MMC still achieves good AC and DC waveform quality [16] [17].

The most common MMC topology is shown in Figure 1.3, in which half-bridge SMs are connected in series within six arms, with two arms per phase to generate stepped sinusoidal voltage waveforms [2]. The improved power rating of MMCs when compared to previous VSC topologies is because large numbers of SMs can be placed in series without impediments such as needing simultaneous switching or suffering poor scaling of component numbers and therefore with only a relatively low voltage blocking capability of each IGBT, a high DC-link voltage can be supported.

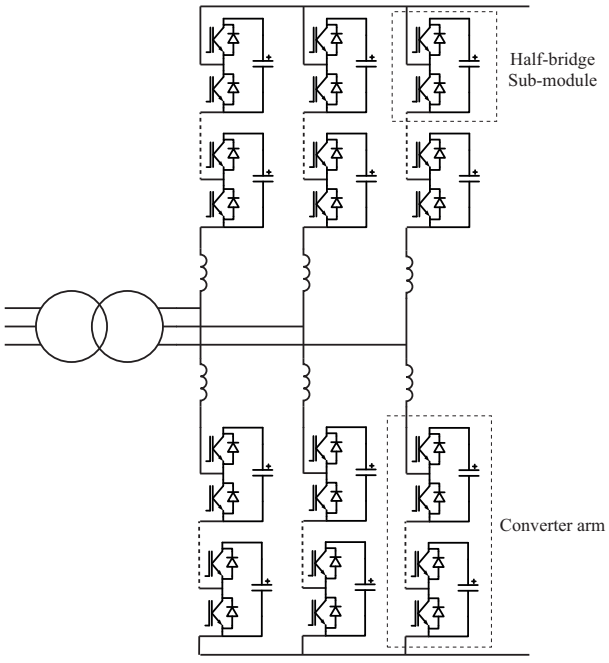


Figure 1.3: Modular multi-level converter with half-bridge sub-modules.

1.2.1 Full-bridge and half-bridge sub-modules

The two most commonly encountered SM topologies for an MMC are the half-bridge and full-bridge as shown in Figure 1.4, although it should be noted that many further types have been proposed in the literature as summarised in, for instance, [18].

The half-bridge SM, shown in Figure 1.4 (a), has two IGBTs that switch the capacitor in and out of conduction to output the SM voltage. The capacitor is gradually discharged when current flowing through an arm is positive and the capacitor gradually charges when the arm current flowing through the arm is negative (where the definition of positive current is the flow from the mid-point of the two IGBTs in Figure 1.4 (a) and completing the circuit by flowing through the bottom connector).

The full-bridge SM, shown in Figure 1.4 (b), has twice the number of the IGBTs compared to the half-bridge SM but has the ability to output a negative voltage. As well as giving further control and balancing options, the ability to insert negative voltage facilitates control of fault current through the converter in the event of a DC-side short circuit, whereas, with a half-bridge there would be uncontrolled fault current through the anti-parallel diodes [19].

Although the full-bridge SM offers control of DC fault current, the half-bridge SM is the more common choice of SM because the halved number of IGBTs (and halved number in the conduction path too) leads to half the conduction loss compared to the full-bridge SM [10].

Although, as noted above, there are many further SM topologies available, the half- and full–bridge SM are the ones that have been adopted commercially to date and so these are the types considered in this thesis.

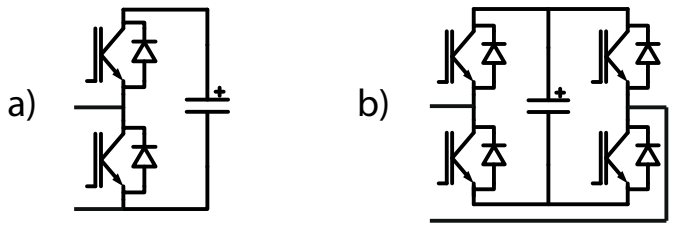


Figure 1.4: Sub-module topologies showing: a) half-bridge and b) full-bridge.

1.2.2 Control architecture

There are several different control techniques for MMCs, with early control strategies developed using rotating frame transformations, e.g. Direct-Quadrature transformation (dq0) [20] [21] [22]. There are however limitations with the dq0 control approach, as some papers consider converter arms as controllable voltage sources which neglects the individuality of each SM, or other approaches model every SM within each arm of the converter which increases the complexity of the control considerably [21] [22].

An alternative approach (which is used within this thesis), is using state-space control techniques, with an example of the control structure used for an MMC shown in Figure 1.5. This example was taken from [20]. The controller is based on several layers of single-model controllers. The energy management at the top (or outer) level is where balancing current reference terms are generated to maintain the energies in each arm close to their design values. The main current references (to which the balancing currents are added) are determined by the power demand. For this computation, the magnitude and angle of the AC grid voltage are needed and these are usually provided by a Phase Lock Loop (PLL). The current controller then determines the voltages that should be applied to achieve the required currents. These voltage references are, in turn, fed into the final part of the controller, the low-level controller which determines how many SM voltages need to be inserted and which SMs will be selected for that duty. The low-level controller is also where SM rotation is performed, so that at periodic intervals the

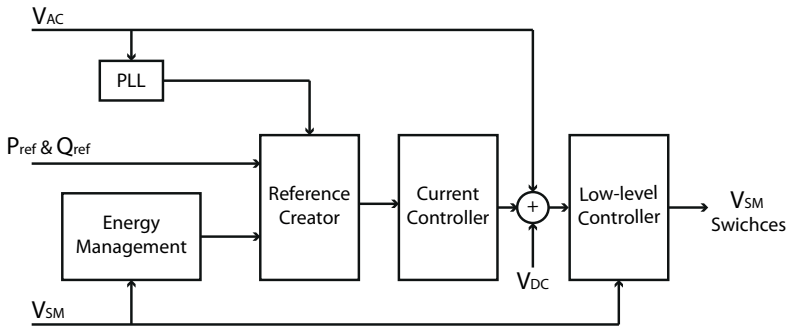


Figure 1.5: Example control structure of an MMC [20].

choice of which SMs are deployed is changed so that the charge (or voltage) of the SMs in each are balanced. For cases where some PWM-like SM switching is required in addition to the basic staircase waveform, the low-level controller will also assign a duty-cycle to the last SM inserted in each arm.

1.3 Motivation and Research Questions

The MMC consists of hundreds of SMs within each arm and this structure bring benefits, as noted above, in power losses and waveform quality which have caused its rise to prominence. Another important benefit is that the modularity of the structure allows inclusion of redundant SMs, and so long as the number of redundant SMs within each arm has been estimated well, it will normally be possible to maintain operation between maintenance windows despite individual SM failures. However, the reliability of VSC-HVDC systems is currently not well documented in terms of field data, perhaps because of the recent rise in application, the small number of VSC-HVDC systems in operation around the world and the continuing commercial competition on performance. It has also not been widely studied from the point of view of how to choose a design configuration to achieve a particular reliability target at system level. The research to be reported in this thesis set out to address some of the issues through analysis of MMC availability in terms of failure rates of the major components.

The MMC is also a promising technology for MV applications but here the trade-off between switching frequency and waveform quality needs to be re-examined because of the much smaller number of SMs needed at MV compared to HV. The smaller number of SMs within each arm also calls for a re-examination of redundancy and maintenance strategies since the cost and power loss penalty of including redundant SMs are proportionately higher than at HV.

The research questions that are to be investigated in this thesis are as follows:

- What method is best to quantify the number of redundant SMs required within an MMC for HVDC and MVDC applications to achieve high availability (e.g., $>$ 99.99 %)?

- What advantages might there be in performing reactive maintenance rather than periodic preventative maintenance for various MMC designs for MVDC applications?
- What is the most efficient MMC design for MVDC applications with inclusion of redundant SMs?
- Does an MMC with a mixed set of SM voltages in each arm create a better design in terms of power losses and waveform quality?
- What is the best control strategy and modulation technique for an MMC with mixed-SM-voltages in each arm?
- How should redundancy be employed in a mixed-SM-voltage MMC to maintain high availability (e.g., $>$ 99.99 %)?
- How do the results of a mixed-SM-voltage MMC compare with those of a conventional MMC at MVDC?
- How well do the results of theoretical analysis and simulation models of a mixed-SM-voltage MMC compare to experimental results from a lab-scale converter?

1.4 Thesis Structure

The structure of this thesis will be as follows:

Chapter 2 presents a literature review of various approaches to analysing and enhancing reliability for power electronic converters as well as assessing the reliability of existing HVDC systems. A discussion of alternative modular converters and cascaded multi-level converters is made, comparing volume, efficiency and tolerance to DC faults. From this literature survey, the most important factors in reliability of HVDC systems are determined and an analysis of the failure rate of the various electronic components within an MMC is performed. Reliability

equations for different failure profiles are examined and a reliability method is outlined for use in subsequent chapters.

Chapter 3 outlines the design, construction and commissioning of a 15 kW MMC in the Maurice Hancock Lab at Imperial College London. The MMC uses MOSFETs as the semiconductor switches and can be reconfigured to have half- or full-bridge SMs and those SMs can be set to operate at different voltages. The lab-scale converter is used to generate experimental results to validate the theoretical analysis and simulation modelling.

Chapter 4 analyses availability a HVDC MMC is expected to achieve in terms of the number of redundant SMs for different periodic maintenance intervals when used. The impact of wear-out failures is compared against constant random failures, with two different analytical methods used for the respective failure profiles. A comparison is made of the the number of redundant SMs required to achieve a given availability for a case-study converter under various assumptions concerning constant random and wear-out failures.

Chapter 5 compares three different MMC designs for MVDC applications and quantifies the number of redundant SMs required in each case. A comparison between periodic preventative maintenance and reactive maintenance is made to determine the best maintenance strategy to reduce the number of redundant SMs within each arm. A power loss study is also performed on the three MMCs to consider how much of an impact redundant SMs have on efficiency at MVDC given the small number of SMs used with a relatively low DC-link voltage.

Chapter 6 presents an MMC topology for MVDC applications to improve power loss and efficiency while maintaining good waveform quality. It uses SMs of two different voltage ratings within each arm and is described as a mixed-SM-voltage MMC. A control algorithm is proposed that deploys the two types of SM to achieve good waveform quality and ensures each SM has its voltage held close to its nominal voltage. Simulation results of the proposed converter are compared with the three MMCs studied in Chapter 5. The simulation results of the proposed MVDC converter are also compared with experimental results using the lab-scale MMC outlined in Chapter 3 operated with the controller developed within Chapter 6. The power loss

and efficiency of the mixed-SM-voltage MMC are compared with corresponding results from Chapter 5 for standard MMCs.

Chapter 7 reports the conclusions from the research, highlighting the method used to quantify the number of redundant SMs required and the choice of maintenance strategy. Power losses and efficiencies of various MMCs for MVDC applications are compared with the results obtained for a mixed-SM-voltage MMC. Future work is also presented within this chapter.

Appendix A records the validation of the Monte Carlo population size used with the Markov Chain models described in Chapter 4, Chapter 5 and Chapter 6 by comparing results with a case where an analytical method is available.

Appendix B shows an extended set of experimental results for a mixed-SM-voltage MMC introduced in Chapter 6, using the lab-scale MMC presented in Chapter 3.

1.5 Publications

1. J. Wylie. P. D. Judge and T. C. Green, "Modular Multi-level Converter for Medium Voltage Applications with Mixed Sub-module Voltages within Each Arm," 2018 8th IEEE PES Innovative Smart Grid Technologies Conference Europe (ISGT Europe), Sarajevo, 2018, pp. 1-6.

2. J. Wylie, M. C. Merlin and T. C. Green, "Analysis of the effects from constant random and wear-out failures of sub-modules within a modular multi-level converter with varying maintenance periods," 2017 19th European Conference on Power Electronics and Applications (EPE'17 ECCE Europe), Warsaw, 2017, pp. P.1-P.10.

3. M. M. C. Merlin, P. D. Judge, G. Chaffey, J. Wylie and T. C. Green, "Soft-switching of the director switch in the alternate arm converter using blocked sub-modules," 2017 IEEE 18th Workshop on Control and Modeling for Power Electronics (COMPEL), Stanford, CA, 2017, pp. 1-7.

4. J. Wylie, C.E. Sheridan, T.C. Green, "Analysis of the Number of Redundant Sub-modules Required within Modular Multi-level Converters for Different Maintenance Periods," 2016 2nd CSEE International Conference on High Voltage Direct Current (HVDC2016), Shanghai, 2016, pp. 1-6.

2 Literature Review

This chapter reviews the literature relevant to reliability studies of MMCs in order to shape the work that was conducted and describe the context further for future chapters within this thesis. The main focus of this chapter is on the state of the art reliability techniques for power electronic converters for high and medium voltage applications within the power industry. This includes investigating converter topologies and different maintenance strategies undertaken to maintain high availability. The reliability of different power electronic components and existing HVDC systems are studied, as well as detailed reliability theory and analysis techniques which are used in future chapters.

The structure of this chapter will be as follows; there will be a brief introduction to the availability of DC interconnectors and a review of the largest contributors to the failure of HVDC links. There will be discussion on power losses and how the efficiency of IGBT modules are effected under different operating conditions. A review of alternative modular multi-level and cascaded multi-level converters is made, discussing fault blocking, power loss and volume of different converter topologies. Different reliability strategies are then discussed within MMCs and a review of the reliability of the main components within a SM in terms of failure rate. There is also a detailed explanation of different reliability calculations techniques for constant random and wear-out failures, with a summery of the chapter to conclude.

2.1 Availability of DC Interconnectors

To maintain high availability of HVDC links, incentive mechanisms are in place for interconnector owners, where the availability incentive give a potential 2 % increase or decrease of the total interconnectors foretasted revenue [23]. The pilot project to consider availability incentives was NEMO, the interconnector between Great Britain and Belgium [24] [25]. The availability incentive framework was drafted for Ofgem and the Belgian regulator CREG, by Sinclair Knight Merz energy consultants [24]. The model was materially updated by GHD consultants in 2016, to ensure the model structure and source data continues to be relevant to present-day interconnectors [26].

The availability incentive was designed to ensure developers maintain high availability of interconnectors, whilst consumers benefit from increased security of supply [23]. The availability target for an interconnector is dependent on design and specification, with two links identical apart from cable length resulting in different availability targets [24]. The NEMO interconnector was calculated within [24] to have an availability value in the range of 97.1 % to 97.8 %, which did not include converter transformers or AC switch gear. The final availability incentive awarded for NEMO was 97 % availability, after taking them into consideration [27].

The failure rate used for the converter within the Sinclair Knight Merz model is based on historical data from LCC converters, due to the maturity and length of service LCCs have been in operation. The Mean Time Between Failures (MTBF) for VSC converters has been assumed to be the same value as onshore LCC converters, highlighting that vendors will mitigate reliability concerns of VSC converters depending on respective designs [24].

The MTBF is defined as the summation of Mean Time To Failure (MTTF) and the Mean Time To Repair (MTTR), as shown in Equation 2.1. The availability is then determined by dividing the MTTF by the MTBF, as shown in Equation 2.2. This shows availability is dependent on MTTR, with faster repair times improving availability.

$$MTBF = MTTF + MTTR \tag{2.1}$$

$$Availability = \frac{MTTF}{MTBF} \tag{2.2}$$

The repair time of HVDC interconnectors in the event of a fault is dependent on time of year and weather conditions [28]. For offshore applications it is beneficial to have planned periodic maintenance during the summer months due to the low number of specialised repair vessels which are in high demand, with calmer seas through the summer months [29] [30].

The Offshore Transmission Owner (OFTO) tender for The Crown Estate licences for offshore wind farms around the UK require an availability of 98 %. The incentive rewards up to 5 % of annual revenue for OFTOs achieving above 98 % availability, with penalties up to 10 % for those who fall short [31] [32]. The availability of the OFTO licence includes any planned and un-planned down-time for maintenance.

The Crown Estate wind farms currently use AC to transmit power to the mainland due to distances, where during Round 3 Dogger Bank was introduced which requires VSC-HVDC to make the project economically viable due to the distance of sub-sea cables required [33] [34]. Dogger bank is currently under planning stages with construction expected to commence in 2022, with the announcement in July 2018 that Norfolk Vanguard has planning accepted to use HVDC to transmit power to the mainland [35] [36].

This shows an increase in availability from VSCs are required to meet The Crown Estate availability licence agreements and a change to how the availability incentive model calculates the failure rate of VSCs is also required, due to historical LCC data being used within the availability calculation for VSCs to-date. This is due to the semiconductor material of VSCs being different to those used in LCC converters.

2.1.1 Line commutated converter links

The Cigré advisory group B4.04 annually collect reliability performance data of HVDC systems in operation around the world. Every two years Cigré publish statistics on the frequency and duration of forced outages of HVDC systems over the two year period, as well as a cumulative average of forced outages since 1983 [37].

The B4.04 advisory group splits forced outages of HVDC systems into six categories which include: AC and auxiliary equipment (AC-E), valves (V), control and protection (C&P), DC equipment (DC-E), transmission line or cable (TL) and other (O). A comparison of the six categories is shown in Table 2.1 for the data gathered between 2009 to 2014, which is from the three most recent Cigré surveys published to date [37] [38] [39].

It is shown in Table 2.1 that most failures occur from AC-E, with transformers accounting for most failures within the category [38]. Although transformers account for most failures, it is stated within [37], that there has been significant improvements in transformer reliability within recent years and expect improvements to continue. The largest downtime of HVDC systems is from TL, with the category contributing to the second least cause of forced outages of HVDC systems. This is reflective in the average duration of a forced outage, where TL has the largest impact on downtime of a HVDC systems and therefore availability of a link.

Although TL has the largest average downtime, less than 10 % of cable faults are caused by natural hazards, where natural hazards refer to cable faults such as insulation breakdown [40]. The largest contributor to cable faults is commercial fishing, which accounted for 40 % of

Table 2.1: Total number of line commutated converter system failures between 2009 to 2014 [37] [38] [39].

	AC-E	V	C&P	DC-E	TL	O
Total Number of Failures	477	275	301	152	141	145
Downtime (Hours)	10,753.3	6,849.5	1,981.1	1,776.1	17,173.4	751.5
Average Duration of Fault (Hours)	22.5	24.9	6.6	11.7	121.8	5.2

submarine power cable failures across the world to date (2015) [40]. The Cigré working group B1.10 looks into submarine cables and came to the same conclusions, where between the years 1990 and 2005 the total number of submarine cable faults caused by internal cable failures was only 8.16 % [41]. Bottom-tending fishing gear, like trawl nets and dredges, is what accounted for most commercial fishing incidents, with anchoring accounting for the second most frequent cause of submarine cable faults [40].

To reduce accident risk of submarine cable faults, cables are buried for water depths down to 600 m [40]. Burying cables is the preferred method of cable protection, but if this is not possible due to environmentally sensitive coastline or crossing another cable already buried for example, there are other options such as placing a concrete mattress or rocks on top of the cable to add protection [42].

2.1.2 Voltage source converter links

There is less historical data available for VSC systems when compared to LCC systems due to the maturity of the technology. The most recent Cigré survey on the reliability of HVDC systems includes two VSC links for the first time [37]. The two HVDC links are Caprivi in Namibia and EstLink1 connecting Estonia and Finland, with reliability performance data available for the years between 2013 to 2014.

Forced outages are categorised the same as within Section 2.1.1, with Table 2.2 showing the total number of failures per category, downtime in hours and average duration of a fault [37]. Over the two year period, the most failures for VSC-HVDC systems were from the converter,

Table 2.2: Total number of failures between 2013 to 2014 for EstLink1 and Caprivi [37].

	AC-E	V	C&P	DC-E	TL	O
Total Number of Failures	7	8	4	3	7	1
Downtime (Hours)	95.9	667.9	7.3	7.8	15.8	2.2
Average Duration of Fault (Hours)	13.7	83.5	1.8	2.6	2.3	2.2

with EstLink1 contributing to 7 of the 8 failures. The average duration of a converter failure is also higher than in LCC systems shown in Table 2.1. The other notable difference between LCC and VSC systems is TL average duration of a fault is considerably lower for VSC systems than for LCC systems. It should be noted that TL failures within Table 2.2 are all from the Caprivi link, which use overhead lines [43]. Overhead line faults can be transient from flash over during storms, whereas cable faults tend to be permanent and require maintenance [44].

Although some conclusions can be made from Table 2.2, the data only covers two VSC-HVDC systems over two years, therefore, some trends may be specific to certain links and may not be representative of all VSC-HVDC systems.

With less than 10 % of cable faults caused by internal failures, the TL data gathered for LCC systems within Table 2.1 is believed to be more representative of what would be observed for VSC systems. The most likely causes for VSC-HVDC system failures are therefore believed to be transmission lines and cables, AC transformers from historical data from LCC-HVDC systems and the VSC converter due to the most recent Cigré survey data showing the converter having the largest fault duration out of all categories.

2.2 Power Loss of IGBT Modules and Converter Efficiency

Power loss within VSC converters are dominated by IGBT modules conducting and switching within an arm, where the IGBT and diode have different power loss characteristics during switching and conducting. The power loss of an IGBT can be split into three categories; IGBT conduction losses, IGBT turn-on losses and IGBT turn-off losses, with the summation the total power loss of an IGBT as shown in Equation 2.3. The IGBT turn-on and turn-off losses are the switching losses of the IGBT switching in and out of conduction. The conduction losses of an IGBT are dominated by the load current, duty cycle and junction temperature, whereas, the switching losses of an IGBT are dependent on load current, DC-link voltage, junction temperature and switching frequency [45]. If the switching frequency or blocking voltage of the

IGBT are high, then the power losses are high from increased energies switching in and out of conduction at an increased frequency [45].

$$P_{IGBT} = P_{Conduction} + P_{Turn-on} + P_{Turn-off} \tag{2.3}$$

The power loss of the free-wheeling diode within the IGBT module can be split into two categories; diode conduction losses and diode reverse recovery, as shown in Equation 2.4. The reverse recovery losses are from the diode switching between its conduction state to its blocking state, where stored charge must be discharged before the diode can block reverse voltage [45].

The combination of both IGBT and diode give the total power loss for an IGBT module, as shown in Equation 2.5.

$$P_{Diode} = P_{Conduction} + P_{Reverse\,Recovery} \tag{2.4}$$

$$P_{IGBT\,Module} = P_{IGBT} + P_{Diode} \tag{2.5}$$

To simulate power losses of different power electronic converter topologies, it is possible to model IGBT modules in Matlab-Simulink to estimate the efficiency of each converter, keeping the gate voltage and temperature constant to maintain fair comparisons. For conduction losses, the V-I characteristics for both the IGBT and diode are transformed from the manufactures data sheets into look-up tables in Matlab-Simulink, where conduction losses are calculated for the respective IGBT and diode when they are conducting, using Equation 2.6.

$$P_{Conduction} = I^2R + V_{CE(Intersect)} \tag{2.6}$$

To calculate the switching losses for the IGBT and diode within a module, a similar process is performed as for the conduction losses, where the E-I characteristics for the IGBTs turn-on and turn-off and the reverse recovery of the diode are transformed from the manufactures data

sheets into look-up tables in Matlab-Simulink. The switching losses are then calculated using Equation 2.7, where the change in energy, E, is divided by the time-step of the simulation, T, to obtain the instantaneous switching loss for the respective IGBT and diode.

$$P_{Switch} = \frac{\Delta E}{\Delta T} \tag{2.7}$$

To determine the total power losses for an IGBT module, Equation 2.5 is used, with the efficiency calculated using Equation 2.8, where $Power_{Rated}$ is the rated power of the converter and $Power_{Loss}$ is the total calculated power loss of the converter by summing together the power losses from each IGBT.

$$Efficiency = \frac{Power_{Rated} - Power_{Loss}}{Power_{Rated}} \tag{2.8}$$

A comparison between the 2-level converter with series connected IGBTs in each arm and the MMC was made in [46], where it was concluded that the IGBTs dominate conduction losses within 2-level converters, whereas the diodes dominate conduction losses within MMCs due to the series connected nature of IGBT modules within the 2-level converter operating at the same power factor. The switching losses of IGBTs and the reverse recovery diodes within MMCs are lower when compared to the 2-level converter, making the MMC the more efficient converter within their study. The biggest saving in power losses between the MMC and 2-level converter come from reduced switching losses within MMCs [46]. This is due to the 2-level and 3-level VSCs having high switching frequencies (1-2 kHz) because of the reduced number of voltage levels the converters can generate. The MMC has a much lower switching frequency (100-150 Hz) due to the ability to generate stepped sinusoidal waveforms, therefore, reducing the distortion within the AC and DC waveforms [47].

IGBT modules within MMCs contribute to power losses from constant conduction and switching within converter arms [10] [48] [45]. The more SMs within each arm, the higher the conduction losses of an MMC from more IGBTs connected in series. The switching losses within an

MMC is affected by the number of voltage levels a converter arm can generate; the more voltage levels within an arm, the lower the switching losses due to the reduced switching frequency required to generate the same waveform quality.

IGBT modules currently used for high and medium voltage applications come in a range of voltages from 600 V to 6,500 V. Different blocking voltage IGBTs have different conduction and switching characteristics, with lower voltage rated IGBTs generally having higher current ratings. Switching energies of IGBTs increase with blocking voltage, which results in higher voltage rated IGBTs having high switching losses if high switching frequencies are required [10]. The choice of IGBT module is therefore dependent on application and converter specification, as higher blocking voltage IGBTs have good conduction losses, but poor switching losses, whereas, lower blocking voltage IGBTs have poor conduction losses but good switching losses [10].

MMCs for HVDC applications tend to use higher blocking voltage IGBTs due to high number of SMs required within each arm to achieve the DC-link voltage with less numbers of SMs per arm. High numbers of SMs result in conduction losses dominating within each arm, therefore, higher blocking voltage IGBTs are preferred. The high number of voltage levels MMCs can generate for HV applications results in low switching frequencies being required, resulting in low switching losses [49].

MV converters have lower DC-link voltages and are currently designed for applications such as motor drives and electrification of ships [50] [51]. MMCs for MV applications have the advantages of higher efficiencies and filter free waveforms when compared to 2-level and 3-level converters with similar power ratings [46] [52]. The preferred IGBT blocking voltages to use for MMCs at MV are 1.2 kV and 1.7 kV modules, which have good switching loss characteristics, which is advantageous at MV due to the reduced number of voltage levels available within an arm, resulting in higher switching frequencies than at HV [52]. Currently power electronic converters for shipping applications are considering 4.5 kV modules, which is comparable with modules used for HV applications [50] [53]. This will lead to higher switching losses and may not be the best IGBT module to use for MV applications.

2.3 Alternate Multi-level Converters

Since the introduction of the MMC, there have been several variations of the topology introduced to lower power losses, improve operation during DC faults and reduce the converter footprint by reducing the filter requirement or reducing the number of SMs within a converter.

The most common SM choice within MMCs is the half-bridge due to its low conduction loss when compared to other SM topologies such as the full-bridge, due to only having two IGBT modules within each SM. The draw-back with the half-bridge MMC is the inability to control fault current through their anti-parallel diodes in the event of a DC-side short circuit, whereas, full-bridge SMs are able to insert a negative voltage to suppress fault current.

2.3.1 Alternate modular multi-level topologies

The hybrid MMC as it is known and shown in Figure 2.1, uses half- and full-bridge SMs within the same arm to offer tolerance to DC faults, with improved efficiency when compared to an MMC using purely full-bridge SMs to achieve tolerance to DC faults [19]. When compared to the half-bridge MMC, there are higher conduction losses, but a considerable saving when compared to the full-bridge MMC. The converter footprint of the hybrid MMC is similar to the equivalent half- and full-bridge MMCs, due to the same number of SMs being within an arm, where the volume of a SM is dominated by the capacitor size for a given energy [54]. The same number of voltage levels are also available using the hybrid MMC when compared to conventional MMCs, resulting in the same AC-side waveform quality if the same IGBT modules are used in each.

The AC-side Cascaded H-Bridge (ACCHB), shown in Figure 2.2, is a topology which uses full-bridge SMs within each phase of the AC current path, with the main power stage of the converter generated from a 2-level converter [55] [56]. The full-bridge SMs within each phase act as active filters, injecting harmonic voltages to refine the stack voltage, reducing the AC-filter size. The 2-level converter consists of series conducting IGBTs, which are able to switch

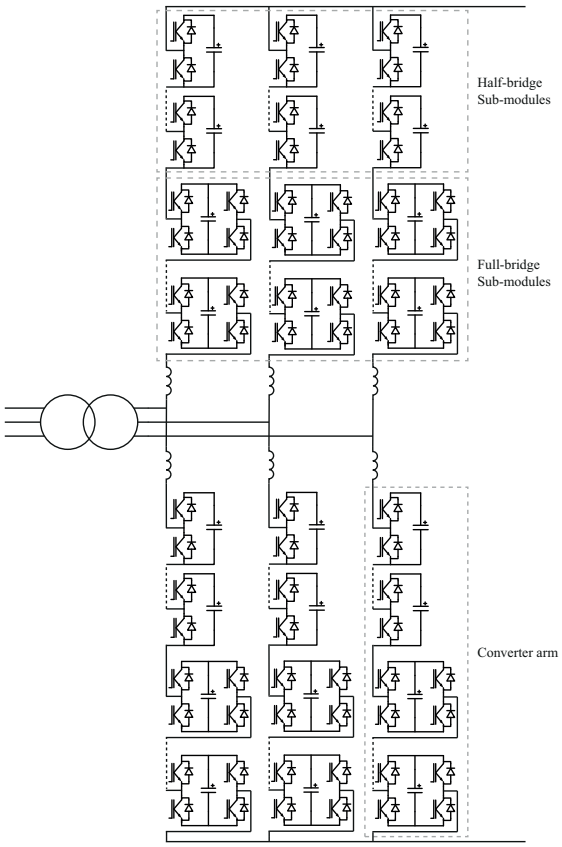


Figure 2.1: Hybrid modular multi-level converter.

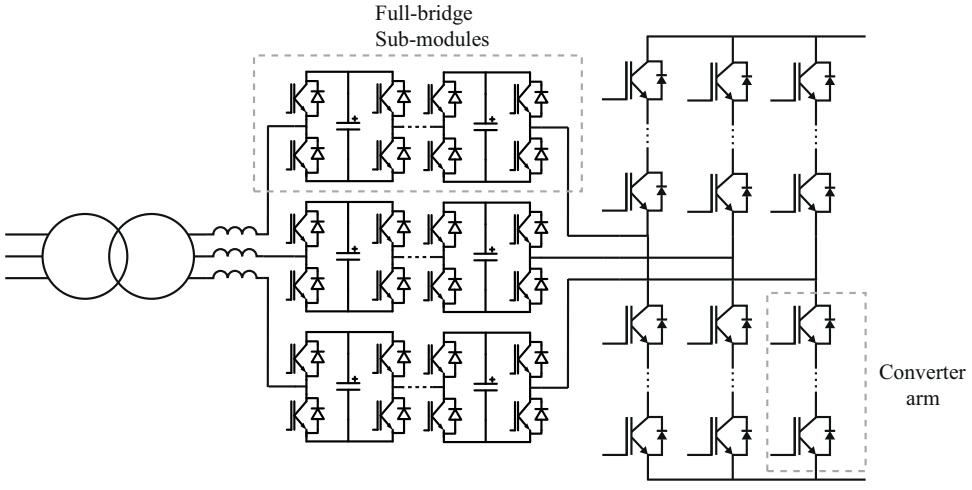


Figure 2.2: AC-side cascaded H-bridge.

slower than conventional 2-level converters due to the active filter component within ACCHBs, which reduces the switching losses when compared to the 2-level converter. The ACCHB, however, requires more complex control switching when compared to the MMC to ensure all IGBT modules simultaneously switch if higher power ratings are required, which is a constraint of the 2-level converter [46]. The footprint of the ACCHB is reduced when compared to the MMC of the same power rating, due to a quarter of SMs required to achieve the same number of voltage levels when compared to an MMC [55]. Overall, the ACCHB has a reduced converter footprint, is tolerant to DC faults when compared to the half-bridge MMC, but has greater conduction losses due to series conducting IGBTs within the 2-level part of the converter [55]. The half-bridge MMC is still more efficient than the ACCHB.

The Alternate Arm Converter (AAC), shown in Figure 2.3, is a multi-level converter with series connected full-bridge SMs and series connected IGBTs within the same arm [57] [58]. The series connected IGBTs are known as director switches and act similar to the operation of a 2-level converter by switching complementary arms in and out of conduction, where the blocking voltage of the director switch is only great enough to block the voltage of an arm. To allow energy balancing between upper and lower arms, the AAC requires an overlap period where both upper and lower arms within the same phase are conducting simultaneously around the zero voltage level to ensure soft current commutation [59]. The footprint of the AAC is reduced when compared to an MMC of same power rating due to the reduced number of SMs required to achieve the same DC-link voltage within each arm, with the director switch supporting the remaining DC-link voltage [56].

When the AAC is compared to the ACCHB, the AAC has a larger converter footprint due to roughly double the number of SMs required to achieve the same power rating, with the AAC also having large DC-side capacitors due to large 6-pulse ripples (although the extended overlap AAC has improved this limitation [58]). The AAC and ACCHB both offer tolerance to DC faults, with the AAC more power efficient than the ACCHB, due to fewer semiconductors within the conduction path and a reduced fundamental switching frequency [55]. Both the

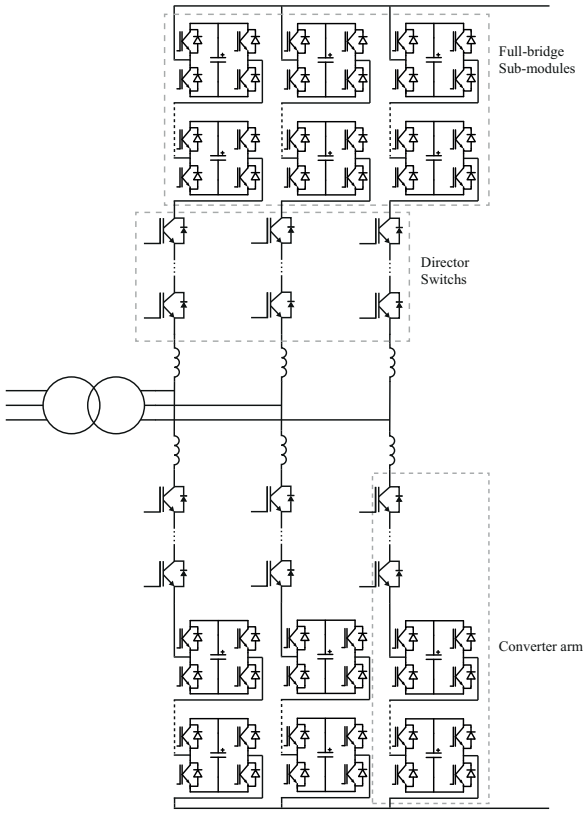


Figure 2.3: Alternative arm converter.

ACCHB and AAC have smaller converter footprints than the MMC and are both more efficient when compared to the full-bridge MMC which is also DC fault tolerant. The half-bridge MMC is still the more efficient converter due to the reduced number of semi-conductor devises within the conduction path, but is not tolerant to DC faults.

The Power Groups (PG) MMC, introduced in [60] and shown in Figure 2.4, uses a mixture of VSC and LCC technology with the combination of full-bridge SMs and thyristors within the same arm. LCC-HVDC systems which use thyristors are inherently more efficient than VSC-HVDC systems using IGBTs, but have less control over active and reactive power flows. The PG MMC splits full-bridge SMs into groups within an arm, with a thyristor positioned across each group to offer a low impedance bypass branch when the SMs are not required to generate arm voltage. The SMs within the PG generate voltage when the thyristors are in their blocking

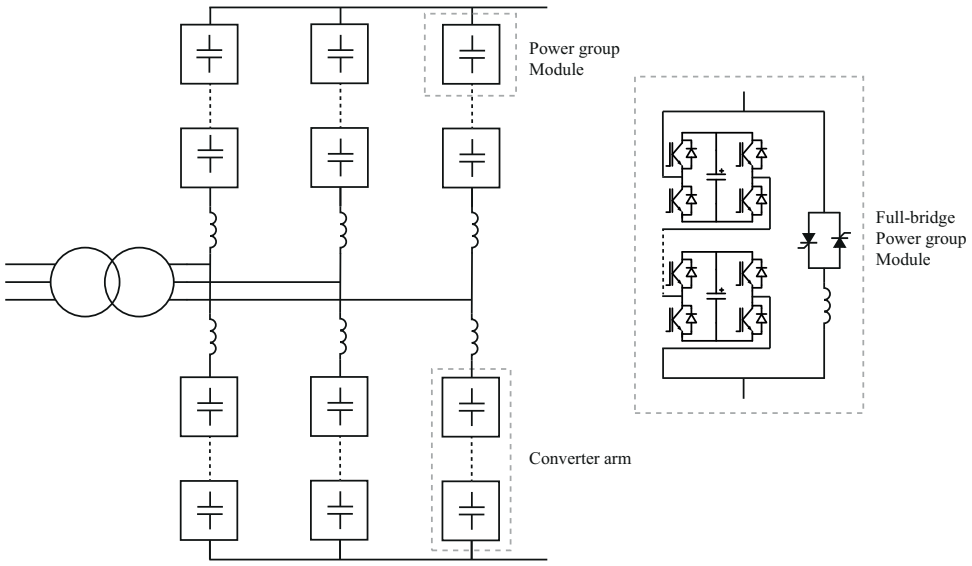


Figure 2.4: Power group modular multi-level converter.

state, with the turn-on and forced commutation of the thyristors achieved by using the SMs within the PG. The use of full-bridge SMs within the PG MMC achieves tolerance to DC faults, giving the PG MMC the controllability of VSC converters and efficiencies from LCCs [61]. The PG MMC is ~ 30 % more efficient compared to equivalent power rated half-bridge MMC, which cannot achieve DC fault tolerance with the same waveform quality achieved [61]. It is expected, however, that the PG MMC will have a larger converter footprint due to the increased number of semiconductor devices, SMs and associated auxiliary equipment when compared to equivalent fault tolerant converters: hybrid MMC, ACCHB, AAC and full-bridge MMC.

There is discussion within [62] to use a single full-bridge SM rated to half the voltage of the half-bridge SMs within the same arm for an MMC of half-bridge SMs. This allows intermediate voltages to be generated in the same arm, with the full-bridge SM acting as an additional auxiliary voltage, but at a cost of an additional SM that is not required to maintain the DC-link voltage. There are no power loss studies performed within [62], with high (50 kV) SM voltages selected which would require series conducting and simultaneously switching IGBT modules within each SM, incurring high switching and conduction losses. An alternative approach to

include intermediate voltage levels within the same arm of an MMC is introduced in [63]. Two different voltages are generated from the same SM, where four IGBTs are configured to switch two different capacitors in and out of conduction to produce two different voltages to support the DC bus. For this to work, each IGBT has to be rated for the highest voltage generated from the larger of the two capacitors, so there is very little saving in power losses due to the same IGBT being used for both low and high voltage SM output.

The use of different voltages within the same arm has the potential to reduce the fundamental switching frequency within the converter from the increased number of voltage levels available.

2.3.2 Cascaded multi-level topologies

There are other multi-level topologies where converters use cascaded full-bridge SMs of different voltages within the same arm [64] [65] [66] [67] [68] [69]. The more full-bridge SMs of different voltages within the same arm, the increased number of voltage levels available. To achieve multiple voltage levels within the same phase, each SM requires an isolated DC power source or bank of series connected capacitors of different values to achieve the different voltage levels [65]. The greater the number of voltage levels the converter can achieve, the lower the distortion within the output voltage and current waveforms, reducing the fundamental switching frequency and the power supported from each semiconductor within each phase. There are various voltage arrangements that can be made within the series connected full-bridge SMs, such as the ternary and quasilinear sequences, which have both shown to be more efficient than equal rated full-bridge SMs within the same phase [66] [68].

The capacitor-clamp cascade multilevel converter is introduced in [67], where each SM is a 3-level capacitor-clamp SM with a different isolated DC source to each SM. This has the advantage of generating greater number of voltage levels from each SM, reducing the number of semi-conductor devices within the converter compared to the equivalent cascaded full-bridge converters with different voltages.

Although efficiency is improved to some extent for cascaded multi-level converters compared

to the 2-level converter due to reduced switching frequency from increased voltage levels created, the main disadvantage is their circuit complexity, with a high number of semiconductor switches which require switching in a dedicated sequence when compared to the 2-level converter. Cascaded multi-level converters also require a great number of isolated DC power sources or banks of series connected capacitor dividers to achieve the desired SM voltage within the converter. These disadvantages make modular converters more attractive than cascaded multi-level converters, with modular multi-level converters able to introduce redundancy at a small cost to volume and losses, which is not the case for unequal cascaded multi-level converters.

2.4 Reliability Strategies for Modular Multi-level Converters

The modular design of the MMC makes it possible to place a percentage of redundant SMs within each arm of the converter to tolerate a small number of SM failures between maintenance [70] [71]. If a SM fails, the MMC would not be able to support the DC-link voltage and would either have to operate under sub-optimum conditions reducing the DC-link voltage, or turn the DC-link off to protect the MMC from further failures [16]. There are two typical ways of implementing redundant SMs; standby redundancy and active redundancy [10] [71].

The number of redundant SMs required within an MMC is an estimated value within literature, with a range from 8 % to 25 % of the total number of SMs within an arm [70] [71] [72] [73] [74]. The optimum number of redundant SMs for different maintenance strategies has not been investigated in detail and is therefore an interesting question that will be investigated within this thesis.

2.4.1 Standby redundancy

Standby redundancy is where redundant SMs are in a dormant state and are electrically bypassed and only become active and switch into conduction once a SM within an arm has failed [12]. This results in the failure rate of redundant SMs being considerably lower than

active SMs within the same arm. Redundant SMs using standby redundancy require a two-time-use mechanical switch for the SM to enter conduction and bypass in the event of the SM failing. A process of pre-charging the SMs capacitor is also required, otherwise transients in other SMs and oscillations in the output current are observed as the SM charges during insertion [71]. Standby redundancy within [71] operates with no mechanical switch by placing redundant SMs in a blocking state, where the capacitor voltage of redundant SMs are controlled to zero. This allows seamless transition of power within the converter in the event of a SM fault, but increases conduction losses within the converter due to redundant SMs conducting within each arm and are therefore not in a dormant state. This increases the failure rate of redundant SMs, but not to the same failure rates observed for active SMs within an arm, due to no switching being performed on redundant SMs.

2.4.2 Active redundancy

Active redundancy rotates redundant SMs with all SMs within an arm, sharing the total system load across all SMs [72]. This results in the failure rate of redundant SMs being equal to all operating SMs within the same arm. Performing active redundancy lowers the switching frequency and operating voltage of each SM compared to standby redundancy, due to more SMs than are required generating the DC-link voltage [12]. This, therefore, lowers the failure rate of all SMs within the same arm due to the reduced stresses and junction temperatures observed across all SMs within an arm [12]. Failed SMs are bypassed in the event of a fault by using switches or inherent capability of pressure contact semiconductor packages to fail to stable short circuit, allowing continuous operation of the converter.

2.4.3 Alternate redundancy techniques

Different periodic preventive maintenance is considered in [73], but only constant random failures are investigated and doesn't study the effects from wear-out of components. Wear-out of SMs within an MMC is studied in [75], which shows wear-out failures have an impact on the

overall life-expectancy of an MMC, but results show the reliability of a converter arm decreases as the number of redundant SMs increases. Similar results are shown in [76] for constant random failures, where increasing redundancy within a converter arm decreases the availability of an MMC. The method that should be used to calculate the reliability of SMs is discussed in Section 2.6, where it was found the wrong formula was used to calculate the availability of a converter arm in [76], therefore yielding the wrong results.

There are also different redundancy techniques that can be performed, where in [77] redundant SMs are not exclusively within each arm, but are placed within each phase of the converter. This allows a reduction in redundant SMs by 17.5 % and a reduction of 33.33 % if redundant SMs are shared across all arms within the converter [77]. Although in theory there are considerable reductions in redundant SMs used within an MMC, the practicality of switching redundant SMs into conduction between arms is not considered within the paper, and is therefore not believed to be a practical option within this thesis. Another redundancy technique using no redundant SMs is considered in [78], by shifting the neutral point within the converter in the event of a SM fault in a particular arm.

When evaluating different redundancy techniques, it is believed standby redundancy is not practical and reliable enough to implement when compared to active redundancy due to the operation of a two-time switch and the practicality of having the capacitor within redundant SMs pre-charged, therefore, active redundancy is performed within this thesis.

2.5 Reliability of Power Electronic Components

The main component within an MMC is the SM, with a detailed half-bridge SM shown in Figure 2.5. There are two IGBTs which switch the capacitor in and out of conduction, with an auxiliary power supply used to charge the SM capacitor during start-up. There is also a thyristor and bypass switch which are active under fault conditions to either protect the SM or bypass the SM in the event of a SM component failure. The control system sends command

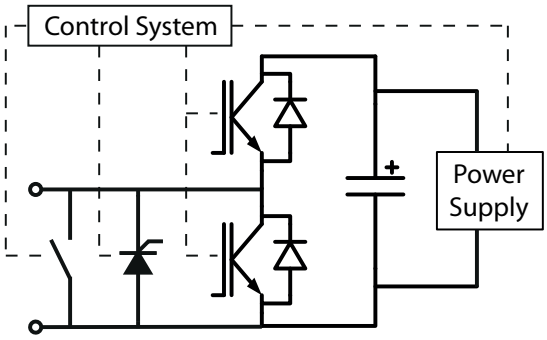


Figure 2.5: Half-bridge sub-module.

signals to various components within the SM and transmits SM voltages and currents to the central controller.

If any component within a SM fails, the SM is bypassed and taken out of service unless redundancy is available. Some manufactures have redundant power supplies within the SM to ensure SMs don't fail during start-up. A study within [75] investigated the impact of the bypass switch and thyristor on the overall failure rate of a SM, where it was concluded it had a negligible impact on the overall failure rate due to low probability of operation. This thesis therefore assumes the IGBTs, SM capacitor and control electronics are the only significant components that contribute towards the failure of a SM during normal operation.

The failure rate of a SM is shown in Equation 2.9, where two IGBTs, capacitor and control electronics are summed together, where λ_{SM} is the failure rate of the SM, λ_{IGBT} is the failure rate of an IGBT, λ_{Cap} is the failure rate of a capacitor and $\lambda_{Control}$ is the failure rate of the control electronics. Equation 2.9 shows if any component fails in the SM, the entire SM fails and is bypassed. The failure rate is defined by many manufacturers in terms of Failure In Time (FIT), with 1 FIT equalling 1 failure per billion (10^9) hours, as shown in Equation 2.10.

$$\lambda_{SM} = 2\lambda_{IGBT} + \lambda_{Cap} + \lambda_{Control} \tag{2.9}$$

$$\lambda = \frac{FIT}{10^9} \tag{2.10}$$

2.5.1 IGBTs

The main cause of failure within an IGBT module is from wirebond and solder joints which are used to electrically, mechanically and thermally connect the semiconductor chips to the baseplate of the module [79] [80]. The reliability of a wirebond is dependent on the operating temperature of the module and the mechanical stresses induced within the wirebond from differences in thermal expansion of the wirebond material and underlying device. The stresses on the materials are continuously applied during switching, where repetitive mechanical stress leads to cracks in the solder joints and bondwires. The bondwires near the edge of the IGBT module show the largest deformation due to higher temperatures observed towards the edge of the module compared to the centre [80].

Increased cooling can improve the reliability of an IGBT module, where dropping the temperature from 120 °C to 80 °C increased the MTBF by a factor of 2.7 within [10], with a cost of larger heat sinks and reduced power density. Similar results were found in [81], where at 80 °C the module failed after 85,360 cycles whereas at 110 °C the module failed after 28,900 cycles. At 80 °C it was concluded that solder fatigue was the cause of failure, whereas at 110 °C it was concluded bondwire lift-off was the cause of the module failing.

The failure rate of an IGBT module is also dependent on how exposed to cosmic rays each module is, where ABB conducted a study to show devices at higher altitudes have higher failure rates [82]. The data provided by ABB show IGBTs operating at a variety of temperatures and altitudes, with results showing the failure rate having a small dependence due to temperature but a strong dependence due to applied voltage [82]. It should be noted that unlike literature above, the small dependence on temperature within [82] shows the failure rate decrease with the rise in temperature. This is most likely due to the design of ABBs press-pack IGBT modules which don't use bondwires and use pressure contacts instead. The applied temperature during different altitude tests was 25 °C, which although is the worst case operating temperature tested for the ABB press-pack IGBT module, it is not a realistic temperature expected to observe during operation of an MMC.

The failure rate of an IGBT module is also dependent on the applied voltage in reference to the rated voltage of the module, with the failure rate increasing as the applied voltage increases [10] [82]. There is however no correlation between different voltage blocking IGBTs and an increase in failure rate observed [82].

The life-expectancy of an IGBT module was calculated as 25 years within [83], where the operating temperature was 80 °C and the applied voltage was the rated voltage of the module. The reliability of an IGBT module is dominated by the operating temperature, with similar lifetime estimates of IGBT modules concluded in [84].

Redundant SMs within an arm would increase the reliability of each IGBT module if active redundancy is performed by reducing the switching frequency. Increasing the number of SMs within an arm can also reduce the applied voltage to each SM, which reduces the junction temperature further within IGBT modules. The combination of reduced switching and lower applied voltage increases the reliability of a SM if active redundancy is performed.

2.5.2 Capacitors

Capacitors are most susceptible to failure when compared to other power electronic components such as semiconductors, Printed Circuit Boards (PCB) and solder joints within a SM [85]. There are three main capacitors made of different materials, which include Aluminium Electrolytic Capacitors (Al-Caps), Multi-Layer Ceramic Capacitors (MLC-Caps) and Metallized Polypropylene Film Capacitors (MPPF-Caps) [86]. All three capacitors have advantages and disadvantages, with the choice of capacitor being determined by the desired application. Al-caps can achieve the highest energy density for the lowest cost per joule, but have relatively high Equivalent Series Resistance (ESR), low current ratings and high wear-out due to the evaporation of the electrolyte with time [86]. MLC-Caps are small in volume with a wide frequency range and can operate under high temperatures, but MLC-Caps have lower capacitance and voltage ratings and are higher in cost [86]. MPPF-Caps are good for high voltage applications and provide low ESR, ripple current and high reliability. MPPF-Caps are, however, large in volume and require

cooler operating environments [86].

MLC-Caps and MPPF-caps have self-healing properties with the dielectric breakdown over time resulting in a reduction in capacitance [86] [87]. This results in high stability for MLC-Caps and MPPF-Caps, with the failure rate dependent on the dielectric material and not capacitance of the capacitor. The failure of MLC-Caps and MPPF-Caps is when the capacitance falls below the minimum operating requirement, with MLC-Caps failing short-circuit and MPPF-Caps failing open-circuit [86]. MLC-Caps as a result have a life-expectancy of thousands of years, with MPPF-Caps having a life-expectancy around 180,000 hours (20.5 years) [88] [89]. In contrast, Al-Caps fail when the dielectric evaporates, causing deterioration of sealing materials over time [86] [90]. As a result, Al-Caps are most likely to have a maximum life-expectancy of 15 years [90].

The capacitors used within the half-bridge structure of a SM are MPPF-Caps, due to their advantages of self-healing, high capacitance, low ESR and ability to operate with high voltages. This leads to the capacitor being the dominate size of a SM, with the volume of a capacitor dependent on the energy requirement for the converter [54].

2.5.3 Control System

The control system for a SM is located on a PCB within the SM, which is used to send signals to gate drivers and transmit SM voltage and current to the central controller. Within the control electronics, Al-Caps are used within the circuitry to smooth localised DC-DC power supplies [90]. It was determined within [75] that the limiting factor for the reliability of a SM is the control electronics and not the IGBT or SM capacitor. Through discussions with GE Grid Solutions, this thesis also assumes the reliability of the control electronics is the limiting factor regarding the overall failure and wear-out rate of a SM. An estimated failure rate for the control electronics of a SM was determined as 1,000 FIT. Table 2.3 shows the components and failure rates associated within an MMC SM, where it is shown the control electronics has the highest failure rate.

Table 2.3: Components and associated FIT data for a sub-module.

Component	Manufacture	Part Number	FIT
IGBT	Infineon	FZ1500R33HE3 [91]	200
Capacitor (MPPF)	EPCOS	B25750H2448k004 [92]	100
Control Electronics Subsystem	Various	N/A	1,000

2.6 Reliability Theory

This section describes the methodology and equations used to calculate the availability of power electronic components within an MMC. The bathtub curve, as shown in Figure 2.6, is regarded as a good representation of the failure of power electronic components over time [93].

The initial high failure rate with respect to time is known as infant failures or "burn in" of components. These failures are caused from manufacturing errors and defects in materials used, where these failures quickly decrease with time as manufacturing processes improve. Most infant failures are only observed during R&D or commissioning stages of large projects. Constant failures with respect to time during a components "useful life" is due to random failures, with different components exerting different constant failure rates due to different materials being able to withstand different temperatures and stresses. The increase in failure rate with respect

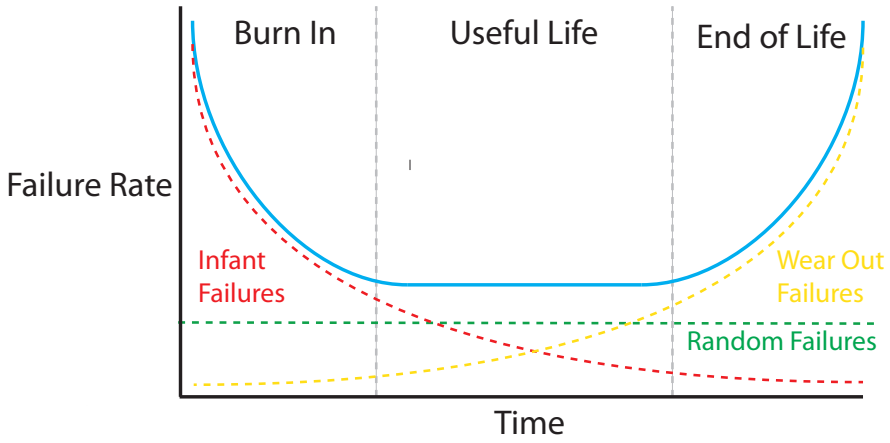


Figure 2.6: Bathtub curve.

to time is due to wear-out of components at an increased rate as components move towards their "end of life". Wear-out failures are only observed towards the end of the life-expectancy, with most projects designed to be decommissioned or renovated before this period in time. The summation of these three discrete sections represent the life-expectancy of a power electronic component over time, which is known as the bathtub curve. Most assumptions within literature do not include infant failures and wear-out failures in the study of MMCs, as they assume infant failures are detected during commissioning, and the life-expectancy of the project is assumed to be complete before wear-out of components take effect [73] [77] [85] [94].

The life-expectancy of HVDC systems are expected to have at least 40 years of service, which is more than the life-expectancy of some components within a SM, making wear-out an important factor to consider [95].

The assumptions within this thesis therefore are infant failures are not observed during the "useful life" of a converter, due to the commissioning stage of HVDC systems eliminating these failures, but wear-out failures are considered alongside constant random failures due to the life-expectancy of some power electronic components being shorter than the planed life-expectancy of HVDC links.

2.6.1 Probability and reliability equations

The cumulative distribution function (cdf) *F(t)*, as shown in Equation 2.11, represents the probability that the observed value T will be less than or equal to t. The derivative of the cdf is the probability density function (pdf) *f(t)*, which represents the probability that T from the random sample is within the defined range *0 - t*. The reliability function *R(t)* is shown in Equation 2.12, which is the probability of an item operating for a defined length of time without failure.

$$F(t) = P(T \leq t) = \int_0^t f(t)\, dt \tag{2.11}$$

$$R(t) = 1 - F(t) \tag{2.12}$$

To characterise the bathtub curve shown in Figure 2.6, the hazard rate *h(t)*, shown in Equation 2.13 is used. The hazard rate is not a probability and is used within the reliability function indicating how the failure rate changes with time. For infant failures, *h(t)* will decrease as time increases, with *h(t)* remaining constant for random failures and *h(t)* increasing with time for wear-out failures.

$$h(t) = \frac{f(t)}{1 - F(t)} = \frac{f(t)}{R(t)} \tag{2.13}$$

2.6.2 Constant random failures

The exponential distribution is typically used when modelling the useful life section of the bathtub curve with a constant failure rate [93]. The cfd and pdf for random failures are shown in Equation 2.14 and Equation 2.15 respectively. The reliability function for random failures is shown in Equation 2.16, where *R(t)* is the reliability function, λ is the failure rate of a SM and t is time. The hazard rate for random failures is calculated using Equation 2.17, where the hazard rate is calculated to be constant, as expected for constant random failures.

$$F(t) = 1 - e^{-\lambda t} \tag{2.14}$$

$$f(t) = \lambda e^{-\lambda t} \tag{2.15}$$

$$R(t) = e^{-\lambda t} \tag{2.16}$$

$$h(t) = \frac{\lambda e^{-\lambda t}}{e^{-\lambda t}} = \lambda \tag{2.17}$$

To calculate the unavailability of a SM due to random failures, the negative exponential shown in Equation 2.18 is used where q is the unavailability, λ is the constant failure rate of a SM and T_M is the maintenance interval. The unavailability of a SM for constant random failures is therefore dependent on the maintenance interval, with more frequent maintenance reducing the unavailability of a SM. To calculate the availability of a converter arm using the unavailability of a SM, the *k-out-of-n* model is used as shown in Equation 2.19, where A is the availability, N is the minimum number of SMs within an arm, R_{SM} is the number of redundant SMs and q is the unavailability of a SM.

$$q = 1 - e^{-\lambda T_M} \tag{2.18}$$

$$A = \sum_{k=0}^{R_{SM}} \frac{(N + R_{SM})!}{k!(N + R_{SM} - k)!} \, q^k \, (1 - q)^{(N+R_{SM})-k} \tag{2.19}$$

The *k-out-of-n* model is very similar to the binomial distribution formula with sigma within the *k-out-of-n* model the difference between the two formulas. To calculate the availability of an MMC arm using the *k-out-of-n* model, the availability of an arm increases as the number redundant SMs increases, as shown in Figure 2.7. The summation is required to calculate all possible failure scenarios with redundant SMs within an arm.

The increase in unavailability as redundant SMs increases within [76], is due to the binomial distribution formula being used and not the *k-out-of-n* model. If the data points within [76] where summed together, they would show the availability of a converter arm increasing as the number of redundant SMs increases. This explains how results within [76] show the availability of a converter decrease with the increase in redundant SMs.

0 Redundant SMs

$$A = \textit{probability of all SMs working}$$

1 Redundant SMs

$$A = \begin{array}{c}\textit{probability of all SMs working} \\ +\,\textit{probability 1 SM failed and rest working}\end{array}$$

2 Redundant SMs

$$A = \begin{array}{c}\textit{probability of all SMs working} \\ +\,\textit{probability 1 SM failed and rest working} \\ +\,\textit{probability 2 SM failed and rest working}\end{array}$$

Figure 2.7: *k-out-of-n* model for 0 - 2 redundant sub-modules.

2.6.3 Wear-out failures

To model the wear-out section of the bathtub curve, the Weibull distribution is used with a variable failure rate [93]. The cfd and pdf for wear-out failures are shown in Equation 2.20 and Equation 2.21 respectively. The reliability function for wear-out failures is shown in Equation 2.22, where *R(t)* is the reliability function, λ is the failure rate of a SM, t is time and β is the shape parameter.

$$F(t) = 1 - e^{-(\lambda t)^{\beta}} \tag{2.20}$$

$$f(t) = \beta \lambda t^{(\beta-1)} e^{-(\lambda t)^{\beta}} \tag{2.21}$$

$$R(t) = e^{-(\lambda t)^{\beta}} \tag{2.22}$$

The shape parameter β within the Weibull distribution is used to model different failure profiles of the bathtub curve. Infant failures are modelled when $\beta < 1$, with wear-out failures modelled when $\beta > 1$. The Weibull distribution simplifies to the exponential distribution when $\beta = 1$, which is the same formula used to model constant random failures in Section 2.6.2.

To determine β for wear-out failures, the hazard rate is plotted using Equation 2.23 where β is the shape parameter, λ is the failure rate of a SM and t is time. Different values of β represent different failure rate profiles when the hazard rate is plotted against time.

$$h(t) = \frac{\beta\lambda t^{(\beta-1)} e^{-(\lambda t)^{\beta}}}{e^{-(\lambda t)^{\beta}}} = \beta\lambda t^{(\beta-1)} \tag{2.23}$$

To calculate the unavailability of a SM due to wear-out failures, the Weibull distribution shown in Equation 2.24 is used where *q(t)* is the unavailability of a SM, λ is the failure rate of a SM, t is time and β is the shape parameter which is determined using Equation 2.23.

$$q(t) = 1 - e^{-(\lambda t)^{\beta}} \tag{2.24}$$

To calculate the availability of an MMC, the *k-out-of-n* model cannot be used to model wear-out failures because the model assumes a constant failure rate. To model wear-out failures a discrete-time Markov chain Monte Carlo simulation is the best method to use. The Markov chains used to model wear-out failures are defined in the respective chapters of this thesis.

To calculate the total number of redundant SMs required within an MMC, wear-out and constant random failures have to be combined to give the correct failure profile, as observed within the bathtub curve in Figure 2.6.

2.7 Summary of Literature Review

This chapter has highlighted the main causes of failure within HVDC systems, comparing both LCC and VSC. The MMC is the preferred converter for VSC-HVDC to-date, with growing interest for MV applications due to its reduced switching frequency and low filter requirement in comparison to other VSC topologies. There are other modular and cascaded multi-level converters available which are tolerant to DC-faults when compared to the half-bridge MMC, but require either more complex control, larger volume or are less efficient when compared to the half-bridge MMC. The modular design of the MMC allows a small number of redundant SMs to be placed within each arm to tolerate a small number of SM failures between maintenance periods. It is not well understood within literature how many redundant SMs should be placed within each arm, with estimations in the region of 8 % to 25 % currently recorded. The advantages of active redundancy are higher than the advantages of standby redundancy because of the reduced switching frequency, reduced failure rate of each IGBT module and is regarded more practical and reliable to implement.

Cigré publish reliability data for HVDC systems around the world and has shown for LCC systems the longest duration per fault is from transmission lines and cables, with AC transformers contributing to most failures. When comparing LCC and VSC systems, there is less data available for VSC systems due to the maturity of LCC systems, however, recent data has shown the converter to contribute to most VSC-HVDC failures. The reliability of VSC systems is therefore believed to be dependent on transmission lines and cables, AC transformers and the VSC converter. With less than 10 % of cable faults due to technical issues and AC transformers improving in reliability, it is believed that the converter is the area of concern regarding the reliability of VSC systems.

The main component within an MMC is the SM, with the IGBT module, SM capacitor and control electronics regarded as the most significant components to contribute towards a SM failure. The control electronics within a SM has been found to be the limiting factor, with a

maximum life-expectancy of 15 years due to the use of electrolytic capacitors within the control circuitry. The failure rate of IGBT modules increases as the applied voltage and operating temperature increase, with the SM capacitor failure rate also dependent on temperature. The choice of IGBT module is also power loss dependent, with different IGBTs having different power loss characteristics. Higher voltage rated IGBT modules are designed to be good at conducting but have poor switching losses, whereas lower voltage rated IGBT modules are better at switching and have poor conduction losses. This also shows different IGBTs are better suited for HV applications than MV and vice versa.

Wear-out failures are believed to be an important factor when calculating the availability of an MMC due to the life-expectancy of a SM compared to the project life of a HVDC system. To calculate the total availability of an MMC, constant random and wear-out failures are combined to represent the complete failure profile. The *k-out-of-n* model is best to calculate the availability of a converter arm due to constant random failures, but can not be used to model wear-out due to the assumption of a constant failure rate. Wear-out failures are best modelled using a Markov chain Monte Carlo simulation with the Weibull distribution used to model the unavailability of a SM with varying and increasing failure rate over time.

3 Design and Build of a Lab-scale Modular Multi-level Converter

In order to generate experimental evidence of the efficiency control algorithms that have been proposed in the course of this thesis, a lab-scale (15 kW) MMC was designed and built in the Maurice Hancock lab at Imperial College London. The converter was designed to the same electrical specification as an existing modular converter within the lab. This was to enable the two converters to operate as a point-to-point link or back-to-back converter if desired. The full converter specification for the MMC is shown in Table 3.1 and it differs from the earlier build in terms of targeting lower power losses and a closer match to the operating point that an ideal MMC would adopt. The design and build was undertaken with help from Dr Paul Judge who had played the leading role in the completion of the first lab-scale MMC.

Table 3.1: Parameters of lab-scale modular multi-level converter.

Characteristic	Value
Power Rating	15 kW
DC Voltage	± 750 V
AC Voltage	950 V
Number of Sub-modules per Arm	10
Sub-module Topology	Half-bridge / Full-bridge
Sub-module Nominal Voltage	150 V
Arm Current	10 A
Sub-module Capacitor	500 / 770 / 890 / 1160 μF
Transformer Arrangement	Star - Delta

This second lab-scale MMC achieves improved efficiency through the use of MOSFETs instead of IGBTs as the semiconductor switches. The advantage of using MOSFETs over IGBTs is the reduced $V_{CE(on)}$ / $V_{DS(on)}$ and $R_{CE(on)}$ / $R_{DS(on)}$, which result in the semiconductor devices having lower conduction power loss, which in-turn increases the efficiency of the converter. There is also a reduction in switching power loss from the faster commutation events. The reduced voltage drops within the converter means that the waveforms generated are a better match to those that would be observed from a large-scale converter and this in turn gives greater confidence when validating control algorithms.

The IGBT and MOSFET used within the two separate converters are outlined in Table 3.2. They both have similar voltage and current ratings, with their respective $V_{CE(on)}$ $V_{DS(on)}$ showing the MOSFET has a lower voltage drop at 10 A. The reason for the high current rated devices compared to their application rating, is to protect the semi-conductors if in the event of a fault in the control or hard-ware set-up exposing the devices to high fault current. The output characteristics of the IGBT and MOSFET for a gate voltage of 15 V are shown in Figure 3.1, where the MOSFET has a lower on-state resistance when compared to the IGBT, where the data was taken directly from the data sheets for both the IGBT and MOSFET. The temperature was recorded as 25°C for both the IGBT and MOSFET to maintain a fair comparison.

The $R_{CE(on)}$ / $R_{DS(on)}$ within Table 3.2 is taken from Figure 3.1, with $R_{CE(on)}$ calculated using Equation 3.1. The IGBT, therefore, has higher losses when compared to the MOSFET due to the initial on-state voltage which is not observed for the MOSFET. For higher current

Table 3.2: Comparison of the IGBT and MOSFET used in the lab-scale MMCs.

	IGBT	MOSFET
Component	IRGP4650DPbF	IPW65R041CFD
Voltage Rating	600 V	650 V
Current Rating	76 A	68.5 A
$V_{CE(on)}$ / $V_{DS(on)}$, (I_C = 10 A)	1.15 V	0.39 V
$R_{CE(on)}$ / $R_{DS(on)}$	0.90 Ω	0.038 Ω
$V_{GE(th)}$ / $V_{GS(th)}$, (min)	4.0 V	3.5 V

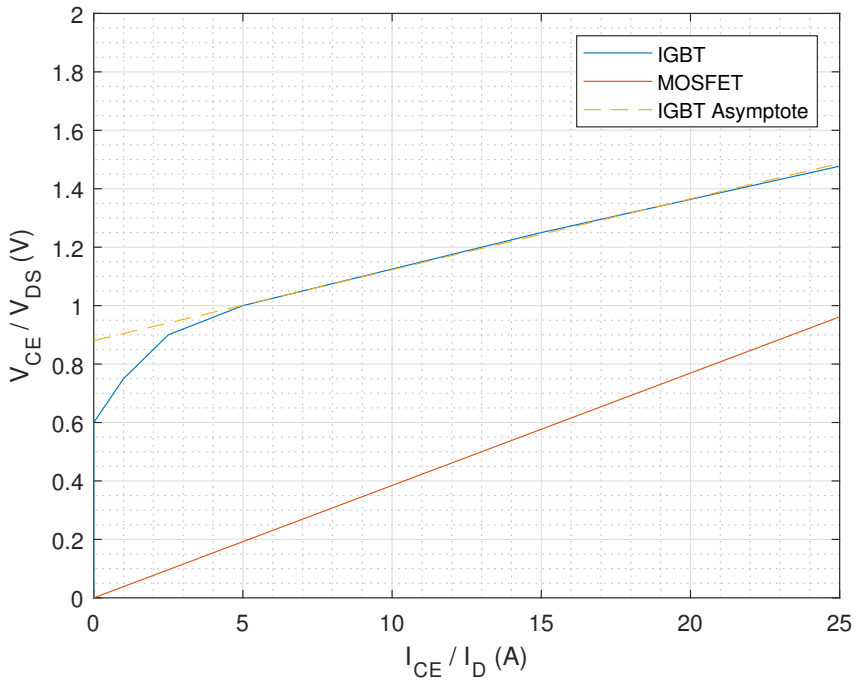


Figure 3.1: Output characteristics of the IGBT and MOSFET outlined in Table 3.2, with V_{GE} / V_{GS} = 15 V and temperature = 25°C.

ratings, however, the IGBT has reduced power losses when compared to the MOSFET due to the IGBTs reduced $R_{CE(on)}$, but for the hardware applications within this thesis, the MOSFET is the more efficient device at 10 A.

$$V_{CE(on)} = V_{CE(Intersect)} + R_{CE(on)} I_{CE} \tag{3.1}$$

The MOSFET lab-scale MMC when operated with half-bridge SMs has an efficiency around 98 %, when compared to the IGBT lab-scale MMC which has an efficiency around 93 % when operated with half-bridge SMs, showing considerable efficiency improvements for the same electrical specification.

The lab-built MOSFET MMC is shown in Figure 3.2, with the PC and Opal-RT OP5600 located at the top of the cabinet. The Opal is a real-time controller, which sends control

signals to SMs via digital-out modules and receives SM voltages and arm currents through analogue-in modules located at the back of the Opal. At the base of the converter is the grid interfacing transformer and on the left-hand side of the cabinet is the arm inductors for MMC operation. The right-hand side of the cabinet is where 60 SMs are positioned, with each column of SMs representing one arm of the converter. At the bottom of each arm is a different module known as the director switch. The director switch consists of two series connected IGBTs with the voltage blocking capability of an entire arm. This allows the converter to operate as an AAC, with changeover switches placed next to the inductors to alter the inductor arrangement accordingly depending on converter topology.

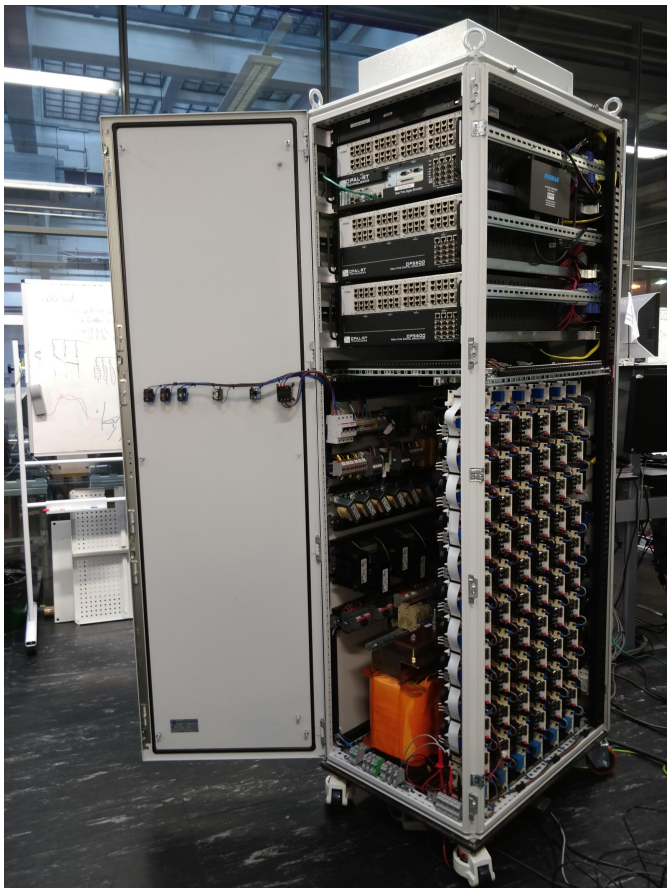


Figure 3.2: MOSFET modular multi-level converter integrated into a single cabinet.

3.1 The IGBT-based Lab-scale MMC

The IGBT modular converter was primarily designed and built by Dr Paul Judge, Dr Geraint Chaffey and Dr Phil Clemow. The IGBT SM is shown in Figure 3.3, which consists of two separate PCBs one electrically connected to the other. The top PCB is the capacitor board with parallel connected capacitors, which act as the total capacitance for the SM. There is also a LEM voltage transducer located on the capacitor PCB which measures the voltage across the SM and sends the measured voltage to the Opal via a ribbon cable. The bottom PCB, which can be seen in more detail in Figure 3.4, contains the full-bridge arrangement of IGBTs, gate drivers and control circuitry. There are also heat sinks, a fan and 3D printed mounting brackets connected to the bottom PCB for heat dissipation and cooling for the IGBTs.

The PCB shown in Figure 3.4 is electrically divided in two half's. The left-hand side of the PCB is the control circuitry for the dead-time generator and gate drivers for the IGBTs. The right-hand side of the PCB is the power circuit for the full-bridge arrangement of IGBTs, which

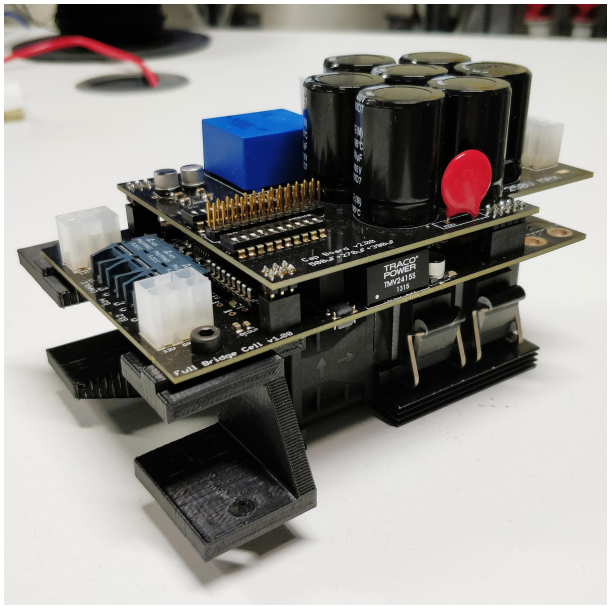


Figure 3.3: IGBT full-bridge sub-module design for modular multi-level converters; designed by Dr Paul Judge.

is electrically isolated from the left-hand side of the PCB to provide good noise immunity from the switching IGBTs.

The power for the control side of the PCB is daisy-chained top and bottom of the PCB to other SMs within the same arm, with a 24 V and 12 V supply. The 24 V supply is used to power isolated DC-DC power supplies, with a 5 V output powering the control circuitry and 15 V outputs powering the gate drivers in the power circuit. The 12 V supply is used to power the fan to cool the IGBTs. The control circuit receives signals from the Opal via three optical receivers; one enables the SM and the other two are used for controlling the two half-bridge IGBT pairs. The control signals from the optical receivers are passed through an inverting Schmitt trigger, to invert the logic sent from the Opal, which are then fed into an IXDP630 PWM control chip to implement the dead-time required between the two pairs of IGBTs. The PWM chip generates the dead time from an RC oscillator pair and passes four signals for each IGBT via two ADuM4223 isolated half-bridge gate drivers.

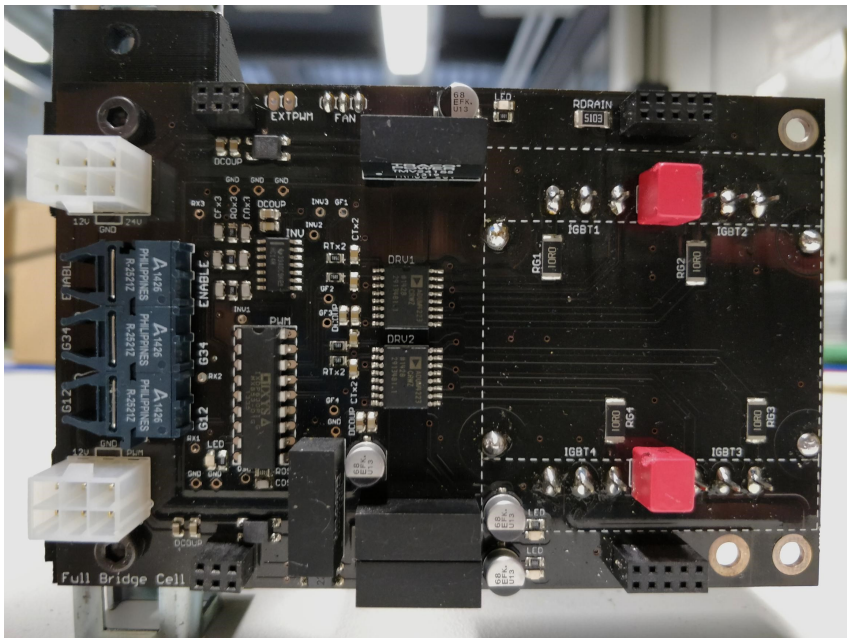


Figure 3.4: Main IGBT sub-module PCB showing control and power circuits; designed by Dr Paul Judge.

The right-hand side of the PCB is the power circuit, with the control circuit connected across the isolated barrier via the two ADuM4223 gate drivers. Power to the gate drivers are provided by three isolated DC-DC power supplies, with one isolated power supply providing power to the two low side IGBTs, whilst the top two IGBTs are powered from independent isolated power supplies. There is a gate resistor located within the gate path of each IGBT and a red film capacitor located between each pair of IGBTs providing high frequency filtering for the DC-link within the SM. The external power connectors for the PCB are located in both corners of the right-hand side of the PCB, which represents the mid-point of the two respective IGBT pairs. The second connector located at the bottom right of the PCB is for operating the SM as purely half-bridge, with the connector electrically bypassing one pair of IGBTs.

3.2 Design of a MOSFET-based Lab-scale MMC

The MOSFET MMC was designed to the same electrical specification as the IGBT converter to allow for point-to-point operation, making the first test a direct swap of semiconductors within the IGBT SM to check if it could operate using MOSFETs. Unfortunately, due to the faster switching characteristics of the MOSFET compared to the IGBT, this was not an optimum solution with up-to 150 % voltage overshoots when the MOSFET switched from its blocking state to its conduction state. This meant a complete re-design of the power circuit was needed, but the decision to keep the control circuit the same was made due to the proven design within the IGBT SM. The gate layout schematics for the IGBT and MOSFET used within the power circuit of the SMs are shown in Figure 3.5, where it can be seen that there are several more components within the gate path for the MOSFET than just a gate resistor which is used within the gate path for the IGBT SM design. To utilise the faster switching characteristics of the MOSFET, the gate resistance was reduced which improved the turn off waveform of the MOSFET, but this led to even larger over-voltage oscillations when the MOSFET turned on due to the inability of the resistor to suppress voltages during its switching state. To reduce

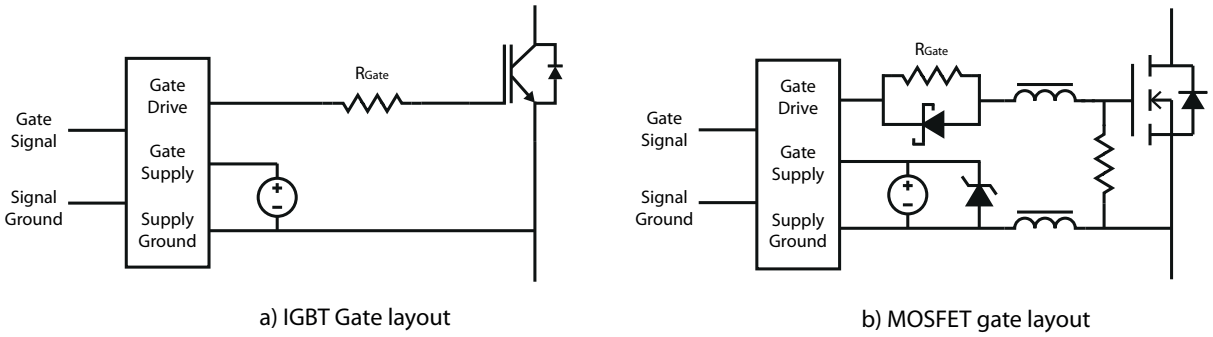


Figure 3.5: Schematic of gate layout for: a) IGBT b) MOSFET.

the over-voltage peaks when the MOSFET turned on, a larger gate resistor was required to dampen the oscillations during switching. This meant there were two different preferred gate designs for switching the MOSFET on and off, which led to the introduction of a shockley diode in parallel with the gate resistor to provide two different current paths for turn on and turn off of the MOSFET. The faster turn off of the MOSFET meant the dead-time between the two pairs of MOSFETs could be reduced when compared to the IGBT SM. The dead-time within the IGBT SM was set to 5 us, whereas the dead-time within the MOSFET SM is 0.9 us. This increases waveform quality and the efficiency of the converter ever so slightly as there is a shorter dead-time period where the SMs are not processing power.

Within the gate path from the MOSFET to the gate driver, there is also a ferrite bead placed as close to the gate of the MOSFET as possible. This helps suppress any high frequency noise travelling along the gate path to the gate drivers and helps prevent false triggering of the MOSFET. There is also a resistor placed across the gate and source of the MOSFET which helps discharge the gate capacitance quicker, therefore, turning the MOSFET off faster and reducing the risk of the MOSFET turning itself on during its blocking state. There is also a zener diode across the power supply within the gate driver circuit to clamp the gate turn on voltage to 15 V and help stop any unexpected voltages turning the MOSFET on during its blocking state. There has also been an increase in de-coupling capacitors across the power supply for the gate driver circuit, which are not illustrated within Figure 3.5. This is to reduce the capacitive noise

generated between the tracks from the isolated DC-DC power supplies to the gate drivers. The de-coupling capacitors are located very close to the gate drivers, to reduce as much noise as possible interfering with the control signals.

The MOSFET designed SM is shown in Figure 3.6 and consists of two separate PCBs, one electrically connected to the other as within the IGBT SM. The capacitor board has the same capacitance as the IGBT SM but uses different capacitors in parallel. The increased number of capacitors within the MOSFET SM helps diversify the voltage ripple observed within each capacitor, as film capacitors are preferred for high power applications but have a considerably larger volume and are more expensive when compared to electrolytic capacitors.

The bottom PCB, which can be seen in more detail in Figure 3.7, contains the full-bridge arrangement of MOSFETs, gate drivers and control circuitry. The first notable difference when compared to the IGBT SM is the introduction of an air-gap down the middle of the PCB, which increases the creepage distance and improves noise resilience for the control circuit. The

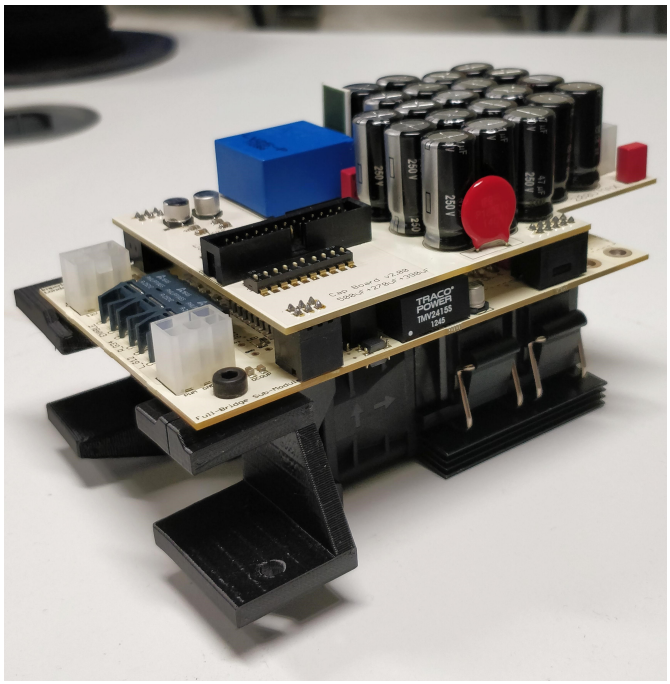


Figure 3.6: MOSFET full-bridge sub-module for modular multi-level converters.

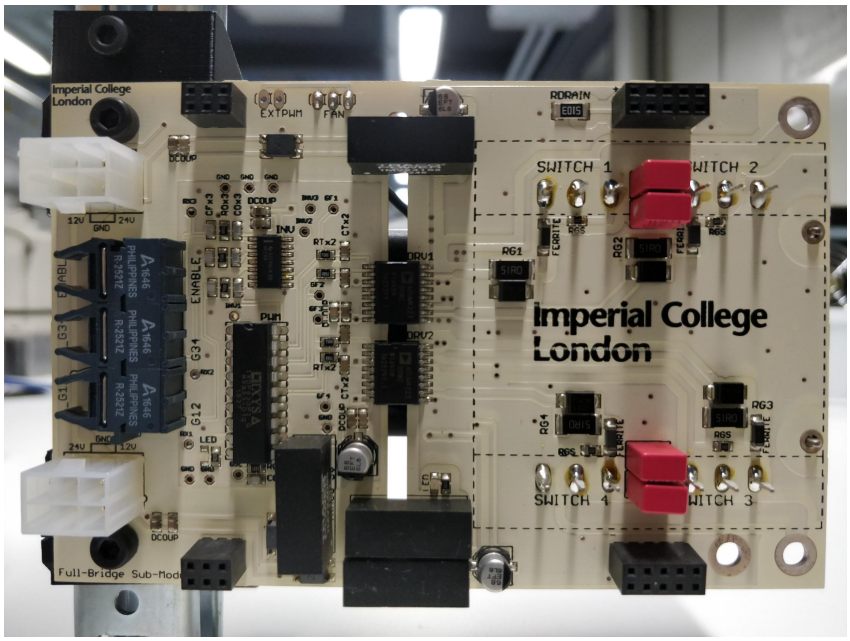


Figure 3.7: Main MOSFET sub-module PCB showing control and power circuits.

main changes to the PCB are within the gate path from the gate drivers to the gate of each MOSFET, as illustrated in Figure 3.5.

3.3 Further Design Improvements for the MOSFET Sub-module

If a future iteration of the MOSFET SM were designed, there are a few design considerations that would improve the performance of the MOSFET SM further. It would be advisable to locate the gate drivers closer to the gate and source of the MOSFETs, as this would reduce the risk further from unwanted noise interfering with the MOSFETs and causing over-voltage oscillations which require suppressed with large gate resistors during the turn on state. The shorter gate path would also enable faster switching, further reducing the dead-time between each pair of MOSFETs within the full-bridge arrangement. This would most probably require a change to the control circuit, resulting in a complete re-design of the SM.

There are also MOSFETs with four inputs; gate, drain and two source pins, which are available in the same TO-247 package [96]. The two source pins allow one pin to carry the high power current whilst having a dedicated source pin for the gate driver circuit. The advantage of a dedicated source return for the gate driver circuit is the reduced noise within the gate path from the MOSFETs switching every cycle due to sharing the same pin.

3.4 Experimental Set-up

The experimental set-up for the MOSFET MMC is shown in Figure 3.8. There is a back-to-back 90 kVA converter which acts as a controllable AC-side voltage source, which generates different desired AC voltages depending on converter topology. The DC bi-pole voltage is supplied to the converter by two DC power supplies connected in parallel. When the converter is operating as a rectifier, there are DC loads connected to displace the power, whereas when the converter is operating as an inverter, the 90 kVA converter is able to sync power into the AC network.

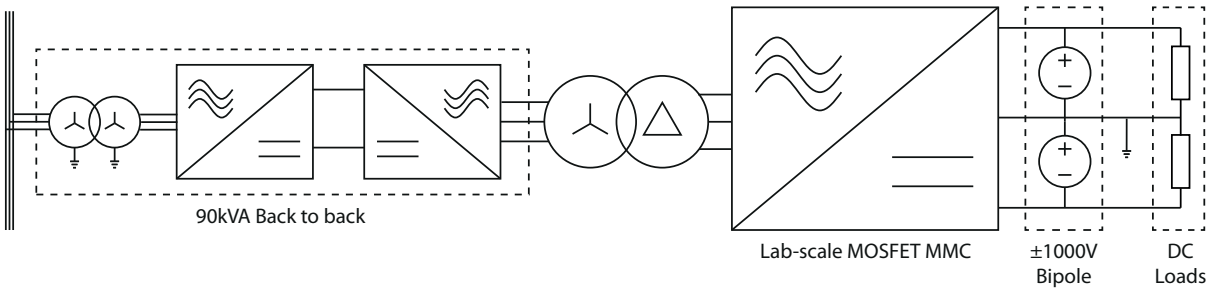


Figure 3.8: Experimental set-up for the lab-scale modular multi-level converter.

3.5 Experimental Results

An example set of results illustrating the converter operates as designed are shown in Figure 3.9 and Figure 3.10 for the MOSFET MMC operating as an inverter at 1 p.u. real power and 0 p.u. reactive power. Later chapters of the thesis will show further results to verify particular aspects of MMC operation and control.

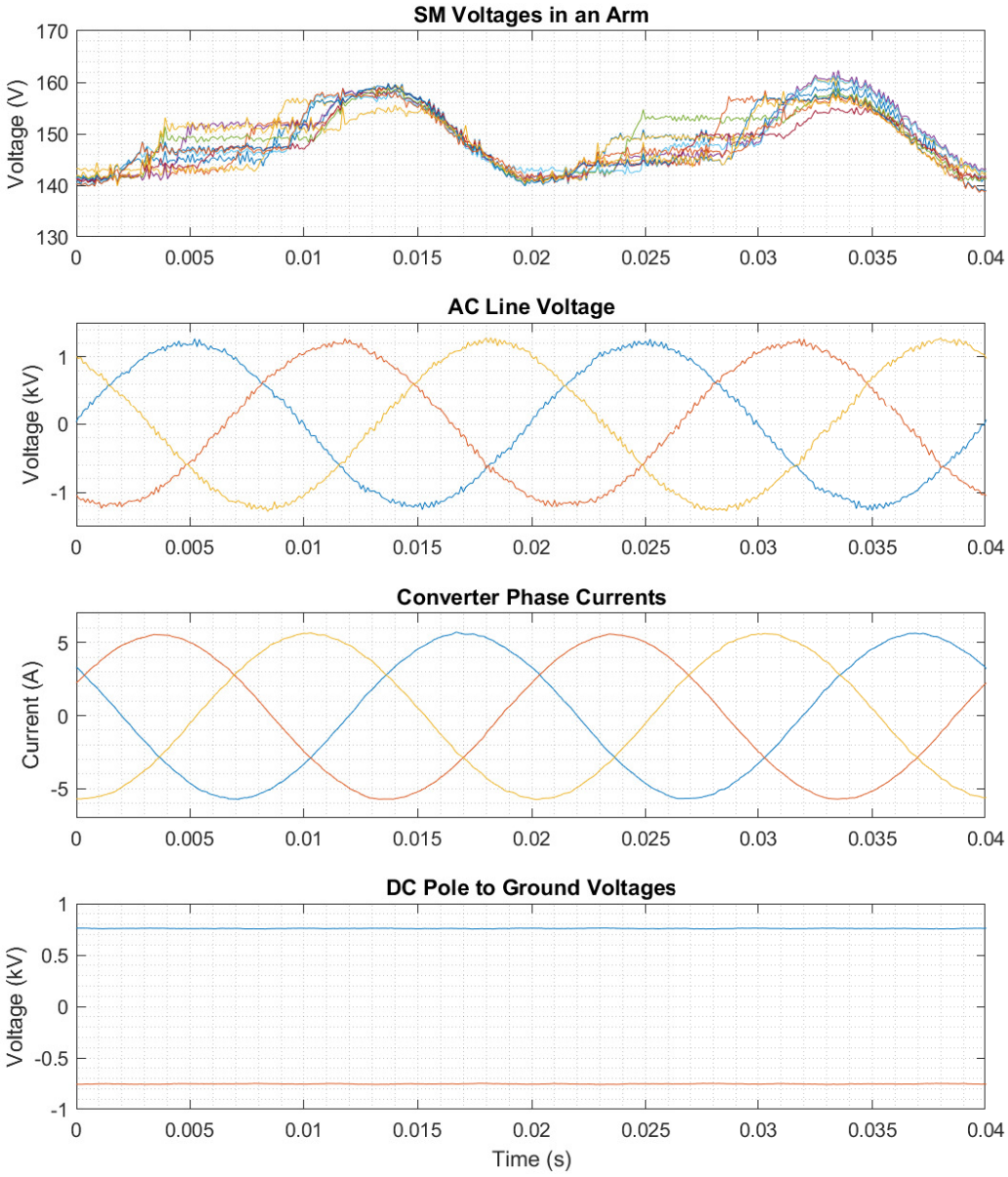


Figure 3.9: Experimental results of lab-scale MOSFET MMC operating at 1 p.u. power and 0 p.u. reactive power showing: SM voltages, AC line voltages, converter phase currents and DC voltages.

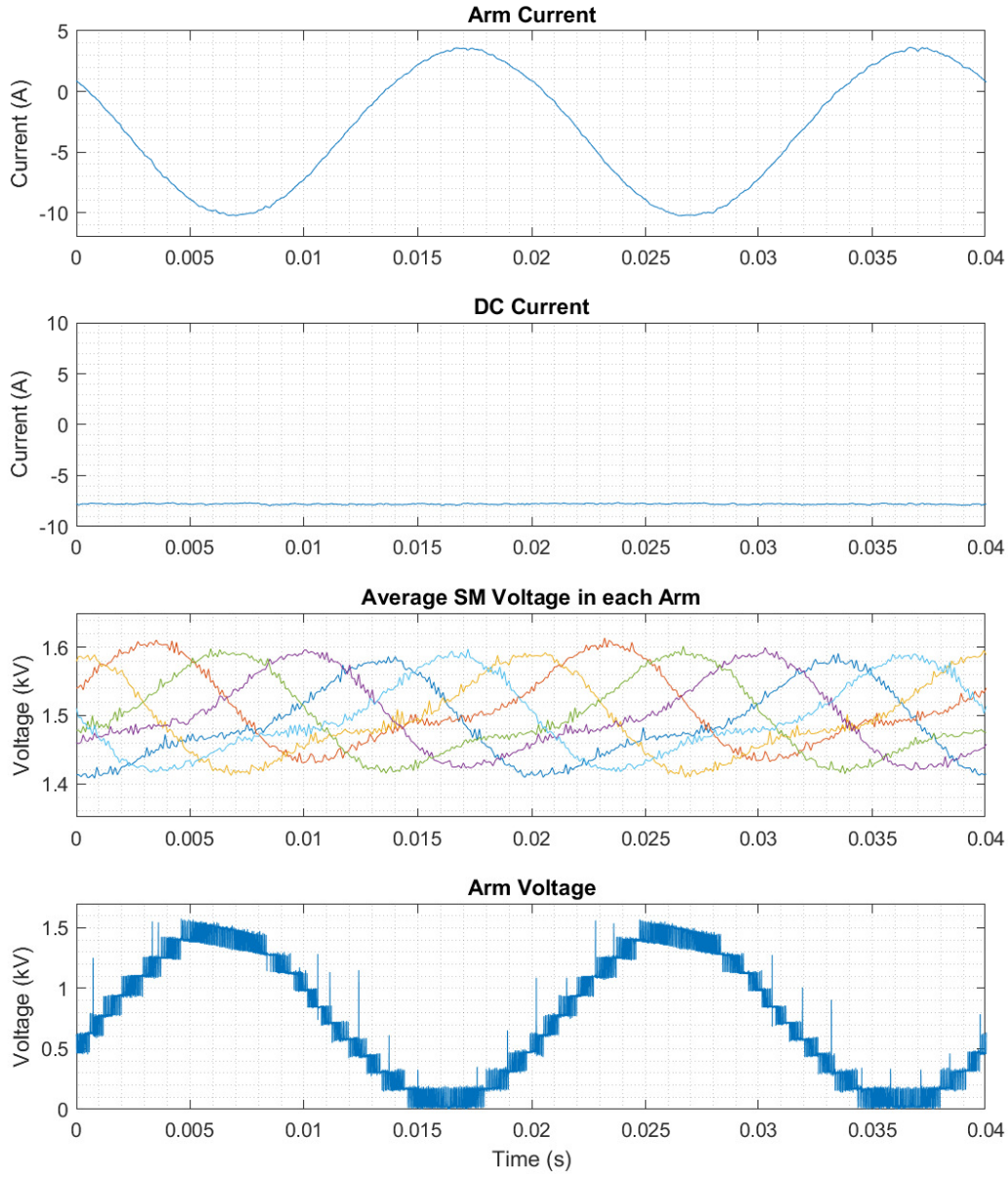


Figure 3.10: Experimental results of lab-scale MOSFET MMC operating at 1 p.u. power and 0 p.u. reactive power showing: arm current, DC current, average SM voltages in each arm and arm voltage.

4 Redundancy in High Voltage MMCs

Redundant SMs are required within MMCs because it has to be anticipated that some SMs will fail between maintenance intervals and the converter can not continue operating at its DC voltage without a full complement of SMs. However, the number of redundant SMs required to maintain full operation between maintenance is not well documented or understood [70] [71]. This chapter investigates how to determine the number of redundant SMs required in an MMC for HV applications considering the effects of both constant random failures and wear-out failures of SMs. The number of redundant SMs required for a given availability is assessed for various intervals of periodic preventative maintenance so as to explore the balance between maintenance costs (which are especially high where specialised repair vessels for offshore HVDC installations are needed) and the capital and operational costs of having more redundant SMs present.

It will be assumed in this work that the redundant SMs provide active redundancy by sharing the total system load and as such are indistinguishable from standard modules. The alternative would be standby redundancy in which redundant SMs are idle and disconnected (or bypassed) mechanically until needed and then switched into circuit (a mechanism for pre-charging the SM capacitor before entering operation may be needed). Industry practice is to not use standby redundancy because of concerns over the practicality and reliability of the switching mechanism.

The following sections of this chapter outline the HV case-study converter and show how the availability of each converter arm is affected by constant-random and wear-out failures of SMs for a given maintenance interval. This is done for various numbers of redundant SMs in each

arm. Converter availability is what really matters to a system operator but here one arm will be analysed and a target set of an arm availability of 99.99 % which implies an unavailability of 0.01 %. This translates to an unavailability of 0.06 % or an availability of 99.94 % for an overall converter comprising 6 arms.

For all the studies that follow, it has been assumed that the service life of the converter should be 40 years, which is the average life-expectancy of HVAC equipment [95].

4.1 Case-study MMC for High Voltage

The MMC case-study converter for this chapter was chosen to be of similar power and DC-link voltage to DolWin3 and BorWin3 offshore HVDC converter stations [97] [98]. The chosen specification is given in Table 4.1.

The nominal SM voltage was chosen as 2.1 kV, which is 65 % the rated voltage of the IGBT selected, which has rated parameters of 3.3 kV, 1.5 kA [91], as shown in Table 4.2. This allows for voltage ripple across the device during normal operation without breaching devices operational limits. The minimum number of SMs required per arm is calculated using Equation 4.1, where N is the minimum number of SMs per arm, V_{DC} is the total DC voltage and $V_{SM_{Nom}}$ is the nominal SM voltage.

Table 4.1: Parameters of HVDC case-study MMC.

Characteristic	Value
Power Rating	900 MW
DC Voltage (V_{DC})	± 320 kV
AC Line Voltage (RMS)	300 kV
Nominal SM Voltage	2.1 kV
Minimum Number of SMs per Arm ($V_{SM_{Nom}}$)	305
Nominal Converter Energy	35 kJ/MVA
Main SM Capacitor	7,806 μF

Table 4.2: Sub-module components and associated FIT data for the HV case-study MMC.

Component	Manufacture	Part Number	FIT
IGBT	Infineon	FZ1500R33HE3 [91]	200
Capacitor (MPPF)	EPCOS	B25750H2448k004 [92]	100
Control Electronics Subsystem	Various	N/A	1,000

$$N = \frac{V_{DC}}{V_{SM_{Nom}}} \tag{4.1}$$

It is assumed that there is a converter transformer present that can be used to match the desired AC converter voltage to the actual AC grid voltage. The capacitor value recorded in Table 4.1 was calculated using Equation 4.2, where S_{Base} is the power rating of the converter, E_{nom} is the nominal energy within the MMC, N is the minimum number of SMs per arm and V_{nom} is the nominal SM voltage. The nominal energy has been chosen as 35 kJ/MVA, which is a common value used for the nominal energy of an MMC [54].

$$C_{SM} = \frac{2S_{Base}E_{nom}}{6NV_{SM_{Nom}}^2} \tag{4.2}$$

The SM in this study are of half-bridge type and only the IGBTs, the main capacitor and the control electronics (as a subsystem) regarded as significant in the failure of a SM. The bypass switch normally present for bypassing a faulted SM and the thyristor normally present for carrying current in the event of a DC-side short-circuit are not operational under normal conditions and are therefore regarded as having no impact on the failure of a SM during normal operation.

The failure rates, expressed in terms of FIT, for the IGBT and main SM capacitor selected for this case-study are given in Table 4.2. The FIT of the control electronics subsystem of the SM is estimated as 1,000 FIT based on a discussions with GE Grid Solutions and the general view that the failure rate of aluminium electrolytic capacitors within the control circuitry is relatively

high. The MPPF capacitor from EPCOS selected in Table 4.2 has a significant failure rate of 100 FIT as outlined in the data sheet for the device [92]. To achieve the SM capacitance noted in Table 4.1 requires two of the capacitor noted in Table 4.2 placed in parallel (because no directly suitable component was available), therefore, the value FIT of the SM capacitor in Table 4.2 is twice the data-sheet value.

The failure rate of a SM is calculated by summing together the FIT of all components of a SM on the basis that if any component within a SM fails, the entire SM is not able to function and has to be bypassed, therefore, the failure rates of two IGBTs, an MPPF capacitor and the control electronics subsystem are summed together, as shown in Equation 4.3.

$$\lambda_{SM} = 2\lambda_{IGBT} + \lambda_{Cap} + \lambda_{Control} \tag{4.3}$$

4.2 Constant Random Failures in High Voltage MMCs

When analysing constant random failures of SMs within an arm of an MMC, it has been assumed that infant failures during the "burn in" period of the bathtub curve have no impact on the "useful life" of a converter, as these failures are detected during the commissioning stage of a converter as discussed within Chapter 2. It has also been assumed in this section of this chapter that wear-out does not contribute any additional SM failures during the "useful life" of the converter, in other words, it is assumed that wear-out only becomes significant after the 40 year service life of the converter (regardless of lifetime estimates of components chosen within Table 4.2).

Under an assumption of constant random failures, the negative exponential formula, Equation 4.4, is used to calculate the unavailability of a SM, q. The maintenance interval for constant random failures is represented as T_M within Equation 4.4, with the failure rate, λ, expressed in terms of years. This results in the unavailability, q, of a SM changing for different maintenance intervals. On average, the same number of SMs fail at the end of each maintenance interval

(assuming they are of equal interval) because the hazard rate within Equation 4.4 is constant throughout 40 years of operation. The hazard rate is calculated using Equation 4.5.

$$q = 1 - e^{-\lambda T_M} \tag{4.4}$$

$$h(t) = \frac{\lambda e^{-\lambda t}}{e^{-\lambda t}} = \lambda \tag{4.5}$$

The availability of an arm of an MMC is found from the unavailability of an individual SM using the *k-out-of-n* model within Equation 4.6 where R_{SM} is the number of redundant SMs, N is the minimum number of SMs needed in an arm to maintain full operation and q is the unavailability of a SM for a given maintenance interval.

$$A = \sum_{k=0}^{R_{SM}} \frac{(N + R_{SM})!}{k!(N + R_{SM} - k)!}\, q^k\, (1 - q)^{(N+R_{SM})-k} \tag{4.6}$$

The availability analysis for the HV case-study converter considering only constant random failures is plotted in Figure 4.1 against the percentage increase in redundant SMs compared to the base number of 305 SMs (from Table 4.1) and has been plotted for several choices of maintenance interval 1 year to 8 years.

First it can be see that availability follows an S-curve, initially rising slowly with degree of redundancy, then climbing steeply and then slowly approaching 100%. It can also be seen that increasing the maintenance interval decreases availability, as might be expected, and therefore more redundant SMs are needed to maintain availability for that increased maintenance interval.

The number of SMs required in an arm in order to achieve and availability greater then 99.99 % is shown in Table 4.3. The first row represents the percentage of redundant SMs compared to the minimum number of SMs required to operate within an arm. The second row displays the number of additional SMs required to maintain continuous operation between maintenance intervals. It should be noted that doubling the maintenance interval does not require double the

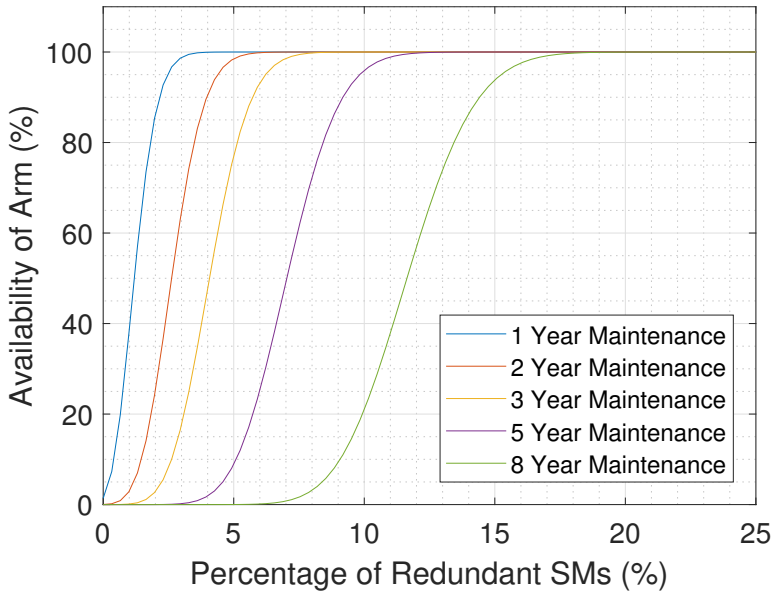


Figure 4.1: Availability of an arm in the HV case-study MMC against percentage of redundant SMs for constant random failures and for various intervals of periodic preventive maintenance.

number of redundant SMs: for instance, an 8-year maintenance interval does not require 4 times more redundancy than the 2-year interval to achieve the same availability. This implies there is an optimum point to be found when designing the total number of redundant SMs considering the total costs of providing and operating additional SMs and the cost of maintenance.

For the case of constant random failures considered here, one would expect to need to replace the same number of SMs at the end of each maintenance interval.

Table 4.3: Number of redundant SMs required for $>$ 99.99 % availability of an arm for various maintenance intervals with SMs subject to constant random failures.

	Maintenance Interval (Years)				
	1	2	3	5	8
Percentage of redundant SMs	4.59 %	7.21 %	9.51 %	13.77 %	20.33 %
No. of redundant SMs	14	22	29	42	62

4.3 Wear-out Failures in High Voltage MMCs

This section considers the combination of constant-random failures and wear-out failures such that the hazard rate of a SM increases with time. The *k-out-of-n* method used to model constant random failures within Section 4.2 cannot be used to model wear-out failures because it assumes a constant hazard rate. Instead, a discrete-time Markov chain Monte Carlo simulation is performed to determine the availability of an arm and this is repeated for various numbers of redundant SMs and different maintenance intervals. The life expectancy has been assumed to be 40 years of operation in all simulations. Infant failures were neglected on the basis that these failures are detected during the commissioning stage of a converter.

To model wear-out failures, the Weibull distribution shown in Equation 4.7 is used, where *q(t)* is the unavailability of a SM for different values of time, λ is the failure rate of a SM and β is the shape parameter which can be adjusted to model wear-out (value of $\beta > 1$ are needed). The corresponding hazard rate is given in Equation 4.8.

$$q(t) = 1 - e^{-(\lambda t)^{\beta}} \tag{4.7}$$

$$h(t) = \frac{\beta \lambda t^{(\beta-1)} e^{-(\lambda t)^{\beta}}}{e^{-(\lambda t)^{\beta}}} = \beta \lambda t^{(\beta-1)} \tag{4.8}$$

For this case-study, it is considered that SMs begin to wear-out after 15 years of continuous operation. This is consistent with the literature referenced in Chapter 2 which highlighted the reliability of aluminium electrolytic capacitors within the control electronics subsystem as being prone to wear-out [90]. To identify a suitable value of β, failure rate λ, was plotted against time using Equation 4.8 for various values of β, as illustrated in Figure 4.2, where a value that causes failure rate to rise significantly after 15 years was chosen. A value of $\beta = 5$ was found to be appropriate. This is consistent with conclusions in [75] for wear-out of power electronic components.

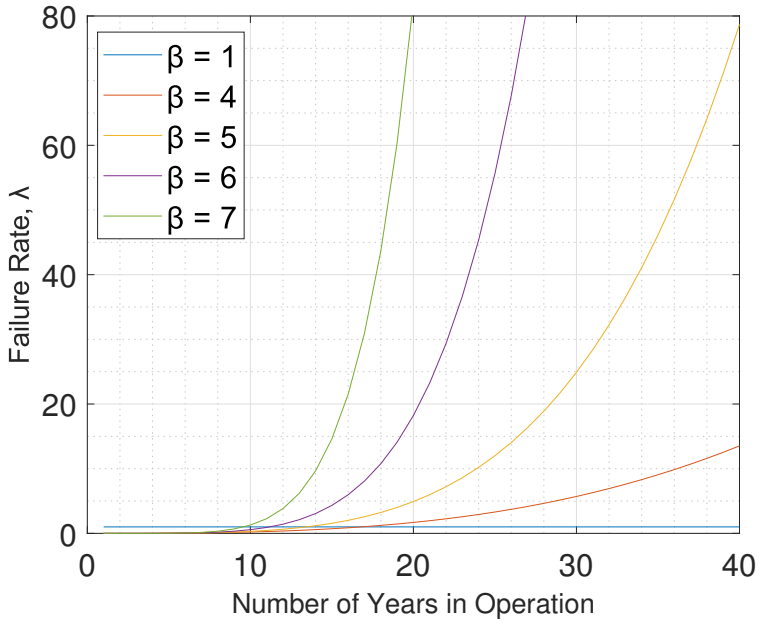


Figure 4.2: The hazard rate for wear-out failures showing the change in failure rate with time for different values of β.

To assess the availability of an arm with SMs subject to constant-random and wear-out failures, the discrete-time Markov Chain of Figure 4.3 was used in which *q(m)* represents an unavailability of a SM for a given maintenance interval, m. Each row of Figure 4.3 shows the states in one of the maintenance intervals, where the first row is the initial condition of the arm.

At each maintenance interval m, SMs transition from their present row to the next. If they remain functional (an available transition of 1-*q(m)* shown in green), then they simply become older by one maintenance interval and slightly more prone to becoming unavailable in the next interval. If the SM has failed (an unavailable transition of *q(m)* shown in red) then the SM is replaced with a new SM where it is treated as being at the beginning of the wear-out function (m=0).

A discrete-time Monte Carlo simulation is performed on the Markov chain with a simulation population of 10,000 converters, with the results examined for the average availability and other statistical properties. The maintenance intervals was set as an integer number of years and the

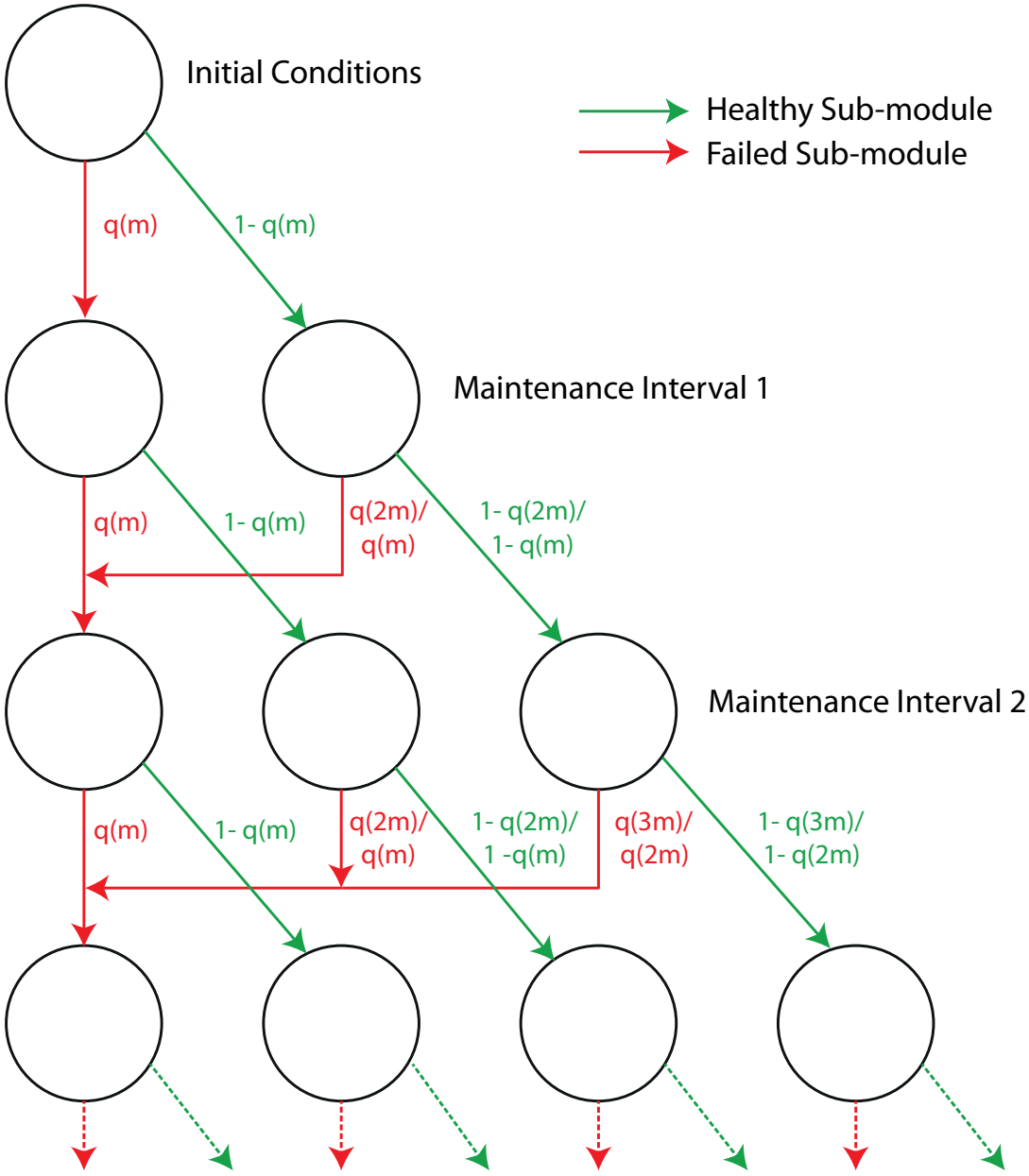


Figure 4.3: Markov chain used to assess the availability of a converter arm subject to wear-out failures for periodic preventive maintenance in which *q(m)* represents the unavailability of a SM during a maintenance interval *m*. Transitions shown in green are SMs that enter the next maintenance period in a functional state and transitions in red are SMs that require replacement at the end of a maintenance interval because thy have failed during that interval.

simulation time step was set as one year. The simulation is run for the expected service life of the converter of 40 years.

The validation of the discrete-time Markov chain Monte Carlo simulation for 10,000 converters can be found in Appendix A. The wear-out function is reduced to no-wear-out failures (constant random failure) by setting $\beta = 1$ so that the Weibull function becomes the negative exponential equation. This allowed a direct comparison between the *k-out-of-n* model outlined in Section 4.2 for constant random failures, against the proposed discrete-time Markov chain Monte Carlo simulation method outlined in this section.

The total number of SM failures calculated within this section are a combination of constant random and wear-out failures, to form the expected failure distribution outlined of a bathtub curve in Figure 2.6. The availability of an arm for constant-random plus wear-out failures is plotted against the percentage increase in redundant SMs and for various maintenance intervals in Figure 4.4. The plots follow a broadly similar shape to those in Figure 4.1 for only constant

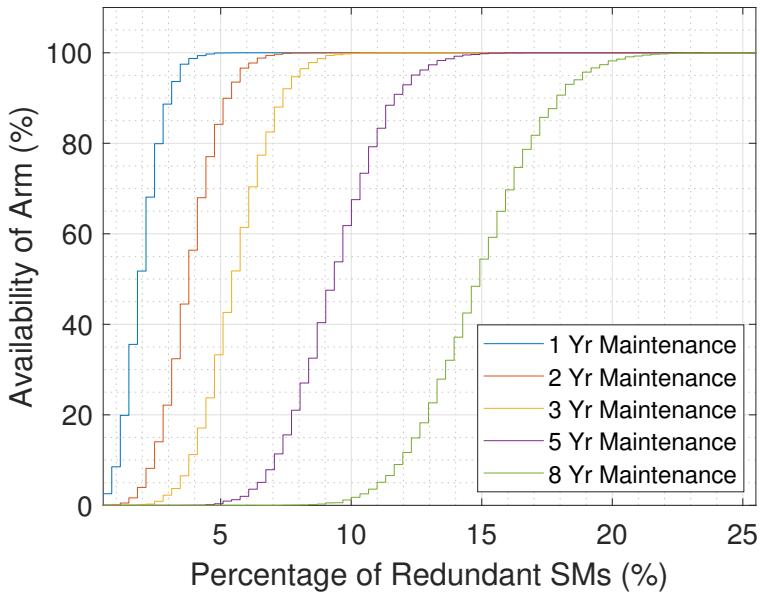


Figure 4.4: Arm availability under constant-random and wear-out failures against percentage of redundant SMs and for various maintenance intervals.

random failure. However, the availability for a given number of redundant SMs and a given maintenance interval are lower as might be expected when subject to two SM failure functions. This is most marked for the longer maintenance intervals.

The number of SMs required for > 99.99 % availability are shown in Table 4.4, where the top row shows the percentage of redundant SMs compared to the minimum number of SMs required to operate within an arm of the case-study MMC. The second row displays the total number of redundant SMs required to guarantee an availability of 99.99 % for an arm. The values in this table for SMs subject to constant-random and wear-out failures can be compared to those in Table 4.3 for constant-random failure only and the increase in redundancy provision over that case is shown in the third row.

It is clear from Table 4.4, that more redundant SMs are required to maintain the same level of availability over 40 years of operation when considering wear-out failures as well as constant random failures. The percentage increase in redundant SMs required when wear-out failures are included shows an increase in redundant SMs around 20 % for each maintenance interval, highlighting the large effect wear-out failures can have on converters over 40 years of operation. These results are, of course, reflective of the assumption that wear-out becomes significant after 15 years and depend on the particular wear-out function chosen (the Weibull function with $\beta = 5$).

Table 4.4: Number of redundant SMs required for > 99.99 % availability of an arm for various maintenance intervals for SMs subject to constant-random plus wear-out failure.

	Maintenance Interval (Years)				
	1	2	3	5	8
Percentage redundant SMs	5.57 %	8.85 %	11.48 %	16.39 %	24.92 %
No. of redundant SMs	17	27	35	50	76
Percentage increase over constant-random failure only	21.42 %	22.73 %	20.69 %	19.01 %	22.58 %

4.4 Discussion of Redundancy Choice with Constant-Random Failures and Wear-Out Failures for High Voltage MMCs

This section compares constant random failures and wear-out failures for the HVDC case-study converter, using the results from the previous sections of this chapter. Here, the number of redundant SMs required to achieve a particular availability for various maintenance intervals is considered. The results are shown in Figure 4.5.

The results cover increasingly onerous availability targets (for an arm) from 90.00 % to 99.99 % for an assumed service life of 40 years. The height of each bar records the percentage increase in redundant SMs required for a SM subject to constant-random plus wear-out failure; the mark on the bar records the number required for constant-random failures alone. It is clear from this split point on each bar that, in all cases, the majority of redundant SMs are required to cover

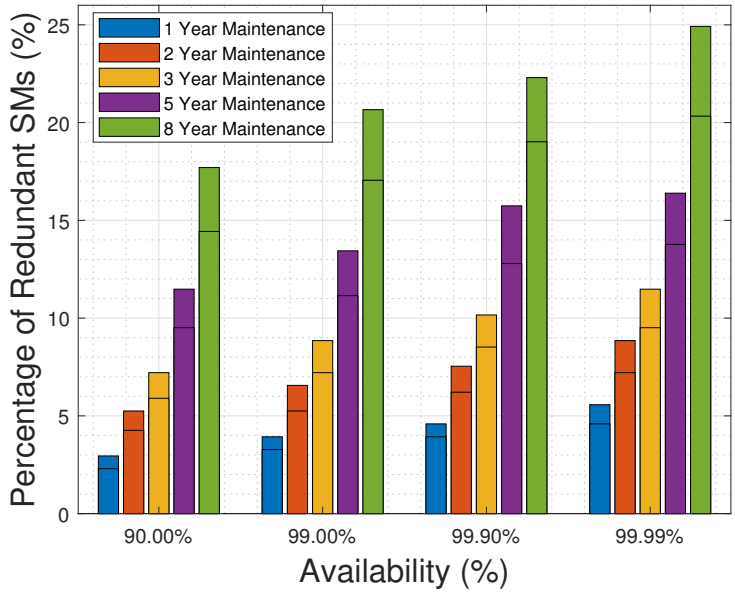


Figure 4.5: Percentage of redundant SMs required for various availability targets and various maintenance intervals for an arm of the case-study HV MMC. Total height of bar is for constant-random plus wear-out failure. Mark on bar is for constant-random failure only.

for constant random failures and a smaller number of additional redundant SMs are required to cover for wear-out failures.

A striking feature of the results is that large gains in availability that can be achieved with relatively small increases in the number of redundant SMs. For instance, under a 5-year maintenance interval, 35 redundant SMs (11.4 % redundancy) achieves 90 % availability but only half as many again (51 redundant SMs or 16.7 % redundancy) achieves 99.99 % availability; a decrease in unavailability of 3 orders of magnitude. This is attractive for HVDC link operators where availability of the link is very important and the financial penalties of planned and more particularly unplanned outages are very high. As would be expected, longer the maintenance intervals require more redundant SMs to meet the same levels of availability but Figure 4.5 shows that the increase in redundancy is at a less than a linear rate for a given availability (noting the irregular spaced choices of maintenance interval). For instance, at 99.99 % availability, a 2-year maintenance interval requires 37 redundant SMs (12.1 % redundancy) but extending the maintenance interval by a factor of 4 to 8 years requires only 75 (24.9 % redundancy), a factor of 2 difference. This observation allows longer maintenance periods to be used for relatively low increase in converter size, which may be a more cost effective overall solution than shorter maintenance intervals, especially offshore where hiring maintenance vessels can be very expensive.

4.5 Conclusions on Redundancy Provision in MMCs for High Voltage

The examination of reliability of the case-study HV MMC has revealed some interesting relationships. Increasing the number of redundant SMs by a small amount increases the availability of an arm by a large amount and this is true for constant-random failures alone and when wear-out failures are also included. Thus achieving high availability expected by operators of an HVDC link does not add greatly to the size, cost and power loss of the converter.

The choice of interval for the periodic preventative maintenance is important because such maintenance can be costly, especially offshore. Extending the maintenance interval does require a greater degree of redundancy but doubling the interval requires less than twice the redundancy. Thus savings in maintenance costs might be greater than the additional cost in SMs, size and power loss.

5 Redundancy in Medium Voltage MMCs

This chapter investigates provision of redundant SMs in MMCs for MV applications considering both constant-random and wear-out failures of SMs. MMCs for MV applications require far fewer SMs than at HV because the same voltage rated SMs can be used and so fewer are needed to match the lower DC-link voltage.

Following the pattern of Chapter 4, this chapter considers the number of redundant SMs required to achieve a given arm availability under various intervals of periodic preventative maintenance albeit for arms with far fewer SMs in the base-case, but goes on to also consider reactive maintenance for reasons that will explained later. Various principles from Chapter 4 are carried over: only active redundancy is considered, in which all SMs share the total system load until a SM fails where upon it is bypassed; infant failures are neglected on the basis that they will be detected during the commissioning; wear-out failures are considered to become significant after 15 years and service life of a converter is 40 years.

The following sections of this chapter outline three MV case-study converters and explore how the availability of a converter arm is affected by constant random and wear-out failures of SMs. Because the base-case (no redundancy) number of SMs is small, the redundancy needed for realistic availability is likely to represent a large increase in SM number. For this reason, the efficiency and power-loss of the case-study MMCs will be investigated.

5.1 Case-study MMC for Medium Voltage

Practice in HVDC is to chose the highest rating IGBT available (at the current rating needed) and build SMs from that. For a foreseeable IGBT rating, there will be a large number of SMs needed and waveform quality will be good because the voltage steps will be relatively small. The choice of the largest IGBT rating is beneficial because it is generally true that on-state conduction voltage scales less than linearly with off-state blocking voltage and conduction power loss (which is the dominant term in the power losses) is reduced this way.

When attention is turned to MVDC, it is no longer certain that the number of SMs will be large enough to guarantee good waveform quality by simple voltage steps alone and in all likelihood some pulse-width modulation at a relatively high switching frequency might be needed. This raises several questions. Might it be better to use a larger number of lower voltage SMs and therefore make less use of PWM (increasing conduction power loss but reducing switching power loss perhaps more)? Do some IGBTs offer a better combination than others of conduction power loss and switching power loss properties for the conditions of an MV MMC? In this section three designs of MMC will be created to a common top-level specification of an MV MMC to explore the answers to these questions, whether there is value choosing for comparing redundant SMs, availability and efficiency for MVDC applications. As has been established, the choice of number of SMs depends on the base number needed to support the DC voltage but then a provision of redundancy on top of that. The degree of redundancy need, in turn depends on the base number of SMs in a non-linear and complex fashion. In what follows, the case-study designs will be created for a common availability target (and a common maintenance regime), they will then be operated to a common waveform quality (expressed in terms of Total Harmonic Distortion, THD) and then assessed for their efficiency.

The parameters for the three MMCs are shown in Table 5.1. All converters are designed for 30 MW, which is the power rating of the three-level NPC converter used within the ANGLE-DC project [99]. All converters are also designed for a DC-link voltage of $\pm$ 12.5 kV but they

Table 5.1: Parameters of medium voltage case-study MMCs.

	Converter 1	Converter 2	Converter 3
Power Rating	30 MW	30 MW	30 MW
DC Voltage	± 12.5 kV	± 12.5 kV	± 12.5 kV
AC Voltage (RMS)	33 kV	33 kV	33 kV
Nominal SM Voltage	2.9 kV	2.1 kV	1.1 kV
Minimum Number of SMs per Arm	9	12	23
Nominal Energy	35 kJ/MVA	35 kJ/MVA	35 kJ/MVA
SM Capacitor	4,624 μF	6,614 μF	12,576 μF

employ IGBTs of different voltage ratings and therefore require different numbers of SMs. All converters are designed around half-bridge SMs and as was the case in Chapter 4, failures of only the IGBTs, the main SM capacitor and the control electronics subsystem as a whole are considered in the reliability assessment.

The base-case (no redundancy) number of SMs required in each design, N, is calculated from Equation 5.1 where V_{DC} is the total DC voltage and $V_{SM_{Nom}}$ is the nominal voltage of the SM being considered. It is assumed that there is a converter transformer used to match the desired AC converter voltage to the actual voltage of the AC grid.

$$N = \frac{V_{DC}}{V_{SM_{Nom}}} \tag{5.1}$$

The three IGBTs of different voltage rating are listed in Table 5.2. The nominal voltage of a SM is set to 65 % the rated maximum voltage of the corresponding IGBT module to allow for voltage ripple across the SM during normal operation. The capacitor values are calculated from Equation 5.2, where S_{Base} is the power rating of the converter, E_{nom} is the nominal energy within the MMC, N is the minimum number of SMs per arm and V_{nom} is the nominal SM voltage. The values calculated were added to Table 5.1 and the type of capacitor chosen is recorded in Table 5.2. As expected, the SM capacitor value increases (but its stored energy decreases) as the nominal voltage of the SM decreases. This can be explained with reference to

Table 5.2: FIT of IGBTs, capacitors and various control electronics for medium voltage case-study.

	Component	Manufacture	Part Number	FIT
Converter 1	IGBT	Infineon	FZ1200R45HL3 [100]	100
	Capacitor	EPCOS	B25650D3258k024 [101]	100
	Control Electronics	Various	N/A	1,000
Converter 2	IGBT	Infineon	FZ1200R33HE3 [102]	100
	Capacitor	EPCOS	B25750H2448k004 [92]	100
	Control Electronics	Various	N/A	1,000
Converter 3	IGBT	Infineon	FZ1200R17HE4 [103]	32
	Capacitor	EPCOS	B25650D1608k024 [104]	100
	Control Electronics	Various	N/A	1,000

Equation 5.3, where for a given stored energy and DC bus voltage, the SM capacitance is an inverse proportion to its nominal voltage, V_{nom} and where E_{nom} is the nominal energy within the MMC and V_{DC} is the DC bus voltage.

The failure rates, expressed in terms of FIT, are taken from manufacturers data sheets of the major components, which are also shown in Table 5.2.

$$C_{SM} = \frac{2S_{Base}E_{nom}}{6NV_{nom}^2} \tag{5.2}$$

$$C_{SM} = \frac{1}{V_{nom}}\frac{2E_{nom}}{V_{DC}} \tag{5.3}$$

As was noted in Chapter 2, it is well-documented that the failure rates of IGBT modules are dependent on the applied voltage, however, it is seen in Table 5.2 that some IGBTs of different voltage ratings have the same FIT quoted by the manufacturer. This is because of the difference between changes in operating voltage of a given IGBT and changes in design of an IGBT to achieve a different maximum voltage while perhaps preserving the same maximum electric field strength. All IGBTs in the designs considered here are operated at 65 % of their maximum

voltage and so would have the same decrease in failure rate from the operating voltage reduction. The FIT of various control electronics subsystem was set at 1,000 FIT for the reasons given in Chapter 4 for the HVDC case-study converter.

The capacitors selected for three designs come from the same family of capacitors and share the same failure rate because the failure rate of these metallised film (MPPF) capacitors are dependent on material and not the voltage rating or capacitance value of the devices [87]. All the SMs require two of the selected capacitors, noted in Table 5.2, in parallel to achieve the desired capacitance noted in Table 5.1, therefore, the FIT for the composite capacitor is twice the manufacturers quoted value. This was also the case for the HVDC design in Chapter 4.

Following the principle established in Chapter 4, the failure rate of a SM is calculated by summing together the failure rate of all components or subsystems that that can individually contribute to the failure of a SM (repeated here as Equation 5.4).

$$\lambda_{SM} = 2\lambda_{IGBT} + \lambda_{Cap} + \lambda_{Control} \tag{5.4}$$

5.2 Reliability of Medium Voltage MMCs with Periodic Preventative Maintenance

Chapter 4 concluded that constant random and wear-out failures are both important factors to consider when evaluating the total number of redundant SMs required to maintain a given availability for a given maintenance interval. In this chapter, the same Markov chain and Monte Carlo simulation as outlined in Chapter 4, Figure 4.3 will be used to determine the number of redundant SMs required for each of the MVDC case-study converters. For HVDC applications, periodic preventive maintenance is preferred to keep maintenance costs and disruption to customers low. These attributes are also beneficial for MVDC applications, therefore, periodic preventive maintenance with various maintenance intervals is again investigated.

Many of the simulation considerations for the MV case-study converters are the same as those

in Chapter 4: the time-step for the Monte Carlo simulation is again a year; population size is 10,000; wear-out failures are set to become significant after 15 years and are modelled with a Weibull function (repeated here as Equation 5.5) with a shape parameter of $\beta = 5$ and infant failures are neglected.

$$q(t) = 1 - e^{-(\lambda t)^{\beta}} \tag{5.5}$$

For each converter, Monte Carlo simulations were run with a range of numbers of redundant SMs and graphs of availability plotted. From these, the percentage of redundant SMs required to achieve an arm availability of > 99.99 % were identified. These results are recorded as bar charts in Figure 5.1 for various maintenance intervals for each of the 3 converter designs. The results show similar trends in redundancy as for the 99.99 % availability case of the HVDC case-study in Figure 4.5. Notably, as the maintenance interval increases, the number of redundant SMs required increases but at less than linear rating (noting the uneven spacing of the maintenance intervals). Thus for Converter 1, 4 redundant SMs (44.4 % redundancy) are need for 2-yearly maintenance but only 7 redundant SMs (77.8 % redundancy) for 8-yearly maintenance. It is clear that these MV converters, with many fewer SMs than HV converters, also need fewer redundant SMs. Further, converter 3, with the highest base number of SMs has the lowest percentage increase in redundant SMs required than either Converter 1 or Converter 2.

These same results are also recorded in Table 5.3, where the top row for each converter expresses the percentage of redundant SMs compared to the minimum number of SMs required to operate an arm of each converter (as shown in Figure 5.1) and the second row is the required number of redundant SMs for each converter. These percentage figures emphasise that although the absolute number of redundant SMs required is small (compared to HVDC applications), they are a large relative addition to the base number of an MVDC converter. This is a concern because redundant SMs add to the conduction power loss and therefore reduce the efficiency in normal use. They will also require significant additional space for the converter.

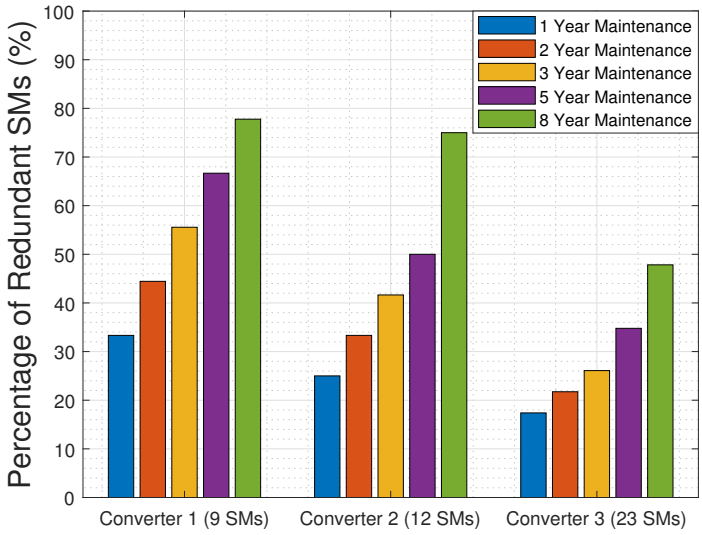


Figure 5.1: Percentage of redundant SMs required to achieve availability > 99.99 % for arms subject to constant random and wear-out failures for various maintenance intervals.

It is clear that long maintenance intervals are liable to create a large penalty in both power losses and space requirement for MV MMCs. Reducing the maintenance interval helps but even at a maintenance interval of only 1 year, the problem is still significant. Even shorter maintenance intervals would be a large burden on a network operator and this is unlikely to be tolerated. This discussion leads to the conclusion that the basis of the maintenance of the MMCs should be re-evaluated for the MV case.

Table 5.3: Number of redundant SMs required for an availability > 99.99 % for arms subject to constant random and wear-out failures.

		Maintenance Interval (Years)				
		1	2	3	5	8
Converter 1 (9 SMs per arm)	Percentage of redundant SMs	33.33 %	44.44 %	55.56 %	66.67 %	77.78 %
	No. of redundant SMs	3	4	5	6	7
Converter 2 (12 SMs per arm)	Percentage of redundant SMs	25.00 %	33.33 %	41.67 %	50.00 %	75.00 %
	No. of redundant SMs	3	4	5	6	9
Converter 3 (23 SMs per arm)	Percentage of redundant SMs	17.39 %	21.74 %	26.09 %	34.78 %	47.83 %
	No. of redundant SMs	4	5	6	8	11

5.3 Reliability of Medium Voltage MMC with Reactive Maintenance

An alternative to periodic preventative maintenance is reactive maintenance in which faulty SMs are replaced (or repaired) upon failure. Performing maintenance in this way in a transmission network is generally not acceptable because access to and down-time of valve halls needs to be planned a long way in advance to avoid conflicts with contracted power flows and because repair times tend to be long (several days) because of the slow process of ensuring complete discharge of the HV equipment. In a distribution network, equipment is more accessible, discharge times can be shorter and repair work can be scheduled into short periods of down-time that can be accommodated into normal network operation or via some network switching. Discussions with UK Power Networks (UKPN) indicated that maintenance on critical assets could be performed quickly if required and that a 5 day period to arrange for an effective repair would be the worst case. For this study the Mean Time To Repair (MTTR) was set as 5 days.

Under reactive maintenance, redundancy is still required so that the converter can continue to operate while waiting for the repair to be effected. Further, there is a small but possibly not negligible risk that while waiting for a repair to be arranged a further SM failure (or even more than one) may occur in the same arm as the failure that triggered the repair and so redundancy to cover this possibility needs to be considered.

To establish the required number of redundant SMs to achieve a given availability under reactive maintenance a new Monte Carlo simulation with a new Markov Chain model is needed. To accommodate an MTTR of 5 days will require the Monte Carlo simulation to use a time-step of a day rather than the one year, as used for periodic maintenance.

The unavailability of an individual SM is again calculated using the Weibull function to model wear-out, as in Section 5.2. The converter population is also kept at 10,000.

The proposed Markov chain, representing a single SM within an arm of an MMC, is shown in Figure 5.2. A SM in the operational state has a probability of $1-q(t)$ of remaining there for the

next time-step (the green transition arrow) and a probability of $q(t)$ of failing and taking the red transition arrow to the failed state. It then moves immediately to the maintenance state where it is no longer able to to produce voltage for the arm and it remains for the MTTR, 5 days in this example. Once maintenance has been preformed, the SM returns to the operational state and its availability is reset to the beginning of the wear-out function to represent a brand-new SM.

If a further SM (or more than one) fails whilst a SM is already in the maintenance state, then all of the failed SMs are not available to produce voltage for the arm and all stay in the maintenance state until the MTTR of the first failed SM expires and then all are repaired together with all returning together to the operational state. This reflects the fact that it is gaining access to the MMC for repair that is considered to be the largest time element rather than performing the SM replacement itself.

A converter arm is judged to have failed, and therefore the converter taken out of service, if the number of SMs in the maintenance state exceeds the redundancy provision (the number of available SMs drops below the base number given in Table 5.1). Clearly, a longer MTTR

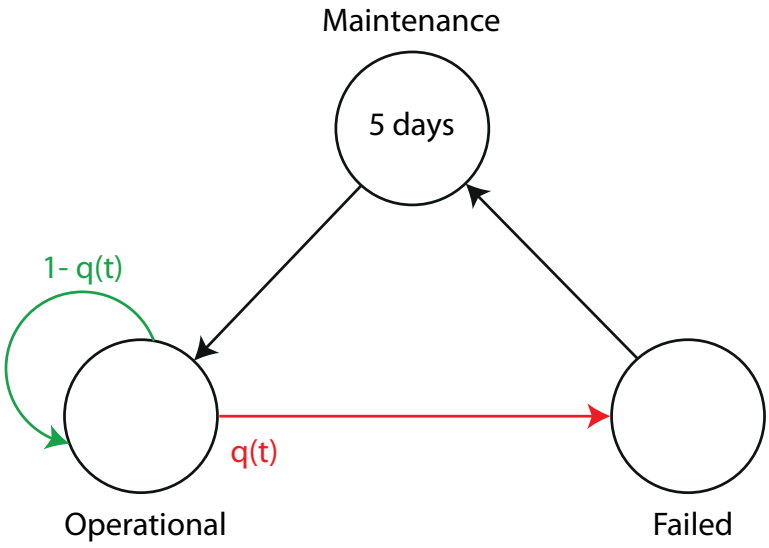


Figure 5.2: Markov Chain for a single SM within an MMC arm under reactive maintenance, where *q(t)* represents the unavailability of a SM (and a transition shown in red).

increases the risk of this occurring and a larger number of redundant SMs reduces the risk.

The Monte Carlo simulation (population of 10,000, 40 year service life) was run for three levels of redundancy provision, namely 0, 1 or 2 SMs provided in addition to the base number, for an arm of each of the three case-study converters. The effectiveness of reactive maintenance was assessed through recording the total number of times an arm required maintenance and the number of times the number of failed SMs exceeded the redundancy provision and the arm as a whole failed. These results are plotted in Figure 5.3. Sub-figure (a) shows that as the number of SMs in each arm increases, the number of maintenance instances needed over the 40 years of service increases. It is to be expected that with more SMs present, more will fail over a given time period. This is true for converters with a higher number of base SMs (Converter 3 requires more maintenance than Converter 1) and true as redundancy is added (Converter 1 with 2 redundant SMs requires more maintenance than Converter 1 in the base case).

Sub-figure (b) shows that with 0 redundant SMs, there is a significant risk of a converter arm failing due to no redundant SMs being present within the arm. None of the blue bars, redundancy = 0, achieve availability of 99.9 %. The red bars, redundancy = 1, all exceed 99.9 % and approach 100 %. Turning to sub-figure (c), which shows the corresponding unavailability on a logarithmic scale, it is clear that for redundancy = 1, the unavailability of all converters is less than 0.001 % and so availability is better than 99.999 % for Converters 1 and 2 and only slightly worse for Converter 3, which are very good results. For the case of redundancy = 2 no arm failures were found among the population of 10,000 for any of the three converters and so no yellow bars appear for unavailability.

Overall, these results show that with a MTTR = 5 days and one redundant SM, very high levels of availability can be achieved, sufficient to meet the expectations of most network operation scenarios and that if even higher availability is needed, then 2 redundant SMs would provide this.

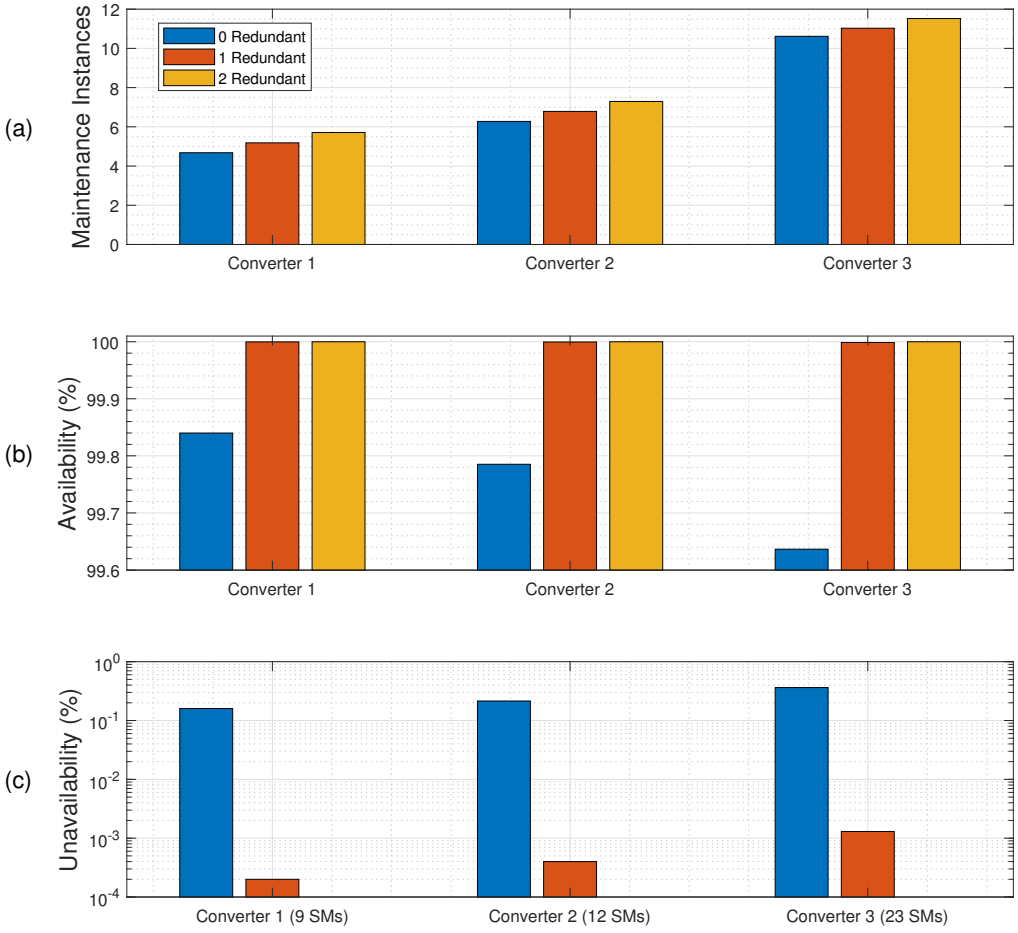


Figure 5.3: Performance of reactive maintenance for the three case-study converters and three levels of redundancy provision (0, 1 and 2 SMs) for MTTR = 5 days. Performance assessed through a) number of maintenance instances (over 40 year service life), b) availability of a converter arm and c) the unavailability of a converter arm (on log scale).

The results shown in Figure 5.3 are also provided in Table 5.4 in which number of maintenance instance and availability of each converter is displayed for each choice of redundancy. Comparing these results to those for periodic preventative maintenance in Section 5.2, reactive maintenance requires fewer redundant SMs per arm in order to achieve an availability > 99.99 %; 1 redundant SM is required for all converters performing reactive maintenance and 3 or 4 redundant SMs are required for periodic preventive maintenance set at one year intervals (taking data from Table 5.3). Yearly periodic preventive maintenance means 40 maintenance events over the service life which compares with reactive maintenance, for a converter rather than an arm, and considering one redundant SM causes 31.2, 40.8 and 66.0 events over 40 years for the three converters. So the maintenance burden is broadly comparable but the penalty in terms of added SMs (and therefore equipment cost, space and power loss) is less.

At this point it is important to note a limitation of the approach taken here. The Monte Carlo simulations are conducted for the SMs of one arm only. The availabilities quoted are for an arm and a converter would be less available because the failure of any one of the six arms causes a converter failure. Thus, the unavailability of an arm needs to be multiplied by 6 to obtain the unavailability of the converter. This holds true if the six arms are independent. However, under reactive maintenance they are not independent in terms of how repairs are conducted. If a SM failure occurs in one arm then the MTTR period is begun. If a failure of a SM occurs in

Table 5.4: Average number of maintenance instance and arm availability for the three case-study converters under reactive maintenance.

		No. of Redundant Sub-modules		
		0	1	2
Converter 1	Average Maintenance Instances	4.68	5.18	5.71
(9 SMs per arm)	Availability	99.8399 %	99.9998 %	100 %
Converter 2	Average Maintenance Instances	6.28	6.79	7.29
(12 SMs per arm)	Availability	99.7852 %	99.9996 %	100 %
Converter 3	Average Maintenance Instances	10.62	11.03	11.52
(23 SMs per arm)	Availability	99.6366 %	99.9987 %	100 %

a second arm during the MTTR of the first arm then it will be repaired together with the first arm and in less than one MTTR period from its own failure. Thus that second arm is exposed to the risk of further SM failures causing an arm failure for a somewhat shorter period, therefore, the risk of a converter failure is somewhat decreased. Treating the arms as independent when they are not in terms of repairs leads to a slightly pessimistic view of failures in the reactive maintenance case. A fuller treatment (a Monte Carlo simulation of a complete converter rather than one arm) would give different results but would still result in the conclusion that only one redundant SM is needed under reactive maintenance to achieve an availability of > 99.99 %. Thus the overall conclusions are in this section unaffected.

Periodic preventive maintenance can reduce the maintenance cost, but extending the interval to, say, 5 years, to give 8 maintenance events over 40 years which would be substantially better than reactive maintenance but (taking data from Table 5.3 requires 6 or 8 redundant SMs not 1, creating a 66 %, 50 % and 35 % increase in SM numbers (and cost, size and power loss of an arm for Converters 1 to 3. This is a very high price to pay for a reduced maintenance burden.

A variation of the approach to reactive maintenance is to only perform maintenance once all redundant SMs in an arm have failed (and the next SM failure would bring an arm and converter failure). This reduces the amount of maintenance that has to be performed over the converters life, but increases the risk of a converter failure and lowers the availability of an arm because of the risk of an additional SM failing during the MTTR (5 days in the examples here). This method was not considered further because of the unacceptably low availability.

5.4 Power Loss and Efficiency of the Case-study Medium Voltage MMCs with Redundant Sub-modules

As discussed briefly in Section 5.2, adding redundant SMs has a large impact on the efficiency of MMCs at MVDC because they are a large fraction of the base-case number of SMs; increases of between 21 % and 44 % for 2-yearly maintenance in Table 5.3, whereas in HVDC applications

an increase of 9 % was needed for 2-yearly maintenance in Table 4.4. To determine exactly the impact on efficiency of adding redundancy in MV MMC case, the three case-study converters were simulated in the time-domain in Matlab-Simulink. Care was taken to tune the current controllers to achieve the same Total Harmonic Distortion (THD) of the AC-current to maintain a fair comparison between the three converters. The waveform quality is achieved by performing PWM on the last SM inserted within the converter arm with the PWM frequency needing to be greater for MMCs with fewer SMs per arm and larger voltage steps and thus there is a penalty in switching power loss. The THD is calculated using the Root Mean Square (RMS) of the total harmonic amplitudes within the AC-current, divided by the RMS of the fundamental AC-current. The THD for each simulation was maintained at 0.35 %, which is well within the 4 % limit set by network operators for MV grid connections [105].

The power loss of the IGBT modules were assessed using the techniques outlined in Chapter 2 within Matlab-Simulink, where the IGBTs switching and conducting characteristics are taken from manufacturers data-sheets for a temperature of 125 °C.

The power loss and efficiency figures obtained for the MVDC case-study converters, and redundancy from 0 to 4 SMs, are plotted in Figure 5.4, where sub-figure (a) shows the conduction power loss of each arm, (b) shows the switching power loss of each arm, (c) shows the total power loss of each converter and (d) shows the efficiency of each converter.

As the number of redundant SMs increases, the conduction loss of each converter increases simply because more SMs are present in the conduction path. In contrast, the switching loss remains essentially independent of the number of redundant SMs because broadly the same number of voltage steps are used still, with only one SM (at any time) required to perform PWM to refine the waveform to achieve the target THD of 0.35 %. There is, however, a large difference in switching power loss between the three converters because the three designs use voltage steps of different sizes requiring different numbers of steps per cycle and the PWM is applied to SMs of different voltage steps and IGBTs of different switching characteristics. It can be seen that the higher voltage IGBTs in Converter 1 with the largest SM voltage steps,

the highest PWM frequency and the highest switching energy loss per commutation has the highest overall switching power loss.

Comparing sub-figures (a) and (b), it can be seen that for Converter 1, with the fewest SMs per arm, the switching loss dominates over the conduction loss, for Converter 2 the conduction

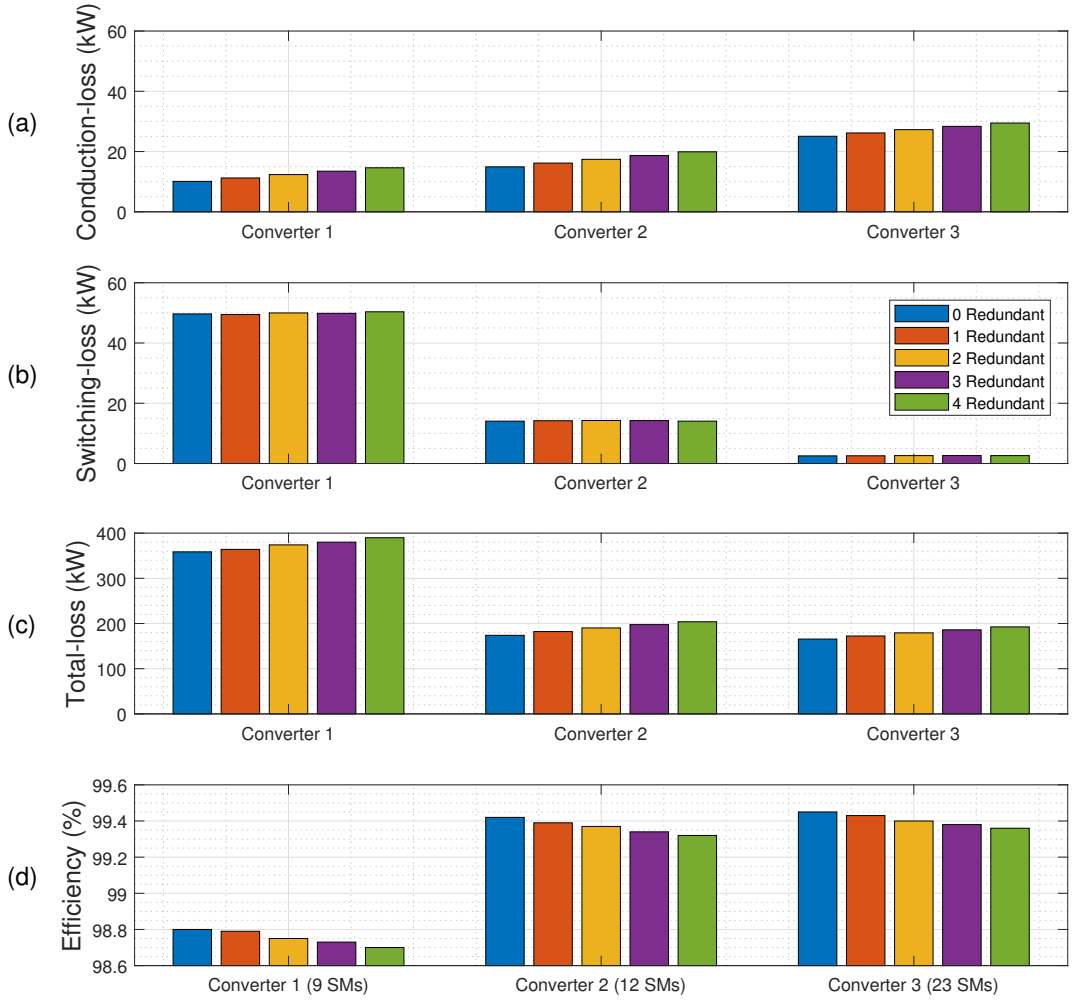


Figure 5.4: Power loss and efficiency of the three case-study MMCs with redundant SMs showing: a) conduction loss of an arm, b) switching loss of an arm, c) total power loss of a converter and d) efficiency of a converter.

power loss is slightly greater than the switching loss and for Converter 3, with the most SMs per arm, the conduction loss dominates. Turning to sub-figures (c) and (d), it is clear that Converter 1 is a relatively poor choice of high total power loss and low efficiency and that Converter 3 is a slightly better overall choice than Converter 2.

The results for the case of one redundant SM are shown again in Table 5.5. One redundant SM in each arm is sufficient under reactive maintenance to achieve availability > 99.99 % in all three converters. The results confirm that Converter 3 is the most efficient, even though Converter 3 has the greatest conduction loss of the three converters. Converter 1 and Converter 2 have fewer SMs per arm resulting in lower conduction loss when compared to Converter 3, but both converters have considerably higher switching loss due to the increased PWM required to achieve the target THD of 0.35 %. Converter 3 is the most efficient because the larger number of voltage levels generated in each arm (from more SMs of lower voltage) creates a reduction in switching power loss that more than offsets the increase in conduction loss.

Table 5.5: Power loss and efficiency of the three case-study MMCs with 1 redundant SM within each arm.

	Converter 1	Converter 2	Converter 3
Nominal SM Voltage	2.9 kV	2.1 kV	1.1 kV
Minimum Number of SMs per Arm	9	12	23
Number of Redundant SMs per Arm	1	1	1
Total Harmonic Distortion	0.35 %	0.35 %	0.35 %
Conduction Loss per Arm	11.23 kW	16.17 kW	26.17 kW
Switching Loss per Arm	49.45 kW	14.20 kW	2.56 kW
Total Power Loss	364.08 kW	182.22 kW	172.38 kW
Efficiency	98.79 %	99.39 %	99.43 %

5.5 Comparison between Periodic Preventive Maintenance and Reactive Maintenance for Medium Voltage MMCs

This chapter has explored two approaches to performing maintenance on MMCs for MVDC applications. Section 5.2 explored the periodic preventive maintenance approach that is the preferred approach in HVDC applications (and was also explored in Chapter 4). It is preferred in HVDC because of the cost penalties for unplanned outages and the long lead times needed to arrange planned maintenance (especially so for offshore applications). The alternative that may well be acceptable for MV converters in distribution networks is reactive maintenance performed very shortly after a first SM fault is detected, as considered in Section 5.3.

For reactive maintenance to achieve > 99.99 % availability with a $MTTR = 5$ days, only one redundant SM was required within each arm for all three of the case-study converters. In contrast, periodic preventive maintenance for Converter 1 and Converter 2 require three redundant SMs and for Converter 3 four redundant SMs are required to maintain availability of a converter arm > 99.99 % under yearly maintenance (and 4, 4 and 5 redundant SMs under 2-yearly maintenance).

The power loss and efficiency of the three case-study MMCs are summarised in Table 5.6 for both periodic preventive maintenance (at 1 year intervals) and reactive maintenance. It can be seen that reactive maintenance, requiring only one redundant SM, results in lower power losses, therefore higher efficiency, in comparison to periodic preventive maintenance for all three of the case-study MMCs and that this is attributable to the differences in conduction loss arising from the smaller number of SMs. It is also apparent that switching loss for all three converters is not affected by the number of redundant SMs for the reasons discussed earlier. Overall, Converter 3 designed for reactive maintenance is the most efficient.

Reactive maintenance of the case-study MMCs achieves similar availability values with fewer redundant SMs per arm, resulting in lower power loss and higher efficiencies. In the case of yearly maintenance, 40 maintenance operations are needed over the converter service life

which is broadly comparable to the number of maintenance events needed for a converter under reactive maintenance (in Section 5.3 total instances of 31.2, 40.8 and 66.0 were found for the three converters with one redundant SM).

Table 5.6: Power loss and efficiency of the three case-study MMCs with redundancy chosen to achieve > 99.99 % availability under yearly preventive maintenance and reactive maintenance.

	Converter 1		Converter 2		Converter 3	
	(Preventive)	(Reactive)	(Preventive)	(Reactive)	(Preventive)	(Reactive)
Nominal SM Voltage	2.9 kV	2.9 kV	2.1 kV	2.1 kV	1.1 kV	1.1 kV
Minimum Number of SMs per Arm	9	9	12	12	23	23
Number of Redundant SMs per Arm for > 99.99 % Availability	3	1	3	1	4	1
Total Harmonic Distortion	0.35 %	0.35 %	0.35 %	0.35 %	0.35 %	0.35 %
Conduction Loss per Arm	13.48 kW	11.23 kW	18.66 kW	16.17 kW	29.46 kW	26.17 kW
Switching Loss per Arm	49.85 kW	49.45 kW	14.26 kW	14.20 kW	2.62 kW	2.56 kW
Total Power Loss	379.98 kW	364.08 kW	197.52 kW	182.22 kW	192.48	172.38 kW
Efficiency	98.73 %	98.79 %	99.34 %	99.39 %	99.36 %	99.43 %

5.6 Conclusions on Design of Medium Voltage MMCs

The analysis in this chapter has shown that reactive maintenance for MV MMCs requires fewer redundant SMs and broadly similar maintenance interventions compared to periodic preventive maintenance at one-year intervals for all three case-study converters. This was assessed considering a combination of constant-random and wear-out failures of SMs. Each of the three case-study MMCs required only one redundant SM in each arm to achieve an availability > 99.99 % under reactive maintenance but required at least three redundant SMs in each arm under 1-year periodic preventive maintenance.

Power loss and efficiency were assessed and as expected, the smaller number of SMs needed with reactive maintenance resulted in lower conduction loss and higher efficiency than for designs for periodic preventive maintenance. The switching loss in each converter remains essentially constant regardless of the number of redundant SMs when configured to achieve comparable THD.

Increasing the interval of periodic maintenance to greater than one year would reduce the number of maintenance instances below those for reactive maintenance but the penalty in power loss for periodic maintenance would become even greater. Reducing the interval would reduce the number of redundant SMs and reduce the power loss penalty but require more maintenance than reactive maintenance.

Although only a full cost analysis based on detailed data for maintenance costs, cost of losses and equipment/space costs can precisely identify the lowest cost converter, it would seem from this analysis (for the MVDC case) that reactive maintenance yields better designs than periodic preventive maintenance and that there is advantage to choosing IGBTs of less than the maximum available rating to take advantage of the lower switching energy loss per commutation and the lower switching frequency arising from a higher number of levels. The evidence is that Converter 3 designed for reactive maintenance achieved the best efficiency of all the design options considered.

6 A Mixed-SM-Voltage MMC for Medium Voltage Applications

This chapter describes the investigation of a proposed variant of the MMC topology which was conceived for use in MVDC applications. Its distinguishing feature is that each arm contains a mixture of SMs of different nominal voltages. The motivation for this approach was the trade-offs that were observed in Chapter 5 between switching power loss and conduction power loss when choosing the SM voltages for MV MMCs. The analysis there showed that using a large number of low-voltage SMs within each converter arm resulted in high conduction power loss because of the large number of IGBTs in series in the conduction path. In contrast, MMCs with fewer but higher voltage SMs within each arm resulted in lower conduction power loss but higher switching power loss. The higher switching loss arose from the increased rate of a SM switching needed in order to maintain the THD at the target level when there were fewer voltage steps available, a factor compounded by the high energy loss per commutation event of higher voltage IGBTs. The investigation reported in this chapter explores the potential advantages of using a mixture of SM voltages within each MMC arm that might be expected from combining the reduced conduction loss of higher voltage SMs (using higher voltage rated IGBTs) with the reduced switching loss of lower voltage SMs (using lower voltage rated IGBTs). This arrangement has been termed a mixed-SM-voltage MMC.

The number of redundant SMs required within each arm for different maintenance strategies was also investigated in Chapter 5, where it was concluded converters designed for reactive

maintenance, as compared to preventive maintenance, had higher efficiencies and required comparable maintenance interventions over the expected lifetime of each converter. That analysis will be extended here to the mixed-SM-voltage MMC. The provision of redundant SMs needed to achieve a given availability under reactive maintenance is investigated with consideration of both constant random failures and wear-out failures.

This chapter will describe the main considerations in designing a mixed-SM-voltage MMC and describe the algorithm proposed for determining which SM to insert during operation of the converter considering both the realisation of the arm reference voltage and balancing of SM voltages. Power loss and efficiency of the mixed-SM-voltage MMC will be compared with results from the conventional (uniform-SM-voltage) MMCs investigated in Chapter 5, with care taken to maintain the THD of the current waveform at 0.35 % so that a fair comparison is made. The comparison will be performed with and without redundant SMs.

6.1 Outline Design for a Mixed-SM-Voltage MMC

The prime advantage of an MMC employing higher voltage SMs (themselves constructed with higher voltage IGBT modules) is the reduced conduction power loss compared to using lower voltage SMs. Further, a high voltage MMC can be constructed with relatively few SMs. For MVDC applications, for which the number of SMs is expected to be low, the disadvantage of high voltage SMs is the increased switching frequency needed to maintain a given THD, coupled with higher commutation energy loss for higher voltage switching, which results in a high switching power loss. In contrast, the advantage of lower voltage SMs is that the increased number of voltage levels available leads to reduced average switching frequency of each IGBT which, coupled with the lower commutation energy loss of lower voltage IGBTs, leads to lower switching power loss when compared to an MMC with higher voltage SMs. That advantage has to be balanced against the disadvantage, which is increased conduction loss arising from more IGBTs in series in the conduction path.

A set of mixed SM voltages within each arm of an MMC appears, at face value, to offer some interesting possibilities to mix the benefits of low and high voltage SMs. To combine the conduction power loss advantages of high voltage-rated IGBTs with the switching power loss advantages of lower voltage-rated IGBTs, high-voltage SMs would be used to contribute the majority of the MMC arm voltage while a small number of low-voltage SMs will perform arm voltage refinement through both smaller steps (increasing the number of available voltage levels) and PWM.

An example circuit schematic of a mixed-SM-voltage MMC is shown in Figure 6.1. Each of the six arms are the same and and each arm contains small SMs (illustrated as full-bridges in this instance) and large SMs (illustrated as half-bridges).

It should be noted that all SMs, and therefore all IGBTs, will have to have the same current rating because the same current flows through each of the series connected SMs and each IGBT. The studies to be reported in this chapter used IGBTs selected from the same family so that the comparisons are on the basis of the same technological generation. IGBTs of two voltage ratings that differ by a factor of approximately 3 were chosen from the manufacturer Infineon and are described in Table 6.1. The choice of nominal SM voltage that will be used with these IGBTs follows the practice adopted in Chapter 4 and Chapter 5 of being set as 65 % of the voltage rating of the IGBT. This allows for SM voltage ripple of 10 % plus some deviation of average SM voltage from its nominal value and some headroom to accommodate device switching transients.

The principle behind mixing SMs of two different nominal voltages in an arm is that the bulk of the required arm voltage will be provided by the large (higher voltage) SMs, and there will

Table 6.1: IGBT choice for mixed-SM-voltage MMC.

Manufacture	Part Number	Current Rating	Voltage Rating	Nominal SM Voltage
Infineon	FZ1200R45HL3 [100]	1200 A	4500 V	2900 V
Infineon	FZ1200R17HE4 [103]	1200 A	1700 V	1100 V

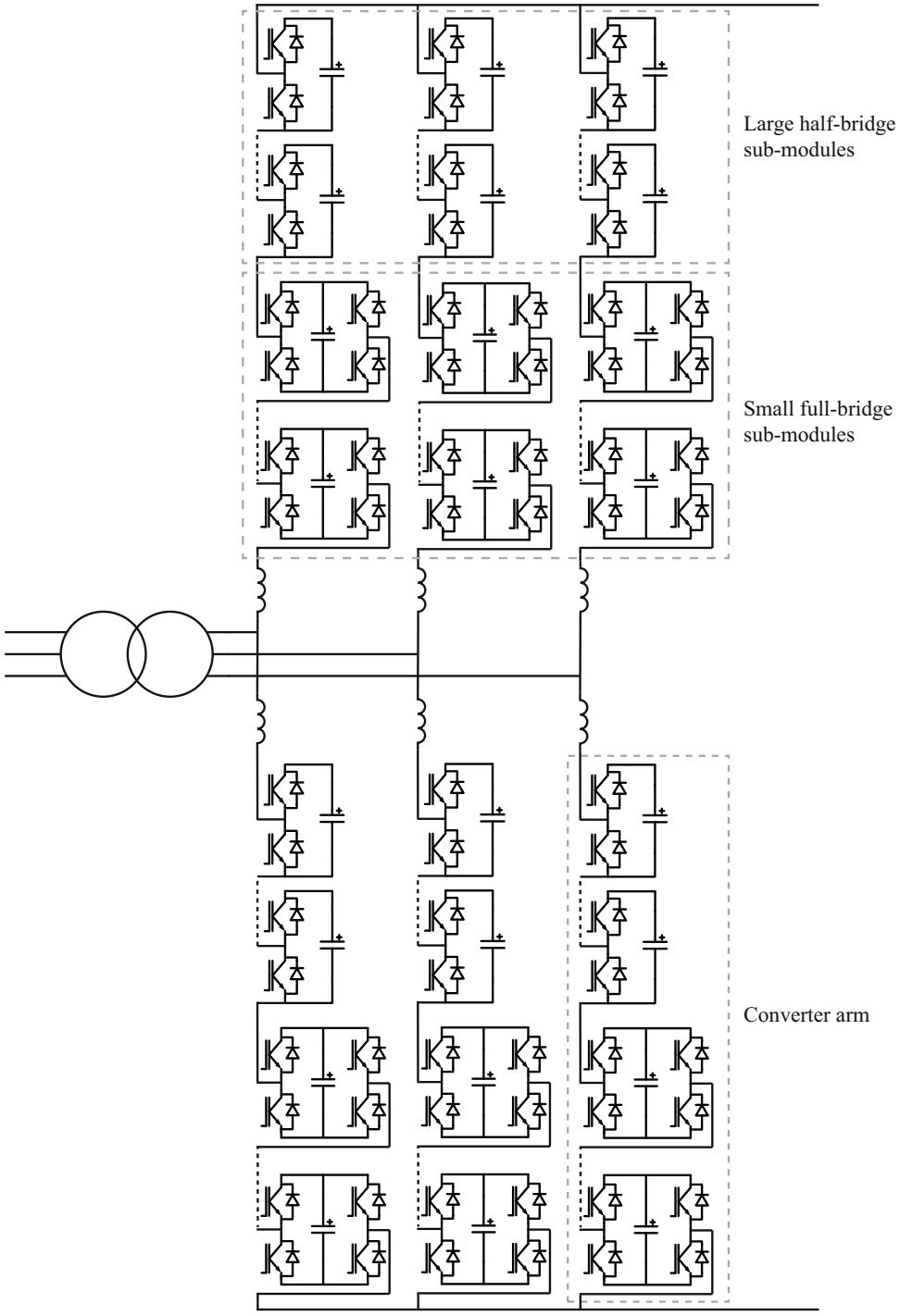


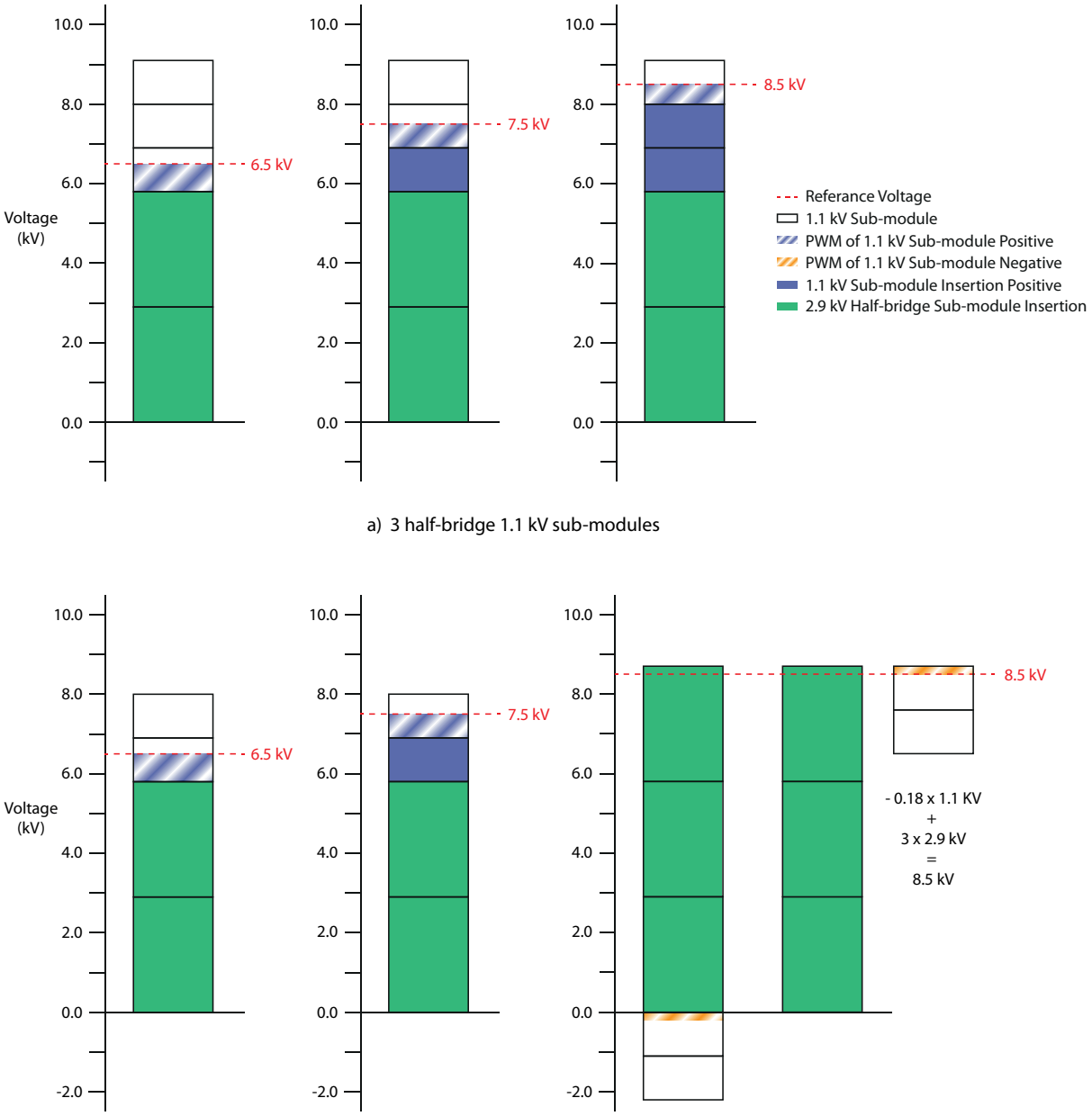
Figure 6.1: Proposed mixed-SM-voltage MMC with two SM types in each arm: large half-bridge SMs and small full-bridge SMs.

be many such large voltage SMs, and then the small (lower voltage) SMs, few in number, will be used to refine that voltage to meet the reference arm voltage as closely as possible either by simply providing smaller steps in voltage or by also pulse-width modulating the inserted voltage to give an accurate average voltage. With the small SMs being set at 1.1 kV and the large SM at 2.9 kV (Table 6.1), the ratio is slightly greater than 1:3 and therefore 3 small SMs can provide the necessary intermediate voltages within the range of one large SM. This choice of 3 small SMs assumes that the small SMs are half-bridges and can contribute only positive voltages into the arm to add to the voltage from the large SMs. If the small SMs were full-bridges then they could add or subtract from the voltage of the large SM and then only 2 would be needed to cover the range of a large SM, as illustrated in Figure 6.2.

Generally, half-bridge SMs are to be preferred because they produce lower conduction loss from fewer IGBTs in the conduction path and this argument prevails in MMCs if DC-side fault blocking is not required. For the mixed-SM-voltage MMC described here, half-bridge SMs are used for the large SMs. For the small SMs, as considered in Figure 6.2, three half-bridge SMs have 3 IGBTs in the conduction path whereas two full-bridge SMs have 4 IGBTs in the path and so on conduction loss ground the three half-bridge SMs would be preferred. There is, however, a further consideration in choosing between half- and full-bridges for the small SM.

It was found through time-domain simulations of designs for various DC-bus voltages that if only half-bridges are used for both the small (1.1 kV) and large (2.9 kV) IGBT modules, then the opportunities to balance the charge on the small SMs were very restricted because they are in near constant use (under PWM) for matching arm voltage reference. Not only are the small SMs in use of a high proportion of the time, they are consistently used in the same sense with respect to the current over each half-cycle. In many cases, SM voltage balancing was not possible and the SM capacitor voltages would drift away from their nominal values.

The problem of charge balancing the small SMs could be addressed by adding more small half-bridge SMs so that more opportunities to balance would be created but this would add to conduction loss. Alternatively, PWM could be applied sometimes to the large SMs to free-up



a) 3 half-bridge 1.1 kV sub-modules

b) 2 full-bridge 1.1 kV sub-modules

Figure 6.2: Illustration of how large and small SMs can be combined to meet various arm voltage references: (a) with 3 half-bridge 1.1 kV SMs available in addition to the 2.9 kV SM and references of 6.5, 7.5 and 8.5 kV; (b) with 2 full-bridge 1.1 kV SMs available and other conditions the same.

the small SMs for balancing, but this would increase the switching loss.

It would appear that using half-bridges for the small SMs is not attractive. In contrast, using full-bridges was found, in simulation, to work well based on two small SMs and a voltage ratio of just less than 3:1, confirming the example illustrated in Figure 6.2 (b). The balancing algorithm has sufficient freedom in choosing the states of the small SMs such that the SM voltages can be held close to their nominal values. In large measure, this is because the SMs are inserted in both the positive sense (to add to voltage from the large SMs when the nearest large SM level is smaller than the reference) and in the negative sense (to subtract voltage from the large SMs when the nearest large SM level is a greater than the reference). Thus, the sense of the inserted voltage with respect to the current is frequently changed across each half-cycle and opportunities to allocate the duties of the small SM to achieve charge balancing are created. However, facilitating balancing of the small SMs by using full-bridges is achieved at the penalty of somewhat increased conduction losses as noted above.

This evidence that balancing is feasible for SMs of mixed voltages and with a small number of full-bridge small SMs, will be presented later in this chapter as time-domain simulations obtained in Matlab-Simulink but before that, the algorithm for the modulation and control processes necessary to run such a simulation model needs to be described.

6.2 A Modulation and Voltage Balancing Algorithm for a Mixed-SM-Voltage MMC

This section will set out a modulation strategy for choosing the correct combination of SMs to insert to achieve the reference voltage set for an arm and the voltage balancing algorithm that modifies the insertion choices to ensure each SM maintains its average voltage close to its nominal value. This has been developed for a ratio of SM voltages of a little less than 3:1 but could be adapted to other ratios. The overall controller used for the converter adopts the architecture proposed in [20] and introduced briefly in Chapter 1. The modifications to the

controller discussed within this chapter relate to the low-level controller only.

The low-level controller receives arm voltage references from the current controller and it has the task of generating the SM firing sequence for the arm, including any rotation or variation of SM duties to balance the SM voltages. This is sometimes referred to as the insertion index of the arm. To reproduce the voltage reference with good fidelity and hence provide good current tracking and low THD of AC-current waveforms, one of the small SMs has its voltage pulse-width modulated to give a fine resolution of the total voltage.

The algorithm for the proposed low-level controller is expressed as a flow chart in Figure 6.3. The inputs to the proposed algorithm are the arm reference voltage (as determined by the higher-level current controller), the measured voltages of each SM, and the arm current (necessary to assess the expected direction of SM voltage deviation).

It is assumed here that the voltages of the large SM are allowed to deviate by ± 10 % from their nominal voltage, in other words the voltage ripple of a 2.9 kV SM should be kept in the range 2.61 kV to 3.19 kV. To achieve this, re-evaluation of the insertion states of SMs is triggered by not only a change in arm reference voltage but also on detection that the voltage of any of the large SMs has reached the upper or lower limit. A re-evaluation is also needed if the arm current changes direction because this changes the direction of voltage change of the inserted SMs.

A voltage deviation of the small SMs does not trigger a re-evaluation of the insertion states because this could lead to very frequent re-evaluations and excessive switching. Instead, during each re-evaluation triggered for other reasons, the small SMs are assessed against a stricter ± 7 % deviation threshold and insertion reconsidered alongside the large SMs. The ± 7 % range equates to voltage ripple between 1.023 kV and 1.177 kV which is well within rated limits of the IGBT and allows a margin for deviation of the voltage before the next re-evaluation is triggered by other factors. However, because of coding limitations discussed below, these limits are not strictly followed and larger deviations will be observed in practice. The stricter threshold for small SMs is in place to allow for the fact these wider deviations occur.

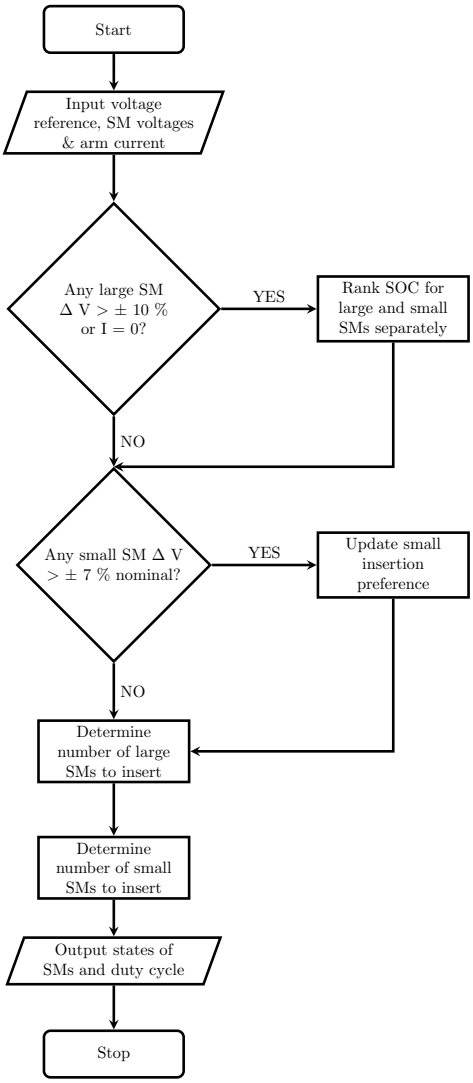


Figure 6.3: Main flow chart of proposed modulation scheme and voltage balancing algorithm for a mixed-SM-voltage MMC.

The first stage of assessing which SMs to insert consists of ranking the SMs according to their measured voltage (or state of charge, SOC). The large and small SMs are ranked in separate lists.

Small SMs are assigned an insertion preference which states whether, for voltage balancing reasons, it is better that they be inserted to create positive or negative voltage. If the voltage of the small SMs are within the ± 7 % threshold, then its existing insertion preference is left unchanged. If the voltage exceed the ± 7 % threshold then the SMs should preferably be inserted in the opposite sense (recalling that the small SMs are full-bridge) in order to change the direction of current flow through the SM capacitor and reverse the direction of voltage change. This will also reverse the inserted voltage and so the algorithm must account for this in the overall voltage generation.

There are four conditions to consider arising from two factors each with two states.

1. If SM is above its nominal voltage and if the current flowing through the arm is positive then the SM preference is to be inserted with positive arm voltage contribution.

2. If SM is above its nominal voltage and if the current flowing through the arm is negative then the SM preference is to be inserted with negative arm voltage contribution.

3. If SM is below its nominal voltage and if the current flowing through the arm is negative then the SM preference is to be inserted with positive arm voltage contribution.

4. If SM is below its nominal voltage and if the current flowing through the arm is positive then the SM preference is to be inserted with negative arm voltage contribution.

Insertion preferred can be expressed more conveniently as an exclusive-or operation:

(positive insertion preferred) = (SM voltage above nominal) XOR (current flow positive).

The determination of insertion preference for the small SMs is illustrated in the flowchart of Figure 6.4.

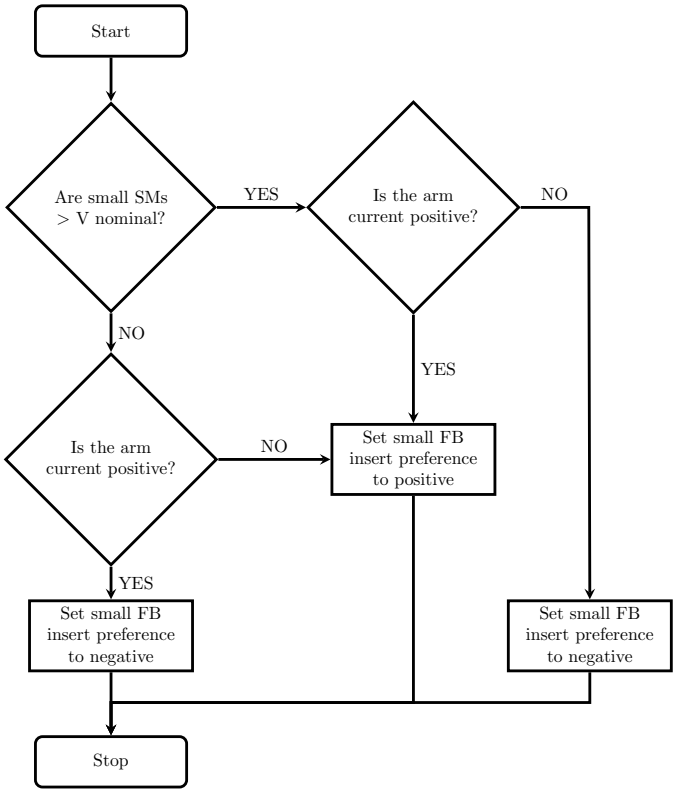


Figure 6.4: Flow chart for determining insertion preference of a small (full-birdge) SM.

The choice of the number of large (2.9 kV) SMs to insert begins by finding the number that would yield an inserted voltage just less than the reference voltage. If the current flowing through the arm is positive, then SMs are selected from those with the highest SM voltage in the rank ordered list of large SMs. If the current is negative then SMs are selected from those with the lowest SM voltage. This is described in Figure 6.5.

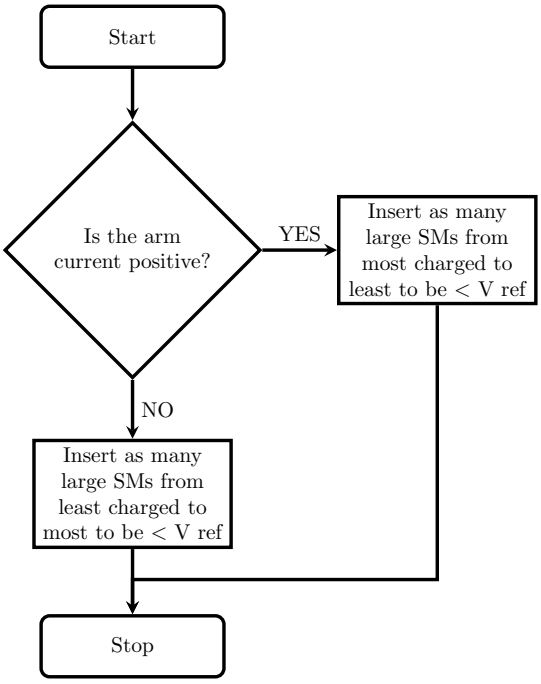


Figure 6.5: Flow chart for determining how many and which large (half-bridge) SM to insert.

The next task in the main algorithm is to determine how many small SMs to insert and what duty-cycle to assign. The algorithm for this is shown in Figure 6.6. The controller first examines whether or not it is necessary to include one more large SM to create a voltage greater than the reference voltage and then insert small (full-bridge) SMs with negative voltage contribution. This decision is based around the small (full-bridge) SM preference of being inserted positive or negative to balance voltages. If an additional large SM is available and at least one small SM has a preference to be inserted negative, then a large SM is inserted giving a voltage from the large SM above the reference voltage and the small SM applied accordingly.

If the conclusion was to insert an extra large SM but all have already been inserted then all the small SMs are inserted with positive voltage even when this overrules the insertion preference because in this case, generating the required arm voltage takes precedence. It is likely that the MMC would be designed to avoid this situation in all but exceptional circumstances.

The controller then determines how many small full-bridge SMs need to be added to the the number of large SMs that have been selected with the objective of meeting the reference value of the arm voltage. If the reference voltage can be achieved by inserting only one full-bridge SM, then one is inserted and given a duty-cycle to PWM to refine the arm voltage. If one full-bridge SM is not enough, then the controller inserts one and then checks if the reference voltage can be achieved by inserting the second full-bridge SM. If so, then the second is inserted and assigned a duty-cycle. If inserting both small SMs is insufficient to achieve the reference voltage, then the insertion preferences of the small SMs are inverted and the process retried, including the decision on whether an extra large SM is required.

The final output from the algorithm is the state (index) of every SM which for the large SM is either 0 or +1 and for the small SM is either -1, 0, +1 or a PWM duty-cycle between -1 and +1. Generally there will always be one of the small SMs assigned a PWM duty-cycle in order to accurately match the arm reference voltage.

This algorithm is performed independently for the six arms of the converter.

A controller based on this algorithm code was created in the Matlab-Simulink environment for

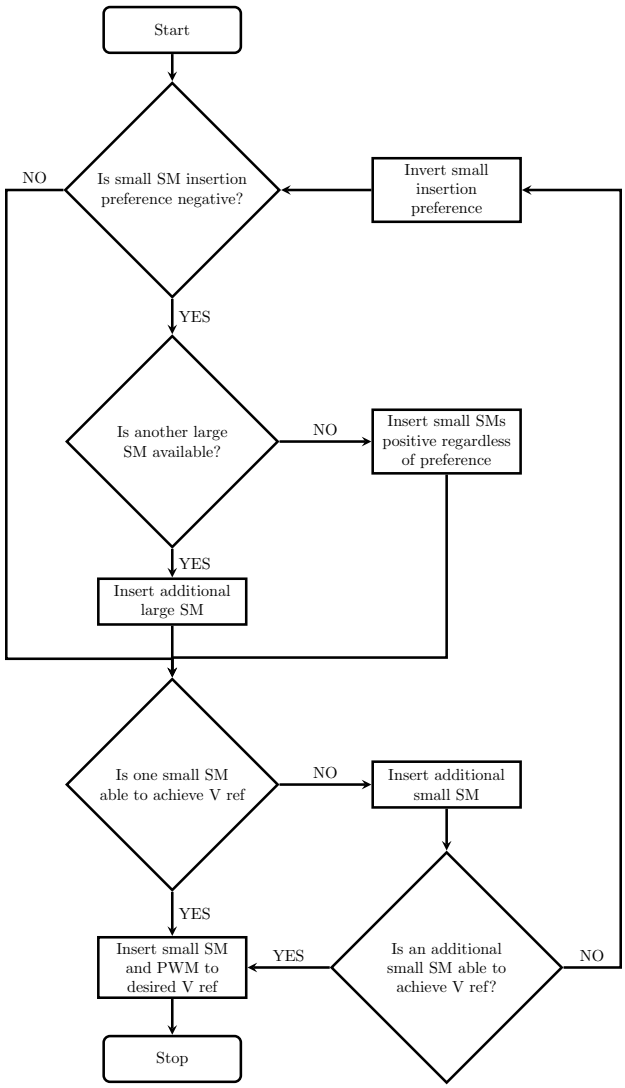


Figure 6.6: Flow chart for determining which small (full-bridge) SMs to insert and in which direction.

use in simulation to evaluate efficacy of the mixed-SM-voltage MMC concept and in particular its power loss and efficiency performance.

6.3 Case-study Design of a Mixed-SM-Voltage MMC

This section describes a case-study design of a mixed-SM-voltage MMC. The outline specification for the converter design is given in Table 6.2. The power rating of the converter is 30 MVA, which is the same power rating as the converters studied in Chapter 5 and is understood to be broadly similar to the MVDC converter used in the ANGLE-DC project [99]. The SMs for this case-study use the IGBTs previously detailed in Table 6.1: the 4.5 kV IGBT is used in half-bridge SMs with a 2.9 kV nominal voltage and the 1.7 kV IGBT used in full-bridge SMs with a 1.1 kV nominal voltage. The converter has been designed to have a stored energy of 35 kJ/MVA, which is the same nominal energy used in case-studies in Chapter 5 and is typical of values used in the literature [54]. The DC voltage is also the same as in Chapter 5 so that a direct comparison between topologies can be made. It is assumed that a converter transformer will be used to match the AC converter voltage (chosen to optimise the converter design) to the AC grid voltage.

The converter will be operated according to the principles laid out in Section 6.1. Equation 6.1 is used to determine how many large half-bridge SMs are required where N_{HB} is the minimum number of large half-bridge SMs per arm, V_{DC} is the DC voltage, V_{FB} is the nominal voltage of the small SMs and V_{HB} is the nominal voltage of the large SMs.

$$N_{HB} = \frac{V_{DC} - 2V_{FB}}{V_{HB}} \tag{6.1}$$

The stored energy of the converter is partitioned between the large and small SMs with different capacitance values calculated for each according to a pro-rata value of stored energy for the rating of the SM group. This is shown in Equation 6.2, where C is the capacitor value, V_{SM} is the nominal SM voltage for the respective SM designs, I_{DC} is the DC current and E_{nom}

Table 6.2: Specification of case-study mixed-SM-voltage MMC.

	Converter 4	
Power Rating	30 MVA	
DC Voltage	± 12.5 kV	
AC Voltage (RMS)	33 kV	
SM Topology	Large Half-bridge	Small Full-bridge
Nominal SM Voltage	2.9 kV	1.1 kV
Number of SMs per Arm	8	2
Nominal Energy	35 kJ/MVA	
SM Capacitor	4,624 μF	12,576 μF

is the nominal energy of the converter. As was established in Chapter 5, there is an inverse relationship between the value of SM capacitance and the nominal SM voltage (for a given DC bus voltage and nominal energy rating of the converter) and therefore the small SM requires a higher value of capacitance (but a lower stored energy given the lower voltage) when compared to the large SMs.

$$C = \frac{I_{DC}\, E_{nom}}{3\, V_{SM}} \tag{6.2}$$

The availability of the mixed-SM-voltage converter was analysed using the principles established in the earlier chapters. The FIT values of the IGBTs and capacitors are shown in Table 6.3. The IGBTs and capacitors are the same components as used in Chapter 5 for Converter 1 and Converter 3 (as recorded in Table 5.1). The IGBTS come from the same family of devices and all IGBTs have the same current rating. The IGBTs failure rates were taken from the data-sheets or supplied by the manufacturers directly where necessary. Interestingly, the lower voltage IGBT also has a lower FIT value. The capacitors were selected to have the same failure rate as those used in Chapter 5 noting that the failure rate of MPPF capacitors is dependent on the material and not the voltage or current rating of the capacitor (as was explained in Chapter 2). In common with all the other case-studies in this thesis, the FIT for

Table 6.3: FIT of IGBTs, capacitors and control electronics used for the case-study mixed-SM-voltage MMC.

	Component	Manufacture	Part Number	FIT
Large (half-bridge) SM	IGBT	Infineon	FZ1200R45HL3 [100]	100
	Capacitor	EPCOS	B25650D3258k024 [101]	100
	Control Electronics	Various	N/A	1,000
Small (full-bridge) SM	IGBT	Infineon	FZ1200R17HE4 [103]	32
	Capacitor	EPCOS	B25650D1608k024 [104]	100
	Control Electronics	Various	N/A	1,000

the control electronics of each SM (as a complete sub-system) was estimated to be 1,000 FIT.

The total FIT of a SM is calculated by summing together the failure rates of all components (or sub-systems) that can independently cause a failure of a SM; the sum is appropriate because failure of any one of the IGBTs, the main SM capacitor and electronic control sub-system. This is expressed as Equation 6.3 and Equation 6.4, noting that the full-bridge SM requires two more IGBTs than the half-bridge SM. The capacitors for the two SMs, noted in Table 6.3, were chosen to maintain a fair comparison with the converters in Chapter 5.

$$\lambda_{HB\,SM} = 2\lambda_{IGBT} + \lambda_{Cap} + \lambda_{Control} \tag{6.3}$$

$$\lambda_{FB\,SM} = 4\lambda_{IGBT} + \lambda_{Cap} + \lambda_{Control} \tag{6.4}$$

6.4 Simulation of the Mixed-SM-Voltage MMC

The case-study MMC, with the proposed algorithm for modulation and voltage balancing, was simulated in the time-domain using Matlab-Simulink.

Figure 6.7 shows the arm voltages and arm currents of the converter when operating at rated power over two cycles. Rated power is shown because this is where the largest SM voltage

ripple is expected. The voltages inserted into the arm by the large and small SMs are shown separately in sub-figures (a) and (b). The large SMs contribute a simple stepped waveform with little additional switching. The small SMs are seen to switch frequently throughout the cycle. The sum of the two arm voltage contributions, the total arm voltage, is shown in sub-figure (c) and is seen to be a relatively smooth and accurate reproduction of a typical arm voltage reference. As a consequence, the current shown in sub-figure (d) is a good quality sine wave; the THD of the current was measured as 0.35 %. This demonstrates that the controller has partitioned the voltage generation successfully such that the large SMs provide the bulk of the voltage and the small SMs refine the waveform to achieve low distortion.

The operation of the converter during a ramp in power, from -1 p.u. to +1 p.u., is shown Figure 6.8 in which sub-figure (a) shows the power reference. This test will reveal whether the algorithm for modulation and voltage balancing copes well with transients and disturbances to the converter operating point. The SM capacitor voltages of the large and small SMs are shown separately in sub-figures (b) and (c). It is shown that the large SMs are held close to their 2.9 kV nominal voltage and generally within the ±10 % range intended even though the operating point is in transition. Similarly, the voltages of the capacitors of the small SMs remain within ±7 % of their nominal value. Sub-figures (d) and (e) show the arm and phase current respectively and reveal that low distortion waveforms are also maintained during the transient.

The simulation results have proven that the proposed mixed-SM-voltage MMC worked as was anticipated by the foregoing analysis. Specifically, the majority of the arm voltage is provided by large SMs which are switched infrequently and the waveform quality is ensured by a small number of smaller SMs that switch much more frequently (but were configured for low switching power loss) and that with a well-designed low-level control algorithm, the SM voltages are held within their target range even during power ramps.

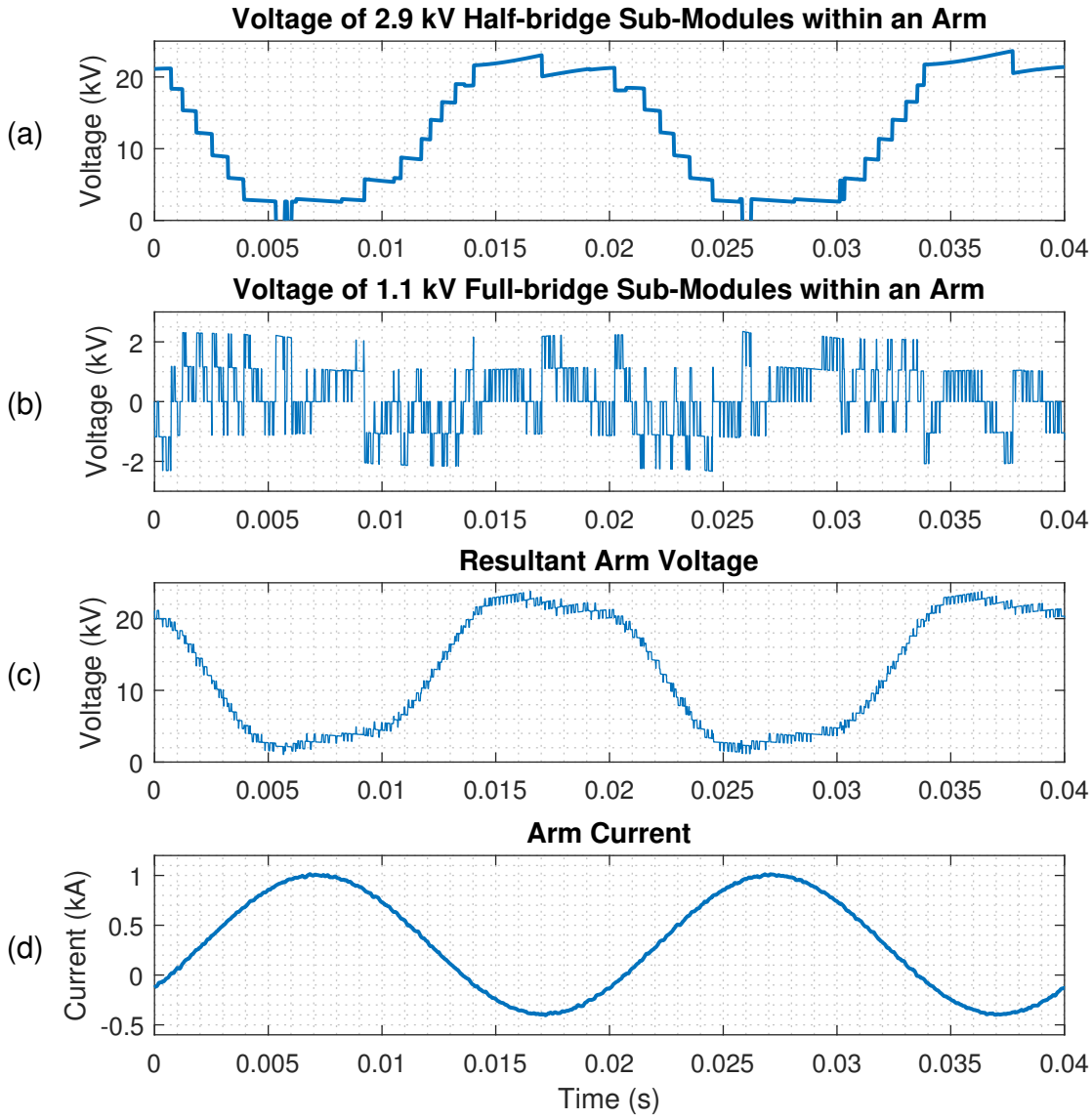


Figure 6.7: Simulation results for mixed-SM-voltage MMC in steady-state: a) arm voltage contribution of the large (2.9 kV) SMs, b) arm voltage contribution of the small (1.1 kV) SMs, c) total arm voltage and d) arm current.

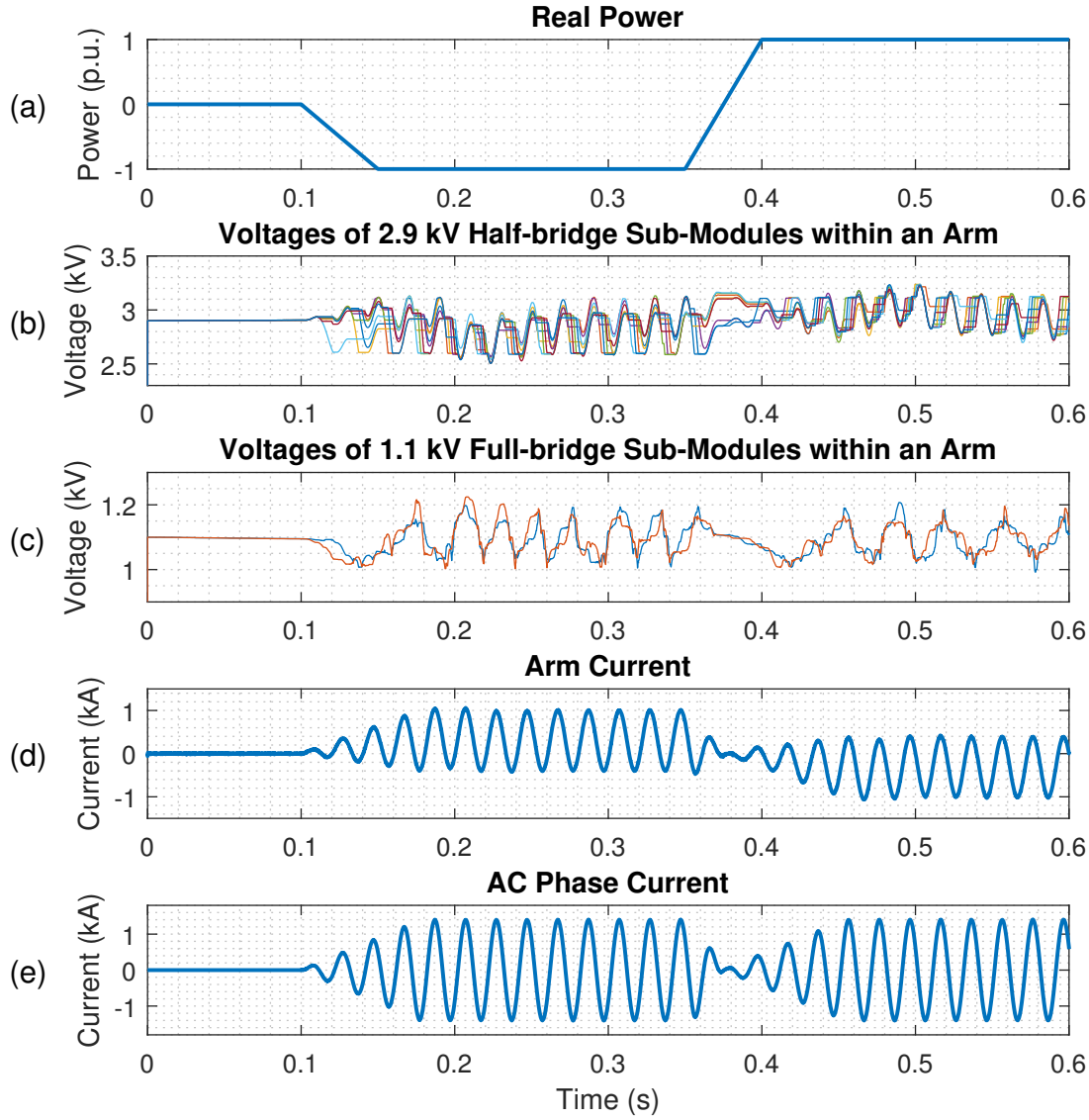


Figure 6.8: Simulation results for mixed-SM-voltage MMC during a power ramp: a) active power reference, b) SM voltages for large SMs, c) SM voltages for small SMs, d) arm current and e) AC phase current.

6.5 Experimental Verification of Mixed-SM-Voltage MMC

To experimentally validate the proposed mixed-SM-voltage MMC, including verification of the modulation algorithm and voltage balancing algorithm, the controller developed for the Matlab-Simulink simulation described in Section 6.2 was transferred to OPAL-RT control platform of the lab-scaled MMC that was described in Chapter 3.

The specification of the lab-scaled MMC with mixed SM voltages is shown in Table 6.4. The ratio between voltages of the small and large SMs was chosen to be the same as the case-study converter in Table 6.2, i.e., approximately 3. Each arm of the experimental converter was configured with two 50 V full-bridge SMs and eight 150 V half-bridge SMs. The SM design in the lab-scale converter allows for different connection points so that they can be configured as full- or half-bridges. The small SMs are identical to the large SMs within the experimental set-up but simply run at a lower voltage.

To achieve the desired capacitance for the small 50 V SMs, additional capacitance was added to each of the full-bridge SMs via a connector on the SM, as each SM capacitor is designed for 150 V operation and therefore has a lower than required capacitance. The increase in capacitance was slightly less than 1:3, which is the voltage ratio between the large and small voltage SMs. The SM capacitors operating at 50 V are slightly smaller than required due to component availability, which means that the small SMs will suffer greater voltage variation (in

Table 6.4: Parameters of the experimental mixed-SM-voltage MMC.

Characteristic	Value	
Power Rating	12 kW	
DC Voltage	± 640 V	
AC Voltage	630 V	
Sub-module Topology	Large Half-bridge	Small Full-bridge
Number of Sub-modules per Arm	8	2
Sub-module Nominal Voltage	150 V	50 V
Sub-module Capacitor	1160 μ F	3360 μ F

absolute and relative terms) than if an appropriate capacitor choice had been available.

The power rating of the lab-scaled MMC is 12 kVA, the DC-bus voltage is ± 640 V and rated DC current is 10 A. In the experiment, the DC voltage was provided by two DC power supplies in series (to give a bi-pole supply of ± 320 V) and the the 3-phase AC voltage of 400 V was provided by a 90 kVA inverter.

Waveforms measured during operation of the experimental converter are shown in Figure 6.9. The plots cover approximately one and half cycles of steady-state operation at a power of 12 kW and 0.2 kVAr. Sub-figure (a) shows the SM capacitor voltages of the eight large (150 V) SMs and these are seen to vary within ±15 V of the nominal 150 V which corresponds to the intended ± 10% tolerance. The SM capacitor voltages of the two small SMs seen in sub-figure (b) operate with ± 9 V of their nominal 50 V which is slightly wider than the intended ± 7% but is largely explained by the use of slightly smaller than necessary SM capacitors, as explained above.

Sub-figures (c) and (d) record the arm voltage contributions of the large and small SMs which show the expected simple stepped waveform from the large SMs and the PWM and rapid switching of the small SMs. Five basic levels are discernible in the voltage from the small SMs which is as expected for two full-bridge SMs. Sub-figures (e) and (f) show that the arm voltage and arm currents are of high waveform quality.

The semiconductors in the lab-scale converter have relatively high forward voltage drops compared to the nominal SM voltages, so efficiency measurements would not be meaningful. Due to differences in optimum capacitor sizing for lab operation and slight different ratio in voltages between large and small SMs, a direct comparison in wave-forms is not representative and therefore has not been performed.

Further experimental results of the modulation and voltage balancing algorithm for the mixed-SM-voltage MMC can be found in Appendix B.

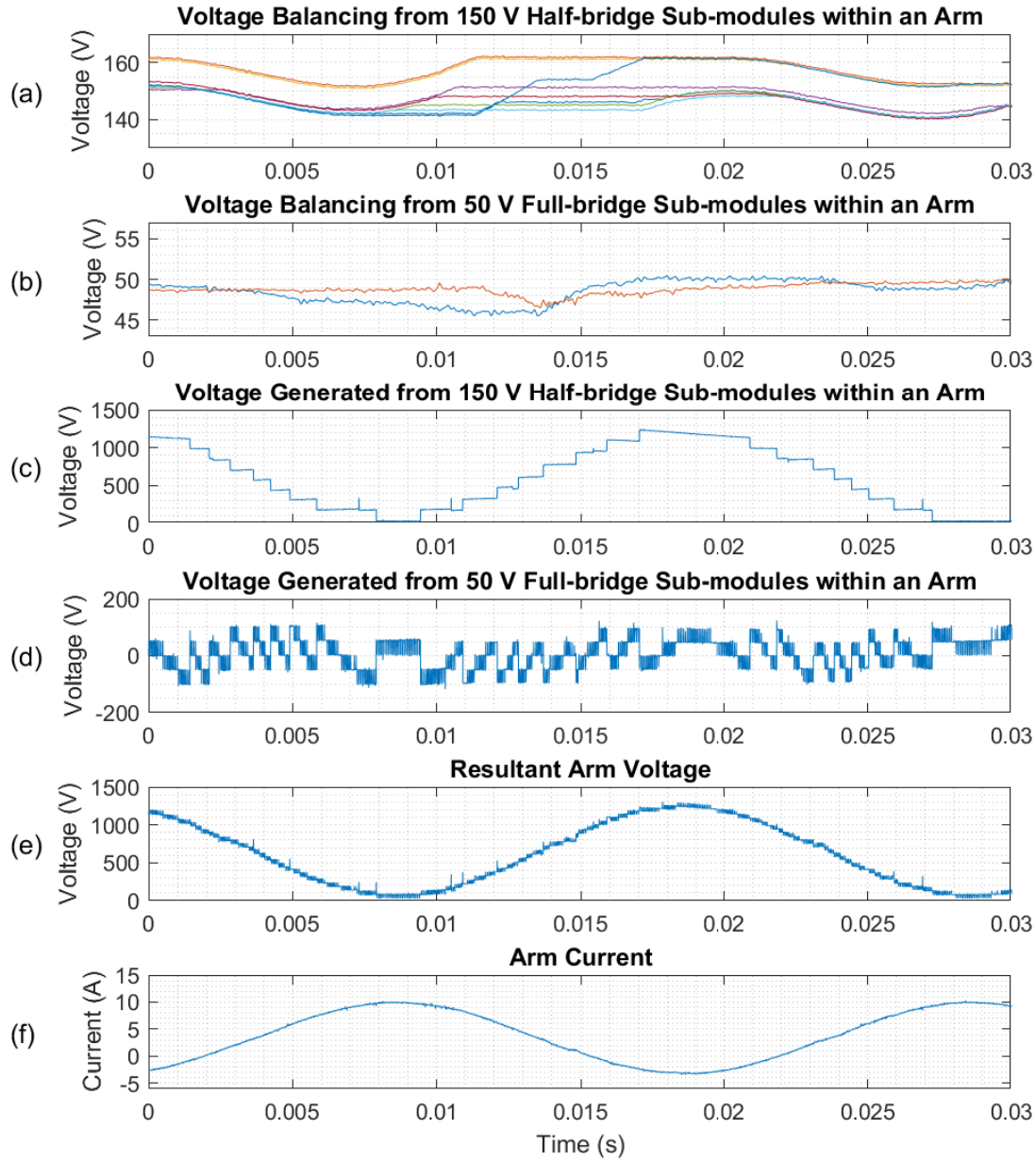


Figure 6.9: Experimental results for the lab-scale mixed-SM-voltage MMC showing: a) SM voltages of the eight large (150 V) SMs, b) SM voltages of the two small (50 V) SMs, c) arm voltage contribution of the large SMs, d) arm voltage contribution of the small SMs, e) resultant arm voltage and f) arm current.

6.6 Power-loss Assessment of a Mixed-SM-Voltage MMC

The mixed-SM-voltage MMC was conceived, following the findings in Chapter 5, to exploit the low conduction power loss possible with high-voltage SMs to provide the bulk of the power processing and exploit the low switching power loss of low voltage SMs to provide good waveform quality. Having proved that the proposed converter functions as expected, attention must now turn to validating the expectations on power loss and to evaluating availability.

Efficiency will be assessed through running a time-domain simulation that includes tracking of conduction and switching power losses and the results can be directly compared with those obtained in Chapter 5 for various conventional MMC designs. All the designs are for same MVDC case-study conditions and so feature relatively few SMs.

The power loss assessment is for the converter outlined in Table 6.2 that uses the IGBTs in Table 6.1. To ensure a fair basis for comparison, the converter controller is tuned to achieve a THD of the AC-current waveform of 0.35 % by adjusting the frequency of the PWM applied to the small SM. The power loss studies use the same techniques outlined in Chapter 2 for simulation within Matlab-Simulink. Conduction and switching characteristics for both IGBT modules are taken from the relevant data-sheets for a junction temperature of 125 °C.

The power loss and efficiency results of the proposed mixed-SM-voltage MMC were compared to those of the converters studied in Chapter 5 and the results are shown in Figure 6.10. Converter 1, Converter 2 and Converter 3 are the conventional MMCs from Chapter 5 and Converter 4 is the proposed mixed-SM-voltage MMC. The results for the conventional MMCs are those for zero redundant SM and therefore correspond to Figure 5.4.

Considering first the conduction loss, shown in sub-figure (a), Converter 4 is seen to have the second lowest conduction loss after Converter 1 (the MMC with the fewest SMs per arm). This is as expected because conduction loss is largely determined by the number of SMs within a converter arm. Converter 4 has 10 SMs, the second lowest of the four converters.

Turning to switching loss, shown in sub-figure (b), Converter 4 is again seen to have the

second lowest loss but in this case Converter 3 (the MMC with the most SMs per arm) is the lowest. With a greater number of lower voltage SMs, a good quality waveform can be produced with less switching.

When looking at the total power loss, sub-figure (c), Converter 4 which was second lowest on the two sub-categories emerges as best overall and consequently Converter 4 is the most efficient, as confirmed in sub-figure (d). It should be remembered that these results are for an

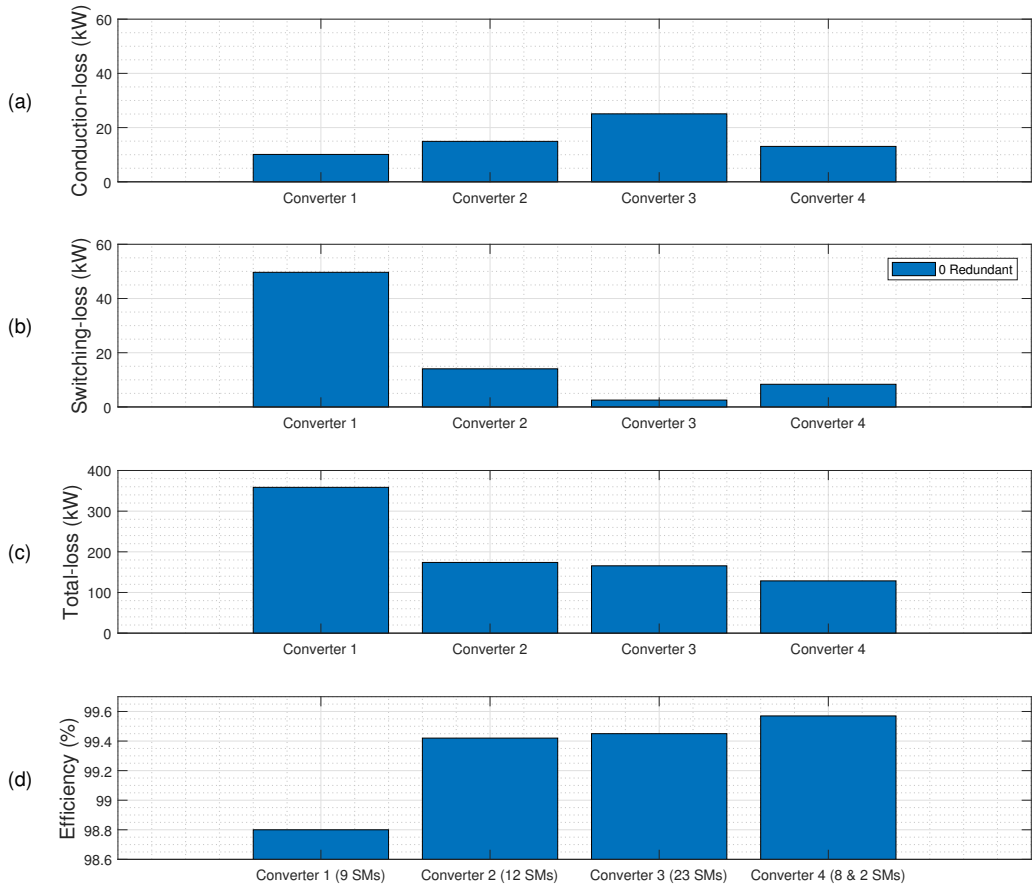


Figure 6.10: Power loss and efficiency of the three conventional MMCs from Chapter 5 and the proposed mixed-SM-voltage MMC: a) conduction loss per arm, b) switching loss per arm, c) total power loss of the converter and d) efficiency.

MMC intended for MV use and with relatively few SMs compared to an MMC intended for HV.

The power loss and efficiency data of the four converters are also recorded in Table 6.5 where a fuller breakdown of the conduction and switching losses of Converter 4 is given, split between the large (2.9 kV) and small (1.1 kV) SMs.

The conduction loss of each half-bridge SM across all converters is approximately 1.1 kW (varying little by SM voltage because the forward voltage drop of the IGBTs varied little) but the full-bridge (small) SMs Converter 4 have roughly double the conduction loss per SM because there are twice as many IGBTs in the conduction path.

The switching loss of the 2.9 kV SMs within Converter 4 have been reduced by around 90 % compared to the switching loss seen in Converter 1 because they are not called on to switch often because the 1.1 kV SMs take the burden of frequent switching. The 1.1 kV SMs in Converter 4 generate slightly more switching loss than the 1.1 kV SMs in Converter 3 despite there being fewer of them. This is explained by the facts that the two 1.1 kV SMs in Converter 4 have to carry the full burden of the PWM required to achieve the target THD, whereas this is spread among several SMs in Converter 3 and overall there will be a broadly similar number of switching events but that the two small SMs in converter 4 are full- not half-bridge SMs so there are more devices capable of being switched.

Table 6.5: Power loss and efficiency of the conventional MMCs (case-study designs from Chapter 5) and the proposed mixed-SM-voltage MMC. None of the converters contain redundant SMs.

	Converter 1	Converter 2	Converter 3	Converter 4	
Nominal SM Voltage	2.9 kV	2.1 kV	1.1 kV	2.9 kV	1.1 kV
Number of SMs per Arm	9 (HB)	12 (HB)	23 (HB)	8 (HB)	2 (FB)
Total Harmonic Distortion	0.35 %	0.35 %	0.35 %	0.35 %	
Conduction Loss per Arm	10.10 kW	14.92 kW	25.07 kW	8.97 kW	4.09 kW
Switching Loss per Arm	49.66 kW	14.06 kW	2.53 kW	5.12 kW	3.24 kW
Total Power Loss	358.56 kW	173.88 kW	165.60 kW	128.52 kW	
Efficiency	98.80 %	99.42 %	99.45 %	99.57 %	

The results presented here have proved that the concept of increasing the efficiency of an MMC by using a mix of SM voltages within each arm. Overall, there is a notable increase in efficiency for the proposed mixed-SM-voltage MMC when compared to conventional MMCs, at least for MV use.

6.7 Redundancy Design for a Mixed-SM-Voltage MMC

The provision of redundant SMs in MMCs has been shown to be effective in achieving high levels of availability through allowing continuity of operation in the event of a small number of SM failures. In Chapter 5, a comparison was made between periodic preventive maintenance and reactive maintenance for MV MMCs. It was concluded that reactive maintenance led to fewer redundant SMs being required (for a given level of availability) and therefore a useful improvement in power losses was possible compared to periodic preventative maintenance. It was also found that reactive maintenance had comparable maintenance interventions, which makes reactive maintenance attractive bearing in mind also that MV equipment is expected to be more readily accessible for maintenance than HV equipment and so short-notice maintenance interventions are plausible.

With those conclusions in mind for conventional MMCs, an investigation is now reported of the redundancy required for the mixed-SM-voltage MMC to achieve a given availability. Consideration will be given to constant-random and wear-out failures. The case-study converter outlined within Table 6.2 is studied for a service life of 40 years.

With two different SMs in each arm, consideration is needed of how many redundant SMs of each type are required because they perform different roles and cannot readily be substituted for each other. A redundant small SM is unable to contribute sufficiently to supporting the DC-bus in the event of the failure of a large SM. Similarly, a redundant large SM would be unable to maintain the required THD without incurring high switching loss in the event of a small SM failure and in fact may not be able to function adequately given it is half-bridge,

not full-bridge. The principle adopted here is that the converter should be able to achieve the same performance targets (voltage rating, THD and efficiency) when using its redundancy to overcome a SM failure up to the maximum number of failures for which redundancy was provided.

The unavailability of a SM is represented using the Weibull distribution, Equation 6.5, where *q(t)* is the unavailability of a SM at a given time, λ is the failure rate expressed in days and β is the shape parameter for modelling wear-out failures. As was the case in previous chapters (following the conclusions drawn in Chapter 4), the shape parameter was chosen as $\beta = 5$ such that wear-out becomes significant after 15 years.

$$q(t) = 1 - e^{-(\lambda t)^{\beta}} \tag{6.5}$$

The failure rate, λ, is assessed separately for each type of SM type using Equation 6.3 and Equation 6.4 and then unavailability values, $q(t)_{HB}$ and $q(t)_{FB}$ are calculated for the two different SMs from Equation 6.5.

As for the conventional MMC, a Monte Carlo simulation based on a Markov chain was used to calculate the availability of a converter arm. The Markov Chain used was based on that in Chapter 5 for reactive maintenance and is illustrated in Figure 6.11. The same mean time to repair a failed SM of 5 days was used.

The Markov Chain has separate representation of the large half-bridge and small full-bridge SMs, with a failure in either SM triggering a maintenance intervention. If further SMs fail while waiting to effect a repair (i.e., during the 5 day MTTR period) then all of those failed SMs are replaced at the upcoming maintenance intervention. If the number of failed SMs accumulated during that MTTR exceeds the number of redundant SMs for either the large or small SM type, then the converter as a whole is declared to have failed and becomes unavailable.

Time-domain simulations with a time-step of one day were run over the expected 40 year lifetime of the equipment. Results were generated for a population 10,000 converters in order

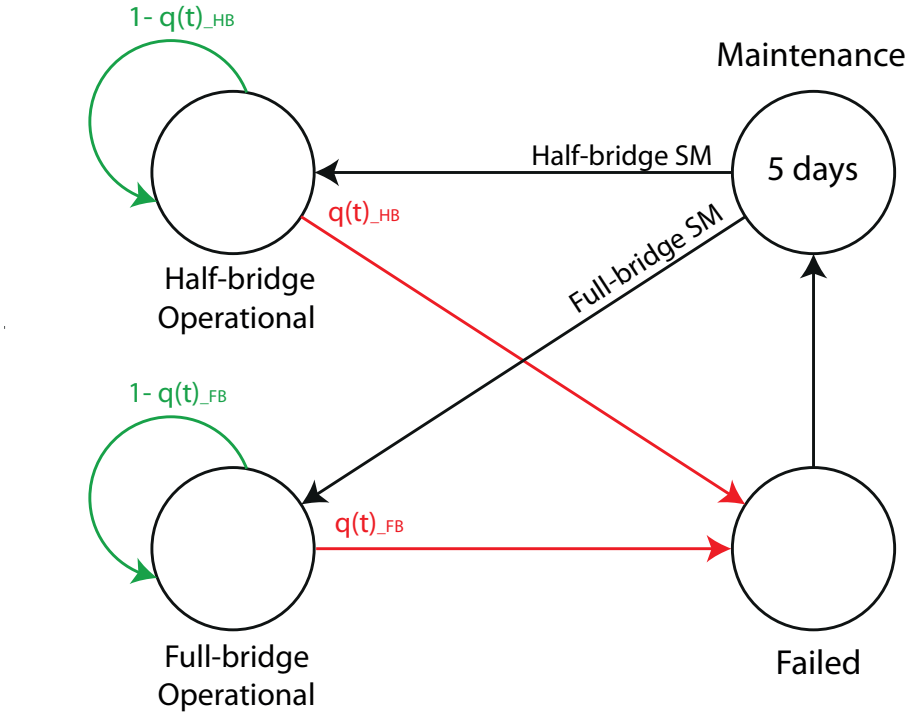


Figure 6.11: The Markov Chain for a mixed-SM-voltage MMC that was used to simulate failure occurrences (including constant-random and wear-out failures) under a reactive maintenance regime. The MTTR was set at 5 days and $q(t)_{HB}$ and $q(t)_{FB}$ represents the unavailability of a half-bridge (large) and full-bridge (small) SMs respectively.

to estimate average availability and other statistical properties. The validation of this choice of population size is discussed in Appendix A.

Simulations were performed on Converter 4 for which the base case (no redundancy) is 8 large SMs and 2 small SMs per arm. Redundancy of one SM of each type and then two of each type was evaluated. The results are shown in Figure 6.12 alongside those of Converter 1, Converter 2 and Converter 3, repeated from Figure 5.3. The results are also recorded in Table 6.6 for ease of reference to numerical values.

Sub-figure (a) shows the average number of maintenance instances for a converter arm required over the 40 year lifetime of the converter. The mixed-SM-voltage converter is seen to have a maintenance burden similar to that of Converter 2 which employed 12 half-bridge SMs

of slightly smaller size than the large SM of Converter 4 which has 8 large and 2 small SMs (SM numbers quoted here are for the base-case of zero redundancy). Bearing in mind that the small SMs of Converter 4 are full-bridge, these two converters have roughly similar numbers of major components: IGBTs and SM capacitors and therefore similar maintenance instances would be expected. Converter 4 requires only slightly more maintenance than Converter 1 with 9 large SMs.

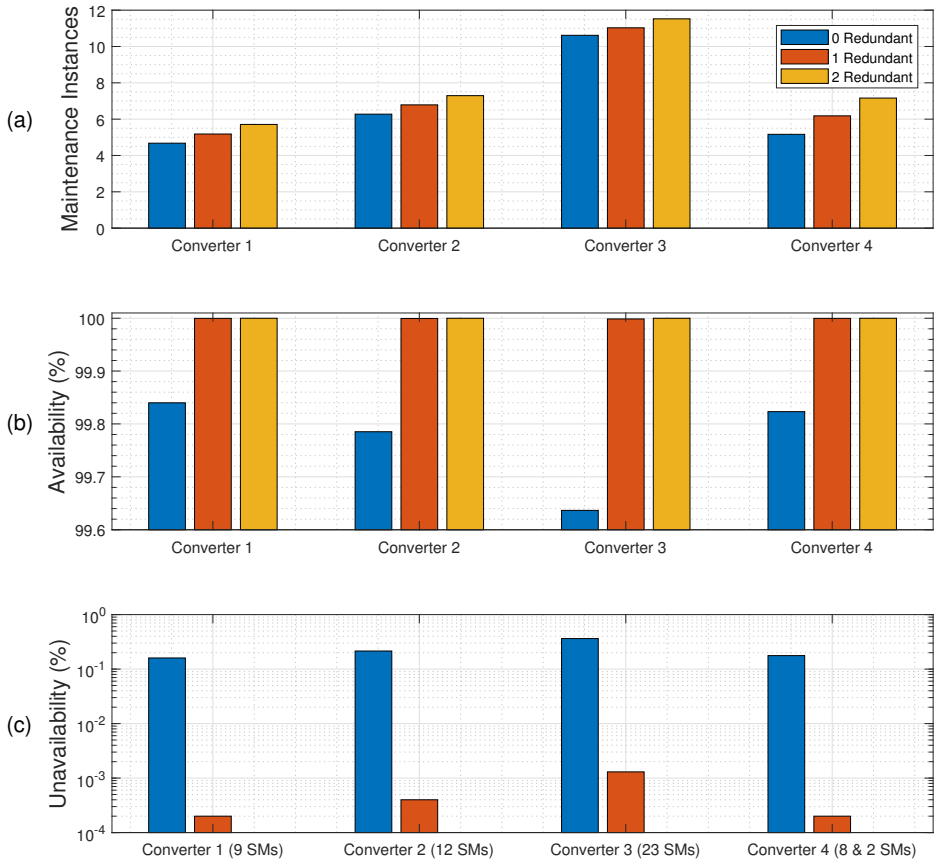


Figure 6.12: Comparison of reliability of a mixed-SM-voltage MMC (Conveter 4) with three conventional MMCs from Chapter 5: a) number of maintenance instances over 40 years of operation for a converter arm, b) availability of a converter arm with MTTR = 5 days, and c) the corresponding unavailability.

The number of maintenance interventions grows with increasing redundancy for all converters because with more SMs present, more maintenance is needed, but the growth is greater for Converter 4 because redundant SMs of both types are provided (i.e., redundancy of 1 means adding one small and one large SM for Converter 4).

Sub-figure (b) shows the availability of a converter arm and sub-figure (c) uses log-linear scale to show the corresponding unavailability which is perhaps more revealing. Redundancy of one (one additional SM or one pair of small and large SM) is seen to be sufficient to achieve the target availability of > 99.99 % in all cases, but for Converter 4 that means a greater component-count, cost and space.

Sub-figure (c) shows the unavailability of the converters on a logarithmic vertical axis to highlight the differences between them. Note that there are no entries for a redundancy of 2 (no yellow bars) because even over a population of 10,000 no complete converter failures were recorded for any of the converters. This would have required two SM failures in an arm to follow within the the 5 day MTTR of a first failure in that arm and clearly this is a very unlikely event.

Considering the data for redundancy of 0 and 1, Converter 4 is seen to have the second lowest unavailability, be the second most available, after Converter 1 and be slightly more

Table 6.6: Availability and maintenance instances of a converter arm (under reactive maintenance) for the three conventional MMCs from Chapter 5 and the proposed mixed-SM-voltage MMC.

		Redundant Sub-modules		
		0	1	2
Converter 1 (9 SMs per arm base-case)	Average Maintenance Instances	4.68	5.18	5.71
	Availability	99.8399 %	99.9998 %	100 %
Converter 2 (12 SMs per arm base-case)	Average Maintenance Instances	6.28	6.79	7.29
	Availability	99.7852 %	99.9996 %	100 %
Converter 3 (23 SMs per arm base-case)	Average Maintenance Instances	10.62	11.03	11.52
	Availability	99.6366 %	99.9987 %	100 %
Converter 4 (8 large & 2 small SMs per arm base-case)	Average Maintenance Instances	5.16	6.18	7.16
	Availability	99.8232 %	99.9998 %	100 %

available than Converter 2. Converter 4 has more SMs than Converter 1 (for base case and with redundancy) and fewer SMs than Converter 2, albeit that some of them are full-bridge and that redundancy is needed in both small and large types.

6.8 Power-loss Analysis of Mixed-SM-Voltage MMC with Redundant Sub-modules

As discussed in the previous sections and Chapter 5, the provision of redundant SMs has an impact on the power loss and efficiency of an MMC, specifically, adding redundant SMs to an arm raises the conduction power loss simply because there are IGBTs in the current path. The mixed-SM-voltage MMC requires two redundant SMs each time an availability increase is sought, one large full-bride SM and one small half-bridge SM, and therefore a greater increase in conduction loss is expected compared to conventional MMCs. The impact on power losses of redundancy in a mixed-SM-voltage MMC will now be examined in detail. Results will be compared with the three case-study conventional MMCs from Chapter 5. Following the procedure already established, a discrete-time Matlab-Simulink simulation was used to calculate power loss for various redundancy provisions. Results are shown in Figure 6.13.

The conduction power loss, shown in sub-figure (a) increases with redundancy for all converter cases because of the presence of more IGBTs in the conduction path. The increase is seen to be steeper for Converter 4 because one additional SM of each types is added at each step and the small SM is also full-bridge. In contrast, the switching loss (sub-figure (b)) remains approximately constant as redundancy is increased for all converters because the number of commutation events is largely unaffected by the presence of redundant SMs. Sub-figure (d) reveals Converter 4 (the mixed-SM-voltage MMC) as having the highest efficiency of the four converters, as might be anticipated from the results with no redundancy shown previously in Figure 6.10, but as redundancy is increased the advantage narrows because of the need for two types of redundant SM. The results in Section 6.7 showed that one redundant SM (of each

type for Converter 4) is sufficient to achieve an expected arm availability > 99.99 % with a MTTR = 5 days for all the converters. Examining Figure 6.13 for the case of redundancy of one shows Converter 4 still has a substantial advantage in efficiency over the other three converters. For easier consideration of the numerical values, the power-loss results for the case on one redundant SM are also recorded in Table 6.7 which confirms that Converter 4 has the lowest power loss. These results can be compared to those in Table 6.5 which was for zero

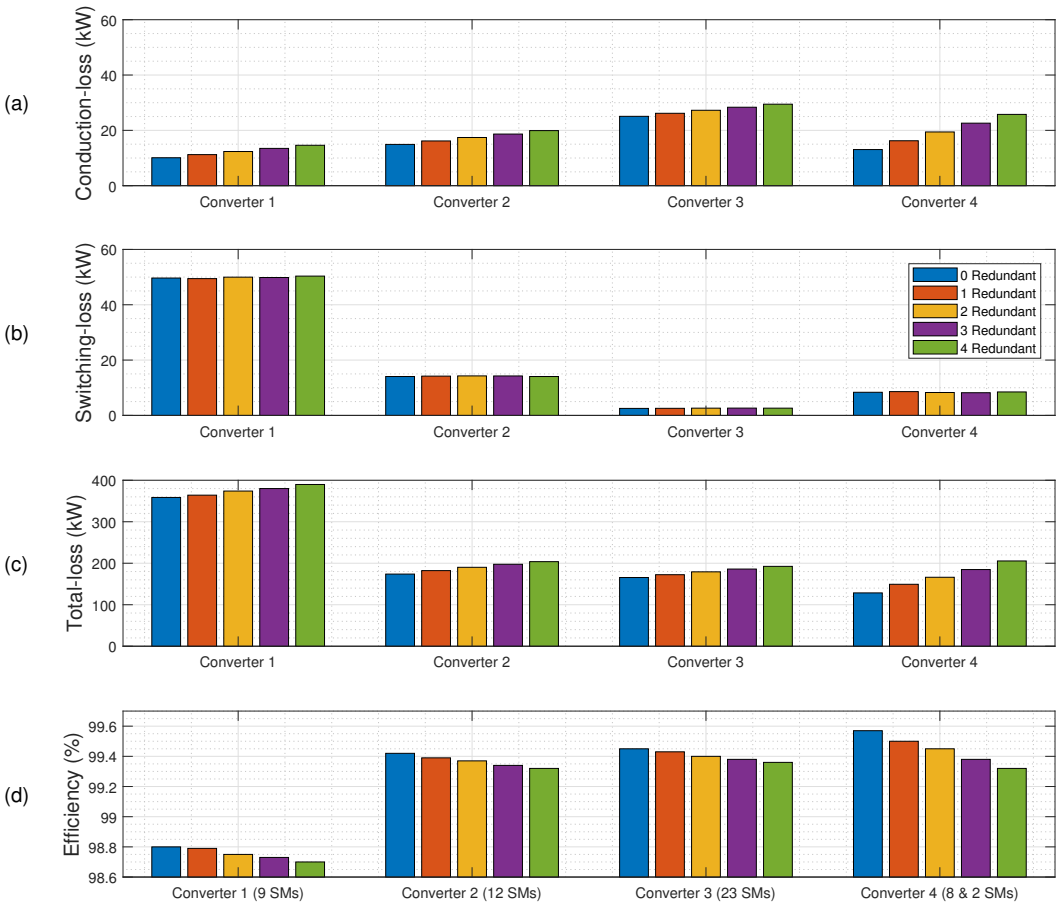


Figure 6.13: Comparison of power loss and efficiency of Converters 1 to 4 showing: a) conduction power loss of an arm, b) switching power loss of an arm, c) total power loss and d) efficiency.

Table 6.7: Power loss and efficiency of the four case-study converters with one redundant SM (one of each type for Converter 4).

	Converter 1	Converter 2	Converter 3	Converter 4	
Nominal SM Voltage	2.9 kV	2.1 kV	1.1 kV	2.9 kV	1.1 kV
Minimum Number of SMs per Arm	9 (HB)	12 (HB)	23 (HB)	8 (HB)	2 (FB)
Number of Redundant SMs per Arm	1	1	1	1	1
Total Harmonic Distortion	0.35 %	0.35 %	0.35 %	0.35 %	
Conduction Loss per Arm	11.23 kW	16.17 kW	26.17 kW	10.10 kW	6.14 kW
Switching Loss per Arm	49.45 kW	14.20 kW	2.56 kW	5.26 kW	3.34 kW
Total Power Loss	364.08 kW	182.22 kW	172.38 kW	149.04 kW	
Efficiency	98.79 %	99.39 %	99.43 %	99.50 %	
Efficiency penalty of 1 Redundant SM	0.01 %	0.03 %	0.02 %	0.07 %	

redundant SMs. The final row of Table 6.7 records the decrease in efficiency incurred adding redundancy of one (one extra SM or SM pair). For the case of the mixed-SM-voltage MMC, the total power loss increases from 128.5 kW to 149.0 kW and efficiency decreases from 99.57% to 99.50% with the one extra SM pair needed for > 99.99 % availability.

6.9 Conclusions on the Mixed-SM-Voltage MMC

In this chapter, a proposed variant of the MMC for MV applications has been investigated. It combines SMs of two different voltage ratings in each arm to overcome the trade-off in SM number that was explored in Chapter 5. That trade-off favours low numbers of large SMs for conduction power loss reduction but high numbers of small SMs for waveform quality improvement. The proposal was for each arm of the MMC to employ SMs with two different voltage ratings. For the case study, a SM voltage rating of 2.9 kV was used for large SMs which are efficient for bulk power processing and many of those are employed. They were supplemented by two small SMs of 1.1 kV which are better able to support fast switching and aid waveform quality. For a 30 MW converter and a $\pm$ 12.5 kV DC-bus, only eight large and two small SMs were required. Despite the relatively small number of SMs (very small compared to HVDC cases), a THD less than 0.35 % was achieved through applying PWM to the small SMs while allowing the large SMs to follow a simple stepped waveform. The resultant efficiency was 99.57 % (for a case with no redundant SMs). This represents a substantial power loss saving over an MMC of solely 2.9 kV SM (98.80 % efficient) and a useful improvement over the case of solely 1.1 kV SM (99.45 % efficient).

Simulation and experimental results have been used to verify a new modulation and voltage balancing algorithm that deploys the two types of SM and maintains the SM voltages within a given band around their nominal values. It was found that the intense use of the small (1.1 kV) SMs required them to be full-bridge in order to give greater flexibility in use and therefore sufficient opportunities to perform energy balancing.

The availability of the mixed-SM-voltage MMC case was investigated for the addition of pairs of redundant SMs (one each of the large and small types). It was shown that for reactive maintenance with a MTTR = 5 days, the addition of only one pair of SMs in each arm achieved an expected arm availability $>$ 99.99 %. After adding redundant SMs, the mixed-SM-voltage MMC is still more efficient than the conventional MMCs designed for the same availability and

operating conditions (those described in Chapter 5). The reduction in efficiency of the mixed-SM-voltage MMC when adding the one pair of redundant SMs needed for > 99.99 % availability is from 99.57 % to 99.50 %.

7 Conclusions

This thesis has addressed the question of how best to arrange redundancy in an MMC, in combination with a choice of maintenance regime, to achieve high availability, taken here to mean availability of greater than 99.99 % for a converter arm. This was considered for both HVDC and MVDC uses of MMCs. The failure rates of IGBT modules, capacitors and control electronics within SMs were the main concern. A discrete-time Monte Carlo simulation of failures of SMs within MMC arms was developed based on Markov Chains. The simulation was verified against analytical findings for simple cases where analysis is tractable. The simulation studies showed that constant-random and wear-out failures are both important factors to consider when evaluating the total number of redundant SMs required within an arm of an MMC.

Periodic preventive maintenance is the industry norm for HVDC applications. Under this regime, large gains in availability can be achieved by increasing the number of redundant SMs by a relatively small amount and so the impact on cost and power losses is small but the gain in avoidance of outage penalties is large. The maintenance intervals can be extended, which is advantageous for HVDC applications to reduce operational costs, by increasing the number of redundant SMs and it was found that number needed increases at less than a linear rate. For instance, under a 5-year maintenance interval, 35 redundant SMs (11.4 % redundancy) achieves 90 % availability but only half as many again (51 redundant SMs or 16.7 % redundancy) achieves 99.99 % availability: a decrease in unavailability of 3 orders of magnitude.

Turning to the case of MVDC, the number of SMs needed within an arm of an MMC to support the voltage is proportionately smaller than at HVDC but the number of redundant

SMs, for the target availability, does not decrease at the same rate with the result that the redundant SMs represent a larger fraction of the total. When power loss and efficiency are evaluated through circuit simulation, relatively high conduction losses are observed because of the relatively large number of SMs in the conduction path of each arm arising from the redundancy provision. In order to improve efficiency at MVDC, it was proposed to change from preventative maintenance to reactive maintenance. Reactive maintenance is feasible in MV distribution because access is more readily available at short notice than in HV transmission (especially for offshore transmission). It was confirmed that reactive maintenance requires only a small number of redundant SMs within each arm sufficient only to sustain operation after a SM failure (or small number of failures) until reactive maintenance has been completed. Further, the Monte Carlo simulation results show similar maintenance interventions are required compared to periodic preventive maintenance for a comparable availability of > 99.99 % for a converter arm.

In investigating use of MMC at MVDC and designing converters to a common waveform quality (judged through total harmonic distortion) it was apparent that the choice of SM voltage is a difficult trade-off between waveform quality, conduction power loss and switching power loss. An MMC designed around IGBTs of relatively high blocking voltage would have a small number of SMs and a low conduction loss because of the small number of IGBTs and their good conduction properties, but high switching loss because of the poorer switching properties of the IGBTs and the need for frequent switching to maintain good THD. On the other hand, an MMC designed around IGBTs of relatively low blocking voltage would have a larger number of SMs and a high conduction loss because of more IGBTs, but a low switching loss because of better switching properties of those IGBTS and the less frequent switching needed to maintain good THD when there are a large number of small voltage steps available.

To combine the advantages of different voltage rating IGBTs in the case of MVDC, an MMC was proposed with mixed-SM-voltages in each arm. The intention was that the majority of the required arm voltage is generated from higher voltage half-bridge SMs which have good

conduction properties and that a small number of lower voltage full-bridge SMs with good switching properties are used to refine the arm voltage. A control algorithm was devised that selected the appropriate combinations of high and low voltage SMs to create the correct overall voltage at each instance and ensure voltage balance of all SM capacitors. It was found that full-bridges are required for the lower voltage SMs in order to provide sufficient opportunities to balance the capacitor voltages regardless of direction of current flow. Through circuit simulation, power loss and efficiency of the mixed-SM-voltage MMC were confirmed to be better than conventional MMCs of same power rating and THD. This was attributed to the relatively high number of available voltage levels for the number of SMs present which allows infrequent switching of high voltage SMs, which form the majority of the arm. Various combinations of high and low voltage SMs were investigated and insights developed into how a design can be optimised. To achieve an arm availability of > 99.99 %, redundant SMs of both low voltage full-bridge and high voltage half-bridge are required. The control and operation of the mixed-SM-voltage MMC was validated through experimental testing of a lab-scale prototype.

7.1 Further Work

The mixed-SM-voltage MMC is more efficient than conventional MMCs of the same power rating for comparable THD at MV, but the economic value of increased efficiency was not determined. A cost-benefit analysis of the increased efficiency could be conducted by evaluating how much energy could be saved over the converter's life if operated at rated power throughout or at some load factor.

To maintain an availability > 99.99 %, redundant SMs of both low voltage full-bridge and high voltage half-bridge are required within the mixed-SM-voltage MMC, which is greater than the number of redundant SMs required within conventional MMCs where reactive maintenance is performed. It may be beneficial to have one type of redundant SM within a converter arm and for that to be a large half-bridge SM. In the event of a failure of a large HV half-bridge

SM, the redundant module is available to take up the role. In the event of a failure of a smaller low voltage full-bridge SM, a high voltage half-bridge SM would need to undertake increased switching (PWM) to maintain waveform quality until reactive maintenance can be performed and this would result in higher power loss for that period. The additional lost energy might be tolerable from an economic perspective but might well raise challenges in thermal management of the SM.

An advantage of modular converters at MVDC is the reduced filter requirement and therefore reduced physical volume to accommodate the filter. The mixed-SM-voltage MMC has a mixture of full- and half-bridge SMs and high and low voltage IGBT modules which differ in size. Further work would be to quantify the footprint of the mixed-SM-voltage MMC and compare against conventional MMCs of comparable THD waveform quality.

The mixed-SM-voltage MMC considered the use of two different voltage levels within each arm which was proven to be an efficient design choice when compared to conventional MMCs, but it may be advantageous to use even more voltage levels within each arm to generate even more voltage levels, reducing the average switching frequency and potentially increasing the efficiency of the mixed-SM-voltage MMC further, using a small number of lower voltage rated SMs to achieve the voltage levels.

There are also further SM topologies which have not been investigated within this thesis, which will have different failure rates and opportunities within the mixed-SM-voltage MMC.

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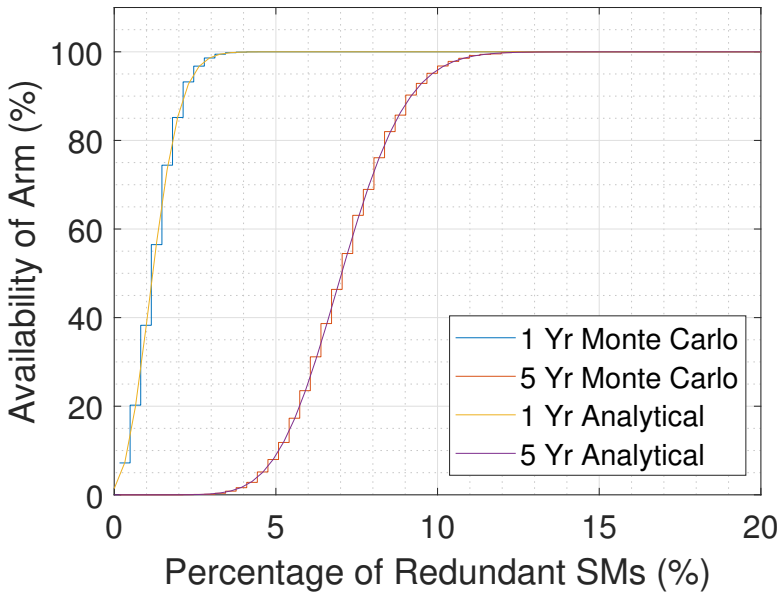
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Appendix

Appendix A

To prove the Markov chain Monte Carlo method outlined in Chapter 4 and the simulation population size of 10,000 iterations within the Monte Carlo simulation, the figure below shows the availability of the *k-out-of-n* model for the HVDC case-study converter outlined in Table 4.1 for constant random failures. The graph shows the number of redundant SMs required for 1 and 5 yearly maintenance intervals, with the Monte Carlo results shown as stepped increases



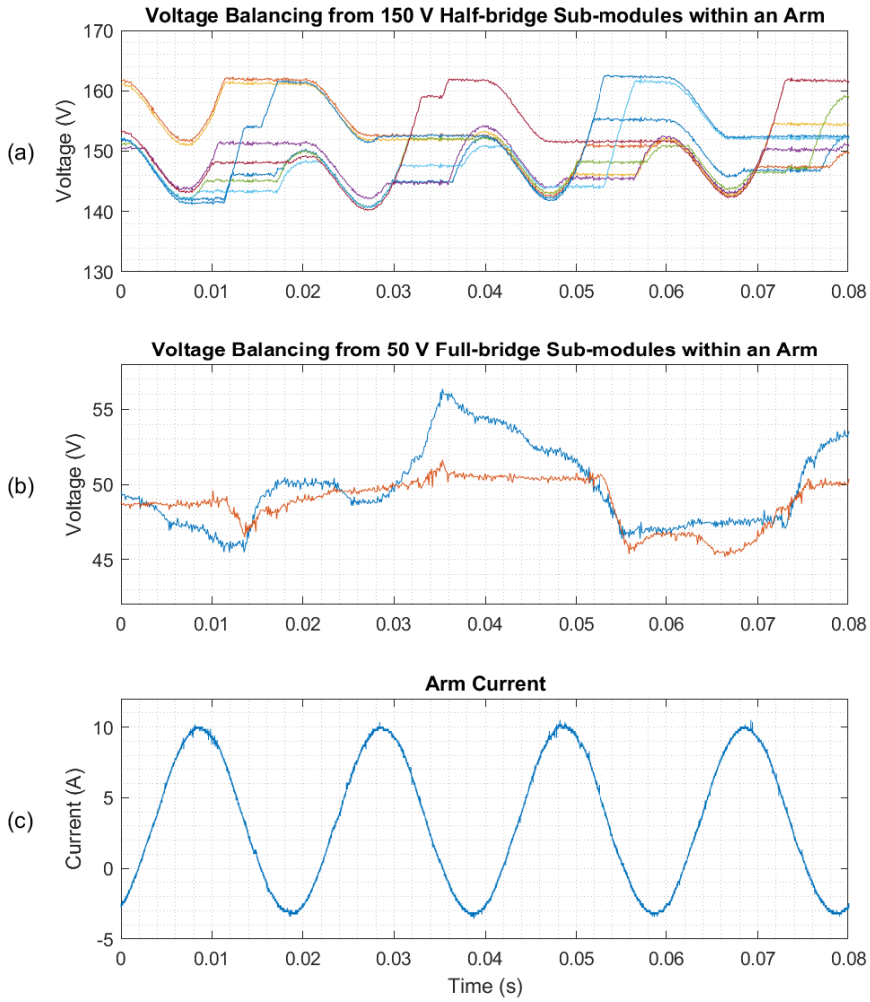
Arm availability of an MMC for constant random failures, proving analytical and Monte Carlo results are the same for 1 year and 5 year periodic maintenance intervals.

for the same converter specification used for the analytical method.

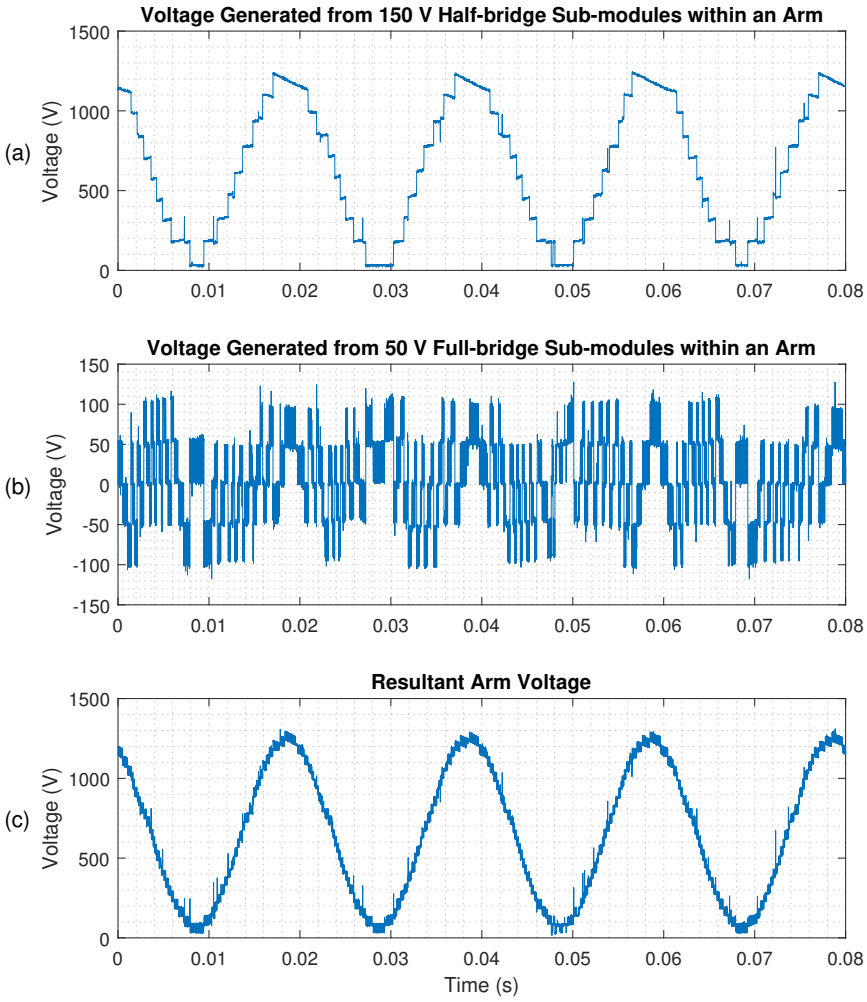
The Markov chain Monte Carlo simulation assumes $\beta = 1$ within the Weibull distribution, which simplifies the Weibull distribution to the negative exponential, which is the same equation used to model unavailability of a SM for constant random failures within the *k-out-of-n* model.

This proves the Markov chain Monte Carlo Simulation is a good representation of the analytical results produced from the *k-out-of-n* model for constant random failures.

Appendix B



Hardware results for mixed-SM-voltage MMC showing: a) half-bridge SM voltages, b) full-bridge SM voltages and c) arm current



Hardware results for mixed-SM-voltage MMC showing: a) arm voltages of 150 V SMs, b) arm voltages of 50 V SMs and c) resultant arm voltage