

An Auto-Offset-Removal circuit for chemical sensing based on the PG-ISFET

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Abstract—This paper presents a novel readout circuit for a pH sensitive Programmable-Gate Ion-Sensitive Field Effect Transistor (PG-ISFET) to overcome bias issues due to threshold voltage variation and increase output-referred sensitivity. Compared to other commonly-used ISFET readouts, this circuit uses two extra programmable nodes which are driven by a feedback configuration. Using the device in a source follower configuration, one node is used to evaluate and cancel the offset of the intrinsic device while the other tracks and amplifies changes in pH. A sample and hold protocol has been developed to minimize the leakage effects and improve the pH sensing range. The system has been designed and fabricated in AMS 0.35 μ m, to compensate for a threshold voltage variation of $\pm 10.5V$ and provide a pH sensitivity of 200mV/pH.

I. INTRODUCTION

Since its introduction in the 1970s, the Ion-Sensitive Field Effect Transistor (ISFET) [1], has been adopted within several chemical and biomedical applications [2]–[4]. Conventionally, the ISFET is regarded as a MOSFET device with the polysilicon gate replaced by a sensing membrane. Depending on the membrane, it can be used to detect various analytes such as hydrogen, sodium and potassium. Originally, the ISFET had been established as a pH sensor due to silicon dioxide which was used as the initial membrane. Since then however, numerous efforts have been made to realize ISFETs in a CMOS-compatible technology, which is passivated with silicon nitride that is also pH sensitive [2]. This has the added advantage of the low cost of production and potential for monolithic integration with other circuits.

However, CMOS ISFETs suffer from many non-idealities, in particular threshold voltage variation and drift [1], which reduce the measurement accuracy. So far, few efforts have proved effective enough to minimize these. In [5], UV radiation had been used to correct/adjust the threshold voltage from 10V to 5V. In [6], an exponential drift model had been proposed based on the dispersive transport to cancel out drift. However, the detailed mechanisms of offset and drift still remain unclear. Additionally, the read-out interface circuits for the ISFET must also be designed to reduce noise in pH measurement. There are two general configurations, the source drain follower [7], and the gate readout [8]. Current research on these has focused on cancelling various nonlinear effects mentioned but also reducing the power consumption and hardware complexity [4]. In [9], a simple Programmable Gate ISFET (PG-ISFET) was proposed which utilises a pro-

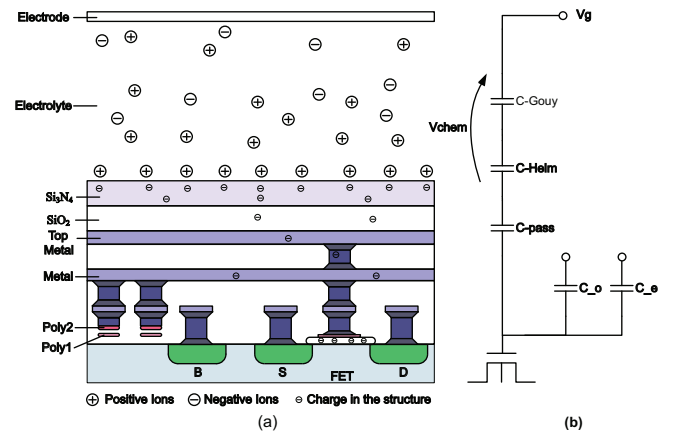


Fig. 1. (a) is the structure of CMOS-based device, (b) is the schematic of this device

grammable gate to adjust the devices threshold voltage without the need for any additional post-fabrication processes.

In this paper, we propose a novel readout based on a PG-ISFET shown in Fig 1, to cancel out threshold voltage variation due to trapped charge in addition to amplifying pH sensitivity. This paper is organized as follows: Section II describes the theory governing ISFET sensors as well as the schematic design of the readout. Section III describes the specific read-out protocol used to sample and readout the pH variation from the sensor. Finally, simulation results and the system fabrication are discussed in Section IV.

II. ISFET THEORY AND READOUT SCHEMATIC

Principally, an ISFET is a MOSFET, with its gate exposed to the electrolyte and the gate bias set using a reference electrode. The overall chemical potential drop through the reference electrode-electrolyte-insulator interface is thus given by [4]:

$$V_{chem} = E_{ref} - \psi_o + \psi_{lj} + \chi^{sol} - \frac{Q_{ox} + Q_{ss}}{C_{ox}} \quad (1)$$

where E_{ref} is the contribution of the reference electrode relative to vacuum; χ^{sol} is the surface dipole potential, ψ_o and ψ_{lj} are the potential drops in the insulator/electrolyte and reference electrode/electrolyte surface. Q_{ox} and Q_{ss} are the charge density in the oxide and the surface state [?]. ψ_o is

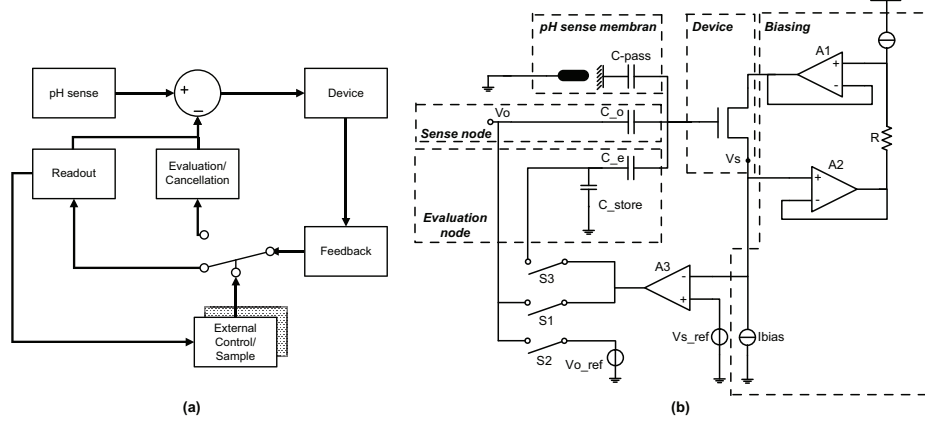


Fig. 2. (a) System structure and (b) readout schematic

the only pH dependent term and therefore the potential which needs to be monitored.

The sensing mechanism of the electrolyte-insulator interface is commonly described by a double layer model coupled to an intrinsic surface site model [3]. This double layer is commonly modelled by two capacitors in series, which describe the equilibrium of charge distribution and exchange. Likewise, the intrinsic surface site model is described by the site-binding theory, in which the exchanging and bonding of ions from the sites are in equilibrium. However, as a result of these two phenomena, the ideal sensitivity of such an interface is sub-nerstian. The sensitivity is thus given as:

$$S = \frac{\partial \psi_o}{\partial pH} = 2.3 \frac{kT}{q} \alpha \quad (2)$$

where α is a scaling down factor which represents these effects.

There has been a recent drive to implement ISFETs in commercial CMOS technologies to take advantage of a low manufacturing cost in addition to exploiting the potential of monolithic integration. This is possible due to the pH sensitivity of native passivation of CMOS dies, which is silicon nitride on silicon dioxide. Amongst various structures reported, the continuous stacked metal layer approach has been proved to be the most effective [2]. This method uses a floating metal stack to connect the the polysilicon gate of the MOSFET to the top passivation where is can sense changes in pH. However, due to the CMOS process flow, this method has been susceptible to trapped charge which results in large threshold voltage variations.

In [5], the threshold variation was shifted by UV illumination, which removed trapped charge in either the surface insulator or the floating layer. By including the effects of trapped charge we define the floating gate voltage of the CMOS ISFET as:

$$V_{FG} = \frac{C_{pass}}{C_T} (V_G - V_{chem}) + \frac{C_{GS}}{C_T} V_S + \frac{C_{GD}}{C_T} V_D + \frac{Q_{TC}}{C_T} \quad (3)$$

where Q_{TC} models the trapped charge, C_{pass} is the capacitance of passivation layer; C_{GS} / C_{GD} are the capacitors between gate and source/drain; C_T is the total capacitance of the floating gate node and V_S and V_D are the source and drain voltages of intrinsic FET device.

In [9] a PG-ISFET was shown to cancel effects of trapped charge by adding an extra capacitor to the floating gate to scale down the voltage. We can see this effect by introducing a capacitor C_e , which can couple a voltage V_e , to the floating gate node which now becomes:

$$V_{FG} = \frac{C_{pass}}{C_T} (V_G + V_{chem}) + \frac{C_{GS}}{C_T} V_S + \frac{C_{GD}}{C_T} V_D + \frac{Q_{TC}}{C_T} + \frac{C_e}{C_T} V_e \quad (4)$$

Assuming we set $Q_{TC} = V_e \cdot C_e$, the programmable gate effectively cancels out the trapped charge. For an N-type ISFET operating in the saturation region, the drain current is defined as:

$$I_D = \frac{k'}{2} \frac{W}{L} (V_{FG} - V_S - V_{th})^2 (1 + \lambda V_{DS}) \quad (5)$$

What we can see from Eq.(5) is that there are five adjustable values which can be used to track the pH changes: V_G , V_S , V_D , V_e and I_D . In one configuration we can fix I_D and V_{DS} , and track the gate voltage [8] as a voltage follower. In another, we can track the source voltage [7] by grounding the reference electrode. Grounding the reference electrode is preferred because first, the changing electrolyte and bubbles in the solution could make the feedback to gate unstable, second, accidentally grounding the electrode through electrolyte or encapsulation will cause large leakage current.

The circuit schematic of the proposed readout is shown in Fig. 2. This is a source follower based on a grounded reference. It includes an evaluation capacitor, C_e which is used to cancel out trapped charge as previously mentioned. This can also be used to bias the device in the same initial region of operation every time a measurement is required, which is stored on capacitor C_{store} .

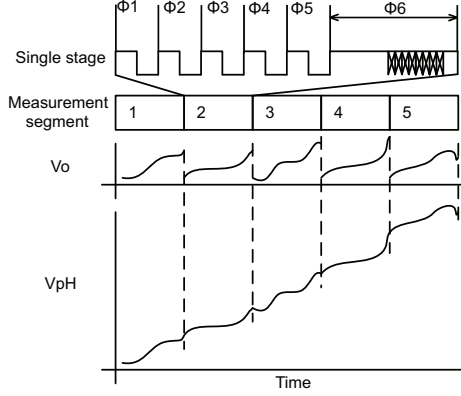


Fig. 3. A typical operation procedure including segments and phases

However, by introducing this capacitor on the floating gate node, it also scales down the voltage drop across the passivation capacitance by C_{pass}/C_T , due to the increase of the total capacitance on the floating gate node. Although V_e can be used to monitor a change V_{chem} as is seen in Eq. (4), because of this scaling it will be significantly small. Furthermore, if V_e is used to cancel the threshold voltage and sense the pH change, the pH sense dynamic range will be limited by the bias voltage required to compensate for the trapped charge.

Therefore, in order to have rail to rail operation for pH sensing, another programmable gate node consisting of the capacitor C_o , need to be introduced to behave as a sense node, Fig. 2. Using this, the feedback loop will sense the change in V_{chem} with regards to V_{S_ref} and control V_o to track a potential drop due to a pH change.

By substituting Eq. (1) into Eq. (4) and including both evaluation and sense nodes and grouping constant terms in κ , V_{FG} becomes:

$$V_{FG} = \frac{C_{pass}}{C_T} V_{chem} + \frac{C_o}{C_T} V_o + \frac{Q_{TC}}{C_T} + \frac{C_e}{C_T} V_e + \kappa \quad (6)$$

By holding V_{FG} constant using the circuit proposed, we see that any pH change is counterbalanced by the voltage V_o and any trapped charge is counterbalanced by the voltage V_e . This scheme therefore compensates and tracks at the same time. A switch controlled by external signal can choose which node should be on operation at any given time. Any change in V_{chem} will now be:

$$\Delta V_o = \frac{C_{pass}}{C_o} \Delta V_{chem} \quad (7)$$

and the pH sensitivity of the entire device becomes:

$$S = 2.3 \frac{kT}{q} \alpha \frac{C_{pass}}{C_o} . pH \quad (8)$$

Therefore it can be observed that, the pH sensitivity is scaled by α and the capacitor ratio. However, by changing the capacitor value of sense node, we can amplify the output voltage due to pH.

TABLE I
DESIGN TARGET SPECIFICATION

Term	Values
Technology	AMS 0.35 μm CMOS 2 Polys and 4 metals
Supply voltage	3.3V
Cell size	600 $\mu m \times$ 500 μm
Storage capacitor	1pF
Sense area	30 $\mu m \times$ 100 μm
V_t handle range	± 10.5 V
External clock frequency	200 KHz
Biasing current	100 μA
Resistor	5 K Ω

III. OPERATION AND CIRCUIT IMPLEMENTATION

The ISFET is biased by fixing the drain current, and source voltage which is defined by I_{bias} and V_{sref} , with a fixed V_{DS} set by the resistor R and the feedback of opamps A1 and A2. As described, in this mode the floating gate voltage V_{FG} will always be fixed to maintain, I_{bias} through the feedback loop using opamp A3. This feedback loop can connect to either V_e or V_o and be used to sense the offset before an ISFET measurement but also measure the pH change during an experiment. Thus, the measurement consists of two phases, the evaluation phase and the sensing phase.

During normal operation it is required that the output voltage, V_o is mid-rail to ensure the maximum dynamic range for fluctuations in pH. Furthermore, a storage capacitor, C_{store} has been added to prevent discharge of node, V_e , which would change the biasing of the sensor. The circuit operation is thus as follows which can be seen in Fig. 3:

Φ1: Switches S1, S2 and S3 are all turned off. Φ2: S2 turns on, connecting V_o to mid-supply to set the sensing node initial operating point. Φ3: S3 turns on, connecting the evaluation node, V_e to the feedback loop to cancel out any trapped charge but also establish a voltage which will keep V_o at mid-supply when sensing. Φ4: S3 turns off, with the programmed voltage stored on C_{store} . Φ5: S2 turns off allowing V_o to temporarily float. Φ6: S1 turns on, connecting V_o to the feedback loop which now tracks and amplifies any changes in pH.

Each measurement is executed using a sequence of segments, in which the above phases are included. By doing so we ensure that any switch leakage is minimized to reduce source of error. Also by segmenting the measurement in this way we always ensure that the output voltage is reset to mid rail, thus allowing the maximum dynamic range for sensing during a single segment. This is advantageous for sensing application where a change in pH is more significant than absolute value. The absolute pH change however can be reconstructed by summing the voltages at Φ6 for every segment.

As we can see in Fig. 3, the measurement phase, Φ6 needs to be longer than the previous phases so that an accurate measurement can be acquired. This is possible as we can switch in phases 1-5 extremely quickly due to the slew rate of the Op-Amp used, not allowing any time for discharge along with the fact that the discharge time constant is extremely large due to the switches used.

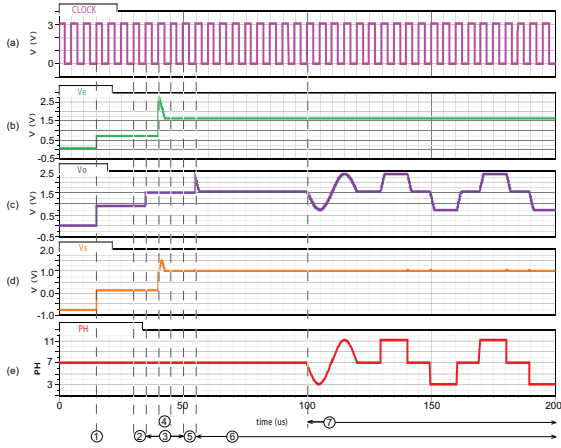


Fig. 4. pH change response: (a) clock, (b) evaluation voltage, (c) sense voltage, (d) source voltage and (e) pH change.

IV. SIMULATION AND DISCUSSION

The circuit has been designed and fabricated in AMS 0.35 μm according to the specifications shown in Table I. The circuit has been designed to compensate for offsets caused by surface trapped charge in the range of $\pm 10\text{V}$, based on results reported in [5] and observed in our own measurements and the offset caused by trapped charge in the floating gate in the range of $\pm 0.5\text{V}$.

Simulation results has been shown in Fig. 4 whereby these charges are modelled using DC voltage sources with initial values of 10V and 0.5V respectively. The ratio of C_{pass}/C_o is set to 4, which will give a pH sensitivity 200mV/pH, and the C_e is set to 1pF, in order to compensate throughout the entire offset range whilst also reduce errors due to leakage. The ISFET pH sensitivity is modeled using a voltage source to represent V_{chem} which is based on silicon nitride or silicon dioxide with a maximum sensitivity of 50mV/pH [2]. We use a test waveform, which combines a single sinusoidal period (with 200mV amplitude and 20 μs period), with a series of voltage steps from -200mV to 0V then to 200mV. This represents a pH change stimulus of a sinusoid change (with 4pH amplitude and 20 μs period) and a series of pH steps from 7 to 3 then to 11, each pH change lasting 10 μs .

Initially, the source voltage will be driven low to keep the transistor in operation; In Fig. 4, point (1), the offset voltage is applied to model a change due to trapped charge. In Fig. 4 period (2), we initialize all the nodes as in $\Phi 1$; In (3), V_o is set to a reference value 1.5V as in $\Phi 2$. In (4), V_e was raised to 1.6V to compensate the offset as in $\Phi 3$ and stored as in $\Phi 4$; In 5, we disconnect both nodes as in $\Phi 5$, no voltage changed; In (6) the sense node was activated and the measurement begins as in $\Phi 6$; In (7) a pH change is simulated, which is tracked and amplified by a factor of 4 at V_o .

The full layout of the system is shown in Fig. 5 with an overlaid floorplan clearly indentifying each block.

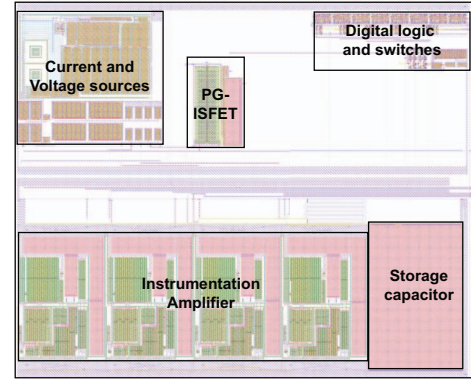


Fig. 5. Circuit layout measuring 600 $\mu\text{m} \times 500\mu\text{m}$ in AMS 0.35 μm CMOS

V. CONCLUSION

This paper has presented a novel solution to a timely challenge in CMOS ISFET sensor interface. An ISFET device with two external capacitively coupled terminals has been developed to minimize the effects of trapped charge found in ISFETs fabricated in commercial CMOS. By using feedback and a specific readout protocol, the circuit can provide compensation for threshold voltage and also amplification of the pH sensitivity. Fabricated in AMS 0.35 μm , the circuit has great potential for making monolithic CMOS based chemical sensing systems.

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