

SEM-EBIC INSPECTION OF VLSI CIRCUITS USING IMAGE PROCESSING

by Jeremy Duncan Russell, M.A., M.Sc.

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Department of Materials
Imperial College of Science, Technology and Medicine
London SW7 2BP

ABSTRACT

The effects of irradiation by the electron beam have been studied in detail on MOS test-transistors, and consist of a shift in threshold voltage, ΔV_t , a decrease in channel mobility, and increased leakage currents. ΔV_t was separated into shifts due to interface and oxide trapped charge. For low doses the variation of ΔV_t with charge dose is linear, and the variation of this damage rate with the beam energy, E_b , has two regimes. At high E_b electrons penetrate the gate oxide, and damage was accounted for by the Everhart-Hoff model and Monte Carlo simulations. At low, non-penetrating E_b , X-rays (Bremsstrahlung) were responsible. Non-destructive EBIC was demonstrated by limiting the radiation dose, using an image processor. Image processing has been shown to efficiently locate defects in VLSI circuits. Both comparisons of good/bad circuits and Fourier transform spatial filtering were useful techniques. For the latter, a fully automatic method was developed, based on thresholding the power spectrum to generate a spatial frequency mask. It acted robustly on a wide range of images. Software for computer controlled "step and repeat" inspection of VLSI circuits was also established. Defects were indexed to co-ordinates of reference points on the chip. This co-ordinate system also allowed convenient coarse positioning for comparing good-bad circuits. Electrostatic discharge (ESD) in chip input circuitry was located using EBIC and comparison techniques. During investigation of such defects, EBIC contrast was observed due to three mechanisms: pn-junction burnout, electrothermomigration of aluminium, and reduced minority carrier lifetime. A computer program was written to acquire quantitative EBIC linescans for analysis. Deconvolution of the beam spreading effect at high E_b was demonstrated, giving an increase in resolution.

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Notations and Abbreviations

Abbreviations

ADC	Analogue to Digital Converter
ASIC	Application Specific Integrated Circuit
ATE	Automatic Test Equipment
CAD	Computer Aided Design
CASE	Cooperative Awards in Science and Engineering
CC	Charge Collection
CCD	Charge Coupled Device
CMOS	Complementary Metal Oxide Semiconductor
DAC	Digital to Analogue Converter
DIL	Dual In Line
DUT	Device Under Test
EBIC	Electron Beam Induced Current
EBIV	Electron Beam Induced Voltage
EBT	Electron Beam Tester/Testing
ESD	Electrostatic Discharge
FFT	Fast Fourier Transform
FFTDIS	Kontron function to display Fourier power spectrum
FFTINV	Kontron inverse FFT function
FFTMSK	Kontron function to remove spatial frequencies from the Fourier transform
GEC	General Electric Company
IBAS	Interaktives Bild-Analysen System (interactive image analysis system)
IC	Integrated Circuit
ICVM5	Induced Current, Voltage Monitor mk. 5
INTU1	Interface Unit mk. 1
JEOL	Japanese Electron-Optical Company
JSM	JEOL Scanning Microscope
M	Mega (byte) $\approx$ 1 million
MEDL	Marconi Electronic Devices Ltd.
MIL STD	Military Standard
MOS	Metal Oxide Semiconductor
MOSFET	MOS Field Effect Transistor
NMOS	N-channel Metal Oxide Semiconductor

OBIC	Optical Beam Induced Current
PCB	Printed Circuit Board
PCD	Probe Current Detector
PMOS	P-channel Metal Oxide Semiconductor
PTFE	Poly Tetra Fluoro Ethane
RAM	Random Access Memory
SE	Secondary Electron
SEM	Scanning Electron Microscope/Microscopy
SMU	Source Measuring Unit
SOMSEM	Scanning Optical Microscope in the SEM
SOS	Silicon On Sapphire
TEM	Transmission Electron Microscope
TTL	Transistor Transistor Logic
VLSI	Very Large Scale Integrated/Integration
VC	Voltage Contrast
ZIF	Zero Insertion Force

Notations

A	(i) area (ii) constant in mobility relationship
A_1	scanned area at $\times 1$ – calibration factor
b	MOSFET channel depth
B	(i) convolution matrix (ii) constant in mobility relationship
C_{ox}	oxide capacitance per unit area
d	junction depth
d_{CRT}	sampling distance on the SEM CRT
d_o	oxide thickness above substrate
d_{spec}	sampling distance on the specimen
d_r	oxide thickness above diffused resistor
D	(i) minority carrier diffusion coefficient (ii) electron beam dose
D_1	Distance per pixel at $\times 1$ – calibration factor
E	energy
E_b	beam energy
E_c	Long-wavelength cut-off of the Bremsstrahlung
E_C	conduction band energy

E_F	Fermi energy
E_g	semiconductor band-gap energy
E_i	intrinsic Fermi energy
E_v	valence band energy
e_i	electron-hole pair generation energy
f	(i) image intensity (ii) fraction of carriers lost at the junction
f_D	fraction of electron beam energy absorbed by gate oxide
F	Fourier transform function
$\mathcal{F}$	Fourier transform operator
G	EBIC gain
G_c	gradient of the MOS conductance curve
G_s	gradient of the MOS subthreshold plot
G_t	threshold value for spatial filtering
g	output image intensity
$g(\underline{r})$	excess carrier density generation rate
i	horizontal index of frame in matrix scan
I	current
I_b	electron beam current
I_D	drain current
I_g	electron beam generated current
I_m	theoretical maximum EBIC current
I_{mg}	current at mid-gap bias
I_{sc}	short-circuit current (EBIC)
j	(i) $(-1)^{\frac{1}{2}}$ (ii) vertical index of frame in matrix scan
J_x	current density
k	(i) Boltzmann constant (ii) fraction of holes trapped in gate oxide
K_α	characteristic X-ray line
L, L_n, L_p	(i) minority carrier diffusion length (for electrons/holes)
L	(ii) gate length
M	magnification
n	(i) free electron density (ii) number of points
n^+	denotes heavy n-type doping
n_i	intrinsic carrier concentration
N	number of pixels in each dimension of an image (usually 512)
N_A	acceptor concentration

N_D	donor concentration
N_{ox}	surface charge number density
p	free hole density
p^+	denotes heavy p-type doping
q	electronic charge
Q_{ox}	surface charge density
Q_{int}	total interface charge
Q_{it}	interface trapped surface charge density
Q_f	fixed oxide surface charge density
Q_m	mobile ionic surface charge density
Q_{ot}	oxide trapped surface charge density
$\underline{r}$	position vector
R	INTU1 ADC sampling rate
R_B	Bethe electron range
R_G	Grün electron range
s	reduced surface recombination velocity = v_s/D
t	time
t_{ox}	gate oxide thickness
T	temperature
u	spatial frequency, x-direction
v	spatial frequency, y-direction
v_o	CRT linescan spot velocity
v_s	surface recombination velocity
V	voltage
V_{DD}	positive power supply voltage
V_{DS}	drain voltage
V_{FB}	voltage for flat-bands
V_{GS}	gate voltage
V_{mg}	mid-gap bias gate voltage
V_{oc}	open circuit voltage
V_{SS}	Negative power supply voltage
V_t	threshold voltage
W	gate width
x	distance, image x-coordinate
x_d	defect x-coordinate
x_s	scan x-coordinate
X_0, X_1	circuit fiducial reference coordinates
y	distance, image y-coordinate
y_d	defect y-coordinate

y_s	scan y-coordinate
Y_0, Y_1	circuit fiducal reference coordinates
Y_s	y-intercept on the MOS subthreshold plot
Z	atomic number
z	depth
β	q/kT
δ	depletion region width
ΔN	change in number density of trapped charges
Δp	excess, injected hole density
ΔV_t	change in threshold voltage
ΔV_{it}	change in interface state threshold voltage contribution
ΔV_{ot}	change in oxide trapped charge threshold voltage contribution
Δu	spatial frequency sampling increment
Δx	sampling increment
ϵ_o	permittivity of free space
ϵ_{ox}	relative permittivity of gate oxide
ϵ_s	relative permittivity of silicon
η	backscattering coefficient
η_{cc}	charge collection efficiency
η'_{cc}	smeared experimental value of η_{cc} due to beam spreading
θ	angle between coordinate systems
κ	fractional, mean energy of backscattered electrons
λ	normalised depth-dose in the Everhart-Hoff polynomial
μ	(i) mobility (ii) X-ray mass attenuation coefficient
ρ	(i) density (ii) charge density
τ	minority carrier lifetime
φ	charge collection probability
φ_m	metal work function
φ_{ms}	metal-semiconductor work function difference
χ	electron affinity
ψ	electrical potential
ψ_b	bulk Fermi potential (measured from the intrinsic level)
ψ_s	silicon surface potential
$*$	convolution operator
$*$	complex conjugate

1 INTRODUCTION

Since the invention of integrated circuits (IC's) in 1959 (Kilby, 1976) circuits of greater size and complexity have continuously been produced. Larger silicon die sizes have allowed the integration of more transistors, and along with smaller minimum geometries have helped to achieve the desired reduction in chip production and system costs. Since the beginning of very large scale integration (VLSI) in about 1975 (Sze 1983, p. 4) we now have, for example, microprocessor circuits containing more than 10^6 transistors each. Visual inspection of such circuits becomes impractical because of the time involved, and operator fatigue which could lead to missed defects anyway.

In parallel with these developments the SEM has become an important tool for IC inspection and failure analysis. Indeed, as minimum IC feature sizes are reduced to 1 μm and smaller, the SEM has become a necessity since the maximum resolution and depth of field of light microscopy is insufficient. SEM's have high resolution and depth of focus, need little specimen preparation, and allow several imaging modes to be easily implemented. In particular, the electron beam induced current (EBIC) mode gives valuable electrical information about the sub-surface device structure. In recent years a popular extension of the instrument has been the addition of an image processor. This allows images to be acquired and stored digitally, but more important, allows computer methods to be utilised for their analysis. The power of these image processors is increasing rapidly.

A government initiative called Alvey led to a project (ALV/VLSI/104) of which the work reported here forms a part. The contribution of the group

at Imperial College was to develop methods whereby image processing could be used as an aid to defect location and identification in VLSI circuits. Unfortunately, delays in the award of the capital grant and then the time taken to deliver the new equipment (a JEOL 840A SEM and Kontron IBAS image processor) meant that work on this aspect could only be carried out for a part of the period of study. Because of this, work was also carried out in areas related to the future goal of automatic defect location and identification.

Irradiation damage is one such aspect. It is well known that SEM examination of MOS devices can be destructive. It is therefore necessary to determine the regimes in which damage occurs. Furthermore, it is essential to gain a theoretical understanding of the mechanisms involved in damage in order to define safe operating regimes for a variety of device types. This may also lead to development of non-destructive methods for use when necessary. The opportunity to do this was given by the facilities of the device failure analysis group at GEC Hirst Research Centre, who funded this CASE studentship.

Once defects have been located, specialised techniques are required for their identification. This group has a history of research in EBIC. For this reason, work was carried out to automate EBIC data acquisition, and to investigate its application to studies of a particular type of defect which could be located by image processing – electrostatic discharge damage.

2 THEORY AND LITERATURE REVIEW

2.1 ELECTRON-SPECIMEN INTERACTIONS

In the SEM, electrons are accelerated to high energy (0.2–40keV) and focussed to a demagnified spot which is raster scanned over the specimen. As primary electrons penetrate the specimen, they undergo two main types of interaction. Inelastic scattering is mainly due to interactions with the electron cloud of atoms and is the main source of energy loss, but results in small deflections in trajectory. Less likely elastic scattering events are due to Coulombic interactions with the (screened) nuclear charge. Owing to the large disparity in mass between the primary electron and the nucleus, there is negligible energy transfer, but large deflection in the electron path. The nett result of these two scattering events is that electrons tend to travel into the specimen losing energy continuously until elastic scattering causes deflections, making the beam "mushroom" out into the characteristic pear shape of the excitation volume. Fig. 1 summarises the variety of emissions which arise from these processes.

Of particular interest in this work is the depth-dose function, $dE(z)/dz$. This describes the average rate of energy loss of an electron with depth averaged over many electrons of a given primary beam energy, E_b . If the electron-hole pair formation energy is known, this enables quantitative calculations of EBIC and beam damage. Two methods of calculating the depth-dose function will now be discussed.

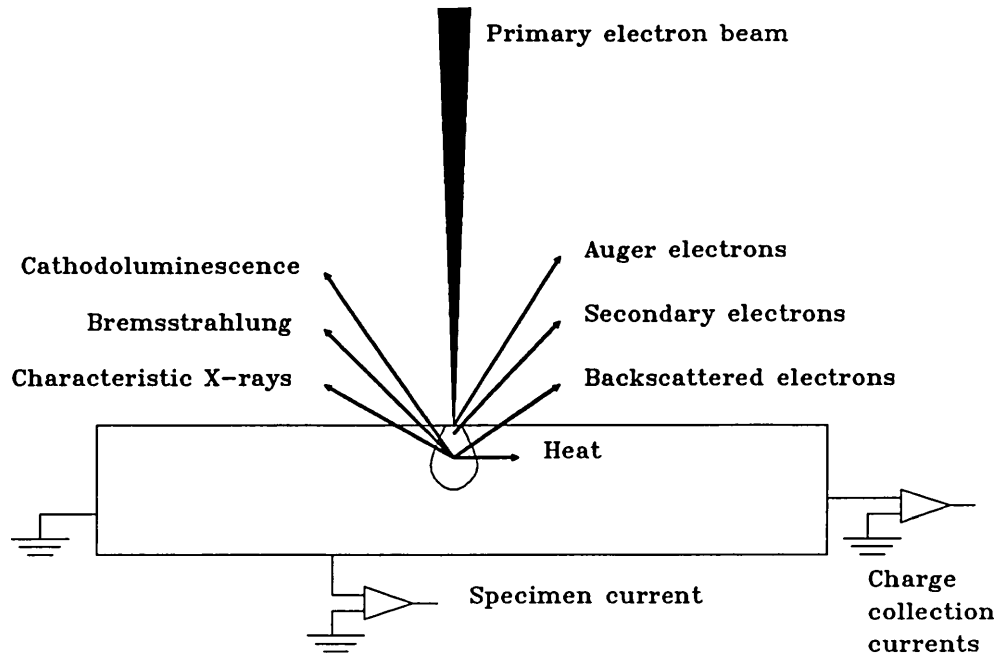


Fig. 1. The emissions resulting from electron-specimen interactions.

2.1.1 The Everhart-Hoff Depth-dose Function

In silicon the depth-dose function can be obtained from the empirical model of Everhart and Hoff (1971), who made measurements of beam induced current in MOS structures. They found that $dE(z)/dz$ could be fitted by a cubic polynomial which was scaled to allow for the deeper penetration at higher E_b . The scaling was accomplished using the Grün (1957) range, R_G , given (in μm) by

$$R_G \rho = 0.040 E_b^{1.75} \quad (1)$$

where ρ = density (gcm^{-3}),
 E_b = beam energy (keV)

From their experimental data they determined a normalised depth-dose function,

$$\lambda(z/R_G) = 0.60 + 6.21 (z/R_G) - 12.40 (z/R_G)^2 + 5.69 (z/R_G)^3 \quad (2)$$

So that

$$\frac{dE}{dz} = \frac{(1-\kappa\eta)E_b}{R_G} \lambda(y) \quad (3)$$

where η = backscattering coefficient,
 κ = fractional mean energy of backscattered electrons.

Sternglass (1954) measured the energy distribution of backscattered electrons, and found that the fractional backscattered energy, κ varied linearly with atomic number, Z :

$$\kappa = 0.45 + 2 \times 10^{-3} Z \quad (4)$$

Thus, for silicon ($Z = 14$), $\kappa = 0.478$. Sternglass (1954) also found that the backscattering coefficient, η varied very weakly with beam energy for $Z < 30$. Fiebiger and Muller (1972) exploited the linear relationship between η and Z to interpolate values for Cu (0.29) and Al (0.145), giving 0.16 for silicon. Thus, the term $(1 - \kappa\eta) \approx 0.92$, and this value has been used by several subsequent authors (Leamy, 1982). It is a small correction factor and can also be evaluated directly using Monte Carlo simulations (Napchan and Holt, 1987), giving a similar result.

In the case of a multi-layered structure, the "mass thickness", ρz , can be considered instead of z , as the former is material invariant. On transforming from z co-ordinates to ρz co-ordinates, Si layers are converted to an equivalent thickness of SiO_2 .

A three dimensional theoretical model of the excitation volume was due to Kanaya and Okayama (1972). This model uses expressions for a part-sphere with its centre at a calculable distance below the surface. However, it does not lend itself easily to multi-layer calculations.

2.1.2 Monte-Carlo Simulations of Electron Trajectories

An alternative method of determining dE/dz is directly from the output of a multi-layer Monte-Carlo simulation. Such programs insert random numbers into a suitable physical model to simulate what might happen to an electron as it penetrates into the specimen. While a single trajectory might be non-typical, the average of a large ensemble should describe the true situation.

The implementation of such programs was well described by Joy (1988), and will only be outlined here. The basic assumptions made are that:

- (i) Inelastic scattering is responsible only for a continuous slowing down (described by the Bethe energy loss expression),
- (ii) Elastic scattering is responsible for all changes in direction of electron trajectory, (given by the Rutherford elastic scattering cross-section).

These assumptions are justified, because elastic scattering angles range from $5-180^\circ$, while inelastic scattering angles are small, typically less than 2° . Two procedures for the calculation are possible:

Plural Scattering

In this case, the Bethe range is calculated (i.e. the distance for an electron to reach some small, cut-off energy) and divided into (say) 50 equal steps. At the end of each step, a scattering angle is calculated using a random component, and the energy lost during that step is assigned to an output energy matrix. The process is then repeated for all 50 steps, and for the number of electrons in the simulation.

Single Scattering

This model should be more accurate. Contrary to the previous method, the energy-dependent mean free path (including a random element) is calculated for each step from the Rutherford scattering cross-section. Again, the energy lost in each step is placed in an output array, and the process repeated until the electron energy falls below some threshold (typically 1keV). Although more accurate, this method is significantly slower.

In this work, a program due to Napchan and Holt (1987) was used, which could account for multi-layered specimens.

2.2 ELECTRON BEAM INDUCED CURRENTS IN IC's

In the following sections, first the physics of EBIC, and then its application to integrated circuits will be described.

2.2.1 Physics of EBIC

When electrons of energy E_b are incident on a semiconducting specimen, the number of electron-hole pairs produced per incident electron is referred to as the gain,

$$G = (1 - \kappa\eta) \frac{E_b}{e_i} \quad (5)$$

where $\kappa\eta$ is the backscattering energy loss, discussed in section 2.1.1. The average electron-hole pair formation energy, e_i is found experimentally to be about three times the energy gap for most semiconductors. This also appears to have some theoretical foundation (Klein, 1968). e_i is independent of the type of ionising radiation (α, β, γ), provided the energy quanta are $\gg E_g$. For kilovolt electrons the only differences are in the depth of penetration and the residual injected charge. In silicon $E_g = 1.12\text{eV}$ while $e_i = 3.6\text{eV}$. Thus, considering a beam energy of 20 keV, in silicon, then equation (5) gives a gain,

$$G \sim 0.92 \times 20 \times 10^3 / 3.6 \sim 5 \times 10^3 \quad (6)$$

This large current gain gives good signal to noise ratios.

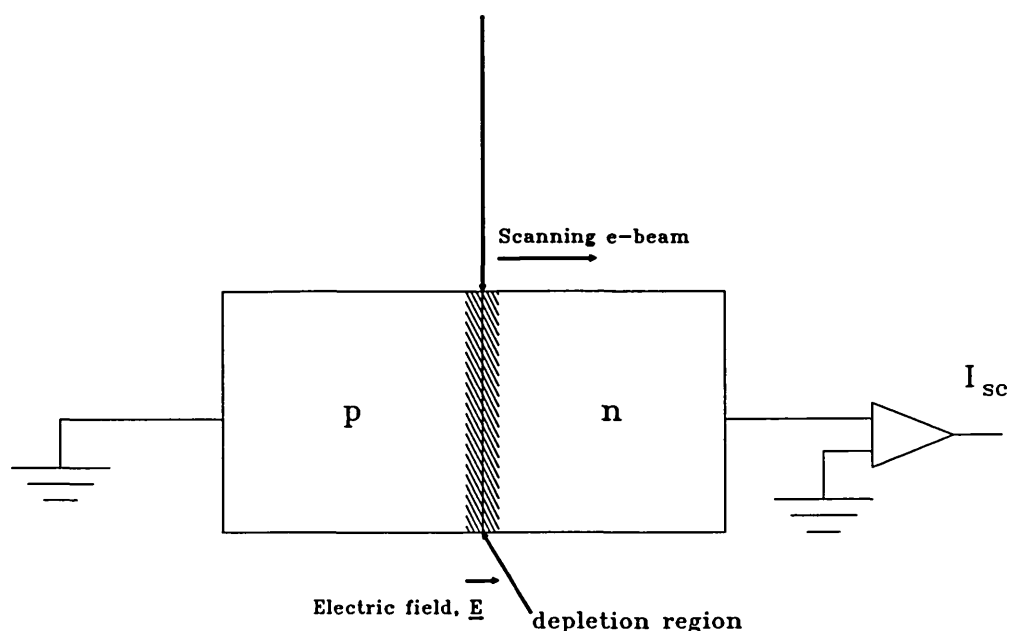


Fig. 2. A simple specimen geometry for EBIC.

If an electric field is present in the vicinity of e-h pair generation the carriers will be separated by drift motion. Furthermore, if they are separated into regions connected to the input terminals of an amplifier, a charge collection (CC) signal is produced. There are three possible sources of the separating field (Holt, 1974):

- (i) barrier electron voltaic effects due to built-in fields at pn-junctions or Schottky barriers,
- (ii) bulk electron voltaic effects occurring, for example at doping inhomogeneities or pp⁺ junctions,
- (iii) an externally applied bias.

A simple specimen geometry for EBIC is shown in Fig. 2, in which the electron beam impinges on a semiconductor containing a pn-junction. A depletion region exists at the junction due to recombination of majority carriers which diffuse across it. This leaves adjacent regions of charged donors and acceptors, leading to the well-known built-in field (Fig. 3)

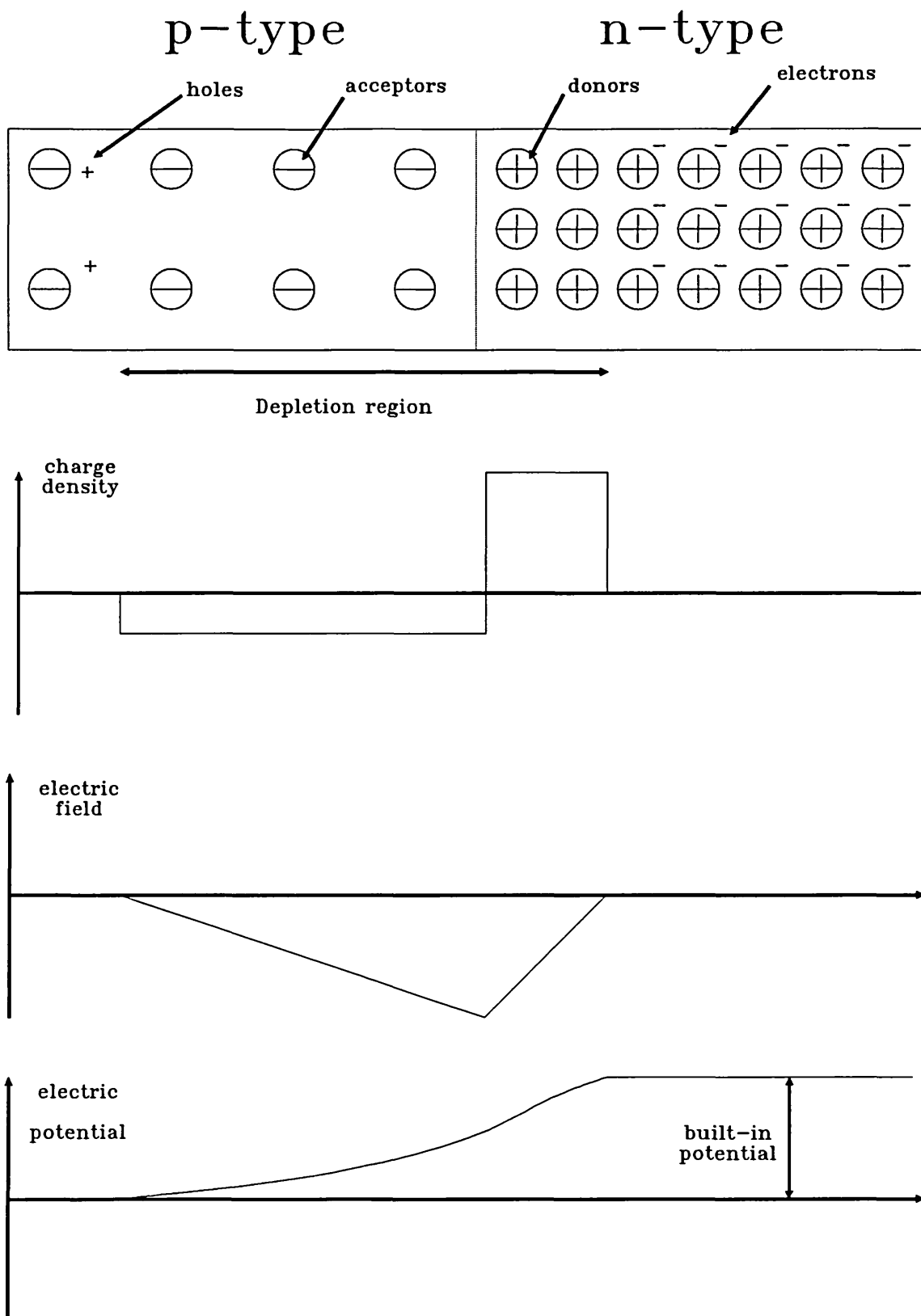


Fig. 3. The variation of various parameters across a pn-junction, showing the origin of the built-in field.

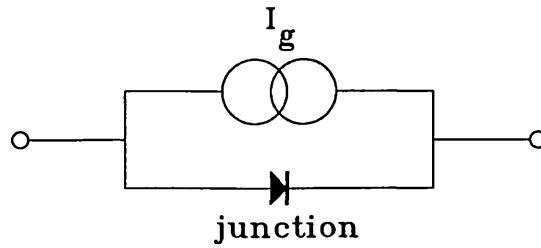


Fig. 4. The equivalent circuit of a diode that is irradiated by an electron-beam.

(Sze, 1981). The electron-hole pairs generated when the electron-beam is outside the depletion region diffuse randomly until they recombine. If they reach the depletion region, the electric field direction and strength is such that they will be swept across it, and become majority carriers on the opposite side of the junction. This movement of charges constitutes a current source in parallel with the junction forcing current in the same direction as the diode reverse leakage current, as represented by the equivalent circuit of Fig. 4. The I-V characteristic of the specimen is then given by

$$I = I_g - I_o \left[e^{qV/nkT} - 1 \right] \quad (7)$$

where

- I_g = current generated by the e-beam,
- I_o = diode saturation current,
- n = diode ideality factor, typically 1-3,
- k = Boltzmann's constant,
- T = absolute temperature.

If the two contacts were short circuited, $V=0$ and a current would flow given by

$$I_{sc} = I_g = \eta_{cc} G I_b \quad (8)$$

where I_b is the beam current and η_{cc} is the charge collection efficiency which expresses the fraction of generated e-h pairs which are collected before they recombine, and G is given by equation (5). In practice I_{sc} is measured using a very low input impedance current amplifier (i.e. $V=0$ in equation (7)), giving true EBIC. It is also possible to measure the open circuit voltage, V_{oc} if the amplifier impedance approaches infinity. This is called true EBIV, but is less often used.

The diffusion and recombination of the excess minority carriers generated by the electron beam is described by the time-independent continuity equation,

$$D \nabla^2 \Delta p(\underline{r}) - \frac{\Delta p(\underline{r})}{\tau} = -g(\underline{r}) \quad (9)$$

where $\Delta p(\underline{r})$ = excess, injected minority carrier density,
 $g(\underline{r})$ = carrier density generation rate (due to the e-beam),
 D = diffusion coefficient,
 τ = minority carrier lifetime,
 $\underline{r}$ = position.

With the addition of the boundary condition that $\Delta p(\underline{r})=0$ at the collecting junction, this has been solved in simple cases for $\Delta p(\underline{r})$. Then I_{sc} is determined from the normal gradient of $\Delta p(\underline{r})$ at the collecting barrier. In the case of the pn-junction of Fig. 2, this gives (e.g. Holt, 1974):

$$I_{sc} = I_m e^{-x/L} \quad (10)$$

where I_m = the theoretical maximum current when $x = 0$ and $\eta_{cc} = 1$,
 L = minority carrier diffusion length $(= (D\tau)^{1/2})$,
 x = distance from the junction.

This equation can be simply rearranged into a logarithmic form with gradient L . Thus EBIC linescans can be used to determine L in principle, and such experiments have been one of the most common uses of EBIC to date (Leamy, 1982). The main complication in this treatment is surface recombination (Hungerford, 1988).

Donolato (1988) described how I_{sc} could be calculated using the notion of charge collection probability, $\varphi(\underline{r})$, which eliminates the intermediate step of determining $\Delta p(\underline{r})$. The collection efficiency is simply the probability that a minority carrier generated at $\underline{r}$ will reach the collecting barrier. As such, it is dependent only on the specimen geometry. It has been shown (Donolato, 1985) that $\varphi(\underline{r})$ obeys a homogeneous version of the continuity equation, (9):

$$D \nabla^2 \varphi(\underline{r}) - \frac{\varphi(\underline{r})}{\tau} = 0 \quad (11)$$

with the boundary condition $\varphi(\underline{r}) = 1$ at the collecting barrier. Not only is this viewpoint more intuitive, but it is more straightforward to calculate than $\Delta p(\underline{r})$ from equation (9). For example, in the one-dimensional case of a Schottky barrier in Fig. 5 it is readily shown by direct substitution into equation 11 that $\varphi(z) = e^{-z/L}$. Once $\varphi(\underline{r})$ is known for a particular geometry, to calculate I_{sc} with a real extended generation source, $g(\underline{r})$, the two are multiplied and integrated over the specimen volume, V :

$$I_{sc} = \int_V \varphi(\underline{r}) g(\underline{r}) dV \quad (12)$$

Such relations can also be applied to pn-junctions. This phenomenological theory of EBIC is a much simpler method of analysing results numerically than direct solution of the continuity equation.

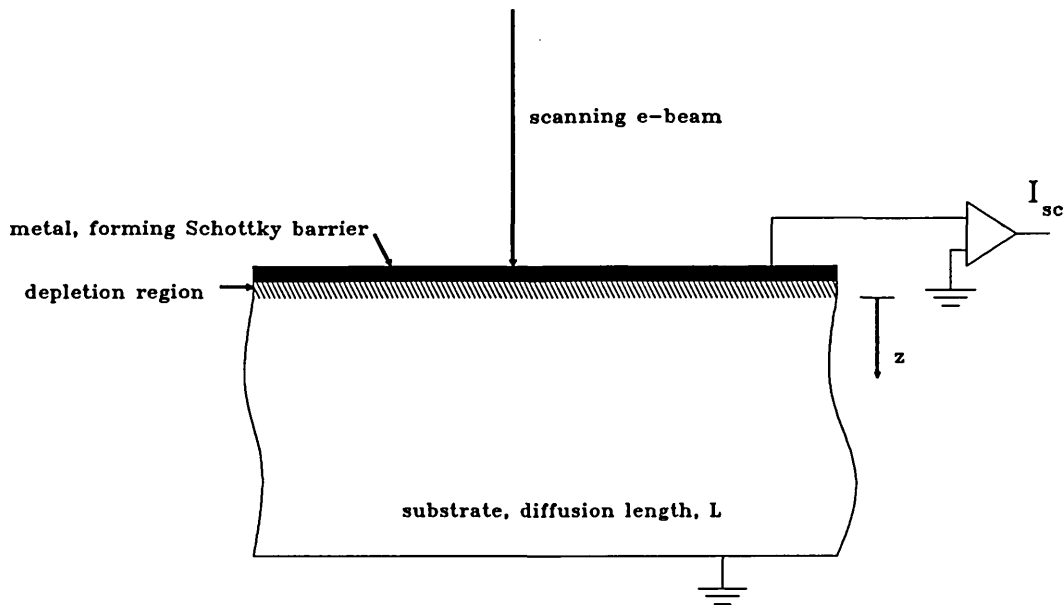


Fig. 5. EBIC geometry of a planar Schottky diode.

2.2.2 EBIC of Integrated Circuits

EBIC images of integrated circuits consist essentially of a map of the junctions, smoothed by the effect of the beam excitation volume and L , and modified by the presence of certain defects. In contrast to the simple geometries described above, IC's have many layers, and a complex, three dimensional structure. Cross-sectioning of devices followed by appropriate staining has long been employed to visualise device structure by SEM (Koellen *et al*, 1985), and with great care, TEM can give very informative images of layers in this planar technology (Marcus and Sheng, 1983). EBIC allows pn-junction electrical properties to be observed in-situ by examining sectioned devices edge-on while operational (Kaitna and Wernisch, 1982). The broadening effect of the junction paths (due to L) can be removed by image processing to improve the spatial resolution (Schink and Rehme, 1983). However, all these techniques are physically destructive. Keeping

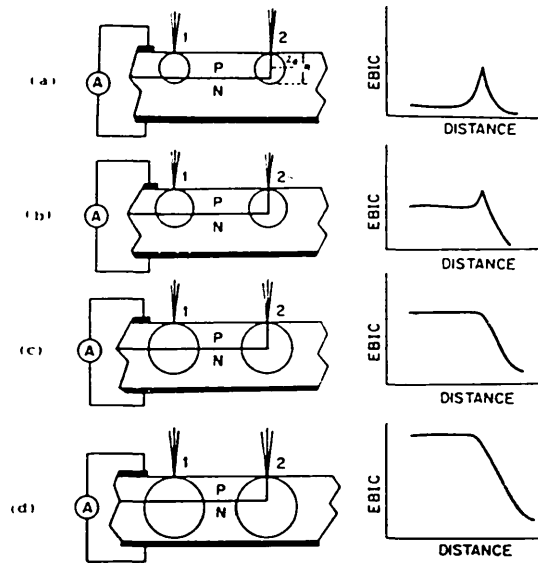


Fig. 6. Schematic representation of the model used for the determination of the depth of a planar pn-junction, after Chi and Gatos (1977).

the device intact, Chi and Gatos (1977) determined the depth of planar pn-junctions by varying the accelerating voltage and thus the penetration depth while scanning across the junction edge region. (Fig. 6). At low E_b (Fig. 6a), the vertical section of the pn-junction contributes strongly, and I_{sc} is peaked at the junction edge. At high E_b (d), the horizontal section of the junction dominates. The E_b at which the peaking behaviour disappeared was related to the junction depth by assuming a spherical beam excitation volume, the centre of which was at half the Gruen range.

Okamura and Mijoshi (1982) and Schick (1985) showed how scanning across an MOS transistor resulted in two EBIC peaks at the source and drain to body junctions, from which they measured the channel length (for a definition of channel length, see Fig. 11).

Interpreting complex integrated circuit images was discussed in detail by Gonzalez (1974). The effect of the multi-layered structure was considered with reference to a diode (Fig. 7). It consisted of a planar pn-junction,

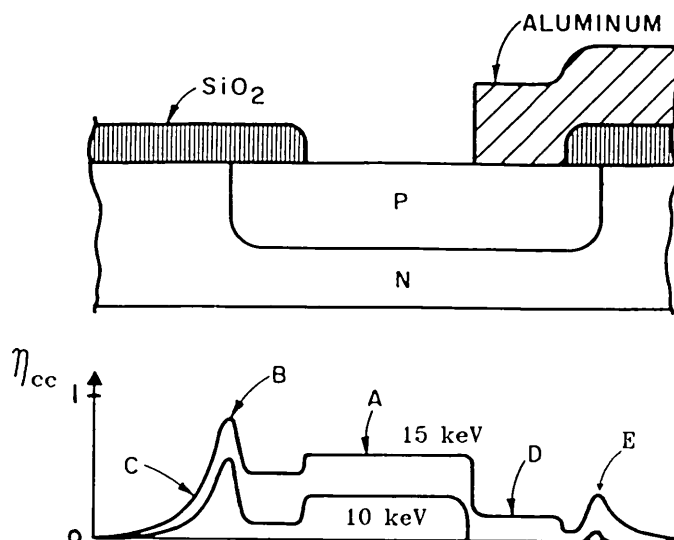


Fig. 7. EBIC response (bottom) of a diode structure (top), after Gonzales (1974).

isolation oxide layer, and aluminium contact metallisation. Considering first the top EBIC profile taken at 15 keV, at A the signal is due to collection by the horizontal junction. The signal is attenuated at D owing to aluminium limiting penetration of the beam. The peaks at B and E are due to an increased area of (vertical) depletion region (the low E_b case of Chi and Gatos (1977)). At C, a pseudo-exponential tail is related to minority carrier recombination in that region (cf equation 10). In the lower curve taken at 10 keV, some parts of the profile disappear, as the beam no longer penetrates deep enough to reach the semiconductor. Thus contrast of devices within IC's is intricately dependent on all the layers present.

The other factor in interpretation of IC EBIC images is secondary devices which may be located near the collecting junction, or connected in the circuit path. Gonzalez (1974) pointed out that adjacent isolated junctions could actually inject carriers into the collecting junction, thereby augmenting I_{sc} . Another common situation is that of two junctions in series, such that the same type of material forms their interconnection. This is effectively

two diodes back to back and the junctions will give signals of opposite polarity, attenuated in each case due to the reverse biased junction impedance.

The main use of EBIC in examining IC's has therefore been confined to qualitative microscopy for the location of failure defects in IC's. Schick (1985) showed how a leaking bipolar transistor could be located easily in an array of 320. When connected between emitter and substrate, "piped" transistors (those with a short through the base) showed up brightly. This was attributed to domination of I_{sc} by the current generated in the collector junction, passing easily through the (resistively) shorted base, as opposed to the two back-to-back diodes of the working transistors. Similar piped transistors were observed by Sørensen *et al* (1980), Fantini, (1984) and IBM (1986).

Griffith *et al* (1976) used EBIC to locate localised defects in MOS devices. Later, Reimer *et al* (1987) attributed the contrast mechanism to local shorts of the gate oxide which allow enhanced EBIC collection. Thus oxide breakdown sites appeared as bright spots due to a resistive short through the gate oxide that allowed collection of charges separated by the depletion region beneath the gate. Bright spot and line defects in CCD image sensor chips have also been observed (Holt and Lesniak, 1985). Piety *et al* (1981) investigated gate shorts in MOS transistors within IC's and discussed the advantages of movable electrical probes inside the SEM and selective track cutting to test discrete transistors. This approach has been used by other workers (Mauduech, 1982) but can be destructive and time consuming, as well as requiring detailed knowledge of the device functionality.

EBIC has also been used for the location of electrostatic discharge (ESD) damage, which is sometimes not visible by light microscopy (Richards and Footner, 1983), and can give informative images of breakdown paths (Trigonis, 1976). The mechanisms of ESD will be discussed later.

Beal *et al* (1980) showed that the visual information about junctions in a device can be used to complement light microscopy, SE and VC images to determine interconnection schemes. The voltage contrast technique (Menzel and Kubalek (1983) is worth a little discussion. Basically it occurs while examining functioning integrated circuits with an SEM. Contrast is due to differences in logic state, because 'high' (+5 V) metal tracks allow fewer secondary electrons to escape than 'low' (0 V) tracks. Hence logic low tracks appear bright and logic high tracks appear dark. A map is therefore built up of the logic states over the whole chip. This can also be done in stroboscopic mode, whereby the beam is blanked in synchronism with an electrical test-cycle of the chip. Each logic state in the cycle is then sampled by varying the beam blanking phase relative to the test-cycle. If the beam is held stationary, the voltage waveform at a point can be reconstructed.

Dressendorfer (1980) showed that EBIC could locate latch-up sites in CMOS circuits. The details of latch-up are beyond the scope of this work, but it is basically due to a pnpn structure formed in CMOS circuits as shown in Fig. 8. This constitutes two parasitic bipolar transistors connected in a loop, such that if the transistors have high enough gains, it causes high power supply currents to flow due to positive feedback. It is possible for system transients to switch on the parasitic transistors, resulting in very large current drain on the power supply, and possible failure (Ong, 1984, p272). If an EBIC amplifier is connected to the power supply pins, Dressendorfer (1980)

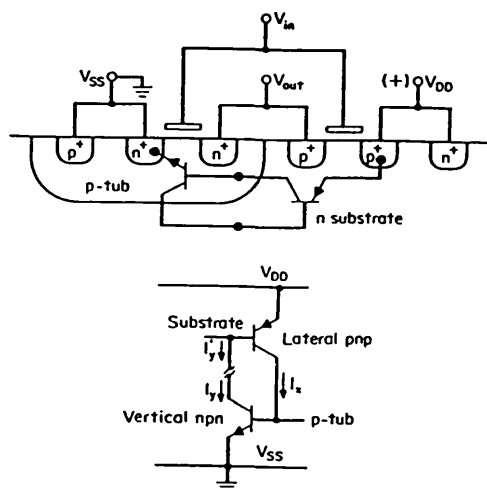


Fig. 8. pnpn structure formed in CMOS circuits which causes latch-up, after Ong (1984).

showed that latch-up could be activated by the electron beam, and that it was manifested as a large increase in EBIC current. Later, Davidson (1983) showed that although rough location using EBIC could be achieved, it was necessary to locate the exact position of the current paths using voltage contrast, and that EBIC was most likely destructive. This method is still employed, mostly using OBIC (e.g. Quinke *et al*, 1987).

In OBIC a scanning, focussed light spot is used instead of the electron beam, and results in images of very similar character to EBIC (Wilson, 1984, pp187–190). Authors often refer to the destructive nature of EBIC, in terms of charging, threshold voltage shifts and enhanced leakage currents. This is a shame, because by varying E_b , the penetration depth can be varied, and also, as the depth-dose function is peaked below the surface, EBIC is more sensitive to the depth of structures being examined. In the scanning optical microscope, varying the penetration depth necessitates more than one laser (Ziegler and Feuerbaum, 1987). An alternative is to use a SOMSEM – scanning optical microscope in the SEM. In this system (Fig. 9) the

scanning electron beam is focussed onto a phosphor screen. Light emitted from the underside is then focussed onto the specimen, scanning in synchronism with the e-beam. By using a carousel of phosphors, the light wavelength can be changed. The signal levels attainable can be quite low, however.

Little systematic work on quantifying the destructive effects of EBIC has been done to date, but its advantages over OBIC suggest this could be a fruitful line of research.

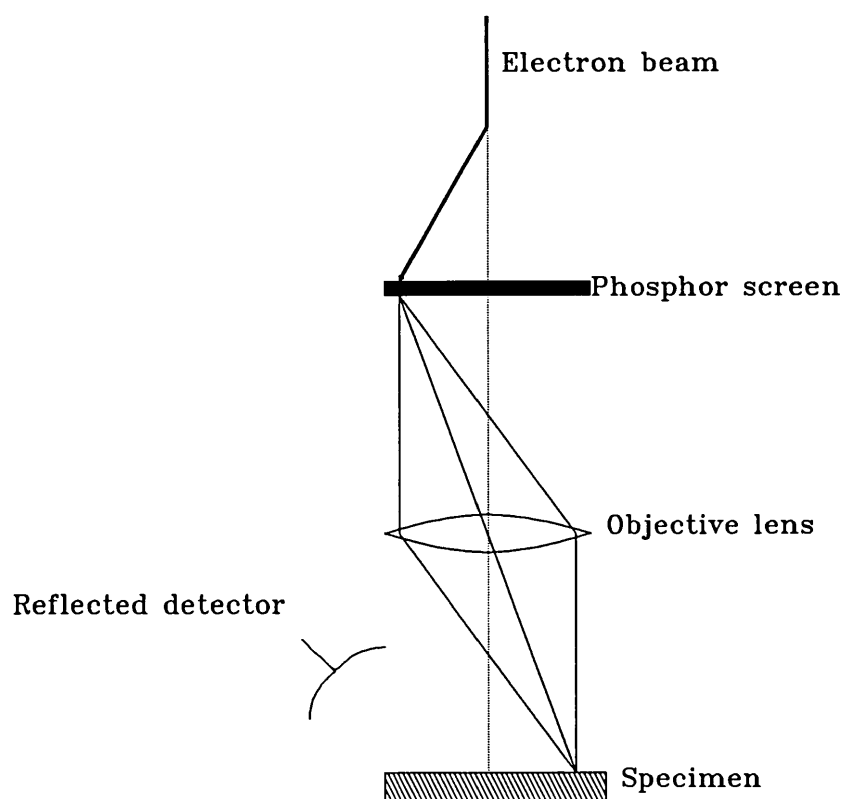


Fig. 9. Principle of the scanning optical microscope in the SEM – the SOMSEM.

2.3 ELECTRON BEAM IRRADIATION DAMAGE

It has long been known that electron beam examination of integrated circuits can have a deleterious effect on device characteristics. Three categories of damage can be identified,

- (i) Atomic displacement damage,
- (ii) Contamination,
- (iii) Charge storage.

The first only occurs at energies in excess of 170keV (Keery *et al*, 1976) and is of no concern in the SEM. Contamination is due to the adsorption of organic vacuum contaminants from diffusion pump oil back-streaming, O-rings, grease etc. These molecules subsequently migrate over the specimen surface before undergoing a cross-linking process induced by the electron beam at the point of impact (Hart *et al*, 1970). Contamination is much less of a problem today with the improvements in vacuum technology. Indeed, there exists a noticeable difference between the two SEM's in this research group – one a ten year old JEOL JSM-35, and a newer JSM-840A. In the latter, contamination is not significant.

In this work the concern is with various types of "charge storage effects" which degrade electrical device performance. MOS (metal oxide semiconductor) devices are particularly prone to this type of damage, and are the ones studied here. In this section, the MOS system, its charges and the relevant device physics will be reviewed before the main discussion of e-beam damage.

2.3.1 Charges in the MOS System

A full account of oxide charges and MOS physics and technology in general can be found in the treatise by Nicollian and Brews (1982). SiO_2 can exist in several crystalline forms, such as quartz, cristobalite and tridymite. However, in MOS technology, SiO_2 is thermally grown on Si at temperatures of 750–1200 °C in tube furnaces and forms a stoichiometric, amorphous layer with a much more open structure. Water is sometimes added to increase growth rates. The oxide consists of tetrahedrally bonded silicon, with bridging oxygen atoms, and is made up of rings containing an average of six silicon atoms. This results in a somewhat open structure, with density 2.2 gcm^{-3} (compared to 2.3 gcm^{-3} for quartz).

The interface region contains a transition layer, with composition SiO_x in which $0 < x < 2$. This layer is approximately 2.5nm thick, and is known to contain all of Si^+ , Si^{2+} and Si^{3+} oxidation states (Henzler, 1986). These are sometimes referred to as dangling bonds. In practice, the situation is complicated still further by the presence of hydrogen or water, which can passivate some of these bonds, and incorporate chemically into the structure. In order to standardise the plethora of names used for oxide charges, Deal (1980) proposed a terminology and notation which is now widely accepted. Each charge has a number density, N_{ox} (cm^{-2}), and a charge density, Q_{ox} (Ccm^{-2}) which is tacitly assumed to be situated at the Si– SiO_2 interface. Referring to Fig. 10, the four charge types are as follows:

Q_m – mobile ionic charge

This is mainly due to alkali metal ions, particularly Na^+ , which drift interstitially in electric fields giving device instabilities. Clean processing, and gettering techniques make this a minor problem today.

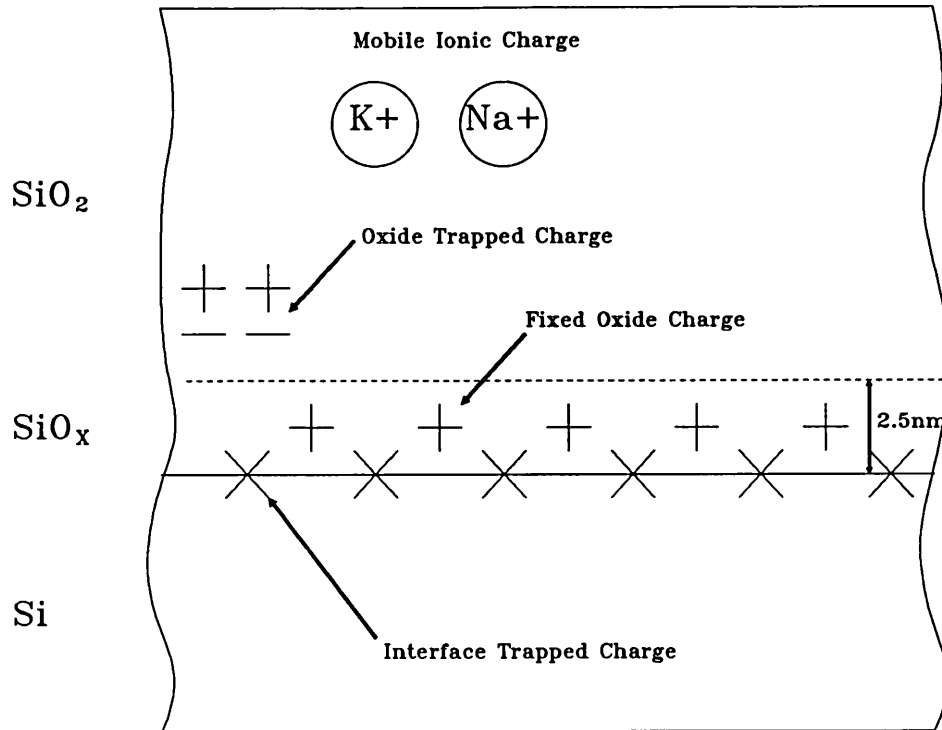


Fig. 10. Oxide charges in the MOS structure, after Deal (1980).

Q_{ot} – oxide trapped charge

This can be either positive or negative, and can be located throughout the oxide thickness. It is the result of trapping of holes or sometimes electrons which have been injected into the oxide by ionising radiation or hot carriers from the Si substrate. The charge can be annealed out at $< 500^\circ\text{C}$ in H_2 , although the neutral traps may need higher temperatures, and some cannot be removed at all (Shimaya *et al*, 1983). In that case, they can simply be filled again. The density of traps is intimately related to processing conditions, and is thought to be due to both water or hydrogen related species, and Si-Si stretched bonds (oxygen vacancies) in the SiO_2 (Hiroshi *et al*, 1988). Generation of neutral traps by ionising radiation during processing is an active area of study at present in electron beam lithography for example (Cummings, 1989).

Q_{it} – interface trapped charge

These charges are situated at the Si–SiO₂ interface, and have energy levels within the Si bandgap. Consequently, they are in electrical communication with the Si, and become charged or discharged as the Si surface potential (band bending) varies due to the applied gate voltage. They are probably associated with dangling bonds in the SiO_x transition layer. More traps may be produced by ionising radiation which can break bonds in this layer as it is heavily strained on an atomic scale.

 Q_f – fixed oxide charge

This is situated within the SiO_x layer, less than 2.5nm from the Si, and is always positive. It is not in electrical communication with the Si, and is probably associated with dangling bonds. Like the other charges, it is strongly process dependent. Obviously there could be confusion with Q_{ot} , but Q_f is usually taken as the charge that remains after a low temperature hydrogen anneal (450°C).

The MOS system, and in particular the Si–SiO₂ boundary is probably the most studied interface to date. Despite many years of research, it is still not fully understood. However, by mainly empirical means, it is possible to maintain close control of the properties of thermally grown SiO₂.

2.3.2 MOS Transistor Physics

In all the following discussions, an n-type substrate is considered (p-channel transistors). The situation for n-channel is obtained by a suitable reversal of carrier type, dopant type and band-bending polarity.

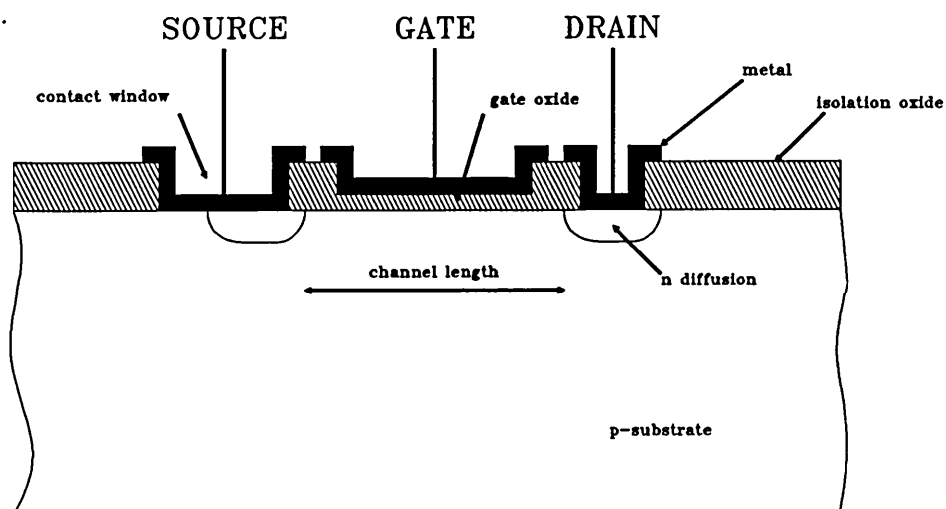
2.3.2.1 Basic Functionality

The main technology for modern VLSI circuits is almost exclusively MOS based. It requires less photolithography steps than bipolar processes, and achieves reasonable speeds with the highest available packing densities.

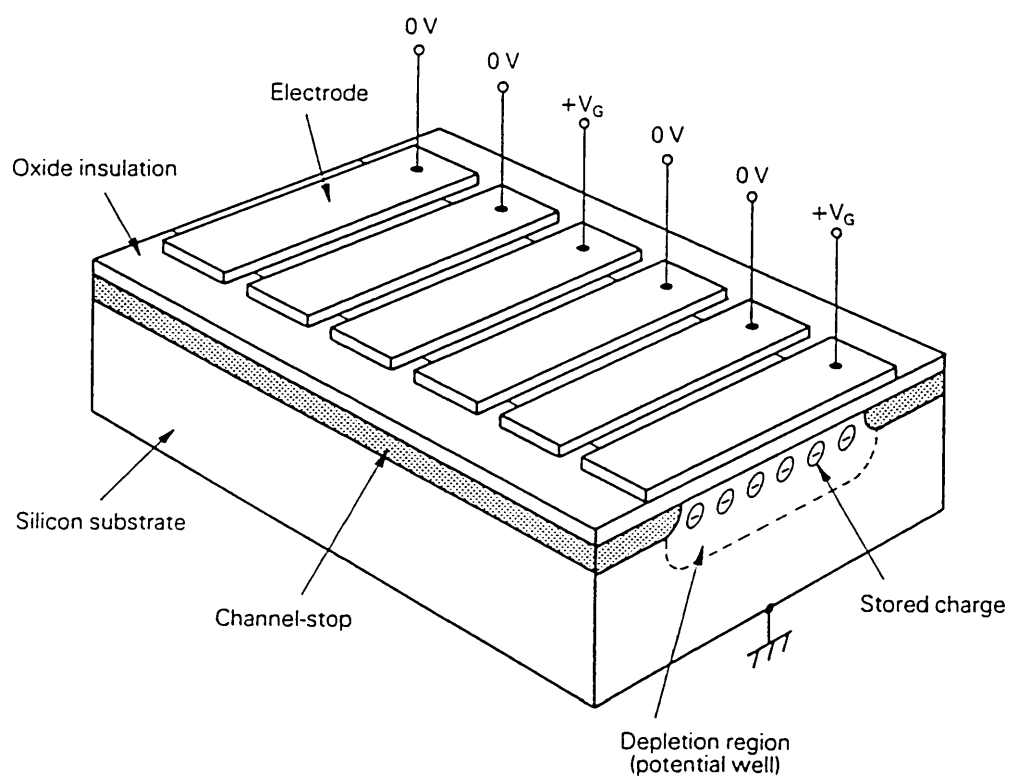
Before discussing the device physics in detail, it is convenient to give a qualitative description of the operation of an ideal MOS transistor as a switch. On referring to Fig. 11a, it is noted that there are three contacts, one of which is electrically insulated by the gate oxide. The basic operation is achieved by firstly applying a potential difference between source and drain, to drive current between them. The body (i.e. substrate or well) is usually grounded. Two conditions can be identified, depending on the gate voltage:

- (i) With 0V applied to the gate, the structure consists of two back to back diodes, and a very small current can flow.
- (ii) If a positive potential is applied to the gate, majority carrier holes will be repelled from a depletion region beneath the gate. When the gate voltage becomes higher still, holes are 'repelled' sufficiently that electrons 'attracted' to the surface remain the residual excess carriers, and a thin n-type inversion layer called the channel is formed. Conduction between source and drain increases dramatically as a continuous n-type layer exists. A threshold voltage, V_t can be defined as the gate potential at which the transistor just begins to conduct.

Therefore, the gate voltage switches the drain-source current. Fig. 11b shows a more specialised type of MOS IC, the charge coupled device (CCD). It consists of a series of electrodes placed across a channel. The



(a) A single MOS transistor.



(b) Part of a charge coupled device (CCD).

Fig. 11. MOS schematics of (a) a single transistor and (b) a charge coupled device (CCD).

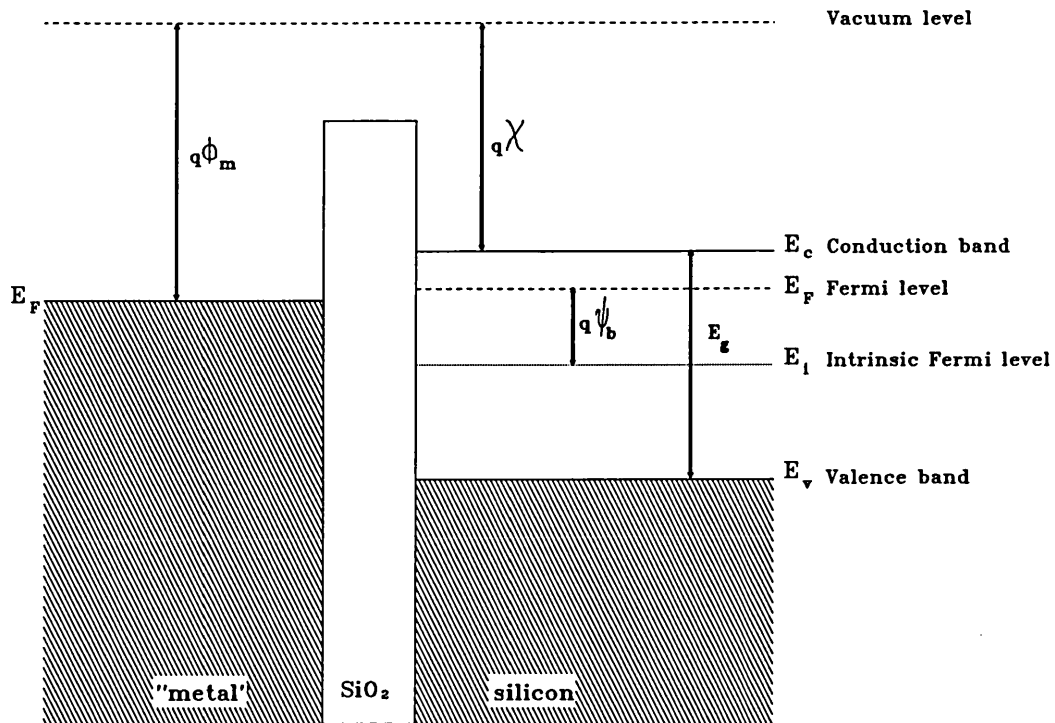


Fig. 13. Energy band diagram for the MOS structure.

2.3.2.2 The Threshold Voltage, V_t

Referring to the MOS band diagram (Fig. 13), it is seen that in general, an external voltage must be applied to maintain the Fermi level difference, with flat semiconductor bands. This is due to the difference in work function between the semiconductor and the gate material, and can be calculated from

$$\phi_{ms} = \phi_m - \chi - \frac{E_g}{2q} + \psi_b \quad (13)$$

where χ = the semiconductor electron affinity,
 E_g = silicon energy gap,
 ψ_b = bulk Fermi level (measured from the intrinsic level),
 ϕ_m = metal work function.

A further correction is necessary if there is a total oxide surface charge density,

$$Q_{ox} = Q_m + Q_{ot} + Q_{it} + Q_f, \quad (14)$$

then an additional gate voltage is required to induce neutralising charge in the gate metal, given by $V = Q_{ox}/C_{ox}$ where $C_{ox} = \epsilon_{ox}\epsilon_0/t_{ox}$, is the oxide capacitance per unit area. Thus the voltage necessary for flat bands is given by

$$V_{FB} = \phi_{ms} - \frac{Q_{ox}}{C_{ox}} \quad (15)$$

The silicon band diagram vertically downwards beneath the gate can now be considered in more detail (Fig. 14). The degree of band-bending is given by the silicon surface potential, ψ_s , which is defined as the potential difference between the intrinsic Fermi level at the surface and its bulk value. As a true electrical potential, it increases downwards on band diagrams. Three distinct conditions can be identified:

(a) Accumulation, $\psi_s > 0$

The bands are bent downwards, leading to an accumulation of electrons at the silicon surface.

(b) Depletion, $-\psi_b < -\psi_s < 0$

When ψ_s is negative and small, the bands are bent upwards, leaving a depletion region of positive donor ions.

(c) Inversion, $-\psi_s > \psi_b$

When $-\psi_s = \psi_b$, the surface layer is just inverted to p-type. Any further increase in $-\psi_s$ leads to the formation of an inversion layer. If

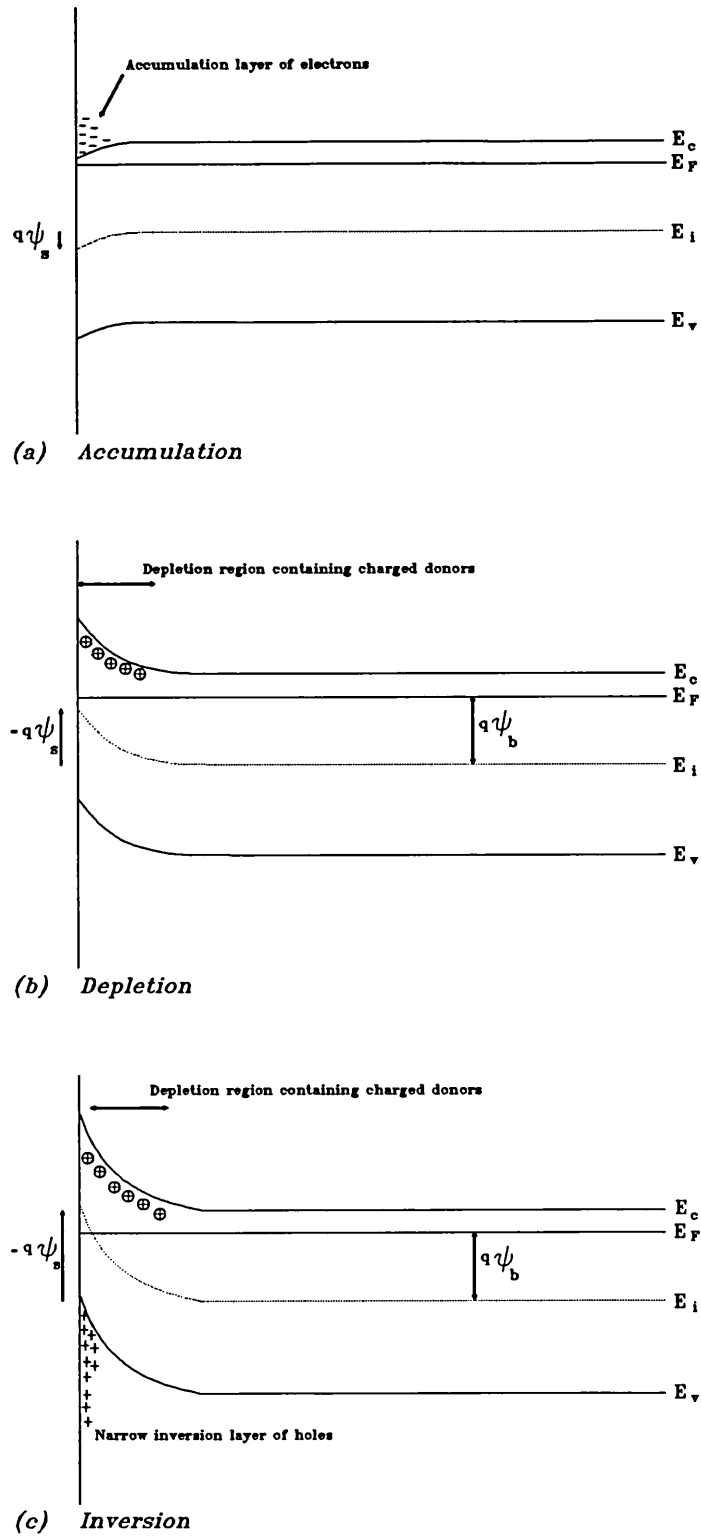


Fig. 14. Silicon band-diagram for the surface band-bending conditions in an MOS transistor, showing different charge distribution.

ψ_s is made still more negative, when $-\psi_s > 2\psi_b$, the surface hole concentration is equal to the bulk electron concentration which is referred to as the onset of strong inversion. The gate voltage necessary to bring about this condition is referred to as the threshold voltage, V_t .

In order to relate the strong inversion condition, $-\psi_s = 2\psi_b$ to a gate voltage, the whole MOS system must next be considered. The depletion layer width in an ideal MOS system when $-\psi_s < \psi_b$ can now be calculated. The one dimensional Poisson equation in the silicon is

$$\frac{d^2\psi(x)}{dx^2} = - \frac{\rho(x)}{\epsilon_s \epsilon_o} \quad (16)$$

where ϵ_s = permittivity of silicon
 ϵ_o = permittivity of free space
 $\rho(x)$ = charge density
 $\psi(x)$ = electrical potential

and $x=0$ at the silicon surface. In general, the charge density is given by

$$\rho(x) = q (N_D - N_A + p - n) \quad (17)$$

where N_D, N_A = donor, acceptor concentrations
 n, p = electron, hole concentrations

A solution of Poisson's equation using a Boltzmann distribution of carriers (Garrett and Brattain, 1955) is then somewhat unwieldy. So a uniformly doped, abrupt depletion region of width δ will be assumed to derive the main features. In this case the above expression simplifies to

$$\rho(x) = -qN_D \quad (18)$$

thus for an n-type substrate,

$$\frac{d^2\psi}{dx^2} = - \frac{qN_D}{\epsilon_s \epsilon_o} \quad (19)$$

Integrating twice gives

$$\frac{d\psi}{dx} = - \frac{qN_D x}{\epsilon_s \epsilon_o} + C_1 \quad (20)$$

and

$$\psi = - \frac{qN_D x^2}{2\epsilon_s \epsilon_o} + C_1 x + C_2 \quad (21)$$

The depletion region edge, $x = \delta$, is defined as the point where the electric field, $E = -d\psi/dx = 0$. The zero of potential, $\psi = 0$ is also defined there. Inserting these boundary conditions, we obtain for the constants of integration,

$$C_1 = \frac{qN_D \delta}{\epsilon_s \epsilon_o} \quad \text{and} \quad C_2 = - \frac{qN_D \delta^2}{2\epsilon_s \epsilon_o} \quad (22)$$

The variation of potential with distance from the silicon surface is thus

$$\psi = \frac{qN_D}{2\epsilon_s \epsilon_o} (x - \delta)^2 \quad (23)$$

Therefore, the surface potential at $x = 0$ is

$$\psi_s = \frac{qN_D\delta^2}{2\epsilon_s\epsilon_o} \quad (24)$$

and the depletion region width is given by

$$\delta = \left[\frac{2\epsilon_s\epsilon_o\psi_s}{qN_D} \right]^{\frac{1}{2}} \quad (25)$$

Once $-\psi_s = 2\psi_b$, inversion occurs, and the depletion region width remains constant. Any further charge induced by the applied gate voltage will be in a very narrow (inversion) layer, because the carrier density drops off exponentially with ψ on moving away from the interface. The threshold voltage, i.e. the gate voltage for the onset of inversion is thus given by adding the flat-band voltage, (15), the surface potential difference, $2\psi_b$ and the potential drop across the oxide due to the depletion layer charge, given by equations (24) and (25), thus

$$V_t = \phi_{ms} - \frac{Q_{ox}}{C_{ox}} + 2\psi_b + \frac{(4qN_D\epsilon_s\epsilon_o\psi_b)}{C_{ox}} \quad (26)$$

It is noted that the right-hand side contains only known, constant material parameters, and includes the oxide charges, given by equation (14).

The inversion layer charge for a particular gate voltage can now be calculated in order to determine its conductance properties. Referring to the p-channel transistor in Fig. 15, the inversion layer charge induced in the channel, at a distance x from the source is given by

$$Q_{ox}(x) = [V_{GS} - V_t - \psi_s(x)] C_{ox} \quad (27)$$

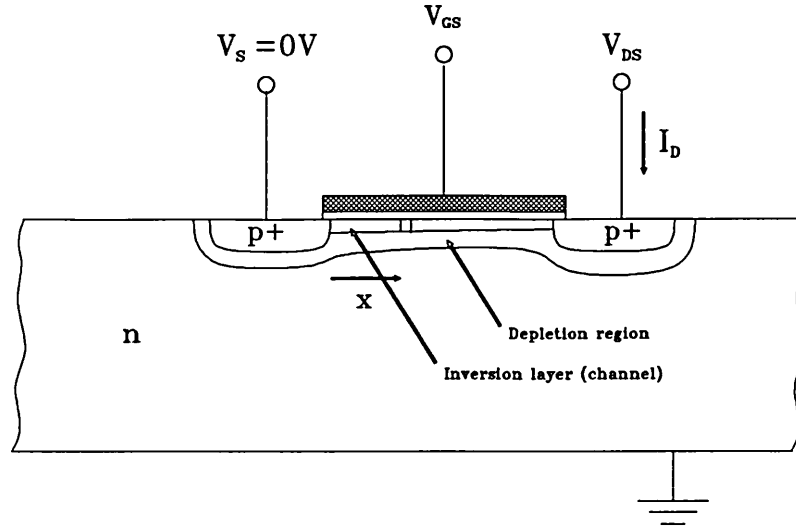


Fig. 15. Co-ordinates for triode equation derivation.

By definition, the electric field along the channel is

$$E_x = - \frac{d\psi_s(x)}{dx} \quad (28)$$

and the drain current, $I_D = -J_x bW$ where J_x is the current density, b is the channel depth, and W is the gate width (perpendicular to the paper in Fig. 15). Assuming the mobility is constant, and that carrier diffusion is insignificant,

$$J_x = nq\mu E_x$$

$$\therefore - \frac{I_D}{bW} = \frac{Q_{ox}(x)}{qb} q\mu \left[- \frac{d\psi_s(x)}{dx} \right]$$

$$I_D dx = \mu W C_{ox} [V_{GS} - V_t - \psi_s(x)] d\psi_s \quad (29)$$

Integrating from the source ($x = 0$) to drain, where $x = L$, the gate length

$$\begin{aligned}
 I_D \int_0^L dx &= \mu W C_{ox} \int_0^{V_{DS}} [V_{GS} - V_t - \psi_s(x)] d\psi_s \\
 I_D L &= \mu W C_{ox} \left[V_{GS} \psi_s - V_t \psi_s - \psi_s^2 \right]_0^{V_{DS}} \\
 I_D &= \mu \frac{W}{L} C_{ox} \left[(V_{GS} - V_t) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \quad (30)
 \end{aligned}$$

This is commonly known as the triode equation and is the basis for experimental determinations of V_t . If V_{DS} is small (0.1V), then the equation approximates to

$$\frac{I_D}{V_{DS}} = \mu \frac{W}{L} C_{ox} (V_{GS} - V_t) \quad (31)$$

where the left-hand side is the conductance. A plot of I_D vs V_{GS} with $V_{DS} = 0.1$ V should give a straight line, with gradient proportional to the mobility and x -intercept V_t . This method of measuring V_t is called the conductance method, and is particularly suitable for small geometry transistors because $V_{DS} \ll V_{GS}$. Ong (1986) discusses other methods.

2.3.2.3 The Sub-threshold Region

The sub-threshold region is part of an MOS device characteristic for gate voltages below V_t . In fact, I_D does not drop to zero at V_t , but decreases approximately exponentially. The gradient of this drop-off describes the details of how the transistor switches on, giving information about noise margins, minimum power supply voltage, etc.

In this work, the sub-threshold is of interest because it can give information about interface state density. As already discussed, a shift in V_t can be due to the sum of the change in both oxide and interface trapped charge. McWhorter and Winokur (1985) reported a means by which these two contributions could be separated in an MOS transistor, without resorting to special capacitor test-structures and capacitance voltage techniques.

They assumed that the interface states in the lower half of the silicon bandgap are donor-like and those in the upper half are acceptor-like. With reference to Fig. 16, it follows that when the bands are bent by ψ_b (Fig. 16a) neither type of states are charged (acceptors are above E_f and donors below). This condition is called the mid-gap gate bias, at which the gate voltage, V_{mg} and drain current, I_{mg} are defined. As the gate voltage is increased (negatively) in Fig. 16b, more states become ionised and hence positively charged, requiring a progressively larger shift in V_{GS} to counteract them. The shift in V_{GS} is a maximum when all donors are ionised (Fig. 16c), at the onset of strong inversion when $V_{GS} = V_t$ and any further increase in interface charge is swamped by the inversion layer charge.

After an irradiation experiment in which both oxide trapped charge and interface state density increase, the subthreshold plot is changed as shown in Fig. 17. The gate voltage shift due to oxide trapped charges is independent of V_{GS} . Furthermore, in the mid-gap condition, interface states are uncharged, so the shift due to oxide trapped charges is

$$\Delta V_{ot} = V_{mg2} - V_{mg1} \quad (32)$$

When $V_{GS} = V_t$, interface states are fully charged, so for a shift in threshold voltage,

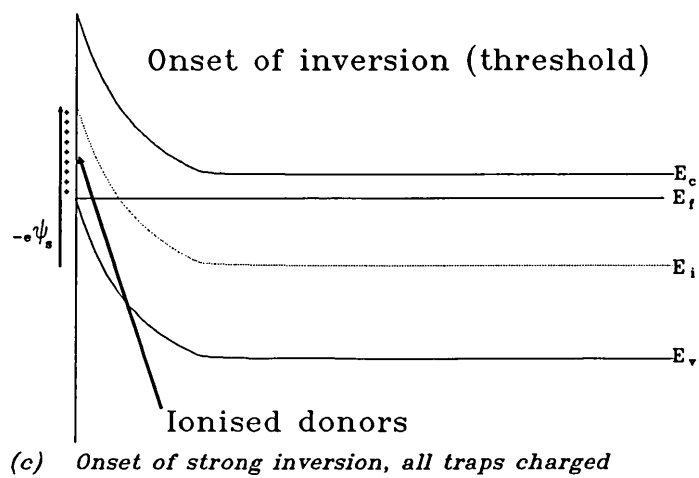
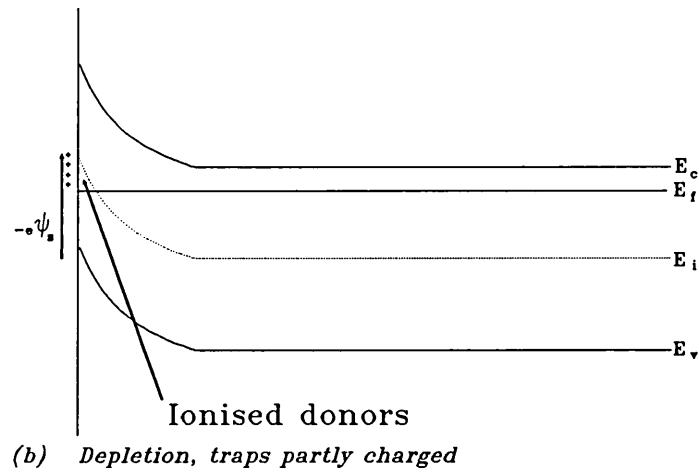
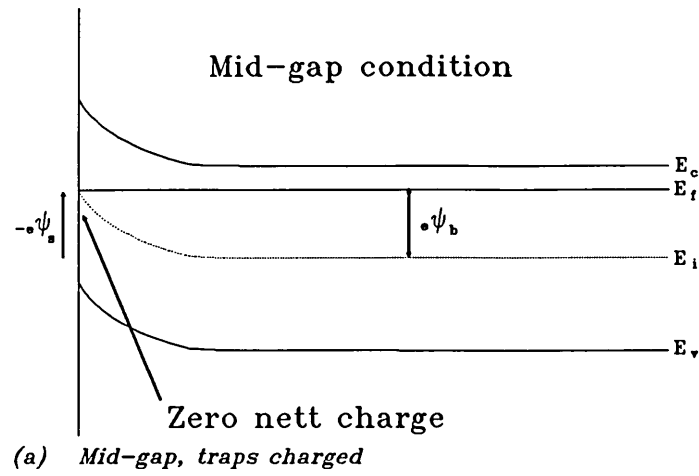


Fig. 16. Charge state of interface traps as a function of the surface potential, ψ_s . States in the upper half of the band-gap are donor-like and become charged when above the Fermi-level

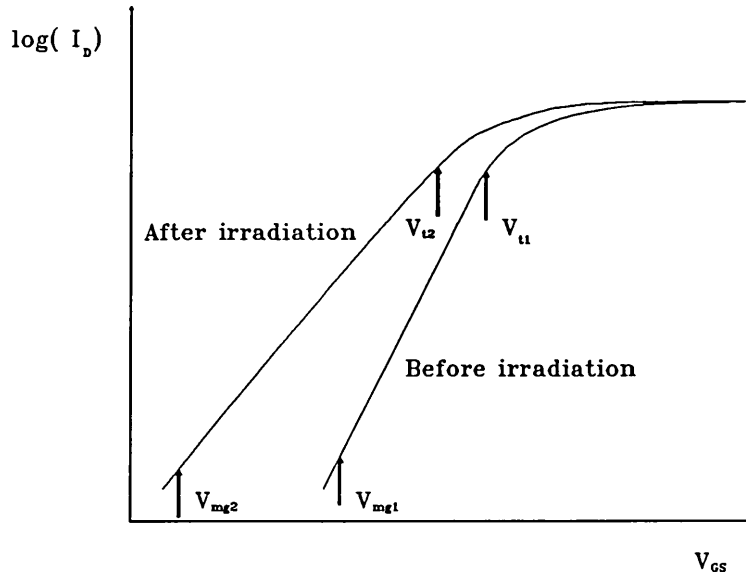


Fig. 17. Effect of an increase in oxide trapped charge and interface state density on the MOS transistor subthreshold characteristic.

$$\Delta V_t = V_{t2} - V_{t1} \quad (33)$$

the contribution due to interface states must be

$$\Delta V_{it} = \Delta V_t - \Delta V_{ot} \quad (34)$$

and hence the two contributions to ΔV_t are separated into $\Delta V_t = \Delta V_{ot} + \Delta V_{it}$. For each of these voltage shifts, the effective charge number density (positioned at the Si-SiO₂ interface) can be calculated via

$$\Delta N_{ox} = \Delta V_t \frac{C_{ox}}{q} \quad (35)$$

Measurement of V_t has already been discussed. V_{mg1} and V_{mg2} can be determined using a theoretical expression for I_{DS} as a function of surface potential, ψ_s , due to Fichtner and Pötzl (1979), who calculated the pure diffusion current along a weakly inverted channel:

$$I_D = \frac{W}{L} \mu \beta \left[\frac{\epsilon_s \epsilon_o k T n_i}{2} \right]^{\frac{1}{2}} \frac{\beta \psi_s}{e} (\beta \psi_s)^{-\frac{1}{2}} \left[1 - e^{-\beta V_{DS}} \right] \quad (36)$$

where W, L = gate width, length,
 μ = mobility,
 n_i = intrinsic carrier concentration,
 β = q/kT .

The surface potential at mid-gap is simply given by the bulk Fermi level, $\psi_b = (kT/e) \ln(n_i/N_D)$ (Sze, 1981, p27). Thus, I_{mg} is calculable because all the parameters are known or can be measured (e.g. μ). V_{mg} can then be read from the sub-threshold plot of I_D vs V_{GS} . In practice, $I_{mg} \sim 0.1$ pA, which may be below the level of drain-source leakage current, but the graph is essentially linear, so an extrapolation is easily made. The validity of this approach has been confirmed by Winokur *et al* (1984) who compared the two components of ΔV_t due to ^{60}Co γ -rays in MOS transistors with the more established techniques using MOS capacitors. They found a good quantitative correlation over a range of different samples with varied radiation hardness.

2.3.3 Electron Beam Irradiation Damage of MOS transistors.

Damage to MOS transistors due to ionising radiation was first observed in 1964 by Hughes and Giroux. They noted a large decrease in transconductance of both PMOS and NMOS transistors intended for space

satellites, which were tested using ^{60}Co γ -radiation. Positive charge stored in the gate oxide was reported as the cause after Szedon and Sandor (1965) observed a shift in capacitance voltage curves due to γ -radiation. Since then a very large body of work has been built up in the study of radiation hardness, notably Mitchell (1967), and more recently Smeltzer and Schnable (1988). In addition many articles on this subject have been published in the IEEE Transactions on Nuclear Sciences.

Studies of electron beam damage have also been made due to interest in electron beam lithography, although this usually involves rather high primary beam energies. In this case, high temperature anneals ($> 450^\circ\text{C}$) are required to remove trapped oxide charge, although neutral traps may remain. These lead to long term instabilities in threshold voltage due to hot electron trapping in the finished devices (Shimaya *et al*, 1983).

One of the first reports of damage to MOS transistors due to SEM examination was Keery *et al* (1976). They studied the change in electrical characteristics of a variety of devices, and in particular, observed a threshold voltage shift in PMOS transistors. They measured no threshold voltage shift below 15 keV, and applied the Everhart-Hoff depth-dose function to the layer structure of their devices. They argued that the apparent lack of threshold shift was due to non-penetration of electrons to the gate oxide. Child *et al* (1976) observed V_t shifts at 7.5 keV but not at 1.5 keV, but on a decidedly different device structure. It thus appeared that at sufficiently low beam energy, electron microscopy was non-destructive.

More careful measurements were made by Nakamae *et al* (1980) of the linear shift of V_t with dose between 5 and 18 keV. They used a positive gate bias (4.0 V) during irradiation, and defined V_t as the gate voltage for

which $I_D = 1 \mu\text{A}$ with $V_{DS} = 5 \text{ V}$. By assuming that

$$\Delta V_t = C E_b f_D D \quad (37)$$

where C = a constant to account for backscattering,
 f_D = the energy fraction absorbed by the gate oxide,
 D = electron dose (Ccm^{-2}),

and $C \neq C(E_b)$, the variation of f_D with E_b was determined for that energy range and device structure. Their results are reproduced in Fig. 18. Two effects are apparent. Firstly, the Everhart-Hoff calculation cuts off too sharply and in fact electrons penetrate more deeply than predicted. The authors referred to this as range straggling, but did not suggest an explanation for the disagreement. Secondly, the point at 5 keV is discontinuous with the rest of the curve. This was attributed to the

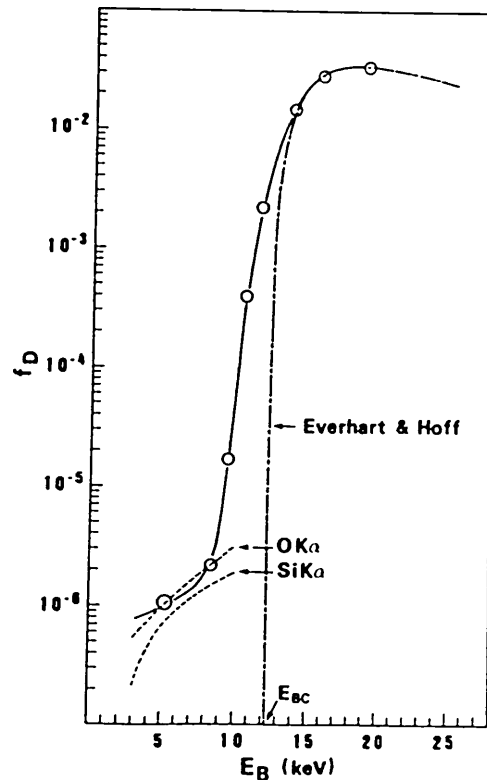


Fig. 18. Results of Nakamae et al (1981) for the fraction of energy absorbed in the gate oxide vs E_b .

generation of secondary X-rays in the upper layers, which penetrate much deeper than the primary electrons. In particular, an estimate of damage due to the oxygen and silicon K_{α} peaks was made as shown in the figure.

By this time it had become generally accepted that high energy SEM examination was an essentially destructive technique (Wolfgang, 1983). However, as voltage contrast techniques became more popular, concern arose about whether these methods were also destructive, despite the lower beam energies employed. Passivated devices were examined using E_b sufficient to generate an electron beam induced conductive path through the passivation layer to metal tracks beneath. Charging was then eliminated, and the emitted electron energy was correlated with the electrical potential of the metal track. The alternative was to use very low E_b at the crossover point at which the emitted electron coefficient is unity, so charging doesn't occur. AC circuit signals can then be sensed by capacitive coupling.

Miyoshi *et al* (1982) presented a study of the effects of voltage contrast testing on short channel MOS transistor characteristics. They irradiated p- and n-channel devices at 1, 2 and 3 keV with all pins grounded. V_t was defined in the same way as Nakamae *et al* (1981) (i.e. $V_{GS} = V_t$ when $I_D = 1 \mu A$ and $V_{DS} = 5 V$). Linear shifts in V_t with dose were caused by such low energies at which electrons did not penetrate. This was ascribed to generation of characteristic X-rays.

Görlich and Kubalek (1983, 1985) irradiated NMOS devices with the pins grounded at 1, 5 and 10 keV. V_t was measured by the intercept of V_{GS} vs $I_D^{1/2}$ with $V_{DS} = 4 V$ (i.e. the device is in saturation). A shift was observed at 1 keV, at which electrons could not penetrate to the gate oxide. Again, this was attributed to secondary X-rays. A novel result was

obtained using a special window-scan mode of the SEM which blanked the beam at the location of transistor gates. Even this did not eliminate damage completely. However, using low E_b reduced damage by several orders of magnitude, and the window-scan mode decreased it still further. The practicalities of this mode do seem somewhat questionable, however.

Another study of e-beam damage was made by Ranasinghe *et al* (1987), who observed strongly non-linear effects in the variation of threshold shift with time of irradiation. Their ΔV_t measurements were made during irradiation, and a feedback arrangement used to apply a gate voltage in order to maintain $I_D = 1 \mu A$ with $V_{DS} = 0.1 V$. This, however, means that the gate voltage varies during the experiment (as V_t shifts) and it is well known from radiation hardness testing that the gate bias has a strong effect on oxide charge storage (e.g. Mitchell, 1967). The authors did, however, prove conclusively that X-ray generation was occurring, by using an X-ray sensitive film above the sample. In addition a windowless detector was placed near the sample to verify X-ray production, and several counts were observed. This was tentatively attributed to the oxygen K_α peak at $\sim 500 eV$.

A more comprehensive study using the same measurement methods as Ranasinghe *et al* was made in ALVEY project ALV/VLSI/104 (Jones 1989). The shift in threshold voltage for E_b between 3 and 0.5 keV was measured as a function of dose in order to define safe operating regimes for device examination.

A more quantitative attempt at understanding ΔV_t phenomenon was made by Reiners *et al* (1985). ΔV_t was measured over a wide E_b range for devices which had several layers above the gate oxide, and all pins grounded. The

method of ΔV_t measurement was not given. They found that plots of ΔV_t vs dose were linear at first, and tended to a saturation value for very high doses. The whole of this curve was fitted to a model adapted from that of Mitchell (1967), which describes the build-up of oxide trapped charge with dose:

$$\frac{\Delta V_t}{\Delta V_{Tsat}} = 1 + \frac{A_2}{gt} \left[\exp \frac{gt}{A_1} - \exp \left[\frac{gt}{A_2} - \frac{gt}{A_1} \right] \right] \quad (38)$$

where ΔV_{Tsat} = saturation value of ΔV_T ,
 A_1, A_2 = parameters,
 g = carrier density generation rate of electron-hole pairs,
 t = time.

The same values of A_1 and A_2 were used at each E_b and gt was determined from the necessary shift of the curve in equation (38) along the time axis to fit the experimental data. The fraction of E_b deposited in the gate oxide, f_D was then calculated from

$$gt = A_3 f_D E_b D \quad (39)$$

where A_3 depends on transistor geometry. This can be compared to equation (37) of Nakamae *et al* (1981). The resulting plot of f_D vs E_b is reproduced in Fig. 19. A large discrepancy is again apparent in comparison with the Everhart-Hoff theory. In the case of the solid line this could be accentuated by the difficulty in calculating exactly for an additional Al layer which extended across only part of the gate oxide of their test transistors. The distinction between deep electron penetration and X-ray induced shifts is not clear for either transistor type. The Bremsstrahlung was thought to be the dominant source of X-rays, and a rough calculation was presented to verify this. The following simplifying assumptions were made:

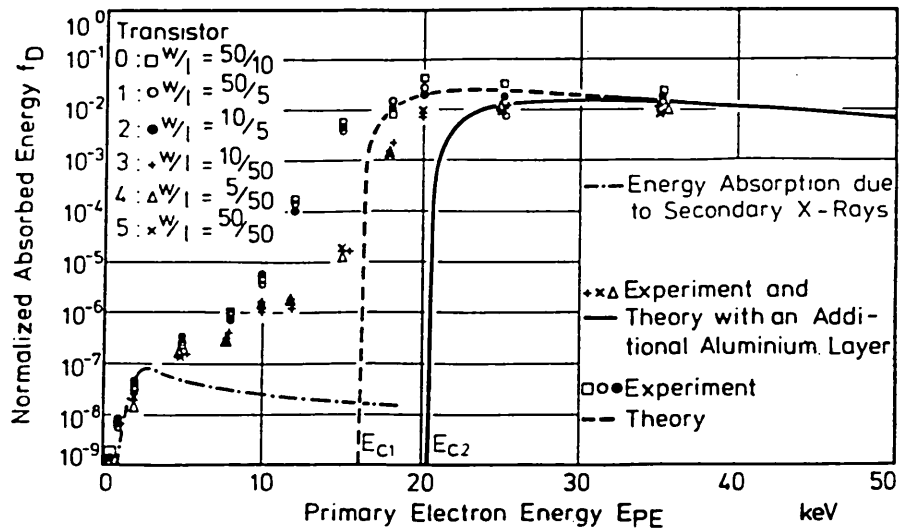


Fig. 19. Fraction of energy deposited in the gate oxide vs beam energy, after Reiners *et al* (1985).

- (i) X-rays generated at the surface
- (ii) The generated intensity $\propto E_b^2$
- (iii) The Bremsstrahlung energy was taken as the maximum of the spectrum which is at $(2/3)E_b$
- (iv) An exponential absorption law.

The resulting curve did, indeed fit at very low E_b (Fig. 19), although the origin of a peak in the graph (at ~ 3 keV) is not clear.

In summarising the previous work, the main features for future work are:

- (i) ΔV_t should be precisely measured with due regard to the whole device characteristic.
- (ii) The thickness and composition of layers above the gate oxide are of critical importance in comparing different data.

Part of this work has already been published (Russell *et al*, 1989)

2.4 DEFECTS IN INTEGRATED CIRCUITS

In this section, a short account of the layout of IC's and their construction will be made. Existing test methods and the types of defects encountered will then be reviewed.

2.4.1 IC Fabrication and Design

In order to investigate defects in integrated circuits it is necessary to understand something of the methods by which IC's are designed and made. All circuit components are fabricated in a thin ($< 10 \mu\text{m}$) layer on the surface of a thicker ($\sim 0.5 \text{ mm}$) supporting substrate – usually of silicon, although sapphire and gallium arsenide are also used at the present time. To make the actual components of a chip, several techniques are necessary – oxidation, ion implantation, chemical vapour deposition, metallisation, dopant diffusion, etching, etc. Photolithography converts these "blanket" processes into the geometrical shapes necessary to make circuits. In a typical process, as many as twenty separate masking steps might be necessary. The details of processing are discussed in great detail in the text by Sze (1983).

For the image processing techniques of this work the overall pattern of devices in a finished IC is most relevant, and is influenced by its final application. Computer-aided design is almost universal for the development of contemporary integrated circuits. Several types of design methodology can be identified (Trimberger, 1982), in order of increasing design cost,

Uncommitted logic array

These circuits consist of a regular array of logic gates on a die. Their function is defined only by the final metallisation stage, by connecting up the appropriate components. A circuit with a new function could be shipped in weeks. Circuit structure consists of regular cells covered by irregular metallisation.

Programmable logic array

In this case, a metallisation structure is rigidly defined, and logic gates can be invoked from a block of AND gates on the left of the chip, and OR gates on the right, completing the circuit between input and output and defining the circuit function. These circuits consist of regular metallisation over an array of logic gates.

Standard-cell

This is used more commonly for application-specific IC's (ASIC's). Logic is implemented from library of standard modules. These circuits often consist of alternating rows of logic gates and interconnections.

Standard-floorplan

This is a method of defining a circuit in terms of modules joined by a defined interconnection scheme. It is best for microprocessors, and leads to a block-like circuit.

Full-custom

This is used only for high volume circuits such as microprocessors and those containing analogue parts in which performance can be optimised at the expense of increased design time. Although some parts will be standard-cells, such as pad-driver circuits, the overall layout will be

heavily optimised to minimise interconnect distances to improve speed, decrease silicon real estate, etc.

The above categories are neither exhaustive nor exact, but emphasise the very different types of structures which may be encountered, from perfectly periodic CCD image sensors to the irregular structure of an ASIC.

2.4.2 Failures and defects

During the manufacture of an IC, inspections are made at various stages to check that processing of each batch has been satisfactory before continuing with the next stage. This often takes the form of a quick light microscope inspection of a few seconds to check for gross processing defects. Once the chip has been completed, electrical functional tests are made. A pattern generator defines a series of input states to drive the chip, while a logic analyser checks the outputs for correct functionality. This automatic test equipment (ATE) has risen to a high degree of complexity and cost, but has been outstripped by IC developments, and cannot fully test the most complex sequential VLSI circuits being produced today. But, by skilful design of test sequences to give good "fault coverage", and incorporating "design for testability", testing can be made adequate. In any case, it is the only quick means available at present to test device functionality.

After their final test and packaging, the failure rate of IC's is found to obey the characteristic "bath-tub curve" (Fig. 20). A number of circuits fail early on. Then, a long period follows with only occasional failures. The final stage is after many tens of years, and hence beyond the useful life of typical systems. The occurrence of infant mortalities suggests that circuits

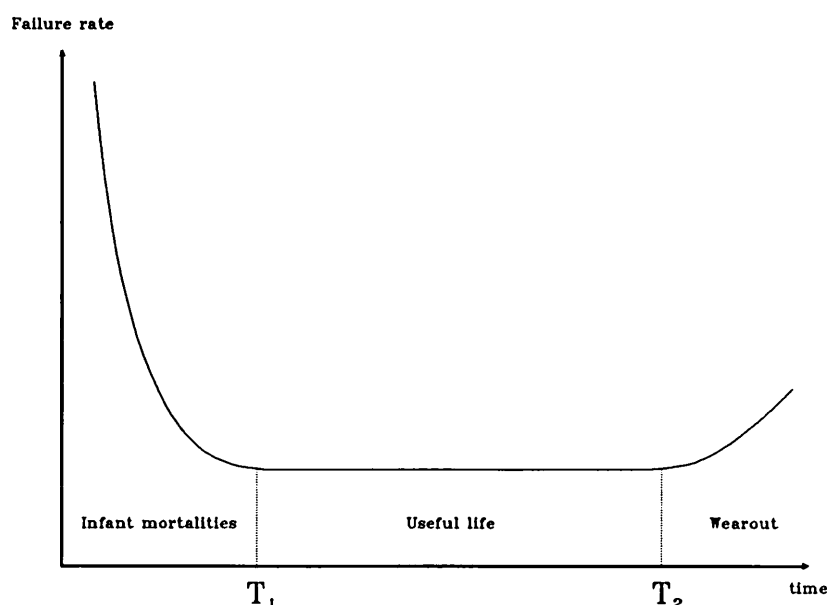


Fig. 20. Universal bath-tub curve of failure rate vs. time for integrated circuits.

passing functional tests may still have marginal defects. For example, if a metal track contained a void which reduced its width to 1/4 of its design size, the circuit might work for a while, but current crowding and heating would soon cause failure. These infant mortalities tend to be more numerous in state of the art technologies. (Pantic, 1986), and are of great interest as their cause provides a means to improve yield (the number of working devices per device manufactured). For special applications in which high reliability (low failure rate) is a necessity, circuits can be powered up for a time, T_1 , and re-tested. The functional ones will then have a lower failure rate. This is called "burn-in", and is usually done at elevated temperatures ($\sim 125^\circ\text{C}$) to reduce T_1 , as most failure mechanisms are thermally activated. It is, however, expensive. During the useful life period, a few failures occur, and they are often analysed to determine if they were extrinsic (application induced) or intrinsic failures of the circuit.

Failure mode	-	nature of the device malfunction e.g. short/open circuit, leakage, etc.
Failure defect	-	the object causing malfunction e.g. microcrack, growth, etc.
Failure mechanism	-	the phenomenon that produced the defect e.g. corrosion, dielectric breakdown, etc.
Failure cause	-	the action which precipitated failure e.g. overheating, poor design, etc

Table 1. Failure analysis terminology.

So, IC defects are of interest at all stages of an IC's life from manufacture through testing, to use in a system. "Failure analysis" of such circuits necessitates a structured approach using a variety of microscopical and analytical techniques (Richards and Footner, 1983). They specified a useful terminology as shown in table 1. One stage in failure analysis is defect location. In VLSI circuits containing perhaps 10^6 transistors, manual defect location is very time-consuming. In this work, it was intended to use an image processing computer to aid this procedure, as will be discussed in section 2.5. First, however, it is appropriate to mention something of the defects themselves, in addition to those described already in section 2.2.2 which were observable using EBIC.

Some idea of the proportions in which various failure modes occur can be derived from the experiences of Schädel (1983) and Fantini (1984). Fig. 21 shows the proportional incidence of failure modes in large numbers of failure analyses. The classifications are somewhat idealised, as they depend on the device types which were analysed. Metallisation is obviously very prone to defects, as are the extremely thin gate oxides used in MOS transistors. Electrical overstress, contamination, pattern (photolithographic) faults and substrate defects were also observed.

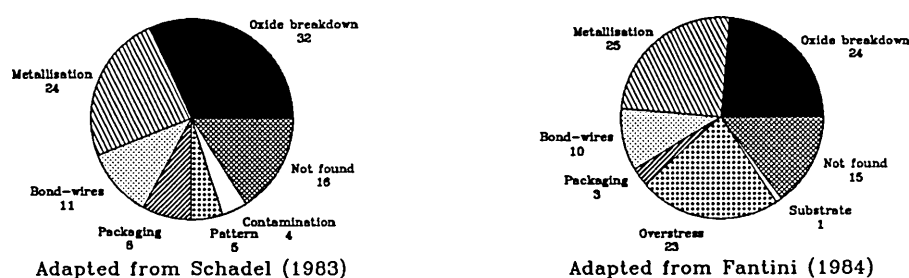


Fig. 21. Proportional occurrence of various failure mechanisms in a large number of failure analyses.

Material defects such as dislocations in the silicon substrate can lead to excess leakage currents when they intersect pn-junction depletion regions (Jastrzebski, 1982). This increases device power consumption, and is undesirable. Their presence is usually determined using part-processed test wafers, or selected layer removal and etching, or even TEM. The electrical activity of such defects can be confirmed by EBIC (Dishman *et al*, 1979).

Processing defects whereby voids or irregularities in any layer may occur usually lead to hard failures on testing. They may also account for many infant mortalities. Contamination during manufacture is often of human origin (Thomas and Calabrese, 1985). It can physically upset devices in the case of large particulates, but residues (e.g. of spittle) can also remain and cause corrosion during use of a chip, when activated by the ingress of moisture (Schnable *et al*, 1979). This is particularly true of aluminium metal tracks in the presence of chloride salts. Corrosion may also be initiated at voids in the passivation oxide overcoat of the die – a processing defect.

In summary, it is not possible to describe every defect type in integrated circuits, but they can be attributed to either processing defects or user induced failures. In all cases defects are accompanied by some sort of

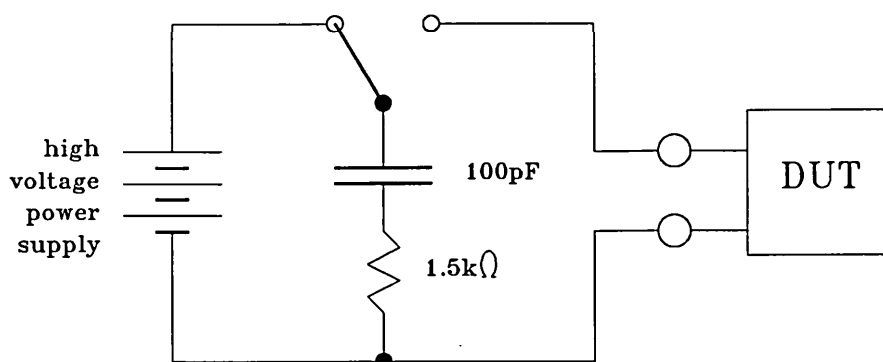


Fig. 22. Experimental arrangement used for ESD testing of IC's according to the human body model.

irregularity in the circuit. If a suitable microscopic technique is used then the defect may be made visible. Defect location in VLSI circuits is then a problem of examining a potentially huge number of images to ascertain the defect position, perhaps with a variety of microscopical techniques.

2.4.3 Electrostatic discharge damage

Triboelectric charging of objects and people with static electricity is well known, and simple processes such as walking across a carpet can induce potentials of 15 kV on a human (Bhar and McMahon, 1983). More important than this is that humans are insensitive to electrostatic discharge (ESD) when charged to less than about 3 kV (Avery, 1984), but semiconductor devices are at risk at lower potentials even though pulse durations are very short ($\approx 1 \mu\text{s}$).

The "human body model" approximates an individual as a 1.5 kΩ (skin) resistance in series with a charged 100 pF (body) capacitor (Fig. 22) which is suddenly discharged through the device under test (DUT). These component values are supposed to mimic a standing person, and vary in

practice. It is, however, the model used for electrostatic discharge (ESD) susceptibility testing to certain standards (such as MIL STD 883). There are three failure mechanisms of IC's due to ESD:

Oxide puncture

Silicon dioxide has a dielectric breakdown strength of $\approx 10^7 \text{ Vcm}^{-1}$, so a gate oxide of 40 nm will only sustain 40 V, or less in the presence of defects. Dielectric breakdown punctures the oxide, leaving a resistive short of electrode material

Metallisation melting

If excessive currents flow in metal tracks the resulting Joule heating can cause melting. This failure mechanism requires the most energy.

Junction burnout

For sufficiently high energy pulses, the junction breaks down destructively, leaving a resistive short circuit, as discussed later.

In order to eliminate such failure mechanisms protection circuitry that will conduct ESD pulses safely away without damaging the circuit is necessary. The most susceptible example is MOS IC inputs which lead directly to a thin gate oxide that must be protected from overvoltages. In Fig. 23 this is achieved using a diffused resistor, R , which limits the pulse rise time, followed by diodes to each power supply rail. D_1 will become forward biased for positive pulses, and clamp the voltage seen by the input gate to one diode drop (0.7 V) above V_{DD} . D_2 will clamp it to one diode drop below V_{SS} for negative pulses. The problem with such a scheme is that the protection circuit itself may eventually become damaged, resulting in increased leakage currents at the affected input, and eventual failure. Thus, MOS IC's may also fail by junction breakdown, as well as oxide puncture.

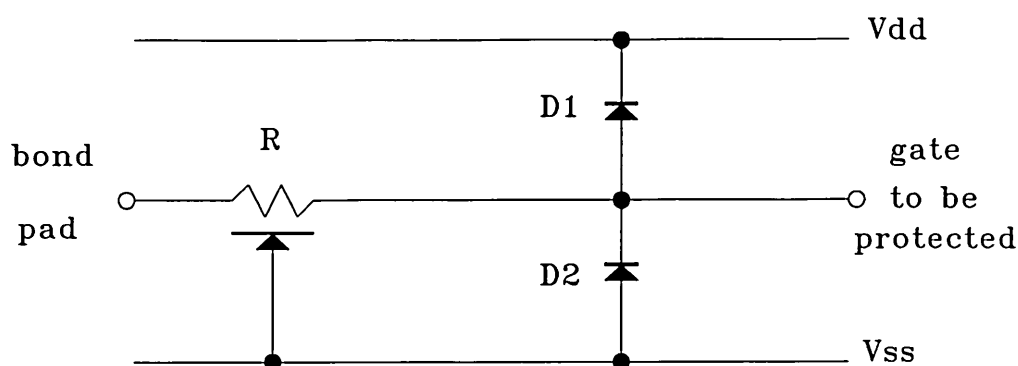


Fig. 23. A simple ESD input protection circuit.

If a pn-junction such as that in a protection diode is reverse biased, it will pass a small leakage current due to thermal carrier generation in the depletion region. The applied voltage is mostly dropped here, so as the voltage increases, the electric field becomes more intense, until the thermally generated carriers are accelerated to energies of more than E_g , resulting in more carrier generation. This is called avalanche multiplication, and is accompanied by a sharp increase in current. If sufficient energy is dissipated at the junction second breakdown occurs (Ferry and Dougal, 1966). This is due to local heating of the silicon which goes intrinsic, thus having a negative temperature coefficient of resistance, resulting in thermal runaway. Damage is usually localised to inhomogeneities in the junction (Smith *et al*, 1973), and if the current is not limited, can result in local melting of silicon (Thomson and Wilkinson, (1967), which may leave a polycrystalline, resistive short across the junction. In less serious cases, melting does not occur, but high temperatures can result in dopant redistributions and thermomigration of aluminium.

2.5 IMAGE PROCESSING

The use of image processing on pictures obtained from SEM's is becoming relatively common. Image processing is an immense subject area, and no attempt at a review will be made here. A useful introductory text is Baxes (1980), more advanced ones are Gonzalez and Wintz (1977), and Rosenfeld and Kak (1982). Aspects of relevance to scanning microscopy were reviewed by Jones and Smith, (1978).

Most systems used in conjunction with SEM's at present are primarily for image enhancement but in addition may also be used for image analysis. Image enhancement can vary from simple signal averaging, to contrast improvement or image sharpening techniques. Image analysis, in which quantitative information is derived from an image, is often used to examine microstructures, automatically picking out phases and measuring relative proportions etc.

For the present purposes, the problem is to locate defects in VLSI circuits. These circuits are so large, and contain so many circuit elements that manual, visual inspection is not possible. What is needed is a method whereby an image processor can be used as an aid to locating the few defects in such IC's. Despite the importance of device testing for VLSI, and the promise which image processing has for defect location, very little work has been reported in this area.

2.5.1 Types of Image Processing

An image can be defined as an intensity, $f(x,y)$ where f , x and y are all quantised. Once an image is digitised, f defines the grey level, while x and y define the pixel co-ordinate following the convention of Fig. 24.

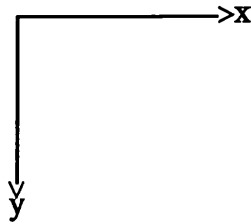


Fig. 24. Pixel co-ordinate convention.

Three types of image processing can be identified, each taking the image $f(x,y)$ and outputting a new image, $g(x,y)$:

(i) Point processing:

$$g(x,y) = A(f) f(x,y) \quad (40)$$

so the pixel grey level is modified in magnitude only. This modifies the image histogram, which is a plot of the frequency of occurrence of each grey level over all pixels in an image. The histogram is very important, as it characterises the brightness levels over the whole image, showing if it is too light or dark, or if any brightness levels dominate.

(ii) Local Point processing:

$$g(x,y) = \sum_{x'=-i}^{+i} \sum_{y'=-i}^{+i} B(x',y') f(x+x',y+y') \quad (41)$$

where i is a small integer, typically 1 or 2, and nearly always < 7 (e.g. for $i = 1$, B would be a 3×3 matrix). Thus each pixel assumes a new value given by weighted contributions from its nearest neighbours. For example, if the matrix B is given by

$$\begin{array}{ccc} -1 & 0 & 1 \\ -1 & 0 & 1 \\ -1 & 0 & 1 \end{array}$$

it is sensitive to vertical detail over distances of order one pixel, so acting as a vertical edge detector. To smooth a very noisy image, the matrix

$$\begin{array}{ccc} 1/9 & 1/9 & 1/9 \\ 1/9 & 1/9 & 1/9 \\ 1/9 & 1/9 & 1/9 \end{array}$$

will work, although this tends to remove fine detail. A better solution is a 'median filter' in which

$$\begin{aligned} B &= 1 && \text{if } f(x,y) \text{ is the median value of the pixels in the range} \\ &&& x-i \rightarrow x+i, y-i \rightarrow y+i \\ B &= 0 && \text{otherwise} \end{aligned}$$

In this case, any noise spikes are removed completely, while the image retains its original sharpness much better. Many other variants are possible for different purposes.

(iii) Frame processing is the most general (and time consuming) and can be defined by

$$g(x,y) = \sum_{\text{all } x'} \sum_{\text{all } y'} C(x',y') f(x,y) \quad (42)$$

where x' and y' vary over the whole frame range. A well known example is the Fourier transform, which converts the image to frequency space.

All of the definitions above assumed just one input frame for simplicity, but of course in general many images may be combined to form the output image.

2.5.2 FFT Spatial Filtering

Since the Fourier transform was first postulated early in the last century by J. B. Joseph, Baron de Fourier, it has found use in many fields. For practical applications, the discovery of the fast Fourier transform (FFT) algorithm (Cooley and Tukey, 1965) made it a usable tool rather than a mathematical convenience. With the more recent advent of digital computers, and specialised hardware, it has become practical for two dimensional calculations on images.

The continuous Fourier transform, $F(u)$ in the frequency domain, of a function, $f(x)$ in the temporal domain, is well known and can be defined by a pair of functions,

$$F [f(x)] = F(u) = \int_{-\infty}^{+\infty} f(x) e^{-2\pi j u x} dx \quad (43a)$$

$$F^{-1} [F(u)] = f(x) = \int_{-\infty}^{+\infty} F(u) e^{+2\pi j u x} du \quad (43b)$$

where x = displacement,
 u = spatial frequency,
 j = $(-1)^{\frac{1}{2}}$

and italic F is used to denote Fourier transformation. In dealing with digital images, the concern is with an intensity function sampled on an $N \times N$ grid. This is accommodated by re-defining $f(x,y)$ by

$$f(x,y) = f(x_0 + x\Delta x, y_0 + y\Delta y) \quad (44)$$

where $\Delta x, \Delta y$ = sampling increments
 x_0, y_0 = x and y offsets

so that now $x, y = 0, 1, \dots, N-1$. The two-dimensional, discrete Fourier transform pair can then be defined as:

$$F(u, v) = \frac{1}{N} \sum_{x=0}^{N-1} \sum_{y=0}^{N-1} f(x, y) e^{-2\pi j(ux+vy)/N} \quad (45a)$$

$$f(x, y) = \frac{1}{N} \sum_{u=0}^{N-1} \sum_{v=0}^{N-1} F(u, v) e^{+2\pi j(ux+vy)/N} \quad (45b)$$

where all of x, y, u, v vary from 0 to $N-1$. We also note that the sampling increments in frequency space are given by

$$\Delta u = 1 / (N\Delta x) \quad (46)$$

Also, both $f(x,y)$ and $F(u,v)$ are periodic so that

$$f(x, y) = f(x + aN, y + bN) \quad (47a)$$

$$F(u, v) = F(u + aN, v + bN) \quad (47b)$$

where a and b are integers.

However, the function $f(x,y)$ is fully recovered using just one period of $F(u,v)$. This is the reason for edge effects in reconstructed images, as sharp transitions near the picture edges cause "ringing".

In an image processor, at first sight $F(u,v)$ requires twice as much memory to store as $f(x,y)$ because both real and imaginary parts of F are generated from the real image, f . However, as the original image contains no imaginary component, an important symmetry condition exists because $f^* = f$. Hence,

$$\begin{aligned}
 F^*(u,v) &= \left[\frac{1}{N} \sum_{x=0}^{N-1} \sum_{y=0}^{N-1} f(x,y) e^{-2\pi j(ux+vy)/N} \right]^* \\
 &= \frac{1}{N} \sum_{x=0}^{N-1} \sum_{y=0}^{N-1} f(x,y) e^{-2\pi j(-ux-vy)/N} \\
 &= F(-u,-v)
 \end{aligned} \tag{48}$$

The corollary of this is that although we could store real and imaginary parts of F (2×512^2 numbers), only half of them are necessary (e.g. $u, v > 0$) while the rest can be reconstructed through the relation $F(-u,-v) = F^*(u,v)$. Hence, as seems reasonable, f and F are in fact described by the same amount of information.

The raw data, which represents the function, $F(u,v)$ is not immediately useful for visualisation and it is usual to calculate the function, $\log(1+|F|^2)$. This looks similar to the familiar Fraunhofer diffraction pattern or power

spectrum. The logarithm is taken to emphasise detail at high spatial frequencies, while $|F|^2$ contains information only about the amplitude of each frequency component. Phase information is eliminated, but this is not a significant problem, as a change in phase of F simply corresponds to a linear shift in f , which is of minor importance, as exact location of features is not required. One further change is necessary to get the familiar pattern because as defined, the origin of the power spectrum, $(0,0)$ is in a corner of the image, and must be translated near the centre for a symmetrical picture. This is entirely justified because of equations (47a,b), which mean that f and F are fully defined by any $N \times N$ section of temporal or frequency space which may be chosen.

A further important result concerns the central bright spot of the power spectrum. Equation 44a with $u, v = 0$ gives

$$\begin{aligned}
 F(0,0) &= \frac{1}{N} \sum_{x=0}^{N-1} \sum_{y=0}^{N-1} f(x,y) \\
 &= N \langle f(x,y) \rangle
 \end{aligned}
 \tag{49}$$

i.e. the zero-order peak is equal to the average grey-level of the original image (to within a constant).

Spatial filtering is the process whereby particular spatial frequencies represented by their co-ordinates in the diffraction pattern are removed (usually by setting them to zero). On performing the inverse transform, an image is reconstructed without those spatial frequencies. This was first carried out using an optical bench, and has long been used to reconstruct the periodic components of noisy images to see the underlying pattern (Klug & De Rosier, 1966). It has also been used to suppress periodic detail to

emphasise defects, such as those in IC photomasks (Watkins, 1969). An early digital system was described by Yokota *et al* (1981). They used it to suppress non-periodic noise in high resolution lattice images from the TEM. These techniques are used in many other fields, and increased in popularity as computers became more powerful. The classic example is the removal of periodic noise from space probe images. Such applications generally require interactive optimisation for best results (Gonzalez and Wintz, 1981)

2.5.3 Defect Location by Image Processing

Traditionally, inspection of integrated circuits has been carried out manually. That is, optical microscopes were used to visually scan a circuit in order to locate defective regions. One of the first uses of digital image processing in this field was as a means to align finished devices for wire bonding in their packages (Kashioka *et al*, 1976). They used local pattern matching techniques on binary images to identify the circuit position. A logical extension (Baird, 1978). was to use computer vision for inspection of discrete devices for correct packaging and die integrity. More recently, Pau (1985) described a system using a laser scanning microscope for inspection during manufacture of GaAs small-scale integrated circuits.

An early application of an SEM-based image processor was Propst *et al* (1984). They used a system based on three minicomputers,

- (i) to exercise the device under test (DUT),
- (ii) to control the digital scan and image acquisition,
- (iii) for offline image processing.

The main imaging modes were EBIC and voltage contrast, the technique described in section 2.2.2. One particular use of image processing was to subtract the image of a device with all pins grounded from a VC image of the same area. This aided image interpretation by removing topographic contrast from the VC information. The authors also performed comparisons of golden (working) and faulty devices for defect location.

In a later paper (Oxford and Propst, 1985) this group moved away from the concept of imaging the whole chip. They pointed out the relationship between field of view and resolution. As an example they cited that for a VLSI circuit digitised at 512×512 , each pixel contains three transistors! Clearly many images need to be taken at higher magnification, but this can lead to storage problems (each image is 0.25 MByte). Their solution, only relevant to VC was to sample at the important circuit nodes, thus drastically decreasing data storage. Failure analysis then amounts to functional testing of good/bad devices.

In spite of this, Child *et al* (1976) had indicated that comparisons were still useful even if faults were below the resolution limit. The average grey level at a pixel was still affected if a significant part of it was in error. Comparison techniques have thus remained popular, especially as the hardware requirements have become much less expensive. In fact, a large number of articles report the use of subtraction as an aid in failure analysis using voltage contrast. (e.g. Artz, 1983, Wolcott and Sziklas, 1987, Savart and Courtois, 1987).

A major development of these techniques, due to May *et al* (1984) is called dynamic fault imaging. In this method, a series of images are taken, of both good and faulty circuits, to span several logic states. They are then

compared to find the origin of the fault.

In the case of in-house design validation, complete knowledge of the circuit layout is available. The results of logic simulation programs allow the designed electrical states of the circuit to be known. Kuji *et al* (1985) were among the first to report use of an image processor to compare VC images with those predicted from computer aided design (CAD) data. They found this successful up to large scale integrated circuits. This facility is now becoming available on most commercially available EBT's (Electron Beam Testers) e.g. the Schlumberger IDS 5000. The development resources of these companies is such that at the present time systems are available which allow the full CAD map of the device to be online, so that chip navigation is automatic once reference points are established. Waveforms can be extracted easily from a point on the DUT and compared with logic simulations using the design data. Such systems are, however, extremely expensive.

An important problem in comparison techniques is registration of the two images. Rough registration can be achieved using a stepper-motor driven stage with suitable reduction gearing. Once reference points are defined on the circuit, reproducible positioning of $\pm 1\mu\text{m}$ is possible with the best stages. Further improvement is not possible due to thermal expansion constraints (Ranasinghe, 1989), although in principle this could be circumvented by (expensive) laser interferometers. Thus, before subtraction can be carried out, fine positioning is usually required. The traditional method for this is cross-correlation which is prohibitively slow, but can be replaced by more efficient algorithms (Barnea and Silverman, 1972). Although some automatic methods have been reported (Kuji *et al*, 1985, Stentiford and Twell, 1987, Michener, 1987) computation time is often large, and at present, of the

commercially available EBT's, none offer automatic image registration (private communication, B. Courtois).

Holt *et al* (1983) and Luther *et al* (1983) described how Fourier transform spatial filtering can locate defects in periodic IC's. They used a laser optical bench, and shone laser light through a micrograph slide which acted as the object for a lens. In the back focal plane of the lens the Fraunhofer diffraction pattern can be captured on a screen. A mask was painstakingly made and inserted at this point, removing all bright points due to the periodic circuit, while the rest of the diffraction pattern due to irregular features could pass through. Although the manual mask fabrication was slow, the result was successful. Another method was to subtract the Fourier transforms of perfect and defective areas using an image processor. This also performed the task quite effectively. The authors also demonstrated the benefits of removing edge detail, and of linear differentiation in certain cases.

An alternative to the Fourier transform is the Hartley transform, given by,

$$H(u, v) = \frac{1}{N} \sum_{x=0}^{N-1} \sum_{y=0}^{N-1} f(x, y) \left\{ \cos[2\pi(ux+vy)/N] + \sin[2\pi(ux+vy)/N] \right\} \quad (50)$$

compared to equation (45a) for the FFT. It has recently been indicated that the fast Hartley transform offers an improvement in speed over the FFT and has the advantage of producing a real result. It differs from the Fourier transform in having no j before the sine term (in the FFT $e^{j\theta} = \cos \theta + j \sin \theta$). However, problems with physical interpretation of Hartley transforms suggest its usefulness may be limited to one of speed alone. Also, the availability of specialist hardware for FFT's which perform

the calculation in real time (less than 1 TV frame-time) mean more development is required for the Hartley transform to compete.

Thus at present the emphasis seems to be on optical inspection during processing and VC for design verification and simple, comparative fault location. Very little work has been reported on the general applicability of image processing techniques to defect location. In addition the usefulness of special modes of the SEM, such as EBIC has been little explored. For this work, it is hoped that localised materials or electrical defects which can be resolved in imaging can be located automatically. It is thus necessary to identify any departures from the correct circuit structure, whether they be ESD (Electrostatic discharge), metallisation faults, passivation defects etc.

3 EXPERIMENTAL TECHNIQUES

3.1 IRRADIATION DAMAGE MEASUREMENTS

3.1.1 Determination of Device Data

The devices used for these irradiation experiments were test structures taken from a standard CMOS process at GEC Hirst Research Centre. This process uses a p-well and phosphorus-doped, polysilicon gate. Each die on the wafer contained several test structures and included discrete transistors which were used for this work. The dimensions, and process parameters were available from the wafer fabrication section as follows:

	p-channel	n-channel
drawn gate length (μm)	2	2
drawn gate width (μm)	20	20
gate thickness (nm)	40	40
substrate/well doping (cm^{-3})	1.2×10^{15}	1.3×10^{16}

Table 2. Transistor design parameters.

Transistors were taken from the same wafer for uniformity, and bonded up in dual in line (DIL) packages. Each source was stitch bonded to the substrate (or well) contact stripe, defining the standard device configuration, with the source and body shorted.

Other important parameters were checked by experiment. EBIC measurements with different connections allowed the locations of the well, and the transistor gate-width to be determined. The layer structure of the devices was very important for calculations of irradiation damage, and so

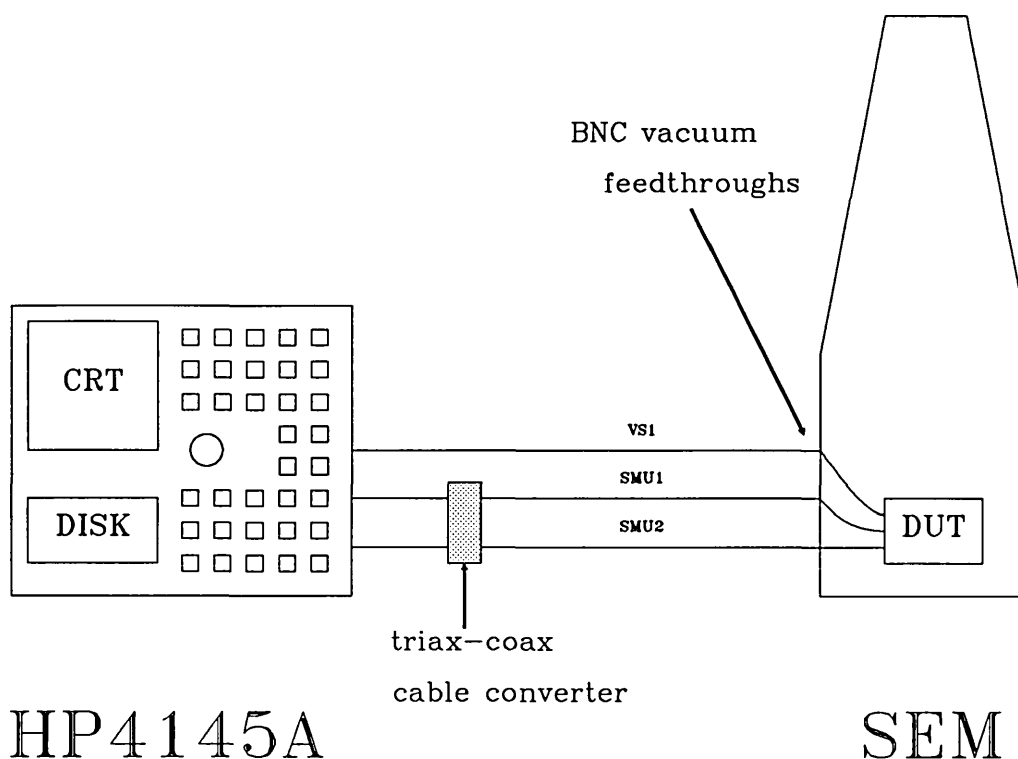


Fig. 25. Experimental set-up for irradiation damage electrical measurements.

one transistor from the test wafer was cross-sectioned with a diamond impregnated polishing wheel. By constant checking of progress, it was possible to obtain a cross-section through the source and drain, allowing all layer thicknesses in the device to be measured in the SEM. The magnification was calibrated with 1.1 μm diameter latex spheres.

3.1.2 Electrical Measurements

Electrical measurements were carried out on an HP4145A parametric analyser. A schematic diagram of the set-up is shown in Fig. 25. To facilitate measurements during irradiation screened cables from the 4145A were connected to BNC vacuum feedthroughs on a JSM 35C side-port.

Inside, three wires were connected to a ZIF (zero insertion force) socket containing the device under test, DUT, to make the source, gate and drain connections. The vacuum chamber acted as a noise shield, allowing stable measurements down to drain currents of 0.1 pA, necessary for the ΔV_{ot} calculations. The 4145A had SMU's (source-measuring units) which were configured as voltage or current monitors to scan V_{GS} and measure I_D . The control program and resulting data were stored on disk, and an auto-sequence was written to perform automatic measurement and data storage. Resulting plots were displayed on the CRT, and a cursor was adjusted to fit straight lines. The gradient and intercept were then displayed on the CRT.

To measure V_t , the "conductance plot" of I_D vs V_{GS} was plotted (Fig. 26). For consistency the same two points were chosen (-5 and $-15 \mu A$ for p-channel and 10 and $30 \mu A$ for n-channel) to give a straight line (Fig. 26). V_t was the x-intercept while the gradient, G_c allowed the mobility to be calculated from equation (31).

To determine ΔV_{ot} , the "sub-threshold plot" (Fig. 27) of $\log(I_D)$ vs V_{GS} was plotted. The low current region for $V_{GS} < V_t$ was exponential, so again a straight line was fitted. Its gradient, G_s , and intercept, Y_s , allowed V_{mg} to be extrapolated once I_{mg} was calculated from equation (36).

In summary, each measurement led to two plots, from which V_t , G_c , G_s , and Y_s were determined. Any other change in characteristic could easily be observed from the accurate plots e.g. leakage currents. Data sets were entered into the Asyst package on an IBM PC-AT clone, and a program was written which would calculate ΔV_{ot} and ΔV_{it} , archive the data and plot the results.

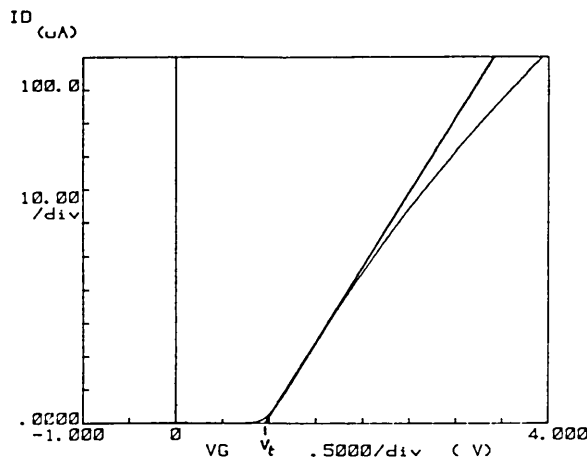


Fig. 26. A typical conductance plot showing the straight-line fitted to determine V_t and the mobility.

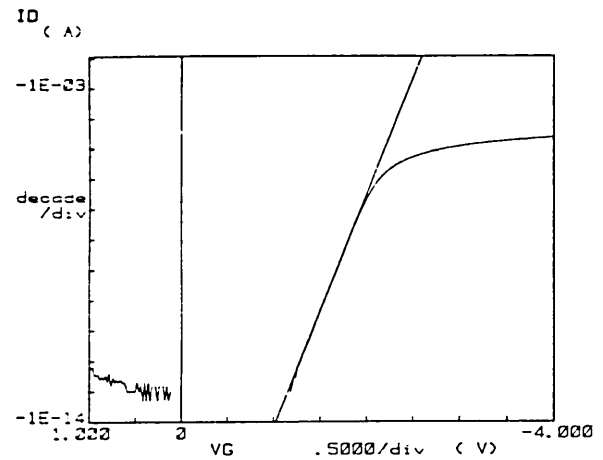


Fig. 27. Typical sub-threshold plot showing how the exponential part was extrapolated.

3.1.3 Irradiation Method

Test transistors were irradiated in a JEOL JSM 35C SEM. Before each experiment the SEM filament saturation and alignment were carefully adjusted (for beam stability). After focussing on the top of a Faraday cup, an appropriate probe current was set (in spot mode), then the chamber was vented. The Faraday cup was replaced by the DUT, which was at the same height as the top of the Faraday cup so no controls had to be adjusted to subsequently image the device. Thus, the beam current during irradiation was the same as that measured previously. It was also verified at the end of each experiment to check for drift. The residual error in I_b of 10% was the largest involved in calculation of doses. The irradiation dose was calculated from

$$D = \frac{I_b M^2 t}{A_1} \quad (51)$$

where I_b = beam current,
 M = magnification,
 t = time,
 A_1 = SEM scanned area at $\times 1$ (108 cm² for the JSM 35C).

For accurate measurements, the factor M^2/A_1 was calibrated. Electrical measurements were made in-situ, and it was necessary to blank the beam during measurements to prevent loading by the beam current or EBIC effects, both of which augment the sub-threshold leakage current. Therefore, the following procedure was used:

<u>Time/min:sec</u>	<u>Action</u>
0:00	Unblank beam
5:00	Blank beam
5:10	Commence measurements and archive data
6:00	Unblank beam and repeat the whole process

The gun chamber isolation valve was used to blank the electron beam. During irradiation, device pins were grounded, and at all times when handling them, full anti-static precautions had to be taken as there was no protection circuitry to prevent destruction of the transistor gate oxides by dielectric breakdown.

3.2 EBIC OF VLSI CIRCUITS

In studying IC's using EBIC, connecting to the circuit was the major problem. For one-off experiments, hard-wiring is often employed. However, in this project it was decided to construct a flexible system which would allow any type of IC package to be placed easily in the SEM, with provision for changing connections to the EBIC amplifier externally.

3.2.1 Specimen holders

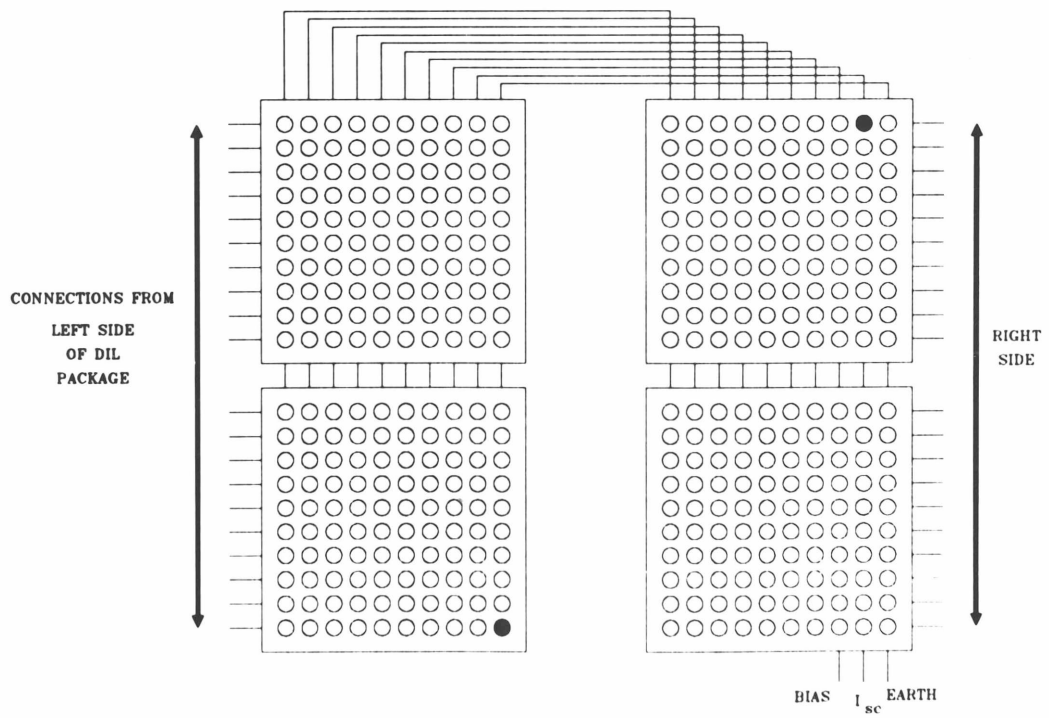
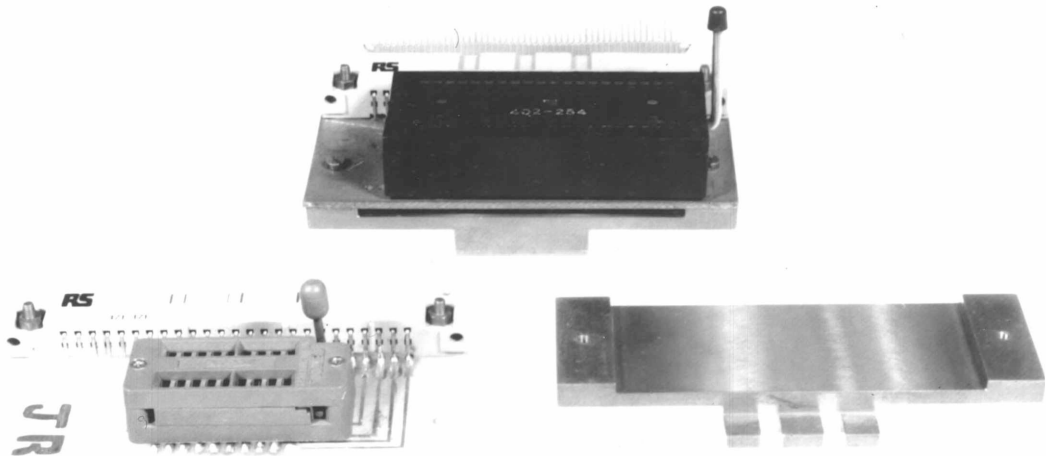
In order to accommodate the many different IC packages available, a system using printed circuit boards (PCB's) containing a zero insertion force (ZIF) socket and a 50 way edge connector was employed. The PCB was supported by screwing it to a specially made brass specimen holder (Fig. 28), maintaining the correct sample height for the eucentric specimen stage of the 840A. Two PCB's with ZIF sockets were used to cover most DIL packages (0.6" and 0.3" pitch), a TO5 socket and PCB was used for devices in cans, and a board was made for the 84-pin grid array socket used by transputer chips. For a different type of package, a new PCB was easily made up. To avoid vacuum contamination, a PTFE ribbon cable was used to make electrical connections to the inside of the 50-way vacuum feedthrough. This emerged as two D-connectors.

3.2.2 Switch Box

Outside the SEM chamber, noise pick-up had to be eliminated, so screened cables were used to connect to the switch-box. This contained four

*Fig. 28. Specimen holders used for integrated circuit EBIC experiments.
Top – mounted 40 way DIL holder with PTFE ribbon cable,
left – 18 way DIL adapter board,
right– brass board holder.*

Fig. 29. External switch–box to make connections for EBIC of IC's using mini–matrix boards. As shown, a 40 pin circuit has pin 20 grounded, and pin 40 connected to I_{sc} .



'mini-matrix boards' (Fig. 29). These had separate row and column contacts which were connected together by inserting special pins. A connection scheme was used which allowed easy correlation with a DIL package device. The rows connect to device pins, while columns 1 and 2 were wired to two BNC connectors for the Matelect EBIC amplifier, while column 3 provided for externally applied biases. In the figure, a 40-pin DIL device would have pin 20 connected to earth and pin 40 to I_{sc} .

3.2.3 Matelect EBIC Amplifier

In order to make quantitative EBIC measurements, a modular detection system is a great advantage, and such a system was built by Lesniak *et al* (1984). This was later developed into a commercial system by Matelect Ltd*. The amplifier consists of a head amplifier, main control unit and an optional computer interface unit (INTU1). The head amplifier was attached directly to the SEM to minimise noise. The ICVM5 control unit consisted of four modules for optimised detection of EBIC currents and signal conditioning for microscopy. Briefly they were:

Signal output – control of seven head amplifier current ranges (± 2 mA to ± 2 nA) for either I_{sc} or I_b measurement.

Analog output – was used for gain (0.1–100), offset and filtering of the video output.

Back-off current – attenuates large DC components of the input signal, allowing use of increased head amplifier sensitivity (± 20 mA in 7 ranges).

Bias voltage – up to ± 20 V could be applied.

* Matelect Ltd, 33 Bedford Gardens, London.

The computer interface unit allowed any of the front panel controls to be set via an RS232C interface, using the 80 available instructions. In contrast to some other instruments, the bias and back-off could not be set to exact values, but had to be adjusted with the un-calibrated DAC's (digital to analogue converters). For data acquisition, a fast (6400 conversions per sec) ADC (analogue to digital converter) was fitted to allow linescan capture of up to 8192 points.

The above describes the system as it existed as a first prototype at the beginning of this work. During program development some added features were found necessary and were kindly incorporated into the instrument by the manufacturers. These were an external (TTL) trigger input to synchronise linescan acquisition, an auxiliary input to the ADC to allow linescans from other sources (e.g. SE) to be acquired, and a special slow ADC rate for long scan times.

3.2.4 SEM Signal Conditioning Unit

The trigger signal and an auxiliary output of suitable voltage range were not immediately available from the SEM, and so a "signal conditioning unit" was built. A primary concern of such a circuit was to fully buffer the SEM electronics, as experience had shown that they contained sensitive circuit components, and straight connections easily led to accidental damage due to inadvertent short circuits by inexperienced users. The signal conditioning unit was first built to buffer the x-scan and image intensity signals for use with a chart recorder, and was later adapted to provide the signals required by the Matelect interface unit for data acquisition.

The auxiliary signal intensity (connector NA2 on the JSM 840A) was buffered using a 741 op-amp (Fig. 30) which although relatively old, has the advantage of full output protection for continuous shorts to ground or either power rail. The Matelect can only handle $\pm 2\text{V}$ signals at its auxiliary input, and this was accommodated by a $10\text{ k}\Omega$ potential divider.

The TTL trigger pulse was derived from the $\pm 10\text{ V}$ saw tooth x-scan from the SEM (pin 1 of connector JC4), after it was first buffered (Fig. 31). The trigger point was sensed by an LM311 comparator. This compared the incoming analogue signal to a reference voltage (set near 0 V with R_2), and had an open collector output, with pull-up resistor, R_4 . A degree of positive feedback (through R_3) was necessary to prevent multiple triggering. The trigger was optically isolated inside the INTU1, and required the $+5\text{ V}$ supply to be connected to the BNC screen to act as a pull-up. As this was easily shorted accidentally, a 50 mA fast-blow fuse protected the SEM power supply.

3.2.5 MATELECT Program for Data Acquisition

Linescans were originally taken with an xy recorder connected to an amplifier output. To calculate EBIC currents involved a measurement of the recorder trace, and tedious calculation of ranges etc, which introduced errors. The distance scale had to be calibrated.

A better method is to use a computer. However, before this is possible, all information necessary for interpretation must also be available if quantitative calculations are to be made. It is not sufficient to produce a set of curves of arbitrary distance vs relative current! The Matelect computer interface

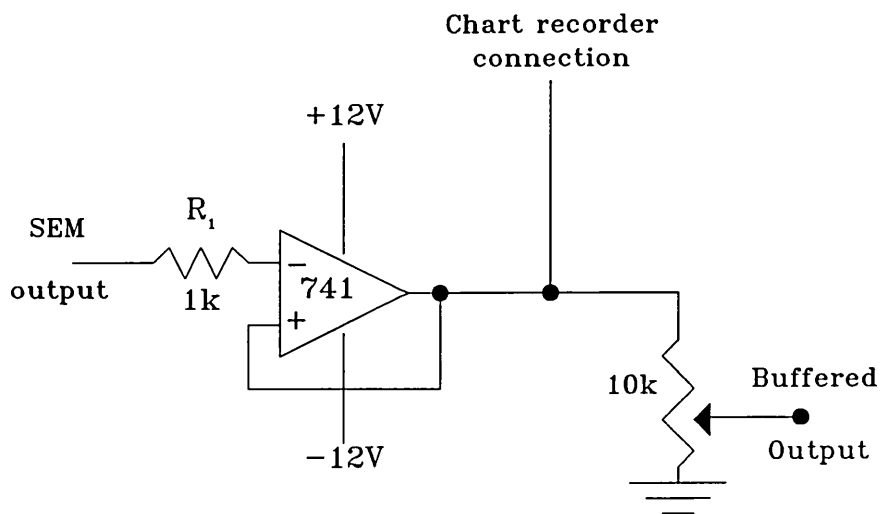


Fig. 30. Buffer amplifier for the auxiliary output of the SEM.

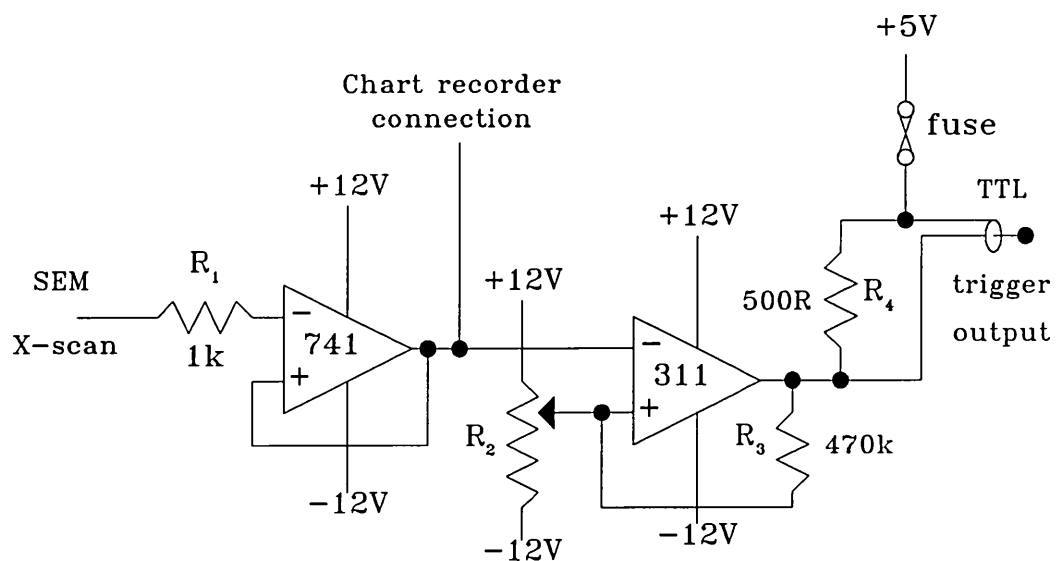


Fig. 31. Linescan trigger circuit, using the x-scan signal from the SEM.

unit goes some way in this respect and has the basic tools with which quantitative measurements may be made. In this work, a computer program called Matelect was written in Turbopascal* for an IBM PC-AT clone which controlled the INTU1 and produced fully calibrated data.

The program was written in a structured manner, consisting of procedures which were called from a user friendly menu with online help-text. All amplifier functions could be controlled via the computer keyboard, enabling fine adjustment of back-off current, current range, bias etc. Linescans were acquired very quickly, and all relevant information could be entered (E_b , comments, magnification, number of points). The beam current was measured using the PCD (probe current detector) consisting of a Faraday cage which was inserted into the beam automatically by compressed air (a standard JEOL add-on). The "dark current" was also measured while the beam was blanked.

Calibration of the distance scale was non-trivial. Modern SEM's usually have correction algorithms which hold the magnification constant within $\sim 5\%$. This is to allow for changes in working distance and E_b . On installation of the JSM-840A, this was checked, and found to be within 1% over the range 5-35 keV and 8-39 mm working distance. The accuracy of the magnification between $\times 100$ and $\times 10,000$ was about 3%. For most purposes, this is adequate, while for critical applications a calibration at the required magnification is advisable. Besides the magnification, calibration of linescans depends on the SEM scan rate, and the INTU1 ADC conversion rate also differed depending on the number of points required for the scan. To correct for all these factors, it is noted that for a given scan rate of

* Boorland International, 4585 Scotts Valley Drive, Scotts Valley, CA, USA.

period, T_{scan} , the spot velocity on the SEM CRT must be a constant, v_o . For an ADC rate, R , the time between samples was $1/R$, thus

$$v_o = d_{\text{CRT}} R \quad (52)$$

where d_{CRT} is the distance between sample points on the SEM CRT. At magnification, M this corresponds to a sampling distance on the specimen,

$$d_{\text{spec}} = d_{\text{CRT}} / M \quad (53)$$

$$\therefore v_o = d_{\text{spec}} M R \quad (54)$$

So, a scan across a test sample was used to determine d_{spec} for a given M, R and hence v_o . This information was stored in a configuration file, so any subsequent scans were automatically calibrated for any R, M . The rate was determined from the required number of points in the scan, as

$$R \approx n / T_{\text{scan}} \quad (55)$$

within the constraints of the ADC acquisition rates.

Once data was downloaded (~ 1 s), it was stored in one of ten buffers in RAM, and displayed graphically. Data could then be extracted interactively using cursors, or alternatively, the scan could be stored on disc (~ 2 s) for later reloading and re-appraisal, or analysis with other software. An example of the information stored in the file header is shown in appendix 1, and contained all information necessary for quantitative analysis. To perform all these functions required a substantial program, consisting of over 1800 lines of source code. For this reason it is not included as an appendix.

3.2.6 Data analysis

All data analysis in this work was performed using the Asyst* programming language. Although very difficult to learn, the vast range of mathematical functions available made it potentially very powerful.

A program (appendix 2) was written to read Matelect data files. Asyst calculations are array based, so for example from a linescan of I_{sc} , η_{cc} could be calculated according to equation (8) almost instantaneously for the whole scan once a suitable procedure was written. Many other procedures were written for data analysis, and will be described at the appropriate juncture in the results section.

* Keithly Instruments, The Minster, 58 Portman Road, Reading, Berks.

3.3 IMAGE PROCESSING

Image processing was carried out with a Kontron* image processor. This system was purchased with part of the capital grant for Alvey project 104. The particular system was chosen as it was well interfaced to JEOL SEM's and exhibited a comprehensive range of software. The system ordered was an upgraded version of this, with an IBM PC-AT compatible host computer, and all the original Fortran software was to be re-written in C. The latter process took longer than expected, and for the major part of this project, work was carried out with provisional software versions. Indeed, at the project end, it was still only possible to access the existing image processing macros. The necessary software tools to program the hardware directly did not become available.

3.3.1 Hardware

A block diagram of the hardware configuration is shown in Fig. 32. The PC-AT clone acts as host, and user interface. A 40M hard disk held programs and allowed for some image storage. Connected to the PC expansion bus were two Bernoulli drives, each of which housed a removable cartridge of 20M capacity. These were high speed devices for both archiving and on-line use. The SEM interface provided a digital scan generator, with two 12bit DAC's. It also had two separate input channels, with 8bit ADC's. All these inputs and outputs were software programmable by a further gain and offset factor (8bit).

* Kontron Bildanalyse GmbH, Breslauer Str. 2, Eching, FRG.

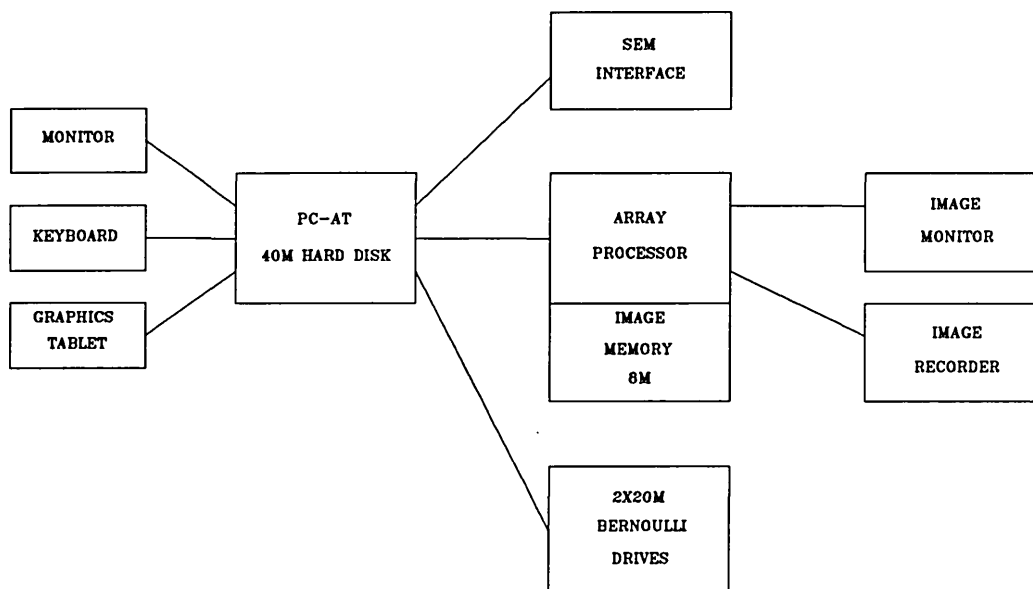


Fig. 32. Block diagram of the Kontron image processing system.

The array processor contained the main image memory (8M), and its specialised architecture allowed fast processing operations to be carried out on complete images. The $512 \times 512 \times 8$ bit image format is commonly used because its resolution is comparable with most display devices. A 1 bit overlay plane was also present on the Kontron for separately writing text etc. on images. A separate image monitor and camera based image recorder were also connected to the array processor. Relevant examples of processing times are as follows:

time	function
3s	loading $512 \times 512 \times 8$ bit image from hard-disk
3s	" " " " Bernoulli cartridge
60s	512×512 FFT
0.8s	fastest SEM frame scan

3.3.2 Software

Although the PC-AT runs under MSDOS, for image processing it runs under its own multi-tasking operating system. IBAS can be used in either a menu or command-line environment, but in either case, commands are selected from a library of functions. This is similar to one of the first image processing languages, SEMPER (Saxton *et al*, 1979). Functions can be chained together to make programs, and the resulting language has variables, and structures, etc. For example, a trivial program to display the first ten images in memory would be:

```
for i=1,i==10,i=i+1
  display i
endfor
```

Program loops could only be nested four levels deep, which turned out to be a severe limitation in some cases. The range of available functions is large, although not comprehensive, and is oriented somewhat towards morphological analysis.

Work done here consisted of writing macros for particular defect location problems, using the primitive functions available. These macros were then to be called up as a user aid to defect location. To make clear the distinction between existing functions, and the macros written in this work, the former will always be referred to as "Kontron [*FunctionName*]".

4 RESULTS AND DISCUSSION

4.1 IRRADIATION DAMAGE

4.1.1 Transistor Structure Determination

The emissive mode image on the left of Fig. 33(a) shows the whole test structure with three gold wires making connections to the p-channel test transistor. On the right is an EBIC image which shows the p-well for the n-channel transistors. In Fig. 33b the transistor itself is shown in SE (left) and EBIC (right) modes. The two bright regions in the EBIC image are the source and drain diffusions, and are traversed by the polysilicon gate. The gate width was measured to be $18\mu\text{m}$.

To determine the thicknesses of the various layers which make up the structure, a die was cross-sectioned and viewed in the SE mode. Sections were not etched as this could give systematic errors in layer thickness determinations. Instead, SE images with signal averaging were sufficient to see all the layers (Fig. 33c). These measurements are summarised in table 3.

	p-channel	n-channel
gate length (μm)	1.7	1.7
gate width (μm)	18	18
gate oxide thickness (nm)	50	50
isolation oxide thickness (μm)	0.65	0.65
gate poly thickness (μm)	0.30	0.30
substrate/well doping (cm^{-3})	1.2×10^{15}	1.3×10^{16}

Table 3 Measured transistor dimensions.

Fig. 33. Images of test transistors.

(a) General view of test structure

left – SE

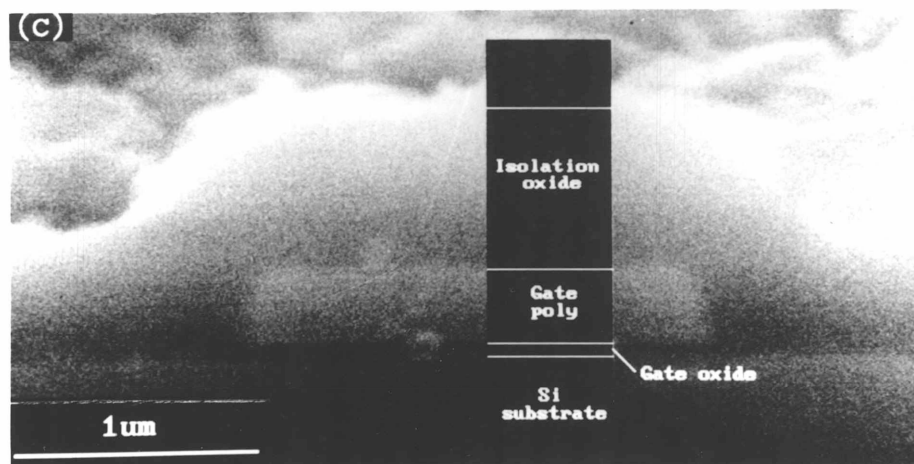
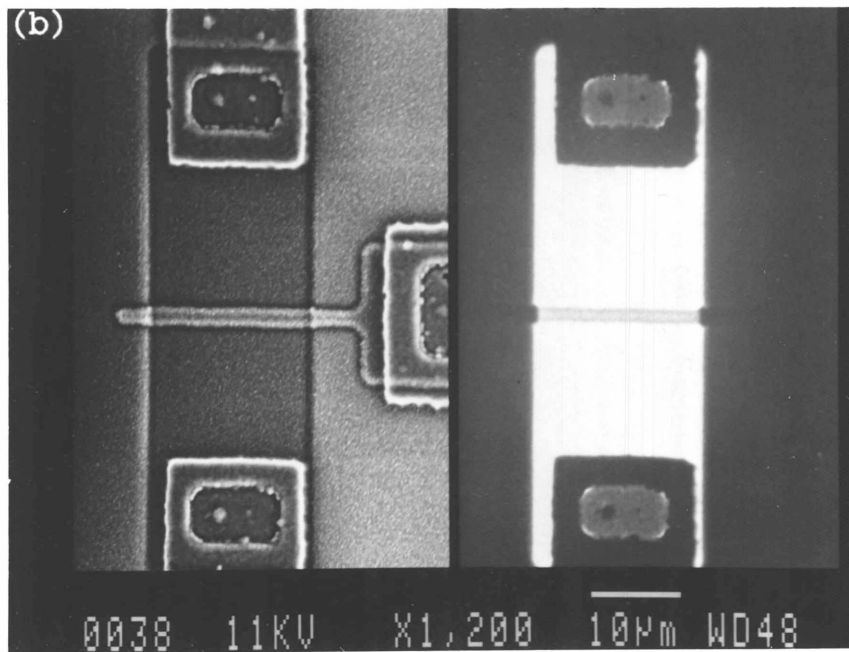
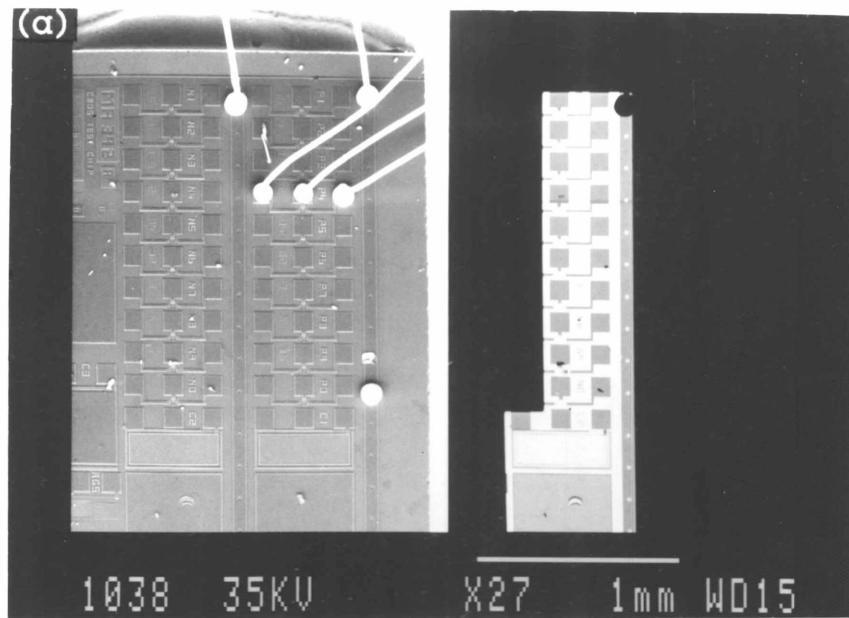
right – EBIC with substrate grounded, well connected to I_{sc}

(b) A single p-channel transistor

left – SE

*right – EBIC with substrate grounded, source and drain
connected to I_{sc}*

(c) Cross-section along a vertical plane in (b).



The measured dimensions can be seen to be $\sim 10\%$ smaller than those as drawn (cf Table 2, section 3.1.1), due to errors in the photolithography process. In the cross-section, the top layer is the isolation oxide, used to insulate metal tracks from the substrate. It should be borne in mind that a finished device would have a further passivation oxide layer of some $0.5 - 1 \mu\text{m}$ above this.

4.1.2 Threshold Voltage Shifts

Early measurements of threshold voltage shift, ΔV_t showed that it was relatively easy to create so much damage that a large ΔV_t was produced, especially at high beam energy. Indeed, so much damage could occur in these transistors that the I_D vs V_{GS} plot became too distorted to derive V_t from it. For this reason, the main batch of experiments were made at lower doses, for which ΔV_t was more easily quantified. For the purposes of discussion, it is convenient to refer to this as a "low damage" condition, and the former as "high damage". High damage can be regarded as a dose which gives $\Delta V_t > 1 \text{ V}$, but the absolute value of dose for this condition is, of course strongly E_b dependent.

Initial experiments were made to study the validity of the dose equation (51). The absence of dose rate effects is implicit in the equation, which by default has been assumed by other authors. However, Hungerford (1987) observed an apparent dose rate dependence in EBIC artefacts due to native oxide charging on silicon. So at 6 keV, using different beam currents and irradiation dwell times (the time between the 1 min measurement periods), ΔV_t was measured (Fig. 34). The graphs all show the same relationship within experimental error. Fig. 34 also serves to show that the variation of

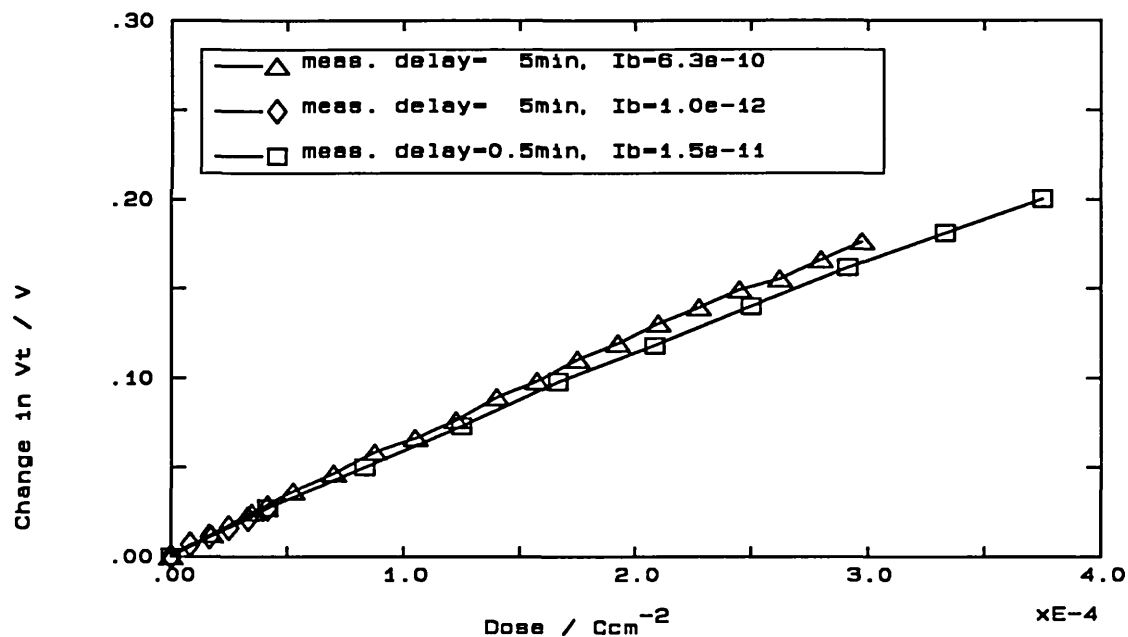


Fig. 34. Shift in threshold voltage vs dose under various irradiation conditions at 6 keV. Shows linear relationship, and absence of dose-rate effects.

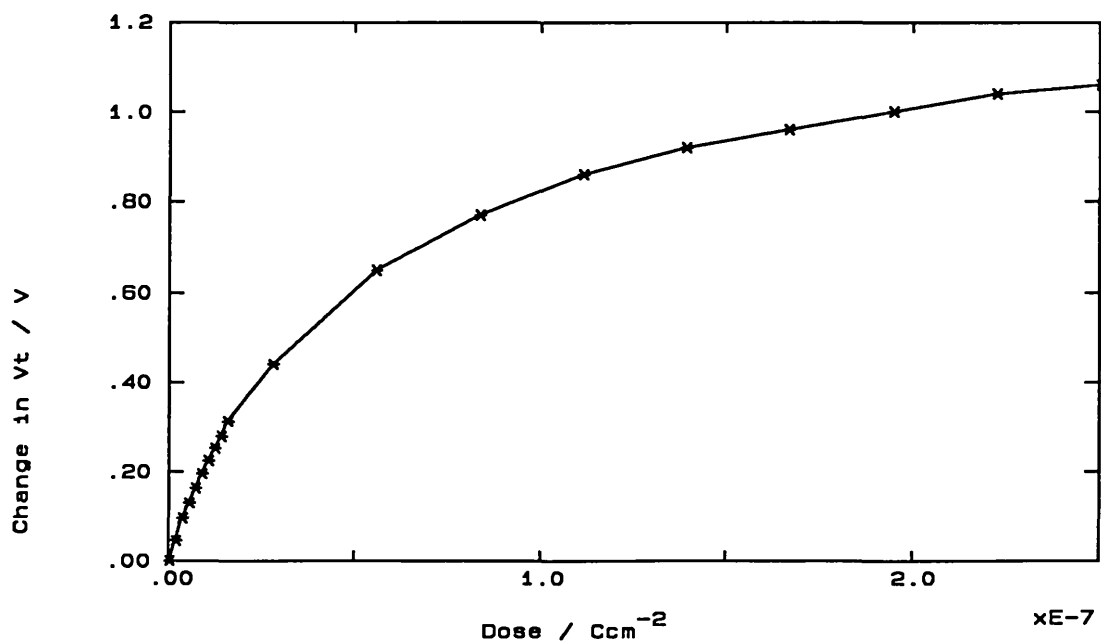


Fig. 35. Saturation of threshold voltage shift at high doses, in this case at 20keV.

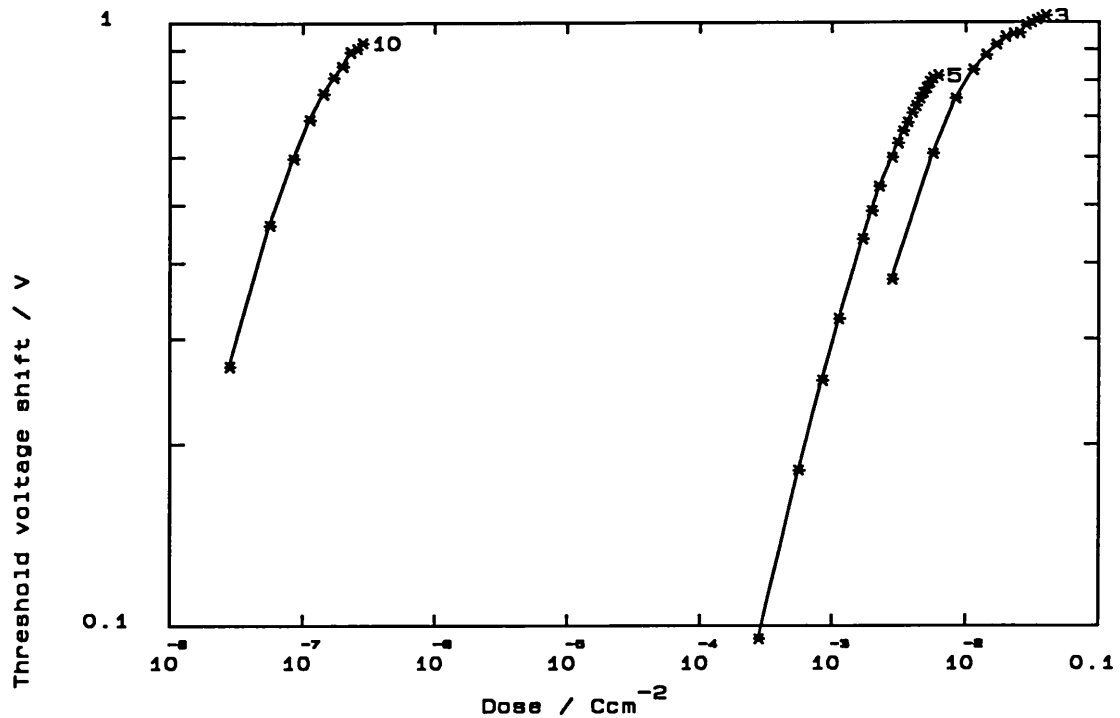


Fig. 36. Threshold shift vs dose for the *n*-channel transistors studied.

ΔV_t with dose was linear, confirming that measurements were in the low-dose regime. A small degree of non-linearity was apparent, and for high doses, ΔV_t eventually began to saturate (Fig. 35), as observed by other authors (Miyoshi *et al*, 1982, Ranasinghe *et al*, 1987, Jones, 1989). However, at this stage circuit operation in critical parts of a real IC would probably have been corrupted. For this reason, subsequent measurements were made at low damage, centred around $\Delta V_t \sim 0.1$ V.

A few *n*-channel transistors were examined at low E_b , and high dose, giving the plots shown in Fig. 36. *N*-channel transistors were prone to develop drain-source leakage currents, especially at high irradiating beam energies, so the main set of experiments to determine beam energy dependence were carried out on *p*-channel devices. A comprehensive set of

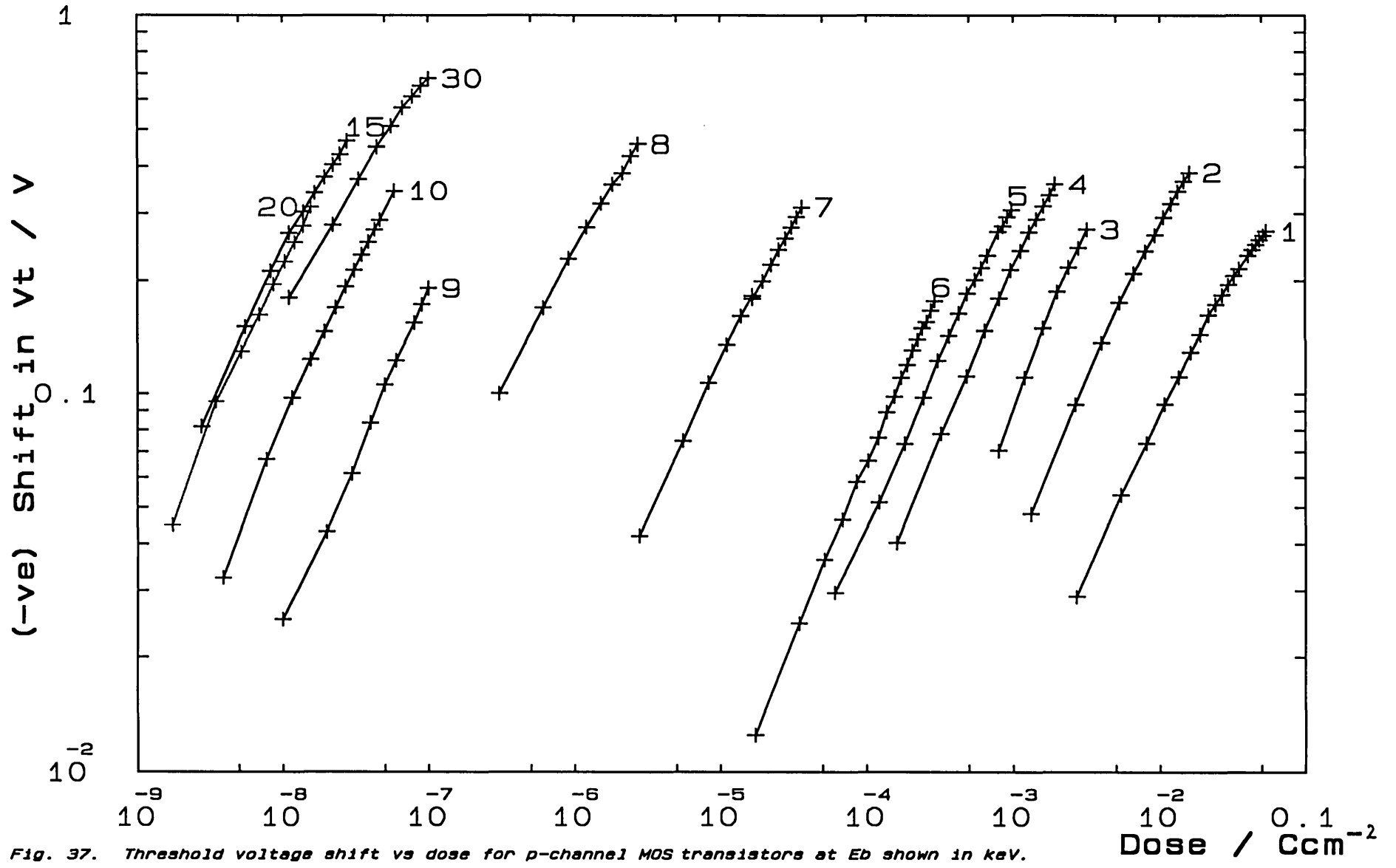


Fig. 37. Threshold voltage shift vs dose for p-channel MOS transistors at E_b shown in keV.

results were obtained between 1 and 30 keV, concentrating on the region below 10 keV. Graphs of ΔV_t vs dose are all plotted in Fig. 37 on log-log axes to accommodate the vast spread of data. From the plots it is obvious that at high E_b , damage is most severe, tailing off towards lower E_b . The second bunching of the lines, at ~ 5 keV is believed to be due to secondary X-rays. Further analysis of this data follows in the next two sections.

4.1.3 Oxide Trapped Charge and Interface States

ΔV_t is in fact composed of two contributions, as discussed in section 2.3.2.3, and can be separated into ΔV_{ot} due to oxide trapped charge, and ΔV_{it} due to charged interface traps. The calculation described therein was possible in all but a few cases, in which leakage currents rose by more than ~ 10 pA. This prevented accurate extrapolation of I_{mg} . The calculated values of ΔV_{ot} and ΔV_{it} are shown in Fig. 38 for n-channel, and in Fig. 39 for p-channel.

The first comment concerns shift polarities (ignored in Figs. 38 and 39). For both n- and p-channel, ΔV_{ot} is negative, i.e. V_{ot} becomes more negative. This is due to an increased density of positive charge in the gate oxide. The polarities of ΔV_{it} are opposite for n- and p-channel transistors. Referring back to Fig. 16c, it is apparent that for p-channel transistors at threshold, the interface state charge is composed of positive, ionised donors, and hence ΔV_{ot} and ΔV_{it} are additive. Conversely, for n-channel transistors, the interface states consist of negative, ionised acceptors. Hence ΔV_{it} combines with ΔV_{ot} subtractively for n-channel transistors.

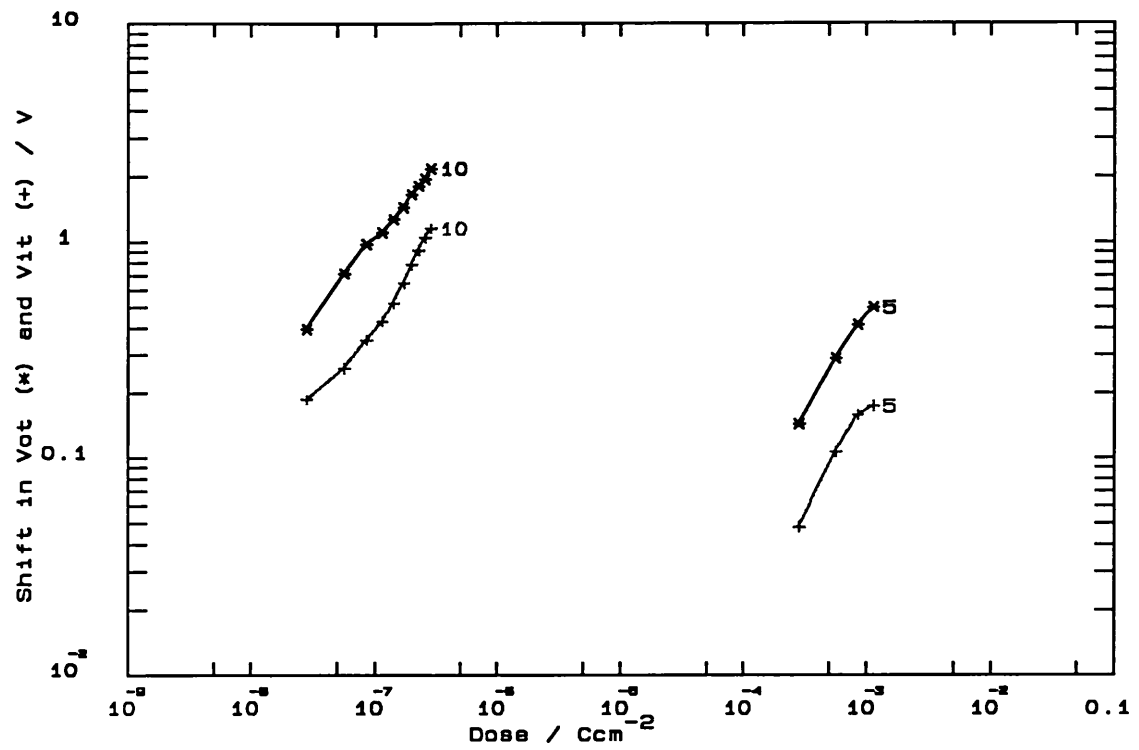


Fig. 38. ΔV_{ot} (*) and ΔV_{it} (+) for *n*-channel transistors.

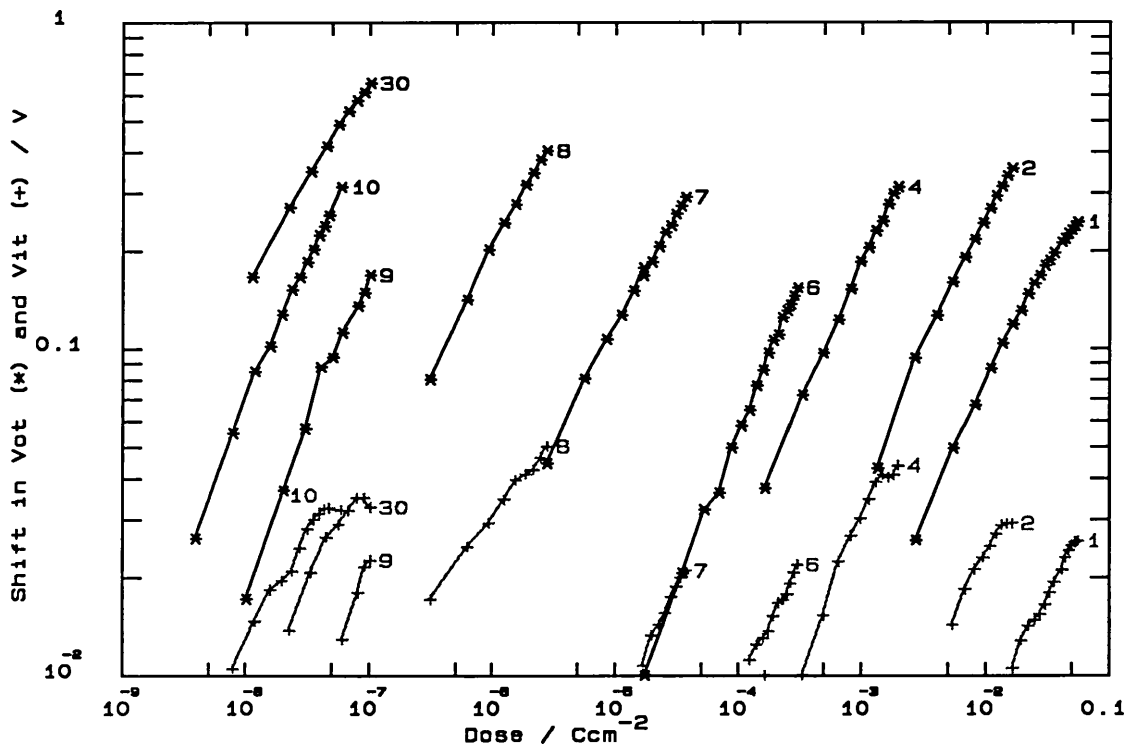


Fig. 39. ΔV_{ot} (*) and ΔV_{it} (+) for *p*-channel transistors.

The ratio of ΔV_{ot} to ΔV_{it} was constant for all E_b within the accuracy to which ΔV_{it} could be determined. The average ratio for p-channel transistors was 9:1 while for n-channel transistors it was 3:1. The error in the p-channel ratio was $\sim 30\%$, and the value for n-channel has to be regarded as an estimate. The difference in the two ratios could be due to a variety of factors, such as the dose regime in which they were measured, or the different φ_{ms} values which would cause the electric field across the oxide to be different. Perhaps more likely is that there are more interface states in the upper half of the bandgap to be sampled in n-channel transistors, than there are in the lower half for the p-channel case. In both examples, however, the oxide trapped charge is the dominant contribution, and the two separate as a constant ratio.

This appears to be the first time that the contributions of ΔV_{ot} and ΔV_{it} have been separated in electron beam irradiation damage of MOS transistors. All studies until now only considered the total ΔV_t .

4.1.4 Variation of Damage Rate With E_b

It has already been shown that at sufficiently low dose, the plots of D vs ΔV_t for each E_b were straight lines with gradient 1 (Fig. 34). Nakamae *et al* (1981) showed how ΔV_t and D were related through the fraction of the beam energy absorbed by the gate oxide, f_D (equation 37). Here, their treatment is extended by writing the change in number density of trapped charges,

$$\Delta N = k \left[f_D (1 - \kappa \eta) \frac{E_b}{e_i} \right] \left[\frac{D}{q} \right] \quad (56)$$

where e_i for $\text{SiO}_2 = 18 \text{ eV}$ (Ausman and McLean, 1975) and k expresses the proportion of holes which become trapped. It also accounts for their distribution, so that if they are assumed to form a sheet at the Si-SiO₂ interface,

$$\Delta V_t = \frac{q\Delta N}{C_{\text{ox}}} \quad (57)$$

As the other terms in the equations are constants for each experiment, $\Delta V_t \propto D$ with gradient $\propto f_D E_b$. The latter was calculated from the Everhart-Hoff model, and Monte Carlo simulations. After the necessary scaling of the experimental data, the plot of Fig. 40 was obtained. The value of k required was 0.056, showing that only a small proportion of the generated holes actually contribute to ΔV_t , with the rest recombining. ΔV_t was used rather than ΔV_{ot} for consistency, as ΔV_{ot} was not available at all E_b . ΔV_t is about 10% less than ΔV_{ot} as discussed earlier.

In Fig. 40 consider first electron penetration, because models are available for the energy that the electrons dissipate. The Everhart-Hoff calculation fits well at higher energies ($> 9 \text{ keV}$), but the fit in the low energy region between 6 and 9 keV is poor. This implies that the tail of the Everhart-Hoff depth-dose function is imprecise. In fact, in their original paper, the authors did note that there was an apparently deeper penetration of electrons at low accelerating voltages, which they attributed to range straggling. The Everhart-Hoff expression is a polynomial, and is forced to zero at $1.1R_G$. In fact, the absolute cut-off could be considered to be the Bethe range, R_B , which is the total length of the path travelled by electrons. A few electrons which undergo very few deviations might be expected to approach R_B which is $1.23R_G$ (Shea *et al*, 1978). The implication is that

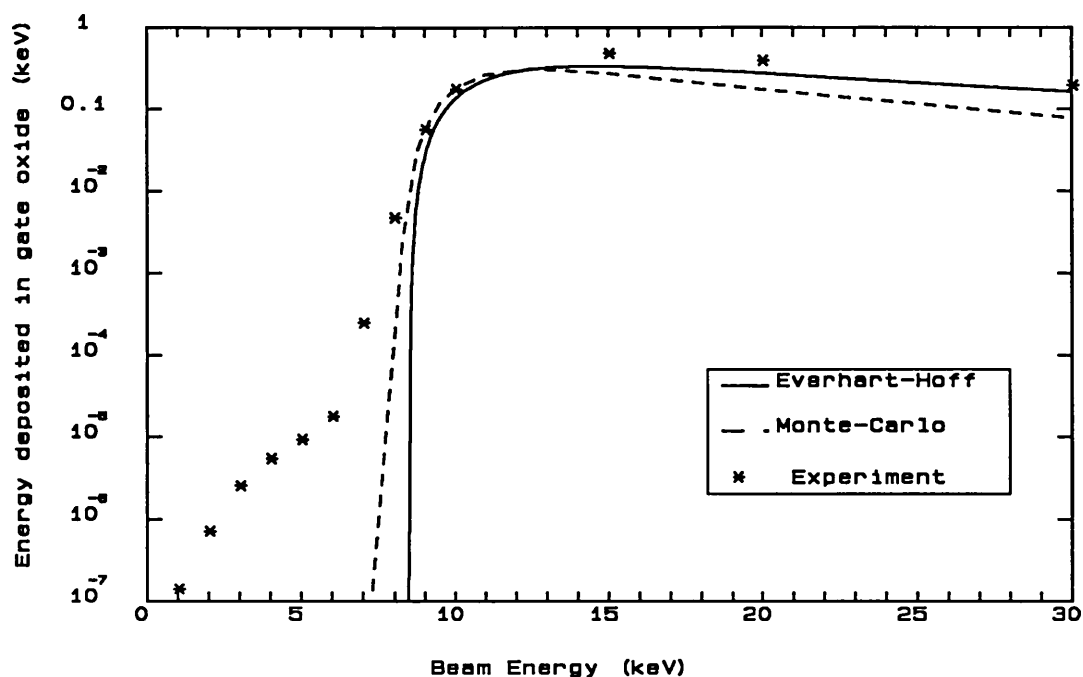


Fig. 40. Calculations of energy absorbed in the gate oxide using the Everhart-Hoff model (1971) and Monte Carlo simulations (Napchan and Holt, 1987). The stars denote experimental results, and clearly show the effect of X-rays below 6keV.

although the Everhart-Hoff model predicts the gross behaviour, the deepest part of the energy dissipation tail is modelled quite poorly. The same phenomenon was observed by Nakamae *et al* (1981).

Monte-Carlo simulations using the multi-layer, plural scattering model program by Napchan and Holt (1987) show yet different results. At high beam energies, the fit is somewhat poor. However, the plural scattering model should not be expected to fit well here. The reason for this can be seen from the program output at 25 keV (Fig. 41) which shows that the trajectory step-length (1/50th of the Bethe range) is comparable with the geometry of the structure. Thus, in this case, near the surface where electrons have undergone little scattering, spurious energy peaks appear in the depth-dose function at the end of each step. These are artefacts. At lower E_b , (below 9keV) where penetration of the tail of the depth-dose

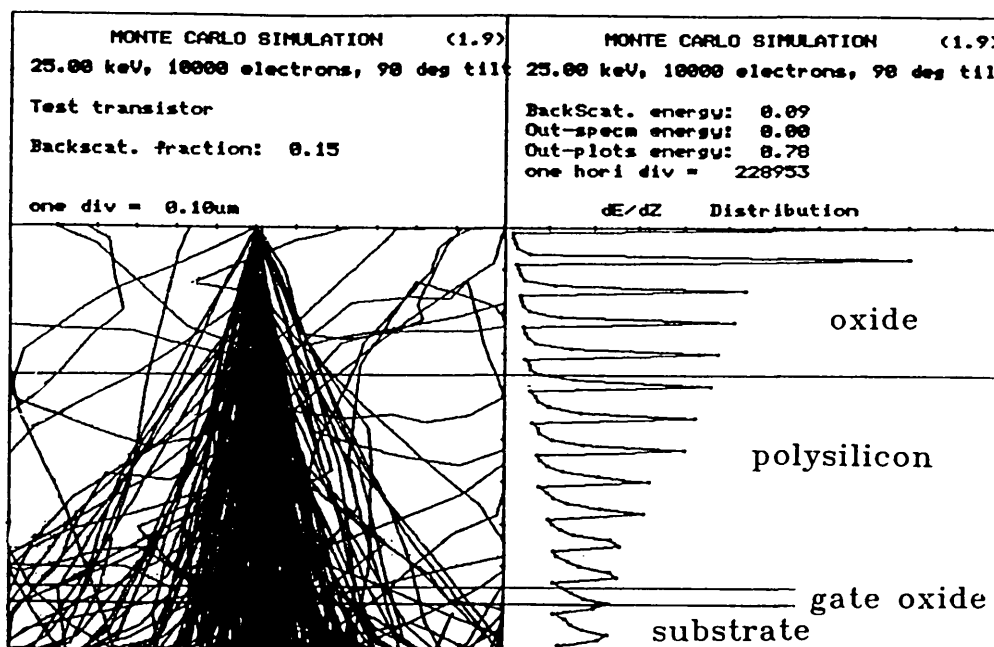


Fig. 41. Monte Carlo program output at 25 keV showing the limited accuracy when the device dimensions become comparable to the simulation step-length.

curve occurs, the fit is better than the Everhart-Hoff results, but still there is a degree of difference with experiment. A single scattering model Monte Carlo simulation was also used, but the results showed no improvement.

Alternative explanations must be considered. The transistor geometry is finite in the plane of the wafer (Fig. 33c). It could be, therefore that edge effects are occurring. For example, electrons might penetrate from the side of the gate, where the silicon is covered only by the isolation oxide. Another possibility is that fast secondary electrons generated by the beam penetrate more deeply than expected. A related effect might be the generation of hot holes in the polysilicon gate which might diffuse to the oxide with sufficient energy to surmount the potential barrier and be injected.

A very clear transition in behaviour is observed below 6 keV. It is believed

that in this regime ΔV_t is due to secondary X-rays which were generated in the upper layers by electrons. X-rays have a much longer penetration depth than electrons. Note that damage due to X-rays at say 1 keV is some six orders of magnitude less than the worst case of electron penetration. This has very important implications for techniques such as voltage contrast, which do not need electrons to penetrate deeply into the device structure. In other words, if electron penetration to gate oxides is avoided, then threshold voltage shifts will be small.

Calculations of the X-ray penetration are few. Nakamae *et al* (1981) made a rough estimate of O K_α and Si K_α X-rays to explain their anomalously high damage at 5 keV. Reiners *et al* (1985) assumed all X-rays were generated at the surface, and so the fit to their data was only good as E_b approached zero, and in fact the f_D vs E_b plot actually exhibited a peak. The true origin of this damage seems most likely to be due to the Bremsstrahlung, or continuum X-rays, as the total, integrated intensity of these is much greater than that of the narrow K_α peaks of the characteristic X-rays. In order to verify this hypothesis, another transistor was irradiated at 0.4keV, which is below the ionisation energy for either of the main characteristic peaks. In this case, a threshold shift of 50 mV was observed after a dose of 0.7 Ccm^{-2} . For this work, a modified version of the Reiners calculation was made to estimate X-ray energy dissipation in the gate oxide. The depth of generation for X-rays of energy E_x was taken from the range equation due to Andersen and Hasler (1966):

$$\rho R = 0.064 (E_b^{1.68} - E_x^{1.68}) \quad (58)$$

The total energy of the emitted X-rays is $\propto E_b^2$, while the wavelength of

the Bremsstrahlung was taken to be all at the maximum of the spectrum, which is known to be $3/2E_c$ where E_c is the long-wavelength cut-off. Absorption was then calculated from Beer's law

$$I = I_0 \exp (- (\mu/\rho)(\rho z)) \quad (59)$$

where I_0 = incident intensity
 I = transmitted intensity
 $\mu(E_x)$ = the mass absorption co-efficient
 ρ = density
 z = depth

The mass absorption coefficient, $\mu(E_x)$ was interpolated from data in Goldstein *et al* (1981, pp615-40) for each E_b used. $\mu(E_x)$ for SiO_2 was calculated from the data for Si and oxygen. Finally, the energy absorbed in the gate oxide was given by the difference of the intensities at the top and bottom of the gate oxide. The result is proportional to f_D due to X-rays, and can be scaled to fit the experimental data (Fig. 42). The step in the calculated curve is due to the Si absorption edge, and is an artifact due to assuming a single energy for the whole of the Bremsstrahlung. Agreement is quite good, although at high energies the penetration is greater than expected. The main trend of the experimental results is, however, explained, within the limits of such a calculation.

4.1.5 Mobility Reduction

In unirradiated transistors, the (channel) mobility of carriers was determined from conductance plots (equation 31). Average values for n- and p-channel transistors were 500 and 200 $\text{cm}^2(\text{Vs})^{-1}$ respectively. After each

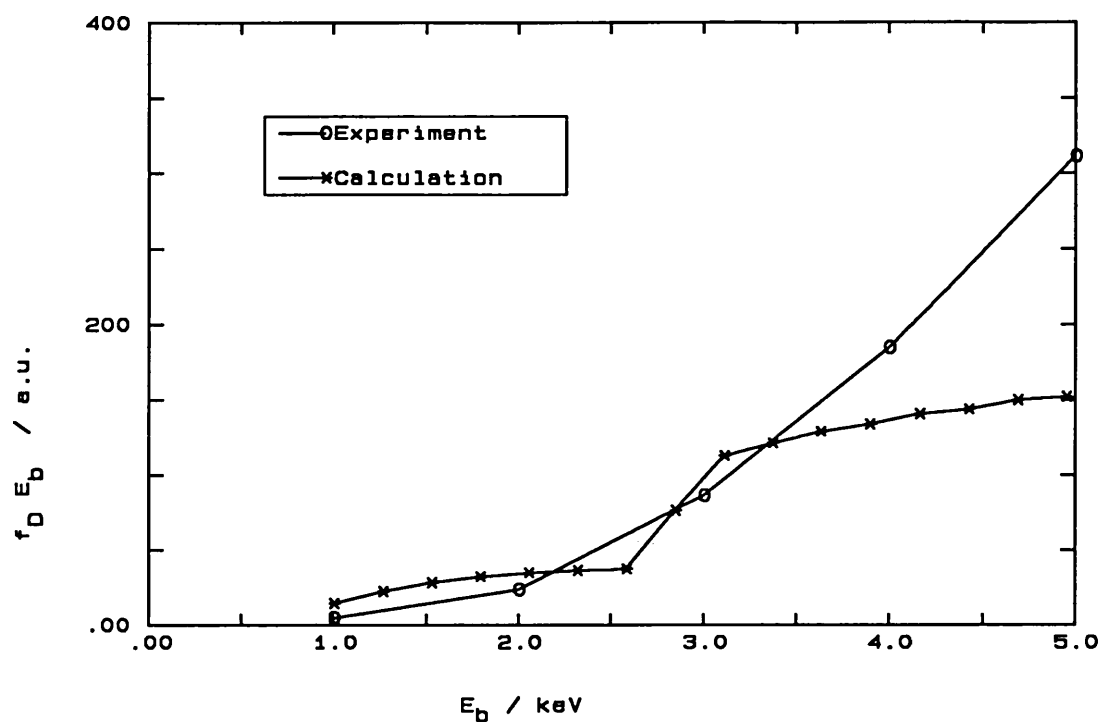
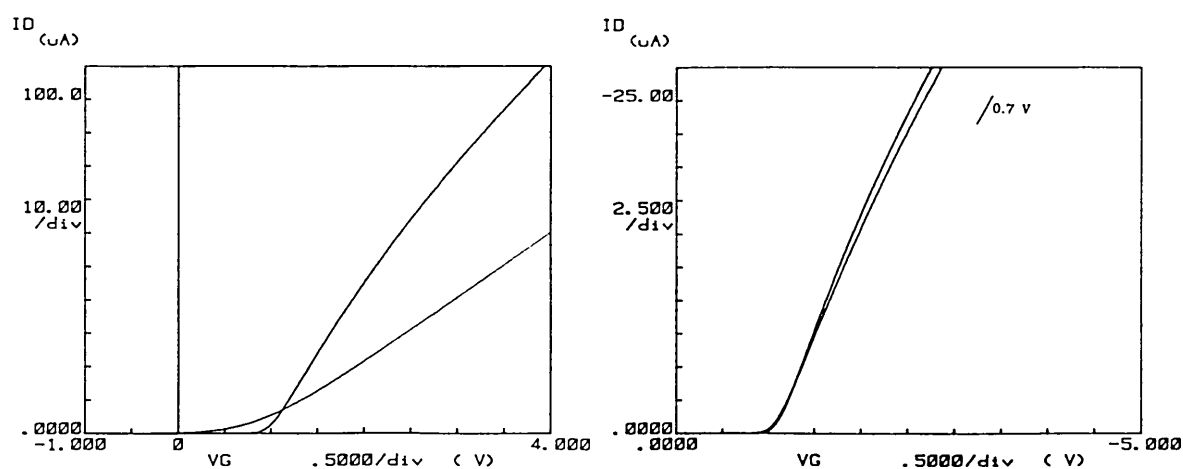


Fig. 42. Comparison of the X-ray damage regime experimental values of gate oxide absorbed energy with results of approximate calculation.



(a) $5 \times 10^{-4} \text{ Ccm}^{-2}$ at 10 keV

(b) $3 \times 10^{-3} \text{ Ccm}^{-2}$ at 5 keV

Fig. 43. Change in gradient of the conductance plot due to decreased mobility. The graph in (b) is offset to make the gradient change clear.

irradiation the gradient of the conductance plot decreased. Fig. 43a shows such a device after a high damage dose for which the gradient dramatically decreased. In the low damage regime, (b) shows that a reduction of $\sim 10\%$ was more usual. In this plot, the second curve was offset by 0.7 V to make the change in gradient clear. On referring to the triode equation (30), it is evident that the mobility is the only parameter which can be responsible. Heating, of course reduces μ due to increased phonon scattering, but under these irradiation conditions the effect is negligible. Measurements taken after removal from the SEM, which would certainly allow thermalisation, showed no relaxation.

Further investigation of this mobility reduction indicated that it was closely correlated with the shift in threshold voltage, for all beam energies (Fig. 44). This bears a qualitative similarity to the plots of ΔV_t vs dose in Fig. 37, although in this case, the plots are non-linear.

Mobility reduction has not often been referred to in the literature. McWhorter and Winokur (1986) made a one sentence reference that they observed a good fit to Sun and Plummer's (1980) relationship. The authors did not show any further data or graphs to substantiate this. Sun and Plummer's comprehensive study was concerned with the many factors which affect surface electron mobility as distinct from bulk mobility. They referred to Q_{it} and Q_f , which led to increased coulombic scattering, and gave a relationship between total interface charge density and mobility:

$$\mu = \frac{\mu_o}{1 + \alpha Q_{int}} \quad (60)$$

where $\mu_o, \alpha =$ constants
 $Q_{int} =$ the total interface charge $= Q_{it} + Q_f$.

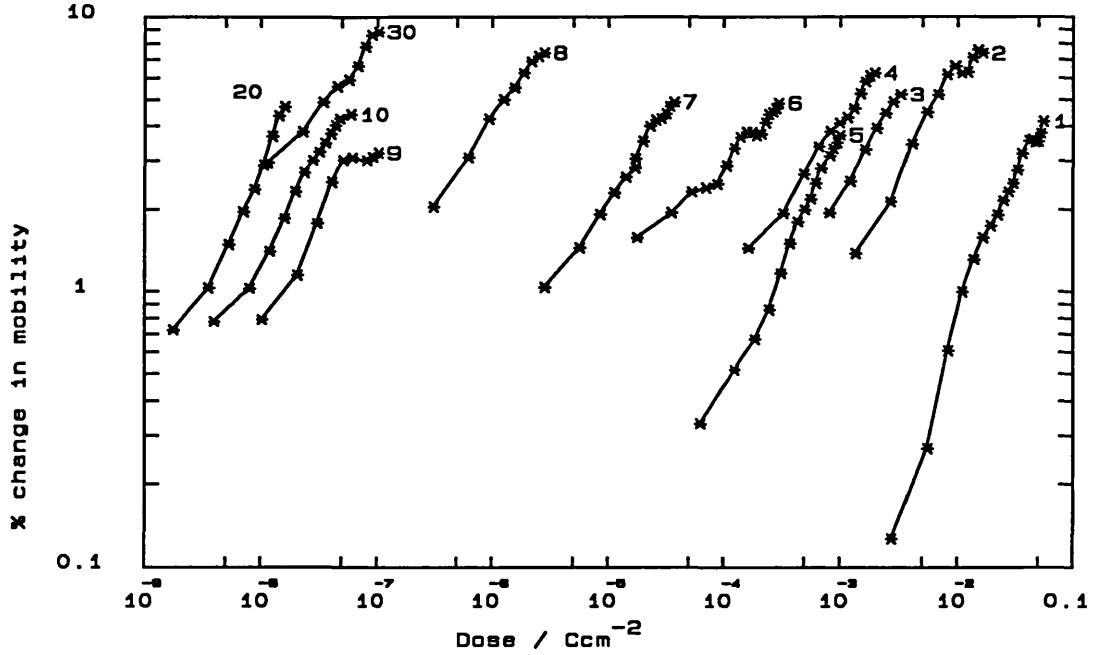


Fig. 44. Percentage change in mobility for *p*-channel transistors at all beam energies studied.

From equation 26, $V_t = Q_{int} + (\text{const})$. Thus, assuming that a similar relationship to (60) holds for surface hole mobility,

$$V_t = A \frac{1}{\mu} + B \quad (61)$$

Where A and B are constants. This plot gives a straight line (Fig. 45). A least squares fit to this and data at other E_b gave $A = (8.7 \pm 1.7) \times 10^{-4} \text{ cm}^2 \text{ s}^{-1}$ and $B = (4.0 \pm 0.4) \times 10^{-3} \text{ V}$ where the errors reflect the variation between different E_b . This is good considering the limited precision with which small changes in mobility could be measured, from the curve tracer, and is consistent with the theory of Sun and Plummer (1980).

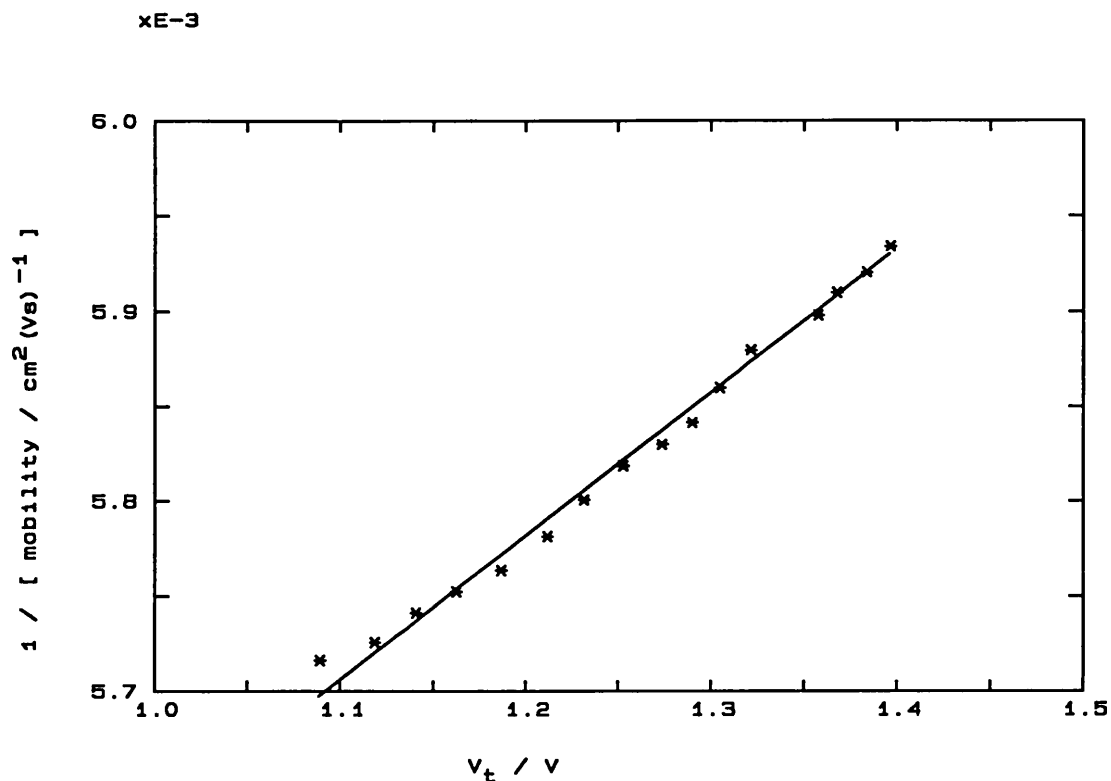


Fig. 45. Plot to test the hyperbolic relationship between mobility and threshold voltage shift.

The total mobility change for $\Delta V_t < 1 \text{ V}$ was $\sim 5\text{--}10\%$, comparable with a measured variation of 10% between test transistors. This variability could be due to fluctuations in gate length and width rather than an actual mobility fluctuation across the wafer, owing to the measurement technique.

4.1.6 Drain Leakage Current

After sufficient irradiation, the drain leakage current increased, as seen in the sub-threshold plot (Fig. 46). Before irradiation, the drain current at low gate potential is less than 0.1 pA. In this case, after a dose of $3 \times 10^{-3} \text{ Ccm}^{-2}$ at 5 keV the leakage current had increased to 0.5 μA . The variation of the leakage enhancement was not related in an obvious way to E_b , although it always increased with dose.

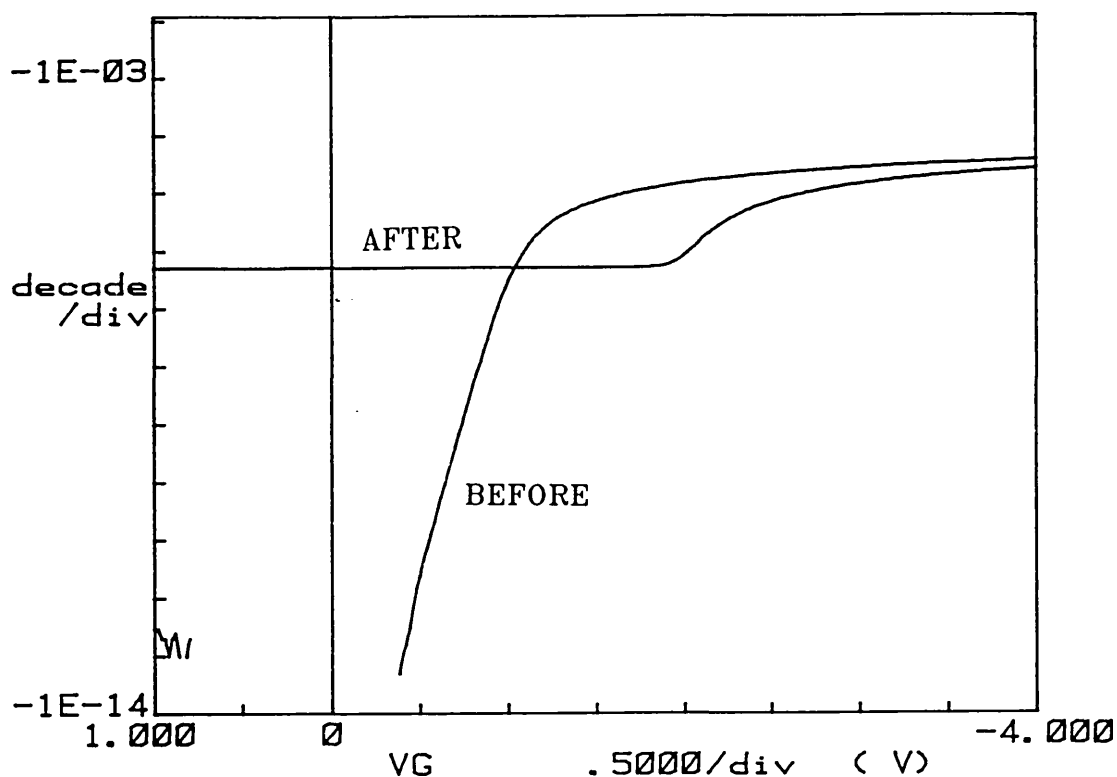


Fig. 46. Drain-source leakage current caused by irradiation.

4.1.7 Non-destructive EBIC

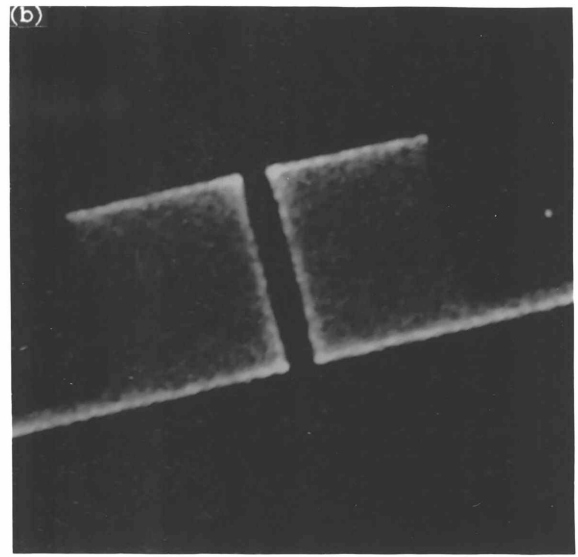
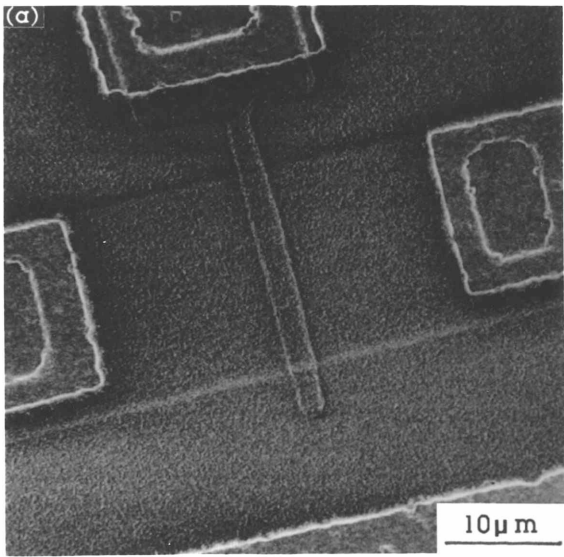
The results of irradiation experiments show that the most important damage is ΔV_t . While leakage currents and mobility reduction occurred, they were only important well after V_t had shifted outside its limits of acceptance. Thus, it was thought that if the dose applied was such that ΔV_t was within acceptable limits, then SEM examination should be non-destructive. In order to confirm this hypothesis, the non-destructive acquisition of an EBIC image of one of the test-transistors was attempted.

To form an EBIC image, electrons must penetrate to the silicon substrate to reach the pn-junctions. This means that the isolation oxide layer must be penetrated. The value of E_b to do this was easily determined as 7 keV,

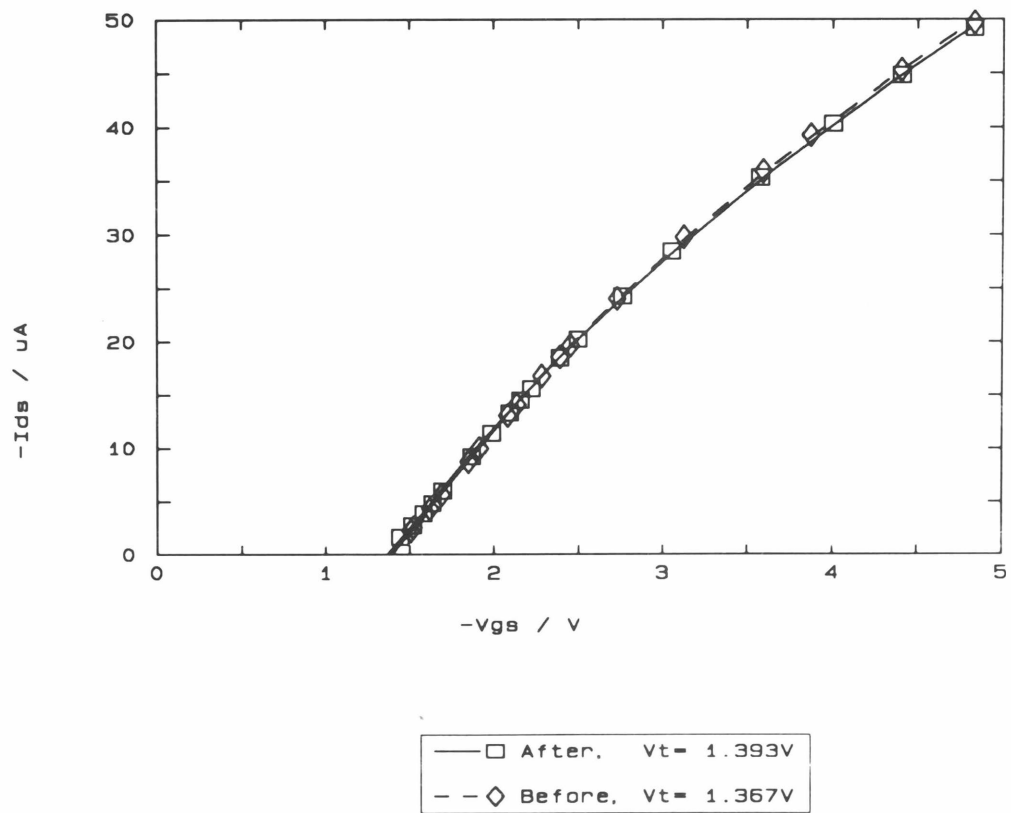
because below this value the isolation oxide would charge strongly. This meant no electron beam conductive path was formed through it to allow the injected beam current to pass to earth via the silicon substrate. Referring to Fig. 37, at 7 keV, to keep $\Delta V_t < 0.1$ V limits the dose to $\approx 5 \times 10^{-6}$ Ccm⁻². Using a small beam current of 10 pA, and with a magnification of $\times 1000$ the safe time of examination can be determined from the dose equation (51) as 54 seconds. The conductance characteristic was first measured and plotted for the test transistor. Then, the transistor was located using $E_b = 1.5$ keV, with negligible damage. The stage coordinates were noted, and a position near the chip edge was sought. After switching to 7 keV, adjusting I_b , and adjusting focus, astigmatism, etc, the beam was blanked using the PCD. Then, on moving to the coordinates of the device the beam could be unblanked, and the EBIC image acquired on the Kontron with only one or two scans. The device characteristic was then re-measured. Fig. 47 shows an SE image taken at 1.5 keV (non-destructively), while (b) shows the EBIC image. Fig. 47c compares the conductive plots before and after image acquisition. The change in V_t of 26 mV was negligible compared to the manufacturing spread. This is believed to be the first example of verifiable, non-destructive EBIC carried out on a radiation sensitive MOS device.

Fig. 47. Non-destructive EBIC of an MOS transistor.

- (a) Non-destructive SE image at 1.5 keV,*
- (b) Limited dose EBIC image,*
- (c) Conductance plot before and after imaging, showing*
 $\Delta V_t = 26 \text{ mV}$.



(c) Device characteristics



4.2 IMAGE PROCESSING

The results presented here are of a study of ways in which image processing can be used as an aid to the location of defects within VLSI circuits. The constraints using a particular standard commercial image processing system, and some ways of surmounting them will be described. It will be shown that the methods are of general applicability although the detailed implementations are specific to the Kontron IBAS system. In this work software was written in the form of 'macros' using the Kontron image processing language to perform new procedures for defect location. A programming library to allow machine-level implementation of extra functions did not become available during the time scale of this project.

4.2.1 Spatial Filtering of Periodic Circuits

Periodic circuit images lend themselves to Fourier transform spatial filtering techniques in order to locate defects. The central problem was finding a suitable masking algorithm to implement the process. Two approaches had been used in the past (Holt *et al*, 1983) to define which spatial frequencies in the power spectrum should be masked out.

(i) Manual mask definition

This involves defining the bright spots in the power spectrum manually. It has the disadvantage of being slow, and requiring manual intervention.

(ii) Using a golden circuit area

The Fourier transform of a perfect region of the circuit is subtracted from the Fourier transform of the test area. On performing an inverse Fourier

transform, only the defects are reconstructed. This method has the disadvantage of requiring a suitable "perfect" area to be defined.

Due to the data storage format in the Kontron image processor, meaningful calculations on $F(u,v)$ could not be easily performed. However, the power spectrum could be calculated using the Kontron FFTDIS function, and a function FFTMSK was implemented, which allowed spatial filtering for an arbitrarily defined mask of the power spectrum (i.e. $|F|$ could be set to zero for any spatial frequencies). In this work, therefore, the most efficient means of producing a mask was sought.

The power spectrum of a periodic circuit image consisted of a regular array of bright spots, corresponding to periodic features in the circuit, and a darker background which contained most of the information due to the irregular defects. It was thought that a way to differentiate between the two would be to apply a binary threshold to the power spectrum. Thus all pixels above a grey level threshold, G_t , were set to black (off), while those below were set to white (on). Using FFTMSK, the value of $F(u,v)$ at each corresponding point was either set to zero or remained unchanged. The resulting $F'(u,v)$ was reverse transformed, and if G_t was chosen correctly, then in principle only defects would remain.

In order to test the above hypothesis, a series of filtering processes was performed, varying the value of G_t , on the memory circuit SE image, shown in Fig. 48a, along with its power spectrum (b). For each value of G_t , Fig. 49 shows (on two pages) the reverse transformed image along with the binary masks that were automatically generated. When $G_t=0$, all of $F(u,v)$ was set to zero, and the result was a blank image. For small G_t , the images contained mostly defects, as the periodic circuit structure was filtered

Fig. 48. Test image for thresholded spatial filtering.

- (a) the secondary electron image of part of a memory integrated circuit with some defects (bright spots),*
- (b) the power spectrum of (a).*

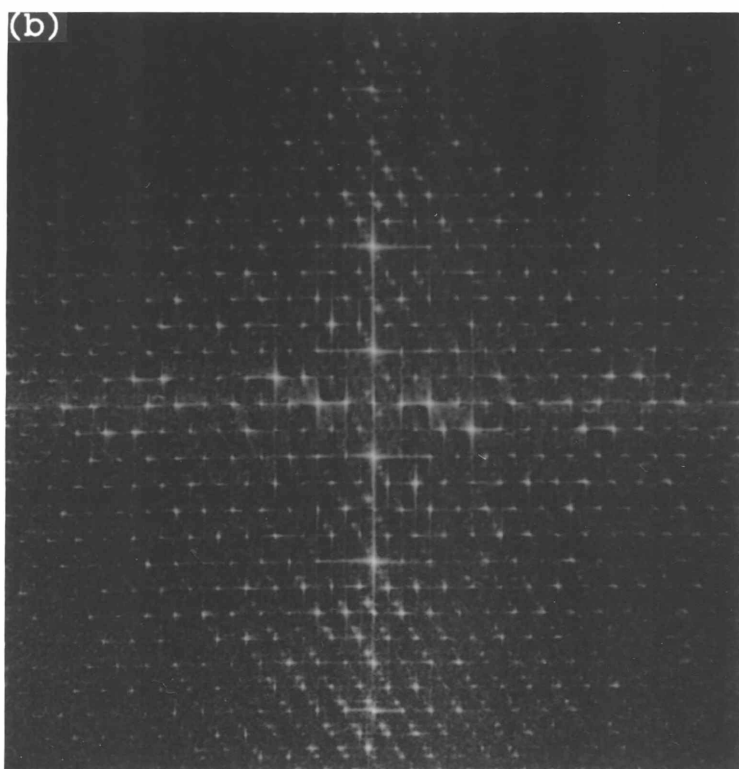
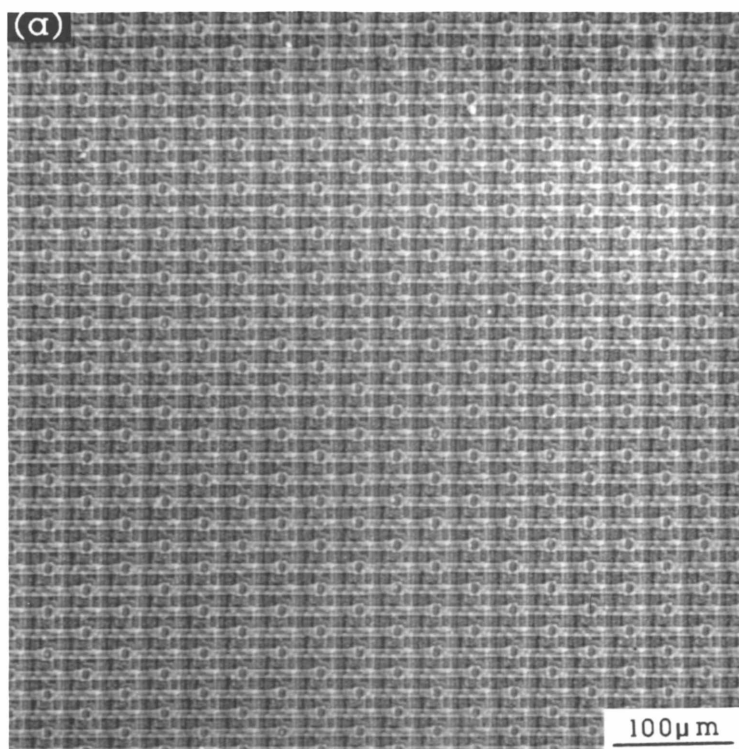
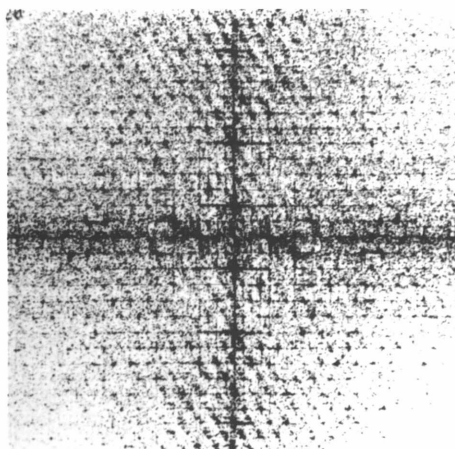
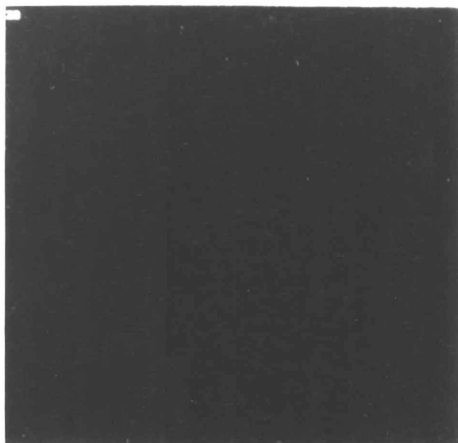
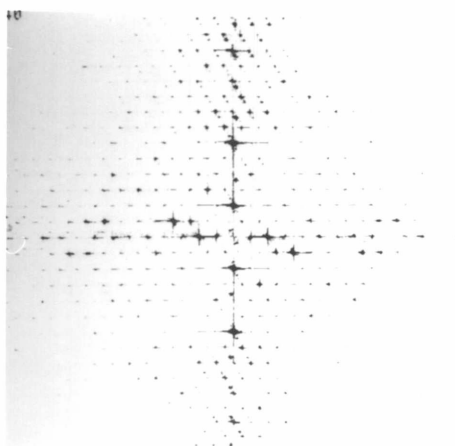
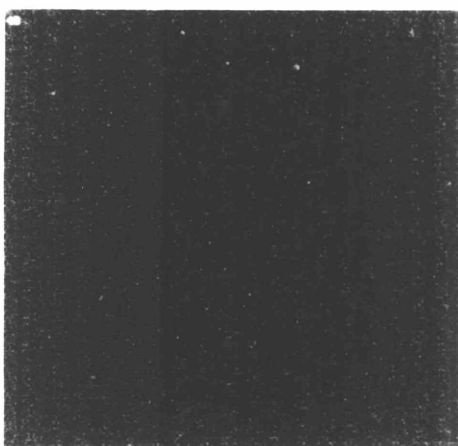


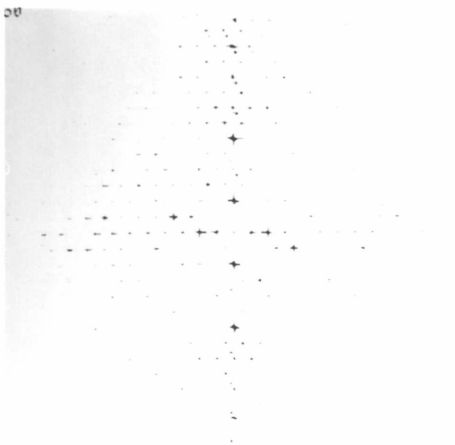
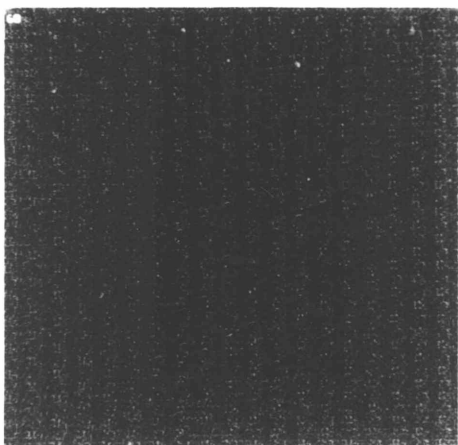
Fig. 49. Opposite and next page: series of spatially filtered images (left) and the binary masks used to generate them (right). G_t was set to the values shown.



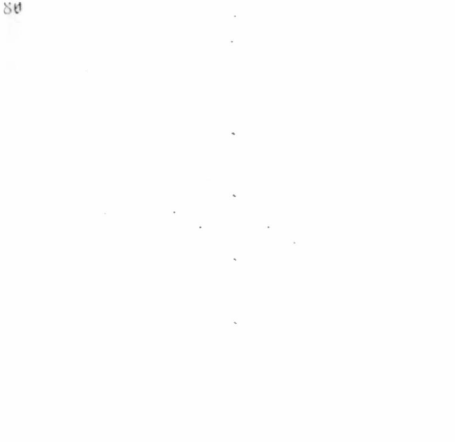
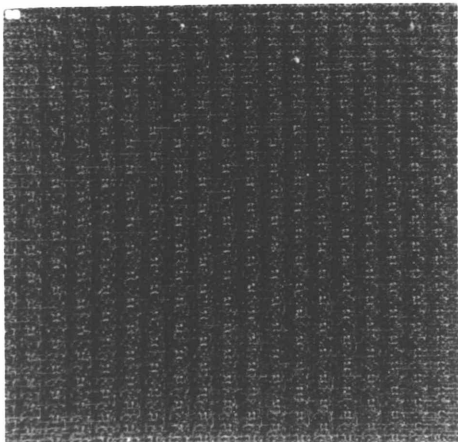
20



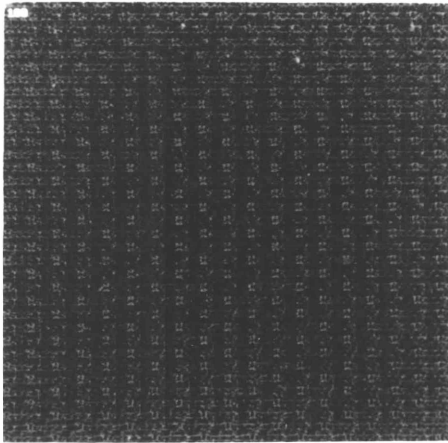
40



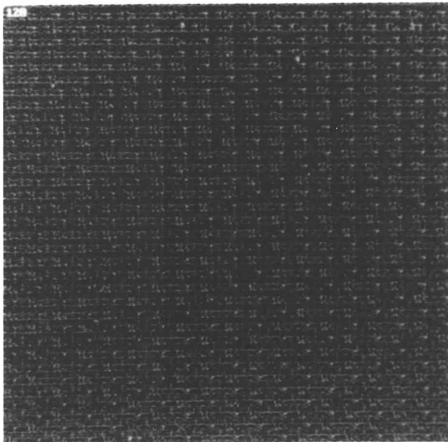
60



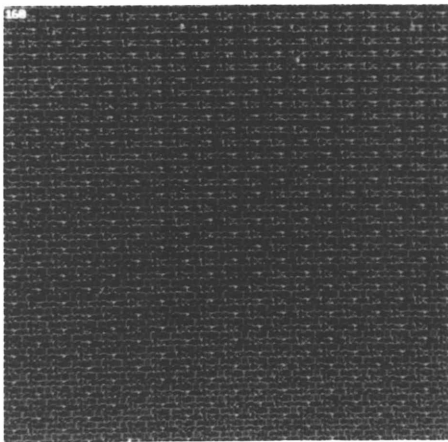
80



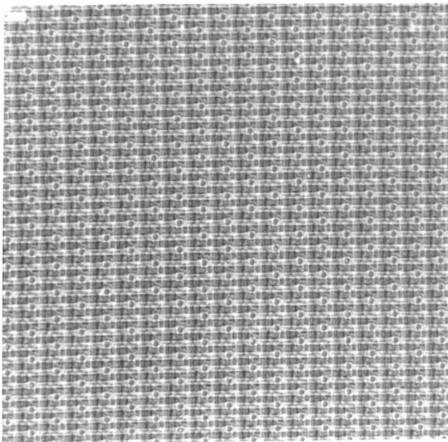
100



120



160



200

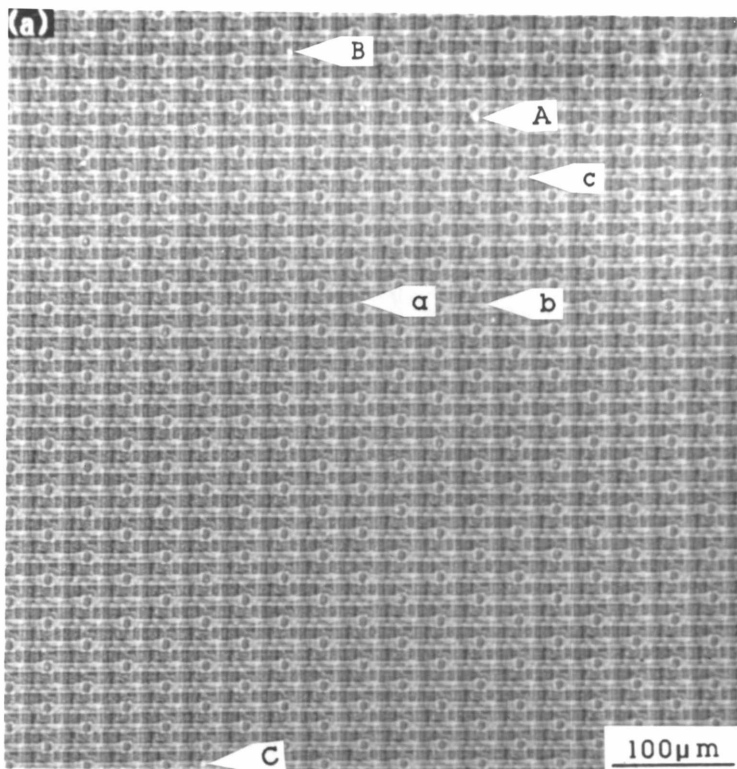
out. Eventually, as G_t increased periodic elements began to break through, until eventually for large G_t , the original circuit was fully reconstructed. The large step at $G_t=200$ corresponds to a threshold which includes the zero-frequency peak (grey level = 200). This point is usually brightest, and corresponds to the average grey-level of the original image (equation 49). However, the most important point is that the value of G_t is not critical, and a value of 50 gives a reasonable compromise between maximising defect brightness, while minimising breakthrough of almost periodic circuit structures (i.e. small perturbations on the regular repeat, such as metallisation irregularities).

With the arrival of version 1.31 of the image processing software it became possible to read grey level values of individual pixels within images. The value of 50 determined in earlier work (Russell and Holt, 1988) was therefore further investigated. For the series of images with varying threshold, grey values were measured at pixels in:

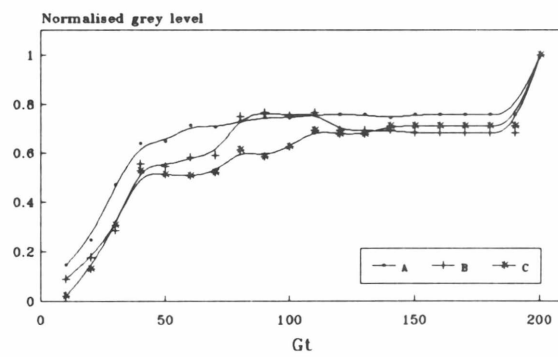
- (i) defects,
- (ii) parts of the circuit which "break through", such as bright metallisation edge irregularities.

The defects (A-C) and circuit pixels (a-c) are labelled in Fig. 50a. Each grey level was written to a disk file for plotting. The grey values were normalised to their value in the original image for comparability, and were plotted against G_t . The sharp step at $G_t = 200$ in both defect and circuit graphs (Fig. 50b,c) was due to reconstruction of the zero-frequency component as discussed above. In the defect plots (Fig. 50b), an initial region shows very low grey levels (poor visibility), followed in most cases by a very pronounced shoulder, before a steady increase towards the final

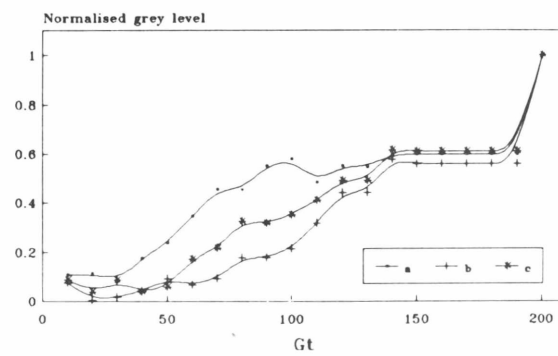
Fig. 50. The variation of pixel intensity with filtering threshold, G_t .
(a) location of defects (A–C) and circuit features (a–c) tested,
(b) Normalised defect grey level vs G_t ,
(c) Normalised circuit grey level vs G_t .



(b) Defects



(c) Circuit break-through



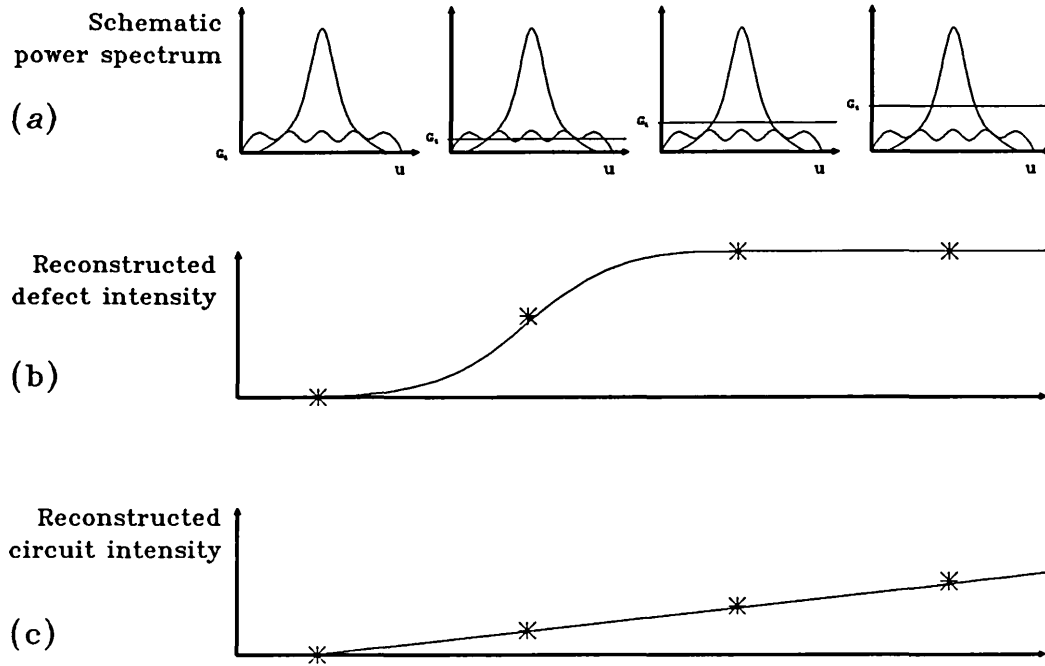


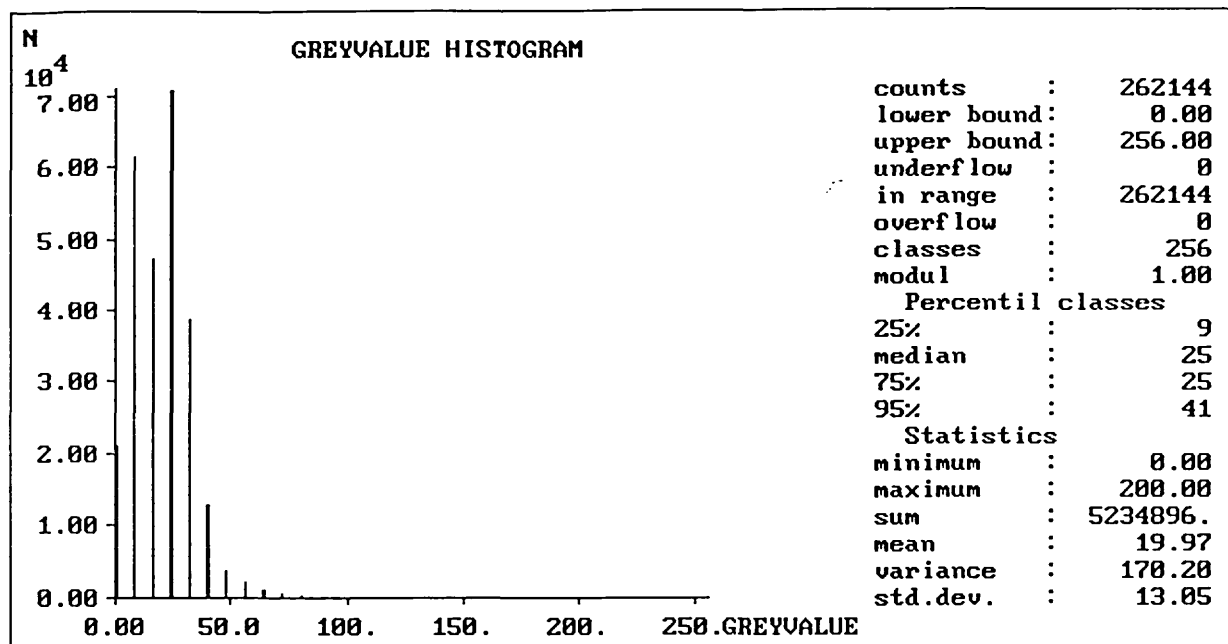
Fig. 51. Explanation of the behaviour observed in Fig. 50.

level. In isolation, this suggests any value of G_t above 50 was suitable. However, considering the circuit breakthrough due to quasi-periodic circuit features (Fig. 50c) the increase in intensity is more steady, without a shoulder. The conclusion was therefore that the exact value of G_t was not that critical, and a wide range of G_t values were acceptable. Nevertheless, it was optimised at values just above the shoulder, at a value of 50, in fact. This is a quantitative vindication of the earlier pictorial result.

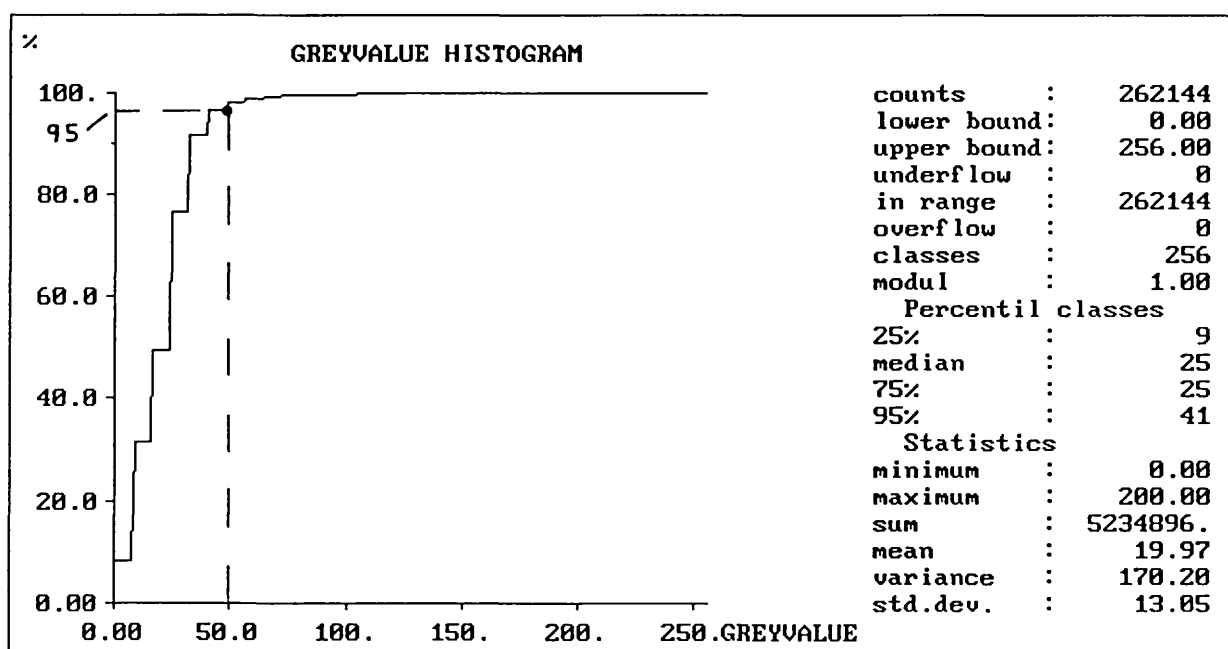
Although the form of these two curves explains why $G_t = 50$ works, the reason for two such different behaviours is less clear. It is believed that their origin can be justified by reference to the spot structure in the power spectrum. The spots are not point-like, but extend over several pixels, due mainly to small deviations from perfect periodicity. In Fig. 51 this is represented at the top (a) by plots of power spectrum grey level vs spatial

frequency, u . Each graph shows the same small area near one power spectrum spot, and consists of a peak for the spot surrounded by a low amplitude background for the defects. In each of the plots spatial frequencies, at which the power spectrum is above G_t are eliminated. On average, the number of spatial frequencies from a circuit or defect feature that are included will be proportional to the reconstructed brightness of the feature. Thus, as G_t is increased from zero in Fig. 51a on the left, low-level defect information is soon fully reconstructed, and the defect intensity (b) levels off. For the periodic features, more of the main spot is still being included, and the circuit intensity continues to increase much longer (c). Thus the trends of the plots in Fig. 50 are explained.

The threshold value of 50 was, of course, dependent on the details of the power spectrum calculation in the Kontron. It was thus necessary to generalise this result so it was useful for other systems. A more suitable viewpoint was suggested by considering the power spectrum image histogram (Fig. 52a). The vast majority of pixels were dark (small grey values). The bright spots in the power spectrum occupied such a small area that they did not show on the scale of the histogram. Hence another way of looking at the thresholding argument was to eliminate spatial frequencies corresponding to a fraction of power spectrum pixels which were brightest. Referring to the cumulative histogram of Fig. 52(b), the threshold value of 50 corresponds to a darkest area fraction of 0.95. The advantage of this viewpoint is that it does not depend on the details of how the power spectrum is calculated (e.g. logarithmic lookup table, $|F|^2$ or $|F|$, etc). As long as the "power spectrum" function of an image processor increases monotonically with $|F|$, then spatial frequencies from the 95% darkest pixels will reconstruct only defects. In fact, using this approach in collaboration with the GEC group, spatial filtering was successfully carried out on their



(a) Image histogram – plot of frequency of occurrence vs grey level.



(b) Cumulative image histogram

Fig. 52. Image histograms of the power spectrum. It is quantised due to the simple (fast) algorithm used to calculate it. In (b) the cumulative histogram is shown, and from the construction, when $G_t=50$ this corresponds to an area fraction of 95% of the darkest pixels.

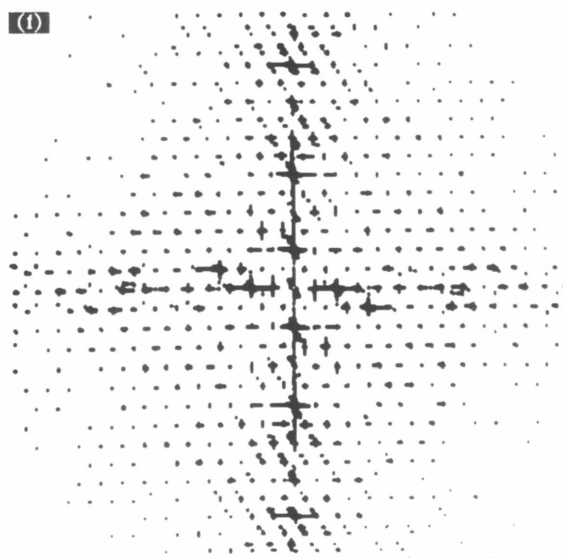
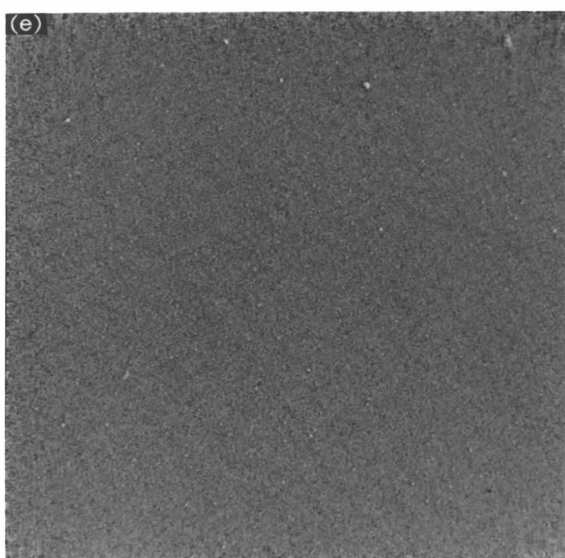
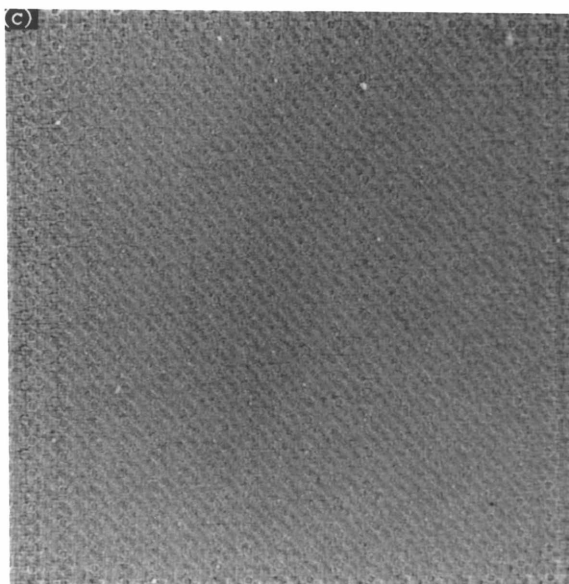
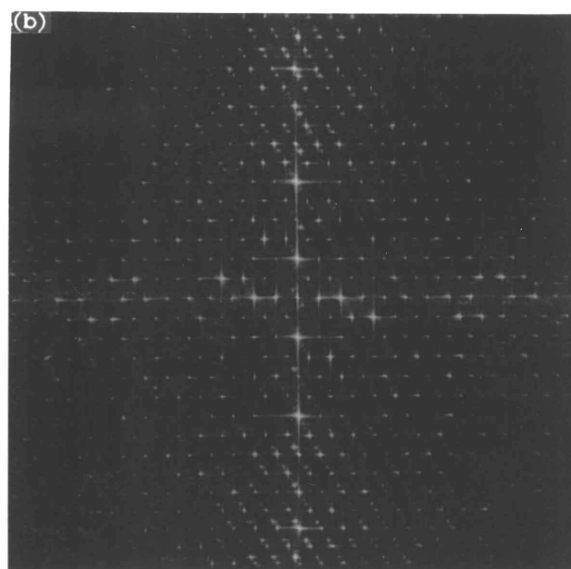
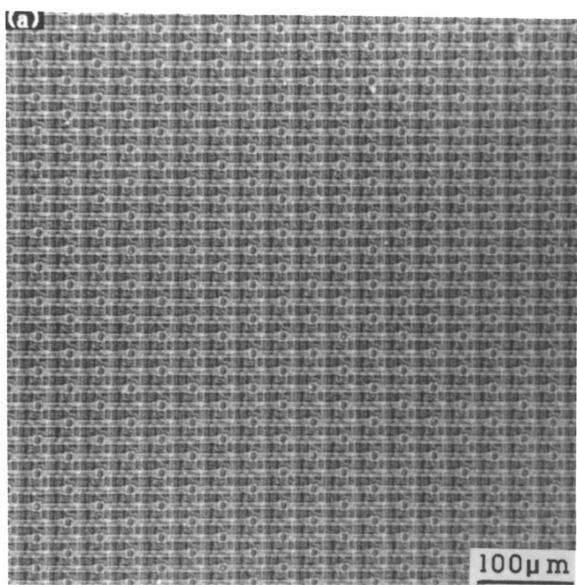
Data Translation equipment which used the SEMPER image processing language. (ALVEY 104 project, GEC class 1 report, 29/3/88).

The thresholding routine could still not locate dark defects effectively. On performing the inverse FFT, their values tended to be too low and were automatically clipped by the Kontron FFTINV function. An initial solution was found to be simply to use the original image with inverted greyscale. However, the best way was to ensure that the zero-frequency component of the power spectrum was not filtered out, thus retaining the average image grey-level so that both dark and bright defects were visible. Early attempts at this were frustrated by a bug in the FFTDIS and FFTMSK functions. These had a relative offset in their coordinates of one pixel, making their superposition close enough for spatial filtering, but useless for setting of the zero-order peak. Once discovered, this was fixed by a pre-shifting of the power spectrum. At this point, it is pertinent to note the importance of such problems, as we are firmly in the hands of the software writers. Experience has shown that it is extremely difficult to obtain documentation on exactly what many routines do, and how they work. This can greatly hamper "non-standard" applications such as those developed for this project. Careful checking is always necessary.

In Fig. 53a,b the original image and power spectrum are repeated for convenience. Fig. 53c shows the reconstructed image, and its mask (d) when the optimum threshold of 50 is used and the zero-frequency component is retained. The result is more visually pleasing than the comparable image of Fig. 49. There is some breakthrough of circuit structure around the periphery of the image because with the discrete Fourier transform, the original image is assumed to "wrap around" (equation 47a). As a consequence of this there are sharp changes in

Fig. 53. Optimised spatial filtering with $G_t=50$, retaining the zero frequency peak.

- (a) original SE test image,*
- (b) power spectrum,*
- (c) spatially filtered image,*
- (d) mask for (c),*
- (e) spatially filtered image using dilation of the mask,*
- (f) dilated mask for (e), using octagonal structuring element.*



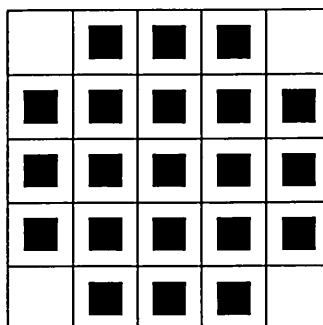


Fig. 54. Octagonal structuring element.

grey-level present at the image edges which require a large number of spatial frequencies to reconstruct precisely by $F(u,v)$. They are therefore more easily disrupted by a spatial filtering process. The affected region is, however small, and can be easily neglected. The second, more noticeable effect is the diagonal banding across the image. This is due to breakthrough of a particular spatial frequency from the original image which was part of the circuit, but led to a point in the power spectrum which was just below the grey-level threshold. It was thus apparent that thresholding of the power spectrum alone was not sufficient to fully suppress all the circuit features. It was then thought that although thresholding would pick out the most important spatial frequencies, a few pixels surrounding them (below the threshold) were also important. Therefore, to improve the results further, it was necessary to add a layer of pixels around each spot in the mask. This was carried out using a dilate function on the power spectrum mask. Dilation is often used in particle shape analysis, and acts on a binary image to add a further layer of bright pixels around every bright pixel in the original image. Of course this can be done more than once to envelop a larger area around the spots, but the spatial filtering results proved to be relatively insensitive to this, once two or more layers were added. Only

one dilation was required if an octagonal structuring element, (Fig. 54) was used instead of a single pixel. This gave the mask of Fig. 53f, using which the reconstructed image of (e) was produced. All periodic breakthrough was then completely suppressed.

4.2.2 Spatial filtering of Non-Periodic Circuits

Many integrated circuits are not ideal for the thresholded spatial filtering described above. However, all integrated circuits have a certain degree of regularity, in terms of constant metal track widths, horizontal and vertical alignment, etc. This ordering suggested that it was possible to suppress the circuit pattern to some extent, emphasizing the appearance of any defects which might be present. The SE image of a CMOS ASIC was chosen as an irregular circuit test image (Fig. 55a). It contained two bright spots which might be aluminium hillocks, or particles (labelled P), and mechanical damage of an aluminium metal track (labelled M). The power spectrum of (Fig. 55b) this image contains no bright spots like those of Fig. 48b.

An alternative to processing in the frequency domain is to do convolutions directly in the temporal domain (equation 41). This has the overwhelming advantage of speed, especially if carried out using an array processor. Convolutions are commonly used for low-pass filtering (smoothing), general edge enhancement, etc. Here, the most useful were directional edge detection methods. A simple edge detector was described in section 2.5.1. In practice such filters were programmed using the Kontron "userfilt" function, and the result was also normalised to fit the 8-bit greyscale. They detect vertical and horizontal edges respectively, but to do this they completely suppress edges at 90°. Edges of other orientations are suppressed

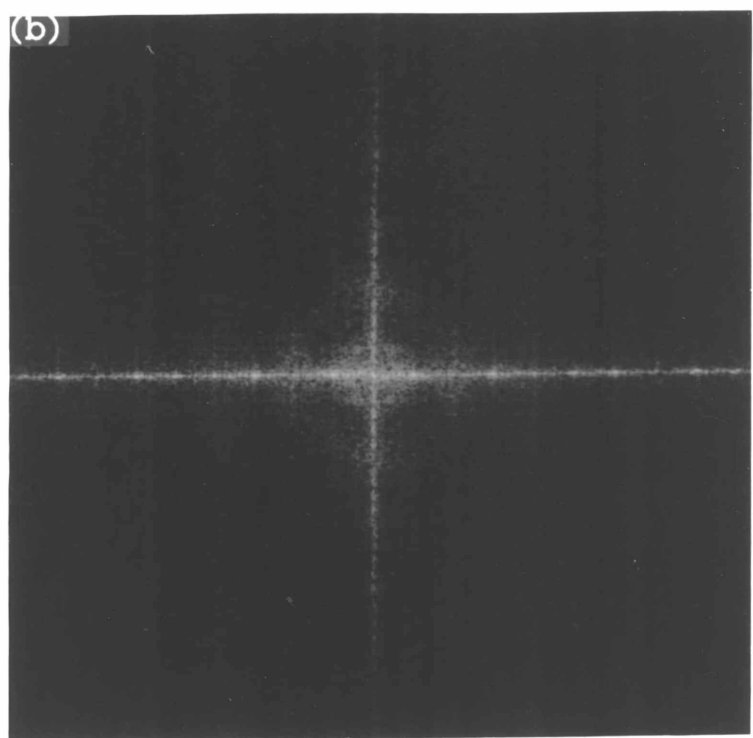
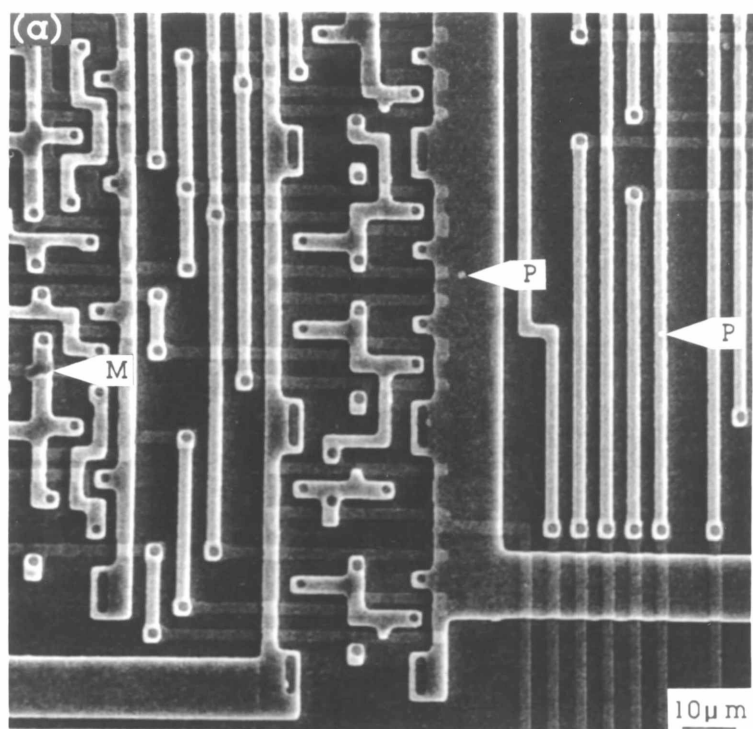
Fig. 55. Non-regular test image, chosen to contain some long, straight metal tracks and also shorter, more complex logic gates.

(a) SE image containing

P – metal hillocks or particulates,

M – metallisation damage

(b) power spectrum



to an intermediate extent. Thus, in principle, sequential passes of both filters should suppress edges in both the x and y directions. Several variants on these simple matrices are possible (Rosenfeld and Kak, 1982, p. 98). Images processed using some of them are shown in Figs. 56–59 in each case processed by (a) vertical suppression, (b) horizontal suppression, and (c) both filters. On using both filters (cases (c)), features such as contact windows result in confusing artefacts, and make location of the defects almost impossible. An exception is Fig. 59c, in which the edges were uniformly enhanced. In all cases (a) and (b), either vertical (a) or horizontal (b) detail was well suppressed, with the first filter (Fig. 56) giving the best results. However, as a means of defect location convolutions are limited to very favourable cases. Parallel, vertical metal tracks which are common in ASICs for example, were searched well in the right side of Fig. 56a, delineating both defects P. The metal defect, M in a less structured part of the circuit was not successfully enhanced.

Convolutions are limited in that they usually only operate on a small region (3×3 pixels in the examples of Figs. 56–59). If Fourier transform methods are used, in effect, a 512×512 convolution is performed. Applying the thresholded spatial filtering algorithm to the irregular circuit test image (repeated in Fig. 42a), resulted in (c) using the mask of (d). A lot of the circuit detail is suppressed, especially the long metal tracks. The more irregular logic gates remain, and an irregular background is introduced. The bright spots are slightly more visible, but the metal defect remains poorly defined. If the dilation was incorporated as well, the mask (Fig. 60f) fits the four lobes present in the power spectrum (Fig. 55b) better, and most of the circuit information was gone from the reconstructed image of (Fig. 60e). The defects were also less bright, however. An alternative strategy is to use an x - y filter in the shape of a "+" cross. Fig. 60b was obtained with

-1	-1	-1
0	0	0
1	1	1

-1	-2	-1
0	0	0
1	2	1

-1	0	1
-1	0	1
-1	0	1

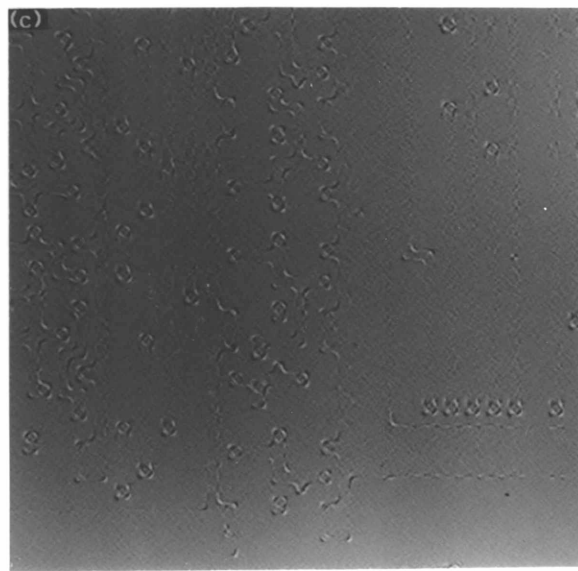
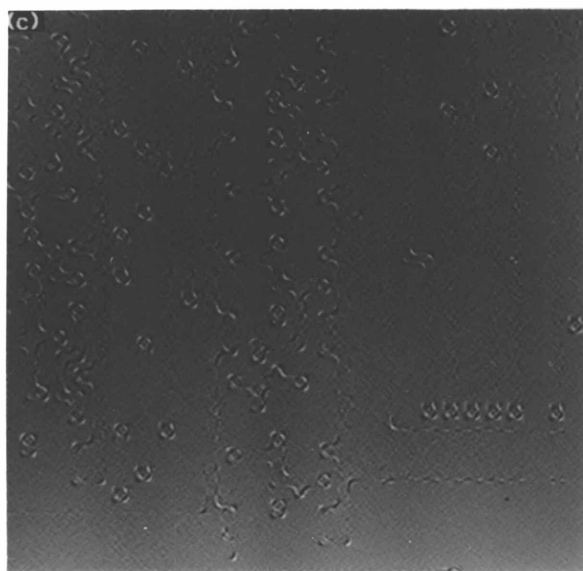
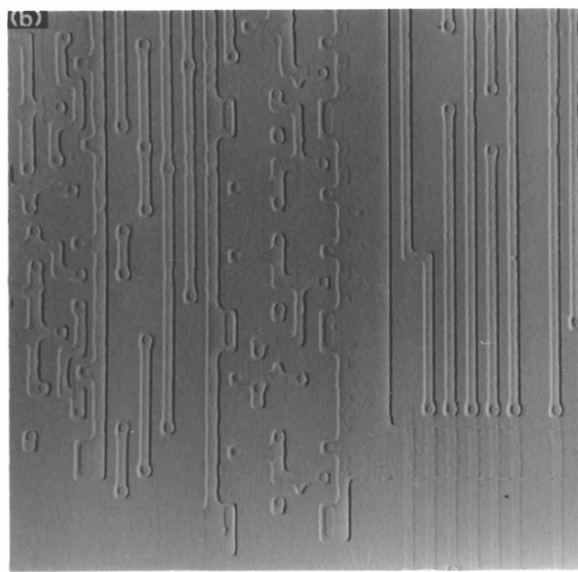
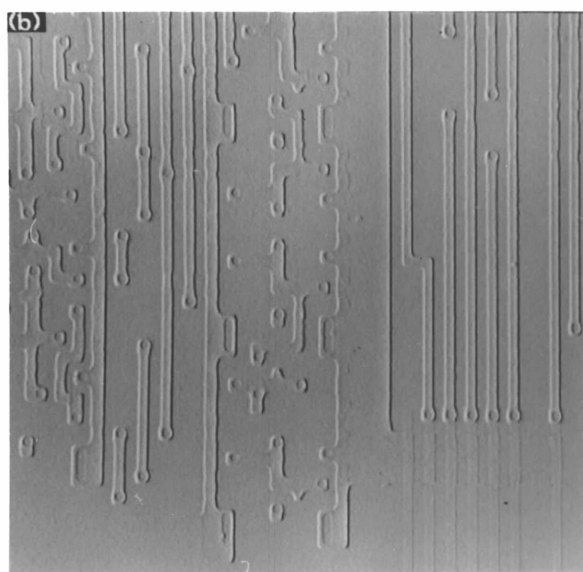
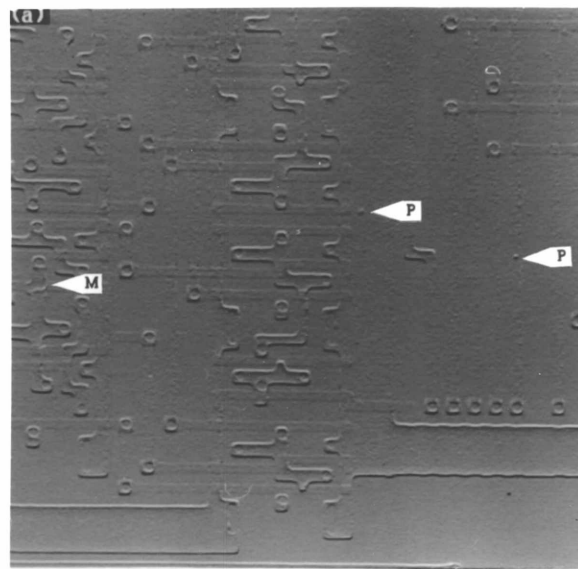
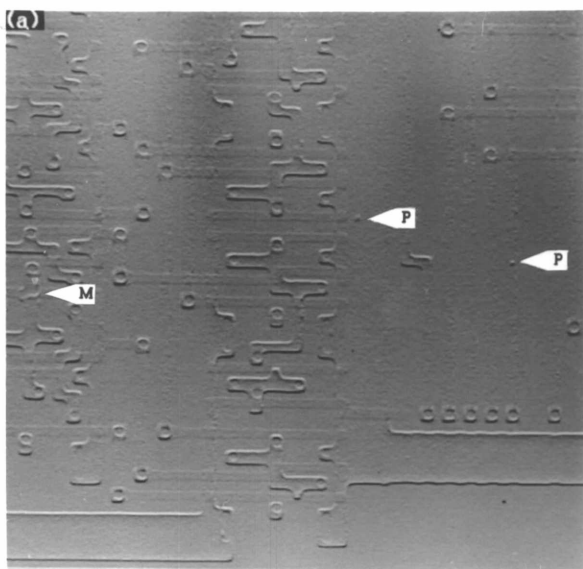
-1	0	1
-2	0	2
-1	0	1

*LEFT**RIGHT*

*Fig. 56. Selective edge suppression by convolution.
(a),(b) using filters above,
(c) using both.*

*Fig. 57. Selective edge suppression by convolution.
(a),(b) using filters above,
(c) using both.*

Test image was Fig. 55a.



-1	-1	-1	-3	-3	-3
1	-2	1	-3	0	-3
1	1	1	5	5	5

-1	1	1	-3	-3	5
-1	-2	1	-3	0	5
-1	1	1	-3	-3	5

LEFT

RIGHT

Fig. 58. Selective edge suppression by convolution. (a),(b) using filters above, (c) using both.

Fig. 59. Selective edge suppression by convolution. (a),(b) using filters above, (c) using both.

Test image was Fig. 55a.

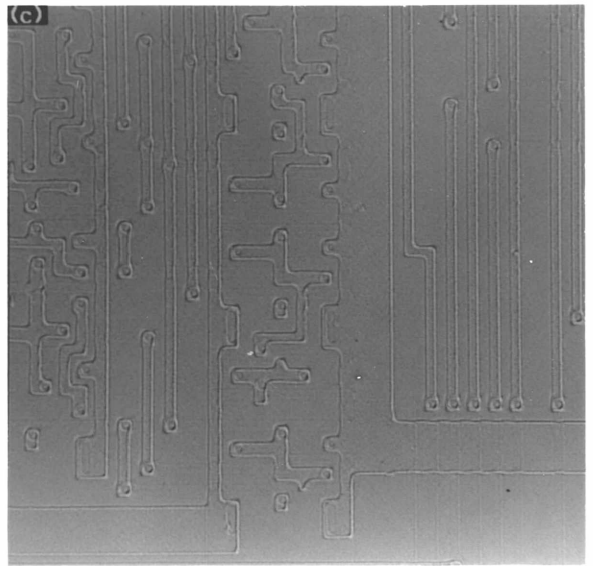
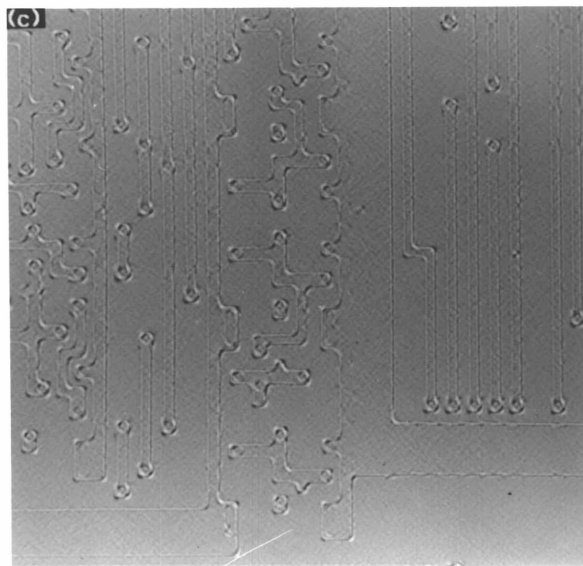
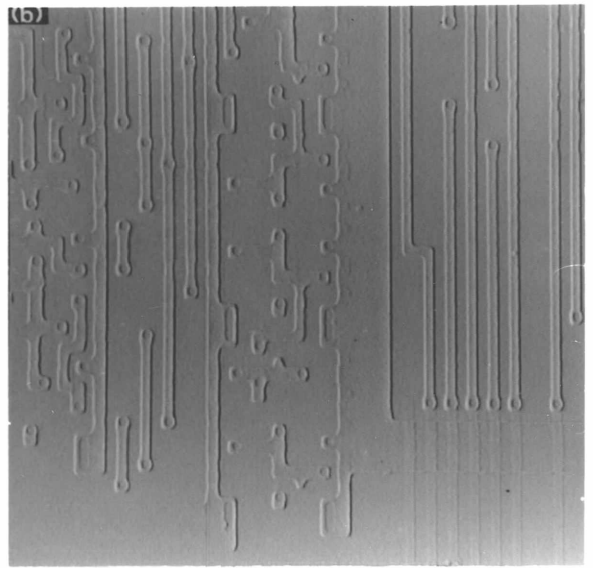
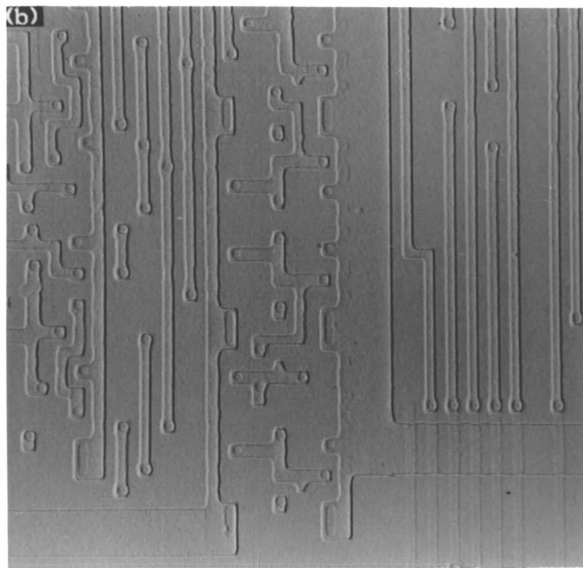
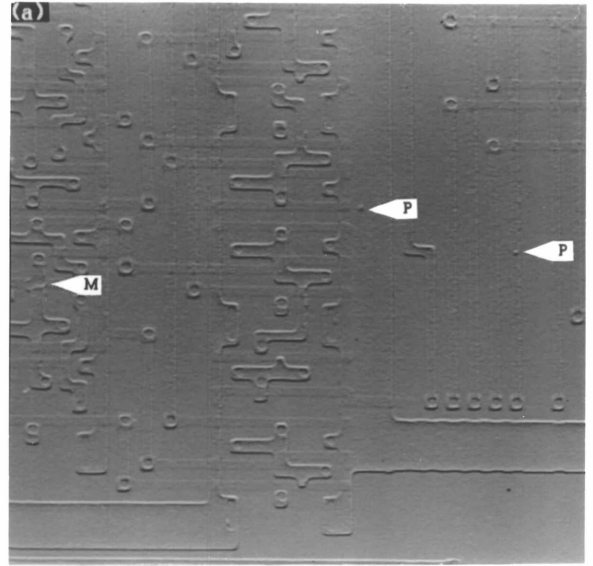
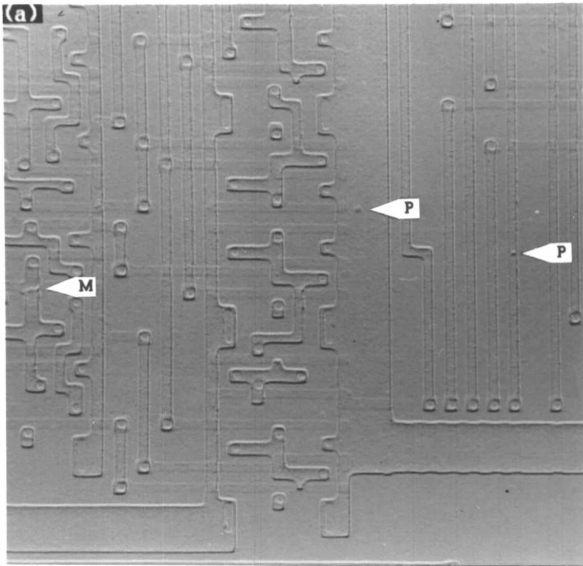
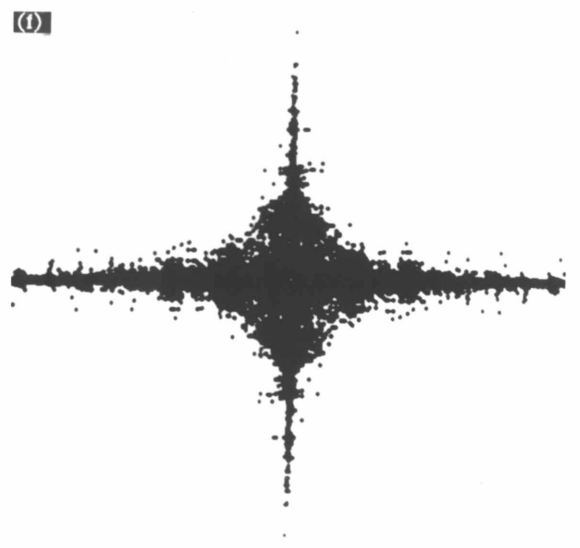
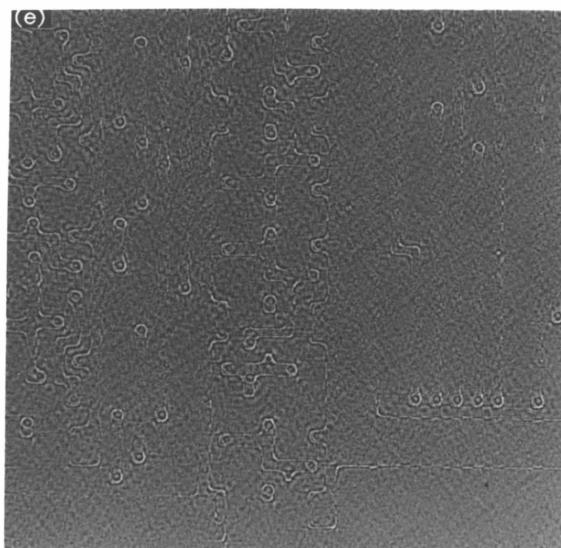
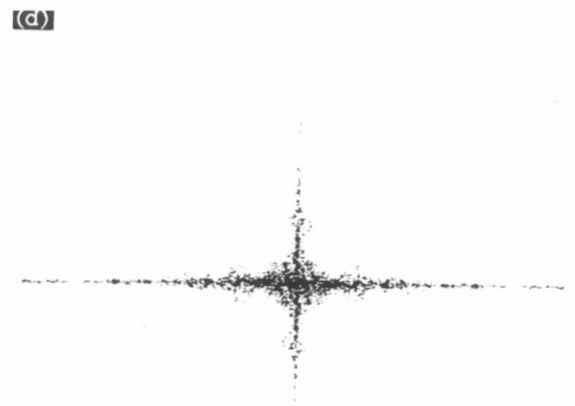
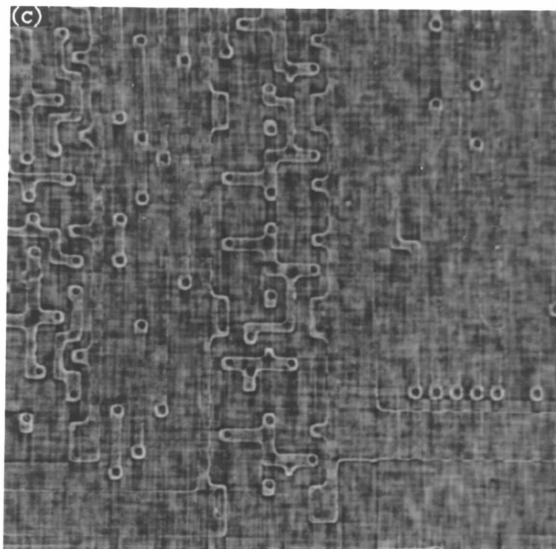
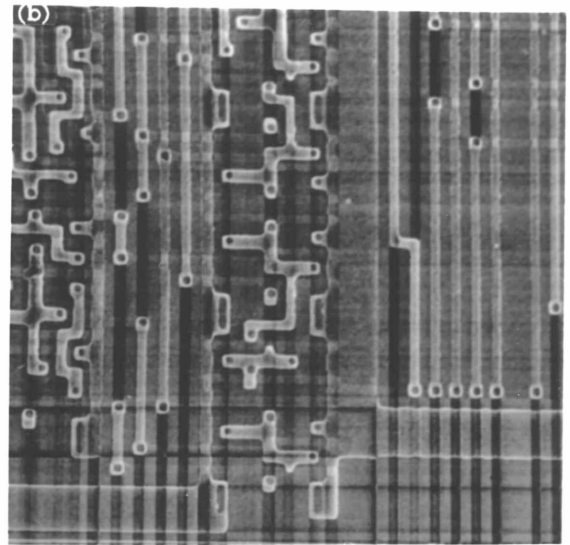
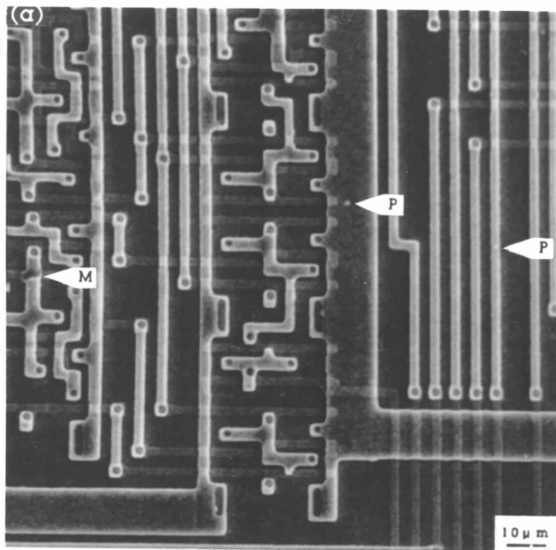


Fig. 60. Spatial filtering of an irregular IC.

- (a) Test image (same as Fig. 55),*
- (b) spatially filtered image using a 1 pixel wide "+" shaped filter,*
- (c) image after thresholded spatial filtering,*
- (d) mask for (c),*
- (e) spatially filtered image using thresholding and dilation,*
- (f) mask for (e).*



a one pixel-wide cross. The image of Fig. 60b is clearly no better than that obtained using the other two methods, as it contains very strong artefacts, such as the dark lines where the long vertical metal tracks are discontinuous. However, the power spectrum (Fig. 55b) suggests the bars of the cross should be widened. Fig. 61 shows a series of reconstructed images with varying "bar thicknesses". As the thickness increases, the longer dark-line artefacts disappear (Fig. 61d), but the contact windows remain. At this stage, the reconstructed images are very similar to those obtained much more quickly by direct convolution.

4.2.3 Spatial Filtering Case Studies

The first example is of a metallisation fault in the memory section of a telecommunications ASIC. The SE image (Fig. 62a) has a rather large, periodic motif, but is also strongly ordered on a much shorter scale, thus the power spectrum (b) is quite complex. The spatially filtered image in Fig. 62c delineates the defect quite well, using the mask of (d). However, the background is rather uneven with pronounced vertical bars. One reason for this is a second low frequency component in the original image, due to extra vertical metal tracks (in every fourth vertical group). When the normal spatial filtering algorithm was combined with a cross filter (1-pixel wide), most of the vertical lines were removed (Fig. 62e). If the mask (d) was dilated the results were even better (Fig. 62f). This is because the dilated mask actually duplicates most of the cross anyway, but also enhances suppression of higher order harmonics. In Fig. 63a, the backscattered electron image of the same region is shown. In this case, the original image is less dominated by topography, so the defect is more clearly visible in the spatially filtered images (Fig. 63c,d), as it has a larger area (the SE defect

Fig. 61. Spatially filtered images (left) using a cross-filter (right) of increasing size (a – e).

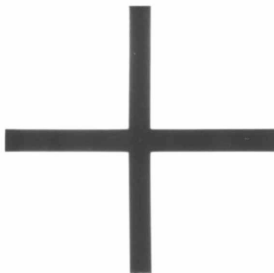
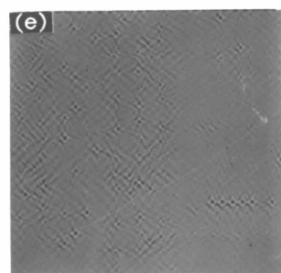
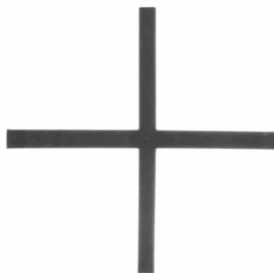
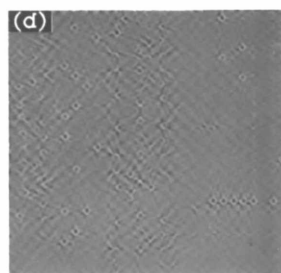
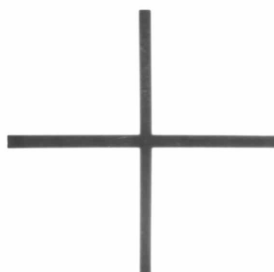
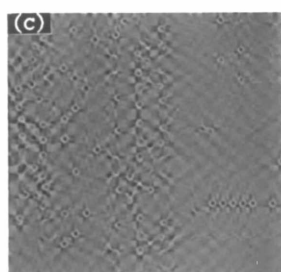
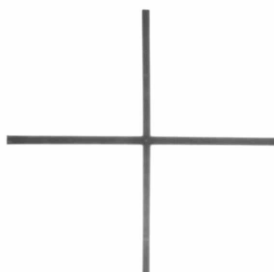
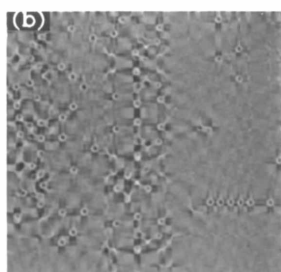
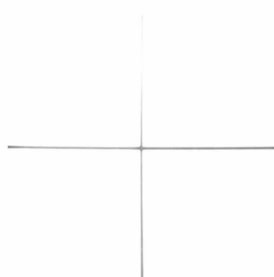
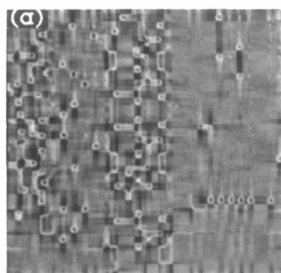


Fig. 62. Spatial filtering of the SE image of a CMOS ASIC.

- (a) SE image,*
- (b) power spectrum,*
- (c) image after thresholded spatial filtering,*
- (d) mask for (c),*
- (e) spatially filtered image using thresholding, but adding a cross to the mask,*
- (f) spatially filtered image using thresholding and dilation.*

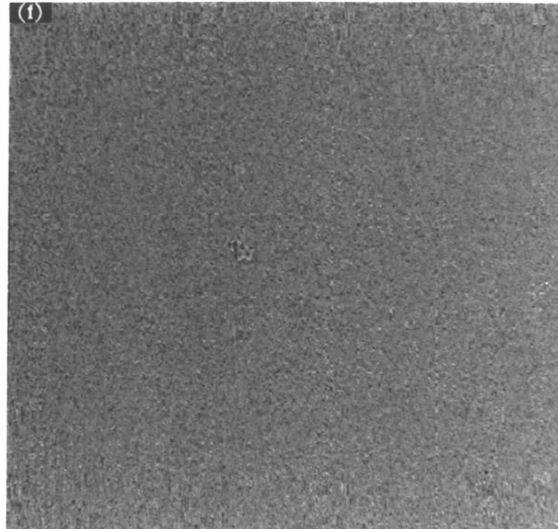
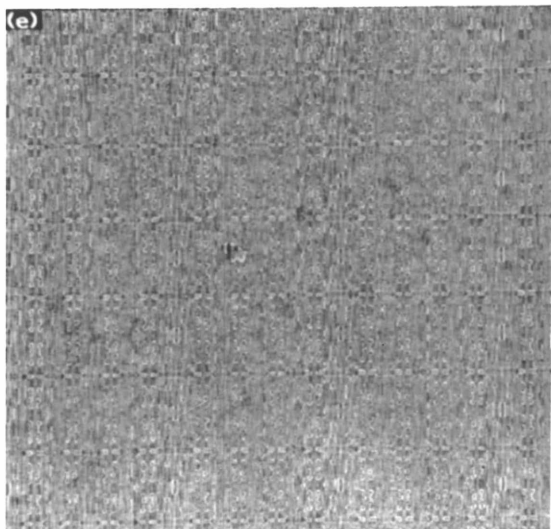
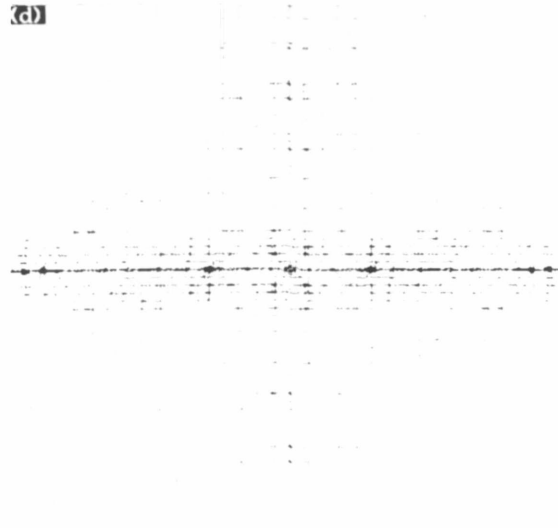
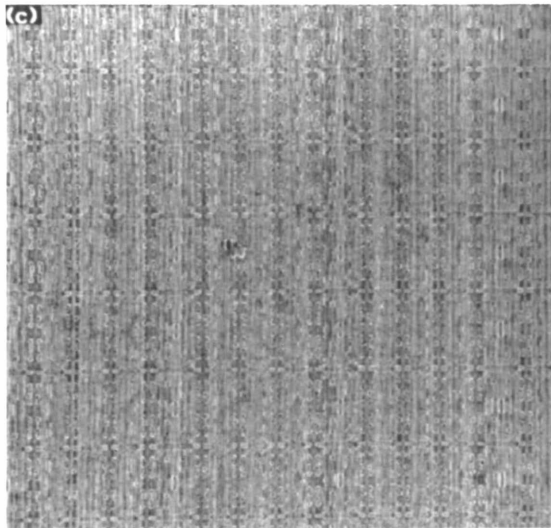
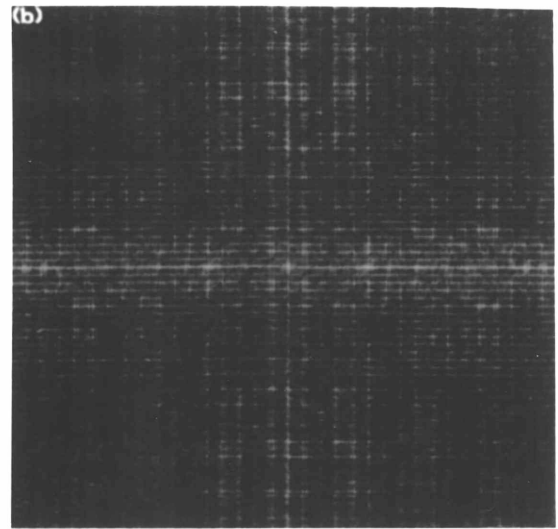
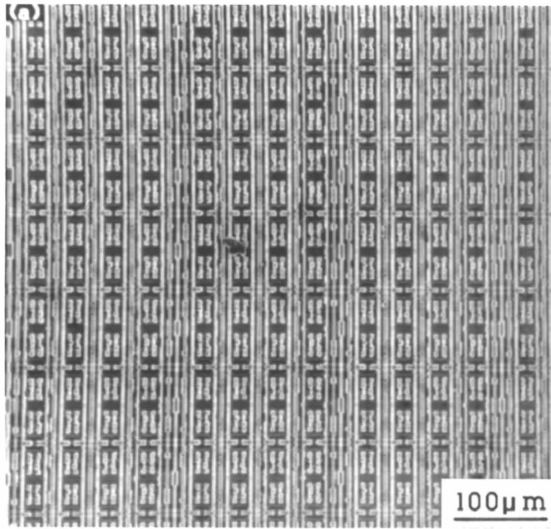


Fig. 63. Spatial filtering of the back-scattered electron image of the same area as in Fig. 62a.

- (a) backscattered image,*
- (b) power spectrum,*
- (c) image after thresholded spatial filtering,*
- (d) spatially filtered image using thresholding and dilation.*

Fig. 64. Back-scattered (left) and SE (right) images of the defect of Figs. 62a and 63a.

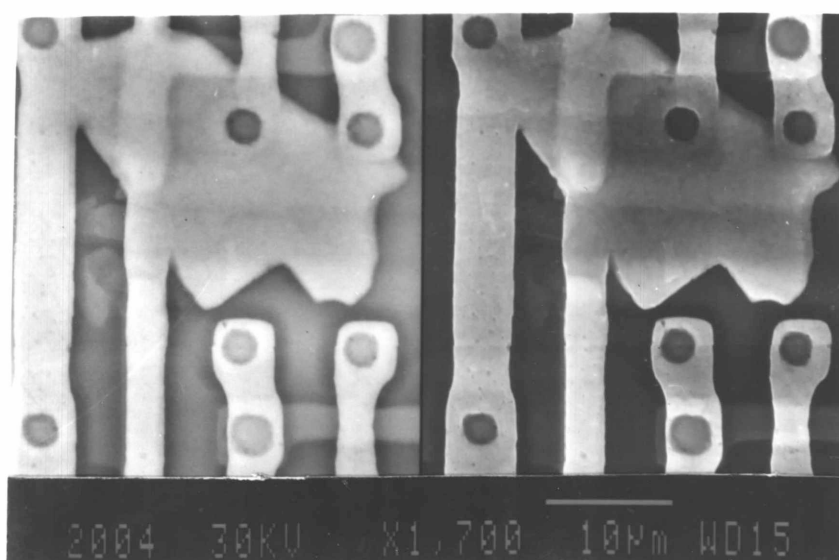
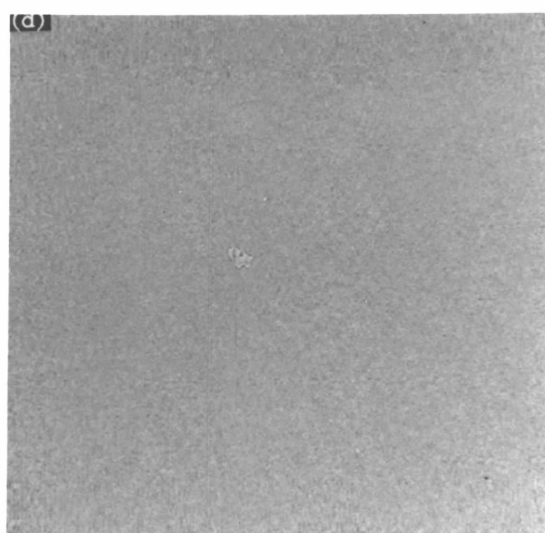
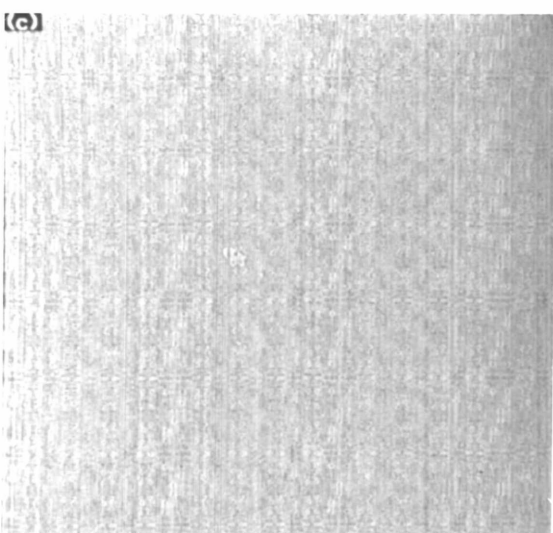
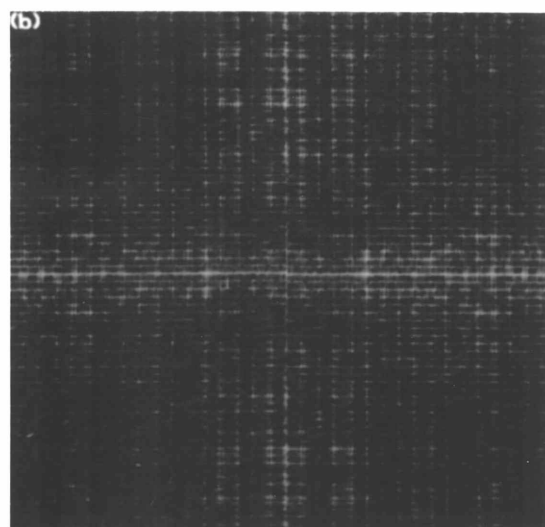
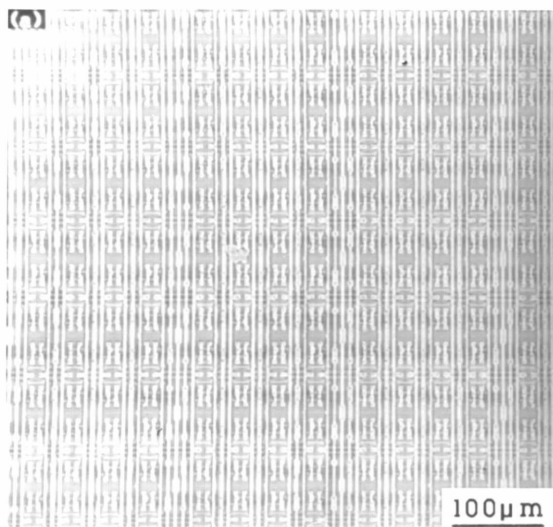


image is dominated by its edges, which are less easily visible). At higher magnification (Fig. 64) the defect could be seen to be continuous with the metallisation, and so could be identified as due to under etching or a mask defect.

An EBIC image of a CCD (Fig. 11b) image sensor chip is shown in Fig. 65a. It was obtained by making connections to the substrate and one of the gate electrodes. I_{sc} is transmitted to the EBIC amplifier by a combination of capacitive coupling and beam induced conductivity through the gate oxide. The electrodes run from top left to bottom right, and are shown in Fig. 65b, and in its spatially filtered image in (c), using the mask, (d). In (c) a line defect is apparent, and using dilation as well (e,f), both circuit information and edge effects were suppressed better. The line-defect was first thought to be similar to that observed by Lesniak *et al* (1984). However, on closer scrutiny this was discovered to be an artefact due to beam damage. The JEOL 840A has a delay in the x-scan cycle at the left-hand side of the image to allow for beam flyback. This led to a strongly enhanced radiation dose at the point at the end of the line scanned, and thus lines of localised radiation damage along the left-hand edge of the frame. Patterns of damage due to the whole frame were also present, but were less apparent for short observation times. The darkening effect was due to a local shift in the threshold characteristics of the gate electrodes, similar to those observed on discrete devices in section 4.1.

In Fig. 66 an SE image from the edge of the active area of a CCD chip was taken. In this case, the image was not completely periodic, although the power spectrum (Fig. 66b) indicated a number of regular structures, due to the substantial periodic parts of the image, in the x-direction. The resulting image after applying spatial filtering (Fig. 66c) was quite good,

Fig. 65. Filtering sequence for the EBIC image of a CCD taken with connections between the substrate and one of the gate electrodes.

- (a) original image,*
- (b) power spectrum,*
- (c) filtered image using thresholding, showing a "line defect",*
- (d) mask for (c),*
- (e) spatially filtered image using thresholding and dilation,*
- (f) mask for (e).*

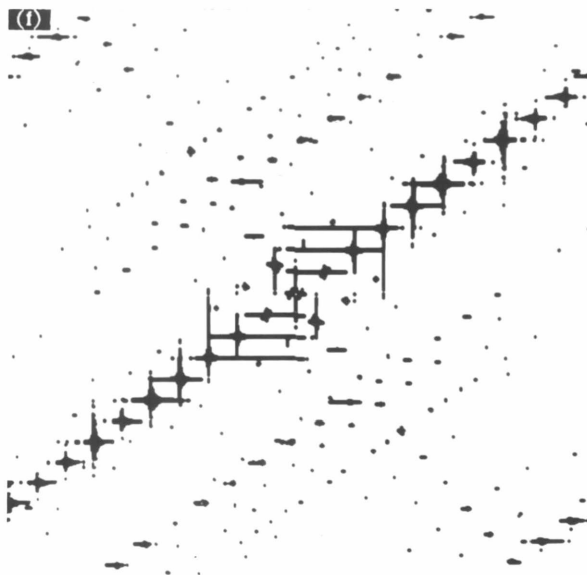
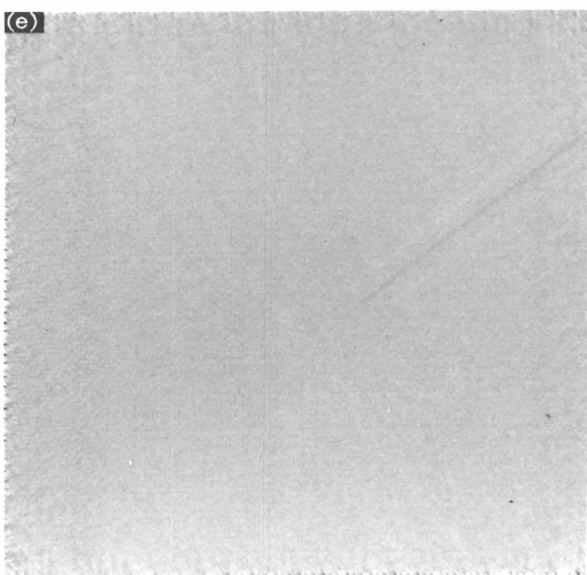
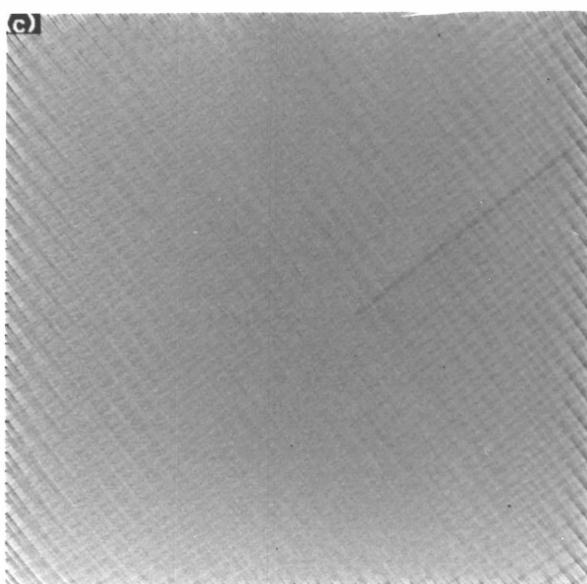
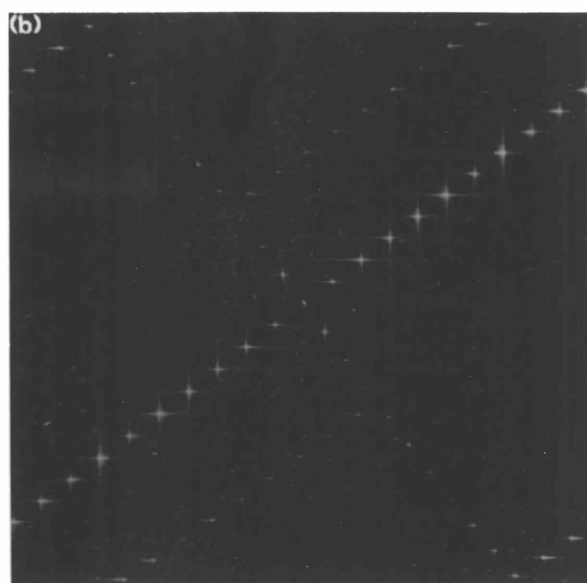
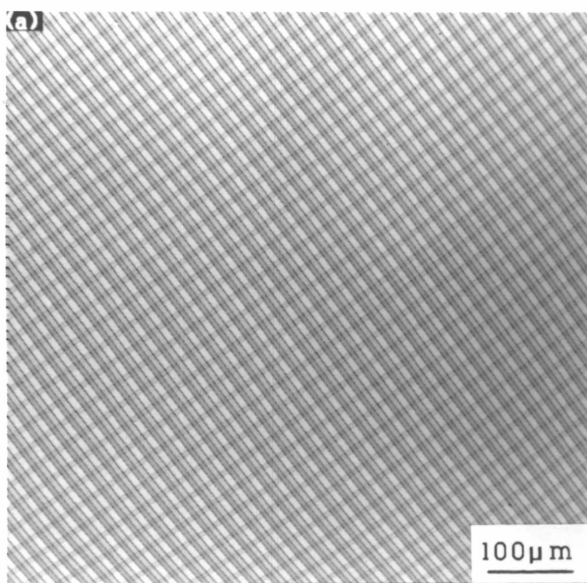
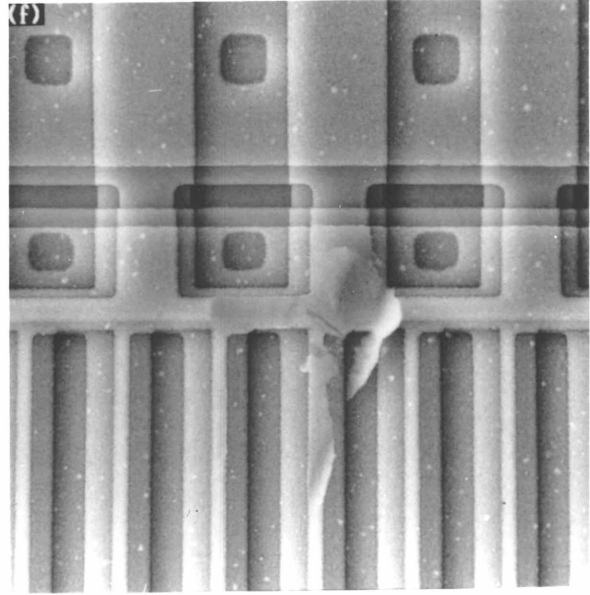
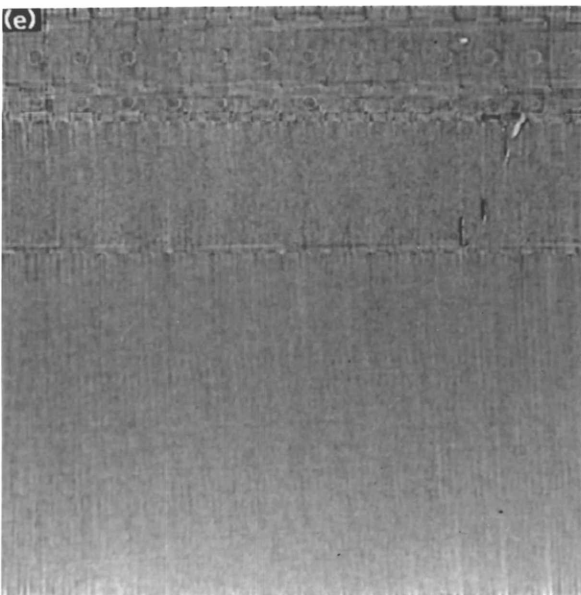
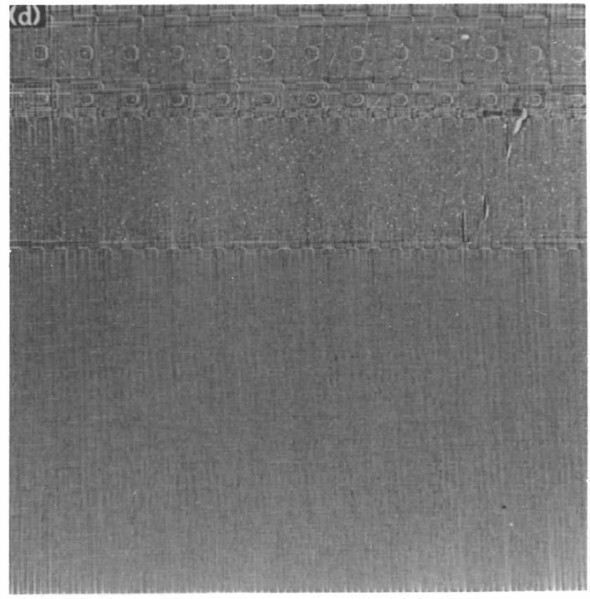
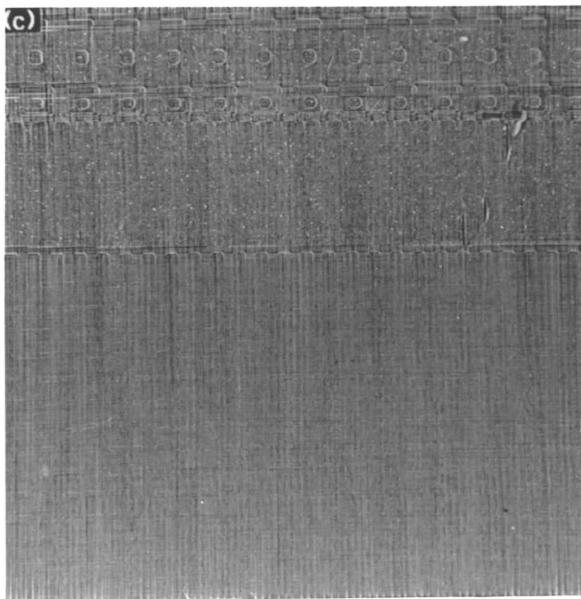
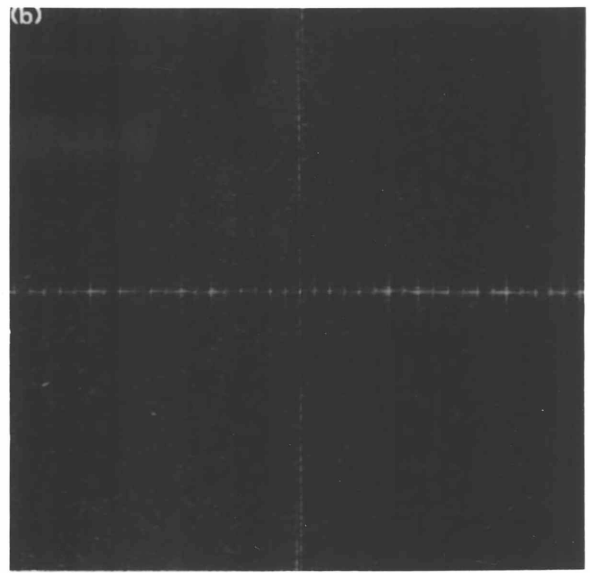
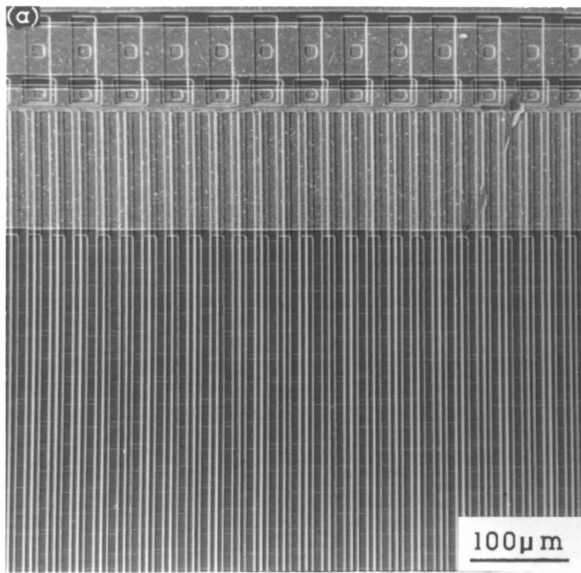


Fig. 66. Spatial filtering of the image of a CCD with mechanical damage.

- (a) SE image,*
- (b) power spectrum,*
- (c) spatially filtered image using thresholding,*
- (d) spatially filtered image using thresholding and a cross,*
- (e) image (c) after a 3×3 median filter,*
- (f) magnified view of top part of defect.*

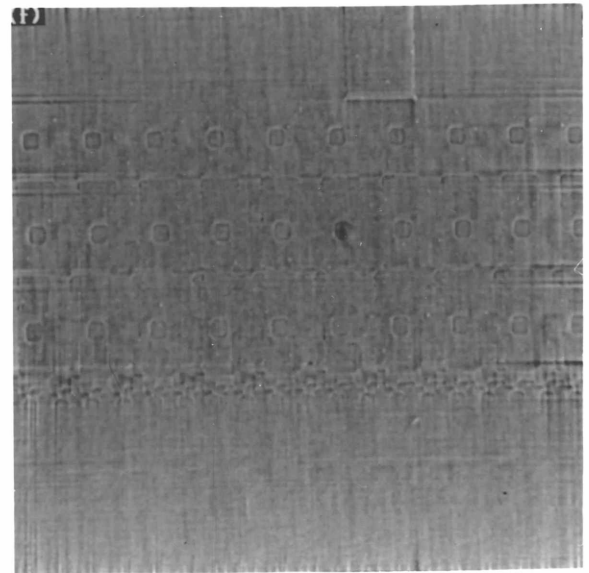
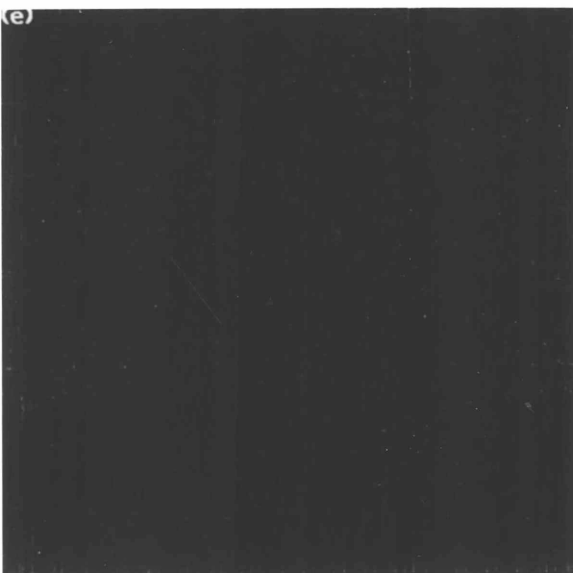
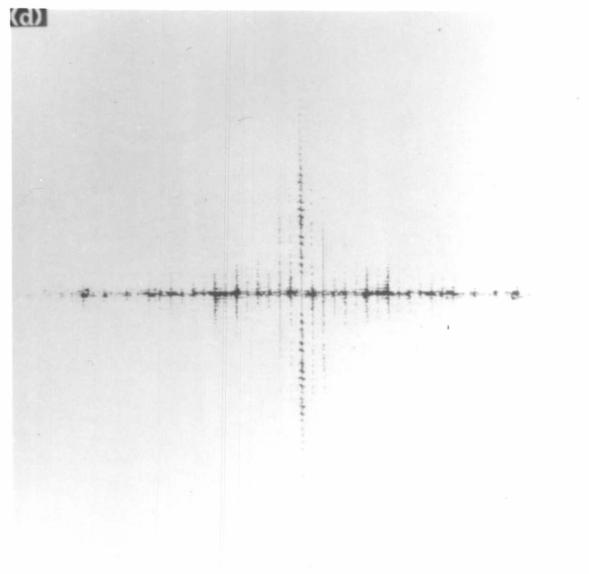
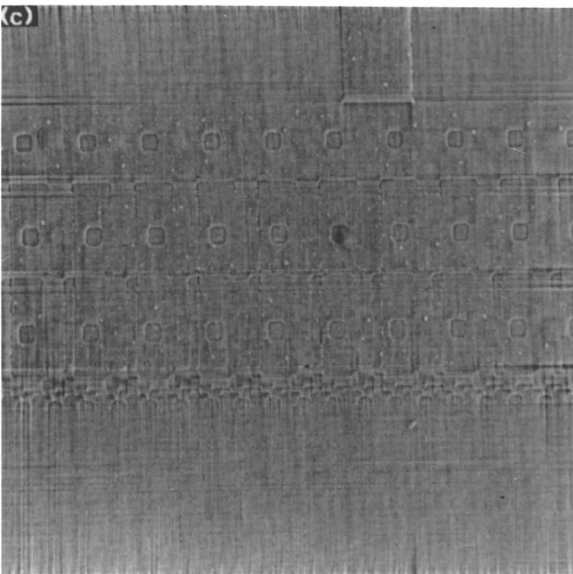
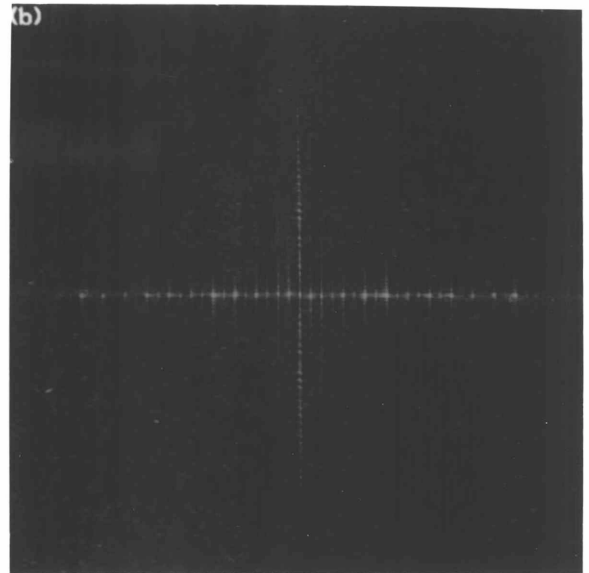
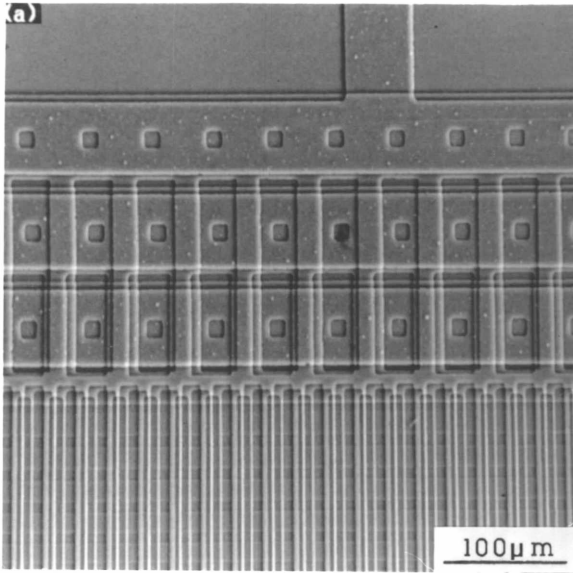


and is improved a little by augmenting the usual thresholded filter mask with a cross (Fig. 66d). A 3×3 median filter (see 2.5.1) was a powerful method of removing pixel-noise (speckle) after spatial filtering (Fig. 66e). Noise was reduced, but the defects remained sharp. The main part of the defect (f) was mechanical damage due to poor handling of the device. Note that in the spatially filtered images (Fig. 66c,d,e) dark lines occur at defects as well as bright ones. These dark lines occur at points where the original image was darker than expected from periodicity (e.g. at a discontinuity in a bright bar). If the zero frequency component had not been retained, these particular defects would have been lost in the black background.

In Fig. 67, the usefulness of retaining the zero-frequency peak is again well illustrated. A dark defect in a contact window near the centre of Fig. 67a is well delineated in (c), compared to the image without the zero frequency component (e) where the defect is seen only as a faint bright patch, in the region adjacent to the defect position. A median filter removed much of the distracting noise in Fig. 67c, giving (f). The dark defect was not a particle. These usually charge up brightly. It was thought to be due to contamination, which would subsequently be a corrosion hazard for the device. This defect could not be examined more closely, as it was an archived image, taken before defect coordinate documenting techniques were established (see later).

In summary, for completely periodic images, thresholded spatial filtering is the most effective method. For irregular circuits, a fast approach is to use edge suppressing filters. These can lead to problems of interpretation, and will fail to identify all types of defect, as the results depend on the defect geometry and local environment. Another approach is to use an x - y spatial filtering mask in the frequency domain, but this has similar limitations.

- Fig. 67. Spatial filtering of an image from the edge of the active area of a CCD containing a dark defect.*
- (a) SE image,*
 - (b) power spectrum,*
 - (c) spatially filtered image using thresholding and retaining the zero frequency component,*
 - (d) mask for (c),*
 - (e) spatially filtered image as in (c) but without the zero frequency component,*
 - (f) image (c) after median filtering.*



A generalised spatial filtering algorithm, `spfilt` was written which allowed maximum flexibility (appendix 3). Its arguments acted as switches as follows:

`norm` : `=1` to normalise the image before filtering,
`thresh` : `=1` to do thresholding of the power spectrum for filtering,
`dilate` : `=1` to do a dilation of the mask,
`cross` : `>1` for a cross filter, of definable size,
`med` : `=1` to do a 3×3 median filter after spatial filtering

For most purposes, thresholding and dilation were nearly always acceptable.

4.2.4 Multiple Image Defect Searching

In this section, the problems of handling multiple images for defect searching will be discussed, followed by a description of the implementations which were developed. Although defect location or defect identification aids were demonstrated for a single image, this single image would only cover a fraction of a VLSI device area. For example, if a resolution comparable to the minimum feature size is required, say $1\mu\text{m}$, then a 512×512 image covers an area $512\mu\text{m}$ square. This compares with a VLSI circuit which is usually $>10\text{mm}$ square. In order to search the whole circuit, several slow stage movements were necessary. To combat this, the digital scan of the Kontron was programmed so that a large area was scanned at lower magnification, but split into a matrix of 512×512 blocks. By acquiring a matrix of n images at one stage position, $n-1$ stage movements were eliminated. In addition, the displacement between these n images was known.

Based on repeatability checks of known points, and 20 measurements of the stage readouts, the standard error of positioning the large goniometric stage on the 840A was $\pm 2\mu\text{m}$. Ultimately some combination of stage movements and digital scan will always be required for observation of large circuits in the SEM because they have a limited field of view and at low magnification are subject to unacceptable barrel or pincushion distortions.

Nevertheless, matrix scans are useful and generate a lot of information. Depending on the size of matrix, image storage was handled as follows:

- (i) single images - images processed in real time, in video memory,
- (ii) 4×4 matrix - 16 images were stored in the video memory, and archived on hard-disk before processing,
- (iii) 8×8 matrix - 64 images, necessitating maximum use of Bernoulli drives for storage, using one cartridge per image set.

Fig. 68 compares the extent of the scans for each case. To illustrate the gain in resolution, Fig. 71 shows a low magnification view of the chip containing the metal defect of Fig. 64. On zooming the centre of Fig. 71a by four times, (b) is obtained, in which the defect (arrowed) is almost invisible. Fig. 71c is a scan acquired from the same region as (b), but with full 512×512 resolution. The visibility of the defect in (c) but not in (b) illustrates the advantage of matrix scans for examining large circuit areas.

A chip was usually examined at more than one stage position, either to cover the whole circuit, or to perform selective analysis of suspect circuit modules. It was thus necessary to refer any defects located to a set of

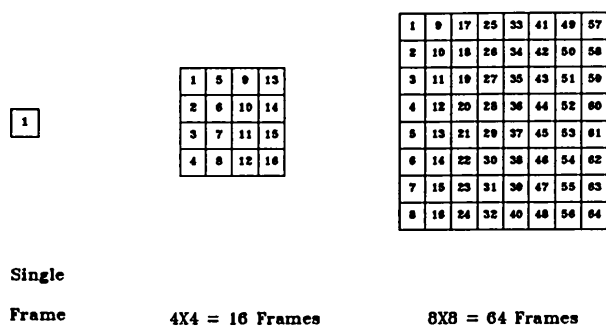


Fig. 68. The relative extent of different matrix-scans.

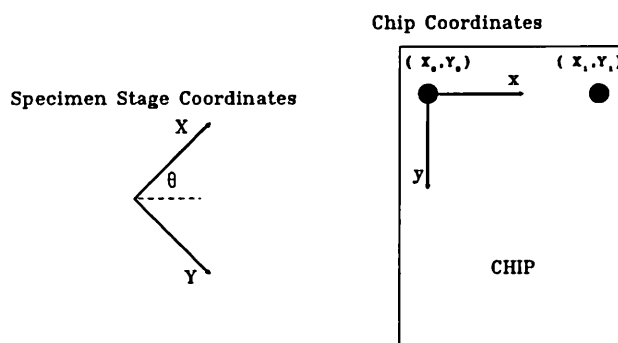


Fig. 69. Relation between stage (vernier) coordinates, (X,Y) and chip coordinates, (x,y) , given two fiducial points, (X_0,Y_0) and (X_1,Y_1) .

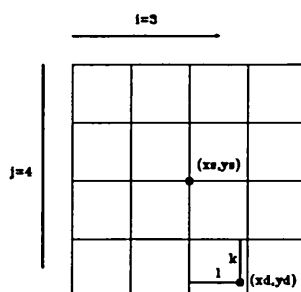
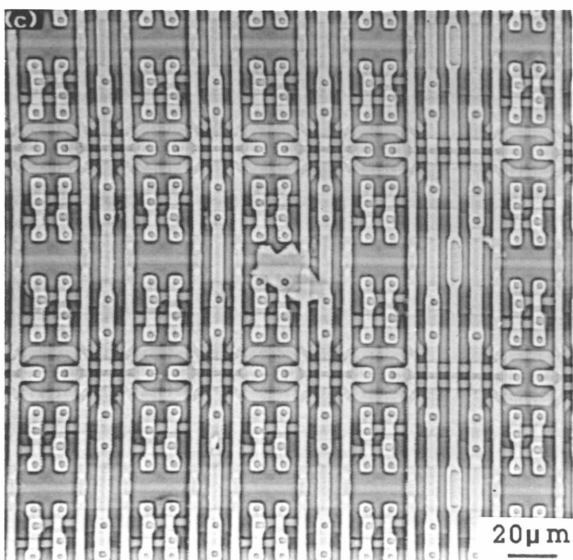
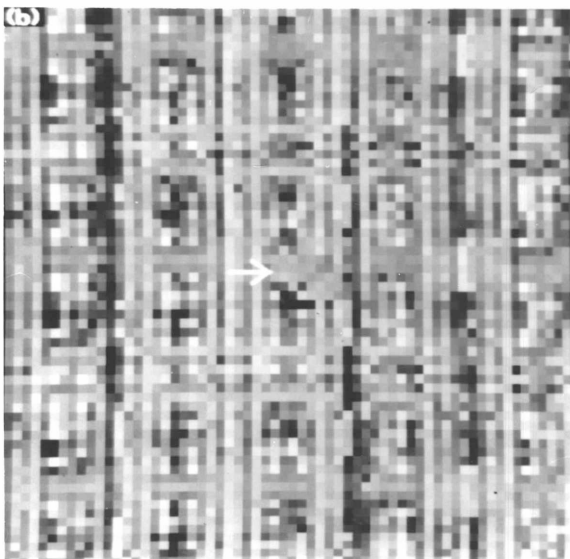


Fig. 70. The three coordinates from which a defect position in circuit coordinates can be calculated.

Fig. 71. The effect of matrix scans on image resolution.

- (a) image taken from the chip containing the metal defect of Fig. 64,*
- (b) central region of (a) magnified digitally by 4 times. The defect is arrowed, but hardly visible,*
- (c) scan of the same area as (b) but using full 512×512 resolution.*



"chip coordinates" so their actual position was known.

Firstly, the stage coordinates, (given by the stage verniers and referred to as (X,Y)) of the centre of a scan (or matrix scan) had to be correlated with a set of chip coordinates (i.e. (x,y) , relative to two fiducial reference points on the chip). This is illustrated in Fig. 69. The relation changes whenever a specimen is re-inserted into the microscope due to small movements in the ZIF socket and sample holder, and would differ for two devices of the same type, as the die is never located in exactly the same position in an IC package. If the stage coordinates of two reference points $((X_0,Y_0)$ and (X_1,Y_1)) on the circuit were read each time, it can be shown (appendix 4) that the stage and chip coordinates are related by:

$$\begin{bmatrix} x \\ y \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} X-X_0 \\ Y-Y_0 \end{bmatrix} \quad (62)$$

$$\text{where} \quad \theta = \tan^{-1} \left[\frac{Y_1-Y_0}{X_1-X_0} \right]$$

Secondly, in a matrix of scanned images if the scan direction was parallel to the circuit coordinate axes, a defect position, (x_d,y_d) was characterised by three coordinates (Fig. 70), as well as the stage coordinates, (X,Y) , as follows:

- (x_s,y_s) – the circuit position of the image matrix scan centre,
- (i,j) – the coordinate of the image within the matrix ($1 \leq i,j \leq n$),
- (k,l) – the pixel coordinate within the defect image

Thus, the circuit coordinate of a defect,

$$x_d = x_s + \frac{D_1}{M} \left[512 \frac{i-(n/2)-1}{n} \right] + \frac{D_1 k}{M n} \quad (63)$$

where D_1 is a constant (=166 μ m per pixel at $\times 1$ for a complete scan)

M is the SEM magnification

n is the matrix size (=4 in this case)

and similarly in the y -direction.

4.2.4.1 Implementation of 16-frame image processing

The general principle behind the operation is shown by a flow diagram (Fig. 72). Solid boxes represent the macros which were written, while dashed boxes represent user actions. The macros from file 16.mcr are all in appendix 5, and each will now be outlined in greater detail. They were all incorporated into the Kontron menu system for ease of use.

StageInit

In this macro, first a fast (256 $\times$ 256 pixel images, no integrations) online image was displayed with a cross-hair in the overlay plane to allow rough positioning of the first fiducal point. Then fine positioning was necessary at a slower scan rate (512 $\times$ 512 pixels, 2 pixel integrations) to eliminate image distortions due to insufficient settling time for the scan DAC's. The stage coordinates were then recorded, and the process repeated at the second fiducal point. Typically these would be the top left and right corners of a circuit, and were necessarily on the same horizontal line. The fiducal reference point coordinates were then stored in the first two records of a database file.

Scan

This macro consisted of the following steps:

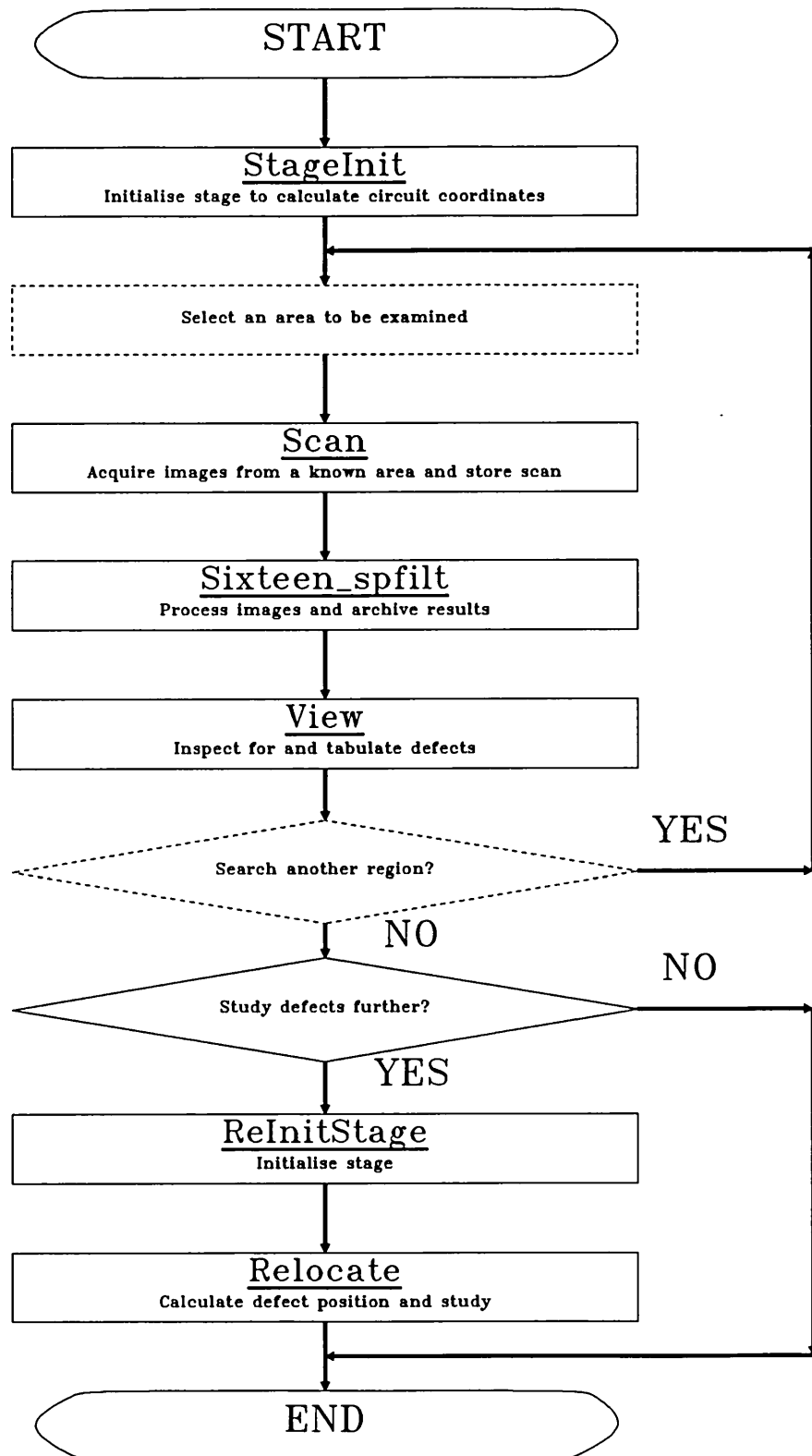


Fig. 72. Flow diagram for multiple image defect searching.

- (i) A fast scan of one of the 16 matrix areas to allow the SEM magnification, and hence the resolution, to be selected and stored (record 3 in the database file),
- (ii) A fast scan the whole 4×4 area at low resolution to allow selection of a suitable circuit region followed by input of stage coordinates and calculation of circuit coordinates (record 4 in the database file),
- (iii) A slow scan (at a rate defined by the macro argument) to optimise image contrast and brightness at one of the 16 images, and to adjust the scan rotation.
- (iv) Scan all images at once in a 2048×2048 block,
- (v) Store all 16 512×512 images on hard-disc.

Sixteen-spfilt

This automatically spatially filtered images, and archived the results on hard disc.

View

The philosophy here was that viewing images of circuits is repetitive and tiring. Therefore, once the circuit structure was suppressed as much as possible, later visual inspection of images showed an acceptable information level, that was more easily analysed visually with fewer mistakes and at a faster rate. To do this all 16 images were automatically stepped through, with three options for the user each time:

- (i) Select next image,
- (ii) Compare – the appropriate original image would be retrieved from hard-disc to allow real-time comparison with the processed result,
- (iii) Defect – a defect had been spotted. Its coordinates would

be read using the digitiser tablet, then both the circuit and stage coordinates were calculated and, along with a comment entered by the operator, were output to printer and appended to the database file.

ReInitStage

This was used to re-enter the new stage coordinates of the fiducal points if the circuit had been moved relative to the stage (by re-insertion for example). The first two entries of the database file would be updated.

Relocate

After the stage was re-initialised, this macro was used to calculate the new stage coordinates of each defect using their circuit coordinates given in the database file.

The whole process was automated to the extent that the operator could flick through images at great speed, and at the end would have a hard copy of the location of and comments about any defects found. A typical output report is shown at the beginning of appendix 5.

4.2.4.2 64-frame processing

For very large IC's, such as CCD image sensors, the above approach still covered insufficient area. So a program was written to use the full 12bits of the digital scan DAC's, and acquire images on a 8x8 grid, giving 64 images in total. These occupy some 16 Mbytes, and were stored on Bernoulli cartridge for later processing. The resulting macros were similar to the 16-frame case, but more complex to manage the data storage. Three macros had to be modified:

Scan

The video memory was insufficient to scan all 64 images at once, so they were scanned in eight groups of 8 images, and stored on Bernoulli (drive F:) using filenames "TEMPIM1.IMG" to "TEMPIM8.IMG".

Spfilt

Images were loaded in groups of eight from the Bernoulli cartridge in F: and the results stored on the cartridge in G:.

View

The appropriate image had to be loaded from Bernoulli before it was viewed. The calculation of defect positions was also modified by the new matrix size, and storage system.

The increase in the amount of data handled meant most macros were slower. In the case of Scan and Spfilt, these could be done offline. View, however, was interactive, and so there was a noticeable decrease in speed, most especially the 3 sec. required to load each image from disc. However, vast areas of chip surface could be searched for defects extremely effectively and systematically.

The accuracy with which defects could be relocated depended on several factors, of which the stage reproducibility was one. The other main source of error was in the accuracy of the scan itself. The JSM 840A has correction algorithms which hold the magnification constant to $\sim 1\%$ at best (3.2.5). When the Kontron was acquiring images, it took over control of the scan, but the ramp voltages generated were passed through the same circuitry, and the correction was still carried out. Additional errors were possible due to instability of the x and y ramp signals from the Kontron, in

particular fast scan rates (compressing the image in the x-direction). Reducing the scan rate to >10 pixel integrations made the effect very small.

Subject to the above qualifications, there was thus a 1:1 relationship between the SEM magnification and the distance per pixel in an image. For a standard 512×512 image this was measured to be (in μm)

$$\text{Distance per pixel} = \frac{167 \mu\text{m}}{M} \quad (64)$$

where M = magnification

Considering a scan error of 1%, the maximum error relative to the central reference point would be in a point $(256^2 + 256^2)^{\frac{1}{2}}$ pixels away. Assuming a typical magnification of $\times 100$, the total error is then

$$\frac{1}{100} \times (256^2 + 256^2)^{\frac{1}{2}} = \frac{167}{100} \approx 6 \mu\text{m} \quad (65)$$

This is small enough to allow the defect to be easily re-located, as it will still be in the field of view at quite high magnification. It would be relatively simple to measure the D_1 value accurately at one particular working distance, magnification and E_b , then maintain these values. Decreasing the error to 0.3% would make it comparable to the stage precision. However, these constraints would be inconvenient in practice.

Several of the defects used as examples in section 4.2.3 were located by this method.

4.2.5 Comparative Defect Location by Multiple Image Searching

Images of integrated circuits which have exactly the same design can be subtracted, with defects showing up in the result. This is the main method of defect location reported in the literature, and it was therefore felt necessary to evaluate some form of comparison technique. The circuit coordinate system described in the previous section was a valuable aid in the first stage of alignment – locating the correct circuit region. This was non-trivial in a large, integrated circuit. It was followed by fine registration of the DUT and golden device images before subtracting to reveal defects. Of the registration methods that have been reported for this, (2.3.2), none were practical to implement on the Kontron. This is because the methods required access to the image data in ways not supported by Kontron functions. Software tools to program the array processor were not available, and accessing picture points one by one via the Kontron readpix function was not intended for such purposes, and was prohibitively slow – for example, reading all 512² pixels in an image would take many hours. Cross-correlation was not implemented on the version of the array processor used in the present study. An interactive alignment function based on defining three reference points was, however, incorporated but by its very general nature this was slow if more than a few images were processed.

In this work, multiple images were compared, by the procedure of Fig. 73. The first steps were similar to those of the previous section (Fig. 72), except that the golden device images were stored as filename "REF". After "ReInitialising" the stage with the new DUT, an "AlignedScan" could be acquired. All sixteen images were aligned, and subtracted by "Compare16", before the results were viewed with "ViewCompared". All the macros written are shown in appendix 5, and will now be discussed in more detail.

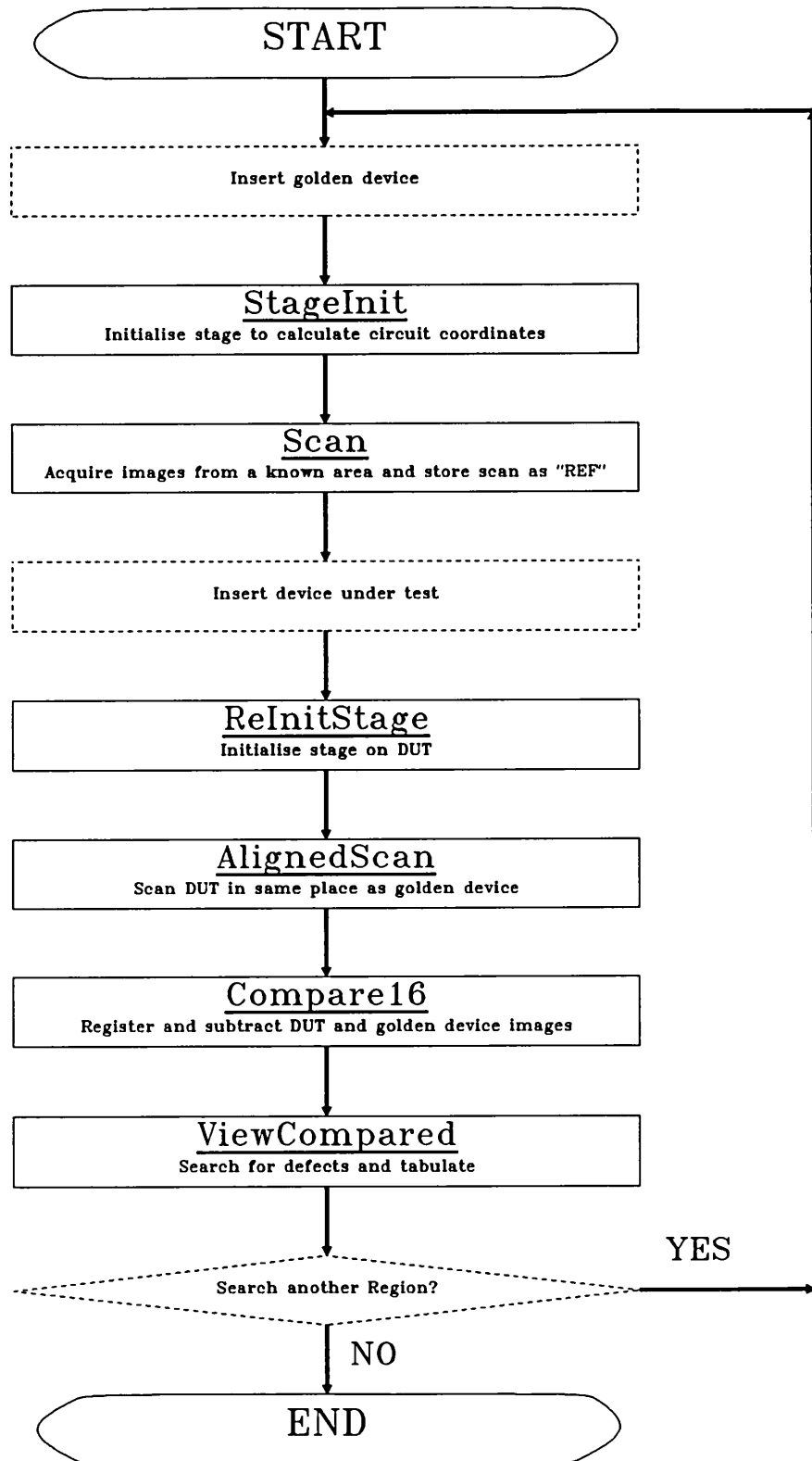


Fig. 73. Flow diagram of how the developed macros (underlined) were used to perform comparisons of matrices of images from the DUT and golden device.

AlignedScan

The circuit coordinate data of the reference scan were used to align the test device to within a few μm . Fine positioning and rotation correction were made using an online image window surrounded by the appropriate reference images. Image contrast was also equalised between the two. All 16 images were then scanned and stored.

Compare16

As angular misalignments of the images had been corrected using the SEM scan rotation, a shift was all that remained necessary for alignment. By defining one reference point in each image, a suitable shift was implemented, and the images subtracted. This was repeated for all 16 images, and the results stored on hard-disk.

ViewCompare

This was similar to "View" in section 4.2.4, except that an additional option in the menu allowed switching between subtracted, original and reference images for unambiguous interpretation once possible defects were found.

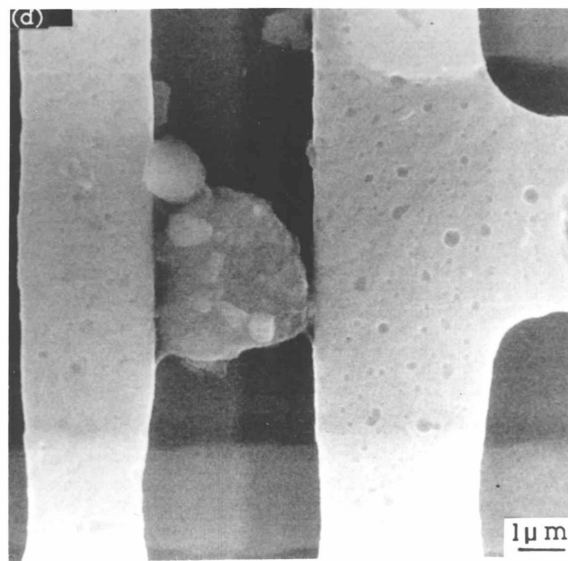
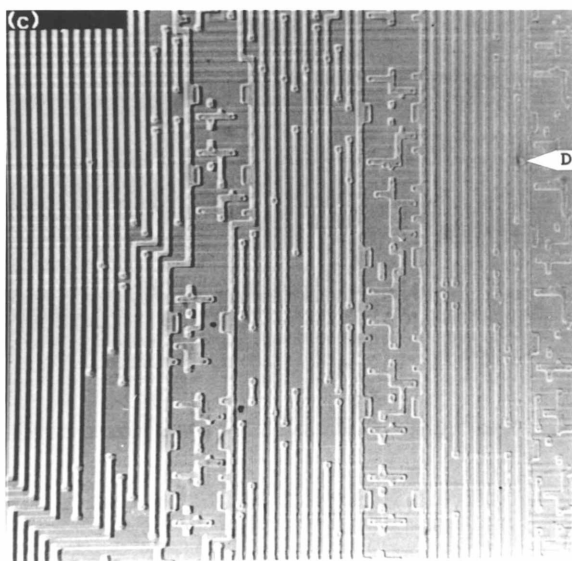
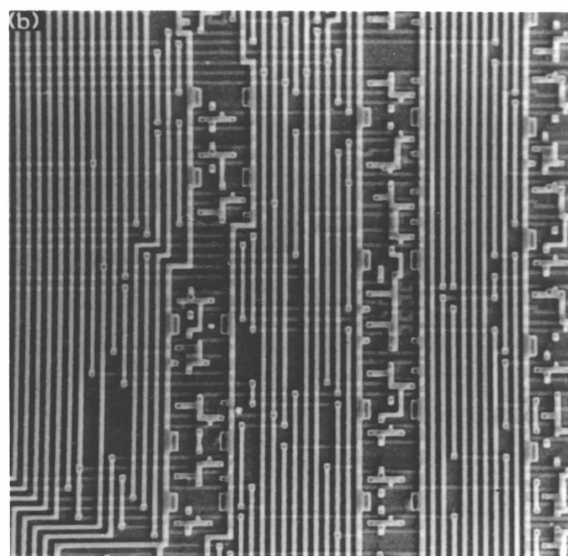
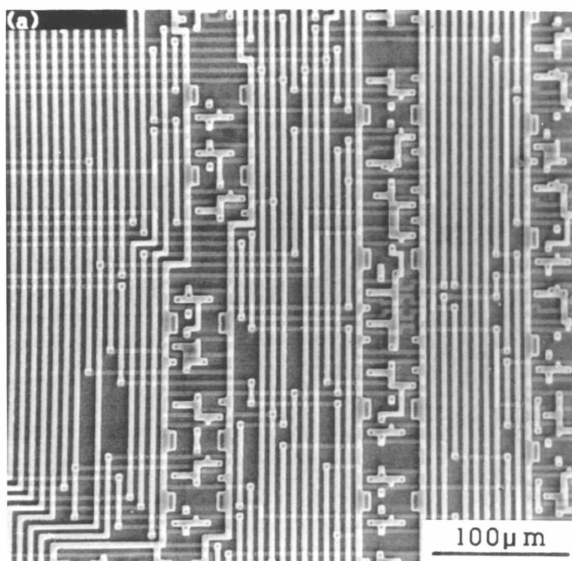
The intermediate result of subtracting two images has a grey-level range of ± 256 , which must be compressed into the usual 256 grey-levels. Taking the absolute value is one way of doing this, so that all defects are bright, superimposed on a dark background. However this does give ambiguities in interpreting whether the defect was dark or bright. A better method was simply to compress the whole range into 256 grey levels (normalisation). Thus identical parts of the two images give a mid-grey background (e.g. greyvalue 128). Bright or dark defects in the test image showed up bright or dark in the difference image respectively. This method was that

preferred by May *et al* (1984) for voltage contrast, dynamic fault imaging. In their work, a black or white region was directly related to whether a logic level was incorrectly low or high. It should be noted that the defect could be in the reference image (with reversed contrast) unless this was completely fault free. Also, it is desirable that the devices are from different batches, as a mask fault, for example would be identical in both circuits.

During an SE, matrix scan of a CMOS logic circuit (Fig. 74), (a) a test and (b) a reference image were subtracted. The result in Fig. 74c is at first sight disappointing, as several lines remain. This occurs due to both rotational misalignment and because the images were shifted by whole numbers of pixels only. Rotation would have been corrected during the "AlignedScan" macro using the continuously variable scan rotation of the SEM. However, assuming exact translational alignment at the image centre, an error of one pixel at the left edge would be due to an angular misalignment of $\tan^{-1}(1/256) \approx 0.23^\circ$. An error in the relative magnifications of the two images would also result in misalignment, although given that E_b and the working distance were generally held constant, these should be small. A transformation function to correct for rotation in addition to the shift was available on the Kontron. However, it was much slower (25s compared to 0.2s), and would require at least two points for definition of its parameters. The most desirable solution is a fully automatic comparison macro, but for reasons explained at the beginning of this section this was difficult to implement, and would give an algorithm so specific to the Kontron that it was not considered a fruitful line of work until the required software tools became available.

Fig. 74. Comparative location of a defect in a CMOS circuit.

- (a) golden device SE image*
- (b) DUT SE image*
- (c) difference of (c) – (a) showing a defect, D*
- (d) close-up of defect*



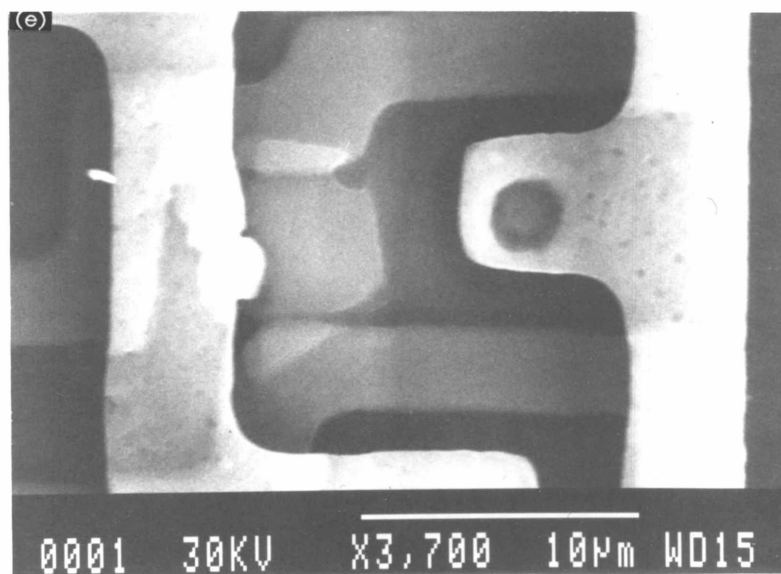
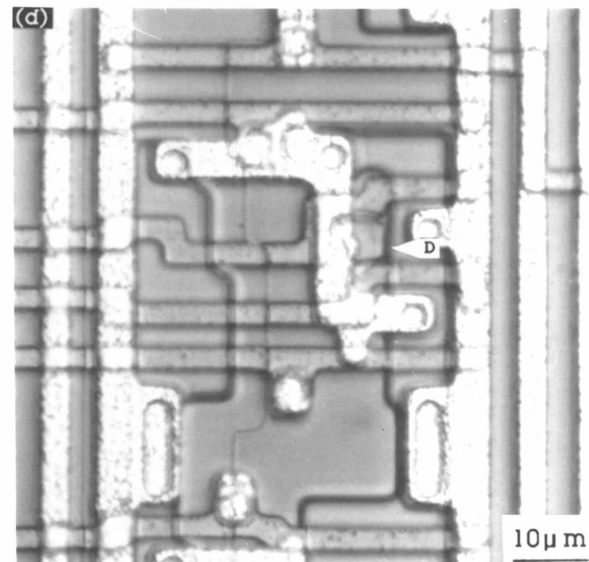
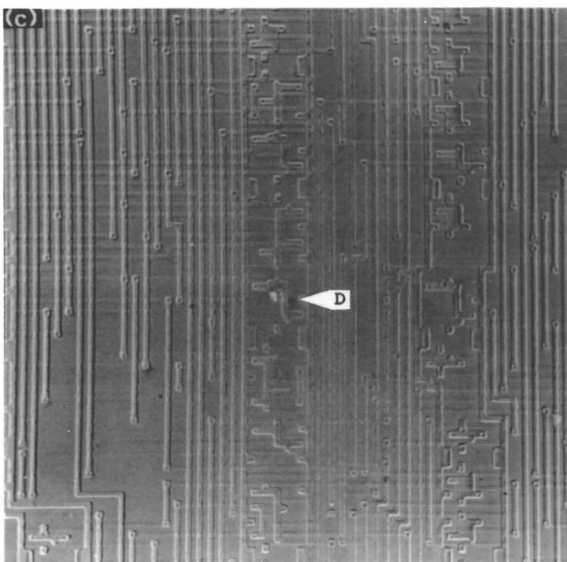
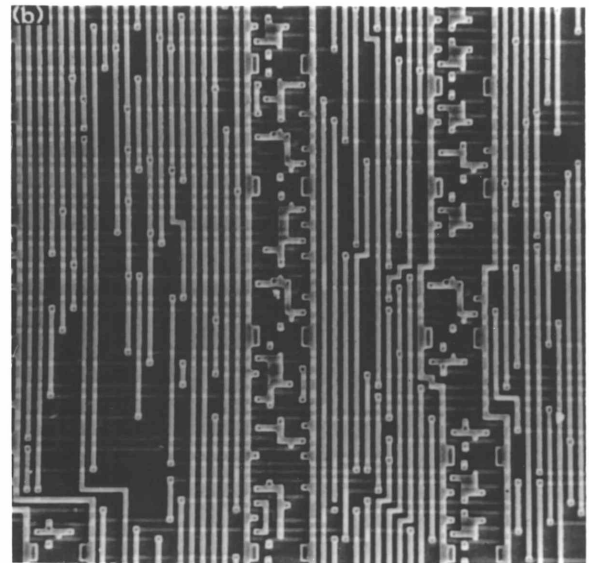
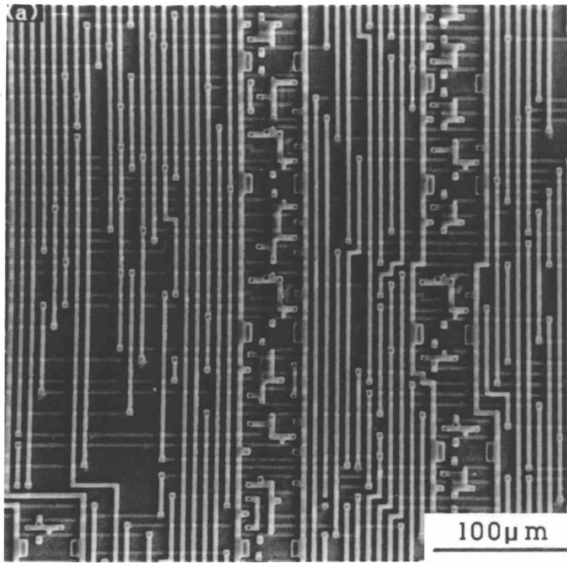
Returning to Fig. 74a,b the DUT and the reference circuit images are shown. Their difference (normalised) in Fig. 74c shows a dark shadow (labelled D). Only then is the defect noticeable in the DUT image of Fig. 74a. At this resolution, it is not possible to investigate the defect further. However, using the stage coordinates given in the printed report, the defect was subsequently relocated, and was examined by conventional SEM techniques at higher magnification (Fig. 74d). It appeared to be a residual particle from processing, and was lodged between two metal tracks. Light microscope observation showed it was non-metallic, although it might well result in electrical interference between the tracks.

In Fig. 75c another defect was located, labelled D. The bright region to the left was dust. The real defect was interesting, because in Fig. 75a, it simply looked like a piece of the circuit (polysilicon). Only in the difference image (Fig. 75c) was it noticeable as a dark shadow. From its circuit coordinates, it was relocated, and examined at high magnification (Fig. 75e). The (horizontal) polysilicon tracks were intact, and the defect was not part of them. In the light microscope at $\times 1000$ (Fig. 75d) the defect was transparent. The limited depth of field of the microscope at high magnification was used to determine heights, by adjusting the focus. It was apparent that the metallisation had been lifted up, which implies the defect was incorporated during processing, and might be photoresist which had not been removed. Similar, less obvious defects can also be seen in Fig. 75a,c, implying it was a processing fault over the whole die.

Alignment errors will be discussed further in the next section. The work outlined in this section, however suggests that even with a relatively simple alignment algorithm, comparisons can locate defects effectively.

Fig. 75. Comparative location of a defect in a CMOS circuit.

- (a) golden device SE image,*
- (b) DUT SE image,*
- (c) difference of (c) – (a) showing a defect, D, this time in the reference device*
- (d) light micrograph at $\times 1000$ of defect,*
- (e) SE micrograph of defect.*



4.2.6 EBIC inspection of pad-driver circuits for ESD damage

Electrostatic discharge (ESD) failures are often located by light microscopy using which they may be identified by melted metallisation in severe cases. Discharges with less energy can cause small cracks in the passivation which are a secondary effect caused by the intense heating which occurs along the discharge path. The electrical disruption caused by an ESD event covers a greater area, but can only be detected by more specialised techniques (Wakefield and Videlo, 1989). Of these, EBIC is one of the most sensitive, and can detect low damage levels which have only subtle effects on the device structure. This will be discussed further in section 4.3.

In this work, advantage was taken of the regularity of the input and output circuitry in a typical IC in which the bond-pad driver circuits are usually taken from a standard CAD library. They are often identical, and thus ideal for comparison techniques.

Three macros were written (appendix 6):

Getref

While a fast-scanned, online SE image was displayed, a suitable region containing the pad-driver circuitry was selected. The reference SE image was then acquired using multiple frame averaging to reduce noise. An EBIC reference image (necessitating a slower scan-rate) was then taken at the same position.

Flip

Often the pad-driver circuitry at two pins was identical but one was a mirror image of the other. Direct registration was thus impossible.

Using this macro, a reflection transformation about a horizontal axis half way down the image was carried out. With the resulting two sets of reference images, all possible orientations of circuitry were testable in principle.

Compare

Alignment of a fast scanned SE image of the test pad-driver circuitry was quickly achieved manually. The reference image was displayed, with an online window-scan of the test pad-driver circuit located at its centre. The stage was thus moved until the central (online) image coincided with the surrounding reference image. Once the position was finalised, an EBIC image of the same area was taken, and subtracted from its reference image automatically.

The advantage of this technique was that the amount of slow EBIC scanning was minimised, and small deviations from normal behaviour were made visible. All examination and alignment was done with fast-scanned SE images. Only the initial set-up of the EBIC image contrast required interactive slow scanning. Before definable window-scans were possible with the software, two alternative registration methods were used. They were firstly, fast switching from the online image to the reference image for, say, 500 ms (Russell and Holt, 1988). Secondly, defining the reference pattern in the image overlay, which could then be displayed over the online image. Both were less efficient than the final method. Other manual registration aids have been reported in the literature. Haardt *et al* (1989) used specialised hardware to display reference and test images using red and green on a colour monitor. Registration was achieved when the whole image was yellow. For fine positioning, Haardt *et al* (1989) displayed the difference image of the incoming video signal and the reference image,

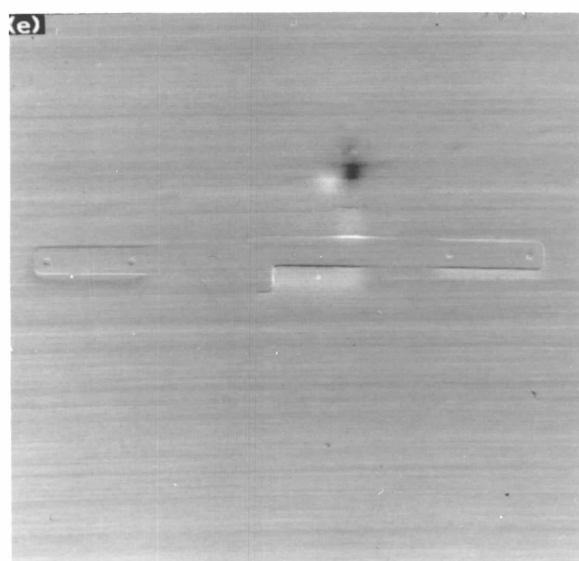
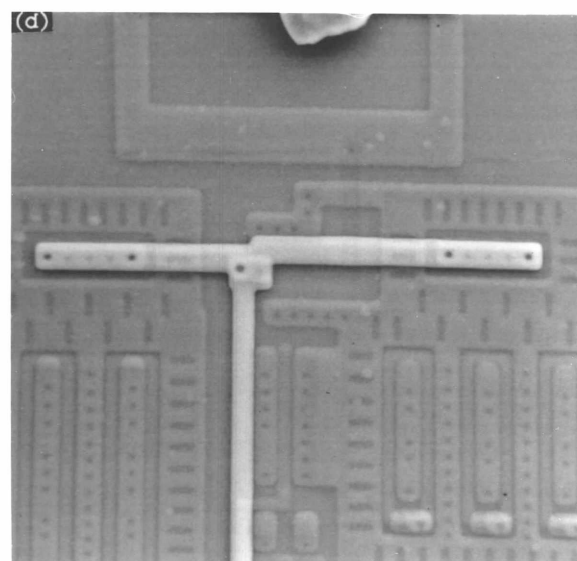
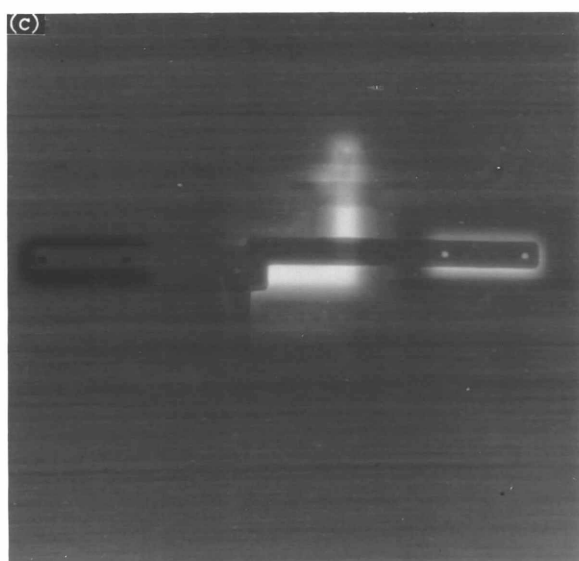
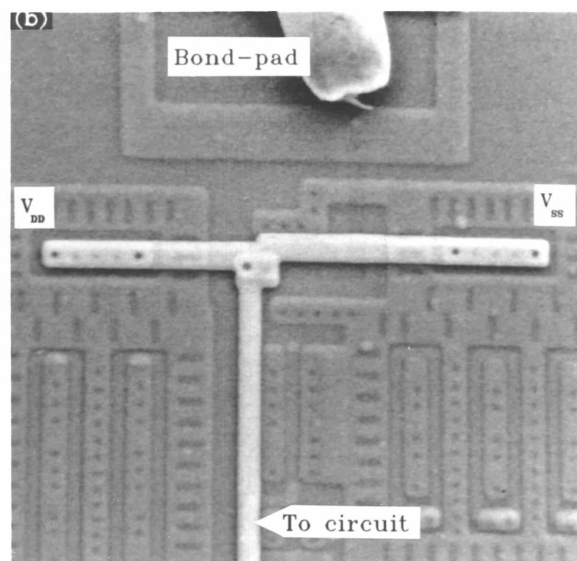
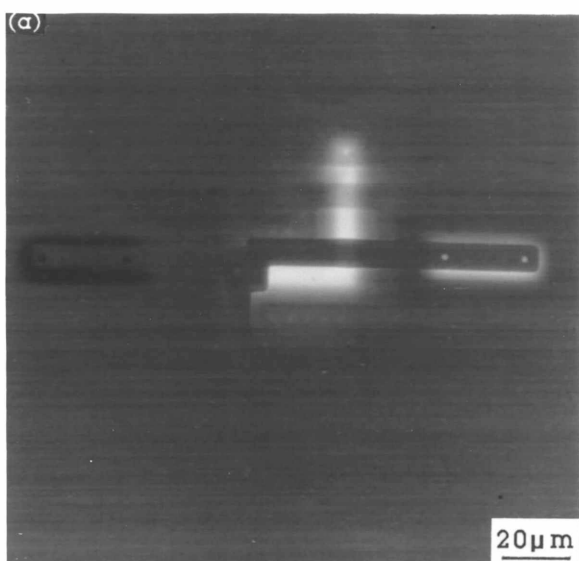
calculated in real time. This facility is, available as an optional extra on the Kontron, but only for composite video input signals (e.g. TV cameras). Unfortunately, the "TV rate" scan of the 840A is incompatible. Nevertheless, for detecting ESD failures using EBIC, the macros written above were the most efficient method.

The first example of this technique was from an MA4055 multi-level metallised CMOS circuit made by MEDL. EBIC images of the input circuitry were made by grounding both V_{SS} and V_{DD} , and connecting the test-pin to I_{sc} . The beam energy was 25 keV, with ~ 1 nA beam current. Using "Getref", EBIC and SE images were taken from pin 1 (Fig. 76a,b). With "Compare", aligned images were taken from pin 3 (Fig. 76c,d) and the subtracted image (e) was generated. The SE images were a necessity for interpretation as they showed the location of metallisation (which blocks the EBIC signal), as well as other features. The difference image (Fig. 76e) showed the defect very clearly, and only then could it easily be seen in the original image, as a faint decrease in the collection efficiency running along the centre of the white diffused resistor. There was also evidence of subsidiary damage immediately to the left as a small bright area, presumably as this was the most direct path to ground metallisation at the contact window (the "hole" leading down to the silicon). The defect was consistent with an ESD event between the input pin and ground, with breakdown occurring along the diffused resistor.

The success of these macros was mainly due to the ease of alignment and the precision with which it could be done. Image alignment errors were less significant than in the case of the multiple image comparisons discussed earlier (section 4.2.5). This was for two reasons. The first can be understood by considering edges in two images with grey-level profiles as

Fig. 76. Comparative location of ESD failure in the input circuitry of an MA4055 multi-level metallised IC. EBIC connections were made with V_{SS} and V_{DD} grounded, while the test pin was connected to I_{SC} .

- (a) EBIC image of reference input (pin 1),*
- (b) SE image of reference input,*
- (c) EBIC image of test input (pin 3),*
- (d) SE image of test input,*
- (e) difference image of (c) – (a). The defect is visible as the dark and bright regions.*



shown in Fig. 77a,b. The increase in grey level along the edge in (a) is gradual while in (b) it is abrupt. In Fig. 77c,d profiles misaligned by one pixel are shown, and subtraction of (c) from (a) and (d) from (b) gives (e) and (f) respectively. In the case of the abrupt edge (Fig. 77b,d), the misalignment error is much brighter (f), while with a smooth edge (a,c) it is flattened out (e). Therefore, as EBIC images often have less abrupt edges than in SE mode, misalignment is less significant.

The second effect on misalignment errors is the magnification chosen. Fig. 78a shows a smooth edge profile, and the result of sampling it at (b) high and (c) low magnification. Fig. 78c would then be compressed for displaying on a screen with the same inter-pixel distance as (b), leading to (d). Thus, the low magnification image will tend to have sharper edges than an image taken at high magnification. Because the area of the pad-driver circuitry was relatively small, a reasonably high magnification setting was used ($\times 500$). Mis-registration was therefore less significant than with images taken at low magnification (to maximise the area covered), like the multiple image comparisons of section 4.2.5.

An unusual case of ESD was that of an output pad-driver in a CT9004 SOS (silicon on sapphire) chip manufactured by MEDL, as it is usually inputs that are affected. The chip was believed to be suffering from ESD failures by the manufacturers. EBIC and SE images (Fig. 79a,b) were taken using the "Getref" macro at pin 4. By grounding V_{SS} and connecting the pin itself to I_{sc} , all of the transistors were seen. Using the "Compare" macro, aligned images near pin 5 were taken (Fig. 79c,d) and the image of (e) produced by a normalised subtraction. As sapphire is insulating, charging occurred on parts of the chip, and is visible on the right of Fig. 79d. The main active area of the output driver circuit was unaffected. The

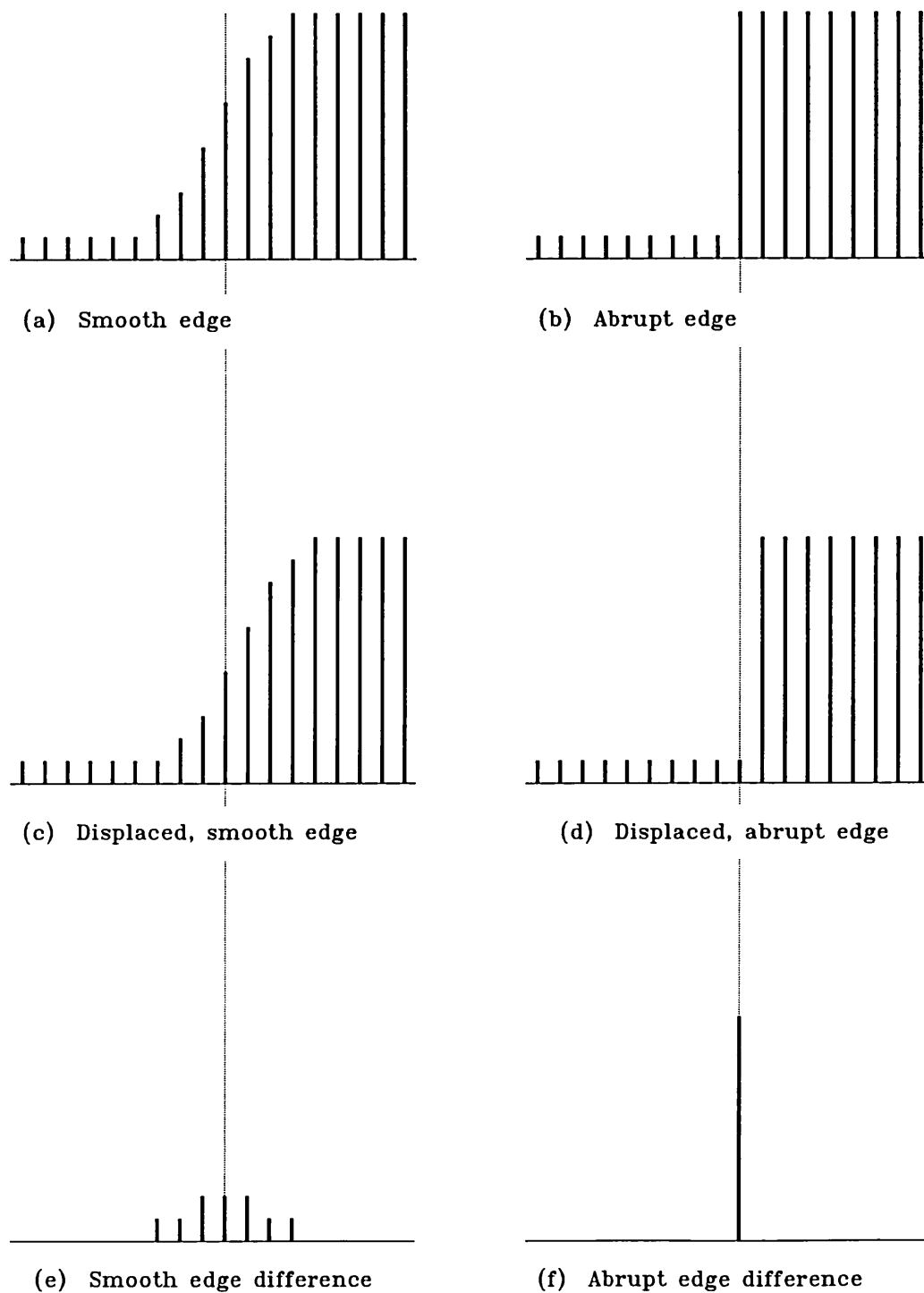
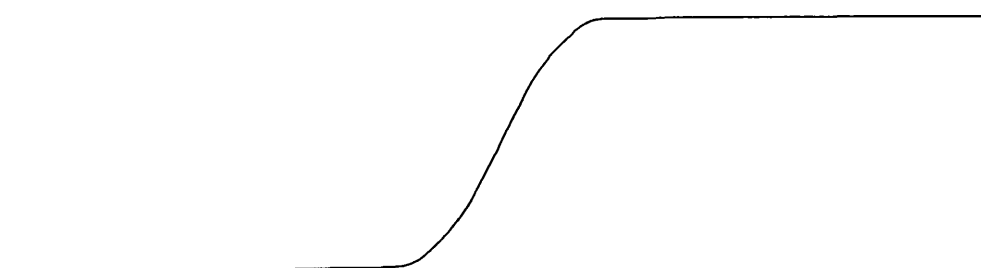
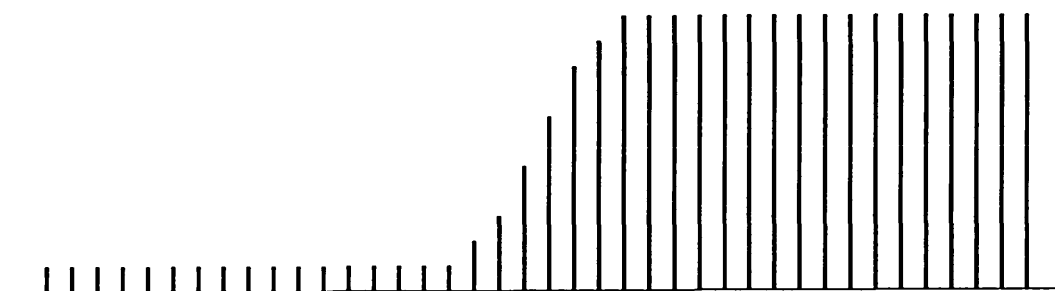


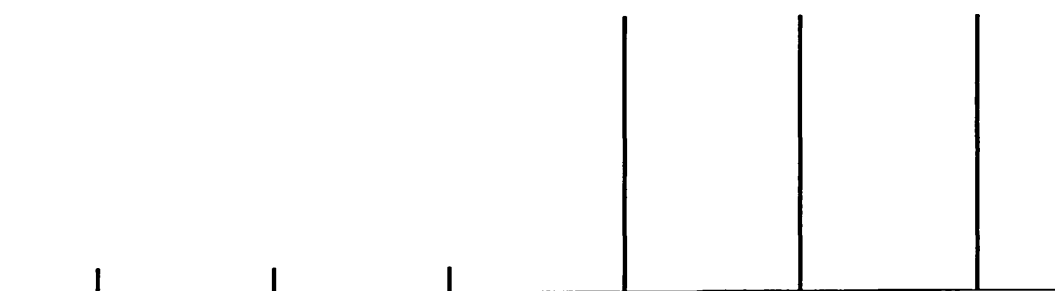
Fig. 77. The effect of edge abruptness on misalignment errors during image subtractions.



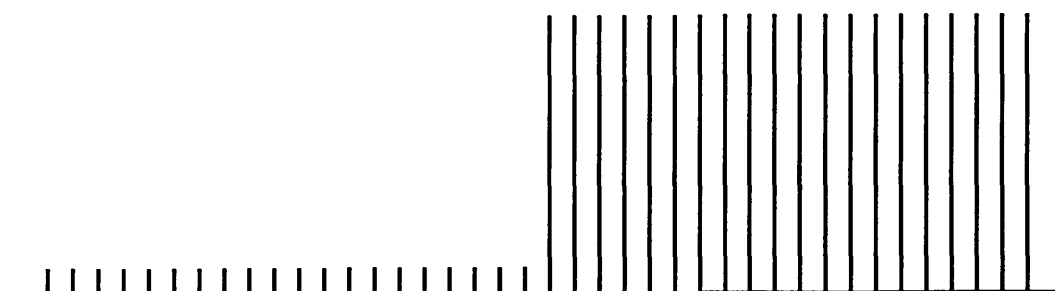
(a) Intensity profile of an edge.



(b) Sampling at small repeat distance (high magnification)



(c) Sampling at large repeat distance (low magnification)

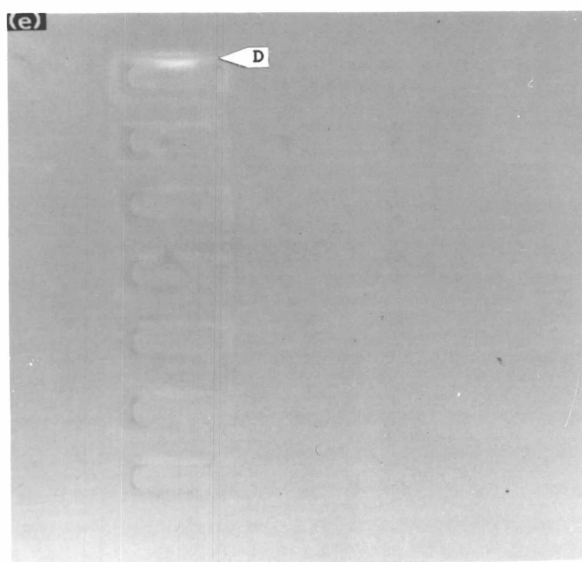
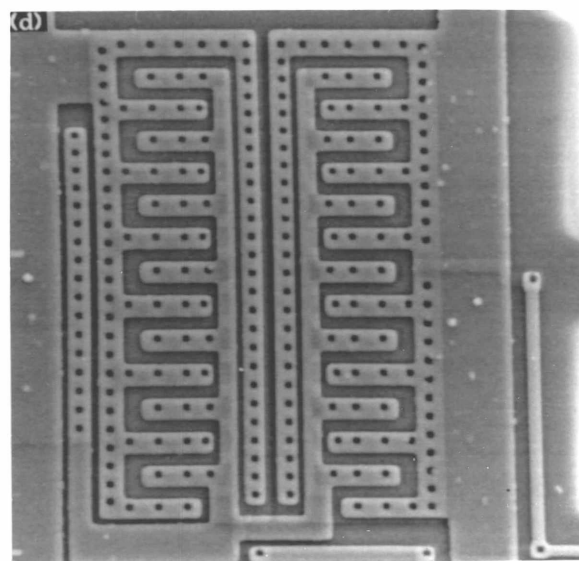
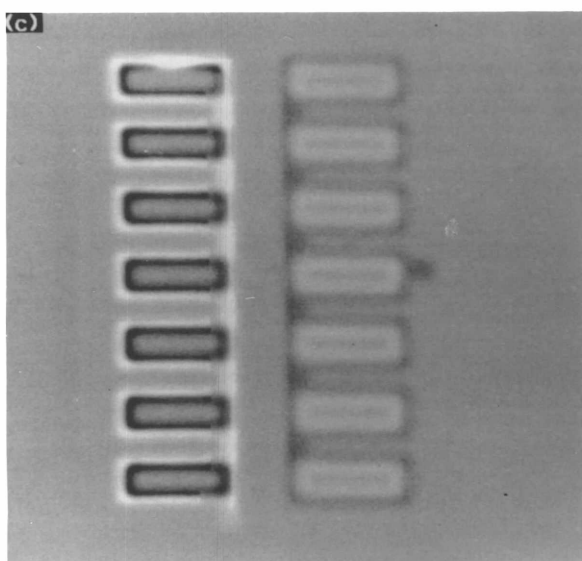
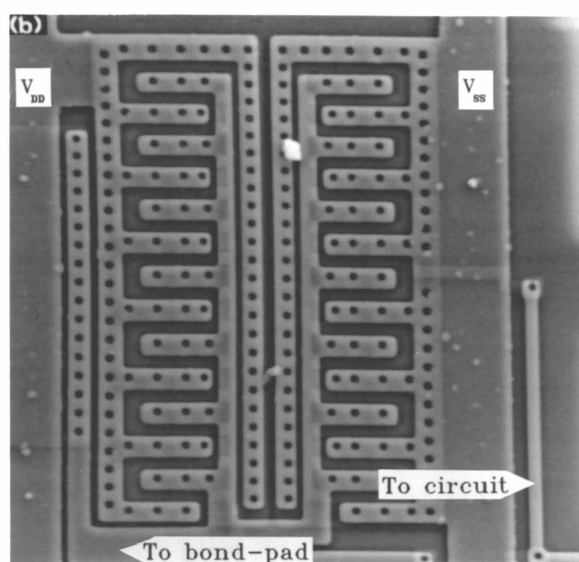
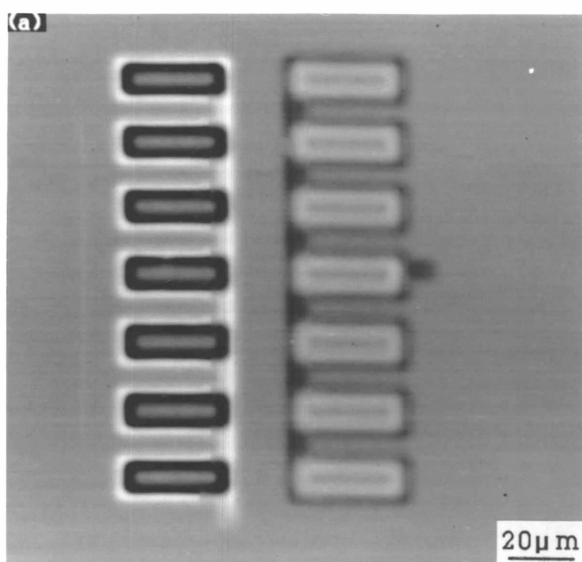


(d) When (c) is compressed to fit into a similar image to (b), the edge becomes abrupt.

Fig. 78. The effect of magnification on misalignment errors.

Fig. 79. Comparison location of ESD in a CT9004 SOS (silicon on sapphire) chip output pad-driver circuit. I_{sc} was connected to V_{ss} and the observed pin was grounded.

- (a) EBIC image of reference pin (4),*
- (b) SE image of reference pin,*
- (c) EBIC image of test pin (5),*
- (d) SE image of test pin showing bright charging on right edge,*
- (e) difference image of (c) – (a), showing defect, D.*



breakdown site was clearly seen in Fig. 79e, labelled D. The characteristics of this defect will be discussed further in section 4.3.1.

The final example (Russell and Holt, 1988) shows the input pad-driver of a CMOS (MA853) chip manufactured by MEDL. This had been zapped by workers at Hirst Research Centre as described later (4.3.2).

EBIC images from circuit #4 were taken with V_{SS} and the input pin connected to I_{sc} , while V_{DD} was grounded. EBIC and SE images were taken from pin 34 (Fig. 80a,b) and pin 33 (c,d). Fig. 80f shows a window image which was viewed during the alignment of similar pins. The test circuitry is in the centre, with the brightness increased to enhance visibility, and is surrounded by the reference image. Any alignment error was very small. In the difference image (Fig. 80e) the ESD site was well delineated and is marked by an arrow. As more than one pin had been zapped, others along the same edge were investigated, with similar success at pin 35 (Fig. 81) and pin 31 (Fig. 82). The detailed structure of the ESD damage will be discussed further in section 4.3.2.

The effect of the "Flip" macro can be seen in Fig. 83. Pin 36 was the reference pin, while pin 33 was the test pin. The two pins were mirror images of one another, so the "Flip" macro was used to generate the reference images of Fig. 83a,b. On subtracting from the test pin image (Fig. 83c) the result (e) was less satisfactory than that of previous examples (e.g. Fig. 80e) due to misalignment between various circuit layers, in particular diffusions and metallisation. This varied in degree, but was always directional. Thus, on "Flipping" the reference images, this misalignment direction would be changed with respect to the test pin, and accentuated in the compared image (Fig. 83e). Contrast in this image was thus due both

Fig. 80. Comparative ESD location in an MA853 CMOS test chip. EBIC images were taken with V_{SS} connected to I_{SC} and V_{DD} grounded.

- (a) EBIC image of reference pin (34)*
- (b) SE image of reference pin*
- (c) EBIC image of test pin (33)*
- (d) SE image of test pin*
- (e) Difference image of (c) – (a), showing defect (arrowed)*
- (f) Example of the online image used for alignment. The reference image surrounds a window at the test pin. Both metallisation and oxide steps (arrowed) are aligned.*

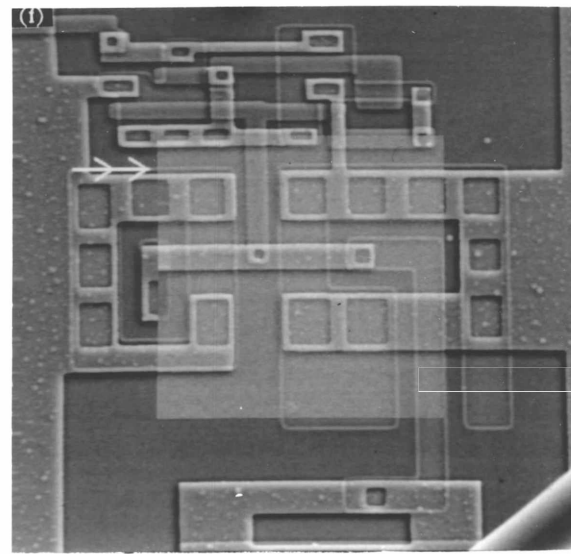
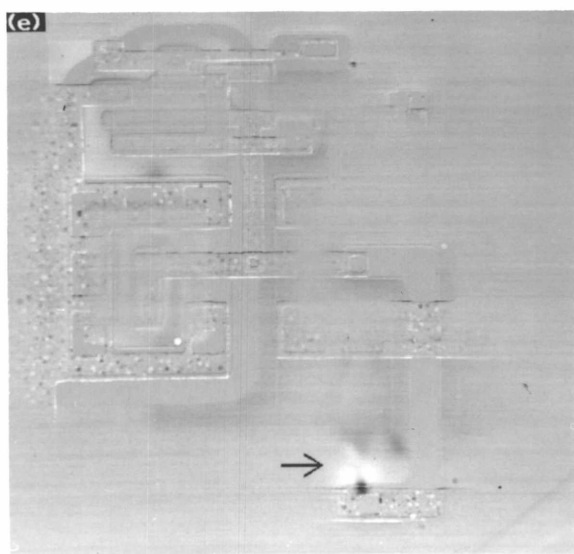
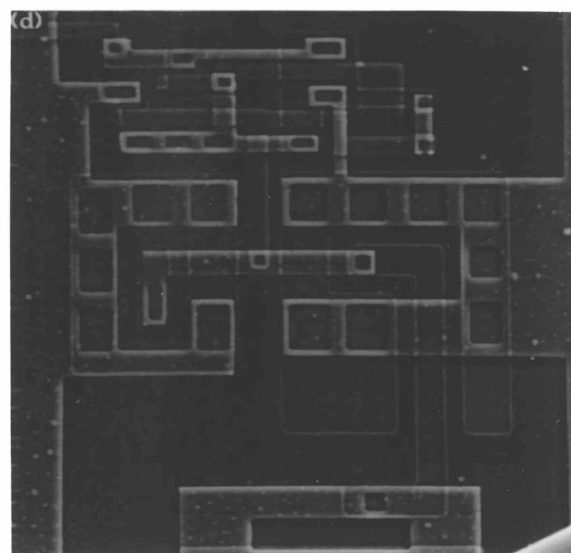
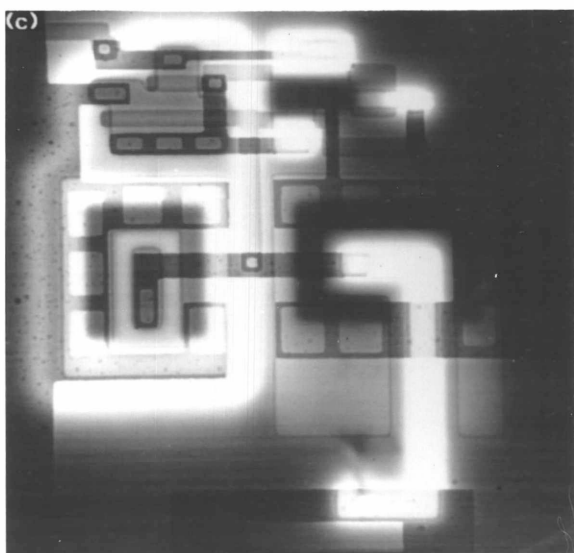
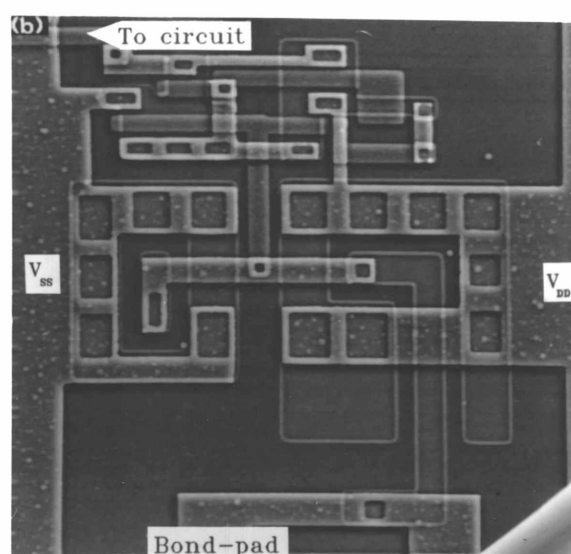
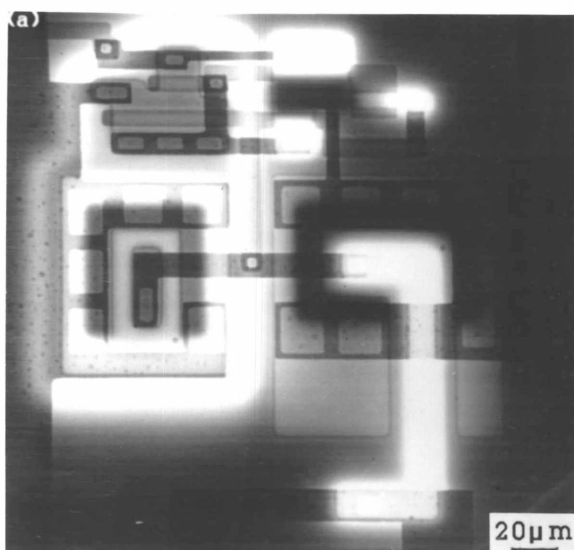


Fig. 81. (LEFT)

*Further ESD location
example at pin 35 using
pin 34 as reference.*

- (a) SE test image*
- (b) EBIC test image*
- (c) difference image*

Fig. 82. (RIGHT)

*Further ESD location
example at pin 31 using
pin 34 as reference.*

- (a) SE test image*
- (b) EBIC test image*
- (c) difference image*

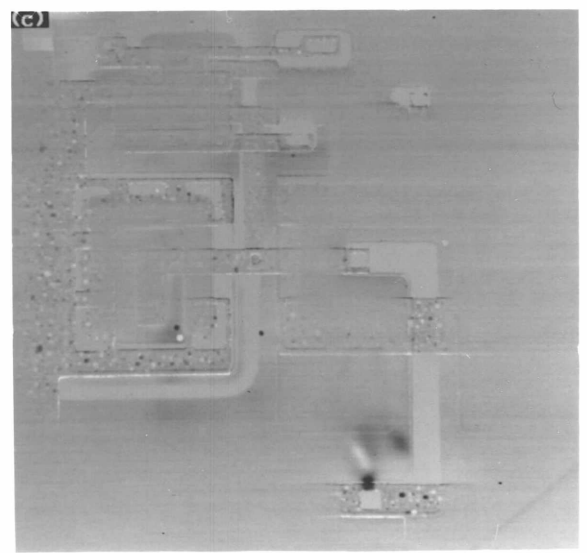
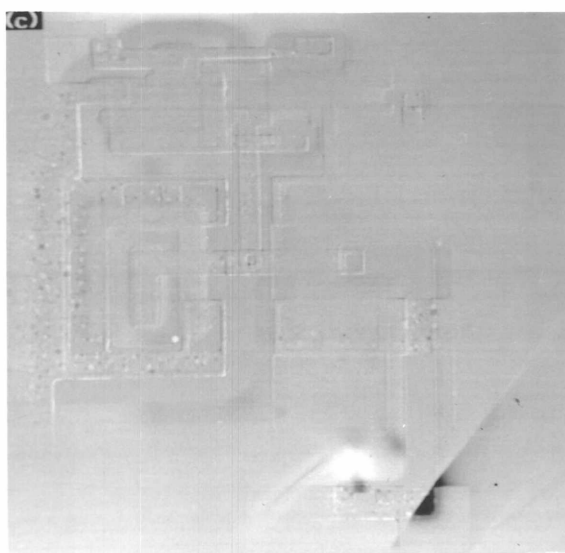
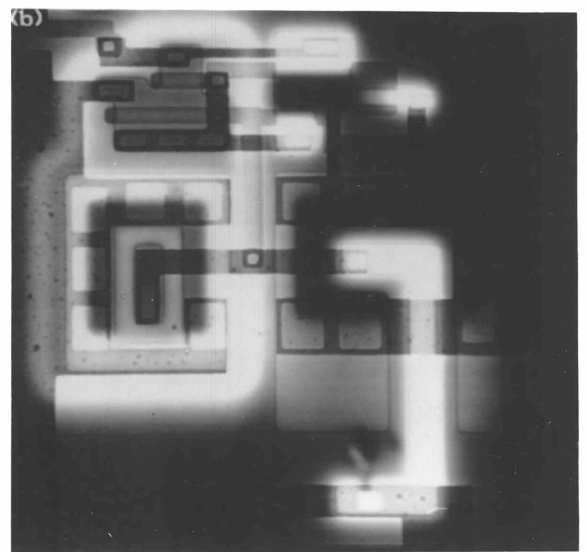
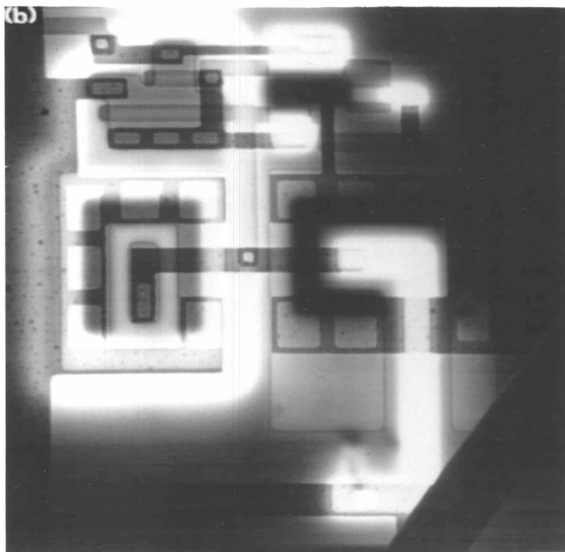
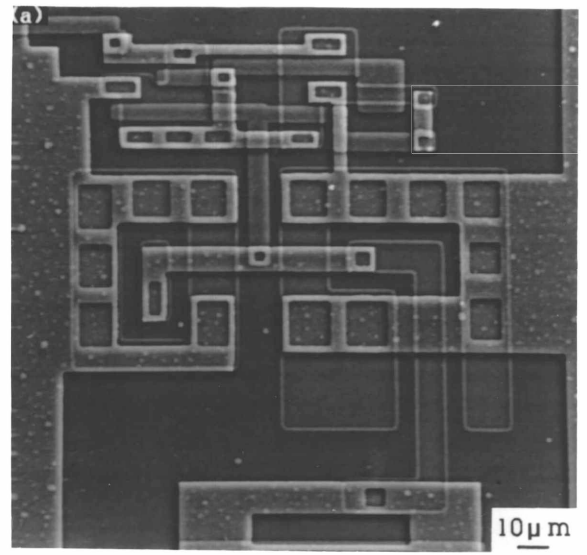
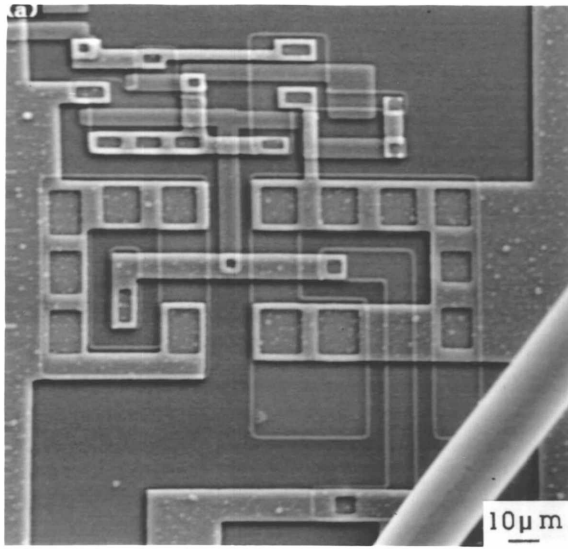
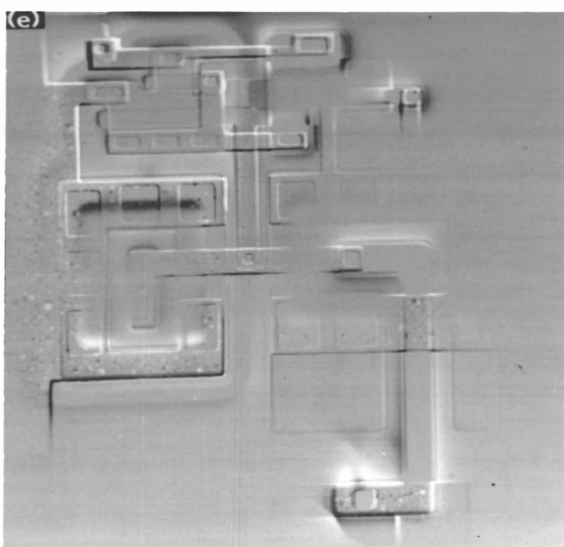
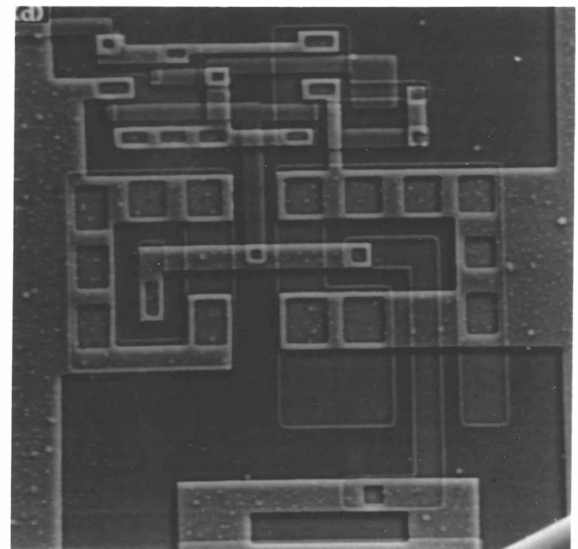
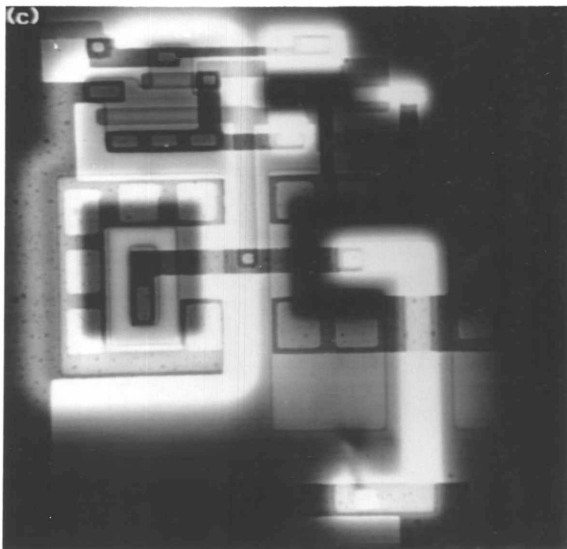
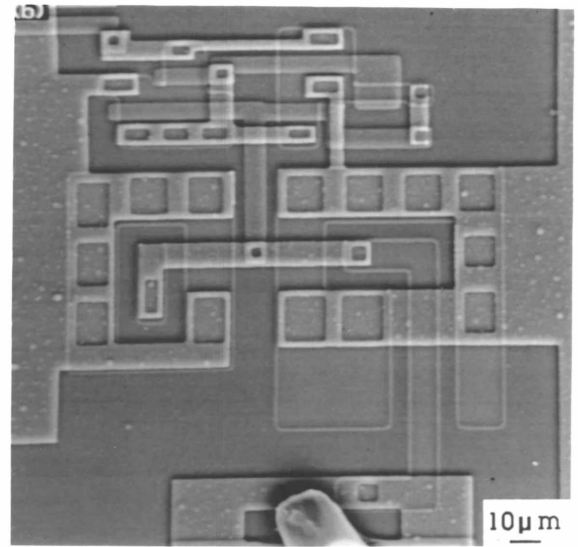
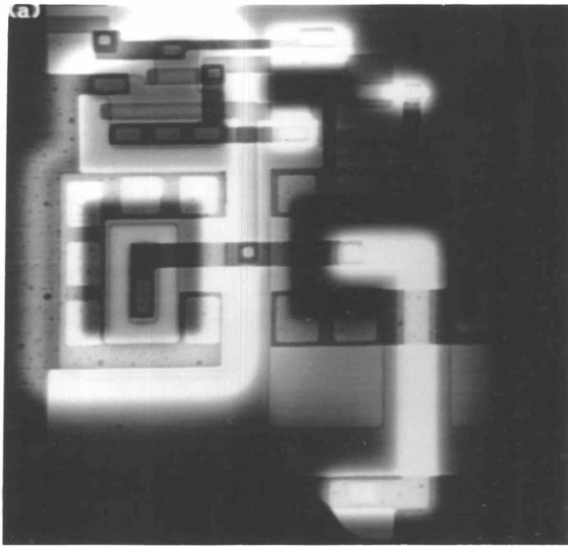


Fig. 83. ESD location using the "Flip" macro.

- (a) reference EBIC image from pin 36 after being "Flipped"*
- (b) reference SE image, also flipped*
- (c) test EBIC image from pin 33*
- (d) test SE image*
- (e) difference of (c) – (a), showing errors due to misalignments*

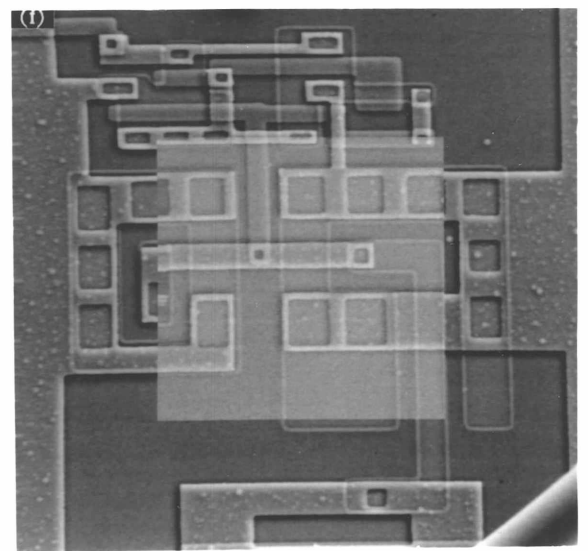
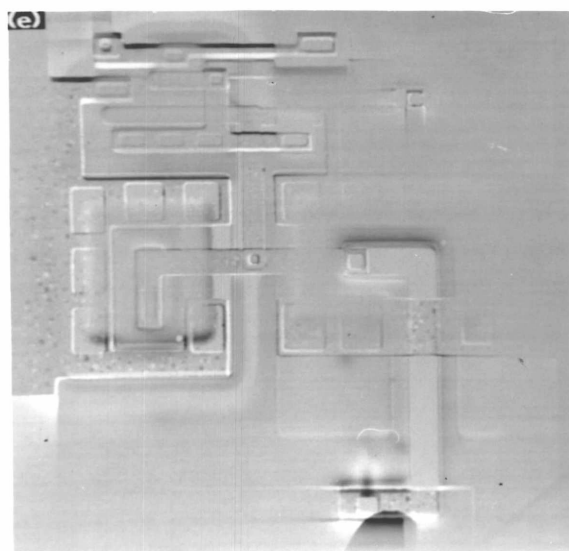
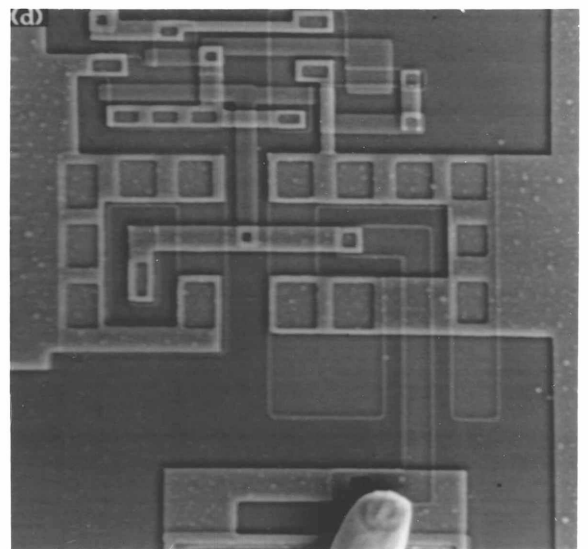
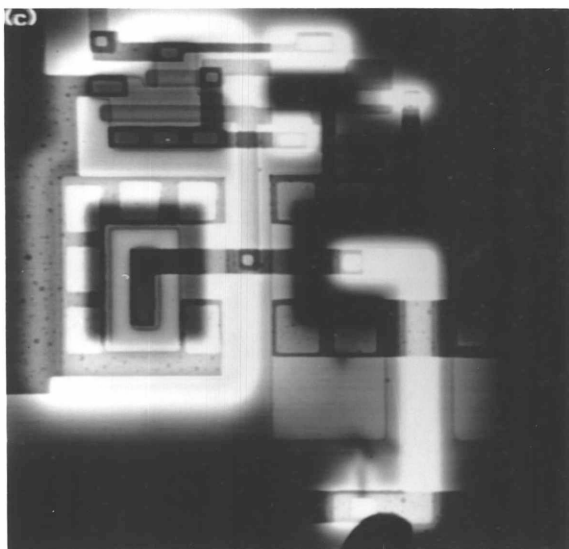
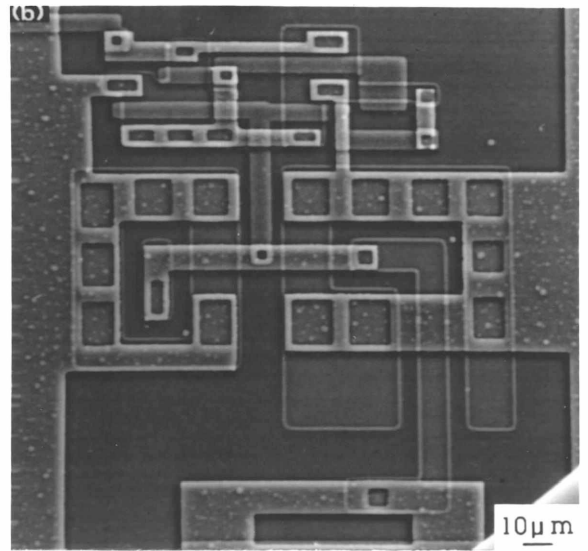
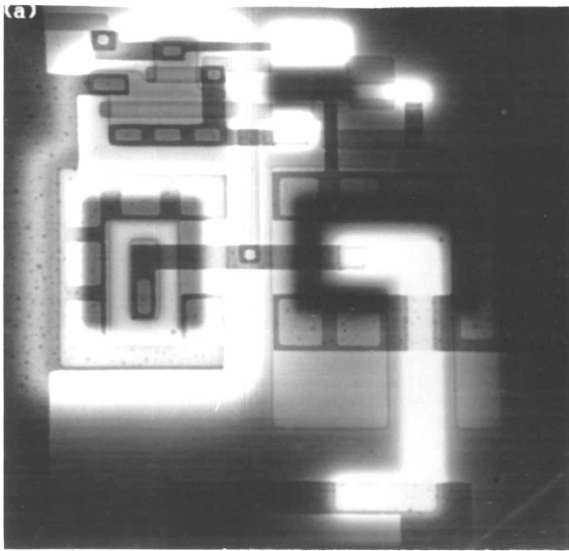


to defects and mask misalignments.

A similar effect is apparent in Fig. 84 when "Flip" was not necessary. The same reference images from pin 34 were used, but in this case the test pad-driver circuitry was oriented at 90° to the reference circuitry on the chip (pin 28). This was corrected using the SEM scan rotation to give Fig. 84c,d. On subtracting (Fig. 84e), the directionality of the misalignment was apparent. Its origin was obvious from Fig. 84f in which the reference image is shown with part of the test SE image in the alignment window used by macro "Compare". The metallisation and the oxide steps cannot be simultaneously aligned. However, the macros were still useful in this case, if such artefacts were allowed for, as their linear nature makes them easy to discern. In fact, for defect free circuits, this is a very sensitive way of *measuring* misalignments.

Fig. 84. Effect of misalignment on ESD location in pad-driver circuits at right angles to each other.

- (a) EBIC reference image from pin 34*
- (b) SE reference image*
- (c) EBIC image from test pin (28), made coincident using the SEM scan rotation*
- (d) SE image of test pin, also rotated*
- (e) difference image of (c) - (a) showing defect and misalignment*
- (f) alignment window image - note that both oxide steps and metallisation cannot be simultaneously aligned (cf Fig. 80f)*



4.3 EBIC STUDIES OF ESD DEFECTS

In section 4.2.6 it was shown that static damage to pad-driver circuitry can be readily located using image processing. Although EBIC has been used in the past to show static damage, no detailed interpretation of the micrographs beyond it showing "discharge paths" has been reported. It was thought that it might be possible to gain further information about ESD from its EBIC contrast.

Because of the complexity of integrated circuits, and the lack of detailed knowledge about their structure (e.g. doping densities, junction depths etc. – closely guarded secrets of the manufacturer), accurate calculations might not be possible. However, using the Matelect program, data can be acquired rapidly, and can be analysed in order to draw general conclusions about the structure under evaluation.

4.3.1 Interpretation of CT9004 SOS device EBIC

As was shown in Fig. 79, static damage of the output at pin 5 of the device consisted of a bright region in one of the output transistors. To interpret this the circuit structure must be considered in more detail. The output driver was an inverter consisting of separate groups of 7 n- and p-channel transistors connected in parallel. Fig. 85 shows one transistor, consisting of a central drain, surrounded by a gate which in turn was surrounded by a source. The source was shared with adjacent transistors on either side. EBIC contrast of concentric bright and dark rings is understood by referring to the cross-section of a single transistor in Fig. 86. It consisted of a p-type body with n-type source and drain at the sides.

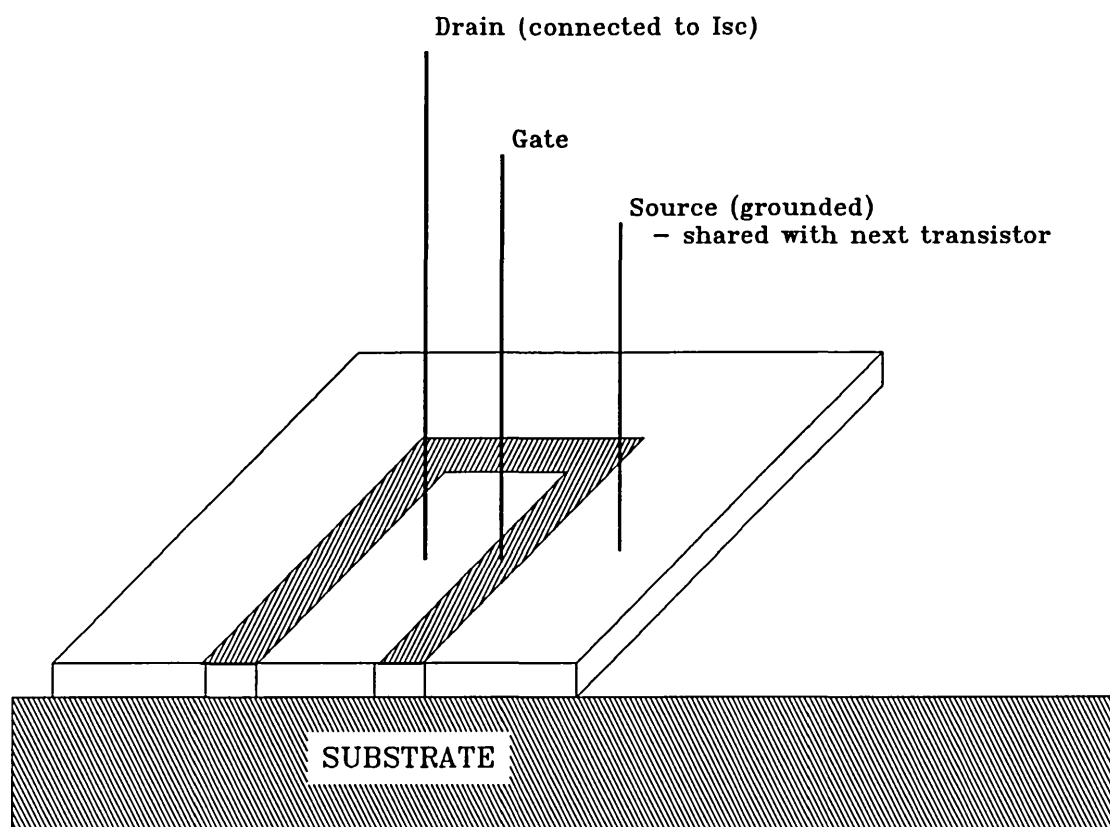
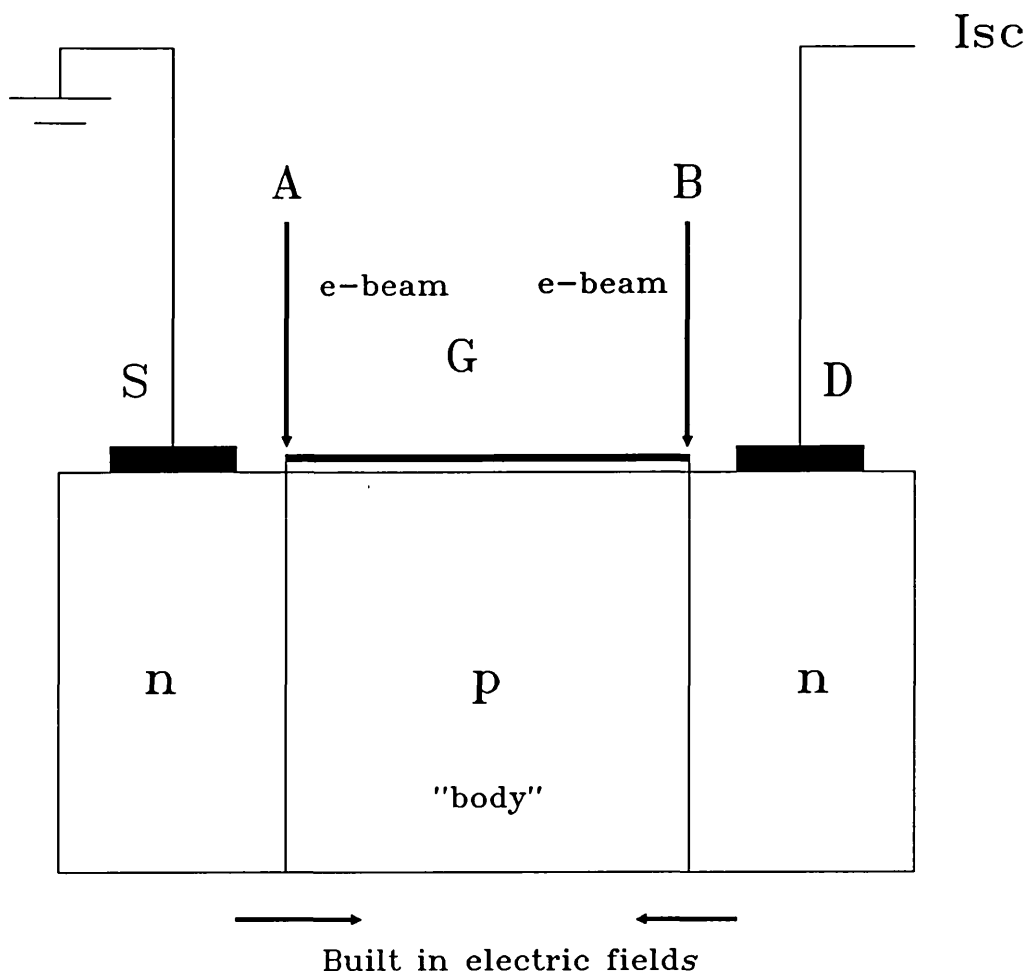
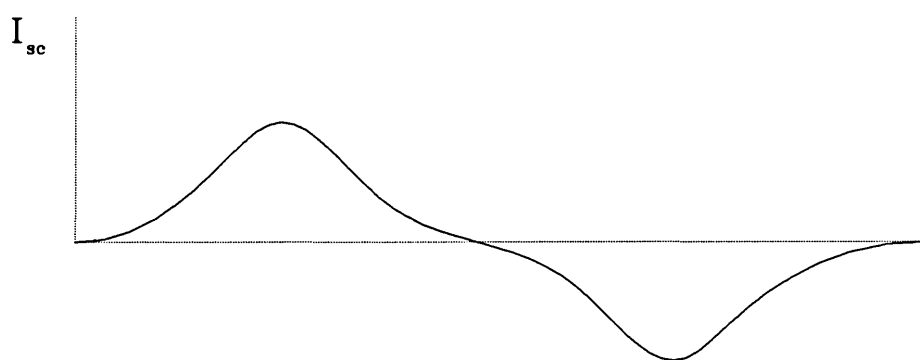


Fig. 85. Schematic of the structure of one of the group of seven n-channel output transistors in the CT9004 SOS circuit.

When the electron beam was incident at A, the generated electron-hole pairs were separated by the field in the source-body depletion region. Electrons would enter the source, and travel easily to ground. Holes entering the body would accumulate, due to the potential barrier at the body-drain junction. Eventually, this accumulation of holes would forward bias both the source-body and body-drain junctions allowing an (attenuated) I_{sc} to flow. When the electron beam was incident at B, the situation was the same, except the currents were reversed so that the body-drain junction appears locally dark in the micrograph (Fig. 79a), and an EBIC linescan from left to right in Fig. 86a would give the profile of (b). In the micrograph this corresponds to a linescan vertically through



(a) Schematic cross-section of SOS transistor



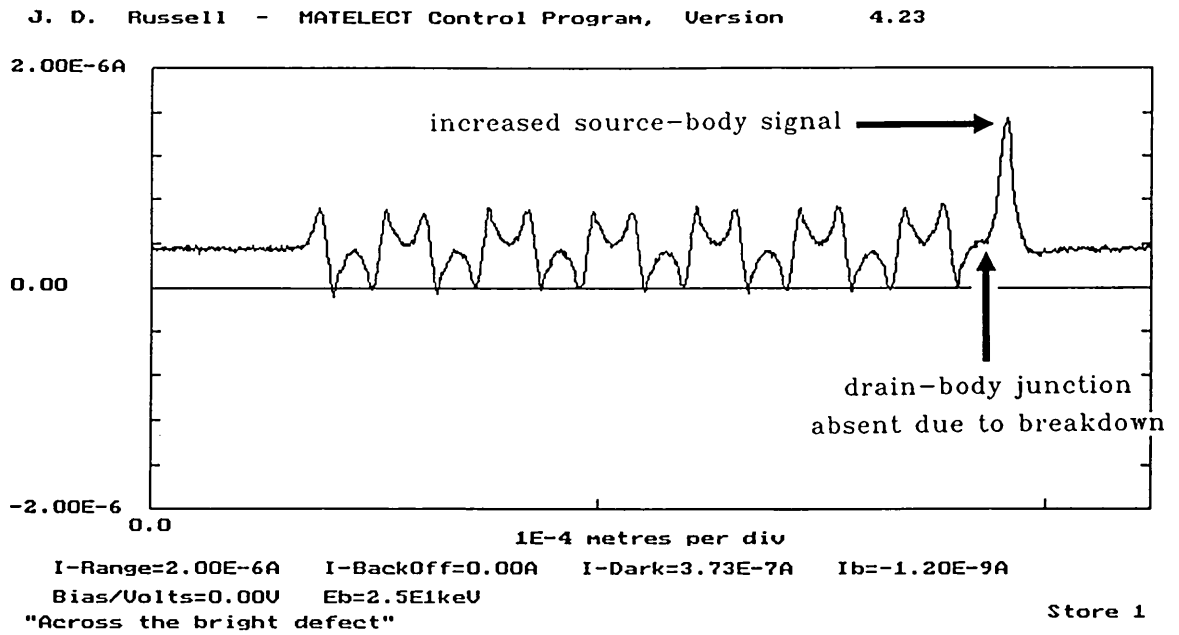
(b) EBIC linescan across structure in (a)

Fig. 86. Cross-section of a CT9004 output transistor, and its EBIC contrast profile.

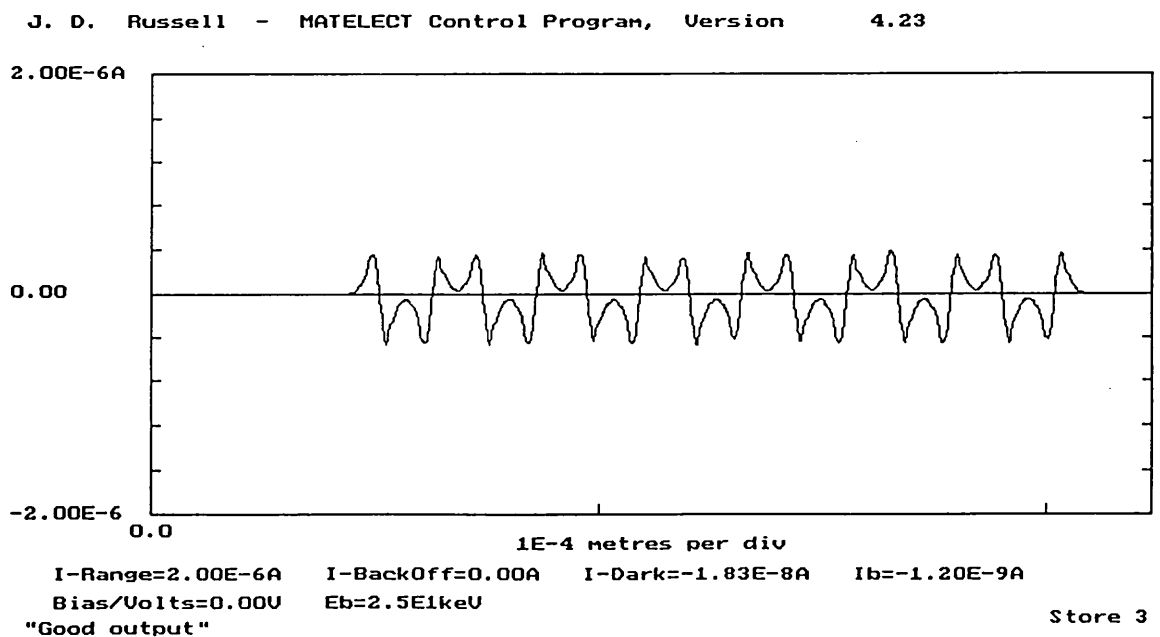
the left-hand group of transistors (Fig. 79a,c).

Such EBIC linescans are shown in Fig. 87a through the defect, and in (b) at the same position on the good output (Fig. 79a). These scans are easily interpreted by comparison. For the defective transistor the drain-body junction had completely disappeared, as it gave an I_{SC} identical to the background level, and the source-body junction was much brighter. Neither of these effects were present in the second linescan (Fig. 87b), taken from the working output. This is consistent with second breakdown of the drain-body junction due to a high voltage transient. The breakdown would generate a localised leakage from the drain contact through the junction. Thus, no charge collection would occur at the damaged part of the drain-body junction. Collection at the source-body junction was locally enhanced because holes no longer had to surmount the drain-body potential barrier. This effect decreases with distance from the drain-body short due to increasing series resistance from the body. Another feature of the linescans worth noting is that the background level is offset in Fig. 87a compared to (b). Clearly, no collection should occur away from active areas, and it would be expected that $I_{SC}=0$ as for the undamaged output. In fact, it is believed that this is an artefact because the resistance of the specimen has become much lower than the EBIC amplifier input impedance. In this case, the offset voltage at the amplifier input generates a current. This is confirmed because the offset current is the same as the dark-current measurement displayed in the data zone of the program output (3.78×10^{-7} A, measured with the PCD inserted).

Having established which junction was probably damaged, it was then possible to draw conclusions about the ESD event itself. Fig. 88 shows the pad driver circuit. To cause breakdown in the drain-body junction, it



(a) Line scan including the defect.



(b) Linescan taken from a good input structure.

Fig. 87. Linescans taken from bottom to top in Fig. 79.

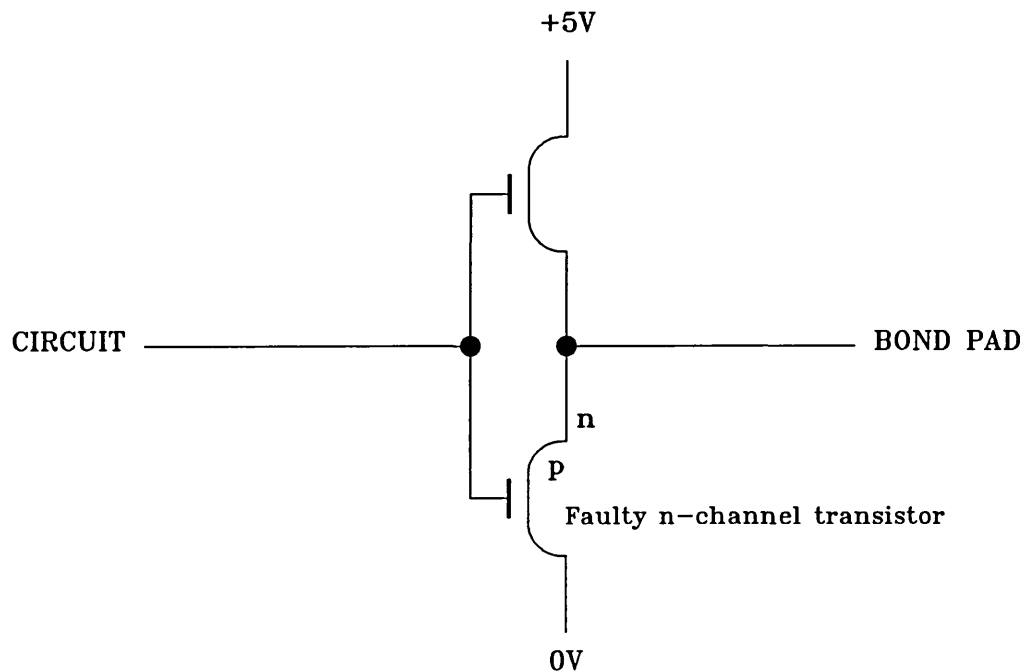


Fig. 88. Circuit diagram of the CT9004 pad-driver circuit. Each transistor represents seven connected in parallel.

would have to be reverse biased in order to cause sufficient, localised energy dissipation (as discussed in section 2.4.3). For this to occur in the drain-body junction of the n-channel transistor would require a large positive voltage to be applied to the pin with respect to ground, reverse biasing the junction. If enough energy was present in the transient, reverse breakdown followed by thermal runaway would cause permanent damage. We can therefore conclude that pin 5 was damaged due to application of a high voltage (positive wrt V_{ss}). In fact, it was later discovered (Private communication, J. King) that failures were due to such high voltages being mistakenly applied by testing equipment.

4.3.2 Electrostatic damage in MA853 circuits

These circuits were used to demonstrate ESD damage location by image processing in section 4.2.6. Two circuits were received from the failure analysis group at GEC Hirst Research Centre after they had been zapped with static electricity under controlled conditions. Similar specimens were generated for a separate Alvey project (ALV/APP/VLSI/052) which partly dealt with various microscopies for detecting ESD.

Zaps had been applied according to a human body model (Fig. 22) using a Hartley Autozap tester. These were charged by a known potential difference before connecting between the test-pin and ground causing a discharge to take place. They were applied with the test-pin negative with respect to ground, and repeated a number of times. Three different conditions were used, and were the same pin for pin on devices #2 and #4 as follows:

5 zaps	at 3 kV	on pins	1, 6, 7, 8, 9, 11
6 zaps	at 4 kV	on pins	12, 13, 14, 15, 18, 19
11 zaps	at 4 kV	on pins	21, 28, 31, 33, 35

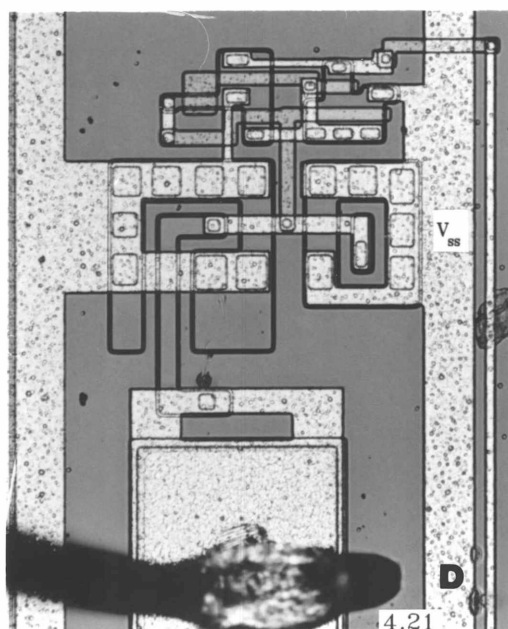
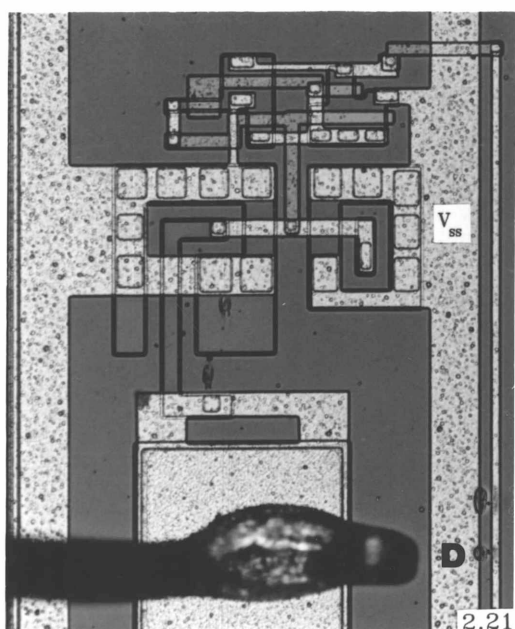
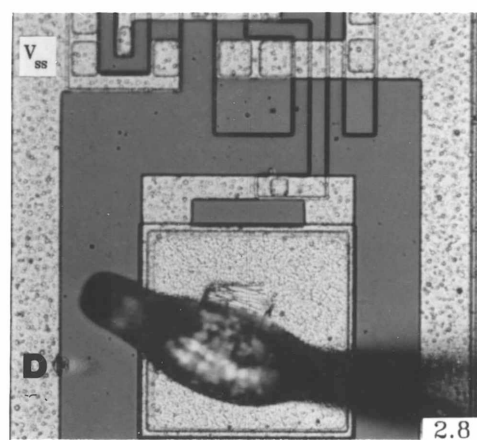
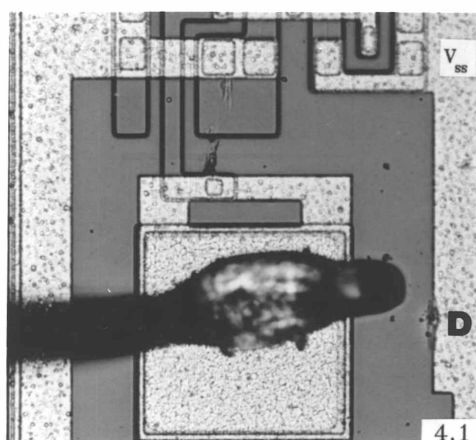
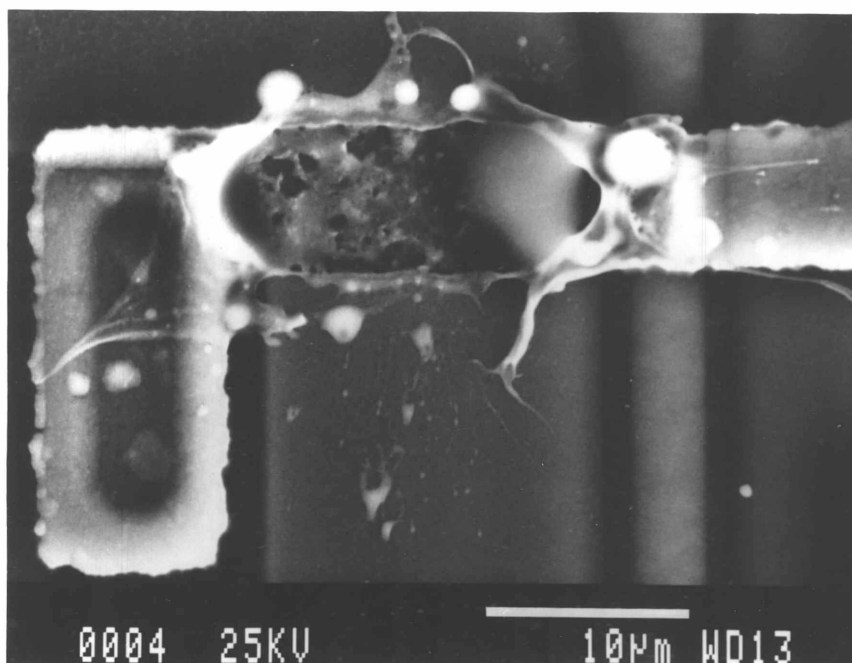
These conditions were such that some of the circuit inputs were exhibiting enhanced leakage currents between the pin and ground.

To examine ESD, the SE mode can be used. Fig. 89 shows a different circuit, an operational amplifier, that received excessively high input currents resulting in obvious metallisation melting. However, if the ESD event contains less energy, it is evident from the figures of section 4.2.6 that SE contrast can be very weak if visible at all. Nevertheless both EBIC and

Fig. 89. Metallisation melting caused by a high energy ESD event in an operational amplifier.

Fig. 90. Examples of direct discharge events (labelled D) from the end of the (dark) bond-wire to the V_{ss} metallisation at pins 4.1 and 2.8.

Fig. 91. Light micrographs of a design weakness in the MA853 chips at pin 21. A discharge (labelled D) occurred adjacent to the bond-wire, between V_{ss} and the input track beyond the protection circuitry.



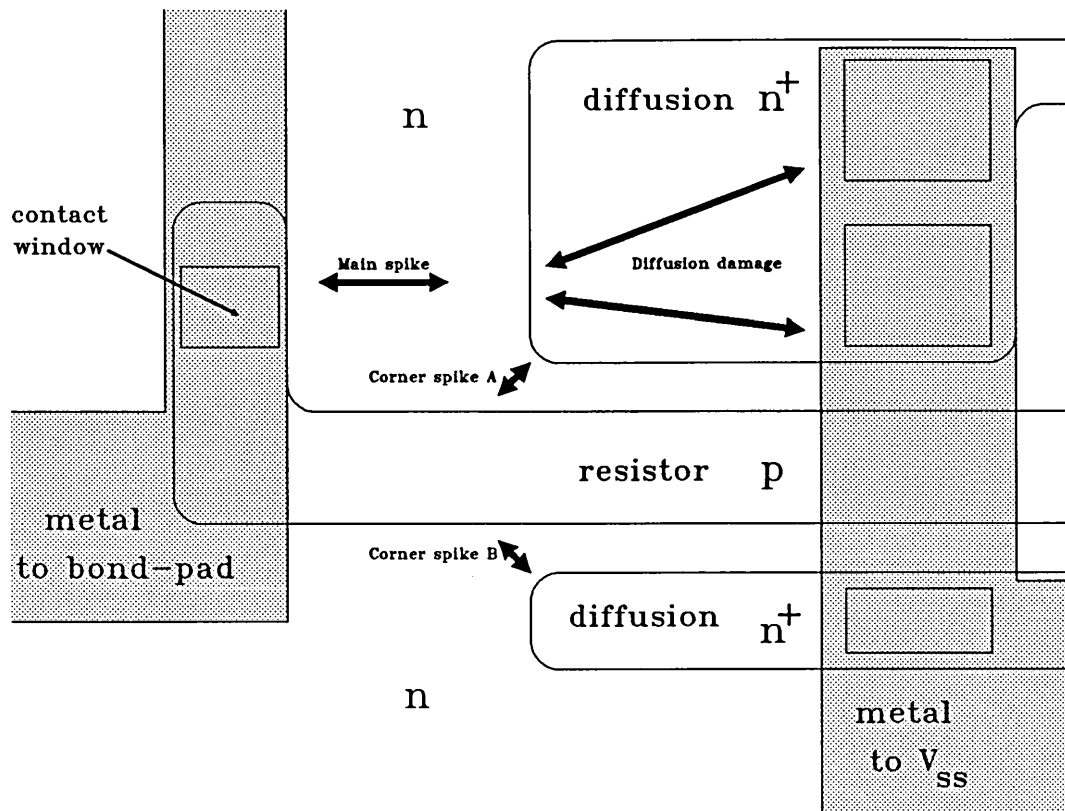


Fig. 92. Plan view of the region containing the four ESD damage sites.

light micrographs were taken of every pin on each circuit. Fig. 92 is a plan view of the region in which four different damage sites were observed, as denoted by double headed arrows. As expected, no two pins showed the same detailed behaviour, but certain common features will now be discussed. The results are summarised in table 4.

4.3.2.1 Light microscopy

Light microscopy is usually the first tool of the failure analyst (Richards and Footner, 1983), and gives information quickly. Several (60%) of the light micrographs exhibited damage to the ground-rail at pins where the end of the bond-wire was close enough to allow arcing between the two due to dielectric breakdown of the atmosphere within the package (labelled D in Fig. 90). As the ground-rail is quite wide, this in itself would not cause

Pin	Optical bond-wire discharge	Optical diffusion damage	EBIC corner spike A	EBIC corner spike B	Leakage current
2.1	×	×	/	×	/
2.6	×	×	/	×	/
2.7	/	/	×	×	/
2.8	/	×	/	×	/
2.9	/	×	/	×	/
2.11	/	×	/	×	/
2.12	×	$\frac{1}{2}$	/	×	×
2.13	×	×	/	×	/
2.14	×	×	/	×	×
2.15	N/A	$\frac{1}{2}$	/	×	×
2.18	N/A	×	/	/	×
2.19	/	$\frac{1}{2}$	/	/	/
2.21	/	/	/	×	×
2.28	N/A	×	/	×	/
2.31	×	$\frac{1}{2}$	/	×	/
2.33	×	/	/	×	×
2.35	N/A	$\frac{1}{2}$	/	×	×
4.1	/	/	/	/	/
4.6	×	$\frac{1}{2}$	/	/	/
4.7	/	/	/	×	/
4.8	×	×	$\frac{1}{2}$	×	×
4.9	/	×	/	×	/
4.11	/	×	/	×	×
4.12	/	$\frac{1}{2}$	/	×	/
4.13	/	$\frac{1}{2}$	/	×	/
4.14	/	$\frac{1}{2}$	/	×	/
4.15	N/A	$\frac{1}{2}$	/	×	×
4.18	N/A	×	/	/	/
4.19	/	/	/	/	×
4.21	/	/	/	/	×
4.28	N/A	/	/	×	/
4.31	×	/	/	×	/
4.33	×	$\frac{1}{2}$	/	×	/
4.35	N/A	$\frac{1}{2}$	/	×	/
Total	57%	96%	21%	44%	65%

Table 4. Occurrences of various damage types in the MA853 circuit inputs.

/ = defect present,

×

$\frac{1}{2}$ = marginal defect,

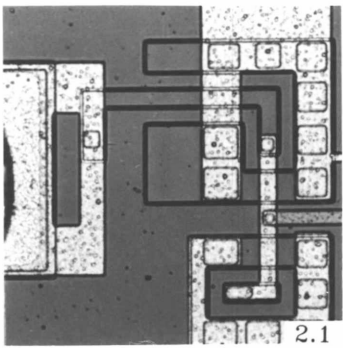
N/A = not applicable because bond-wire didn't approach V_{ss} .

failure unless enough heat was generated to puncture the isolation oxide which separates the ground metallisation from the substrate. Indeed, in some designs spark-gaps are a part of the protection circuitry in the form of adjacent saw-tooth patterns in the ground and input-pin metallisation. Any similar effect due to bond-wire placement is relatively uncontrollable at the design stage and consequently is undesirable. One case of a reliability problem was at pin 21 (Fig. 91). In this case, the aluminium track emanating from the protection circuitry ran back at a minimal distance from the ground-rail. At D the track was opposite the bond-wire overhang, a discharge between the metal track and ground-rail occurred. This is serious because a narrow circuit track has been subject to damage. The bond-wire may have induced a localised charge on the adjacent ground-rail, enhancing the electric field between the ground-rail and circuit track sufficiently to nucleate the breakdown site.

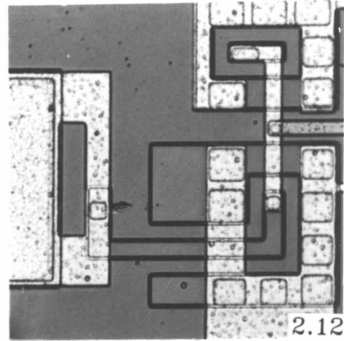
The input circuitry itself was also damaged in most cases, and this showed up as dark lines leading from the bond-pad contact window ("main spike" in Fig. 92). This is where the metallisation contacts the silicon, making it the most favourable discharge path. A representative selection of micrographs is shown in Fig. 93. A whole spectrum of damage occurred, from none (pin 2.11) in one case, through a small line (pin 2.1), multiple lines (pin 4.15) to large fractures in the passivation (pin 2.28). Generally, damage increased with the applied stress particularly the number of zaps (6×4 kV cf 11×4 kV), and none of the pins stressed at 11×4 kV showed mild damage at all. Nevertheless, some pins zapped at only 5×3 kV showed severe damage (pin 4.8). All this is consistent with the random element involved in discharge processes. In 40% of cases lines were visible at the diffusion opposite the contact window ("diffusion damage" in Fig. 92). This damage was quite well correlated with stress conditions.

*Left**5 × 3 kV**Centre**6 × 4 kV**Right**11 × 4 kV*

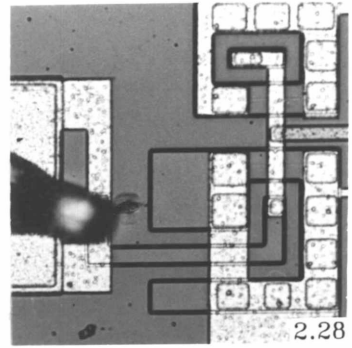
Fig. 93. A representative selection of light micrographs of the damaged MA853 input circuitry, tested under the number of zaps and charging voltage given above.



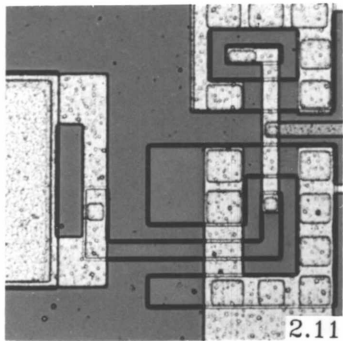
2.1



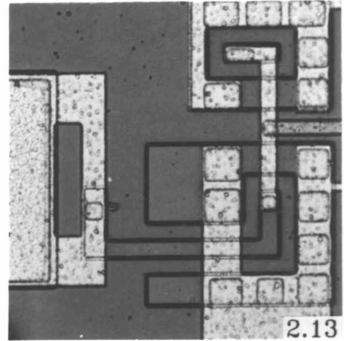
2.12



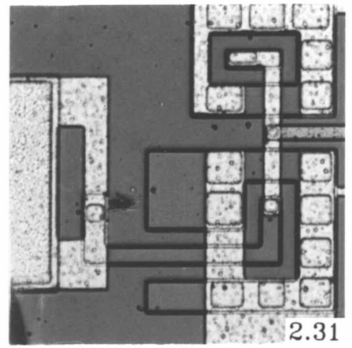
2.28



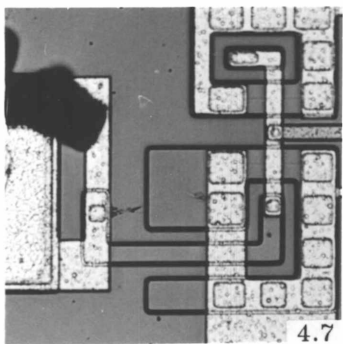
2.11



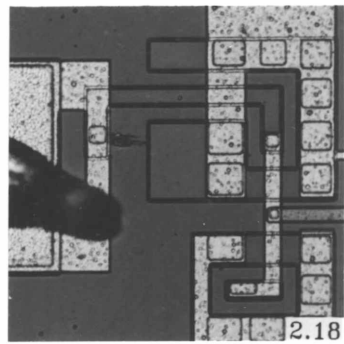
2.13



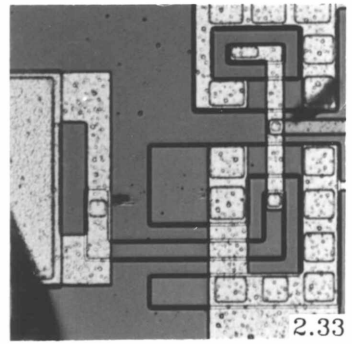
2.31



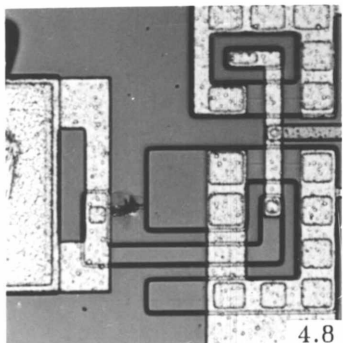
4.7



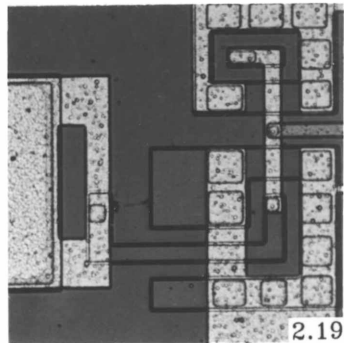
2.18



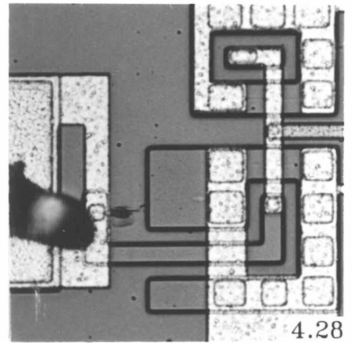
2.33



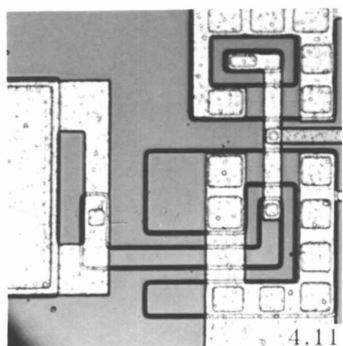
4.8



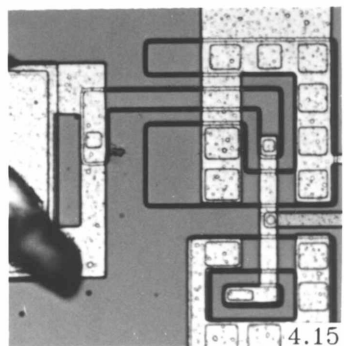
2.19



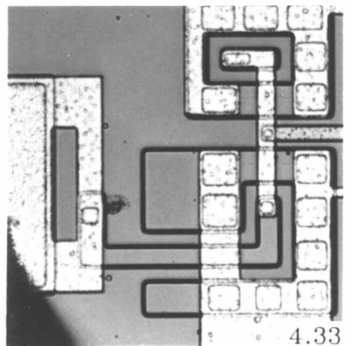
4.28



4.11



4.15



4.33

These dark lines may be due to cracks in the passivation and isolation oxide layers above the silicon, and are the most usual manifestation of ESD reported. The heat generated in second breakdown originates in the silicon, and the shortest route between metallisation contact windows is near the surface. The linear thermal expansion coefficient of SiO_2 (5×10^{-7}) is five times smaller than that of Si (2.6×10^{-6}). Thus, local heating in the vicinity of the Si-SiO₂ interface will cause the SiO₂ to be in tension. Furthermore, the thermal conductivity of silicon ($0.6 \text{ Wcm}^{-1}\text{K}^{-1}$) is 42 times larger than for SiO₂ ($0.014 \text{ Wcm}^{-1}\text{K}^{-1}$), so heat generated close to the interface would diffuse away more slowly, making it a more likely location for thermal damage.

4.3.2.2 Qualitative EBIC microscopy

EBIC images from all of the pins of both devices are shown in Fig. 94 ($5 \times 3 \text{ kV}$), Fig. 95 ($6 \times 4 \text{ kV}$) and Fig. 96 ($11 \times 4 \text{ kV}$). The damage is on the left side of each image (cf Fig. 92). Their precise location can be seen by referring to the numerous full images of section 4.2.6.

Before discussing the contrast of the defects it is necessary to consider that of the circuit itself. Referring to Fig. 92, the following conclusions can be drawn about the relevant features:

The "resistor" is connected directly to the bond-pad and hence to the I_{sc} amplifier terminal. As the resistor is bright, I_{sc} was positive. To give a positive current, carriers separated by the resistor pn-junction on the resistor side must be holes. Hence the resistor is p-type, and the substrate n-type.

The "diffusion" shows only weak contrast, and is connected to the V_{DD} metallisation rail, which is in turn connected to ground. Any charge collection current flowing into this contact must be due to electrons in order

Fig. 94. EBIC images of all input pins of MA853 circuits tested with 5×3 kV pulses, on device #2 (left) and #4 (right).

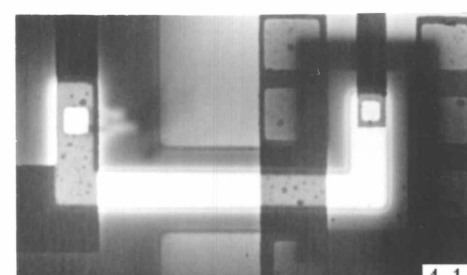
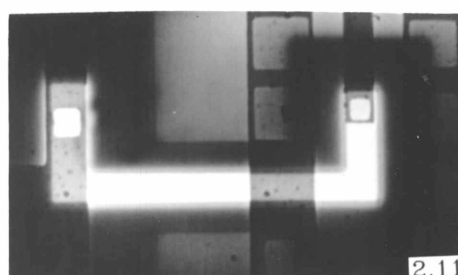
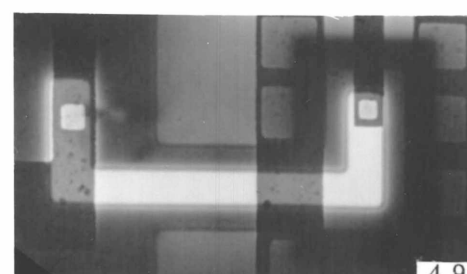
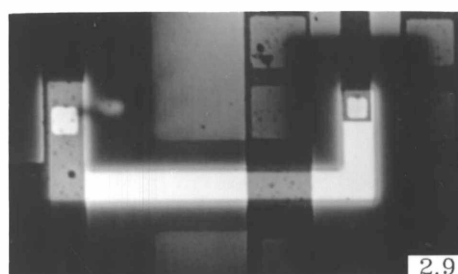
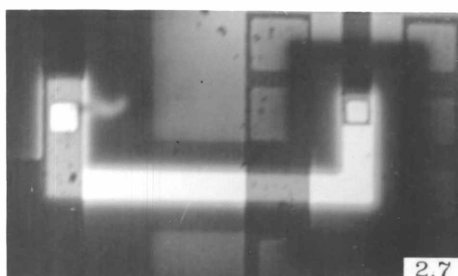
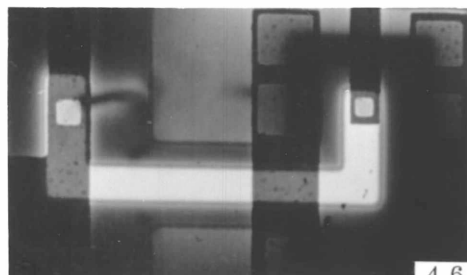
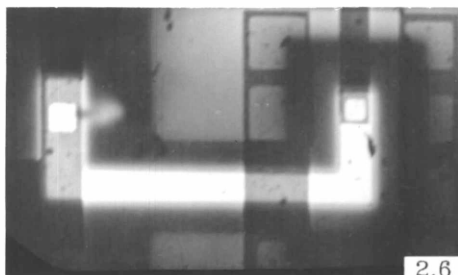
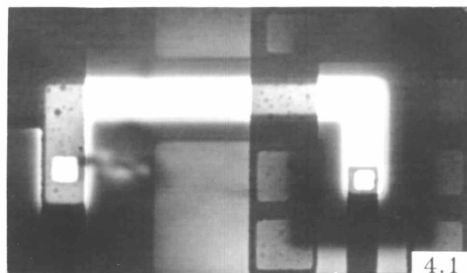
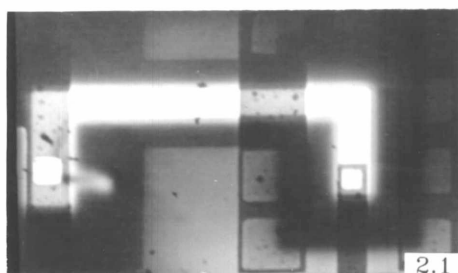
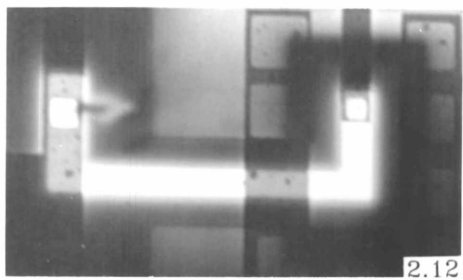
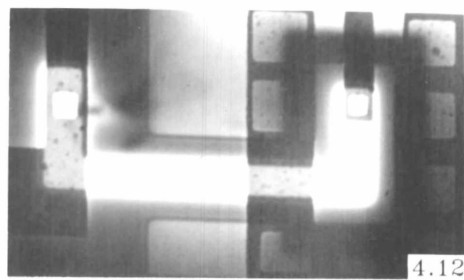


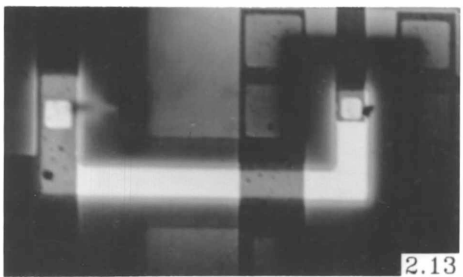
Fig. 95. EBIC images of all input pins of MA853 circuits tested with 6×4 kV pulses, on device #2 (left) and #4 (right).



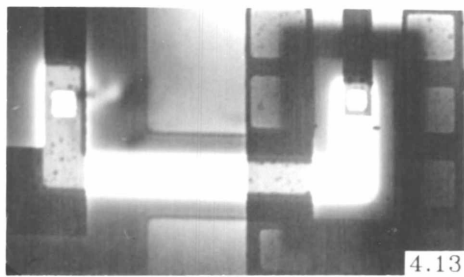
2.12



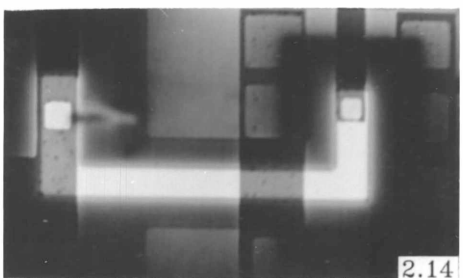
4.12



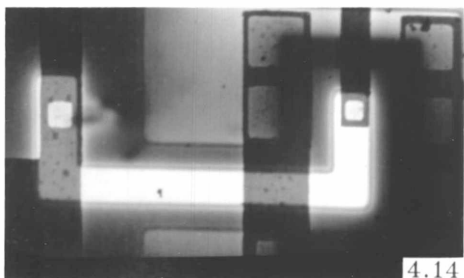
2.13



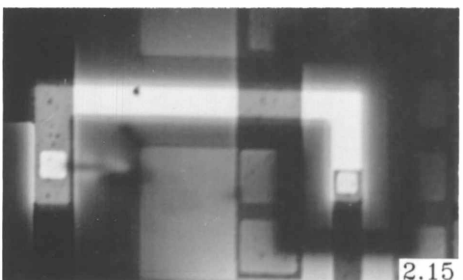
4.13



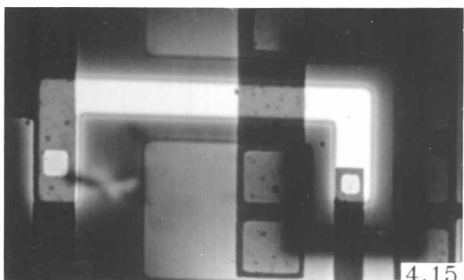
2.14



4.14



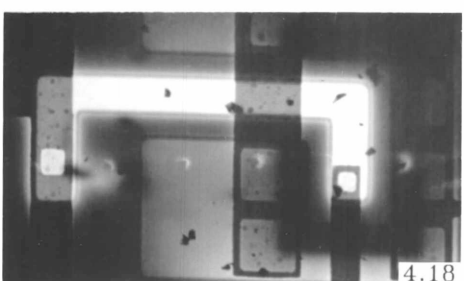
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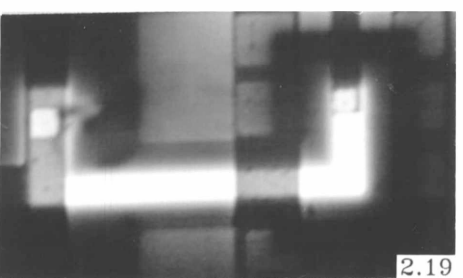
4.15



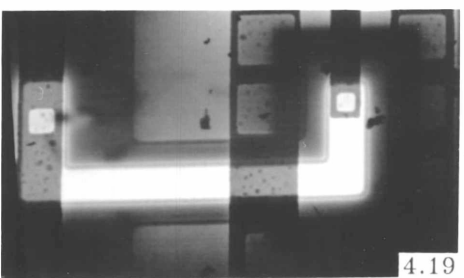
2.18



4.18

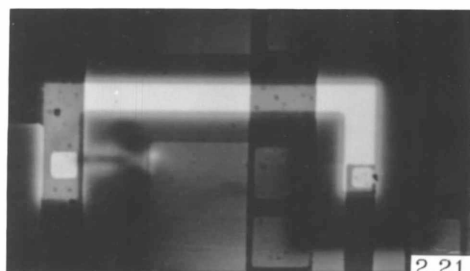


2.19

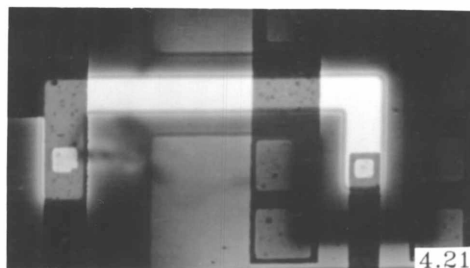


4.19

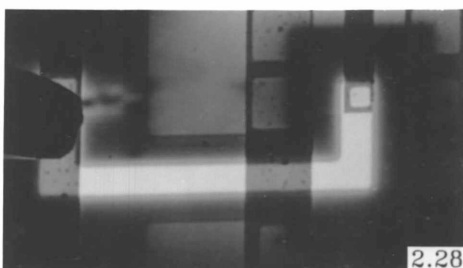
Fig. 96. EBIC images of all input pins of MA853 circuits tested with 11×4 kV pulses, on device #2 (left) and #4 (right).



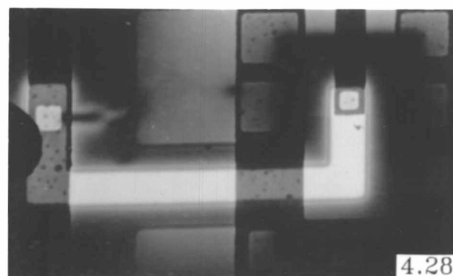
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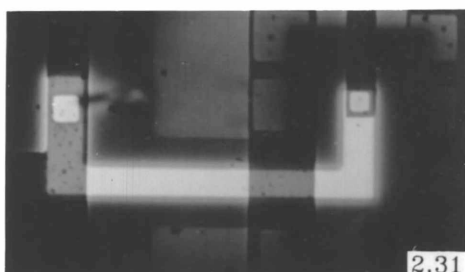
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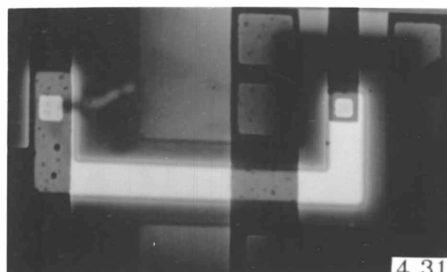
2.28



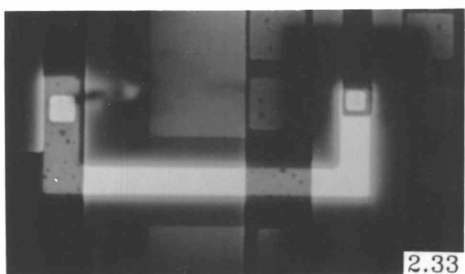
4.28



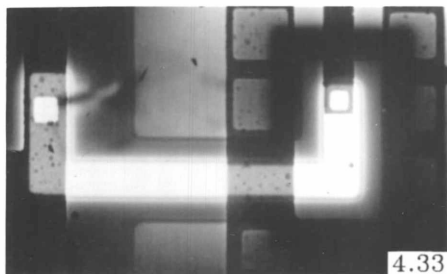
2.31



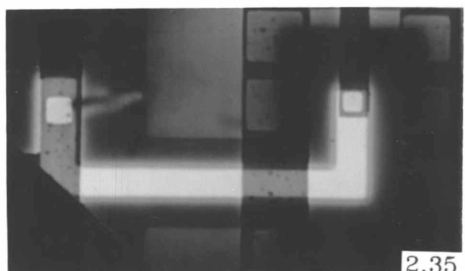
4.31



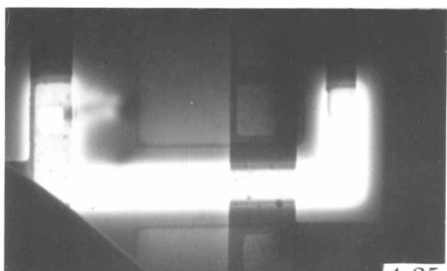
2.33



4.33



2.35



4.35

to give a positive signal output. This is consistent with an n^+ diffusion, making a nn^+ bulk electron voltaic effect which separates electrons to the n^+ side. The holes which are separated to the substrate have to either diffuse to the resistor, and be collected, or if they recombine, would accumulate, reducing the nn^+ barrier voltage to maintain equilibrium. The nett result is that the charge collection current is rather weak. The n^+ diffusion was a guard-ring for the protection diode to V_{DD} .

EBIC contrast due to the four defect sites of Fig. 92 will now be discussed:

Corner spike A

These were regular dark lines extending diagonally from the diffused resistor to the corner of the guard diffusion, because of the electric field concentration. The defects locally decreased the collection efficiency, due to a decreased minority carrier lifetime. This caused recombination before carrier collection by the resistor pn junction. It is likely that the dark defects were regions where silicon dielectric breakdown and the resulting heat generation induced crystal disorder. Associated trap-levels in the band-gap subsequently enhanced minority carrier recombination.

Corner spike B

These were identical in character to those at A, but occurred less frequently. This implies the electric field was less intense on that side.

Diffusion damage

This occurred in the guard diffusion opposite to the bond-pad contact window, and consisted of irregular dark paths. Damage increased in severity with increasing pulse voltage and number of repeats. The

origin of the dark contrast was most likely the same as in corner spike A, i.e. silicon dielectric breakdown, leading to crystal imperfections and a reduced carrier lifetime.

Main spike

This was present in all the damaged inputs, and consisted of a bright region extending from the bond-pad contact window towards the diffusion. The bright region was accompanied by dark filaments in most cases. They tended to combine as a dark line with a white halo, although in some cases were more uneven (e.g. 4.15 in Fig. 95). Such spikes were usually visible in light micrographs as passivation cracks, although this was sometimes a poor damage indicator (e.g. 2.1 in Figs. 93,94). In all cases there was a close correlation between the site of the EBIC damage and the cracks, although the bright/dark parts of the EBIC contrast showed little detailed correlation with the cracks. It therefore seems the cracks were purely a secondary heating effect, and that only EBIC identifies electrical damage. The bright region is believed to be due to aluminium migration on the following grounds. For the negative zaps, the pn junction near the bond-pad contact window would be in reverse bias, and hence subject to second breakdown (section 2.4.3). Aluminium is a p-type dopant in silicon, and when ionised, is negative, hence diffusion away from the contact window would be field-assisted. Such electro-thermomigration is well known (Christou, 1973), and would explain the apparent extension of a p-type region away from the contact window. Dopant diffusion is a further possibility, but the concentration of boron available in the resistor is orders of magnitude lower.

A general comparison of Figs. 94–96 does indicate the expected increase in damage. Comparing Fig. 94 and Fig. 95, the increase in zap voltage increases the size of the main spike. On increasing the number of zaps, (Figs. 95 and 96), diffusion damage becomes slightly more prominent. The dark defects (A,B and the diffusion damage) do not fit into the three categories usually described for ESD damage (2.4.3). There is no evidence of junction burnout in these cases, as the damage is not localised at junctions. Rather, it seems that such electrically active defects are due to dielectric breakdown of silicon, and associated Joule heating.

The above observations disagree with the report of Wakefield and Videlo (1989). They examined what appeared to be an identical circuit structure and contended that EBIC could not add to the information available using the light microscope. With light microscopy they reported only the last of the four damage types observed with EBIC in this work.

4.3.4 Quantitative EBIC analysis of the MA853 input structure

By varying the electron beam energy, and hence the penetration depth, information about the depth of specimen features can in principle be obtained. A computer program was written to allow extremely fast, convenient acquisition of EBIC linescans, using a Matelect EBIC amplifier, equipped with a computer interface unit. The linescans obtained were stored on hard-disk, and contain all data necessary for fully quantitative measurements, as discussed in section 3.2.5.

In this work the intention was to investigate the extent to which quantitative EBIC could be applied to glean information about defects once they had

been located by image processing. These ESD defects were chosen, as their origin was well known, and many similar defects were available. The main spikes ran roughly parallel to the diffused resistor leading from the bond-pad. The resistor was used as a reference structure, as its geometry was reasonably well known. Linescans were taken perpendicular to the resistor, as shown in Fig. 97a. The cross-section along these paths (Fig. 97b) includes the resistor pn-junction, and the step in the oxide due to the window cut in the oxide to mask the p-type deposition and subsequent diffusion. In Fig. 97c, linescans at 20, 30 and 40keV are shown, with I_{sc} converted digitally to collection efficiency using equation (8).

4.3.4.1 Oxide thickness

Neither the oxide coating thickness nor the resistor junction depth were known. However, using charging, an estimate of the thicknesses d_r and d_o was made by varying the SEM beam energy. In Fig. 98a at low E_b , the excitation volume is totally within the insulating oxide layer. Hence the injected beam current cannot escape, and the surface charges negatively, giving the characteristic bright charging effect, as the local electric field repels a greater number of secondary electrons from the surface. In Fig. 98b at higher E_b , the excitation volume completely penetrates the oxide. Then, many electron-hole pairs are generated along this path, and this momentary increase in carrier density increases the oxide conductivity enough to allow the injected beam current to flow to the silicon and then to earth. In practice, a small positive charge may build up as in the case of the gate oxides in MOS transistors, but its magnitude will be much smaller. Nevertheless, in the high E_b case there will be no negative charging.

Considering the uncontrollable nature of charging, this technique worked surprisingly well. The series of linescans in Fig. 99a,b were taken by

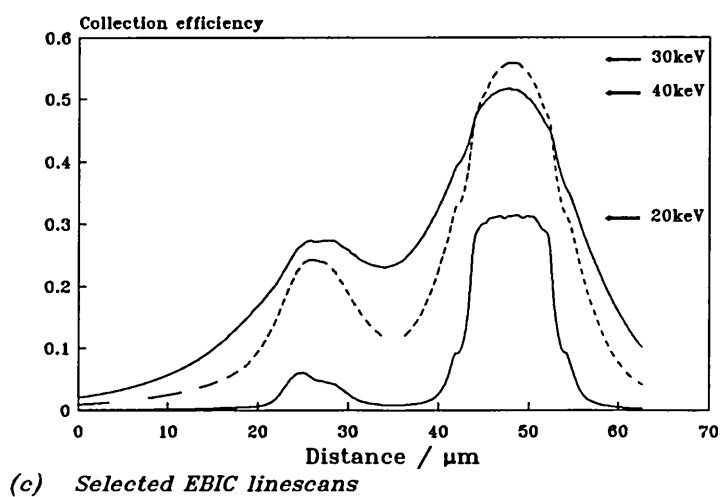
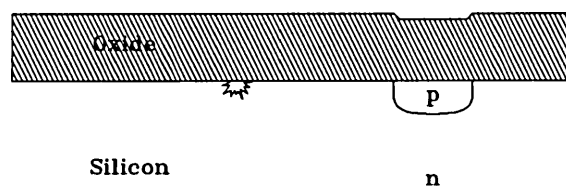
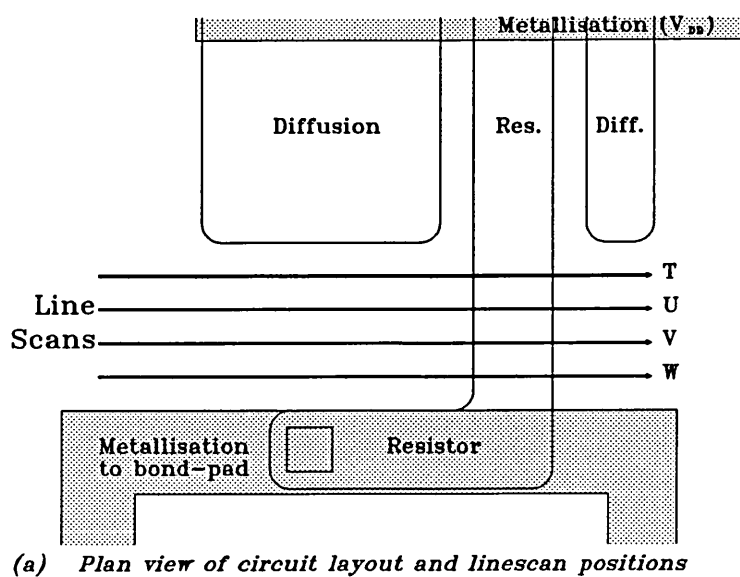
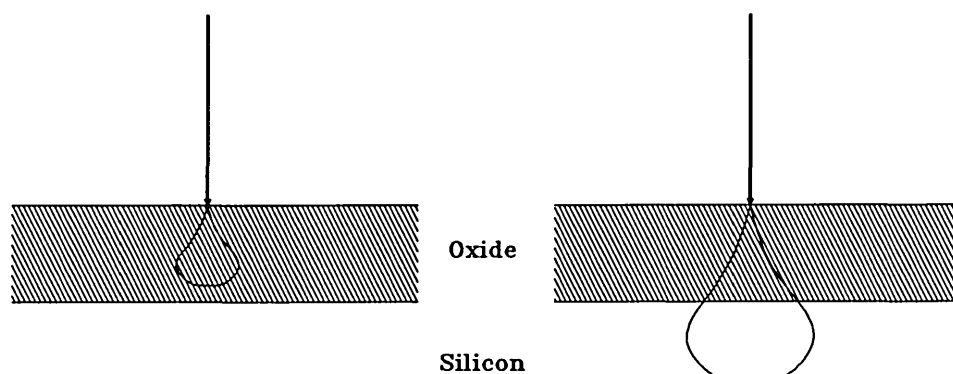


Fig. 97. Configuration from which EBIC linescans of the MA853 were obtained.



(a) Low beam energy

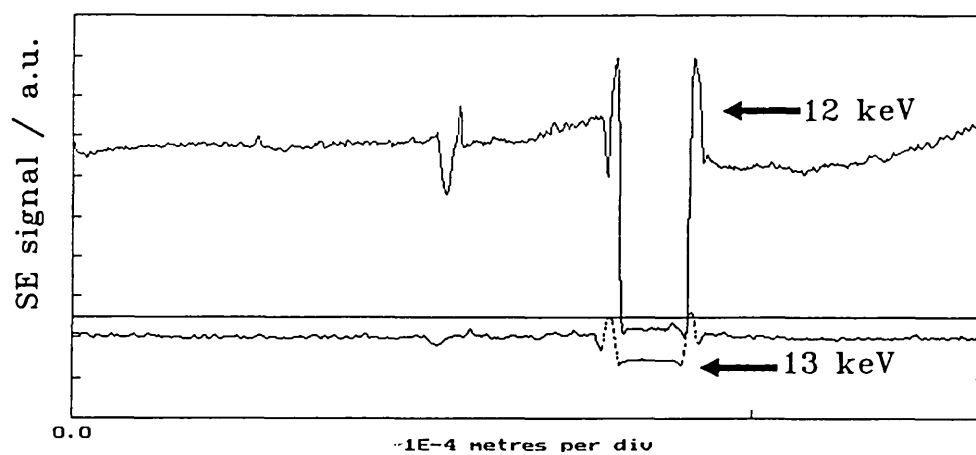
(b) High beam energy

Fig. 98. Method of oxide depth determination by oxide charging.

connecting the microscope SE signal to the auxiliary input of the INTU-5 and using the Matelect program. These scans of secondary electron emission current vs distance were recorded between scans U and V of Fig. 97a. At high E_b with no charging, the scan was flat except for small perturbations at the oxide steps. At low E_b , charging elevated the SE signal to a higher level. So, on decreasing from 13 keV to 12 keV (Fig. 99a) the surrounding oxide began to charge, and the SE signal either side of the resistor increased. It was not until the 10–9 keV transition that oxide above the resistor became bright as well (Fig. 99b). The small peak to the left on some of the scans was due to differential charging at the crack caused by the ESD. All of the transitions were also clearly evident in TV rate observation of the SE images over a wide range of probe currents.

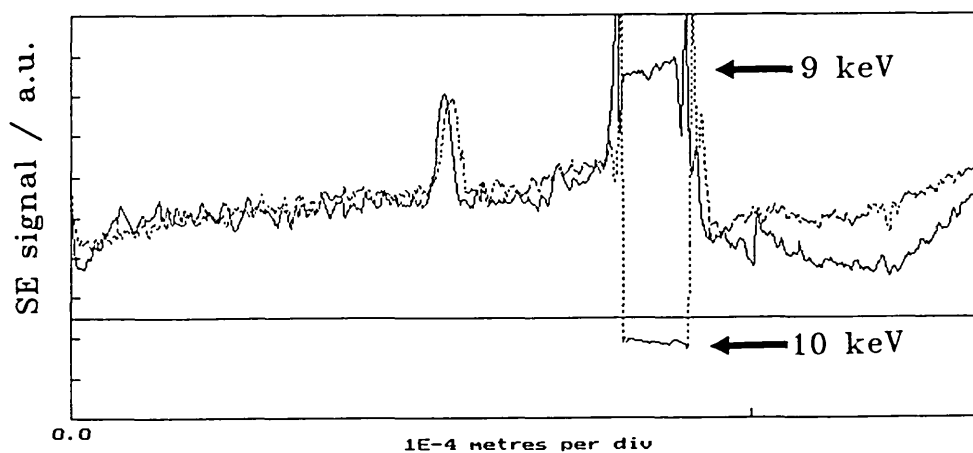
The depth of penetration of electrons at these E_b can be determined from the Grün range given by equation (1), using the density of $\text{SiO}_2 = 2.3 \text{ gcm}^{-3}$. The Everhart–Hoff polynomial (equation 2) falls to zero at $1.1R_G$, so for the relevant beam energies

J. D. Russell - MATELECT Control Program, Version 4.23



(a) Charging transition between 12 and 13 keV.

J. D. Russell - MATELECT Control Program, Version 4.23



(b) Charging transition between 9 and 10 keV.

Fig. 99. Linescans across oxide in MA853 showing the charging transitions as a function of E_b , enabling the thickness to be estimated.

$$\begin{array}{rcl}
 1.1R_G(9) & = & 0.94 \mu\text{m} \\
 1.1R_G(10) & = & 1.1 \mu\text{m} \\
 1.1R_G(12) & = & 1.5 \mu\text{m} \\
 1.1R_G(13) & = & 1.8 \mu\text{m}
 \end{array}
 \left. \vphantom{\begin{array}{rcl} 1.1R_G(9) \\ 1.1R_G(10) \\ 1.1R_G(12) \\ 1.1R_G(13) \end{array}} \right\}
 \begin{array}{l}
 d_r \approx 1.0 \mu\text{m} \\
 d_o \approx 1.6 \mu\text{m}
 \end{array}$$

Analysis of the radiation damage results has shown that carriers may in fact be generated somewhat deeper, so the above thicknesses of $d_r \approx 1.0 \mu\text{m}$ and $d_o \approx 1.6 \mu\text{m}$ should be regarded as lower limits.

4.3.4.2 Deconvolution of linescans

The lateral resolution of EBIC linescans is mainly limited by the size of the electron beam excitation volume. To a good approximation the linescan is smeared by the electron beam lateral dose function, $g(x)$, of the energy deposited within the silicon. This function was determined using 10,000 electron Monte Carlo simulations at each beam energy for the oxide thickness determined by the charging experiments. The Monte Carlo output matrix was integrated laterally in the silicon only, to give $g(x)$. Some results of these calculations are shown in Fig. 100, for 20, 30 and 40 keV, and oxide thicknesses of $1.1 \mu\text{m}$ and $1.8 \mu\text{m}$. It is apparent from the figure that the lateral dose function is relatively insensitive to the oxide thickness assumed, in the region of study.

With this knowledge of $g(x)$, the smearing process can be written as a convolution:

$$\eta'_{cc}(x) = \eta_{cc}(x) * g(x) \quad (66)$$

where η_{cc} = true collection efficiency from equation (8),
 η'_{cc} = actual measured collection efficiency.

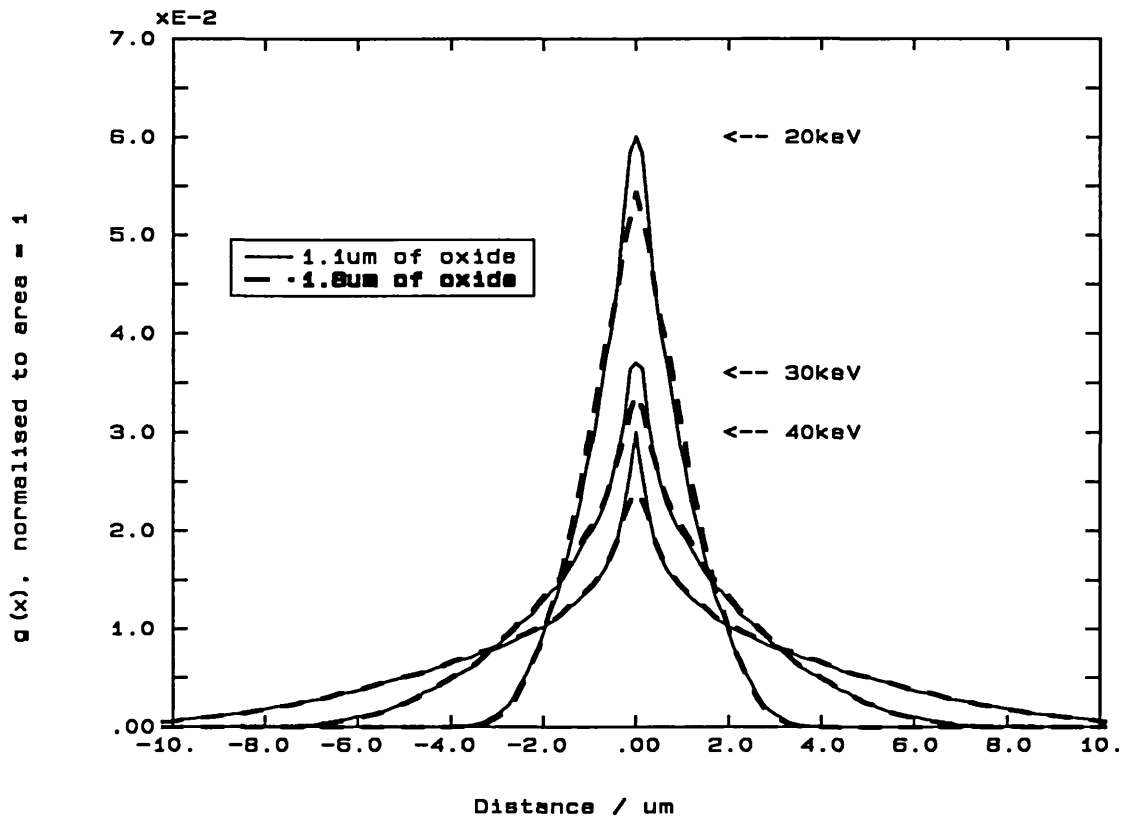


Fig. 100. Lateral dose function in silicon covered by 1.1 and 1.8 μm of SiO_2 .

It is well known from the convolution theorem (Riley, 1978, p221) that on taking Fourier transforms the right hand side becomes a product. Thus, on rearranging, the true charge collection efficiency,

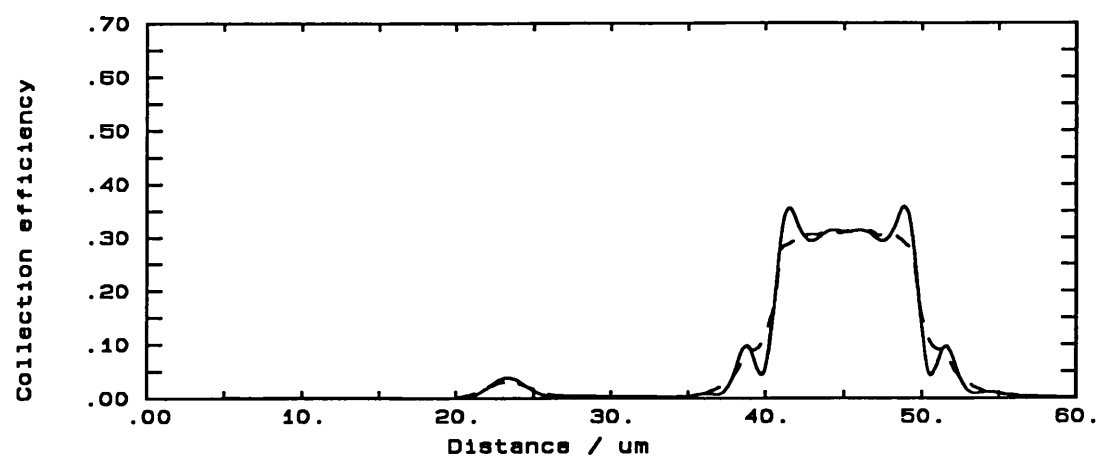
$$\eta_{cc}(x) = F^{-1} \left\{ \frac{F \left[\eta'_{cc}(x) \right]}{F \left[g(x) \right]} \right\} \quad (67)$$

where F represents Fourier transformation and the process on the right is referred to as deconvolution. However, at x for which $|F[g(x)]|$ approaches zero, the quantity in brackets approaches infinity, and if $|F[\eta'_{cc}(x)]|$ is also zero it becomes indeterminate. On inverse transformation such components appear as severe noise spread across the whole linescan. Fortunately, EBIC profiles do not usually have extremely sharp features, as

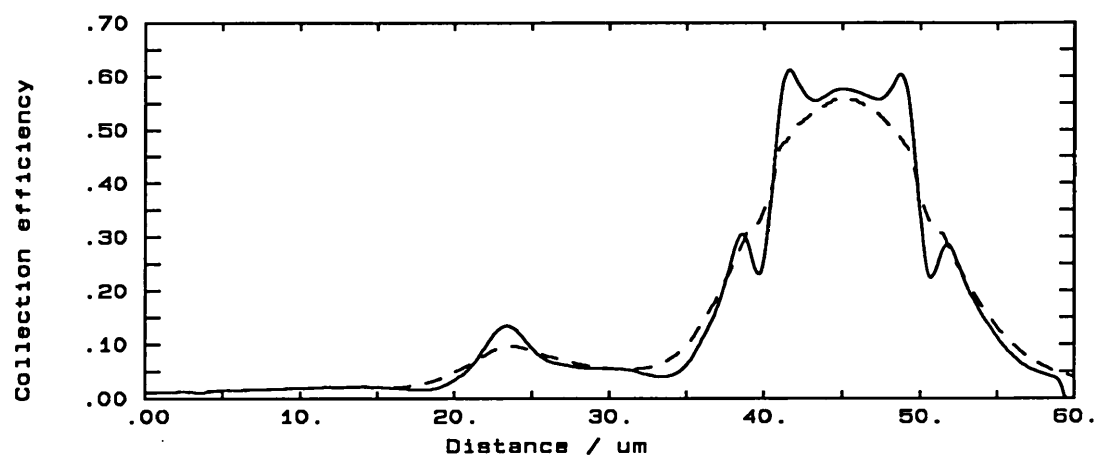
they are smoothed out by the effect of carrier diffusion, and also, in this case a large number of acquired points (512) means good resolution. The "noise" could therefore be removed by smoothing without information loss. The Asyst SMOOTH function is a low-pass filter, optimised to produce minimal ringing, and has a variable cut-off frequency. By trial and error, this was adjusted until all of the "noise" was removed.

To do the digital deconvolution, it was also necessary to convert the x -increments of $g(x)$ to the same as those for the linescan by interpolation, normalise, and pad the final array with zeroes to match that of η'_{cc} (512 points).

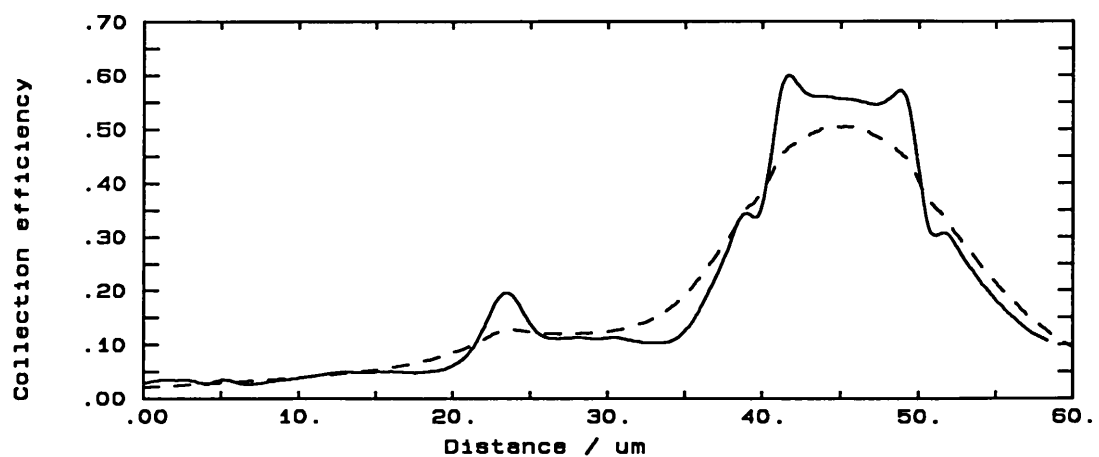
Results are shown in Fig. 101–104 for linescans T, U, V, W, taken progressively further from the bond-pad. Only 20, 30, 40 keV are shown for clarity. The resistor profile shows the same behaviour in each case. At 20 keV, the central flat region at the resistor was unchanged on deconvolution as expected, since at low E_b , $g(x)$ was relatively narrow and only rounded the edges of the resistor profile. At 30 and 40 keV (Fig. 101–104b,c) the deconvolved shape was similar, in particular the central flat region was well reconstructed. The peaks either side are believed to be due to incidence on the vertical section of the pn-junction giving enhanced collection. In contrast to the work of Chi and Gatos (1977), the peaks do not disappear at high E_b because for a deconvolved linescan the contribution due to the horizontal junction section should be suppressed. The subsidiary peaks half way down the resistor profile are believed to be related to the surface oxide step. This would be caused by the change in oxide thickness, junction depth and also the backscattered electron fraction due to topography.



(a) 20keV

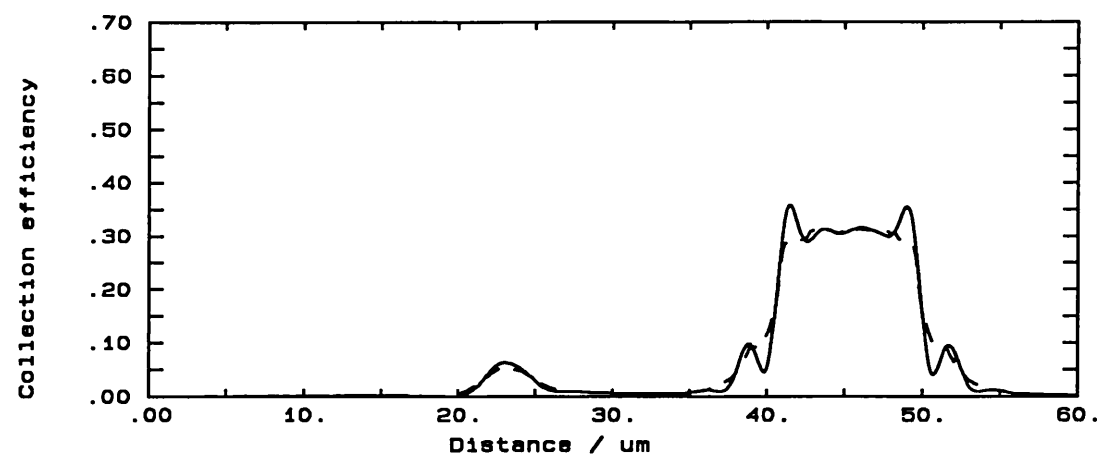


(b) 30keV

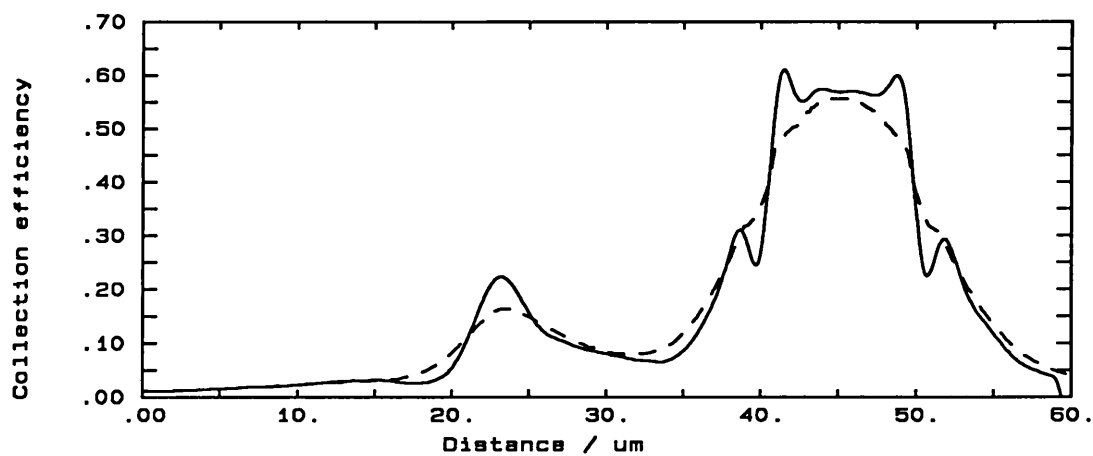


(c) 40keV

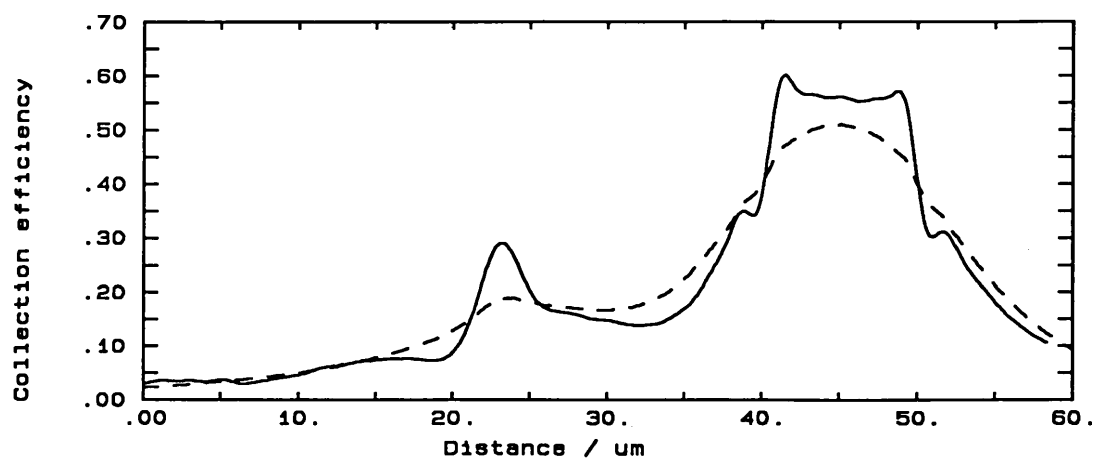
Fig. 101. Deconvolved EBIC linescans across path T of Fig. 97 at 20, 30, 40 keV, closest to the guard diffusion. The dashed line is the original scan.



(a) 20keV



(b) 30keV



(c) 40keV

Fig. 102. Deconvolved EBIC linescans across path U of Fig. 97 at 20, 30, 40 keV. The dashed line is the original scan.

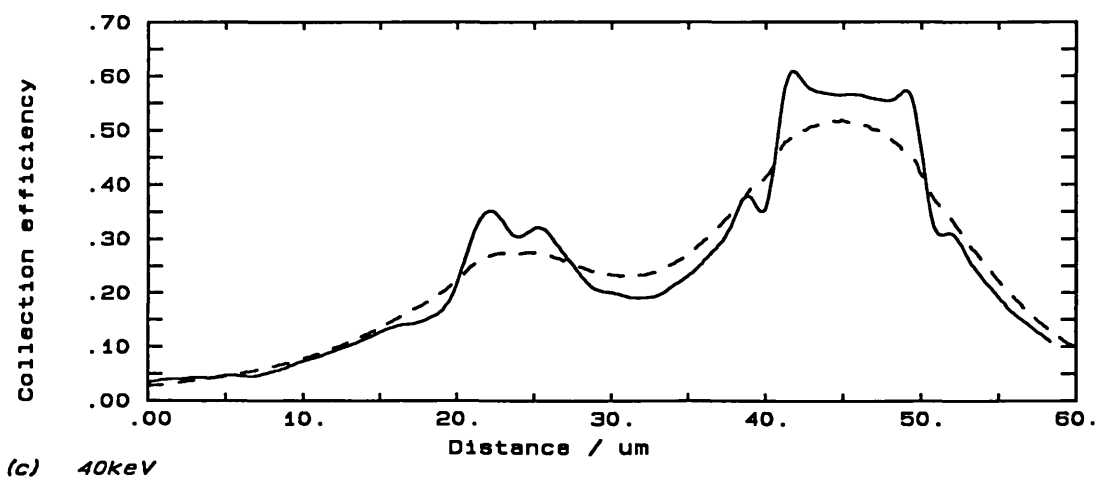
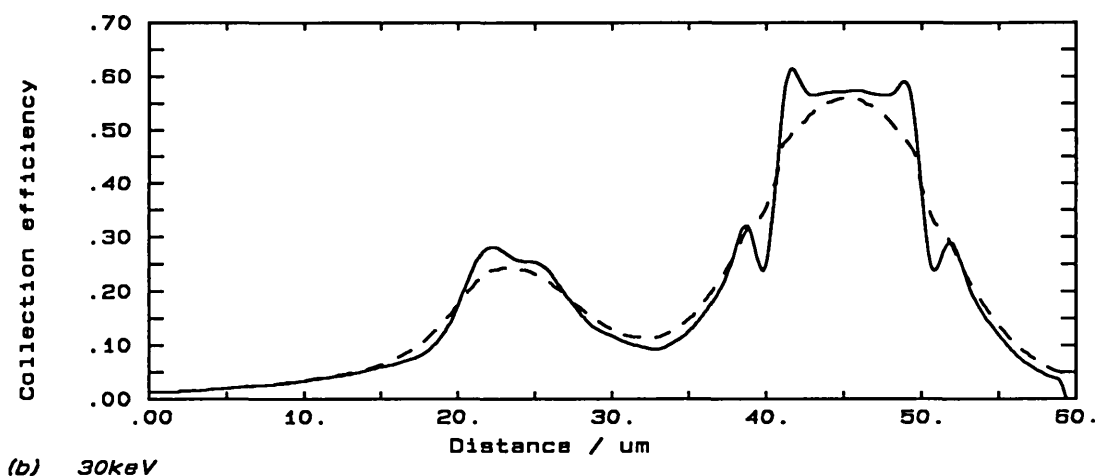
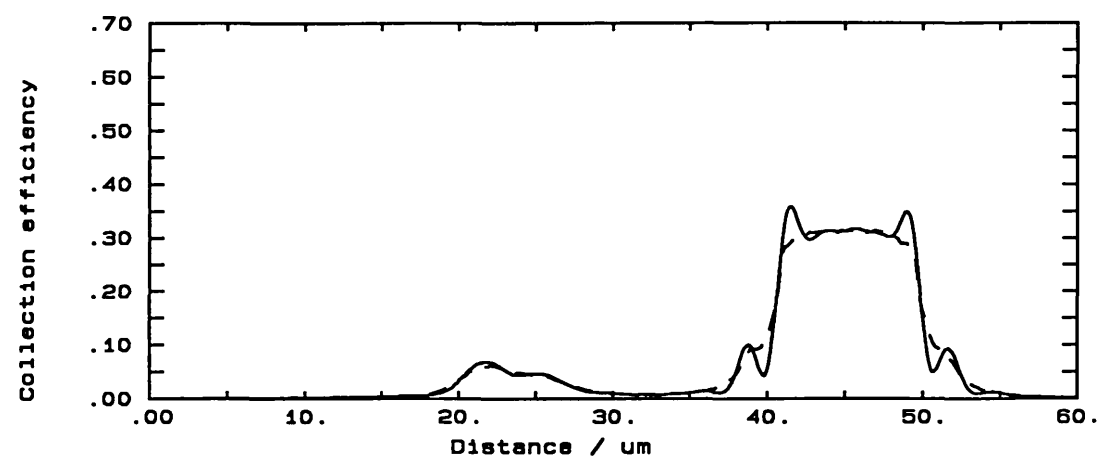
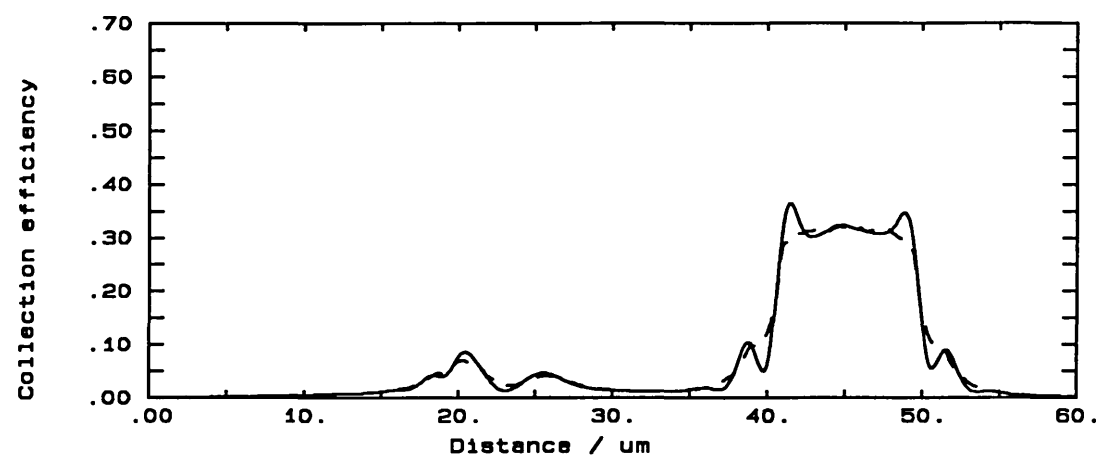
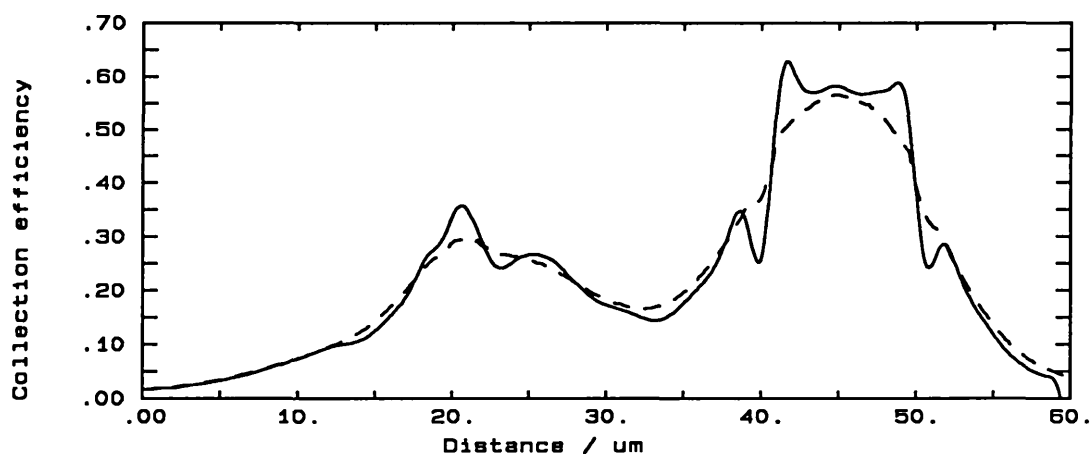


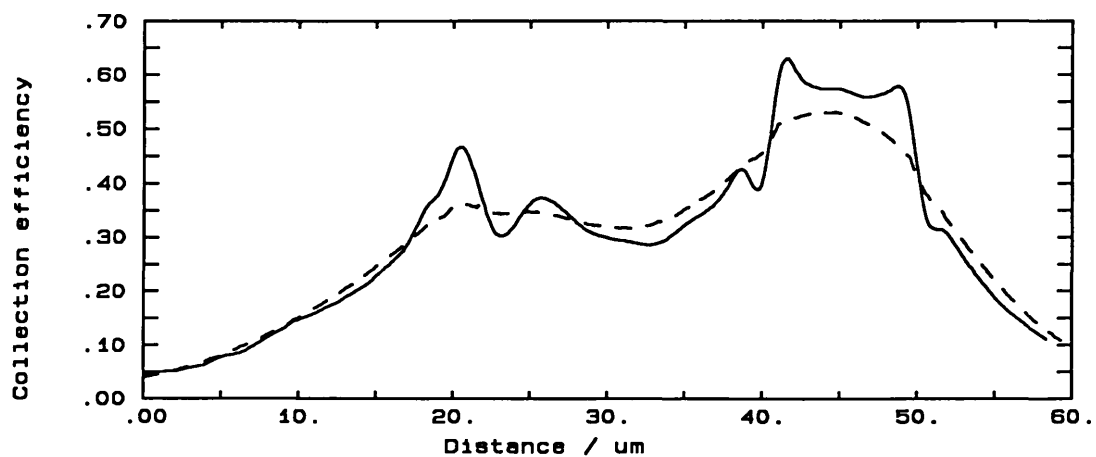
Fig. 103. Deconvolved EBIC linescans across path V of Fig. 97 at 20, 30, 40 keV. The dashed line is the original scan.



(a) 20keV



(b) 30keV



(c) 40keV

Fig. 104. Deconvolved EBIC linescans across path W of Fig. 97 at 20, 30, 40 keV, closest to the bond-pad contact window. The dashed line is the original scan.

The dual peak-structure of the ESD contrast was also enhanced, most markedly at 40 keV, and for paths V and W where it was hardly resolvable in the original. On scans T and U however, only the left peak is present. It seems that the EBIC contrast is due to two mechanisms:

- (i) A disrupted discharge path – possibly a melt-filament, causing lifetime degradation and dark contrast, as observed in the other damaged regions,
- (ii) A p-region extending towards the guard diffusion, probably consisting of electro-thermomigrated aluminium.

It is also likely that (i) generated the heat to enable (ii) to occur. If η_{cc} vs E_b is plotted for the ESD peak of scans T, U, V, and W (Fig. 105a) η_{cc} is attenuated with distance from the bond-pad due to series resistance. If the scans are normalised (Fig. 105b), the variation is very similar for each scan. Given the spread of the data points it is not realistic to draw conclusions about the depth variation of the static damage with distance along the discharge path, and it may, indeed follow the Si-SiO₂ interface.

4.3.4.3 Resistor collection efficiency variation with E_b

The deconvolved linescans all showed similar variation of η_{cc} with E_b at the diffused resistor. The vertical cross-section of the resistor was more complex than those usually employed in quantitative EBIC work. However, the variation of η_{cc} with E_b exhibited a maximum, suggesting that the excitation volume was penetrating beneath the junction. It thus appeared to be possible to derive some information from such plots. So, a one dimensional model of the collection probability was postulated as shown in Fig. 106, based on relationships derived by Donolato. Using the variables

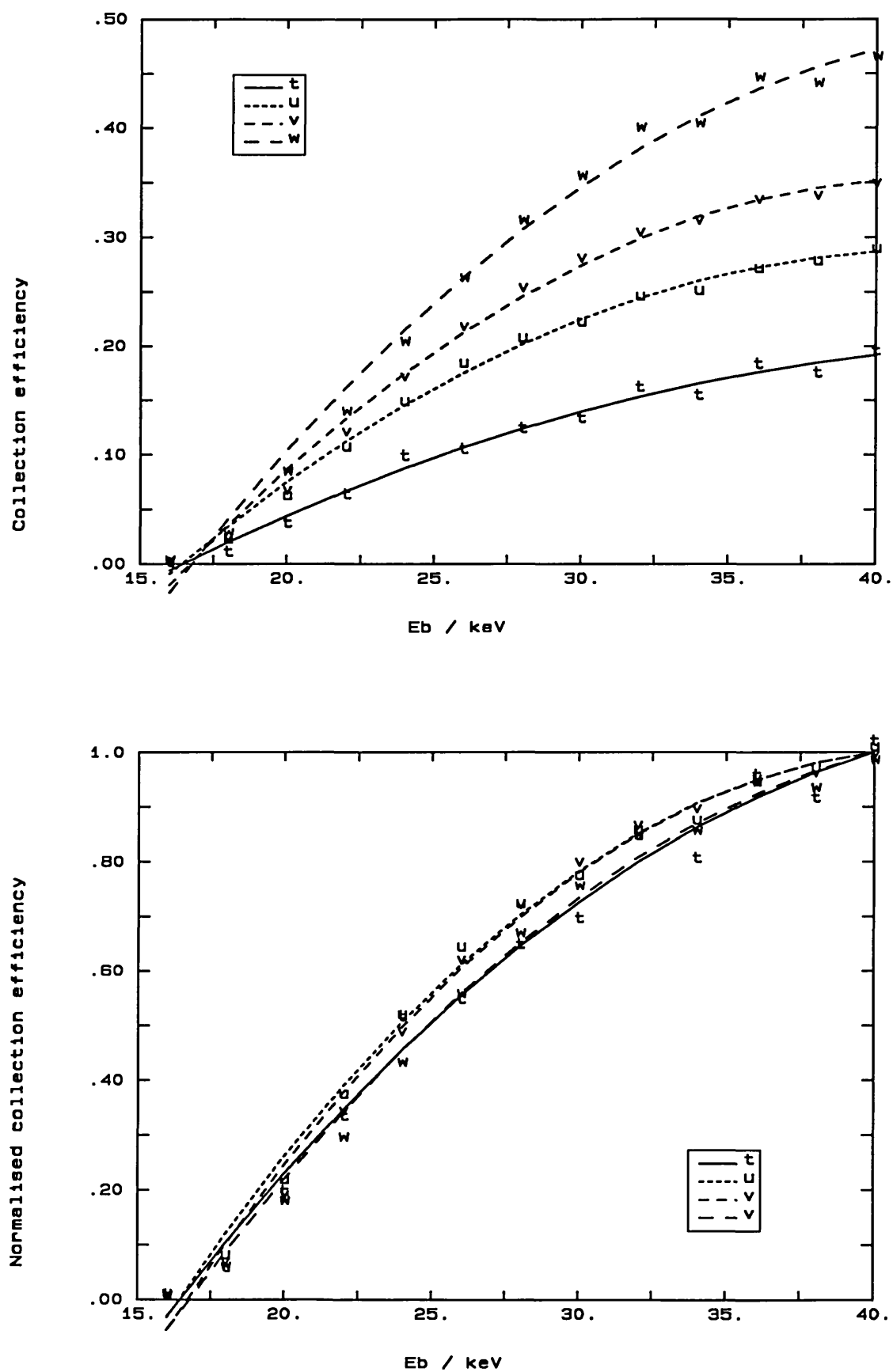
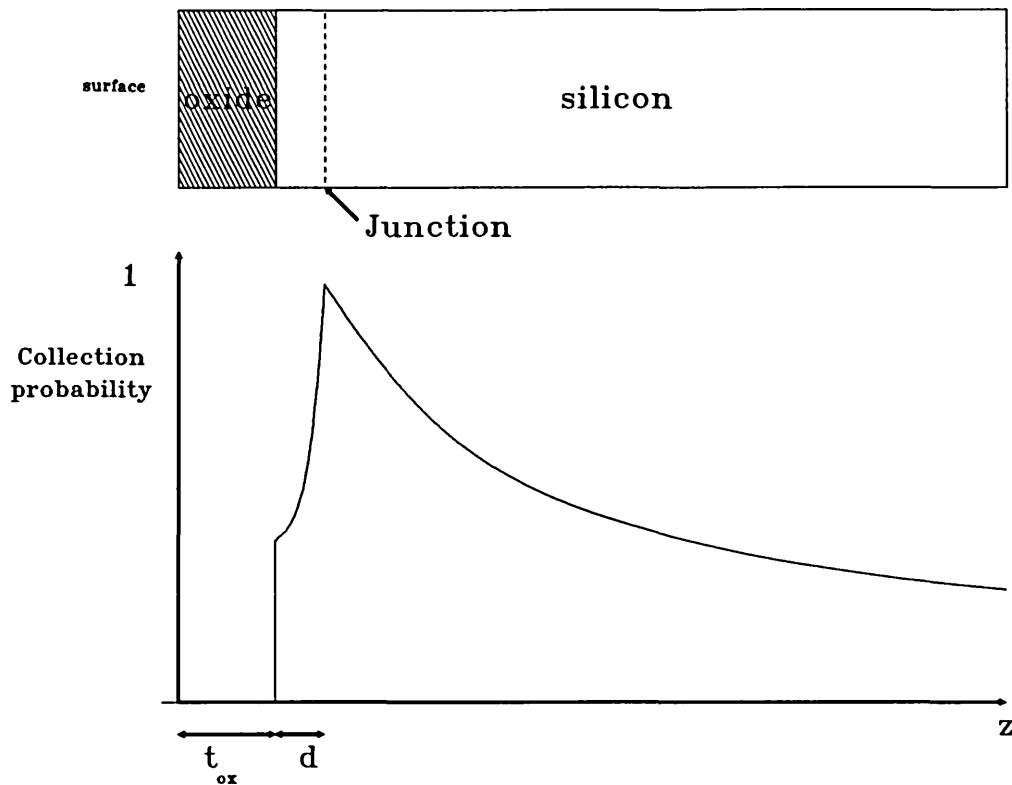


Fig. 105. Variation of η_{cc} with E_b at ESD peaks in deconvolved EBIC linescans.



*Fig. 106. Collection probability model for the diffused resistor.
Top – structure of resistor, with top surface on left.
Bottom – corresponding charge collection probability.*

shown in the figure, the collection probability,

$$\varphi(z) = 0 \quad : z < d_r \quad (68)$$

$$= (1-f) \frac{\cosh [(z-d_r)/L_p] + sL_p \sinh [(z-d_r)/L_p]}{\cosh (d/L_p) + sL_p \sinh (d/L_p)} \quad : d_r \leq z < (d_r + d)$$

$$= (1-f) \exp - [z - (d_r + d)] / L_n \quad : z > d_r + d$$

where L_n, L_p = minority carrier diffusion length for electrons/holes,
 s = reduced surface recombination velocity, v_s/D ,
 d_r = oxide thickness,
 d = junction depth,
 f = fraction of carriers lost in the junction.

The first equation simply expresses the fact that carriers generated in the oxide are relatively immobile. The second expression (Donolato, 1981) is similar in form to the exponential of the third expression for $\varphi(z)$, except that it also takes account of surface recombination at the Si-SiO₂ interface. An Asyst program was written to calculate $\varphi(z)$ according to this model. $g(z, E_b)$ was calculated from the Everhart-Hoff depth-dose function (equation 2), and then η_{cc} was calculated by integrating the product (equation 12) numerically over 200 points. In $\eta_{cc}(E_b, L_p L_n, s, t_{ox}, f, d)$ the variation with E_b was measured experimentally, and the other variables were treated as parameters. After choosing sensible values of each, they could be refined using an asyst function, CURVE.FIT.

Fig. 107 shows the experimental data and the theoretical curve, showing a good fit. It might be argued that so many fitting parameters make some sort of fit inevitable. While this is true to an extent, it should be noted that the final values of the fit parameters, $1-f = 0.99$, $d_r = 1.57 \mu\text{m}$ and $d \approx 0.39 \mu\text{m}$ are not unreasonable. Also, reproducibility between all four scans was good. However, as a means of determining these parameters, it is most likely subject to significant errors. η_{cc} was so insensitive to L_p and s for example, that the curve of η_{cc} vs E_b was equally well fitted by representing $\varphi(z)$ by a straight line between 0 at the Si-SiO₂ interface and 1 at the junction (cf Fig. 106). The small value of L_n corresponds to a doping density of $\sim 10^{17} - 10^{18} \text{ cm}^{-3}$ (Hungerford, 1989, p22). This is far too high for substrate material (cf 1.2×10^{15} for the substrate of the MOSFET test specimens). This indicates the major limitation of this 1D model, which is that the resistor is tacitly assumed to be infinitely wide for Donolato's results to apply. This is not the case, and so a smaller L is necessary to compensate. Improving the model would necessitate a considerably more complex 2D theory for which solutions do not exist at present.

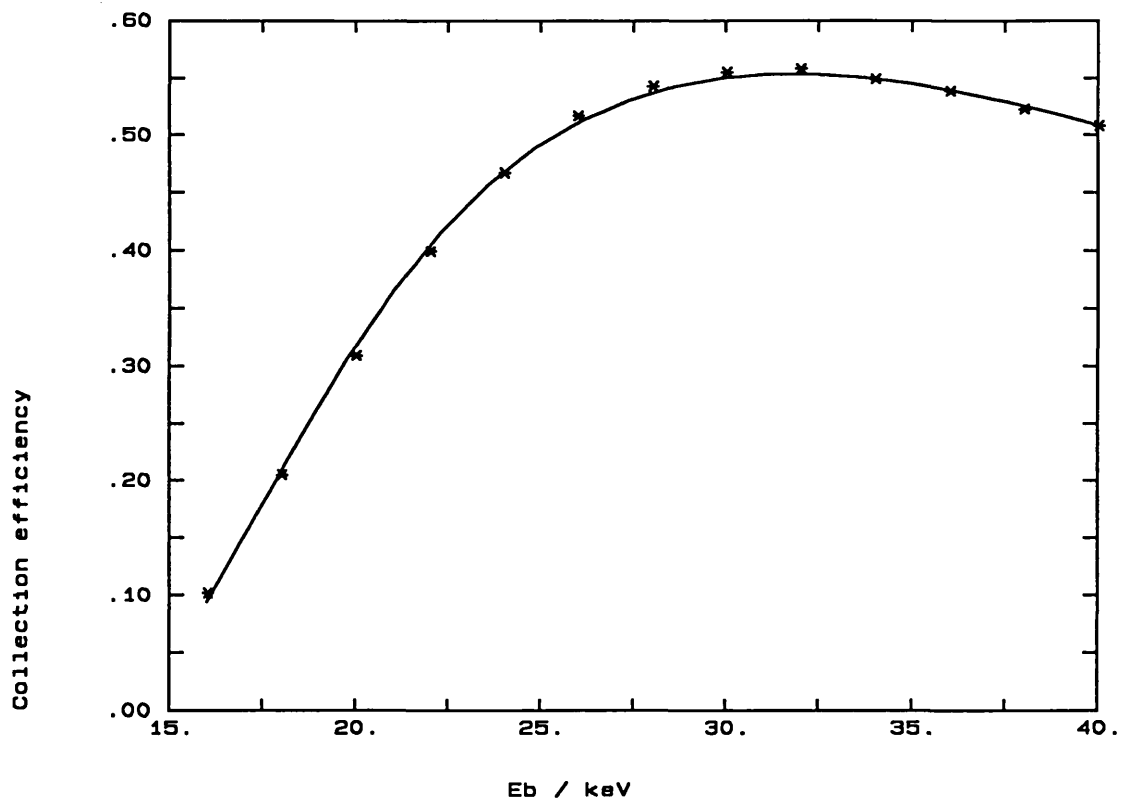


Fig. 107. Results of curve fitting (solid line) compared to experimental data (*), for scan V. Fitting parameters were:

Scan	$L_n/\mu\text{m}$	$L_p/\mu\text{m}$	s	$d_r/\mu\text{m}$	$d/\mu\text{m}$	$1-f$
T	5.47	0.788	1.00	1.57	0.360	0.997
U	5.47	0.787	1.00	1.57	0.397	0.998
V	5.46	0.786	1.00	1.57	0.396	0.999
W	5.48	0.783	1.00	1.57	0.452	1.005

The other source of inaccuracy assuming the line profile smearing is due only to the averaged lateral dose function. The lateral dose of a slice at depth z will vary to some extent with z . Here, the average lateral dose was used for deconvolution. This is a useful simplifying assumption, and improves the resolution of linescans. Application of the same method in an image processor would have a similar result, improving the generally poor quality of high E_b images of small geometry IC's.

5 CONCLUSIONS

5.1 Irradiation damage

Electron beam irradiation damage of MOS test transistors has been studied in detail. Large doses caused a decrease in channel mobility and an increase in drain leakage current. The shift in threshold voltage, ΔV_t was dominant at lower doses and was separated into two contributions:

- (i) ΔV_{ot} due to positive charge trapped in the oxide, especially near the Si-SiO₂ interface. Primary electrons generate electron-hole pairs, and holes have much smaller mobility than electrons. Holes thus become trapped (~5.6% of them in the p-channel transistors studied).
- (ii) ΔV_{it} due to an increase in Si-SiO₂ interface state density, probably caused by breaking of strained bonds in the interface layer.

ΔV_{ot} was nine times larger than ΔV_{it} for the p-channel transistors, and showed no systematic variation with E_b . The change in mobility agrees with a Coulombic scattering model due to increased interface charge.

Plots of ΔV_t vs dose were linear at small doses, and the gradient is proportional to the energy absorbed in the gate oxide. The variation of this energy with E_b was compared with that calculated from the Everhart-Hoff model and Monte Carlo simulations. Above 9keV agreement was good. Between 6 and 9 keV there was an anomalously deep penetration of electrons, indicating that the above calculations may be imprecise in their modelling of the tail of the depth-dose curve. A step at 6 keV and below

is attributable to penetration of secondary X-rays. A threshold shift at $E_b = 0.4$ keV (below Si and O characteristic X-ray ionisation energies) and the smooth variation of damage with E_b in this range indicates that the Bremsstrahlung is dominant.

The two regimes of electron and X-ray damage are clearly visible in the experimental results.

There is no safe E_b that causes no irradiation damage, but 1 keV examination induces six orders of magnitude less damage than higher E_b at which electrons penetrate. Low E_b examination is approximately non-destructive for normal observation times. At high E_b , it has been shown that EBIC images can be obtained by careful dose limitation.

5.2 Image processing

The feasibility of image processing for rapid defect location in VLSI circuits has been systematically explored. The problem of limited resolution and circuit coverage due to finite memory resources has been addressed. Solutions to this, and effective methods for defect location have been developed by programming a commercial image processor in a number of ways:

A fully automatic algorithm for spatially filtering images of periodic and quasi-periodic IC's to locate defects has been developed. It is based on setting a threshold in the Fourier power spectrum. This defines a mask of the spatial frequencies to be removed before reverse transformation. The mask is improved by dilating the de-selected regions, and retaining the

zero-frequency point enables both bright and dark defects to be located. The method was fully investigated, and acted robustly on many input images, locating a wide range of manufacturing defects.

A specialised method for aligning EBIC images of identical pad-driver circuits to locate ESD defects was developed and successfully employed. It was also found to be a sensitive check on misalignments between the processed layers of the chip.

For irregular circuits defect location was less successful by either spatial filtering or direct convolutions. Only comparison techniques worked satisfactorily in giving readily interpretable images.

To examine a complete VLSI circuit requires acquisition of many images for adequate resolution. Software macros were written allowing a matrix of up to 64 adjacent images to be acquired at one stage position. These images could then be processed automatically. To facilitate subsequent relocation and examination of defects it was essential to calculate their position relative to fiducal points on the circuit itself. These were calculated from

- (i) the defect position within an image,
- (ii) the scan position within the matrix of images,
- (iii) the stage coordinates.

In addition, this coordinate system made alignment of golden and test chips possible within the stage accuracy. A simple interactive alignment adjustment then enabled defect location by subtraction.

5.3 EBIC contrast

A computer program was written to rapidly acquire fully calibrated linescans using a Matelect EBIC amplifier. Such scans allow analyses which were impractical with manually recorded data.

In studying subtle ESD defects, EBIC gives more information than light microscopy or the SE mode. Detailed analysis of EBIC images and linescans in favourable cases gives important information concerning failure mechanisms. Three types of EBIC contrast due to ESD have been observed:

- (i) junction breakdown, causing bright contrast due to reduced series impedance,
- (ii) electrothermomigration of aluminium causing extended p-type regions, and bright contrast,
- (iii) Dark contrast due to locally reduced minority carrier lifetime, attributed to silicon dielectric breakdown and Joule heating.

Lateral dose functions in silicon under a passivation layer were determined from Monte Carlo simulations. A correction for the passivation oxide layer was made by estimating the thickness from the variation of charging with E_b . This was sufficiently accurate to allow deconvolution of EBIC linescans to correct for smearing due to beam spreading, giving an apparent resolution increase.

6 FURTHER WORK

On irradiation damage, modelling of the energy dissipated in the gate oxide due to Bremsstrahlung should be investigated further. A full Monte Carlo simulation of continuum X-rays and its absorption in the gate oxide should be carried out.

The quantitative EBIC analysis of device structures should be followed up in association with other techniques such as cross-sectioning and etching or TEM, to determine device structures and check the validity of simulations.

Two practical difficulties in defect location are now surmountable due to options finally available from Kontron. The first is to motorise the specimen stage under computer control, to avoid the tedious, manual entry of stage coordinates. The second is an automatic image alignment algorithm. Once written, it could be substituted directly into the Compare16 macro of section 4.2.5.

The masking algorithm for spatial filtering can be calculated very quickly, but the FFT limits overall speed. By using dedicated FFT hardware, the spatial filtering algorithms could be used to display real-time defect images.

Longer term studies must be directed towards defect identification, because it will be necessary for the computer to determine which inhomogeneities are defects automatically, thus replacing interactive defect identification procedures by fully computerised alternatives.

APPENDIX 1Matelect Data File Header Example

```

Version      4.23
comment      Linescan across centre of ESD defect and diffused resistor
Scantype     Head Amplifier
SEMControls  SLOW2, LINE, YZ-MOD, HOR6
Mag          1000
SpotVel      2.77566666666623E-0001
ScanTime     4.80000000000018E-0001
Rate         1.06666666666605E+0003
DistPerPoint 2.62155562499086E-0007
Eb           2.00000000000000E+0001
BackOff      -1.89999999999912E-0006
DarkCurrent  -1.892700000000054E-0006
BiasVolts    0.00000000000000E+0000
Ib           -1.996000000000004E-0009
I-Range      1.99999999999853E-0006
n-points     512
-1.8823E-6
-1.8823E-6
-1.8940E-6
..... more points

```

APPENDIX 2Asyst Program to Read Matelect Data Files

```

\ DEFINITION OF VARIABLES
20  string filename
token data token x
real  scalar version
80    string comment
80    string ScanType
80    string SEMControls
real  scalar Mag
      scalar DistAtX1
      scalar ScanTime
      scalar Rate
      scalar DistPerPoint
      scalar Eb
      scalar Backoff
      scalar DarkCurrent
      scalar BiasVolts
      scalar Ib
      scalar I-range
integer scalar n-points
real dim[ 13 ] array info

: matread.JAM      \ (fileroot --- t/f )
\ READS AN ASYST FORMAT FILE
?file.open if file.close then
" .JAM" "cat
defer>
file.open
1 comment> comment      ":-
2 comment> ScanType     ":-
3 comment> SEMControls  ":-
1 subfile file>unnamed.array becomes> data
2 subfile info file>array
file.close
true                                     \ .JAM found, so return TRUE

ONERR:
?drop                                  \ fix for Asyst bug
?error# dup 560 =                      \ check if file not found
IF
drop false                            \ .JAM NOT FOUND so return FAL
SE
ELSE
." ERROR! in matread.JAM"
error
THEN
;

: matread.MAT      \ ( fileroot --- )
\ READS A MATELECT FORMAT FILE
"text.file "swap                      \ save old default for editing
" .MAT" "cat defer> basic.open
defer> text.file                      \ restore default

```

```

basic.read drop info [ 1 ] :=          \ first part of info
"basic.read comment      " :=
"basic.read Scantype      " :=
"basic.read SEMControls   " :=
14 2
DO
  basic.read drop info [ i ] :=        \ rest of info
LOOP

\ generate data array
info []size swap [ ? ]                \ last element of info= n-poi
nts
dup                                    \ save n-points for
loop
  ramp float becomes> data
  1 + 1                                \ 1 to n-points
DO
  basic.read drop
  data [ i ] :=                        \ get entry and delete number
LOOP
basic.close
;

: matwrite.JAM \ ( fileroot --- )
\ WRITES SCAN DATA INTO AN ASYST FORMAT FILE FOR FAST LOADING
file.template
  3 comments
  data []form.subfile
  info []form.subfile
end
?file.open if file.close then
" .JAM" "cat
"dup defer> file.create defer> file.open
comment      1 >comment
Scantype      2 >comment
SEMControls 3 >comment
1 subfile data array>file
2 subfile info array>file
file.close
;
: header
\ PRINTS HEADER INFORMATION
\ any of these variables can be called within Asyst for calculations
CR comment      "type
CR Scantype      "type
CR SEMControls   "type
CR Version       ." Version      " .
CR Mag           ." Mag          " .
CR DistAtX1      ." DistAtX1     " .
CR ScanTime      ." ScanTime     " .
CR Rate          ." Rate         " .
CR DistPerPoint  ." DistPerPoint " .
CR Eb            ." Eb           " .
CR BackOff       ." BackOff      " .
CR DarkCurrent   ." DarkCurrent  " .
CR BiasVolts     ." BiasVolts    " .
CR Ib            ." Ib           " .
CR I-Range       ." I-Range      " .

```



```

CR n-points      ." n-points      " .
;

: matread.      \ ( fileroot --- )
\ MAIN LOADING ROUTINE
\ FIRST TRIES TO LOAD AN ASYST FORMAT FILE
\ IF NONE EXISTS, READS MATELECT (ASCII) FILE, THEN WRITES AN ASYST FILE
"dup matread.JAM      \ try for JAM file
IF
  "drop
  CR ." Loaded .JAM file"
ELSE
  "dup matread.MAT
  CR ." Loaded .MAT file"
  matwrite.JAM
  CR ." Written .JAM file"
THEN
info [ 1 ] Version      :=
info [ 2 ] Mag          :=
info [ 3 ] DistAtX1     :=
info [ 4 ] ScanTime     :=
info [ 5 ] Rate         :=
info [ 6 ] DistPerPoint :=
info [ 7 ] Eb           :=
info [ 8 ] BackOff      :=
info [ 9 ] DarkCurrent  :=
info [ 10 ] BiasVolts   :=
info [ 11 ] Ib          :=
info [ 12 ] I-Range     :=
info [ 13 ] n-points    :=
;

: matread
\ INTERACTIVE LOADING ROUTINE
CR .dir
CR ." Enter filename without extension:" "input
matread. \ main routine
header
;

: x \ ARRAY OF X DATA
n-points ramp 1 - DistPerPoint *
;

: Isc \ ARRAY OF TRUE Isc VALUES
data BackOff -
;

: look
\ PLOTS DATA AUTOMATICALLY AND ALLOWS INTERACTIVE DATA READING
x Isc xy.auto.plot
normal.coords
" Isc (A)" y$.
" Distance (um)" x$.
.5 .975 readout>position
world.coords
array.readout
;

```

APPENDIX 3

```

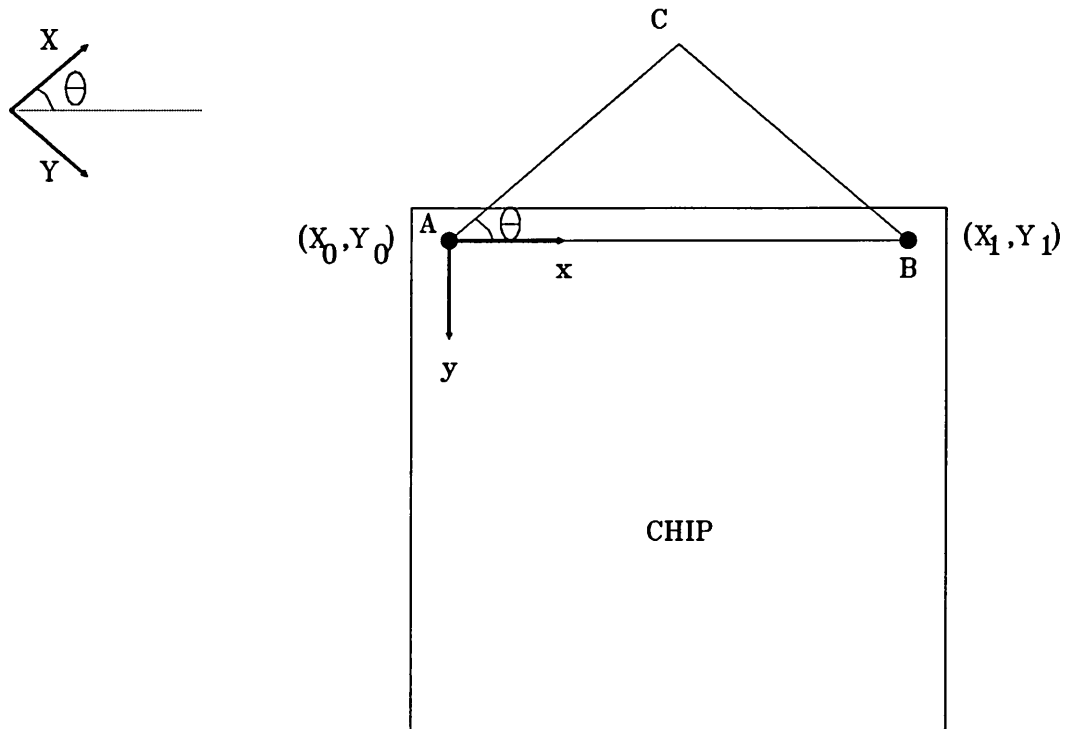
macro spfilter (in=1, out=2, aux1=27, aux2=28, norm=—ON, thresh=—ON,
dilate=—ON, cross=1, med=—ON)
# Macro to spatial filter an image

# normalisation?
display out
if norm
  write "Normalising"
  normim in,out,1
else
  copy in,out
endif
# FFT
display aux1
fft out,aux1,aux2
clear out
clovl out
display out
# thresholded spatial filtering?
if thresh
  write "Thresholded spatial filtering"
  fftdis aux1,aux2,out
  shift out,out,0,1 # fix for bug in Kontron FFT 21/10
  discr out,out,0,50,—ON
endif
# dilated spatial filtering?
if dilate
  write "Dilating the mask"
  dilate out,out,7,0,1 # octagonal structuring element
endif
# X-Y spatial filtering?
if cross>1
  write "X-Y spatial filtering"
  for i=0,( i<(cross-1) ),i=i+1
    Grectg out,0,256-i,512,i*2,-1,0
    Grectg out,256-i,0,i*2,512,-1,0
  endfor
endif
# reverse transform
ovlgrey out,out,out,0 # Combine masks
clovl out
GWpixel out,256,256,255 # keep zero order
fftmask out,aux1,aux2
fftinv aux1,aux2,out
# Median filter?
if median
  write "Median filtered"
  copy out,aux1
  median3 aux1,out
endif
endmacro

```

APPENDIX 4

Derivation of Equation (62)



Transformation of specimen stage coordinates (X, Y) into circuit coordinates, (x, y) given two fiducial points, (X_0, Y_0) and (X_1, Y_1) can be done as follows:

The angle between the coordinate systems, θ , is given by

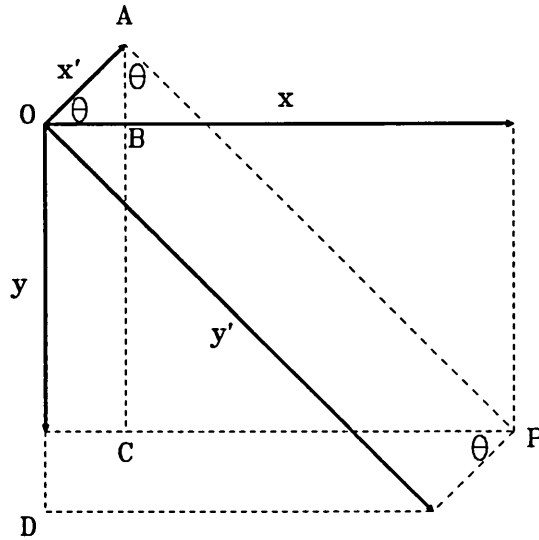
$$\tan \theta = \frac{CB}{AC} = \frac{Y_1 - Y_0}{X_1 - X_0}$$

To simplify the calculation, translate (X, Y) to a system (x', y') which has an origin co-incident with (x, y) . Thus,

$$x' = X - X_0$$

$$y' = Y - Y_0$$

The new coordinates are then as shown below:



thus,

$$\begin{aligned} x &= OB + CP \\ &= x' \cos \theta + y' \sin \theta \end{aligned}$$

$$\begin{aligned} y &= -AB + OD \\ &= -x' \sin \theta + y' \cos \theta \end{aligned}$$

$\therefore$ expressing the result in matrix form, and resubstituting for (x', y') ,

$$\begin{bmatrix} x \\ y \end{bmatrix} = \begin{bmatrix} \cos \theta & \sin \theta \\ -\sin \theta & \cos \theta \end{bmatrix} \begin{bmatrix} X - X_0 \\ Y - Y_0 \end{bmatrix}$$

$$\text{where } \theta = \tan^{-1} \left[\frac{Y_1 - Y_0}{X_1 - X_0} \right]$$

also, on multiplying by the reciprocal matrix, the reverse transformation is

obtained:

$$\begin{bmatrix} X-X_0 \\ Y-Y_0 \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} x \\ y \end{bmatrix}$$

APPENDIX 5

Relocate Macro Example Output

```
*****
***** Relocate *****
*****
```

```
DBfile: test
Defects found during scan at:
Stage coords (um): xs=26687 ys=33349
Circuit coords (um): xc=-3591 yc=1636
Magnification X50
```

```
Circt coord Stage coord
xc/um yc/um xs/um ys/um comment
-4405 1247 25995 32770 scratch
-3428 1507 26877 33264 metal defect
-3308 1837 26911 33614 large dust
-4296 2334 25831 33849 bond-pad scuff
-3285 2351 26806 34117 small dust
-3495 2124 26659 33845 particulate
-3014 2032 27147 33875 bond-pad mark
=====
```

Macros for Multiple Image Defect Searching

```
macro Initialise (SEM=ON)
  makeim "big",0,0,2048,2048,2048,2048
  makeim "matrix",0,0,2048,2048,512,512
  if SEM : jsemini
endmacro

macro StageInit (DBfile="j")
# initialises stage coordinates and stores them
for i=1,i<7,i=i+1 : write
  fwrite "prn","*****"
  fwrite "prn","***** StageInit *****"
  fwrite "prn","*****"
  fwrite "prn"
  fwrite "prn","DBfile: ",DBfile
  write "Initialising stage"
  write "===== "
  write
  write "1. Select SEM1"
  beep 100,200
  display 1
  clovl 1
# draw cross-hairs
setframe "F256"
Gvector 1,128,0,128,256,-1
```

```

Gvector 1,0,128,256,128,-1
write
write "2. Locate 1st fiducal point roughly with stage"
write "    at high magnification (X2,000)",esc
semlut 1,0,-ON,"lut-file.lin" # lut for 256x256 images
sempar 1,1,1
semonl 1,0,-ON
write " ... now locate fiducal point accurately",esc
setframe "F512"
clovl 2
display 2
Gvector 2,256,0,256,512,-1
Gvector 2,0,256,512,256,-1
sempar 1,1,2,0,0,0,0
semlut 2,0,-ON,"lut-file.lin"
semonl 2,0,-ON
# enter stage co-ords once located
x0=y0=0.0
while (x0==0) : read "Enter stage co-ordinates (mm): x0=",x0," y0=",y0
x0=x0*1e3 # convert to um
y0=y0*1e3
c0=""
while c0=="": read "Fiducal description:",c0
write
write "3. Locate 2nd fiducal point roughly with stage"
write "    and parallel to x-axis of chip",esc
setframe "F256"
display 1
semlut 1,0,-ON,"lut-file.lin"
sempar 1,1,1,0,0,0,0
semonl 1,0,-ON
write " ... now locate fiducal point accurately",esc
setframe "F512"
display 2
semlut 2,0,-ON,"lut-file.lin"
sempar 1,1,2,0,0,0,0
semonl 2,0,-ON
x1=y1=0.0
while (x1==0) : read "Enter stage co-ordinates (mm): x1=",x1," y1=",y1
x1=x1*1e3 # convert to um
y1=y1*1e3
c1=""
while c1=="": read "Fiducal description:",c1
# store variables in database file, DBfile
DBerase DBfile
global X,Y,C
X=Y=0.0
C="1234567890123456789012345678901234567890123445678901234"
coord[]=X,Y,C
DBcreate DBfile,"coord"
X=x0
Y=y0
C=c0
DBappend DBfile
X=x1
Y=y1
C=c1
DBappend DBfile

```

```

DBclose DBfile
# print report
fwrite "PRN","Initialised stage coordinates (um):"
fwrite "PRN","x0=",int(x0)," y0=",int(y0)," ",c0
fwrite "PRN","x1=",int(x1)," y1=",int(y1)," ",c1
fwrite "prn","_____ "
formfeed
endmacro

macro Scan (PixInt=50,DBfile="j",ImFile="tempim1")
  DistX1=166.7 # um per pixel (= 6 pixels per mm )
# initialises xc and yc : rel. positions of scan centre
# also stores magnification
clearallof
clearall
for i=1,i<7,i=i+1 : write
fwrite "prn","*****"
fwrite "prn","***** Scan *****"
fwrite "prn","*****"
fwrite "prn"
fwrite "prn","DBfile: ",DBfile
fwrite "prn","Imfile: ",ImFile
write "Scanning matrix of 4X4 images"
write "===== "
write
write "1. Adjust microscope for resolution",esc
write "    ... and ensure scan is not rotated"
display 1
semwindow 1,-ON,192,192,128,128,-OFF,-ON
sempar 1,1,1
semonl 1,0,-ON
mag=0
while (mag==0) : read "Magnification: ",mag
write "-> Resolution=",DistX1/mag/4,"um"
write
write "2. Move stage to the region of interest",esc
semwindow 1,-ON,0,0,512,512,-OFF,-OFF
semonl 1,0,-ON
sempar 1,1,PixInt,0,0,0,0
write
write "3. Now adjust image contrast",esc
semwindow 1,-ON,192,192,128,128,-OFF,-ON
semonl 1,0,-ON
xs=ys=0.0
while xs==0 : read "Enter stage co-ordinates (mm): xs=",xs," ys=",ys
xs=xs*1e3
ys=ys*1e3
fwrite "PRN","Stage coords (um):    xs=",int(xs)," ys=",int(ys)
cs=""
while cs=="" : read "Scan description: ",cs
# store mag and xc,yc in DB file
DBopen DBfile,"coord"
DBread DBfile
x0=X
y0=Y
DBread DBfile
x1=X
y1=Y

```



```

X=DistX1
Y=mag
C="DistX1 and mag"
DBwrite DBfile
theta=atan((y1-y0)/(x1-x0))
xc=(xs-x0)*cos(theta) + (ys-y0)*sin(theta)
yc=(ys-y0)*cos(theta) - (xs-x0)*sin(theta)
X=xc
Y=yc
C=cs
DBwrite DBfile
DBclose DBfile
fwrite "PRN","Circuit coords (um): xc=",int(xc)," yc=",int(yc)
fwrite "PRN","Magnification X",mag
write "scanning ..."
display "big[1]"
semlut "big[1]",0,—ON,0,"bigscan.lut"
semscan "big[1]",0,—ON
while (—STATUS!=0) # timeout in transfer or other error
    write "Kontron SEM error No:",—STATUS," during scan ... trying again"
    jsemini —ON
    semlut "big[1]",0,—ON,0,"bigscan.lut"
    semscan "big[1]",0,—ON
endwhile
fwrite "prn","===== "
formfeed
setframe "F512"
clovl 1
write "Storing original images ..."
storeseq ImFile,"matrix",1,16,1
endmacro

macro GetOrgImg (filename="tempim1")
    getseq filename,"matrix",1,1,16,1
endmacro

macro Spfilt16 (norm=—ON,thresh=—ON,cross=1,med=—ON)
    # macro to spatially filter 16 images acquired by macro sixteen
    setframe "matrix"
    for i=1,i<7,i=i+1 : write
    write "Spatially filtering the 16 images"
    for i=1,i<17,i=i+1
        write "image = ",i
    # set arguments
    in=i
    out="F512[26]"
    aux1="F512[27]"
    aux2="F512[28]"
    display out
    if norm
        write "Normalising"
        normim in,out,1
    else
        copy in,out
    endif
    # FFT
    display aux1
    fft out,aux1,aux2

```

```

clear out
clovl out
display out
if thresh
  write "Thresholded spatial filtering"
  fftdis aux1,aux2,out
  shift out,out,0,1 # fix for bug in Kontron FFT 21/10
  discr out,out,0,50,-ON
endif
if cross>1
  write "X-Y spatial filtering"
  for i=0,( i<(cross-1) ),i=i+1
    Grectg out,0,256-i,512,i*2,-1,0
    Grectg out,256-i,0,i*2,512,-1,0
  endfor
endif
# reverse transform
ovlgrey out,out,out,0          # Combine masks
clovl out
CWpixel out,256,256,255        # keep zero order
fftmsk out,aux1,aux2
fftinv aux1,aux2,out
# Median filter?
if median
  write "Median filtered"
  copy out,aux1
  median3 aux1,out
endif
# end of macro spfilter
  copy out,i
endfor
write "Storing the processed images ... "
storeseq "tempim2","matrix",1,16,1
setframe "F512"
endmacro

macro GetProcImg (filename="tempim2")
  setframe "matrix"
  getseq filename,"matrix",1,1,16,1
  setframe "F512"
endmacro

macro View(DBfile="j")
  # first get scan position info from DB
  for i=1,i<7,i=i+1 : write
    DBopen DBfile,"coord"
    DBread DBfile      # 1st fiducal point
    x0=X
    y0=Y
    DBread DBfile      # 2nd fiducal point
    x1=X
    y1=Y
    theta = atan ( (y1-y0)/(x1-x0) )
    DBread DBfile      # scaling , mag
    DistX1=X
    mag=int(Y)
    DBread DBfile
    xc=X

```

```

yc=Y
cc=C
xs=xc*cos(theta)-yc*sin(theta)+x0
ys=xc*sin(theta)+yc*cos(theta)+y0
write "xc=",xc," yc=",yc
write "xs=",xs," ys=",ys
fwrite "prn","*****"
fwrite "prn","***** View *****"
fwrite "prn","*****"
fwrite "prn"
fwrite "prn","DBfile: ",DBfile
fwrite "prn","Defects found during scan at:"
fwrite "prn","Stage coords (um):  xs=",int(xs),"  ys=",int(ys)
fwrite "prn","Circuit coords (um): xc=",int(xc),"  yc=",int(yc)
fwrite "prn","Magnification X",mag
fwrite "prn"
fwrite "prn","Circ coord Stage coord"
fwrite "prn","xc/um yc/um xs/um ys/um  comment"
setframe "matrix"
m= "F768[5]"
clovl m
display m
# Set up menu
for i=0,i<170,i=i+40 : Grectg m,520,i,200,40,-1,0
Gstring m,530,10,"Next Image",-1,1,0
Gstring m,530,50,"Defect",-1,1,0
Gstring m,530,90,"Compare",-1,1,0
Gstring m,530,130,"Quit",-1,1,0
clovl "F768[6]"
copyimovl m,"F768[6]"
for im=1,im<17,im=im+1
  copy im,"F512[5]"
  i=int((im-1)/4-0.5)+1      # co-ords of
  j=im-(i-1)*4              # image in block
  # input from menu
  while 1
    Gcursori m,x,y,1
    if y<40 : break          # NEXT
    if ((y>=40)and(y<80))   # DEFECT
      write "Select defect with digitiser"
      Gcursori m,k,l
      comstr=""
      read "comment:",comstr
      # calculate circuit coords of defect rel. to fiducal pt
      #      - sign below is due to left-handed stage axes
      xcD=xc - DistX1/mag*((i-3)*512+k)/4
      ycD=yc + DistX1/mag*((j-3)*512+l)/4
      xsD=xcD*cos(theta)-ycD*sin(theta)+x0
      ysD=xcD*sin(theta)+ycD*cos(theta)+y0
      fwrite "PRN",int(xcD)," ",int(ycD)," ",int(xsD)," ",int(ysD)," ",
comstr
      X=xcD
      Y=ycD
      C=comstr
      DBwrite
      continue # restart loop
    endif
    if ((y>=80)and(y<120)) # COMPARE

```

```

        getseq "tempim1","F512",im,6,1,1
        setframe "F512"
        review 5,2,0,15,-OFF
        display "F768[5]"
        setframe "matrix"
        continue # restart loop
    endif
    if ((y>=120)and(y<160))
        im=17 # exit for loop
        break
    endif
endwhile
endfor
fwrite "prn","-----"
formfeed
DBclose DBfile
endmacro

macro Relocate (DBfile="j")
# outputs a list of defects and their stage coordinates
# if the stage has been reinitialised
for i=1,i<7,i=i+1 : write
    DBopen DBfile,"coord"
    DBread DBfile      # 1st fiducal point
    x0=X
    y0=Y
    DBread DBfile      # 2nd fiducal point
    x1=X
    y1=Y
    theta = atan ( (y1-y0)/(x1-x0) )
    DBread DBfile      # scaling , mag
    DistX1=X
    mag=int(Y)
    DBread DBfile
    xc=X
    yc=Y
    cc=C
    xs=xc*cos(theta)-yc*sin(theta)+x0
    ys=xc*sin(theta)+yc*cos(theta)+y0
write "xc=",xc," yc=",yc
write "xs=",xs," ys=",ys
    fwrite "prn","*****"
    fwrite "prn","***** Relocate *****"
    fwrite "prn","*****"
    fwrite "prn"
    fwrite "prn","DBfile: ",DBfile
    fwrite "prn","Defects found during scan at:"
    fwrite "prn","Stage coords (um):  xs=",int(xs),"  ys=",int(ys)
    fwrite "prn","Circuit coords (um): xc=",int(xc),"  yc=",int(yc)
    fwrite "prn","Magnification X",mag
    fwrite "prn"
    fwrite "prn","Circ coord Stage coord"
    fwrite "prn","xc/um yc/um xs/um ys/um  comment"
while 1
    DBread DBfile
    if -STATUS : break  #eof
    xcD=X

```

```

        ycD=Y
        xsD=xcD*cos(theta)-ycD*sin(theta)+x0
        ysD=xcD*sin(theta)+ycD*cos(theta)+y0
        fwrite "prn",int(xcD)," ",int(ycD)," ",int(xsD)," ",int(ysD)," ",C
    endwhile
    fwrite "prn","-----"
    formfeed
    DBclose DBfile
endmacro

# macros to allow comparisons of 16 frames
# acquired using macros above
# ref.img      = reference image file
# tempim1.img = test images
# tempim2.img = subtracted images

macro ReInitStage (DBfile="j")
    esc=", ... press <ESC>"
    write
    write "CHECKING IF SEMINI HAS BEEN DONE ..."
    sempar 1,1,1,0,0,0,0
    if -STATUS=-3015 # check for semini
        write " ... Initialising"
        jsemini
        sempar 1,1,1
    else
        write " ... OK"
    endif
    for i=1,i<7,i=i+1 : write
    fwrite "prn","*****"
    fwrite "prn","***** ReInitStage *****"
    fwrite "prn","*****"
    fwrite "prn"
    fwrite "prn","DBfile: ",DBfile
    write "Re-Initialising stage"
    write "===== "
    write
    write "1. Select SEM1"
    display 1
    clovl 1
    # draw cross-hairs
    setframe "F256"
    Gvector 1,128,0,128,256,-1
    Gvector 1,0,128,256,128,-1
    write
    DBopen DBfile,"coord[]"
    DBread DBfile
    c0=C
    write "2. Locate **",c0,"** roughly with stage"
    write " at high magnification (X2,000)",esc
    semlut 1,0,-ON,"lut-file.lin" # lut for 256x256 images
    semonl 1,0,-ON
    write " ... now locate fiducal point accurately",esc
    setframe "F512"
    clovl 2
    display 2
    Gvector 2,256,0,256,512,-1
    Gvector 2,0,256,512,256,-1

```

```

sempar 1,1,2,0,0,0,0
semlut 2,0,-ON,"lut-file.lin"
semonl 2,0,-ON
# enter stage co-ords once located
x0=y0=0.0
while (x0==0) : read "Enter stage co-ordinates (mm): x0=",x0," y0=",y0
x0=x0*1e3 # convert to um
y0=y0*1e3
X=x0
Y=y0
DBup DBfile
DBwrite DBfile
write
DBread DBfile
c1=C
write "3. Locate **",c1,"** roughly with stage"
write " and parallel to x-axis of chip",esc
setframe "F256"
display 1
semlut 1,0,-ON,"lut-file.lin"
sempar 1,1,1,0,0,0,0
semonl 1,0,-ON
write " ... now locate fiducal point accurately",esc
setframe "F512"
display 2
semlut 2,0,-ON,"lut-file.lin"
sempar 1,1,2,0,0,0,0
semonl 2,0,-ON
x1=y1=0.0
while (x1==0) : read "Enter stage co-ordinates (mm): x1=",x1," y1=",y1
x1=x1*1e3 # convert to um
y1=y1*1e3
X=x1
Y=y1
DBup DBfile
DBwrite DBfile
DBclose DBfile
# print report
fwrite "PRN","Stage Re-initialised:"
fwrite "PRN","x0=",int(x0)," y0=",int(y0)," ",c0
fwrite "PRN","x1=",int(x1)," y1=",int(y1)," ",c1
fwrite "prn","===== "
formfeed
endmacro

macro AlignedScan (PixInt=5,DBfile="j")
# for comparisons
DistXl=166.7 # um per pixel (= 6 pixels per mm )
# initialises xc and yc : rel. positions of scan centre
# also stores magnification
# in DB file
esc=", ... press <ESC>"
write
write "CHECKING IF SEMINI HAS BEEN DONE ..."
sempar 1,1,5,0,0,0,0
if -STATUS=-3015 # check for semini
write " ... Initialising"
jsemini

```

```

    sempar 1,1,1
else
    write " ... OK"
endif
clearallov
clearall
for i=1,i<7,i=i+1 : write
fwrite "prn","*****"
fwrite "prn","***** AlignedScan *****"
fwrite "prn","*****"
fwrite "prn"
fwrite "prn","DBfile: ",DBfile
write "Scanning matrix of 4X4 images"
write "===== "
write
# load DBfile information
DBopen DBfile,"coord[]"
DBread DBfile
x0=X
y0=Y
DBread DBfile
x1=X
y1=Y
DBread DBfile
DistX1=X
mag=Y
DBread DBfile
xc=X
yc=Y
theta=atan((y1-y0)/(x1-x0))
xs= xc*cos(theta) - yc*sin(theta) + x0
ys= xc*sin(theta) + yc*cos(theta) + y0
write "1. Set magnification to X",mag,esc
write " ... and ensure scan is not rotated"
write
write "2. Move stage to position (um):"
write " X=",int(xs)," Y=",int(ys)
write "3. Now Align images:"
getseq "ref","matrix",6,6,2,1
getseq "ref","matrix",10,10,2,1
write "Press <ESC> when finished"
clearallov
display "big[1]"
semwindow "big[1]",-ON,768,768,512,512,-OFF,-OFF
semonl "big[1]",0,-ON
xs=xs/1e3
ys=ys/1e3
read "Enter stage co-ordinates (mm): xs=",xs," ys=",ys
xs=xs*1e3
ys=ys*1e3
cs=C
read "Scan description: ",cs
xc=(xs-x0)*cos(theta) + (ys-y0)*sin(theta)
yc=(ys-y0)*cos(theta) - (xs-x0)*sin(theta)
X=xc
Y=yc
C=cs
DBup DBfile

```

```

DBwrite DBfile
DBclose DBfile
fwrite "PRN","Stage coords (um):  xs=",int(xs)," ys=",int(ys)
fwrite "PRN","Circuit coords (um): xc=",int(xc)," yc=",int(yc)
fwrite "PRN","Magnification X",mag
write "scanning ..."
display "big[1]"
semlut "big[1]",0,-ON,0,"bigscan.lut"
semscan "big[1]",0,-ON
while (-STATUS!=0) # timeout in transfer or other error
    write "Kontron SEM error No:",-STATUS," during scan ... trying again"
    jsemini -ON
    semlut "big[1]",0,-ON,0,"bigscan.lut"
    semscan "big[1]",0,-ON
endwhile
fwrite "prn","-----"
formfeed
write "Storing original images ..."
storeseq "tempim1","matrix",1,16,1
endmacro

macro ViewComp(DBfile="j")
# version of view to allow comparisons as well
# assumes tempim.img is in memory (test images)
# first get scan position info from DB
for i=1,i<7,i=i+1 : write
DBopen DBfile,"coord"
DBread DBfile      # 1st fiducal point
x0=X
y0=Y
DBread DBfile      # 2nd fiducal point
x1=X
y1=Y
theta = atan ( (y1-y0)/(x1-x0) )
DBread DBfile      # scaling , mag
DistX1=X
mag=int(Y)
DBread DBfile
xc=X
yc=Y
cc=C
xs=xc*cos(theta)-yc*sin(theta)+x0
ys=xc*sin(theta)+yc*cos(theta)+y0
write "xc=",xc," yc=",yc
write "xs=",xs," ys=",ys
fwrite "prn","*****"
fwrite "prn","***** ViewComp *****"
fwrite "prn","*****"
fwrite "prn"
fwrite "prn","DBfile: ",DBfile
fwrite "prn","Defects found during scan at:"
fwrite "prn","Stage coords (um):  xs=",int(xs)," ys=",int(ys)
fwrite "prn","Circuit coords (um): xc=",int(xc)," yc=",int(yc)
fwrite "prn","Magnification X",mag
fwrite "prn"
fwrite "prn","Circ coord Stage coord"
fwrite "prn","xc/um yc/um xs/um ys/um  comment"
setframe "matrix"

```



```

m= "F768[5]"
clearallov
clear m
display m
# Set up menu
for i=0,i<170,i=i+40 : Grectg m,515,i,205,40,-1,0
Gstring m,525,10,"Next Image",-1,1,0
Gstring m,525,50,"Defect",-1,1,0
Gstring m,525,90,"Compare",-1,1,0
Gstring m,525,130,"Compare with ref",-1,1,0
Gstring m,525,170,"Quit",-1,1,0
copyimovl m,"F768[6]"
copyimovl m,"F768[7]"
Gstring "F768[7]",530,480,"Reference Image",-1,1,0
Gstring "F768[6]",530,480,"Test Image",-1,1,0
for im=1,im<17,im=im+1
  copy im,"F512[5]"
  i=int((im-1)/4-0.5)+1      # co-ords of
  j=im-(i-1)*4              # image in block
  # input from menu
  while 1
    Gcursori m,x,y,1
    if y<40 : break          # NEXT
    if ((y>=40)and(y<80))   # DEFECT
      write "Select defect with digitiser"
      Gcursori m,k,l
      comstr=""
      read "comment:",comstr
      # calculate circuit coords of defect rel. to fiducal pt
      #      - sign below is due to left-handed stage axes
      xcD=xc - DistX1/mag*((i-3)*512+k)/4
      ycD=yc + DistX1/mag*((j-3)*512+l)/4
      xsD=xcD*cos(theta)-ycD*sin(theta)+x0
      ysD=xcD*sin(theta)+ycD*cos(theta)+y0
      fwrite "PRN",int(xcD)," ",int(ycD)," ",int(xsD)," ",int(ysD)," ",
comstr
      X=XD
      Y=YD
      C=comstr
      DBwrite
      continue # restart loop
    endif
    if ((y>=80)and(y<120)) # COMPARE
      getseq "tempim1","F512",im,6,1,1
      setframe "F512"
      review 5,2,0,15,-OFF
      display "F768[5]"
      setframe "matrix"
      continue # restart loop
    endif
    if ((y>=120)and(y<160)) # COMPARE WITH REF
      getseq "tempim1","F512",im,6,1,1
      getseq "ref","F512",im,7,1,1
      setframe "F512"
      review 5,3,0,15,-OFF
      display "F768[5]"
      setframe "matrix"
      continue # restart loop

```

```
endif
if ((y>=160)and(y<200))
    im=17 # exit for loop
    break
endif
endwhile
endfor
fwrite "prn","-----"
formfeed
DBclose DBfile
endmacro
```

APPENDIX 6

Macros to Search Circuit Inputs/Outputs for ESD Damage

```
macro Getref (SE-ref=27,CC-ref=28)
# Macro to input a reference SE image for alignment
# of the CC images
  clovl SE-ref
  for i=1,i<7,i=i+1 : write
    sempar 1,1,1 # For fast viewing
    write "Select a reference image"
    write "then press <ESC>"
    Grectg SE-ref,128,128,256,256,-1,0
    display SE-ref
    semonl SE-ref,0,-ON
    sempar 5,1,1 # Use frame integration to keep pic. square
    semscan SE-ref,0,-ON
    sempar 1,1,50 # Slow scan to eliminate noise etc.
    display CC-ref
    write
    write "Press <ESC> when OK"
    semonl CC-ref,1,-ON # 1 is EBIC
    semscan CC-ref,1,-ON
    for i=1,i<7,i=i+1 : write
endmacro
```

```
macro Flip (SE-ref=27,CC-ref=28,aux=26)
  write "Mirroring about a horizontal line!"
  display aux
  rotate SE-ref,aux,255,255,0,1.0,-1.0,0,0,-OFF
  copy aux,SE-ref
  rotate CC-ref,aux,255,255,0,1.0,-1.0,0,0,-OFF
  copy aux,CC-ref
  write "Finished"
endmacro
```

```
macro Compare (input=1,output=2,SE-ref=27,CC-ref=28)
# Macro to register two SE images by manual alignment
# and then acquire an EBIC image with 50 integrations
  for i=1,i<7,i=i+1 :write
    sempar 1,1,1,0,0,0
    copy SE-ref,input
    display input
    write "Align images with stage, ... press <ESC>"
    sempar 1,1,1
    semwindow input,-ON,128,128,256,256,-OFF,-OFF
    semonl input,0,-ON
    write "Performing scan"
    sempar 1,1,50,0,0,0
    semlut input,0,-ON,0,"lut-file.lin"
    clovl input
    semscan input,1,-ON # CH1 = CC channel
    subimage input,CC-ref,output
    write "Finished"
endmacro
```

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