

RRAM, Device, Model and Memory

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Abstract— The memristor is an innovative passive electrical device that has gained popularity in recent years as a potential candidate for next-generation non-volatile memory (NVM) and analog computing. This popularity stems from the memristor's ability to store information in a manner that is inaccessible to external power sources. It is possible to electrically modify the resistance state, and this change will be retained even after the external bias has been removed. This is a distinctive electrical characteristic of the device. In this paper, we present a comprehensive presentation and illustration about SkyWater memristor device and model. A read/write operation for a standalone memristor (1R), and a 1 transistor 1 memristor (1T1R) were conducted. The RRAM successfully can be written and read 1-bit information by dividing the resistance of the memristor (memristance) into two states of $R_{ON}=10.07\text{ K}\Omega$ as a bit 1 and $R_{OFF}=3.38\text{ M}\Omega$ as a bit 0.

Keywords— Non-volatile memory, memristor, RRAM, 1R, 1T1R, SkyWater.

I. INTRODUCTION

A non-linear device known as a memristor combines the memory and resistor functions into a single package. In 1971, Chua made the initial conceptual proposal for memristors, also referred to as resistive memory devices. The resistance of the memristor can be adjusted by the voltages applied on it, the pulse width, and/or number of pulses applied [1]. A memristor memory uses the resistance of a memristor to represent logic 0 or logic 1, depending on the state of the memory. The status of the memristor memory can therefore be maintained even after the power has been turned off. As a result, the memristor memory is an example of a potential non-volatile memory of the future. Memristors and memristor crossbar arrays have found widespread use in a variety of applications, including logic circuits, neuromorphic computing, machine learning, and image processing[2, 3]. This is primarily attributable to the memristors' compact structure and their promising compatibility with conventional CMOS manufacturing. Using the memristor as memory is one of the most important applications of this material and can become an efficient future memory device and has great potential to be integrated into the CPU to optimize latency.

The crossbar structure is the simplest approach for creating a memristor memory array. In this construction, only a single memristor (1R) is connected to both the bitline (BL), and the wordline (WL). Memory arrays made on 1R memristors are capable of reaching the highest possible density and low power consumption. Nevertheless, it suffers from the issue of sneak path. It's possible that the sneak path current will cause the write operation on the selected cell to fail, as well as an unwanted write operation on a cell that wasn't even selected and a failed read operation. This sneak current has the potential to significantly distort the precision of the cross-point analog resistance measurement. The sneak path impact was

reduced because of the implementation of a number of different biasing strategies[4, 5]. However, these solutions are unable to eradicate the sneak path current, which results in an intolerably high power consumption when the array size is increased. The transistor is yet another device that can be used as a selector; more specifically, each node comprises of an access transistor as well as a memristor (1T1R). A memristor memory that uses 1T1R cells has the ability to eliminate of sneak-path current, which enables the usage of bipolar memristor. RRAM arrays with 1T1R cell configuration remain the most prevalent option. The 1T1R crossbar design is highly comparable to that of DRAM.

A metal-oxide based bipolar resistive random access memory (also known as RRAM) is an intriguing possibility for the development of non-volatile memory technology in the future. In order to meet the growing demand for high-level simulation of developing memories, a number of analytical models that describe resistive switching behaviour have been developed. On the other hand, these models either do not take into account the stochastic nature of the filament switching process or they were not effectively implemented for circuit simulation[6].

In this paper, we present and illustrate the RRAM device that was developed and modeled by SkyWater corporation. The most important contributions made in this paper are as follows: A comprehensive presentation and illustration about SkyWater memristor device and model. Moreover, we provided a method for 1T1R RRAM programming (FORM, SET, and RESET) that reduces the amount of disruption caused in surrounding cells (on the same 1T1R structure). In addition, examples of writing and reading operations of 1R and 1T1R RRAM is illustrated here as well, with each RRAM cell having the capacity to store one bit. The following is the structure of the paper: In Section II, the device model and Verilog-A that was used and utilised in this work is described. In Section III, memory writing and reading operation and results are described. The last part of the paper is Section VII, which wraps everything up.

II. MEMRISTOR MODEL AND CHARACTERIZATION

A. Device Model

A resistive random access memory device is typically made up of a metal-oxide switching layer (such as HfO_x , TaO_x , TiO_x , or AlO_x by atomic layer deposition), which is then sandwiched by top and bottom metal electrodes to form a two-terminal metal-insulator-metal (MIM) structure.

In this model[7], the complex process of ion and vacancy migration was reduced to the formation of a single dominating filament, yet the crucial switching mechanics were maintained (see Fig. 1[6]). Device resistance is primarily determined by the size of the tunnelling gap (g), which is the distance between the tip of the filament and the opposing electrode. Modelling the switching dynamics of

RRAM utilising a series of differential and constitutive equations.

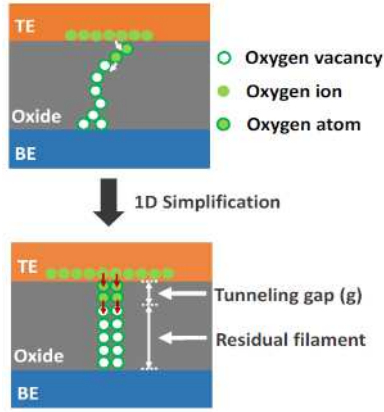


Fig. 1 Simplified conceptual structure for filament growth.

The current conduction depends exponentially on the distance of the tunnelling gap. This distance is calculated by taking into account the electric field, temperature-enhanced oxygen ion migration, and the local temperature due to Joule heating while estimating the expansion of the gap.

B. FORMING, SET, RESET Operation

There are three different modes of operation, which are as follows[7]:

- Formation, which is the stage during which the first oxygen filament is produced. RRAM starts out as an insulator because it's built out of HfO_2 , which has a high resistivity when it's first created. We are able to create a channel for oxygen vacancies between the top and bottom electrodes of the gadget by delivering a positive voltage to it. The application of an electric field between the electrodes will drive the production and movement of oxygen vacancies within the insulator oxide, which will ultimately lead to the generation of conductive filaments within the oxide. This is referred to as FORMING. A new (unformed) RRAM cell begins at an extremely high resistance (ultra-low conductance state), but with the production of the first filament by way of oxygen vacancies, the cell eventually reaches a low resistance state.
- Writing, which involves changing the conductive properties of a filament by the application of an electric field. Writing can be further broken down into two distinct modes. SET – in which resistance is decreased by applying a positive electric field across the device bringing it from HRS to LRS. RESET – in which resistance is increased by applying a negative electric field across the device bringing it from a LRS to a HRS. Often the HRS is used to store a logical '0' as RESET and the LRS stores a logical '1' as SET. RRAM setup usually follows this sequence: FORM - > RESET -> SET.
- Reading, which is the process of sensing the resistance or conductivity of the filament and converting that data into a digital value. During this step, the value can be read. Reading an RRAM device typically involves applying a low voltage (for example, 0.1-0.2 V), and then utilising current

sensing to figure out what state the device is in.

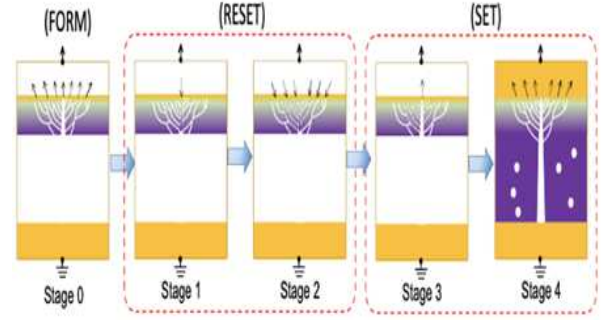


Fig. 2. Stages of SkyWater RRAM programming.

Fig. 2[7] provides the five stages of the RRAM device programming.

- FORMING
 - Stage 0: HfO_2 is responsible for the formation of a large filament that has a wide radius. In addition, smaller filaments may be seen extending all the way up to the top electrode from the end of the primary filament. Following formation, the resistance is denoted by Low state resistance (LRS).
- RESET
 - Stage 1, the main filament recedes cause an abrupt reduction in conductance.
 - Stage 2, the tiny filaments gradually disappear, which results in a steady decrease in conductance high state resistance (HRS).
- SET
 - Stage 3, At this stage, the main filament is reconnected, which causes a jump in conductance.
 - Stage 4, the tiny filaments begin to reconnect, and the conductance begins to gradually increase (LRS).

C. Verilog-A Model

The SkyWater model is a dynamic RRAM miniaturised model that makes use of the circuit-compatible Verilog-A language. The RRAM compact model has been updated to take into consideration fluctuations and differences in filament growth[6]. Both DC switching data and pulse data are utilised in the model's verification process. Pulse data fitting has been discovered to be more effective, to be more realistic of the practical usage scenario, and to follow the physics of the filament growth in a more precise manner[6]. The complete Verilog-A of SkyWater memristor can be found in [8].

D. Device Electrical Design

SkyWater offers the RRAM device as a Pcell in their Process Design Kit (PDK). RRAM can be directly fabricated in the back-end-of-line (BEOL) process without impacting the front-end-of-line (FEOL) portion of a silicon chip. This is important for analog designs manufactured in larger process nodes which often require Low-density, high-endurance embedded NVM. Fig. 3[9] shows that RRAM is located between metal 1 and metal 2 in SkyWater 130nm process. Vias to metal layer is to create link between memristor and other cells (transistors, capacitors, resistors, etc.) in the FEOL.

Schematic symbol and layout of the SkyWater memristor are illustrated in Fig.4[9]. Layers are annotated corresponding to its MIM physical structure. After creating the symbol in a simulator tool, the memristive device is ready to be applied into circuit visually, whose parameters can be changed to represent different initial and resistance values.

RRAM between met1/met2

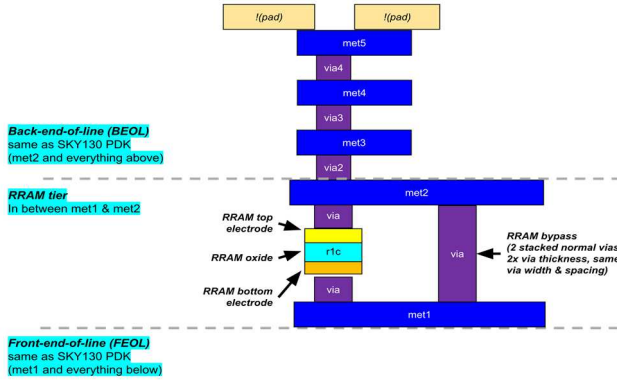


Fig. 3. RRAM stack diagram[9].

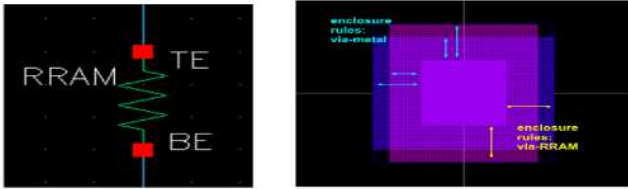


Fig. 4 RRAM schematic symbol (left) and cell layout (right)

III. MEMORY WRITING AND READING OPERATION

A Verilog-A model with altered switching parameters is utilised to simulate the memristor's switching behaviour. CAD tools such as Cadence Virtuoso can be used to develop with memristors in CMOS technology using this paradigm.

By separating the resistance of the memristor, also known as the memristance, into two distinct states, the RRAM is able to successfully write and read one bits of information. The SkyWater RRAM device can vary (LSR) to (HSR). The device is characterized by two resistance values $R_{ON}=10.07K\Omega$ (LRS) and $R_{OFF}=3.38M\Omega$ (HRS) with a ratio of $OFF/ON=335$. The initial resistance of the Memristor can be changed by adjusting the thickness of the conductive filament in Verilog-A.

A. Standalone memristor

The cell has two terminals connected to the WL, and BL of the memory array as shown in Fig. 5. The memristor cell operations depend on the duration of access time, number of pulses applied, and the amplitude applied on WL and BL. Fig. 6 shows a 1R memristor cell writing and reading simulation. We conduct the reading operation while we are writing.

Alternatively, as depict in Fig. 7, we can apply different signals other than the pulse signal such as reverse ramp signal to program the RRAM. It removes the frequency limitation when setting the pulse signal. Note that the resistance changes of the RRAM happen whenever there is

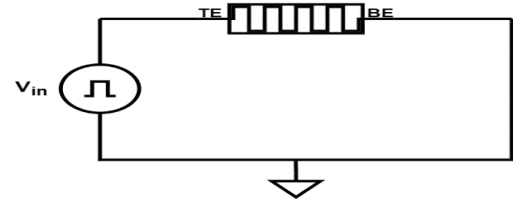


Fig. 5. 1R testbench schematic.

abrupt change on the signal applied. Therefore, with an appropriate rise and fall time of the reverse ramp signal, The RRAM can be programmed. Fig. 7 shows the signal applied with resistance change from HRS to LRS.

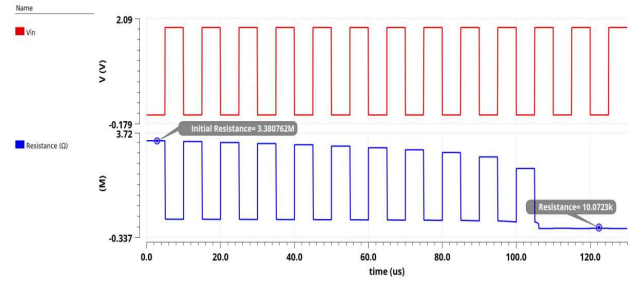


Fig. 6. 1R pulse signal simulation waveform.

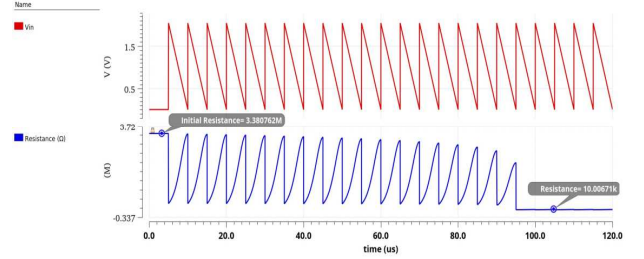


Fig. 7. Reverse ramp signal simulation waveform.

B. 1T1R

Table 1[9] provides a summary of the standard SET/RESET pulses used with the SkyWater RRAM characteristics. These pulses are utilized with binary (1-bit/cell) RRAM. It is important to keep in mind that these are dependent on the initial forming conditions that were utilized (as discussed above). For the sake of completeness, we will also go over those conditions. The following steps are to be taken if a range is specified: The BL voltage should be fixed first (for FORM/SET, the SL voltage should be used for RESET), and then the WL pulse amplitude should be increased by the provided step size until the cell is successfully formed, set, or reset, to verify the effect of the gate voltage on the source current, and therefore on the memristor resistance. If the cell is failed, then increase the BL voltage by the step size, and continue doing this until you reach the maximum voltage.

Table 1 1T1R FORM/SET/RESET pulses values

1T1R	WL (V)	BL (V)	SL (V)
Form	1.4-3.0 (0.1 step)	2.6-3.1 (0.1 step)	0
Reset	2.5	0	2.6
Set	1.7	2.4	0

As illustrated in Fig. 8, If a Write-0 operation is carried out, V_{Write} will be applied to BL, and SL will be connected to ground. This will cause the resistance of the memristor to

transition to HRS. If a Write-1 operation is carried out, V_{Write} will be applied to SL, and BL will be connected to ground. This will cause the resistance of the memristor to change to an LRS. To read, a small voltage known as V_{Read} is applied to BL while SL is connected to ground in order to read the data from a selected cell. This is done in such a way that the read current is lower than the threshold current necessary to change the state of the memristor[10].

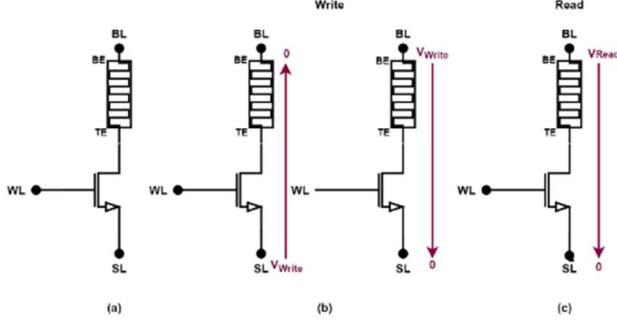


Fig. 8. (a) 1T1R cell. (b) Bias conditions of write operations. (c) Bias conditions of read operation.

Fig. 9 shows the simulation for the 1T1R ReRAM memory cell, in which a read operation is carried out with the write operation simultaneously. The initial resistance is 3.38M, the resistance gets decreasing as more pulses applied.

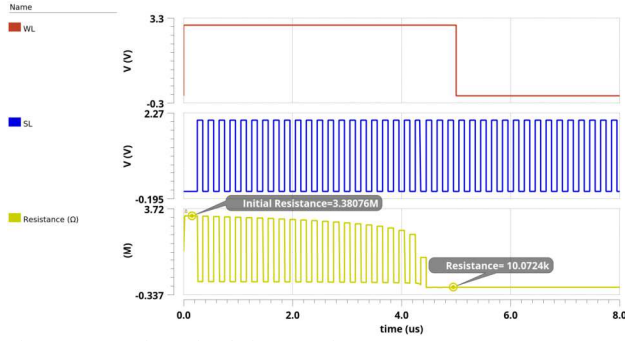


Fig. 9. 1T1R write 1 simulation waveform.

We conducted both of write 1 and 0 in Fig.10. The initial resistance was R_{OFF} (3.38M Ω). When we moved from HRS to LRS to write 1, it was enough to apply a small voltage pulse at WL, because the resistance is big, and a small current that flow through the memristor would be enough to excite the memristor voltage to switch. However,

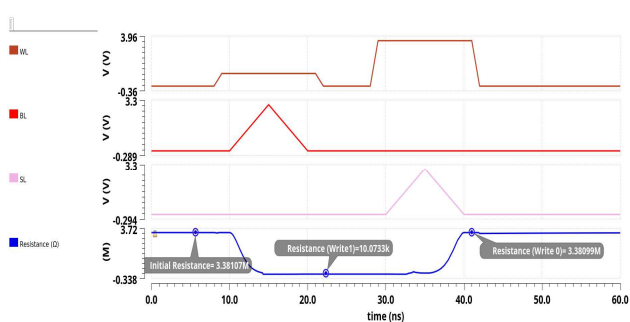


Fig. 10. 1T1R write 1 and 0 simulation waveform

when the resistance is R_{ON} (10.07K Ω) and want to move from LRS to HRS to write 0, we needed to apply a larger

voltage pulse at WL, because the resistance is small, to have a larger current flowing through the memristor that is enough to excite the memristor to switch. As a part of NxM crossbar array structure, the feasibility of 1T1R single cell based on the SkyWater- Memristor is successfully proved.

CONCLUSION

In this paper, a comprehensive study of SkyWater RRAM device and model has been presented. The model can be easily employed for circuit level simulation using the Verilog-A model. The Verilog-A model proved a compatibility applicability to various RRAM array topologies. A method for programming 1T1R RRAM (FORM, SET, and RESET) that causes less disruption to neighbouring cells has been discussed. Examples of writing and reading operations that can be performed on 1R and 1T1R RRAM have been shown as well, with the capacity of each RRAM cell to store one bit.

Challenges include the lack of the current SkyWater's Verilog-A model for power analysis, corner and mismatch analysis, or post-layout simulation, so the precision and stability of memristor switching can only be tested on-chip.

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